

# Compal Confidential

## KAV60 Schematics Document

Intel Diamondville Processor with Calistoga(945GSE) + DDRII + ICH7M

2009-02-22

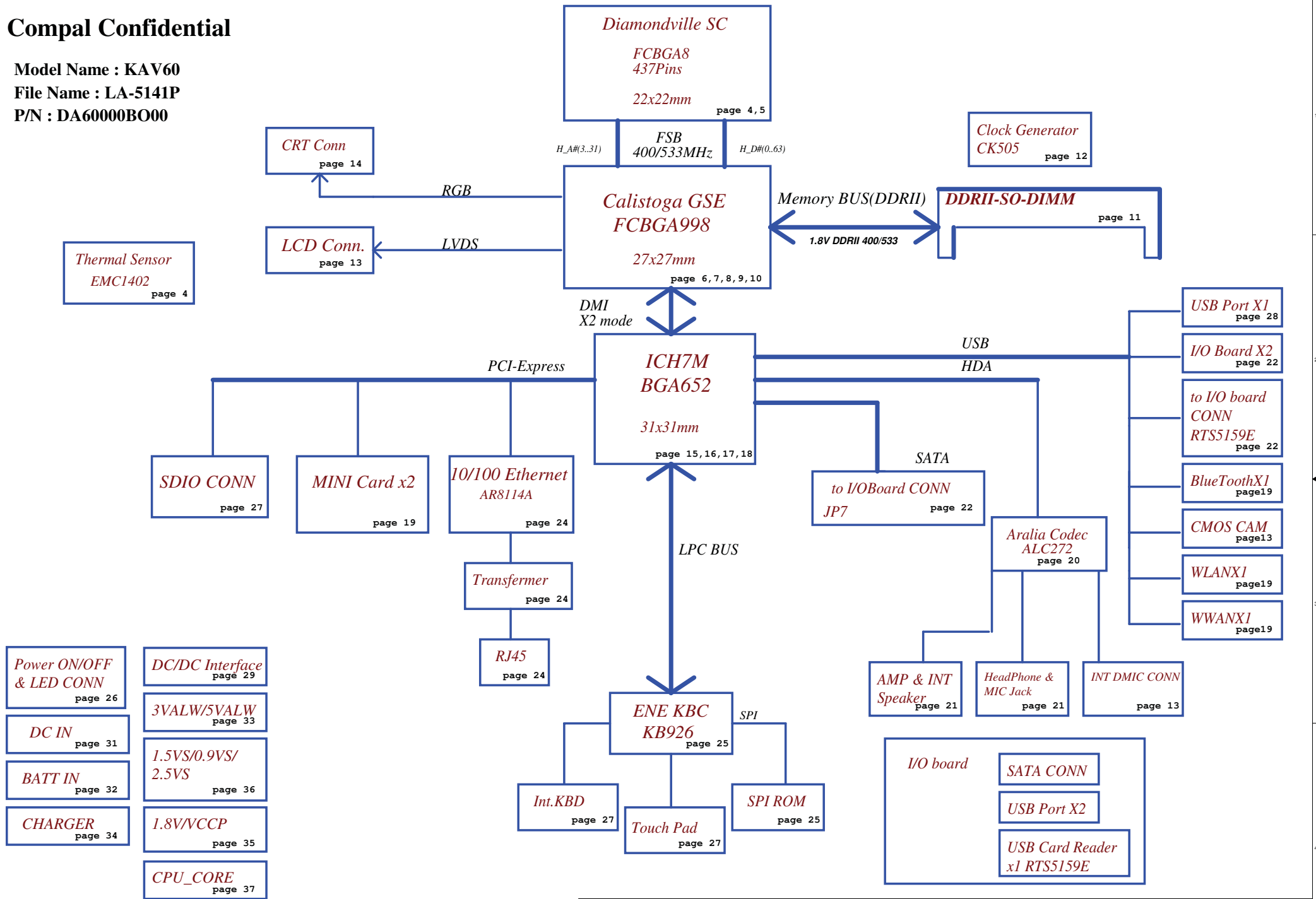
REV: 1.0

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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	Cover Page	
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Model Name : KAV60  
 File Name : LA-5141P  
 P/N : DA60000BO00



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- DC IN page 31
- BATT IN page 32
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- CPU\_CORE page 37
- DC/DC Interface page 29
- 3VALW/5VALW page 33
- 1.5VS/0.9VS/2.5VS page 36
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## Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+VCCP	VCCP switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE	SIGNAL	SIGNAL						
		SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	ClOCK
Full ON		HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	ON	OFF	OFF	OFF

## BOARD ID Table(Page 25)

ID	BRD ID	Ra	Rb	Vab
0	R01 (EVT)	NC	0	0V
1	R02 (DVT)	100K	8.2K	0.25V
2	R03 (PVT)	100K	18K	0.50V
3	R10A (MP)	100K	NC	3.3V

## External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
--------	---------	-----------	------

No PCI Device

## EC SM Bus1 address

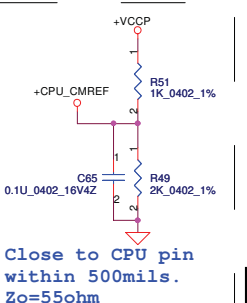
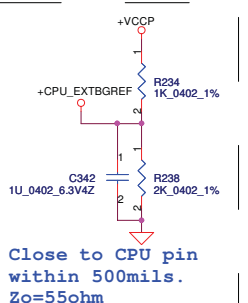
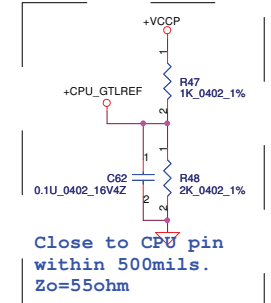
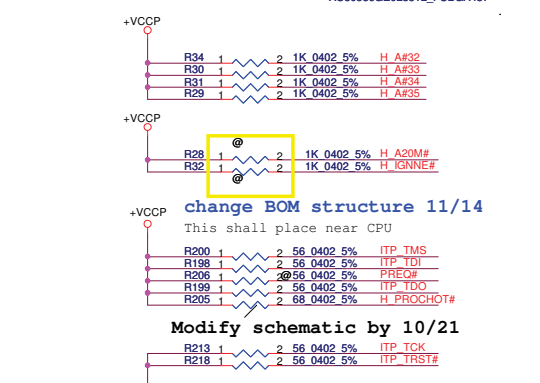
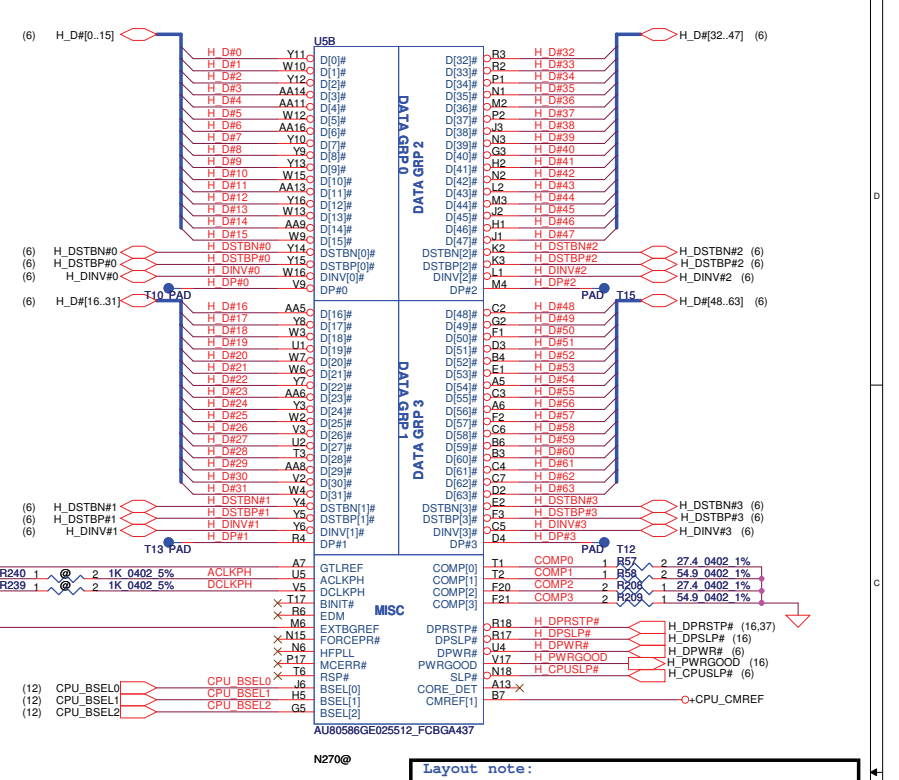
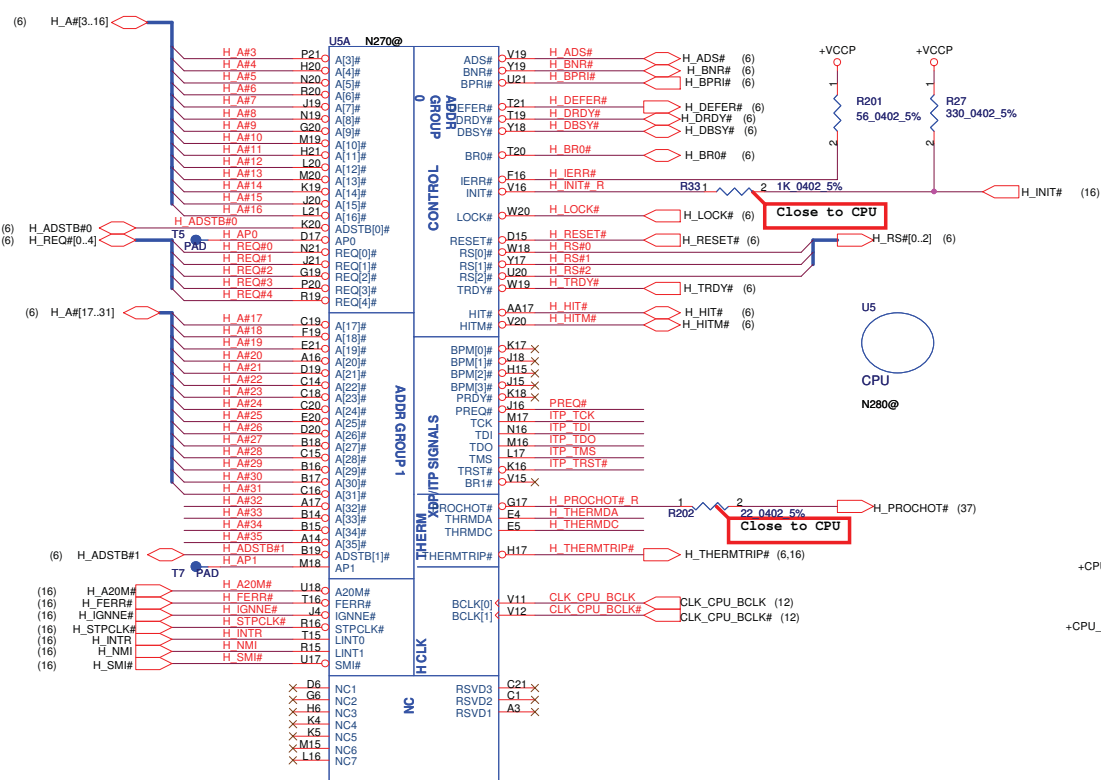
## EC SM Bus2 address

Device	Address	Device	Address
Smart Battery	0001 011X b	EMC1402	1001 100X b
EEPROM(24C16/02)	1010 000X b		

## ICH7M SM Bus address

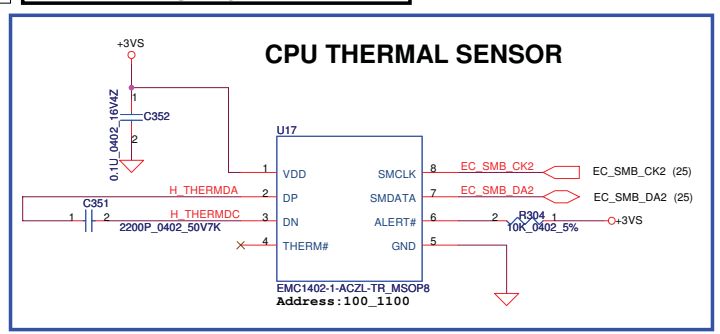
Device	Address
Clock Generator (SLG8SP556VTR)	1101 001Xb
DDR DIMMA	1010 000Xb

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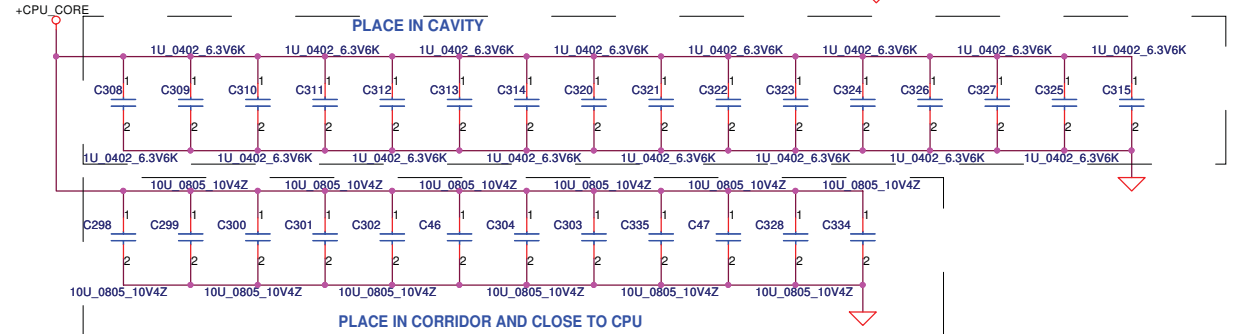
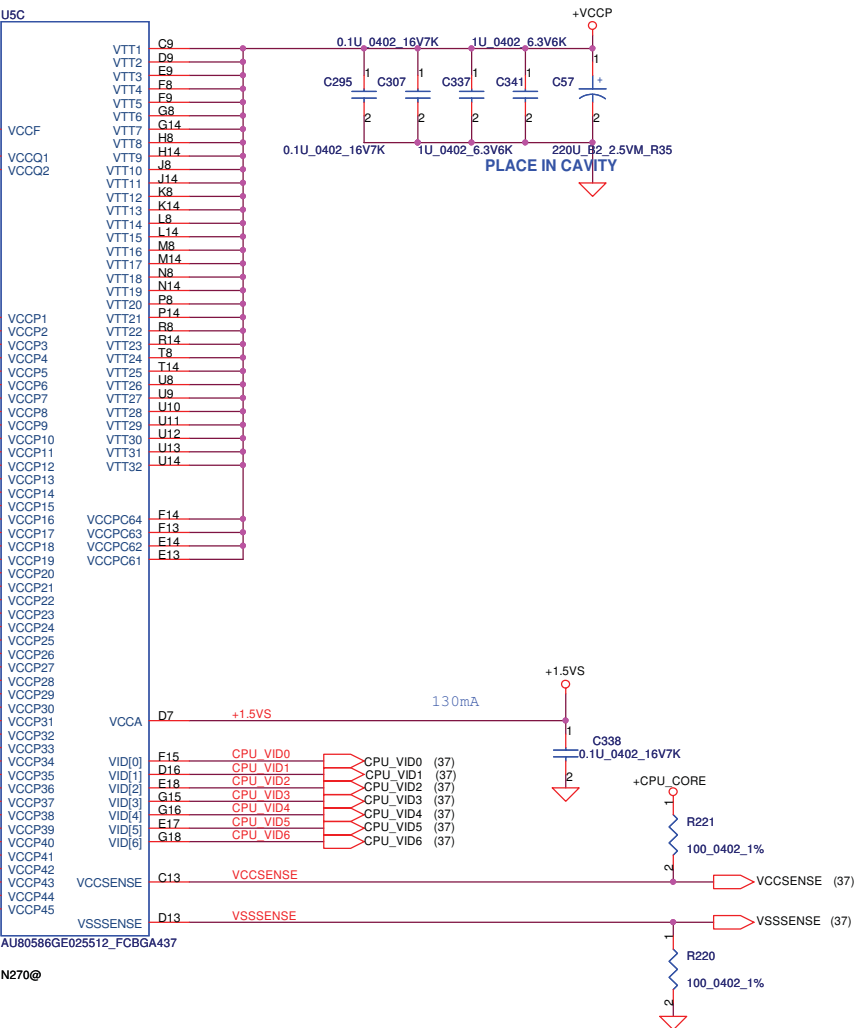
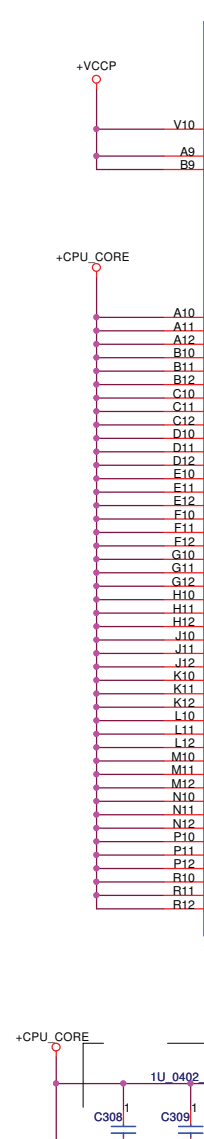
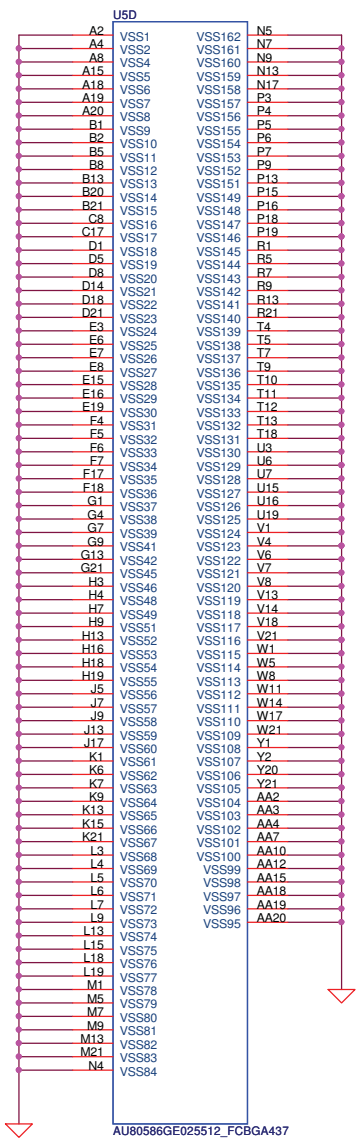


H\_THERMDA, H\_THERMDC routing together.  
Trace width / Spacing = 10 / 10 mil

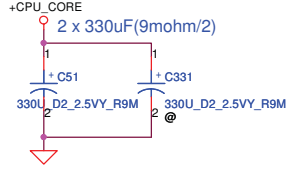
Layout note:  
COMP0,2 connect with Zo=27.4ohm +/-15%, make trace length shorter than 0.5"  
COMP1,3 connect with Zo=55ohm +/-15%, make trace length shorter than 0.5"



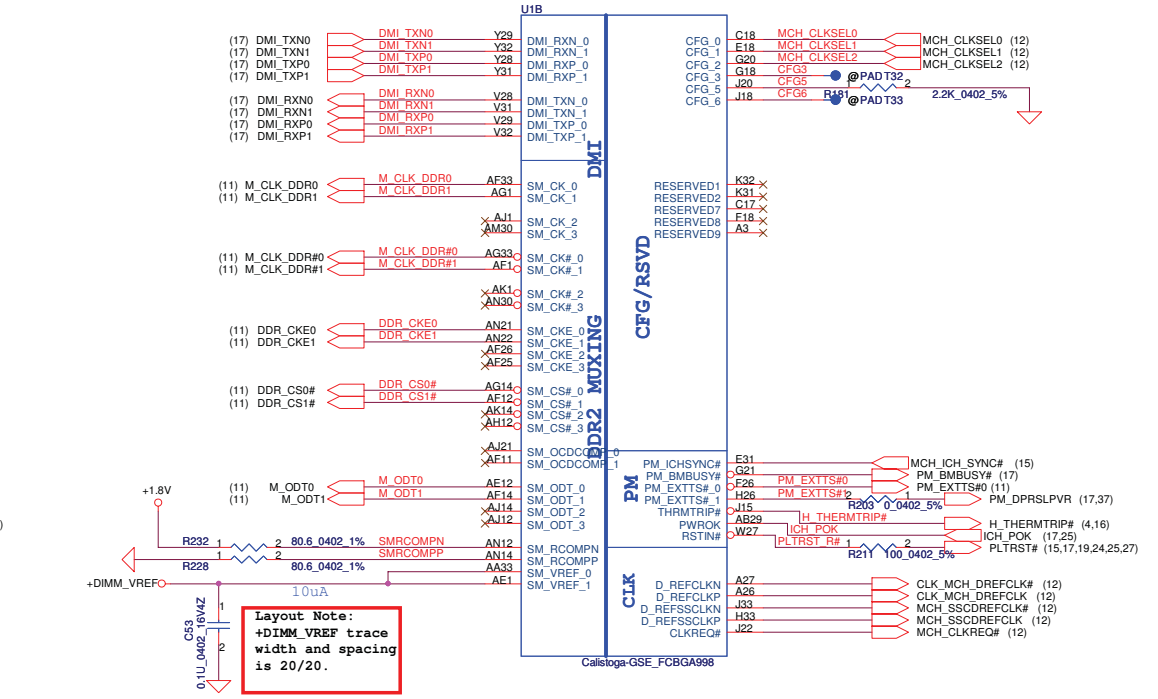
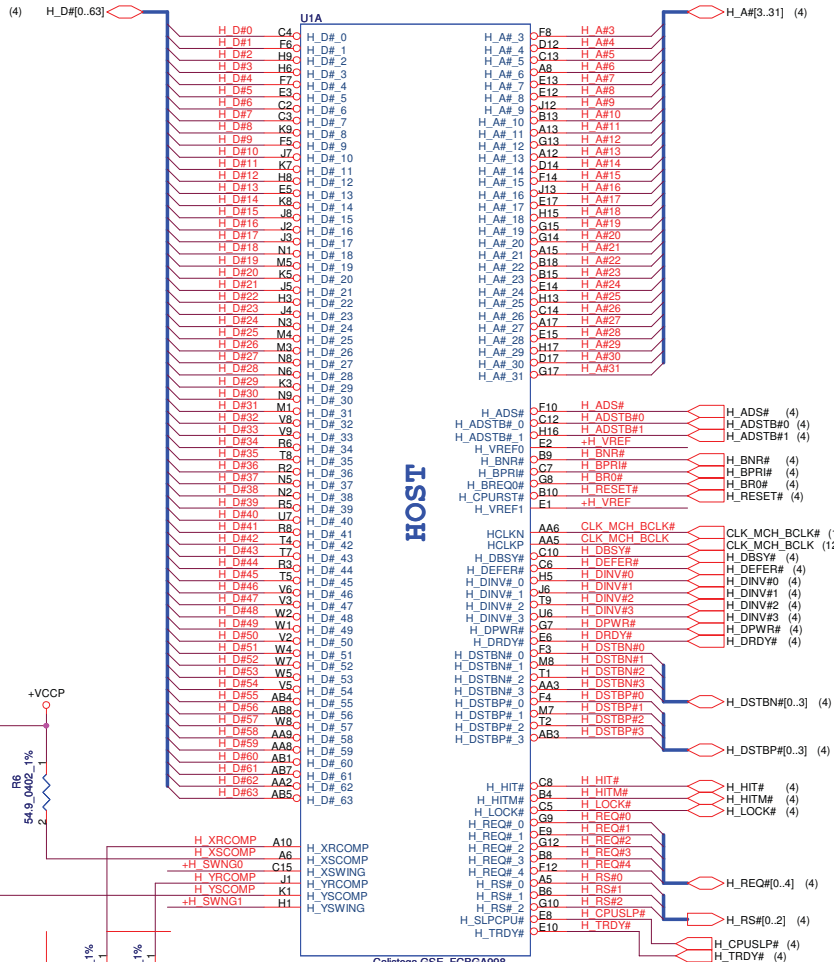
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Length match within 25 mils  
The trace space 7 mils,  
 $Z_0=27.4\text{ohm}$



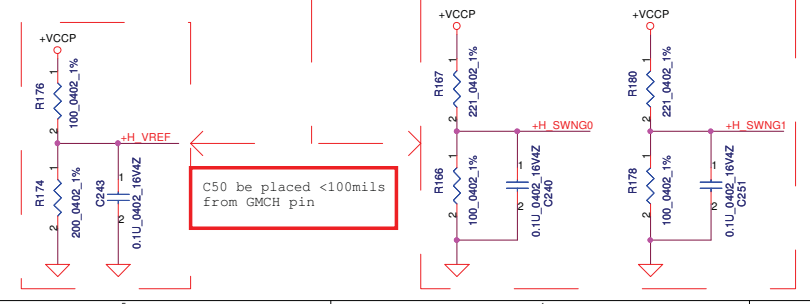
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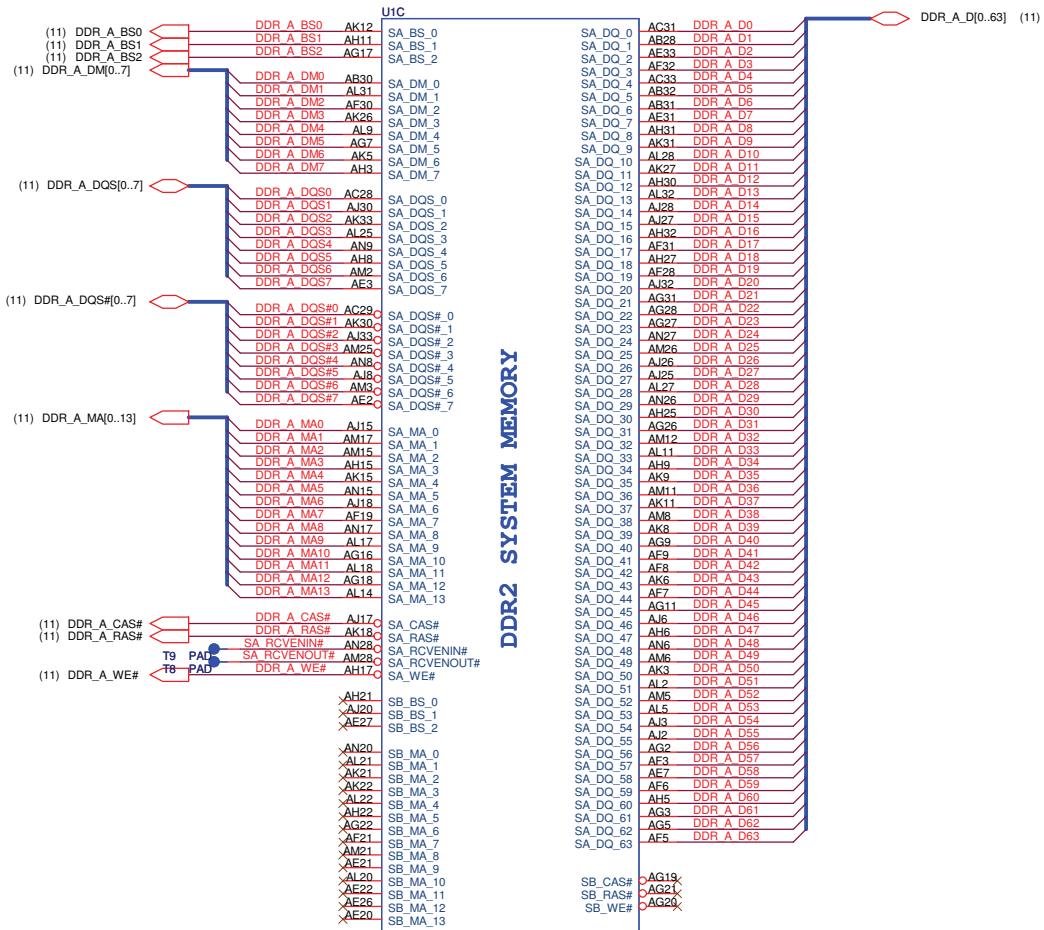
**Strap Pin Table**

CFG5	Low = DMI x 2 *
	High = DMI x 4

**Layout Note:**  
H\_XRCOMP / H\_YRCOMP / H\_VREF / H\_SWNG0 / H\_SWNG1 trace width and spacing is 10/20.

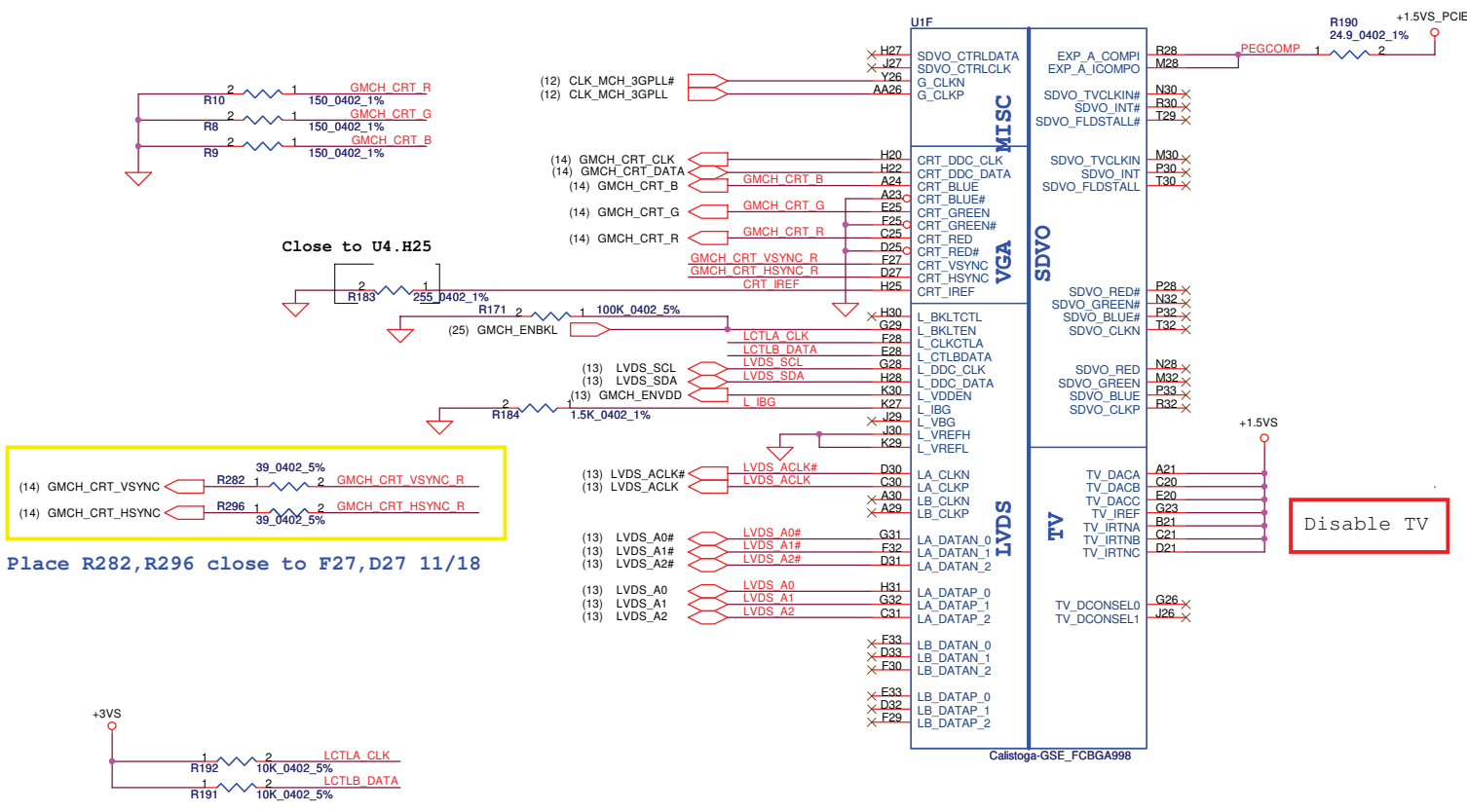


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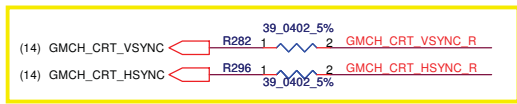


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Close to U4.H25

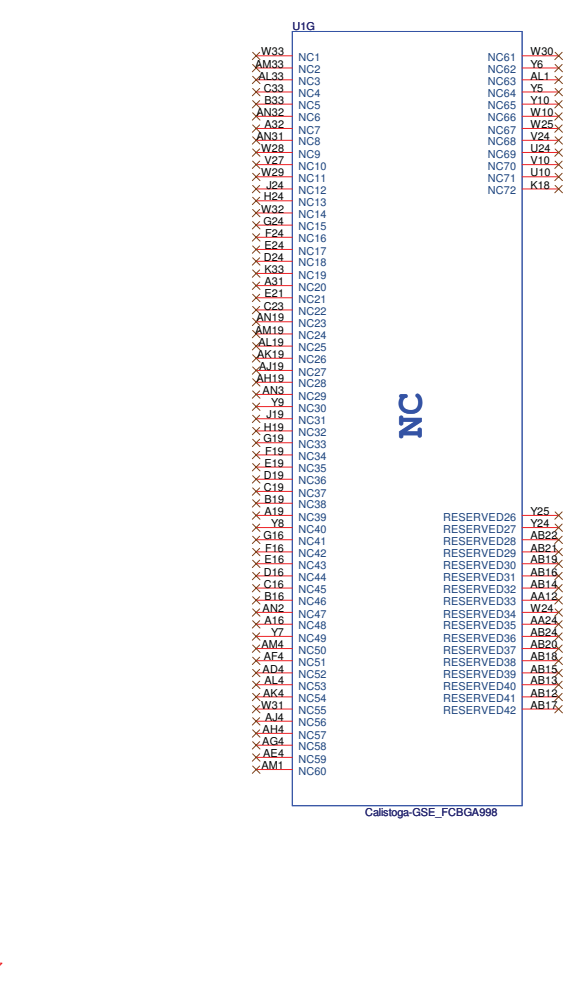
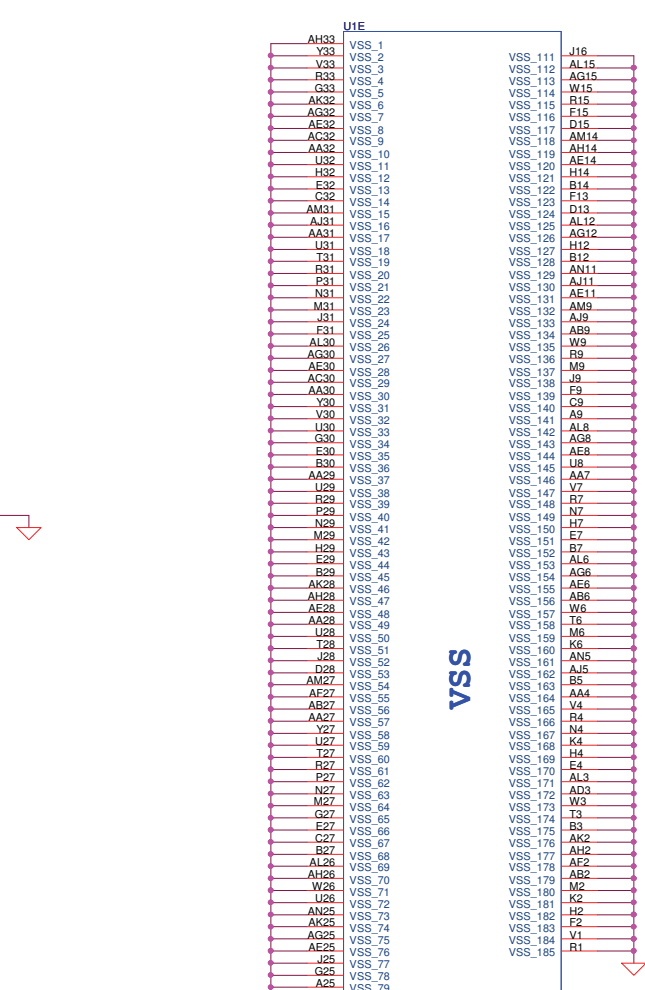
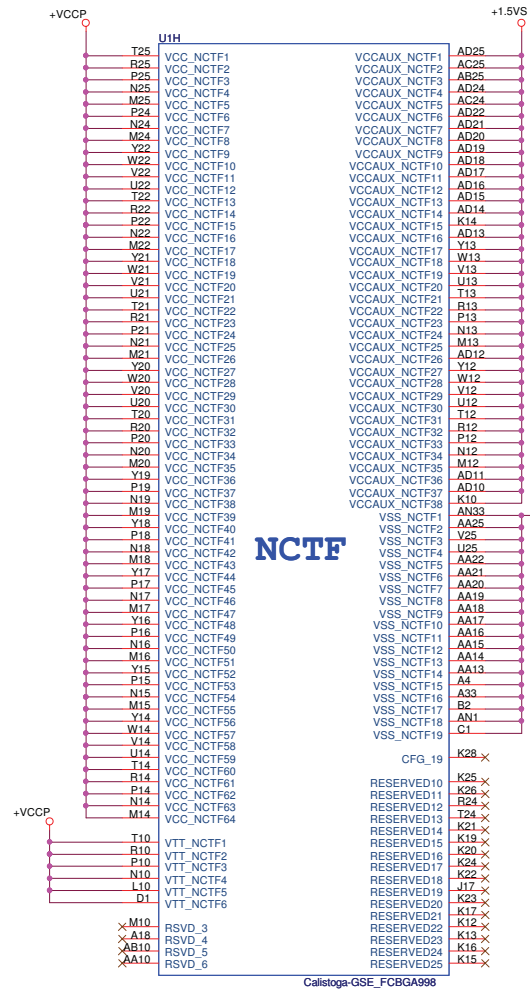


Place R282, R296 close to F27, D27 11/18

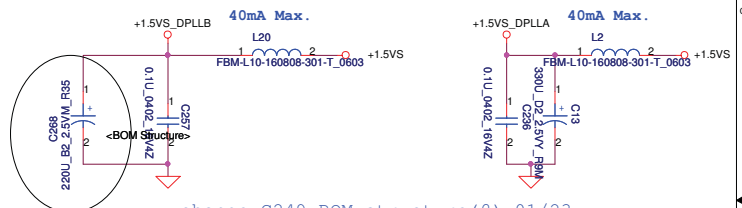
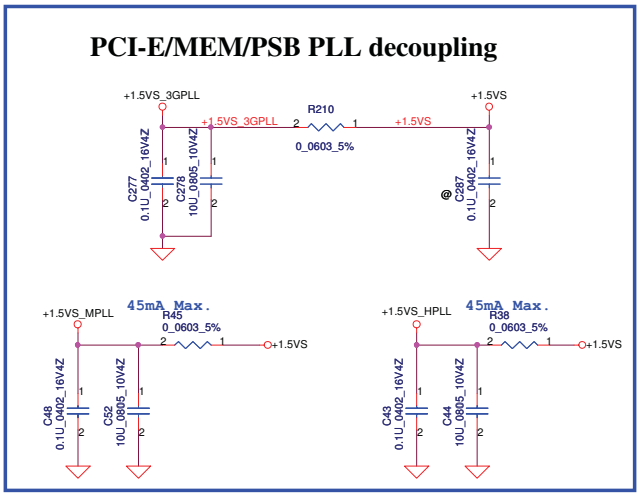
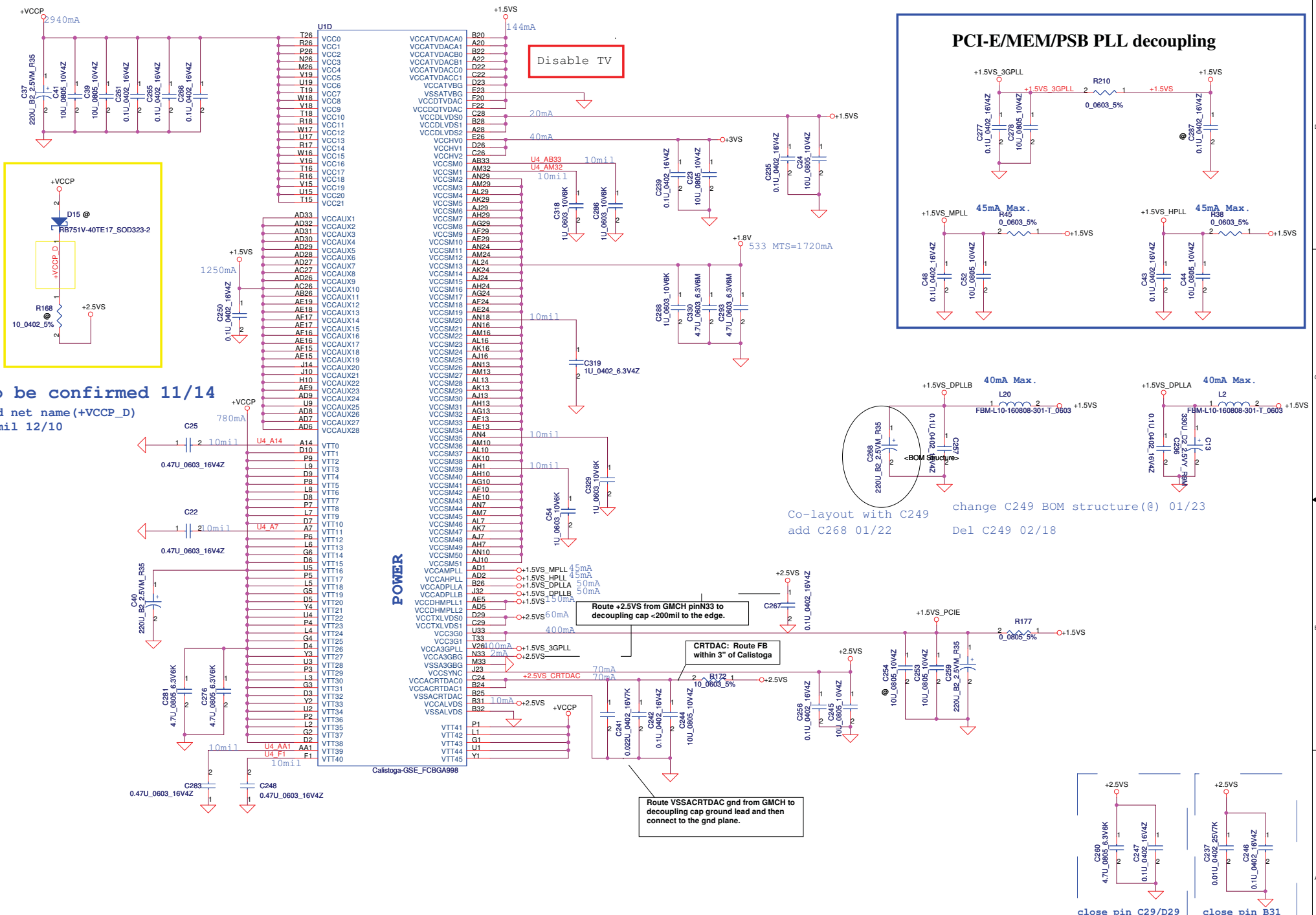
Disable TV

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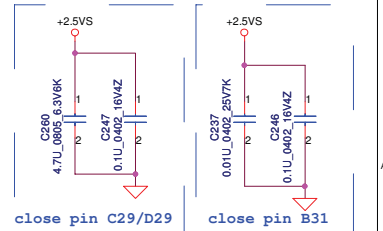




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Co-layout with C249 change C249 BOM structure(@) 01/23  
 add C268 01/22 Del C249 02/18



To be confirmed 11/14  
 add net name (+VCCP\_D)  
 20mil 12/10

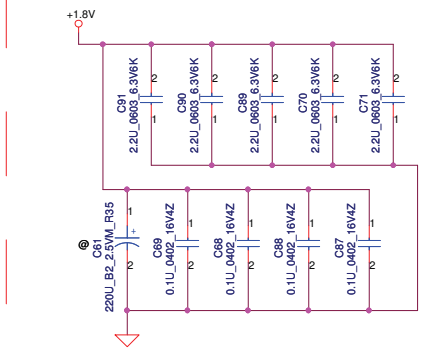
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Title			
Calistoga(5/5)-PWR/GND			
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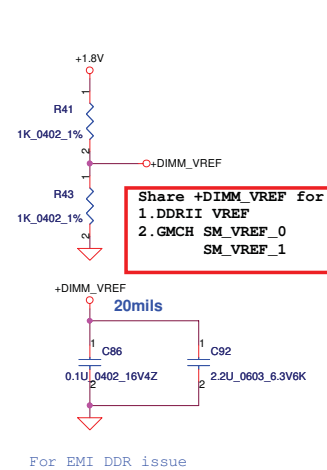
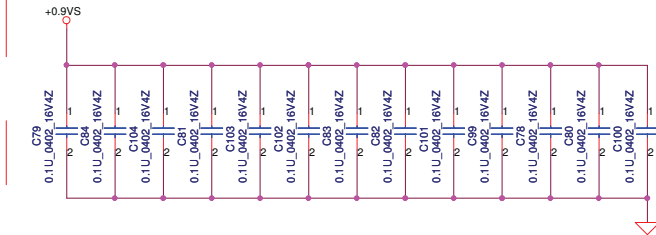
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- (7) DDR\_A\_DQS#[0..7]
- (7) DDR\_A\_D[0..63]
- (7) DDR\_A\_DM[0..7]
- (7) DDR\_A\_DOS#[0..7]
- (7) DDR\_A\_MA[0..13]

**Layout Note:**  
Place near JDIM1



**Layout Note:**  
Place one cap close to every 2 pullup resistors terminated to +0.9VS



For EMI DDR issue

del C94 C95 01/22

add JDIM1 pin 200 and pin 201 to GND 01/20

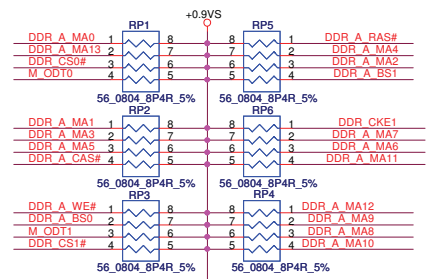
return the H5.2 footprint 11/24



change DIMMA from H5.2 to H4 11/17



**DIMMA**



**Layout Note:**  
Place these resistor closely DIMMA, all trace length < 750 mil

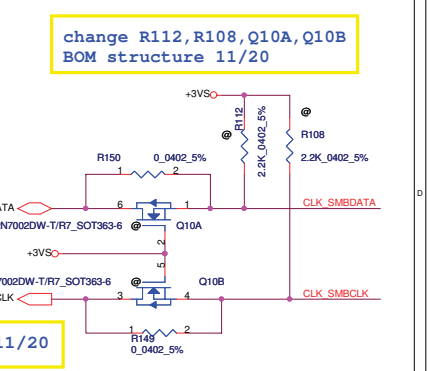
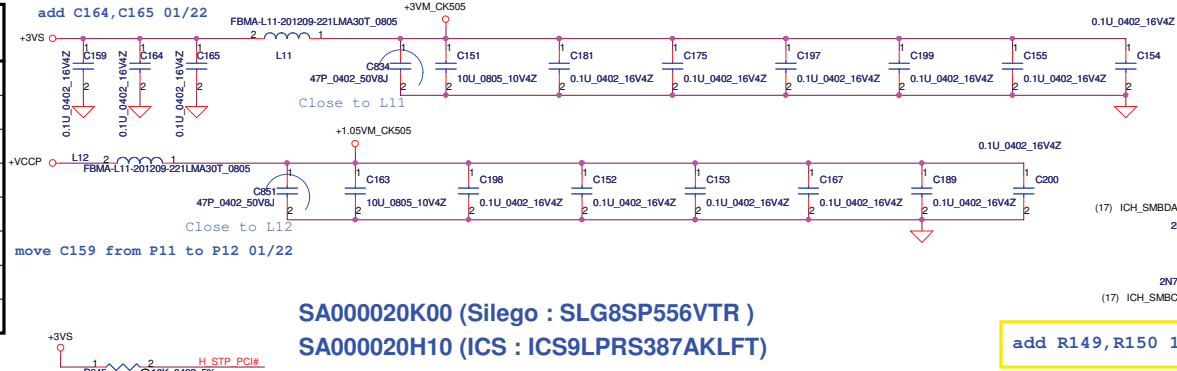
**Layout Note:**  
Place these resistor closely DIMMA, all trace length Max=1.3"

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Title		
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FSC	FSB	FSA	CPU	SRC	PCI	REF	DOT_96	USB
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz	MHz	MHz	MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1						
Reserved								



SA000020K00 (Silego : SLG8SP556VTR )  
 SA000020H10 (ICS : ICS9LPRS387AKLFT)

change R141, R140, R147, R81, R91  
 R82, R97, R95, R98 BOM structure 12/29  
 change R141, R140, R147, R81, R91  
 R82, R97, R95, R98 BOM structure 01/17

del R143 and CLK\_SD\_48M 11/21

Change R137 from 12 ohm  
 to 33 ohm 11/21

change R137 BOM structure 12/15  
 add R143 12/15

del R143 12/15

change C32 from 10pF to  
 15pF 02/06

change R137 from 33 to  
 39 ohm 02/06

change C32 C33 C42 C45  
 BOM structure 12/14

add C45 for keypart 12/14

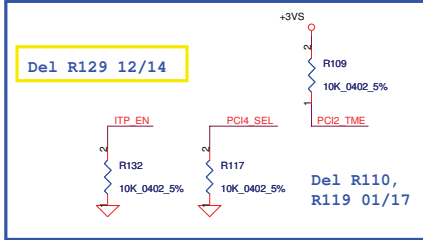
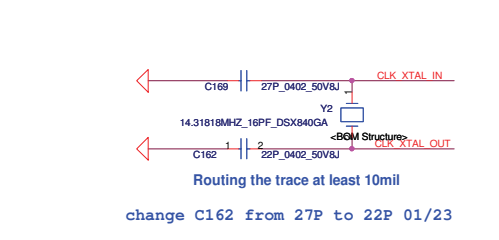
change C42, C45 from  
 22pF to 15pF 02/06

change R115, R121 from  
 39 ohm to 47 ohm 02/06

1 = Pin24/25 : SRC\_0 / SRC\_0#  
 Pin28/29 : 27M/27M\_SS

For PCI2\_TME:0=Overclocking of CPU and SRC allowed  
 (ICS only) 1=Overclocking of CPU and SRC NOT allowed

For ITP\_EN, 0 = SRC8/SRC8#; 1 = ITP/ITP#  
 For PCI4\_SEL, 0 = Pin24/25 : DOT96 / DOT96#  
 Pin28/29 : LCDCLK / LCDCLK#



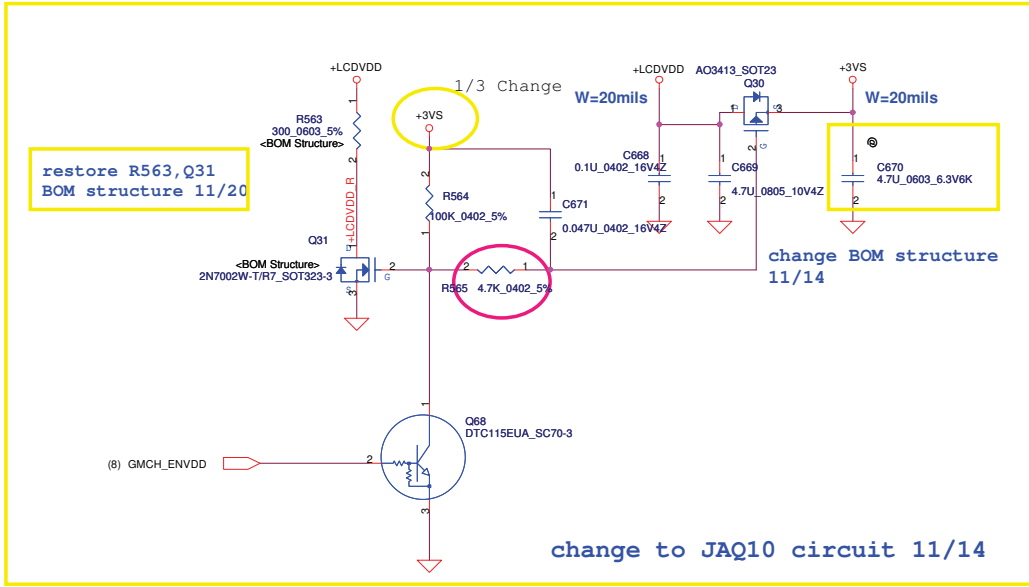
SRC PORT LIST

PORT	DEVICE
SRC0	MCH_DREFCLK
SRC2	SATA HDD
SRC3	MCH_3GPLL
SRC4	PCIE_CARDREADER
SRC6	PCIE_WLAN
SRC7	PCIE_WWAN
SRC8	
SRC9	PCIE_LAN
SRC10	PCIE_ICH
SRC11	

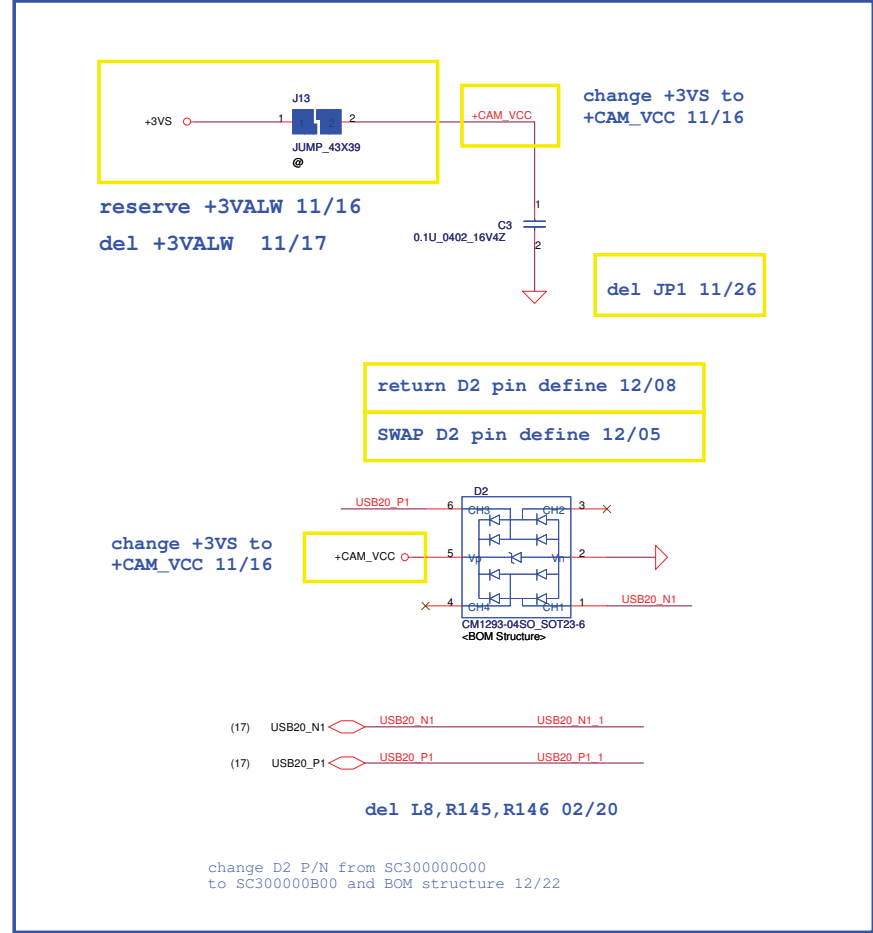
REQ PORT LIST

PORT	DEVICE
REQ_3#	MCH_3GPLL
REQ_4#	
REQ_6#	PCIE_WLAN
REQ_7#	PCIE_WWAN
REQ_9#	
REQ_10#	
REQ_11#	
REQ_A#	SATA

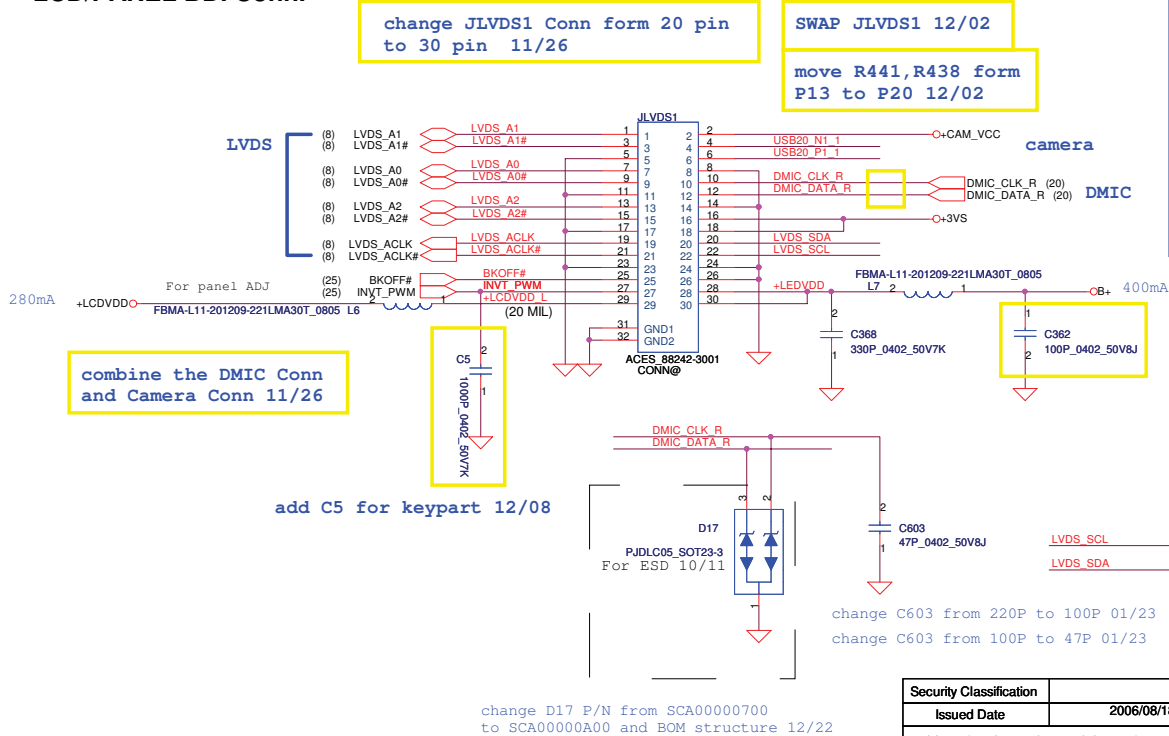
# LCD POWER CIRCUIT



# CMOS Camera CONN

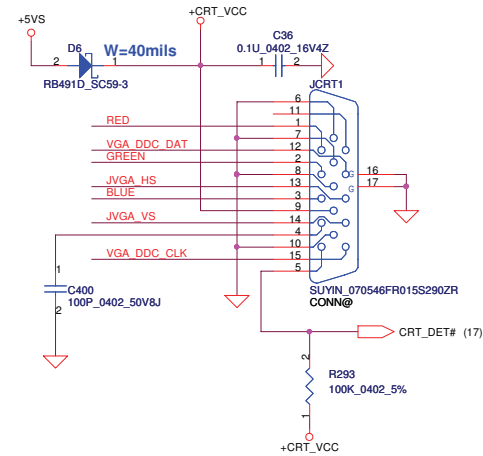
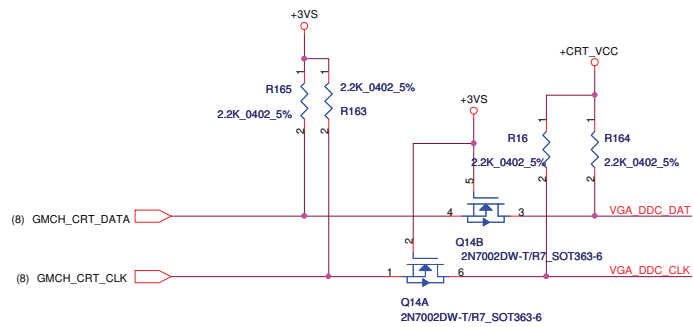
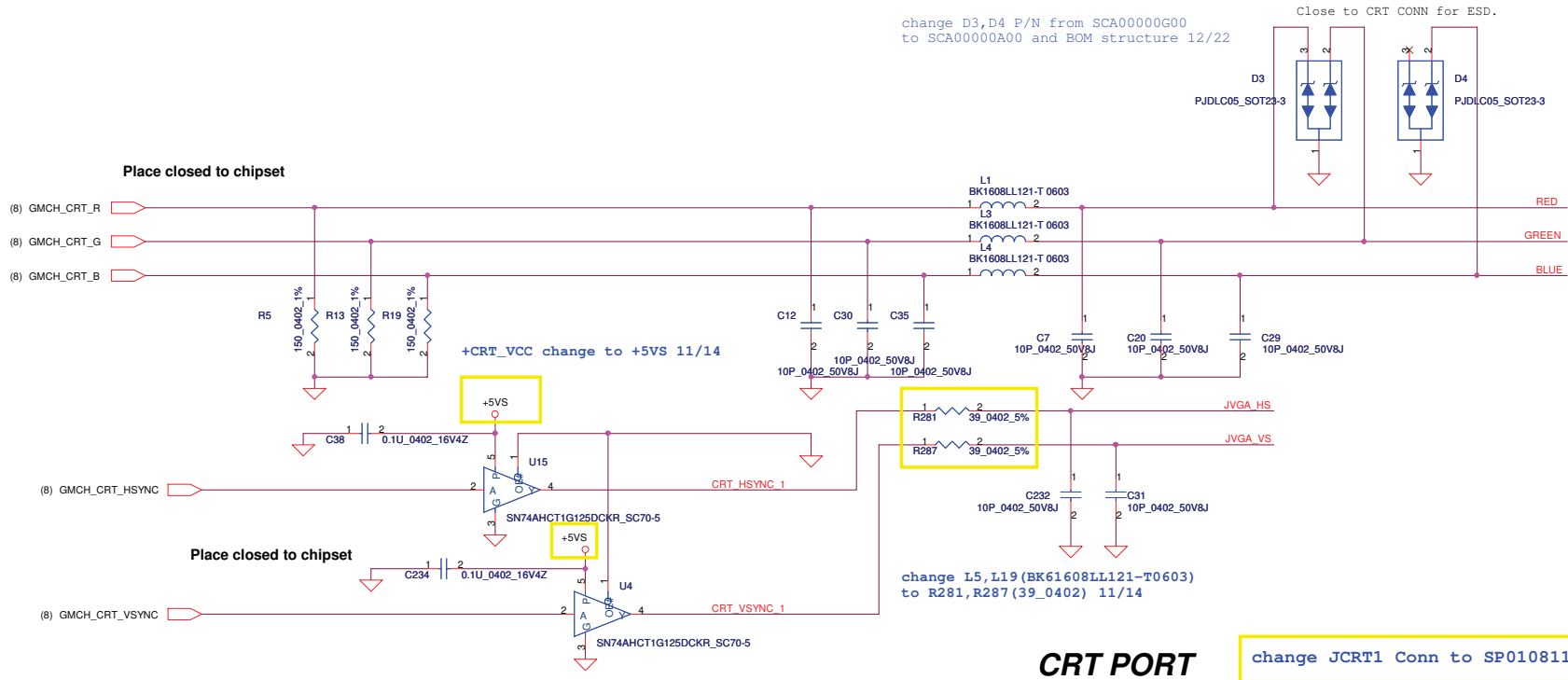


# LCD/PANEL BD. Conn.

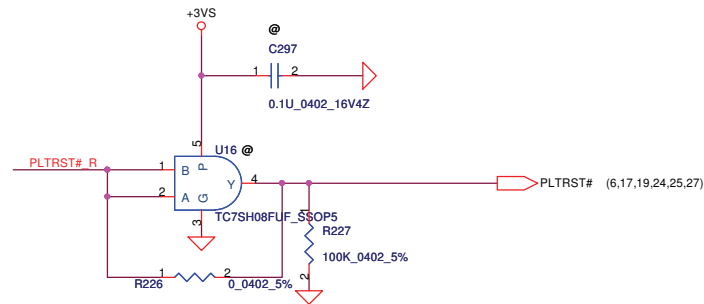
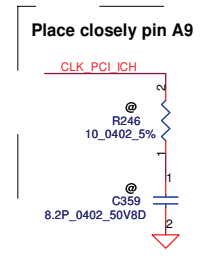
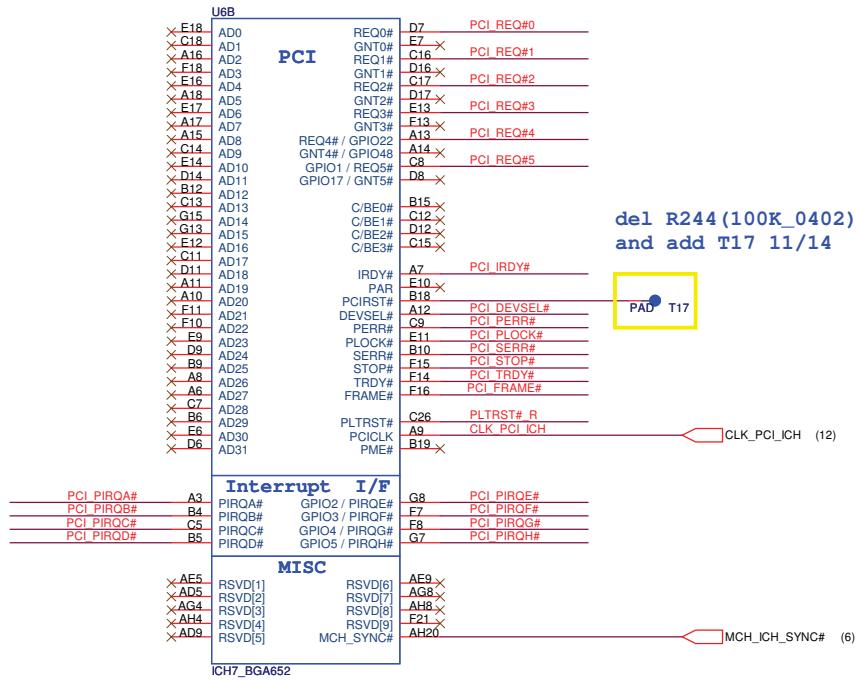
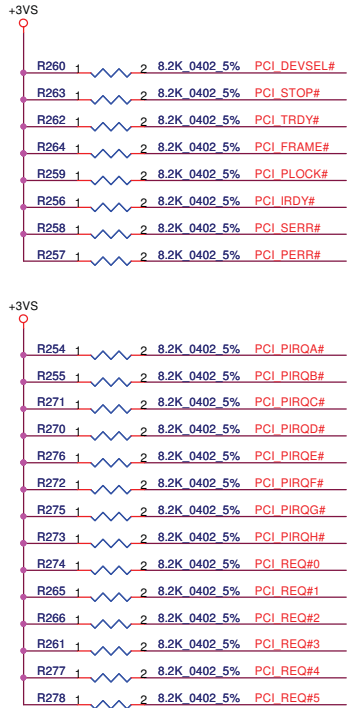


Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title		
				LVDS/Camera/DMIC conn		
				Size B	Document Number	Rev 0.2
				KAV60 LA-5141P		
				Date:	Sunday, February 22, 2009	Sheet 13 of 40

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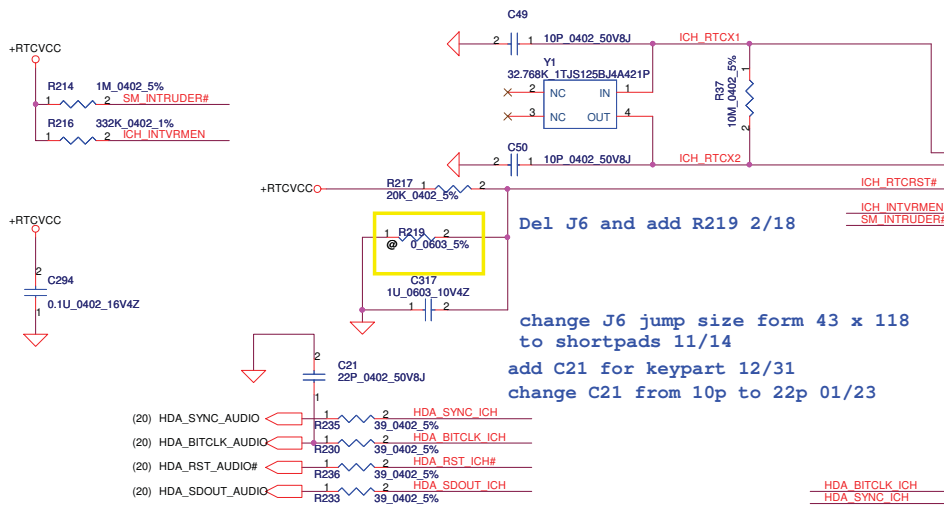


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				CRT PORT	
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				Date:	Revision
				Sunday, February 22, 2009	14 of 40



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Size	Document Number	Rev		0.2	
Date:	Sunday, February 22, 2009	Sheet	15	of 40	

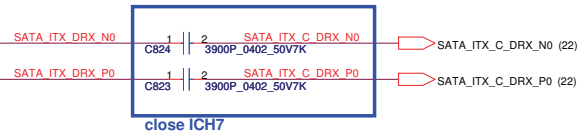
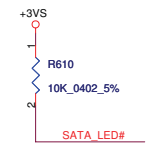
change C49 C50 from 18pf to 10pf 01/23



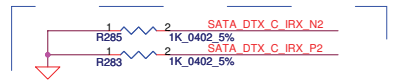
Del J6 and add R219 2/18

change J6 jump size form 43 x 118 to shortpads 11/14  
add C21 for keypart 12/31  
change C21 from 10p to 22p 01/23

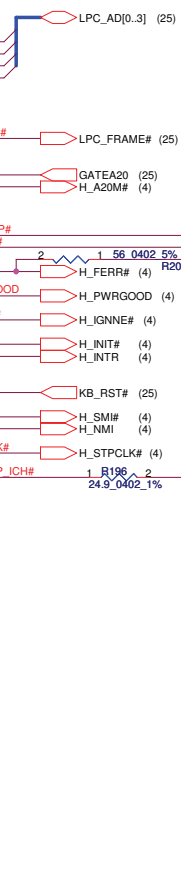
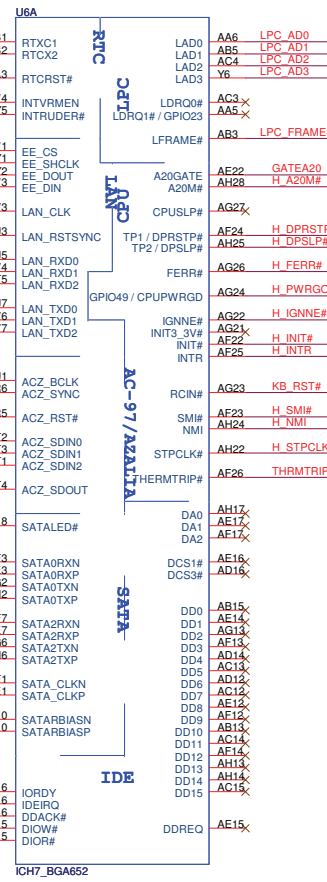
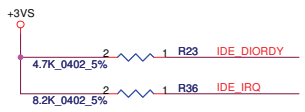
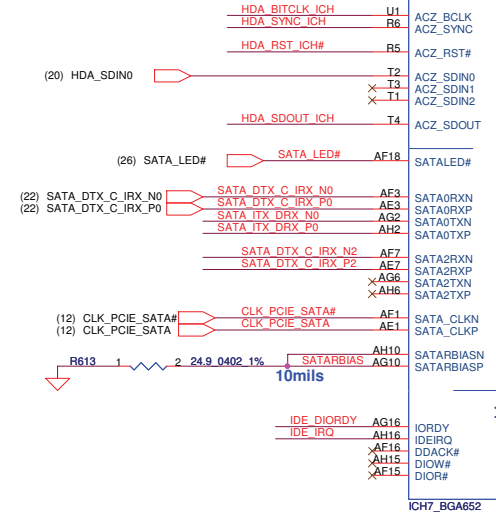
add C9 for keypart 12/08  
del C9 12/31



close ICH7

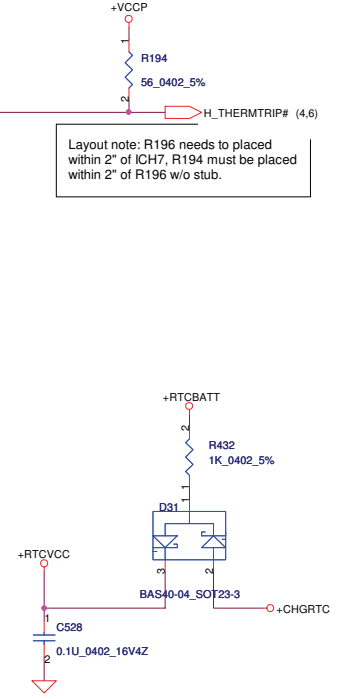


SATA\_RXn/p need tie to ground when SATA port not used



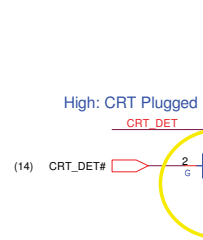
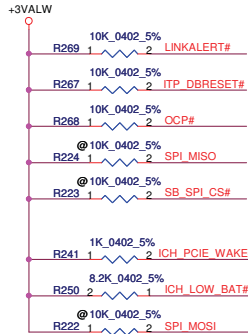
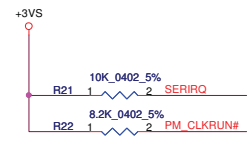
change R204 BOM structure 11/14  
Move R204 from P16 to P25 11/18

Layout note: R196 needs to be placed within 2" of ICH7, R194 must be placed within 2" of R196 w/o stub.



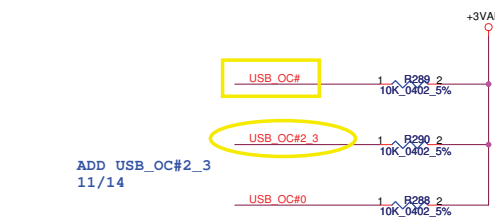
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	ICH7M(2/4)LAN,ATA,LPC,RTC
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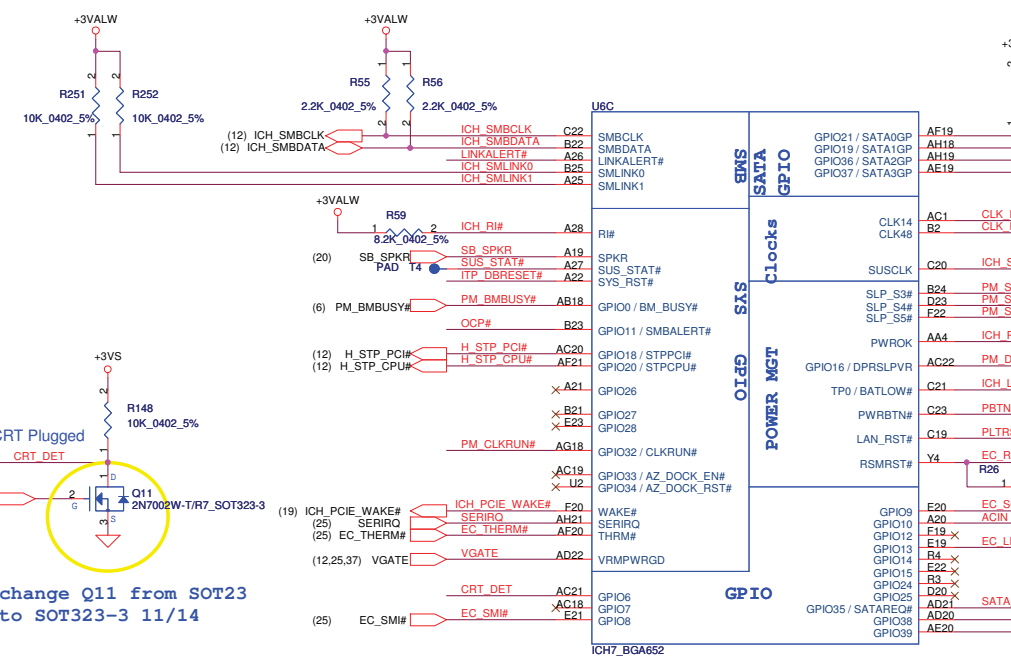


High: CRT Plugged  
CRT\_DET

change Q11 from SOT23 to SOT323-3 11/14



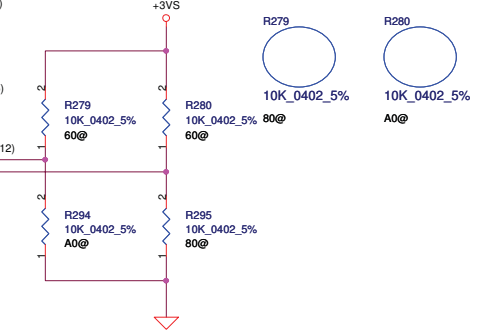
ADD USB\_OC#\_2\_3 11/14



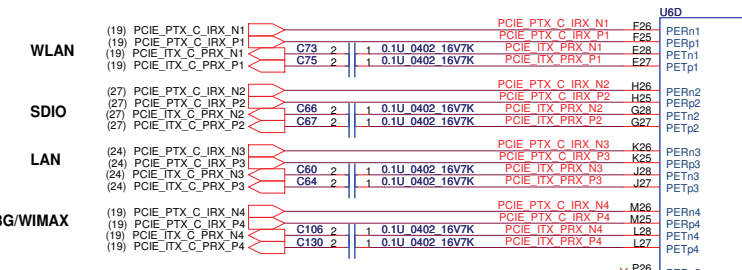
Place closely pin B2

Place closely pin AC1

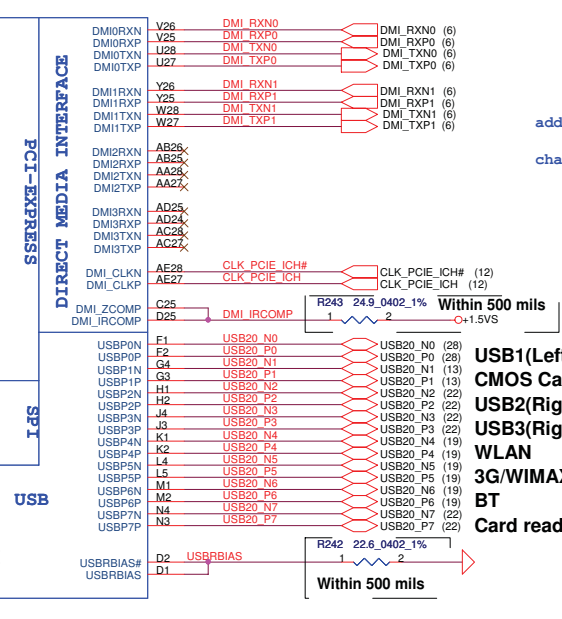
change R24 BOM structure 11/17  
Move R24 from P17 to P25 11/18



add R279, R280, R294, R295 02/04  
change R279, R280, R294, R295 BOM structure 02/18



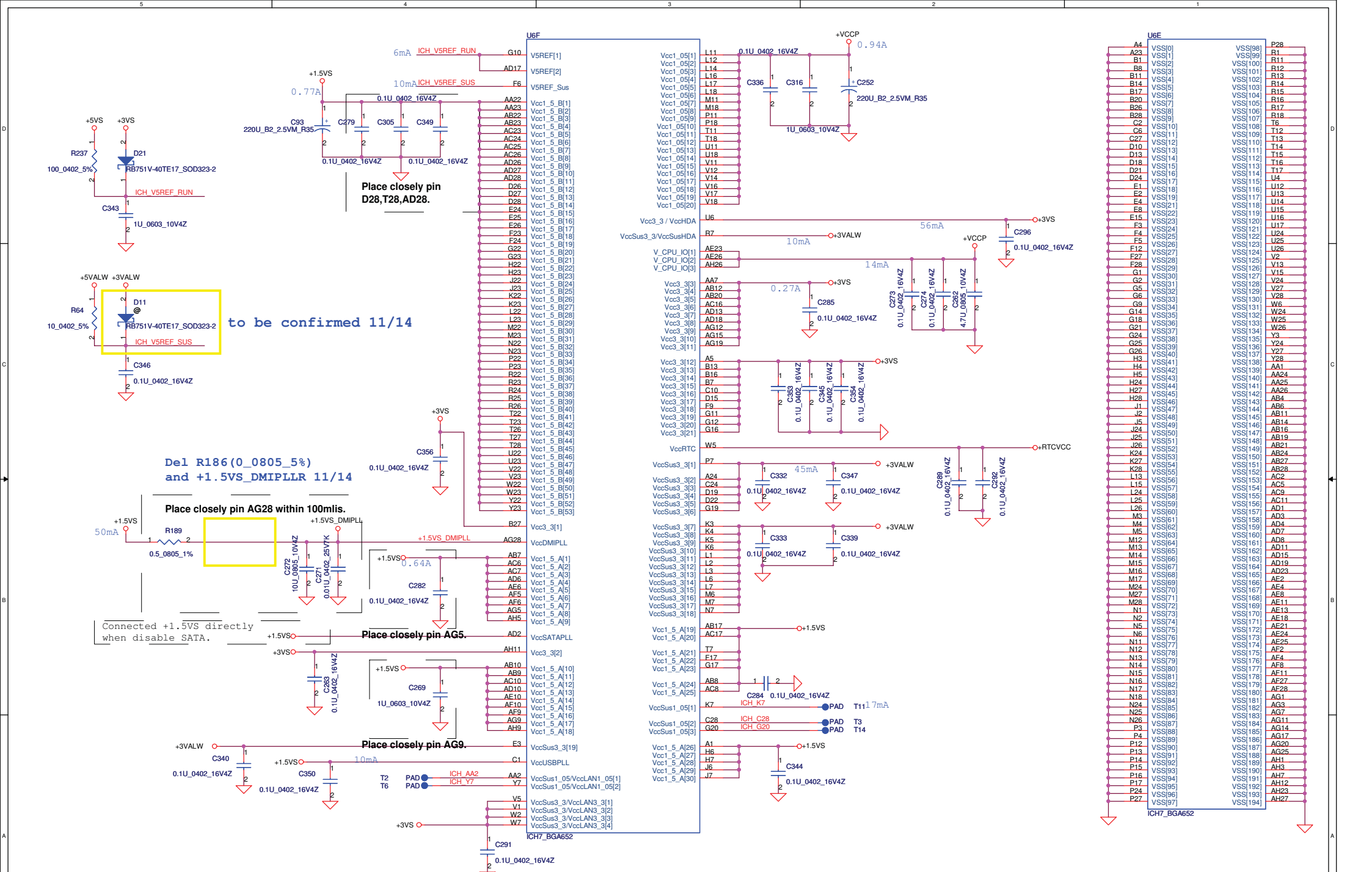
change USB\_OC# circuit 11/14



Within 500 mils

USB1(Left)  
CMOS Camera  
USB2(Right)  
USB3(Right)  
WLAN  
3G/WIMAX  
BT  
Card reader

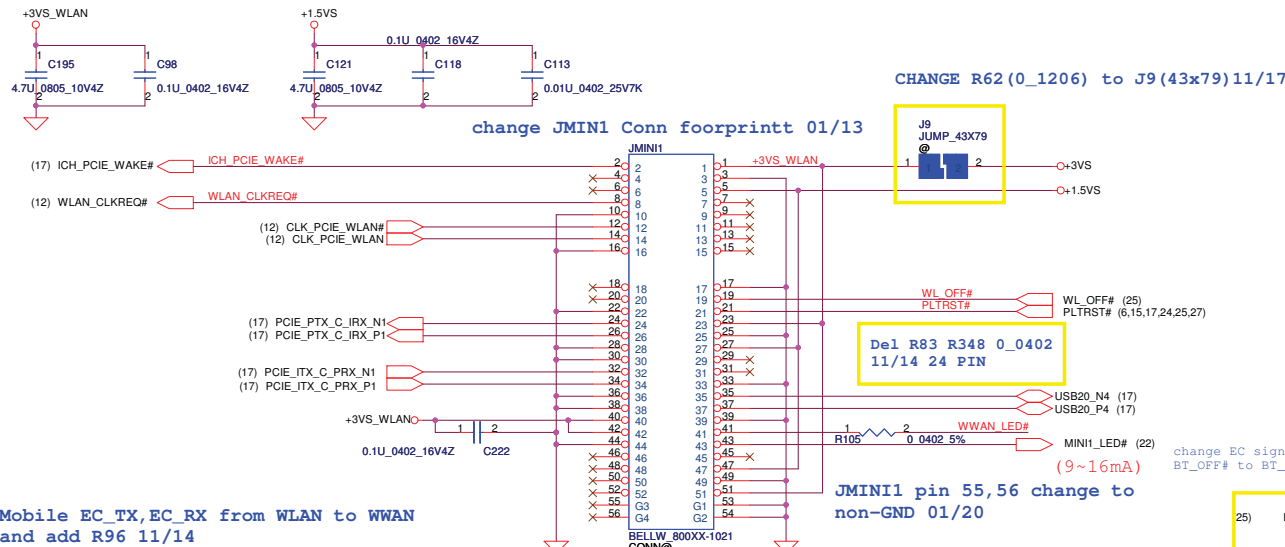
Security Classification		Compal Secret Data		Title	
Issued Date		Deciphered Date		ICH7M(3/4)USB,GPIO,PCIE	
2006/08/18		2007/8/18		KAV60 LA-5141P	
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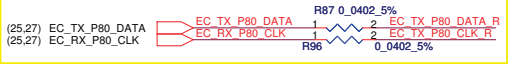
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Issued Date	2006/08/18	Deciphered Date
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Title		
ICH7M(4)POWER/GND		
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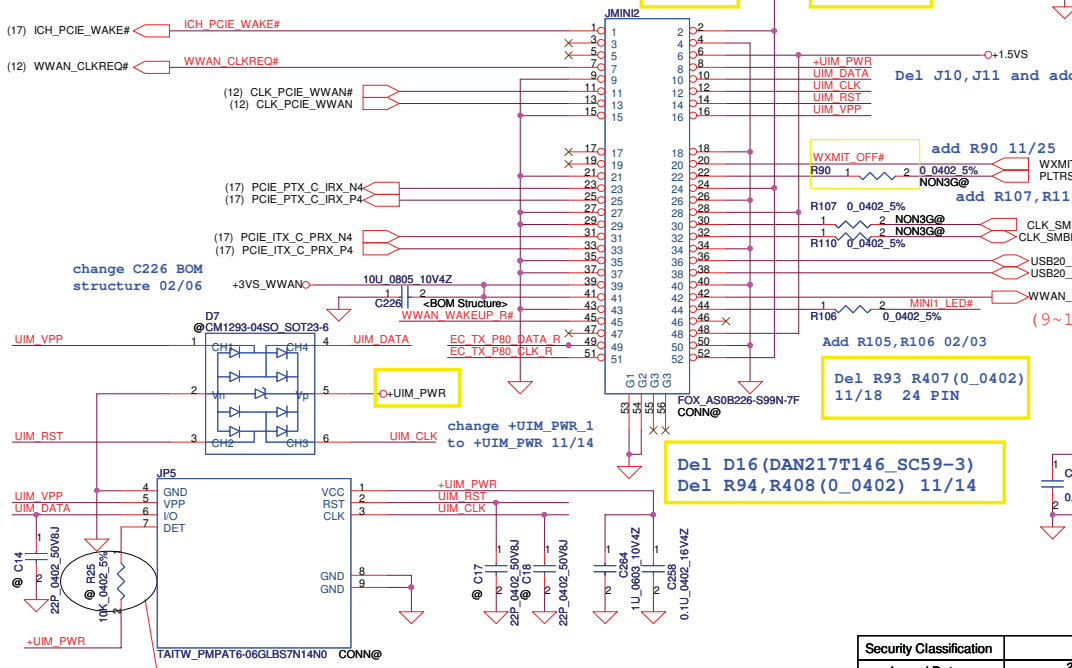
# Mini-Express Card for WLAN



Mobile EC\_TX, EC\_RX from WLAN to WWAN and add R96 11/14

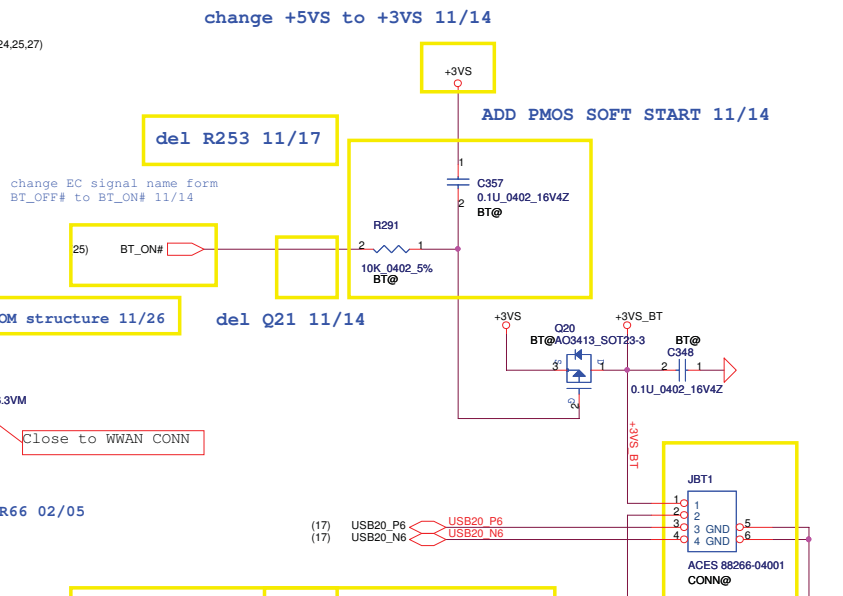


# Mini-Express Card for WWAN



Reserve for SIM card does not meet rise time and pull-up is needed.

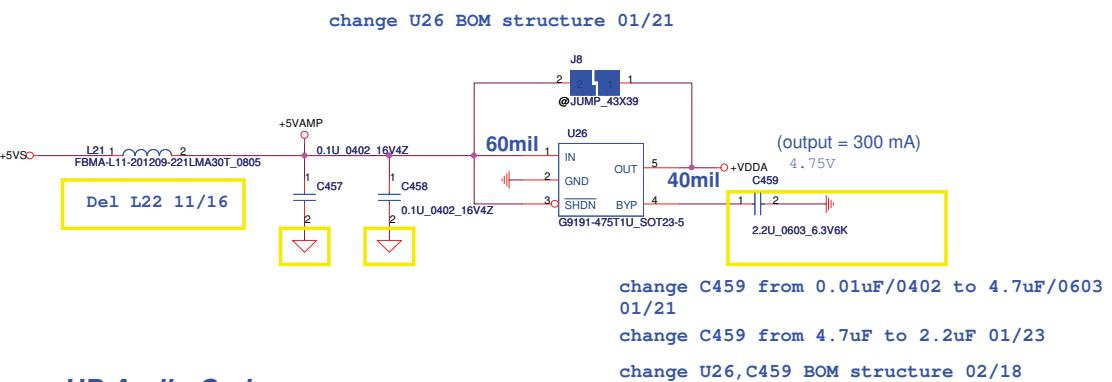
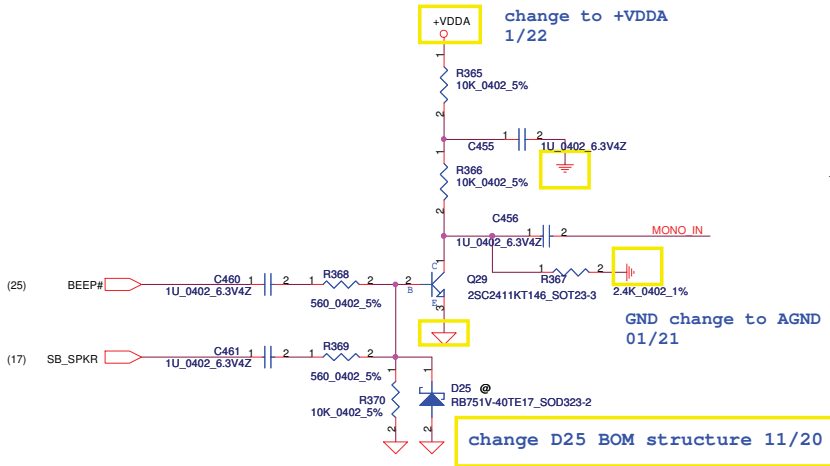
## BT MODULE CONN



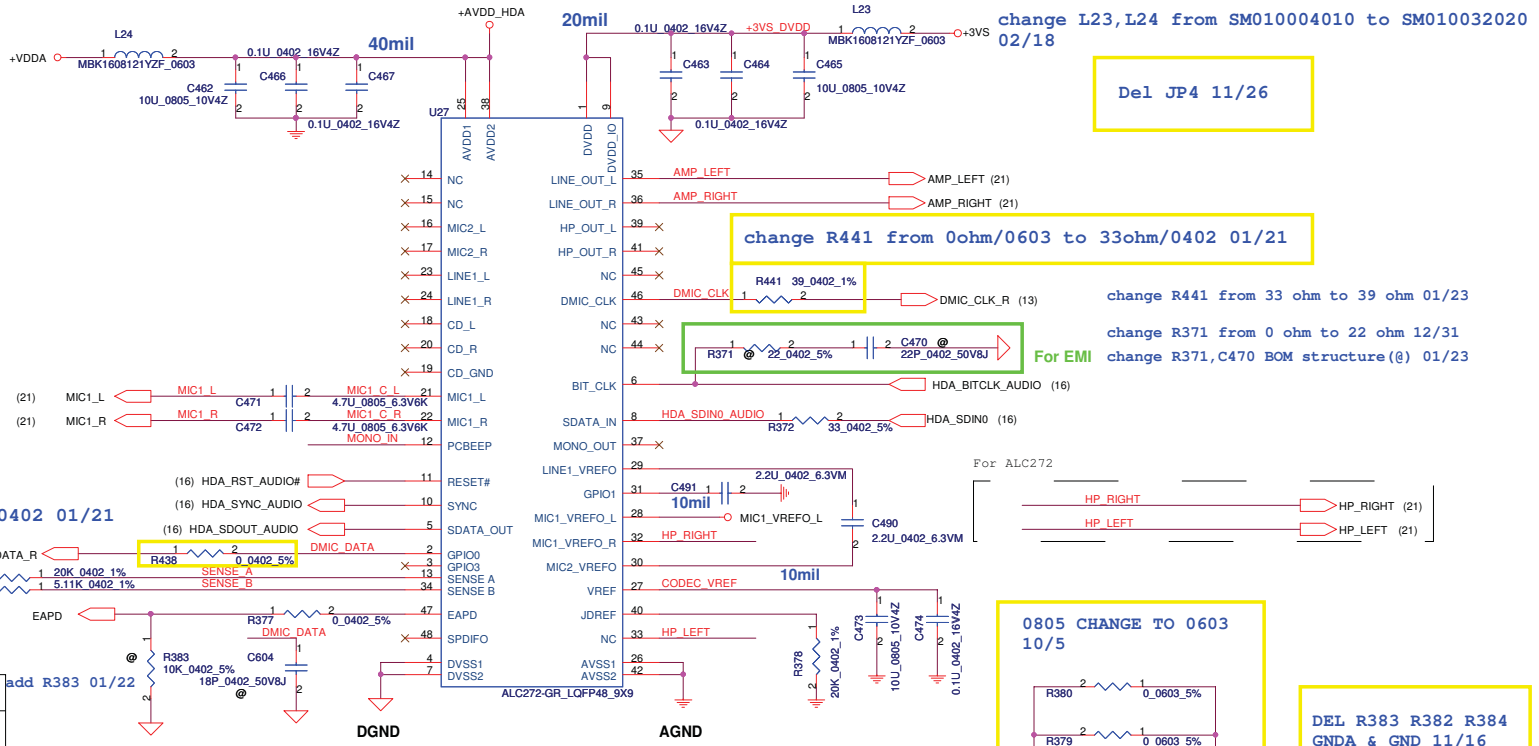
Security Classification	Compal Secret Data	
Issued Date	2006/08/05	Deciphered Date
		2007/8/18

Compal Electronics Inc.			
Title Mini-Card/BT-CONN			
Size	Document Number	Rev	
	KAV601A-5141P	0.2	
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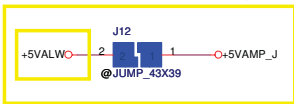
### HD Audio Codec



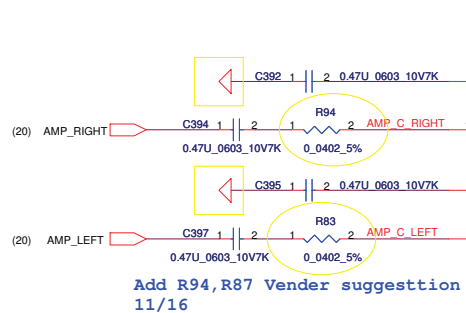
change R438 from 0ohm/0603 to 0ohm/0402 01/21

Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
SENSE B	5.1K	PORT-D (PIN 35, 36)
	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
5.1K	PORT-H (PIN 45, 46)	

add J12 12/04

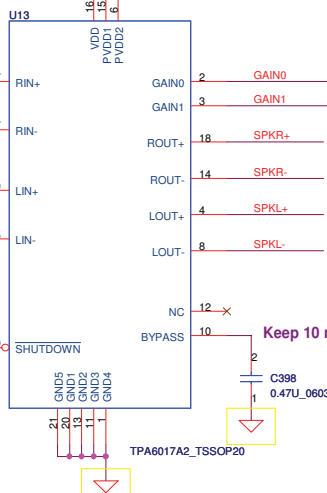


+5VS change to +5VALW 12/11



Add R94, R87 Vender suggestion 11/16

(25) EC\_MUTE#

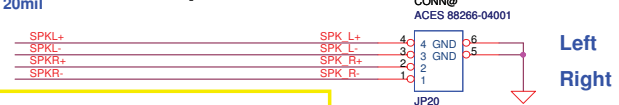


change +5VAMP to +5VS 12/02

20081029 Update to 6dB

Analog ground change to digital ground 08/11/16

Int. Speaker Conn.

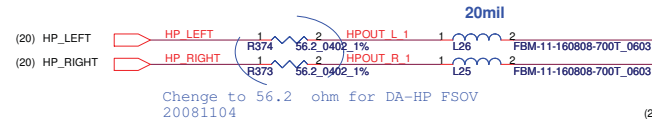


change JP20 Conn and pin design 11/26

del R388, R387, R386, R385, D10, D13 12/11

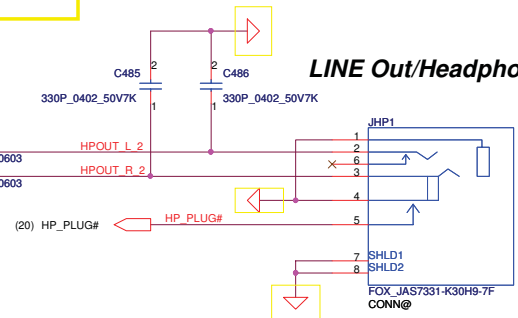
change JP20 Conn 01/16

SWAP JP20 01/20

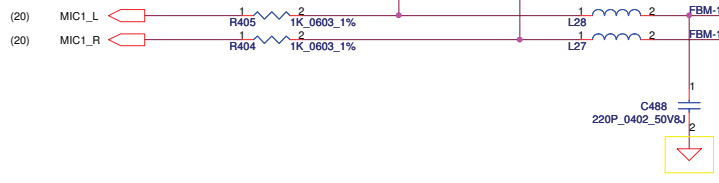
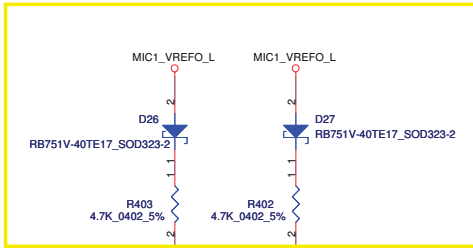


Change to 56.2 ohm for DA-HP FSOV 20081104

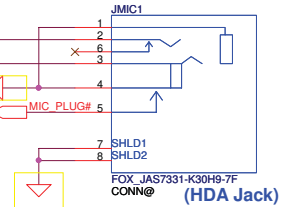
LINE Out/Headphone Out



11/16



MIC JACK



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Move SATA HDD Conn to small board 11/21

SWAP JP7 pin define 12/03

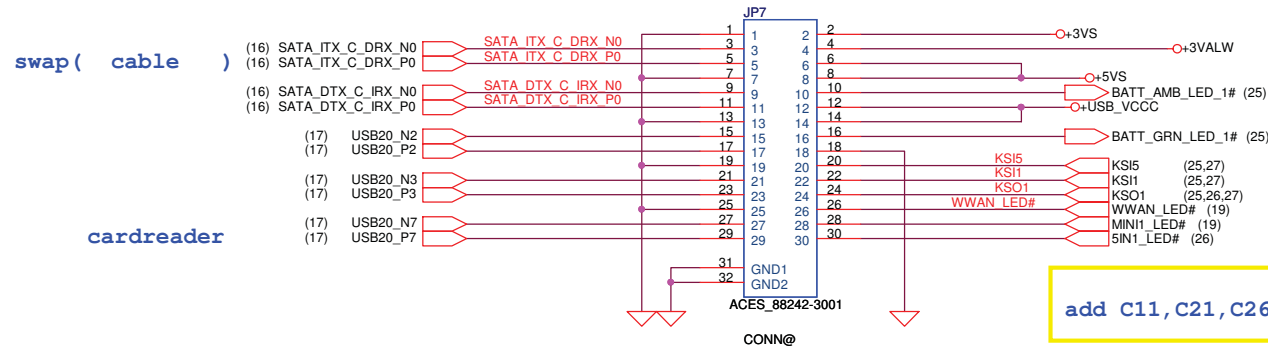
To cardreader/B Conn.

	KSO1
KSI1	WL_BTN#
KSI5	3G_BTN#

+3VS\_READER change to +3VALW 12/15

add net name BATT\_AMB\_LED#  
BATT\_GRN\_LED# 12/15

### SATA&CARDREADER&USB Conn



add J15 J16 12/08  
del J15, J16, C21 12/15

add C11, C21, C26, C27 for keypart 12/08

add C28 for keypart 01/14

del C11, C28, C26 01/21

del C26 02/03

ADD SATA&CARDREADER&USB Conn (JP7) 11/26

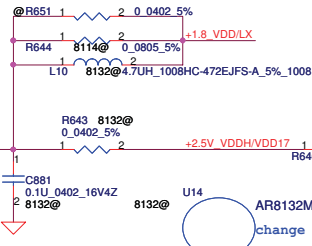
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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title
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Size	Document Number	KAV60 LA-5141P		Rev
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Move Card Reader to small board 11/21

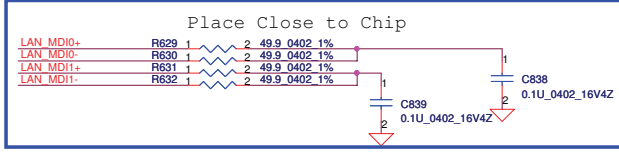
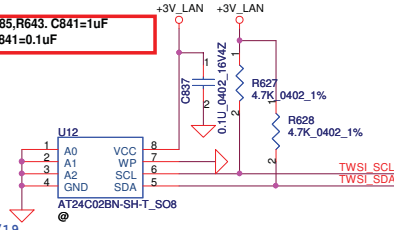
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Issued Date	2006/08/04	Deciphered Date	2007/8/18	Title		
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				Size	Document Number	Rev
				B	KAV60 LA-5141P	0.2
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hexair@hotmail.com

change R644 from 0603 to 0805 12/31  
 change R643 from 0603 to 0402 12/31  
 change C841 from 0603 to 0402 12/31  
 add R651 0\_0402 02/03  
 change C841 from 0402 1U to 0603 1U  
 02/03



AR8114A: remove L1,C881,C885,R643. C841=1uF  
 AR8132:remove R644,R645. C841=0.1uF



Chang C855 form 4.7U to 10U 11/16 vendor suggest

del C843,C844 12/02

(25) LAN\_WAKE#

(12) CLK\_PCIE\_LAN#

(12) CLK\_PCIE\_LAN#

(17) PCIE\_ITX\_C\_PRX\_P3

(17) PCIE\_ITX\_C\_PRX\_N3

(17) PCIE\_PT\_X\_IRX\_P3

(17) PCIE\_PT\_X\_IRX\_N3

LAN X1 LAN X2

change C852,C853,Y5 BOM structure 12/15

add C55 on page 24 12/15

del C55 12/16

change C852,C853 from 27p to 15p 01/23

LAN\_ACTIVITY#

LAN\_ACTIVITY#

LAN\_ACTIVITY#

LAN\_ACTIVITY#

LAN\_ACTIVITY#

LAN\_ACTIVITY#

LAN\_ACTIVITY#

LAN\_ACTIVITY#

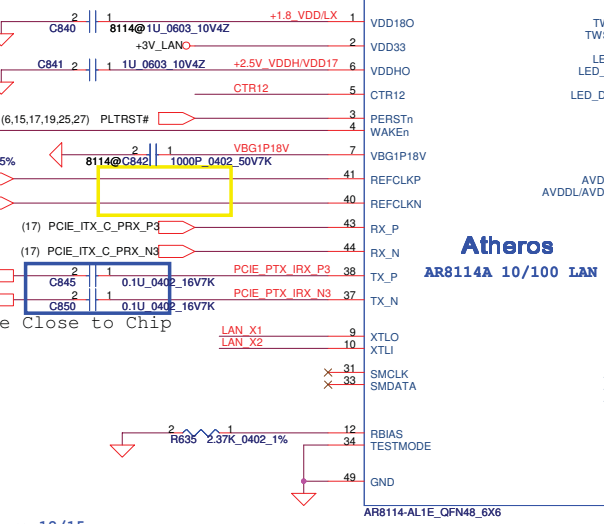
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LAN\_ACTIVITY#

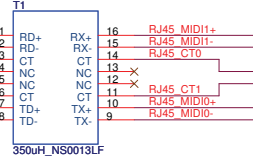
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LAN\_ACTIVITY#

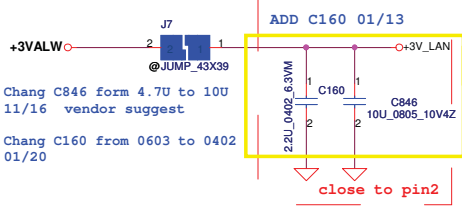
LAN\_ACTIVITY#



**Atheros**  
**AR8114A 10/100 LAN**



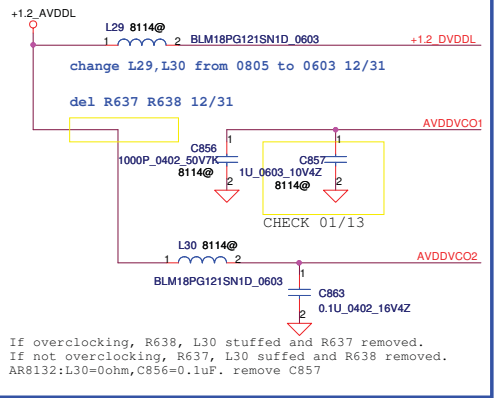
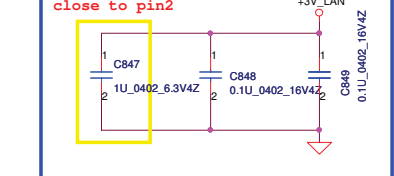
change RJ45 Conn 11/26



change BJT form MMJT9435T1G to MBT35200 11/16

Layout Notice : Place as close chip as possible.

change C847 from 0.1u to 1u 12/02



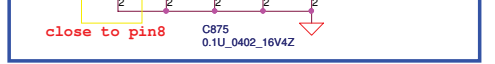
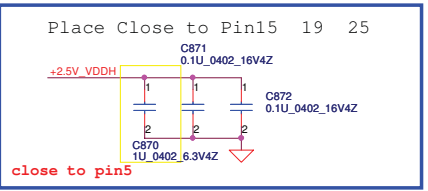
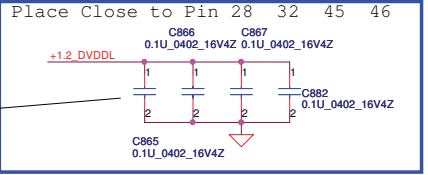
change L29,L30 from 0805 to 0603 12/31

del R637 R638 12/31

change L30,C856,C857 BOM structure 12/22

change C873 from 0.1u to 1u 12/02

change C873 from 0.1u to 1u 12/02



change L29,L30 from 0805 to 0603 12/31

del R637 R638 12/31

change L30,C856,C857 BOM structure 12/22

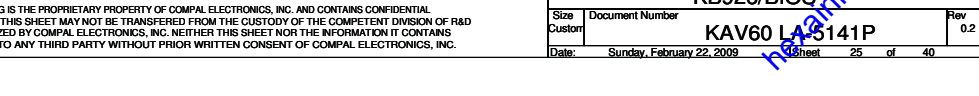
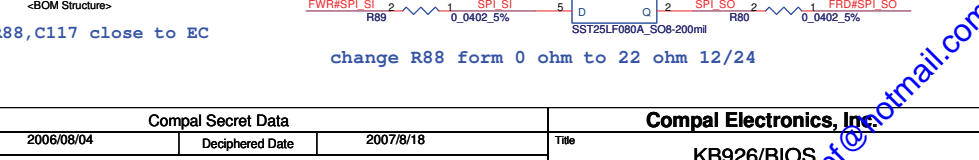
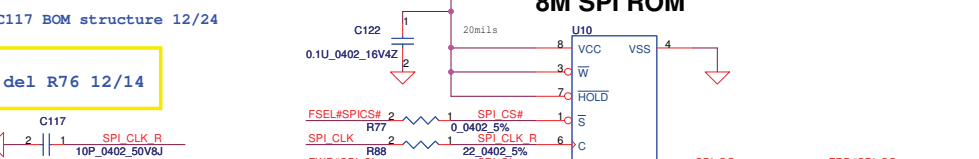
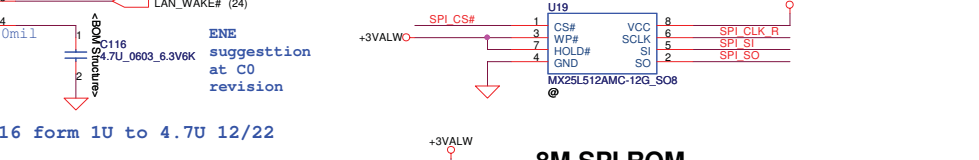
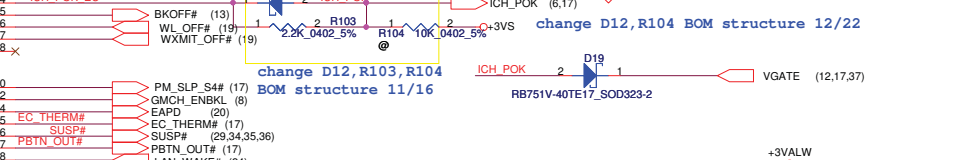
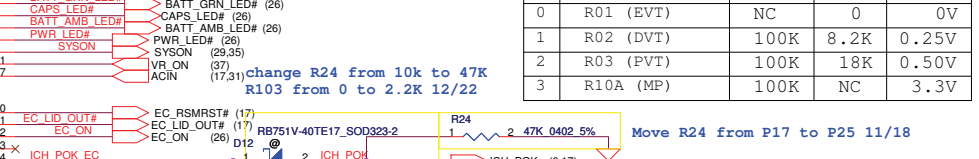
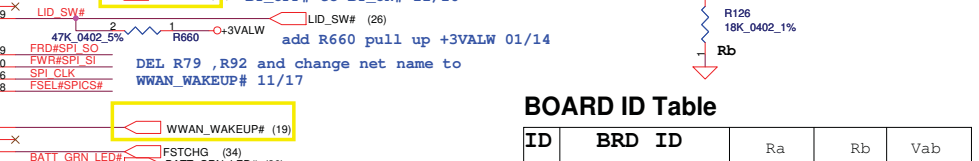
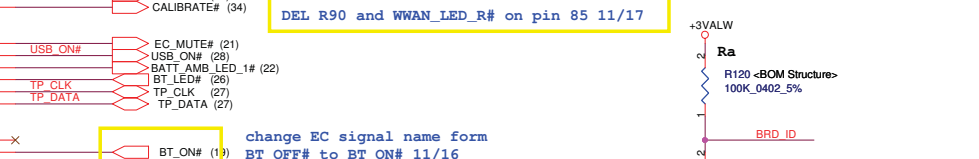
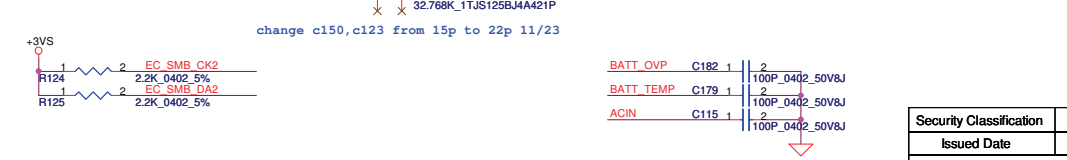
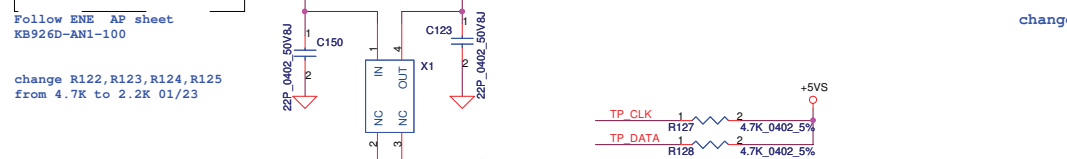
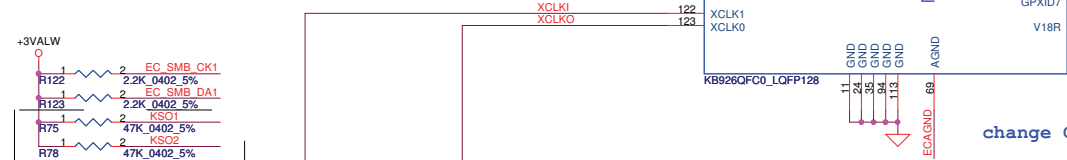
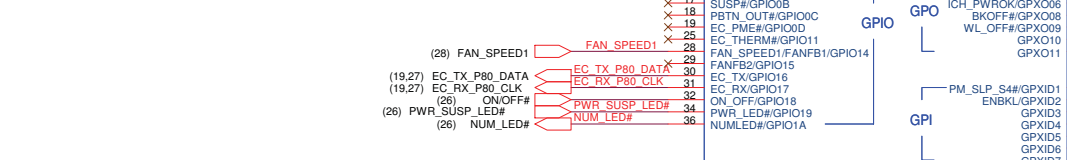
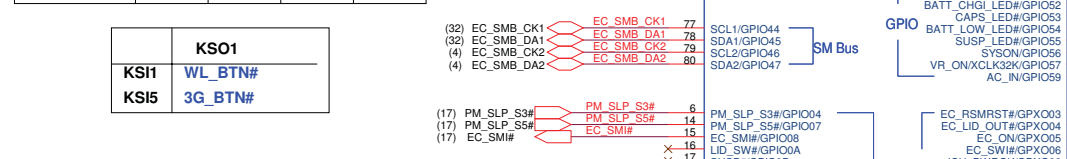
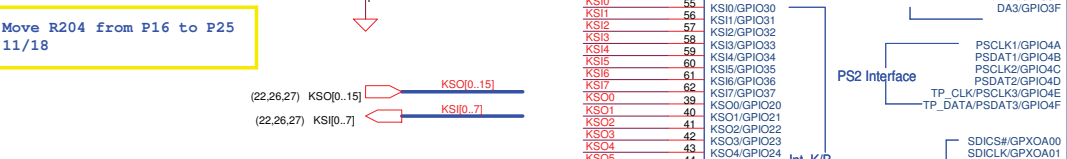
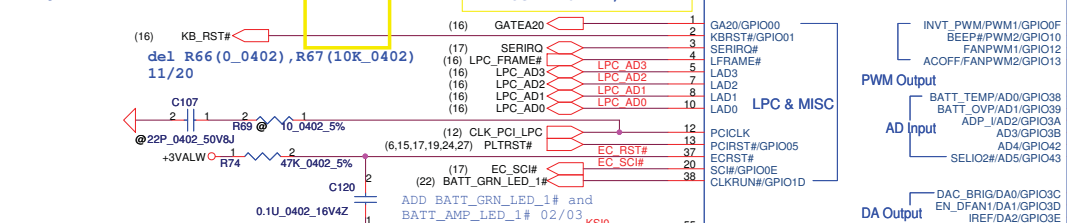
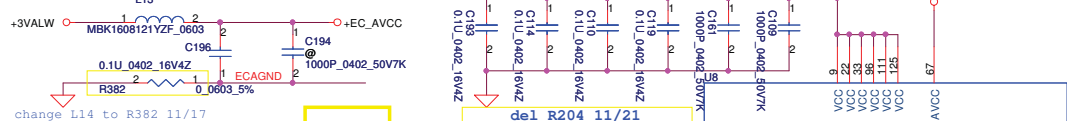
change C873 from 0.1u to 1u 12/02

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AR8114		
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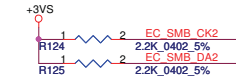
Move R204 from P16 to P25 11/18

	KSO1	KSI1	KSI5	GPIO15
WLAN_OFF#	v	v		High
WXMIT_OFF#	v		v	High
WXMIT_ON#	v	v		Low

	KSO1
KSI1	WL_BTN#
KSI5	3G_BTN#

Follow ENE AP sheet KB926D-ANI-100

change R122, R123, R124, R125 from 4.7K to 2.2K 01/23

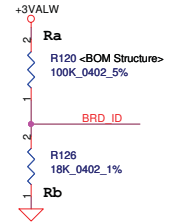


change c150, c123 from 15p to 22p 11/23

BATT_OVP	C182	1	2	100P_0402_50V8J
BATT_TEMP	C179	1	2	100P_0402_50V8J
ACIN	C115	1	2	100P_0402_50V8J

change R120 and R126 to PVT ID 01/14

DEL R90 and WWAN\_LED\_R# on pin 85 11/17



change EC signal name form BT\_OFF# to BT\_ON# 11/16

add R660 pull up +3VALW 01/14

DEL R79, R92 and change net name to WWAN\_WAKEUP# 11/17

### BOARD ID Table

ID	BRD ID	Ra	Rb	Vab
0	R01 (EVT)	NC	0	0V
1	R02 (DVT)	100K	8.2K	0.25V
2	R03 (PVT)	100K	18K	0.50V
3	R10A (MP)	100K	NC	3.3V

change R24 from 10k to 47k R103 from 0 to 2.2K 12/22

Move R24 from P17 to P25 11/18

change D12, R104 BOM structure 12/22

change D12, R103, R104 BOM structure 11/16

ENE suggestion at C0 revision

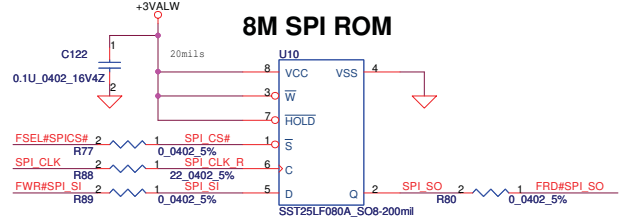
change C116 form 1U to 4.7U 12/22

change C117 BOM structure 12/24

del R76 12/14

R88, C117 close to EC

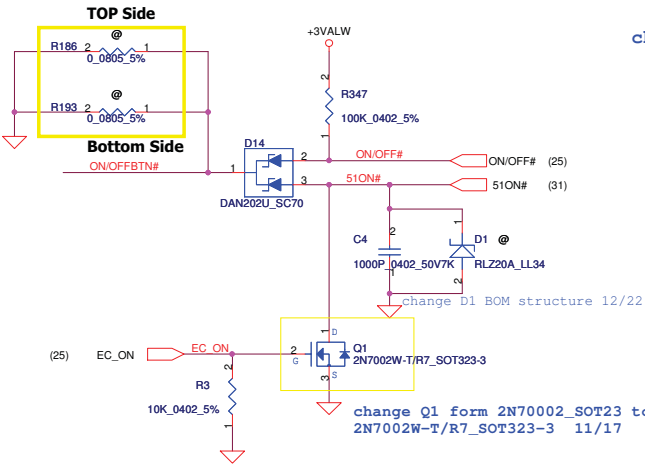
change R88 form 0 ohm to 22 ohm 12/24



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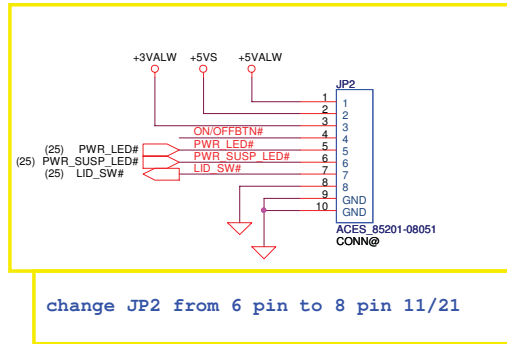
# ON/OFF switch

change J1, J3 (43 x 79) to R186, R193 (0\_0805) 11/16



change JP2 Conn 12/01

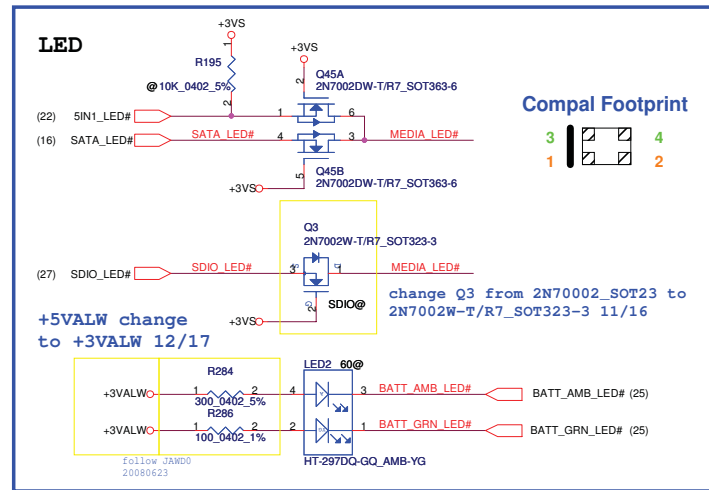
change JP2 Conn 11/25 **To PWR/B Conn.**



change JP2 from 6 pin to 8 pin 11/21

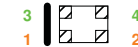
Change PWR\_LED and PWR\_SUSP\_LED Net name 01/13

change R518 from 300 to 422 ohm 02/06



## LED

Compal Footprint



+5VALW change to +3VALW 12/17

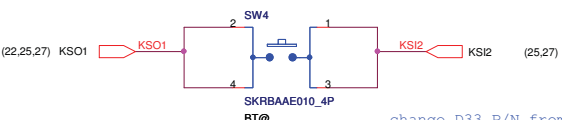
change R284 from 150 ohm to 300 ohm R286 from 120 ohm to 100 ohm 01/23

**DEL LID Switch 11/21**

KSO1	
KSI2	BT_BTN#

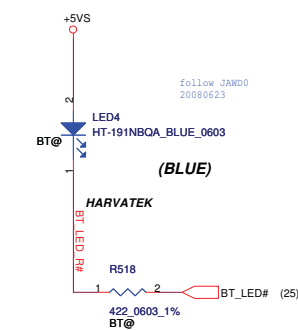
Change SW4 P/N to SN111005800 01/13

## Bluetooth Button

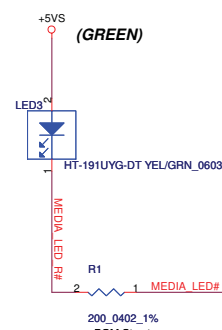


change D33 P/N from SC10T24C000 to SCA00000A00 and BOM structure 12/22

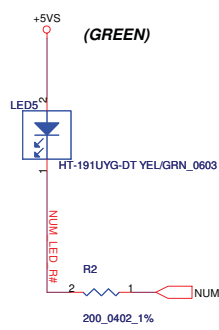
## Bluetooth LED



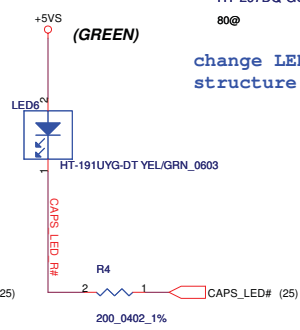
## MEDIA\_LED



## NUM\_LED



## CAPS\_LED



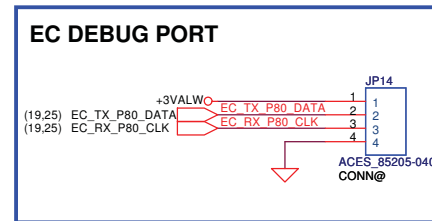
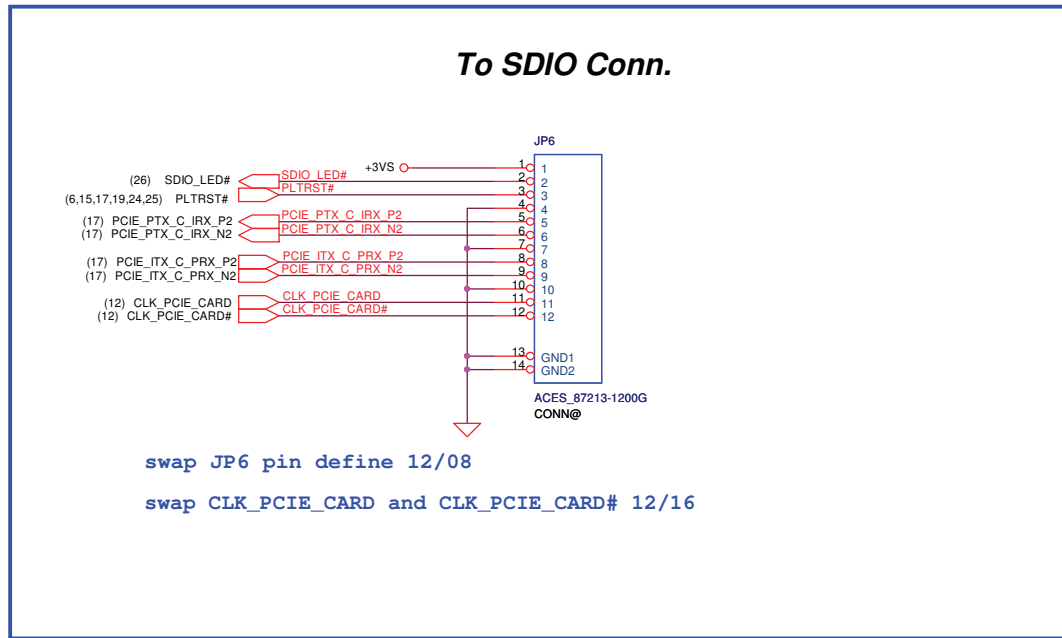
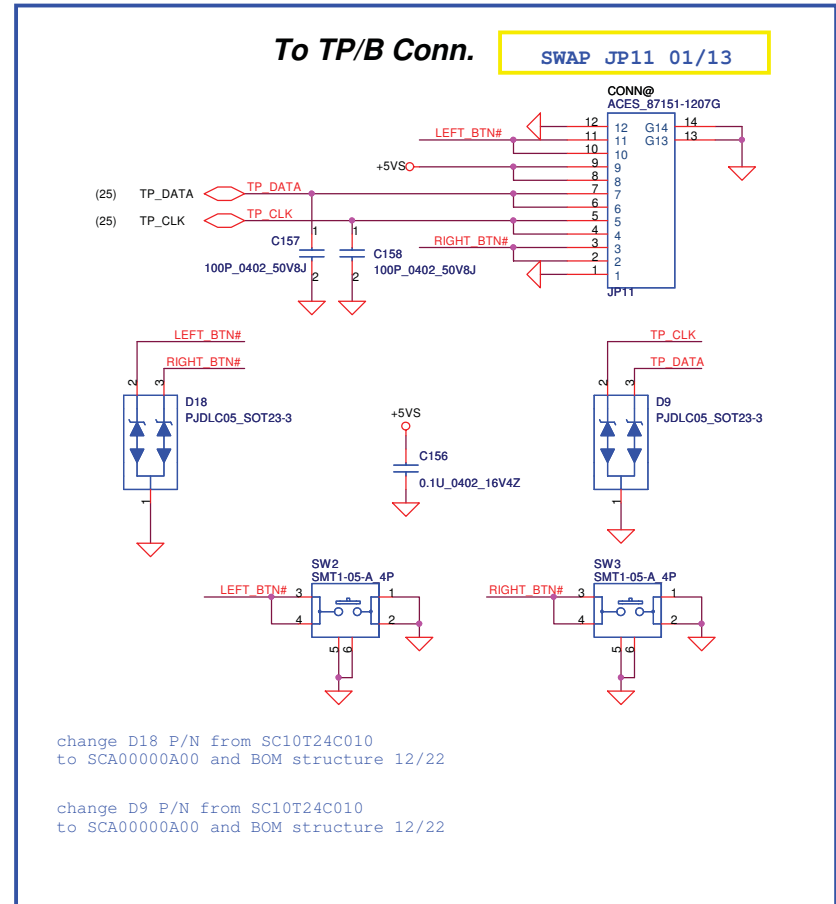
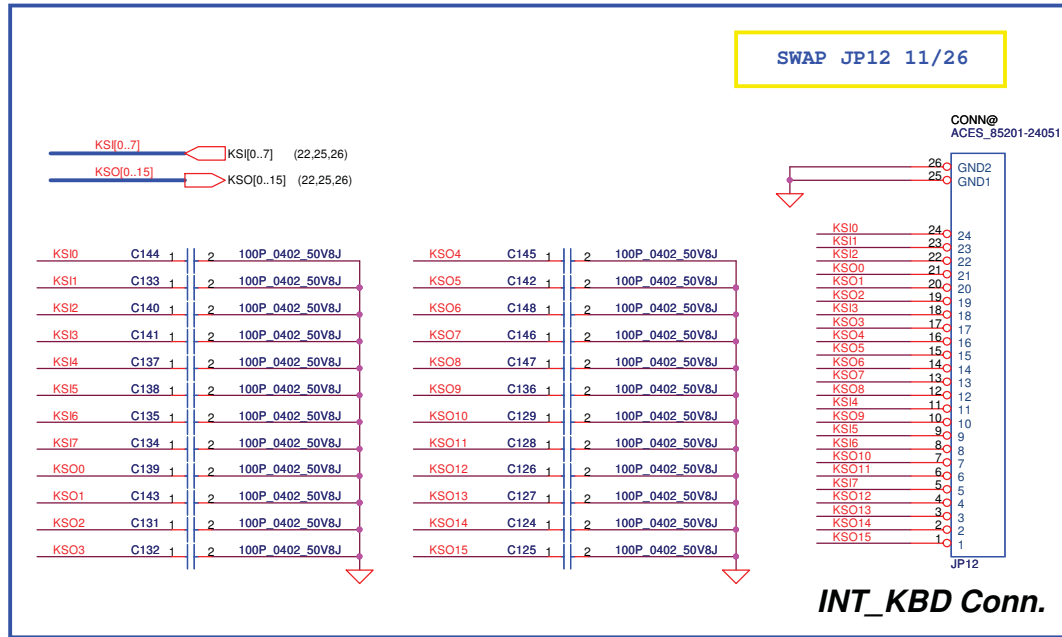
change LED2 BOM structure 02/18

R2, R4, R518 close to EC 12/03

R1 close to Q3 12/03

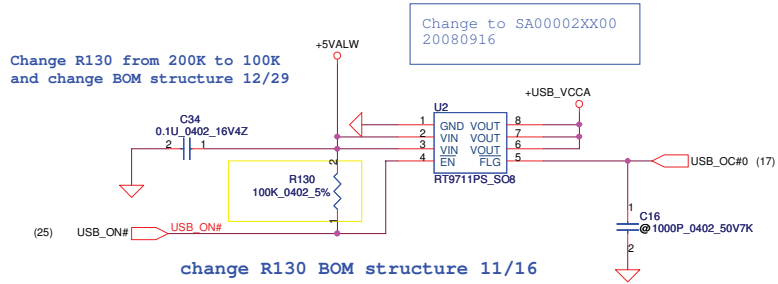
change R1, R2, R4 from 300 to 200 ohm 02/06

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U2 Change to SA000033H00  
12/24

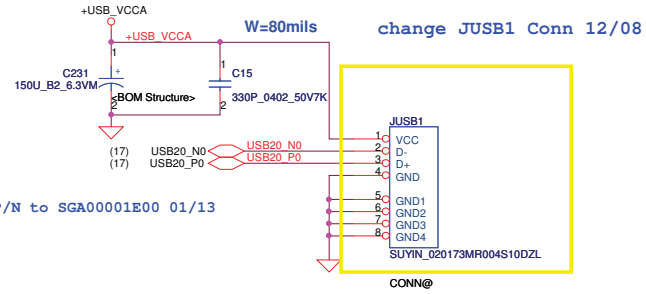


change D29 P/N from SC300000000 to SC300000B00 and BOM structure 12/22

SWAP D29 Pin Define 12/10

del D29 ,L9,R144,R136 01/16

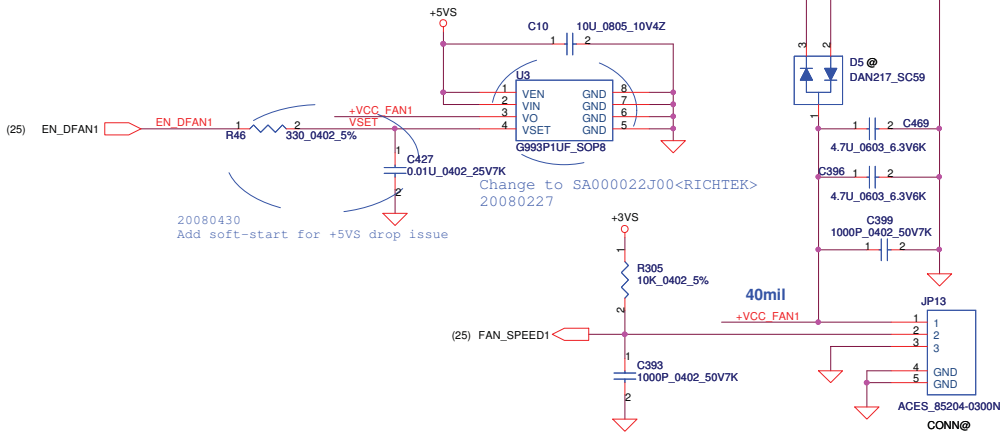
USB CONN. 1



U3 Change to SA000035G00  
12/31

Change U3 from SA000035G00 to SA000022J00 02/06

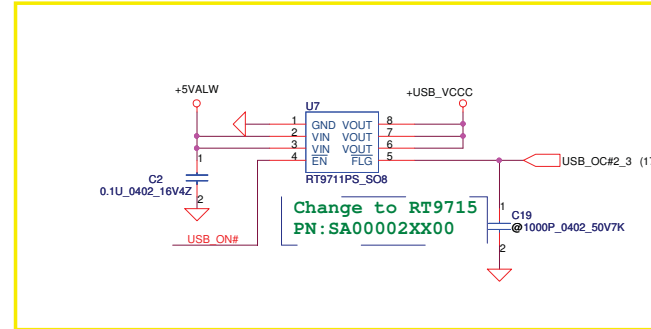
FAN1 Conn



change JP13 Conn 11/25

change C396 from 10U/0806 to 4.7U/0603 01/22  
add C469 01/22

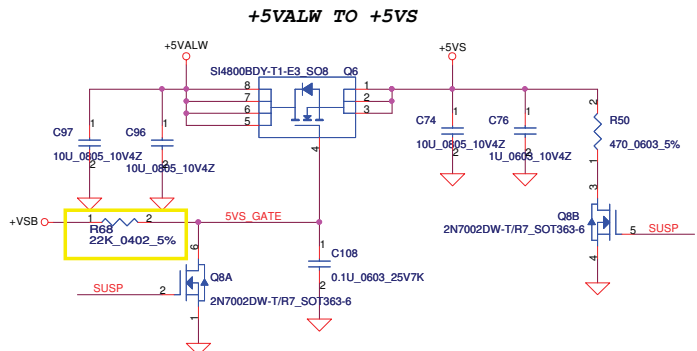
del JP3 11/26



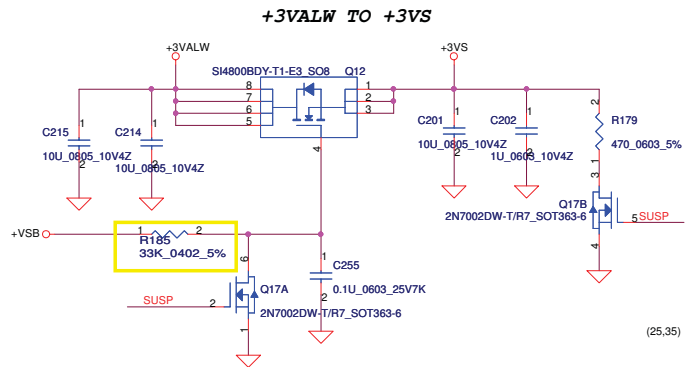
add U7 11/26

U7 Change to SA000033H00  
12/24

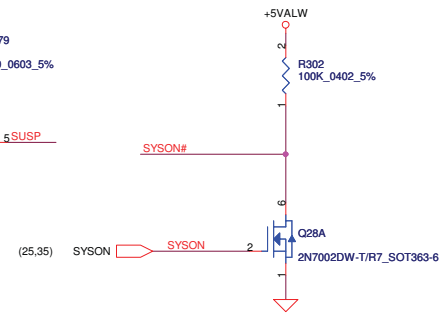
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								USB PORTS/FAN					
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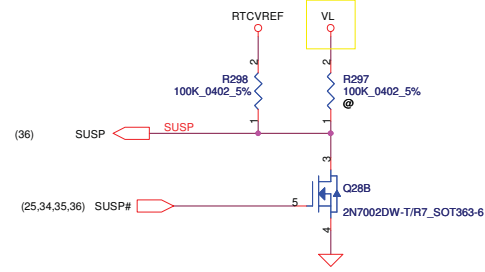
change R68 from 200K to 22K 12/10



change R185 from 200K to 33K 12/10



+5VALW CHANG TO VL 11/16

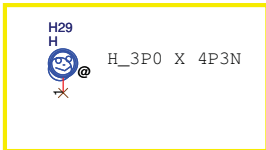


change Q2, Q15, Q24, Q7, Q23 form 2N70002\_SOT23 to 2N7002W-T/R7\_SOT323-3 11/17

change R18, R169, R280, R61, R279 Q2, Q15, Q24, Q7, Q7, Q23 BOM structure 11/16

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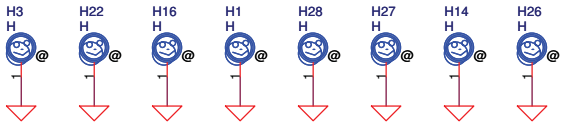
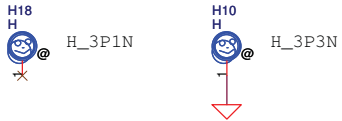
Hotmail.com



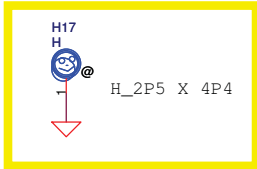
update Screw 12/04

del H11 H\_3P0N 12/10

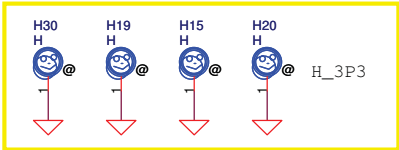
change H18 from 3P2N to 3P1N 02/22



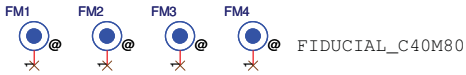
del H31 01/16



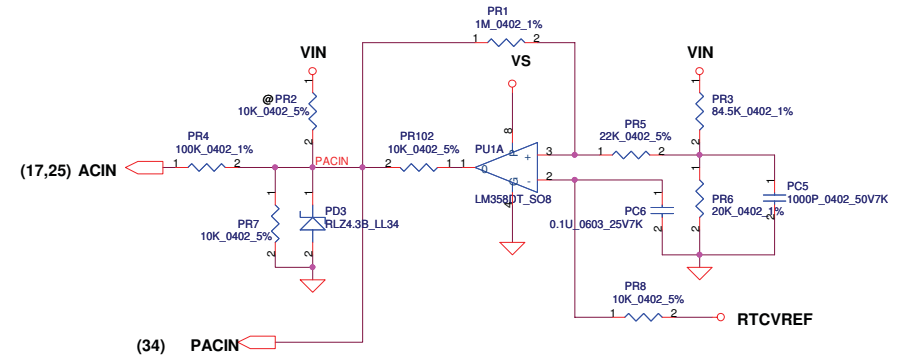
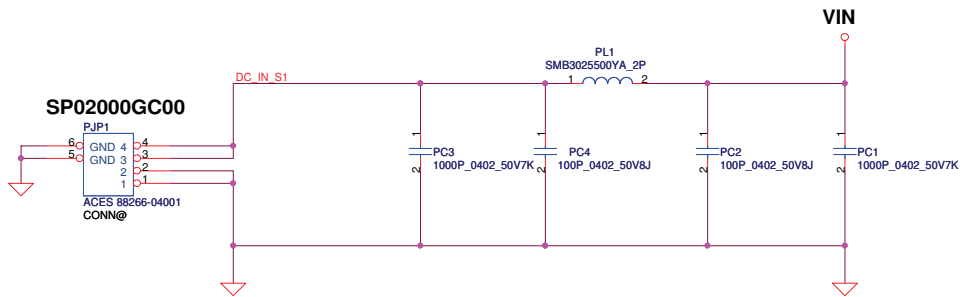
change H17 from H\_2P5 to H\_2P5 X 4P4



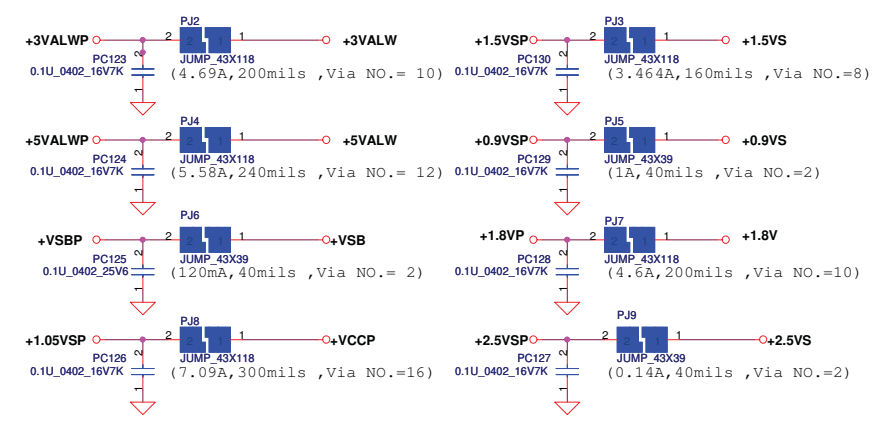
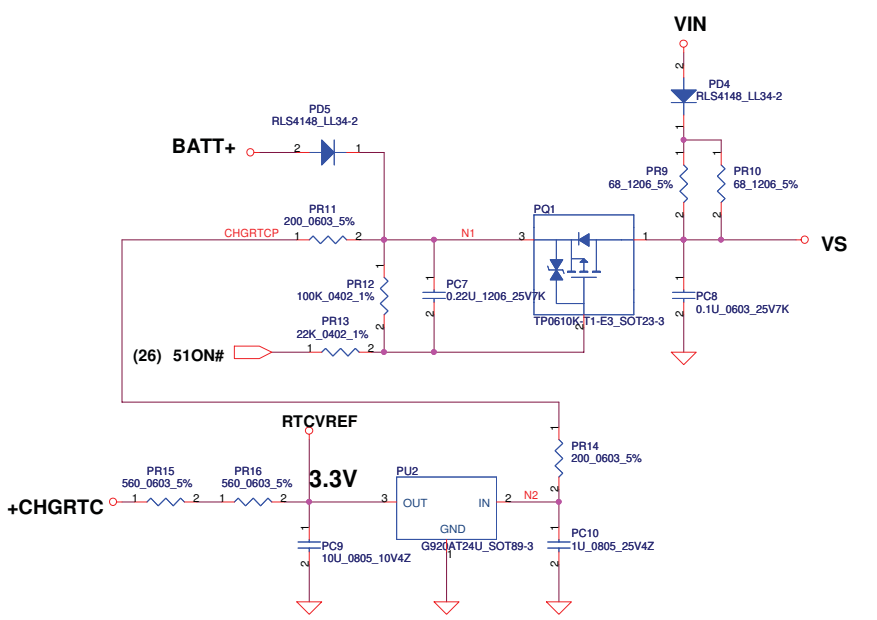
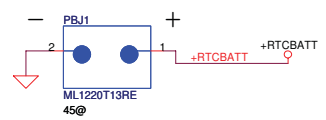
add H32 12/17  
 modify H15, H19, H20, H29, H30 12/17  
 update H15, H19, H20, H30 from 3P8 to 3P6 01/22  
 update H15, H19, H20, H30 from 3P6 to 3P3 02/22

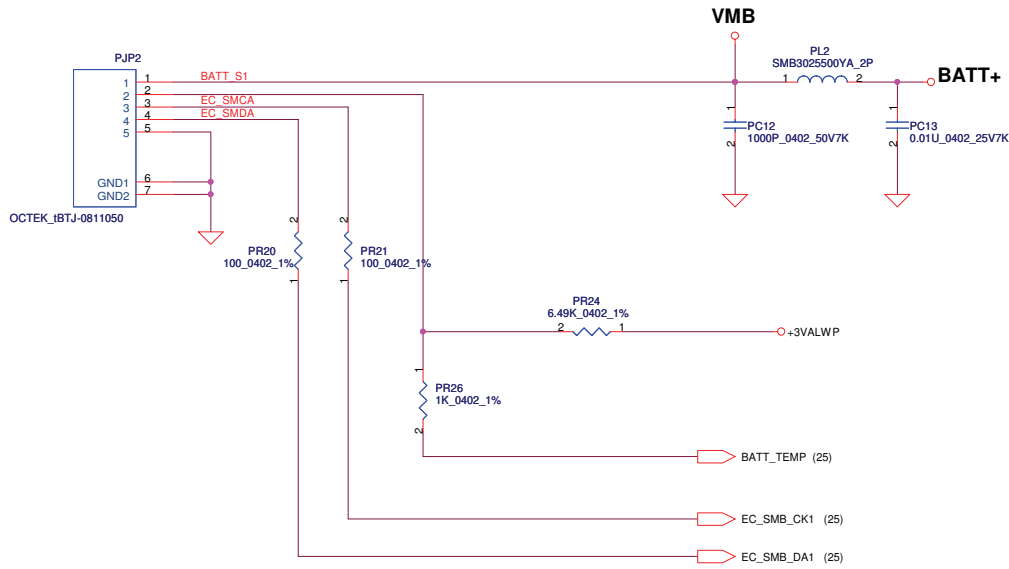


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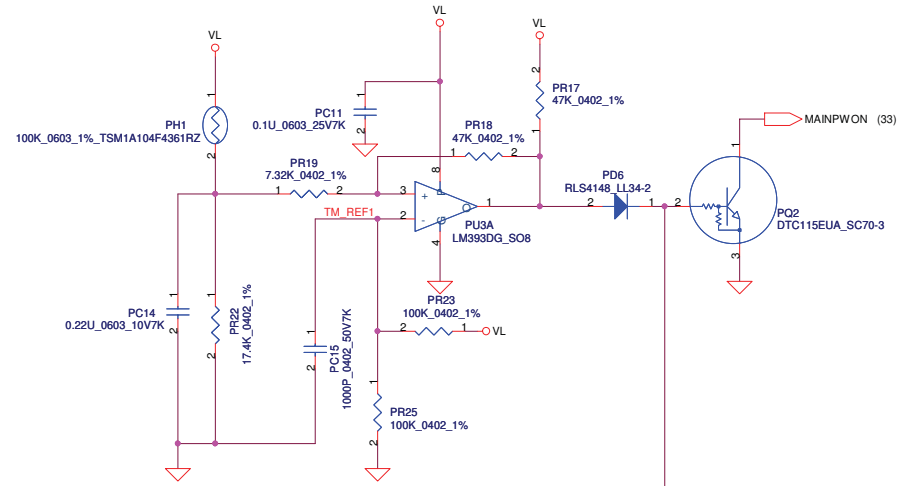


Vin Dectector			
	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V

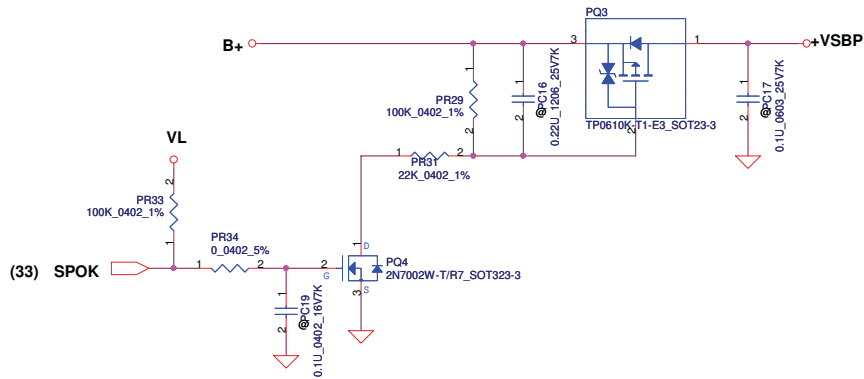
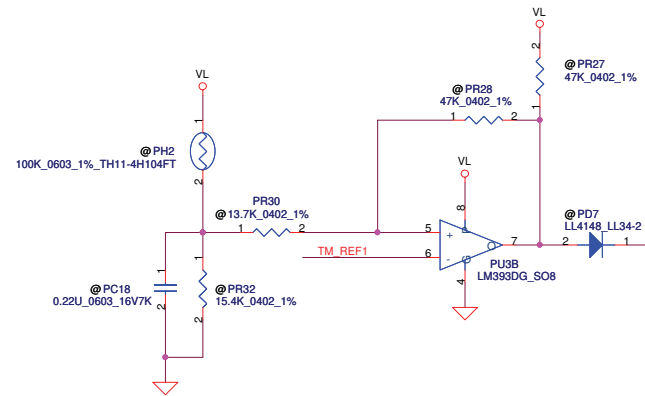




**PH1 under CPU botten side :**  
 CPU thermal protection at 92 degree C  
 Recovery at 56 degree C

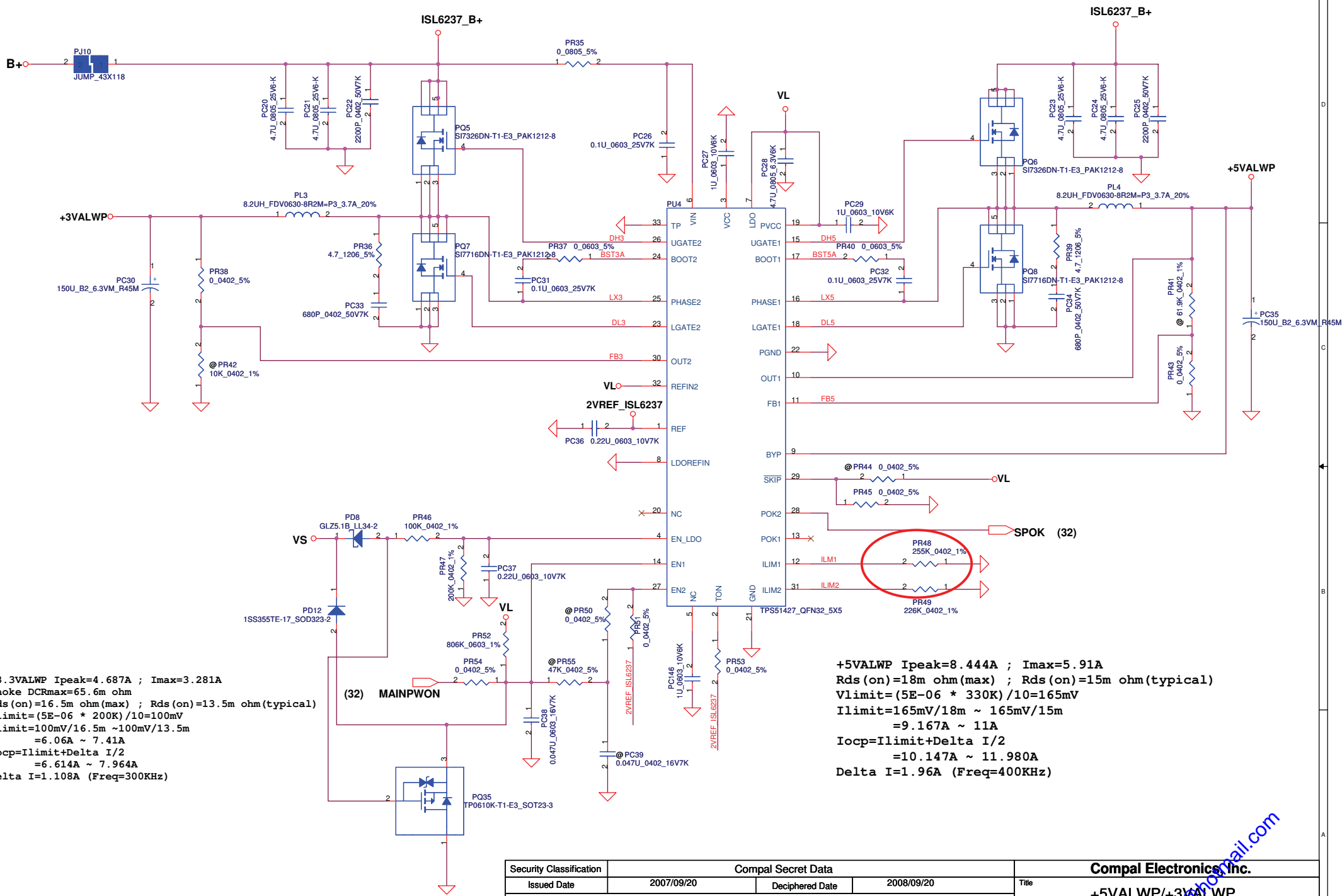


**PH2 near Battery CONN :**  
 BAT. thermal protection at 92 degree C  
 Recovery at 56 degree C



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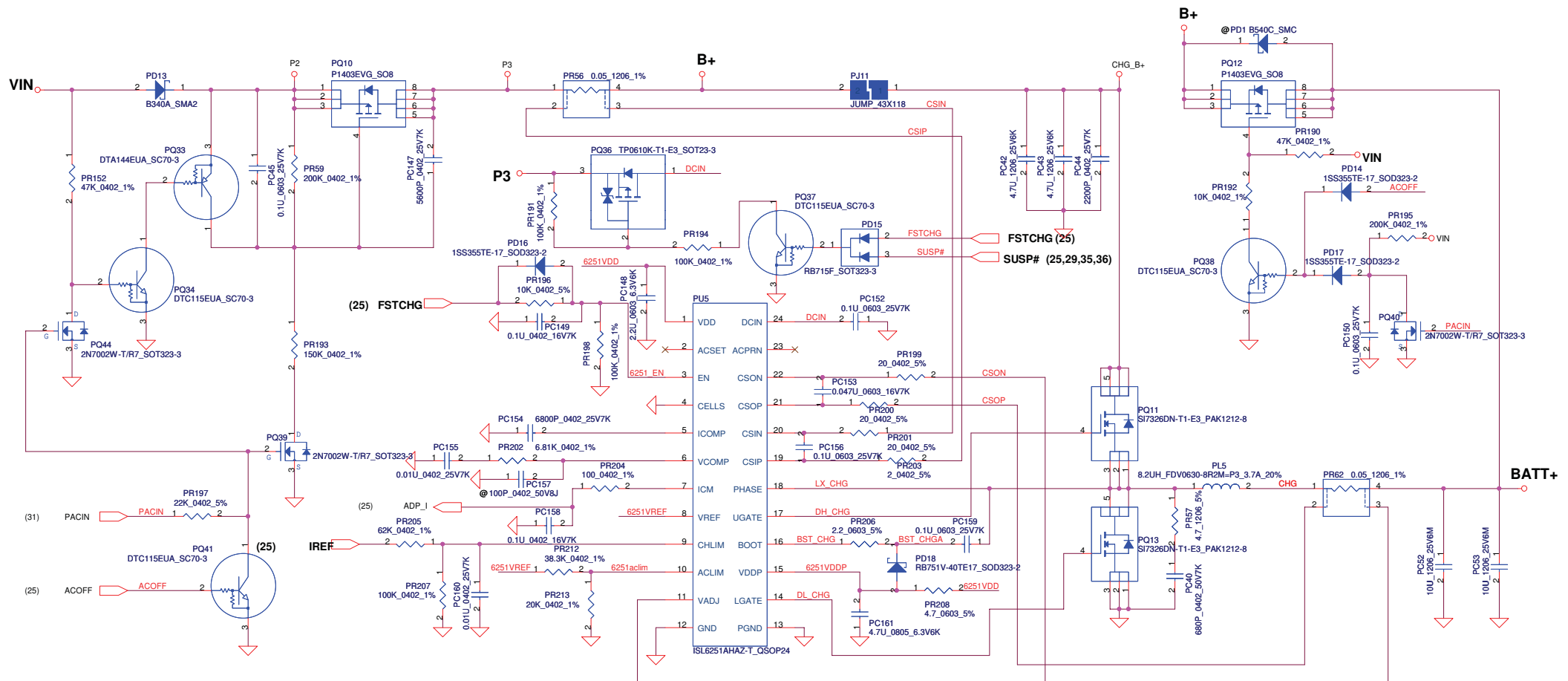


+3.3VALWP Ipeak=4.687A ; I<sub>max</sub>=3.281A  
 Choke DCR<sub>max</sub>=65.6m ohm  
 R<sub>ds(on)</sub>=16.5m ohm(max) ; R<sub>ds(on)</sub>=13.5m ohm(typical)  
 V<sub>l</sub>limit=(5E-06 \* 200K)/10=100mV  
 I<sub>l</sub>limit=100mV/16.5m ~100mV/13.5m  
 =6.06A ~ 7.41A  
 I<sub>ocp</sub>=I<sub>l</sub>limit+Delta I/2  
 =6.614A ~ 7.964A  
 Delta I=1.108A (Freq=300KHz)

+5VALWP Ipeak=8.444A ; I<sub>max</sub>=5.91A  
 R<sub>ds(on)</sub>=18m ohm(max) ; R<sub>ds(on)</sub>=15m ohm(typical)  
 V<sub>l</sub>limit=(5E-06 \* 330K)/10=165mV  
 I<sub>l</sub>limit=165mV/18m ~ 165mV/15m  
 =9.167A ~ 11A  
 I<sub>ocp</sub>=I<sub>l</sub>limit+Delta I/2  
 =10.147A ~ 11.980A  
 Delta I=1.96A (Freq=400KHz)

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$I_{ada} = 0 \sim 1.58A (30W)$   $CP = 85\% * I_{ada}$  ;  $CP = 1.343A$

CP mode  
 $V_{aClim} = 2.39 * (20K / (20K + 38.3K)) = 0.8199V$   
 $I_{input} = (1 / 0.05) * (0.05 * V_{aClim}) / 2.39 + 0.05$   
 where  $V_{aClim} = 0.8199V$ ,  $I_{input} = 1.343A$

**CC=0.3~1.76A**  
**IREF=1.62\*Icharge**  
**IREF=0.486V~2.85V**  
**3.24V==>2A**

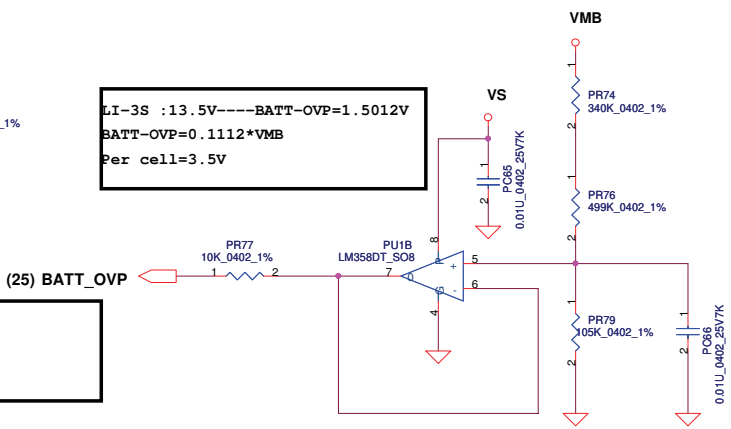
BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

(25) CALIBRATE#

CALIBRATE#	Pre Cell
H	4.35V
L	3.99V

VADJ-->VREF-->4.41V  
 VADJ-->Ground-->3.39V  
 $V_{cell} = (0.175 * VADJ) + 3.99$

LI-3S :13.5V---BATT-OVP=1.5012V  
 BATT-OVP=0.1112\*VMB  
 Per cell=3.5V

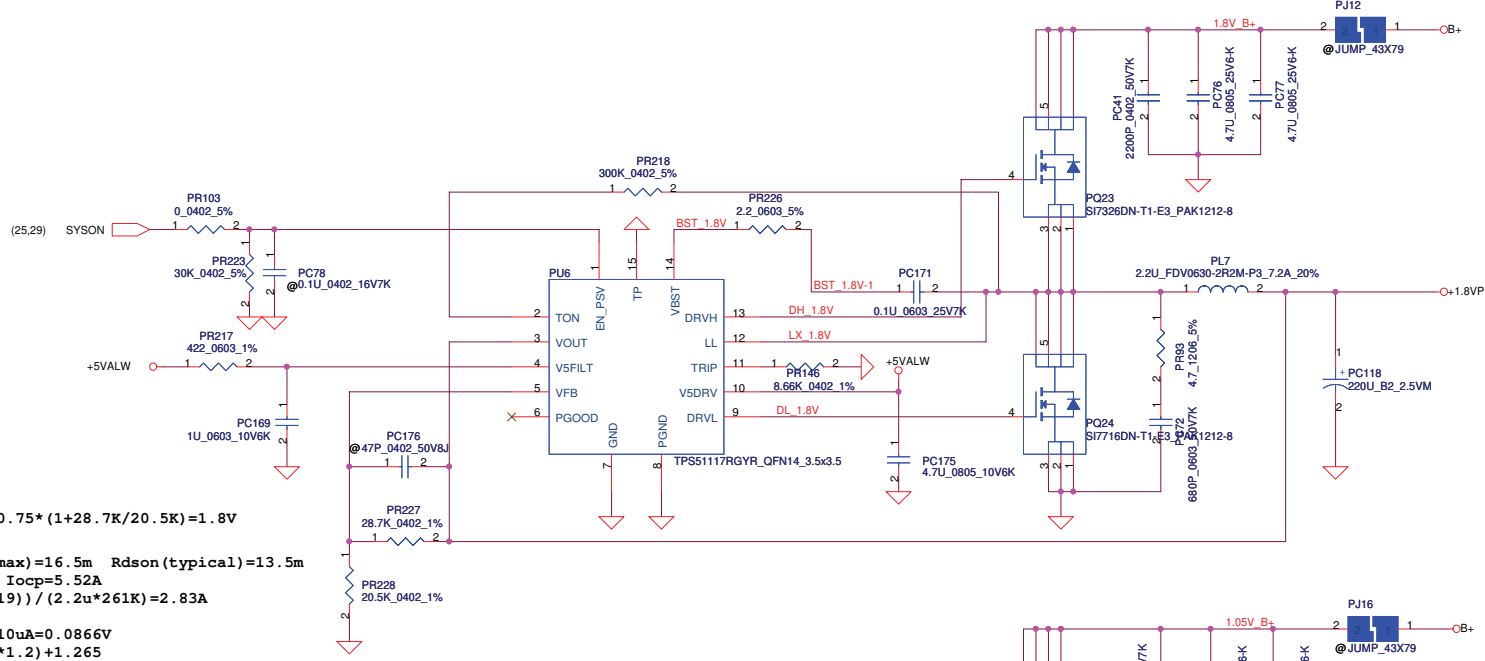


Charger ADJ	Calibrate#	PR211	PR220
4.2V	N/A	@	@
3.99V	L	301K	499K
4.35V	H	301K	499K

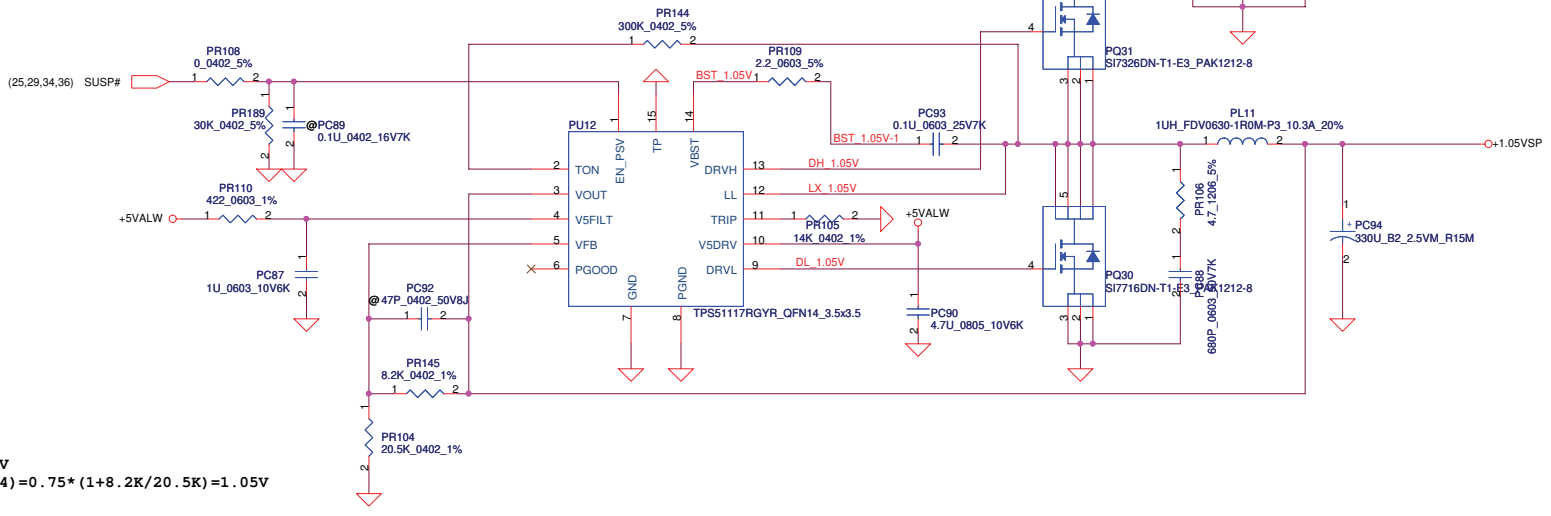
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CHARGER		
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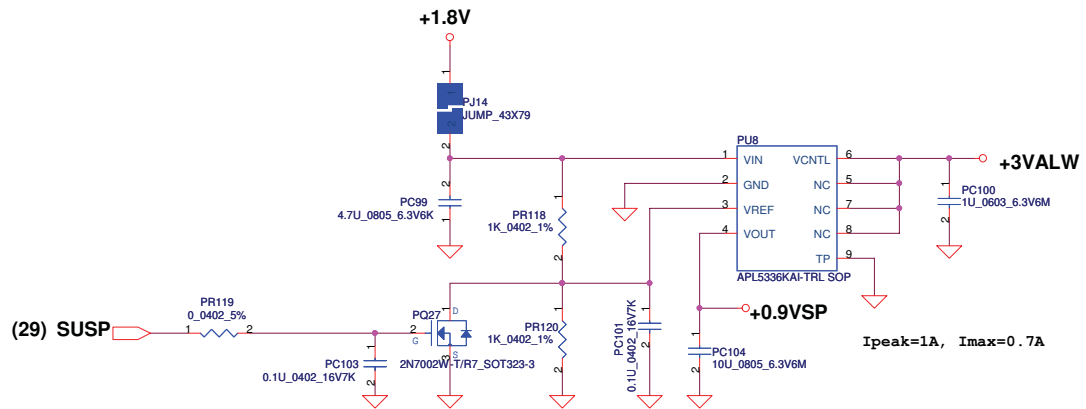
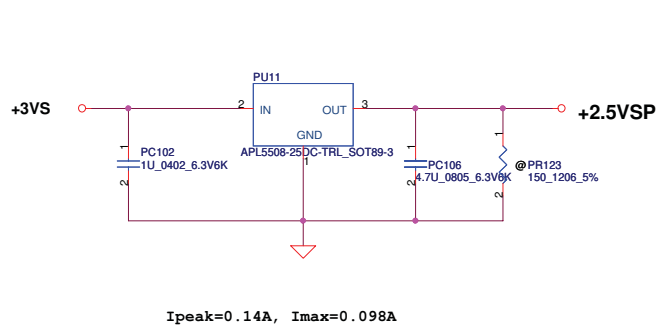
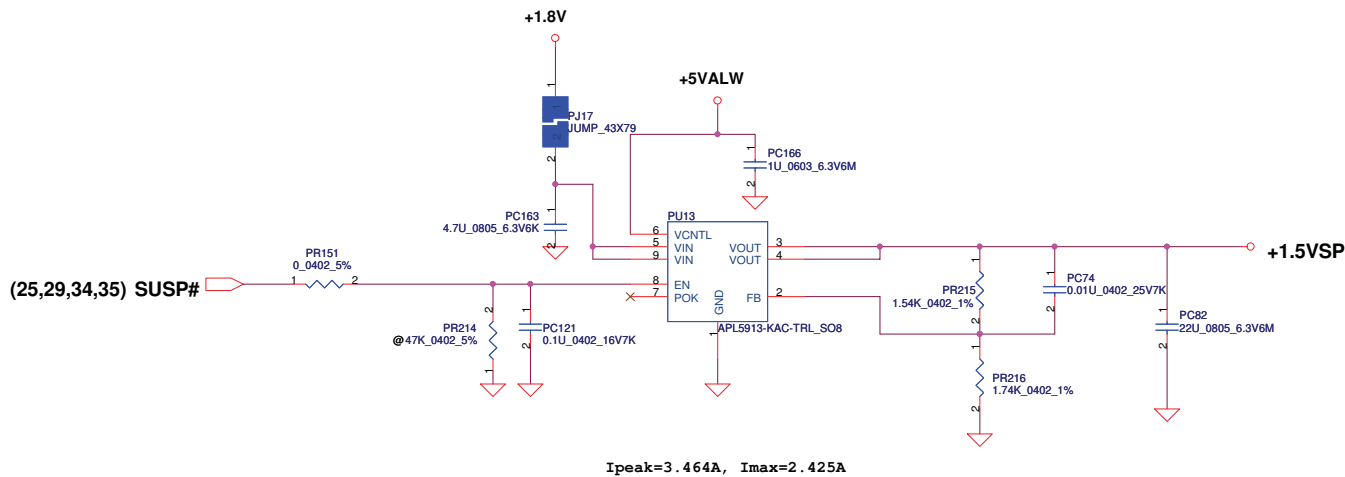


$V_o = 1.8V$      $V_{FB} = 0.75V$   
 $V_o = V_{FB} * (1 + PR227/PR228) = 0.75 * (1 + 28.7K/20.5K) = 1.8V$   
 $F_{sw} = 262KHz$   
 $C_{out} ESR = 15m\ \Omega$      $R_{dson(max)} = 16.5m\ \Omega$      $R_{dson(typical)} = 13.5m\ \Omega$   
 $I_{peak} = 4.6A$ ,     $I_{max} = 3.22A$ ,     $I_{ocp} = 5.52A$   
 $\Delta I = ((19 - 1.8) * (1.8/19)) / (2.2u * 261K) = 2.83A$   
 $\Rightarrow 1/2 \Delta I = 1.42A$   
 $V_{trip} = R_{trip} * I_{0uA} = 8.66K * 10uA = 0.0866V$   
 $I_{ocpmin} = V_{trip} / (R_{dsonmax} * 1.2) + 1.265$   
 $= 0.0866 / (0.0165 * 1.2) + 1.42 = 5.79A$   
 $I_{ocpmax} = (0.0866 / (0.0135 * 1.2)) + 1.42A = 6.77A$   
 $I_{ocp} = 5.79A \sim 6.77A$

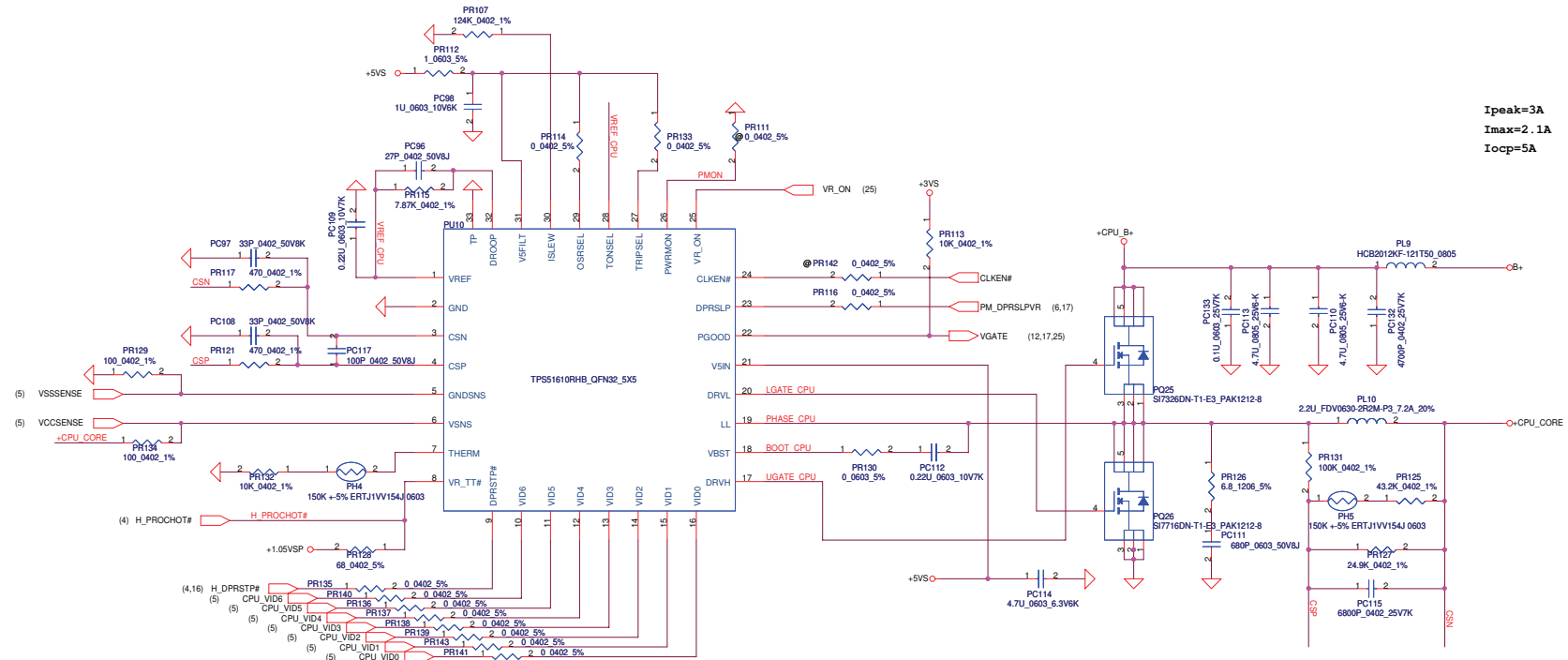


$V_o = 1.05V$      $V_{FB} = 0.75V$   
 $V_o = V_{FB} * (1 + PR145/PR104) = 0.75 * (1 + 8.2K/20.5K) = 1.05V$   
 $F_{sw} = 261KHz$   
 $C_{out} ESR = 15m\ \Omega$      $R_{dson(max)} = 16.5m\ \Omega$      $R_{dson(typical)} = 13.5m\ \Omega$   
 $I_{peak} = 7.09A$ ,     $I_{max} = 4.963A$ ,     $I_{ocp} = 8.51A$   
 $\Delta I = ((19 - 1.05) * (1.05/19)) / (1.5u * 261K) = 2.53A$   
 $\Rightarrow 1/2 \Delta I = 1.265A$   
 $V_{trip} = R_{trip} * I_{0uA} = 14K * 10uA = 0.14V$   
 $I_{ocpmin} = V_{trip} / (R_{dsonmax} * 1.2) + 1.265$   
 $= 0.14 / (0.0165 * 1.2) + 1.265 = 8.34A$   
 $I_{ocpmax} = (0.14 / (0.0135 * 1.2)) + 1.265A = 9.91A$   
 $I_{ocp} = 8.34A \sim 9.91A$

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Ipeak=3A  
 Imax=2.1A  
 Iocp=5A

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Modify CPU OTP circuit	For thermal team request	0.1	31	Change PR19 to SD034732180 (S RES 1/16W 7.32K +-1% 0402) Change PR22 to SD034174280 (S RES 1/16W 17.4K +-1% 0402)	09/01/14	DVT
2	Modify 3/5V output cap	design change	0.1	32	Change PC30 to SGA00004H00 (S POLY C 150U 6.3V M B2 LESR25M PSL H1.9) Change PC35 to SGA00004H00 (S POLY C 150U 6.3V M B2 LESR25M PSL H1.9)	09/01/14	DVT
3	Modify Charger modify	regulate charger ADJ voltage	0.1	33	add PR211 to SD034301380 (S RES 1/16W 301K +-1% 0402 ) add PR220 to SD034499380 (S RES 1/16W 499K +-1% 0402 )	09/01/14	DVT
4	Modify 1.8v/1.05v boost circuit	for APW7141 issue	0.1	34	Change PR226 to SD013220B80 (S RES 1/10W 2.2 +-5% 0603 ) Change PR109 to SD013220B80 (S RES 1/10W 2.2 +-5% 0603 )	09/01/14	DVT
5	add all sunbber	for 3G and EMI team request	0.1	34	add all sunbber	09/01/14	DVT
6	Modify HMOS and LMOS	for cost down	0.1	34	H-side to SB00000IA00 (S TR SIS412DN-T1-GE3 1N POWERPAK1212-8 ) L-side to SB00000I400 (S TR IRFH3707TRPBF 1N PQFN )	09/01/14	DVT
7	add input capacitance	for 3G solution	0.1	34	add PC41 PC46 SE074222K80 (S CER CAP 2200P 50V K X7R 0402)	09/01/21	DVT
8	modify 1.05v TRIP R	modify ocp point	0.1	34	modify PR105 to SD034140280 ( S RES 1/16W 14K +-1% 0402)	09/02/02	DVT
9	modify 3V/5V OCP point	design change	0.1	34	Change PR48 SD034255380 (S RES 1/16W 255K +-1% 0402 )	09/02/02	DVT
10	modify 3V/5V OCP point	design change	0.1	34	Change PR49 SD034226380 (S RES 1/16W 226K +-1% 0402)	09/02/18	PVT
11	modify chager circuit	design change	0.1	34	Add PQ44 SB000006800 S TR 2N7002W T/R7 1N SOT-323	09/02/18	PVT
12	modify chager circuit	design change	0.1	34	Add PQ34 SB301150000 S TR DTC115EUA NPN (UMT3)	09/02/18	PVT
13	modify chager circuit	design change	0.1	34	Add PR152 SD034470280 S RES 1/16W 47K +-1% 0402	09/02/18	PVT
14	modify chager circuit	design change	0.1	34	Add PQ33 SB101440200 S TR DTA144EUA PNP UMT3	09/02/18	PVT
15							
16							
17							
18							
19							
20							
21							
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23							

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A-TEST Change

- <8/25>
  - Update Power SCH
- <8/26>
  - Update Power SCH
  - Change
    - D7 SC30000D00 to SC30000000
- <8/27>
  - Update Power SCH
  - Modify
    - RJ45 temp footprint FOX\_JM3611A-R4122-7F\_12P-T
- <8/28>
  - Update Power SCH
- <9/1>
  - Update Screw
- <9/5>
  - SWAP USB20\_1 Signal.
- <9/10>
  - Remove Mini card pin55 .pin56 GND
  - Change JREAD1.42 H26 to GNDA
- <9/12>
  - Swap 3G ESD pin neme
- <9/15>
  - Update Audio Jack footprint
  - Change R641 - R642 300ohm to 511ohm for Arthros
  - Update L footprint
- <9/16>
  - Update POWER SCH.
- <9/17>
  - Update POWER SCH.
  - ADD R380 - R383 for ESD.
- <9/18>
  - Update ATHEROS 10/100 LAN <AR8132/AR8114>
- <9/24>
  - Change C870 0.1u to 1u.
- <9/26>
  - R88 change to 0ohm.

B-TEST Change

- <10/21>
  - Remove C389 for Audio can't detect issue on page 16
  - Add KSO1/KSO2 PU +3VALW on page25
  - Add R205 for schematic mistake on page 04
  - Change EC RST to PLTRST on page 25
  - Add J8 to cost down Audio LDO on page 20
  - Add R72 to reserve +3VALW for 3G on page 19
  - Reserve C238 for CRTDAC on page 10
  - Add R87 for Debug card on page 19
  - Change C108/C255 to 0.1uF for random hang issue
  - Change JP3 pin assignment on page 28
- <10/21>
  - Update Power SCH
- <10/29>
  - Audio AMP 10dB update to 6dB
- <11/3>
  - Update Power SCH
- <11/4>
  - Change R373 - R374 to 56.2 ohm for DA-HP FSOV
  - Add C834 C851 for 3G noise
  - Change KB926 C1 to D2
  - Card reader RT5158E change to RT5159-GR
- <11/5>
  - Swap D7 pin define
- <11/10>
  - EC add R79 - R90 R92 for SMS wakeup

A-TEST Change

- <2008/11/14>
  - change R28,R32 BOM structure on page 4
  - change LCD POWER CIRCUIT form KAW10 to JAQ10 on page 13
  - change C670 BOM structure on page 13
  - change L5,L19(BK61608LL121-T0603) to R281,R287(39\_0402) on page 14
  - change +CRT\_VCC to +5VS on page 14
  - del R244(100K\_0402) and add T17 on page 15
  - change J6 jump size form 43 x 118 to shortpads on page 16
  - change R204 BOM structure on page 16
  - change Q11 from SOT23 to SOT323-3 on page 17
  - change USB OC# circuit on page 17
  - Del R186(0\_0805\_5%) and +1.5VS DMIPLLR on page 18
  - CHANGE R62(0\_1206) to J9(43x39) on page 19
  - Del R83 R348 0\_0402 on page 19
  - Mobile EC\_TX,EC\_RX from WLAN to WWAN and add R96 on page 19
  - CHANGE R65,R70(0\_1206) to J10,J11(43x39) on page 19
  - change +UIM\_PWR\_1 to +UIM\_PWR on page 19
  - Del D16(DAN217T146\_SC59-3),R94,R408(0\_0402) on page 19
  - change +5VS to +3VS on page 19
  - change EC signal name form BT\_OFF# to BT\_ON# on page 19
  - del Q21 on page 19
  - ADD PMOS SOFT START on page 19

- <2008/11/16>
  - +VDDA CHANGE TO +5VS on page 20
  - Analog ground change to digital ground on page 20
  - Del L22 on page 20
  - DEL R383 R382 R384 GNDA & GND on page 20
  - change R380,R379,R381 form 0805 to 0603 page 20
  - Add R94,R87 Vender suggesttion on page 21
  - Analog ground change to digital ground on page 21
  - reserve C5,C6,C883,C884 on page 22
  - reserve +3VALW on page 22
  - change +3VS to +CAM\_VCC on page 22
  - change R651,R634 form (0\_0603) to 43 x 39 jump on page 23
  - add net name +3VS\_READER on page 23
  - add net name AV\_PLL on page 23
  - add net name VREG on page 23
  - +3VS change to +3VS\_READER on page 23
  - change R619 BOM structure on page 23
  - add net name RREF on page 23
  - del R623(0\_0402) on page 23
  - Chang C855 form 4.7U to 10U on page 24 vendor suggest
  - Chang C846 form 4.7U to 10U on page 24 vendor suggest
  - change BJT form MMJT9435T1G to MBT35200 on page 24
  - change EC signal name form BT\_OFF# to BT\_ON# on page 25
  - change D12,R103,R104 BOM structure on page 25
  - change J1,J3(43 x 79) to R186,R193(0\_0805) on page 26
  - change Q3 from 2N70002\_SOT23 to 2N7002W-T/R7\_SOT323-3 on page 26
  - change Q1 form 2N70002\_SOT23 to 2N7002W-T/R7\_SOT323-3 on page 26
  - change net name form WWAN\_LED# to WWAN\_LED\_R# on page 28
  - change R130 BOM structure on page 28
  - change JP3 pin assignment on page 28
  - change Q2,Q15,Q24,Q7,Q23 form 2N70002\_SOT23 to 2N7002W-T/R7\_SOT323-3 on P29
  - change R18,R169,R280,R61,R279,Q2,Q15,Q24,Q7,Q23 BOM structure on age 29
  - +5VALW CHANG TO VL on page 29

- <2008/11/17>
  - update POW SCH
  - change DIMMA from H5.2 to H4 on page 11
  - change +3VS to +5VS on page 14
  - change J9,J10,J11 from 43x39 to 43x79 on page 19
  - change R563,Q31 BOM structure on page 13
  - del +3VALW on page 22
  - del +1.5VS,+VCCP,+0.9VS,+1.8V Discharge path R18,R280,R61,R279 Q2,Q24,Q7,Q23 on page 29
  - change R24 BOM structure on page 17
  - del R253 on page 19
  - change L14 to R382 on page 25

- <2008/11/17>
  - ADD WWAN\_WAKEUP# ON pin 45 on page 19
  - DEL R79 ,R92 and change net name to WWAN\_WAKEUP# on page 25
  - DEL R90 and WWAN\_LED\_R# on pin 85 on page 25
  - change net name form WWAN\_LED\_R# to WWAN\_LED# on page 28

- <2008/11/18>
  - Place R282,R296 close to F27,D27 on page 8
  - Del R93 R407(0\_0402) on page 19
  - Move R204 from F16 to P25
  - Move R24 from P17 to P25
  - change Q10A,Q10B to 0 ohm on page 12
  - del pull up resistance (R112,R108) on page 12
  - change C883 from 4.7u to 10u on page 22

- <2008/11/20>
  - change R112,R108,Q10A,Q10B BOM structure on page 12
  - add R149,R150 on page 12
  - add pull up resistance R292 on page 19
  - del R66(0\_0402),R67(10K\_0402) on page 25
  - restore R563,Q31 BOM structure on page 13
  - change D25 BOM structure on page 20

- <2008/11/21>
  - Change +3VS to +3VALW on page 19
  - del R204 on page 25
  - del R143 and CLK\_SD\_48M on page 12
  - Change R137 from 12 ohm to 33 ohm on page 12
  - Move Card Reader to small board on page 23
  - Move SATA HDD Conn to small board on page 22
  - ADD JP7 on page 22
  - change JP2 from 6 pin to 8 pin on page 26
  - DEL LID Switch on page 26

- <2008/11/24>
  - return the H5.2 footprint on page 11

- <2008/11/25>
  - add add R90 on page 19
  - change JMIN1 Conn printfoot on page 19
  - change JP2 Conn on page 26
  - change JP13 Conn on page 28
  - update power SCH

- <2008/11/26>
  - change JP20 Conn and pin design on page 21
  - change JBT1 form 8 pin to 4 pin on page 19
  - del JP1 on page 13
  - SWAP JP12 on page 27
  - change JLVDS1 Conn form 20 pin to 30 pin on page 13
  - Del JP4 on page 20
  - combine the DMIC Conn and Camera Conn on page 13
  - add U7 on page 28
  - del JP3 on page 28
  - ADD SATA&CARDREADER&USB Conn(JP7) on page 22
  - update Power SCH
  - change C233 BOM structure on page 19
  - change JRJ45 Conn on page 24

- <2008/11/28>
  - update Power SCH

- <2008/12/01>
  - chang JP2 Conn on page 26
  - update Power SCH

- <2008/12/02>
  - SWAP JLVDS1 on page 13
  - del C843,C844 on page 24
  - change C847 from 0.1u to 1u on page 24
  - change C873 from 0.1u to 1u on page 24
  - move R441,R438 form P13 to P20 on page 20
  - change +5VAMP to +5VS on page 21
  - R2,R4,R518 close to EC on page 26
  - R1 close to Q3 on page 26

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Revaif@hotmail.com

<2008/12/03>  
 1. SWAP JP7 pin define on page 22  
 2. change PJP2 connector on page 32

<2008/12/04>  
 1. update Screw on page 30  
 2. change JCR71 Conn to SP010811273 on page 14  
 3. SWAP PJP2 pin define on page 32  
 4. add J12 on page 21

<2008/12/05>  
 1. del D8 and change D5 P/N on page 28  
 2. SWAP D2 pin define on page 13  
 3. change JBT1 Conn on page 19  
 4. update POWER SCH

<2008/12/08>  
 1. add J15 J16 on page 22  
 2. return D2 pin define on page 13  
 3. change JUSB1 Conn on page 28  
 4. swap JP6 pin define on page 27  
 5. add C32,C33,C42 for keypart on page 12  
 6. add C5 for keypart on page 13  
 7. add C9 for keypart on page 16  
 8. add C11,C21,C26,C27 for keypart on page 22

<2008/12/10>  
 1. del H11 H\_3P0N on page 30  
 2. Change to SA00002CI10 to SA00002CI20  
 S IC ALC272X-GR LQFP 48P CODEC on page 20  
 3. add net name(+VCCP\_D) 20mil on page 10  
 4. SWAP D29 Pin Define on page 28  
 5. change R185 from 200K to 33K on page 29  
 6. change R68 from 200K to 22K on page 29

<2008/12/11>  
 1. change H17 from H\_2P5 to H\_2P5x4P4 on page 30  
 2. del R388,R387,R386,R385,D10,D13 on page 21  
 3. update Power SCH  
 4. +5VS change to +5VALW on page 21

<2008/12/14>  
 1. Del R129 on page 12  
 2. add C45 for keypart on page 12  
 3. del R76 on page 25

<2008/12/15>  
 1. change R137 BOM structure and add R143 on page 12  
 2. change C852,C853,Y5 BOM structure on page 24  
 3. add C55 on page 24  
 4. change C842 BOM structure on page 24  
 5. del J15,J16,C21 on page 22  
 6. add net name BATT\_AMB\_LED# BATT\_GRN\_LED# on page 22  
 7. +3VS\_READER change to +3VALW on page 22

<2008/12/16>  
 1. del R143 on page 12  
 2. del C55 on page 24  
 3. swap CLK\_PCIE\_CARD and CLK\_PCIE\_CARD# on page 27

<2008/12/17>  
 1. modify H15,H19,H20,H29,H30 on page 30  
 2. add H32 on page 30  
 3. +5VALW change to +3VALW on page 26

<2008/12/18>  
 1. add R102 on page 19

<2008/12/19>  
 1. change R284 from 453 ohm to 150 ohm R286 from 300 ohm to 120 ohm on page 26  
 2. change R132 P/N to SA000033N00 on page 40

<2008/12/22>  
 1. change D1 BOM structure on page 26  
 2. change C116 form 1U to 4.7U on page 25  
 3. change R24 from 10k to 47K R103 from 0 to 2.2K on page 25  
 4. change D12,R104 BOM structure on page 25  
 5. change L30,C856,C857 BOM structure on page 24  
 6. change D17 P/N from SCA00000700 to SCA00000A00 and BOM structure on page 13  
 7. change D2 P/N from SC300000000 to SC300000B00 and BOM structure on page 13  
 8. change D3,D4 P/N from SCA00000G00 to SCA00000A00 and BOM structure on page 14  
 9. change D33 P/N from SC10T24C000 to SCA00000A00 and BOM structure on page 26  
 10. change D18 P/N from SC10T24C010 to SCA00000A00 and BOM structure on page 27  
 11. change D9 P/N from SC10T24C010 to SCA00000A00 and BOM structure on page 27  
 12. change D29 P/N from SC300000000 to SC300000B00 and BOM structure on page 28

<2008/12/24>  
 1. change C32 C33 C42 C45 BOM structure on page 12  
 2. change C117 BOM structure on page 25  
 3. change R88 from 0 ohm to 22 ohm on page 25  
 4. U2 Change to SA000033H00 on page 28  
 5. U7 Change to SA000033H00 on page 28

**Pre C-TEST Change**

<2008/12/29>  
 1. change R141,R140,R147,R81,R91 R82,R97,R95,R98 BOM structure on page 12  
 2. Change R130 from 200K to 100K and change BOM structure on page 28  
 3. change D5 BOM structure on page 28

<2008/12/231>  
 1. change R371 from 0 ohm to 22 ohm on page 20  
 2. U3 Change to SA000035G00 on page 28

**Memo control**

<2008/12/31>  
 1. del C9 on page 16  
 2. add C21 for keypart on page 16  
 3. change R644 from 0603 to 0805 on page 24  
 4. change R643 from 0603 to 0402 on page 24  
 5. change C841 from 0603 to 0402 on page 24  
 6. change L29,L30 from 0805 to 0603 on page 24  
 7. del R637 R638 on page 24

<2009/01/13>  
 1. SWAP JP11 on page 27  
 2. change SW4 P/N to SN111005800 on page 26  
 3. ADD C160 on page 24  
 4. change JMINI Conn footprint on page 19  
 5. Change PWR\_LED and PWR\_SUSP\_LED# Net name on page 26  
 6. Change C231 P/N to SGA00001E00 on page 28

<2009/01/14>  
 1. add R660 pull up +3VALW on page 25  
 2. change R120 and R126 to PVT ID on page 25  
 3. update Screr  
 4. add C28 for keypart on page 22

<2009/01/16>  
 1. del H31 on page 30  
 2. change JP20 Conn on page 21  
 3. del D29,L9,R144,R136 on page 28

<2009/01/17>  
 1. Del R110,R119 on page 12  
 2. change R141,R140,R147,R81,R91,R82,R97,R95,R98 BOM structure on page 12

<2009/01/20>  
 1. add JDIMI pin 200 and pin 201 to GND on page 11  
 2. JMINI1 pin 55,56 change to non-GND on page 19  
 3. SWAP JP20 on page 21  
 4. change H18 to non-GND on page 30  
 5. Chang C160 from 0603(4.7u) to 0402(2.2u) on page 24

<2009/01/21 Ivan>  
 1. change R441 from 0ohm/0603 to 33ohm/0402  
 2. change C459 from 0.01uF/0402 to 4.7uF/0603  
 3. change R438 from 0ohm/0603 to 0ohm/0402

<2009/01/21-1>  
 1. change U26 BOM structure on page 20 memo  
 2. del C11,C28,C26 on page 22  
 3. Update Power SCH

<2009/01/22>  
 1. update H15,H19,H20,H30 from 3P8 to 3P6 01/22

<2009/01/22-1>  
 1. del C94 C95 on page 11  
 2. add C164,C165 01/22  
 3. move C159 from page 11 to page 12  
 4. add R383 on page 20

<2009/01/22-2>  
 1. change C396 from 10U/0806 to 4.7U/0603 on page 28  
 2. add C469 on page 28

<2009/01/22-3>  
 1. add C268 01/22

<2009/01/23>  
 1. change C249 BOM structure(0) on page 10  
 2. change C603 from 220P to 100P on page 13  
 3. change C21 from 10p to 22p on page 16  
 4. change C459 from 4.7uF to 1uF on page 20  
 5. change R371,C470 BOM structure(0) on page 20  
 6. change C604 from 220P to 18P on page 20  
 7. change R122,R123,R124,R125 from 4.7K to 2.2K on page 25  
 8. change R284 from 150 ohm to 300 ohm R286 from 120 ohm to 100 ohm on page 26  
 9. change D5 BOM structure(0) on page 28  
 10. change C162 from 27P to 22P on page 12  
 11. change C852,C853 from 27p to 15p on page 24  
 12. change C49 C50 from 18pf to 10pf on page 16  
 13. change c150,c123 from 15p to 22p on page 25

<2009/01/23-1>  
 1. change C42,C45 from 10p to 22p on page 12  
 2. R115,R121 from 33 ohm to 39 ohm on page 12  
 3. change C603 from 100P to 47P on page 13  
 4. change R441 from 33 ohm to 39 ohm on page 20  
 5. change C604 Bom structure(0) on page 20

**C-TEST Change**

<2009/02/03>  
 1. Add R105,R106 on page 19  
 2. ADD BATT\_GRN\_LED\_1# and BATT\_AMP\_LED\_1# on page 25  
 3. add R651 O\_0402 on page 24

<2009/02/04>  
 1. add R279,R280,R294,R295 on page 17  
 2. del C26 on page 22  
 3. change C841 from 0402 1U to 0603 1U on page 24

<2009/02/05>  
 1. Del J10,J11 and add R65,R66 on page 19

<2009/02/06>  
 1. change C226 BOM structure on page 19  
 2. Change U3 from SA000035G00 to SA000022J00 on page 28  
 3. change L13 from SM01000AL00 to SM010004010 on page 25  
 4. change L23 from SM010032020 to SM010004010 on page 20  
 5. change U26,C459 BOM structure(0) on page 20  
 6. change R1,R2,R4 from 300 to 200 ohm on page 26  
 7. change R518 from 300 to 422 ohm on page 26  
 8. change R137 from 33 to 39 ohm on page 12  
 9. change C32 from 10P to 15p ohm on page 12  
 10. change C42,C45 from 22p to 15p on page 12  
 11. change R115,R121 from 39 ohm to 47 ohm on page 12

**Pre C memo**

<2009/02/18>  
 1. change R279,R280,R294,R295 BOM structure on page 17  
 2. change U26,C459 BOM structure on page 20  
 3. change L13 from SM010004010 to SM010032020 on page 25  
 4. change L23,L24 from SM010004010 to SM010032020 on page 20

**Pre MP-TEST Change**

<2009/02/18>  
 1. Del J6 and add R219 on page 16  
 2. Del C249 on page 10  
 3. change LED2 BOM structure on page 26

<2009/02/20>  
 1. update Power SCH  
 2. del L8,R145,R146 on page 13

<2009/02/22>  
 1. update H15,H19,H20,H30 from 3P6 to 3P3 on page 30  
 2. change H18 from 3P2N to 3P1N on page 30  
 3. add R107,R110 on page 19

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