

Page	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20
Rev.	A.0	A.0	A.0	A.0	A.0	A.0	A.0	A.0	A.0	A.0	A.0	A.0	A.0	A.0	A.0	A.0	A.0	A.0	A.0	A.0
Data	2005/07/11	2005/07/11	2005/07/11	2005/07/11	2005/07/11	2005/07/11	2005/07/11	2005/07/11	2005/07/11	2005/07/11	2005/07/11	2005/07/11	2005/07/11	2005/07/11	2005/07/11	2005/07/11	2005/07/11	2005/07/11	2005/07/11	2005/07/11

Page	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37
Rev.	A.0	A.0	A.0	A.0	A.0	A.0	A.0	A.0	A.0	A.0	A.0	A.0	A.0	A.0	A.0	A.0	A.0
Data	2005/07/11	2005/07/11	2005/07/11	2005/07/11	2005/07/11	2005/07/11	2005/07/11	2005/07/11	2005/07/11	2005/07/11	2005/07/11	2005/07/11	2005/07/11	2005/07/11	2005/07/11	2005/07/11	2005/07/11

Voltage Rails	ON S0-S1	ON S3	ON S4	ON S5	Control signal
12VOUT	X	X	X	X	
3V_591	X	X	X	X	
5VPCU	X	X	X	X	
+3V_S5	X	X	X	X	S5_ON
+1.5V_S5	X	X	X	X	S5_ON
+1.8VSUS	X	X			SUSON
+3VSUS	X	X			SUSON
+5VSUS	X	X			SUSON
+0.9VSUS	X	X			SUSON
CPU_CORE	X	X			VR_ON
+0.9V	X				MAINON
+VCCP	X				MAINON
+1.5V	X				MAINON
+1.8V	X				MAINON
+2.5V	X				MAINON
+3V	X				MAINON
+5V	X				MAINON
+12V	X				MAINON

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
Giga LAN	AD22	0	B
Mini-PCI	AD23	1	C, D
CardBus+1394	AD24	2	E, F, G

EC SM Bus1 address

Device

Smart Battery
THERMAL SENSOR 1001 100X b

SB450MB SM Bus address

Device

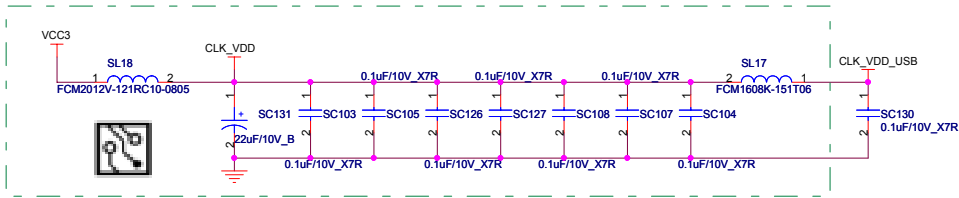
SODIMM 1010 000X b
Clock Gen 1101 001x b

Functions with Spread Spectrum Capability for Clock

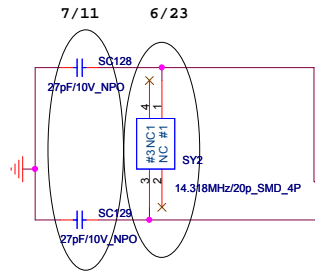
Memory
LVDS
Host Bus
PCIE Interface

Elitegroup Computer Systems

Title			
SYSTEM INFO			
Size	Document Number	Rev	Rev
Custom	400-1-4-01	A.0	A.0
Date:	Monday, July 11, 2005	Sheet	2 of 35



- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE AS U300 AS POSSIBLE
- 2- ROUTE ALL CPUCCLK/#, NBCLK/# AND ITPCLK/# AS DIFFERENT PAIR RULE
- 3- PUT DECOUPLING CAPS CLOSE TO U300 POWER PIN



From uP--> 14 CLKEN# 16.33 CPUSTP#

11,12,17 SCLK SDATA

$$I_{REF} = VDD / (3 \times RR)$$

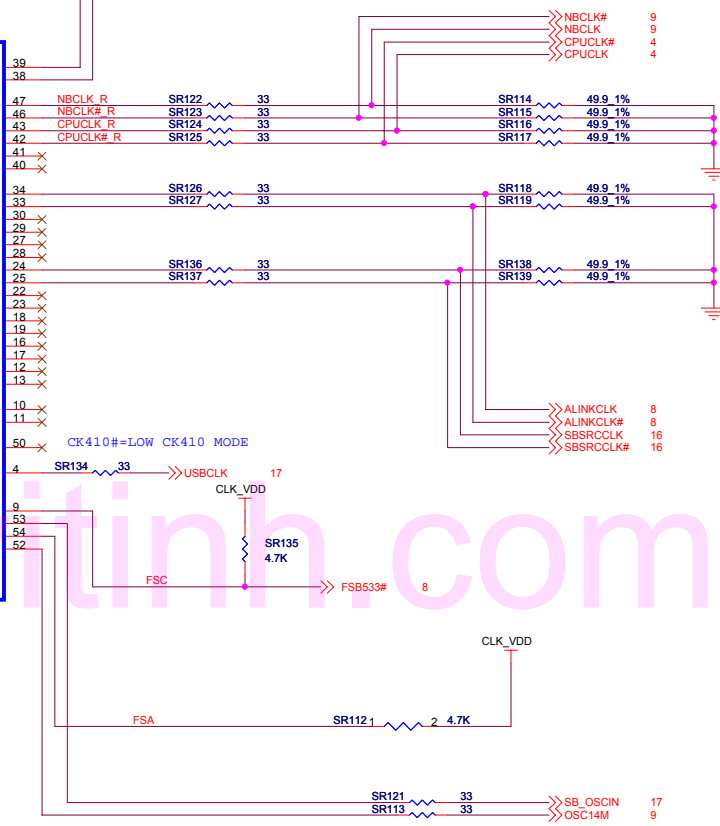
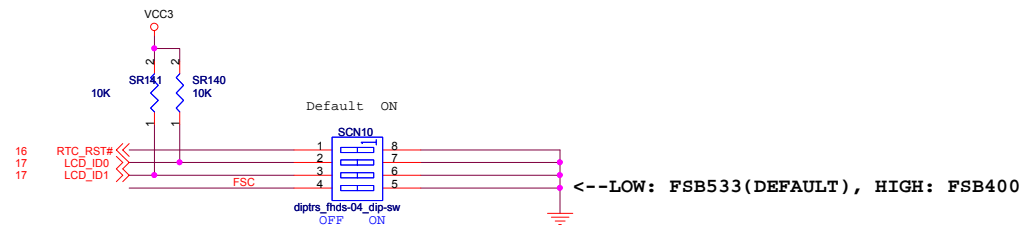
$I_{oh} = 6 \cdot I_{ref}$
 (2.32mA)
 $V_{oh} = 0.7V @ 50 ohm$

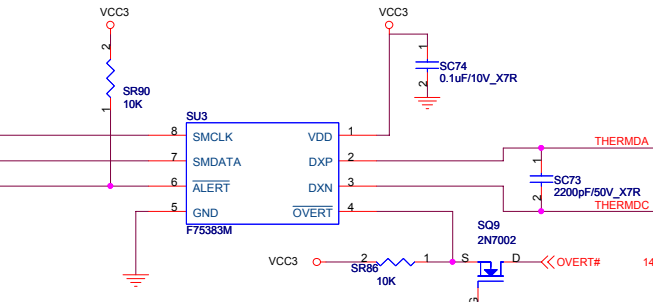
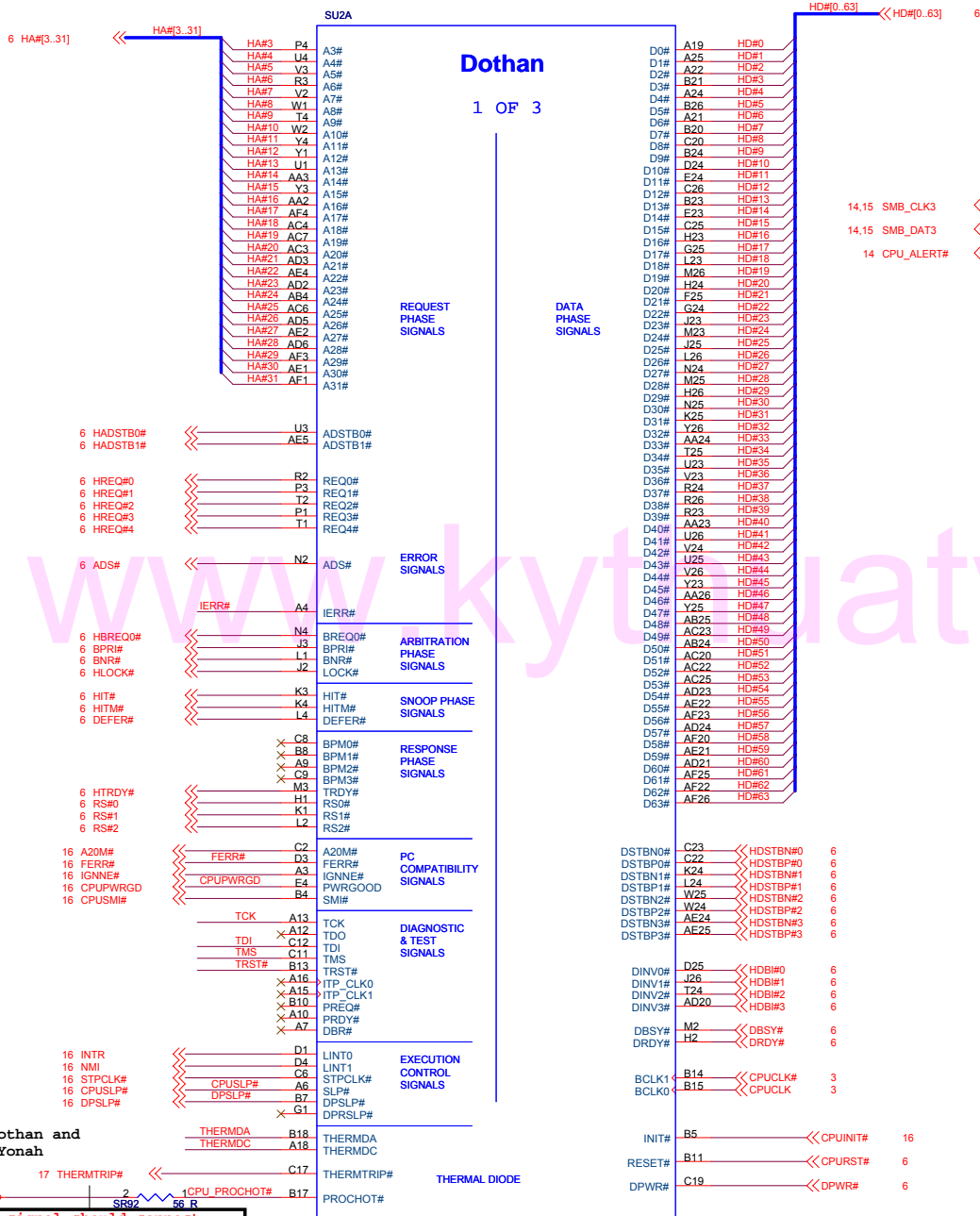
ICS951413/RTM851

CK410 FREQUENCY SELECT TABLE(MHZ)

FSC	FSB	FSA	CPU	SRC	PCI	REF
BSEL2	BSEL1	BSEL0				
1	0	1	100	100	33	14.31
0	0	1	133	100	33	14.31
0	1	1	166	100	33	14.31
0	1	0	200	100	33	14.31
0	0	0	266	100	33	14.31
1	0	0	333	100	33	14.31
1	1	0	400	100	33	14.31
1	1	1	Resv	100	33	14.31

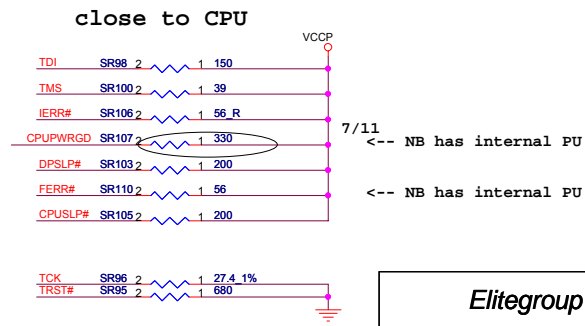
Check if needed in next version -->





Slave Addresses=1001100

Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm +/- 5%	VTT	Within 2.0" of the CPU
TMS	39 ohm +/- 5%	VTT	Within 2.0" of the CPU
TRST#	680 ohm +/- 5%	GND	Within 2.0" of the CPU
TCK	27 ohm +/- 5%	GND	Within 2.0" of the CPU
TDO	Open	NC	Within 2.0" of the CPU

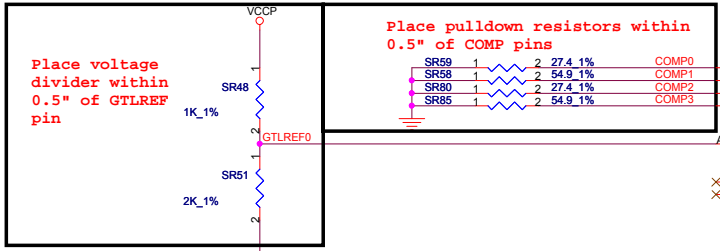


The signal should connect to SB and NB w/o T-ing (No stub)

Elitegroup Computer Systems

Dothan (HOST BUS)

File: _____
 Size: _____ Document Number: **400-1-4-01** Rev: A.0
 Date: Monday, July 11, 2005 Sheet 4 of 35



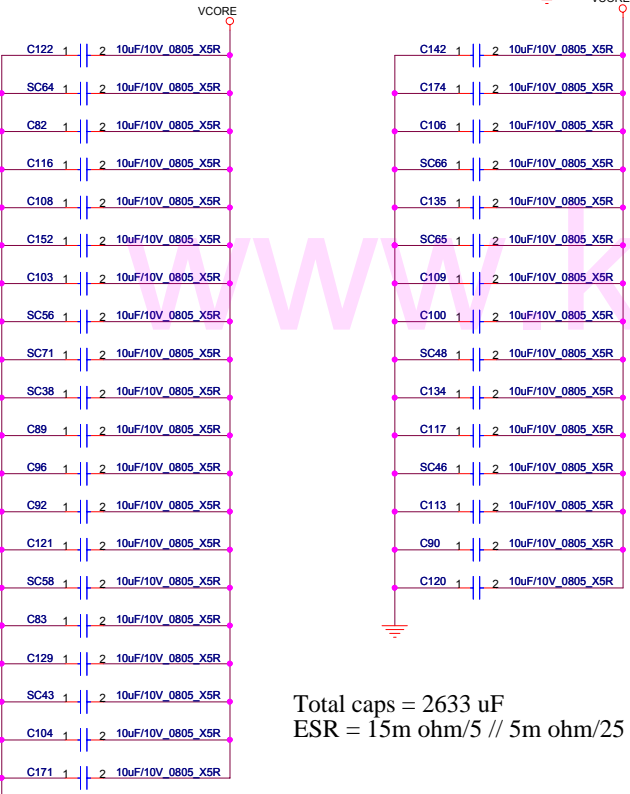
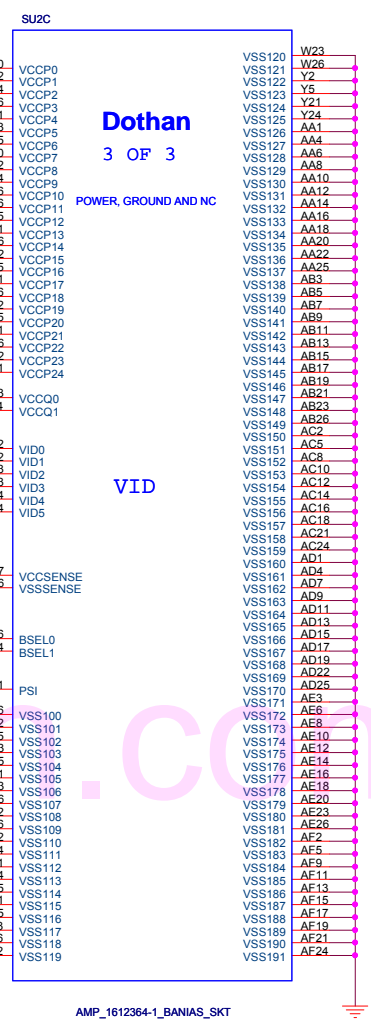
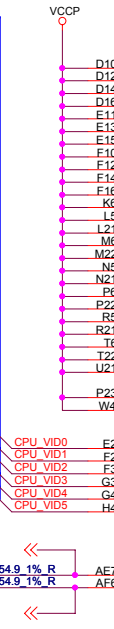
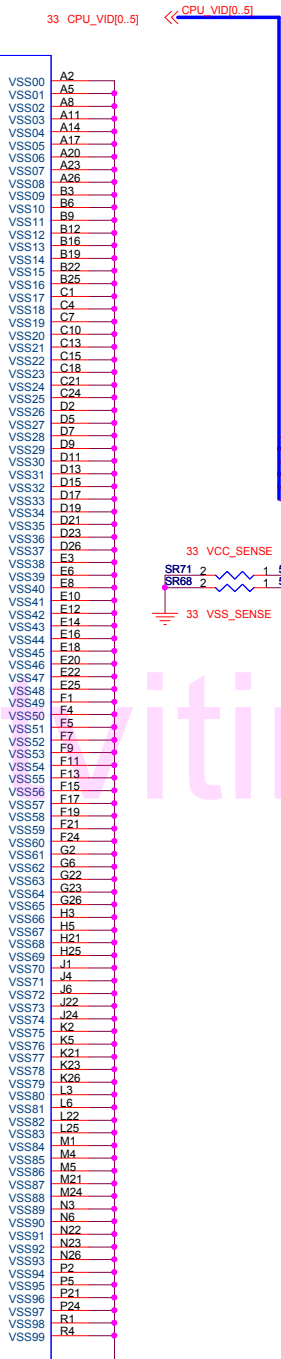
Place pulldown resistors within 0.5" of COMP pins

SR59	1	2	27.4 1%	COMP0	P25
SR58	1	2	54.9 1%	COMP1	P26
SR80	1	2	27.4 1%	COMP2	AB2
SR85	1	2	54.9 1%	COMP3	AB1

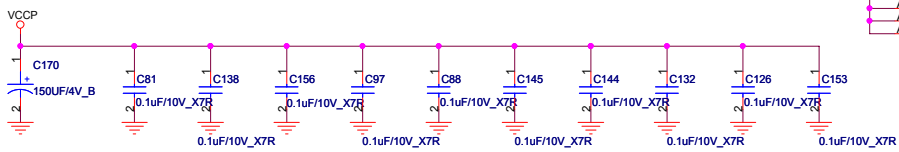
Dothan
2 OF 3

POWER, GROUND, RESERVED SIGNALS

- AD26 GTLREF0
- C5 TEST1
- F23 TEST2
- C3 RSV2D2
- AF7 RSV2D3
- AC1 RSV2D4
- E26 RSV2D5
- AC26 VCCA3
- N1 VCCA2
- B1 VCCA1
- F26 VCCA0
- D6 VCC00
- D8 VCC01
- D18 VCC02
- D20 VCC03
- D22 VCC04
- E5 VCC05
- E7 VCC06
- VCS07
- E17 VCC08
- E19 VCC09
- E21 VCC10
- F6 VCC11
- F8 VCC12
- F18 VCC13
- F20 VCC14
- F22 VCC15
- G21 VCC16
- VCS17
- H6 VCC18
- H22 VCC19
- J5 VCC20
- K22 VCC21
- U5 VCC23
- V6 VCC24
- V22 VCC25
- W5 VCC26
- W21 VCC27
- Y6 VCC28
- Y22 VCC29
- AA5 VCC30
- AA7 VCC31
- AA9 VCC32
- AA11 VCC33
- AA13 VCC34
- AA15 VCC35
- AA17 VCC36
- AA19 VCC37
- AA21 VCC38
- AB6 VCC39
- AB8 VCC40
- AB10 VCC41
- AB12 VCC42
- AB14 VCC43
- AB16 VCC44
- AB18 VCC45
- AB20 VCC46
- AC9 VCC47
- AC9 VCC48
- AC11 VCC49
- AC13 VCC50
- AC15 VCC51
- AC17 VCC52
- AC19 VCC53
- AD8 VCC54
- AD10 VCC55
- AD12 VCC56
- AD14 VCC57
- AD16 VCC58
- AD18 VCC59
- AE9 VCC60
- AE11 VCC61
- AE13 VCC62
- AE15 VCC63
- AE17 VCC64
- AE19 VCC65
- AF8 VCC66
- AF10 VCC67
- AF12 VCC68
- AF14 VCC69
- AF16 VCC70
- AF18 VCC71
- VSS00 A2
- VSS01 A5
- VSS02 A8
- VSS03 A11
- VSS04 A17
- VSS05 A20
- VSS06 A23
- VSS07 A26
- VSS08 B3
- VSS09 B6
- VSS10 B9
- VSS12 B12
- VSS13 B16
- VSS14 B19
- VSS16 B22
- VSS16 B25
- VSS17 C1
- VSS18 C4
- VSS18 C7
- VSS19 C10
- VSS20 C13
- VSS20 C15
- VSS22 C18
- VSS23 C21
- VSS24 C24
- VSS25 D2
- VSS27 D5
- VSS28 D9
- VSS29 D11
- VSS30 D13
- VSS31 D15
- VSS32 D17
- VSS33 D19
- VSS34 D21
- VSS35 D23
- VSS37 D26
- VSS38 E3
- VSS39 E6
- VSS40 E8
- VSS41 E10
- VSS42 E12
- VSS43 E14
- VSS44 E18
- VSS44 E20
- VSS46 E22
- VSS47 E25
- VSS48 F1
- VSS49 F4
- VSS51 F5
- VSS52 F7
- VSS53 F9
- VSS53 F11
- VSS54 F13
- VSS55 F15
- VSS56 F17
- VSS57 F19
- VSS58 F21
- VSS59 F24
- VSS60 F24
- VSS61 G2
- VSS62 G6
- VSS63 G23
- VSS64 G26
- VSS65 G26
- VSS66 H3
- VSS67 H6
- VSS68 H21
- VSS69 H25
- VSS70 J1
- VSS71 J4
- VSS72 J8
- VSS73 J22
- VSS74 J24
- VSS75 K2
- VSS76 K5
- VSS77 K21
- VSS78 K23
- VSS78 K26
- VSS79 L3
- VSS81 L6
- VSS82 L22
- VSS82 L25
- VSS83 M1
- VSS84 M4
- VSS85 M5
- VSS86 M21
- VSS87 M24
- VSS88 N3
- VSS89 N6
- VSS90 N6
- VSS91 N22
- VSS92 N23
- VSS93 N26
- VSS94 P2
- VSS95 P5
- VSS96 P21
- VSS97 P24
- VSS98 R1
- VSS99 R4



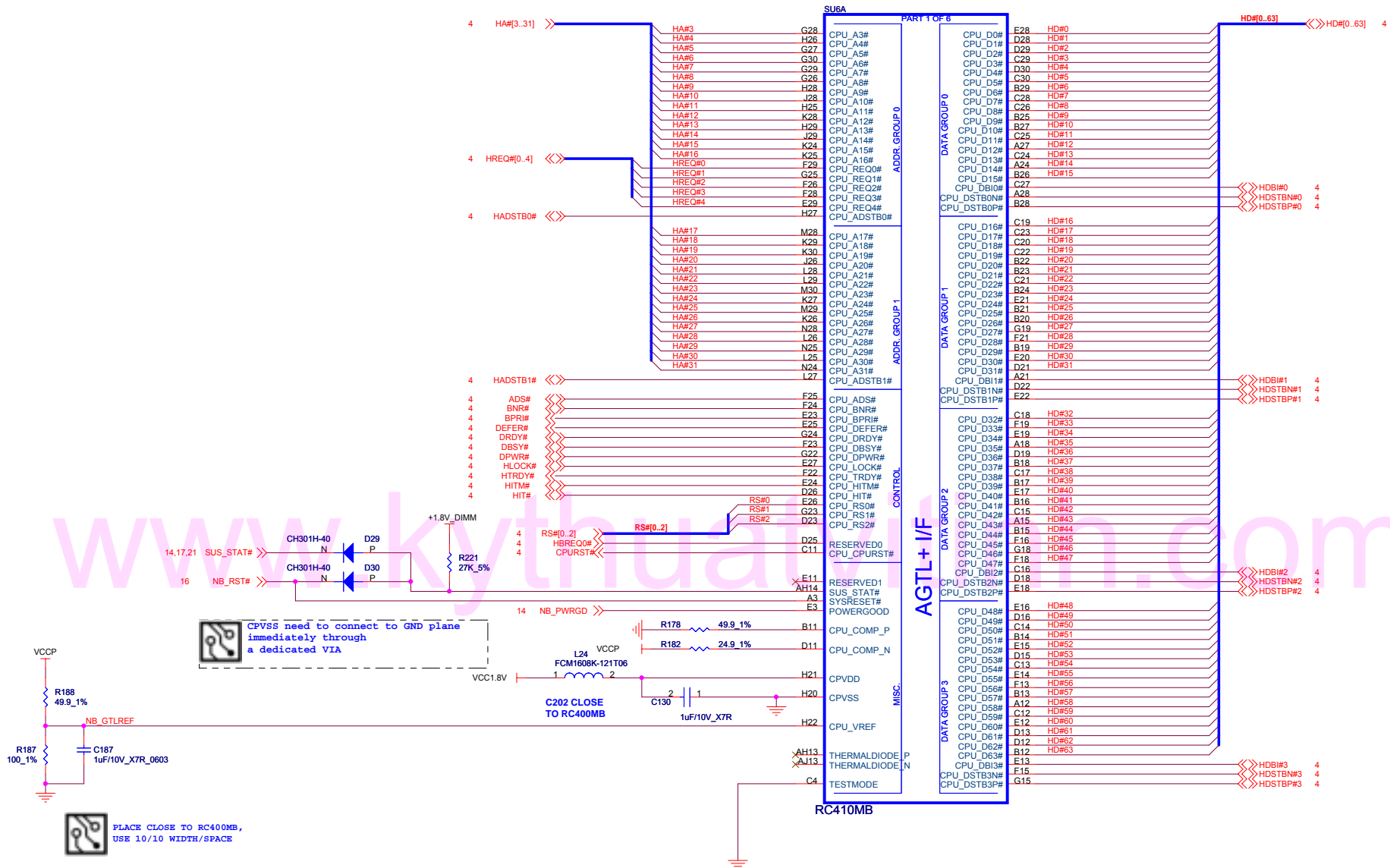
Total caps = 2633 uF
ESR = 15m ohm/5 // 5m ohm/25 // 5m ohm/15



AMP_1612364-1_BANIAS_SKT

Elitegroup Computer Systems

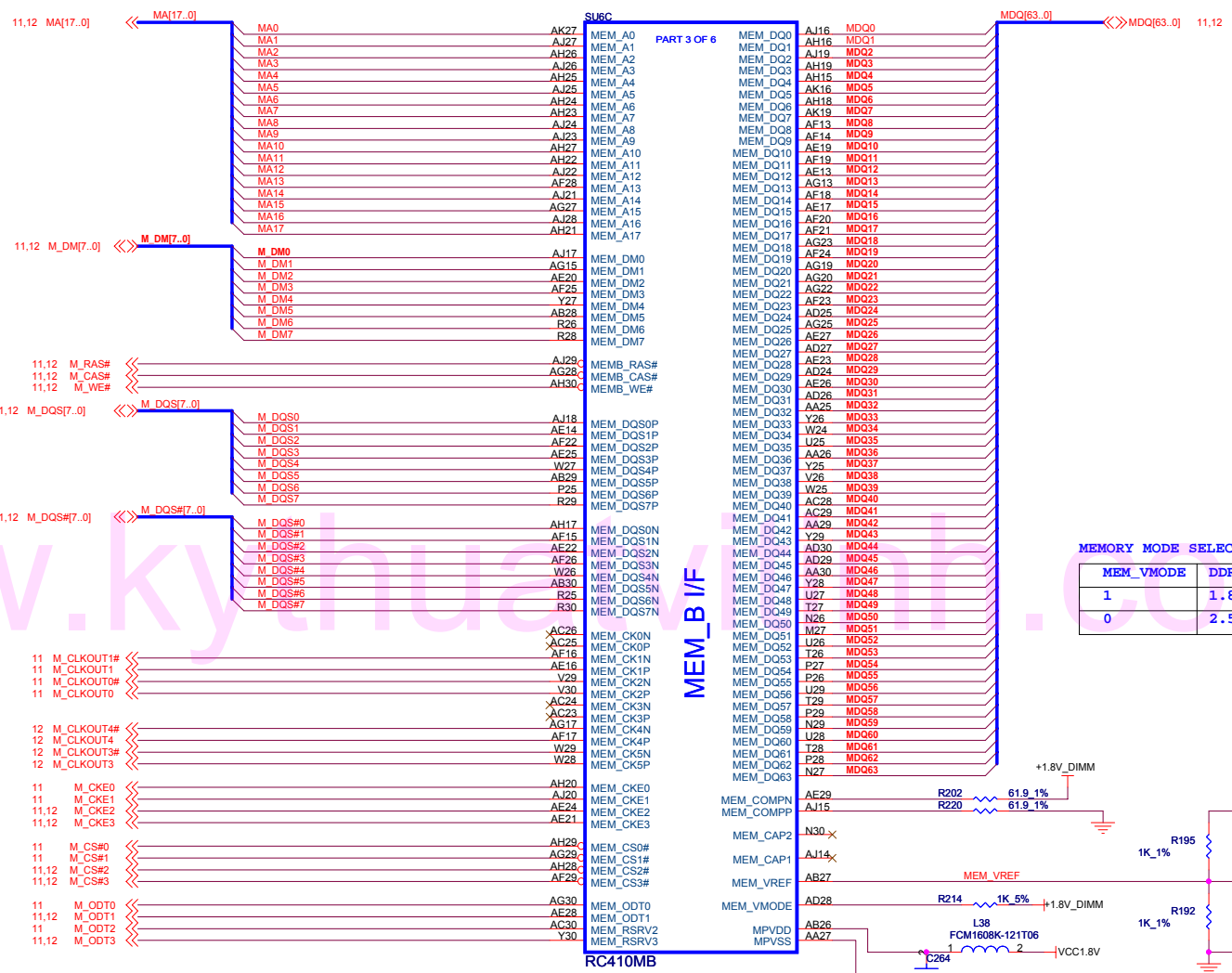
Title			Rev		
Dothan (POWER/NC)					
Size	Document Number			Rev	
Custom	400-1-4-01				
Date:	Monday, July 11, 2005	Sheet	5	of	35



www.kyathuath.com

CPVSS need to connect to GND plane immediately through a dedicated VIA

PLACE CLOSE TO RC400MB, USE 10/10 WIDTH/SPACE

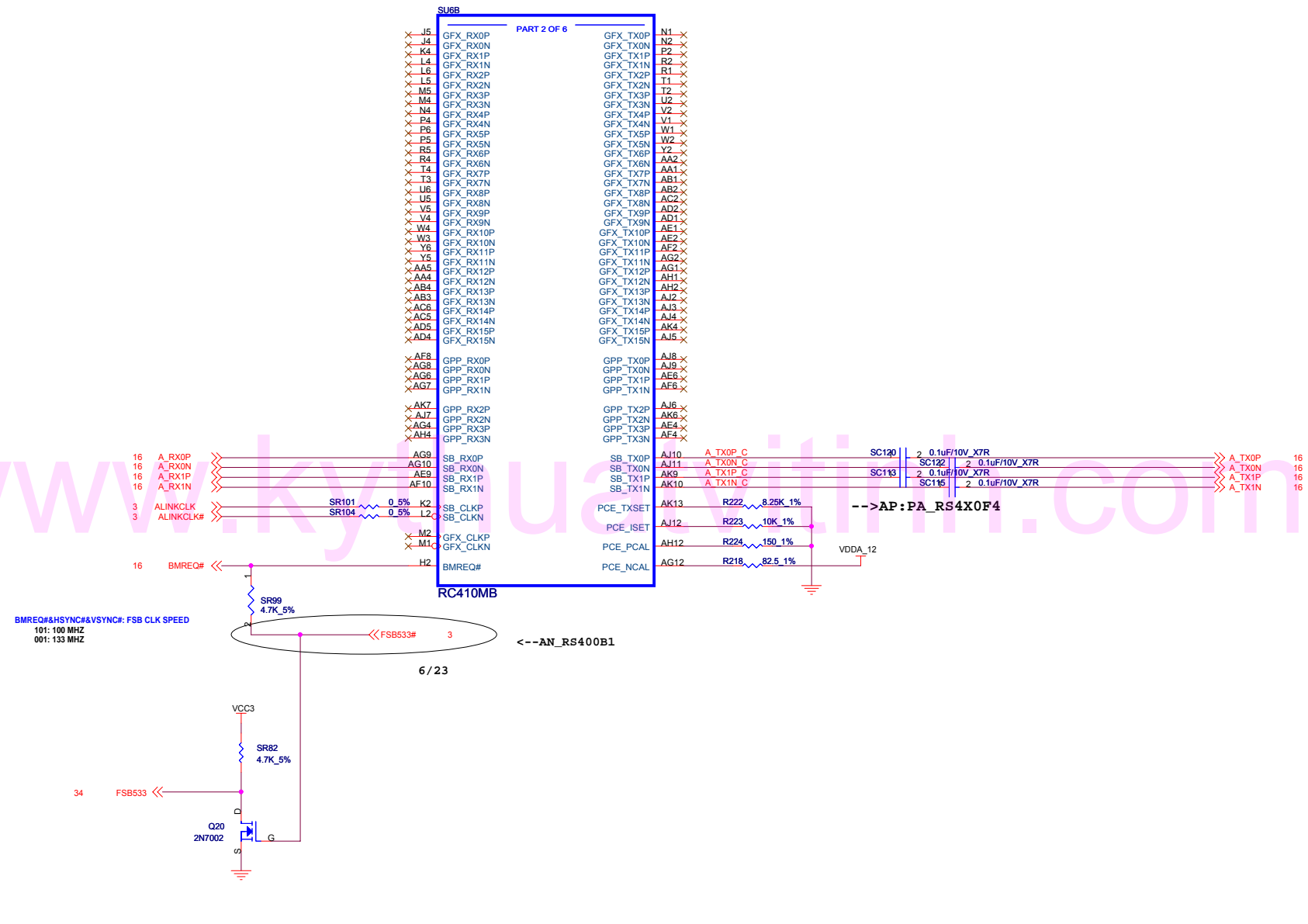


MEMORY MODE SELECT

MEM_VMODE	DDR MODE
1	1.8V DDRII
0	2.5V DDR

MPVSS need to connect to GND plane immediately through a dedicated VIA

www.kyusaiti.com

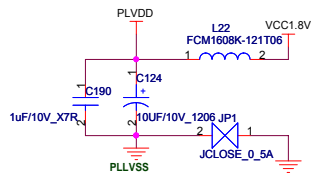
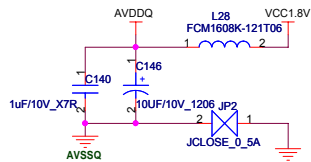




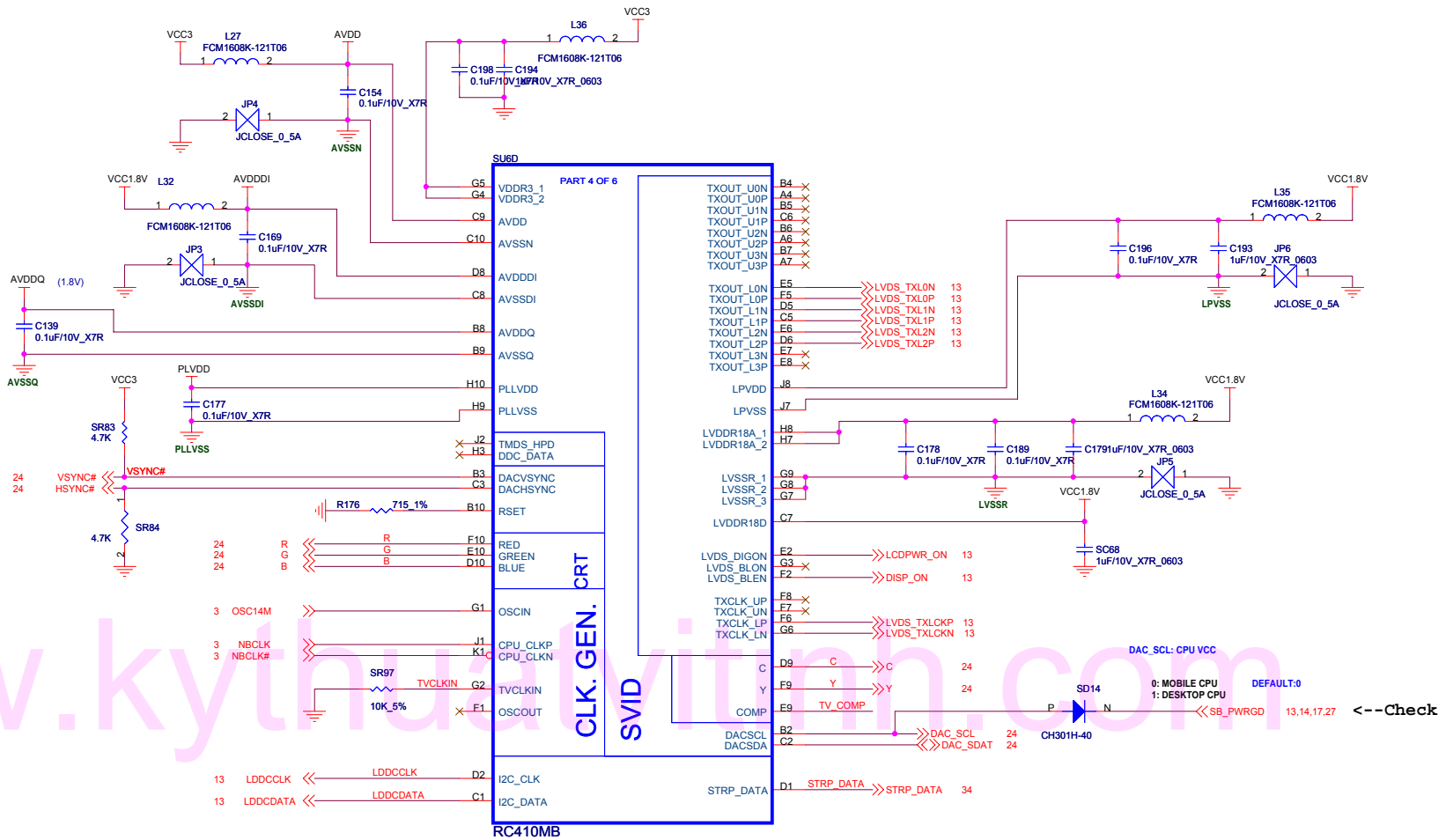
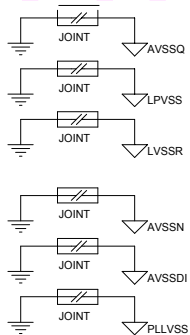
PUT AVDD, AVDDDI, AVDDQ, PLVDD DECOUPLING CAPS ON THE BOTTOM SIDE, CLOSE TO BALLS



RSET resistor R246 need 10mils trace with at least 10mils spacing. Also need to connect GND at AVSSQ HF cap.



Connect to GND plane after HF Cap with >=20mils trace



0: MOBILE CPU
1: DESKTOP CPU
DAC_SCL: CPU VCC
SB_PWRGD 13,14,17,27 <--Check

STRP_DATA: Debug strap
DEFAULT: 1
0: MEMORY CHANNEL STRAPING
1: E2PROM STRAPING

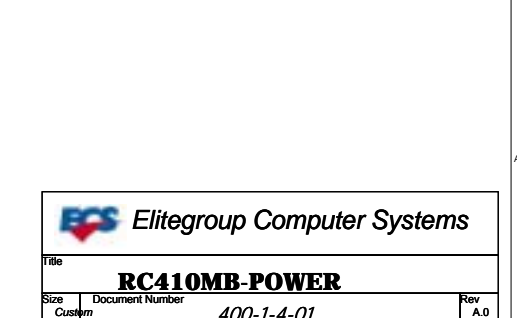
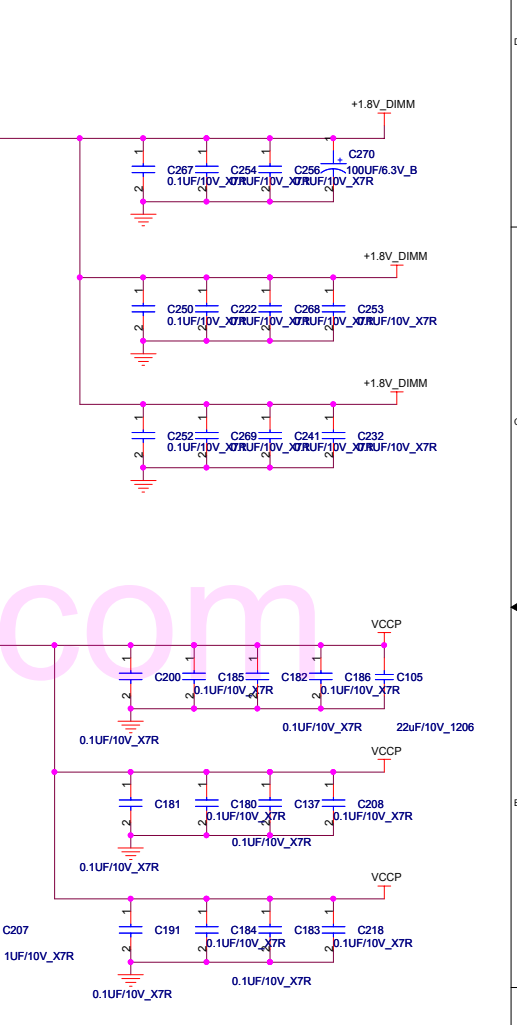
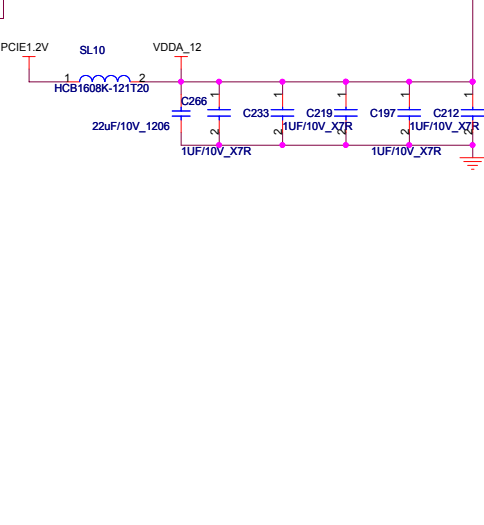
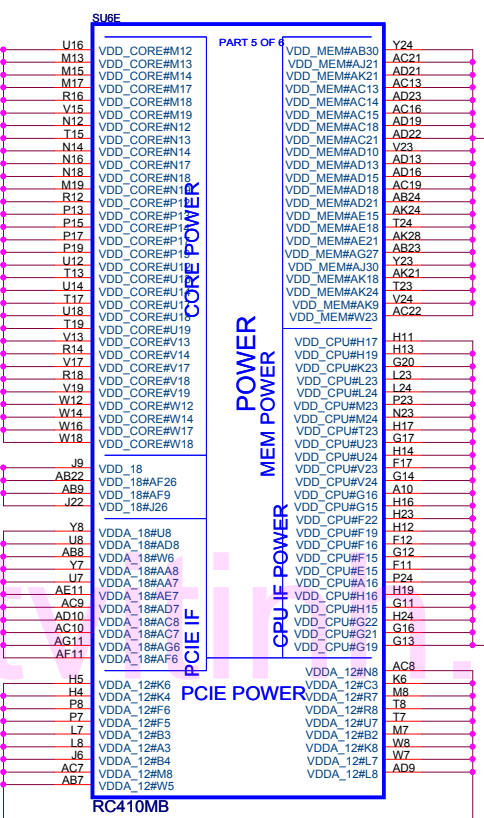
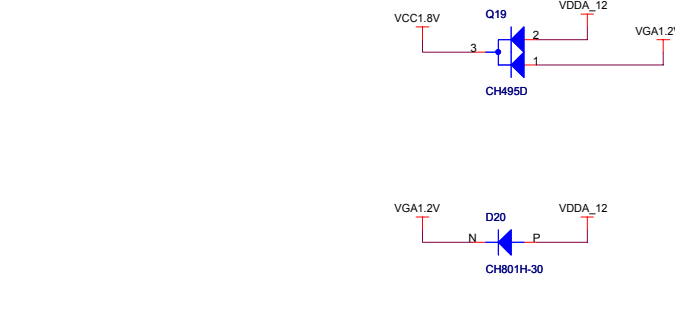
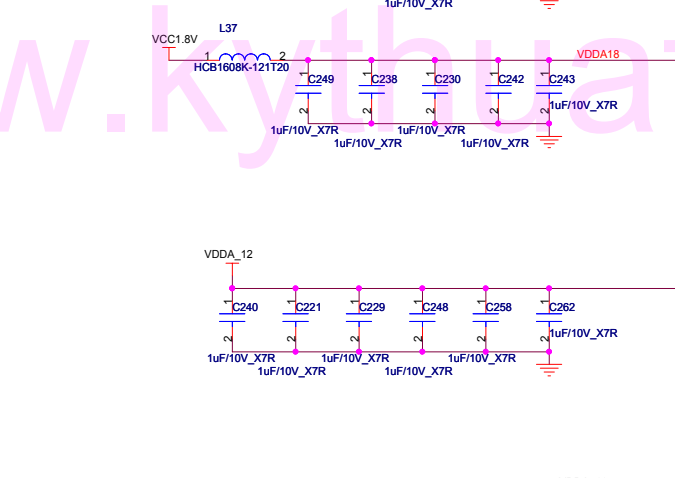
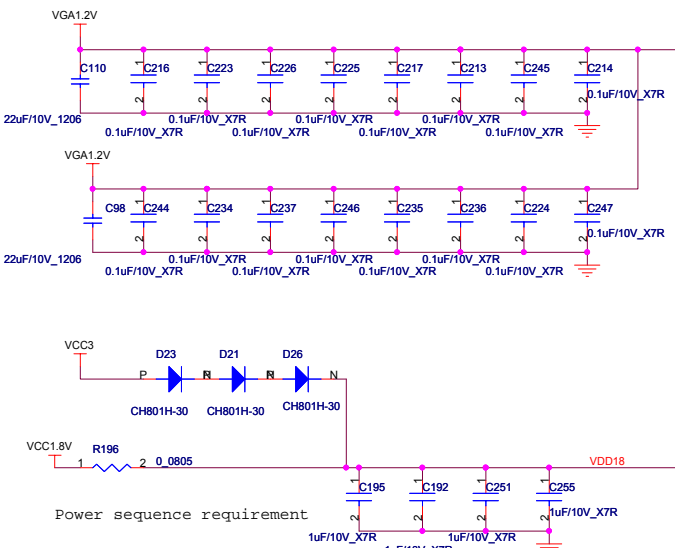
TV_COMP	R179	1	2	75_1%
R	R185	1	2	75_1%
G	R186	1	2	75_1%
B	R181	1	2	75_1%
Y	R184	1	2	75_1%
C	R180	1	2	75_1%

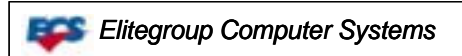
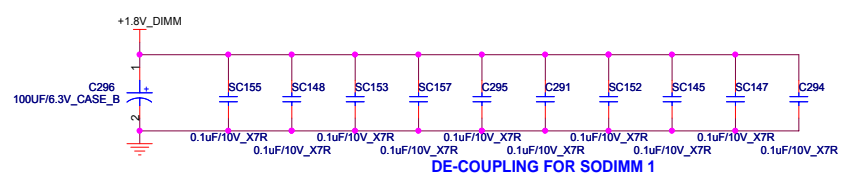
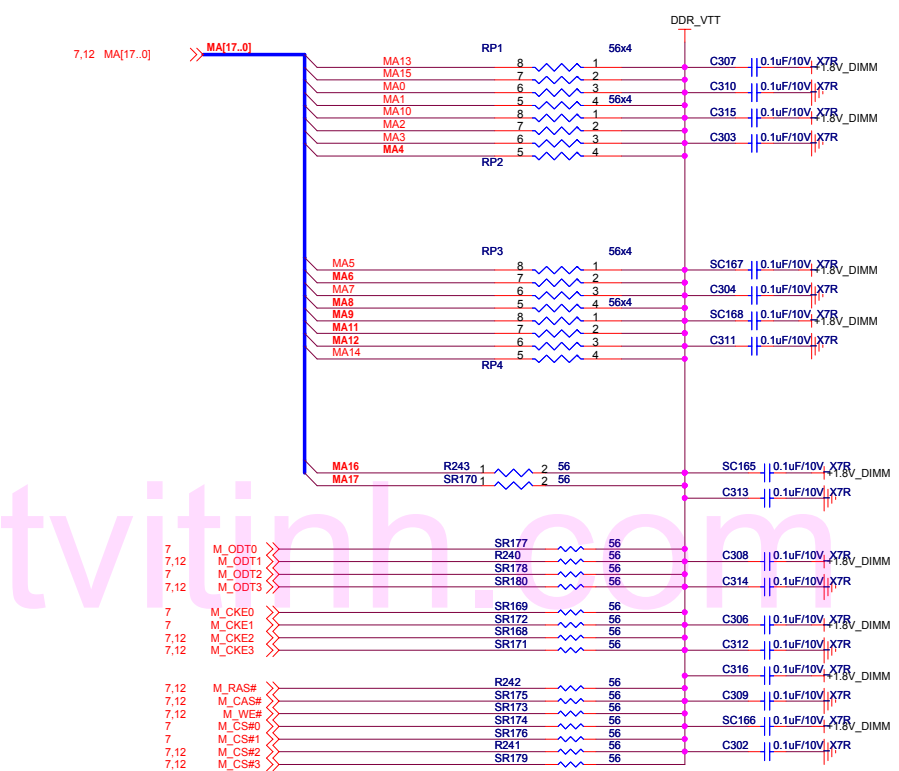
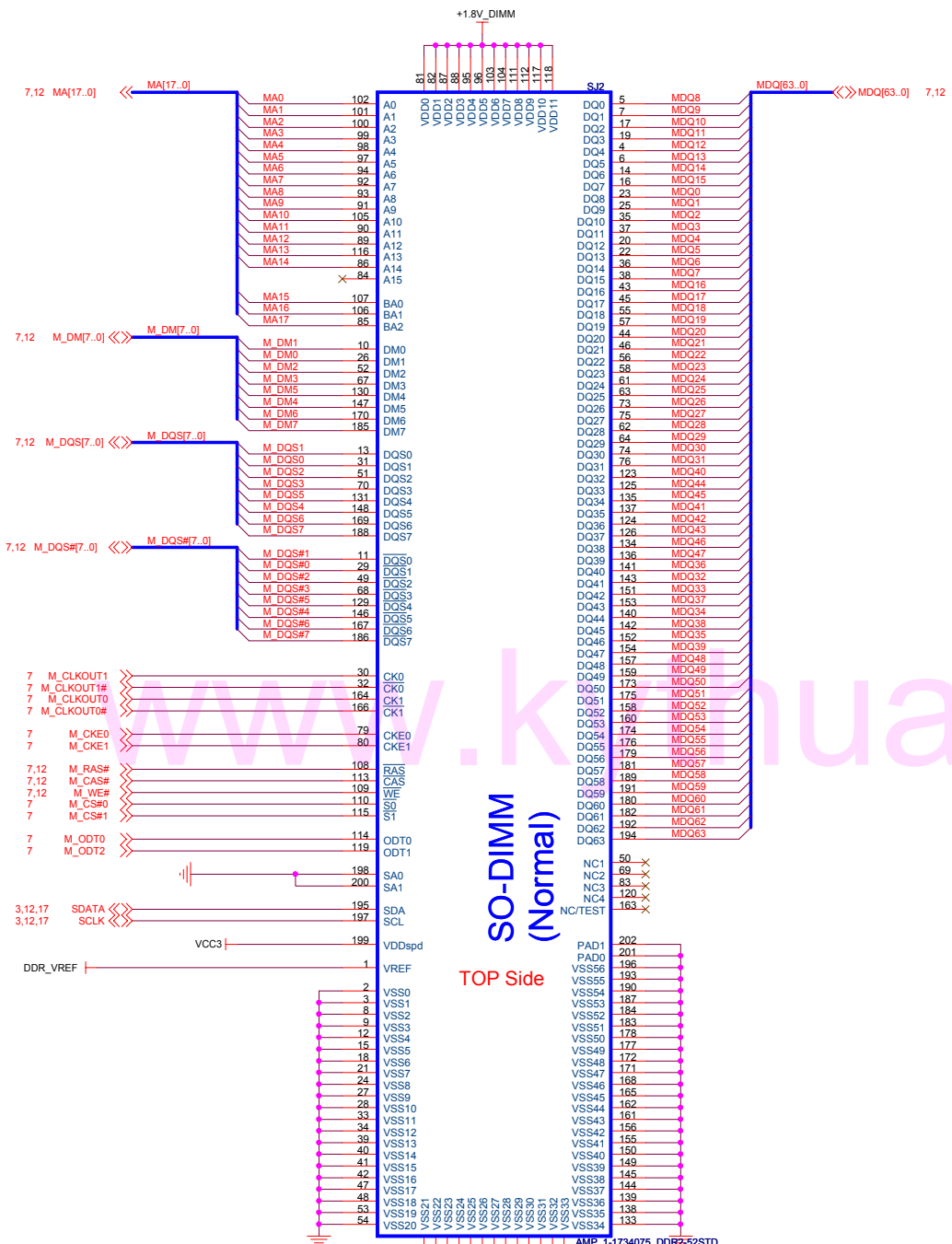
Close to NB-->



Title			
RC410MB-VIDEO&CLK			
Size	Document Number	Rev	A.0
Custom	400-1-4-01		
Date:	Monday, July 11, 2005	Sheet	9 of 35

SUBF		PART 6 OF 6	
W5	VSSA#U5	VSS#M15	M14
W6	VSSA#U6	VSS#G14	AG16
AB5	VSSA#Y5	VSS#G27	A22
AB6	VSSA#Y6	VSS#G3	A2
V7	VSSA#P8	VSS#G3	D27
AA8	VSSA#P7	VSS#H13	AG26
AA7	VSSA#U8	VSS#H14	H18
AD7	VSSA#Y7	VSS#H18	H18
AD8	VSSA#Y8	VSS#H23	A16
N8	VSSA#L8	VSS#H4	A9
R7	VSSA#L7	VSS#J23	AD17
R8	VSSA#L8	VSS#J24	J24
R7	VSSA#K7	VSS#J30	B27
N7	VSSA#A2	VSS#K30	D24
AF7	VSSA#AF5	VSS#K30	T30
AG5	VSSA#AC6	VSS#V30	U19
T6	VSSA#AC5	VSS#U19	M16
N5	VSSA#P6	VSS#AD11	AD11
T5	VSSA#P5	VSS#M30	H15
N6	VSSA#L6	VSS#N15	N15
N5	VSSA#L5	VSS#N15	N19
AH7	VSSA#H6	VSS#N16	D3
K6	VSSA#H5	VSS#N23	A25
AH3	VSSA#P4	VSS#N27	F3
AH8	VSSA#AE3	VSS#P15	R15
AH7	VSSA#AD3	VSS#P16	P16
AH6	VSSA#AC3	VSS#P23	G10
AD3	VSSA#A3	VSS#P24	M24
AC3	VSSA#Y3	VSS#R12	M12
AA3	VSSA#Y3	VSS#R13	R13
Y3	VSSA#U3	VSS#R12	P12
U3	VSSA#R3	VSS#R14	P14
R3	VSSA#P3	VSS#R15	U13
P3	VSSA#M3	VSS#R17	R17
M3	VSSA#L3	VSS#R18	V18
L3	VSSA#J3	VSS#R19	R19
AF5	VSSA#H3	VSS#R23	R23
AF3	VSSA#N3	VSS#R24	R24
AF9	VSSA#AG3	VSS#R30	J30
AH9	VSSA#AE9	VSS#T12	T12
AH10	VSSA#AH7	VSS#T13	M13
AC20	VSSA#A15	VSS#T14	T14
J23	VSSA#A24	VSS#T15	E18
A23	VSSA#A29	VSS#T16	T16
W30	VSSA#A29	VSS#T17	T18
W23	VSSA#A23	VSS#T18	W19
AA28	VSSA#A24	VSS#T19	J27
AJ30	VSSA#AB27	VSS#T27	J27
AC12	VSS#AC12	VSS#U15	U15
AC15	VSS#AC16	VSS#U16	N17
K8	VSS#AC8	VSS#V16	V16
AD12	VSS#AD12	VSS#V17	W17
AD15	VSS#AD16	VSS#W27	M26
AD18	VSS#AD19	VSS#V12	V12
AC17	VSS#AD8	VSS#W13	W13
AE30	VSS#AD23	VSS#W13	V14
AD14	VSS#AD30	VSS#W15	W15
AC11	VSS#AD9	VSS#Y23	U23
AE12	VSS#AE12	VSS#Y24	U24
AE27	VSS#AE27	VSS#C19	V28
AG14	VSS#AC19	VSS#C17	AG24
F4	VSS#AG12	VSS#AH26	AA24
AG18	VSS#AG18	VSS#AG25	AA23
AG21	VSS#AG21	VSS#F30	F30
AK25	VSS#AG9	VSS#F25	K23
V27	VSS#AH28	VSS#D27	D20
AJ1	VSS#AJ1	VSS#D25	A19
AD20	VSS#AK10	VSS#D23	D17
AK12	VSS#AK13	VSS#D20	D14
AK15	VSS#AK16	VSS#D17	F27
AK18	VSS#AK19	VSS#C3	D4
AK2	VSS#AK2	VSS#C28	M23
AH11	VSS#AH11	VSS#B30	B30
J8	VSS#AJ11	VSS#B1	B1
AC27	VSS#AK25	VSS#AK29	AK29
		VSS#AK22	AK22





Title			Rev		
DDR2 SODIMM 1			A.0		
Size	Document Number				
Custom	400-1-4-01				
Date:	Monday, July 11, 2005	Sheet	11	of	35

+1.8V_DIMM

81 82 83 84 85 86 87 88 89 90 91 92 93 94 95 96 97 98 99 100 101 102

MA0 MA1 MA2 MA3 MA4 MA5 MA6 MA7 MA8 MA9 MA10 MA11 MA12 MA13 MA14 MA15 MA16 MA17

M_DM1 M_DM0 M_DM2 M_DM3 M_DM4 M_DM5 M_DM6 M_DM7

M_DQS1 M_DQS0 M_DQS2 M_DQS3 M_DQS4 M_DQS5 M_DQS6 M_DQS7

M_DQS#1 M_DQS#0 M_DQS#2 M_DQS#3 M_DQS#4 M_DQS#5 M_DQS#6 M_DQS#7

M_CLKOUT4 M_CLKOUT## M_CLKOUT3 M_CLKOUT3#

M_KE2 M_KE3

M_RAS# M_CAS# M_WE# M_CS#2 M_CS#3

M_ODT1 M_ODT3

SDATA SCL

VDDspd VREF

VSS0 VSS1 VSS2 VSS3 VSS4 VSS5 VSS6 VSS7 VSS8 VSS9 VSS10 VSS11 VSS12 VSS13 VSS14 VSS15 VSS16 VSS17 VSS18 VSS19 VSS20

VSS21 VSS22 VSS23 VSS24 VSS25 VSS26 VSS27 VSS28 VSS29 VSS30 VSS31 VSS32 VSS33 VSS34

69 70 71 72 73 74 75 76 77 78 79 80 81 82 83 84 85 86 87 88 89 90 91 92 93 94 95 96 97 98 99 100 101 102

AMP_1717833-4_DDR2-40RVS

5 MDQ8 MDQ9 MDQ10 MDQ11 MDQ12 MDQ13 MDQ14 MDQ15 MDQ0 MDQ1 MDQ2 MDQ3 MDQ4 MDQ5 MDQ6 MDQ7 MDQ16 MDQ17 MDQ18 MDQ19 MDQ20 MDQ21 MDQ22 MDQ23 MDQ24 MDQ25 MDQ26 MDQ27 MDQ28 MDQ29 MDQ30 MDQ31 MDQ32 MDQ33 MDQ34 MDQ35 MDQ36 MDQ37 MDQ38 MDQ39 MDQ40 MDQ41 MDQ42 MDQ43 MDQ44 MDQ45 MDQ46 MDQ47 MDQ48 MDQ49 MDQ50 MDQ51 MDQ52 MDQ53 MDQ54 MDQ55 MDQ56 MDQ57 MDQ58 MDQ59 MDQ60 MDQ61 MDQ62 MDQ63

NC1 NC2 NC3 NC4 NC/TEST

PAD1 PAD0 VSS56 VSS55 VSS54 VSS53 VSS52 VSS51 VSS50 VSS49 VSS48 VSS47 VSS46 VSS45 VSS44 VSS43 VSS42 VSS41 VSS40 VSS39 VSS38 VSS37 VSS36 VSS35 VSS34

AMP_1717833-4_DDR2-40RVS

MDQ[63..0] MDQ[63..0]

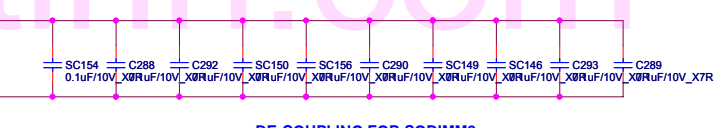
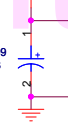
5 MDQ8 MDQ9 MDQ10 MDQ11 MDQ12 MDQ13 MDQ14 MDQ15 MDQ0 MDQ1 MDQ2 MDQ3 MDQ4 MDQ5 MDQ6 MDQ7 MDQ16 MDQ17 MDQ18 MDQ19 MDQ20 MDQ21 MDQ22 MDQ23 MDQ24 MDQ25 MDQ26 MDQ27 MDQ28 MDQ29 MDQ30 MDQ31 MDQ32 MDQ33 MDQ34 MDQ35 MDQ36 MDQ37 MDQ38 MDQ39 MDQ40 MDQ41 MDQ42 MDQ43 MDQ44 MDQ45 MDQ46 MDQ47 MDQ48 MDQ49 MDQ50 MDQ51 MDQ52 MDQ53 MDQ54 MDQ55 MDQ56 MDQ57 MDQ58 MDQ59 MDQ60 MDQ61 MDQ62 MDQ63

NC1 NC2 NC3 NC4 NC/TEST

PAD1 PAD0 VSS56 VSS55 VSS54 VSS53 VSS52 VSS51 VSS50 VSS49 VSS48 VSS47 VSS46 VSS45 VSS44 VSS43 VSS42 VSS41 VSS40 VSS39 VSS38 VSS37 VSS36 VSS35 VSS34

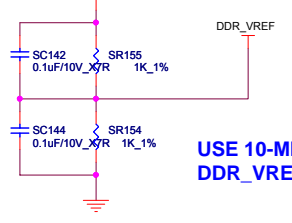
AMP_1717833-4_DDR2-40RVS

+1.8V_DIMM



DE-COUPLING FOR SODIMM2

+1.8V_DIMM

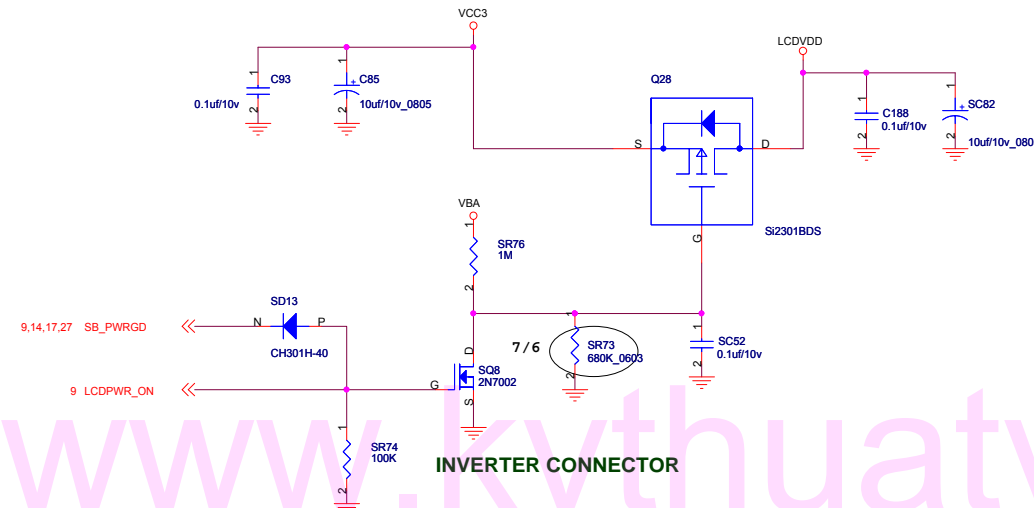


USE 10-MIL TRACE ON DDR_VREF

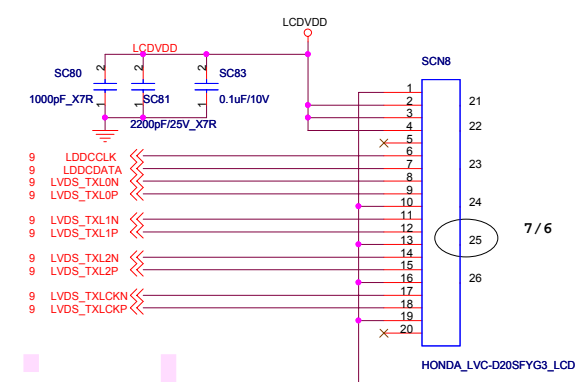


Title			Rev		
DDR2 SODIMM2			A.0		
Size	Document Number				
Custom	400-1-4-01				
Date:	Monday, July 11, 2005	Sheet	12	of	35

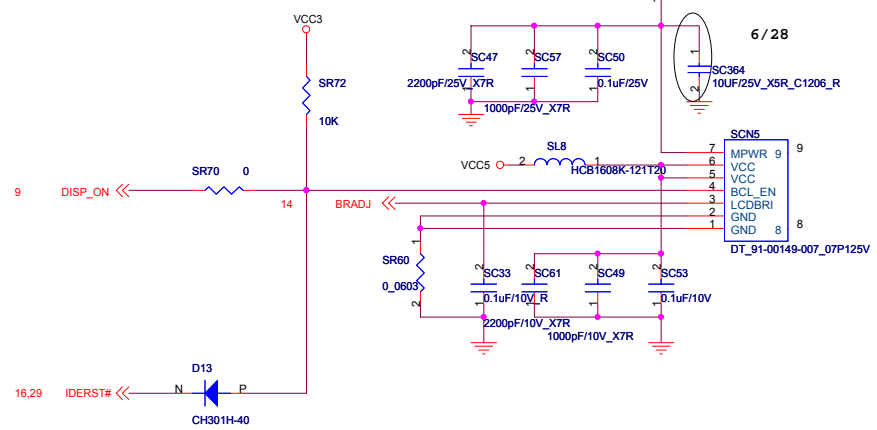
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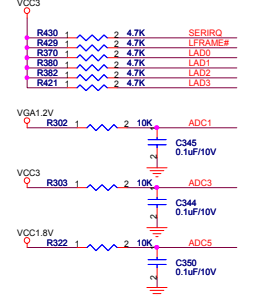
INVERTER CONNECTOR



HONDA_LVC-D20SFYG3_LCD

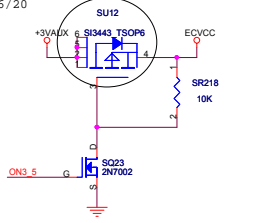
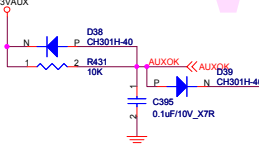
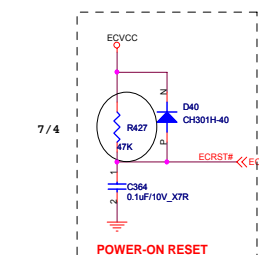


Elitegroup Computer Systems			
Title			
LVDS PANEL CONN			
Size	Document Number	Rev	
Custom	400-1-4-01	A.0	
Date:	Monday, July 11, 2005	Sheet	13 of 35

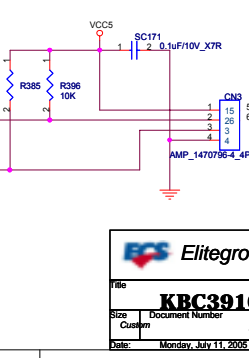
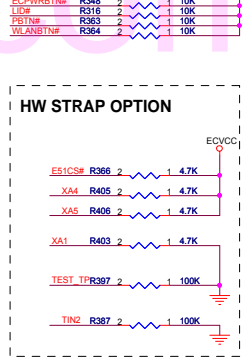
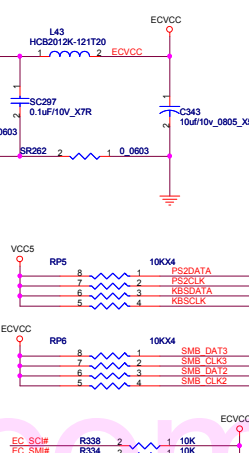
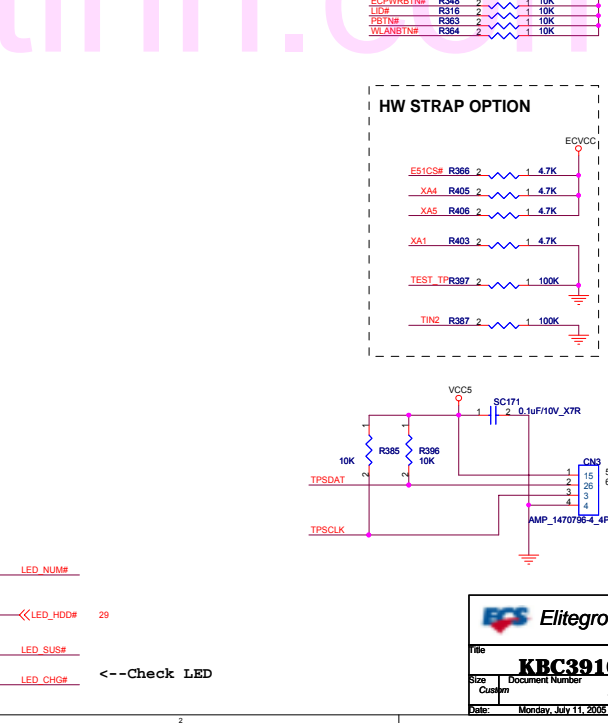
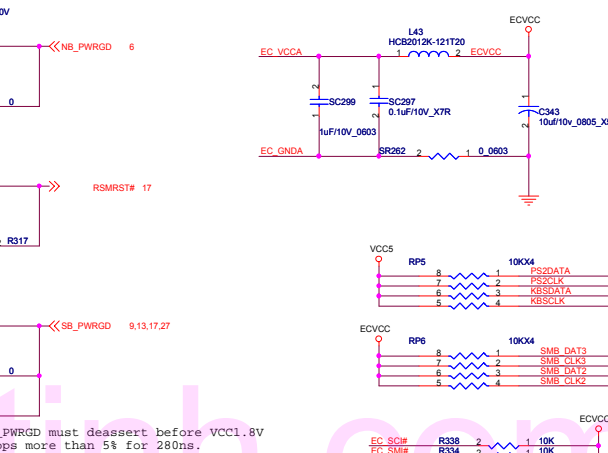
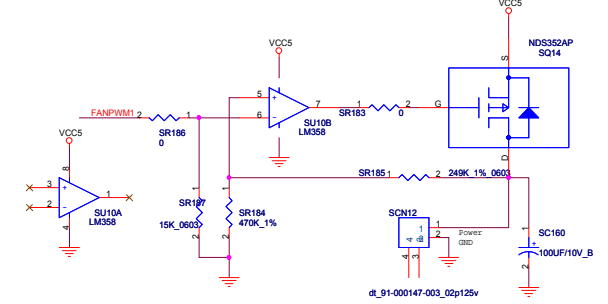
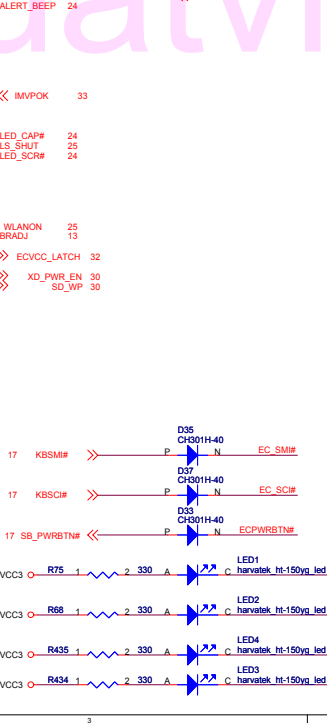
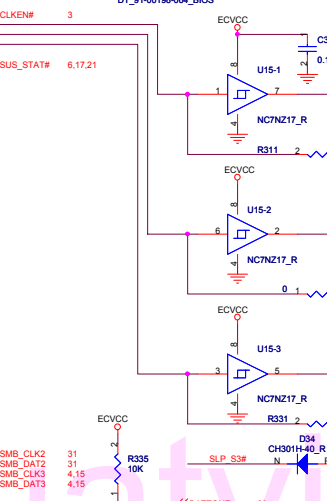
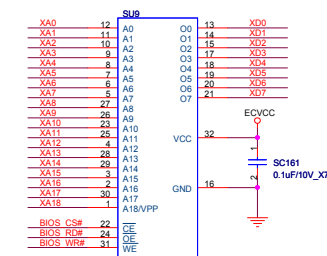


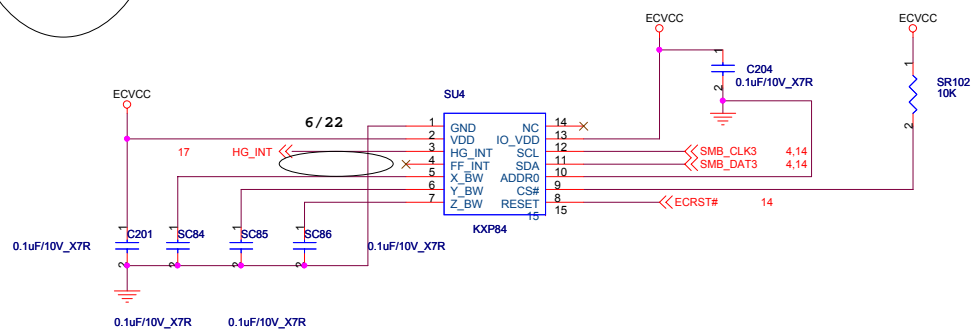
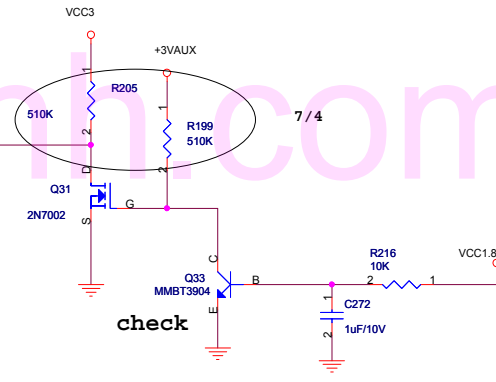
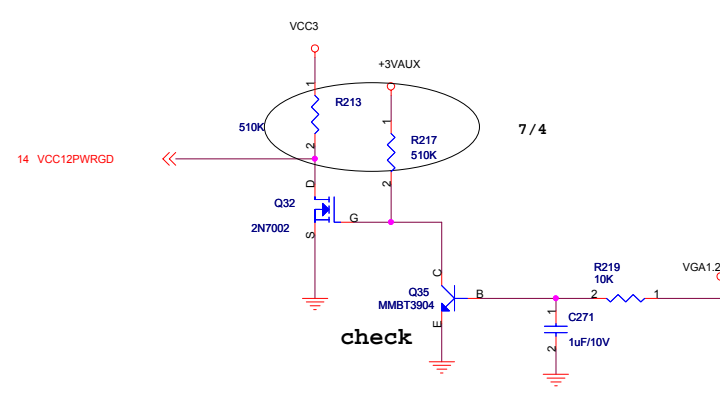
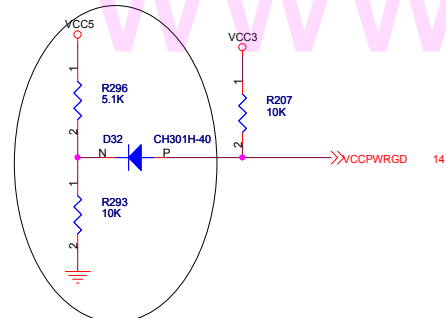
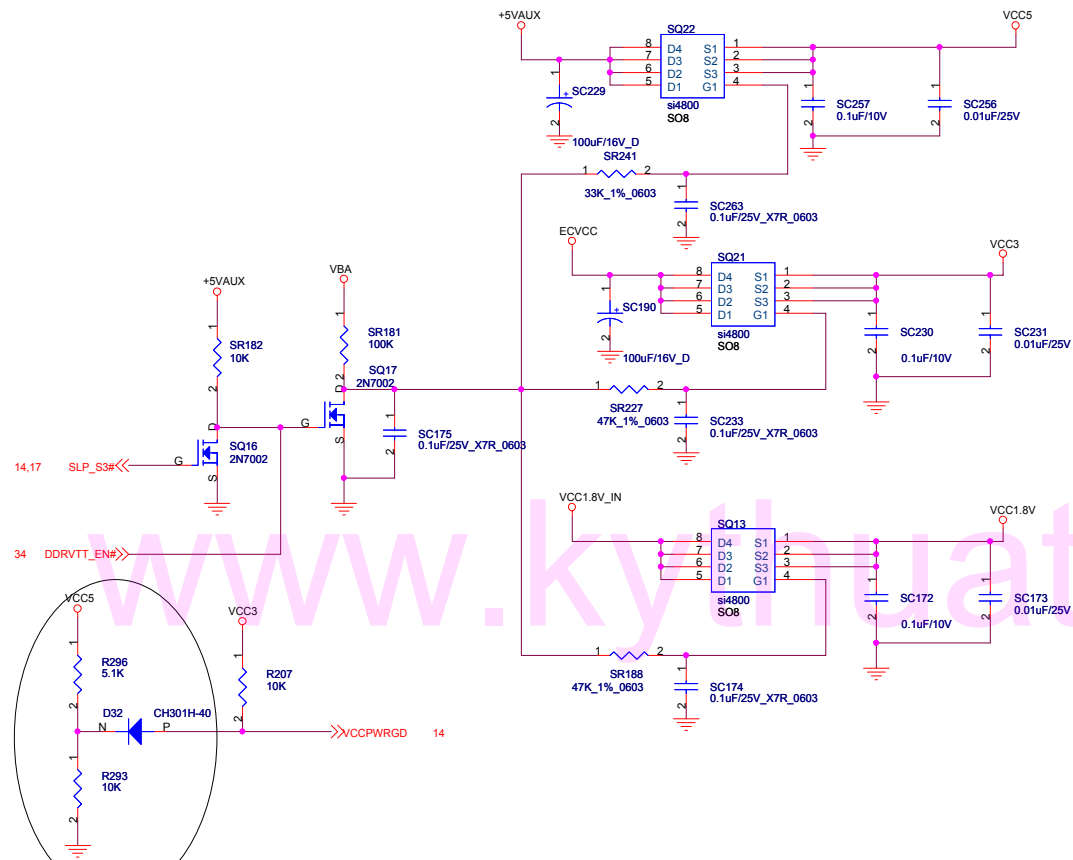
RCIN# should be deasserted before ARST# deasserted.

Pull-Down resistor required to avoid leakage current

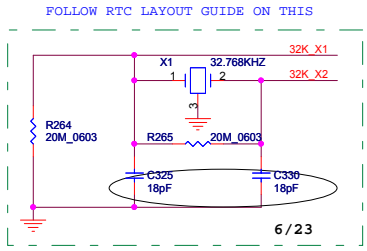


Pin	Function	Pin	Function	Pin	Function
1	VCC3	16	LFRAME#	31	ENCHG
2	VCC3	17	LAD3	32	PRECHG
3	VCC3	18	LAD2	33	PRECHG
4	VCC3	19	LAD1	34	MDIO0
5	VCC3	20	LAD0	35	MDIO1
6	VCC3	21	LAD0	36	MDIO2
7	VCC3	22	LAD1	37	MDIO3
8	VCC3	23	LAD2	38	MDIO4
9	VCC3	24	LAD3	39	MDIO5
10	VCC3	25	LAD0	40	MDIO6
11	VCC3	26	LAD1	41	MDIO7
12	VCC3	27	LAD2	42	MDIO8
13	VCC3	28	LAD3	43	MDIO9
14	VCC3	29	LAD0	44	MDIO10
15	VCC3	30	LAD1	45	MDIO11
16	VCC3	31	LAD2	46	MDIO12
17	VCC3	32	LAD3	47	MDIO13
18	VCC3	33	LAD0	48	MDIO14
19	VCC3	34	LAD1	49	MDIO15
20	VCC3	35	LAD2	50	MDIO16
21	VCC3	36	LAD3	51	MDIO17
22	VCC3	37	LAD0	52	MDIO18
23	VCC3	38	LAD1	53	MDIO19
24	VCC3	39	LAD2	54	MDIO20
25	VCC3	40	LAD3	55	MDIO21
26	VCC3	41	LAD0	56	MDIO22
27	VCC3	42	LAD1	57	MDIO23
28	VCC3	43	LAD2	58	MDIO24
29	VCC3	44	LAD3	59	MDIO25
30	VCC3	45	LAD0	60	MDIO26
31	VCC3	46	LAD1	61	MDIO27
32	VCC3	47	LAD2	62	MDIO28
33	VCC3	48	LAD3	63	MDIO29
34	VCC3	49	LAD0	64	MDIO30
35	VCC3	50	LAD1	65	MDIO31
36	VCC3	51	LAD2	66	MDIO32
37	VCC3	52	LAD3	67	MDIO33
38	VCC3	53	LAD0	68	MDIO34
39	VCC3	54	LAD1	69	MDIO35
40	VCC3	55	LAD2	70	MDIO36
41	VCC3	56	LAD3	71	MDIO37
42	VCC3	57	LAD0	72	MDIO38
43	VCC3	58	LAD1	73	MDIO39
44	VCC3	59	LAD2	74	MDIO40
45	VCC3	60	LAD3	75	MDIO41
46	VCC3	61	LAD0	76	MDIO42
47	VCC3	62	LAD1	77	MDIO43
48	VCC3	63	LAD2	78	MDIO44
49	VCC3	64	LAD3	79	MDIO45
50	VCC3	65	LAD0	80	MDIO46
51	VCC3	66	LAD1	81	MDIO47
52	VCC3	67	LAD2	82	MDIO48
53	VCC3	68	LAD3	83	MDIO49
54	VCC3	69	LAD0	84	MDIO50
55	VCC3	70	LAD1	85	MDIO51
56	VCC3	71	LAD2	86	MDIO52
57	VCC3	72	LAD3	87	MDIO53
58	VCC3	73	LAD0	88	MDIO54
59	VCC3	74	LAD1	89	MDIO55
60	VCC3	75	LAD2	90	MDIO56
61	VCC3	76	LAD3	91	MDIO57
62	VCC3	77	LAD0	92	MDIO58
63	VCC3	78	LAD1	93	MDIO59
64	VCC3	79	LAD2	94	MDIO60
65	VCC3	80	LAD3	95	MDIO61
66	VCC3	81	LAD0	96	MDIO62
67	VCC3	82	LAD1	97	MDIO63
68	VCC3	83	LAD2	98	MDIO64
69	VCC3	84	LAD3	99	MDIO65
70	VCC3	85	LAD0	100	MDIO66
71	VCC3	86	LAD1	101	MDIO67
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74	VCC3	89	LAD0	104	MDIO70
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76	VCC3	91	LAD2	106	MDIO72
77	VCC3	92	LAD3	107	MDIO73
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79	VCC3	94	LAD1	109	MDIO75
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86	VCC3	101	LAD0	116	MDIO82
87	VCC3	102	LAD1	117	MDIO83
88	VCC3	103	LAD2	118	MDIO84
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96	VCC3	111	LAD2	126	MDIO92
97	VCC3	112	LAD3	127	MDIO93
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99	VCC3	114	LAD1	129	MDIO95
100	VCC3	115	LAD2	130	MDIO96





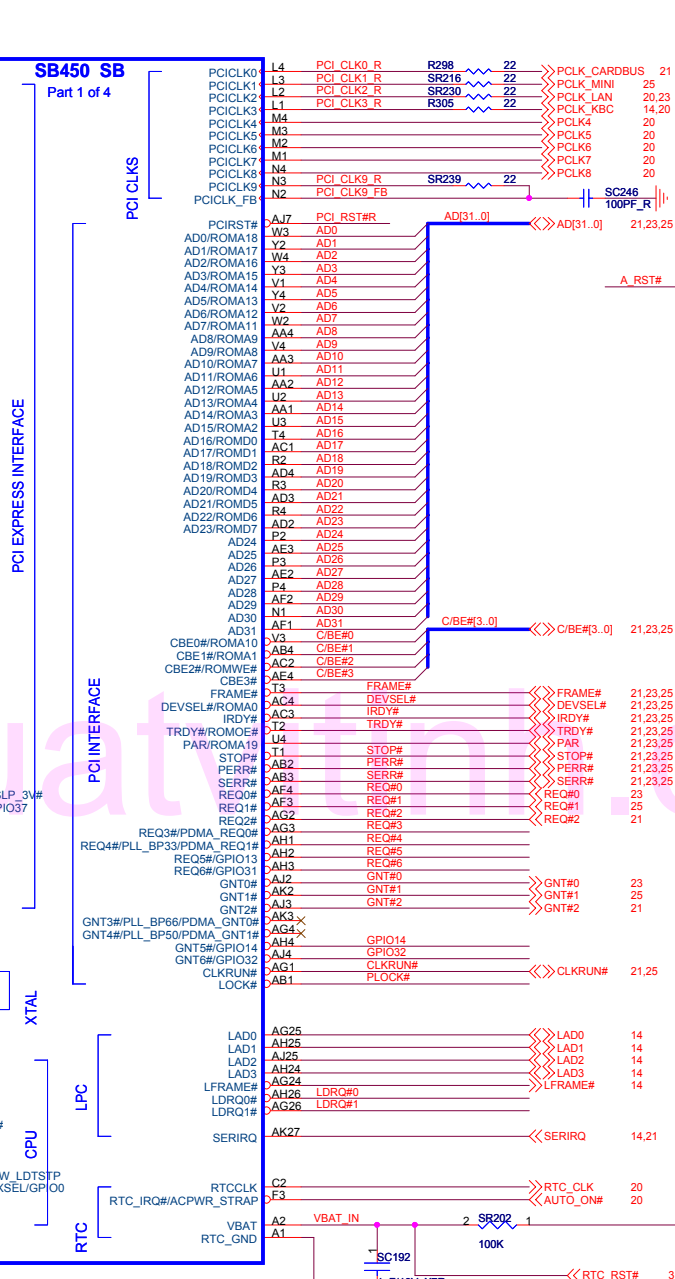
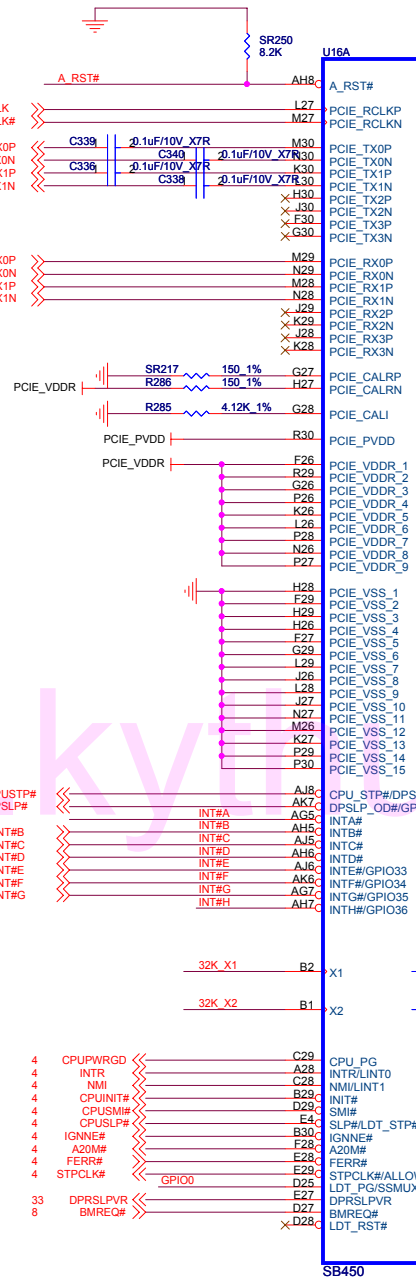
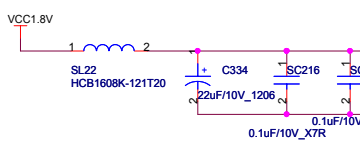
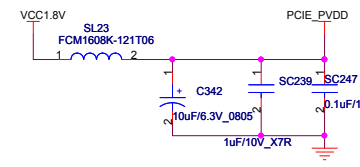
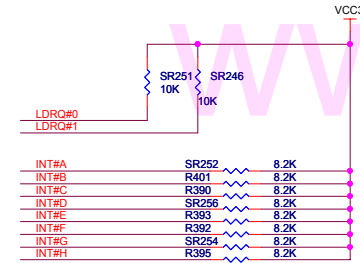
Elitegroup Computer Systems			
VCC Switches and Accelerometer			
File	Document Number	Rev	A.0
Size	400-1-4-01		
Date:	Monday, July 11, 2005	Sheet	15 of 35



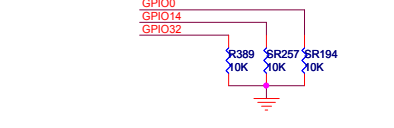
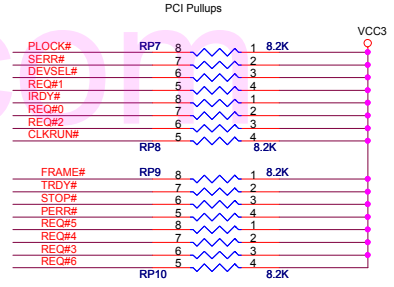
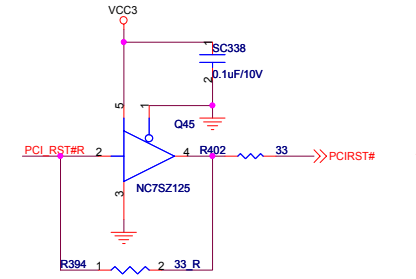
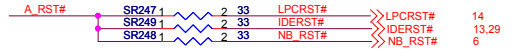
Note: RTC crystal need to lay down

<- PA_IXP400AY3

3.33 CPUSTP#
4 DPSLP#



Minum PCI CLK_FB length



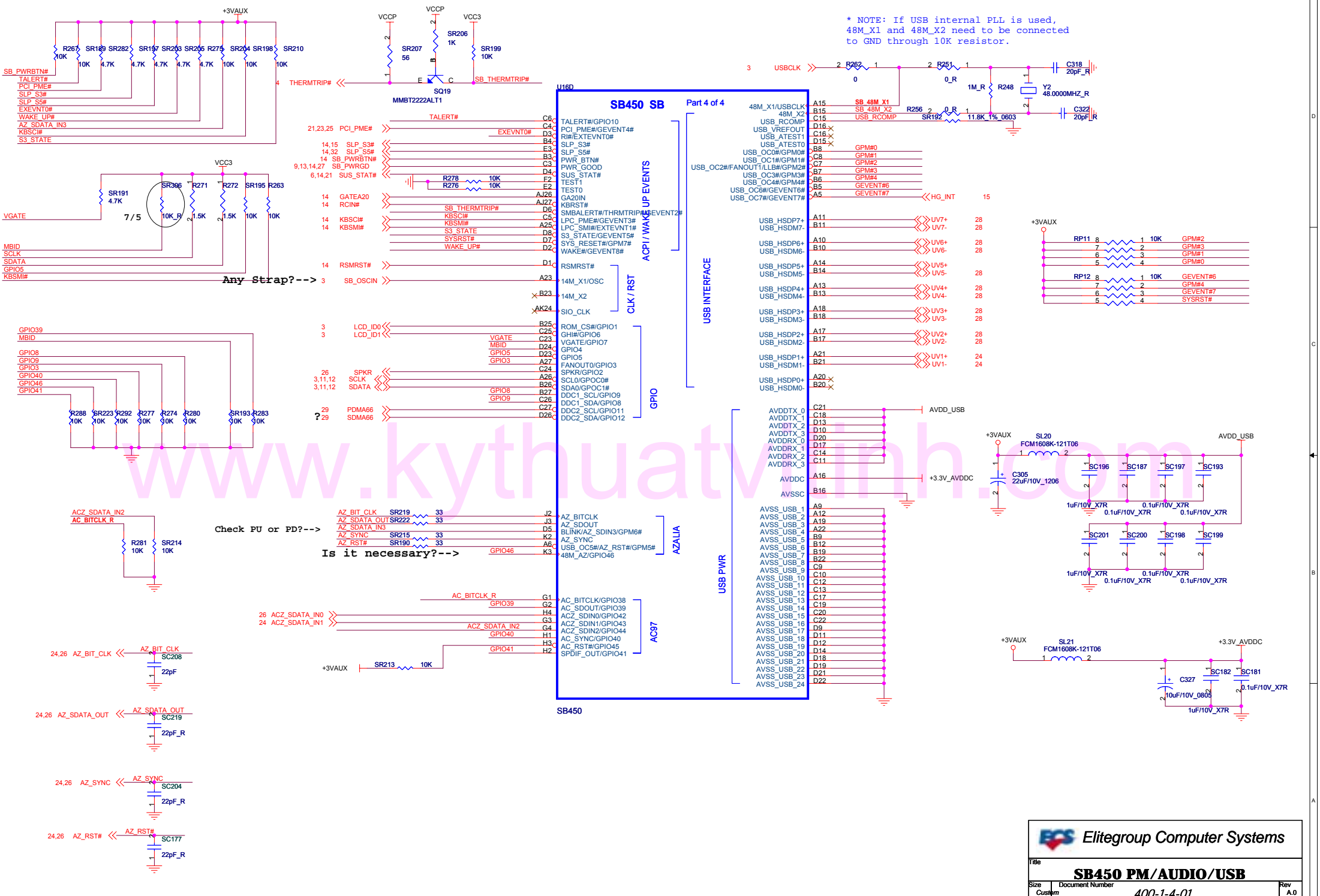
Clear-CMOS can only be done when +3VAUX is not exist(battery mode)

Elitegroup Computer Systems

Title: **SB450 PCI/CPU/LPC/RTC**

Size: Custom Document Number: **400-1-4-01**

Date: Monday, July 11, 2005 Sheet 16 of 35



* NOTE: If USB internal PLL is used, 48M_X1 and 48M_X2 need to be connected to GND through 10K resistor.

Any Strap?-->

Check PU or PD?-->

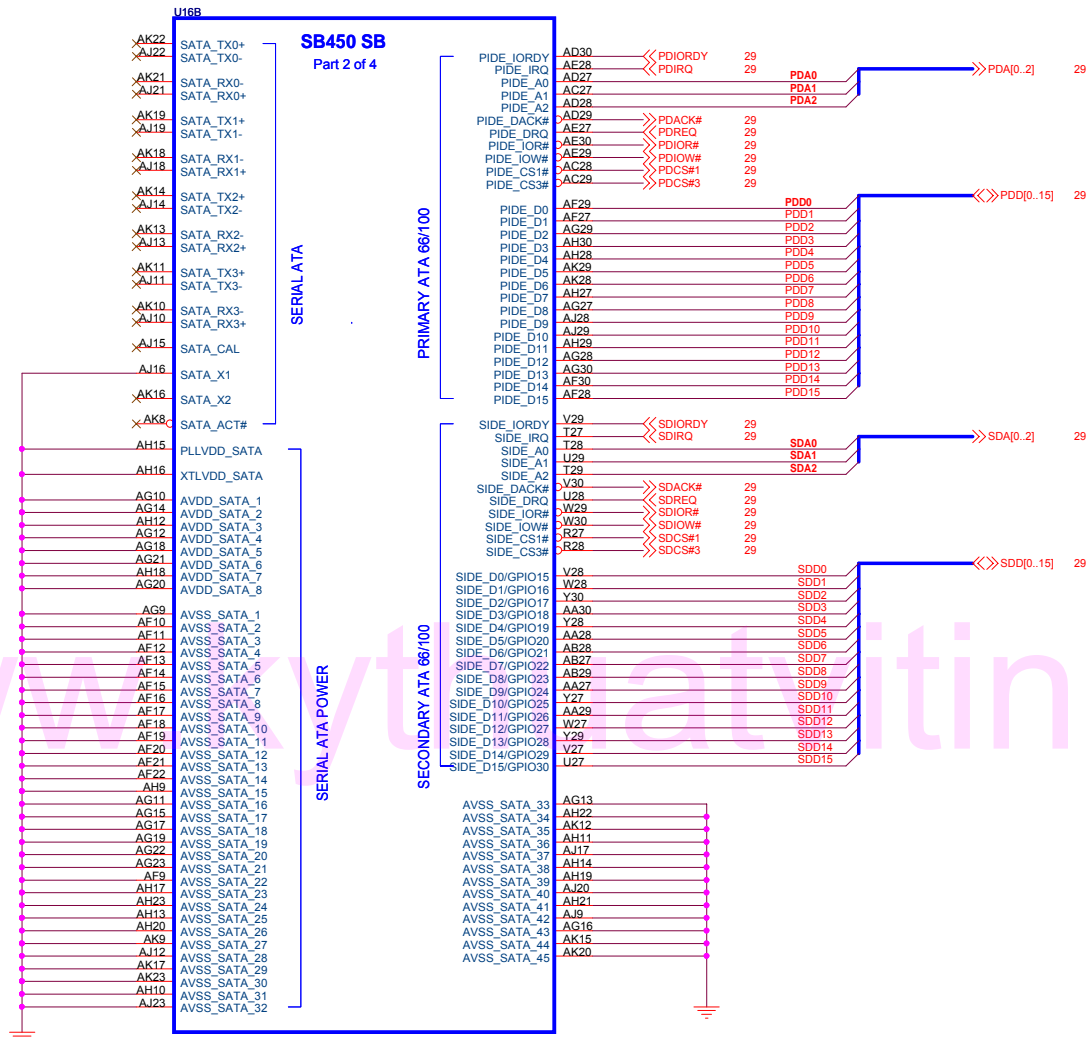
Is it necessary?-->

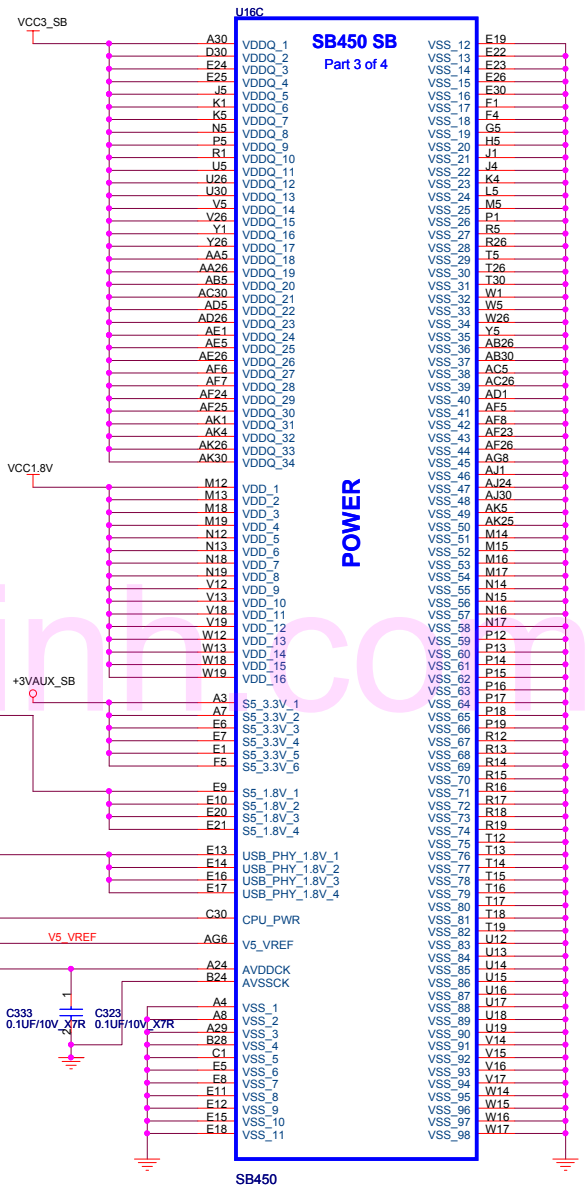
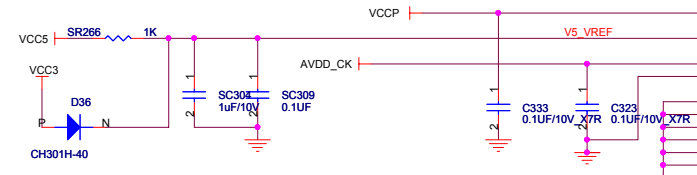
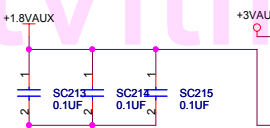
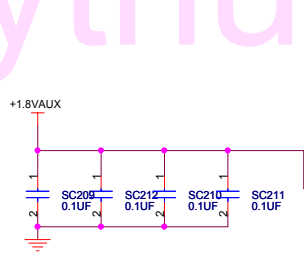
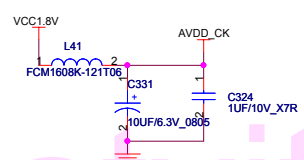
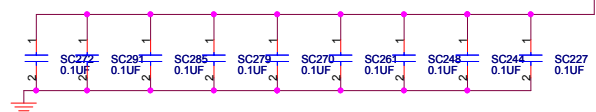
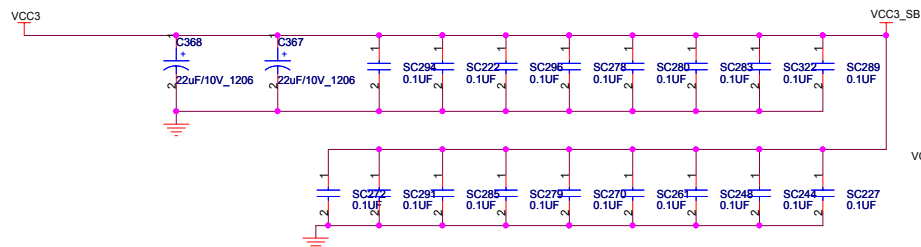
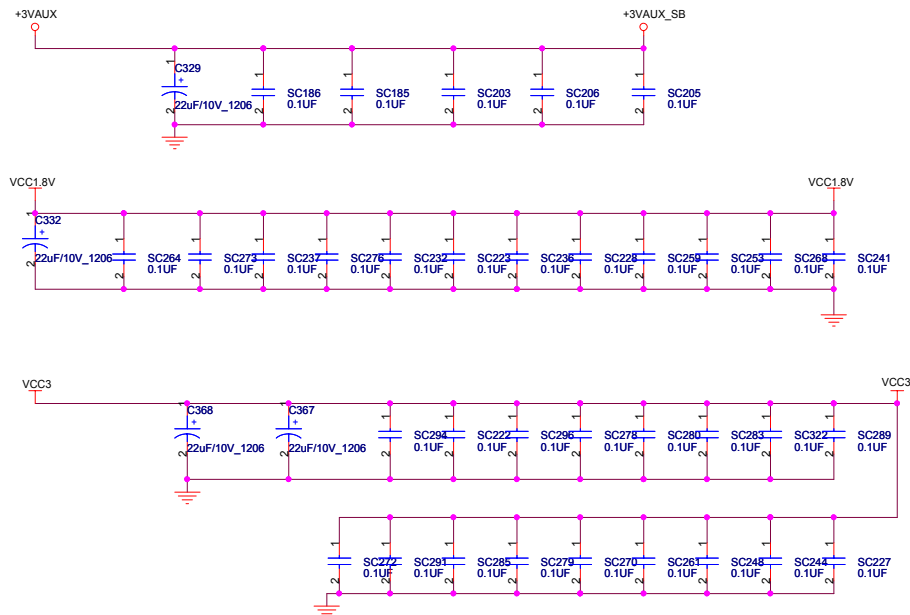
Elitegroup Computer Systems

Title: **SB450 PM/AUDIO/USB**

Size: Custom Document Number: **400-1-4-01** Rev: A.0

Date: Monday, July 11, 2005 Sheet: 17 of 35





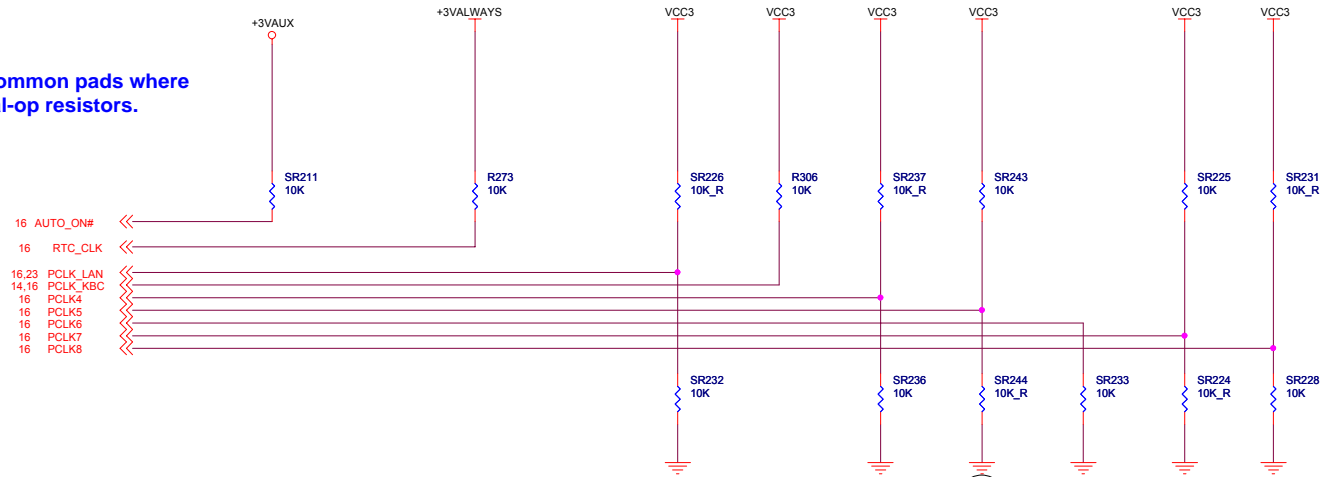
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Title			Rev		
SB450 POWER			A.0		
Size	Document Number			Date:	
Custom	400-1-4-01			Monday, July 11, 2005	
Date:		Monday, July 11, 2005	Sheet	19	of 35

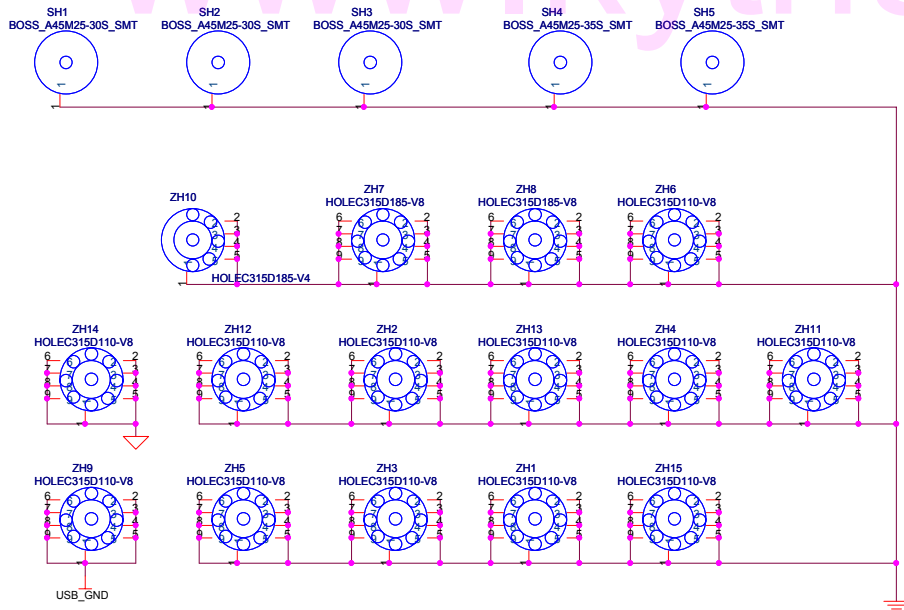


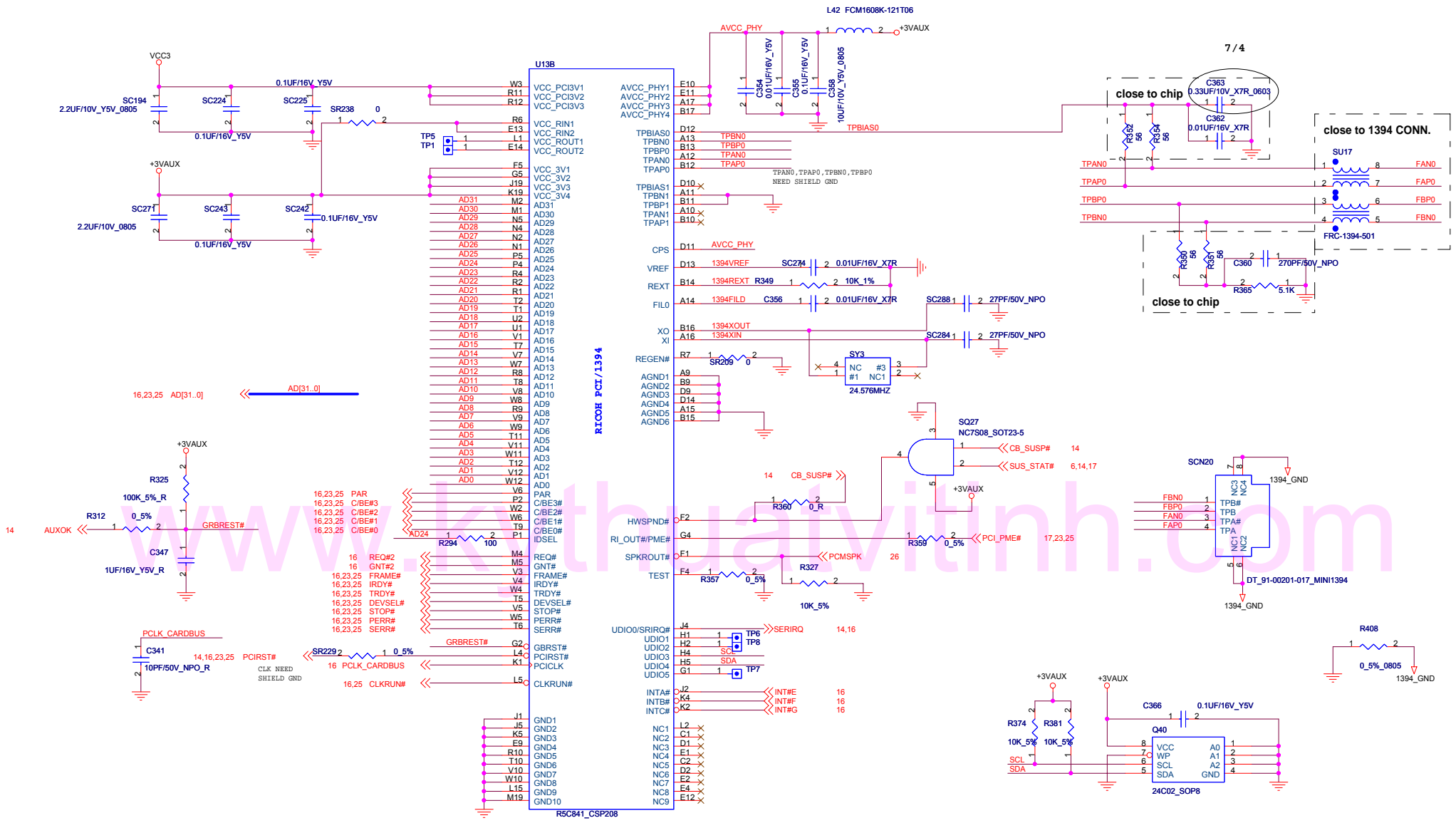
Note: Overlap common pads where possible for dual-op resistors.

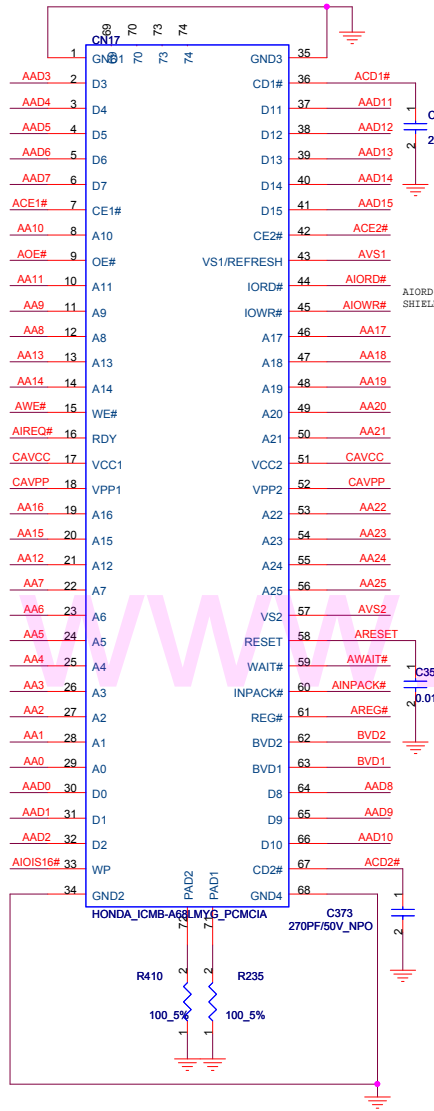


	ACPWON	AC_SDOUT	RTC_CLK	SPDIF_OUT	PCI_CLK2 PCLK_LAN	PCI_CLK3 PCLK_KBC	PCI_CLK4	PCI_CLK5	PCI_CLK6	PCI_CLK7	PCI_CLK8
PULL HIGH	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	SIO 24MHz	48MHz Crystal Pad DEFAULT	USB PHY PWRDOWN DISABLE DEFAULT	48MHz from Internal USB PLL DEFAULT	A-Link Auto Detect DEFAULT	CPU I/F = K8	ROM TYPE H,H = PCI ROM	
PULL LOW	AUTO PWR ON	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC (NOT SUPPORTED W/ IT8712)	SIO 48MHz DEFAULT	48MHz Clock Input Buffer	USB PHY PWRDOWN ENABLE	48MHz from external	A-Link 2 Lanes	CPU I/F = P4 DEFAULT	H,L = LPC ROM I LPC Address Mapped to top 4G DEFAULT	L,H = LPC ROM II LPC Address Mapped below 1M L,L = FWH ROM

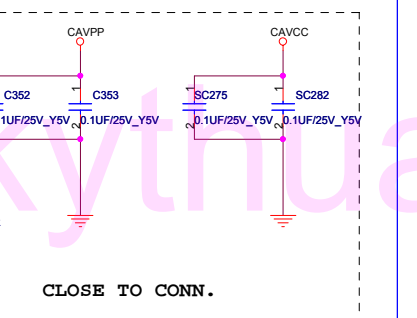
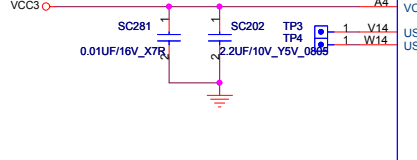
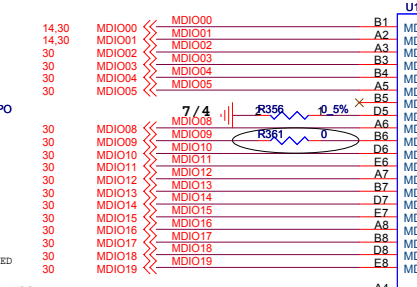
6/20



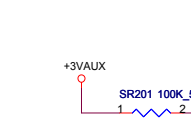
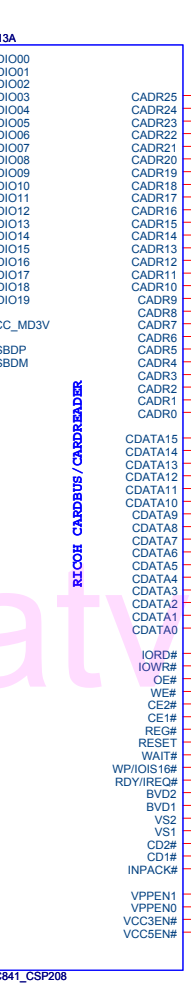
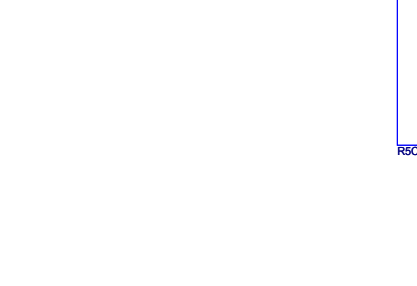




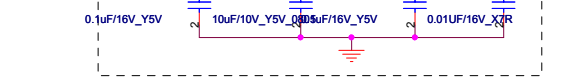
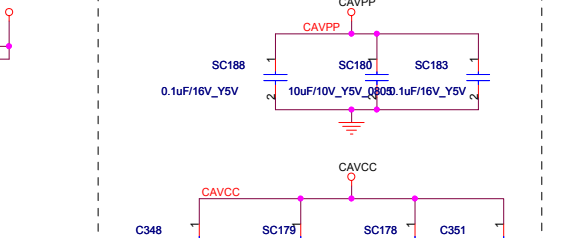
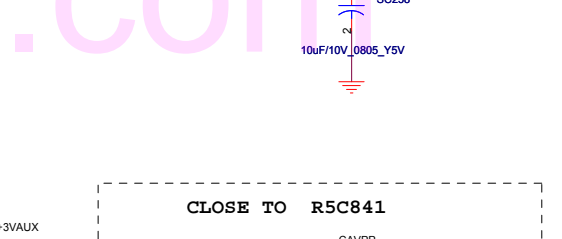
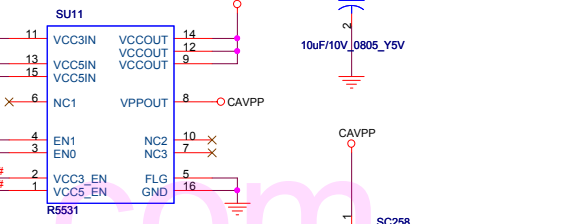
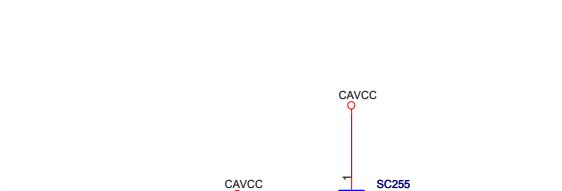
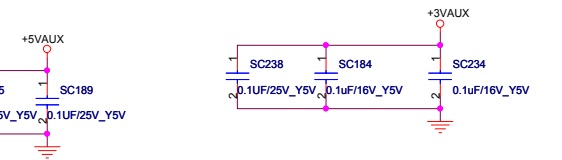
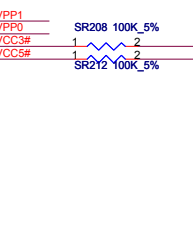
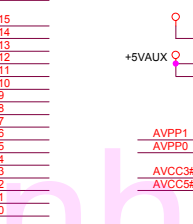
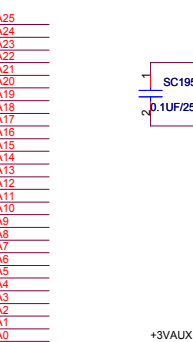
R992 ,R993 CLOSE TO R5C841 CHIP

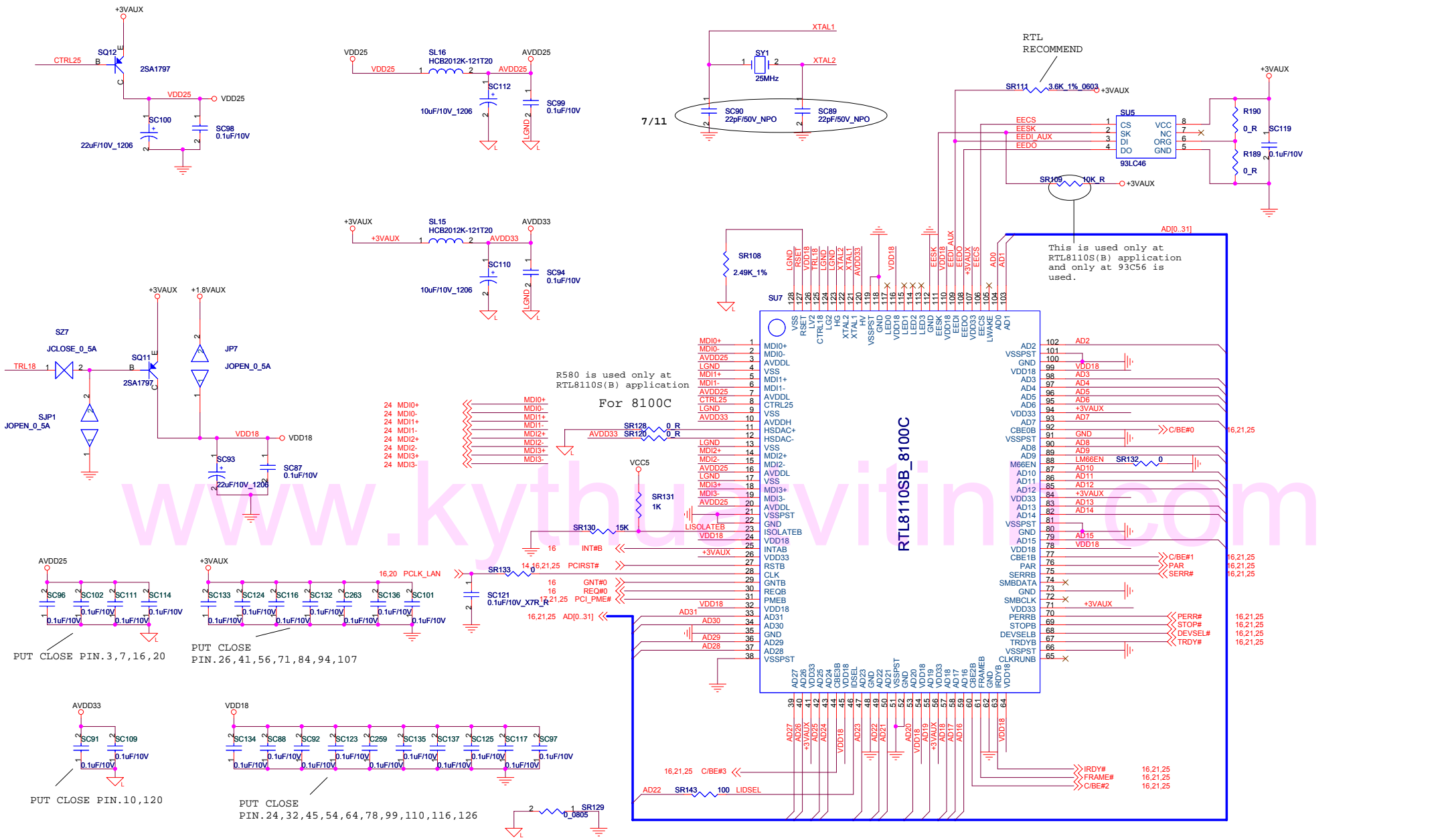


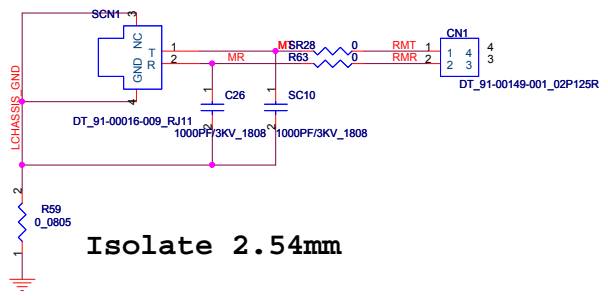
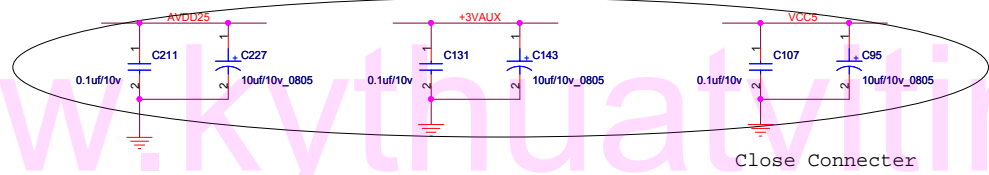
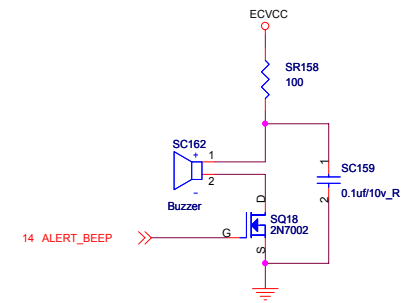
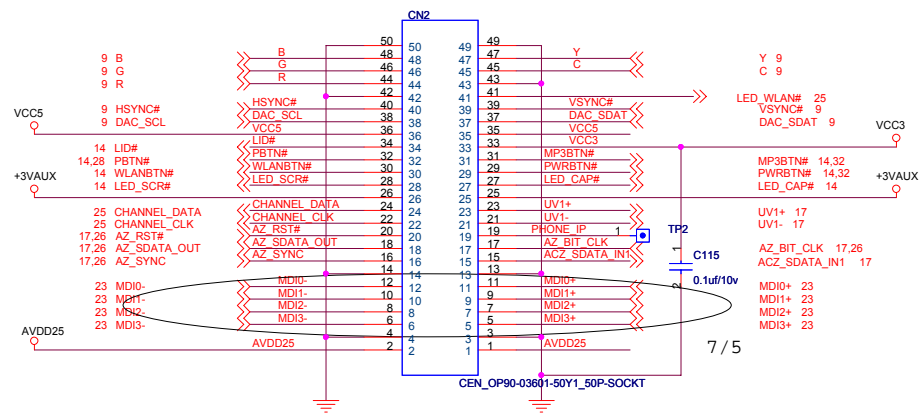
CLOSE TO CONN.



AA16 is critical signal R994 close to chip



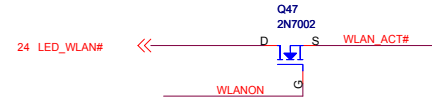




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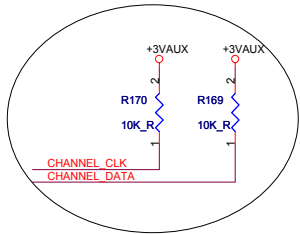
16,21,23 AD[0..31]

AD[0..31]

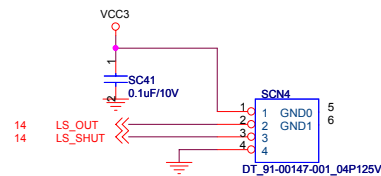
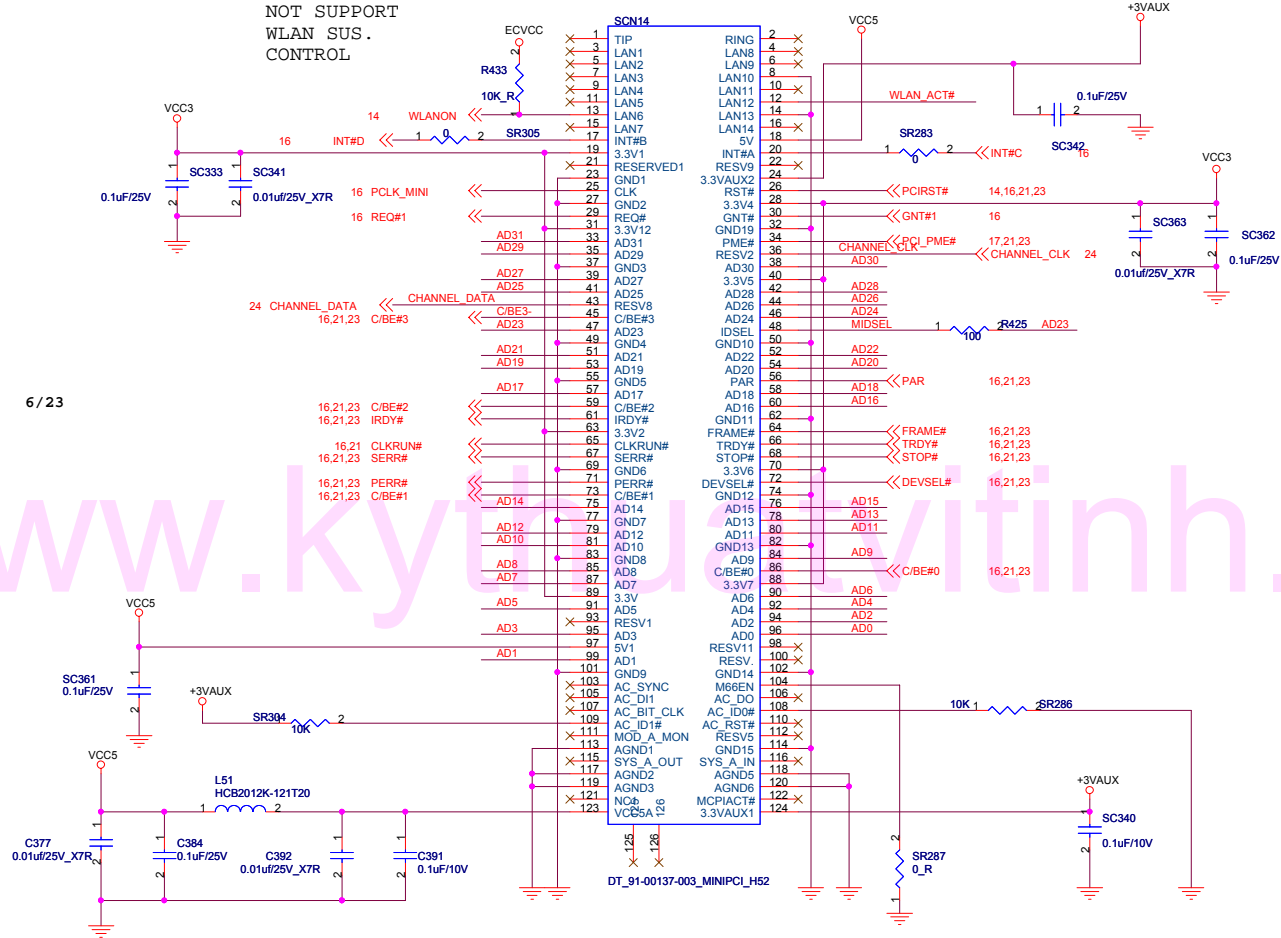


MINI PCI SOCKET

NOT SUPPORT
WLAN SUS.
CONTROL

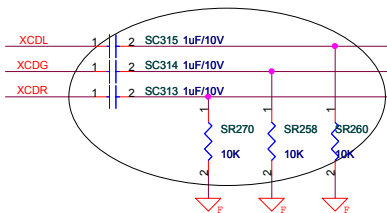
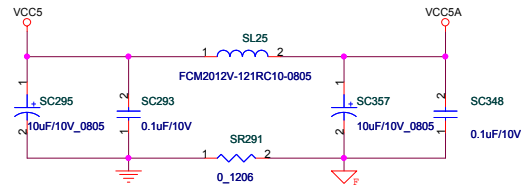
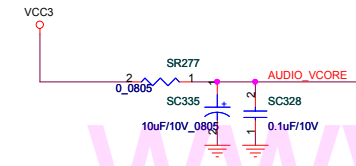
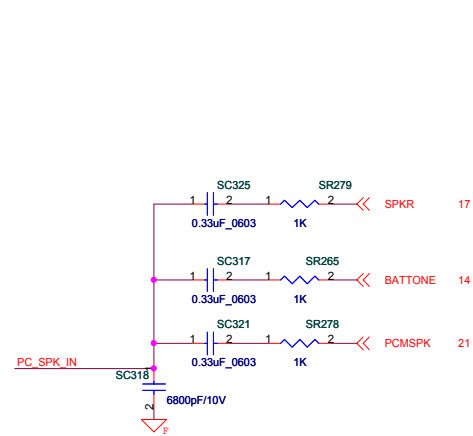


6 / 23

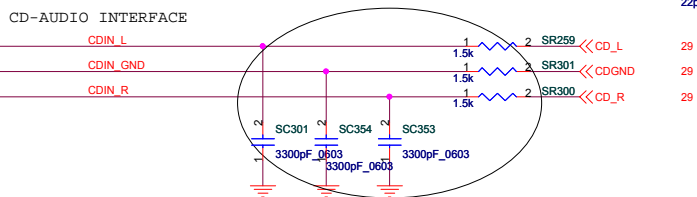


LIGHT SENSOR CONNECTOR

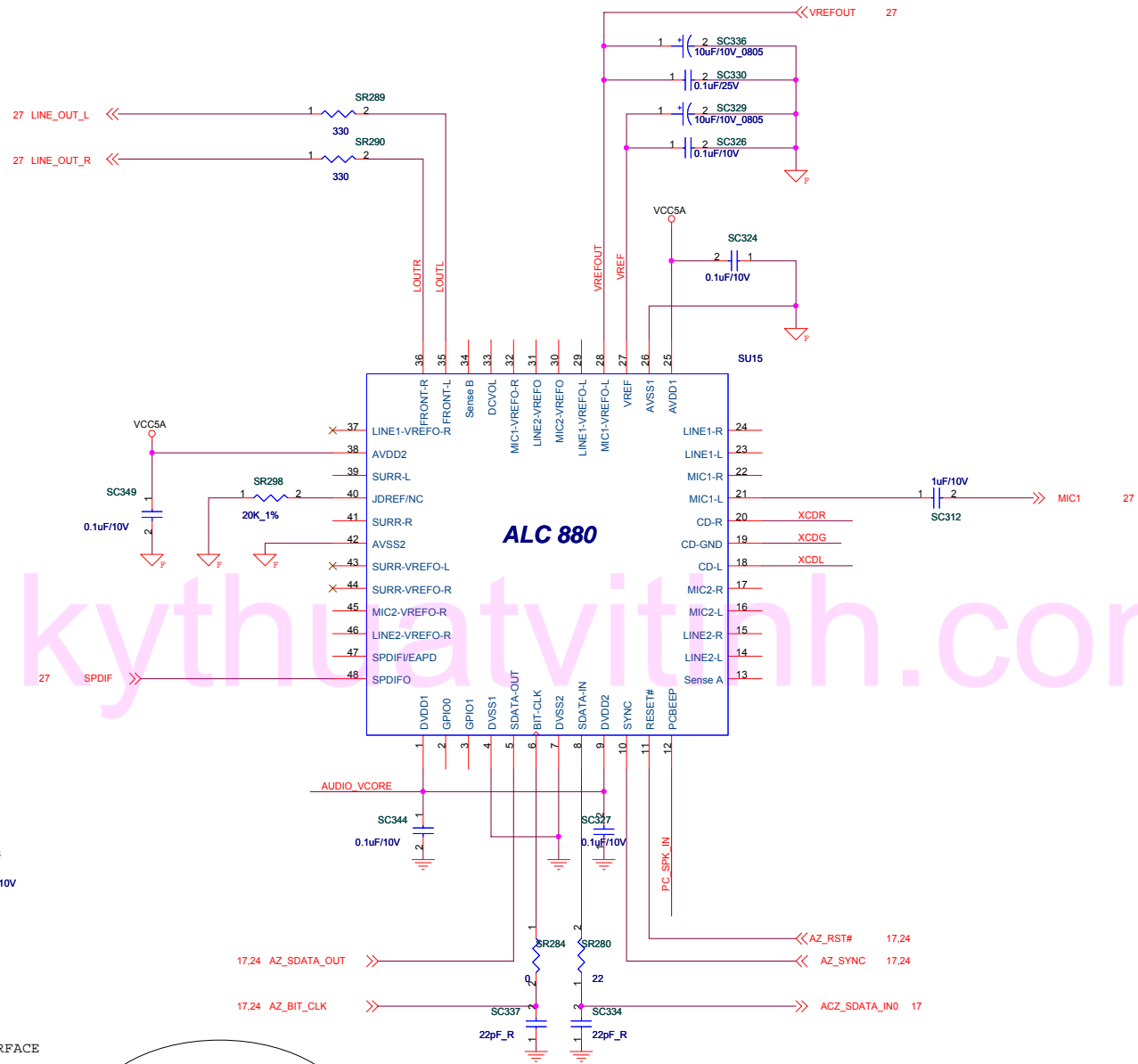
Elitegroup Computer Systems			
Title: MINIPCI&LIGHT SENSOR CONN.			
Size: Custom	Document Number: 400-1-4-01	Rev: A.0	
Date: Monday, July 11, 2005	Sheet: 25	of 35	



Close Codec

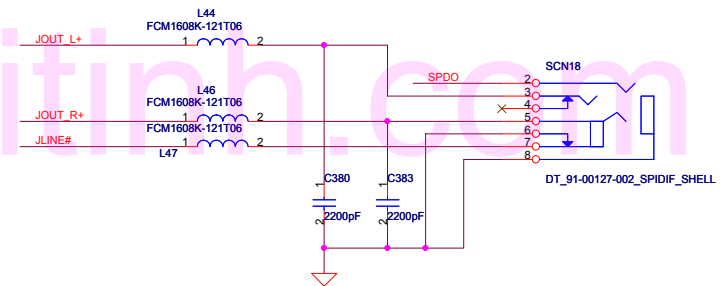
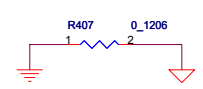
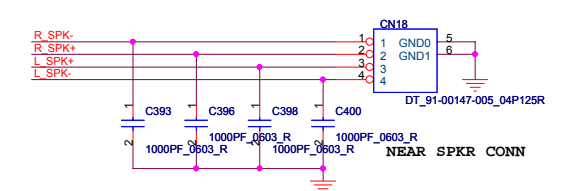
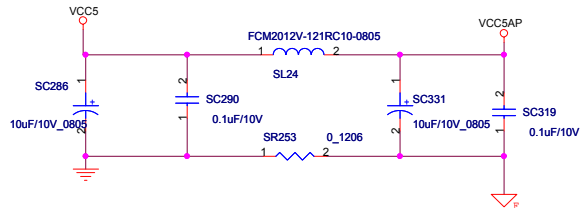
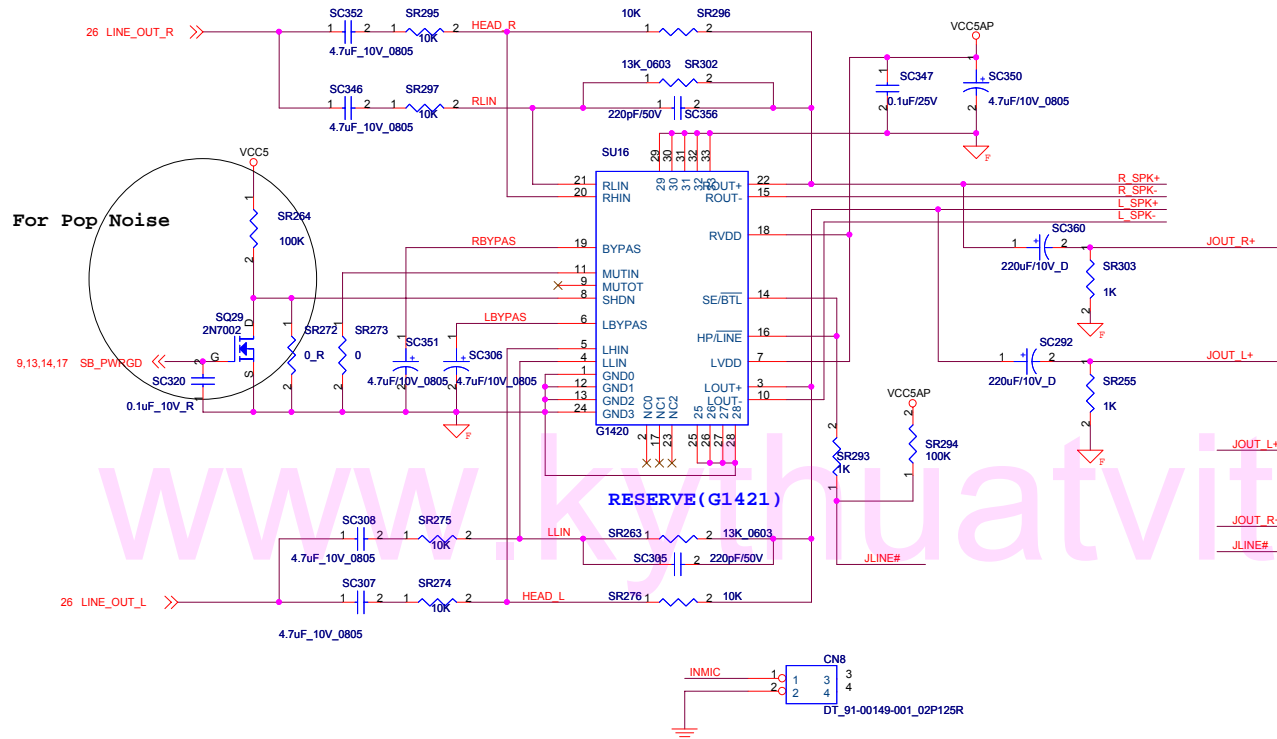


Close ODD CNR



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Elitegroup Computer Systems		
Title		
Audio Codec (ALC 880)		
Size	Document Number	Rev
Custom	400-1-4-01	A.0
Date:	Monday, July 11, 2005	Sheet 26 of 35

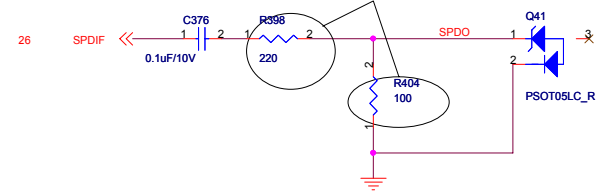


For Pop Noise

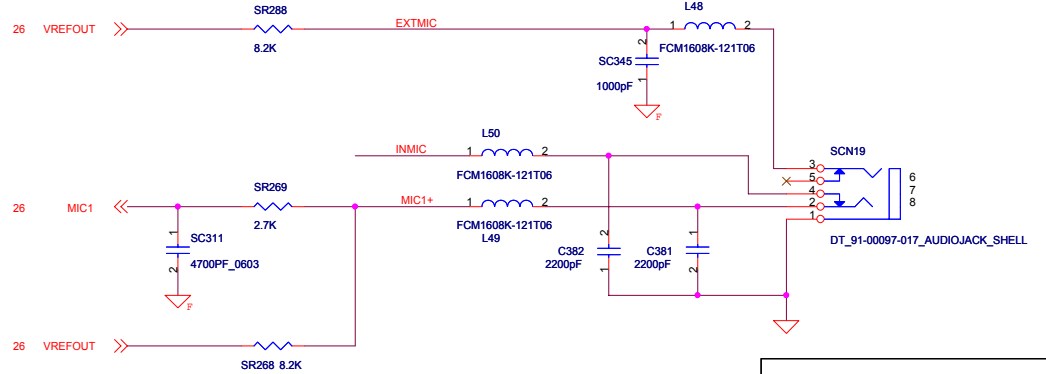
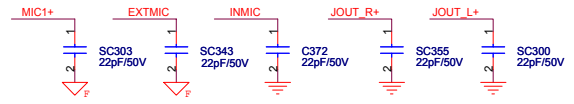
9.13.14.17 SB_PWRGD
0.1uF_10V_R

RESERVE (G1421)

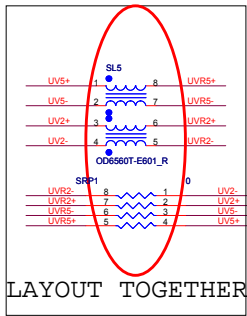
若訊號因為外部CABLE線衰減太大,將此電阻互換!!



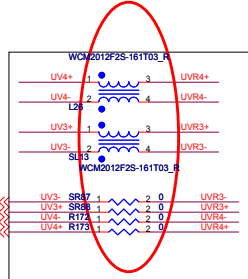
PC2001 SPEC. 12KHz--15KHz
 $F_c = 1 / [2 * 3.14 * R(2.7K) * C(4700PF)] = 12.548KHz$
 VREFOUT CONTROL MIC & REAR_OUT_R/L FUNCTION



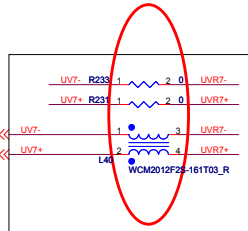
Elitegroup Computer Systems		
Title OPA & AUDIO JACK		
Size Custom	Document Number 400-1-4-01	Rev A.0
Date: Monday, July 11, 2005	Sheet 27	of 35



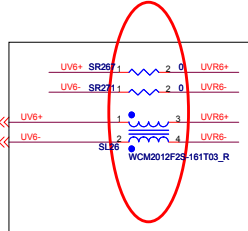
LAYOUT TOGETHER



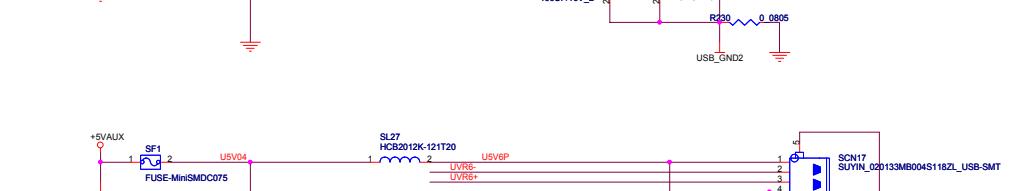
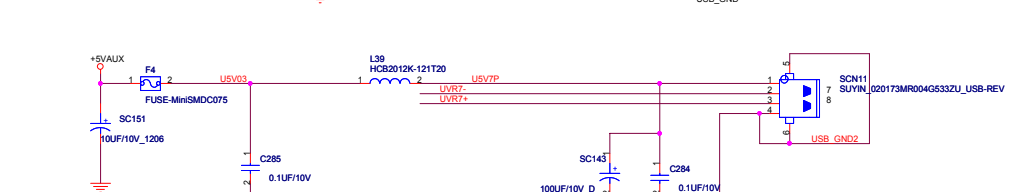
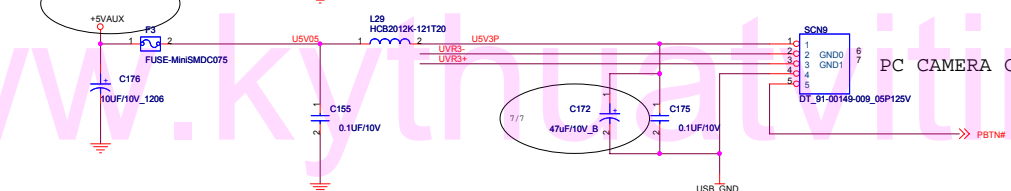
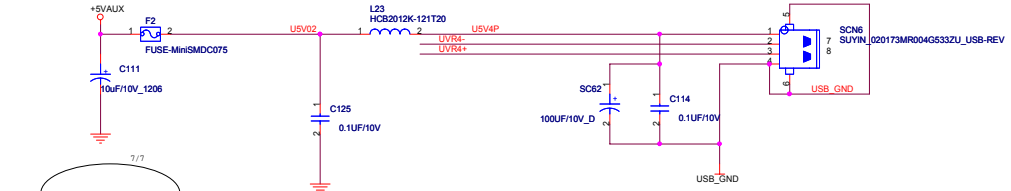
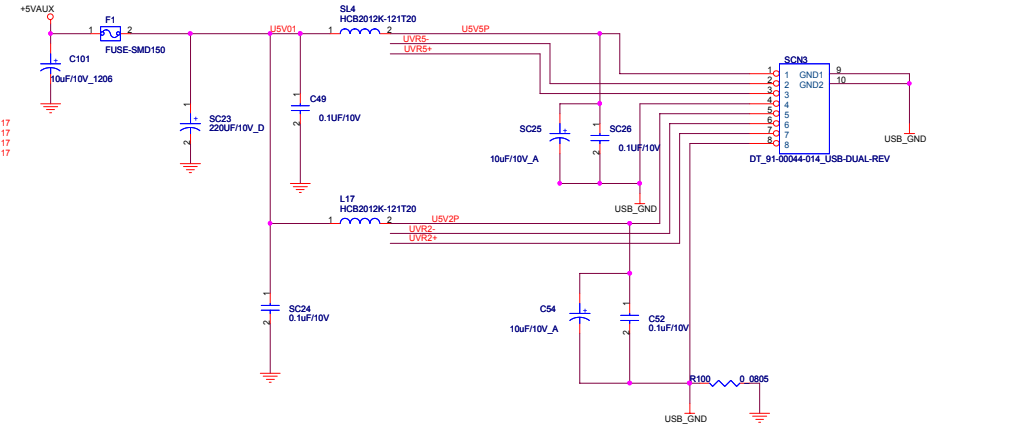
LAYOUT TOGETHER



LAYOUT TOGETHER



LAYOUT TOGETHER



ALL THIS PAGE

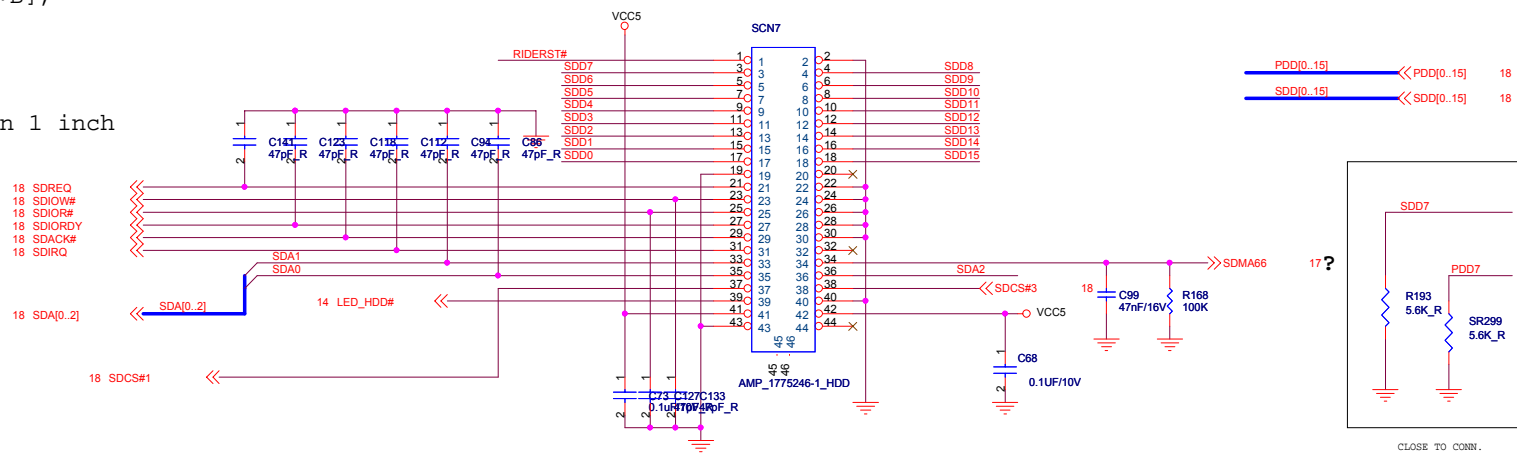
ALL THESE CLOSE TO CONNECTOR

17 UV3-
17 UV3+
17 UV4-
17 UV4+

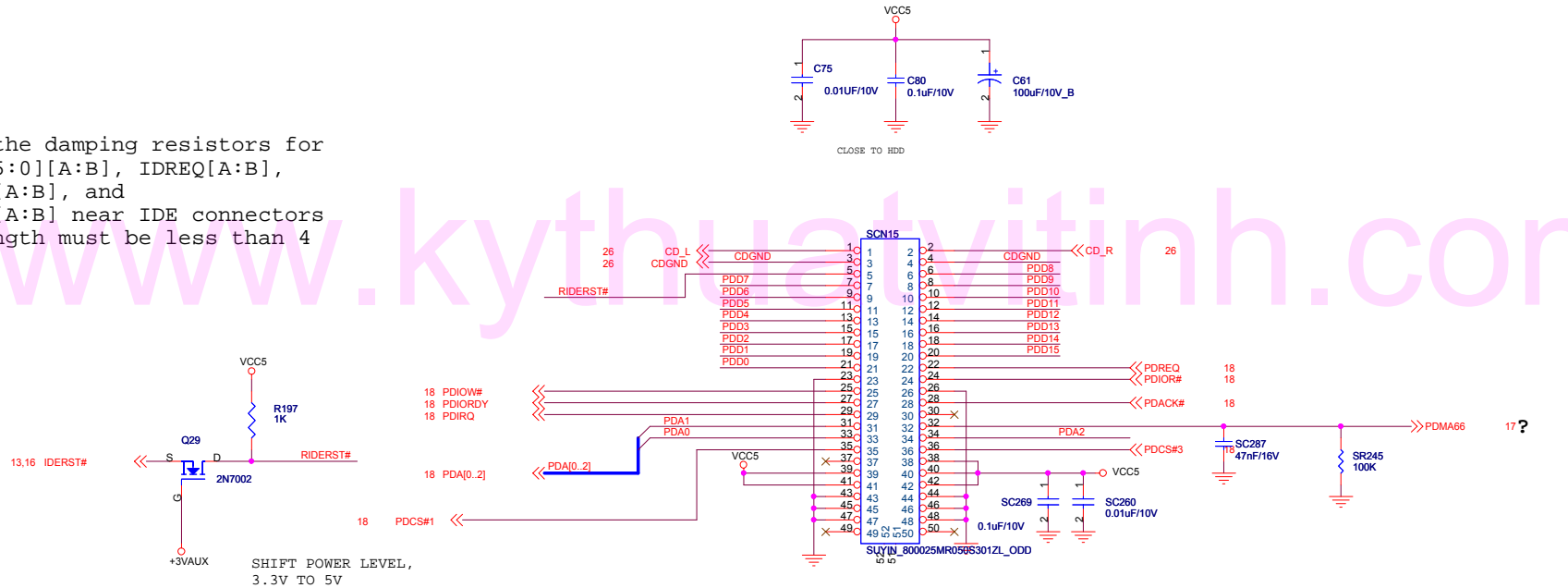
PC CAMERA CONN.

Place the damping resistors for
 IDEA[2:0][A:B], IDECS[1:0][A:B],
 IDEIOR[A:B]#, and
 IDEIOW[A:B]#, and
 IDACK[A:B]# near
 SiS962L

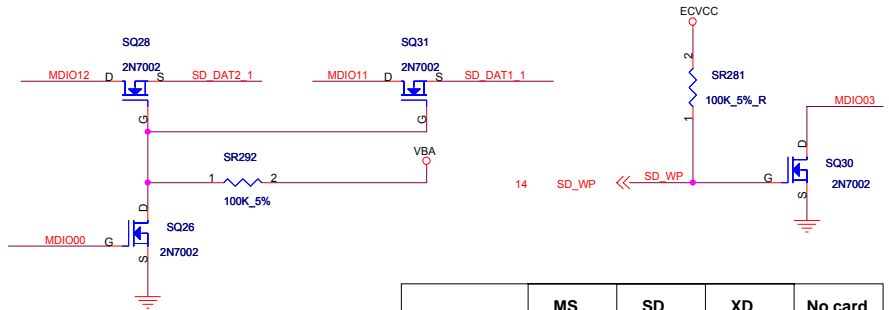
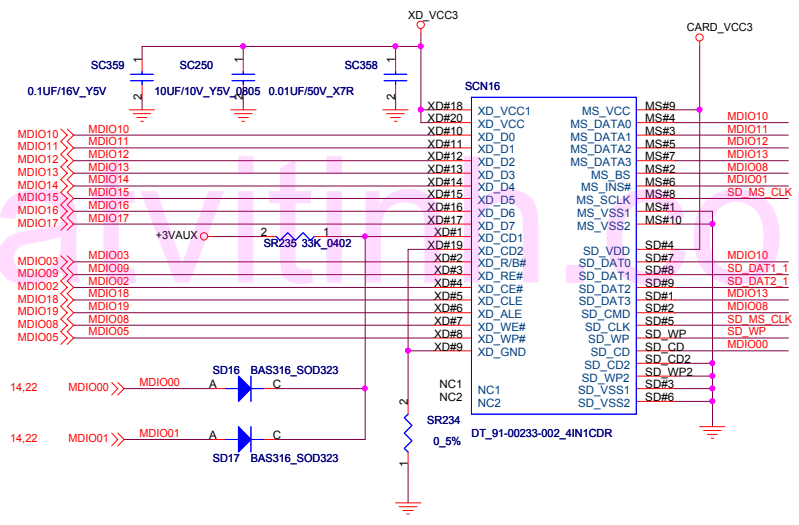
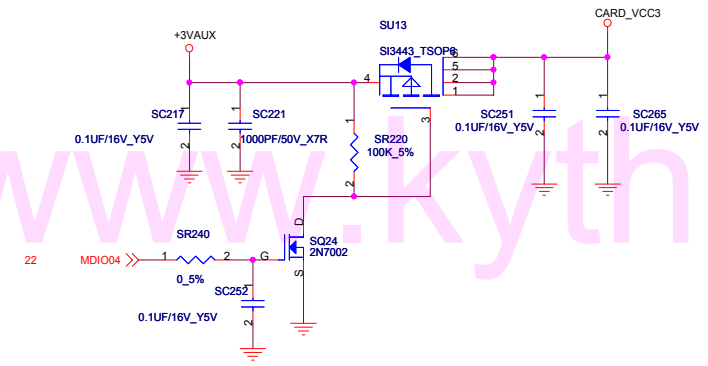
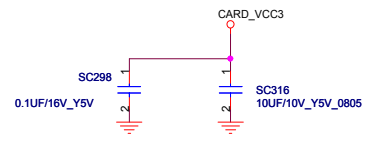
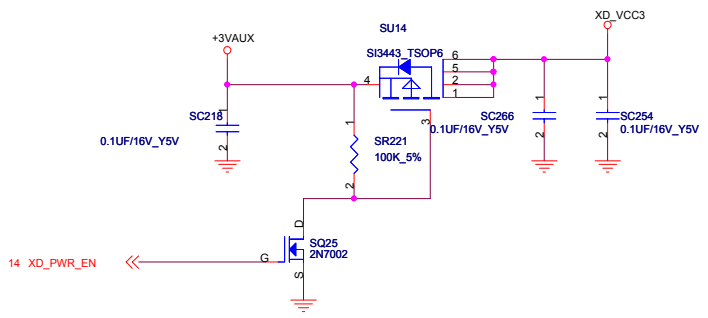
The length must be less than 1 inch



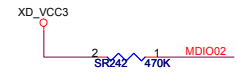
Place the damping resistors for
 IDED[15:0][A:B], IDREQ[A:B],
 ICHRDY[A:B], and
 IDEIRQ[A:B] near IDE connectors
 The length must be less than 4
 inches



CSEL : "NC" : "Hi" --> Master(CDROM) / Slave(DVDROM)
 CSEL : "Low" --> Slave(CDROM) / Master(DVDROM)



	MS	SD	XD	No card
MDIO00	HIGH	LOW	LOW	HIGH
MDIO01	LOW	HIGH	LOW	HIGH
XD_PWR_EN	LOW	LOW	HIGH	LOW
SD_WP	LOW	HIGH	LOW	LOW



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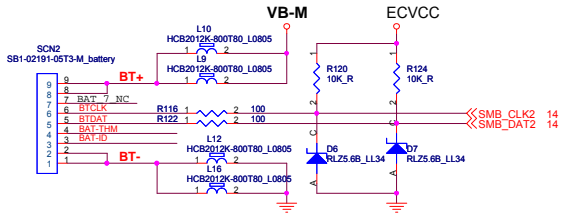
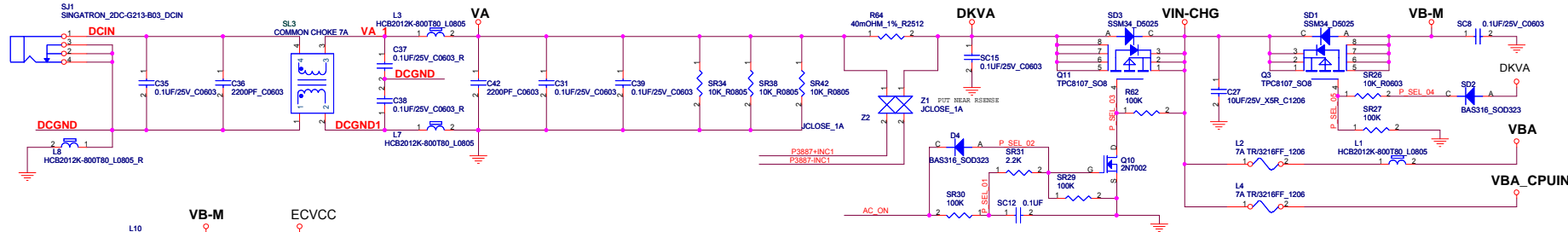
Card Reader Slot

Title: **Card Reader Slot**

Size: Custom Document Number: **400-1-4-01** Rev: A.0

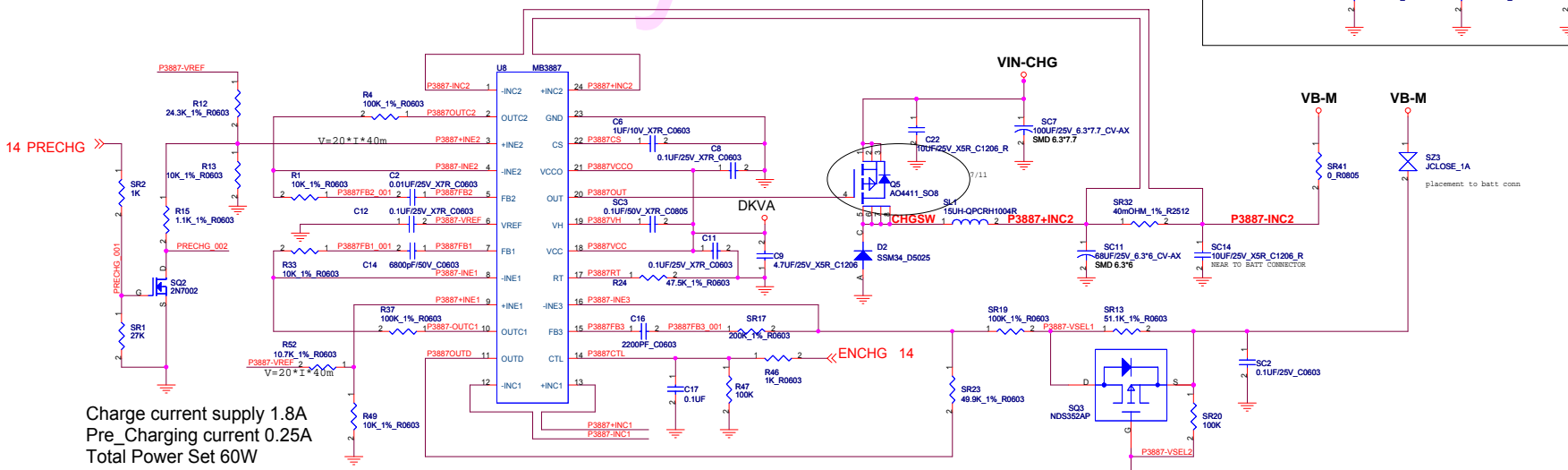
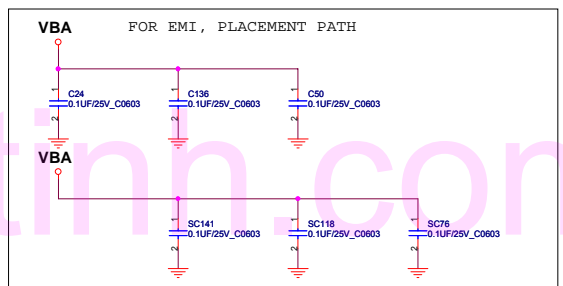
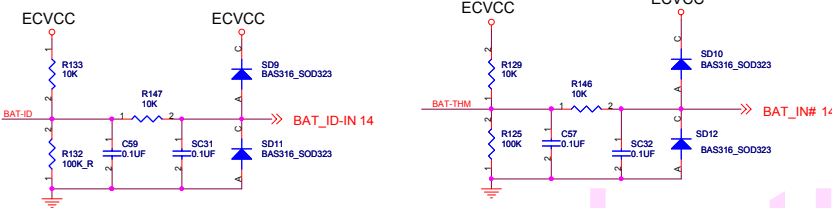
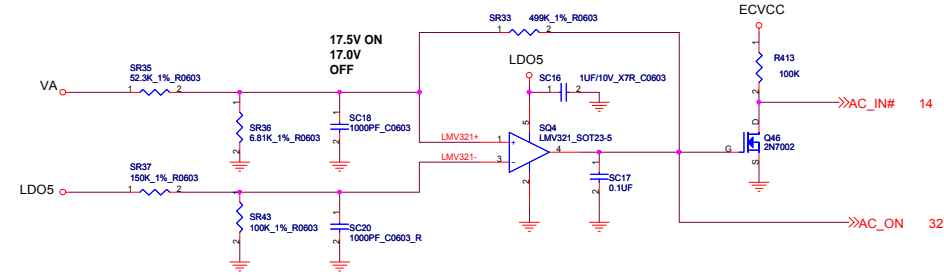
Date: Monday, July 11, 2005 Sheet: 30 of 35





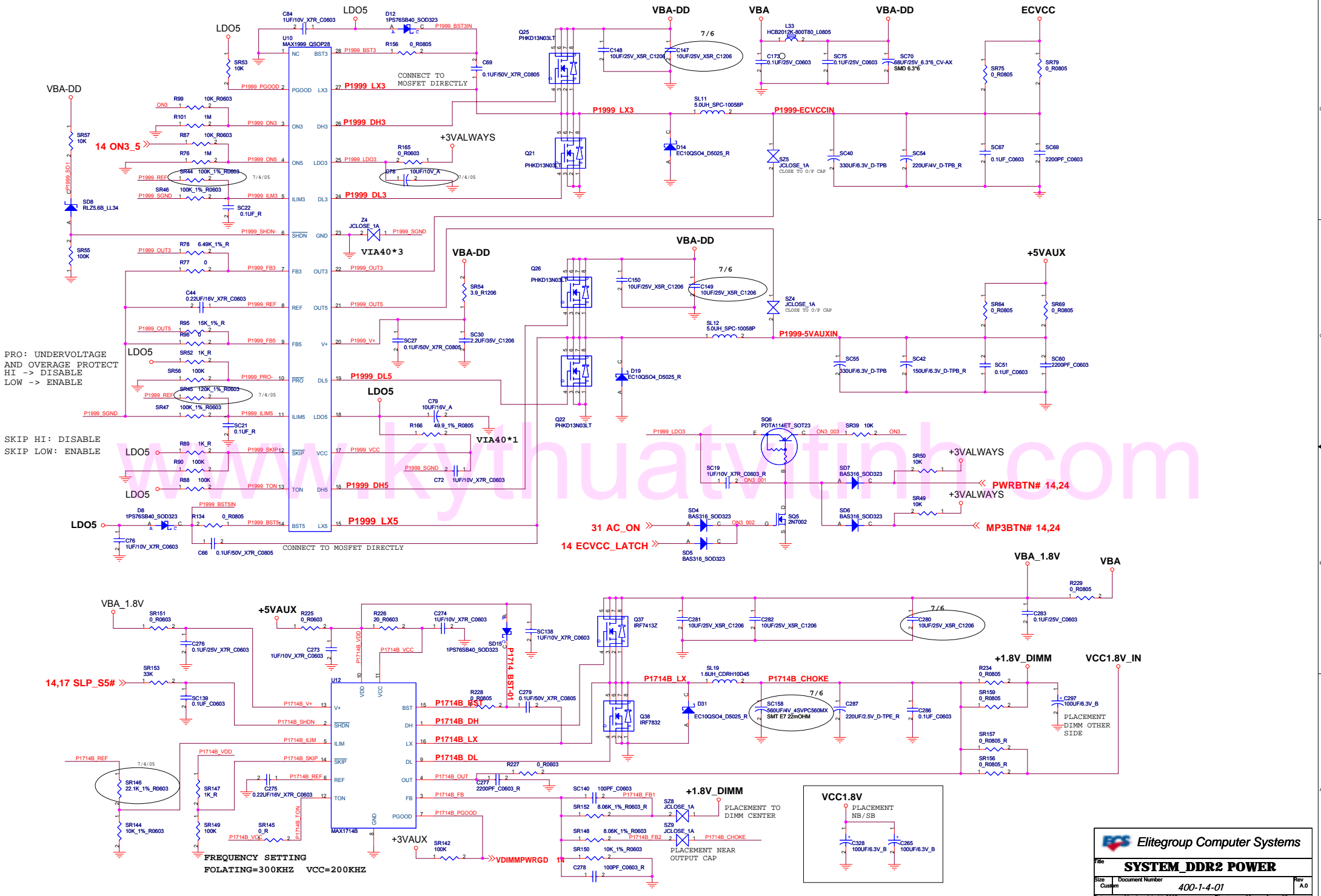
BAT-THM:
 300 ohm: Battery present
 Floating: No battery insert

BAT-ID:
 300 ohm: 4S2P 8 Cells
 Floating: 3S2P 6 Cells



Charge current supply 1.8A
 Pre-Charging current 0.25A
 Total Power Set 60W

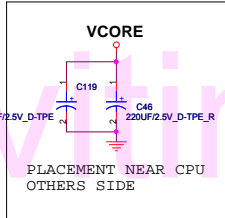
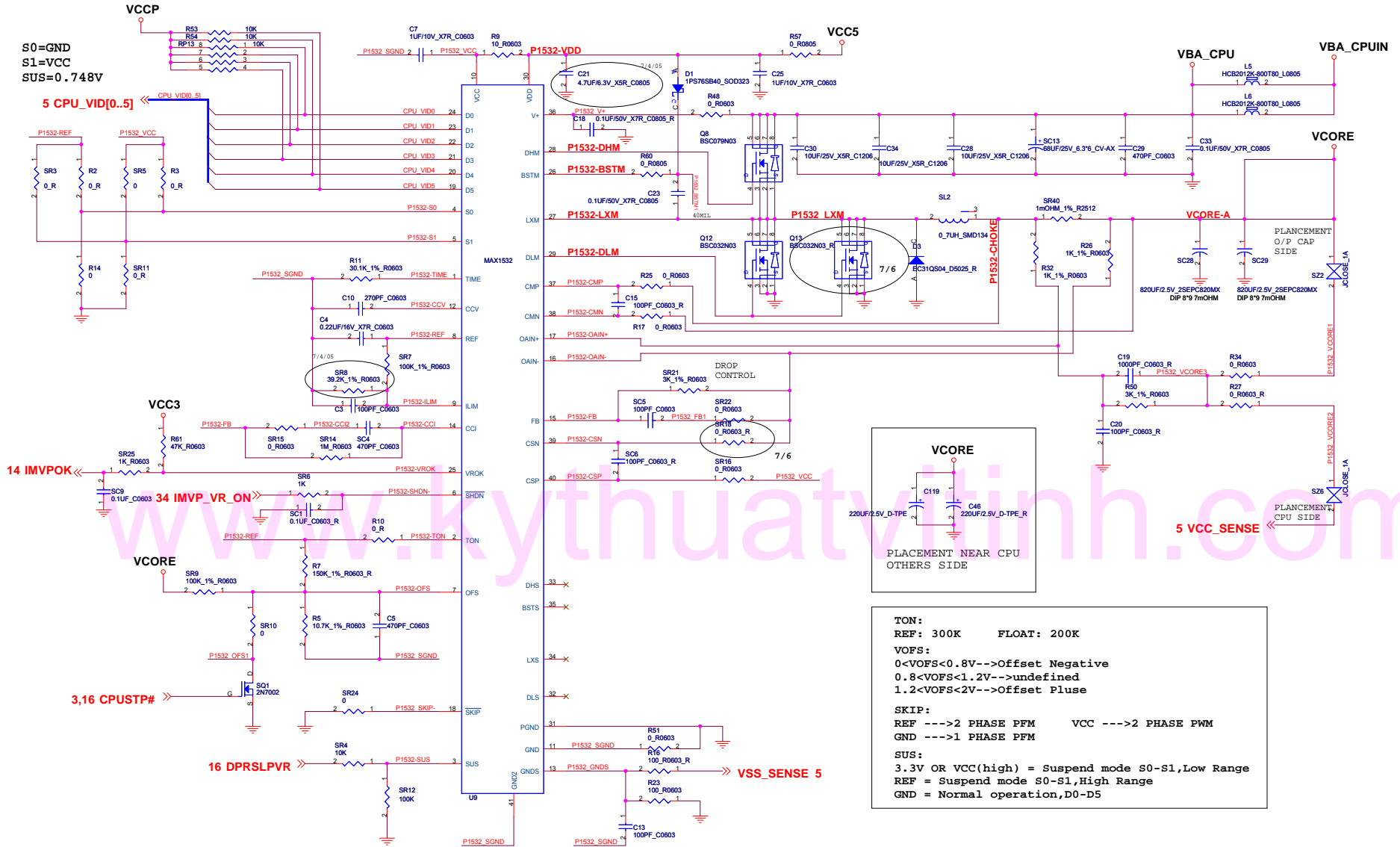
Battery 6Cell/12.6V &
 4/8Cell/16.8V



PRO: UNDERVOLTAGE AND OVERAGE PROTECT
 HI -> DISABLE
 LOW -> ENABLE

SKIP HI: DISABLE
 SKIP LOW: ENABLE

FREQUENCY SETTING
 FOLATING=300KHZ VCC=200KHZ

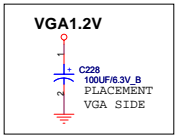
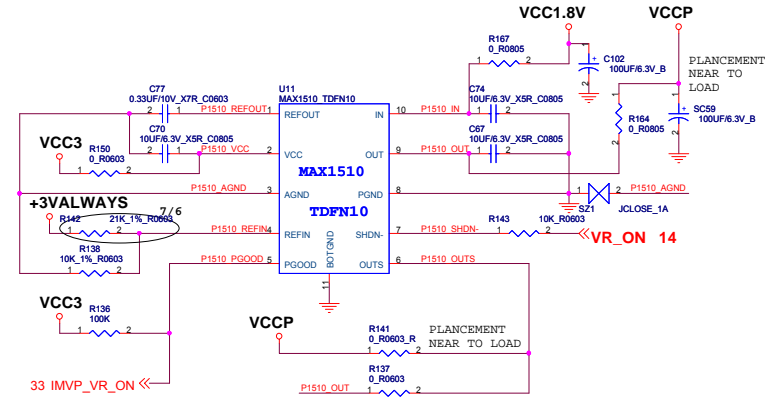
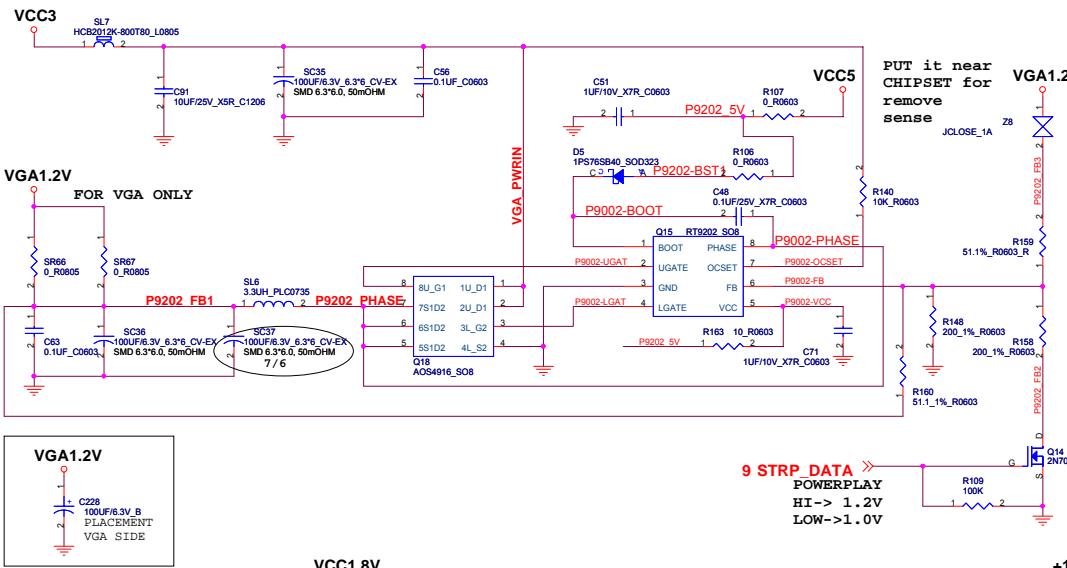


TON: REF: 300K FLOAT: 200K

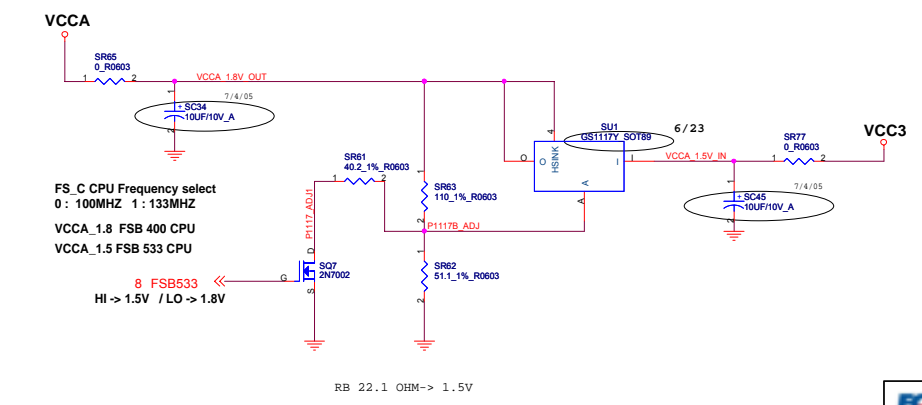
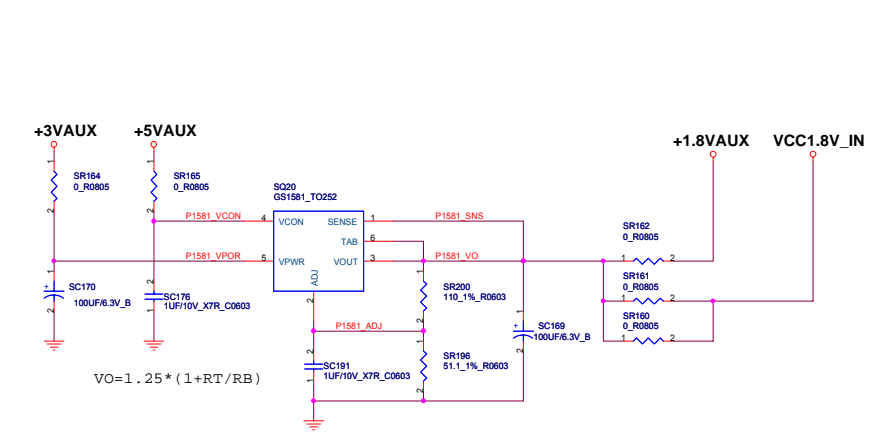
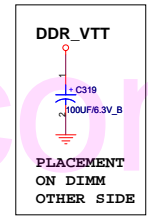
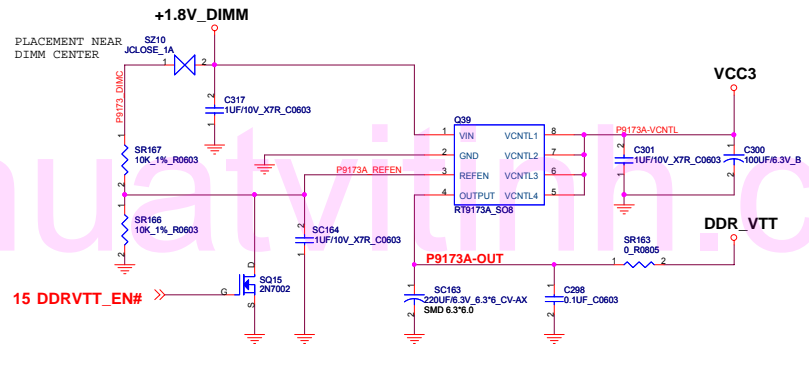
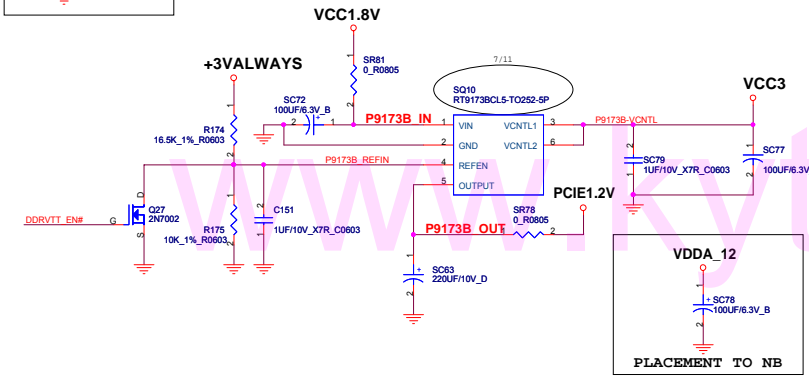
VOFS: 0<VOFS<0.8V-->Offset Negative
0.8<VOFS<1.2V-->undefined
1.2<VOFS<2V-->Offset Pluse

SKIP: REF --->2 PHASE PFM VCC --->2 PHASE PWM
GND --->1 PHASE PFM

SUS: 3.3V OR VCC(high) = Suspend mode S0-S1, Low Range
REF = Suspend mode S0-S1, High Range
GND = Normal operation, D0-D5



9 STRP_DATA POWERPLAY
 HI -> 1.2V
 LOW -> 1.0V




FS_C CPU Frequency select
 0 : 100MHZ 1 : 133MHZ
 VCCA_1.8 FSB 400 CPU
 VCCA_1.5 FSB 533 CPU
 8 FSB533
 HI -> 1.5V / LO -> 1.8V

RB 22.1 OHM -> 1.5V

V.A: 2005/07/11 Initial Release 15-F66-010010

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 Elitegroup Computer Systems		
Title History		
Size	Document Number	Rev
Custom	400-1-4-01	A.0
Date:	Monday, July 11, 2005	Sheet 35 of 35