


P/N :
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REV																					
DATE																					

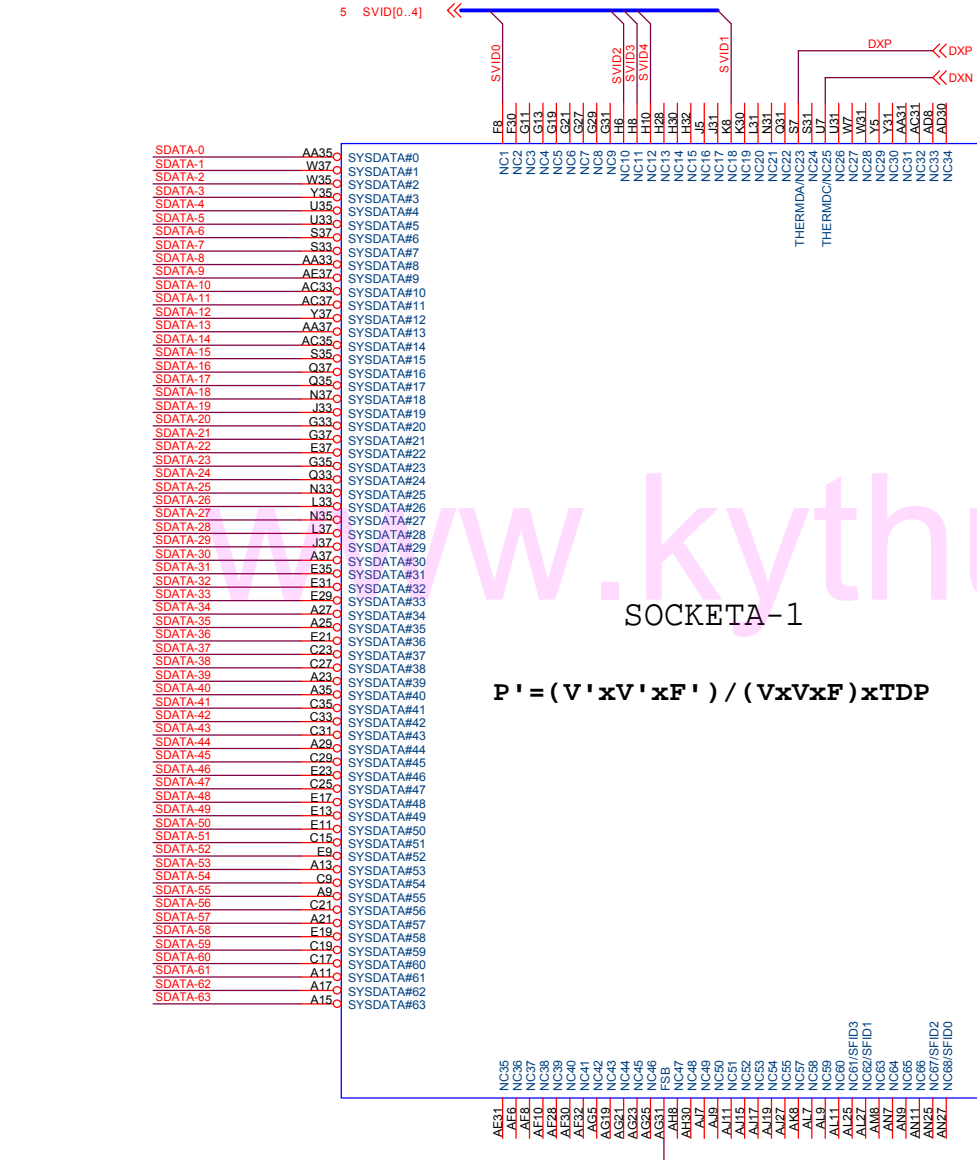
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DATE																				

Designed	by	Checked	by	Approved	by

 Elitegroup Computer Systems		Tit	
		COVER PAGE	
Size	Document Number	Rev	
B	A535-1-4-01	2.3	
Date:	Tuesday, May 25, 2004	Sheet	1 of 39

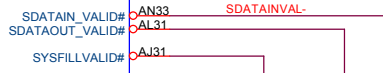
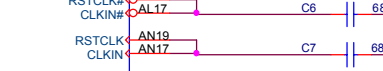
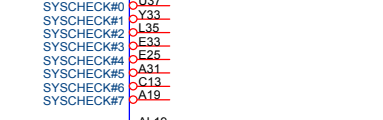
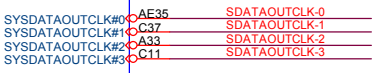
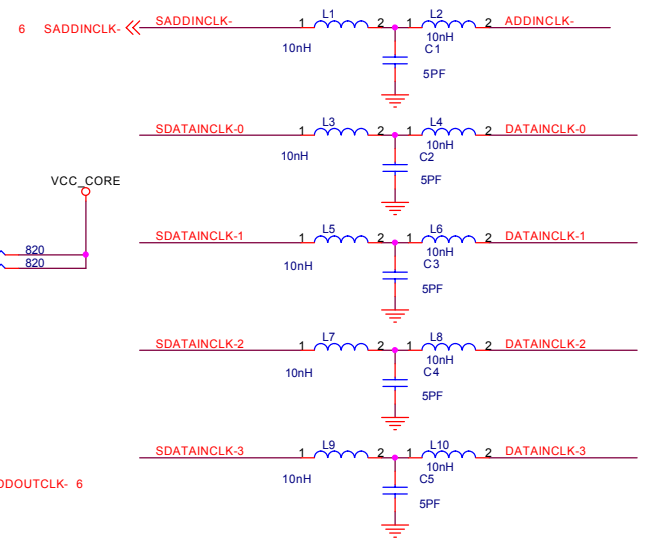
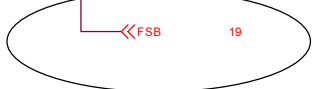
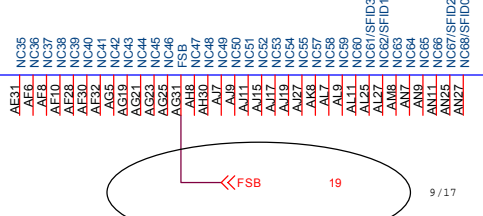
P. Leader

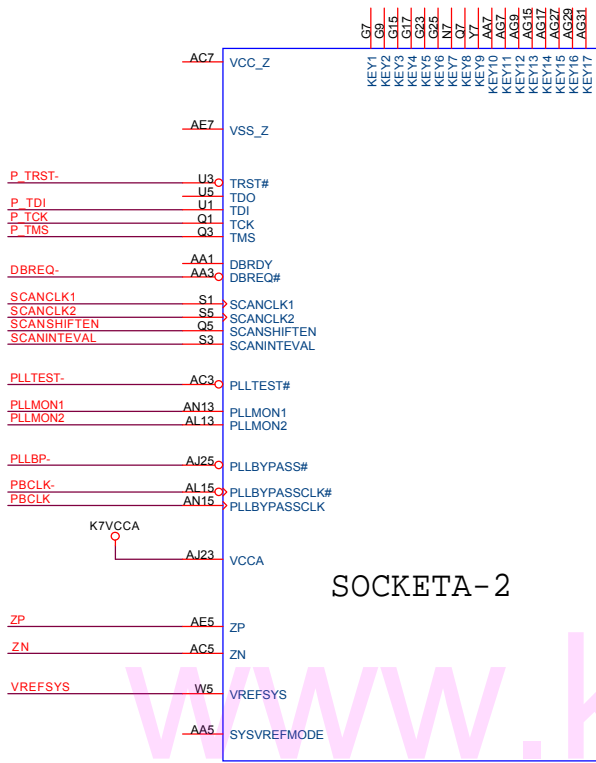
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 6 SDATAOUTCLK-[0..3] << SDATAOUTCLK-[0..3]
 6 SADDIN-[2..14] << SADDIN-[2..14]
 6 SADDOUT-[2..14] << SADDOUT-[2..14]
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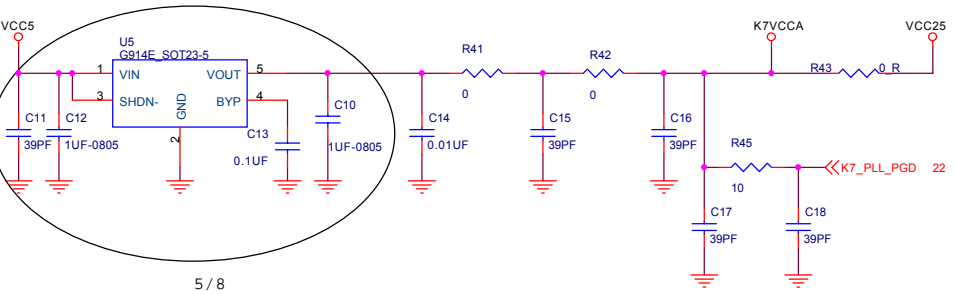
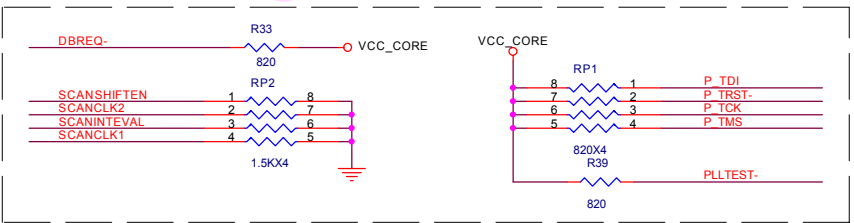
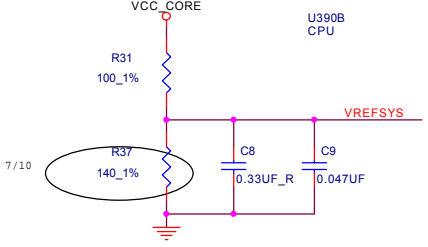
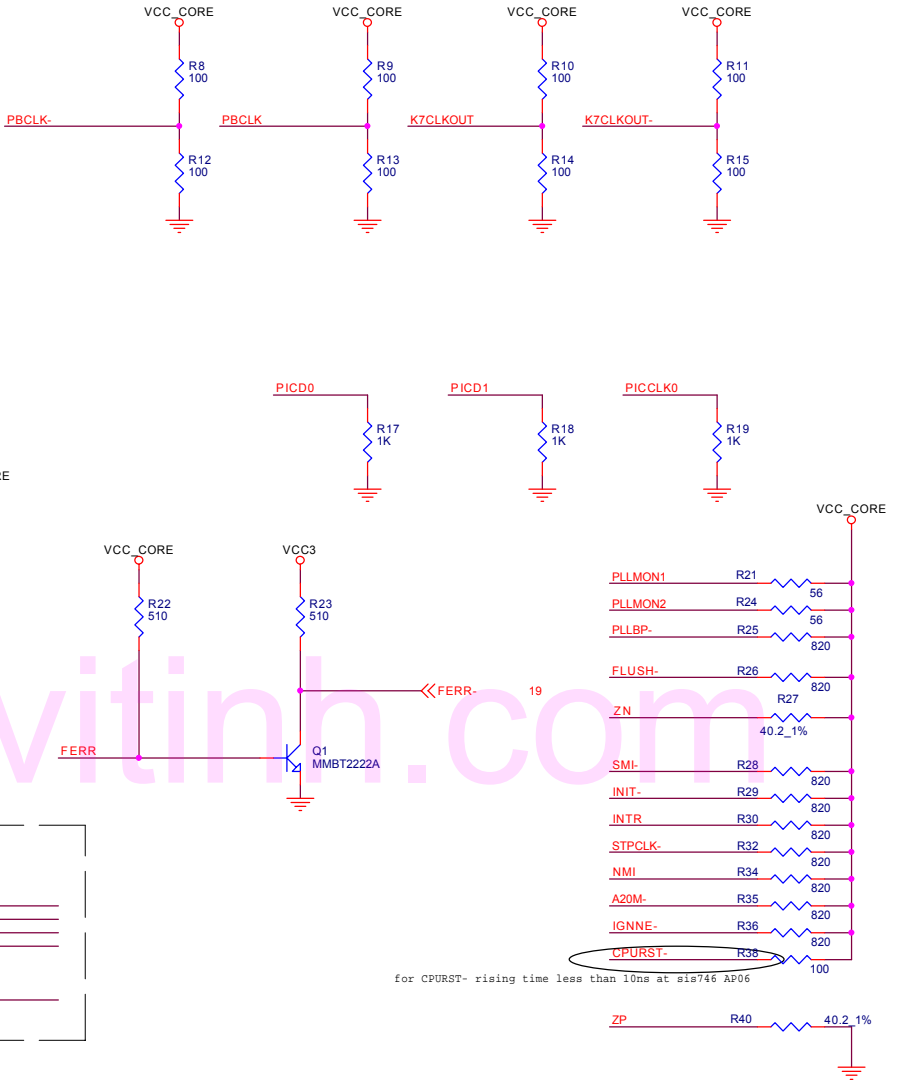
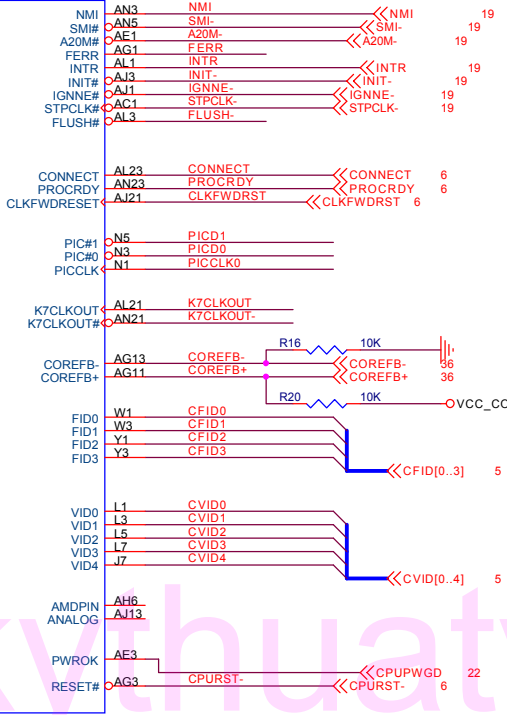
SOCKET A-1

$$P' = (V'xV'xXF') / (VxVxXF) xTDP$$





SOCKETA-2



VCC_CORE

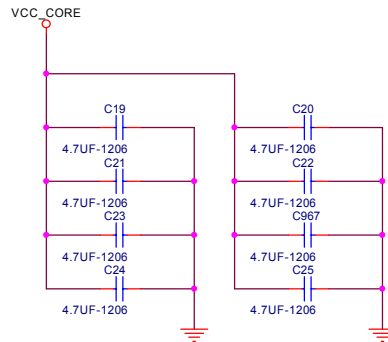
U390C

AB30 VCC_CORE1
 AB32 VCC_CORE2
 AB34 VCC_CORE3
 AB36 VCC_CORE4
 AD2 VCC_CORE5
 AD4 VCC_CORE6
 AD6 VCC_CORE7
 AF14 VCC_CORE8
 AF18 VCC_CORE9
 AF22 VCC_CORE10
 AF26 VCC_CORE11
 AF34 VCC_CORE12
 AF36 VCC_CORE13
 AH10 VCC_CORE14
 AH14 VCC_CORE15
 AH18 VCC_CORE16
 AH2 VCC_CORE17
 AH22 VCC_CORE18
 AH26 VCC_CORE19
 AH4 VCC_CORE20
 AJ6 VCC_CORE21
 AK10 VCC_CORE22
 AK14 VCC_CORE23
 AK18 VCC_CORE24
 AK22 VCC_CORE25
 AK26 VCC_CORE26
 AK30 VCC_CORE27
 AK34 VCC_CORE28
 AK36 VCC_CORE29
 AL5 VCC_CORE30
 AM10 VCC_CORE31
 AM14 VCC_CORE32
 AM18 VCC_CORE33
 AM2 VCC_CORE34
 AM22 VCC_CORE35
 AM26 VCC_CORE36
 AM30 VCC_CORE37
 AM34 VCC_CORE38
 B12 VCC_CORE39
 B16 VCC_CORE40
 B20 VCC_CORE41
 B24 VCC_CORE42
 B28 VCC_CORE43
 B32 VCC_CORE44
 B36 VCC_CORE45
 B4 VCC_CORE46
 B8 VCC_CORE47
 D12 VCC_CORE48
 D16 VCC_CORE49
 D2 VCC_CORE50
 D20 VCC_CORE51
 D24 VCC_CORE52
 D28 VCC_CORE53
 D32 VCC_CORE54
 D4 VCC_CORE55
 D8 VCC_CORE56
 F12 VCC_CORE57
 F20 VCC_CORE58
 F24 VCC_CORE59
 F28 VCC_CORE60
 F32 VCC_CORE61
 F34 VCC_CORE62
 F36 VCC_CORE63
 H12 VCC_CORE64
 H16 VCC_CORE65
 H2 VCC_CORE66
 H20 VCC_CORE67
 H24 VCC_CORE68
 H4 VCC_CORE69
 H4 VCC_CORE70
 K32 VCC_CORE71
 K34 VCC_CORE72
 K36 VCC_CORE73
 M2 VCC_CORE74
 M4 VCC_CORE75
 M6 VCC_CORE76
 M8 VCC_CORE77
 P30 VCC_CORE78
 P32 VCC_CORE79
 P34 VCC_CORE80
 P36 VCC_CORE81
 R2 VCC_CORE82
 R4 VCC_CORE83
 R6 VCC_CORE84
 R8 VCC_CORE85
 T30 VCC_CORE86
 T32 VCC_CORE87
 T34 VCC_CORE88
 T36 VCC_CORE89
 V2 VCC_CORE90
 V4 VCC_CORE91
 V6 VCC_CORE92
 V8 VCC_CORE93
 X30 VCC_CORE94
 X32 VCC_CORE95
 X34 VCC_CORE96
 X36 VCC_CORE97
 Z2 VCC_CORE98
 Z4 VCC_CORE99
 Z6 VCC_CORE100
 Z8 VCC_CORE101

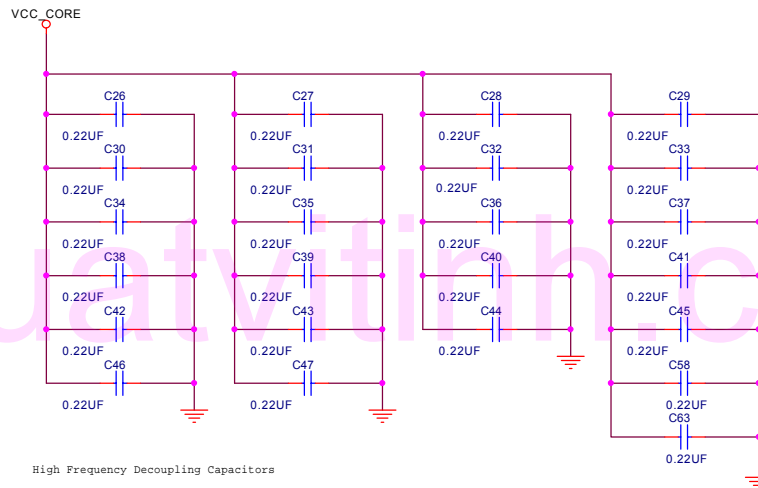
CPU

VSS1 AB2
 VSS2 AB4
 VSS3 AB6
 VSS4 AB8
 VSS5 AD32
 VSS6 AD34
 VSS7 AD36
 VSS8 AF12
 VSS9 AF16
 VSS10 AF2
 VSS11 AF20
 VSS12 AF24
 VSS13 AF4
 VSS14 AH12
 VSS15 AH16
 VSS16 AH20
 VSS17 AH24
 VSS18 AH28
 VSS19 AH32
 VSS20 AH34
 VSS21 AH36
 VSS22 AK12
 VSS23 AK16
 VSS24 AK2
 VSS25 AK20
 VSS26 AK24
 VSS27 AK28
 VSS28 AK32
 VSS29 AK4
 VSS30 AK6
 VSS31 AM12
 VSS32 AM16
 VSS33 AM20
 VSS34 AM24
 VSS35 AM28
 VSS36 AM32
 VSS37 AM36
 VSS38 AM4
 VSS39 AM6
 VSS40 B10
 VSS41 B14
 VSS42 B18
 VSS43 B22
 VSS44 B26
 VSS45 B30
 VSS46 B34
 VSS47 B6
 VSS48 D10
 VSS49 D14
 VSS50 D18
 VSS51 D22
 VSS52 D26
 VSS53 D30
 VSS54 D34
 VSS55 D6
 VSS56 D6
 VSS57 D6
 VSS58 F14
 VSS59 F18
 VSS60 F2
 VSS61 F22
 VSS62 F26
 VSS63 F4
 VSS64 F6
 VSS65 H14
 VSS66 H18
 VSS67 H22
 VSS68 H26
 VSS69 H34
 VSS70 H36
 VSS71 K2
 VSS72 K4
 VSS73 K6
 VSS74 M30
 VSS75 M32
 VSS76 M34
 VSS77 M36
 VSS78 P2
 VSS79 P4
 VSS80 P6
 VSS81 P8
 VSS82 R30
 VSS83 R32
 VSS84 R34
 VSS85 R36
 VSS86 R32
 VSS87 T2
 VSS88 T4
 VSS89 T6
 VSS90 T8
 VSS91 V30
 VSS92 V32
 VSS93 V34
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 VSS100 Z32
 VSS101 Z34
 VSS102 Z36

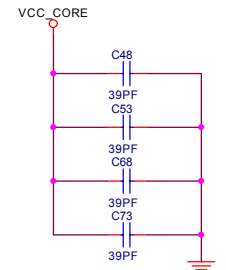
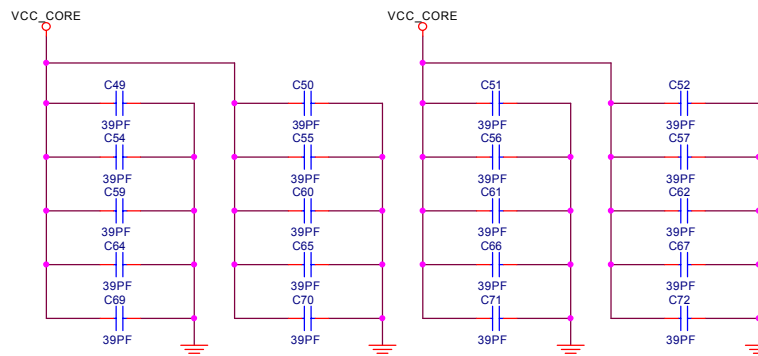
High Frequency Decoupling Capacitors




High Frequency Decoupling Capacitors

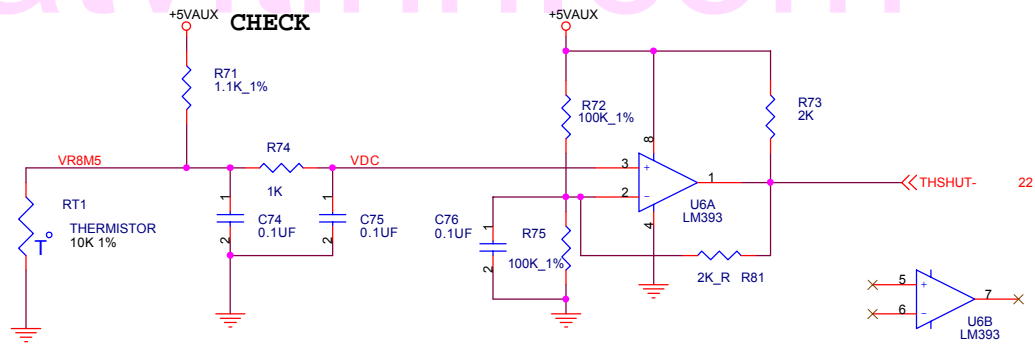
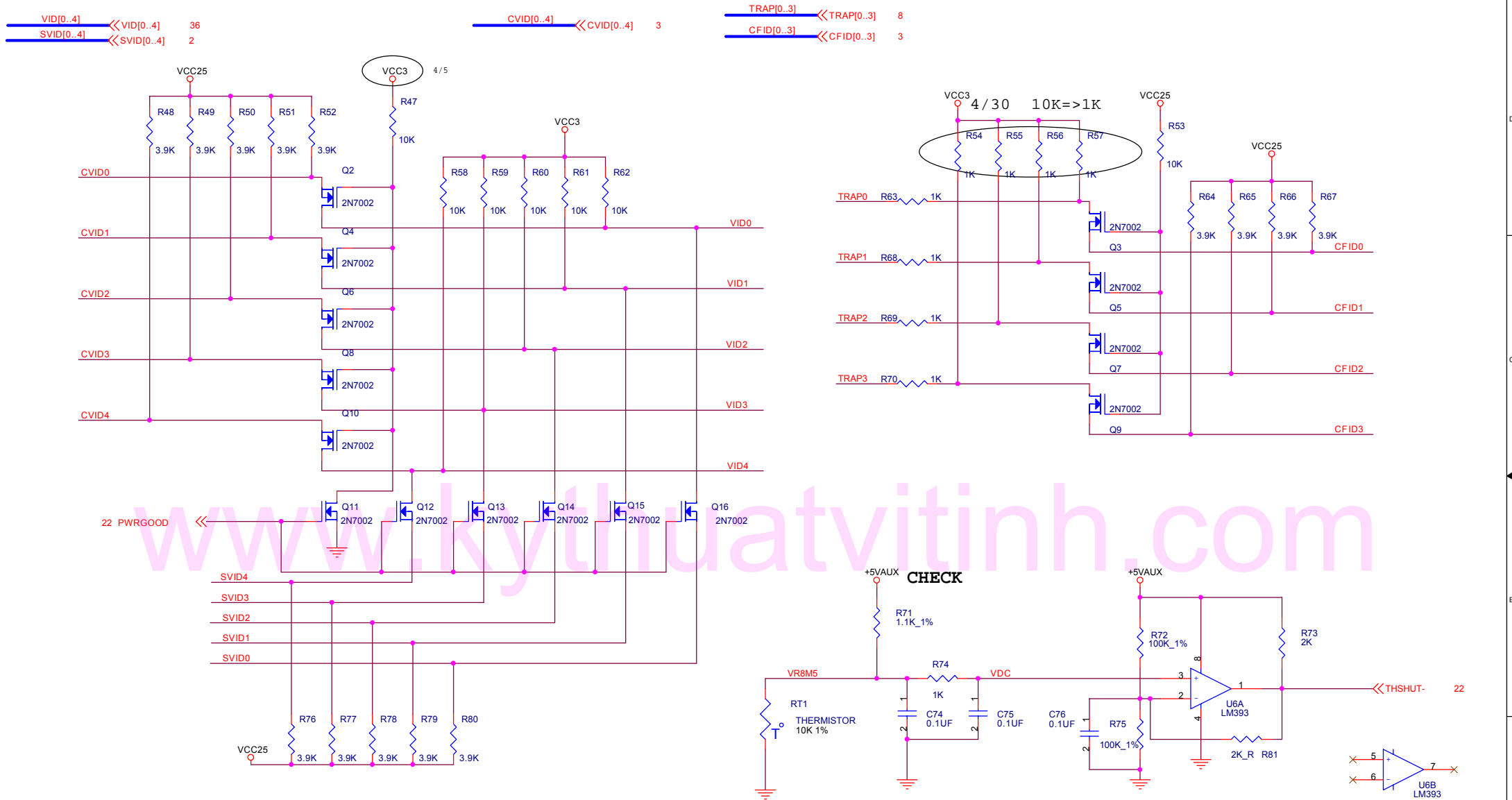



High Frequency Decoupling Capacitors

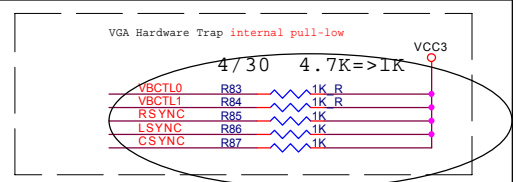
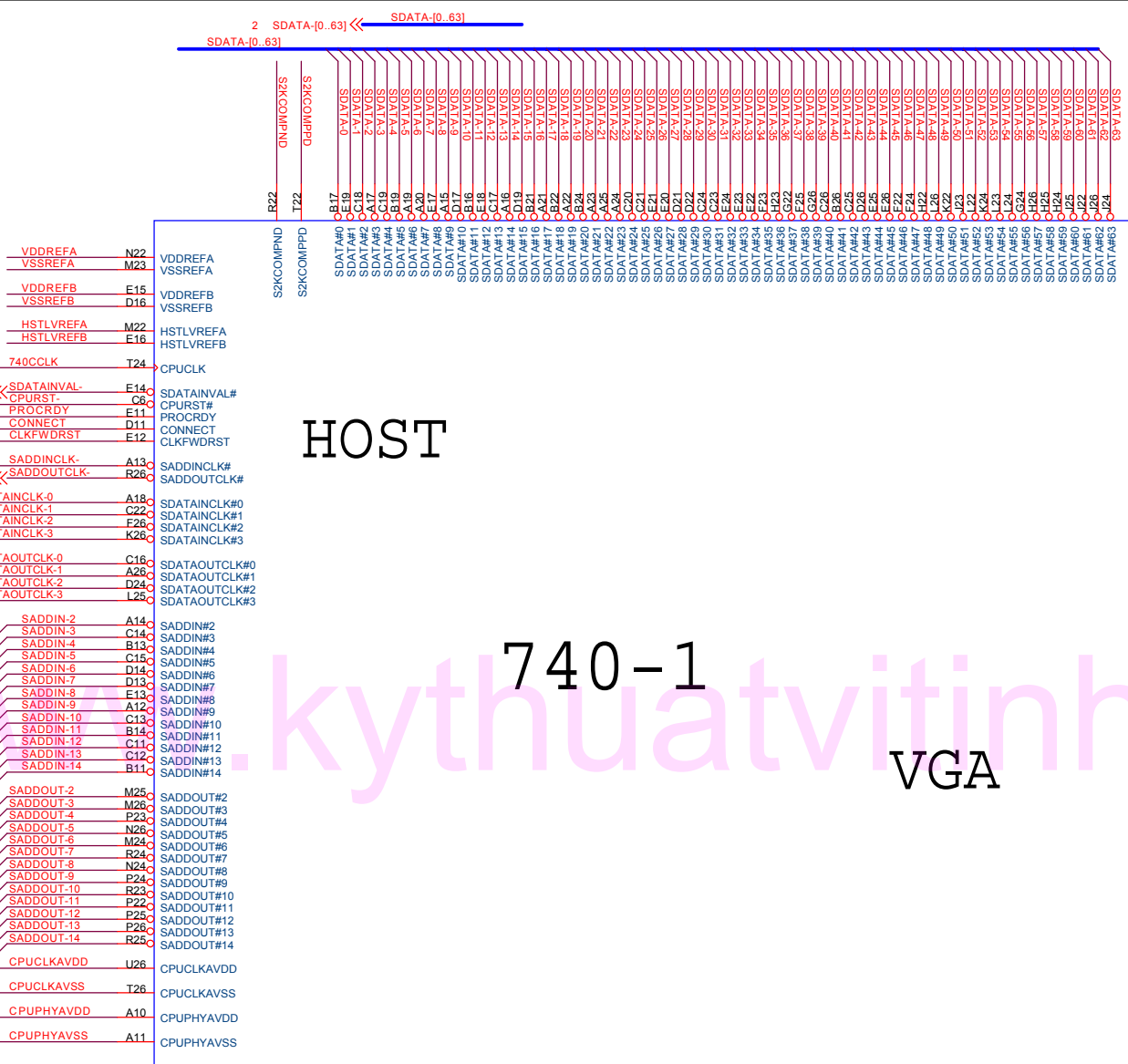
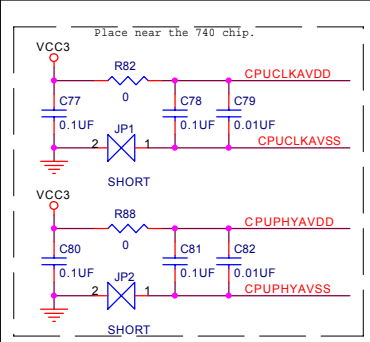


solder side

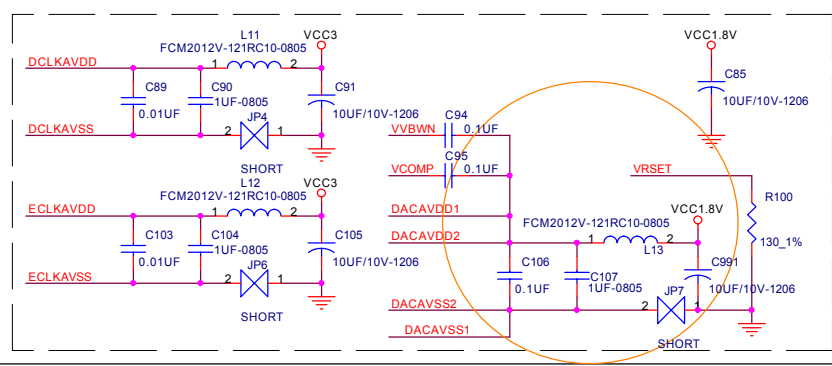
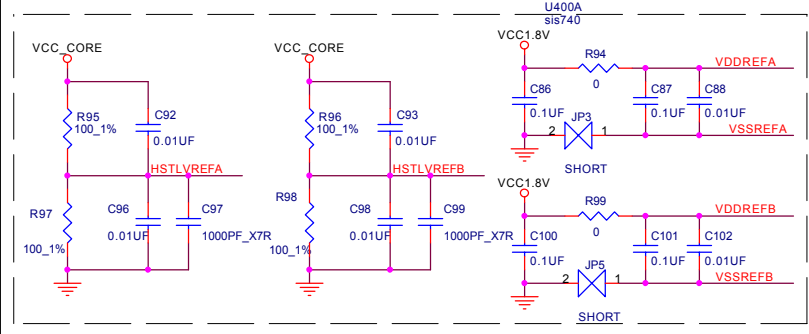
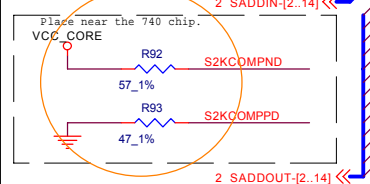
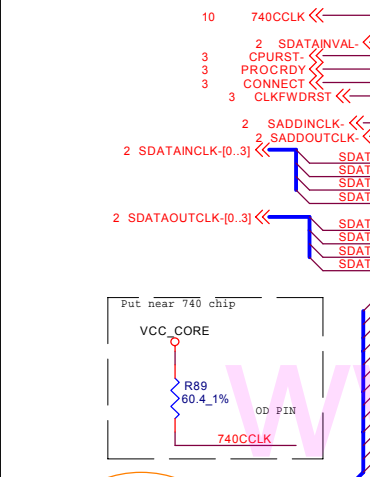
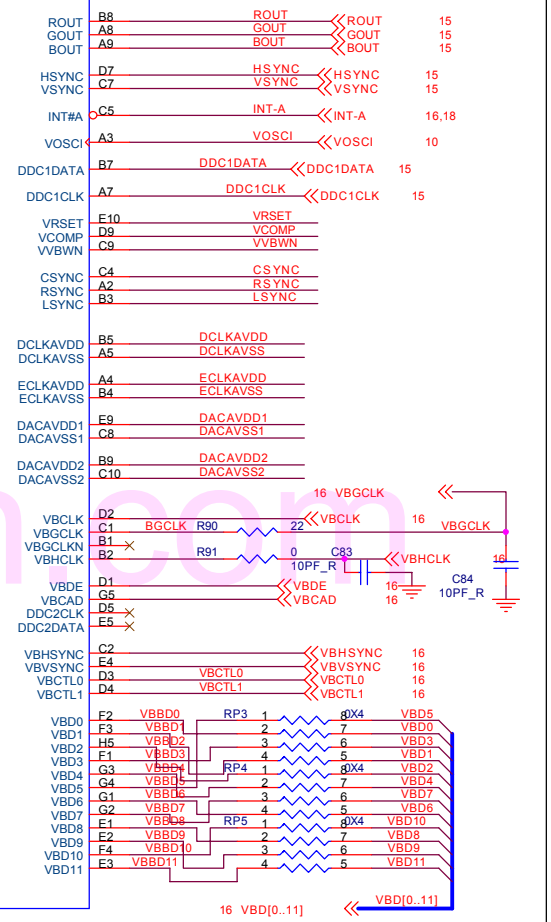
 Elitegroup Computer Systems		
Title SOCKETA-3		
Size B	Document Number A535-1-4-01	Rev 2.3
Date: Tuesday, May 25, 2004	Sheet 4	of 39



		
Elitegroup Computer Systems		
Title: SOCKETA-3		
Size: B	Document Number: A535-1-4-01	Rev: 2.3
Date: Tuesday, May 25, 2004	Sheet: 5	of 39



RSYNC: This interrupt function is for patch some our vga issues
 LSYNC : The panel link please set to 1.
 CSYNC : The Vb voltage select please set to 1.

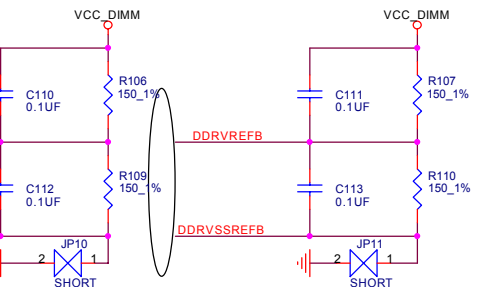
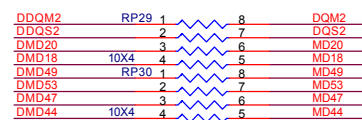
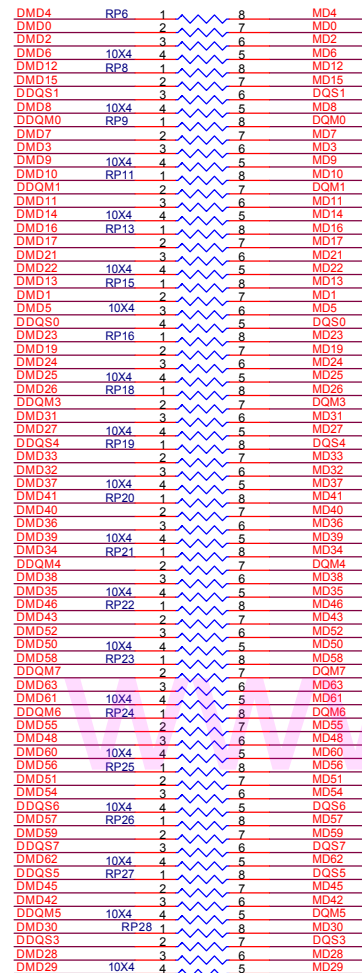


	ON/1	OFF/0	Default	
VBCTL0	Reserved	FAL	NTSC	Off
VBCTL1	Reserved	DISABLE	ENABLE	Off
RSYNC	Vga Interrupt	ENABLE	DISABLE	Off
LSYNC	Panel Link	ENABLE	DISABLE	Off
CSYNC	Vb VCC_SEL	3.3V	1.8V	3.3V

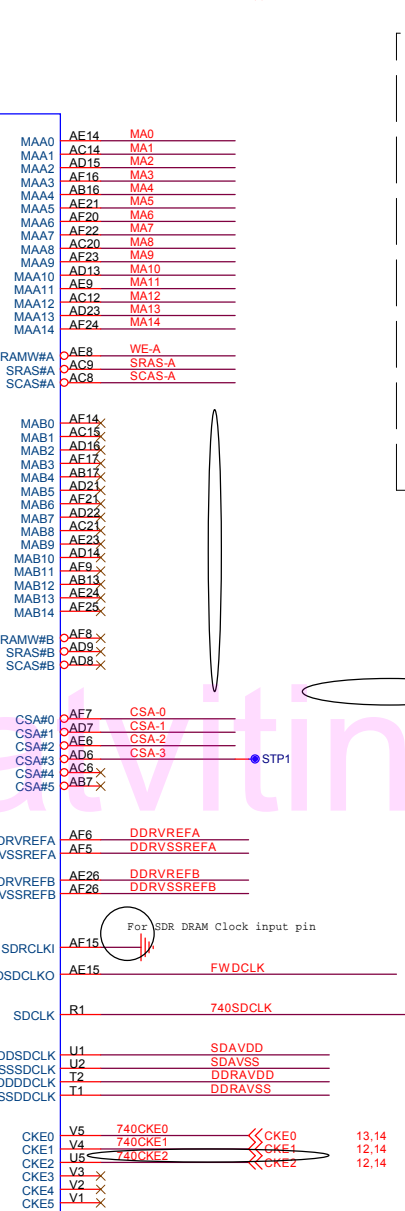
Near to DDR module

Series Resistances can swap by layout result.

DDR MODULE TO DDR SELL ABOUT 2"

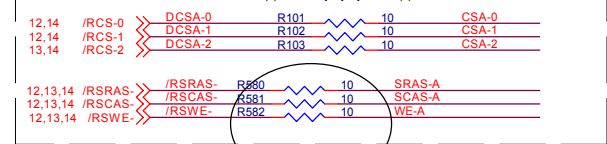
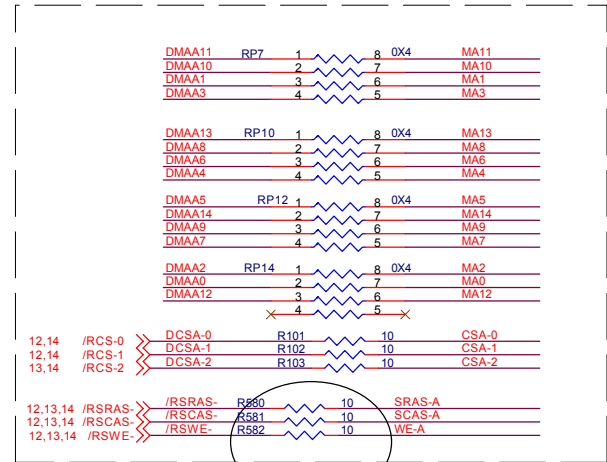


740-2

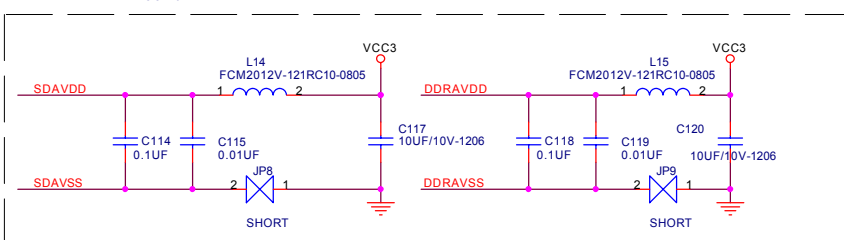
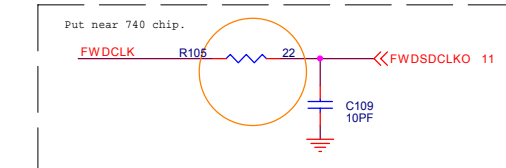
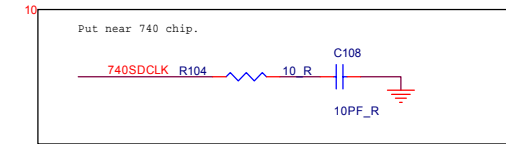


Near to DDR module

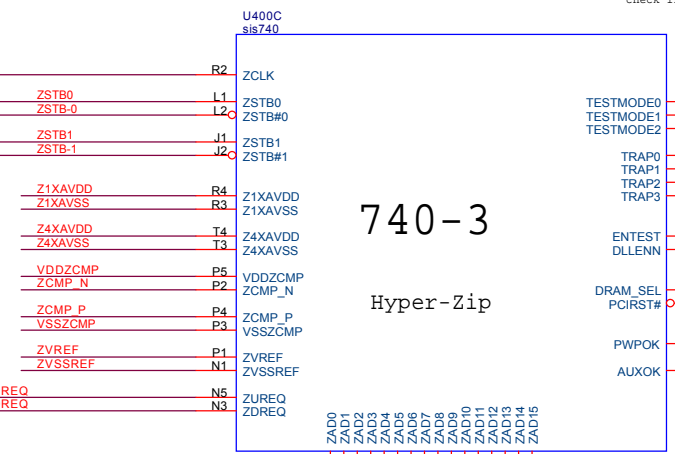
DDR MODULE TO DDR SELL ABOUT 2"



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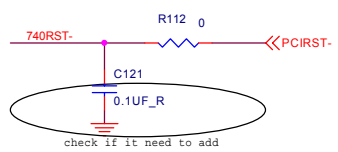
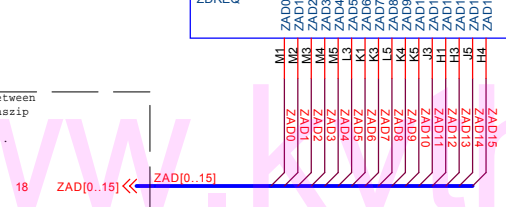


The differences between the traces of teanszip strobes should be smaller than 0.1* .

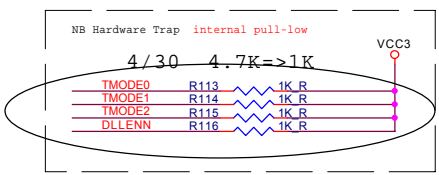


740-3 Hyper-Zip

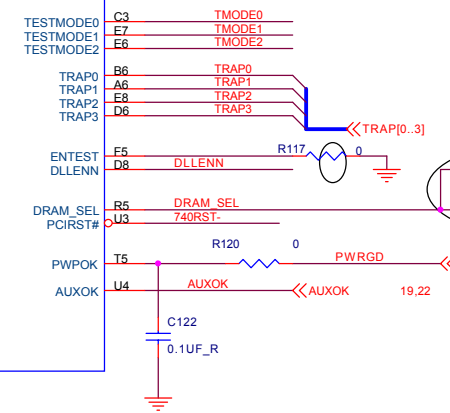
The differences between the traces of teanszip strobes should be smaller than 0.1* .



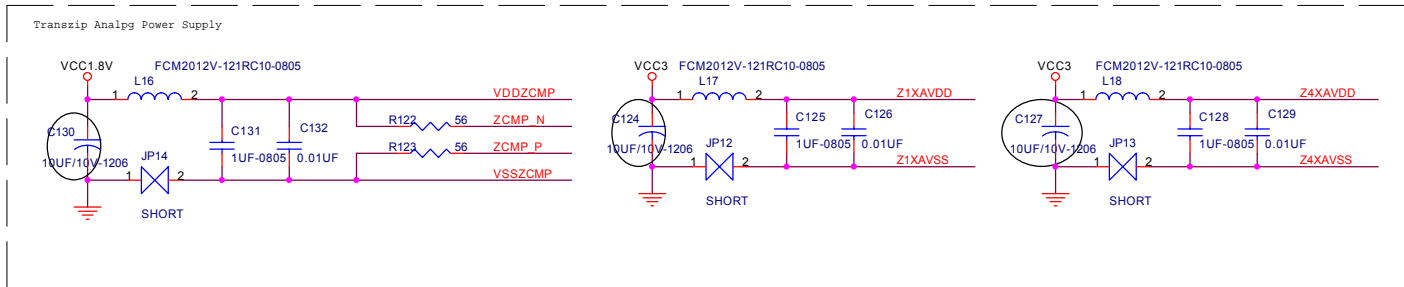
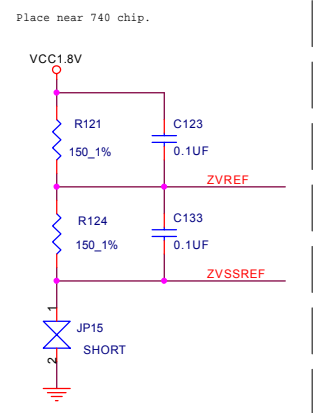
	DES.	ON/1	Off/0	Default
DLENN	CPUCLK SDCLK PLL/DLI CIRCUIT ENABLE	DISABLE	ENABLE	OFF
DRAM_SEL	SDRAM SELECT	DDR	SDR	ON (DDR)
TMODE0	SYSTEM CLOCK SpeED			OFF
TMODE1	SYSTEM CLOCK SpeED			OFF FOR INNER LOGIC
TMODE2	740 Debug Mode SELECTION	ENABLE	DISABLE	OFF



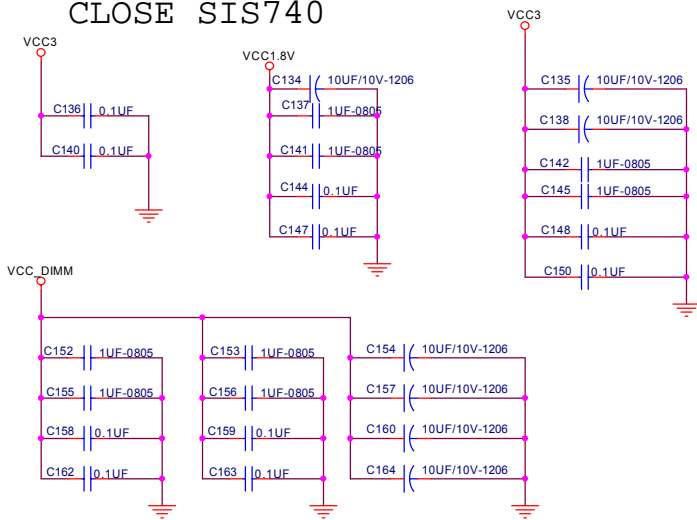
TMODE1	TMODE0	MODE	default
0	0	100MHZ	default
0	1	66MHZ	
1	0	90MHZ	
1	1	133MHZ	



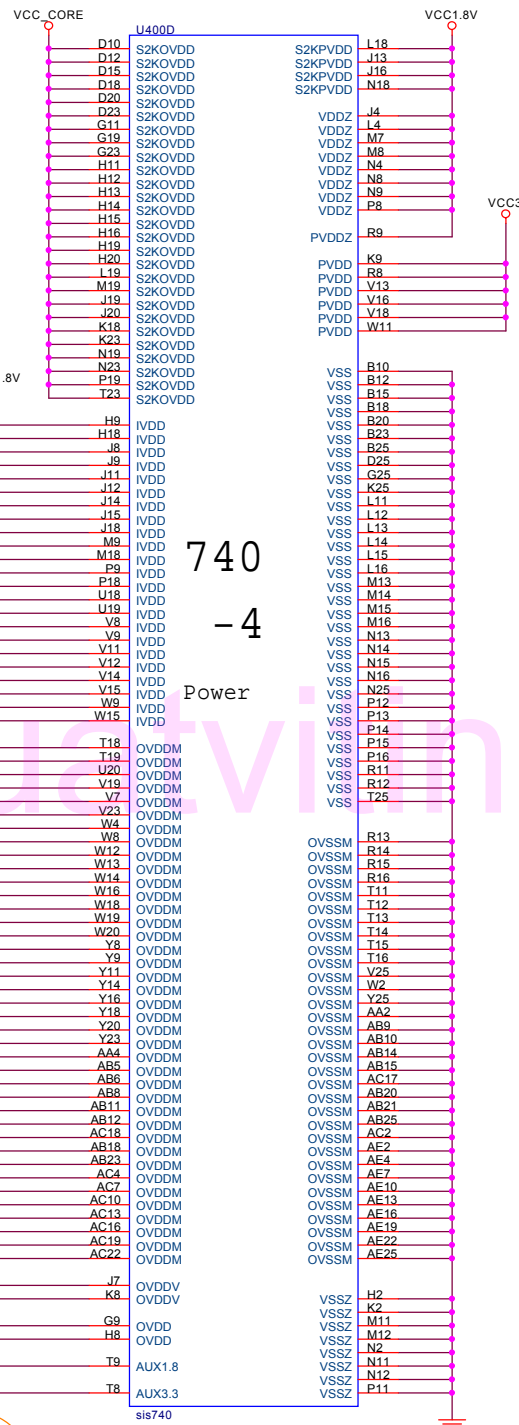
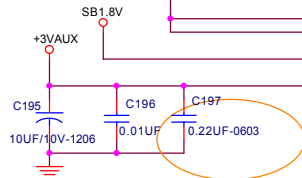
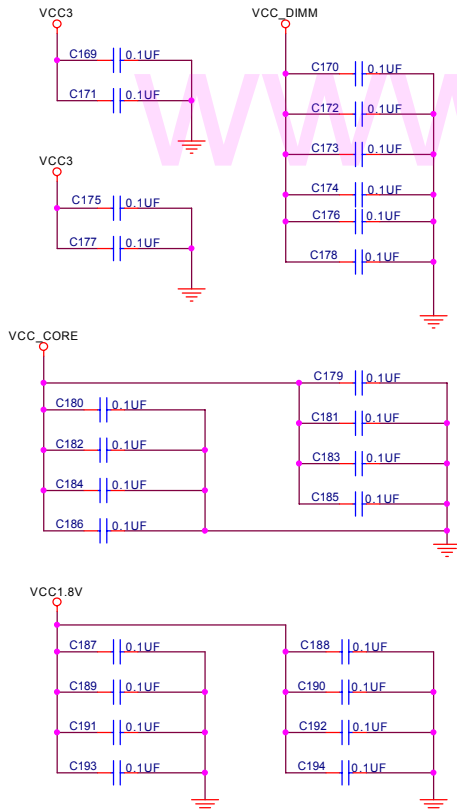
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CLOSE SIS740

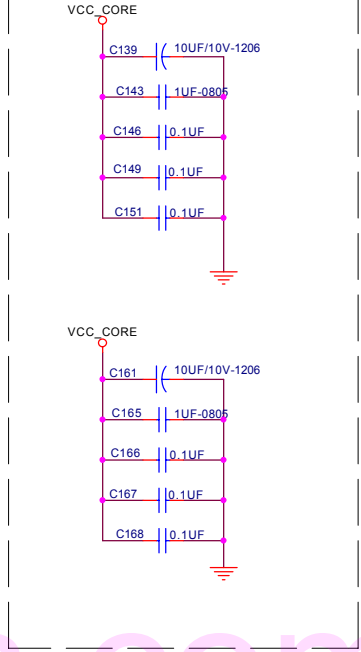


Place these capacitors under 740 solder side.



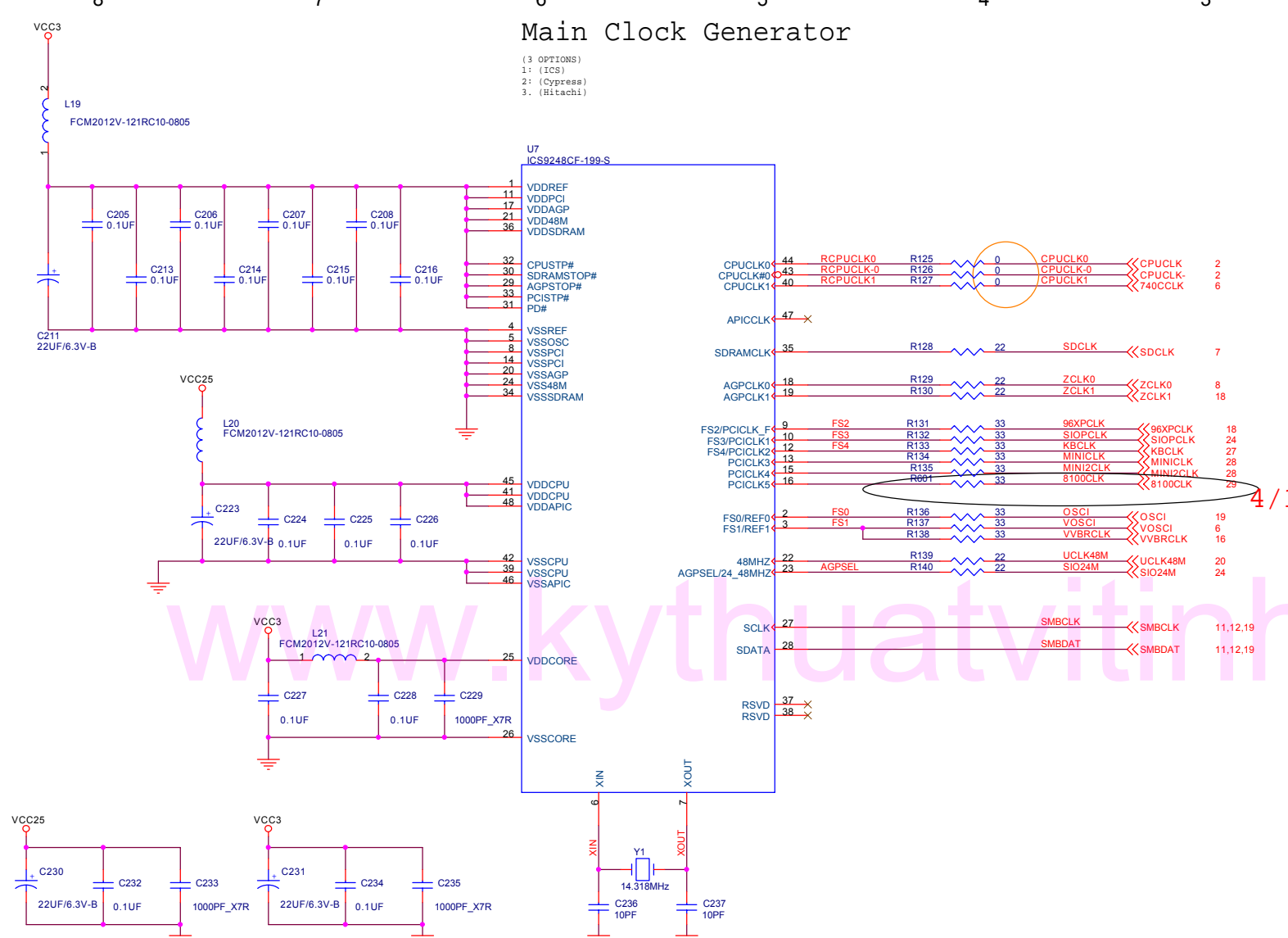
740
-4
Power

CLOSE SIS740



Main Clock Generator

(3 OPTIONS)
 1: (ICS)
 2: (Cypress)
 3: (Hitachi)



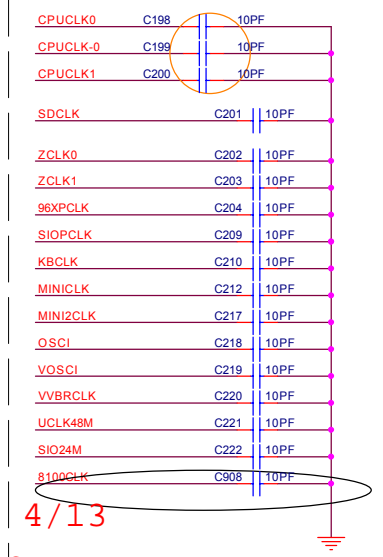
24_48MHz has internal pull-up of 120K to VCC3

FS[0..4], AGPSEL, PCI_STOP#, CPU_STOP#, SDRAM_STOP#, AGP_STOP# have internal pull-down of 120K to GND

SIS740 CLOCK					AGPCLK (MHz)			
(FS3)	(FS2)	(FS1)	(FS0)	CPU (MHz)	SDRAM (MHz)	PCI (MHz)	AGPSEL=0	AGPSEL=1
0	0	0	0	66.6	66.6	33.3	66.6	50
0	0	0	1	100	100	33.3	66.6	50
0	0	1	0	166	166	33.3	66.6	55.6
0	0	1	1	133	133	33.3	66.6	50
0	1	0	0	66.6	100	33.3	66.6	50
0	1	0	1	100	66.6	33.3	66.6	50
0	1	1	0	100	133	33.3	66.6	50
0	1	1	1	133	100	33.3	66.6	50
1	0	0	0	112	112	33.6	67.2	56
1	0	0	1	124	124	31	62	46.5
1	0	1	0	138	138	34.5	69	51.8
1	0	1	1	150	150	30	60	50
1	1	0	0	66.6	133	33.3	66.6	49.84
1	1	0	1	133	166	33.3	66.6	55.3
1	1	1	0	150	100	30	60	50
1	1	1	1	160	120	30	60	48

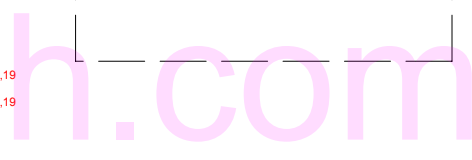
NOTE:
 PCI1CLK=34.5MHz

By-Pass Capacitors
 Place near to the Clock Outputs



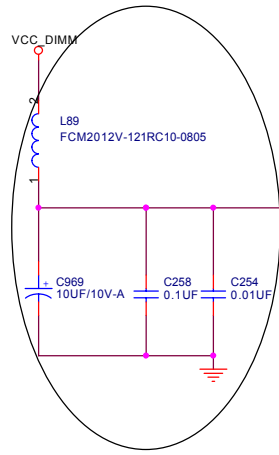
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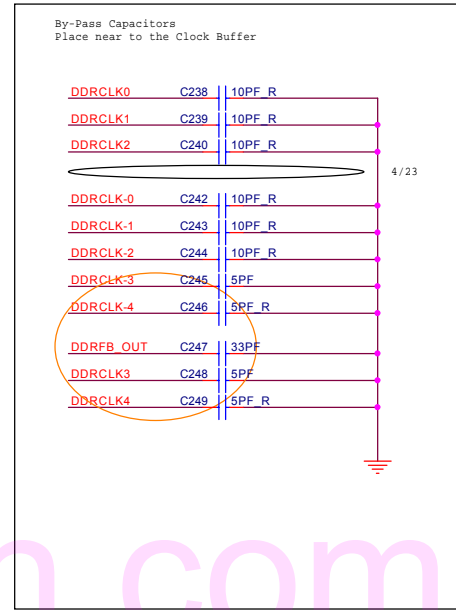
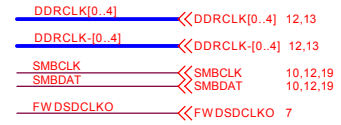
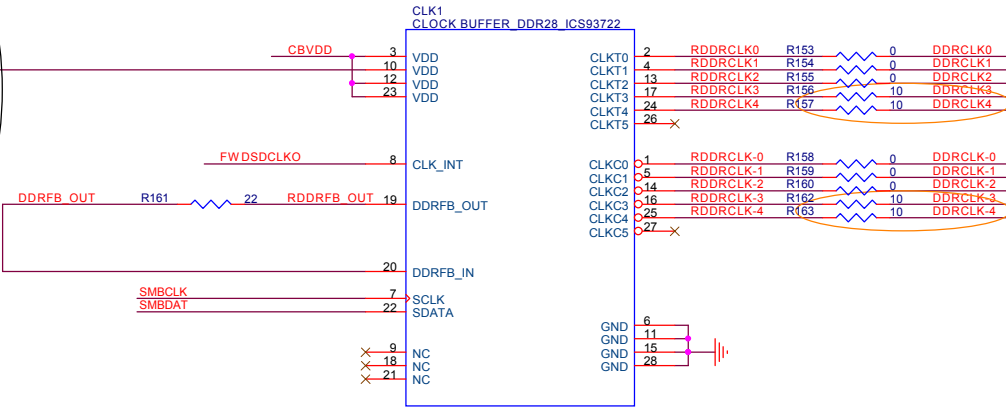


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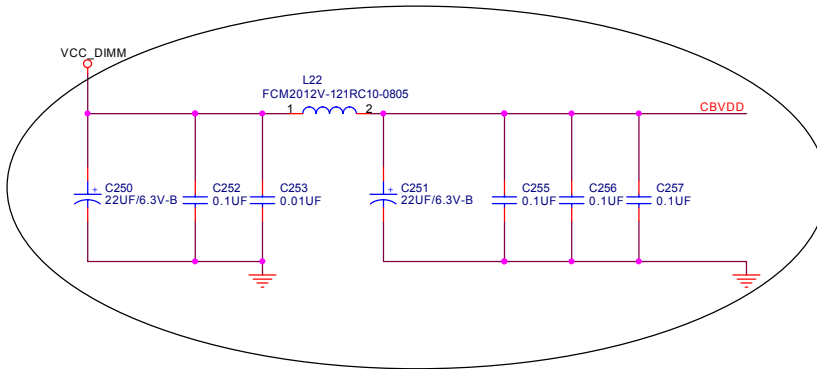
Clock Buffer (DDR)

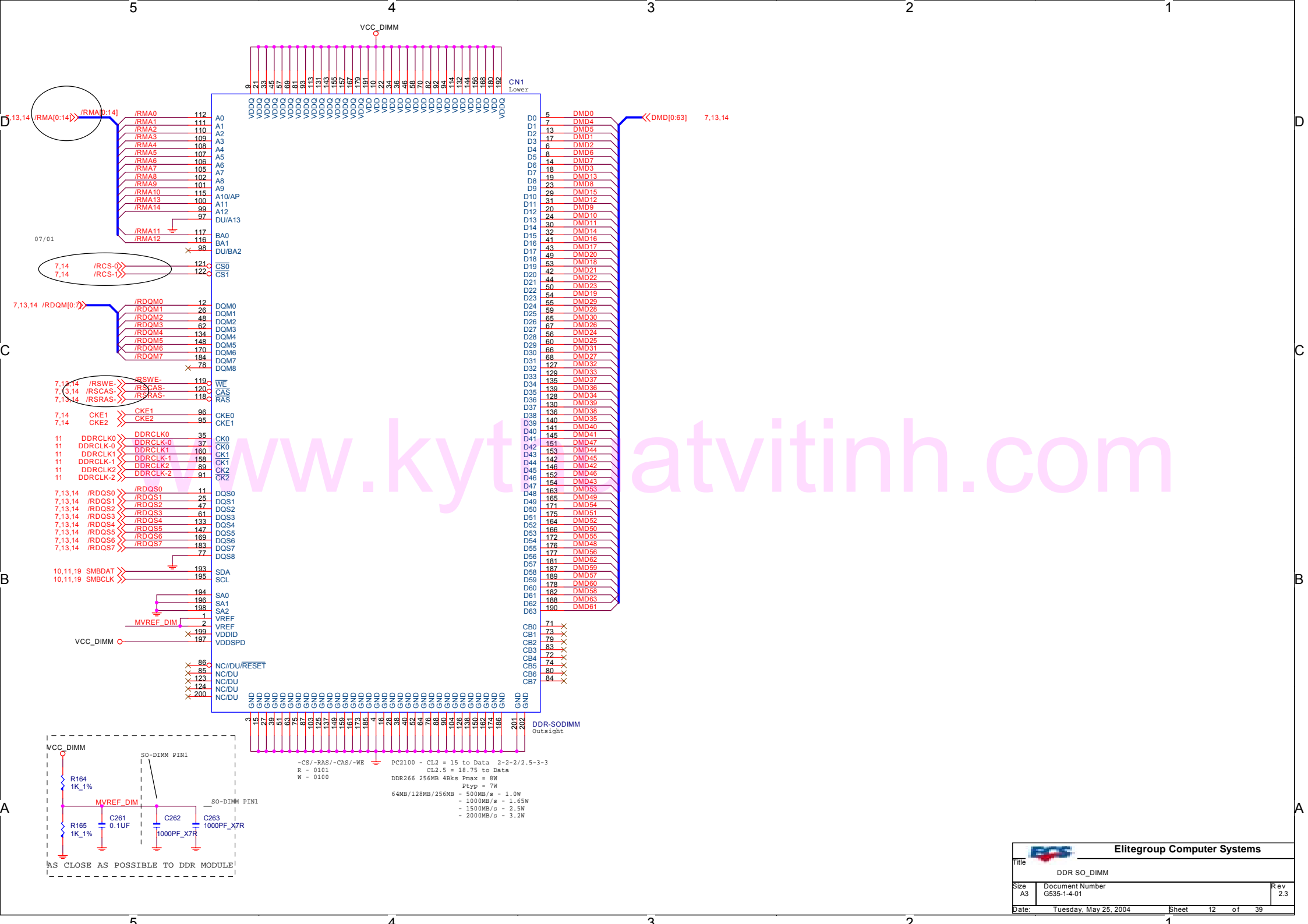


(OPTIONS)
1* (IC9-93705)



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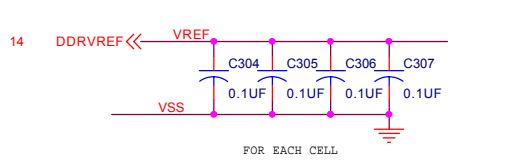
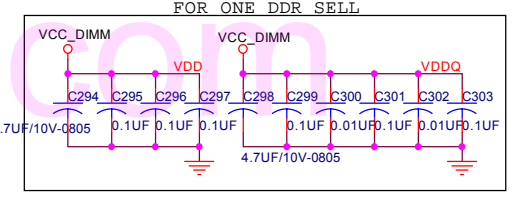
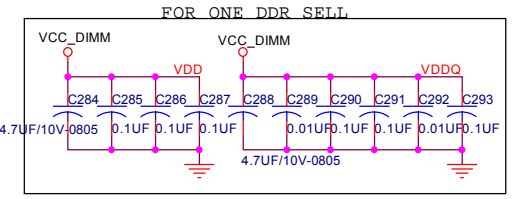
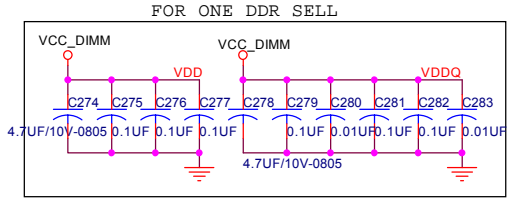
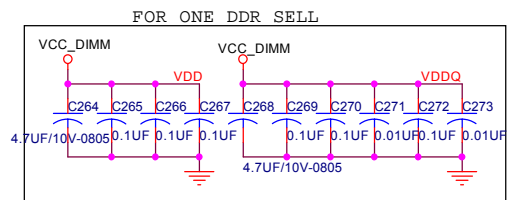
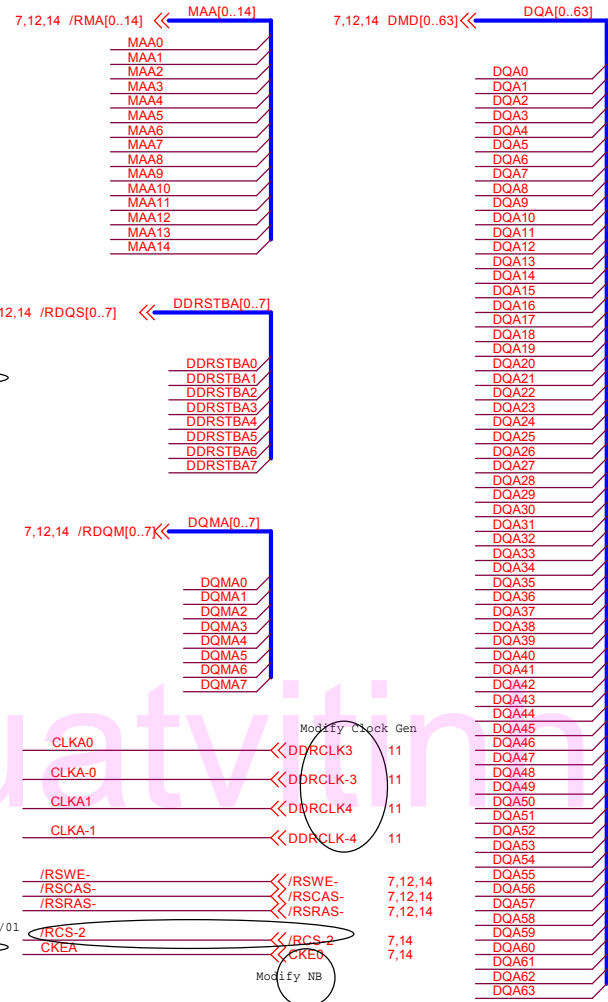


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VDD	1	VDD	VSS
DQA0	2	DQ0	DQ15
VDDQ	3	VDDQ	VSSQ
DQA1	4	DQ1	DQ14
DQA5	5	DQ2	DQ13
VSS	6	DQ2	DQ13
DQA1	7	VSSQ	VDDQ
DQA3	8	DQ3	DQ12
VDDQ	9	DQ4	DQ11
DQA7	10	DQ5	VSSQ
DQA2	11	DQ6	DQ10
VSS	12	DQ6	DQ9
DQA6	13	VSSQ	VDDQ
DQA1	14	DQ7	DQ8
VDDQ	15	NC	NC
DDRSTBA0	16	VDDQ	VSSQ
VDD	17	LDQS	UDQS
VDD	18	NC	NC
VDD	19	VDD	VREF
DQMA0	20	VSS	VSS
/RSWE-	21	UDM	UDM
/RSCAS-	22	WE	CLK
/RSRAS-	23	CAS	CLK
/RCS-2	24	RAS	CKE
VDD	25	CS	NC
MAA11	26	NC	A12
MAA12	27	BA0	A11
MAA10	28	BA1	A9
MAA0	29	A10/AP	A8
MAA1	30	A0	A7
MAA2	31	A1	A6
MAA3	32	A2	A5
VDD	33	VDD	VSS

U10			
VDD	1	VDD	VSS
DQA32	2	DQ0	DQ15
VDDQ	3	VDDQ	VSSQ
DQA33	4	DQ1	DQ14
DQA37	5	DQ2	DQ13
VSS	6	DQ2	DQ13
DQA36	7	VSSQ	VDDQ
DQA35	8	DQ3	DQ12
VDDQ	9	DQ4	DQ11
DQA39	10	DQ5	VSSQ
DQA34	11	DQ6	DQ10
VSS	12	DQ6	DQ9
DQA38	13	VSSQ	VDDQ
DQA1	14	DQ7	DQ8
VDDQ	15	NC	NC
DDRSTBA4	16	VDDQ	VSSQ
VDD	17	LDQS	UDQS
VDD	18	NC	NC
VDD	19	VDD	VREF
DQMA4	20	VSS	VSS
/RSWE-	21	UDM	UDM
/RSCAS-	22	WE	CLK
/RSRAS-	23	CAS	CLK
/RCS-2	24	RAS	CKE
VDD	25	CS	NC
MAA11	26	NC	A12
MAA12	27	BA0	A11
MAA10	28	BA1	A9
MAA0	29	A10/AP	A8
MAA1	30	A0	A7
MAA2	31	A1	A6
MAA3	32	A2	A5
VDD	33	VDD	VSS

U9			
VDD	1	VDD	VSS
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VDDQ	3	VDDQ	VSSQ
DQA17	4	DQ1	DQ14
DQA20	5	DQ2	DQ13
VSS	6	DQ2	DQ13
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DQA19	8	DQ3	DQ12
VDDQ	9	DQ4	DQ11
DQA23	10	DQ5	VSSQ
DQA22	11	DQ6	DQ10
VSS	12	DQ6	DQ9
DQA21	13	VSSQ	VDDQ
DQA1	14	DQ7	DQ8
VDDQ	15	NC	NC
DDRSTBA2	16	VDDQ	VSSQ
VDD	17	LDQS	UDQS
VDD	18	NC	NC
VDD	19	VDD	VREF
DQMA2	20	VSS	VSS
/RSWE-	21	LDM	UDM
/RSCAS-	22	WE	CLK
/RSRAS-	23	RAS	CLK
/RCS-2	24	RAS	CKE
VDD	25	CS	NC
MAA11	26	NC	A12
MAA12	27	BA0	A11
MAA10	28	BA1	A9
MAA0	29	A10/AP	A8
MAA1	30	A0	A7
MAA2	31	A1	A6
MAA3	32	A2	A5
VDD	33	VDD	VSS

U11			
VDD	1	VDD	VSS
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VDDQ	3	VDDQ	VSSQ
DQA54	4	DQ1	DQ14
VSS	5	DQ2	DQ13
DQA51	6	VSSQ	VDDQ
DQA48	7	DQ3	DQ12
VDDQ	8	DQ4	DQ11
DQA55	10	DQ5	VSSQ
DQA50	11	DQ6	DQ10
VSS	12	DQ6	DQ9
DQA52	13	VSSQ	VDDQ
DQA1	14	DQ7	DQ8
VDDQ	15	NC	NC
DDRSTBA6	16	VDDQ	VSSQ
VDD	17	LDQS	UDQS
VDD	18	NC	NC
VDD	19	VDD	VREF
DQMA6	20	VSS	VSS
/RSWE-	21	LDM	UDM
/RSCAS-	22	WE	CLK
/RSRAS-	23	RAS	CLK
/RCS-2	24	RAS	CKE
VDD	25	CS	NC
MAA11	26	NC	A12
MAA12	27	BA0	A11
MAA10	28	BA1	A9
MAA0	29	A10/AP	A8
MAA1	30	A0	A7
MAA2	31	A1	A6
MAA3	32	A2	A5
VDD	33	VDD	VSS

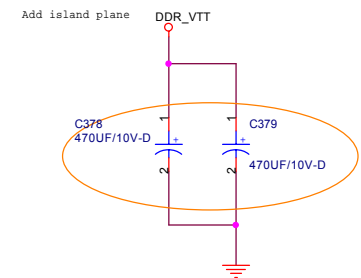
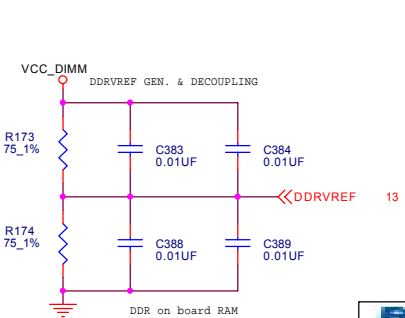
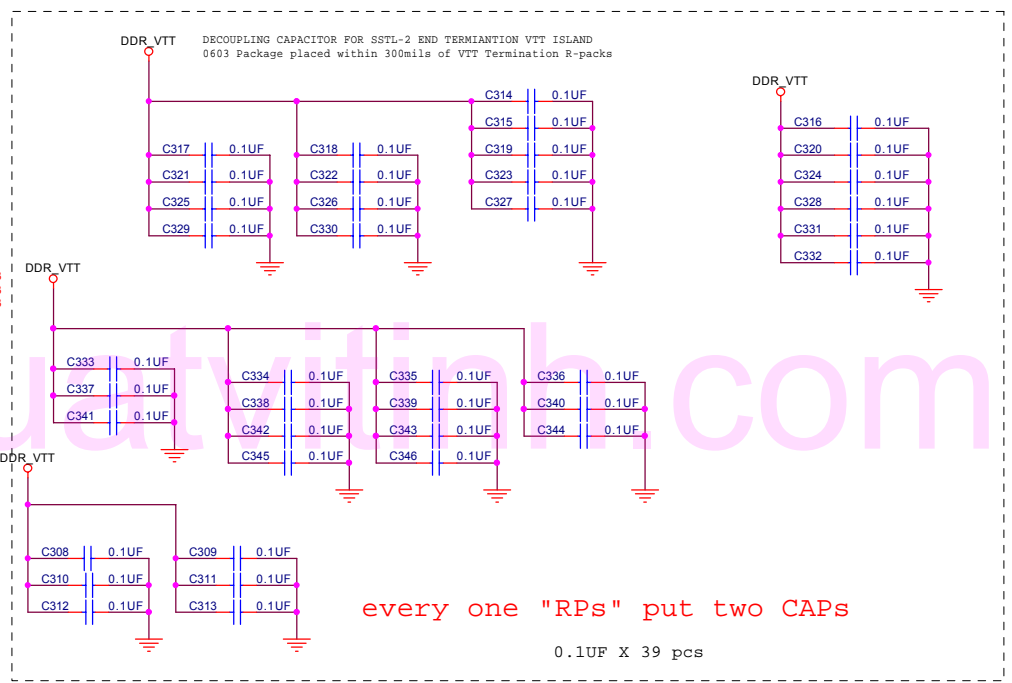
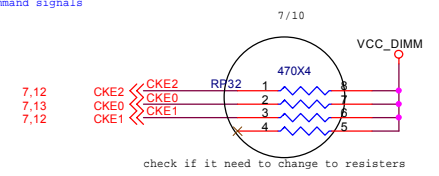
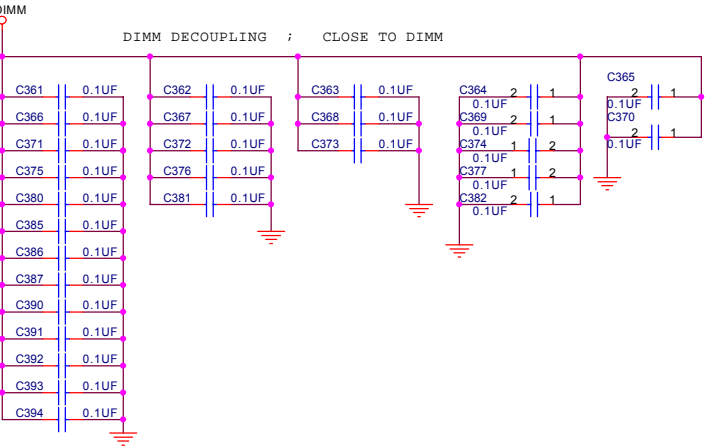
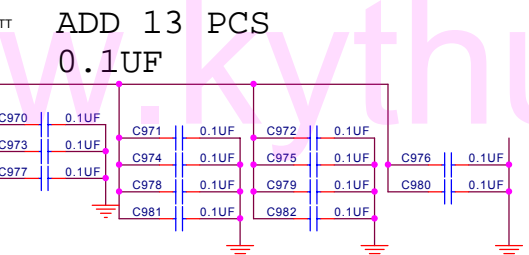
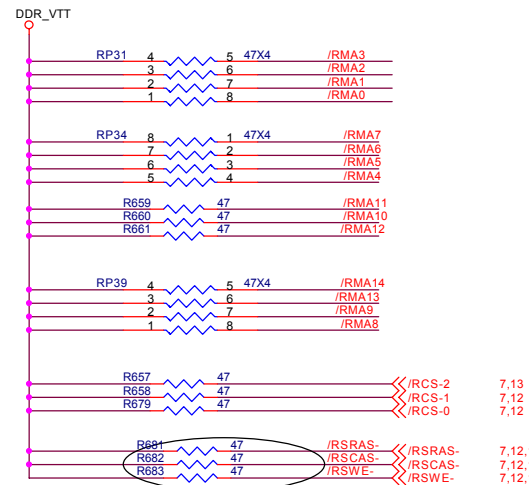
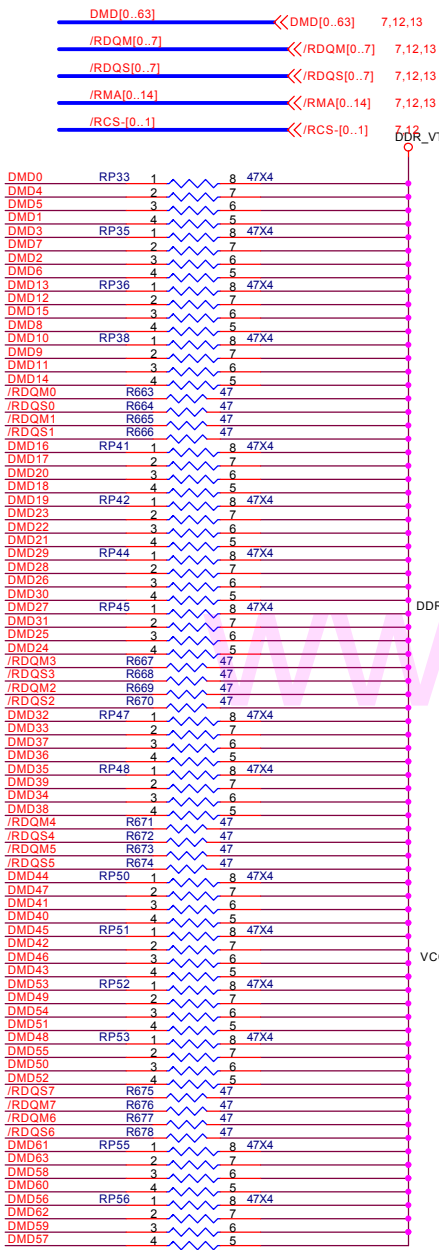


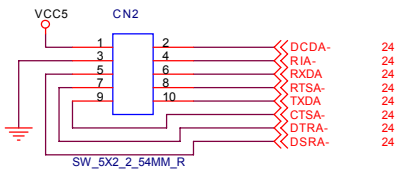
SO-DIMM no "WP" pin

SSTL-2 Termination Resistors

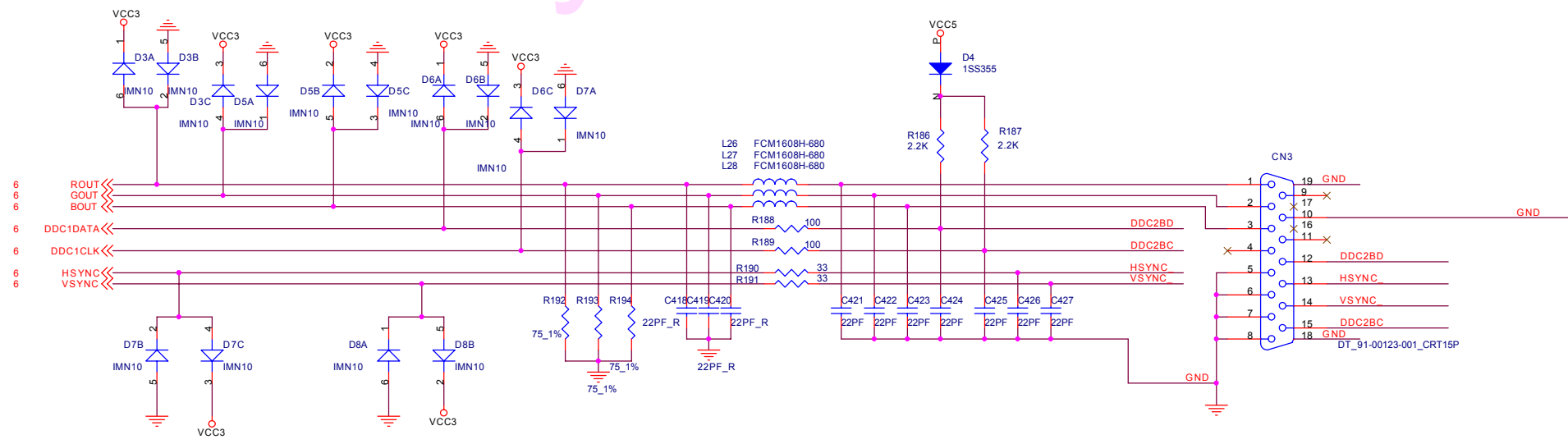
	SDR		DDR		DDR
MD/DQM (/DQS)	LV-CMOS	R#	SSTL-2	R#	1.0
MA/Control	LV-CMOS	0/10/-	SSTL-2	0	47
CS	LV-CMOS	0	SSTL-2	0	47
CKE	DD 3.3V	0	SSTL-2	0	47

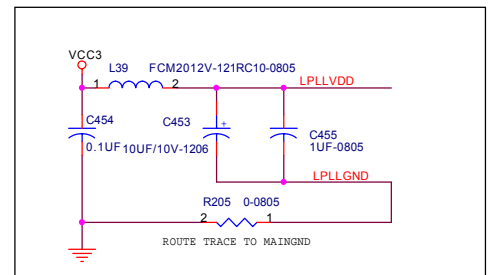
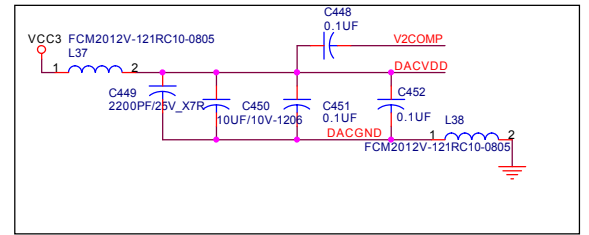
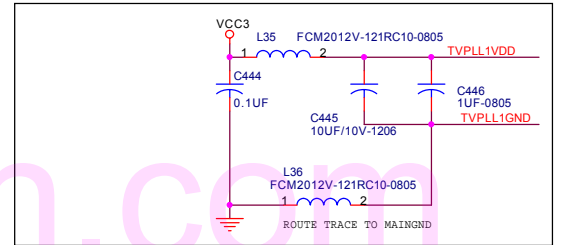
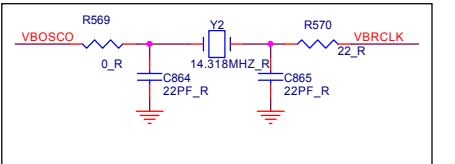
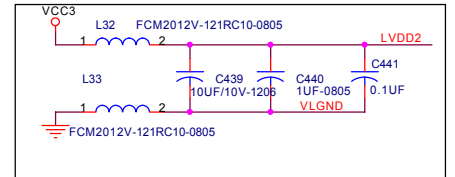
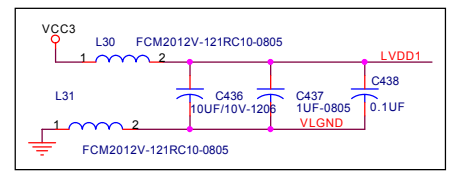
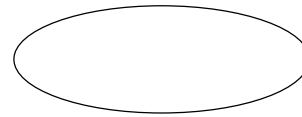
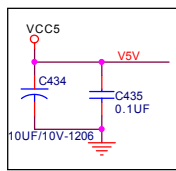
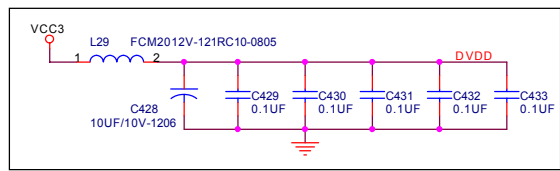
Control signals can NOT be placed within the same RPs as data , strobe , or command signals





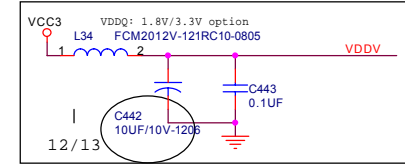
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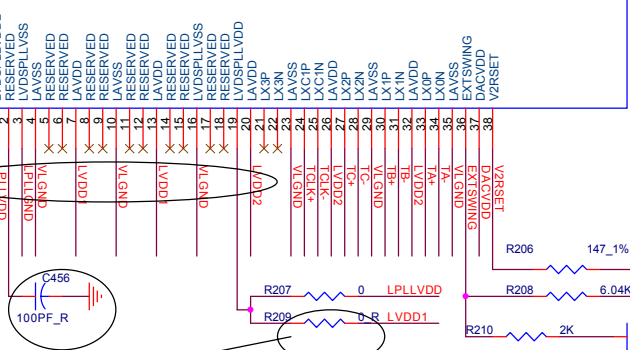
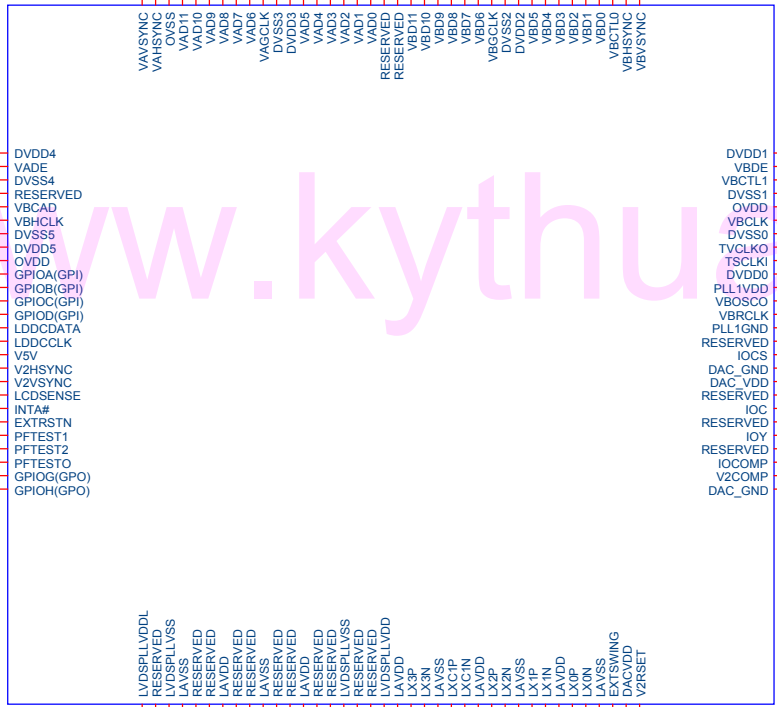
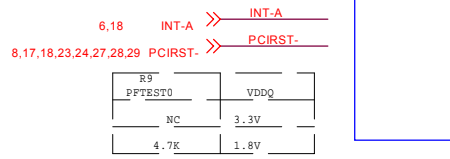
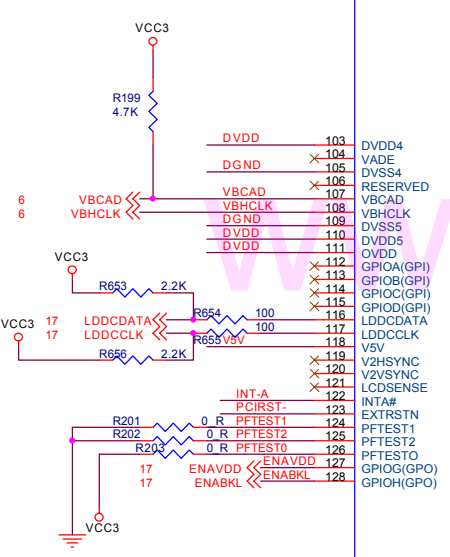
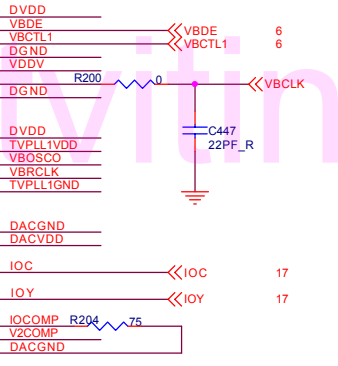
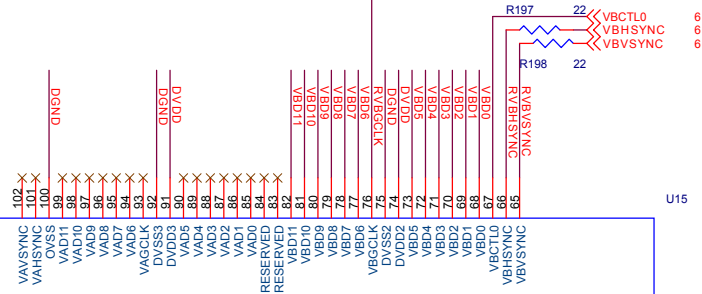


6 VBD[0..11] << VBD[0..11]

10 VBVRCLK << R196 VBVRCLK

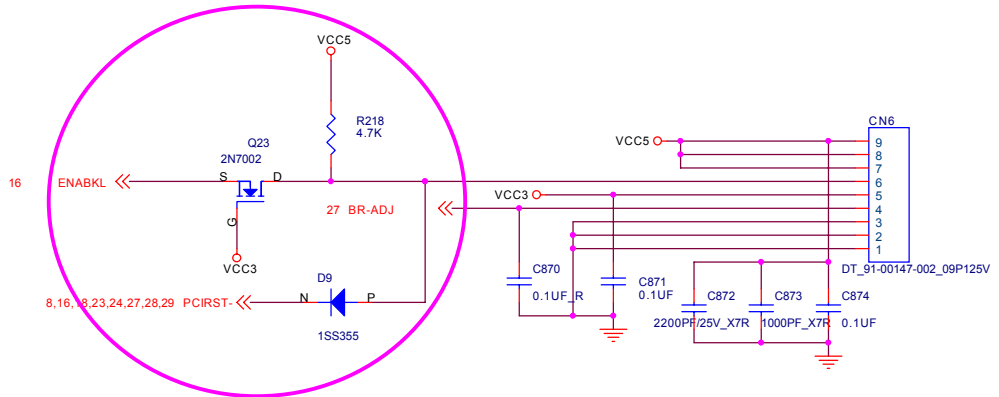
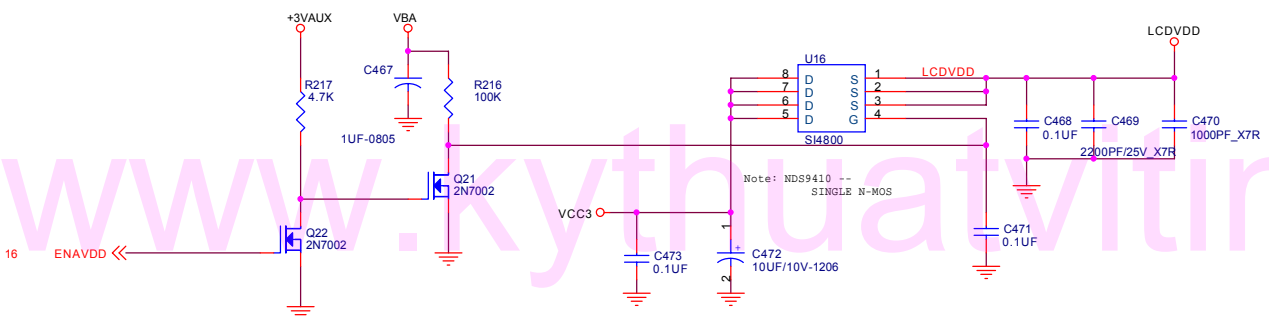
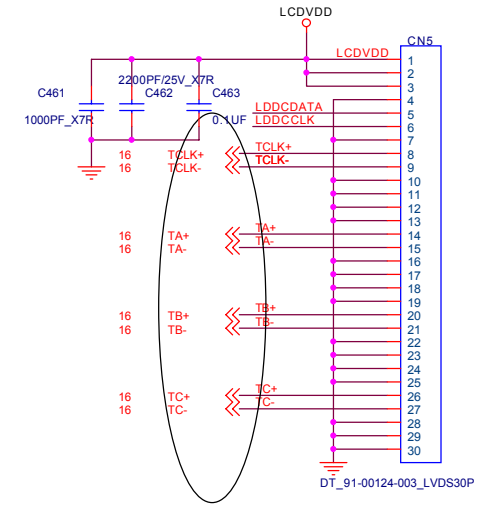
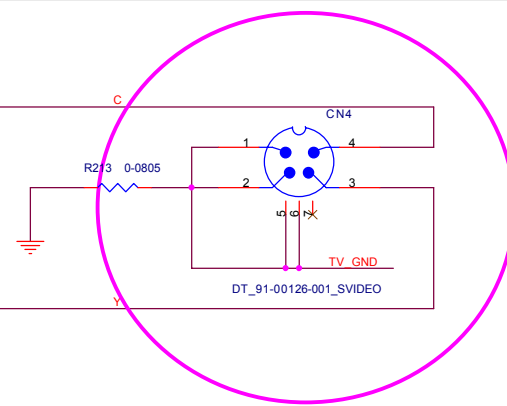
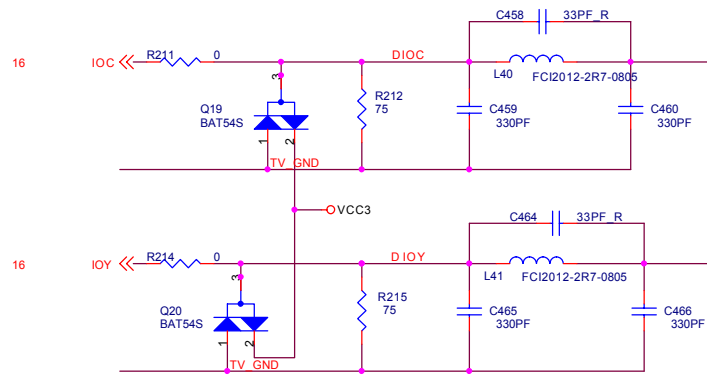


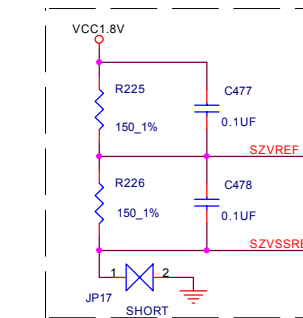
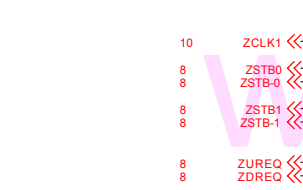
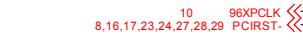
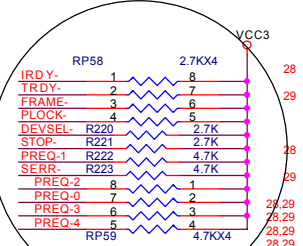
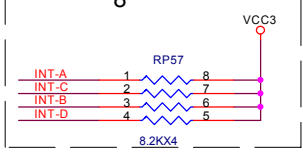
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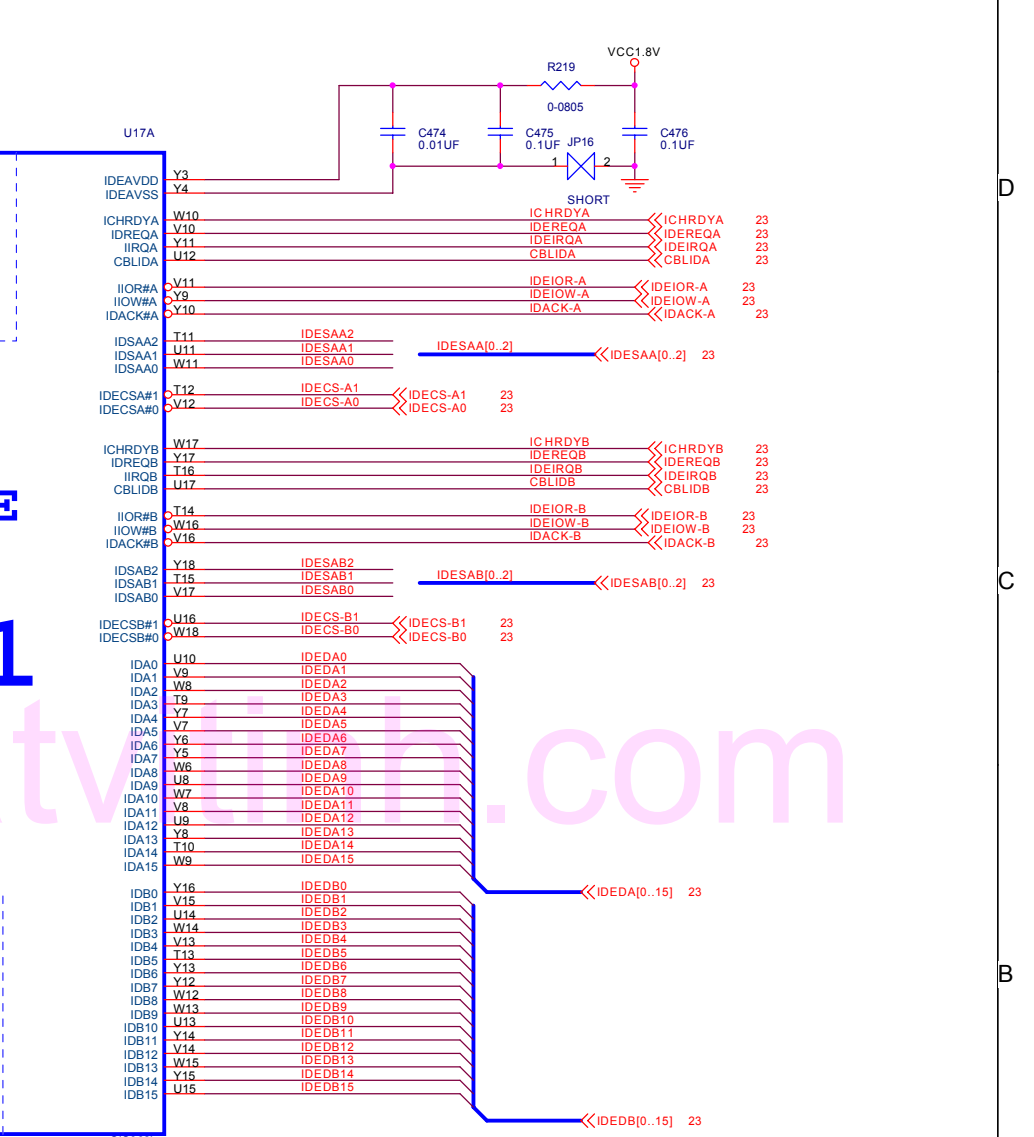
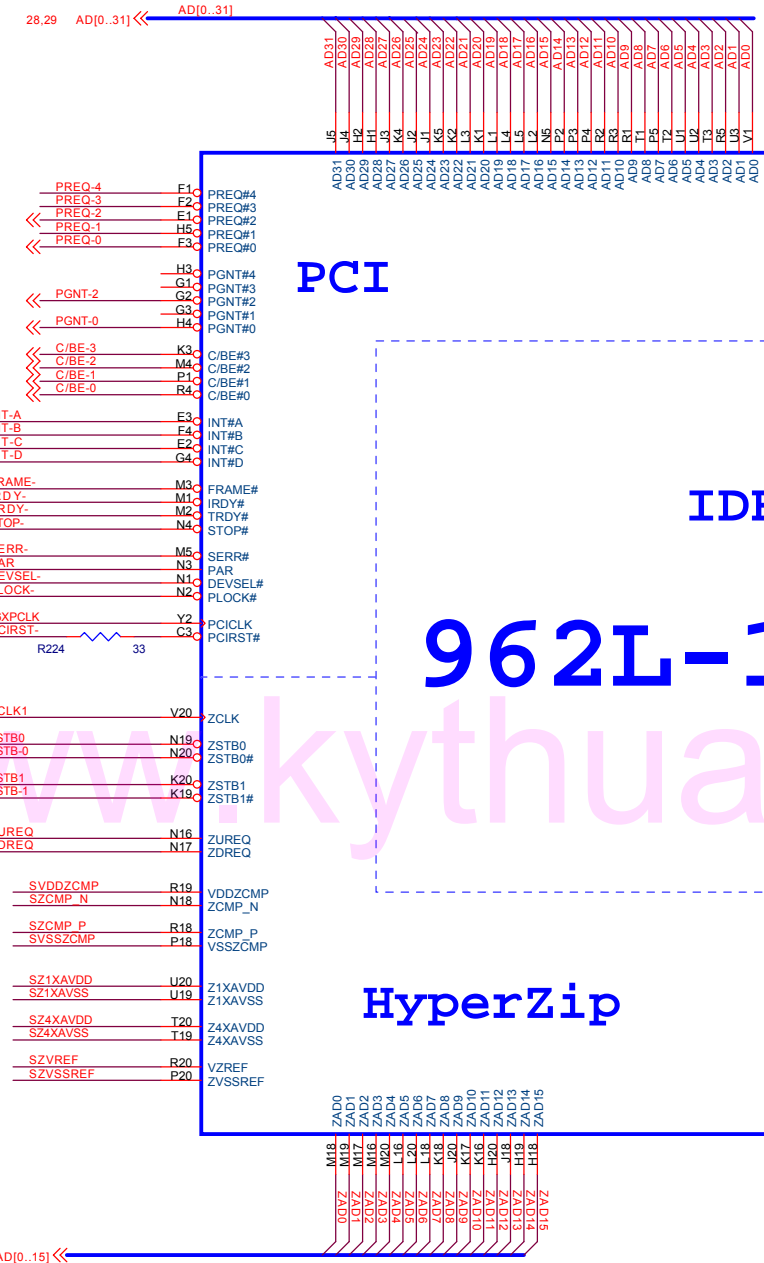
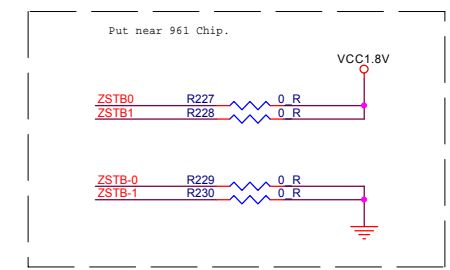
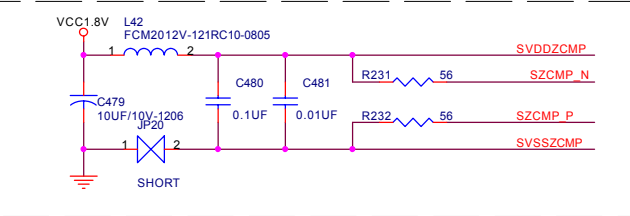
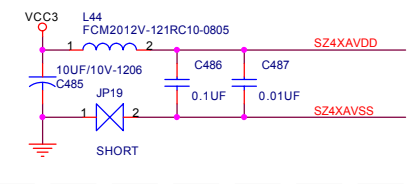
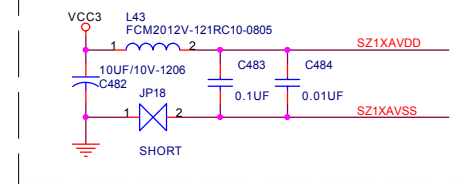
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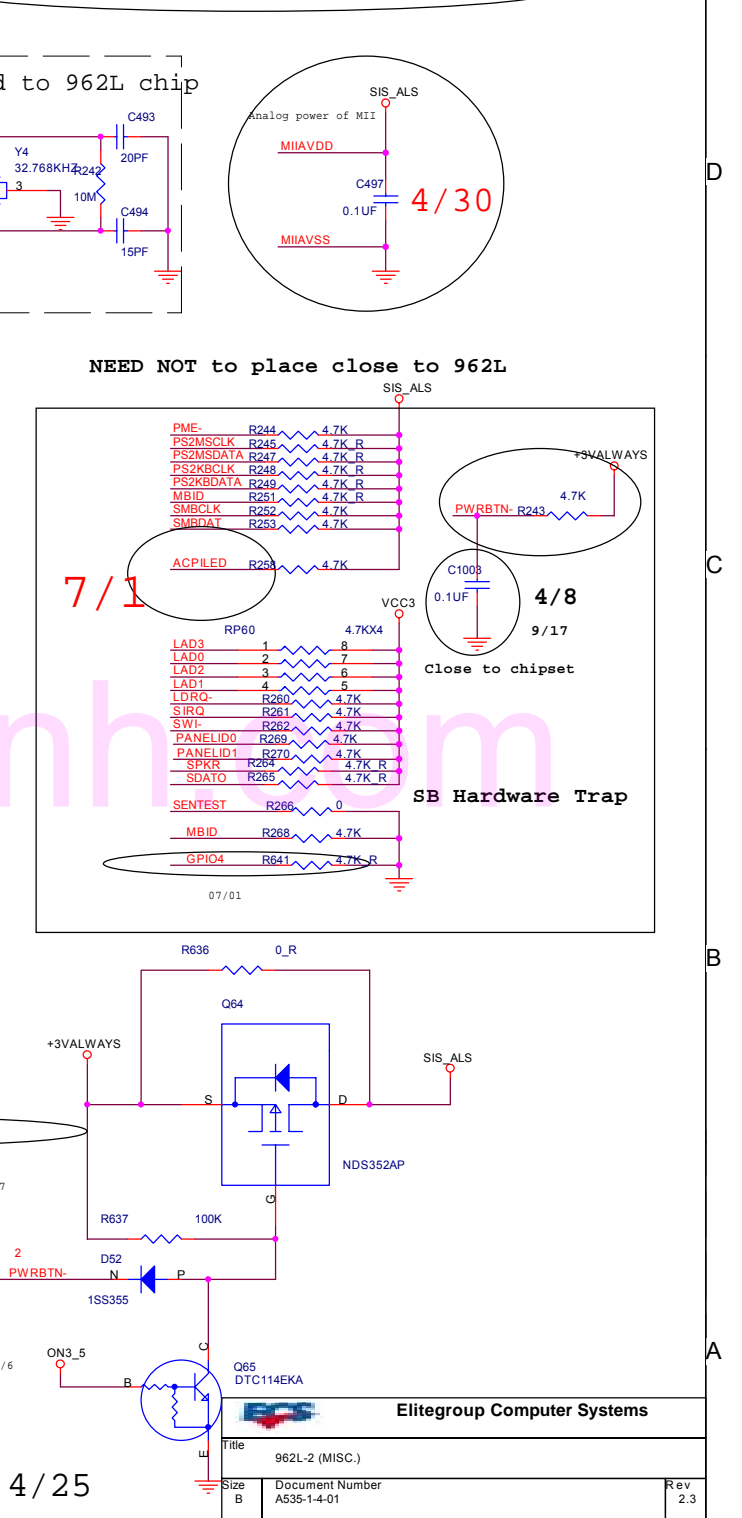
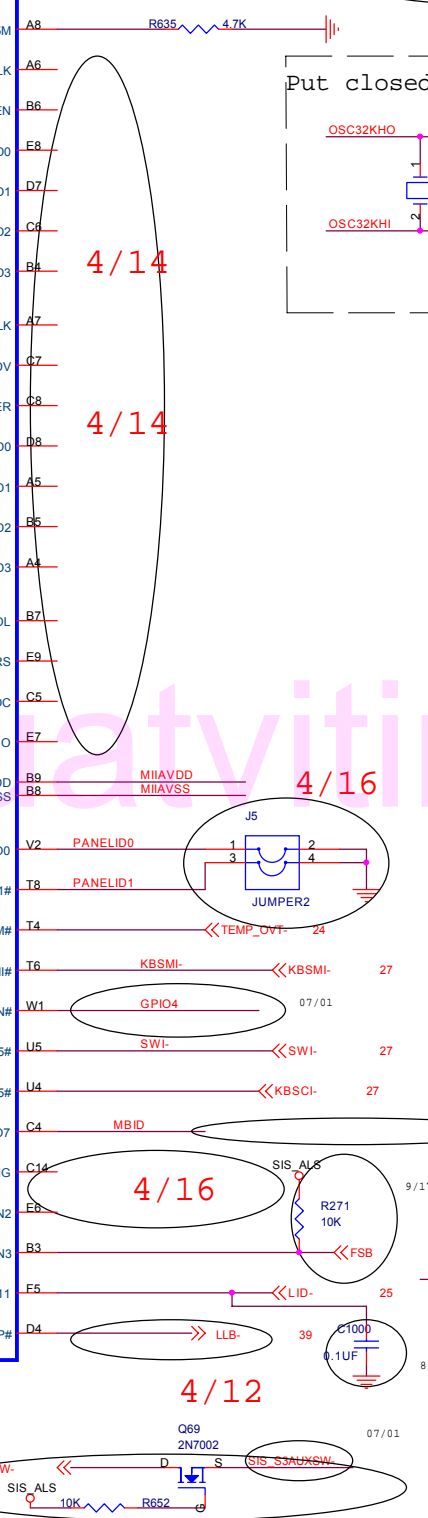
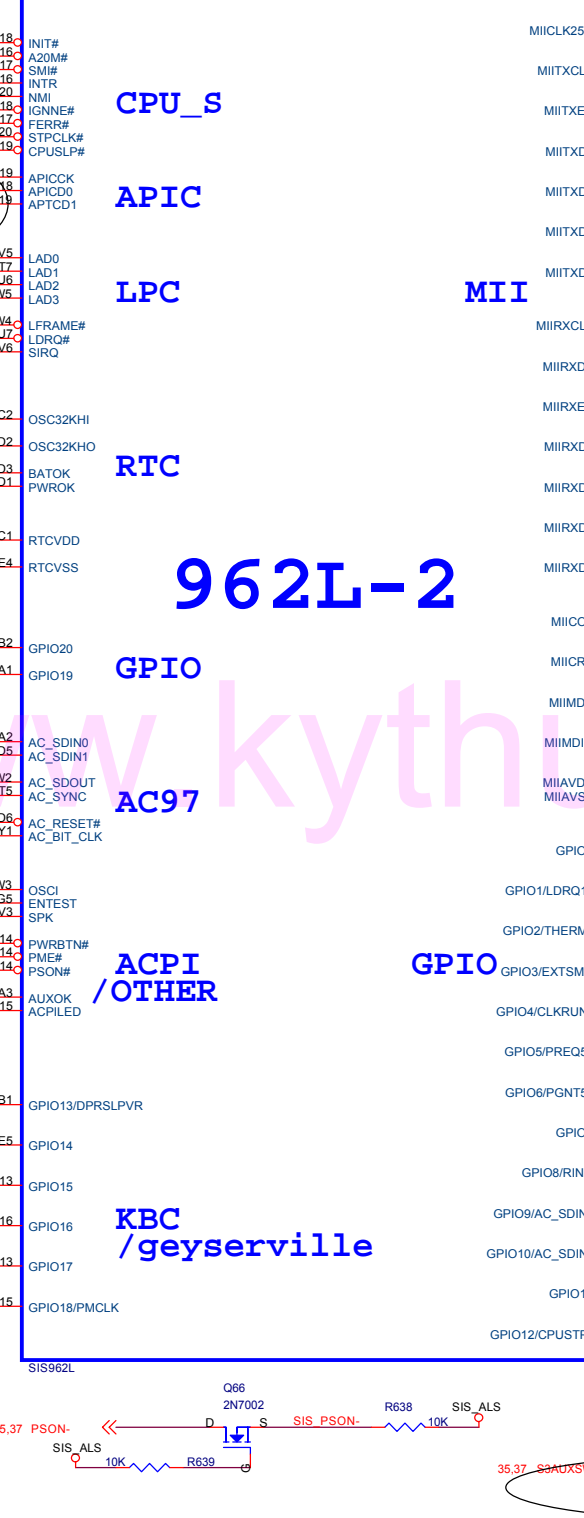
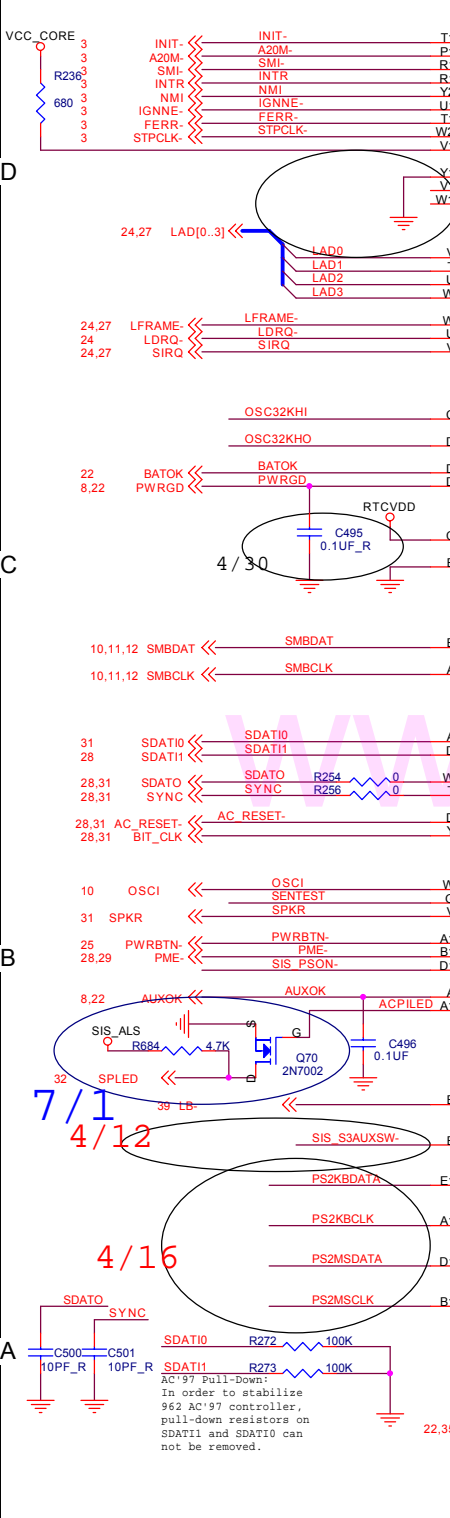
FOR 302LV





Analog Power supplies of Transzip function for 961 Chip.





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962L-2

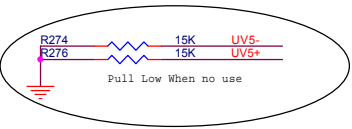
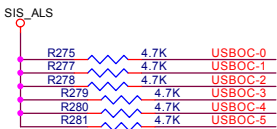
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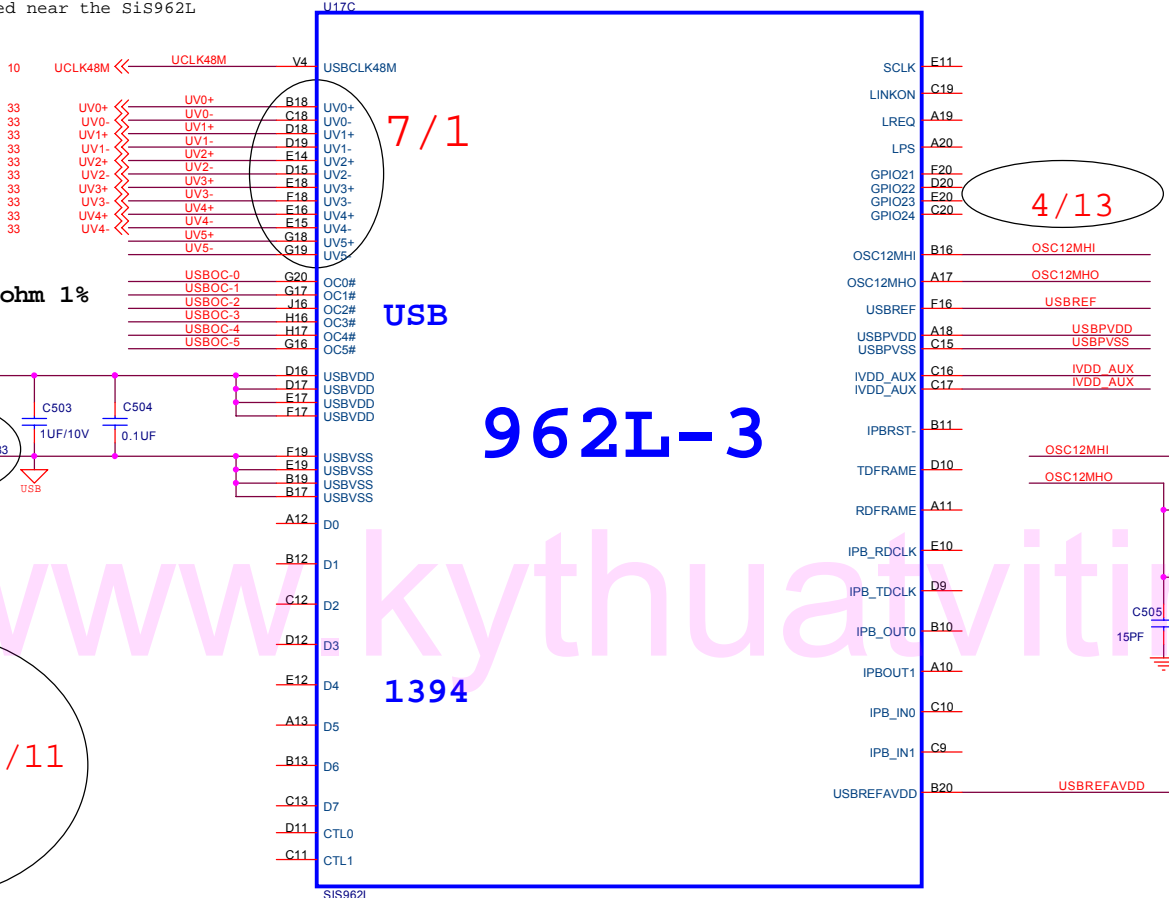
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Size	Document Number	Rev
B	A535-1-4-01	2.3
Date:	Tuesday, May 25, 2004	Sheet 19 of 39



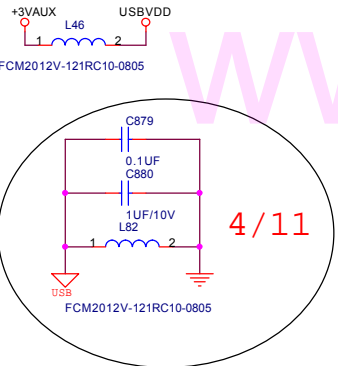
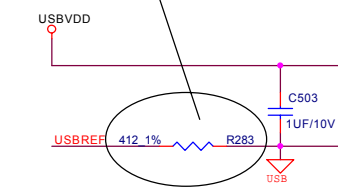
4/1

They don't need to be placed near the SiS962L



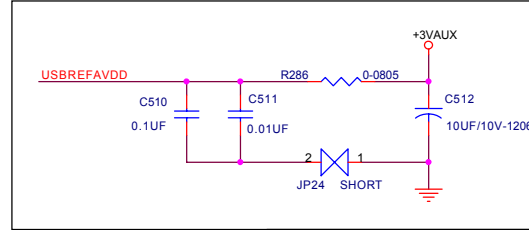
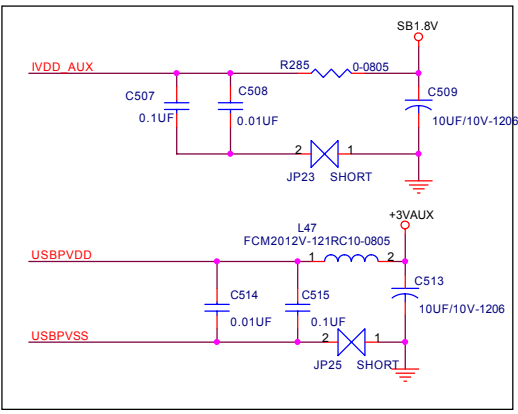
BOM CHANGE

412 ohm or 422 ohm 1%



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	0	1	Default
SPKR (LPC addr mapping)	disable	enable	0
SDATO (TRAP MODE)		ROM	PCI_AD
OC4- (SB debug mode)	enable	disable	1
OC5- (DLENN)	DISABLE	ENABLE	1
SYNC (PCI CLK PLL)	enable	disable	0
IPB_OUT0 (MULTIOL CLOCK PLL)	enable	disable	0

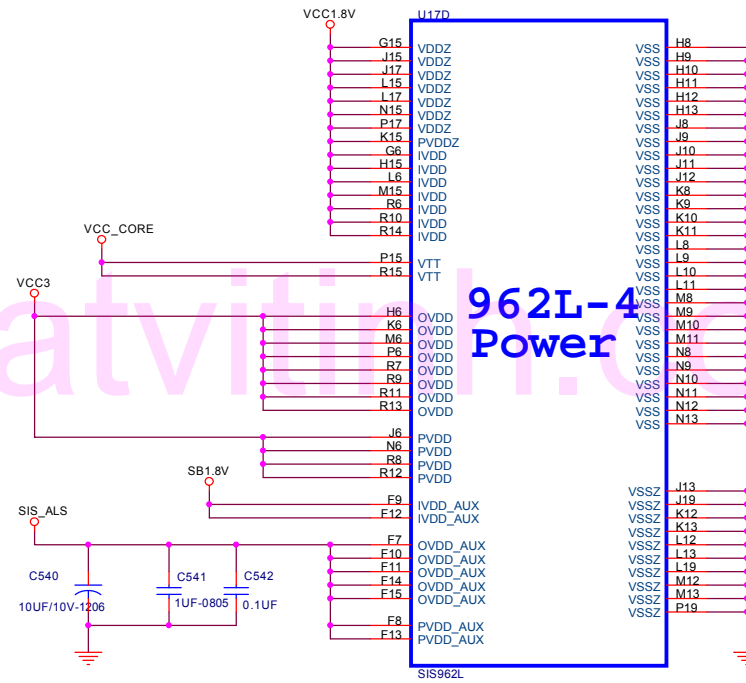
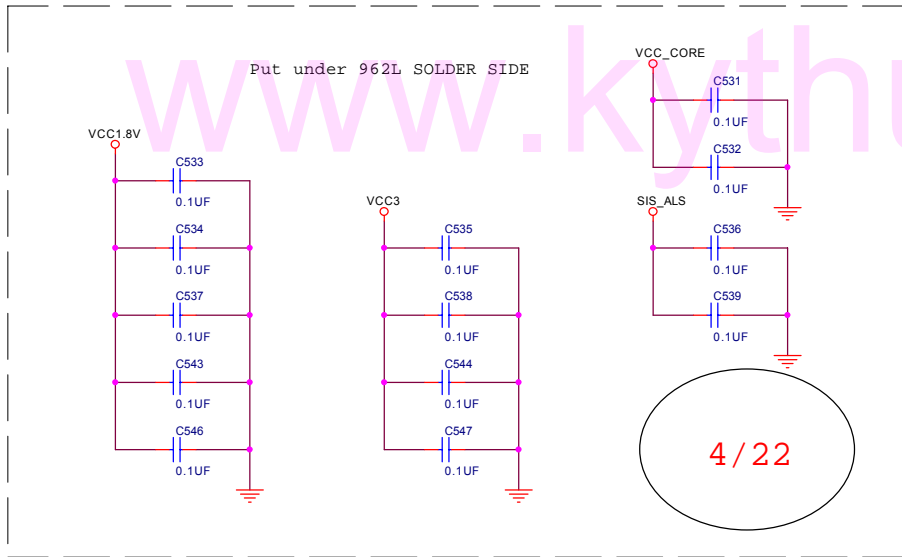
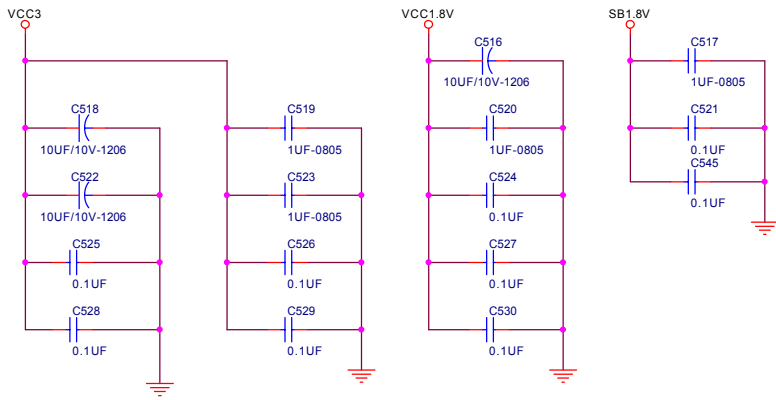


Elitegroup Computer Systems

Title: 962L-3(USB/OTHERS)

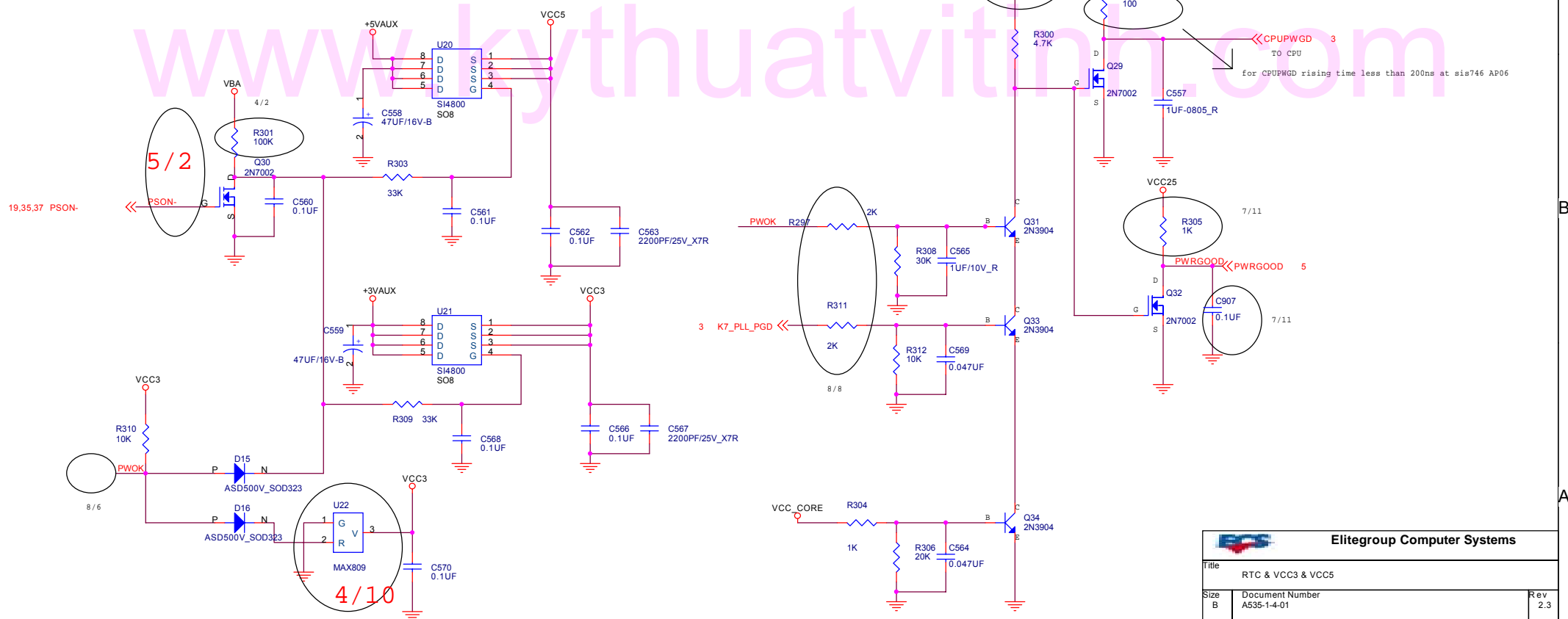
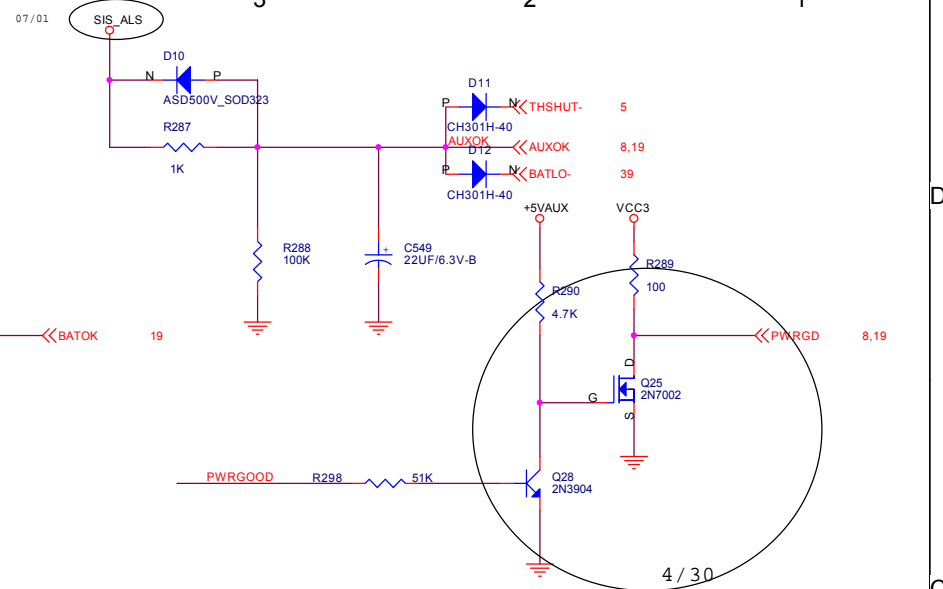
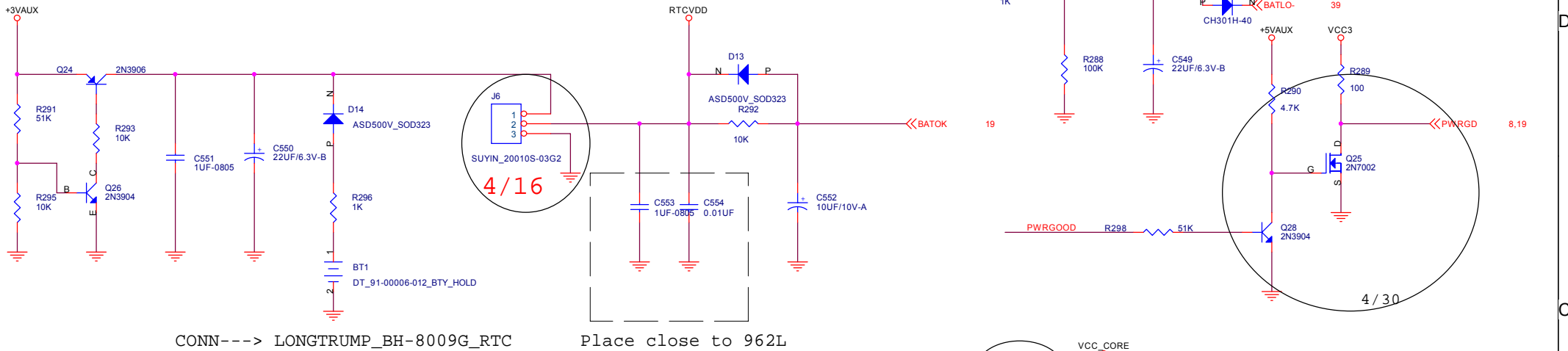
Size B Document Number: A535-1-4-01 Rev 2.3

Date: Tuesday, May 25, 2004 Sheet 20 of 39

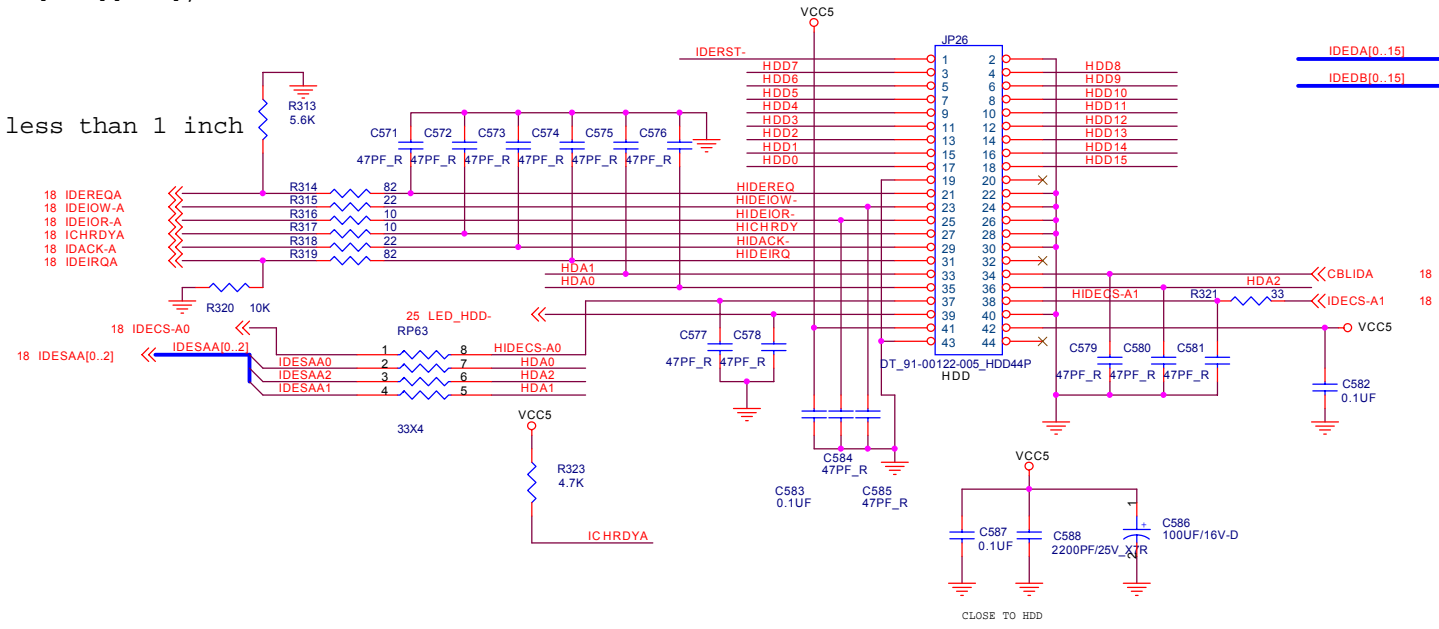


NOTE!

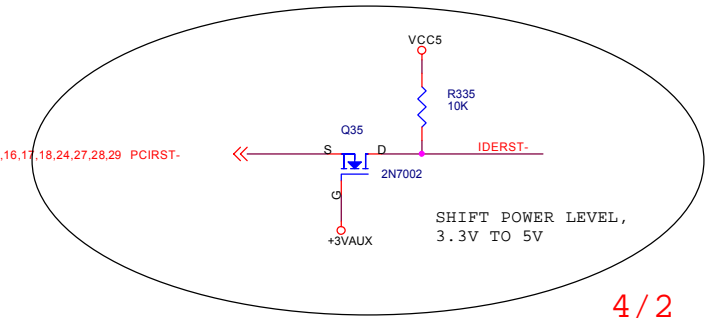
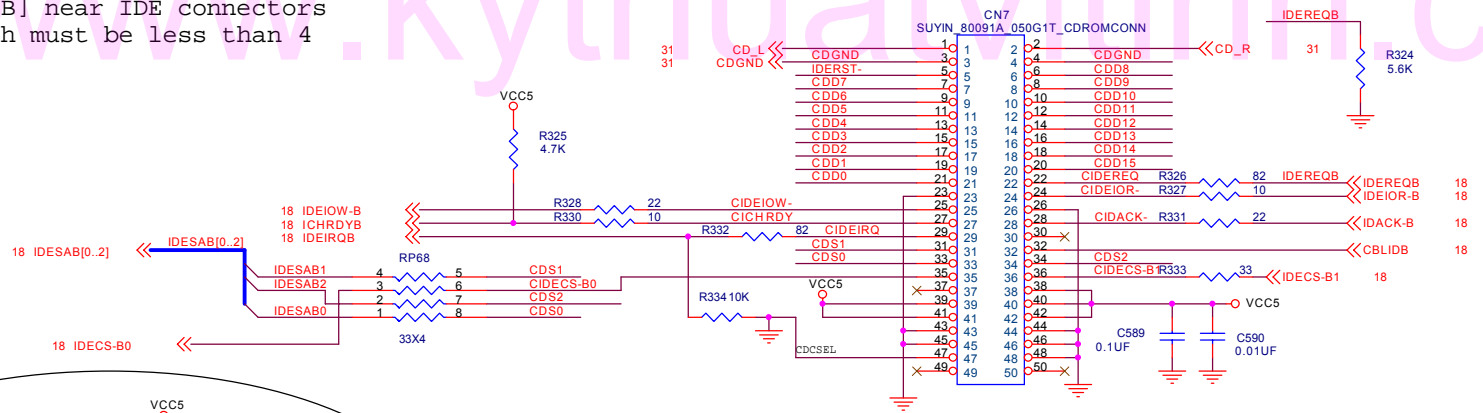
- 1.The RTCVDD is 3V
 - 2.Decoupling capacitor must be close to 962L RTCVDD pin.
 - 3.RTC circuit must strictly follow SiS's recommended design
- SiS is not responsible for RTC problems from foreign designs.



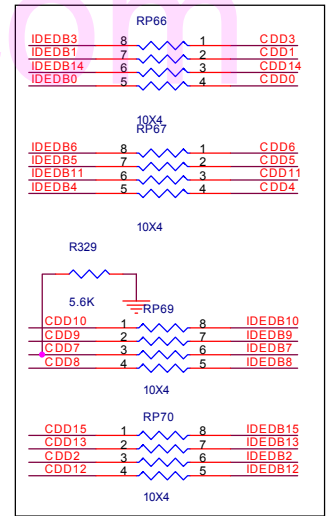
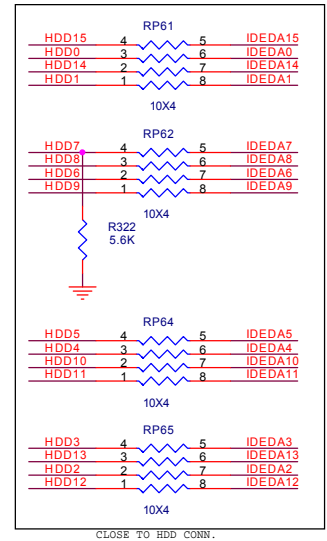
Place the damping resistors for
 IDEA[2:0][A:B], IDECS[1:0][A:B],
 IDEIOR[A:B]#,
 IDEIOW[A:B]#, and
 IDACK[A:B]# near
 SiS962L
 The length must be less than 1 inch



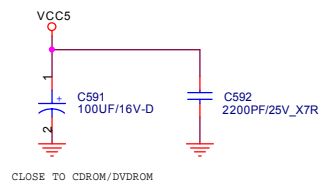
Place the damping resistors for
 IDED[15:0][A:B], IDREQ[A:B],
 ICHRDY[A:B], and
 IDEIRQ[A:B] near IDE connectors
 The length must be less than 4
 inches



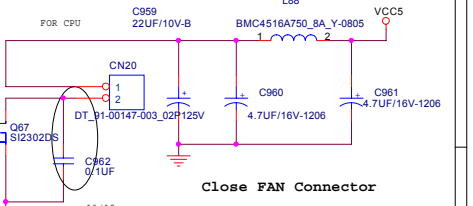
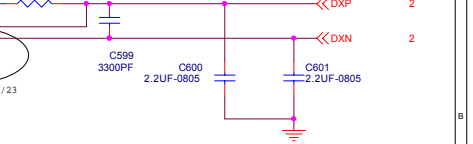
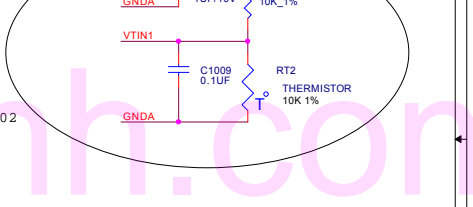
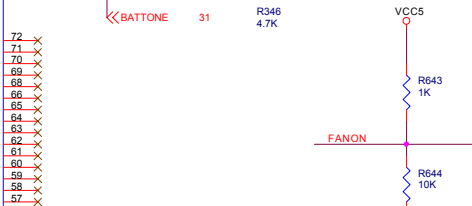
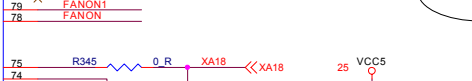
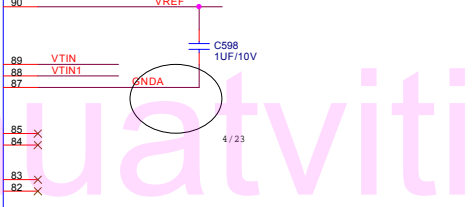
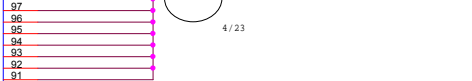
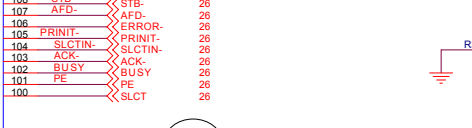
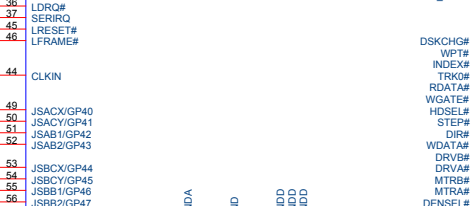
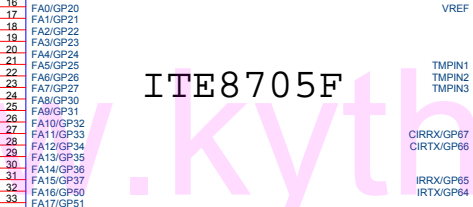
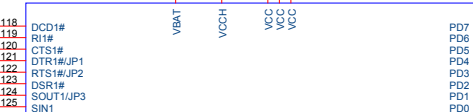
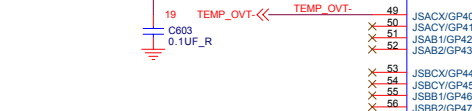
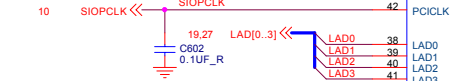
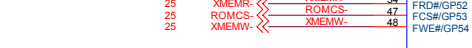
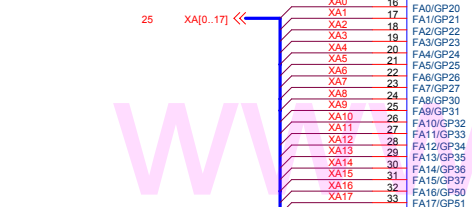
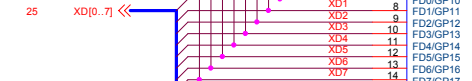
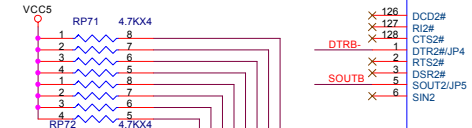
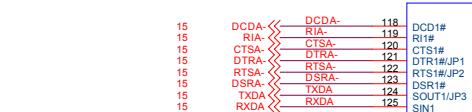
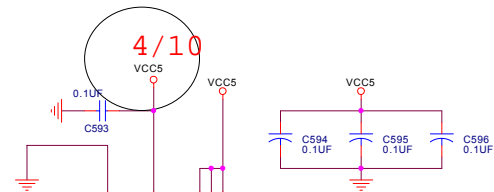
4/2



CSEL : "NC" ; "Hi" --> Master(CDROM)/Slave(DVDROM)
 CSEL : "Low" --> Slave(CDROM)/Master(DVDROM)

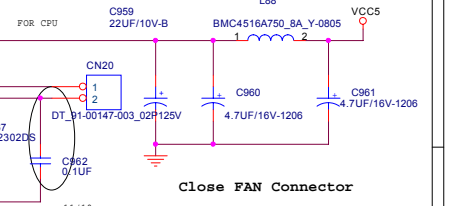
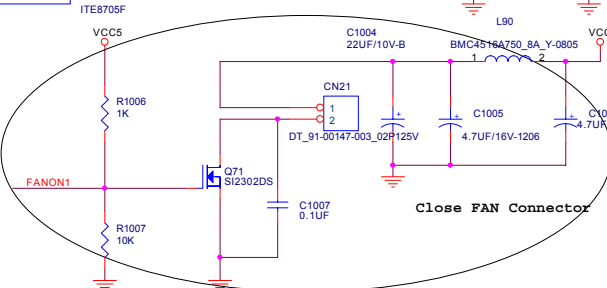


JP4:
 1-2:CIR Password Function Enable
 2-3:CIR Password Function Disable



ITE8705F

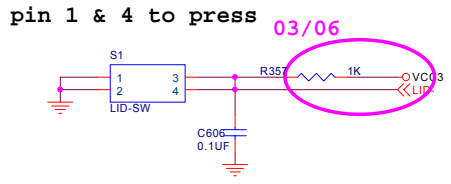
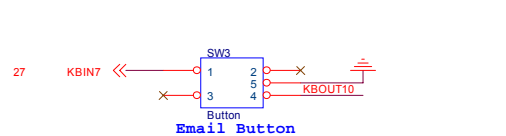
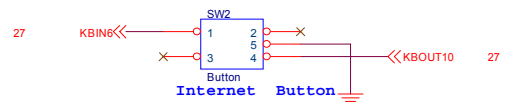
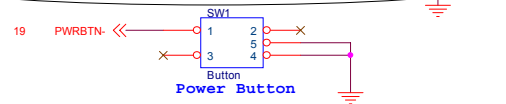
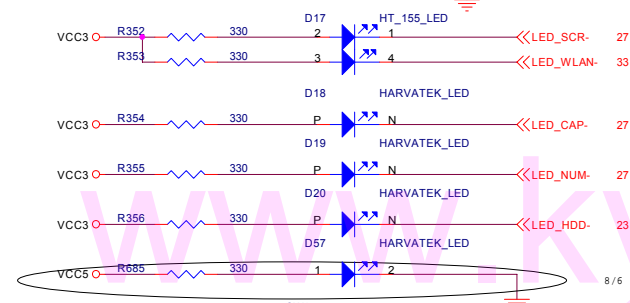
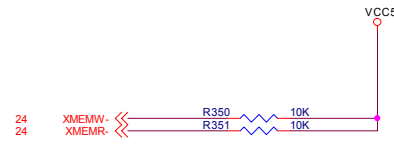
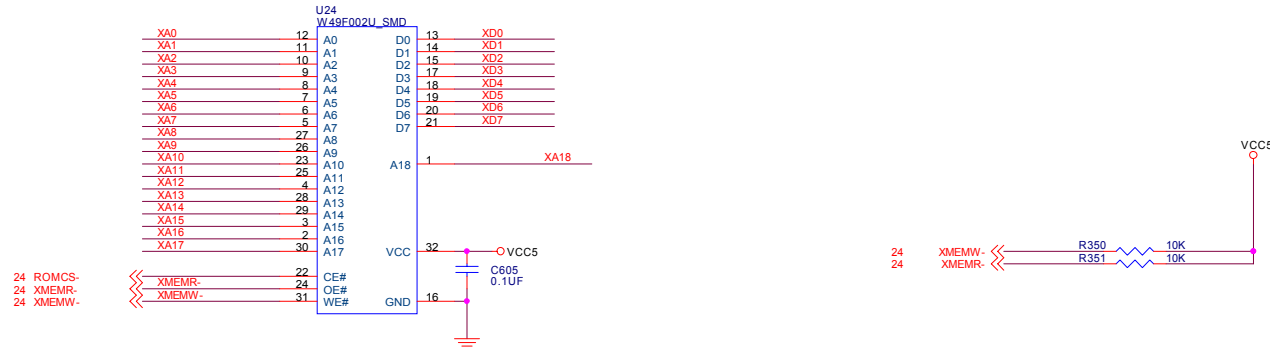
www.kyrbuatvitinh.com

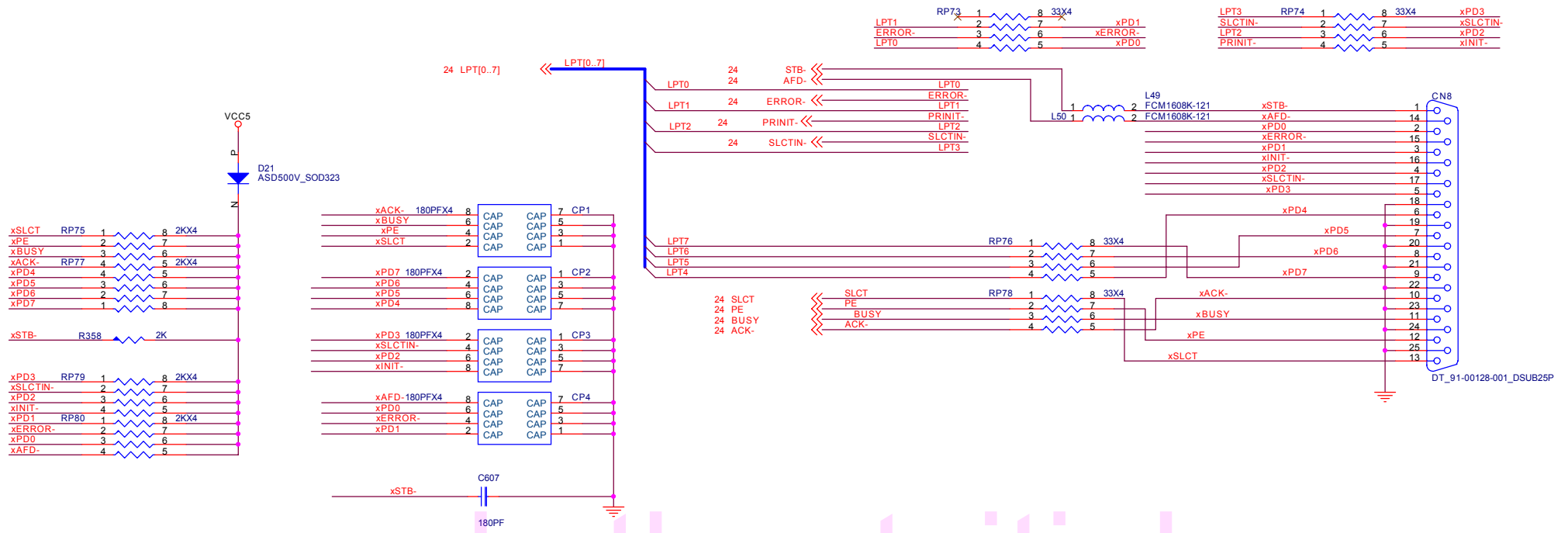


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File	ITE 8705F	
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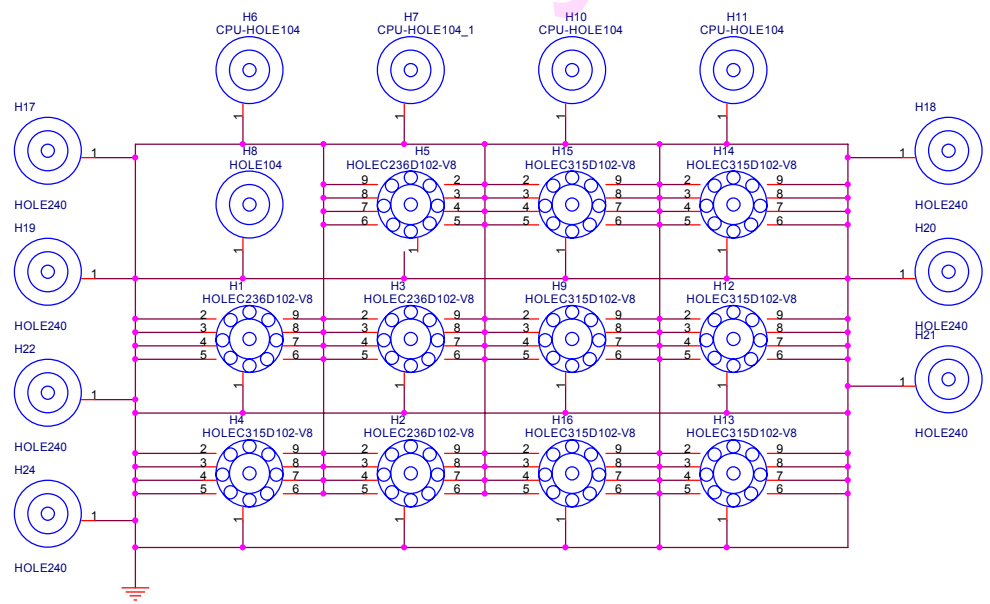
24 XA[0..18] << XA[0..18]
 24 XD[0..7] << XD[0..7]

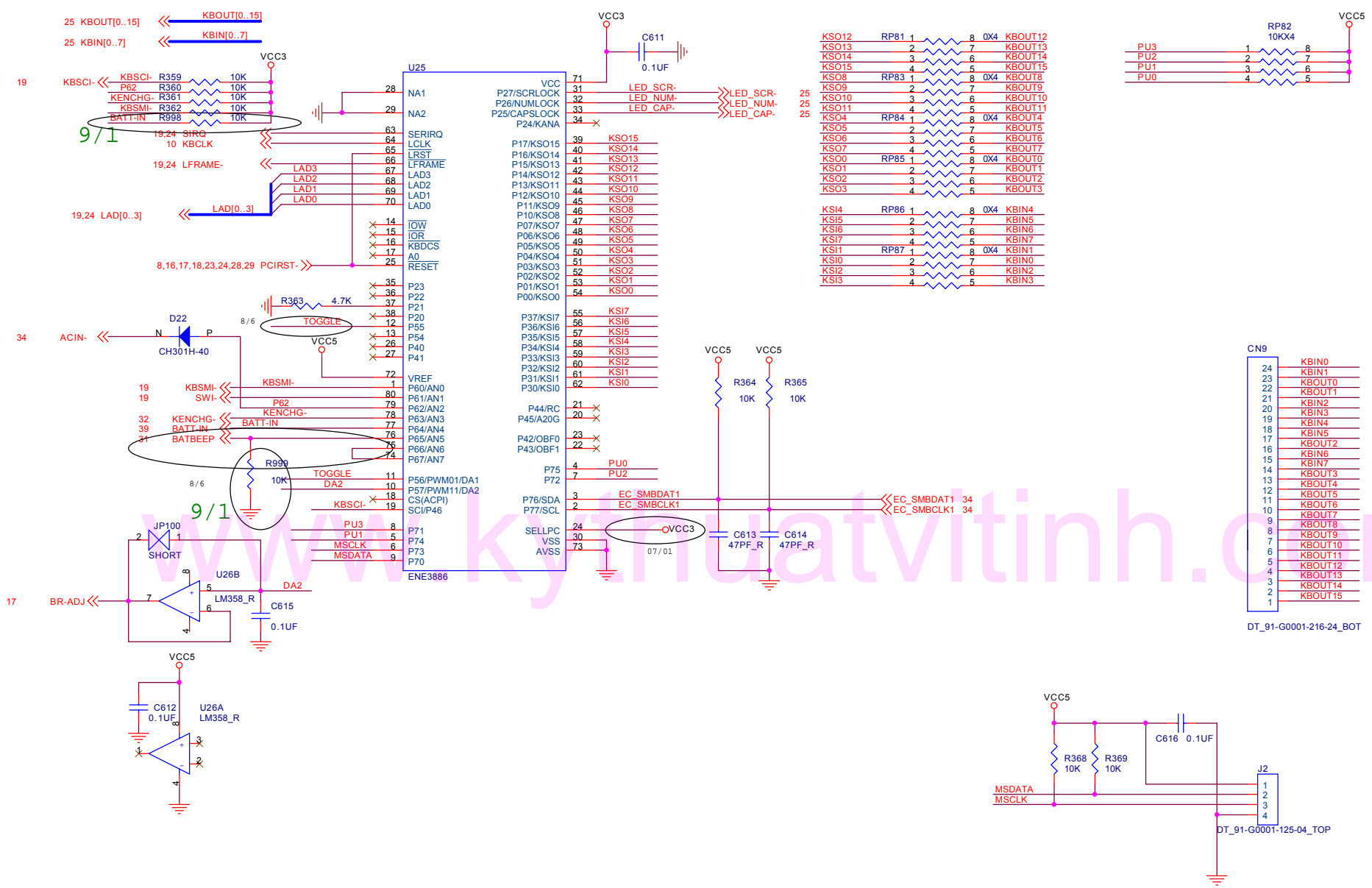
USE WINBOND





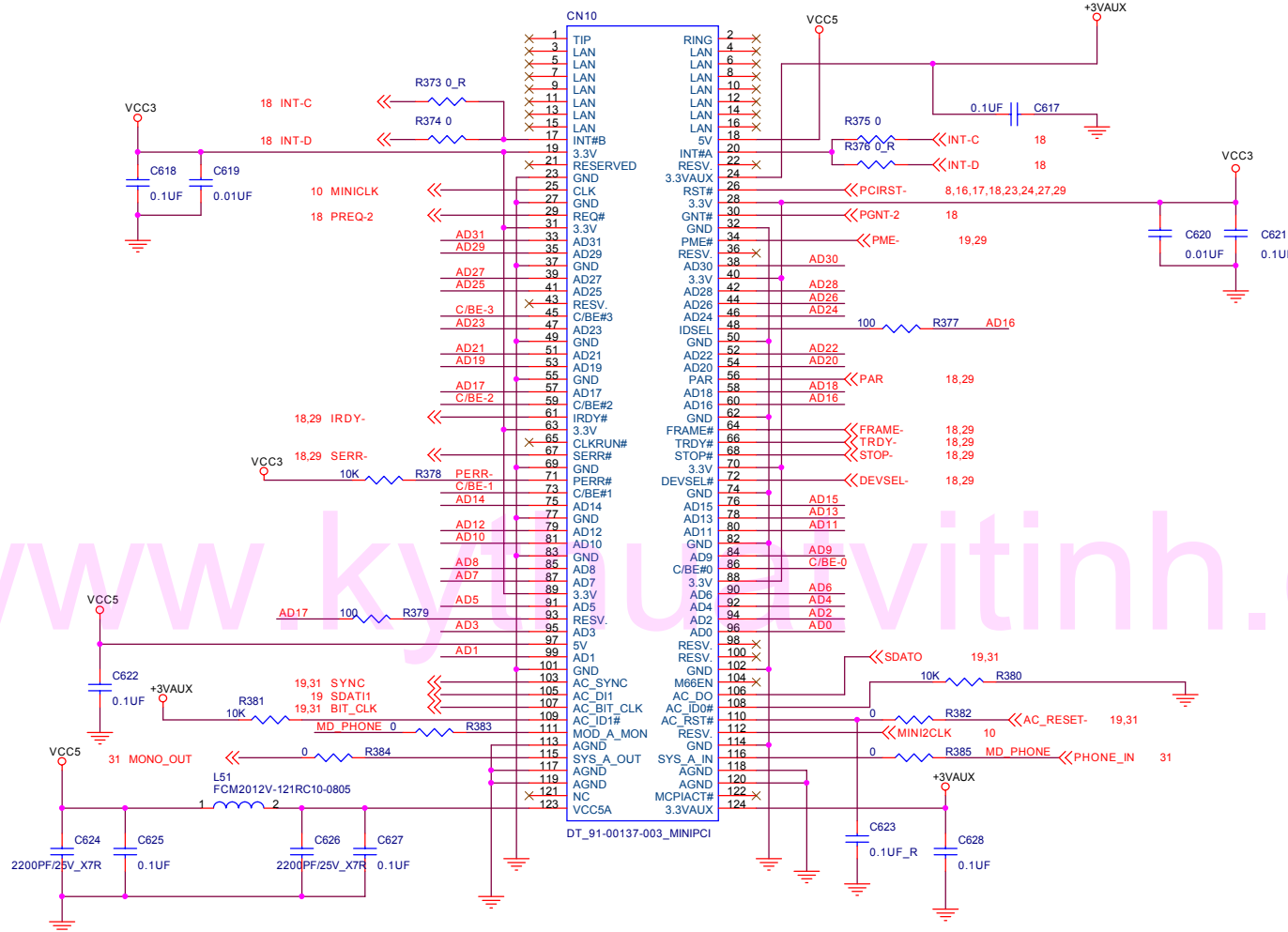
www.kythuatvithinh.com

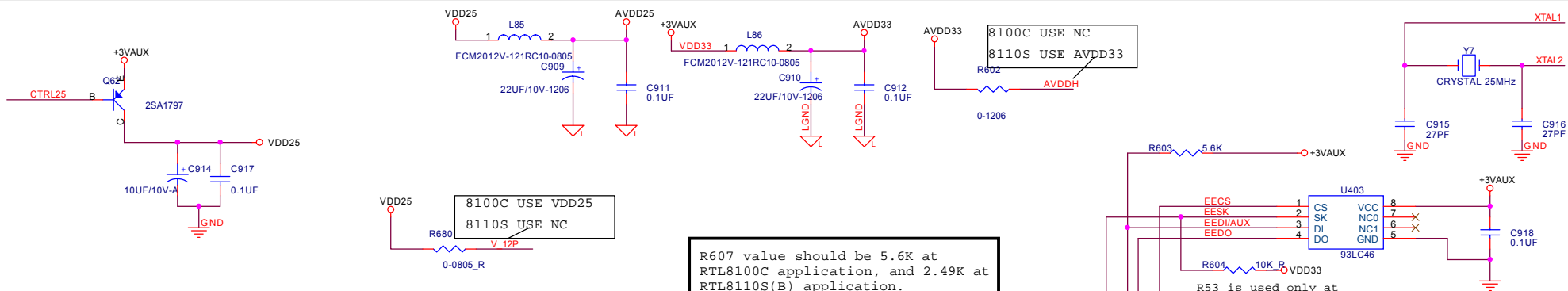




18,29 AD[0..31] << AD[0..31]
 18,29 C/BE-[0..3] << C/BE-[0..3]

MINI PCI SOCKET

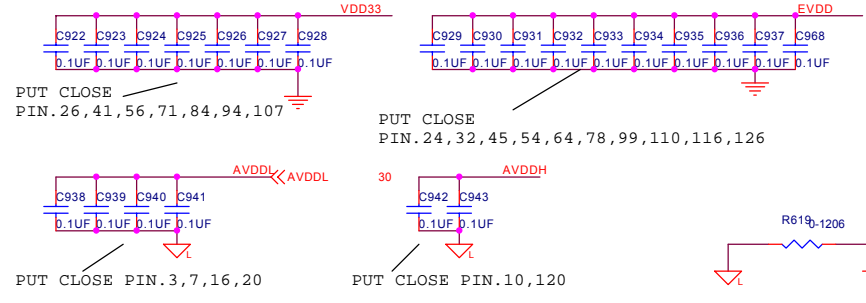
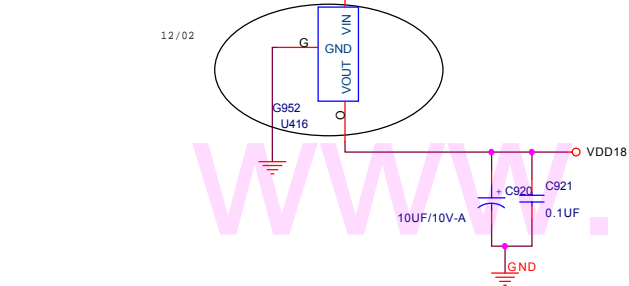
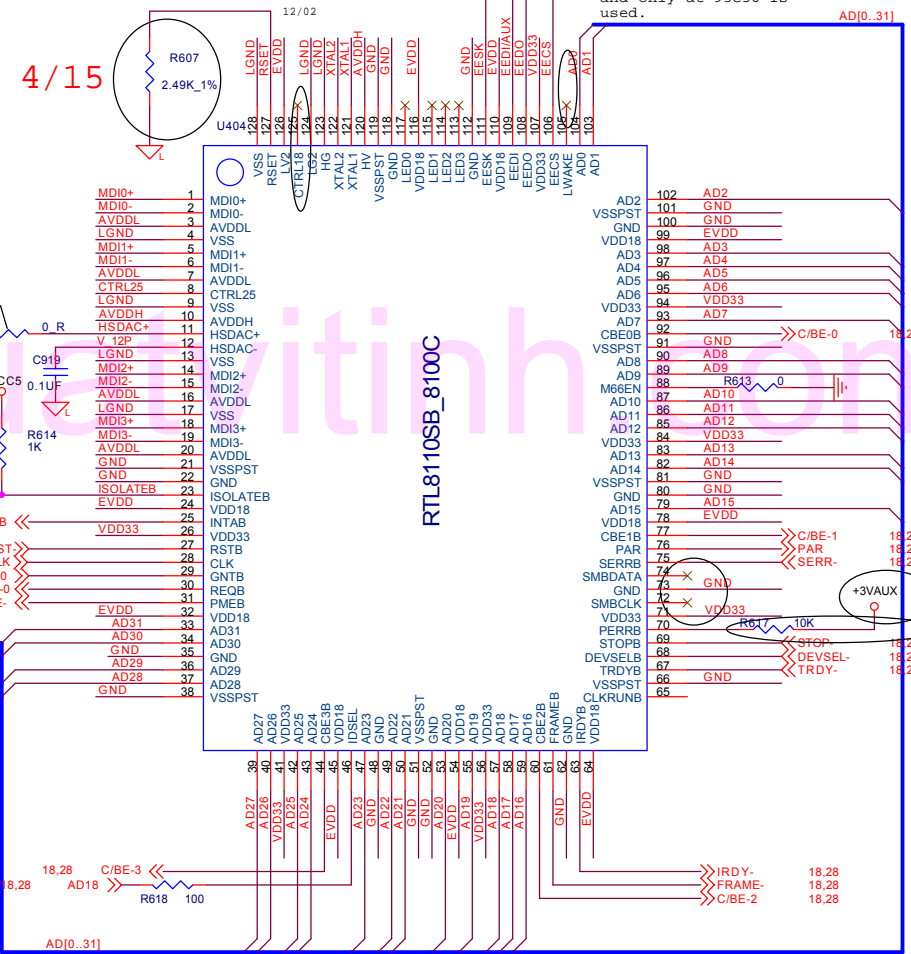


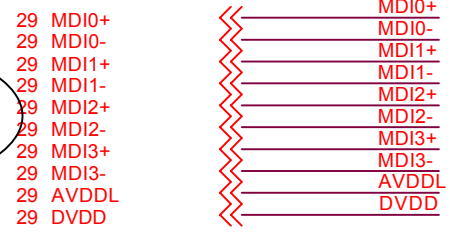
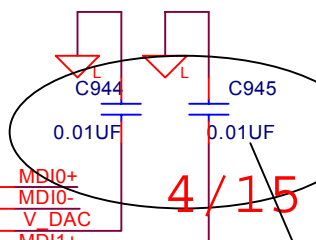
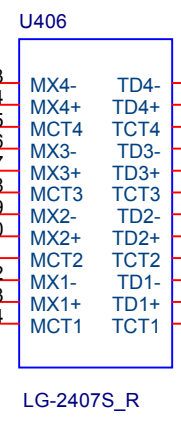
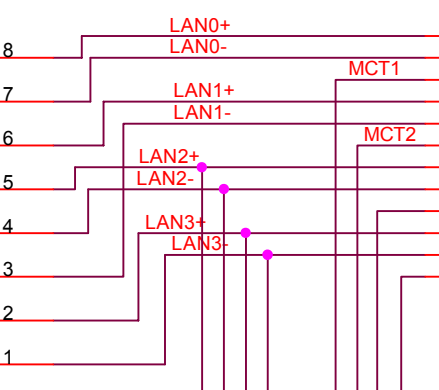
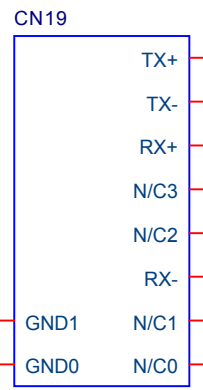


R607 value should be 5.6K at RTL8100C application, and 2.49K at RTL8110S(B) application.

R53 is used only at RTL8110S(B) application and only at 93C56 is used.

Keep R611at RTL8110SB application.





U408 PIN1 USE THE SAME CAP(C945) WITH U406 PIN 7



4/15

4/15

7/1

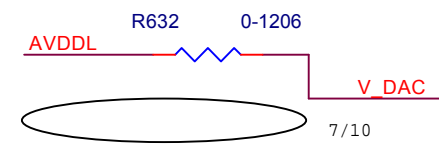
At RTL8100C application, remove R628, R629, R630, R631, C956, C957, C948, C949, C944, and change C945 value from .01uF to .1uF.

R632 and R633 are only for RTL8110S application. Remove R633 and keep R632 for default application. Keep R633 and remove R632 for low power consumption. For RTL8100C and RTL8110SB applications, remove both R632 and R633.

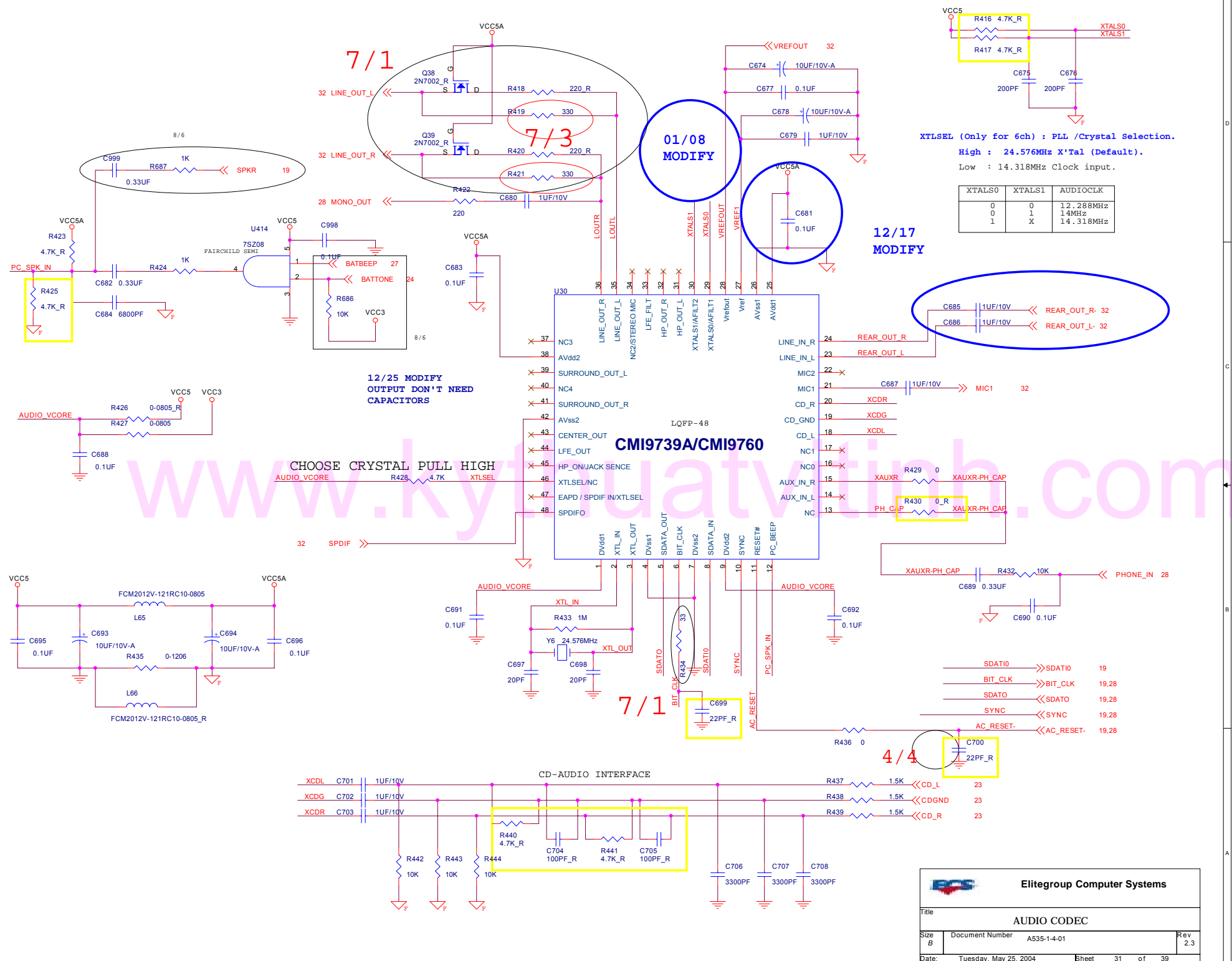
U408 AND U406 DUAL LAY

9/25

(CONNECT TO CHASSIS GND)



Elitegroup Computer Systems		
Title RJ45		
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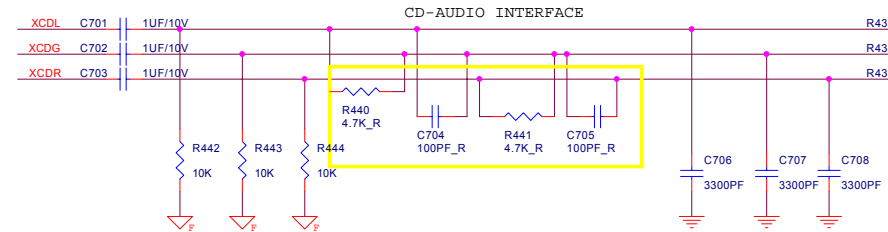


XTLSEL (Only for 6ch) : PLL /Crystal Selection.
 High : 24.576MHz X'Tal (Default).
 Low : 14.318MHz Clock input.

XTALSO	XTALS1	AUDIOCLK
0	0	12.288MHz
0	1	14MHz
1	X	14.318MHz

12/25 MODIFY
 OUTPUT DON'T NEED
 CAPACITORS

CHOOSE CRYSTAL PULL HIGH
 AUDIO_VCORE R428 4.7K XTLSEL

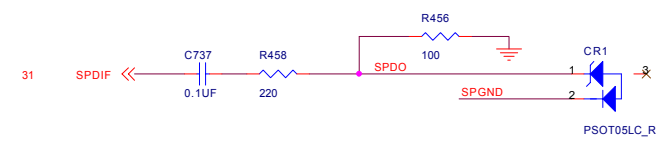
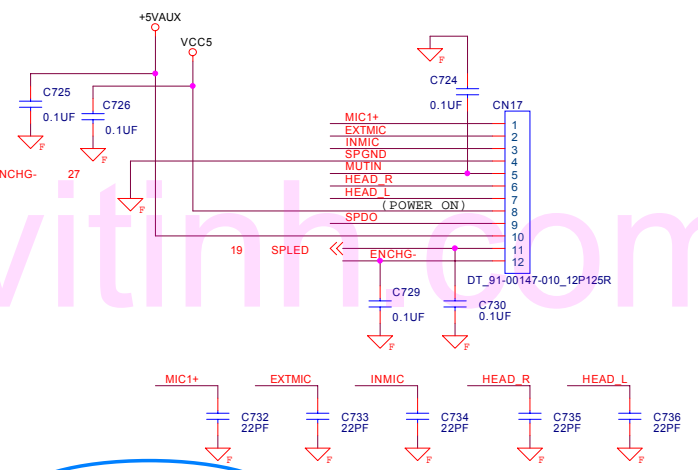
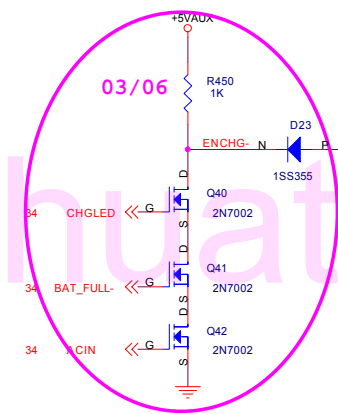
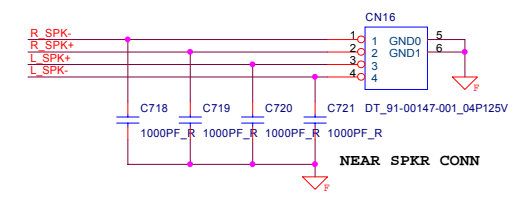
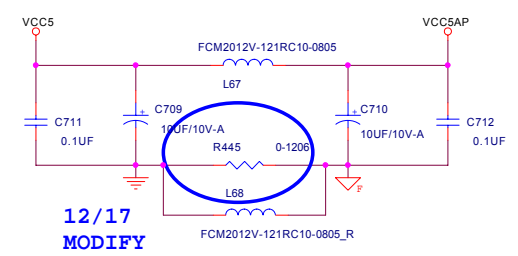
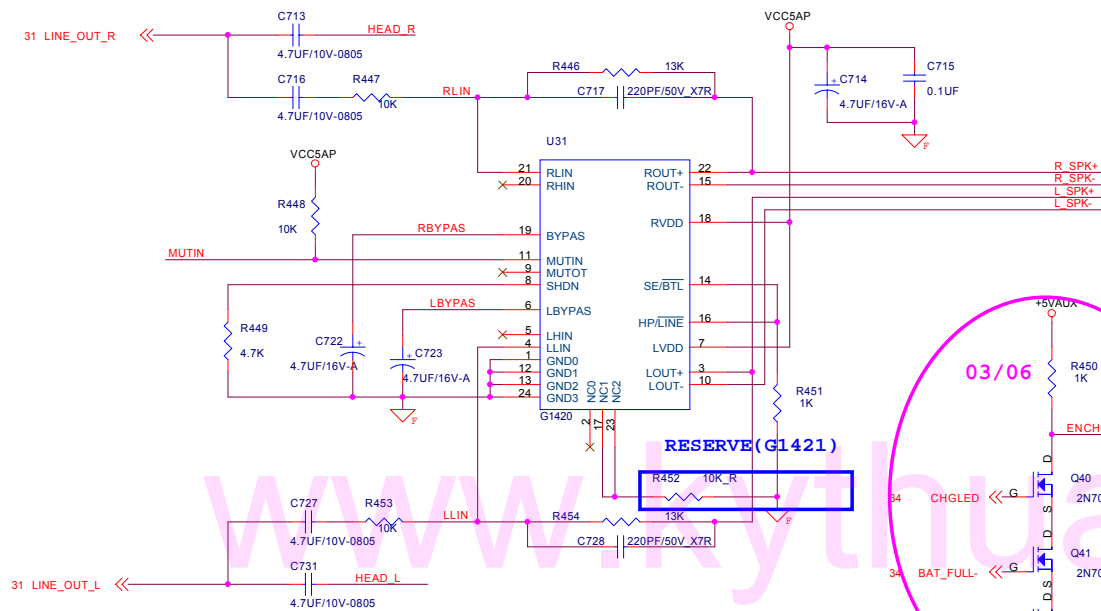


Elitegroup Computer Systems

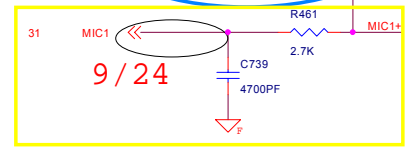
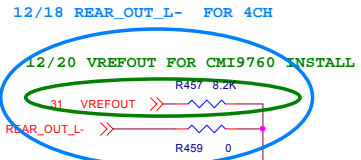
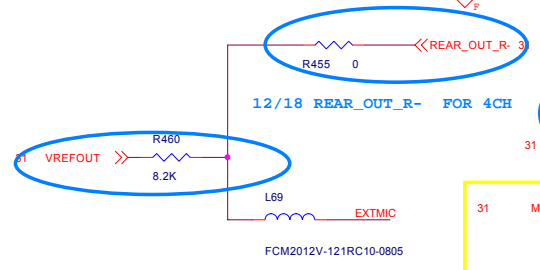
Title: **AUDIO CODEC**

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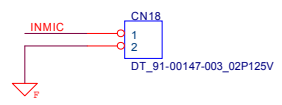
12/20 VREFOUT FOR 4CH



PC2001 SPEC. 12KHz--15KHz

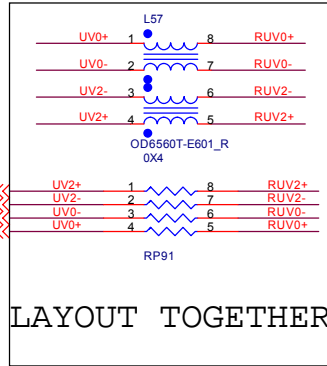
$F_c = 1 / [2 * 3.14 * R(2.7K) * C(4700PF)] = 12.548KHz$

VREFOUT CONTROL MIC & REAR_OUT_R/L FUNCTION

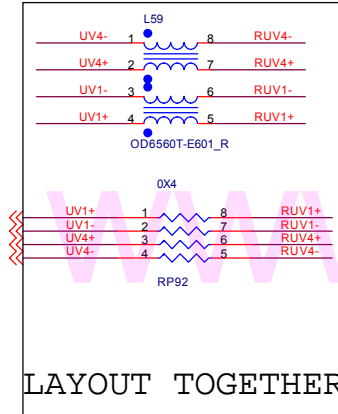


Elitegroup Computer Systems			
Title OPA & AUDIO JACK			
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20 UV2+
20 UV2-
20 UV0-
20 UV0+

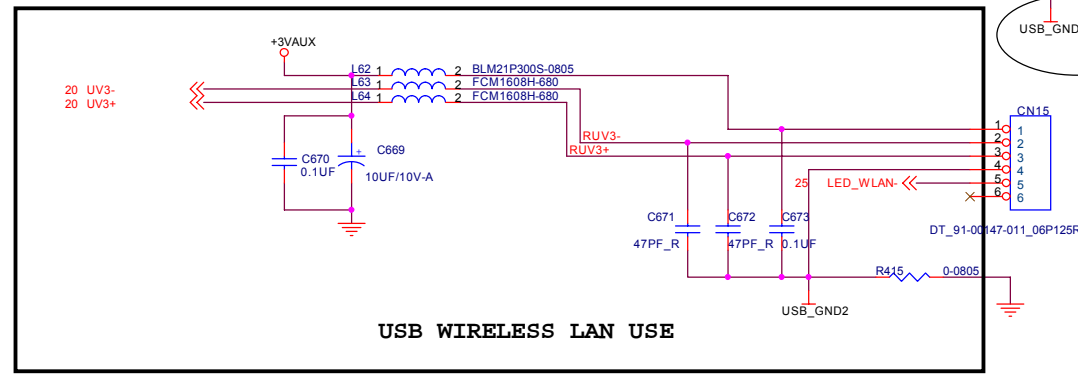
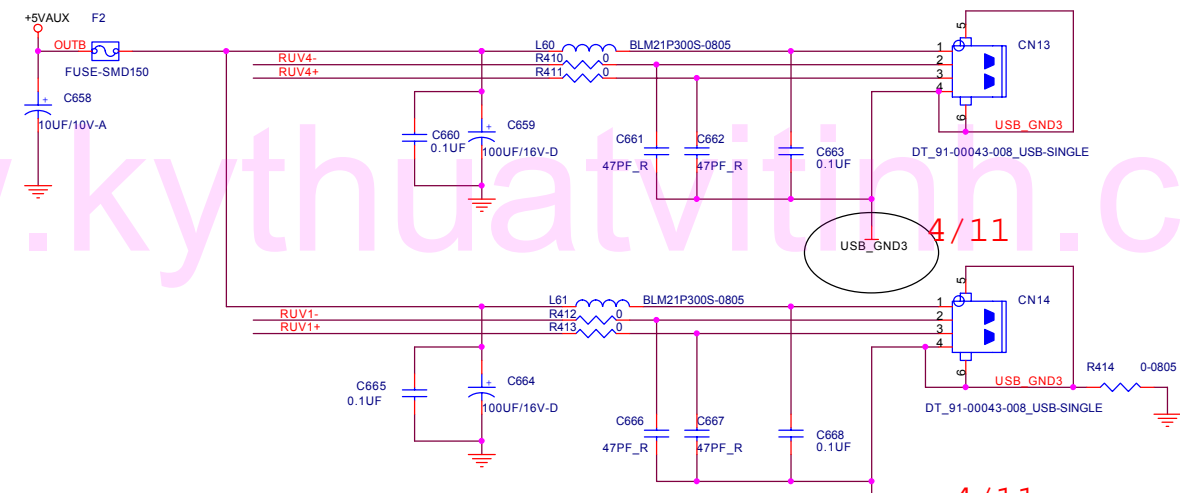
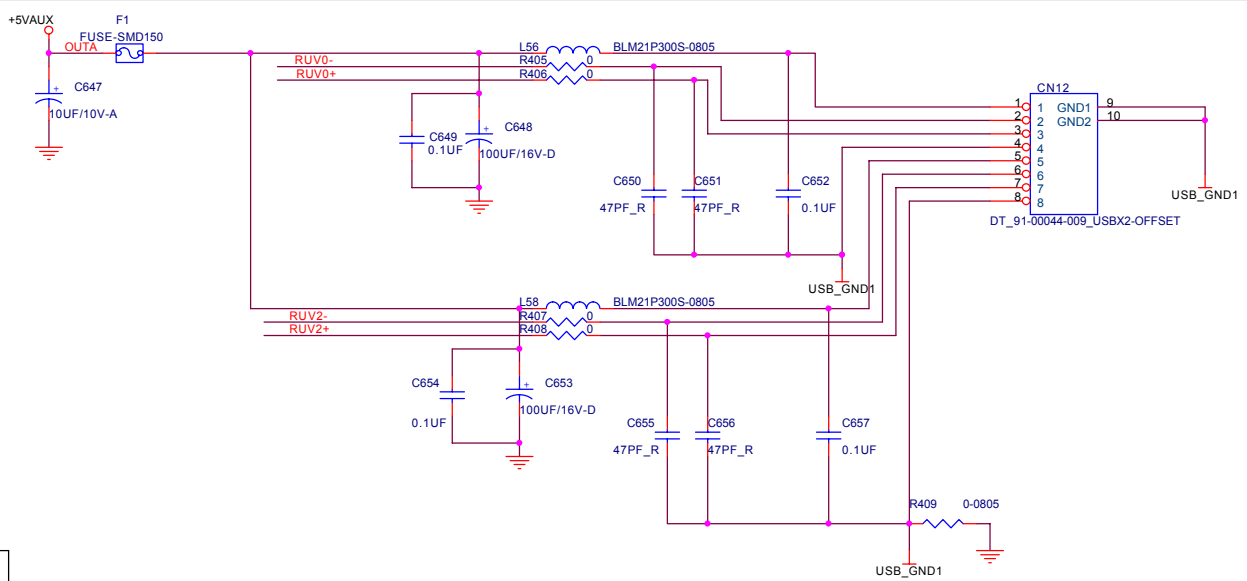



20 UV1+
20 UV1-
20 UV4+
20 UV4-



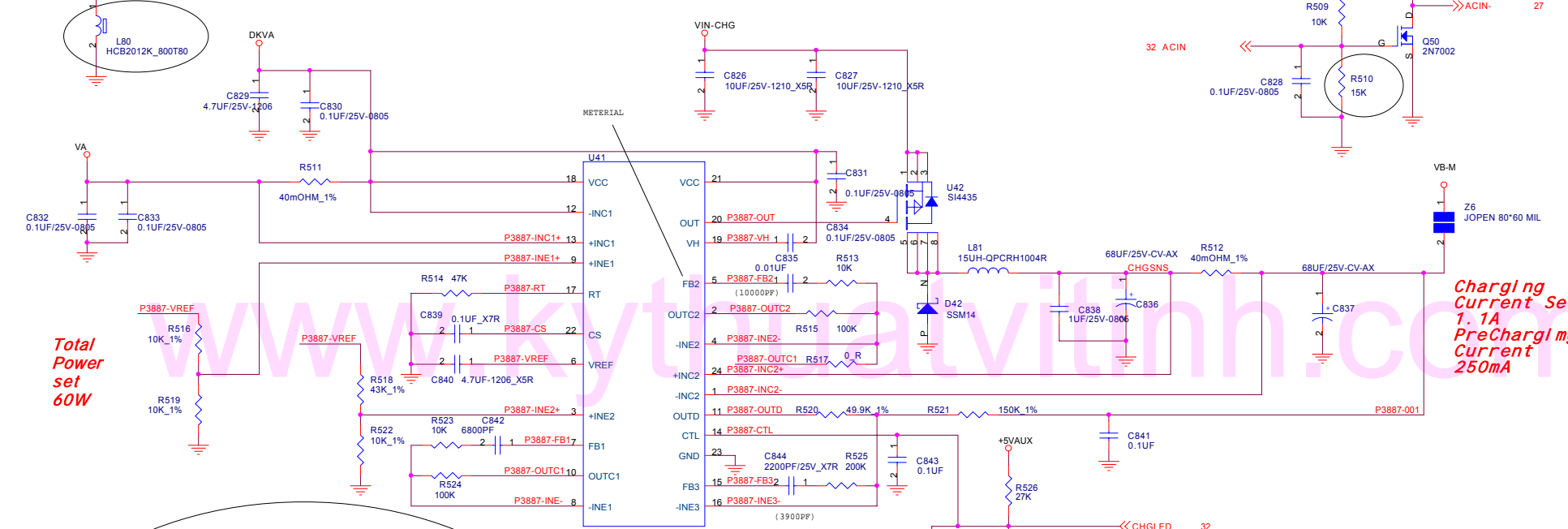
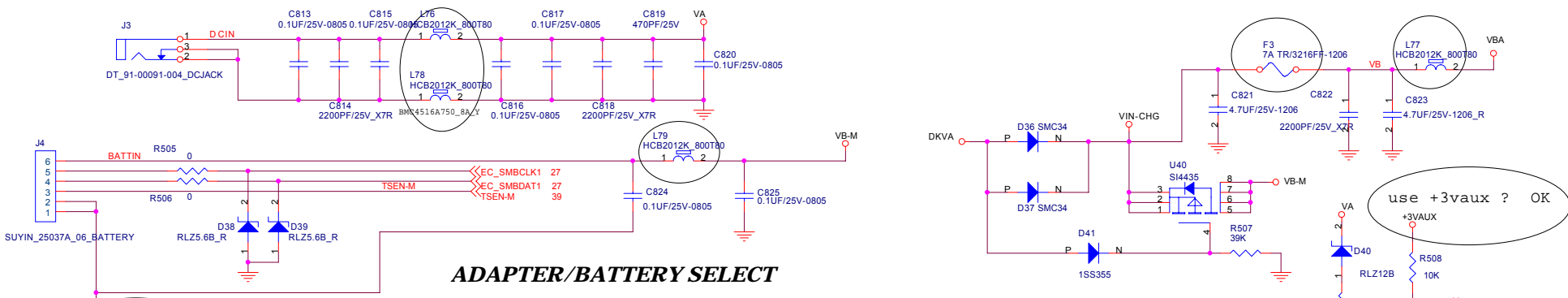
7/1
ALL THIS
PAGE

ALL THESE CLOSE TO CONNECTOR

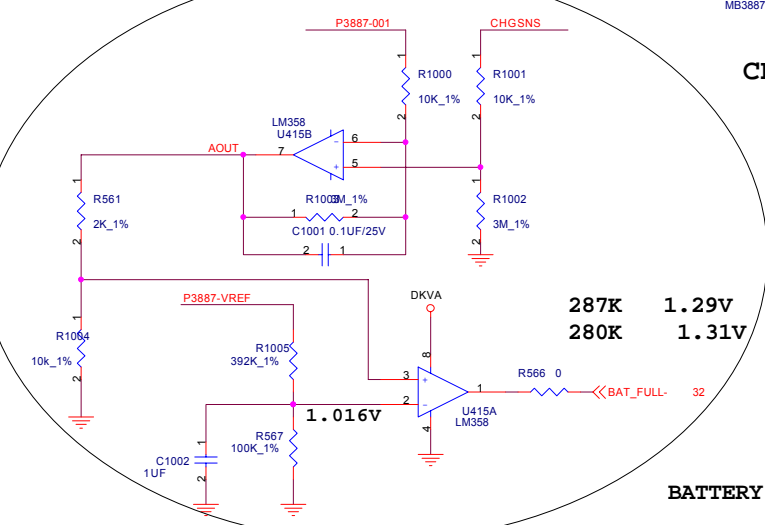


 Elitegroup Computer Systems		
Title: USB PORT		
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ADAPTER/BATTERY SELECT

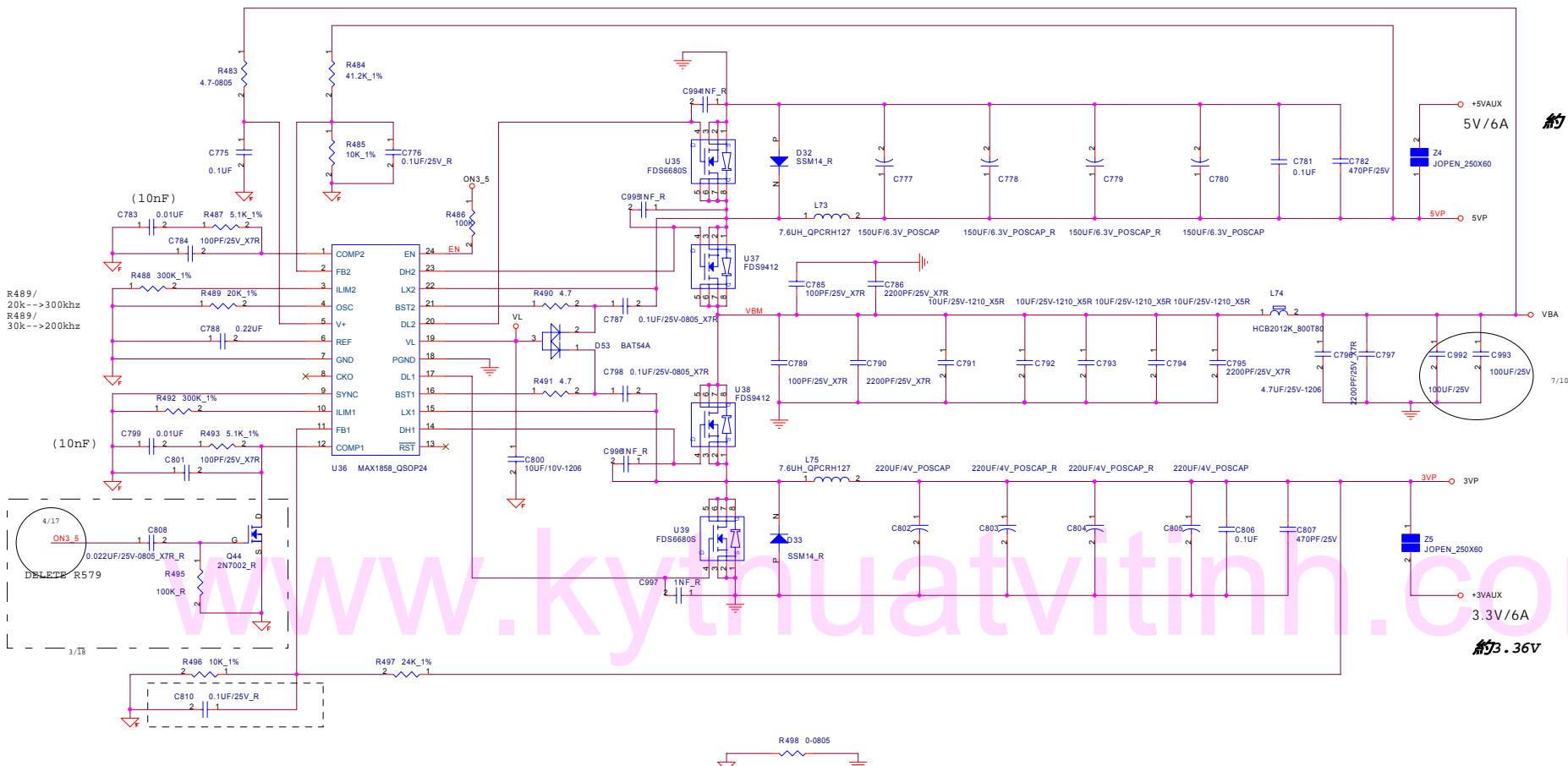


CHARGE



BATTERY FULL VOLTAGE PROTECT





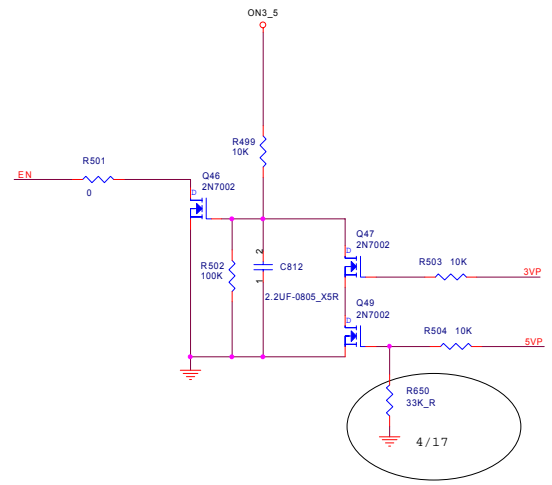
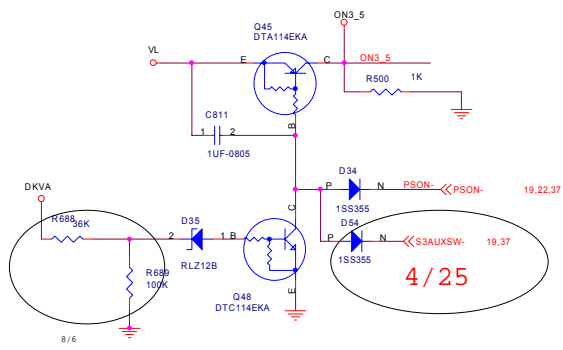
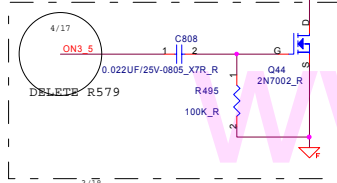
R489/
20k-->300khz
R489/
30k-->200khz

約 5.1V

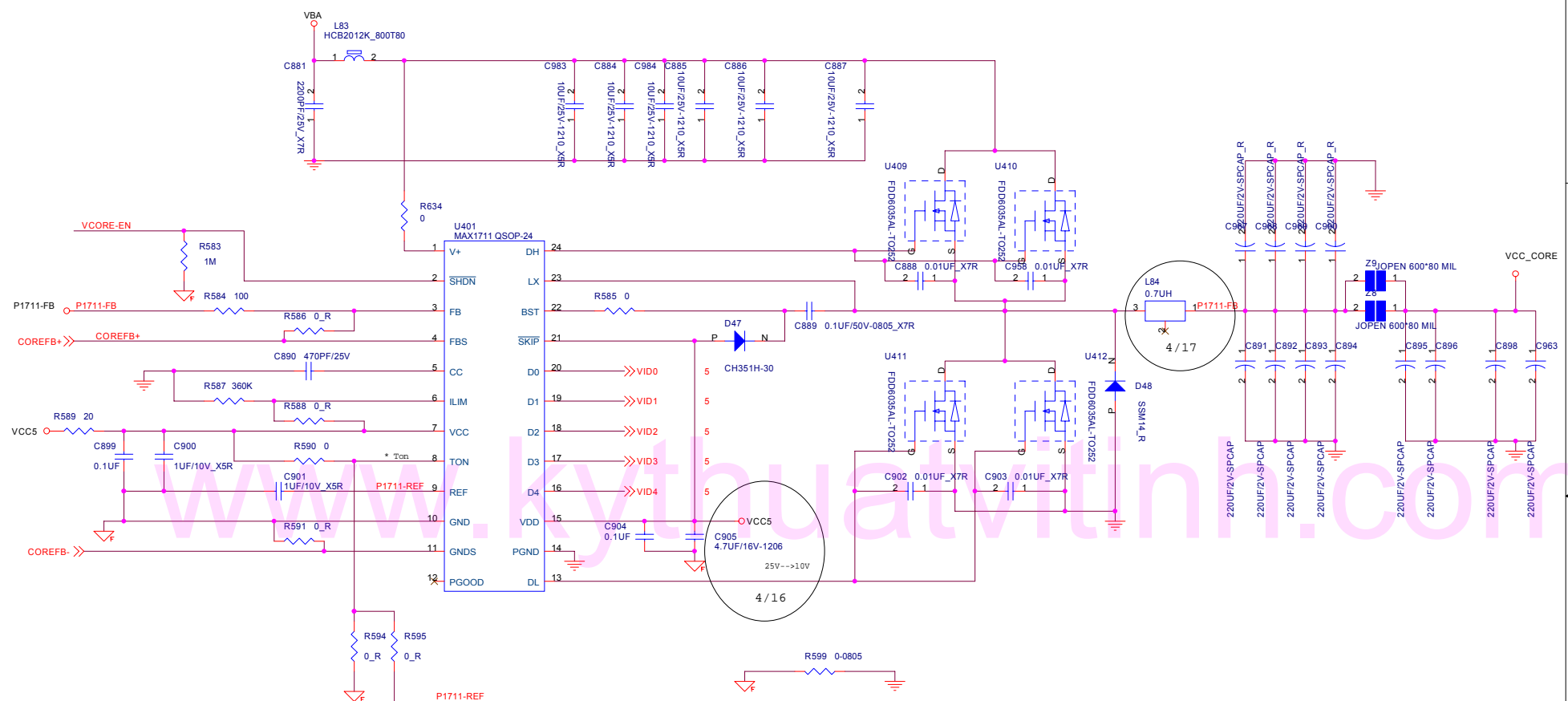
5V/6A

約 3.3V

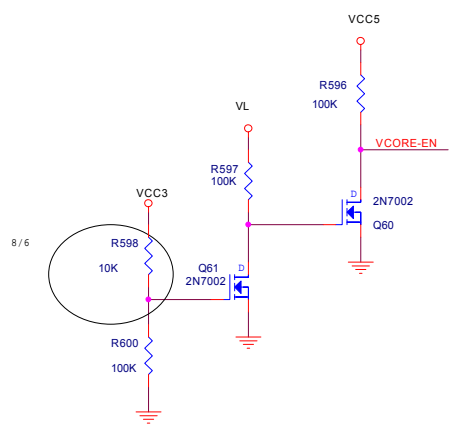
3.3V/6A



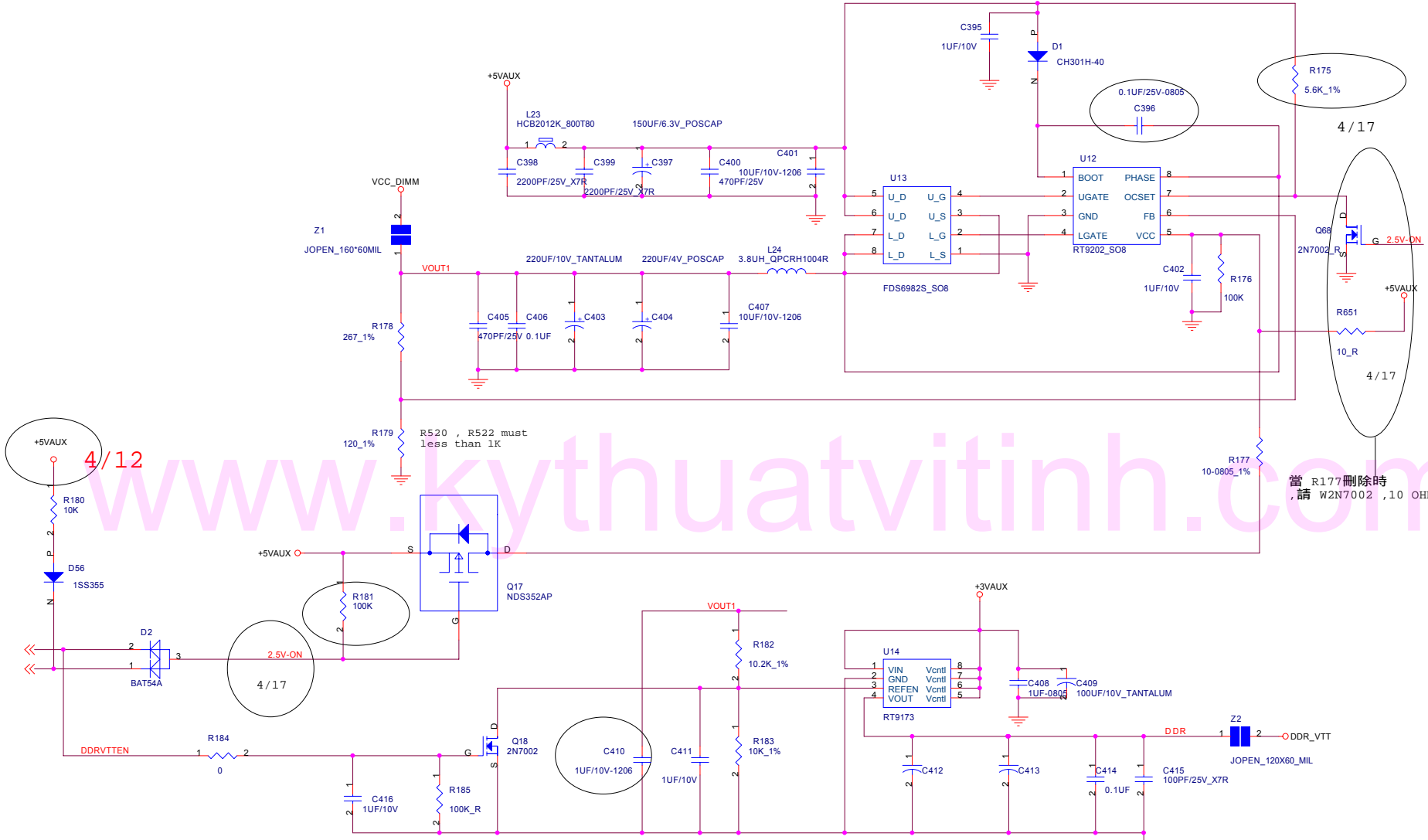
Elitegroup Computer Systems			
Title: MAX1858 DC-DC 2.5V/5VAUX			
Size C:	Document Number	A535-1-4-01	Rev 2.3
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* t_{on}
 OPEN -> 300KHz
 VCC -> 200KHz
 REF -> 400KHz
 GND -> 550KHz

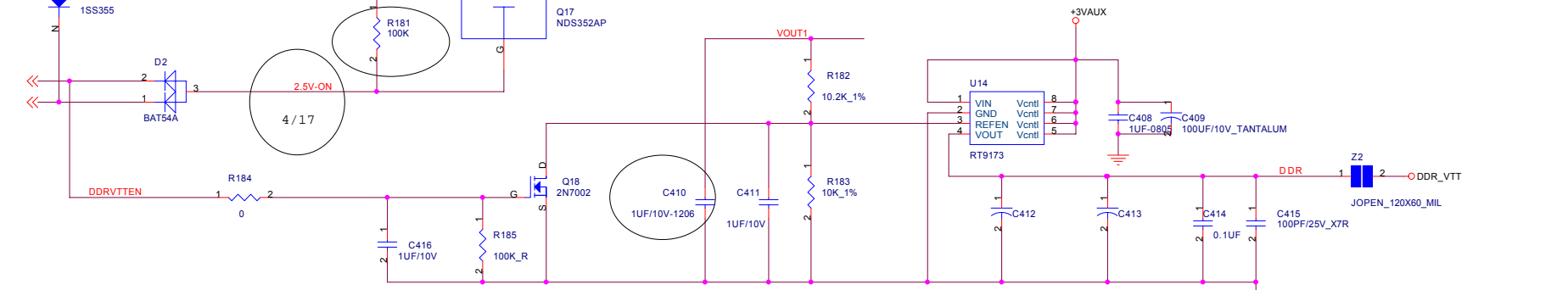


VCC2.5V SUPPLY 5A FOR VCC_DIMM



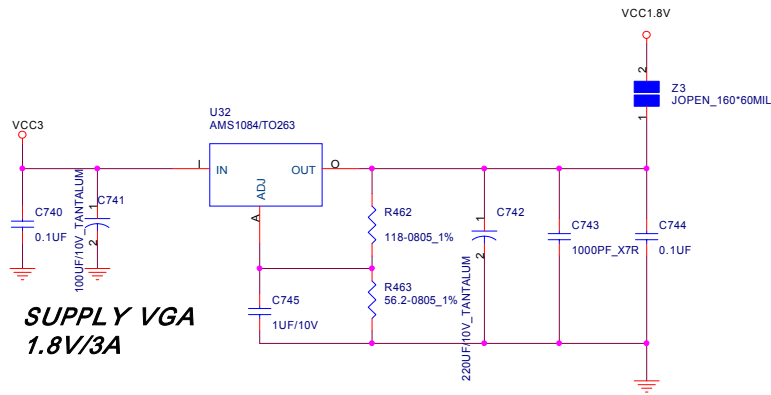
當 R177刪除時，請 W2N7002 ,10 OHM

SUPPLY DDR_VTT 1.25V/1A

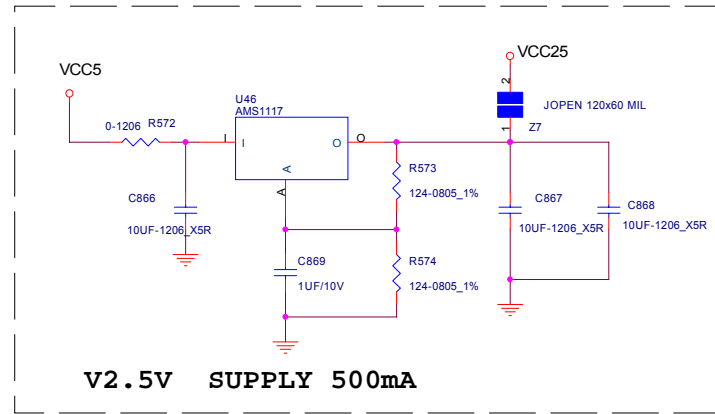


- 3 8.3K .5 7K
- 4 5.9K 6 3K
- 7 2.2K .5 1.97K
- 8 1.71K .5 1.49K
- 9 1.30 .5 1.14
- 10 1.0

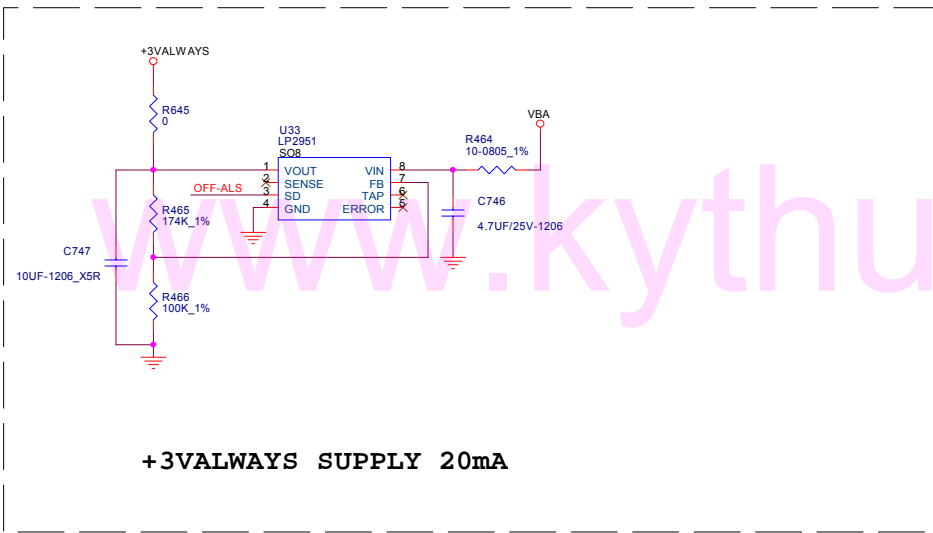
Title DDR POWER (2.5V/1.25V)	
Size Custom	Document Number A535-1-4-01
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**SUPPLY VGA
1.8V/3A**



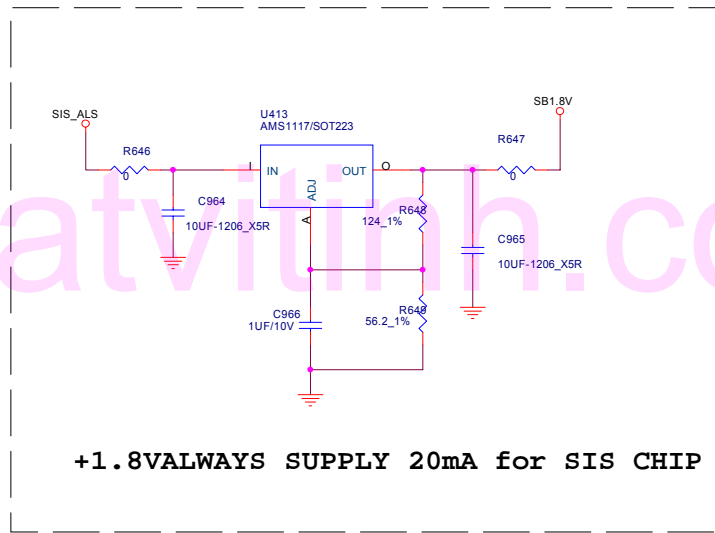
V2.5V SUPPLY 500mA



+3VALWAYS SUPPLY 20mA

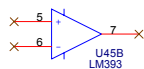
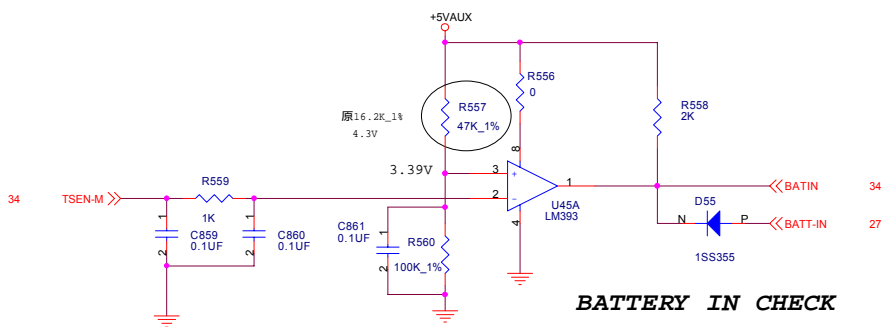
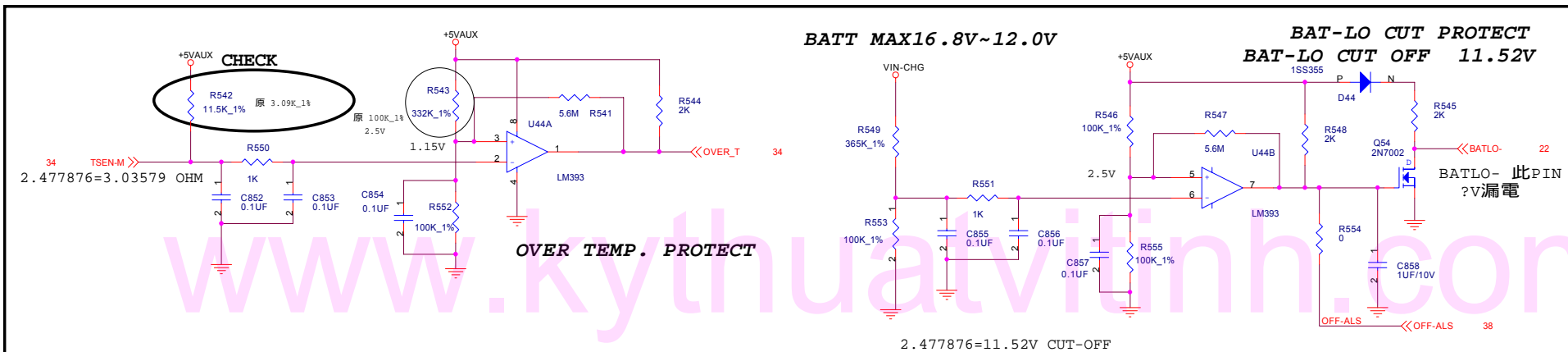
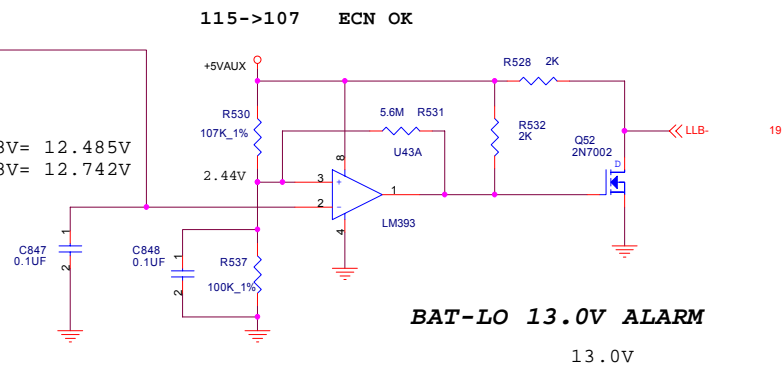
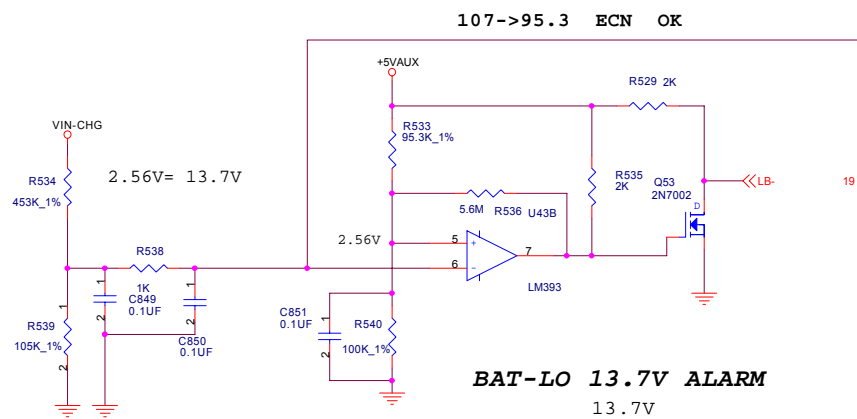
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**未 PLACEMENT
CLOSE CHIPSET**



+1.8VALWAYS SUPPLY 20mA for SIS CHIP

**未 PLACEMENT
CLOSE CHIPSET**



T	MAX	Typ	MIN
0C-->	27.844K	27.303K	26.974K
5C -->	22.442K	22.075K	21.727K
25C-->	10.1k	10.0k	9.9k
55C-->	3.6k	3.54k	3.463k
60C-->	3.083k	3.0215k	2.9536k