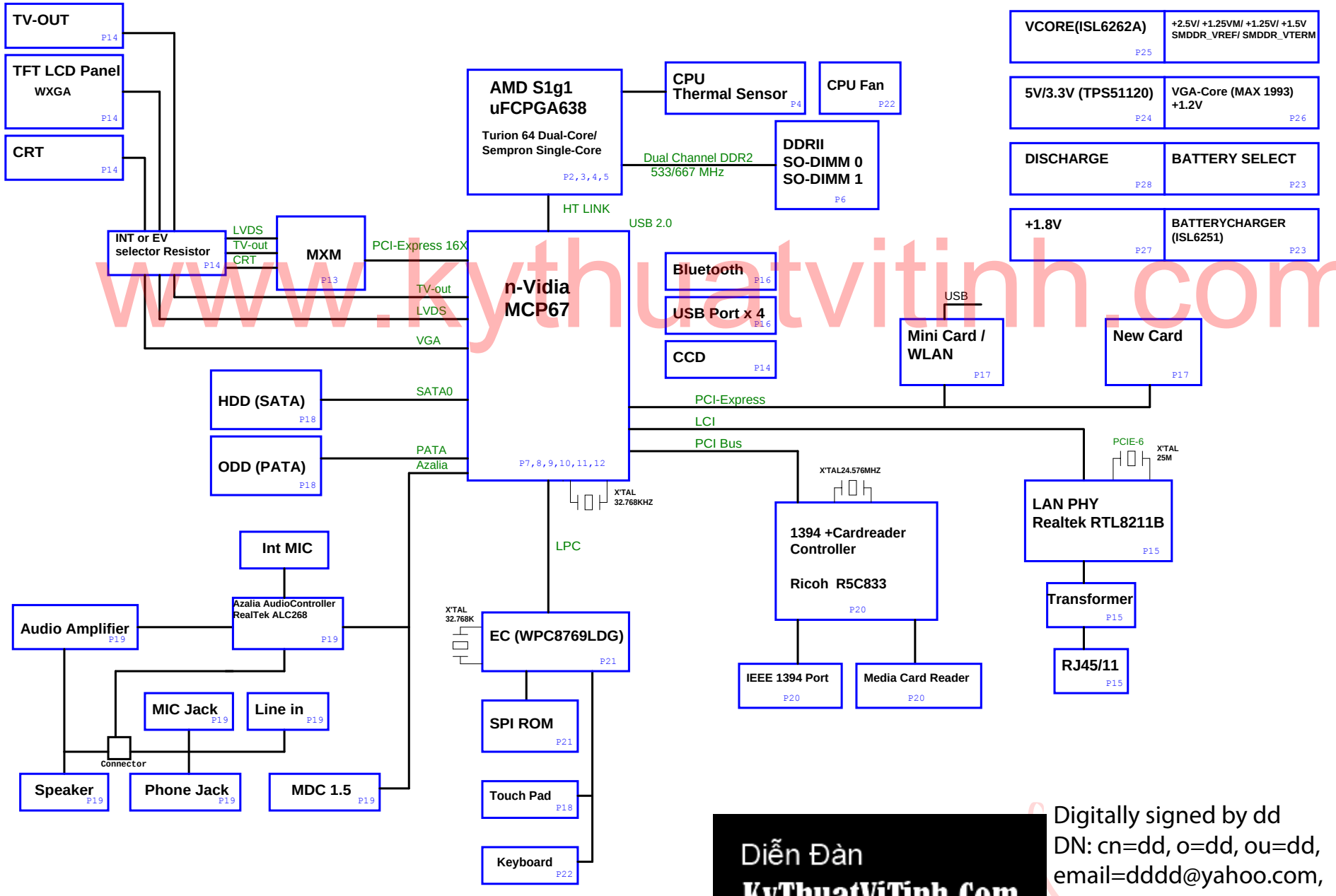
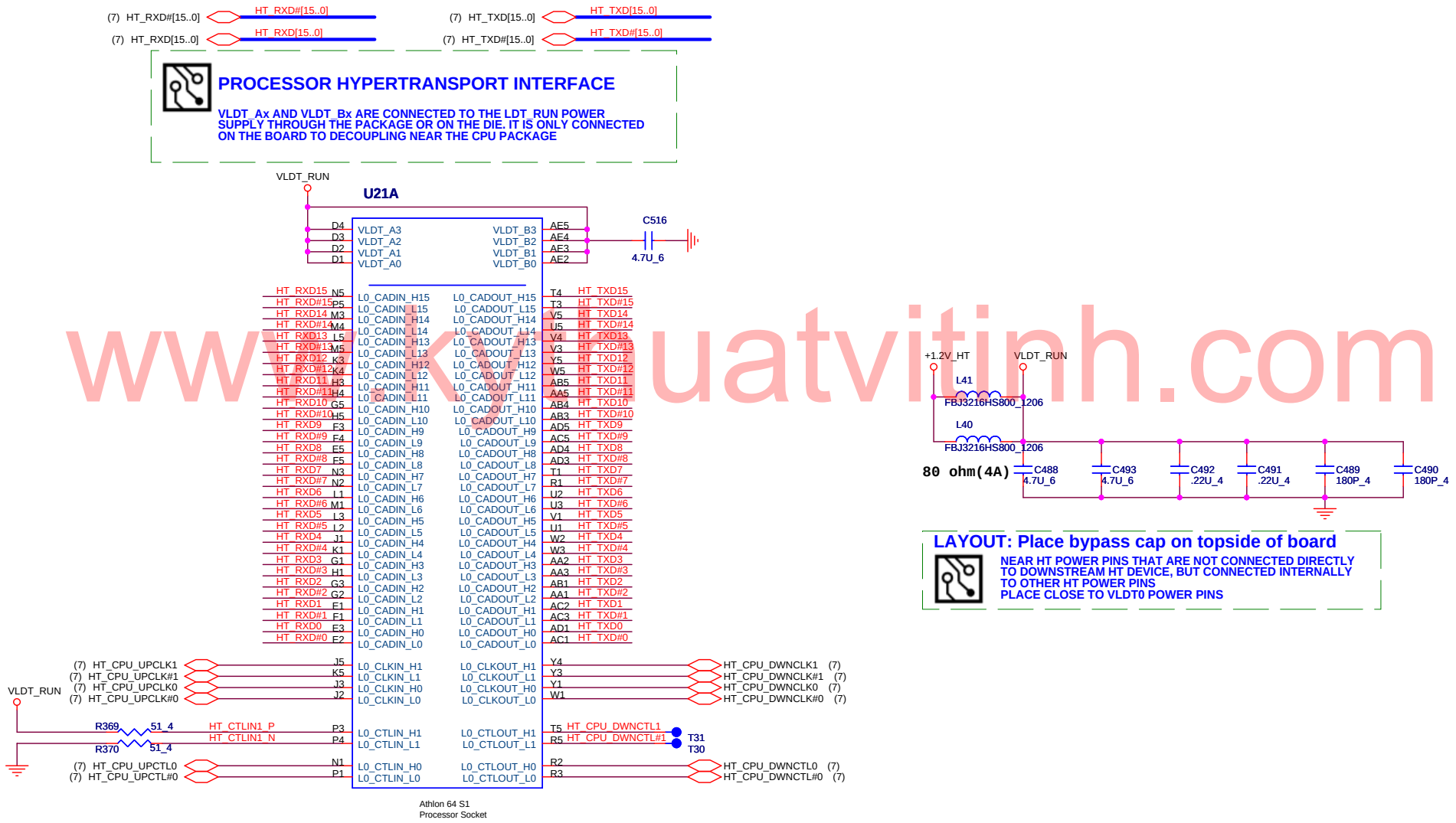
ZO3 SYSTEM BLOCK DIAGRAM



PROJECT : ZO3
Quanta Computer Inc.
Size: Document Number: Block Diagram Rev: 1A
Date: Wednesday, April 25, 2007 Sheet 1 of 30



PROJECT : ZO3
Quanta Computer Inc.

Size	Document Number	Rev
	ATHLON64 HT I/F	1A
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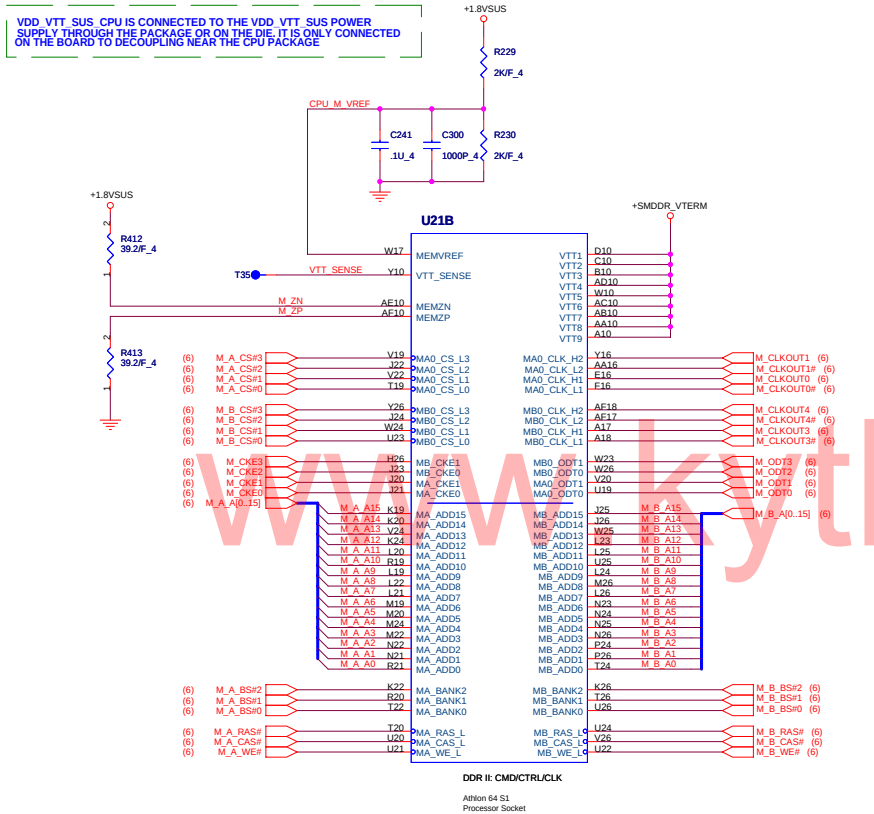
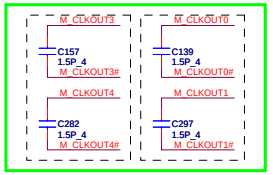
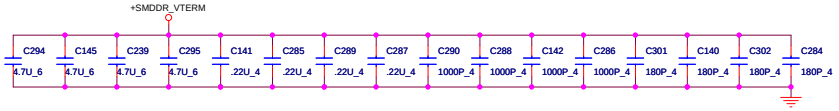
Processor DDR2 Memory Interface

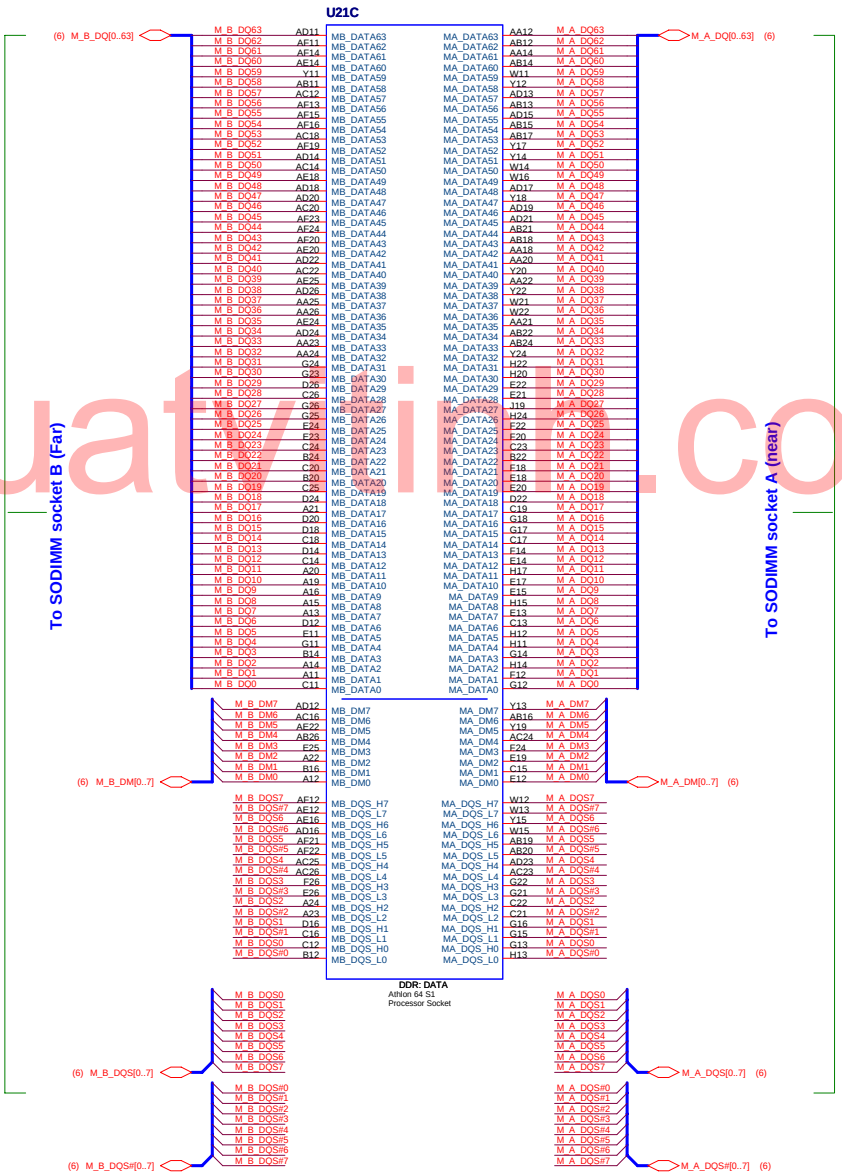
VDD_VTT_SUS_CPU IS CONNECTED TO THE VDD_VTT_SUS POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE



Near CPU L<1200mil







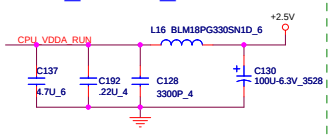
PROJECT : ZO3
Quanta Computer Inc.

Size	Document Number	Rev
	ATHLON64 DDRII MEMORY I/F	1A
Date: Wednesday, April 25, 2007	Sheet 3 of 30	

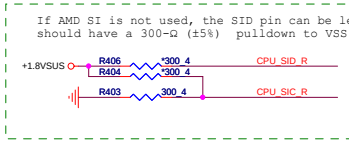
ATHLON Control and Debug

LAYOUT: ROUTE VDDA TRACE APPROX. 50 mils WIDE (USE 2x25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.

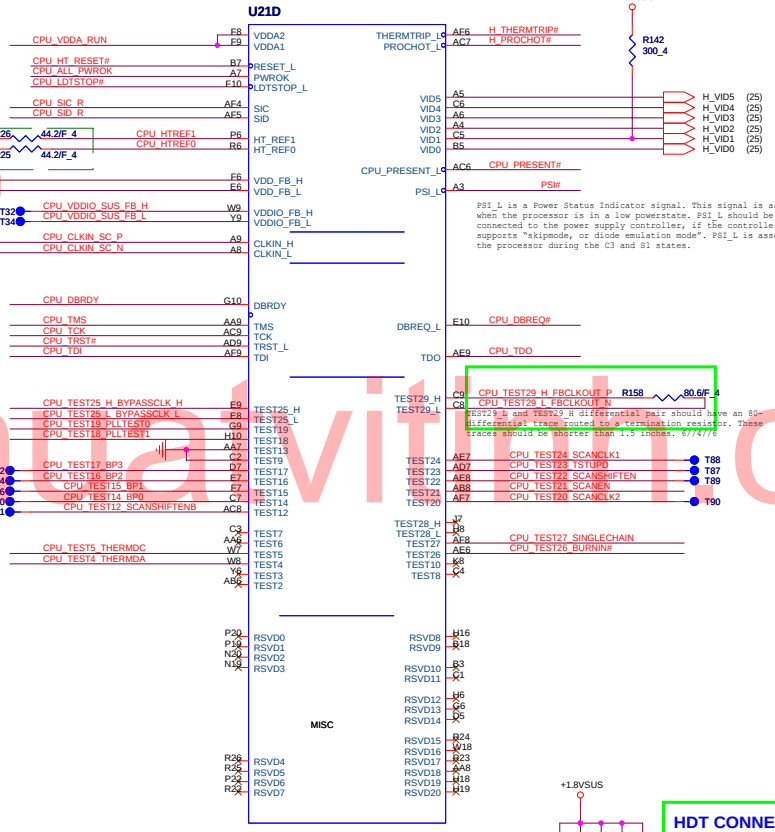
CPU_VDDA_RUN



If AMD SI is not used, the SID pin can be left unconnected and SIC should have a 300-Ω (±5%) pulldown to VSS.



U21D

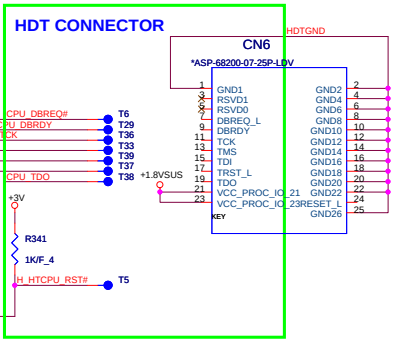


AMD NPT S1 SOCKET
Processor Socket

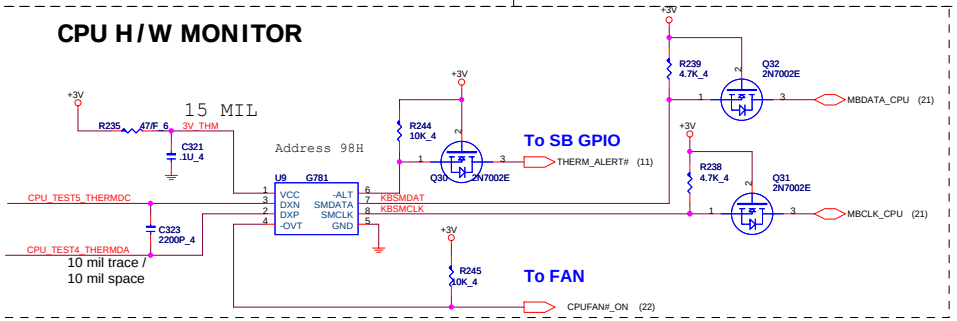
PSI_L is a Power Status Indicator signal. This signal is asserted when the processor is in a low powerstate. PSI_L should be connected to the power supply controller, if the controller supports "skipmode, or diode emulation mode". PSI_L is asserted by the processor during the C3 and S1 states.

TEST29_H and TEST29_L differential pair should have an 80-ohm differential trace routed to a termination resistor. These traces should be shorter than 1.5 inches. 6/4/06

HDT CONNECTOR



CPU H/W MONITOR



PROJECT : ZO3			
Quanta Computer Inc.			
Size	Document Number		Rev
	ATHLON64 CTRL & DEBUG		2A
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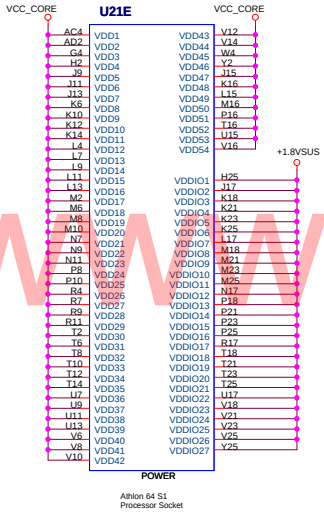
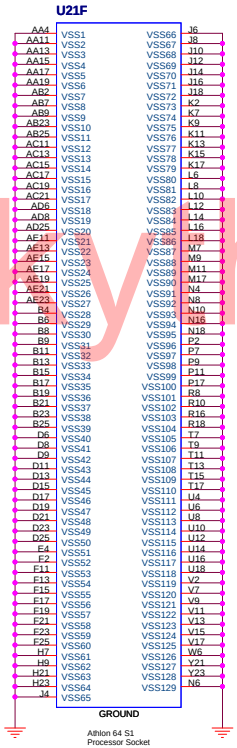
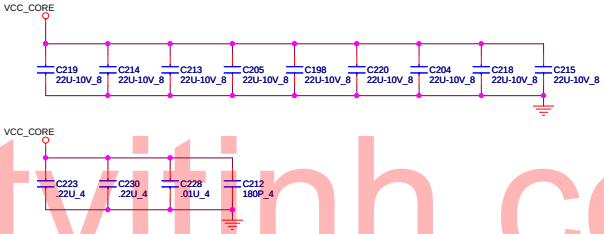
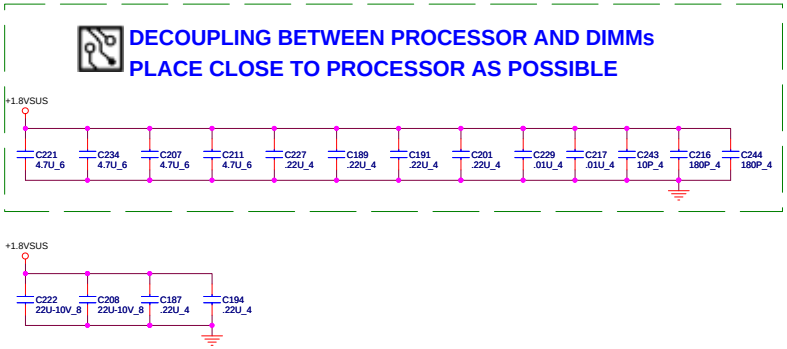
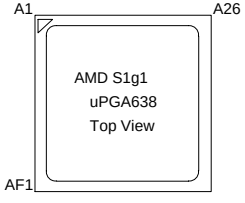
PROCESSOR POWER AND GROUND











PROJECT : ZO3
Quanta Computer Inc.

Size	Document Number	Rev
	ATHLON64 PWR & GND	1A

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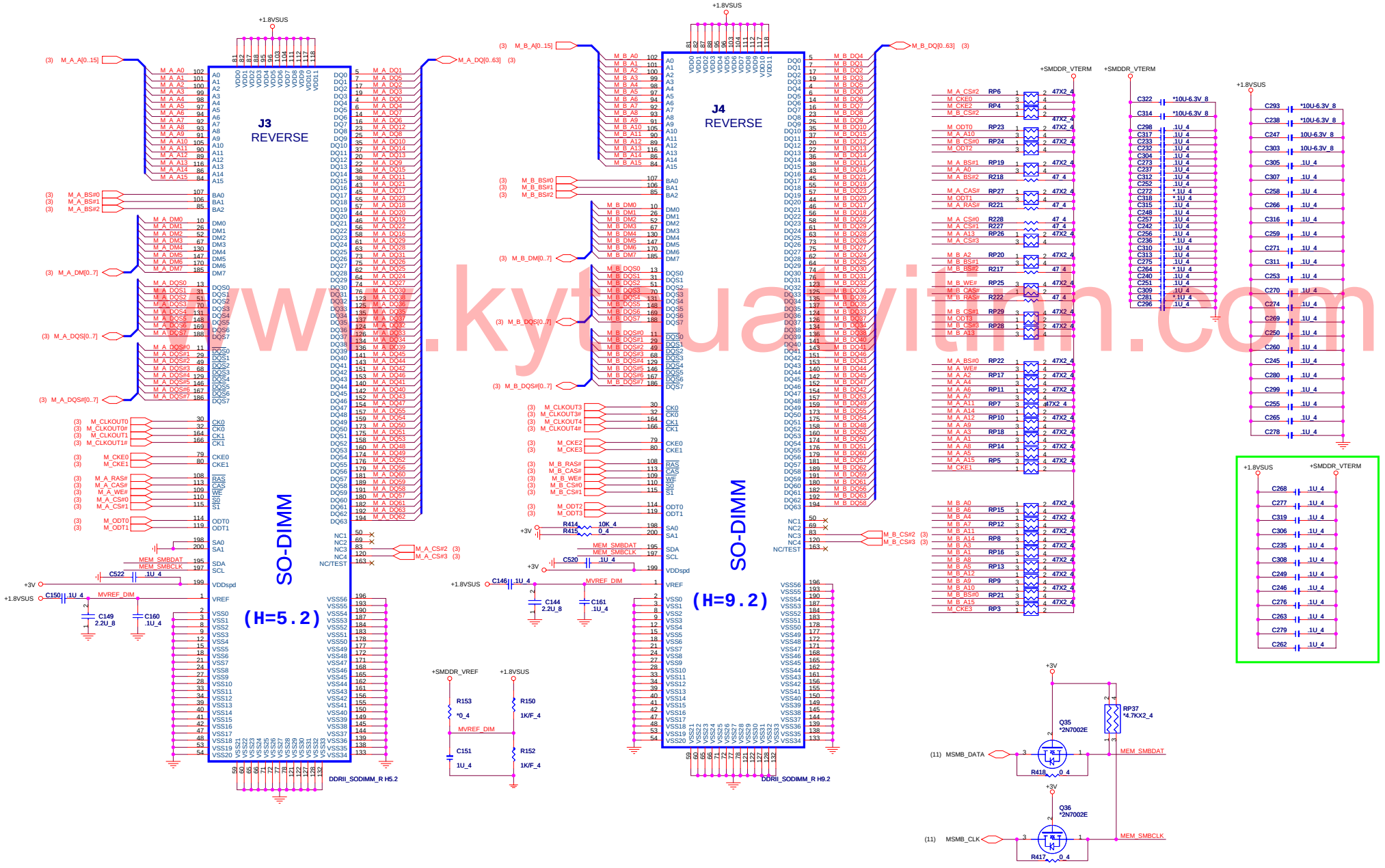

PROJECT : ZO3		
Quanta Computer Inc.		
Size	Document Number: DDR-II SODIMM*2	Rev: 1A
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A1:AJMCP670T00
A2:AJMCP670T04

MCP67 Used UMA Only	
MCP67 Signal Name	Component
RGB_DAC_RSET	STUFF
RGB_DAC_VREF	STUFF
DDC_DATA0	*10K LEAVE NC
TV_DAC_RSET	STUFF
TV_DAC_VREF	STUFF
IFPAB_RST	STUFF
IFPAB_VPROBE	STUFF
DDC_DATA2	*10K LEAVE NC
HPLUG_DET3	22K PULLDOWN
HDMI_RSET	STUFF
HDMI_VPROBE	STUFF
DDC_DATA3_R	10K PULLHIGH
HDCP_ROM_SDATA	10K PULLHIGH
HPLUG_DET2_R	6.2K PULLDOWN

MCP67 Unused UMA Only	
MCP67 Signal Name	Component
RGB_DAC_RSET	STUFF
RGB_DAC_VREF	STUFF
DDC_DATA0	10K PULLHIGH
TV_DAC_RSET	STUFF
TV_DAC_VREF	STUFF
IFPAB_RST	STUFF
IFPAB_VPROBE	STUFF
DDC_DATA2	10K PULLHIGH
HPLUG_DET3	22K PULLDOWN
HDMI_RSET	STUFF
HDMI_VPROBE	STUFF
DDC_DATA3_R	10K PULLHIGH
HDCP_ROM_SDATA	10K PULLHIGH
HPLUG_DET2_R	6.2K PULLDOWN

U20A
MCP67 1 OF 7
HT
DACS
FLAT PANEL
[LVDS]
FOR UMA ONLY
UNUSED HDMI ONLY
FOR DVI IS NOT IMPLEMENTED
MCP67

B2B: changed CAP value
C3A: Remove C426,R332 for Nvidia suggest.
C3A: Remove C77,R331 for Nvidia suggest.
B2A: Remove R168,R139
Datasheet error its should be +1.8 plane

PROJECT : ZO3
Quanta Computer Inc.

Size	Document Number	Rev
	MCP67(HT/VGA/FLAT_PANEL)	1A
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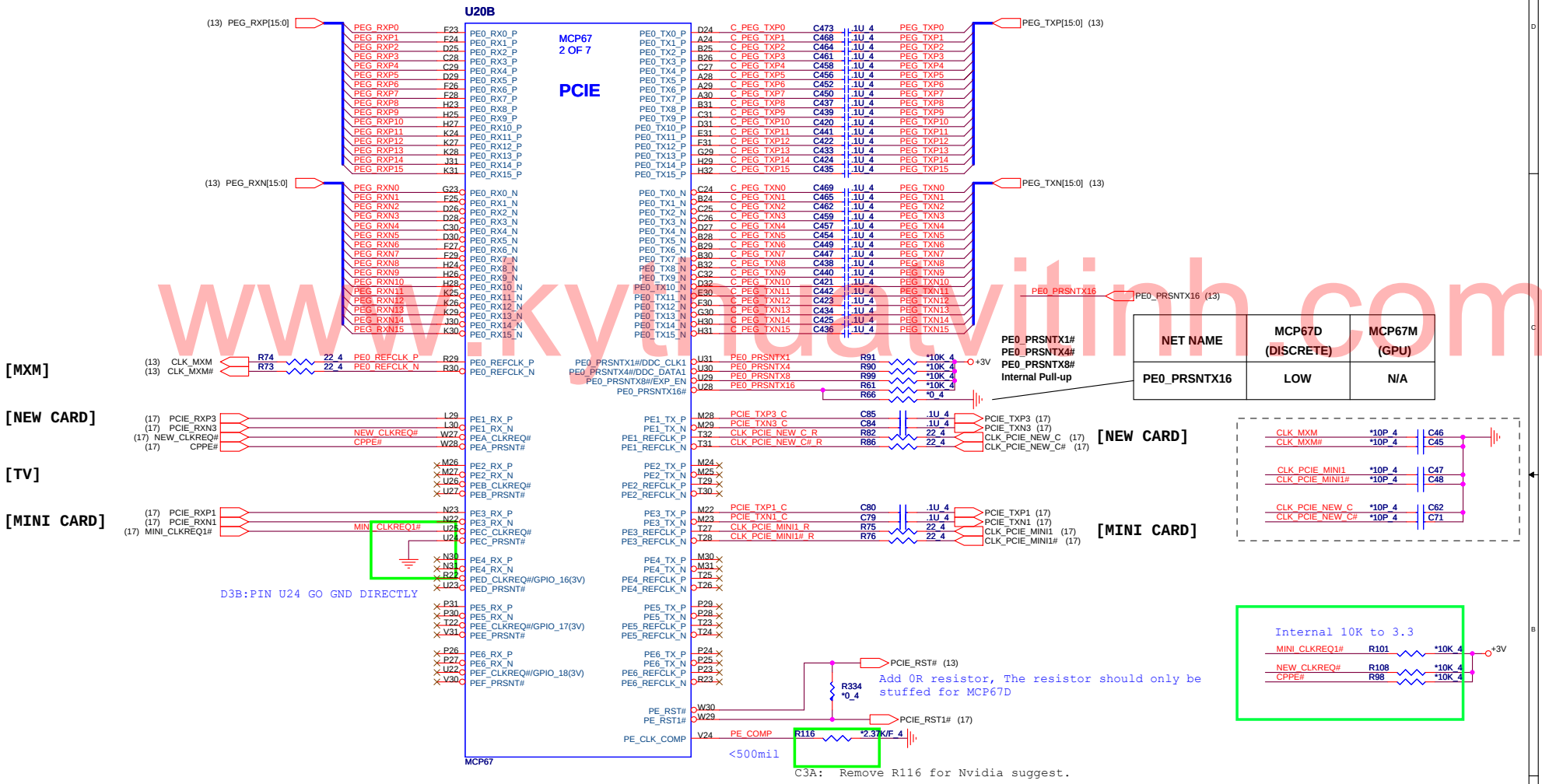

NET NAME	MCP67D (DISCRETE)	MCP67M (GPU)
PE0_PRSNTX16	LOW	N/A

PROJECT : ZO3
Quanta Computer Inc.

Size	Document Number	Rev
	MCP67(PCI-E)	1A

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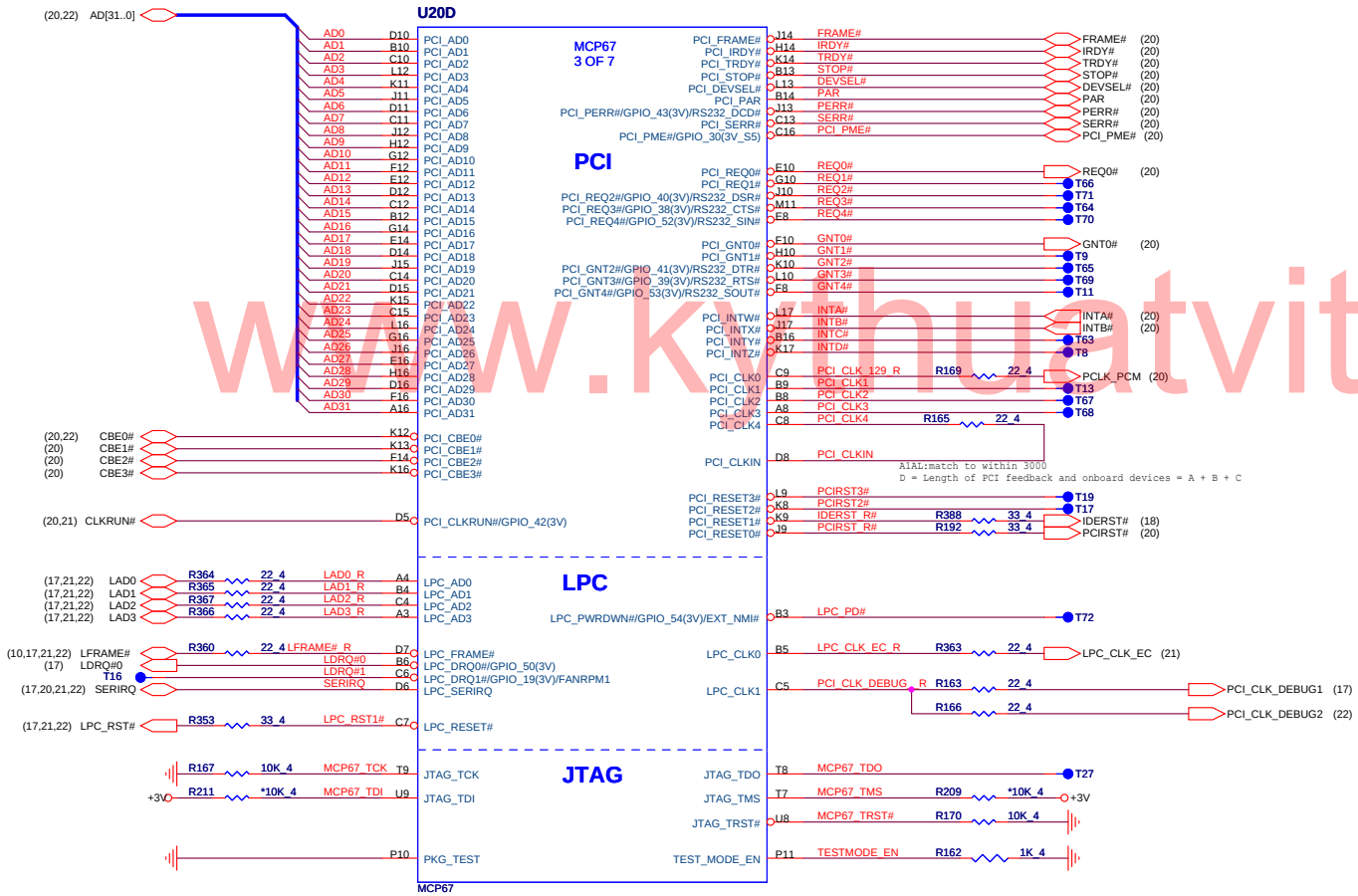
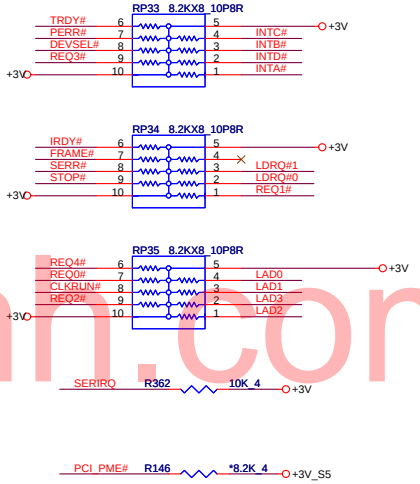
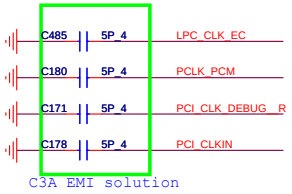


PCI/LPC PULL-UP

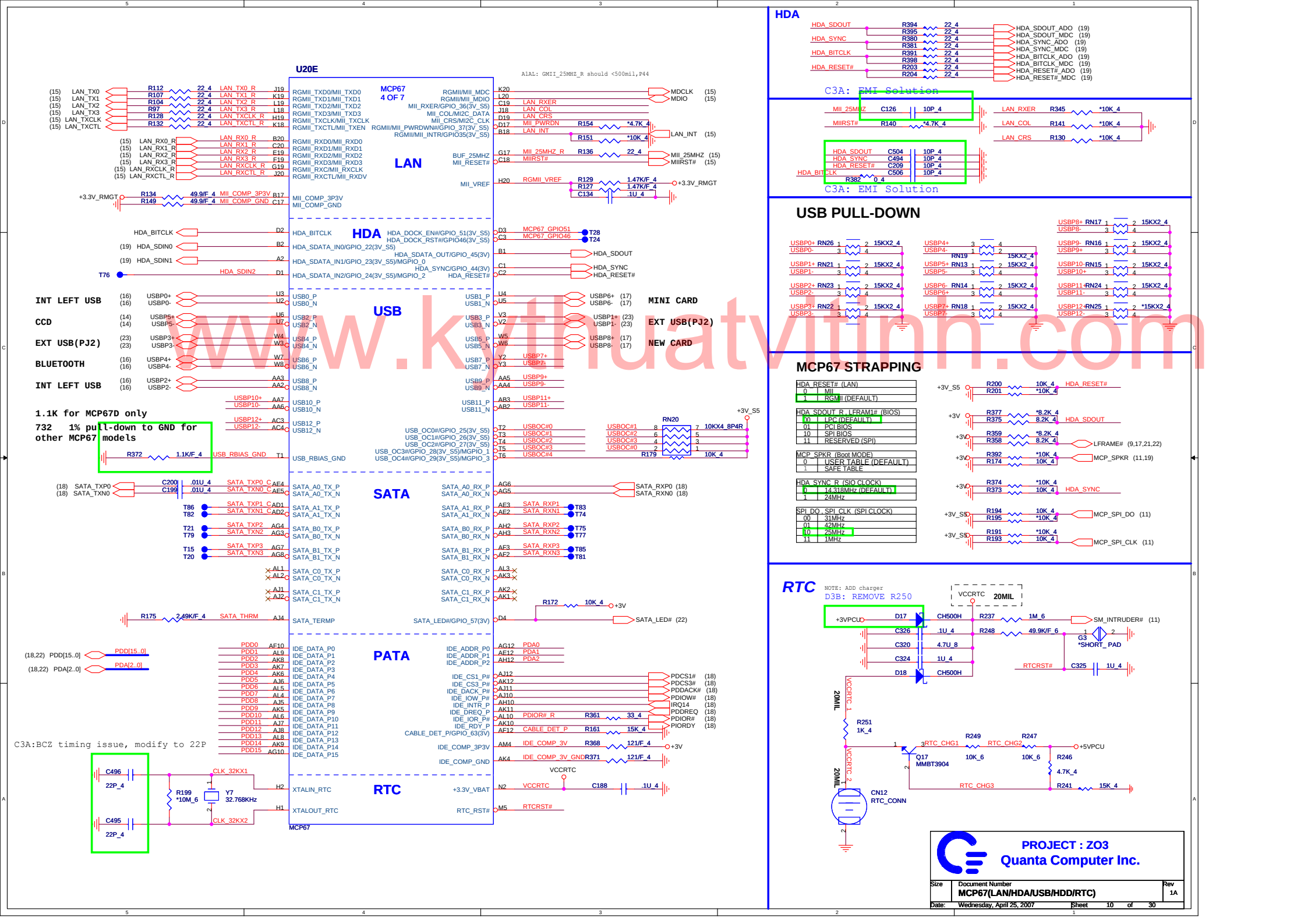


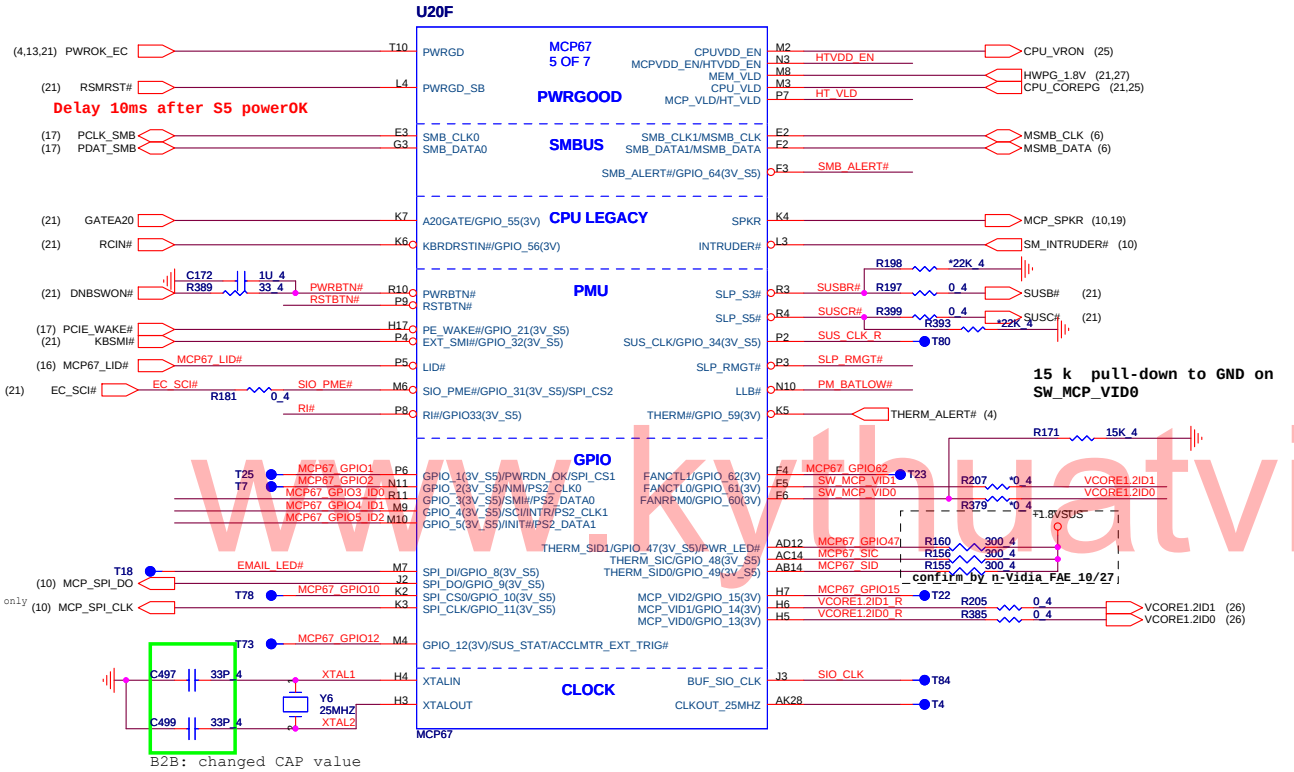
CLOCK BYPASS

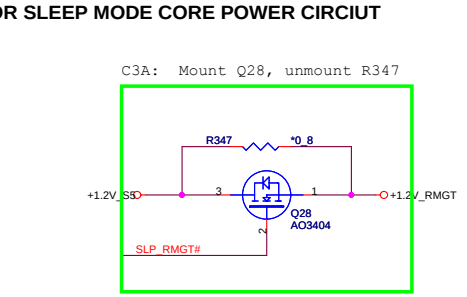


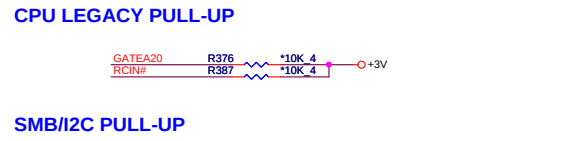
PROJECT : ZO3
Quanta Computer Inc.

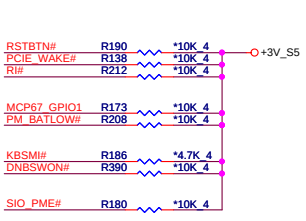
Size	Document Number	Rev
	MCP67(PCI/LPC/JTAG)	1A
Date: Wednesday, April 25, 2007	Sheet 9 of 30	

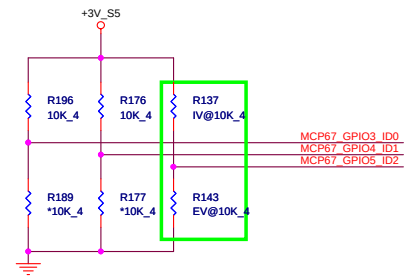


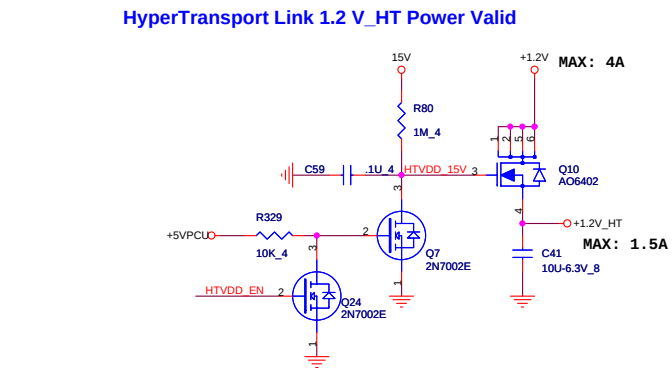


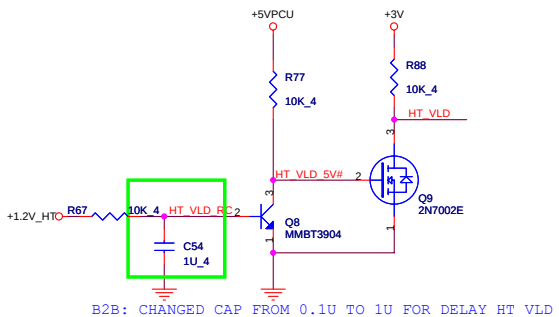












ID0	ID1	ID2	M/B
0	0	0	17" D
0	0	1	X
0	1	0	15" D
1	0	0	15" U
1	0	1	X
1	1	0	14" D
1	1	1	14" U

PROJECT : ZO3
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Size	Document Number	Rev
	MCP67(SMB/GPIO/CLK/PMU)	1A
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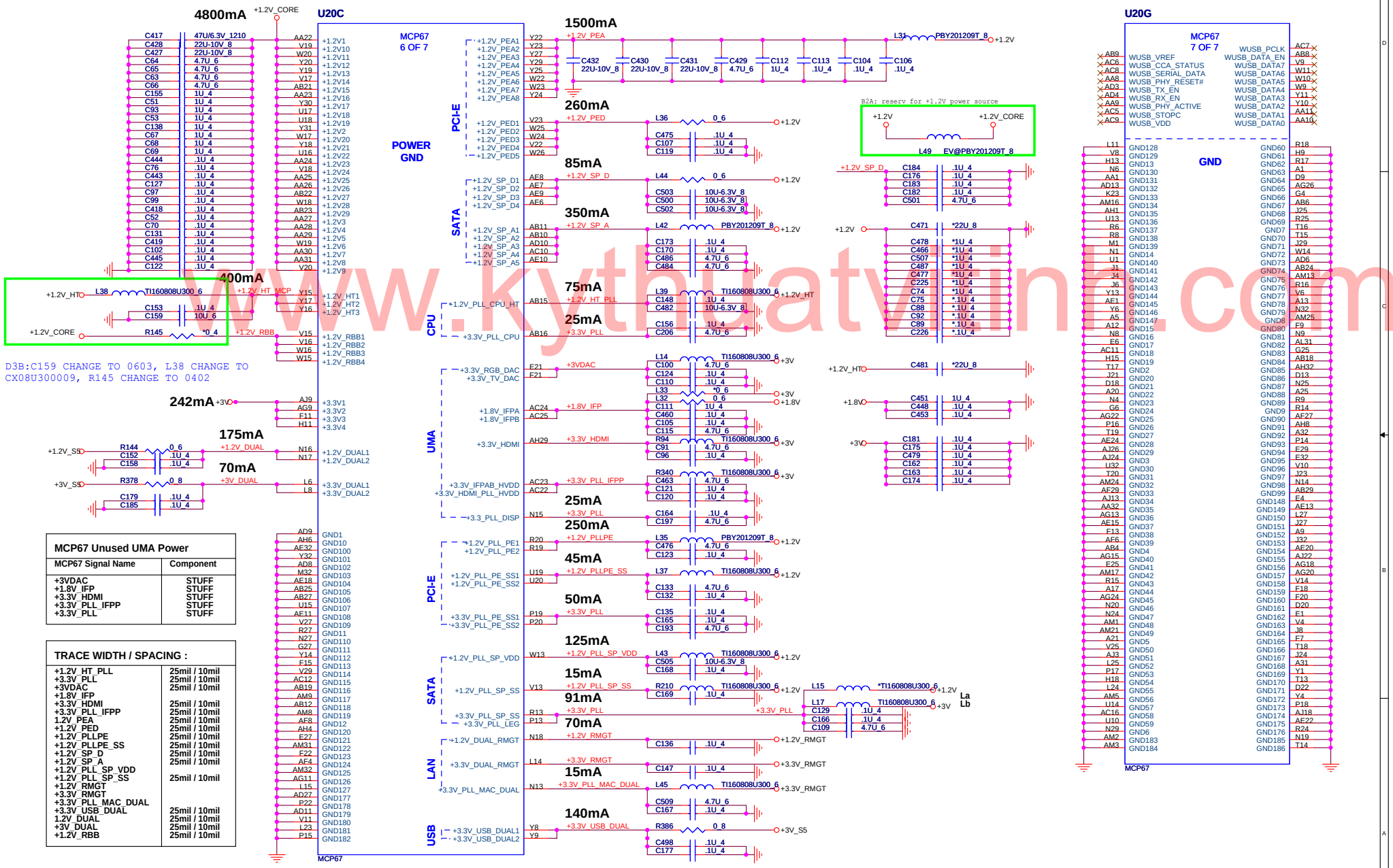
MCP67 POWER PLANE/GND & BYPASS



D3B:C159 CHANGE TO 0603, L38 CHANGE TO CX08U300009, R145 CHANGE TO 0402

MCP67 Unused UMA Power

MCP67 Signal Name	Component
+3VDAC	STUFF
+1.8V_IFP	STUFF
+3.3V_HDMI	STUFF
+3.3V_PLL_IFPP	STUFF
+3.3V_PLL	STUFF

TRACE WIDTH / SPACING :

+1.2V_HT_PLL	25mil / 10mil
+3.3V_PLL	25mil / 10mil
+3VDAC	25mil / 10mil
+1.8V_IFP	
+3.3V_HDMI	25mil / 10mil
+3.3V_PLL_IFPP	25mil / 10mil
1.2V_PEA	25mil / 10mil
+1.2V_PED	25mil / 10mil
+1.2V_PLLPE	25mil / 10mil
+1.2V_PLLPE_SS	25mil / 10mil
+1.2V_SP_D	25mil / 10mil
+1.2V_SP_A	25mil / 10mil
+1.2V_PLL_SP_VDD	
+1.2V_PLL_SP_SS	25mil / 10mil
+1.2V_RMGT	
+3.3V_RMGT	
+3.3V_PLL_MAC_DUAL	
+3.3V_USB_DUAL	25mil / 10mil
1.2V_DUAL	25mil / 10mil
+3V_DUAL	25mil / 10mil
+1.2V_RBB	25mil / 10mil

PROJECT : ZO3
Quanta Computer Inc.

Size	Document Number	Rev
	MCP67(POWER/GND)	1A

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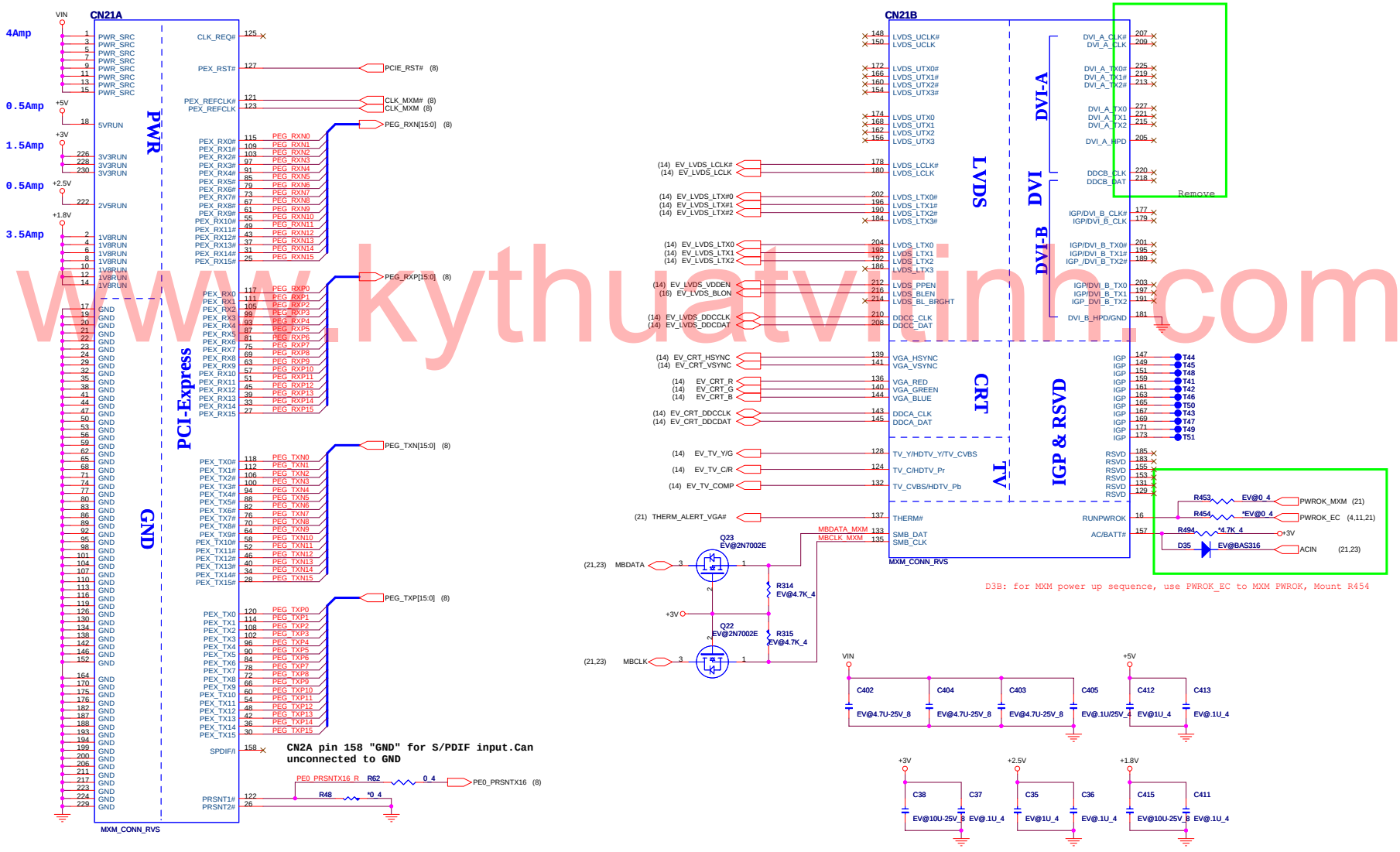


LVDS

SINGLE_CH

Close MXM CONN

(7) INT_TXLCLKOUT-
(7) INT_TXLCLKOUT+
IV@0X2_4
RN9
TXLCLKOUT-
TXLCLKOUT+

(7) INT_TXLOUT0-
(7) INT_TXLOUT0+
IV@0X2_4
RN12
TXLOUT0-
TXLOUT0+

(7) INT_TXLOUT1-
(7) INT_TXLOUT1+
IV@0X2_4
RN11
TXLOUT1-
TXLOUT1+

(7) INT_TXLOUT2-
(7) INT_TXLOUT2+
IV@0X2_4
RN10
TXLOUT2-
TXLOUT2+

(13) EV_LVDS_LCLK#
(13) EV_LVDS_LCLK
EV@0X2_4
RN4

(13) EV_LVDS_LTX#0
(13) EV_LVDS_LTX0
EV@0X2_4
RN7

(13) EV_LVDS_LTX#1
(13) EV_LVDS_LTX1
EV@0X2_4
RN6

(13) EV_LVDS_LTX#2
(13) EV_LVDS_LTX2
EV@0X2_4
RN5

Edison-- 1025 Modify the LVDS pin difinition

CN4
CON30X2_0

TXLOUT0+
TXLOUT0-
TXLOUT1+
TXLOUT1-
TXLOUT2+
TXLOUT2-
TXLCLKOUT+
TXLCLKOUT-
(10) USBP5-
(10) USBP5+

LCD_EDIDCLK
LCD_EDIDDATA
VIN_LCD
BL_ON
BRIGHTNESS
C23 .1U_4
+3V
LCD_VCC
CCD_PWR

BRIGHTNESS
R18 *0_6
R19 0_6
L_BKLT_CTRL (7)
EC_L_BKLT_CTRL (21)

VIN
R20 0_8
VIN_LCD
4.7U-25V_8 C21
C18 1000P-25V_4

+3V
R321 2.2K_4
(13) EV_LVDS_DDCCLK
R322 EV@0_4
LCD_EDIDCLK
(7) INT_LVDS_EDIDCLK
R326 IV@0_4

+3V
R324 2.2K_4
(13) EV_LVDS_DDCDAT
R323 EV@0_4
LCD_EDIDDATA
(7) INT_LVDS_EDIDDATA
R327 IV@0_4

LCD POWER

+3V
C24 1U_4
U4
AAT4280
IN
IN
ON/OFF
OUT
GND
GND
LCDVCC_1
R21 0_8
C26 .1U_4
C25 10U-6.3V_8
C27 .1U_4
C20 .01U_4
C22 10U-6.3V_8
LCD_VCC

Close to CONN CN3

(7) INT_LVDS_DIGON
R16 IV@0_4
DISP_ON
(13) EV_LVDS_VDDEN
R15 EV@0_4

<demo circuit>
Crestline suggest 100K
G73 suggest 10K(ZS1 Default)

Unstuff R275 for EV_LVDS_VDDEN signal

R17 IV@10K_4

CAMERA MODULE POWER

+3V
CCD_PWR
R497 0_8
Q4 *AO3413
C17 10U-6.3V_8
C19 1000P_4
+3V
R14 *4.7K_4
Q3 *DTC144EU
CCD_POWERON (21)

BECAUSE UR'S SUGGESTION,
ACTICE CHANGE FROM LOW TO HIGH.
Confirm by Joms

B2A: unstuff Q4, mount R497 for saving Q4

CRT

Close MXM CONN

(13) EV_CRT_R
(13) EV_CRT_G
(13) EV_CRT_B
(13) EV_CRT_HSYNC
(13) EV_CRT_VSYNC
(13) EV_CRT_DDCCLK
(13) EV_CRT_DDCDAT
R42 EV@0_4
R43 EV@0_4
R44 EV@0_4
R36 EV@0_4
R38 EV@0_4
R34 EV@0_4
R35 EV@0_4
SYS_VGA_RED
SYS_VGA_GRN
SYS_VGA_BLU
HSYNC
VSYNC
CRTDCLK
CRTDDAT

(7) INT_CRT_RED
(7) INT_CRT_GRN
(7) INT_CRT_BLU
(7) INT_HSYNC
(7) INT_VSYNC
(7) INT_CRT_DDCCLK
(7) INT_CRT_DDCDAT
R45 IV@0_4
R46 IV@0_4
R47 IV@0_4
R37 IV@0_4
R39 IV@0_4
R40 IV@0_4
R41 IV@0_4

+5V
D3 1N5819HW
CRTVDD5
R13 150/F_4
R12 150/F_4
R10 150/F_4
C14 10P_4
C11 10P_4
C9 10P_4
C8 10P_4
C10 10P_4
C15 10P_4
L7 BK1608LL680_6
L6 BK1608LL680_6
L5 BK1608LL680_6
CRT_R1
CRT_G1
CRT_B1

CN18
CRT_CONN
DDCDAT_1
CRTHSYNC
CRTVSYNC
DDCCLK_1

C3A: Add C9,C11,C14 for EMI solution

R3 0_4
CRT_SENSE# (21)

CRTVDD5 .1U_4 C5
CRTVSYNC *10P_4 C6
CRTHSYNC *10P_4 C7
DDCCLK_1 10P_4 C3
DDCDAT_1 10P_4 C12

+5V
C4 1U_4
C13 .22U_6
+3V
C16 1U_4
U3
CM2009
VCC_SYNC
SYNC_OUT2
SYNC_OUT1
VCC_DDC
BYP
VCC_VIDEO
SYNC_IN2
SYNC_IN1
VIDEO_1
VIDEO_2
VIDEO_3
GND
DDC_IN1
DDC_IN2
DDC_OUT1
DDC_OUT2
SYS_VGA_RED
SYS_VGA_GRN
SYS_VGA_BLU
VSYNC1
HSYNC1
L3 BLM18BA220SN1_6
L4 BLM18BA220SN1_6
CRTVSYNC
CRTHSYNC
VSYNC
HSYNC
CRTDCLK
CRTDDAT
R9 2.7K_4
R8 2.7K_4
DDCCLK_1
DDCDAT_1
CRTVDD5
R11 2.7K_4
R7 2.7K_4

TV Out (SVHS) MiniDIN 7-pin

(13) EV_TV_Y/G
(13) EV_TV_C/R
(13) EV_TV_COMP
R50 EV@0_4
R49 EV@0_4
R51 EV@0_4
SYS_TV_Y/G
SYS_TV_C/R
SYS_TV_COMP

(7) INT_TV_Y/G
(7) INT_TV_C/R
(7) INT_TV_COMP
R53 IV@0_4
R52 IV@0_4
R54 IV@0_4

D3B: Change L8,L9,L10 P/N

CN20
S_VIDEO
SYS_TV_C/R
L10 BK1608LL680_6
TV-CHROMA
R33 150/F_4
C33 6P_4
C34 6P_4
TV-LUMA
L9 BK1608LL680_6
SYS_TV_Y/G
C31 6P_4
C32 6P_4
R32 150/F_4
TV-COMP
L8 BK1608LL680_6
SYS_TV_COMP
C28 6P_4
C29 6P_4
R27 150/F_4

ESD Protect

+3V
D7
TV-COMP
*DA204U
+3V
D9
TV-CHROMA
*DA204U
+3V
D8
TV-LUMA
*DA204U

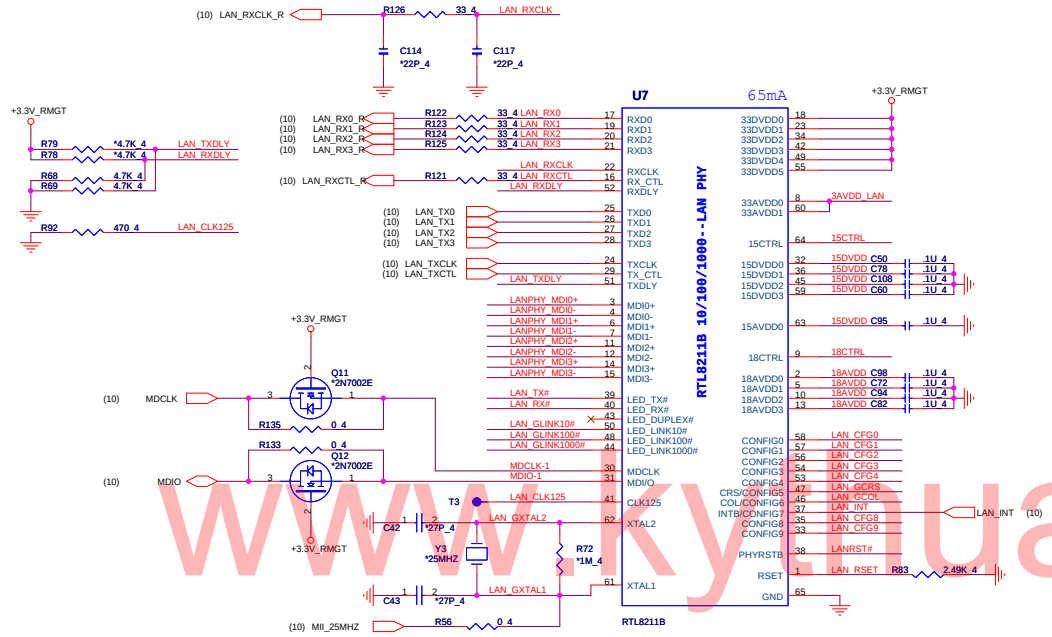
Remove HDMI

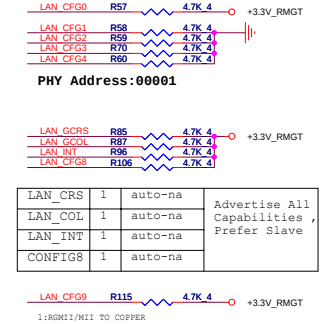
PROJECT : ZO3
Quanta Computer Inc.

Size	Document Number	Rev
	LVDS/CRT/TV-OUT/HDMI	1A

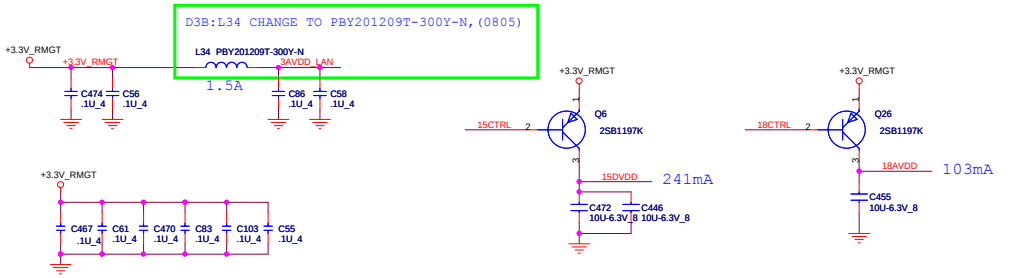
Date: Wednesday, April 25, 2007 Sheet 14 of 30

LAN

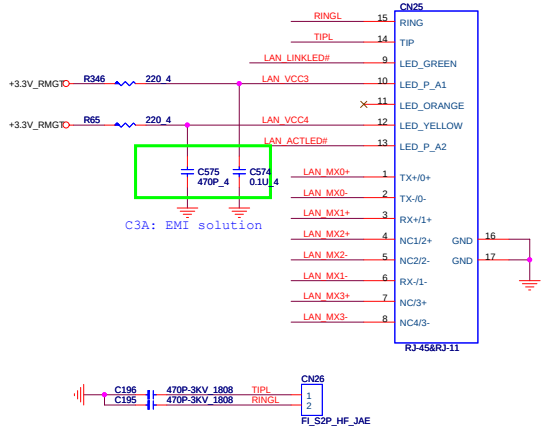




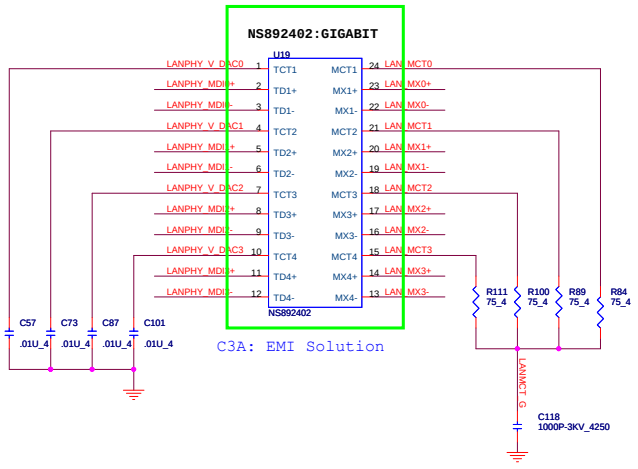
LAN_CRS	1	auto-na	Advertise All Capabilities , Prefer Slave
LAN_COL	1	auto-na	
LAN_INT	1	auto-na	
CONFIG8	1	auto-na	



RJ45-11

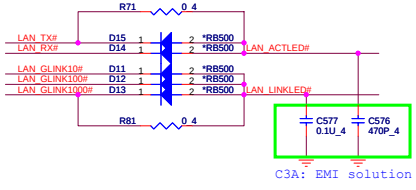


Transformer



LED Configuration

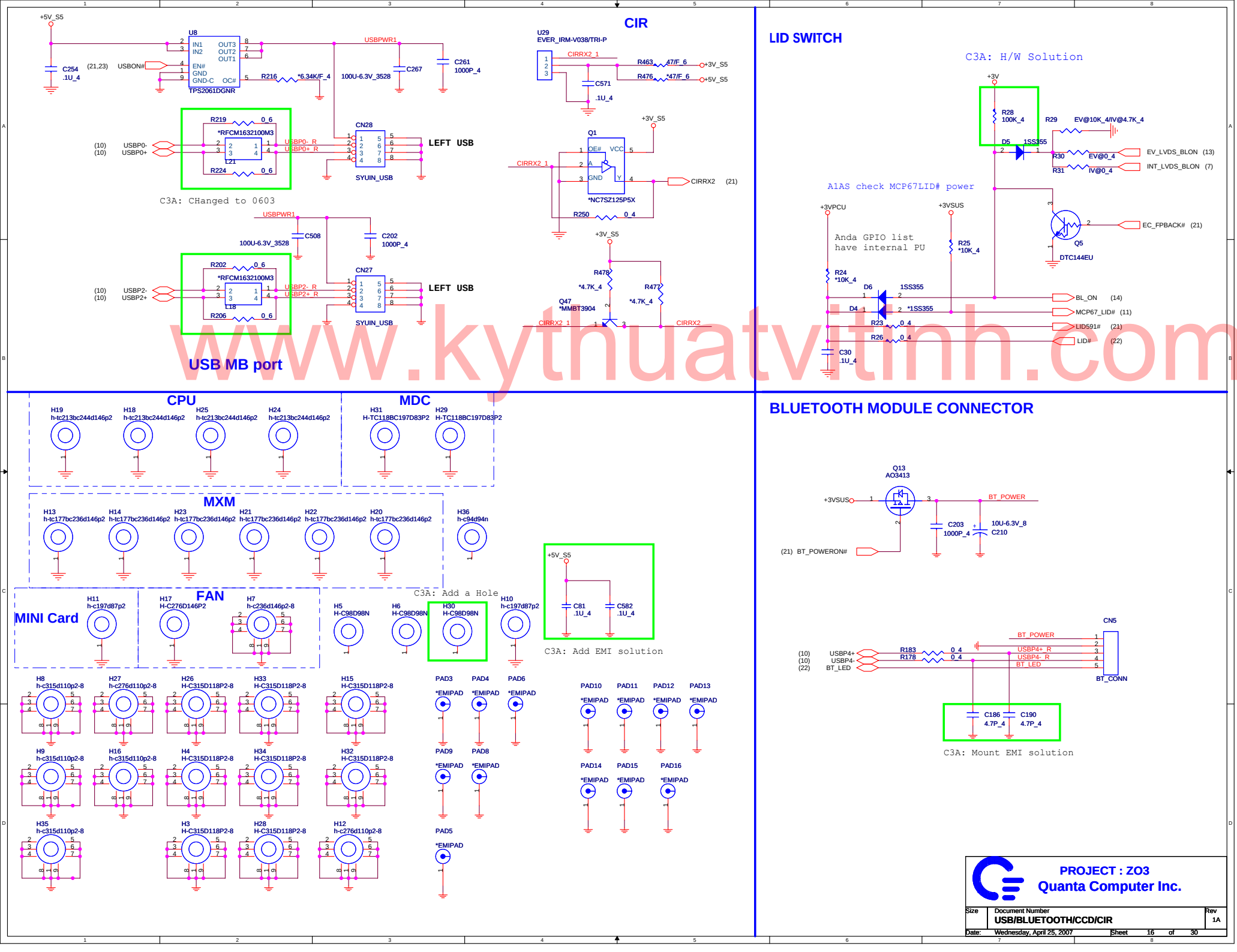
	Set Register 24 Control Bit=1
LED_LINK1000	LOW=LINK UP (ANY SPEED)
LED_TX	BLINKING=TRANSMITTING OR RECEIVING



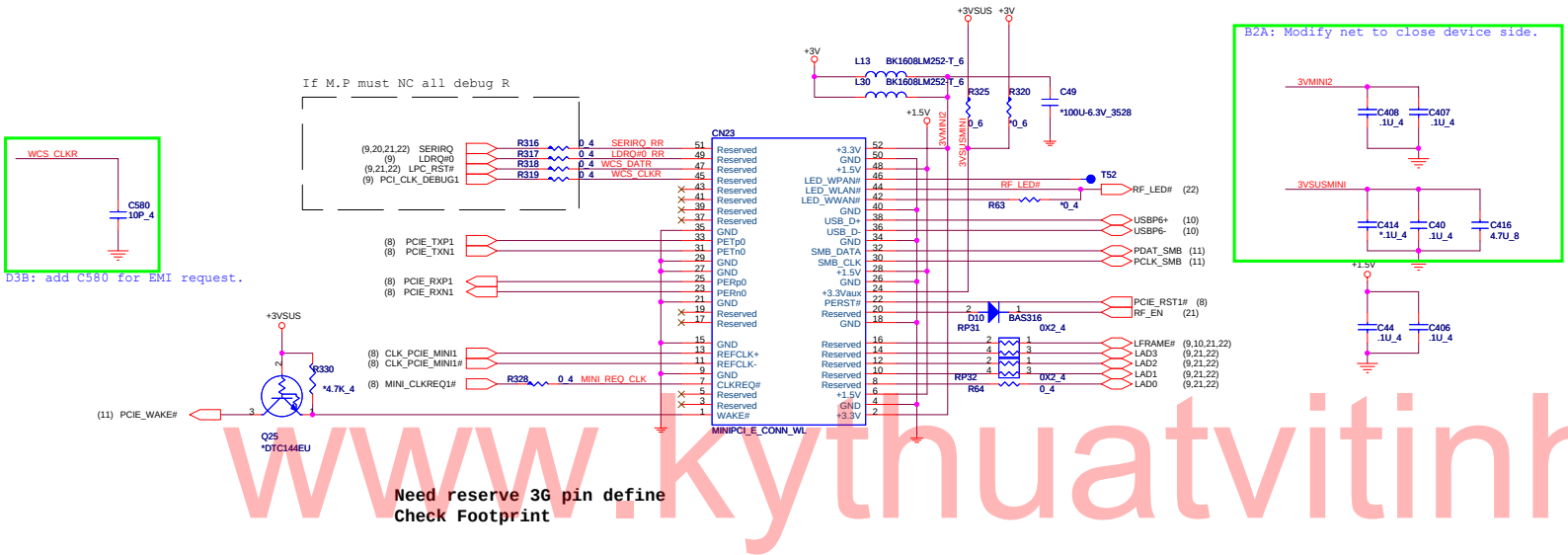
PROJECT : ZO3
Quanta Computer Inc.

Size	Document Number	Rev
	RTL8211B (GigaLAN)	1A

Date: Wednesday, April 25, 2007 Sheet 15 of 30

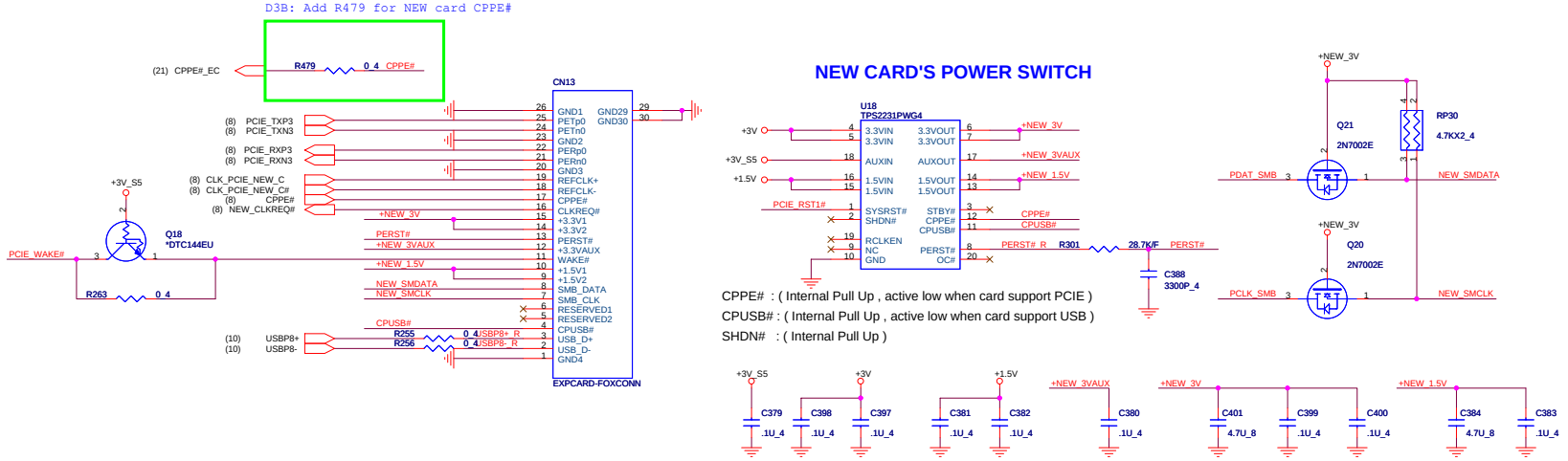


MINI-Card



Need reserve 3G pin define
Check Footprint

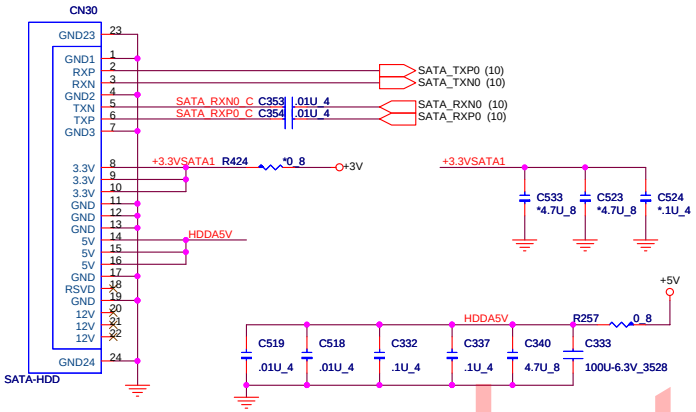
New card



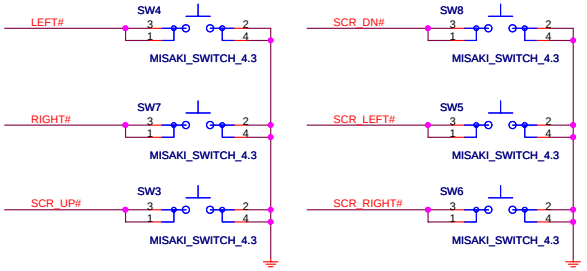
PROJECT : ZO3
Quanta Computer Inc.

Size	Document Number	Rev
	MINI PCI-E card & NEW CARD	1A
Date: Wednesday, April 25, 2007	Sheet 17 of 30	

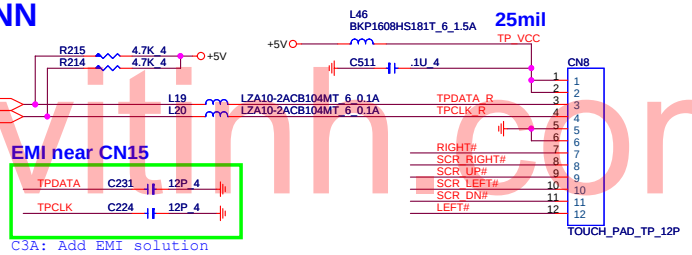
SATA HDD1



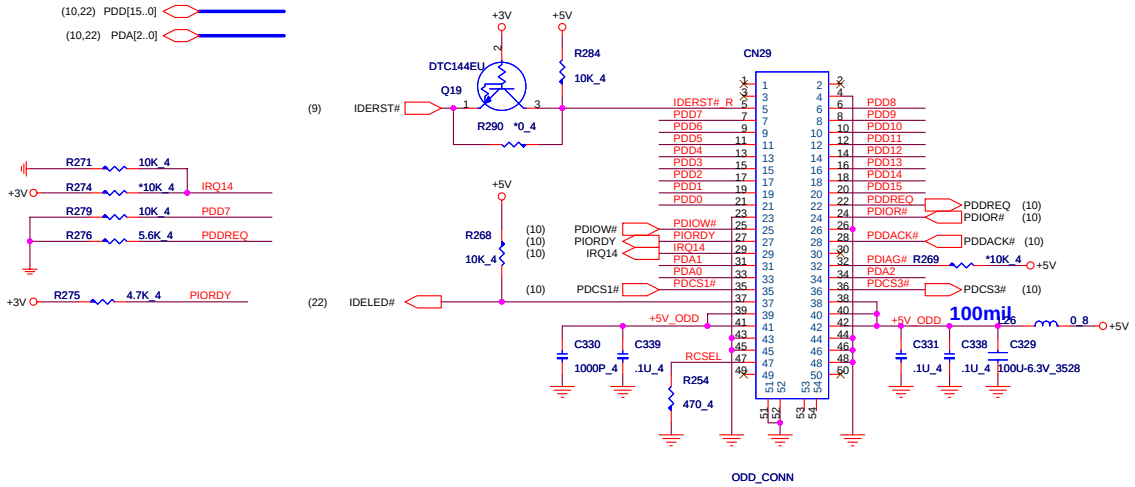
TP SWITCH



TP CONN

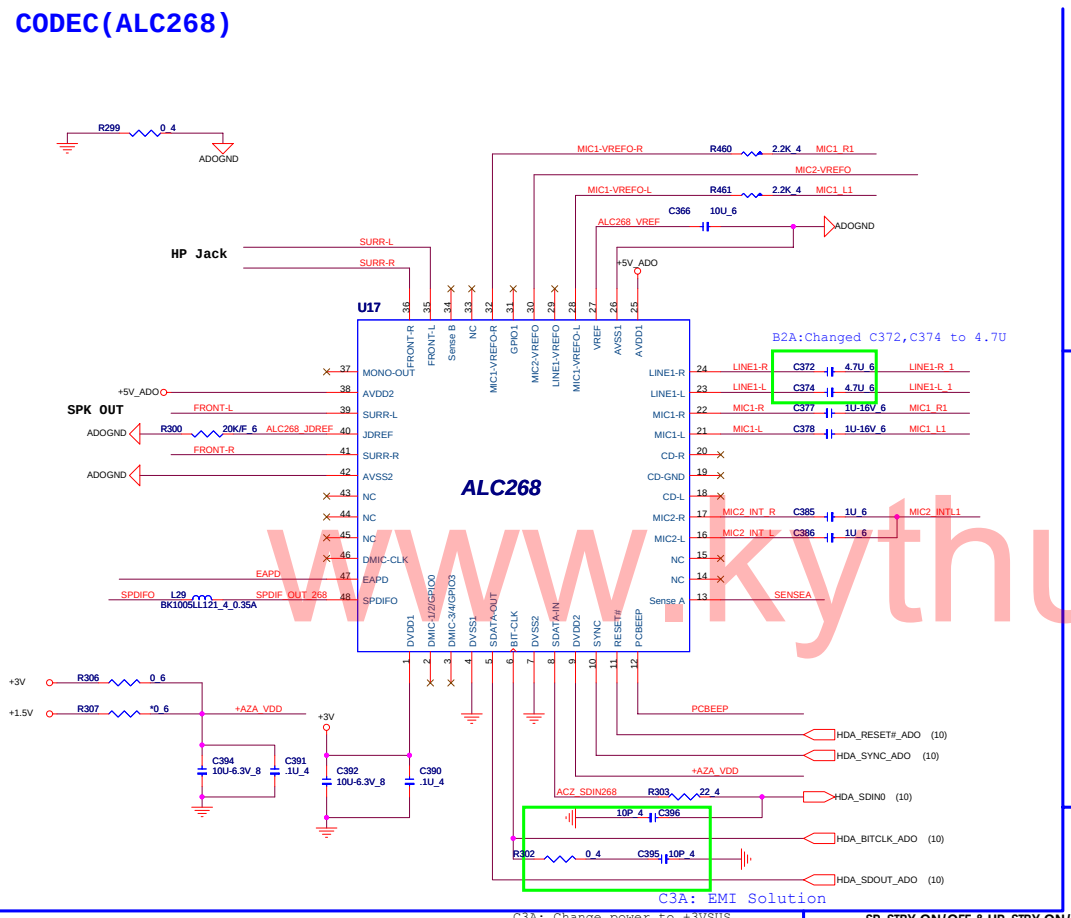


ODD (PATA)

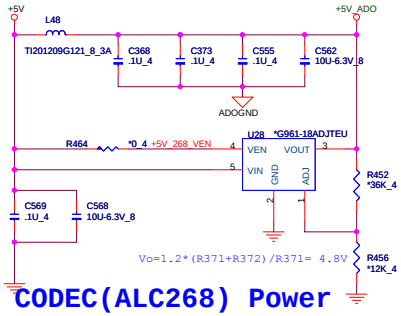


PROJECT : ZO3		
Quanta Computer Inc.		
Size	Document Number: SATA-HDD & PATA-ODD	Rev: 1A
Date: Wednesday, April 25, 2007	Sheet 18 of 30	

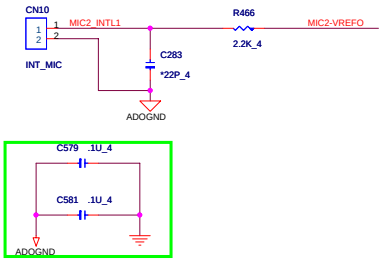
CODEC(ALC268)

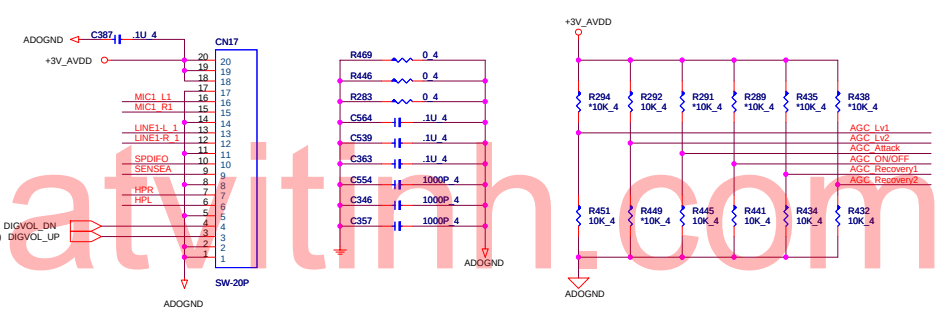


CODEC(ALC268) Power



INT MIC array





AGC-attack-time selection

AGC_Attack (4 pin)	Attack time
LOW	1 ms
Hi	2 ms

AGC ON/OFF selection

AGC_ON/OFF (6 pin)	AGC ON/OFF
LOW	ON
Hi	OFF

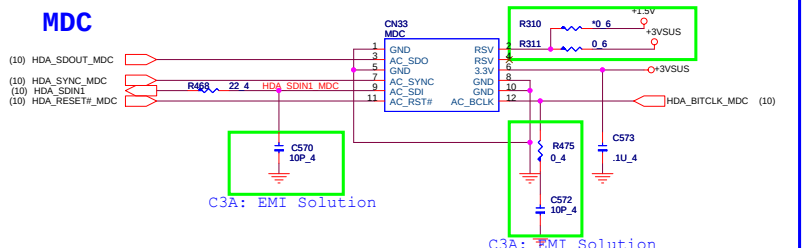
AGC-recovery-time selection

AGC_Recovery1 (10 pin)	AGC_Recovery2 (11 pin)	Recovery Time
LOW	LOW	1.0 s
LOW	Hi	2.0 s
Hi	LOW	4.0 s
Hi	Hi	8.0 s

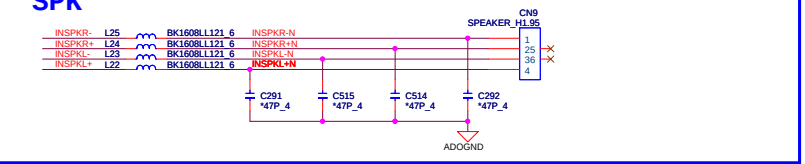
AGC-on-level selection

AGC_Lv1 (2 pin)	AGC_Lv2 (3 pin)	AGC ON Level	Output Po (RL=8 ohm)
LOW	LOW	9.8 dBV	1.2 W
LOW	Hi	9.0 dBV	1.0 W
Hi	LOW	8.1 dBV	0.8 W
Hi	Hi	6.0 dBV	0.5 W

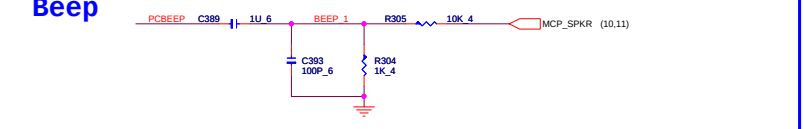
MDC



SPK



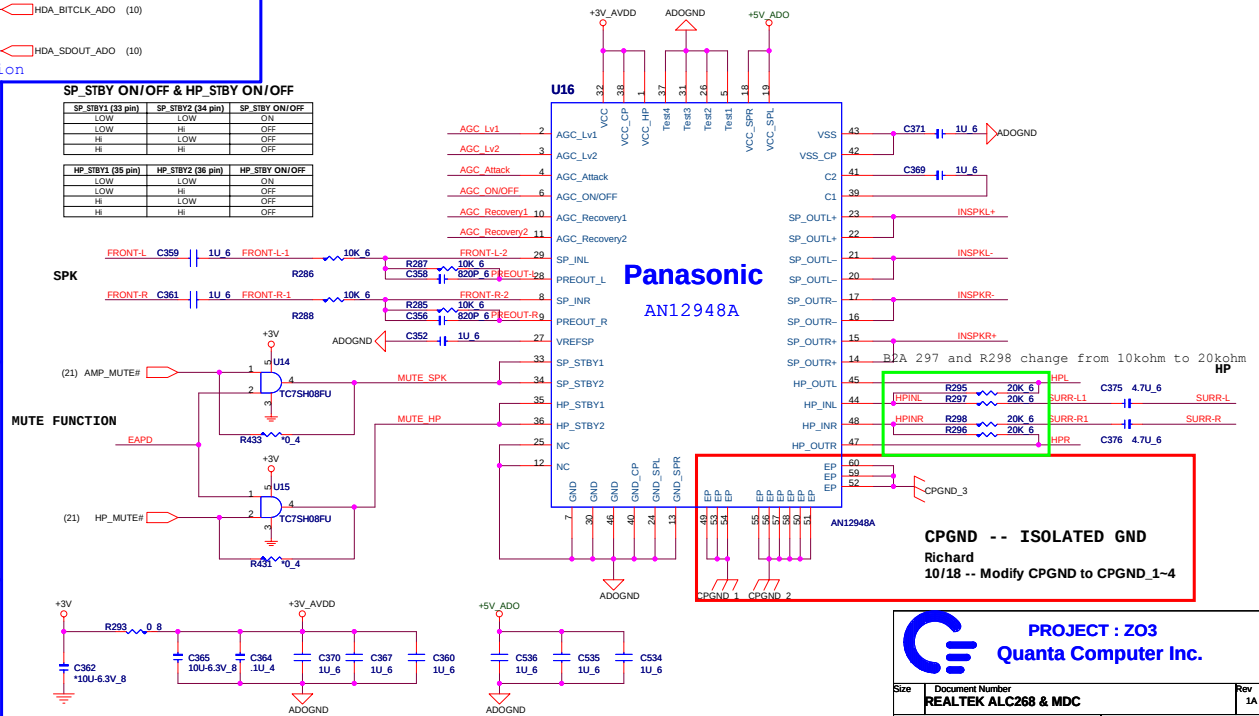
Beep



SP_STBY ON/OFF & HP_STBY ON/OFF

SP_STBY1 (33 pin)	SP_STBY2 (34 pin)	SP_STBY ON/OFF
LOW	LOW	ON
LOW	Hi	OFF
Hi	LOW	OFF
Hi	Hi	OFF

HP_STBY1 (35 pin)	HP_STBY2 (36 pin)	HP_STBY ON/OFF
LOW	LOW	ON
LOW	Hi	OFF
Hi	LOW	OFF
Hi	Hi	OFF



PROJECT : ZO3		
Quanta Computer Inc.		
Size	Document Number	Rev
	REALTEK ALC268 & MDC	1A
Date: Wednesday, April 25, 2007	Sheet 19 of 30	

R5C832 : AJ5C8320H26
R5C833 : AJ5C8330H05

U26B

PCI / OTHER

R5C832T_V00

U26A

IEEE1394/SD

R5C832T_V00

B2B: changed CAP value

AS CLOSE AS POSSIBLE TO R5C833 and GUARD GND

REQ2# AD25
GNT2# INTA#,B#

PowerOnReset for VccCore

When GRESET# is controlled by system, the pull-up resistor(R4066) and capacitor(C4093) do not need to apply.

When HWSPND# is controlled by system, the pull-up resistor(R4059) dose not need to apply.

B2A: pin pull-up can saving the EEPROM, remove R439, stuff R436

C3A: EMI Solution

Close to CONN.

Reduced external noise by FAE confirm

XD_RE#/CLK should shield GND.

> 1 ms >60 ns

VCC

GRST#

PRST#

> 100 ns

HWSPND#

PCLK(33MHz)

5 IN 1 CARD READER

CN31

CARD_READER_TTN_R013-B10-XX-C

CARDREADER POWER

30mil

U25 *G5241T1U

CN32 PROCONN-MXP038-A0-4010-NB4

Reserve MS DUO card issue

1394

AS CLOSE AS POSSIBLE TO R5C833

COMMON MODE CHOKE NEAR CONN.

CN22 1394_CONN

EEPROM

* NOT Use EEPROM :
R4063 : installed
R4064,U38,C4106 : NOT installed
* Use EEPROM :
R4064,U38,C4106 : installed
R4063 : NOT installed

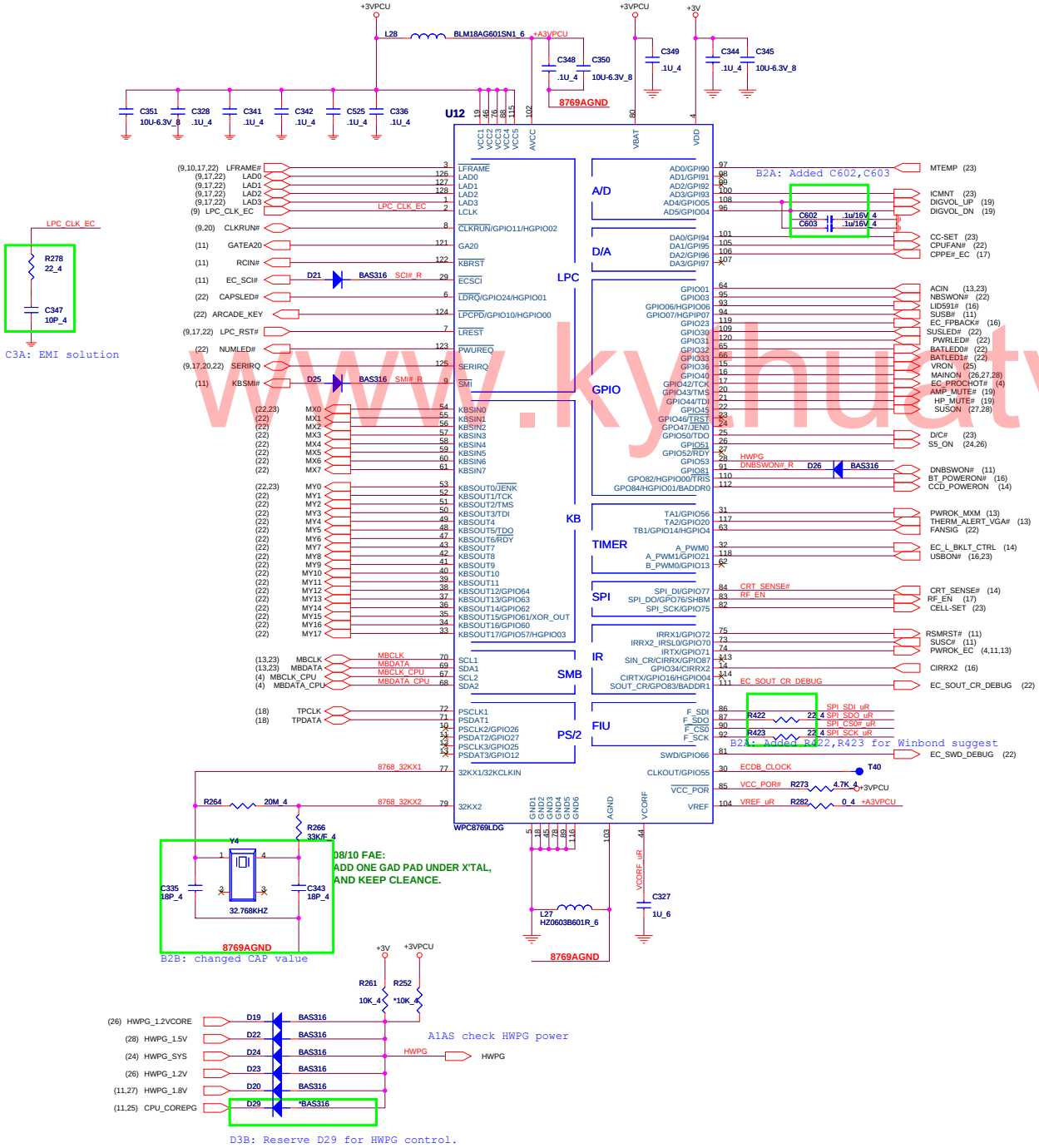
B2A: Remove U27,C594

PROJECT : Z03
Quanta Computer Inc.

Size	Document Number	Rev
	R5C832/833(5IN1/1394)	1A

Date: Wednesday, April 25, 2007 Sheet 20 of 30

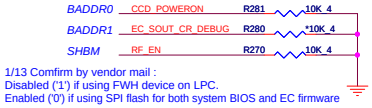
WPC8769LDG



I/O ADDRESS SETTING

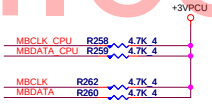
	I/O Address	
BADDR1-0	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS

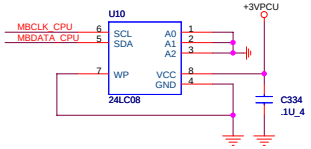


1/13 Comfirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

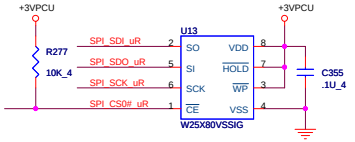
SMBUS PULL-UP



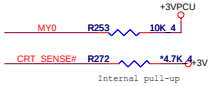
ACER ID



SPI FLASH



INTERNAL KEYBOARD STRIP SET



PROJECT : Z03		
Quanta Computer Inc.		
Size	Document Number	Rev
	PC8769L & FLASH	1A
Date: Wednesday, April 25, 2007	Sheet 21 of 30	

INT K/B

(21,23) MY[17..0]
(21,23) MX[7..0]

CN7
FFC_26P_KB

+3VSUS
RP36
10KX8_10P8R

CA6 *220P-50V_8P4CCA7 *220P-50V_8P4C
CA3 *220P-50V_8P4CCA5 *220P-50V_8P4C
CA4 *220P-50V_8P4CCA8 *220P-50V_8P4C
CA9 *220P-50V_8P4C

LED

10/16:Changed. Follow BL3 LED

+3VPCU
R309 330_4 PWRLED#-R
R308 330_4 SUSLED#-R
LED6 LED_G/Y_LTST-C155KGJSKT
R313 330_4 BATLED0# (21)
R312 330_4 BATLED1# (21)
LED7 LED_G/Y_LTST-C155KGJSKT

(21) CAPSLED# CAPSLED# R5 330_4 +3V
LED5 LED_G_UP

(21) NUMLED# NUMLED# R4 330_4 +3V
LED4 LED_G_UP

IDE_LED# R6 330_4 +3V
LED3 LED_G_UP

Q43 2N7002E
PWRLED#-R
Q44 2N7002E
R455 10K_4 +3V
(21) PWRLED#

Q42 2N7002E
SUSLED#-R
Q46 2N7002E
R462 10K_4 +3VSUS
(21) SUSLED#

C3A: Modify LED control behavior

CPU FAN

+3V
R55 10K_4
(21) FANSIG
CN24
+5V
U6
VIN VO
/FON GND
VSET GND
G995
(4) CPUFAN#_ON
(21) CPUFAN#
TH_FAN_POWER
C410 10U-6.3V
C409 8.01U_4
C39 *.01U_4
FAN_CONN

FANPWR = 1.6*VSET

DEBUG PORT

EC Debug Port
Reserved for LPC debug card

+3VPCU
CN16
(21) EC_SOUT_CR_DEBUG
(21) EC_SWD_DEBUG
*INT_SPK

+3V
CN11
(9,17,21) LAD0
(9,17,21) LAD1
(9,17,21) LAD2
(9,17,21) LAD3
(9) PCI_CLK_DEBUG2
(9,10,17,21) LFRAME#
(9,17,21) LPC_RST#
(9,17,20,21) SERIRQ
*WTB_10P

Button

BUTTON MATRIX

	MY0
MX1	MAIL
MX2	WWW
MX4	WIRELESS
MX5	BLUETOOTH

+3VPCU +3V
CN3
(21) ARCADE_KEY
(17) RF_LED#
(16) BT_LED
(21) NBSWON#
SUSLED#-R
PWRLED#-R
SW-20P

R22 330_4 +3VPCU
LID#
MR3
MRSS23E_NEC
C578 1U_4
D3B: add C578

R267 10K_4
R265 10K_4
(18) IDELED#
(10) SATA_LED#
IDE_LED#
U11
TC7SH08FU

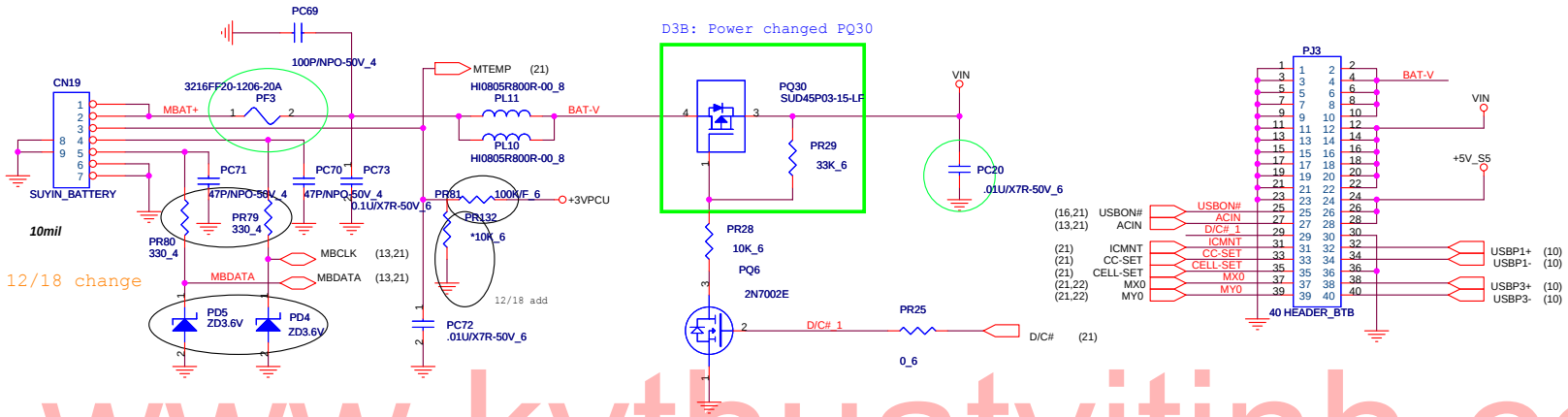
Debug

(9,20) AD[31..0]
(9,20) CBE0#
CN15 *AMP_2-767004-2
R420 0_4

(10,18) PDD[15..0]
(10,18) PDA0
CN14 *AMP_2-767004-2
(16)

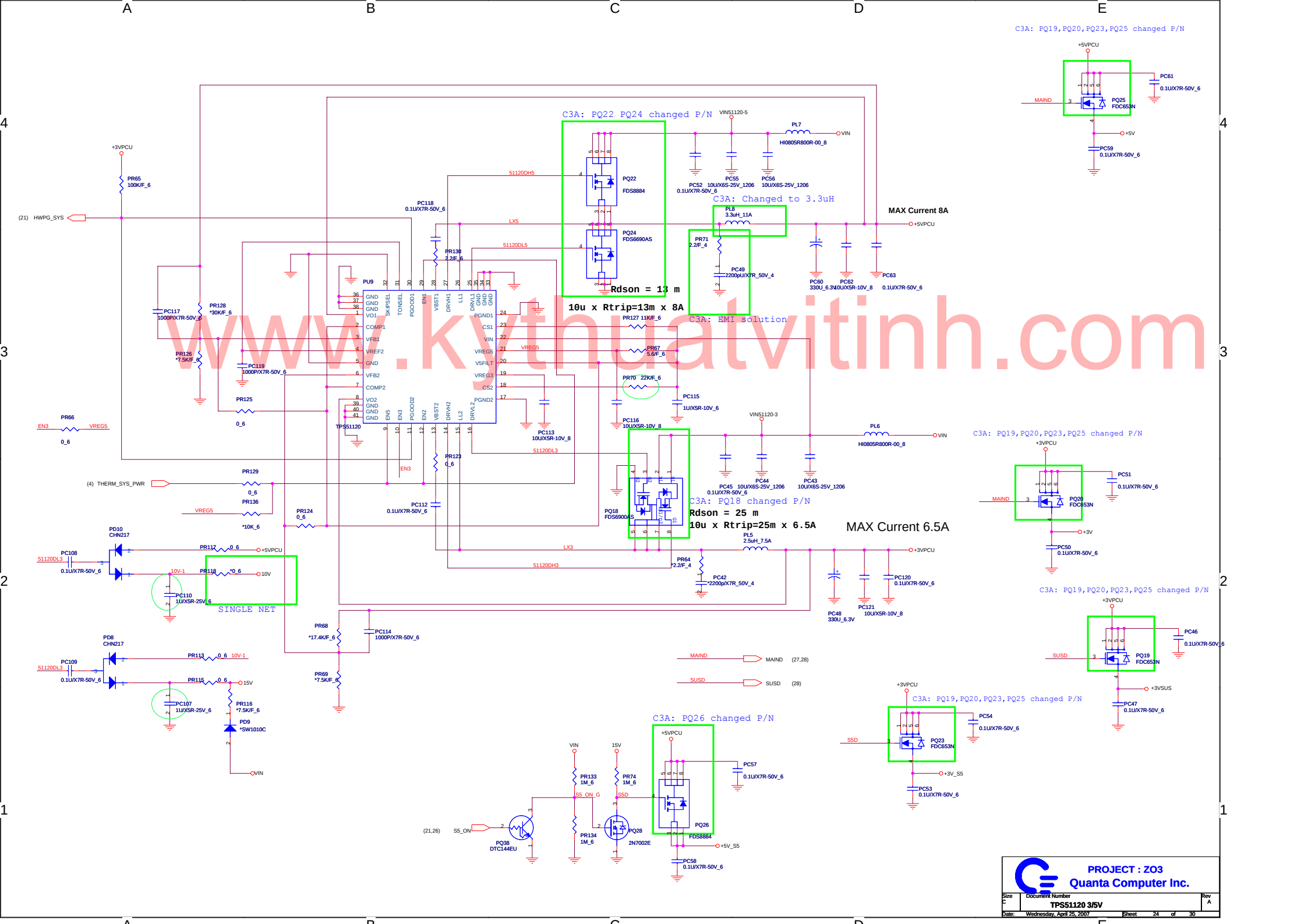
Size	Document Number	Rev
	FAN,SWITCH,LED,KB,DEBUG PORT,TP	1A
Date: Wednesday, April 25, 2007	Sheet 22 of 30	

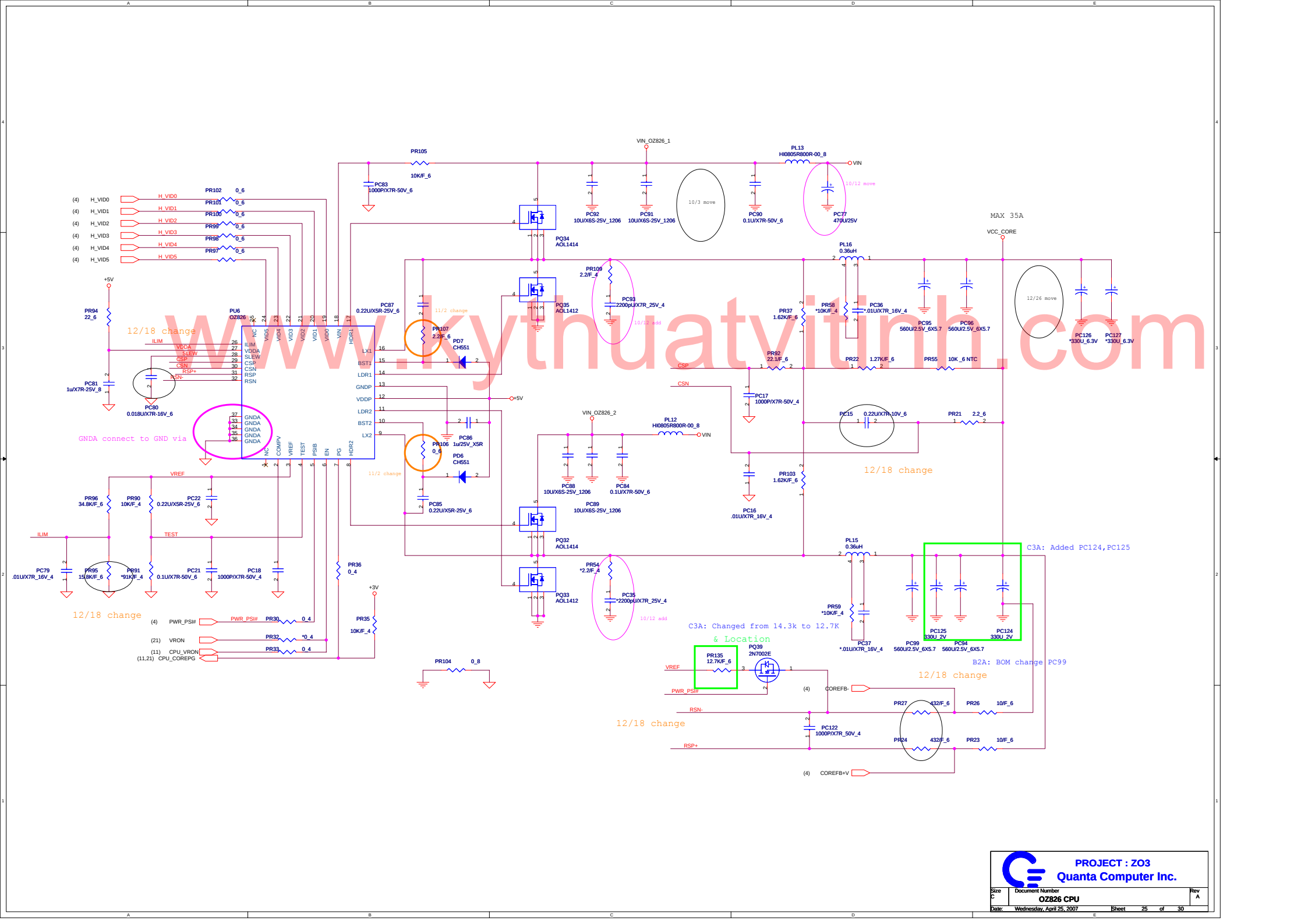
PROJECT : ZO3
Quanta Computer Inc.



CELL-SET = Hi ----> Cells = VDD ----->4S
CELL-SET = Low ----> Cells = GND ----->3S

PROJECT : ZO3		
Quanta Computer Inc.		
Size: Custom	Document Number: ISL6251 CHARGER	Rev: A
Date: Wednesday, April 25, 2007	Sheet 23 of 30	





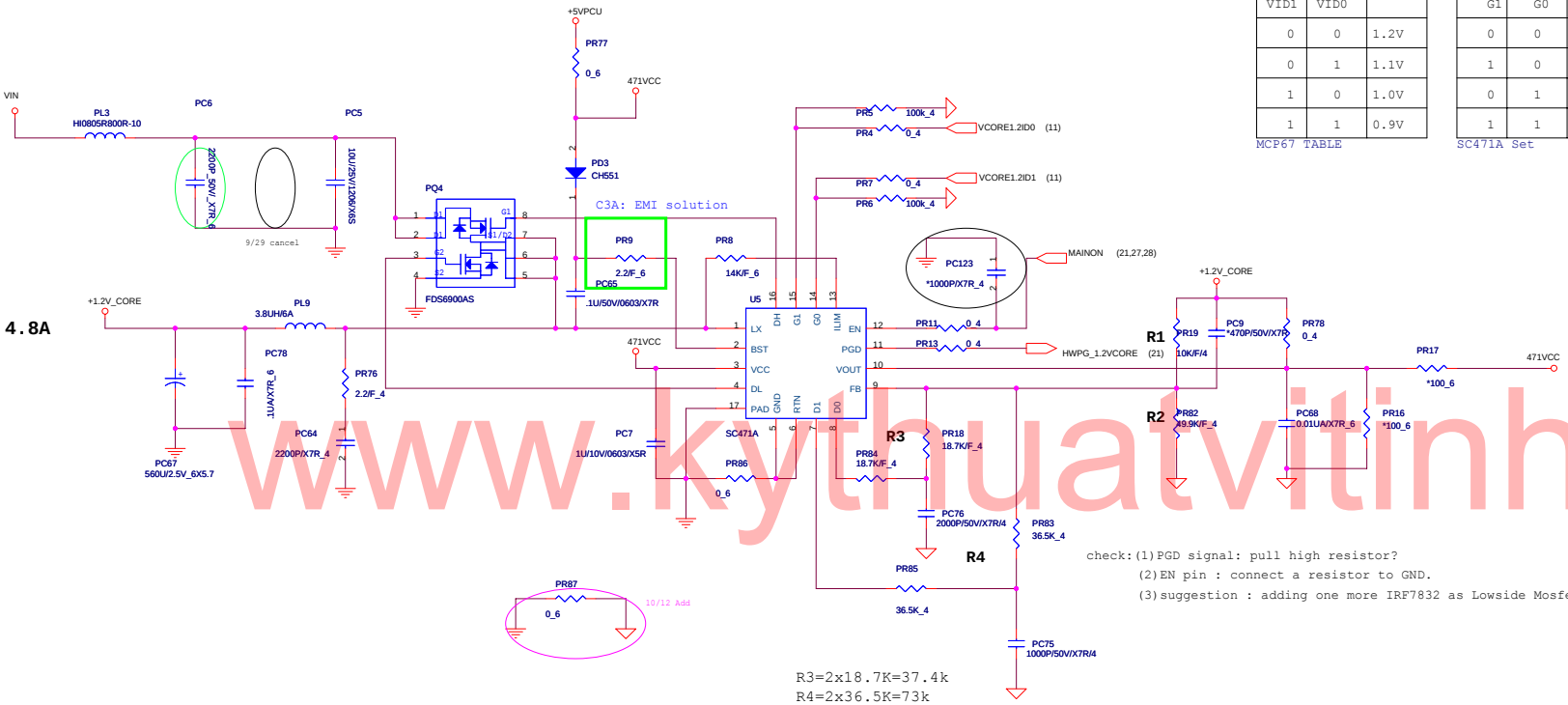
PROJECT : ZO3			
Quanta Computer Inc.			
Size: C	Document Number: OZ826 CPU		Rev: A
Date: Wednesday, April 25, 2007	Sheet 25 of 30		

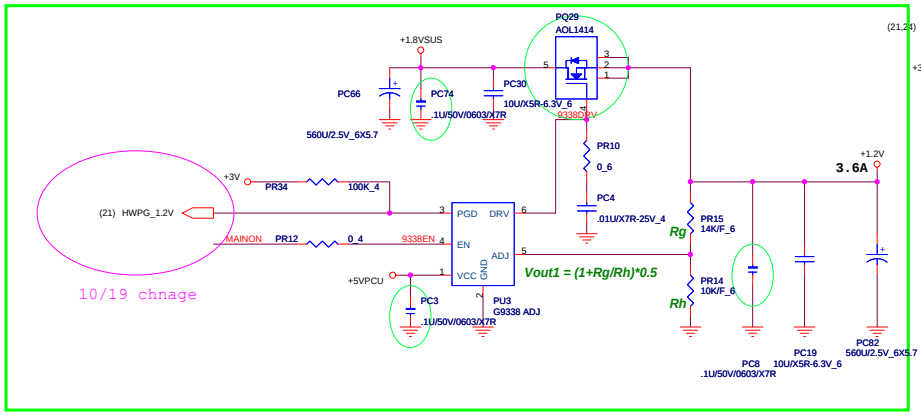
VID[1:0]		
VID1	VID0	
0	0	1.2V
0	1	1.1V
1	0	1.0V
1	1	0.9V

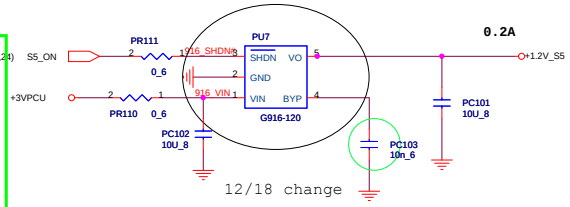
MCP67 TABLE

INPUTS		OUTPUTS	VOUT1
G1	G0	OD1 OD2 OD3	
0	0	0.75x(1+R1/R2+R1/R3+R1/R4)	1.2V
0	1	0.75x(1+R1/R2+R1/R3)	1.1V
1	0	0.75x(1+R1/R2+R1/R4)	1.0V
1	1	0.75x(1+R1/R2)	0.9V

SC471A Set







PROJECT : ZO3
Quanta Computer Inc.

Size	Document Number	Rev
C	SC471J 1.2V	A

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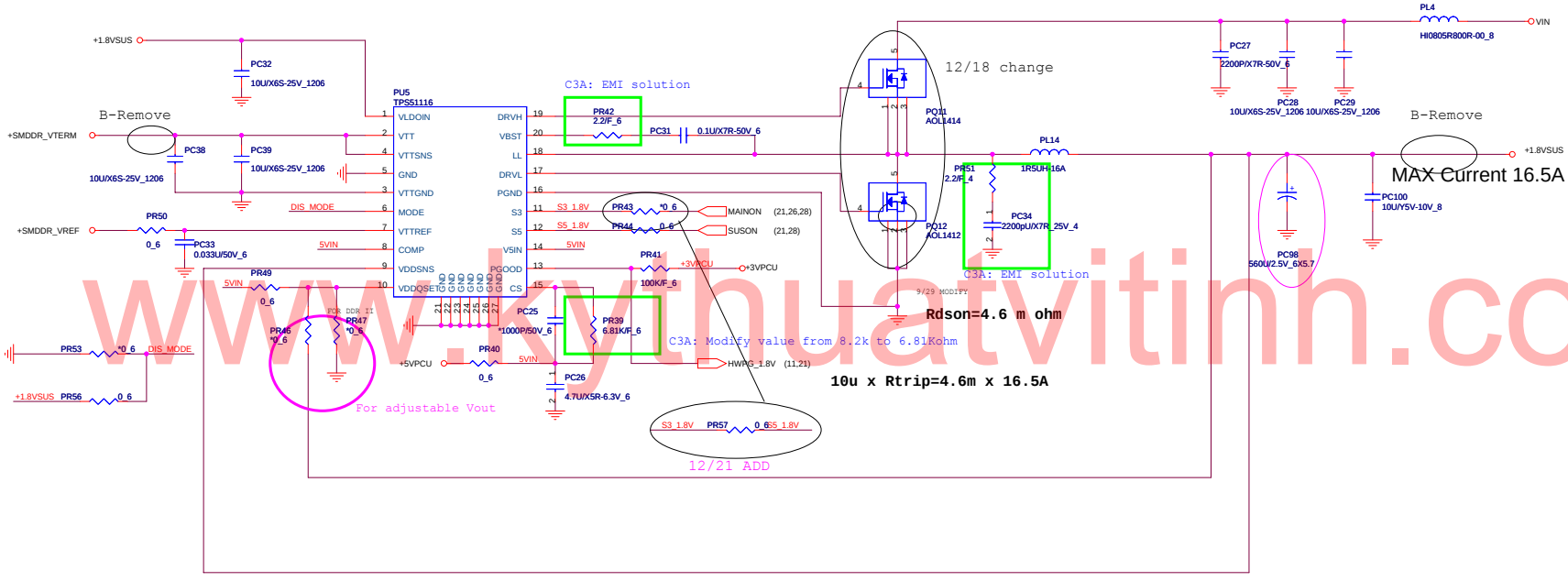

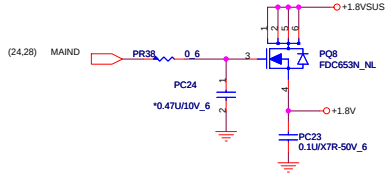

MAX Current 3.5A

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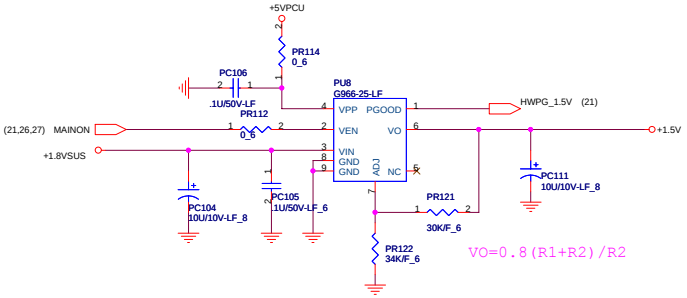

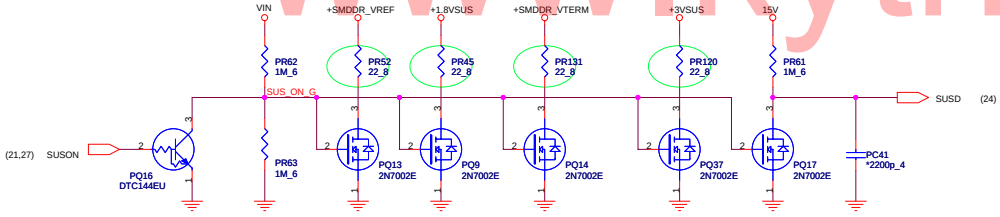

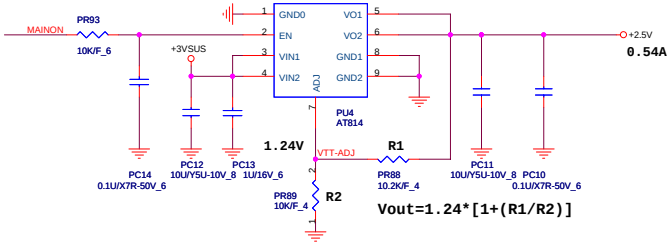

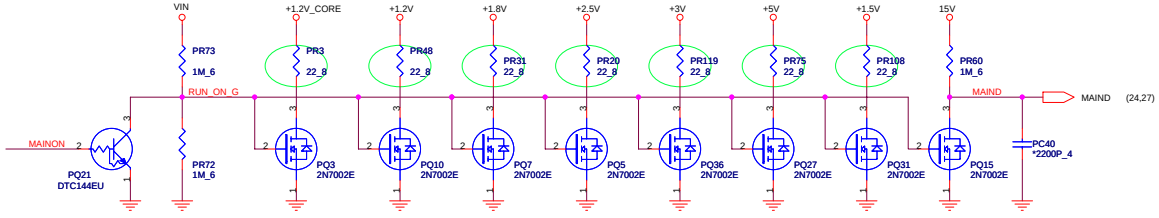

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