

# Bolsena-E(AB2) Block Diagram

Project Code: 91.4G401.001  
 REVISION: 05236-SA

- Dummy when use '10/100'
- Dummy when use 'GIGA'
- Dummy when use 'UMA'
- Dummy when use 'DIS'
- Dummy when use 'SATA'
- Dummy when use 'IDE'

**CLK GEN**  
 IDT CV137<sub>3</sub>

LEDs 16  
 RTC BAT. 17  
 BUTTONs 33

**AMD CPU**  
 35W/25W  
 4,5,6,7

200-PIN DDR SODIMM  
 DDR x2  
 8,9,10

**PWR SW**  
 CP2211  
 26

PCMCIA I/F

**PCMCIA SLOT**  
 Support TypeII  
 26

**ENE**  
 CB1410  
 1\* Slot Cardbus  
 25

HyperTransport  
 6.4GB/S 16b/8b

**ATI**  
 RS482M  
 AGTL+ CPU I/F + UMA  
 11,12,13,14

tv 16

LVDS LCD 16

RGB CRT CRT 15

MS/MS Pro/xD/  
 MMC/SD 5 in 1 28

1394 CONN 28

**RICOH**  
 R5C832  
 1394 CardReader  
 27,28

PCI-Express x2

ATI M52P  
 49,50,51,52,53

VRAM x4  
 54,55

Mini-PCI 802.11a/b/g 29

RJ45 31

TXFM 31

TXFM 31

1000Mb

10/100Mb

**PCI LAN**  
 Realtek  
 RTL8110SBL  
 1000/100/10  
 RTL8100C  
 100/10  
 30

**ATI**  
 SB450  
 PCI ACPI 2.0 6xUSB 2.0  
 AZALIA  
 LPC I/F  
 ATA I33 17,18,19,20,21

USB x 4 24

AZALIA

**CODEC**  
 ALC883 32

Line In MIC In 3

Line Out 33

Int. SPKR 33

**OP AMP**  
 G1421 33

MODEM MDC Card 23

RJ11 CONN 31

BlueTooth miniUSB 23

PIDE

HDD 24

SIDE

DVD/CD-RW 24

SATA 24

LPC Bus / 33MHz

**NS SIO**  
 PC87381 37

FIR TFDU6102 37

Thermal & Fan G792 23

**KBC**  
 KB3910 34

Touch Pad 35

Int. KB 35

ISA ROM 36

XBUS

**PCB Layer Stackup**

- L1: Signal 1
- L2: VCC
- L3: Signal 2
- L4: Signal 3
- L5: GND
- L6: Signal 4

Power Block Diag -> Page 40

<Variant Name>

**緯創資通 Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **BLOCK DIAGRAM**

Size A3 Document Number **Bolsena-E** Rev SA

Date: Thursday, October 13, 2005 Sheet 1 of 58

### PCI Routing

	IDSEL	IRQ	REQ/GNT
MiniPCI	21	F	0
LAN	23	H	2
7411	22	E (CardBus)	1
7411	17	G (1394)	3
7411	17	E (FlashMedia)	3

www.kythuativinh.com

Ref.	function	schematic	BOM
U81	cpu socket	62.10055.121	(DON'T CHANGE) (3mm high)
U80	north bridge	71.RS482.M03	71.RS482.M03 (ver A12)
U43	south bridge	71.SB400.B0U	71.SB400.D0U (ver A13)
U32	clock gen.	71.00137.C0W	71.00137.C0W
---			
U70	VGA M52	71.0M52P.A0U	
U64	VRAM FOR M52		
U65	VRAM FOR M52		
U69	VRAM FOR M52		
U71	VRAM FOR M52		
---			
U66	BIOS SOCKET	72.39040.G03	62.10002.032 (NO NEED WHEN PD)
U66	BIOS IC	72.39040.G03	72.39040.H03 (DIP STAGE IN LAB, SMT IN PD)
---			
U75	GIGA LAN	71.08110.00G	71.08110.A0G
U75	10/100 LAN	71.08110.00G	71.08100.C0G

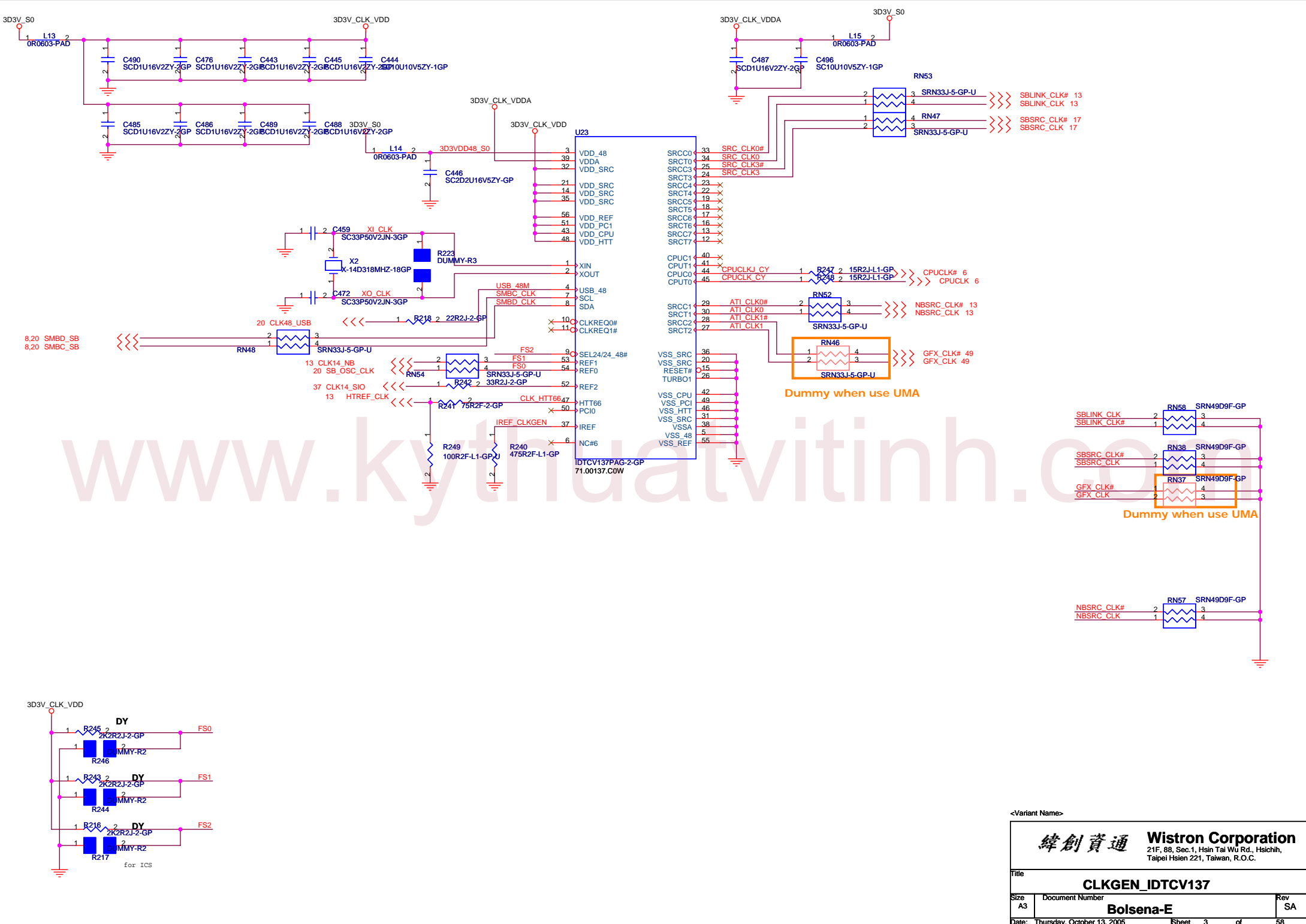
<Variant Name>

**緯創資通** **Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **HISTORY**

Size A3	Document Number <b>Bolsena-E</b>	Rev SA
------------	-------------------------------------	-----------

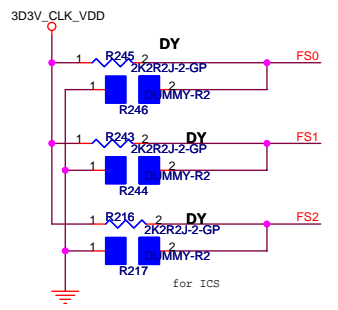
Date: Thursday, October 13, 2005 Sheet 2 of 58



8.20 SMBD\_SB  
8.20 SMBC\_SB

Dummy when use UMA

Dummy when use UMA



<Variant Name>

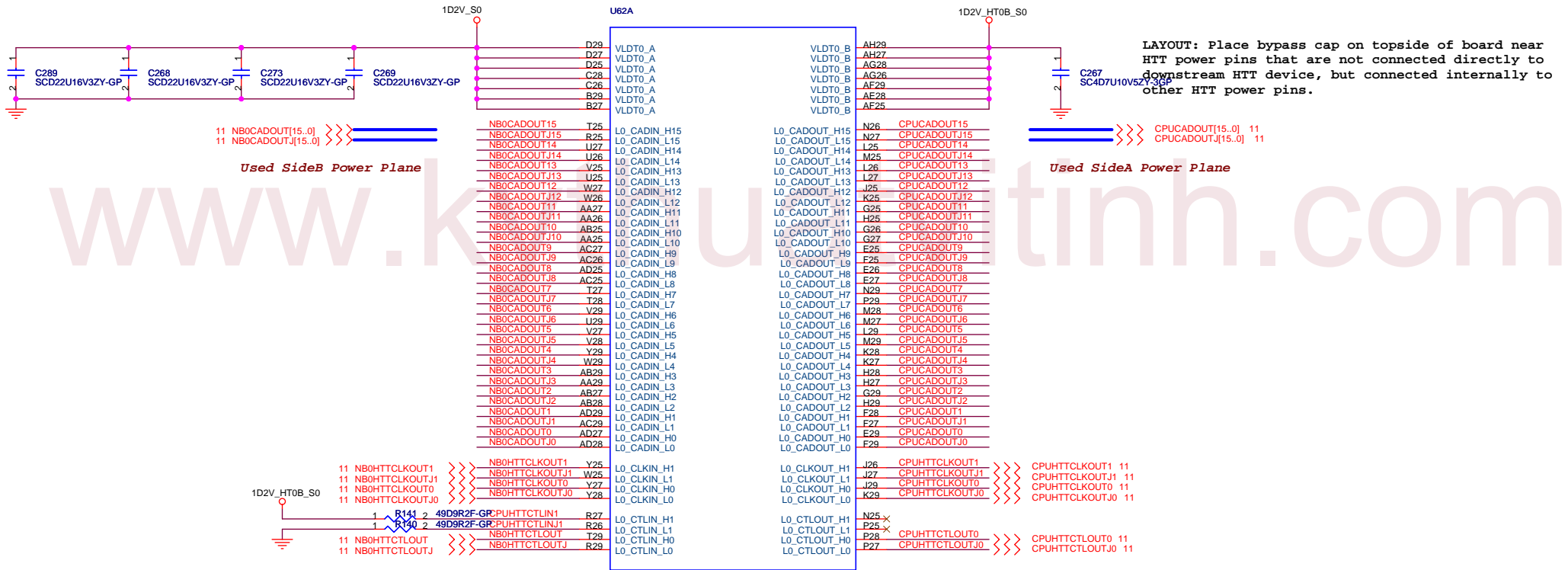
**緯創資通 Wistron Corporation**  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **CLKGEN\_IDTCV137**

Size A3	Document Number	Rev SA
<b>Bolsena-E</b>		
Date: Thursday, October 13, 2005	Sheet 3	of 58

HTT for CPU sideA  
 Transmit power  
 and NB sideA Receive  
 power

HTT for CPU sideB  
 Receive power  
 and NB sideA  
 Transmit power



ME : 62.10055.121  
 2nd:62.10055.101

<Variant Name>

**緯創資通 Wistron Corporation**  
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

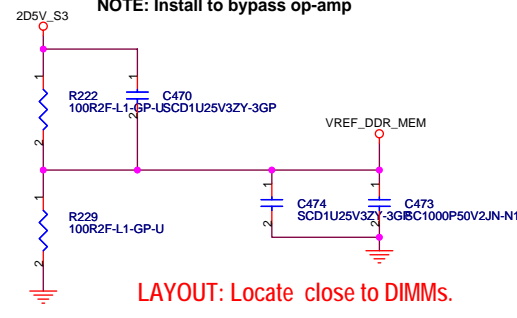
Title: **CPU(1/4)\_HyperTransport I/F**

Size: A3 Document Number: **Bolsena-E** Rev: SA

Date: Thursday, October 13, 2005 Sheet 4 of 58

# VREF\_DDR\_MEM

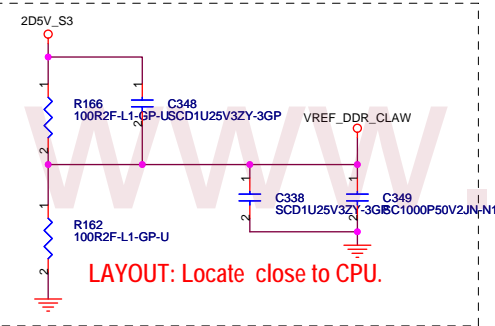
NOTE: Test with passive probes only.  
NOTE: Install to bypass op-amp



LAYOUT: Locate close to DIMMs.

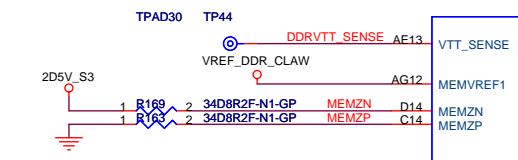
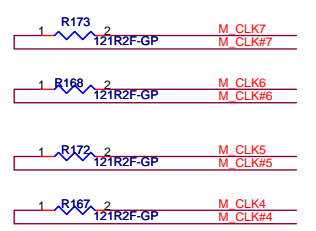
NOTE: Remove to bypass op-amp

# VREF\_DDR\_CLAW



LAYOUT: Locate close to CPU.

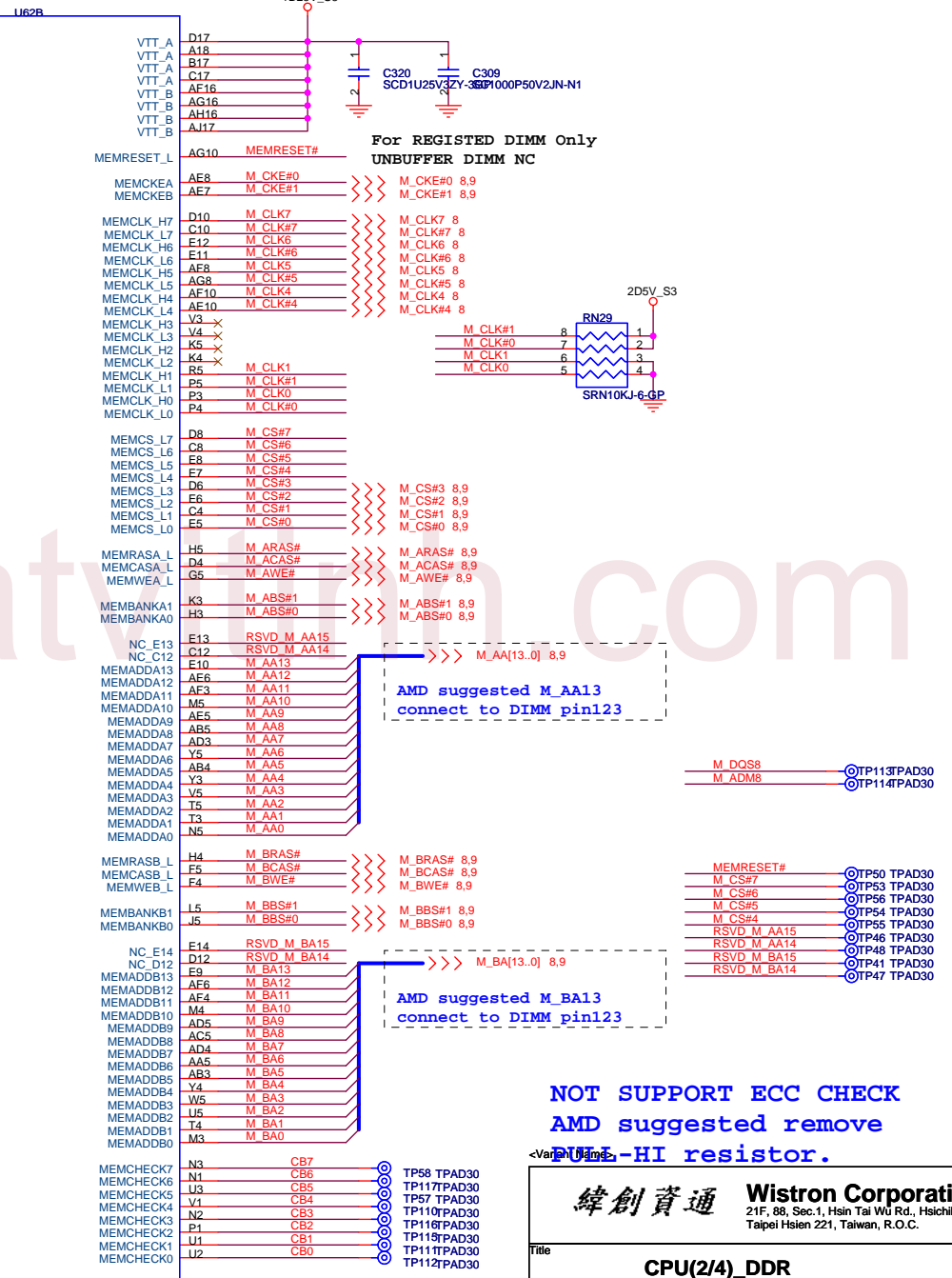
Place it near CPU



9 M\_DATA[63..0]

9 M\_ADM[7..0]

9 M\_DOS[7..0]



For REGISTERED DIMM Only  
UNBUFFER DIMM NC

>>> M\_AA[13..0] 8,9  
AMD suggested M\_AA13 connect to DIMM pin123

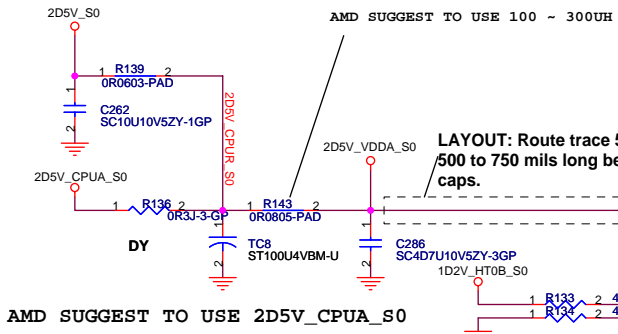
>>> M\_BA[13..0] 8,9  
AMD suggested M\_BA13 connect to DIMM pin123

NOT SUPPORT ECC CHECK  
AMD suggested remove  
DQS-HI resistor.

緯創資通 Wistron Corporation  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title <b>CPU(2/4)_DDR</b>		
Size A3	Document Number <b>Bolsena-E</b>	Rev SA
Date: Thursday, October 13, 2005 Sheet 5 of 58		

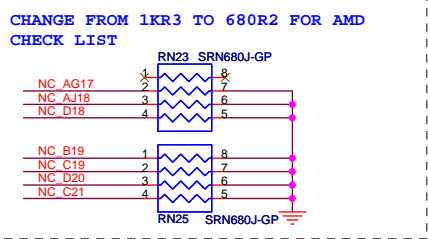
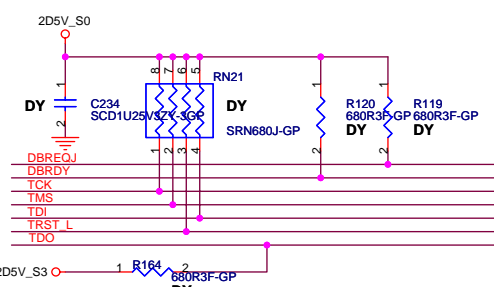
# 2D5V\_VDDA\_S0



**KEMET, NT: 5.7, B2 size**  
**ST100U4VBM-1 (80.10716.321)**  
 Tripple=1.1A, ESR=70mohm

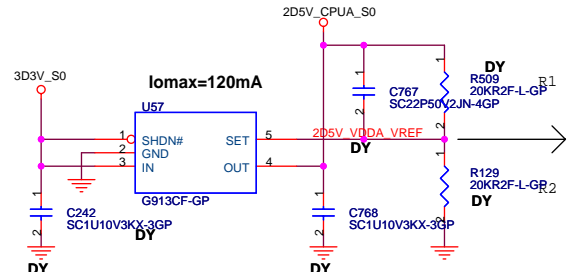
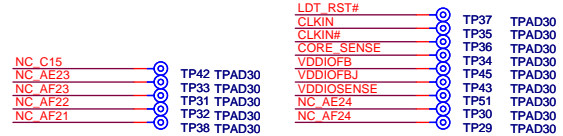
**SANYO, NT: 6.1**  
 Tripple=1.1A, ESR=70mohm  
 3.5/2.8/2.0  
 77.21071.031

AMD suggest voltage from 2D5V\_S0 to 2D5V\_S3 differentially impedance 100



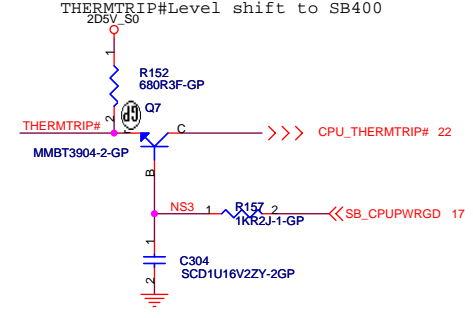
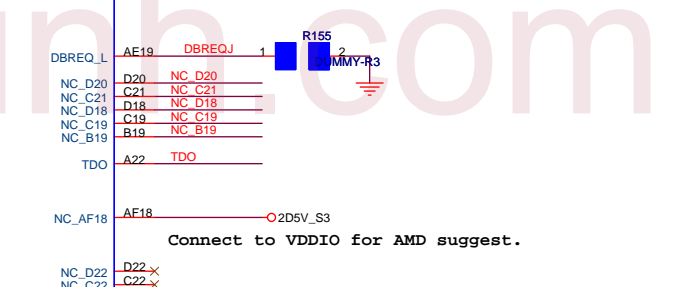
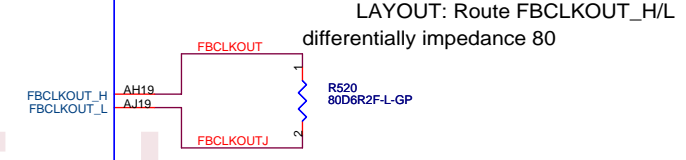
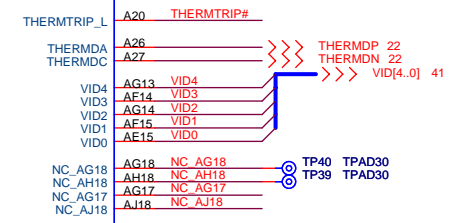
## Validation Test Points

LAYOUT: Place close to the CPU.



LAYOUT: Route trace 50 mils wide and 500 to 750 mils long between these caps.

LAYOUT: Route VDDA trace approx. 50 mils wide (use 2x25 mil traces to exit ball field) and 500 mils long.



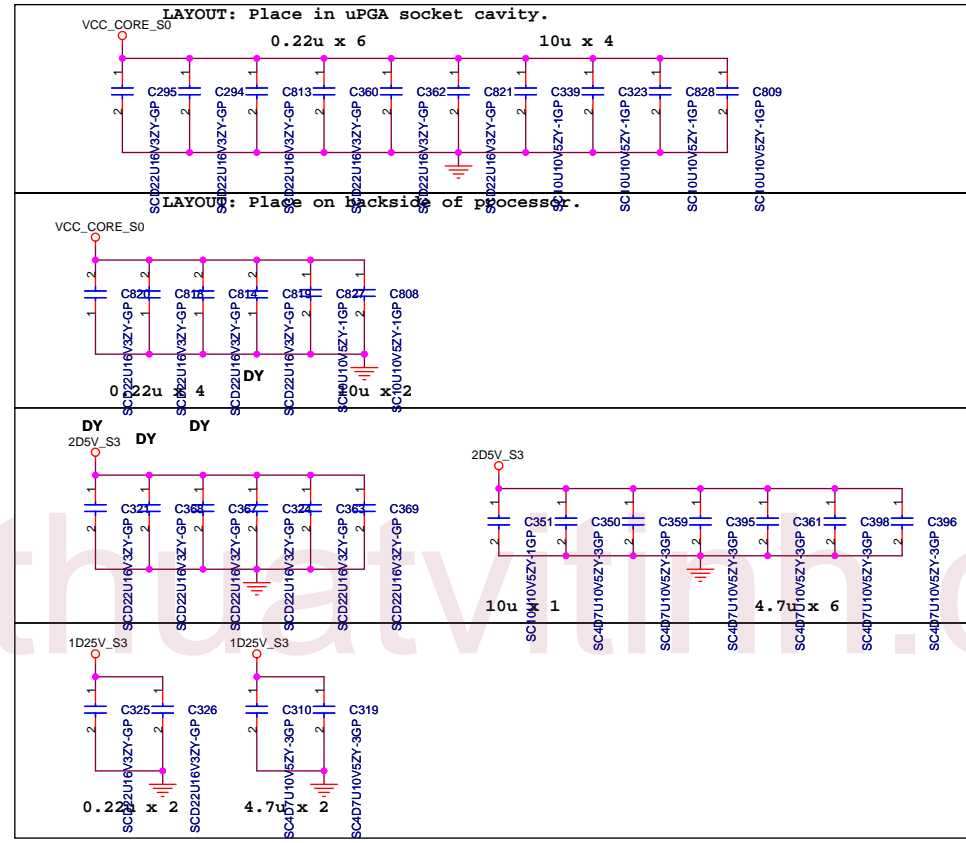
Wistron Corporation  
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

**CPU(3/4)\_Control & Debug**

Bolesna-E

Thursday, October 13, 2005

U62E	VSS	N20	VDD	E4
Y17	VSS	L20	VDDIO	G4
K17	VSS	I20	VDDIO	J4
H17	VSS	AF19	VDDIO	L4
F17	VSS	AD19	VDDIO	N4
E18	VSS	AB19	VDDIO	U4
AJ26	VSS	B20	VDDIO	W4
AE29	VSS	K19	VDDIO	AA4
AC16	VSS	H22	VDDIO	AC4
AA16	VSS	F19	VDDIO	AE4
J16	VSS	D19	VDDIO	D5
G16	VSS	AC18	VDDIO	AF5
F16	VSS	AA18	VDDIO	H6
AH14	VSS	G18	VDDIO	K6
AD15	VSS	R16	VDDIO	M6
AE15	VSS	AD17	VDDIO	T6
K15	VSS	AB17	VDDIO	V6
E15	VSS	H15	VDDIO	Y6
D16	VSS	F15	VDDIO	AB6
AE14	VSS	G28	VDDIO	AD6
AC14	VSS	D28	VDDIO	D7
AA14	VSS	B28	VDDIO	J7
G14	VSS	C27	VDDIO	AA7
AE17	VSS	H16	VDDIO	AC7
AD13	VSS	AB16	VDDIO	AE7
V13	VSS	Y26	VDDIO	F8
V13	VSS	G17	VDDIO	H8
V13	VSS	J17	VDDIO	AB8
H13	VSS	M26	VDDIO	AD8
F13	VSS	M26	VDDIO	D9
AH12	VSS	H26	VDDIO	G9
AC12	VSS	D26	VDDIO	AC9
AA12	VSS	F18	VDDIO	AF9
G12	VSS	C25	VDDIO	F10
AD12	VSS	Y18	VDDIO	AD10
AD11	VSS	AB18	VDDIO	D11
AB11	VSS	AJ24	VDDIO	AE11
Y11	VSS	AG24	VDDIO	F12
K11	VSS	AD18	VDDIO	AD12
H11	VSS	AC24	VDDIO	D13
V11	VSS	E19	VDDIO	AE13
V11	VSS	G19	VDDIO	F14
AH10	VSS	AC19	VDDIO	F16
AC10	VSS	AA19	VDDIO	AD16
W10	VSS	AJ19	VDDIO	D15
U10	VSS	N24	VDDIO	R4
R10	VSS	H19	VDDIO	U28
N10	VSS	F20	VDDIO	D11
L10	VSS	E20	VDDIO	AA28
J10	VSS	D20	VDDIO	AE27
G10	VSS	C20	VDDIO	R7
B10	VSS	B20	VDDIO	M8
AD9	VSS	AJ20	VDDIO	P8
V9	VSS	AG22	VDDIO	T8
V9	VSS	AC22	VDDIO	V8
V9	VSS	AA22	VDDIO	Y8
T9	VSS	E23	VDDIO	J9
T9	VSS	D23	VDDIO	N9
P9	VSS	AJ22	VDDIO	R9
M9	VSS	AG22	VDDIO	U9
K9	VSS	AC22	VDDIO	W9
H9	VSS	AA22	VDDIO	AA9
F9	VSS	E22	VDDIO	H10
AE9	VSS	D22	VDDIO	K10
AC9	VSS	AJ22	VDDIO	M10
W8	VSS	AG22	VDDIO	P10
U8	VSS	AC22	VDDIO	T10
R8	VSS	AA22	VDDIO	Y10
R8	VSS	E22	VDDIO	AB10
NR	VSS	D22	VDDIO	G11
LR	VSS	AJ22	VDDIO	H11
JR	VSS	AG22	VDDIO	AA11
GR	VSS	AC22	VDDIO	AC11
B8	VSS	AA22	VDDIO	H12
AD7	VSS	E23	VDDIO	K12
AB7	VSS	D23	VDDIO	L12
V7	VSS	AJ23	VDDIO	AB12
V7	VSS	AG23	VDDIO	J13
V7	VSS	AC23	VDDIO	AA13
AH6	VSS	AA23	VDDIO	AC13
AC6	VSS	E24	VDDIO	H14
AA6	VSS	D24	VDDIO	AB26
U6	VSS	AJ20	VDDIO	E28
R6	VSS	AG20	VDDIO	J28
R6	VSS	AC20	VDDIO	
N6	VSS	AA20	VDDIO	
LR	VSS	E24	VDDIO	
LR	VSS	D24	VDDIO	
GR	VSS	AJ24	VDDIO	
B6	VSS	AG24	VDDIO	
B6	VSS	AC24	VDDIO	
AH4	VSS	AA24	VDDIO	
B4	VSS	E25	VDDIO	
AH2	VSS	D25	VDDIO	
AD2	VSS	AJ25	VDDIO	
AB2	VSS	AG25	VDDIO	
Y2	VSS	AC25	VDDIO	
V2	VSS	AA25	VDDIO	
V2	VSS	E26	VDDIO	
T2	VSS	D26	VDDIO	
P2	VSS	AJ26	VDDIO	
M2	VSS	AG26	VDDIO	
K2	VSS	AC26	VDDIO	
H2	VSS	AA26	VDDIO	
F2	VSS	E27	VDDIO	
C29	VSS	D27	VDDIO	
AH28	VSS	AJ27	VDDIO	
AF28	VSS	AG27	VDDIO	
AC28	VSS	AC27	VDDIO	
W28	VSS	AA27	VDDIO	
R28	VSS	E28	VDDIO	
L28	VSS	D28	VDDIO	





M_AA0	112	A0
M_AA1	111	A1
M_AA2	110	A2
M_AA3	109	A3
M_AA4	108	A4
M_AA5	107	A5
M_AA6	106	A6
M_AA7	105	A7
M_AA8	102	A8
M_AA9	101	A9
M_AA10	115	A10 / AP
M_AA11	100	A11
M_AA12	99	A12
M_ABS#0	117	BA0
M_ABS#1	116	BA1
M_DATA R 0	5	DQ0
M_DATA R 1	7	DQ1
M_DATA R 2	13	DQ2
M_DATA R 3	17	DQ3
M_DATA R 4	6	DQ4
M_DATA R 5	8	DQ5
M_DATA R 6	14	DQ6
M_DATA R 7	18	DQ7
M_DATA R 8	19	DQ8
M_DATA R 9	29	DQ9
M_DATA R 10	23	DQ10
M_DATA R 11	31	DQ11
M_DATA R 12	20	DQ12
M_DATA R 13	24	DQ13
M_DATA R 14	30	DQ14
M_DATA R 15	32	DQ15
M_DATA R 16	41	DQ16
M_DATA R 17	43	DQ17
M_DATA R 18	49	DQ18
M_DATA R 19	53	DQ19
M_DATA R 20	42	DQ20
M_DATA R 21	44	DQ21
M_DATA R 22	50	DQ22
M_DATA R 23	54	DQ23
M_DATA R 24	55	DQ24
M_DATA R 25	59	DQ25
M_DATA R 26	65	DQ26
M_DATA R 27	67	DQ27
M_DATA R 28	56	DQ28
M_DATA R 29	60	DQ29
M_DATA R 30	66	DQ30
M_DATA R 31	68	DQ31
M_DATA R 32	127	DQ32
M_DATA R 33	129	DQ33
M_DATA R 34	135	DQ34
M_DATA R 35	139	DQ35
M_DATA R 36	128	DQ36
M_DATA R 37	130	DQ37
M_DATA R 38	136	DQ38
M_DATA R 39	140	DQ39
M_DATA R 40	141	DQ40
M_DATA R 41	145	DQ41
M_DATA R 42	151	DQ42
M_DATA R 43	153	DQ43
M_DATA R 44	142	DQ44
M_DATA R 45	146	DQ45
M_DATA R 46	152	DQ46
M_DATA R 47	154	DQ47
M_DATA R 48	165	DQ48
M_DATA R 49	163	DQ49
M_DATA R 50	171	DQ50
M_DATA R 51	175	DQ51
M_DATA R 52	164	DQ52
M_DATA R 53	166	DQ53
M_DATA R 54	172	DQ54
M_DATA R 55	176	DQ55
M_DATA R 56	177	DQ56
M_DATA R 57	181	DQ57
M_DATA R 58	187	DQ58
M_DATA R 59	189	DQ59
M_DATA R 60	178	DQ60
M_DATA R 61	182	DQ61
M_DATA R 62	188	DQ62
M_DATA R 63	190	DQ63

# REVERSE TYPE 5.2MM

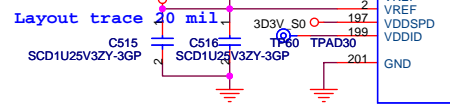
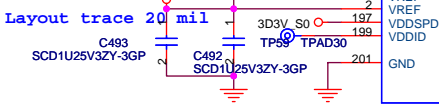
/CS0	121	M_CS#0 5.9
/CS1	122	M_CS#1 5.9
CKE0	96	M_CKE#0
CKE1	95	M_CKE#0 5.9
DQS0	11	M_DQS R0
DQS1	25	M_DQS R1
DQS2	47	M_DQS R2
DQS3	61	M_DQS R3
DQS4	133	M_DQS R4
DQS5	147	M_DQS R5
DQS6	169	M_DQS R6
DQS7	183	M_DQS R7
DQS8	77	
DM0	12	M_DM#0
DM1	26	M_DM#1
DM2	48	M_DM#2
DM3	62	M_DM#3
DM4	134	M_DM#4
DM5	148	M_DM#5
DM6	170	M_DM#6
DM7	184	M_DM#7
DM8	78	
CK0	35	M_CLK# 5
/CK0	37	M_CLK#5 5
CK1	160	M_CLK# 5
/CK1	158	M_CLK# 5
CK2	89	DDR_CLK# 5
/CK2	91	DDR_CLK# 5
SCL	195	SMBC_SB
SDA	193	SMBD_SB
SA0	194	
SA1	196	
SA2	198	
VDD	9	
VDD	10	
VDD	21	
VDD	22	
VDD	33	
VDD	34	
VDD	36	
VDD	46	
VDD	57	
VDD	58	
VDD	69	
VDD	70	
VDD	81	
VDD	82	
VDD	92	
VDD	93	
VDD	94	
VDD	113	
VDD	114	
VDD	131	
VDD	132	
VDD	143	
VDD	144	
VDD	155	
VDD	156	
VDD	157	
VDD	167	
VDD	168	
VDD	179	
VDD	180	
VDD	191	
VDD	192	
VSS	3	
VSS	4	
VSS	15	
VSS	16	
VSS	27	
VSS	28	
VSS	38	
VSS	39	
VSS	40	
VSS	51	
VSS	52	
VSS	63	
VSS	72	
VSS	74	
VSS	80	
VSS	84	
VSS	85	
VSS	86	
VSS	97	
VSS	98	
VSS	123	
VSS	124	
VSS	200	

NOT SUPPORT ECC CHECK  
AMD suggested pull-low

1ST 62.10017.701 - 2ND 62.10017.201

Part Number = 62.10017.701  
SKT-SODIMM200-24GP

ME : 62.10017.701  
2nd : 62.10017.691



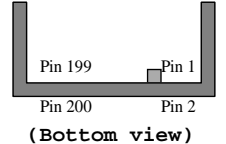
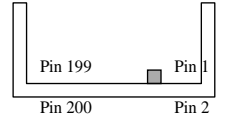
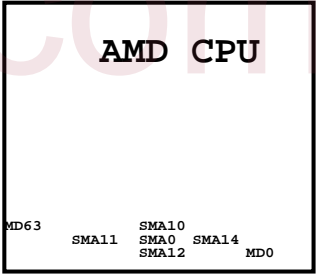
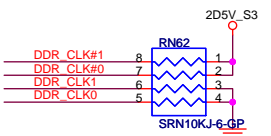
M_BA0	112	A0
M_BA1	111	A1
M_BA2	110	A2
M_BA3	109	A3
M_BA4	108	A4
M_BA5	107	A5
M_BA6	106	A6
M_BA7	105	A7
M_BA8	102	A8
M_BA9	101	A9
M_BA10	115	A10 / AP
M_BA11	100	A11
M_BA12	99	A12
M_BBS#0	117	BA0
M_BBS#1	116	BA1
DM0	12	M_DM#0
DM1	26	M_DM#1
DM2	48	M_DM#2
DM3	62	M_DM#3
DM4	134	M_DM#4
DM5	148	M_DM#5
DM6	170	M_DM#6
DM7	184	M_DM#7
DM8	78	
CK0	35	M_CLK# 5
/CK0	37	M_CLK#5 5
CK1	160	M_CLK# 5
/CK1	158	M_CLK# 5
CK2	89	DDR_CLK# 5
/CK2	91	DDR_CLK# 5
SCL	195	SMBC_SB
SDA	193	SMBD_SB
SA0	194	
SA1	196	
SA2	198	
VDD	9	
VDD	10	
VDD	21	
VDD	22	
VDD	33	
VDD	34	
VDD	36	
VDD	46	
VDD	57	
VDD	58	
VDD	69	
VDD	70	
VDD	81	
VDD	82	
VDD	92	
VDD	93	
VDD	94	
VDD	113	
VDD	114	
VDD	131	
VDD	132	
VDD	143	
VDD	144	
VDD	155	
VDD	156	
VDD	157	
VDD	167	
VDD	168	
VDD	179	
VDD	180	
VDD	191	
VDD	192	
VSS	3	
VSS	4	
VSS	15	
VSS	16	
VSS	27	
VSS	28	
VSS	38	
VSS	39	
VSS	40	
VSS	51	
VSS	52	
VSS	63	
VSS	72	
VSS	74	
VSS	80	
VSS	84	
VSS	85	
VSS	86	
VSS	97	
VSS	98	
VSS	123	
VSS	124	
VSS	200	

# REVERSE TYPE 9.2MM

/CS0	121	M_CS#2 5.9
/CS1	122	M_CS#3 5.9
CKE0	96	M_CKE#1 5.9
CKE1	95	
DQS0	11	M_DQS R0
DQS1	25	M_DQS R1
DQS2	47	M_DQS R2
DQS3	61	M_DQS R3
DQS4	133	M_DQS R4
DQS5	147	M_DQS R5
DQS6	169	M_DQS R6
DQS7	183	M_DQS R7
DQS8	77	
DM0	12	M_DM#0
DM1	26	M_DM#1
DM2	48	M_DM#2
DM3	62	M_DM#3
DM4	134	M_DM#4
DM5	148	M_DM#5
DM6	170	M_DM#6
DM7	184	M_DM#7
DM8	78	
CK0	35	M_CLK# 5
/CK0	37	M_CLK#4 5
CK1	160	M_CLK# 5
/CK1	158	M_CLK#6 5
CK2	89	DDR_CLK#1
/CK2	91	DDR_CLK#1
SCL	195	SMBC_SB 3.20
SDA	193	SMBD_SB 3.20
SA0	194	
SA1	196	
SA2	198	
VDD	9	
VDD	10	
VDD	21	
VDD	22	
VDD	33	
VDD	34	
VDD	36	
VDD	46	
VDD	57	
VDD	58	
VDD	69	
VDD	70	
VDD	81	
VDD	82	
VDD	92	
VDD	93	
VDD	94	
VDD	113	
VDD	114	
VDD	131	
VDD	132	
VDD	143	
VDD	144	
VDD	155	
VDD	156	
VDD	157	
VDD	167	
VDD	168	
VDD	179	
VDD	180	
VDD	191	
VDD	192	
VSS	3	
VSS	4	
VSS	15	
VSS	16	
VSS	27	
VSS	28	
VSS	38	
VSS	39	
VSS	40	
VSS	51	
VSS	52	
VSS	63	
VSS	72	
VSS	74	
VSS	80	
VSS	84	
VSS	85	
VSS	86	
VSS	97	
VSS	98	
VSS	123	
VSS	124	
VSS	200	

! NOT THIS LIBRARY

- ⟨⟨ M\_ADM\_R[7..0] 9
- ⟨⟨ M\_DATA\_R\_[63..0] 9
- ⟨⟨ M\_DQS\_R[7..0] 9
- ⟨⟨ M\_AA[13..0] 5.9
- ⟨⟨ M\_ABS#[1..0] 5.9
- ⟨⟨ M\_BA[13..0] 5.9
- ⟨⟨ M\_BBS#[1..0] 5.9



DDR1(Reverse 5.2mm)

DDR2(Reverse 9.2mm)

62.10017.391  
ME : 62.10017.391

Wistron Corporation  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

**Bolsena-E**

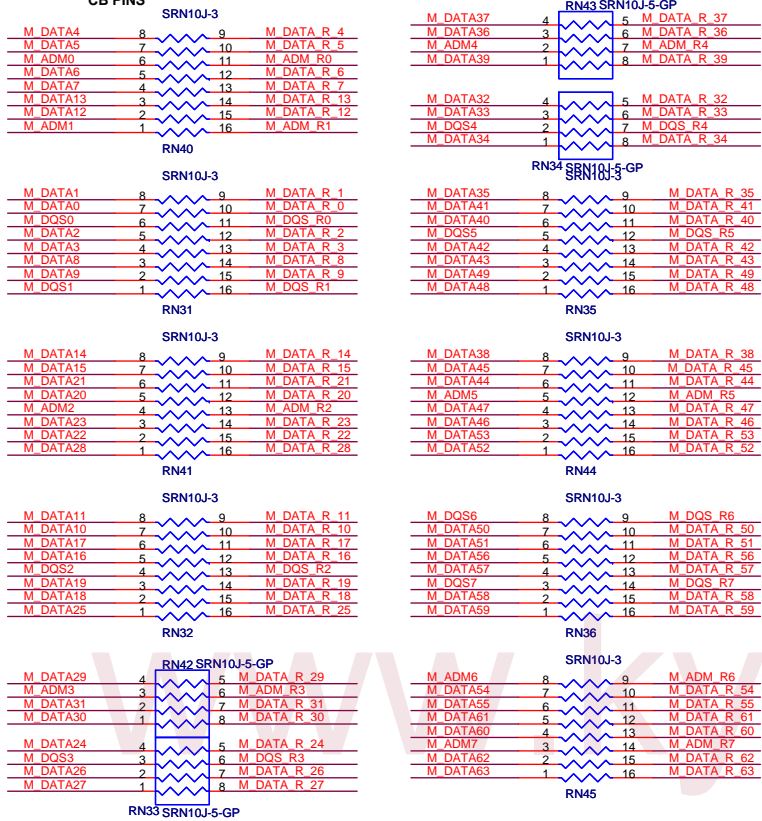
DDR SO-DIMM SKT

Sheet 8 of 58



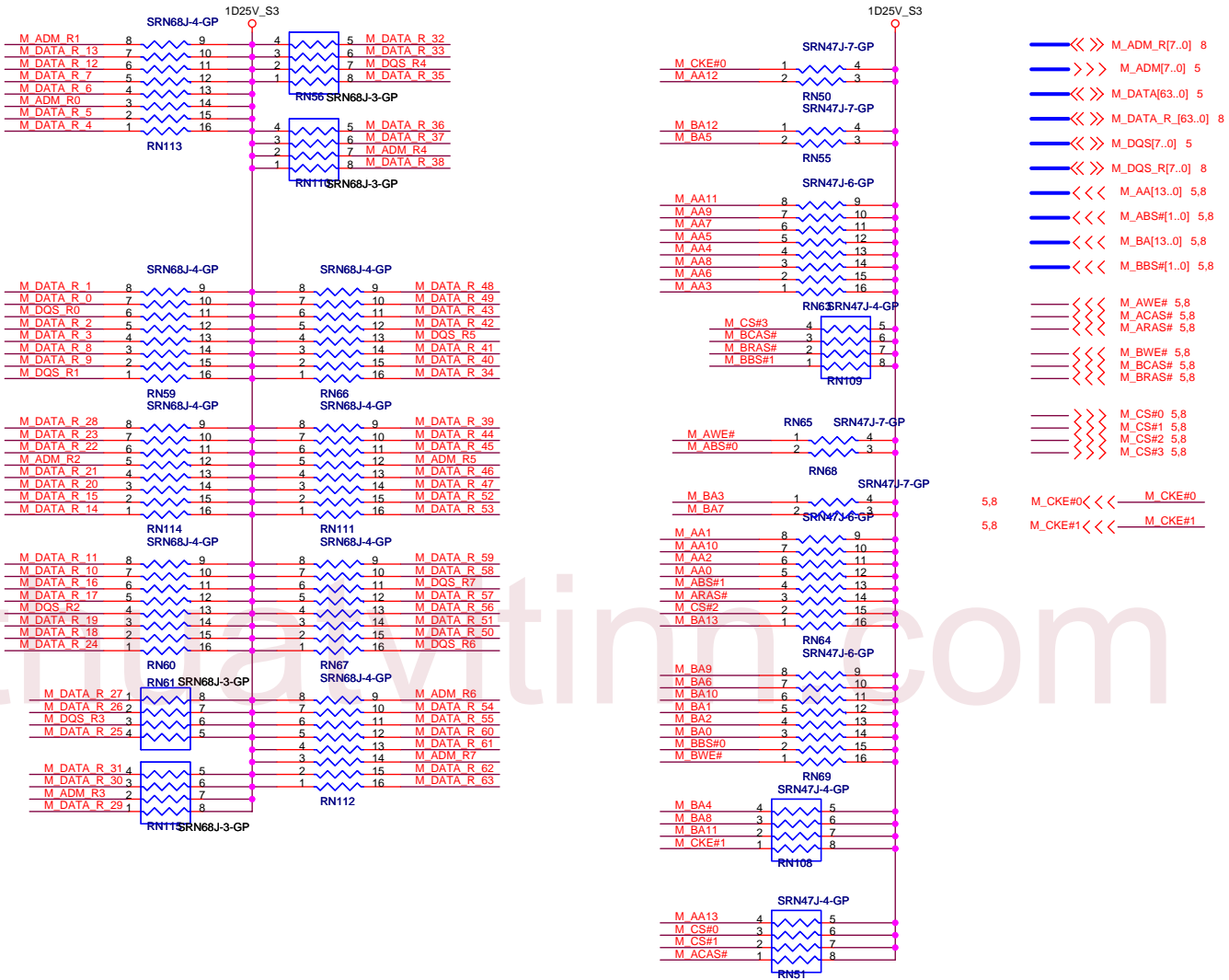
# SERIES DAMPING

PLACE Rns CLOSE TO FIRST DIMM, < 0.75"  
STRICT EQUAL LENGTH LIMITATION WITH DQS,  
CB PINS



# PARALLEL TERMINATION

PULL HIGH STUBS < 0.8", PLACE RPs CLOSE TO SECOND DM ( DM2 )  
NO EQUAL LENGTH LIMITATION

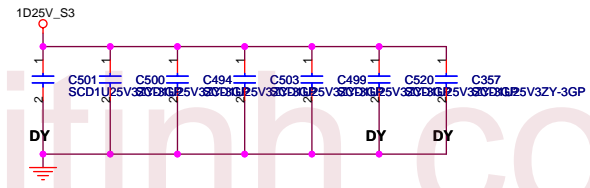
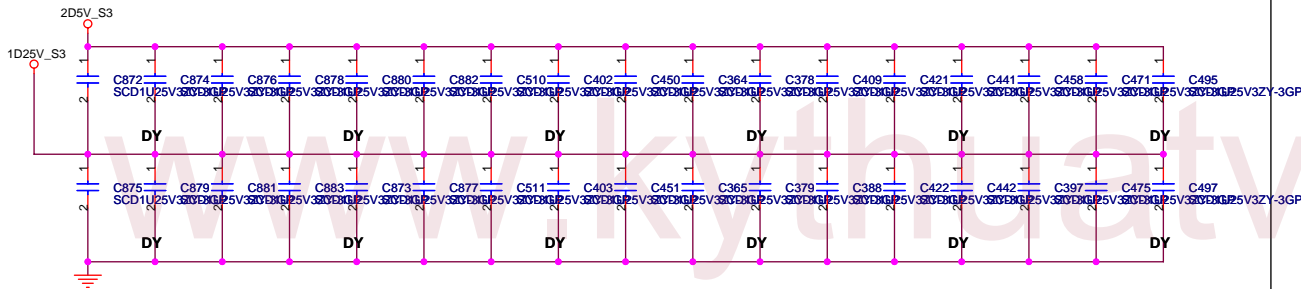
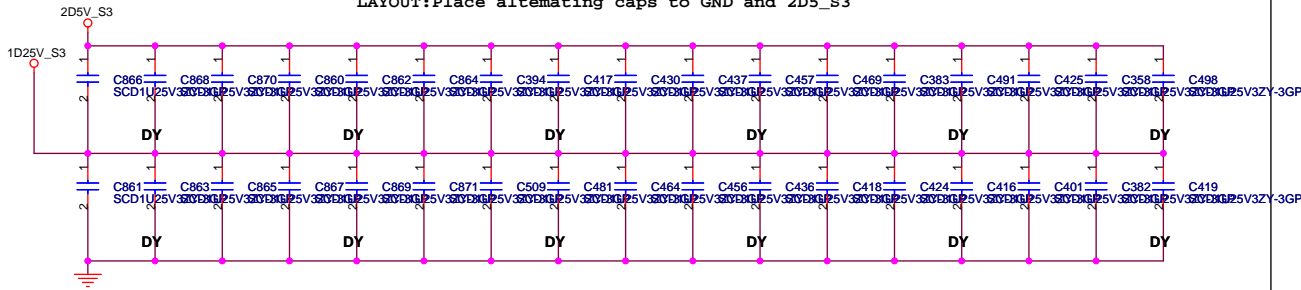


05/10  
Remove the damping resistor for AMD suggest.

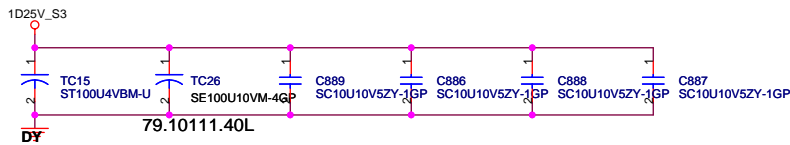
<Variant Name>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
<b>DDR DAMPING &amp; TERMINATION</b>		
Size	Document Number	Rev
A3		SA
<b>Bolsena-E</b>		
Date:	Thursday, October 13, 2005	Sheet 9 of 58

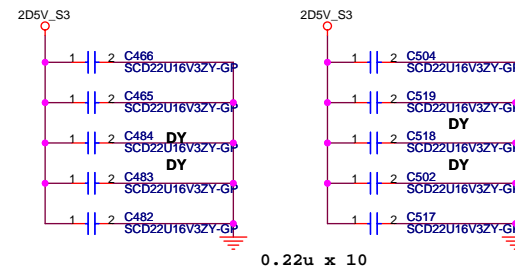
LAYOUT: Place alternating caps to GND and 2D5\_S3



LAYOUT: Place at end of the DIMMs



LAYOUT: Place close to Power Pin of DDR socket.



<Variant Name>

**緯創資通 Wistron Corporation**  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **DDR DECOUPLING**

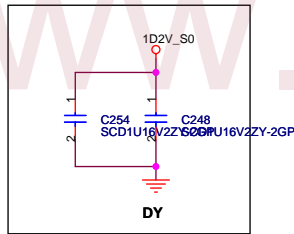
Size: A3	Document Number: <b>Bolsena-E</b>	Rev: SA
Date: Thursday, October 13, 2005 Sheet 10 of 58		

**CLAW HAMMER TO NB**

**NB TO CLAW HAMMER**

4 CPUCADOUT[15..0] >>>  
4 CPUCADOUTJ[15..0] >>>

>>> NB0CADOUT[15..0] 4  
>>> NB0CADOUTJ[15..0] 4



AROUND NB

4 CPUHTTCLKOUT1 >>>  
4 CPUHTTCLKOUTJ1 >>>  
4 CPUHTTCLKOUT0 >>>  
4 CPUHTTCLKOUTJ0 >>>  
4 CPUHTTCTLOUT0 >>>  
4 CPUHTTCTLOUTJ0 >>>

1D2V\_S0  
1 R124 2 49D9R2F-GP RXCALN D27  
1 R125 2 49D9R2F-GP RXCALP E27

CPUCADOUT15	T26	HT_RXCAD15P
CPUCADOUTJ15	R26	HT_RXCAD15N
CPUCADOUT14	U25	HT_RXCAD14P
CPUCADOUTJ14	U24	HT_RXCAD14N
CPUCADOUT13	V26	HT_RXCAD13P
CPUCADOUTJ13	U26	HT_RXCAD13N
CPUCADOUT12	W25	HT_RXCAD12P
CPUCADOUTJ12	W24	HT_RXCAD12N
CPUCADOUT11	AA25	HT_RXCAD11P
CPUCADOUTJ11	AA24	HT_RXCAD11N
CPUCADOUT10	AB26	HT_RXCAD10P
CPUCADOUTJ10	AA26	HT_RXCAD10N
CPUCADOUT9	AC25	HT_RXCAD9P
CPUCADOUTJ9	AC24	HT_RXCAD9N
CPUCADOUT8	AD26	HT_RXCAD8P
CPUCADOUTJ8	AC26	HT_RXCAD8N
CPUCADOUT7	R23	HT_RXCAD7P
CPUCADOUTJ7	R28	HT_RXCAD7N
CPUCADOUT6	T30	HT_RXCAD6P
CPUCADOUTJ6	R30	HT_RXCAD6N
CPUCADOUT5	T28	HT_RXCAD5P
CPUCADOUTJ5	T29	HT_RXCAD5N
CPUCADOUT4	V29	HT_RXCAD4P
CPUCADOUTJ4	U23	HT_RXCAD4N
CPUCADOUT3	Y30	HT_RXCAD3P
CPUCADOUTJ3	W30	HT_RXCAD3N
CPUCADOUT2	Y28	HT_RXCAD2P
CPUCADOUTJ2	Y29	HT_RXCAD2N
CPUCADOUT1	AB23	HT_RXCAD1P
CPUCADOUTJ1	AA23	HT_RXCAD1N
CPUCADOUT0	AC23	HT_RXCAD0P
CPUCADOUTJ0	AC28	HT_RXCAD0N

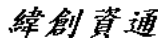
**PART 10F6**

**HYPER TRANSPORT CPU I/F**

HT_TXCAD15P	R24	NB0CADOUT15
HT_TXCAD15N	R25	NB0CADOUTJ15
HT_TXCAD14P	N26	NB0CADOUT14
HT_TXCAD14N	P26	NB0CADOUTJ14
HT_TXCAD13P	N24	NB0CADOUT13
HT_TXCAD13N	N25	NB0CADOUTJ13
HT_TXCAD12P	L26	NB0CADOUT12
HT_TXCAD12N	M26	NB0CADOUTJ12
HT_TXCAD11P	J26	NB0CADOUT11
HT_TXCAD11N	K26	NB0CADOUTJ11
HT_TXCAD10P	J24	NB0CADOUT10
HT_TXCAD10N	J25	NB0CADOUTJ10
HT_TXCAD9P	G26	NB0CADOUT9
HT_TXCAD9N	H26	NB0CADOUTJ9
HT_TXCAD8P	G24	NB0CADOUT8
HT_TXCAD8N	G25	NB0CADOUTJ8
HT_TXCAD7P	L30	NB0CADOUT7
HT_TXCAD7N	M30	NB0CADOUTJ7
HT_TXCAD6P	L28	NB0CADOUT6
HT_TXCAD6N	L29	NB0CADOUTJ6
HT_TXCAD5P	J29	NB0CADOUT5
HT_TXCAD5N	K29	NB0CADOUTJ5
HT_TXCAD4P	H30	NB0CADOUT4
HT_TXCAD4N	H29	NB0CADOUTJ4
HT_TXCAD3P	E29	NB0CADOUT3
HT_TXCAD3N	E28	NB0CADOUTJ3
HT_TXCAD2P	D30	NB0CADOUT2
HT_TXCAD2N	E30	NB0CADOUTJ2
HT_TXCAD1P	D28	NB0CADOUT1
HT_TXCAD1N	D29	NB0CADOUTJ1
HT_TXCAD0P	B29	NB0CADOUT0
HT_TXCAD0N	C29	NB0CADOUTJ0
HT_RXCLK1P	L24	NB0HTTCLKOUT1
HT_RXCLK1N	L25	NB0HTTCLKOUTJ1
HT_RXCLK0P	F29	NB0HTTCLKOUT0
HT_RXCLK0N	G29	NB0HTTCLKOUTJ0
HT_RXCTLP	M29	NB0HTTCTLOUT
HT_RXCTLN	M28	NB0HTTCTLOUTJ
HT_TXCALN	E28	HT_TXCALP
HT_TXCALN	A28	HT_TXCALN



<Variant Name>

 <b>Wistron Corporation</b> 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>ATI-RS482M (1 of 4) HT</b>	
Size A3	Document Number <b>Bolsena-E</b>
Date: Thursday, October 13, 2005	Sheet 11 of 58

49 PEG\_TXP[15..0] <<< ———  
 49 PEG\_TXN[15..0] <<< ———  
 49 PEG\_RXP[15..0] >>> ———  
 49 PEG\_RXN[15..0] >>> ———

**U61C PART 3 OF 6**

AE17	NC#AF17	NC#AF28	AE28
AK17	NC#AK17	NC#AF27	AE27
AH16	NC#AH16	NC#AG28	AG28
AF16	NC#AF16	NC#AF26	AE26
AJ22	NC#AJ22	NC#AE25	AE25
AJ21	NC#AJ21	NC#AE24	AE24
AH20	NC#AH20	NC#AF24	AF24
AH21	NC#AH21	NC#AG23	AG23
AK19	NC#AK19	NC#AE29	AE29
AH19	NC#AH19	NC#AF29	AF29
AJ17	NC#AJ17	NC#AG30	AG30
AG16	NC#AG16	NC#AG29	AG29
AG17	NC#AG17	NC#AH28	AH28
AH17	NC#AH17	NC#AF29	AF29
AJ18	NC#AJ18	NC#AJ28	AJ28
		NC#AH27	AH27
		NC#AJ27	AJ27
		NC#AE23	AE23
AG26	NC#AG26	NC#AG22	AG22
AJ29	NC#AJ29	NC#AF23	AF23
AE21	NC#AE21	NC#AF22	AF22
AH24	NC#AH24	NC#AE20	AE20
AH12	NC#AH12	NC#AG19	AG19
AG13	NC#AG13	NC#AF19	AF19
AH8	NC#AH8	NC#AH26	AH26
AE8	NC#AE8	NC#AJ26	AJ26
		NC#AH30	AH30
AE25	NC#AE25	NC#AG20	AG20
AH30	NC#AH30	NC#AH25	AH25
AG20	NC#AG20	NC#AJ24	AJ24
AJ25	NC#AJ25	NC#AH23	AH23
AH13	DVO_IDCKP	NC#AJ23	AJ23
AF14	NC#AF14	NC#AH22	AH22
AJ7	NC#AJ7	NC#AK14	AK14
AG8	NC#AG8	DVO_D11	D11
		DVO_D10	D10
		DVO_D9	D9
		DVO_D8	D8
		DVO_D7	D7
		DVO_D6	D6
		DVO_D4	D4
		NC#AE15	AE15
		NC#AF15	AF15
		NC#AG14	AG14
		NC#AE14	AE14
		NC#AE12	AE12
		NC#AF12	AF12
		NC#AG11	AG11
		NC#AE11	AE11
		DVO_D5	D5
		DVO_D2	D2
		DVO_D3	D3
		DVO_D0	D0
		DVO_DE	DE
		DVO_HSYNC	HSYNC
		DVO_VSYNC	VSYNC
		NC#AG10	AG10
		NC#AF11	AF11
		NC#AF10	AF10
		NC#AE9	AE9
		NC#AG7	AG7
		NC#AF8	AF8
		NC#AF7	AF7
		NC#AE7	AE7
		NC#AH5	AH5
		NC#AD30	AD30

**U61B PART 2 OF 6**

PEG_TXP15	D8	GFX_RX0P	GFX_TX0P	A7	PEG_RXP15_NB	C752	1	2	SCDTU16V22Y-2GP	PEG_RXP15
PEG_TXN15	D7	GFX_RX0N	GFX_TX0N	B7	PEG_RXN15_NB	C753	1	2	SCDTU16V22Y-2GP	PEG_RXN15
PEG_TXP14	D5	GFX_RX1P	GFX_TX1P	B6	PEG_RXP14_NB	C754	1	2	SCDTU16V22Y-2GP	PEG_RXP14
PEG_TXN14	D4	GFX_RX1N	GFX_TX1N	B5	PEG_RXN14_NB	C755	1	2	SCDTU16V22Y-2GP	PEG_RXN14
PEG_TXP13	F4	GFX_RX2P	GFX_TX2P	A5	PEG_RXP13_NB	C756	1	2	SCDTU16V22Y-2GP	PEG_RXP13
PEG_TXN13	F4	GFX_RX2N	GFX_TX2N	A4	PEG_RXN13_NB	C757	1	2	SCDTU16V22Y-2GP	PEG_RXN13
PEG_TXP12	G5	GFX_RX3P	GFX_TX3P	B4	PEG_RXP12_NB	C758	1	2	SCDTU16V22Y-2GP	PEG_RXP12
PEG_TXN12	G4	GFX_RX3N	GFX_TX3N	B3	PEG_RXN12_NB	C759	1	2	SCDTU16V22Y-2GP	PEG_RXN12
PEG_TXP11	H4	GFX_RX4P	GFX_TX4P	C1	PEG_RXP11_NB	C771	1	2	SCDTU16V22Y-2GP	PEG_RXP11
PEG_TXN11	J4	GFX_RX4N	GFX_TX4N	D1	PEG_RXN11_NB	C770	1	2	SCDTU16V22Y-2GP	PEG_RXN11
PEG_TXP10	H5	GFX_RX5P	GFX_TX5P	D2	PEG_RXP10_NB	C775	1	2	SCDTU16V22Y-2GP	PEG_RXP10
PEG_TXN10	G1	GFX_RX5N	GFX_TX5N	E2	PEG_RXN10_NB	C774	1	2	SCDTU16V22Y-2GP	PEG_RXN10
PEG_TXP9	G1	GFX_RX6P	GFX_TX6P	E2	PEG_RXP9_NB	C776	1	2	SCDTU16V22Y-2GP	PEG_RXP9
PEG_TXN9	G2	GFX_RX6N	GFX_TX6N	F1	PEG_RXN9_NB	C784	1	2	SCDTU16V22Y-2GP	PEG_RXN9
PEG_TXP8	K5	GFX_RX7P	GFX_TX7P	H2	PEG_RXP8_NB	C783	1	2	SCDTU16V22Y-2GP	PEG_RXP8
PEG_TXN8	K4	GFX_RX7N	GFX_TX7N	J2	PEG_RXN8_NB	C789	1	2	SCDTU16V22Y-2GP	PEG_RXN8
PEG_TXP7	L4	GFX_RX8P	GFX_TX8P	J1	PEG_RXP7_NB	C792	1	2	SCDTU16V22Y-2GP	PEG_RXP7
PEG_TXN7	M4	GFX_RX8N	GFX_TX8N	K1	PEG_RXN7_NB	C791	1	2	SCDTU16V22Y-2GP	PEG_RXN7
PEG_TXP6	M4	GFX_RX9P	GFX_TX9P	K2	PEG_RXP6_NB	C790	1	2	SCDTU16V22Y-2GP	PEG_RXP6
PEG_TXN6	N4	GFX_RX9N	GFX_TX9N	L2	PEG_RXN6_NB	C794	1	2	SCDTU16V22Y-2GP	PEG_RXN6
PEG_TXP5	P4	GFX_RX10P	GFX_TX10P	M2	PEG_RXP5_NB	C795	1	2	SCDTU16V22Y-2GP	PEG_RXP5
PEG_TXN5	R4	GFX_RX10N	GFX_TX10N	LM1	PEG_RXN5_NB	C801	1	2	SCDTU16V22Y-2GP	PEG_RXN5
PEG_TXP4	P5	GFX_RX11P	GFX_TX11P	N1	PEG_RXP4_NB	C799	1	2	SCDTU16V22Y-2GP	PEG_RXP4
PEG_TXN4	P6	GFX_RX11N	GFX_TX11N	N2	PEG_RXN4_NB	C798	1	2	SCDTU16V22Y-2GP	PEG_RXN4
PEG_TXP3	P2	GFX_RX12P	GFX_TX12P	R1	PEG_RXP3_NB	C800	1	2	SCDTU16V22Y-2GP	PEG_RXP3
PEG_TXN3	R2	GFX_RX12N	GFX_TX12N	T1	PEG_RXN3_NB	C805	1	2	SCDTU16V22Y-2GP	PEG_RXN3
PEG_TXP2	T5	GFX_RX13P	GFX_TX13P	T2	PEG_RXP2_NB	C804	1	2	SCDTU16V22Y-2GP	PEG_RXP2
PEG_TXN2	T4	GFX_RX13N	GFX_TX13N	U2	PEG_RXN2_NB	C810	1	2	SCDTU16V22Y-2GP	PEG_RXN2
PEG_TXP1	U4	GFX_RX14P	GFX_TX14P	V2	PEG_RXP1_NB	C811	1	2	SCDTU16V22Y-2GP	PEG_RXP1
PEG_TXN1	V4	GFX_RX14N	GFX_TX14N	V1	PEG_RXN1_NB	C812	1	2	SCDTU16V22Y-2GP	PEG_RXN1
PEG_TXP0	W1	GFX_RX15P	GFX_TX15P	Y2	PEG_RXP0_NB	C816	1	2	SCDTU16V22Y-2GP	PEG_RXP0
PEG_TXN0	W2	GFX_RX15N	GFX_TX15N	AA2	PEG_RXN0_NB	C817	1	2	SCDTU16V22Y-2GP	PEG_RXN0

LANE REVERSE

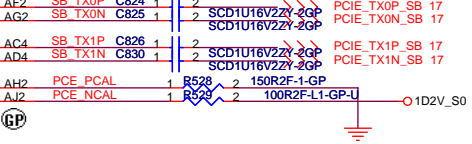
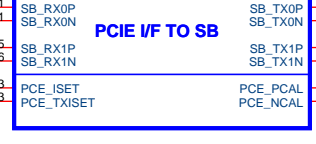
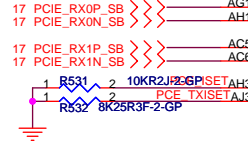
PCIE I/F TO VIDEO

LANE REVERSE

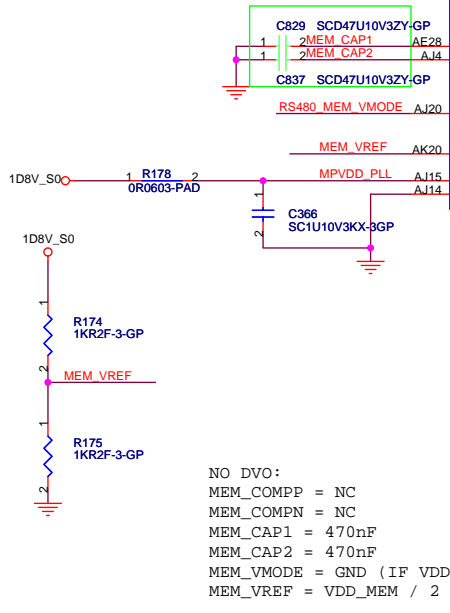
AE1	GPP_RX0P/SB_RX2P	GPP_TX0P/SB_TX2P	AD2	
AE2	GPP_RX0N/SB_RX2N	GPP_TX0N/SB_TX2N	AD1	
AB2	GPP_RX1P/SB_RX3P	GPP_TX1P/SB_TX3P	AA1	
AC2	GPP_RX1N/SB_RX3N	GPP_TX1N/SB_TX3N	AB1	
AB5	GPP_RX2P	GPP_TX2P	Y5	
AB4	GPP_RX2N	GPP_TX2N	Y6	
Y4	GPP_RX3P	GPP_TX3P	W5	
AA4	GPP_RX3N	GPP_TX3N	W4	

PCIE I/F TO SLOT

PCIE I/F TO SB



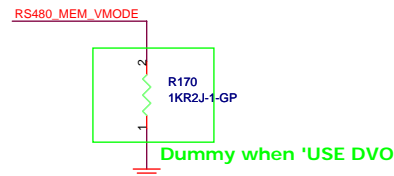
Dummy when 'USE DVO'



MEM\_A I/F

NO DVO:  
 MEM\_COMP = NC  
 MEM\_COMPN = NC  
 MEM\_CAP1 = 470nF  
 MEM\_CAP2 = 470nF  
 MEM\_VMODE = GND (IF VDD\_MEM = 2.5V)  
 MEM\_VREF = VDD\_MEM / 2

WITH DVO:  
 MEM\_COMP = 61.9 OHM TO GND  
 MEM\_COMPN = 61.9 OHM TO VDD\_MEM  
 MEM\_CAP1 = NC  
 MEM\_CAP2 = NC  
 MEM\_VMODE = 1.8V (IF VDD\_MEM = 1.8V)  
 MEM\_VREF = VDD\_MEM / 2



Dummy when 'USE DVO'

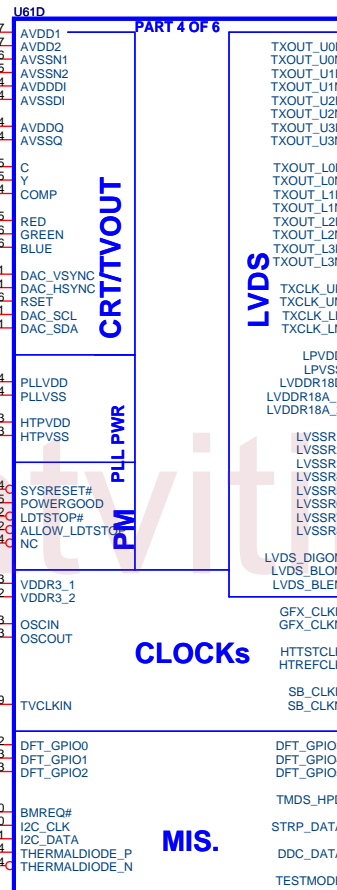
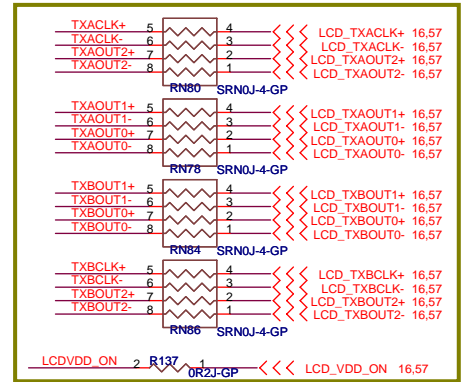
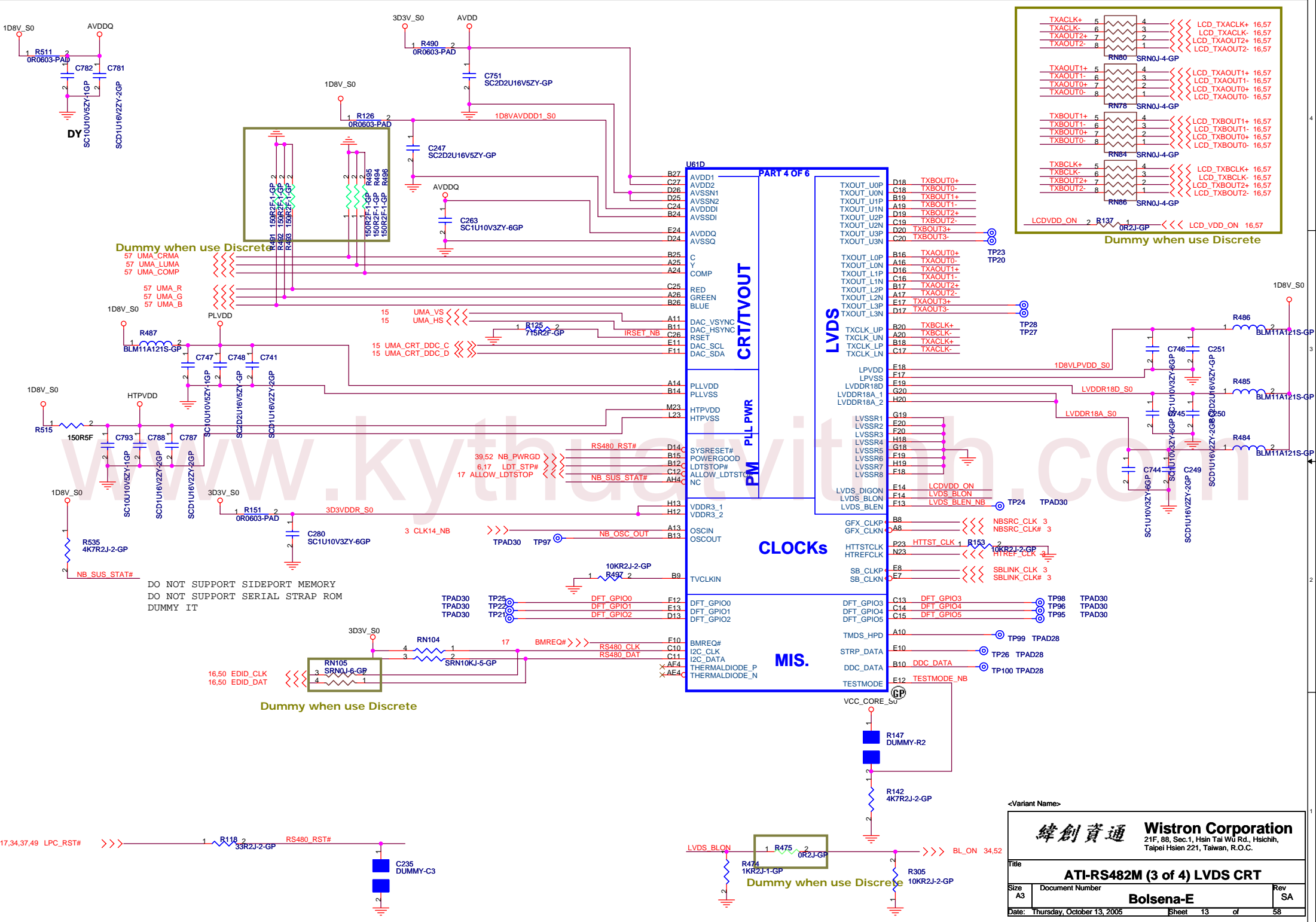
<Variant Name>

**緯創資通 Wistron Corporation**  
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **ATI-RS482M (2 of 4) PCIE**

Size: A3 Document Number: **Bolsena-E** Rev: SA

Date: Thursday, October 13, 2005 Sheet 12 of 58



<Variant Name>

**緯創資通 Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

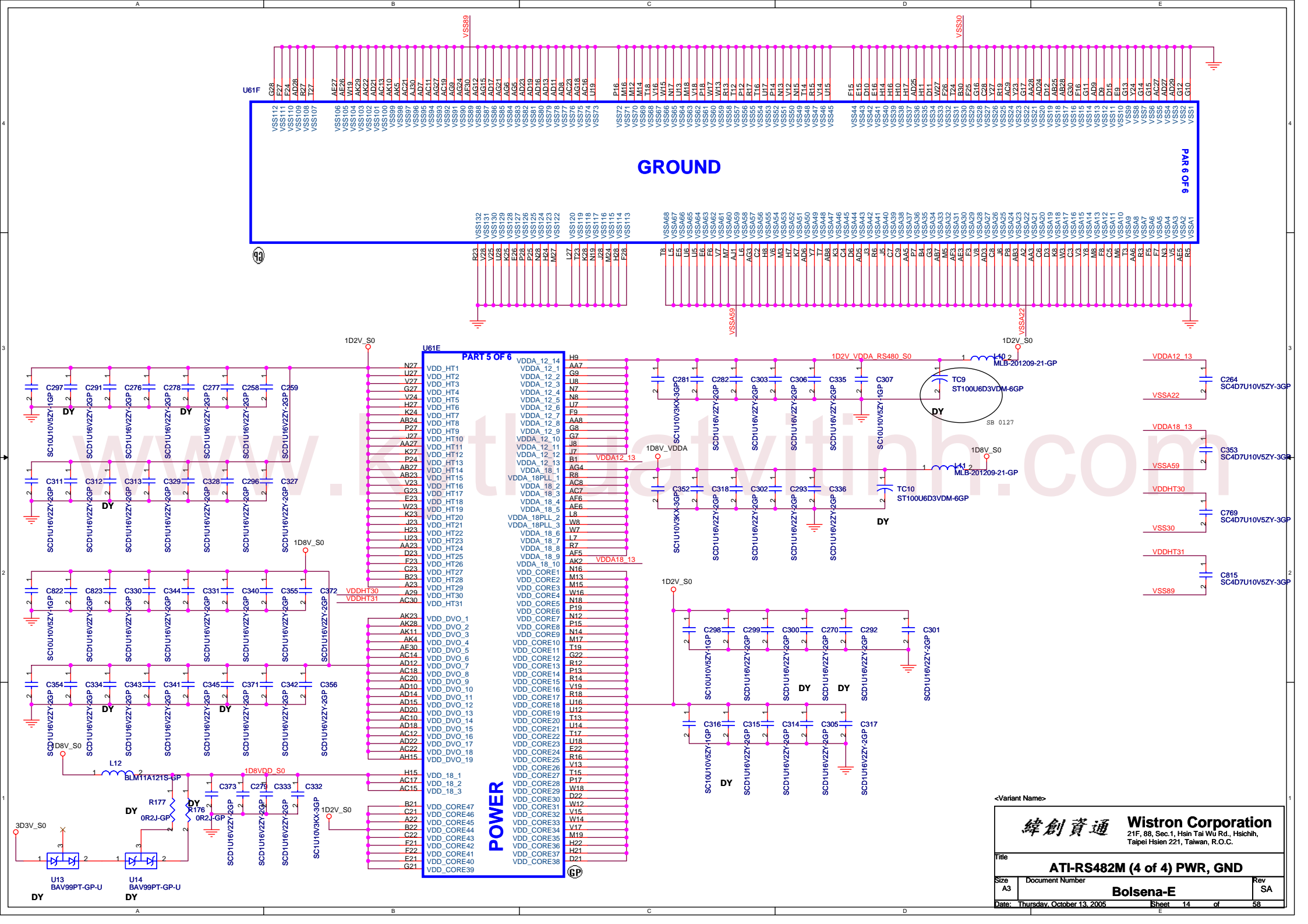
**ATI-RS482M (3 of 4) LVDS CRT**

Title	Document Number	Rev
Size	A3	SA
<b>Bolsena-E</b>		
Date: Thursday, October 13, 2005	Sheet 13 of 58	

DO NOT SUPPORT SIDEPORT MEMORY  
 DO NOT SUPPORT SERIAL STRAP ROM  
 DUMMY IT

**Dummy when use Discrete**

**Dummy when use Discrete**



**GROUND**

**POWER**

Wistron Corporation  
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

ATI-RS482M (4 of 4) PWR, GND

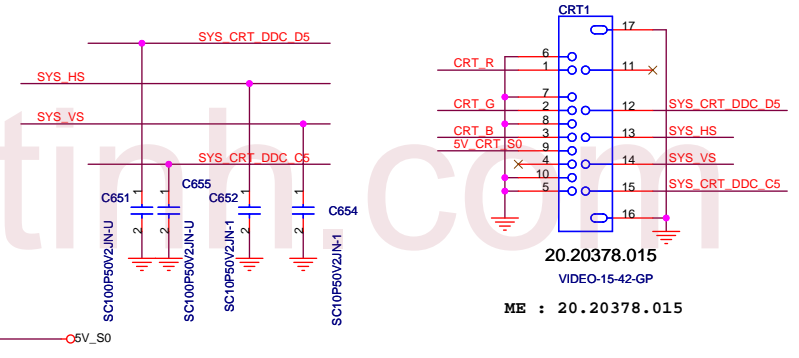
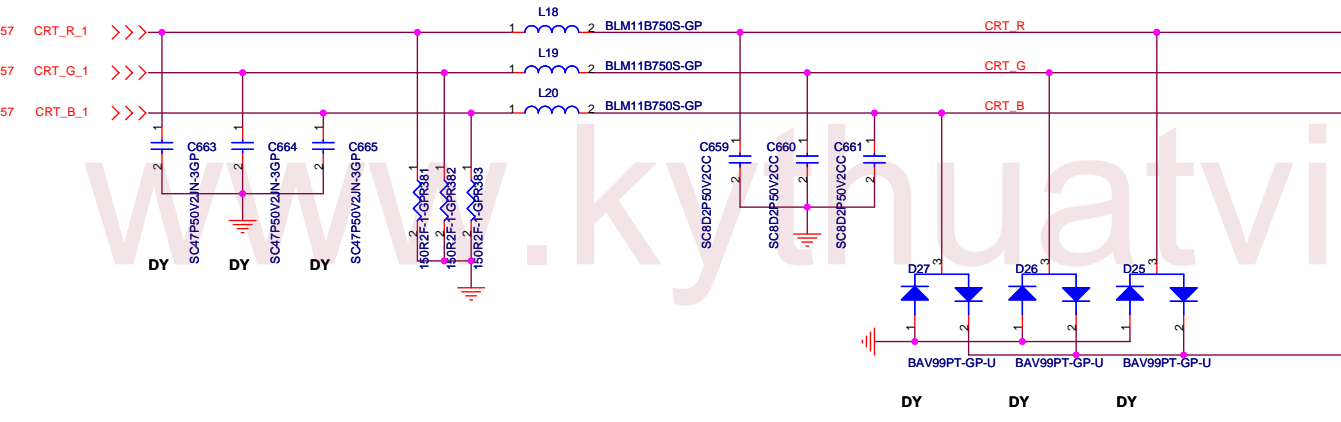
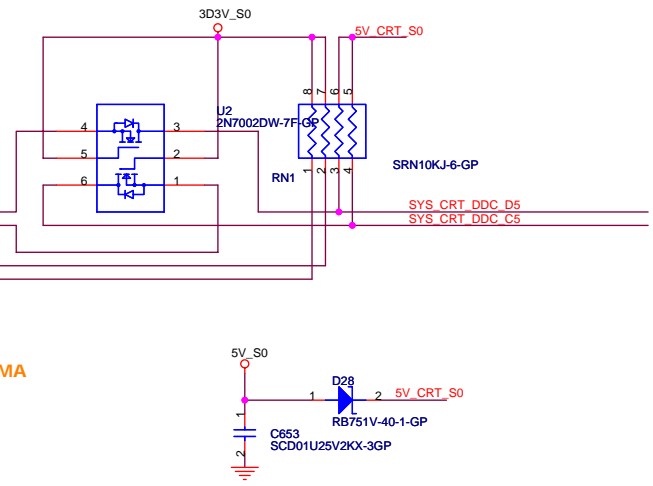
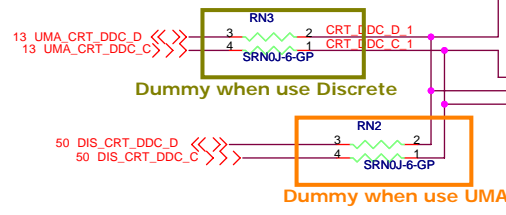
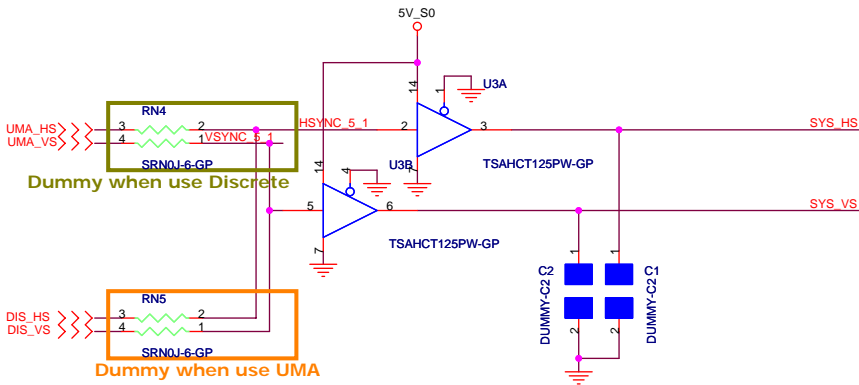
Bolsena-E

Document Number: SA  
 Date: Thursday, October 13, 2005

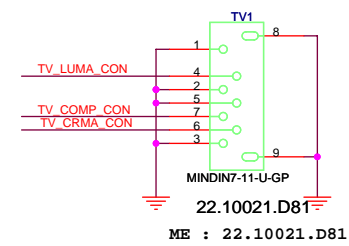
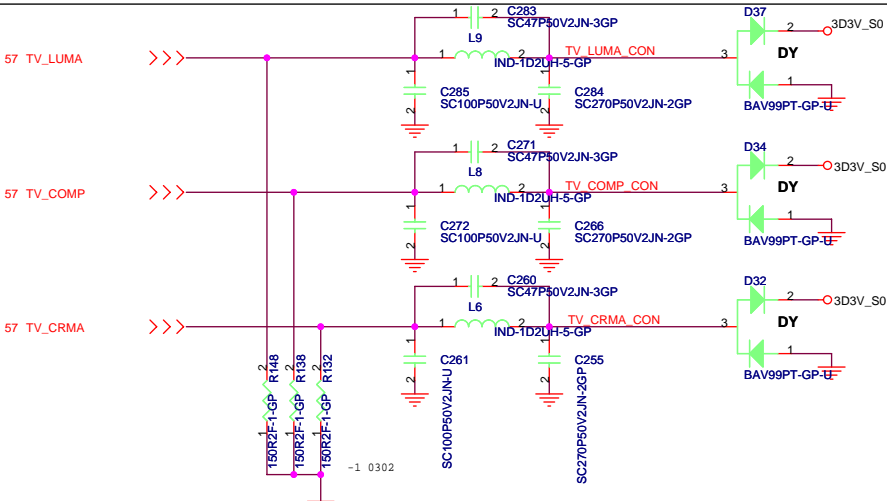


# CRT CONN

200mA Rating/Spec 500mA

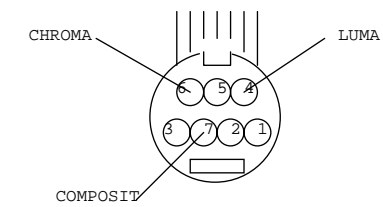


20.20378.015  
VIDEO-15-42-GP  
ME : 20.20378.015



22.10021.D81  
ME : 22.10021.D81

# TV CONN



<Variant Name>

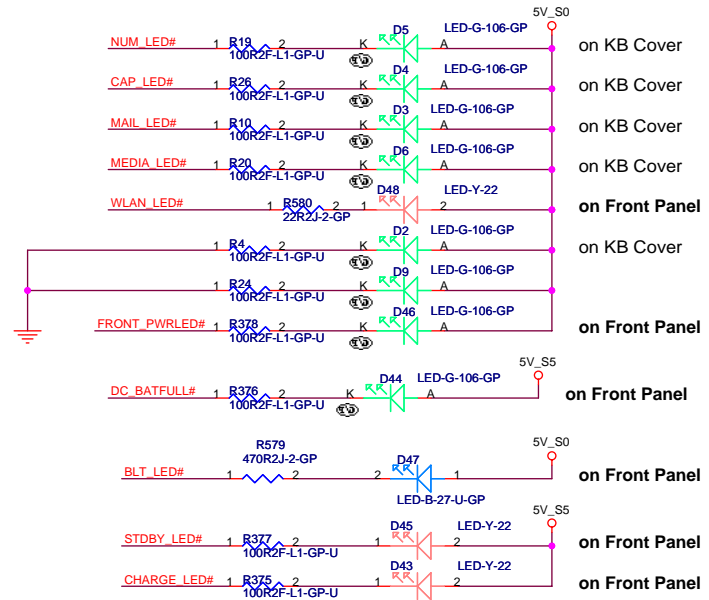
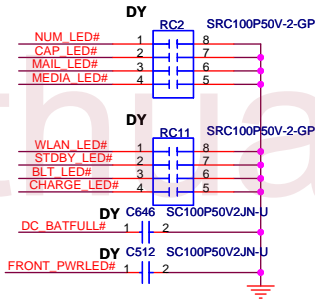
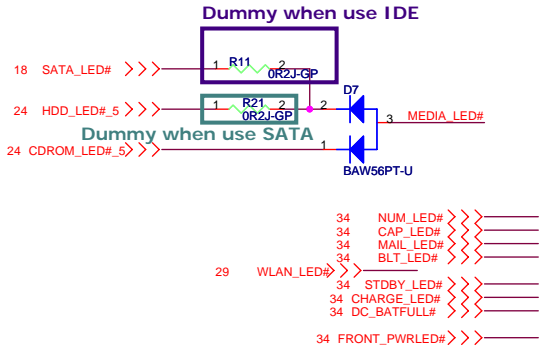
**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **CRT/TV**

Size A3	Document Number	Rev SA
	<b>Bolsena-E</b>	

Date: Thursday, October 13, 2005 Sheet 15 of 58

# LEDs



on KB cover

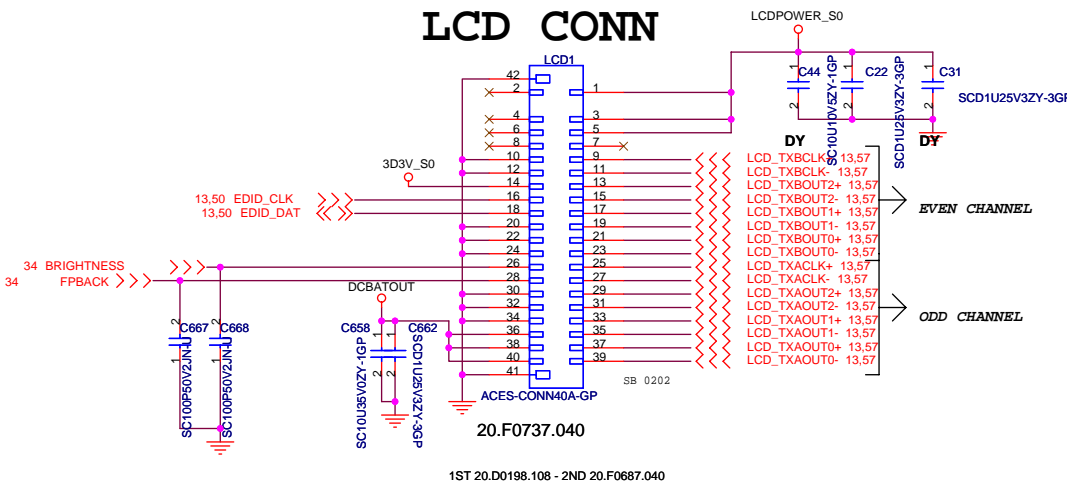
LED	V	V	V	V	V	V	V	V
Button	V	V	V	V	V	V	V	V
	POWER1	E-MAIL	INTERNET	e-BTN	PROGRAM	CAPS	NUM	HDD

Front panel

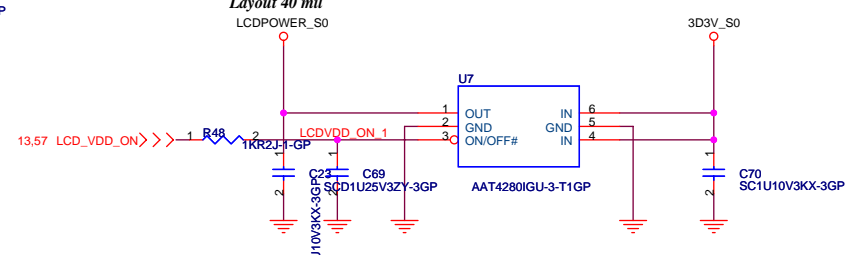
LED	V	V	V	V	Charger:	Power2:
Button	V	V	V	V	Green : DC only with Battery full with DC	Green : S0
					Orange : Charging	Orange : S3
					Orange Blink : Battery low	Orange Blinking : Enter S4

(Please See M.E. drawing LED position)

# LCD CONN



# LCD POWER



<Variant Name>

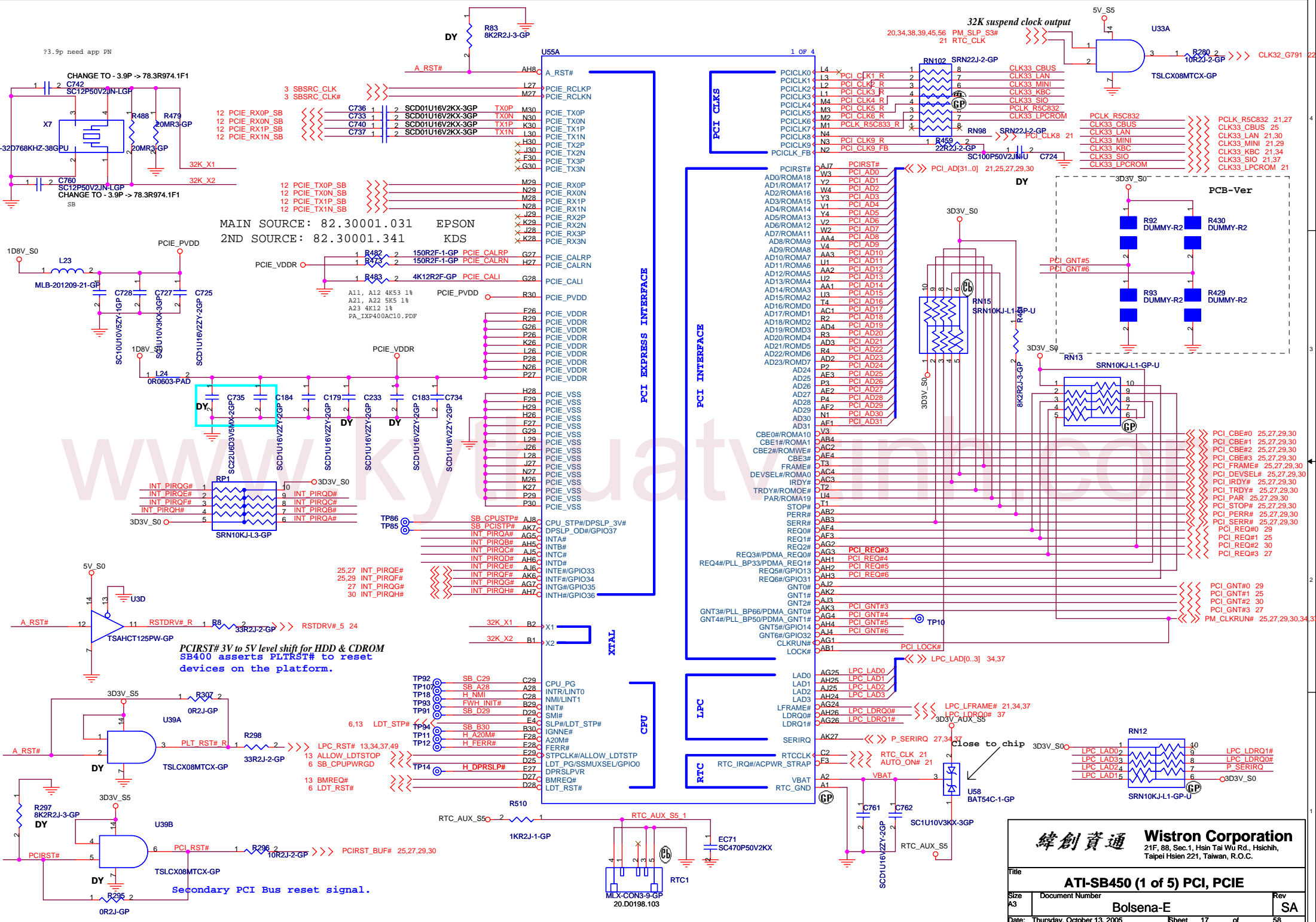
**緯創資通 Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **LCD / LEDs**

Size A3 Document Number: **Bolsena-E** Rev SA

Date: Thursday, October 13, 2005 Sheet 16 of 58

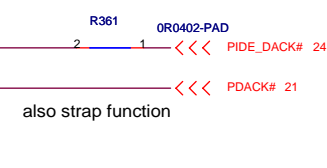
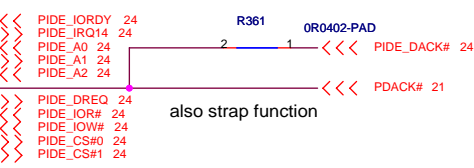
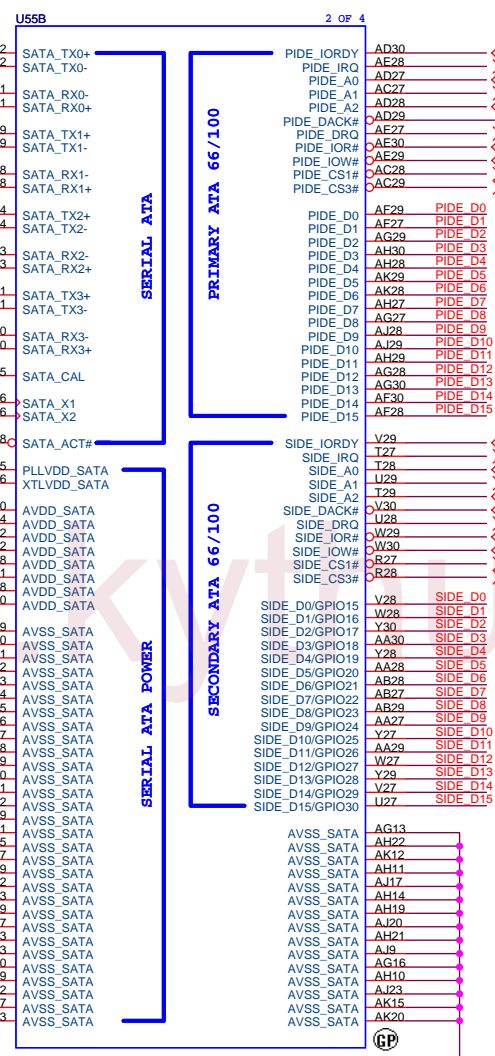
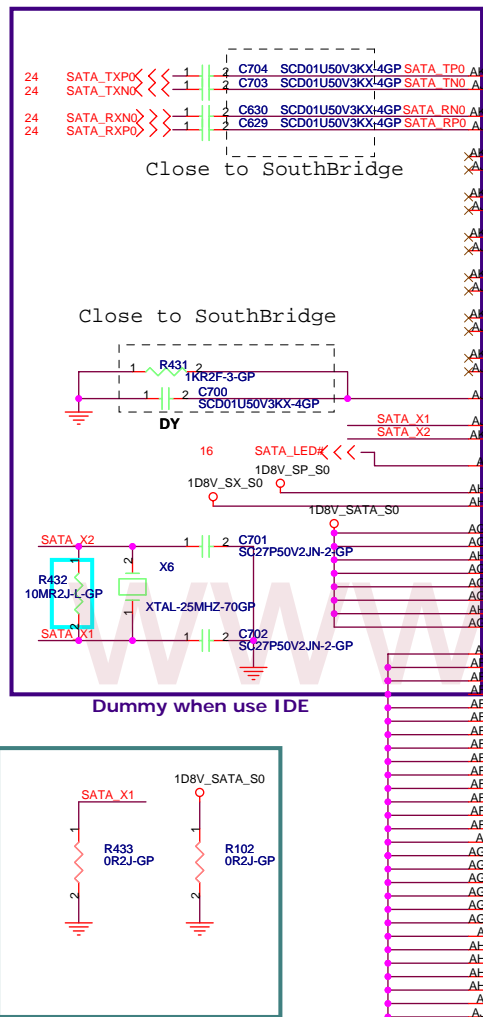


MAIN SOURCE: 82.30001.031 EPSON  
 2ND SOURCE: 82.30001.341 KDS

**PCIRST# 3V to 5V level shift for HDD & CDROM**  
 SB40 asserts FLTRST# to reset devices on the platform.

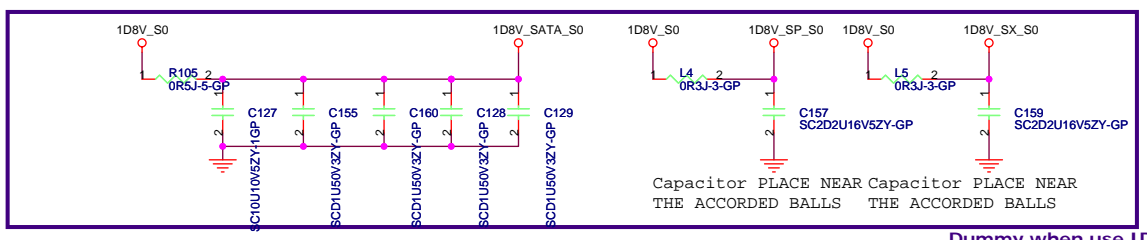
Secondary PCI Bus reset signal.

		<b>Wistron Corporation</b> 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
<b>ATI-SB450 (1 of 5) PCI, PCIE</b>		
Title Size A3 Date: Thursday, October 13, 2005	Document Number <b>Bolsena-E</b> Sheet 17 of 58	Rev <b>SA</b>



PIIDE\_D[15..0] 24

SIDE\_D[15..0] 24



Capacitor PLACE NEAR THE ACCORDED BALLS Capacitor PLACE NEAR THE ACCORDED BALLS

Dummy when use IDE

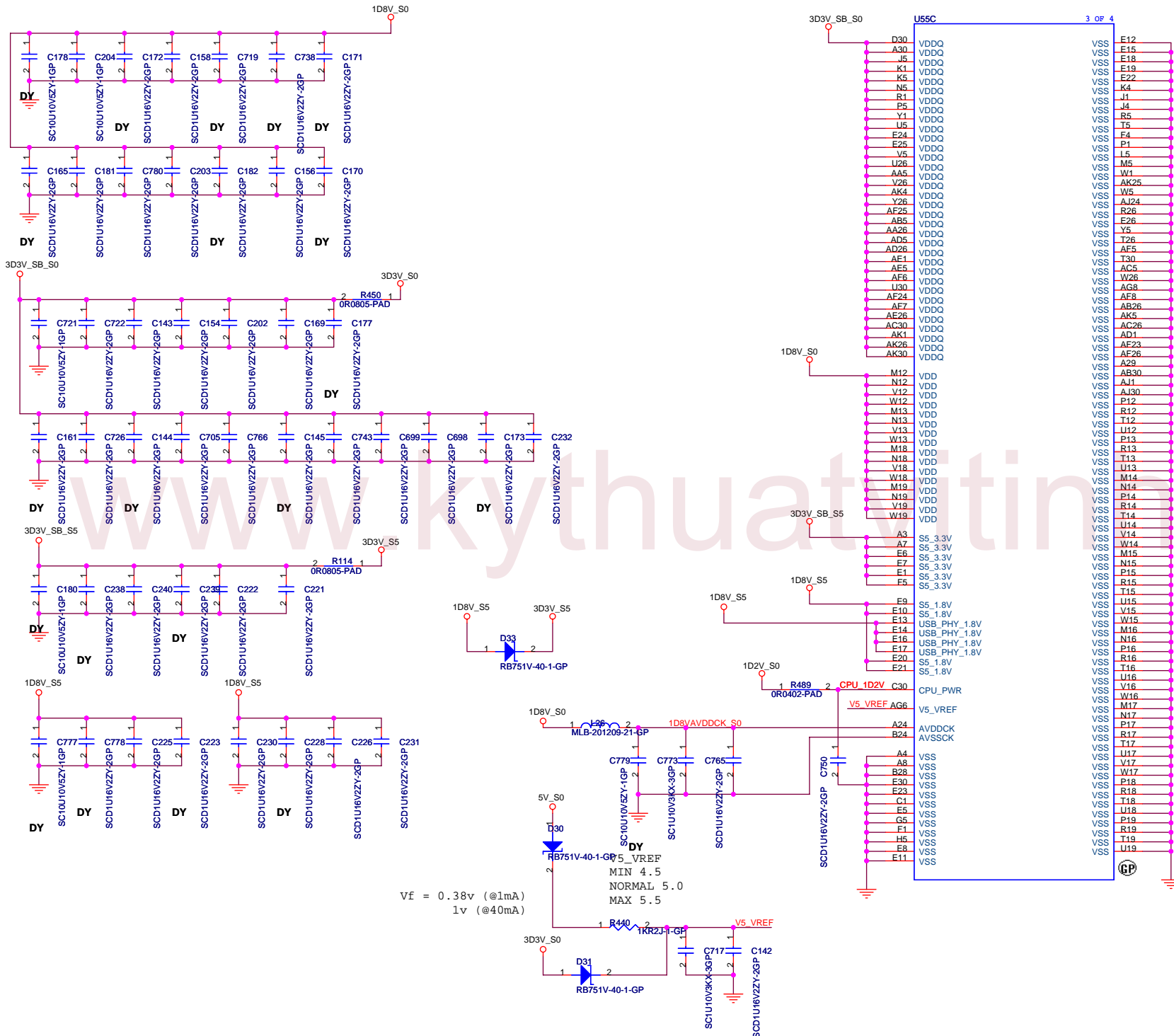
<Variant Name>

**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **ATI-SB400 (2 of 5) IDE**

Size A3 Document Number: **Bolsena-E** Rev: **SA**

Date: Thursday, October 13, 2005 Sheet 18 of 58

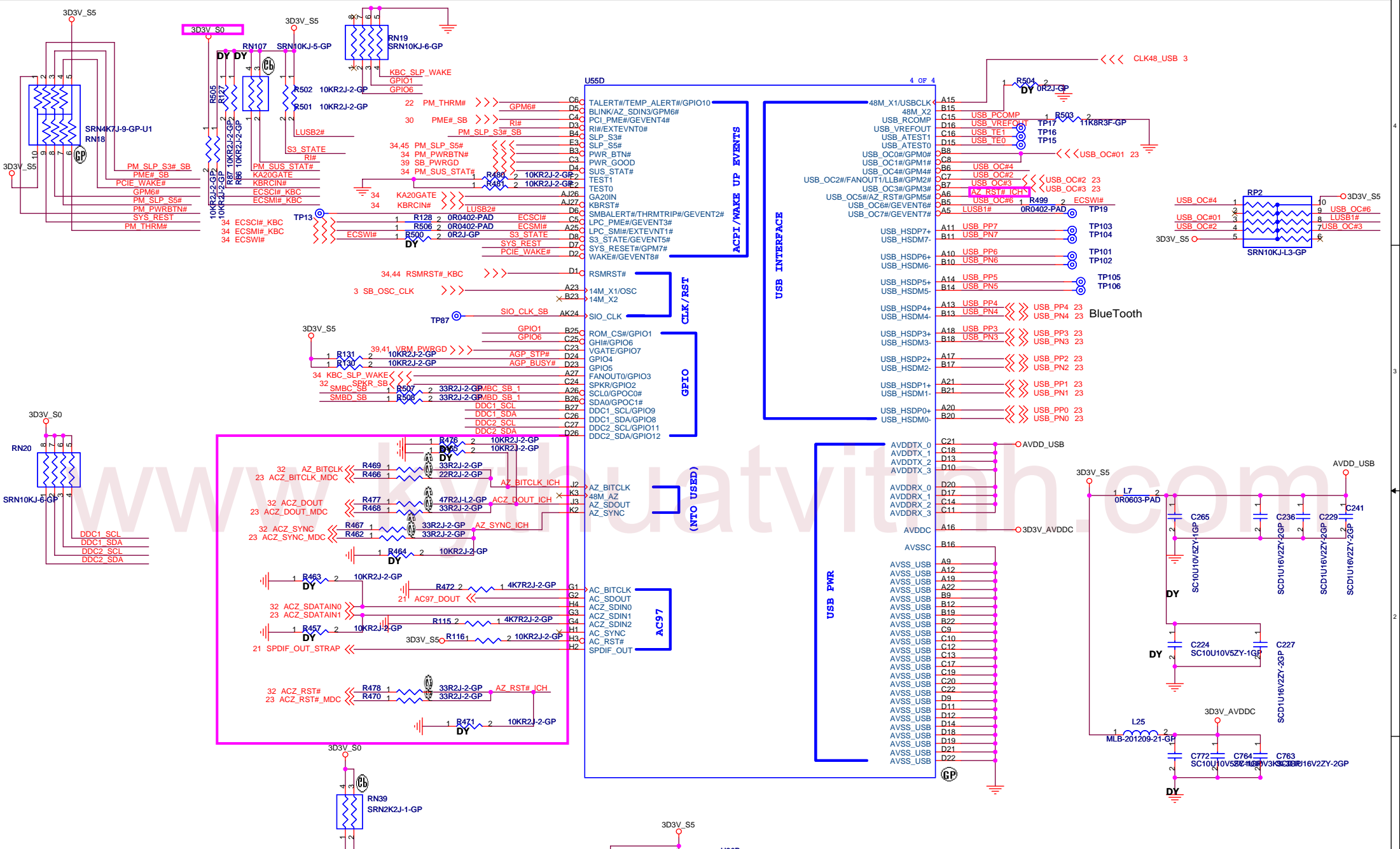


-<Variant Name->

**緯創資通**   **Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title: **ATI-SB400 (3 of 5) POWER**

Size A3	Document Number	Rev SA
<b>Bolsena-E</b>		
Date: Thursday, October 13, 2005 Sheet 19 of 58		



3.8 SMBC\_SB <>>> SMBC\_SB

3.8 SMBD\_SB <>>> SMBD\_SB

U30B

7LSLCX08MTCX-GP

PM\_SLP\_S3# SB <>>> PM\_SLP\_S3# 17,34,38,39,45,56

<Variant Name>

**緯創資通 Wistron Corporation**

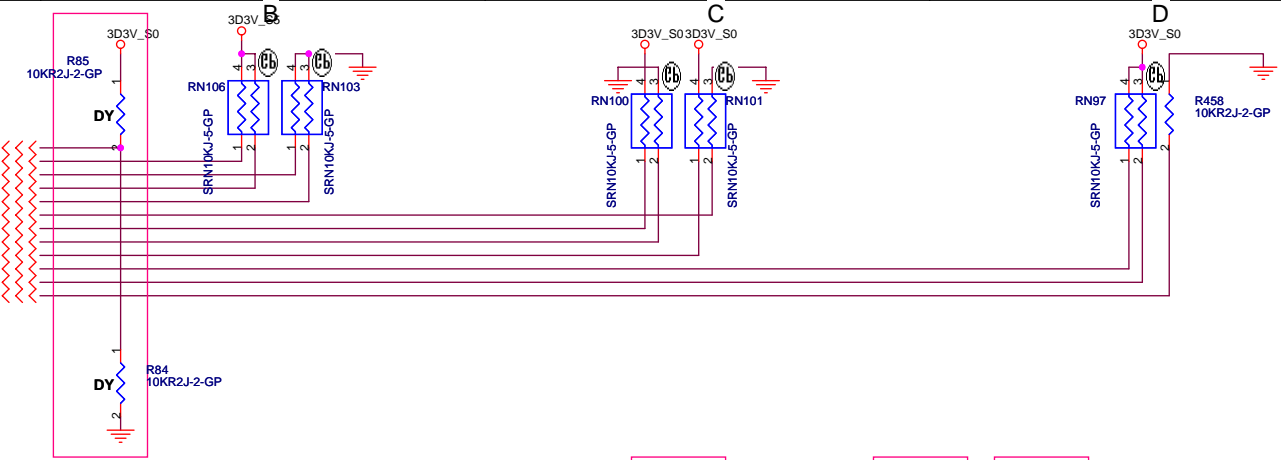
21F, 8B, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **ATI-SB450 (4 of 5) USB GPIO**

Size A3	Document Number	Rev SA
<b>Bolsena-E</b>		
Date: Thursday, October 13, 2005		Sheet 20 of 58



- 17,34,37 LPC\_LFRAME#
- 17 AUTO\_ON#
- 20 AC97\_DOUT
- 17 RTC\_CLK
- 20 SPDIF\_OUT\_STRAP
- 17,30 CLK33\_LAN
- 17,29 CLK33\_MINI
- 17,34 CLK33\_KBC
- 17,37 CLK33\_SIO
- 17 CLK33\_LPCROM
- 17,27 PCLK\_R5C832
- 17 PCI\_CLK8

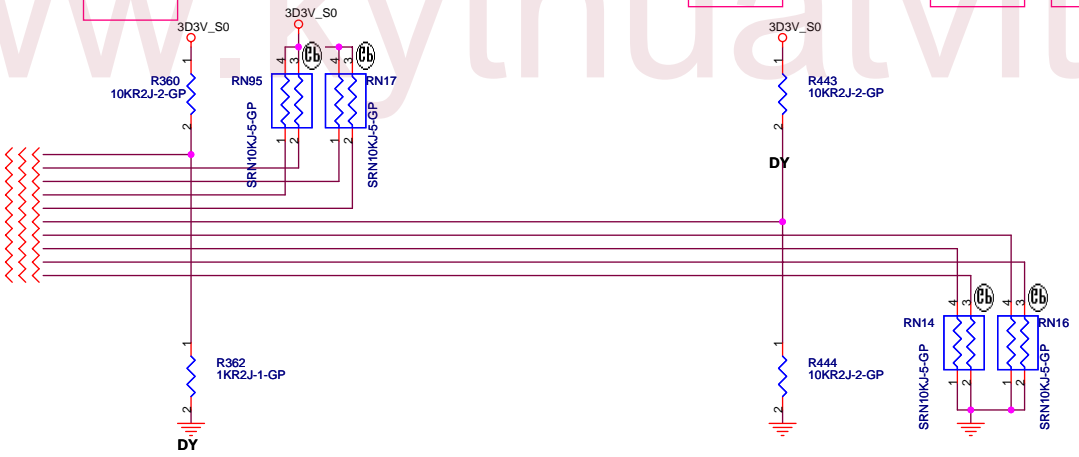


Place these R close to SouthBridge if possible

**REQUIRED SYSTEM STRAPS**

	LFRAME#	ACPWRON	AC_SDOUT	RTC_CLK	SPDIF_OUT	PCI_CLK2 (CLK33_LAN)	PCI_CLK3 (CLK33_MINI)	PCI_CLK4 (CLK33_KBC)	PCI_CLK5 (CLK33_SIO)	PCI_CLK6 (CLK33_LPCROM)	PCI_CLK7 (PCLK_R5C832)	PCI_CLK8
STRAP HIGH	Thermal Trip is not enable as default Optional	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	SIO 24MHz	48MHZ -Crystal Pad DEFAULT	USB PHY PWRDOWN DISABLE DEFAULT	USB INT PLL48	PCIE_CM_SET HIGH DEFAULT	CPU I/F=K8 DEFAULT	ROM TYPE H,H=PCI (X Bus) ROM H,L=LPC ROM I	
STRAP LOW	Thermal Trip is enable as default Optional	AUTO PWR ON	IGNORE DEBUG STRAPS DEFAULT	EXTENNAL RTC (NOT SUPPORTED W/IT8712)	SIO 48MHz DEFAULT	48MHZ-Clock Input Buffer DEFAULT	USB PHY PWRDOWN ENABLE	USB EXT. 48MHZ Use External only	PCIE_CM_SET LOW	CPU I/F=P4	L,H=LPC ROM II L,L=Firmware Hub ROM	

- 18 PDACK#
- 17,25,27,29,30 PCI\_AD31
- 17,25,27,29,30 PCI\_AD30
- 17,25,27,29,30 PCI\_AD29
- 17,25,27,29,30 PCI\_AD28
- 17,25,27,29,30 PCI\_AD27
- 17,25,27,29,30 PCI\_AD26
- 17,25,27,29,30 PCI\_AD25
- 17,25,27,29,30 PCI\_AD24
- 17,25,27,29,30 PCI\_AD23



**DEBUG STRAPS**

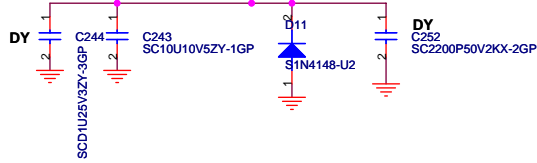
	PDACK#	PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
STRAP HIGH	USE LONG RESET DEFAULT	RESERVED	RESERVED	RESERVED	RESERVED	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	RESERVED
STRAP LOW	USE SHORT RESET					USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	

Variant Name: **ATI-SB400 STRAPPING(5 of 5)**

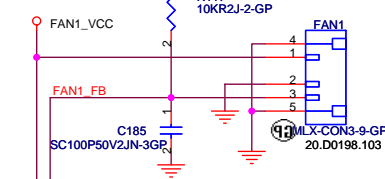
**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Date: Thursday, October 13, 2005 Sheet 21 of 58

\*Layout\* 15 mil

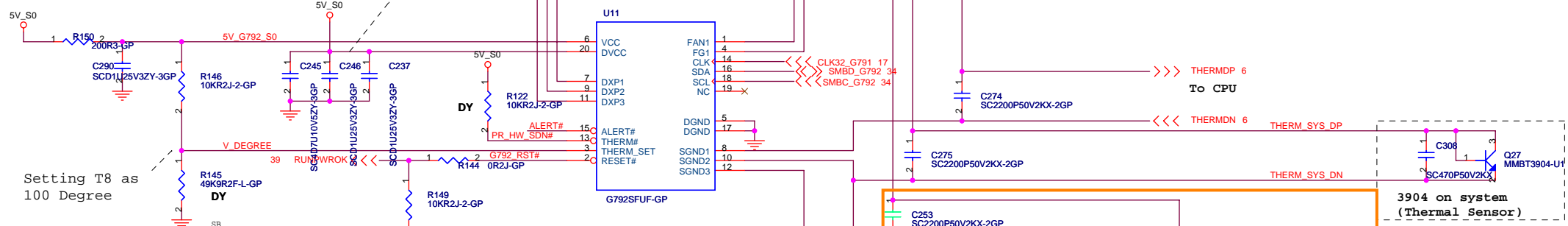


\*Layout\* 15 mil



ME : 20.D0198.103  
2nd: 20.F0714.003

\*Layout\* 30 mil



Setting T8 as 100 Degree

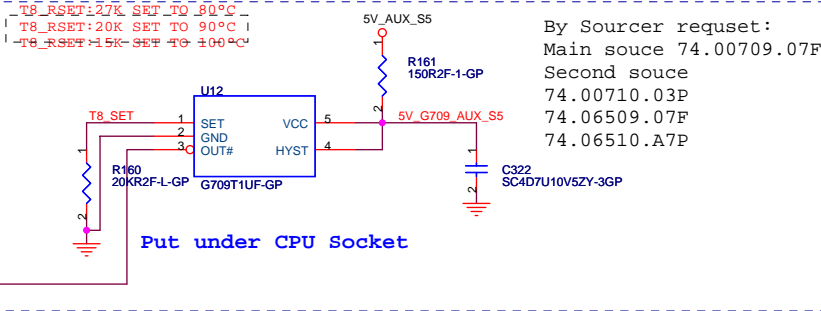
V\_DEGREE  
= ((Degree-72)\*0.02)+0.34)\*VCC  
HW thermal shut down temperature setting 95 degree . Put Near CPU .

DXP1: 108 Degree  
DXP2: H/W Setting  
DXP3: 88 Degree

3904 on system (Thermal Sensor)

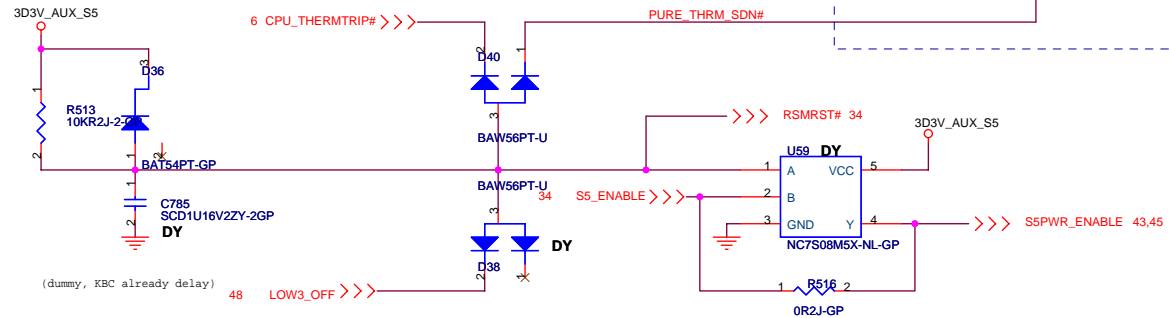
Dummy when G792 enhanced T8 function

Dummy when use UMA



By Sourcer request:  
Main souce 74.00709.07P  
Second souce 74.00710.03P  
74.06509.07P  
74.06510.A7P

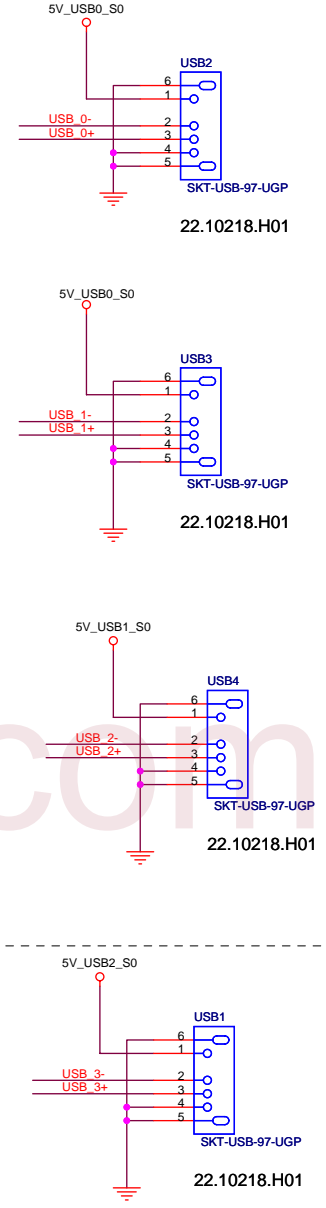
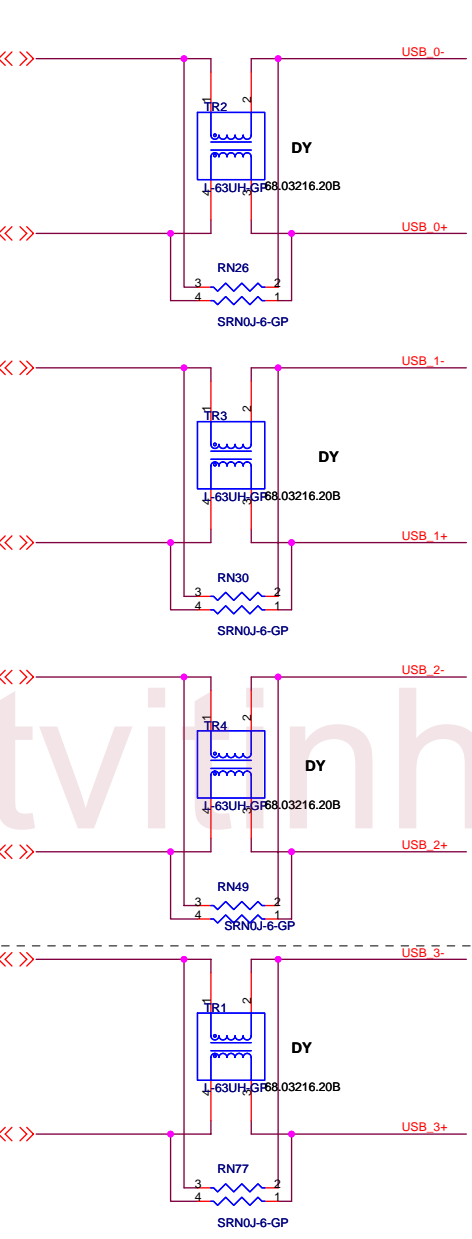
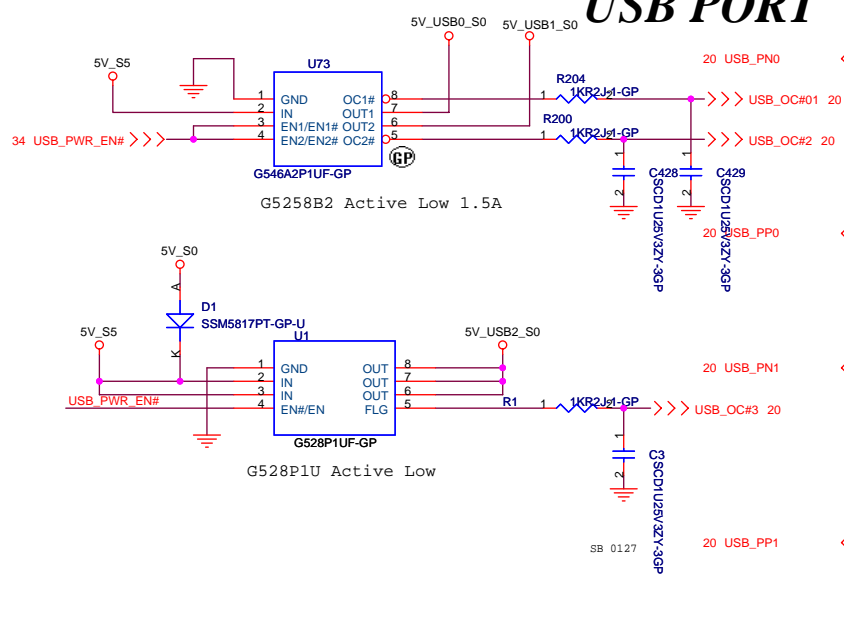
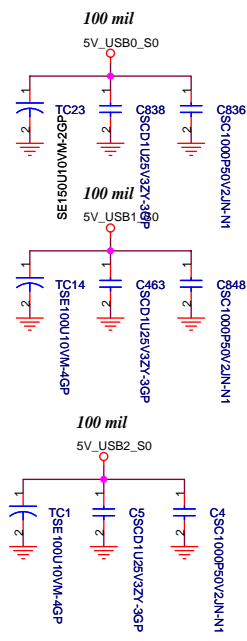
Put under CPU Socket



(dummy, KBC already delay)

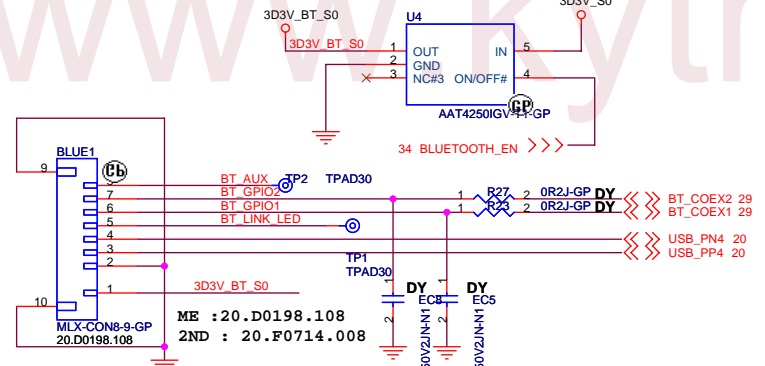
<p>&lt;Variant Name&gt;</p> <p><b>緯創資通 Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</p>		
<p>Title</p> <p><b>THERMAL G792</b></p>		
Size	Document Number	Rev
Custom	Bolsena-E	SA
Date: Thursday, October 13, 2005	Sheet 22 of 58	

# USB PORT

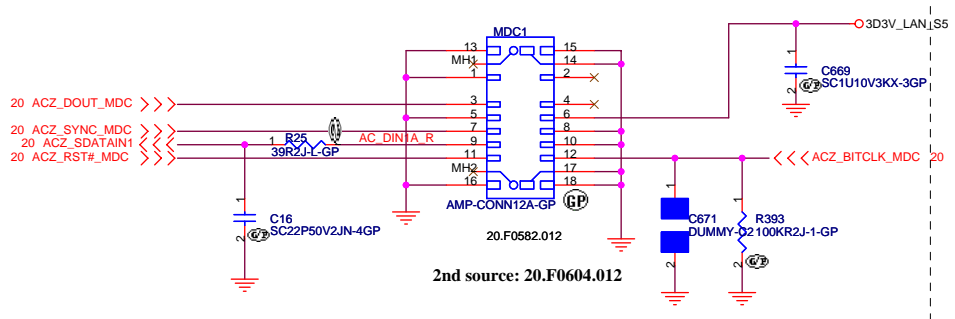


ME : 22.10218.H01  
2ND : 22.10245.H11

## BLUETOOTH MODULE



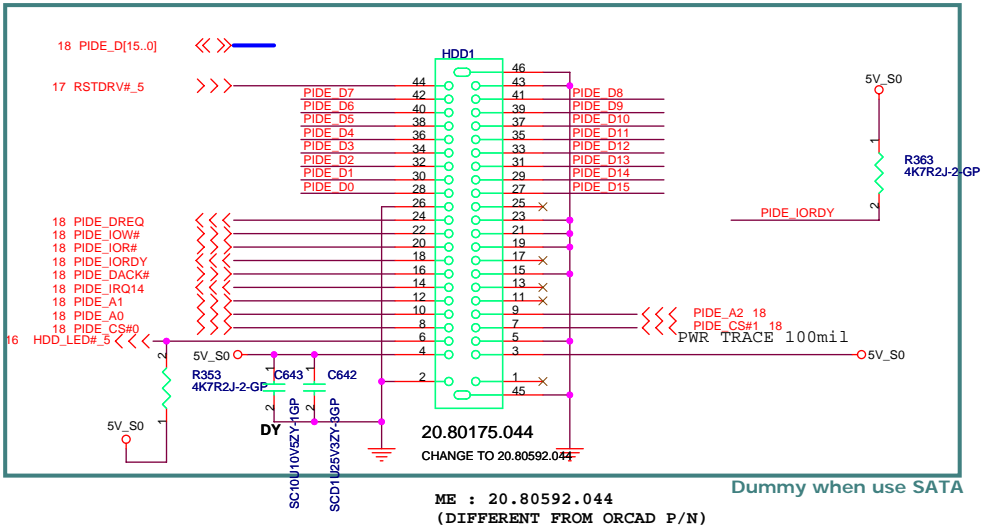
## MDC 1.5 CONN



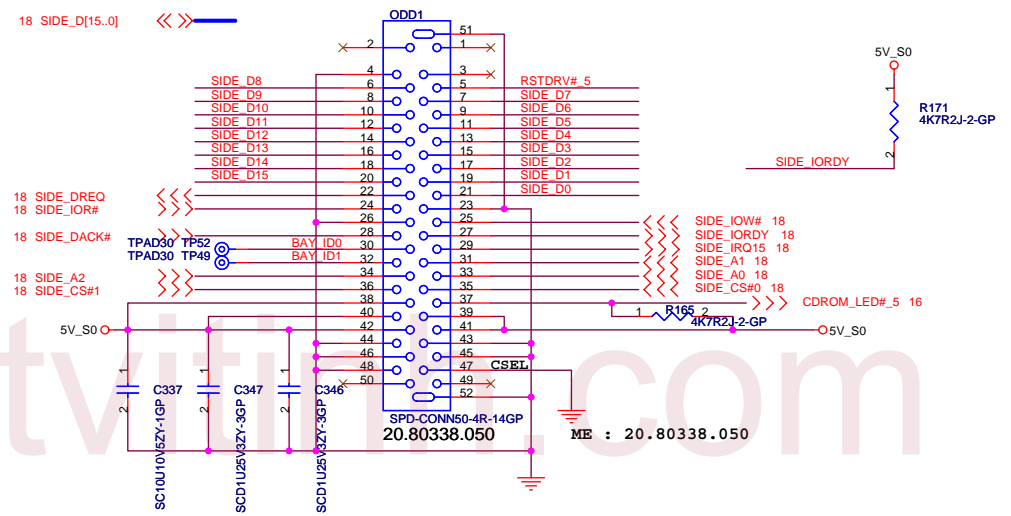
<Variant Name>

<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>USB / MDC / BLUETOOTH</b>			
Title	Document Number	Rev	
A3	<b>Boisena-E</b>	SA	
Date: Thursday, October 13, 2005	Sheet 23	of 58	

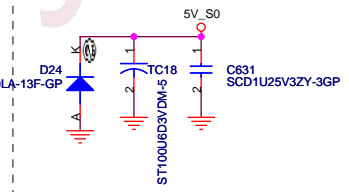
# HDD



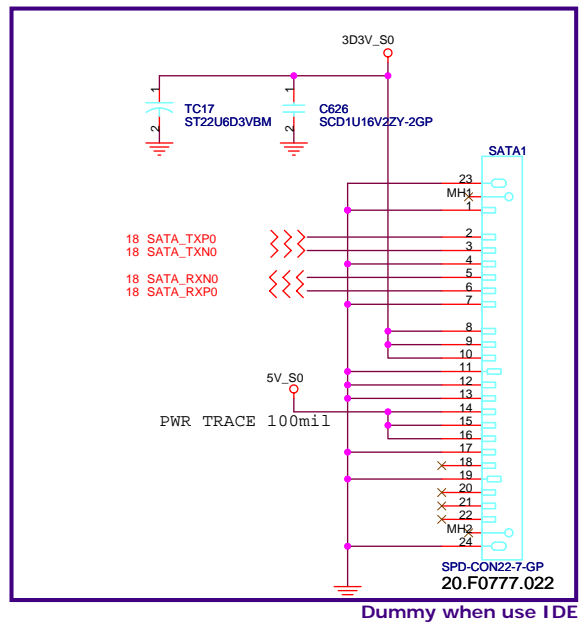
# CDROM



For HDD & SATA both



# SATA Connector



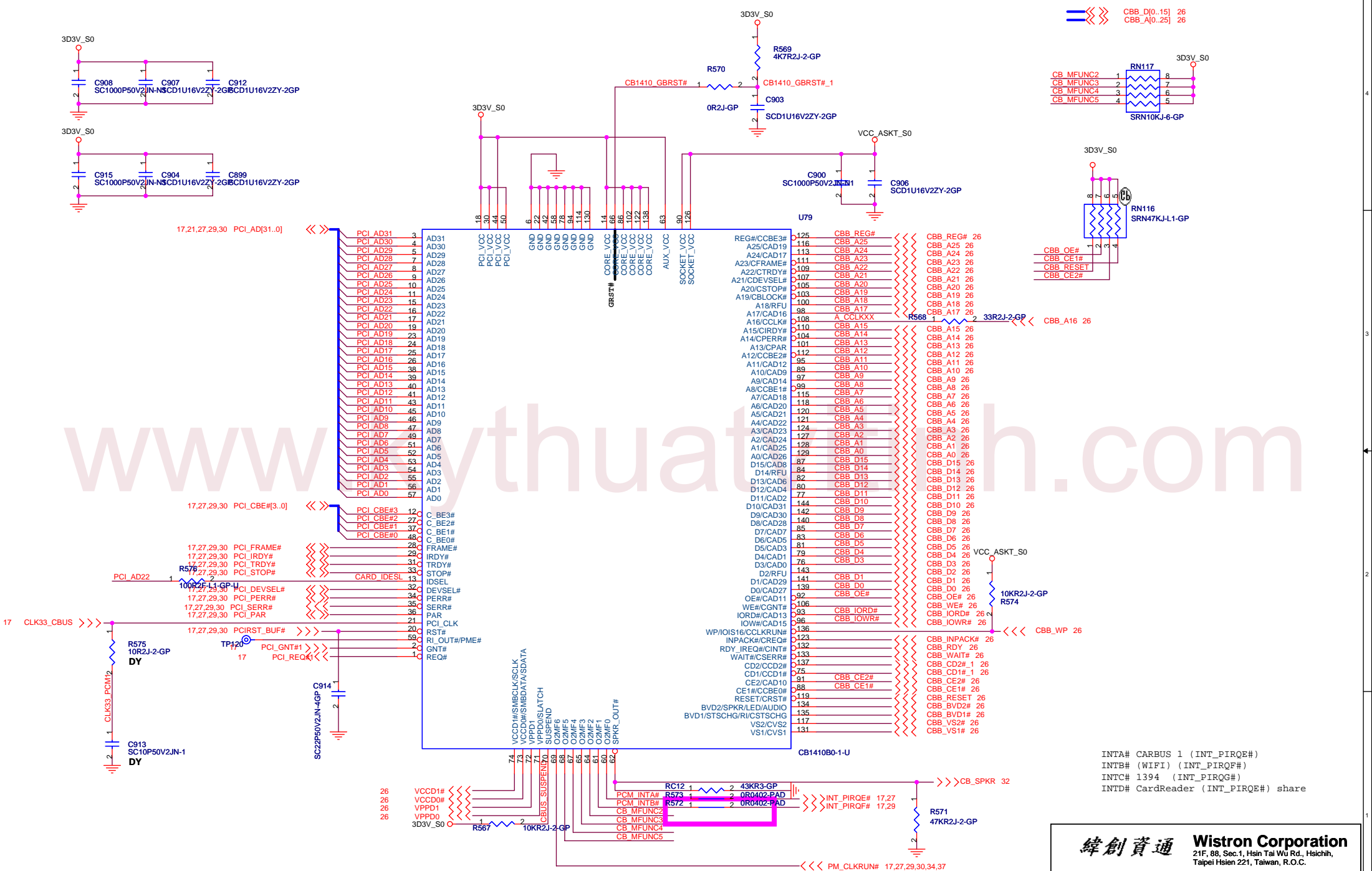
<Variant Name>

**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

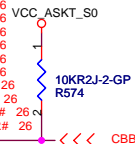
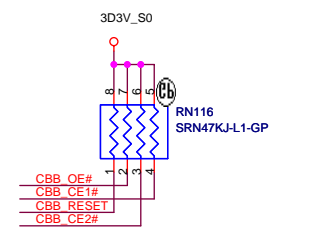
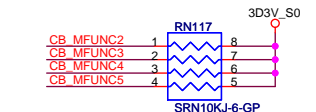
Title: **HDD / CDROM / SATA**

Size: A3 Document Number: **Bolsena-E** Rev: SA

Date: Thursday, October 13, 2005 Sheet 24 of 58



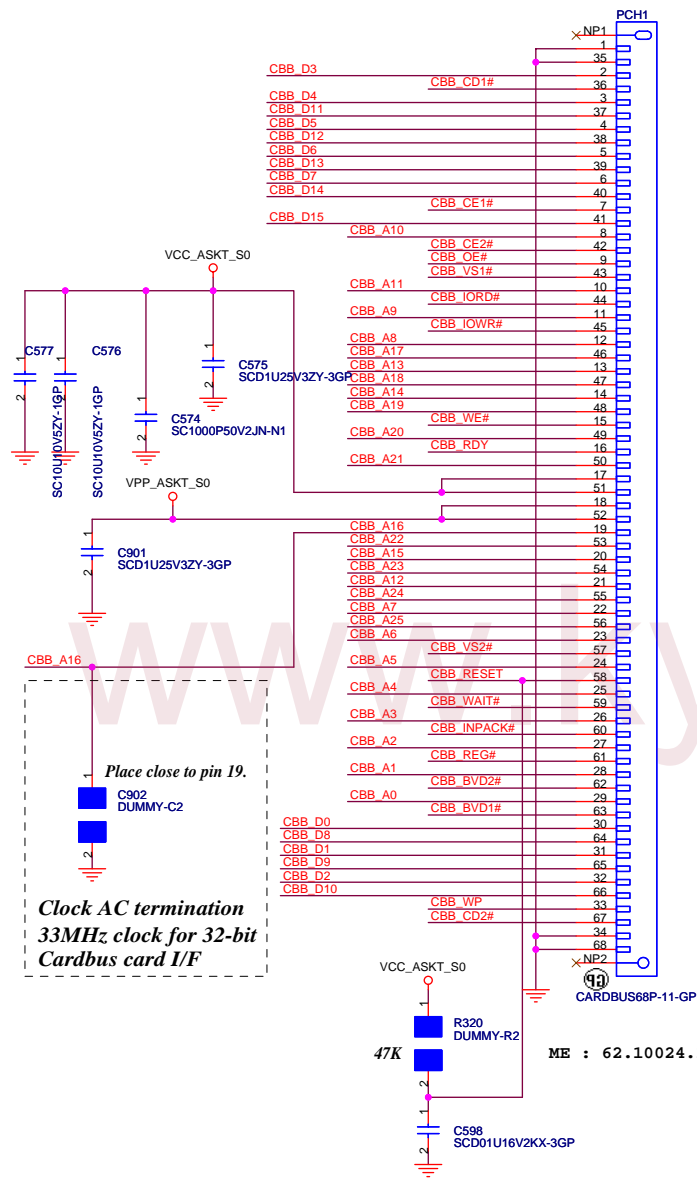
CBB\_D[0..15] 26  
 CBB\_A[0..25] 26



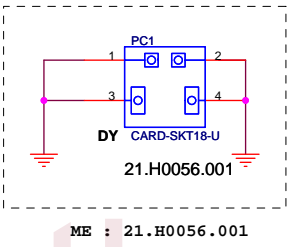
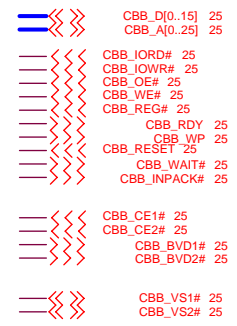
INTA# CARBUS 1 (INT\_PIRQ#)  
 INTB# (WIFI) (INT\_PIRQ#)  
 INTC# 1394 (INT\_PIRQ#)  
 INTD# CardReader (INT\_PIRQ#) share

<b>Wistron Corporation</b> 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>CardBus_ENE CB1410</b>	
Title Size A3 Date: Thursday, October 13, 2005	Document Number <b>Bolsena-E</b> Sheet 25 of 58
Rev <b>SA</b>	

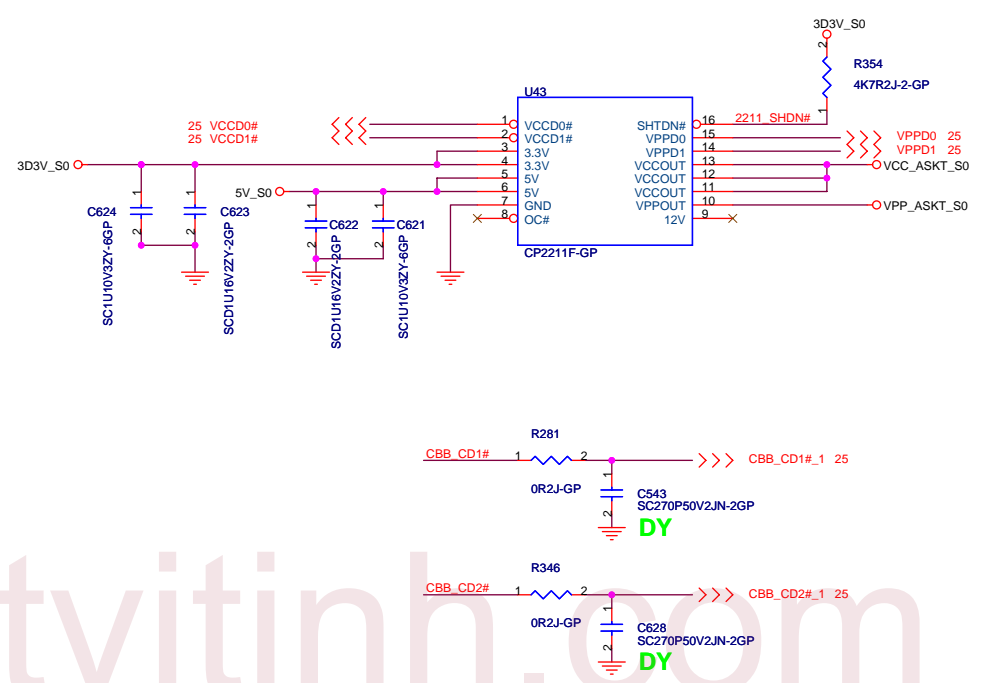
# PCMCIA Socket



# Cardbus I/F



# Power switch



Clock AC termination  
33MHz clock for 32-bit  
Cardbus card I/F

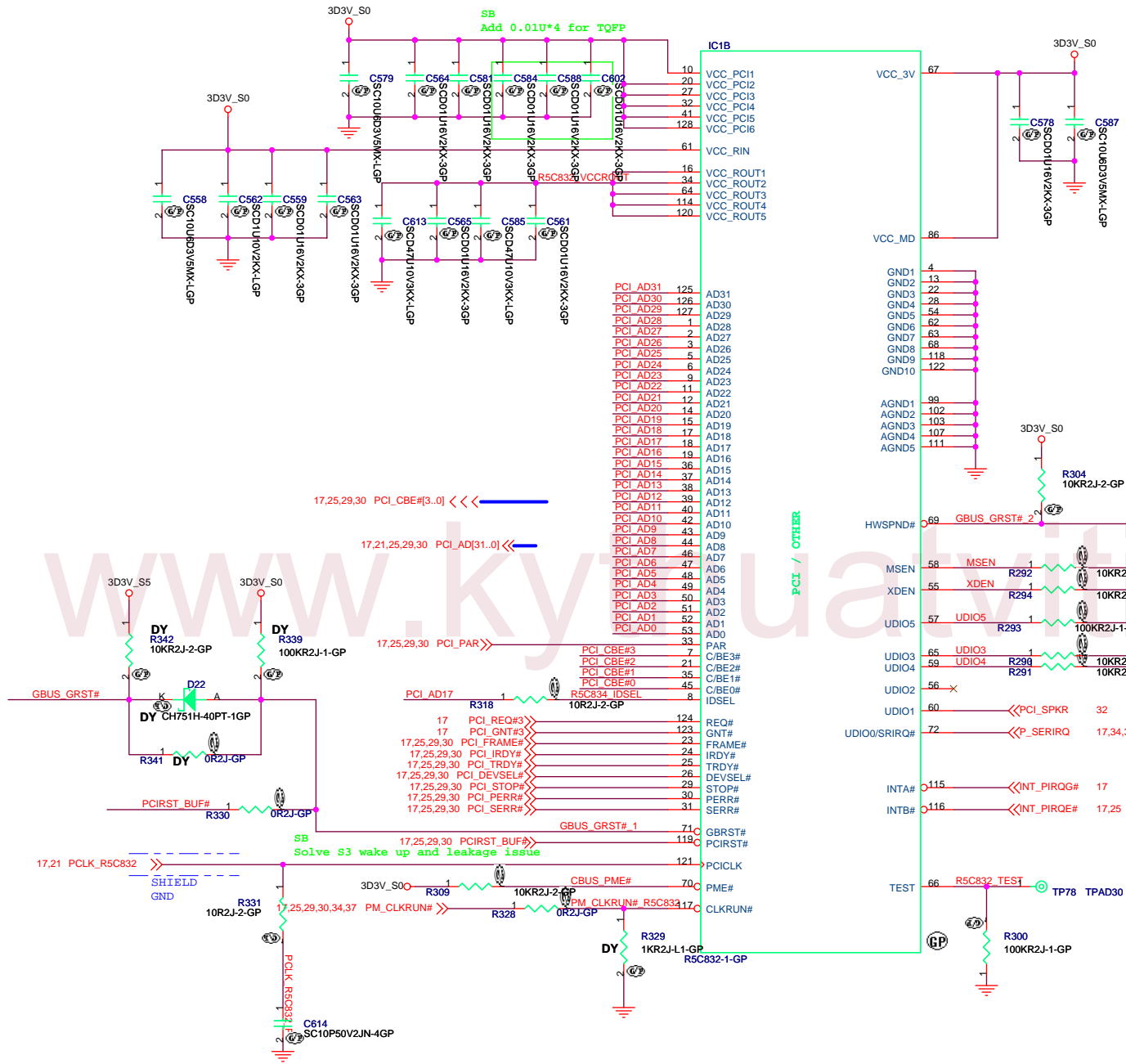
<Variant Name>

**緯創資通 Wistron Corporation**  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCMCIA / 1394 / CARD READER**

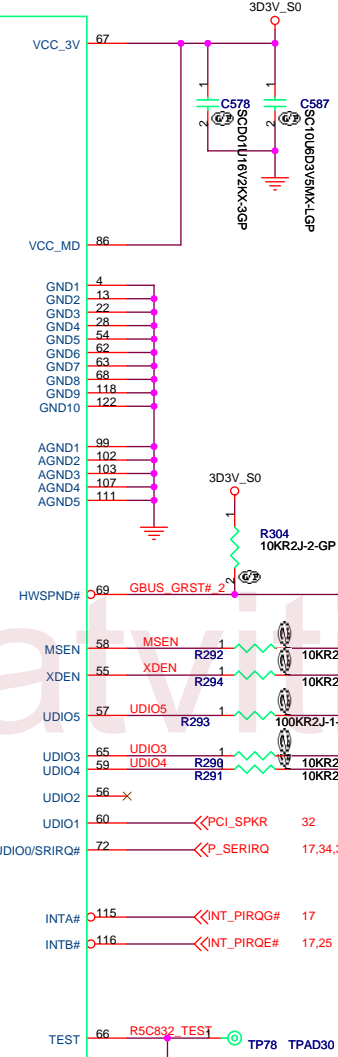
Size: A3	Document Number: <b>Bolsena-E</b>	Rev: SA
Date: Thursday, October 13, 2005	Sheet: 26 of 58	





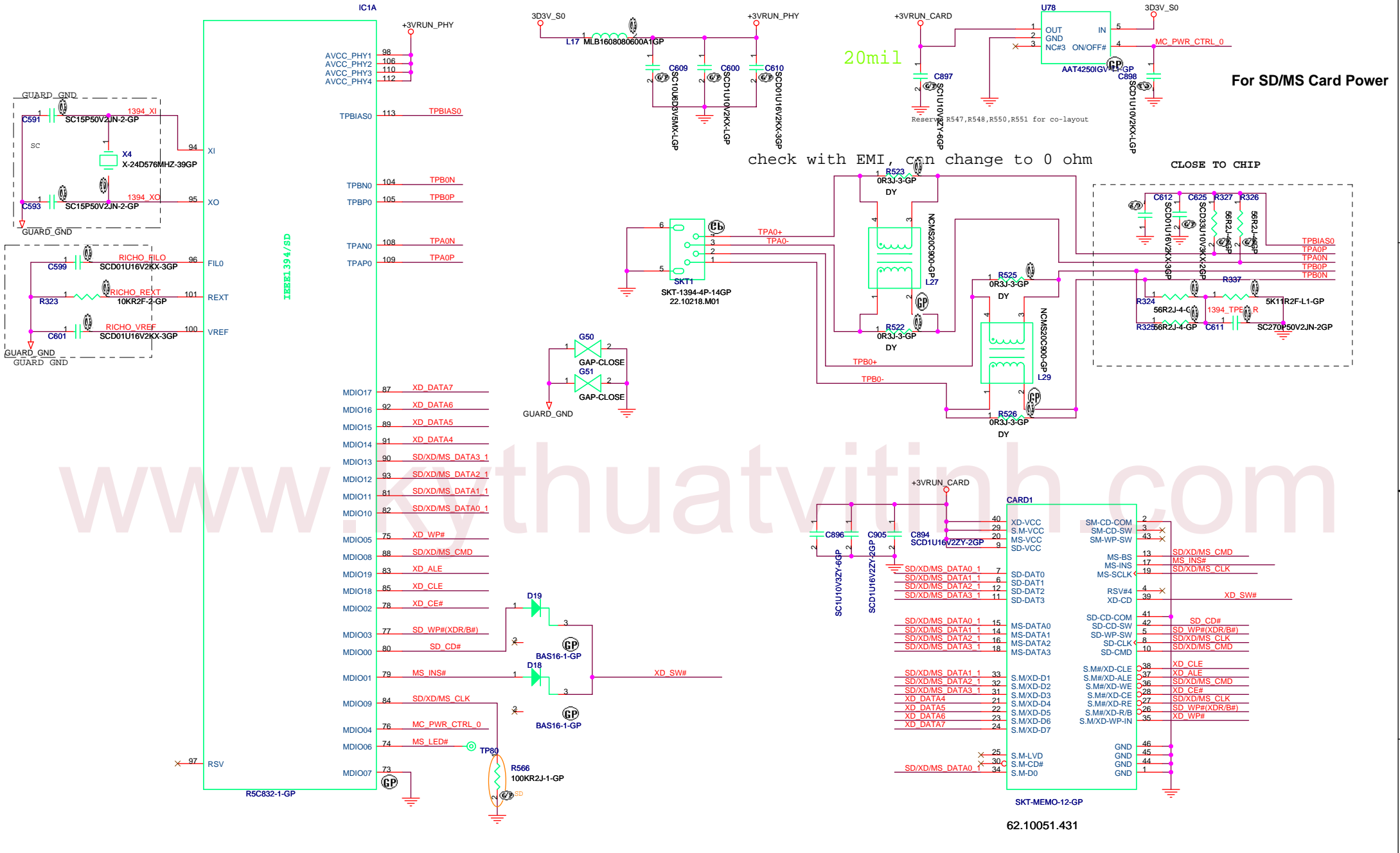
PCI / OTHER

IC1B	10	VCC_PC1
	20	VCC_PC2
	27	VCC_PC3
	32	VCC_PC4
	41	VCC_PC5
	128	VCC_PC6
	61	VCC_RIN
	16	VCC_ROUT1
	34	VCC_ROUT2
	64	VCC_ROUT3
	114	VCC_ROUT4
	120	VCC_ROUT5
	125	AD31
	126	AD30
	127	AD29
	1	AD28
	2	AD27
	3	AD26
	5	AD25
	6	AD24
	9	AD23
	11	AD22
	12	AD21
	14	AD20
	15	AD19
	17	AD18
	18	AD17
	19	AD16
	36	AD15
	37	AD14
	38	AD13
	40	AD12
	41	AD11
	42	AD10
	43	AD9
	44	AD8
	46	AD7
	47	AD6
	48	AD5
	49	AD4
	50	AD3
	51	AD2
	52	AD1
	53	AD0
	33	PAR
	7	CBE#3
	21	CBE#2
	35	CBE#1
	45	CBE#0
	8	IDSEL
	124	REQ#
	123	GNT#
	23	FRAME#
	24	IRDY#
	25	TRDY#
	26	DEVSEL#
	29	STOP#
	30	PERR#
	31	SERR#
	71	GBRST#
	119	PCIRST#
	121	PCICLK
	70	PME#
	17	PM_CLKRUN#
	17	PCI_REQ#3
	17	PCI_GNT#3
	17,25,29,30	PCI_FRAME#
	17,25,29,30	PCI_IRDY#
	17,25,29,30	PCI_TRDY#
	17,25,29,30	PCI_DEVSEL#
	17,25,29,30	PCI_STOP#
	17,25,29,30	PCI_PERR#
	17,25,29,30	PCI_SERR#
	71	GBRST#
	119	PCIRST#
	121	PCICLK
	70	PME#
	17	PM_CLKRUN#



1394 : INTA#  
 7in1 : INTB#(INT\_PIRQE#)share

<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>R5C832 1394 7IN1(2/2)</b>	
Title	Rev
Size A3	SA
Document Number	
<b>Bolsena-E</b>	
Date: Thursday, October 13, 2005	Sheet 27 of 58



20mil

check with EMI, can change to 0 ohm

For SD/MS Card Power

CLOSE TO CHIP

www.thuathvith.com

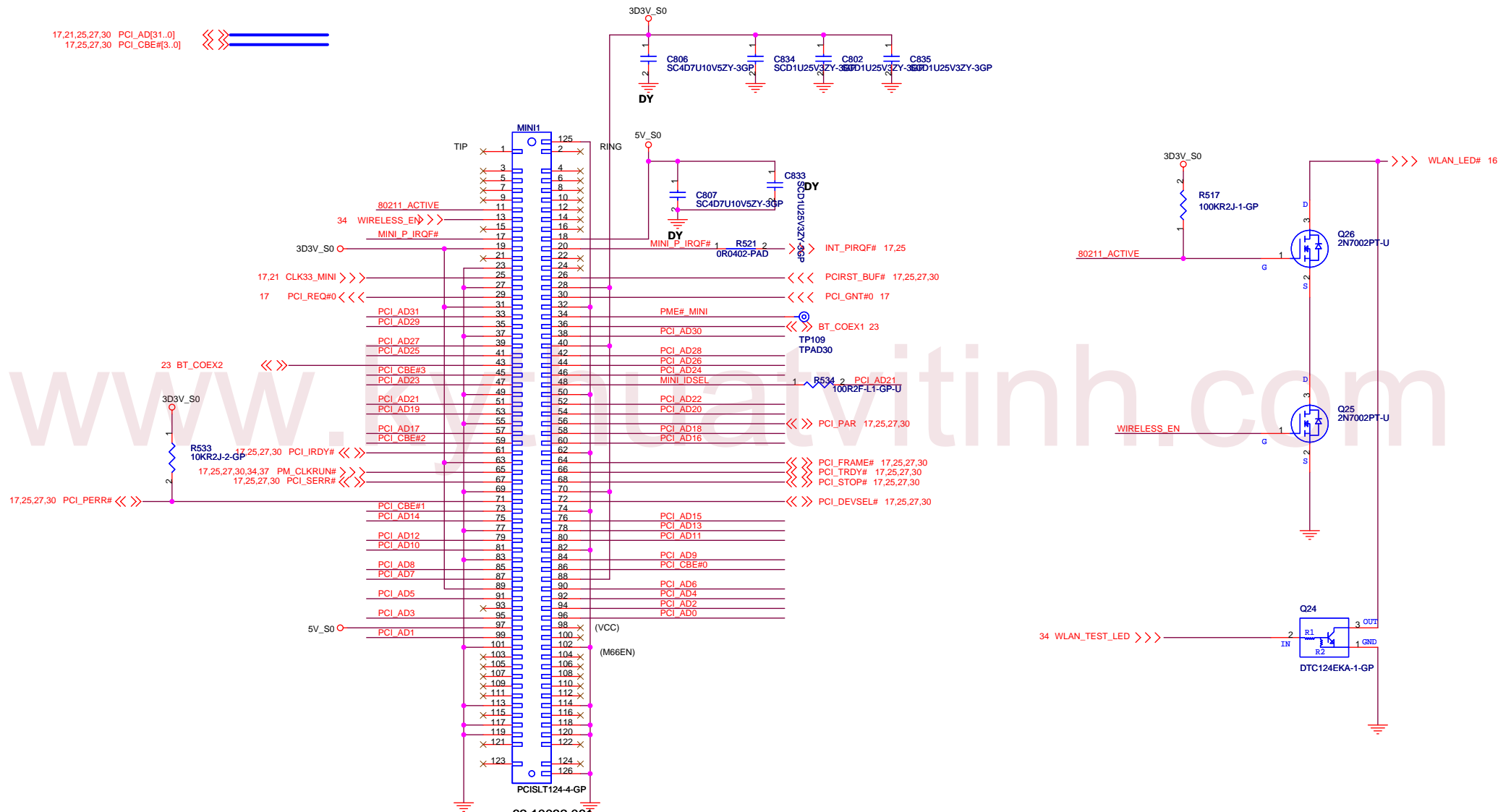
**緯創資通 Wistron Corporation**  
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **R5C832 1394 7IN1(2/2)**

Size: A3 Document Number: **Bolsena-E** Rev: **SA**

Date: Thursday, October 13, 2005 Sheet: 28 of 58

# MINI-PCI



ME : 62.10032.061  
 2ND : 62.10043.221

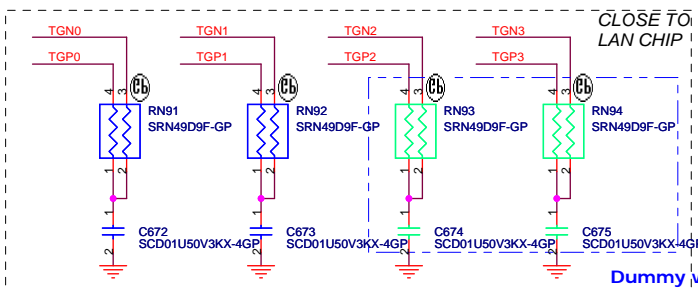
62.10032.031 - 2ND

<Variant Name>

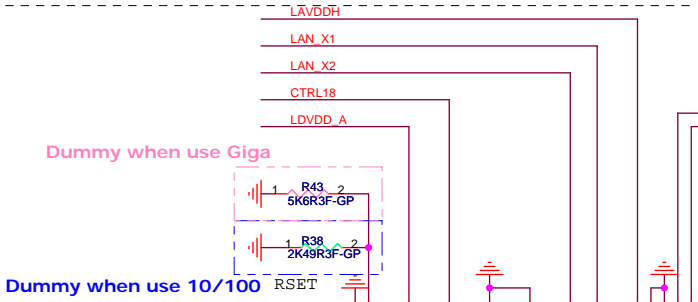
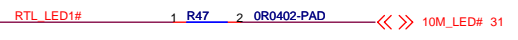
**緯創資通 Wistron Corporation**  
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **MINI-PCI**

Size: A3	Document Number: <b>Bolsena-E</b>	Rev: SA
Date: Thursday, October 13, 2005	Sheet: 29	of 58

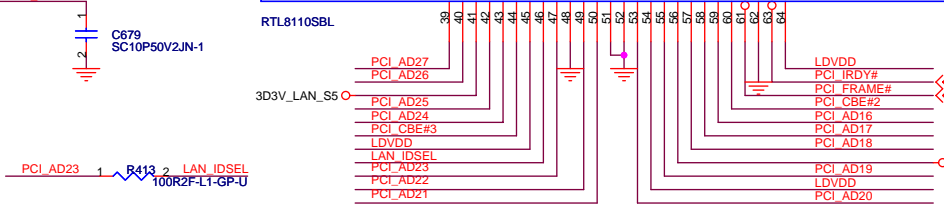
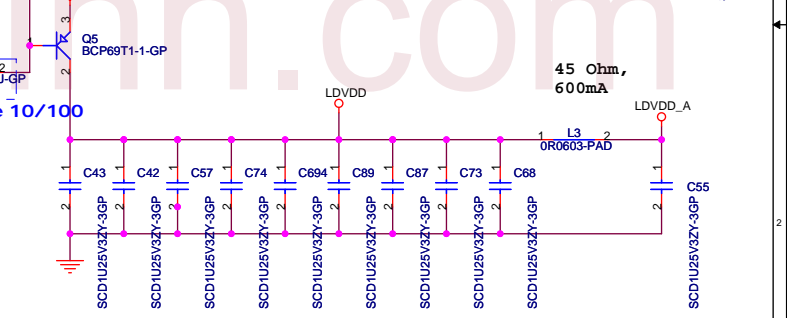
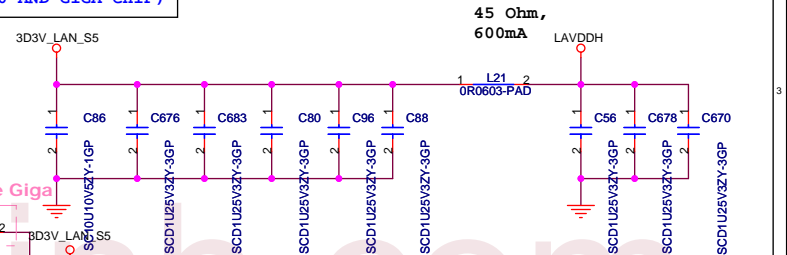
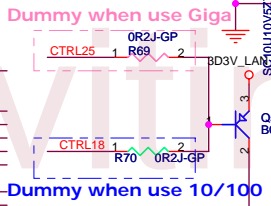
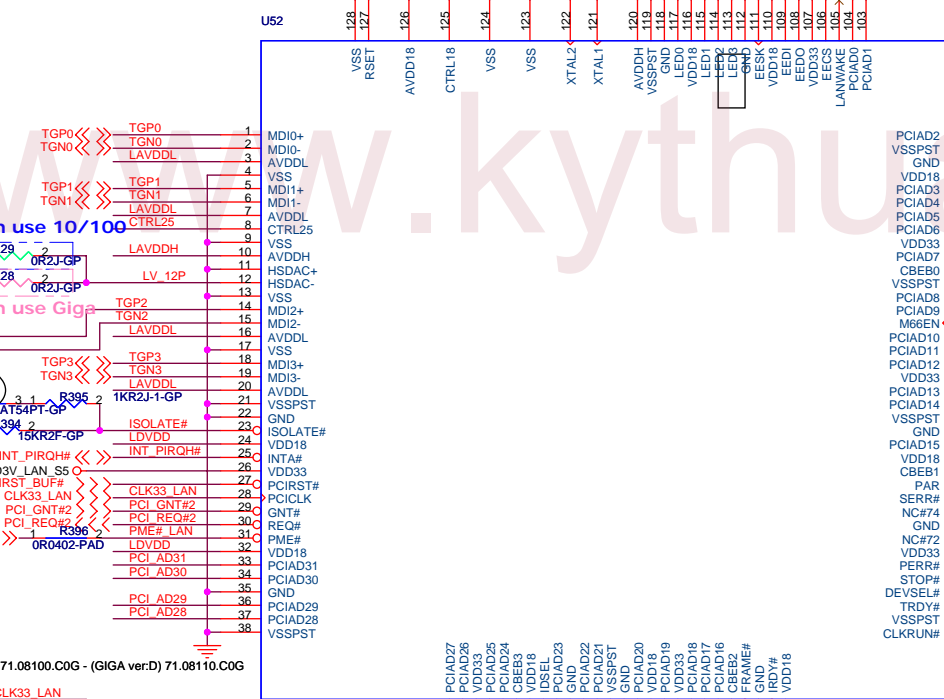


=> LED1 : LINK

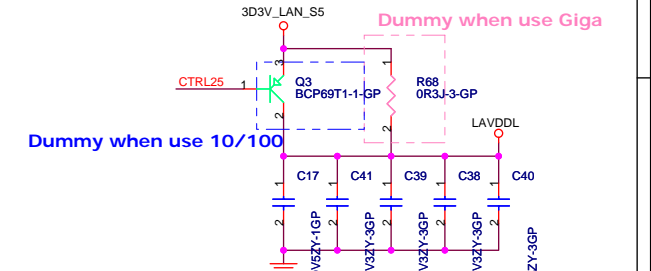


EEPROM LED OPTION USE '01'  
(DEFINED IN SPEC)  
=> LED0 : ACT  
=> LED1 : LINK  
(BOTH 10/100 AND GIGA CHIP)

ACT\_LED# <<>> ACT\_LED# 31  
LDVDD  
RTL\_LED1# => LED0 : ACT



GIGALAN: RTL8110SBL  
10/100 LAN: RTL8100C



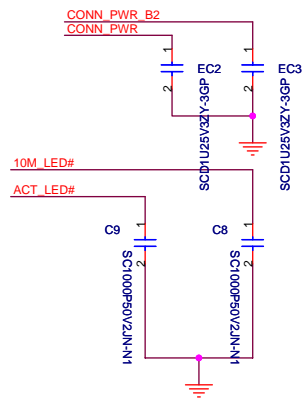
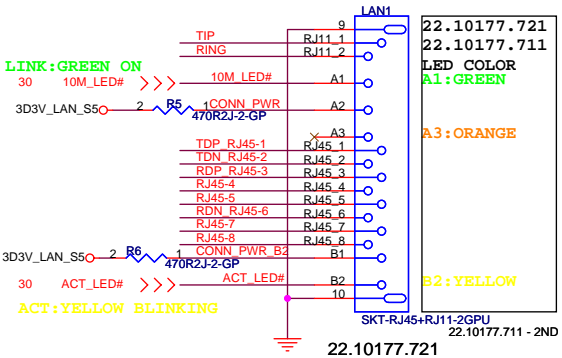
Wistron Corporation  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **RTL8110SBL/RTL8100C**

Size: A3, Document Number: **Bolsena-E**, Rev: SA

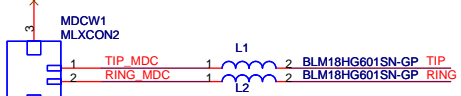
Date: Thursday, October 13, 2005, Sheet 30 of 58

Link: Green - 10Mbps/802.11b  
 Orange - 100Mbps/802.11a  
 Yellow - 1Gbps



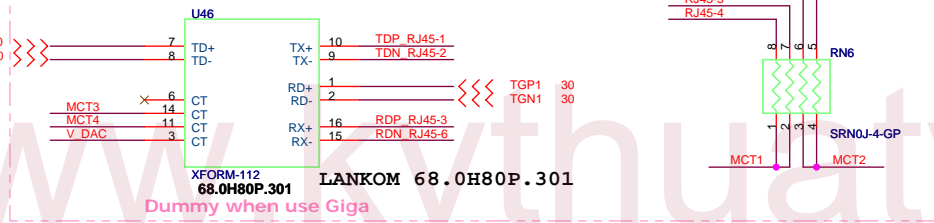
3D3V\_LAN\_S5 -> R5 -> 470R2J-2-GP  
 30 10M\_LED# >>>  
 30 10M\_LED# >>>  
 3D3V\_LAN\_S5 -> R6 -> 470R2J-2-GP  
 30 ACT\_LED# >>>  
 ACT\_LED# >>>  
 ACT:YELLOW BLINKING

ME : 22.10177.721  
 2nd : (canceled)



21.D0010.102  
 ME : 21.D0010.102

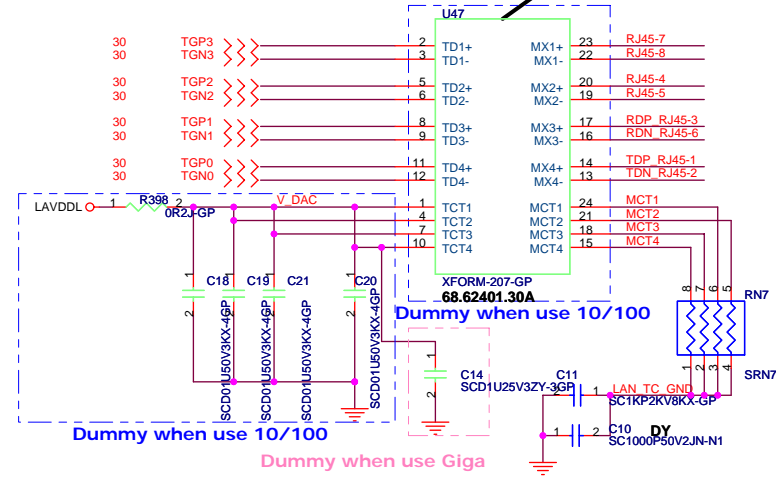
**10/100M Lan Transformer**



**GIGA Lan Transformer**

LANKOM 68.02402.30A  
 netsWAP 68.62401.301 (GIGA ,Thick)

NETSWAP GIGA THICK PN IS 68.62401.301, DON'T USE NETSWAP THIN



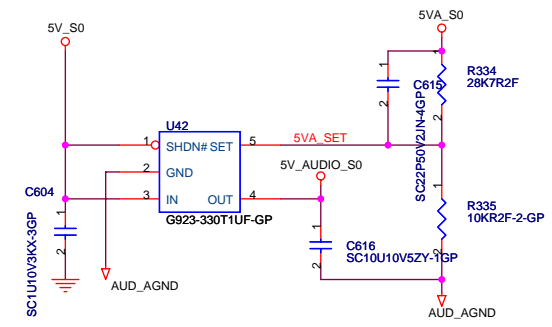
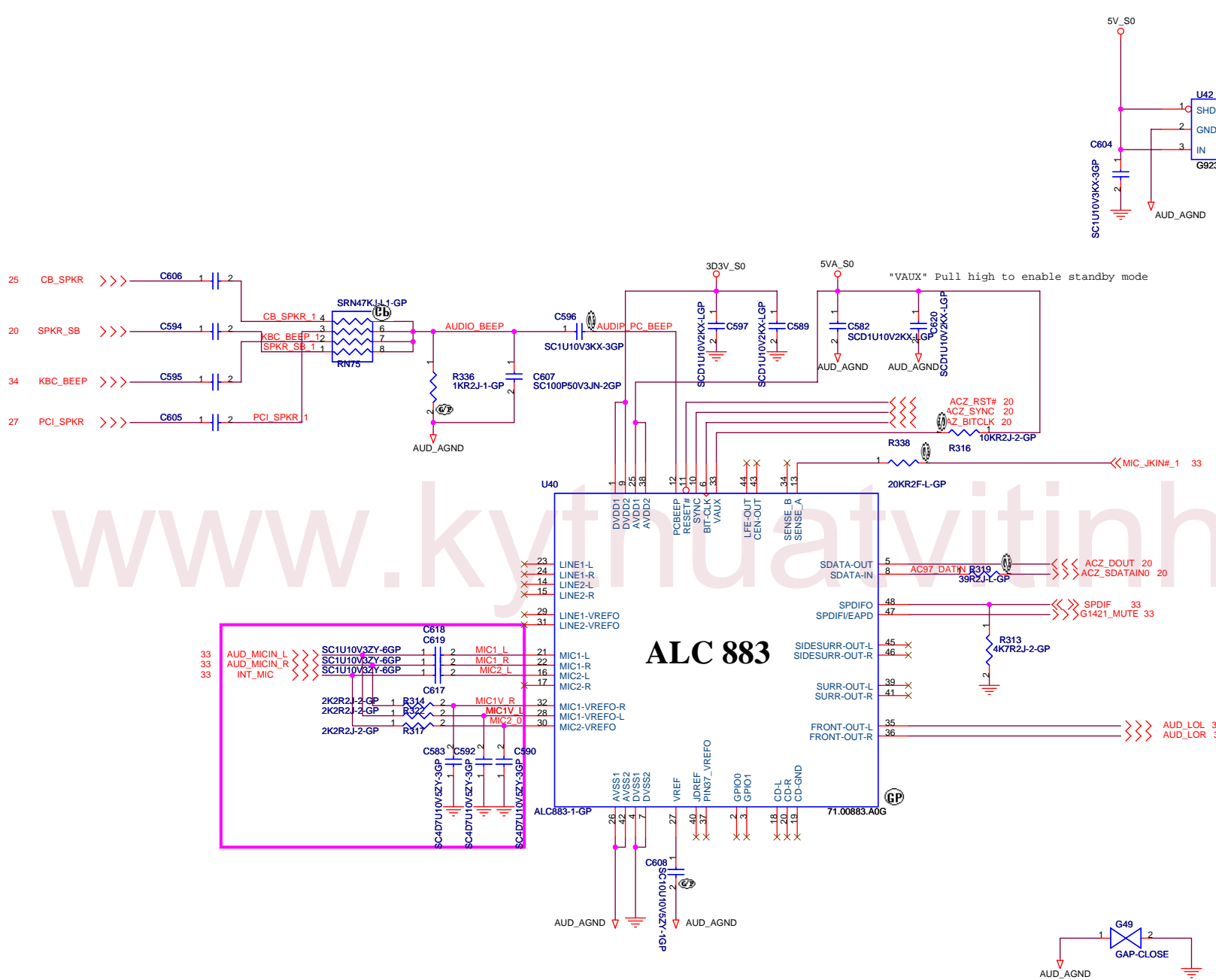
- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat, except RJ-45 moat.

緯創資通 Wistron Corporation  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN CONN

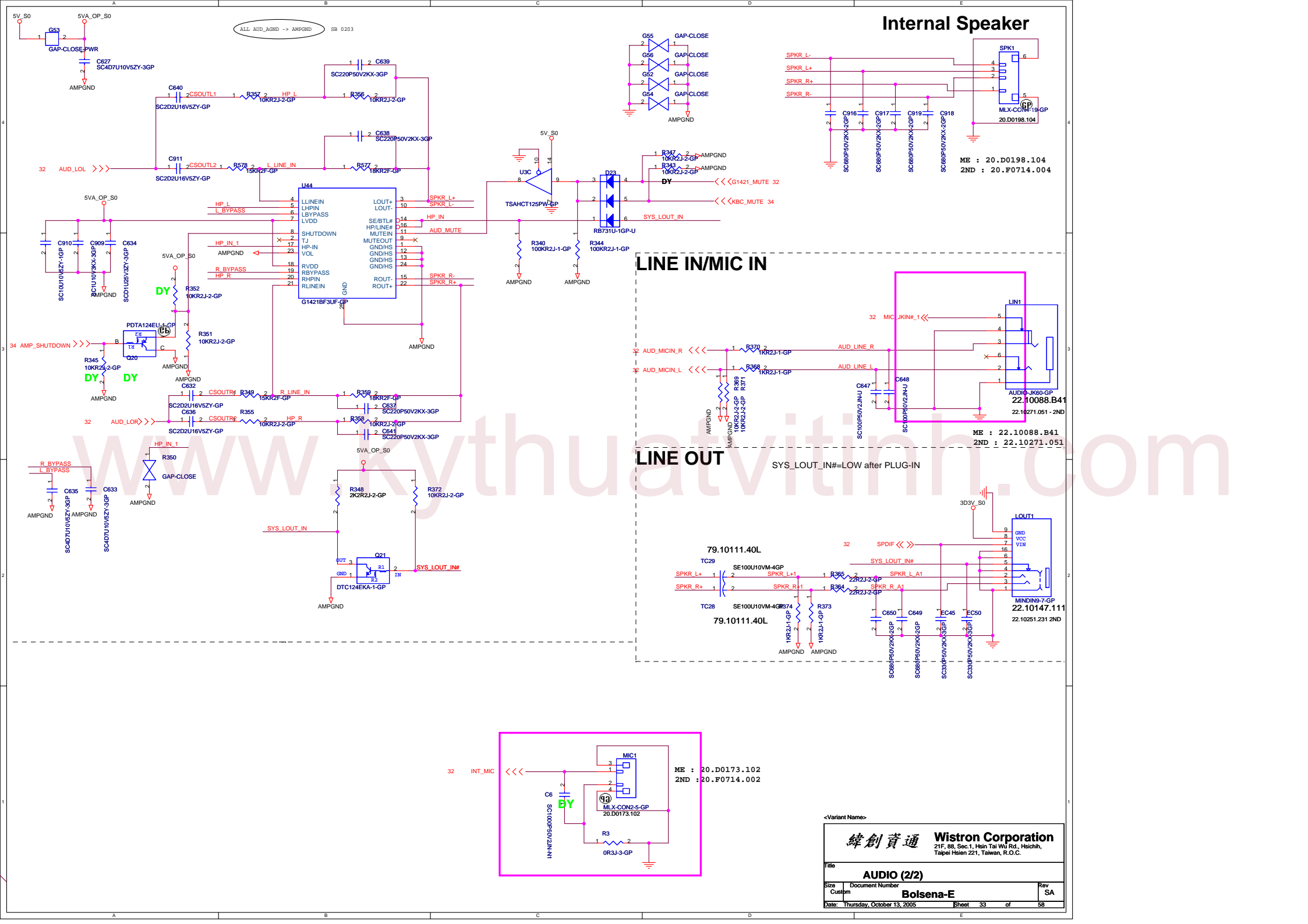
Size A3 Document Number: Bolsena-E Rev SA

Date: Thursday, October 13, 2005 Sheet 31 of 58



www.kytnuatvith.com

<b>Wistron Corporation</b> 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>AUDIO (1/2) -- CODEC ALC655</b>	
Size	Document Number
A3	<b>Bolsena-E</b>
Date: Thursday, October 13, 2005	Sheet 32 of 58



**Internal Speaker**

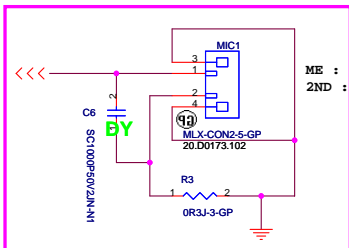
ME : 20.D0198.104  
2ND : 20.F0714.004

**LINE IN/MIC IN**

ME : 22.10088.B41  
2ND : 22.10271.051

**LINE OUT**

SYS\_LOUT\_IN#-LOW after PLUG-IN

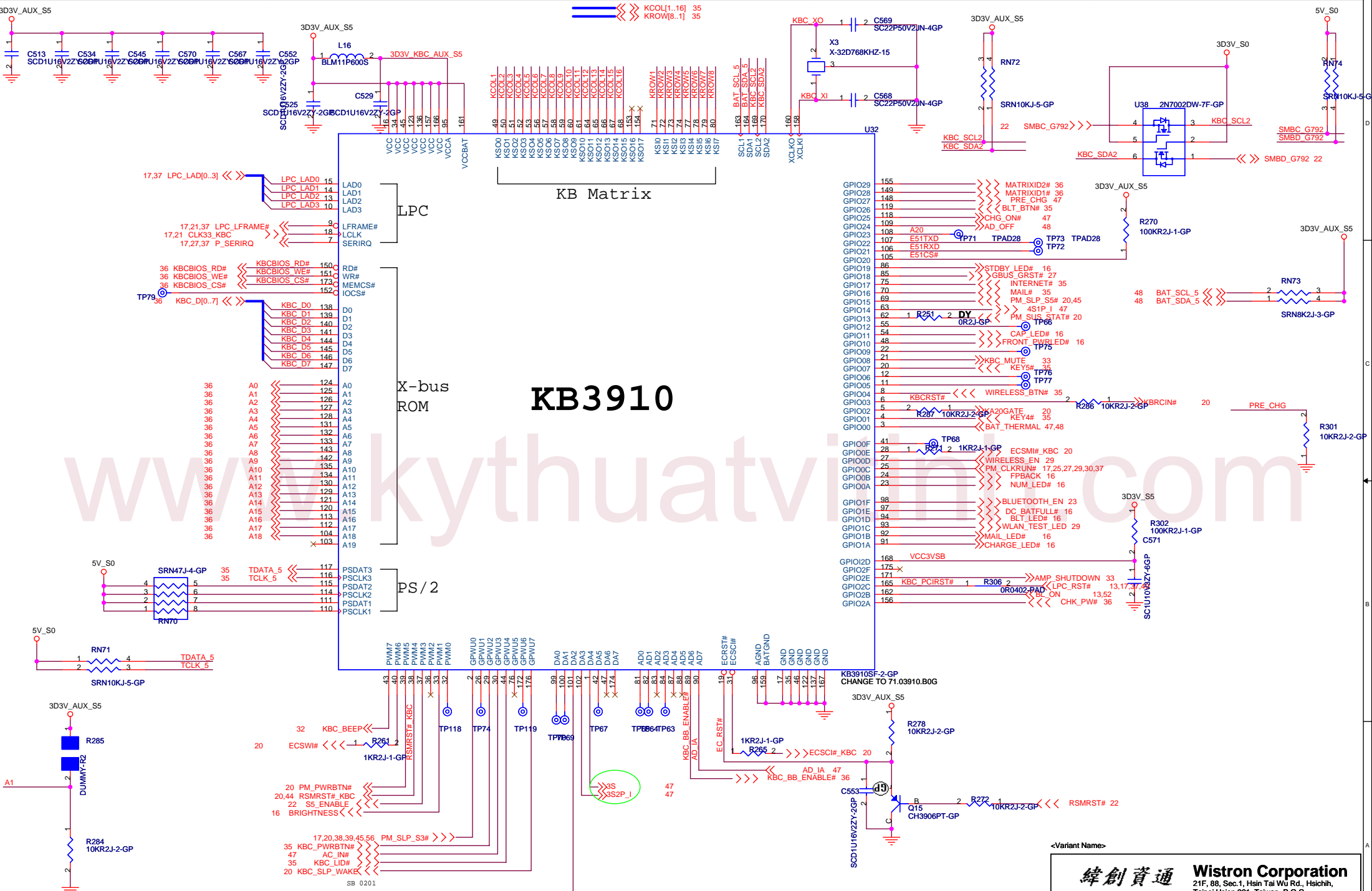


<Variant Name>

**緯創資通** **Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

File		
<b>AUDIO (2/2)</b>		
Size	Document Number	Rev
Custom	<b>Bolsena-E</b>	SA
Date: Thursday, October 13, 2005 Sheet 33 of 58		





# KB3910

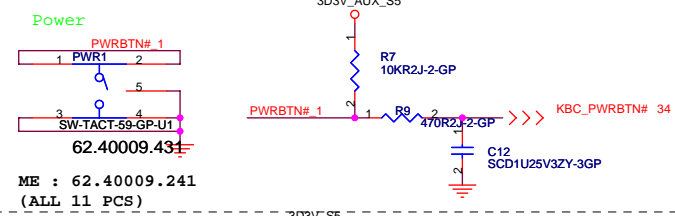
A1 for the internal pull-up resistors on XIOCS[F:0] pins==>High=enable,Low=Disable  
 A4 for DMRP==>High=Disable,Low=Enable  
 A5 for EMWB==>High=Enable,Low=Disable  
 GPIO05 for Clock test mode==>High=test Mode,Low=32KHz clock in normal running(Recommended)  
 GPIO06 for DPLL test mode==>High=Test Mode,Low=Normal operation(Recommended)

<Variant Name>

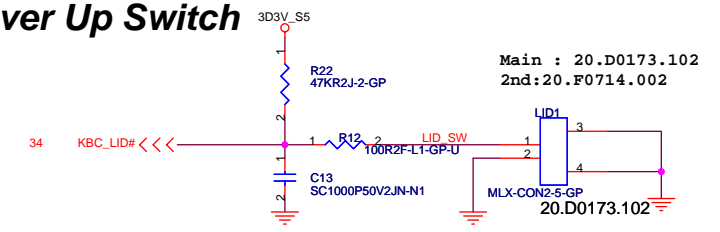
**緯創資通 Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	<b>KBC KB3910</b>	
Size A3	Document Number	Rev SA
Date: Thursday, October 13, 2005	Bolsena-E	Sheet 34 of 58

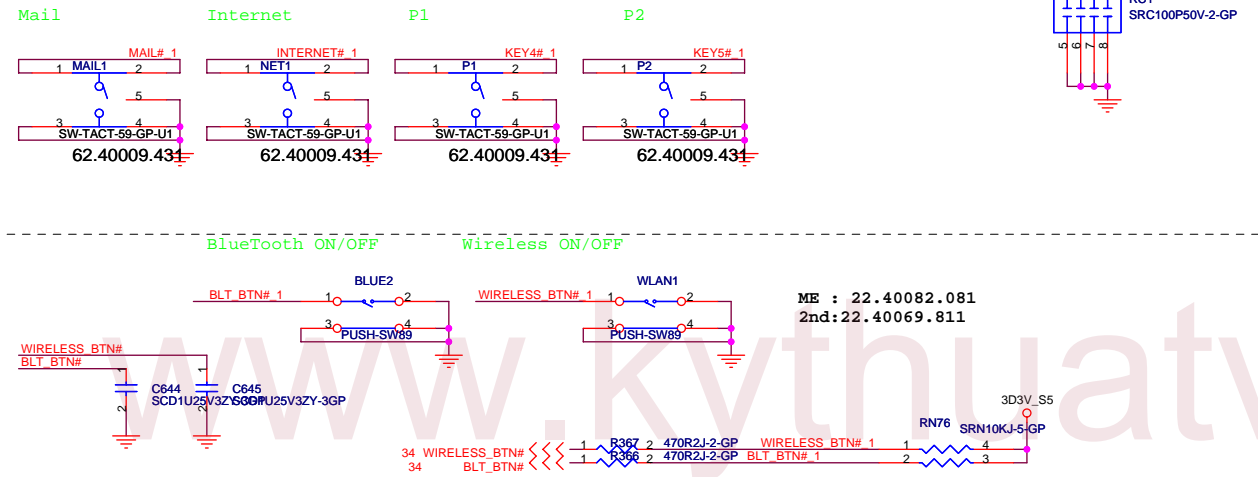
# POWER BUTTON



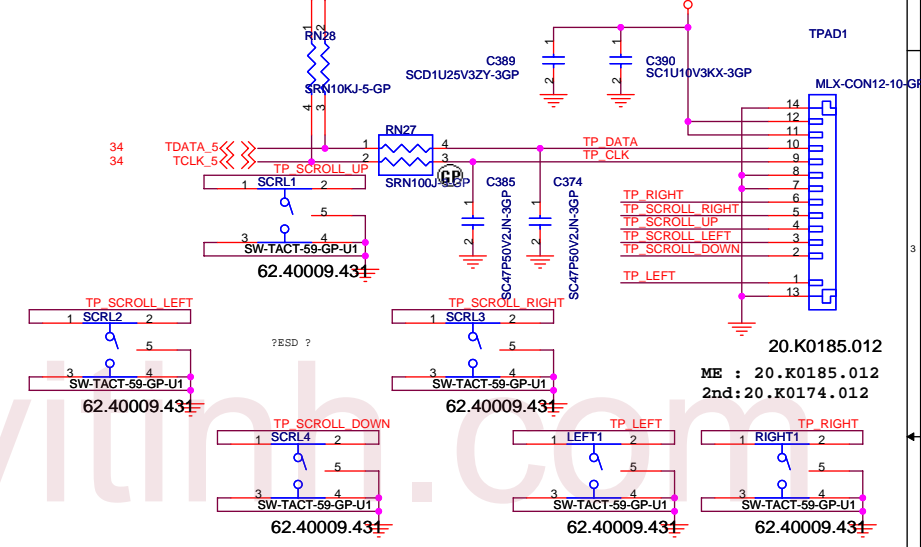
# Cover Up Switch



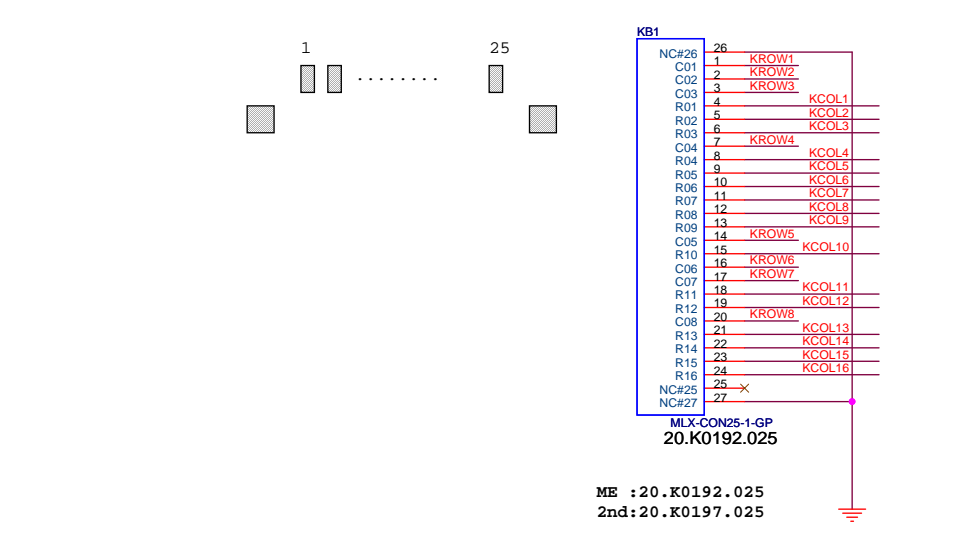
# Buttons



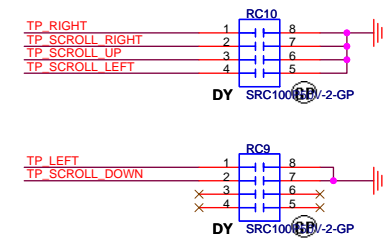
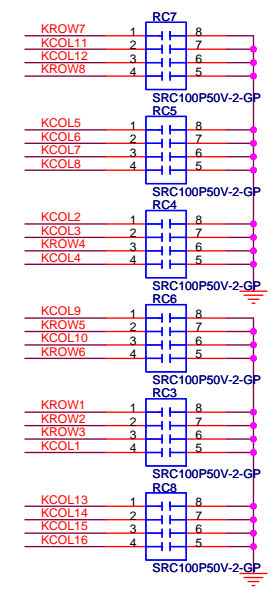
# TOUCH PAD



# Internal KeyBoard CONN



# EMI Bypass cap.



<Variant Name>

**緯創資通 Wistron Corporation**  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsein 221, Taiwan, R.O.C.

Title: **BUTTONS / KB / TOUCHPAD**

Size: A3 Document Number: **Bolsena-E** Rev: SA

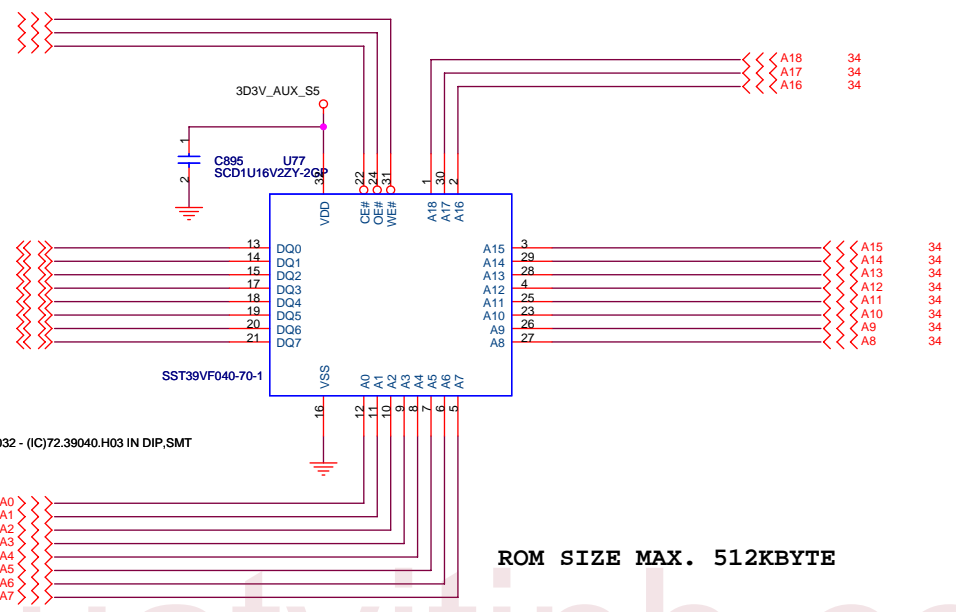
Date: Thursday, October 13, 2005 Sheet: 35 of 58

>>> KBC\_D[0..7] 34

34 KBCBIOS\_WE#  
34 KBCBIOS\_RD#  
34 KBCBIOS\_CS#

34 KBC\_D0  
34 KBC\_D1  
34 KBC\_D2  
34 KBC\_D3  
34 KBC\_D4  
34 KBC\_D5  
34 KBC\_D6  
34 KBC\_D7

34 A0  
34 A1  
34 A2  
34 A3  
34 A4  
34 A5  
34 A6  
34 A7



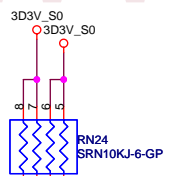
SST39VF040-70-1

(SOCKET) 62.10002.032 - (IC)72.39040.H03 IN DIP,SMT

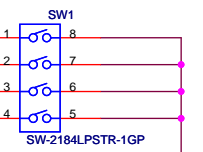
ROM SIZE MAX. 512KBYTE

PLCC32 Socket P/N:  
SSKT3262.10002.032  
SSKT32 62.10005.032

www.kythuavietinh.com



34 KBC\_BB\_ENABLE# <<<<  
34 CHK\_PW# <<<<  
34 MATRIXID1# <<<<  
34 MATRIXID2# <<<<

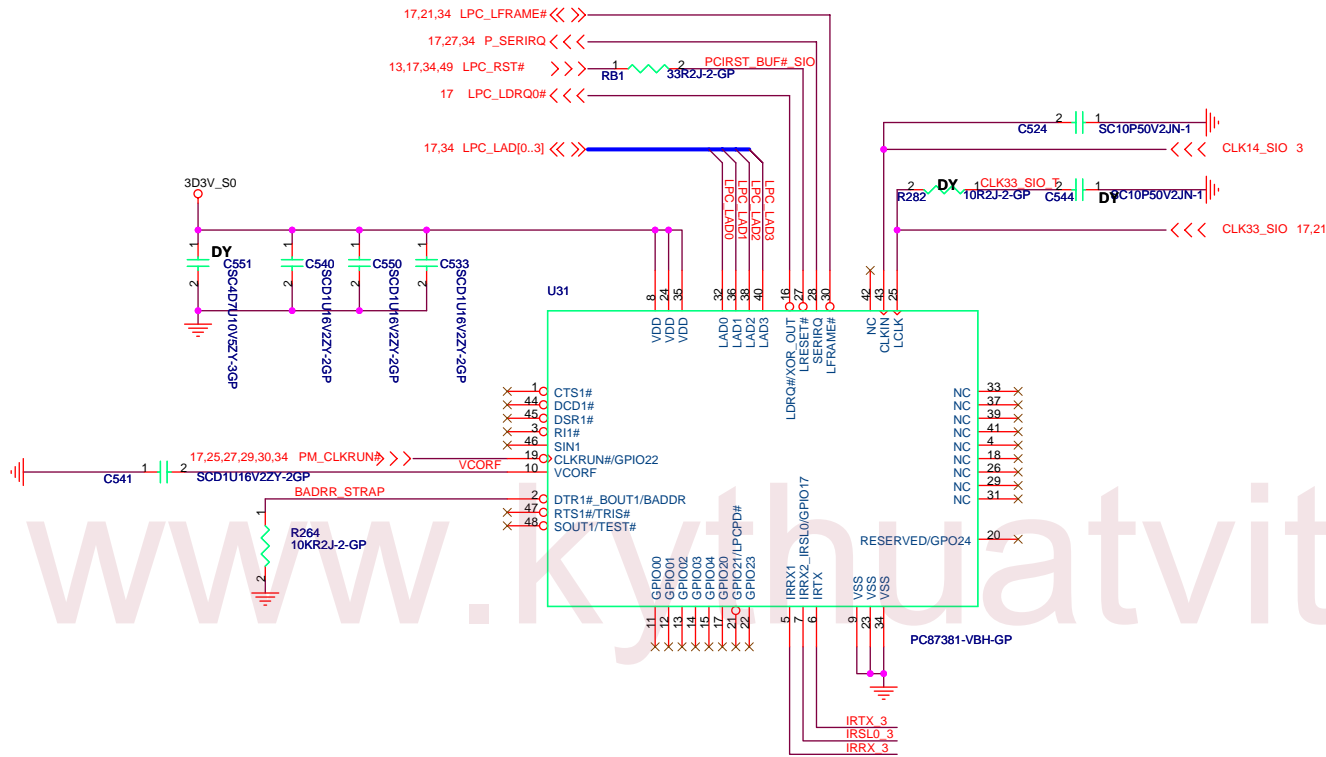


Keyboard matrix ( from vendor )

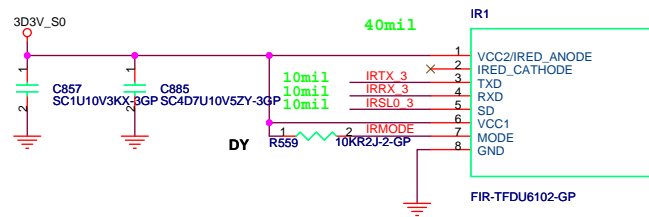
	US	Jap	Eur	Other
Low Bit MATRIXID1#	1	1	0	0
High Bit MATRIXID2#	1	0	1	0

<Variant Name>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>BIOS ROM</b>			
Size A3	Document Number		Rev
	<b>Bolsena-E</b>		<b>SA</b>
Date: Thursday, October 13, 2005	Sheet	36 of	58



### Infineon FIR Module

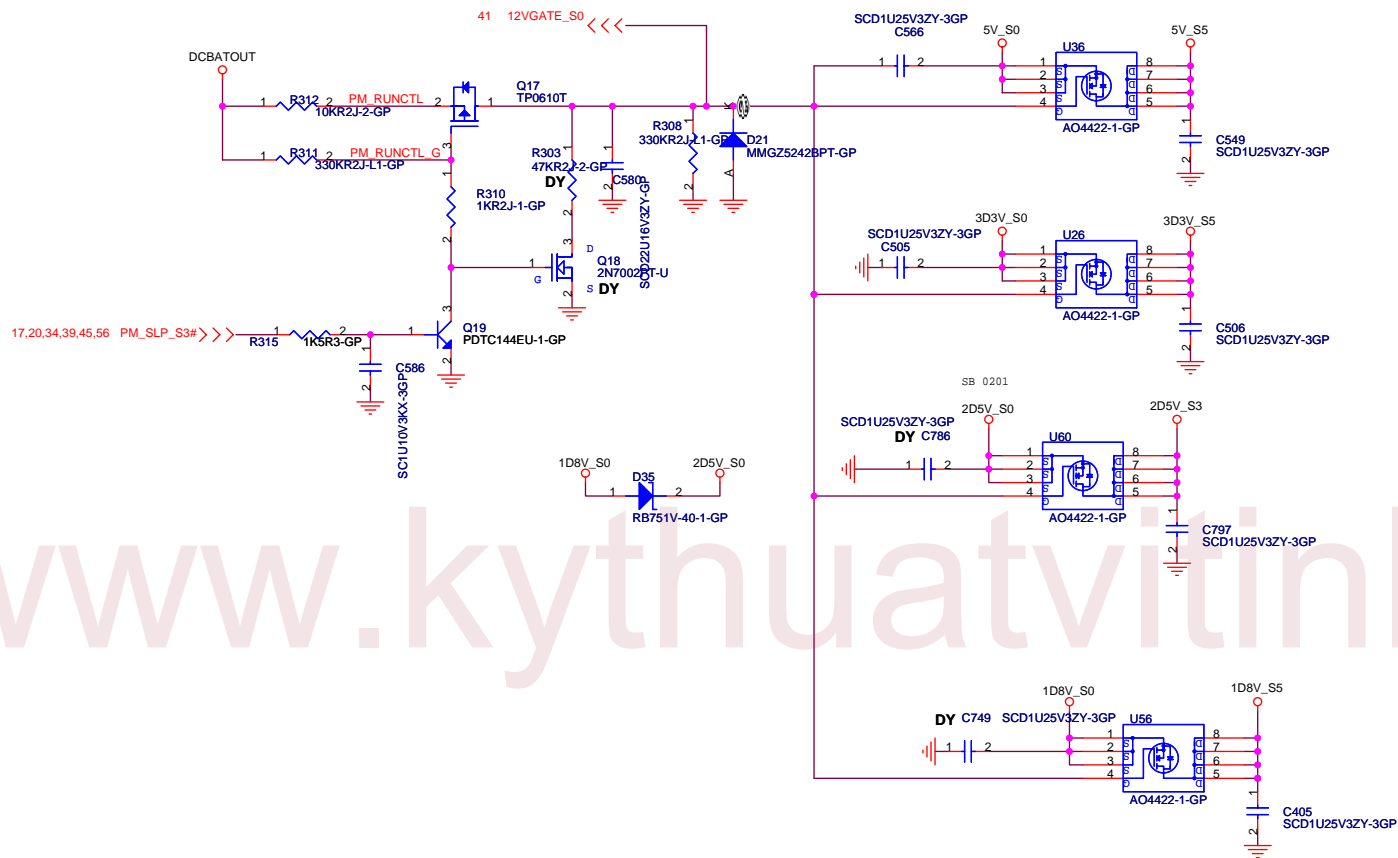


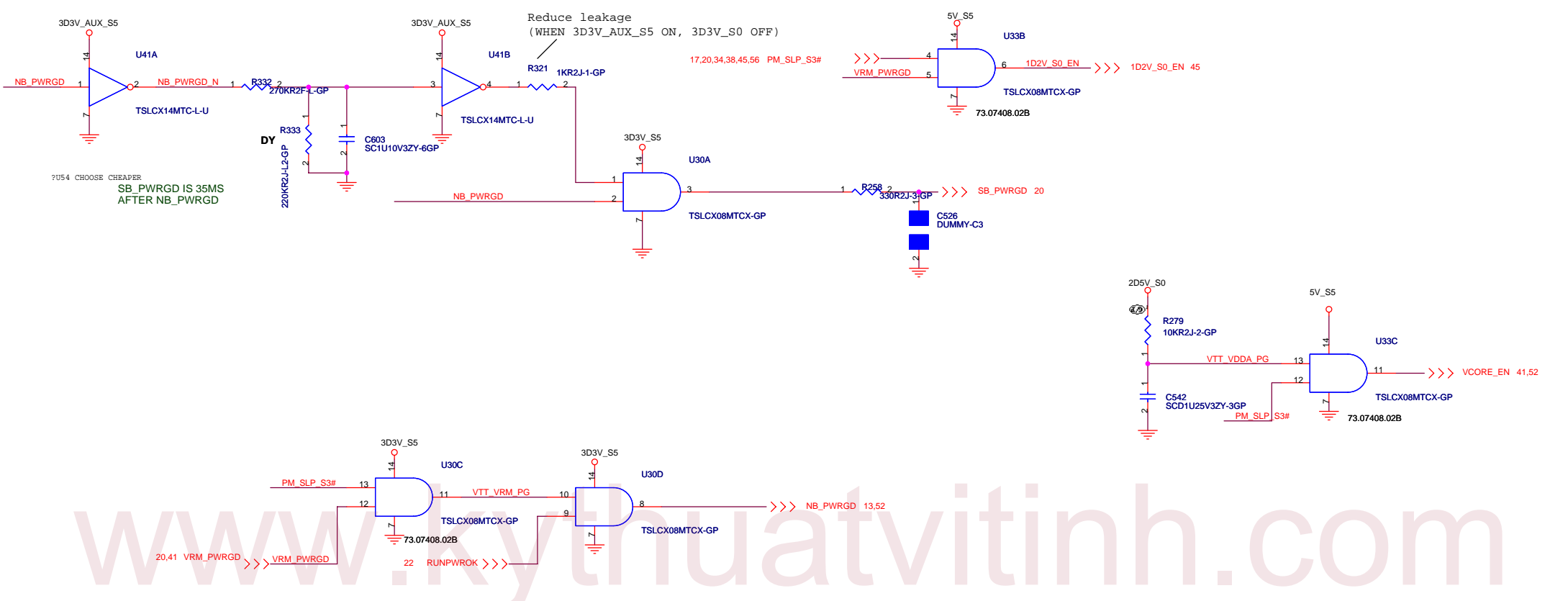
56.15001.051

緯創資通 Wistron Corporation  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

Title		
SUPER IO NC87381		
Size	Document Number	Rev
A3	SNIFE	-2
Date:	Thursday, October 13, 2005	Sheet 37 of 58

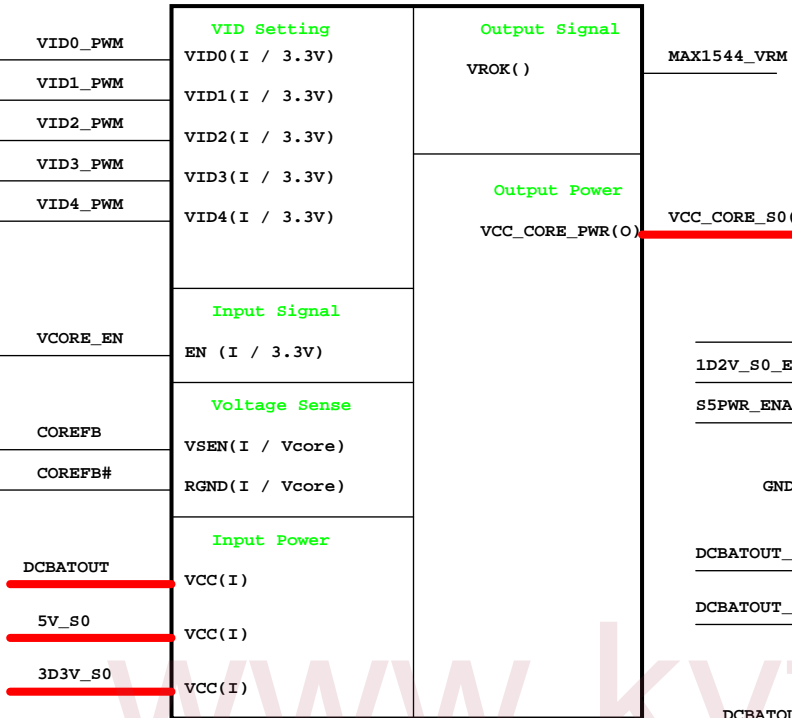
# Run Power



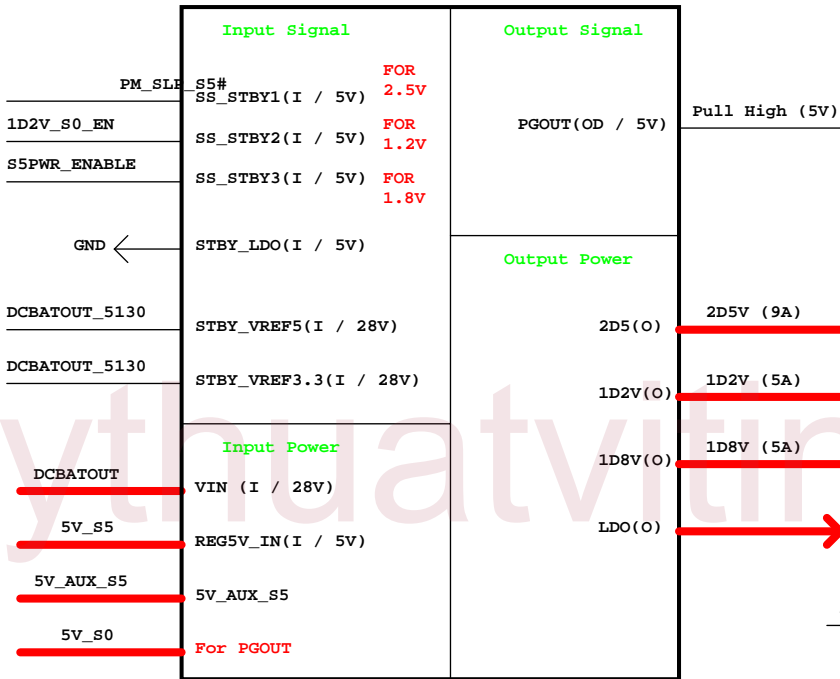


www.kyathuatvith.com

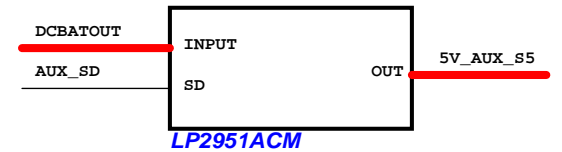
**CPU\_CORE**  
**MAX1544ETL**



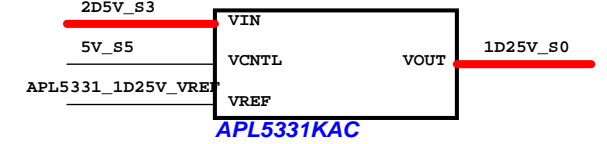
**TI TPS5130**  
**2D5V/1D2V/1D8V**



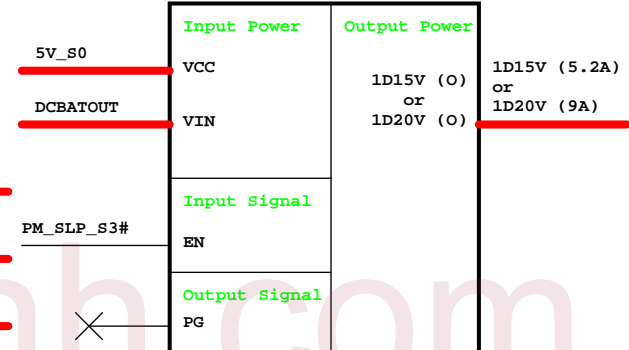
**5V\_AUX\_S5**



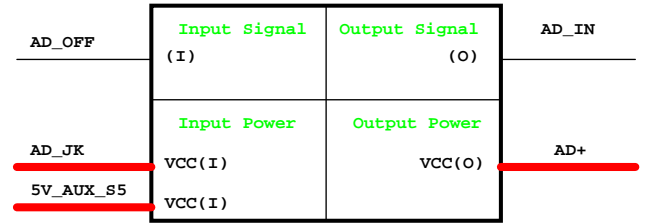
**1D25V\_S3**



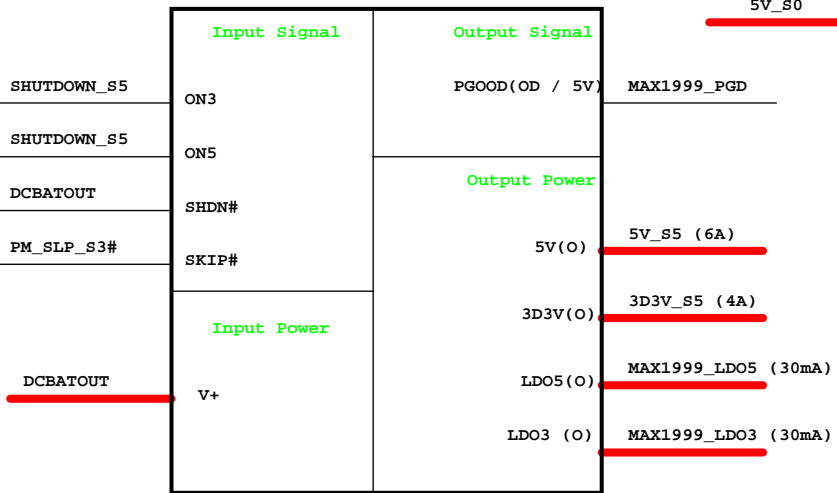
**FAN5234\_VGA\_Core**  
**1D15V or 1D20V**



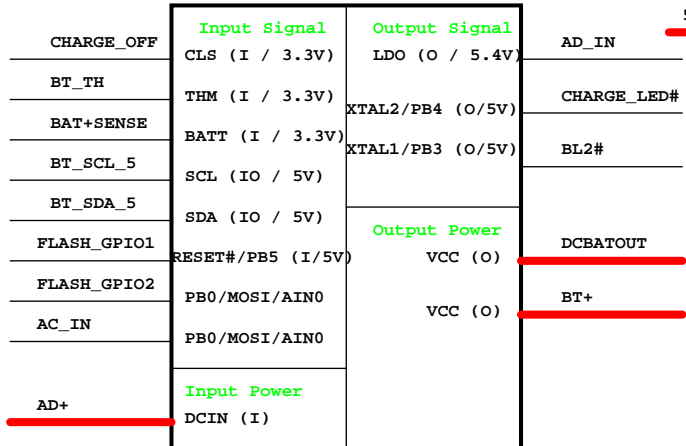
**Adapter**



**TPS51120**  
**5V/3D3V**



**Charger\_Max8725**



(Power Team)

<Variant Name>

**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **POWER BLOCK DIAGRAM**

Size: A3 Document Number: **Bolsena-E** Rev: SA

Date: Thursday, October 13, 2005 Sheet: 40 of 58

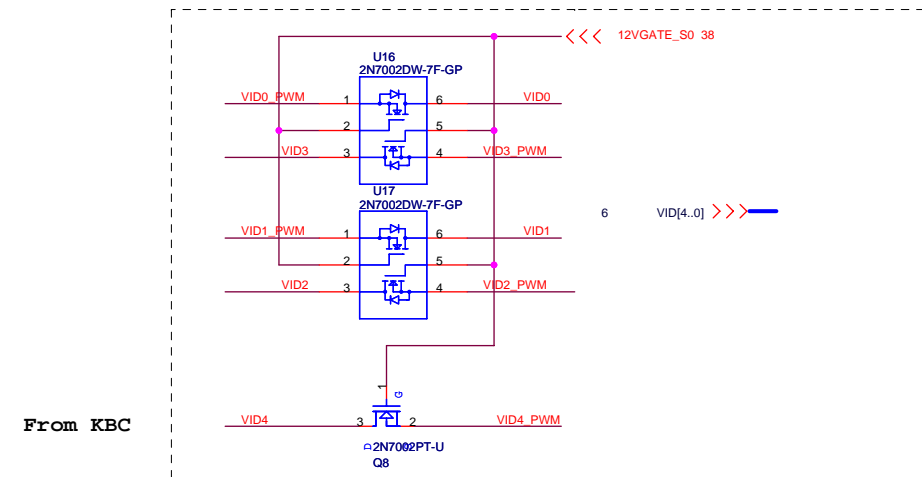


CPU\_VCORE  
 VID=1.20V  
 I<sub>omax</sub>=27.3A (35W)  
 OCP=40A~45A

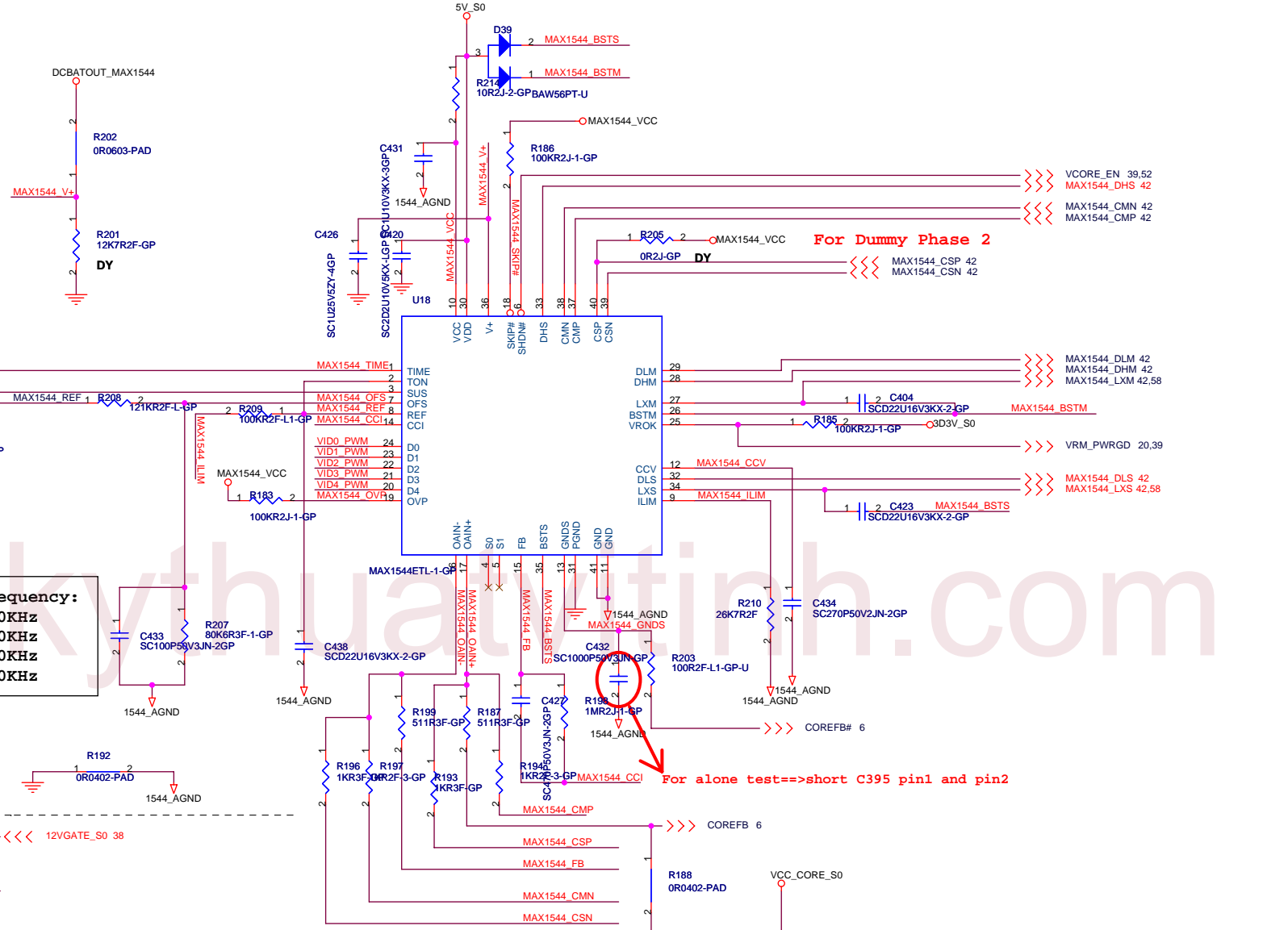
TABLE 1. VOLTAGE IDENTIFICATION CODES

VID4	VID3	VID2	VID1	VID0	DAC
0	0	0	0	0	1.550
0	0	0	0	1	1.525
0	0	0	1	0	1.500
0	0	0	1	1	1.475
0	0	1	0	0	1.450
0	0	1	0	1	1.425
0	0	1	1	0	1.400
0	0	1	1	1	1.375
0	1	0	0	0	1.350
0	1	0	0	1	1.325
0	1	0	1	0	1.300
0	1	0	1	1	1.275
0	1	1	0	0	1.250
0	1	1	0	1	1.225
0	1	1	1	0	1.200
0	1	1	1	1	1.175
1	0	0	0	0	1.150
1	0	0	0	1	1.125
1	0	0	1	0	1.100
1	0	0	1	1	1.075
1	0	1	0	0	1.050
1	0	1	0	1	1.025
1	0	1	1	0	1.000
1	0	1	1	1	0.975
1	1	0	0	0	0.950
1	1	0	0	1	0.925
1	1	0	1	0	0.900
1	1	0	1	1	0.875
1	1	1	0	0	0.850
1	1	1	0	1	0.825
1	1	1	1	0	0.800
1	1	1	1	1	Shutdown

TON: Frequency:  
 GND 550KHz  
 REF 300KHz  
 OPEN 200KHz  
 VCC 100KHz



From KBC



For alone test==>short C395 pin1 and pin2

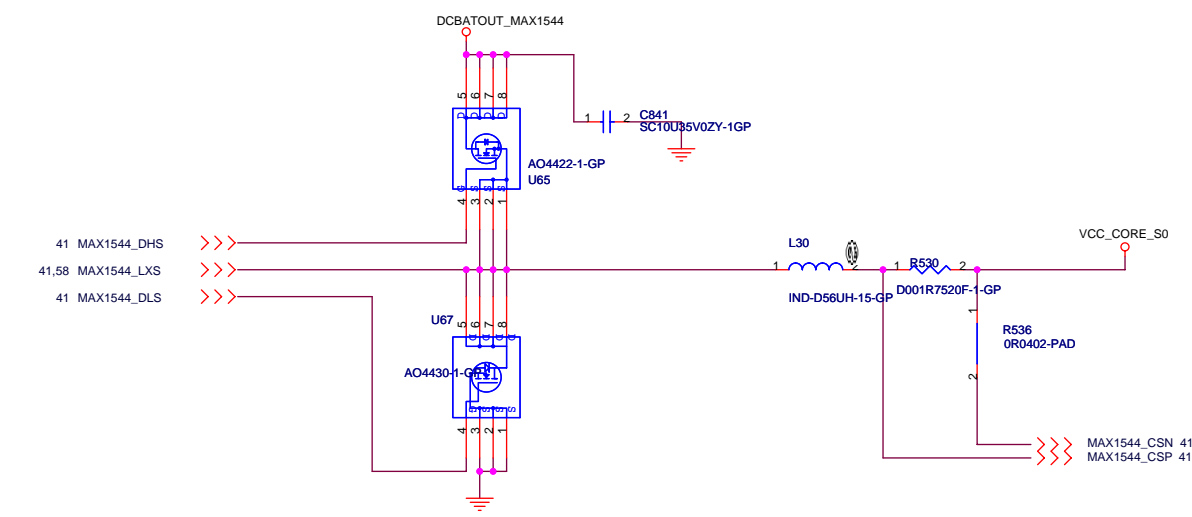
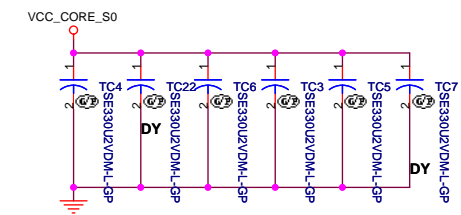
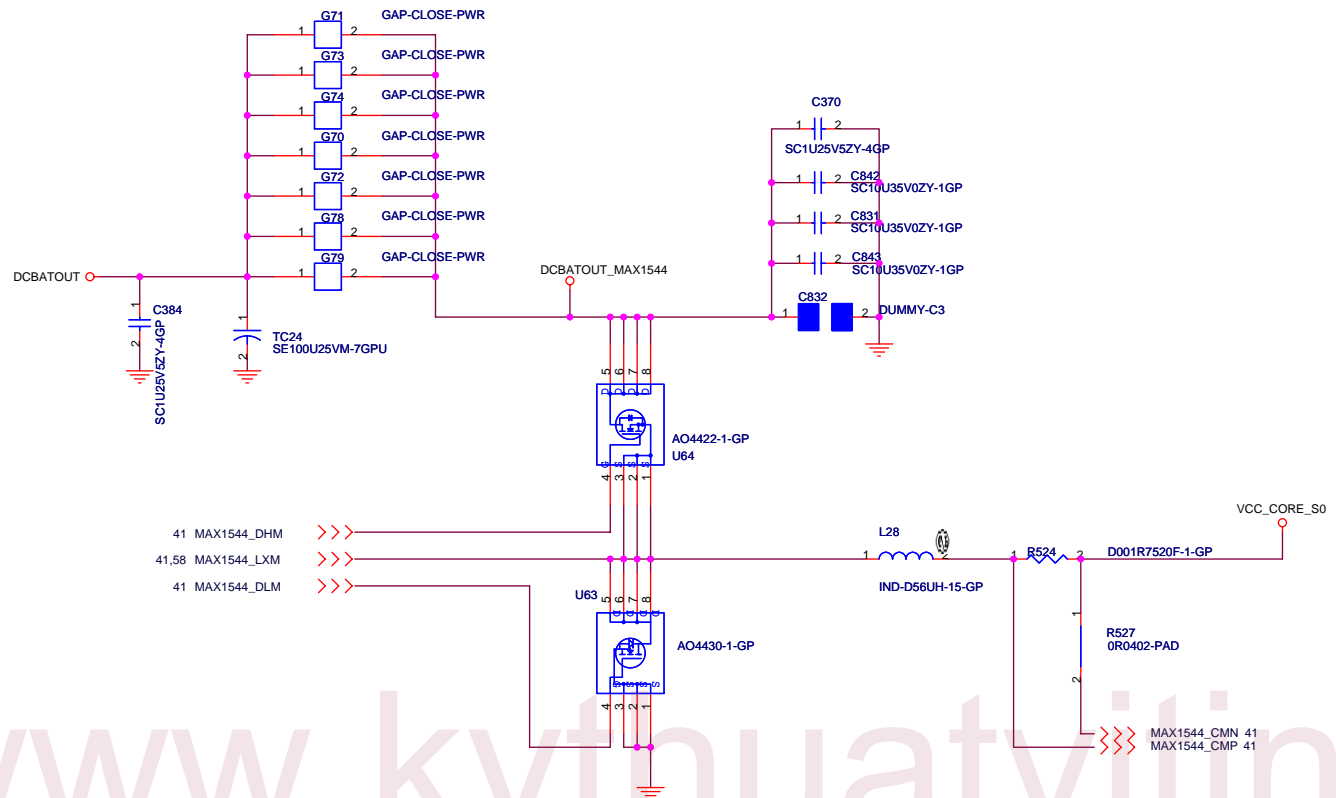
<Variant Name>

**緯創資通 Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU Vcore 1**

Size A3	Document Number	Rev SA
<b>Bolsena-E</b>		
Date: Thursday, October 13, 2005	Sheet 41	of 58

(Power Team)



SB 0203

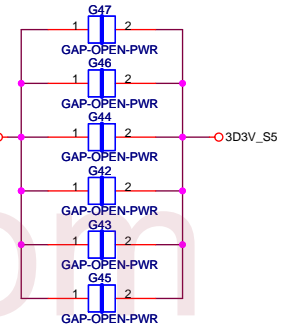
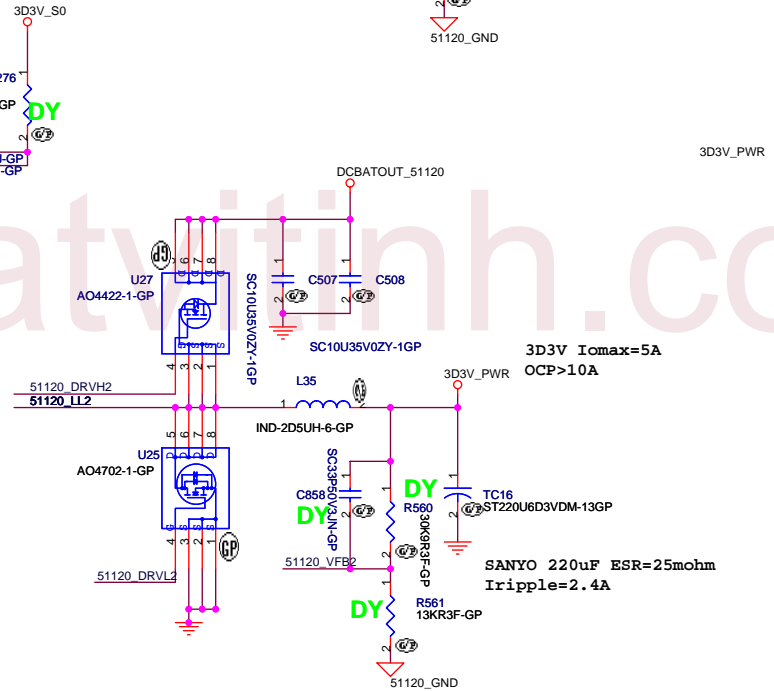
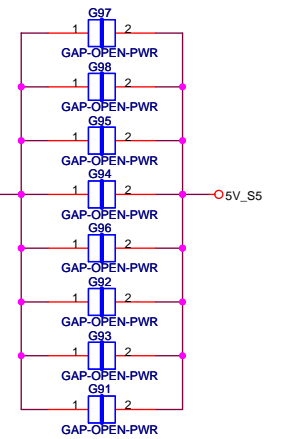
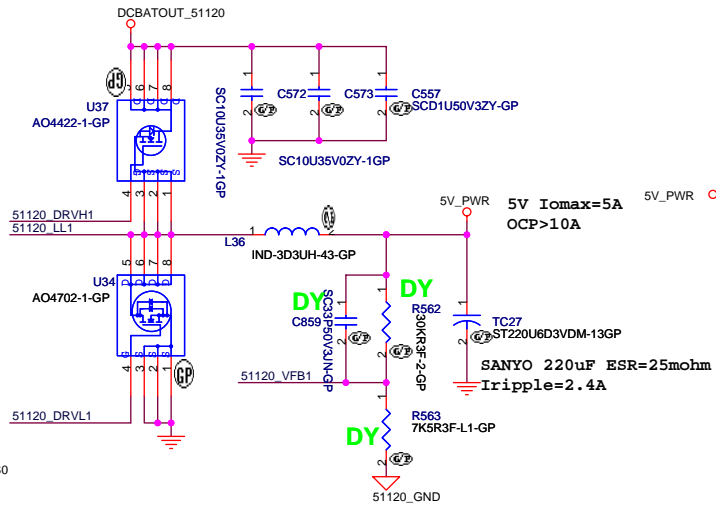
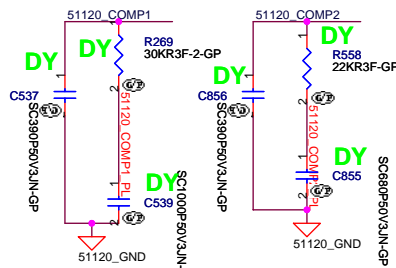
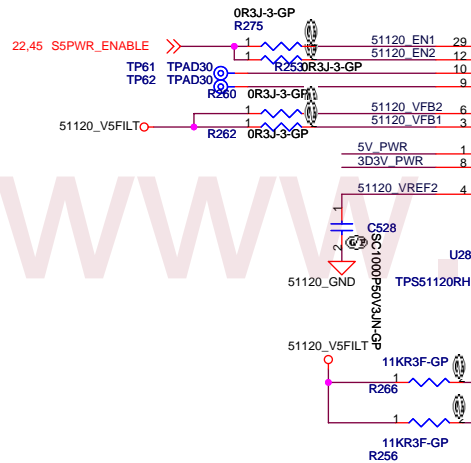
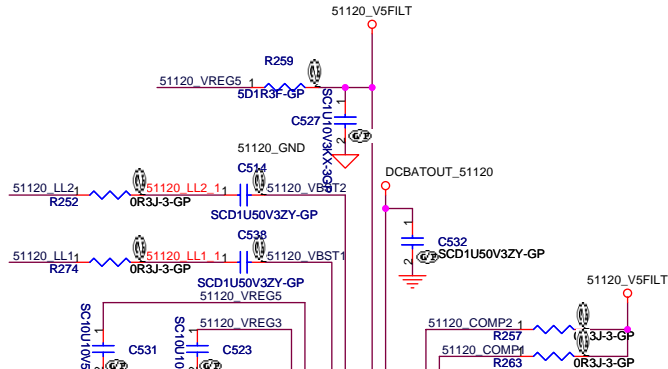
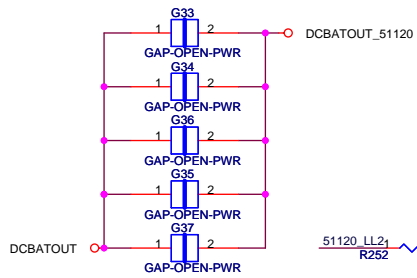
<Variant Name>

**緯創資通 Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU Vcore 2**

Size: A3	Document Number: <b>Bolsena-E</b>	Rev: SA
Date: Thursday, October 13, 2005	Sheet: 42 of 58	

(Power Team)



$$V_{out} = 1V * (R1 + R2) / R2$$

For TPS51120,  
Vout=5V

- If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
- If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
- If you use a 3.3uH inductor, the minimum ESR is 34m ohm.

Vout=3.3V

- If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
- If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
- If you use a 2.5uH inductor, the minimum ESR is 27m ohm.

	GND	VREF2	FLOAT	V5FILT
SKIPSEL	AUTOSKIP	AUTOSKIP / FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	D-Cap MODE
TONSEL	380k/CH1 590k/CH2	290k/CH1 440k/CH2	220k/CH1 330k/CH2	180k/CH1 280k/CH2
VFB1	N/A	not use	ADJ.	5V Fixed Output
VFB2	N/A	not use	ADJ.	3.3V Fixed Output
EN1, EN2	switcher OFF	not use	Switchchr ON	Switcher ON
EN3, EN5	LDO OFF	not use	LDO ON	VREG3 on

Wistron Corporation  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **TPS51120 / 3D3V / 5V**

Size: Document Number  
A3

Date: Thursday, October 13, 2005

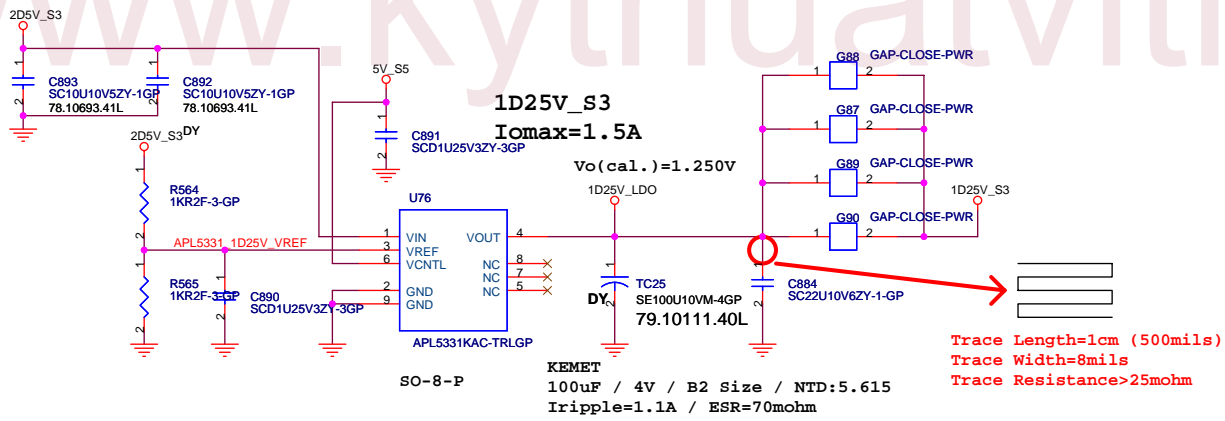
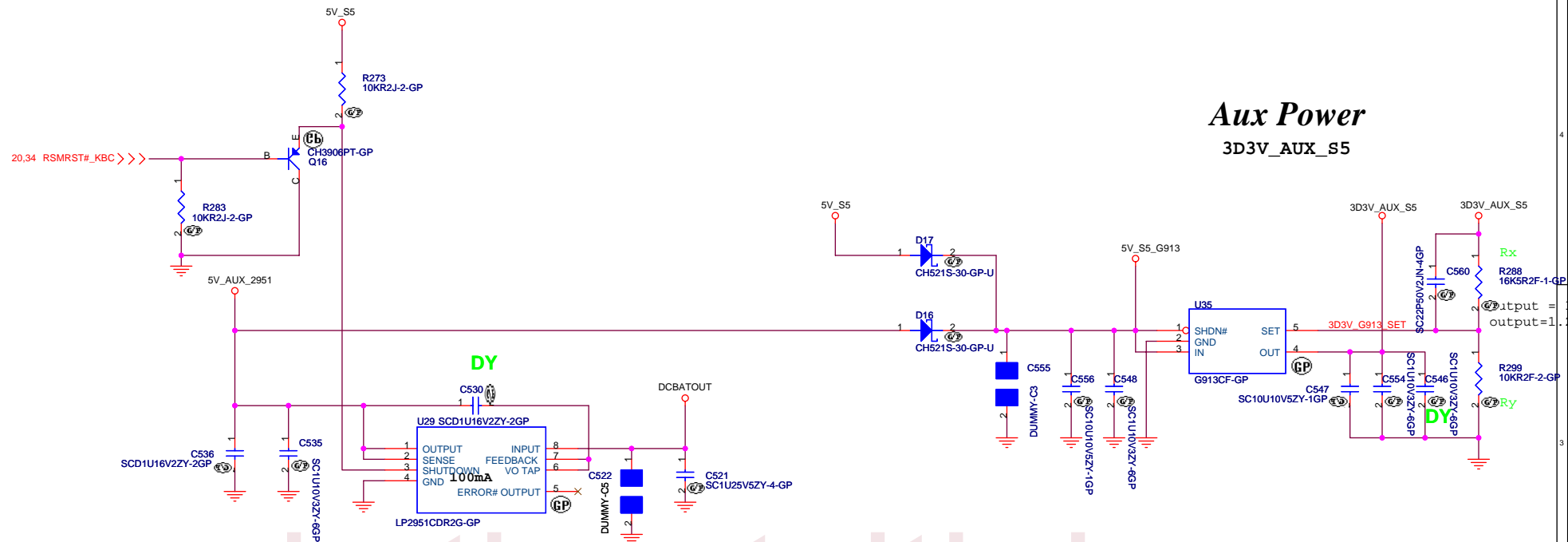
Sheet 43 of 58

Rev: -1

Bolsena-E

# Aux Power

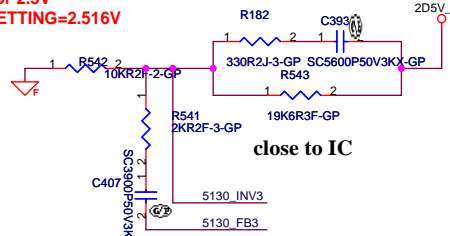
## 3D3V\_AUX\_S5



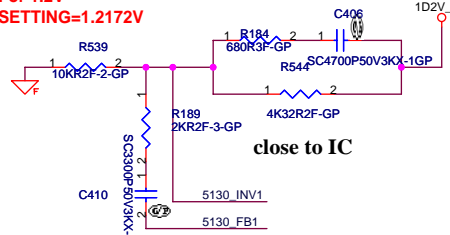
www.kythuovatvinh.com

緯創資通 <b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>1D2V_S3 / 3D3V_AUX</b>	
Size A3	Document Number <b>Bolsena-E</b>
Date: Thursday, October 13, 2005	Sheet 44 of 58
(Power Team)	Rev SA

For 2.5V  
SETTING=2.516V

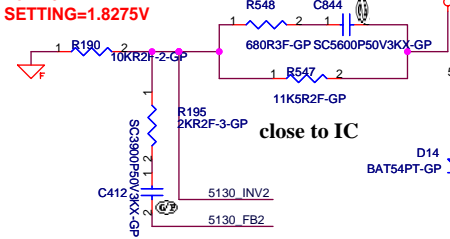


For 1.2V  
SETTING=1.2172V

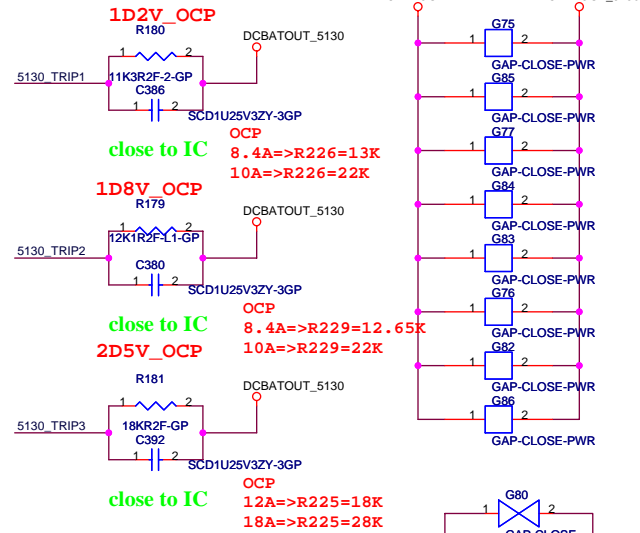
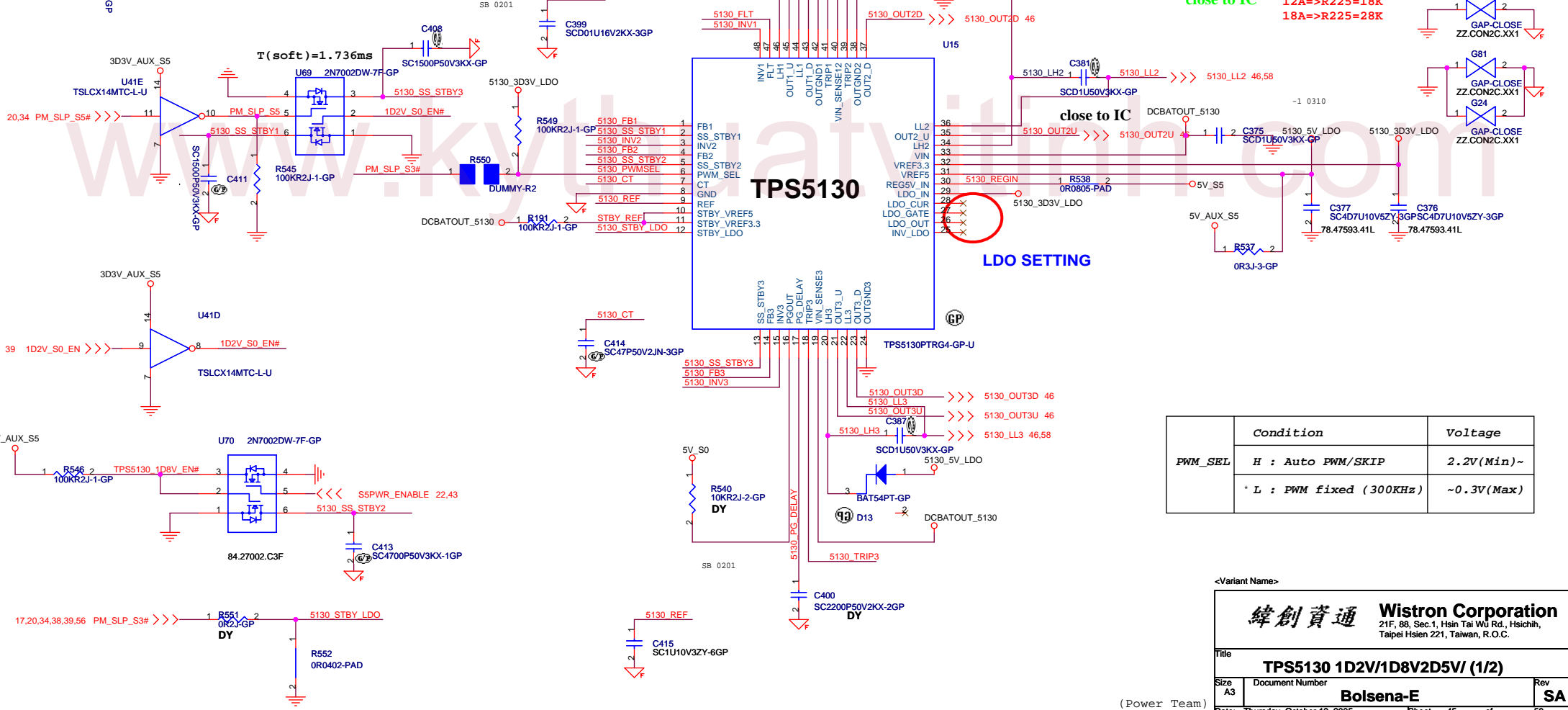


**TI TPS5130 for 2.5V, 1.2V, 1.8V**  
 $V_o = (R1 \cdot 0.85) / R2 + 0.85$   
 (1D2V=>CH1 , 1D8V=>CH2 , 2D5V =>CH3)

For 1.8V  
SETTING=1.8275V



	Condition	Voltage
PWM_SEL	H : Auto PWM/SKIP	2.2V(Min)~
	* L : PWM fixed (300KHz)	~0.3V(Max)



**LDO SETTING**

	Condition	Voltage
PWM_SEL	H : Auto PWM/SKIP	2.2V(Min)~
	* L : PWM fixed (300KHz)	~0.3V(Max)

<Variant Name>

**緯創資通 Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **TPS5130 1D2V/1D8V2D5V/ (1/2)**

Size A3 Document Number **Bolsena-E** Rev **SA**

Date: Thursday, October 13, 2005 Sheet 45 of 58

# TI TPS5130 for 1D2V, 1D8V, 1D8V

(1D2V=>CH1 , 1D8V=>CH2 , 2D5V =>CH3)

D

45 5130\_OUT1U  
45,58 5130\_LL1

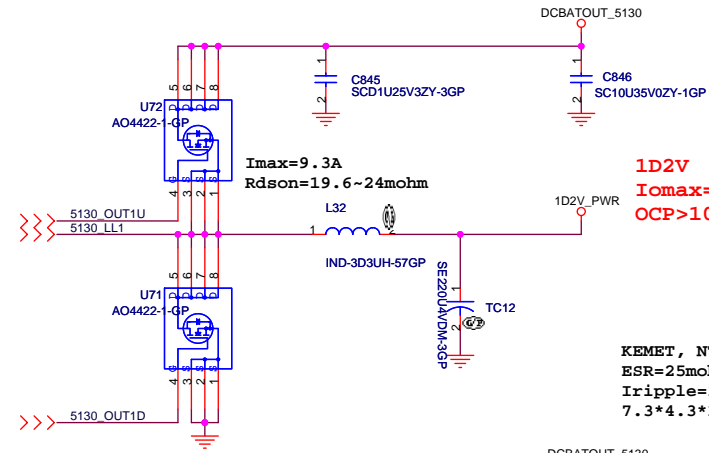
45 5130\_OUT1D

45 5130\_OUT2U  
45,58 5130\_LL2

45 5130\_OUT2D

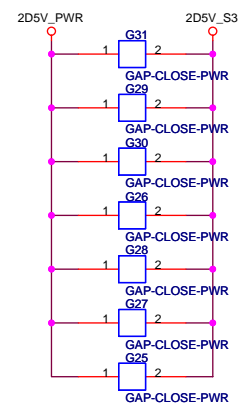
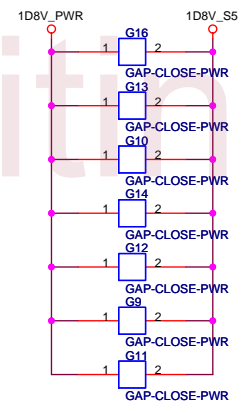
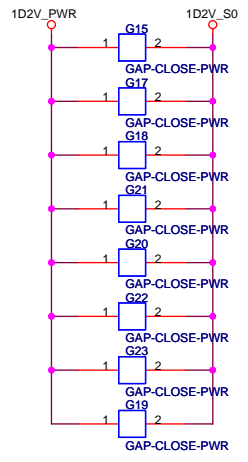
45 5130\_OUT3U  
45,58 5130\_LL3

45 5130\_OUT3D



**1D2V**  
**I<sub>omax</sub>=5A**  
**OCP>10A**

**KEMET, NTD:10.5 (Q1)**  
**ESR=25mohm**  
**I<sub>ripple</sub>=2.2A**  
**7.3\*4.3\*1.9**



C

B

A

D

C

B

A

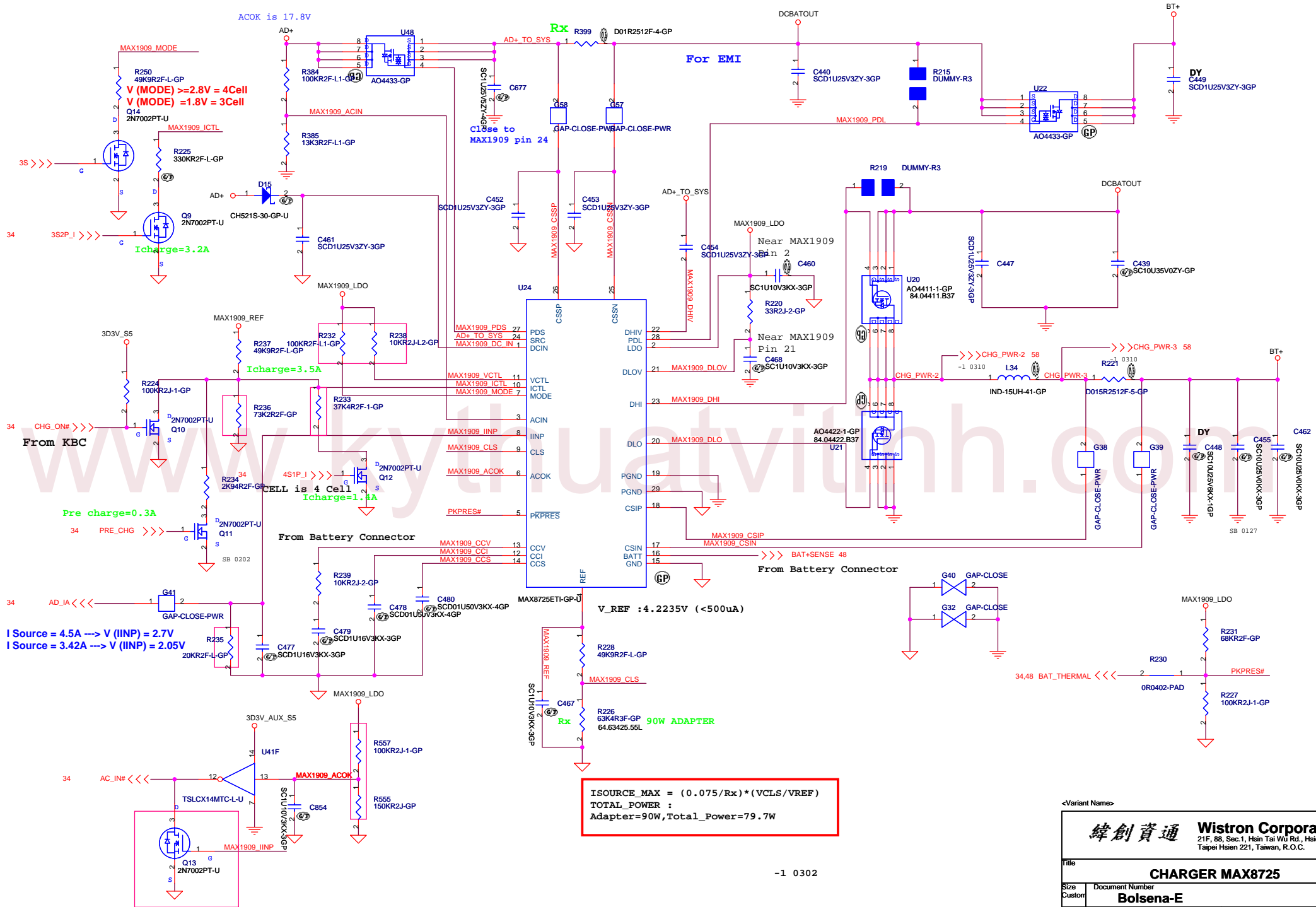
www.kyathuatvith.com

(Power Team)

<Variant Name>

<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>TPS5130 1D2V/1D8V/2D5V/ (2/2)</b>			
Size A3	Document Number	Bolsena-E	
Date: Thursday, October 13, 2005		Sheet 46	of 58

AC\_IN Threshold 2.089V Max.  
 AC\_IN > 2.089V --> AC DETECT

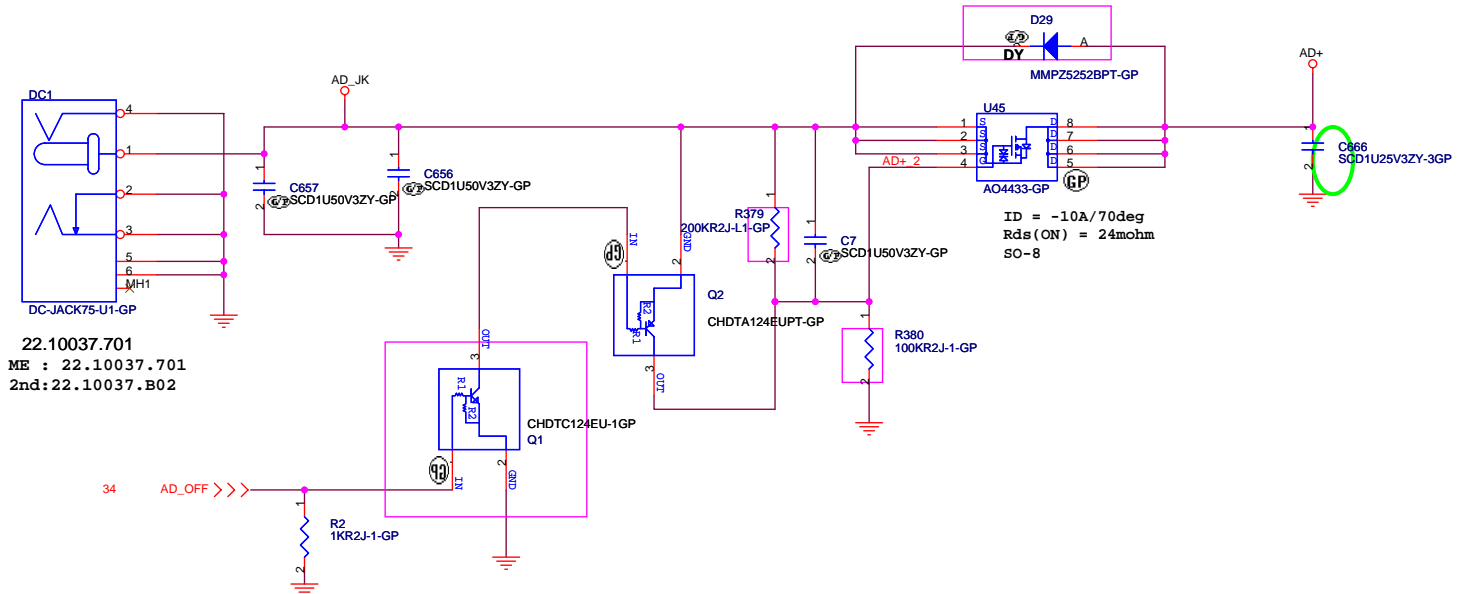


$$I_{SOURCE\_MAX} = (0.075/R_x) * (V_{CLS}/V_{REF})$$
**TOTAL\_POWER :**  
 Adapter=90W, Total\_Power=79.7W

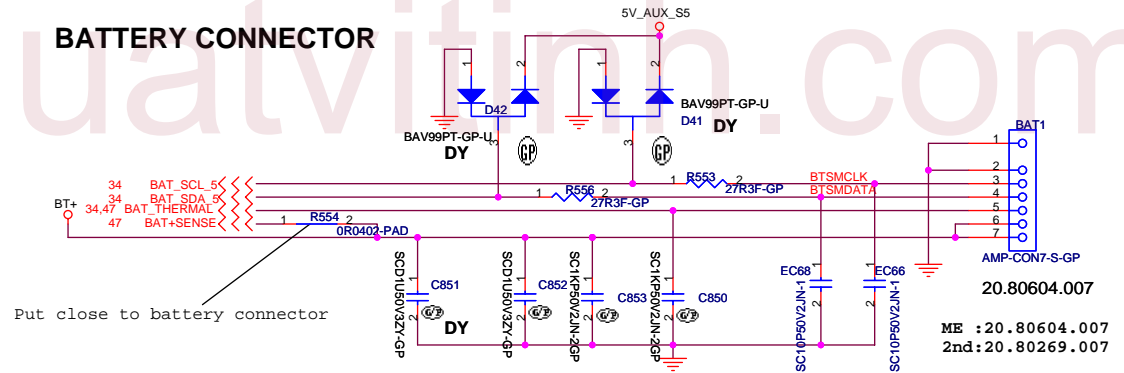
<b>緯創資通 Wistron Corporation</b>		
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
<b>CHARGER MAX8725</b>		
Title	Document Number	Rev
Size	<b>Bolsena-E</b>	SA
Custom		
Date: Thursday, October 13, 2005	Sheet 47 of	58



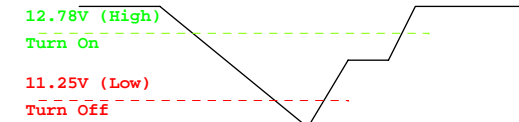
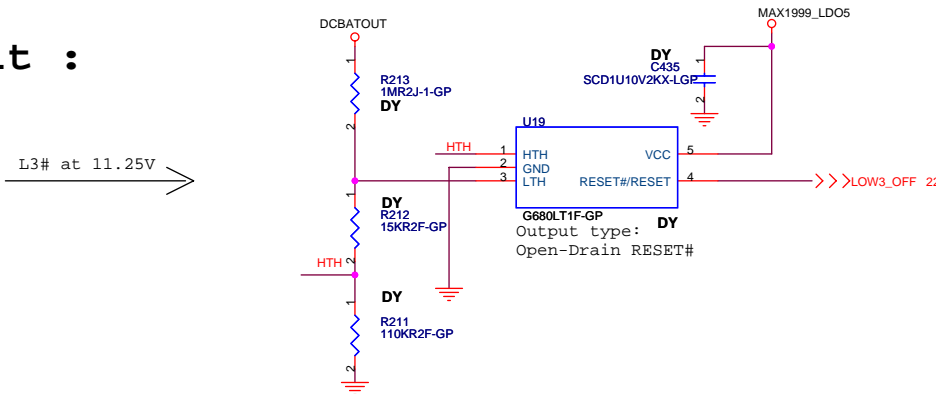
# Adaptor in to generate DCBATOUT



# BATTERY CONNECTOR

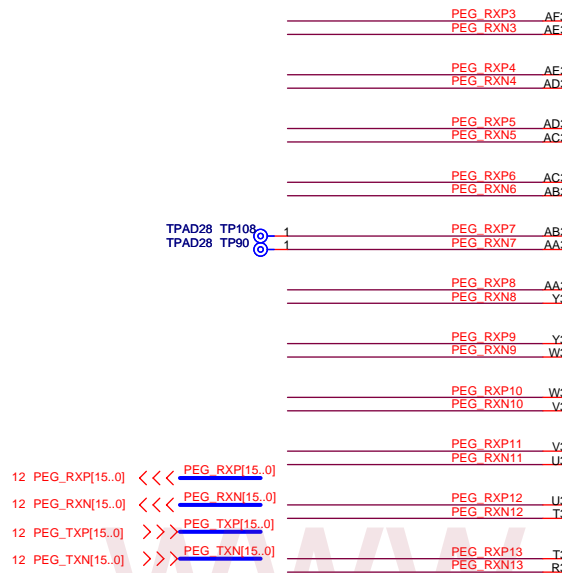


# Low3 Circuit :

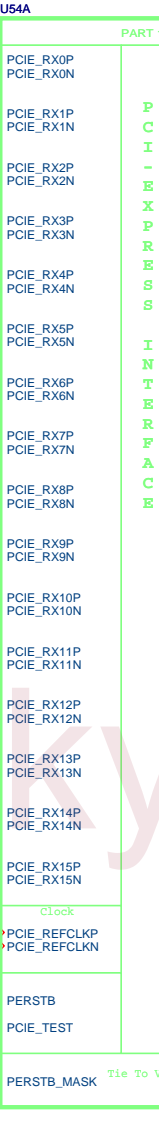
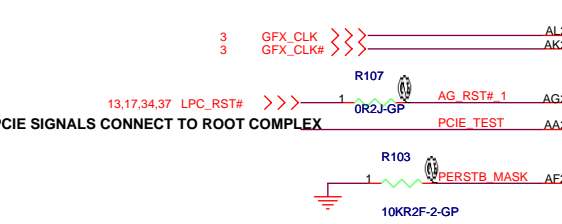


**PCIE TEST PADS**

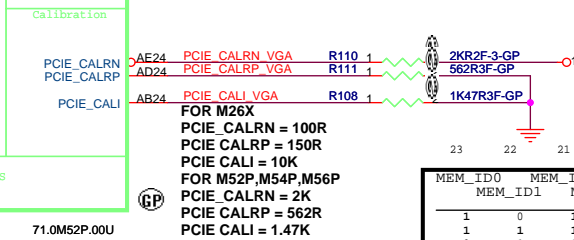
PCIE TEST POINTS MUST BE WITHIN 250 MILS OF THE ASIC BALL WITH POSITIVE AND NEGATIVE SIGNALS THE SAME DISTANCE



REFER TO PCI EXPRESS DESIGN GUIDE FOR RECOMMENDED AC COUPLING CAPS PLACEMENT ALONG THE TX INTERCONNECT



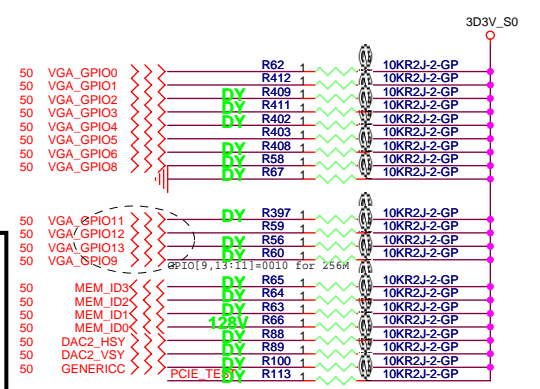
PCIE Pin	Chip Pin	Chip Pin	Strap	Strap Value	Strap Value	Strap Description	Strap Description
PCIE_RX0P	AJ31	AK27	C219	1	2	SCD1U16V2ZY-2GP	PEG_TXP0
PCIE_RX0N	AH31C	AJ27	C220	1	2	SCD1U16V2ZY-2GP	PEG_TXN0
PCIE_RX1P	AH30	AJ25	C200	1	2	SCD1U16V2ZY-2GP	PEG_TXP1
PCIE_RX1N	AG30C	AH25	C201	1	2	SCD1U16V2ZY-2GP	PEG_TXN1
PCIE_RX2P	AG32	AH28	C217	1	2	SCD1U16V2ZY-2GP	PEG_TXP2
PCIE_RX2N	AF32C	AG28	C218	1	2	SCD1U16V2ZY-2GP	PEG_TXN2
PCIE_RX3P	AF31	AG27	C198	1	2	SCD1U16V2ZY-2GP	PEG_TXP3
PCIE_RX3N	AE31C	AF27	C199	1	2	SCD1U16V2ZY-2GP	PEG_TXN3
PCIE_RX4P	AE30	AE25	C215	1	2	SCD1U16V2ZY-2GP	PEG_TXP4
PCIE_RX4N	AD30C	AE25	C216	1	2	SCD1U16V2ZY-2GP	PEG_TXN4
PCIE_RX5P	AD32	AE28	C196	1	2	SCD1U16V2ZY-2GP	PEG_TXP5
PCIE_RX5N	AC32C	AD28	C197	1	2	SCD1U16V2ZY-2GP	PEG_TXN5
PCIE_RX6P	AC31	AD27	C213	1	2	SCD1U16V2ZY-2GP	PEG_TXP6
PCIE_RX6N	AB31C	AD27	C214	1	2	SCD1U16V2ZY-2GP	PEG_TXN6
PCIE_RX7P	AB30	AC25	C194	1	2	SCD1U16V2ZY-2GP	PEG_TXP7
PCIE_RX7N	AA30C	AB25	C195	1	2	SCD1U16V2ZY-2GP	PEG_TXN7
PCIE_RX8P	AA32	AB28	C211	1	2	SCD1U16V2ZY-2GP	PEG_TXP8
PCIE_RX8N	Y32C	AA28	C212	1	2	SCD1U16V2ZY-2GP	PEG_TXN8
PCIE_RX9P	Y31	AA27	C192	1	2	SCD1U16V2ZY-2GP	PEG_TXP9
PCIE_RX9N	W31C	Y27	C193	1	2	SCD1U16V2ZY-2GP	PEG_TXN9
PCIE_RX10P	W30	Y25	C209	1	2	SCD1U16V2ZY-2GP	PEG_TXP10
PCIE_RX10N	V30C	W25	C210	1	2	SCD1U16V2ZY-2GP	PEG_TXN10
PCIE_RX11P	V32	W28	C190	1	2	SCD1U16V2ZY-2GP	PEG_TXP11
PCIE_RX11N	U32C	V28	C191	1	2	SCD1U16V2ZY-2GP	PEG_TXN11
PCIE_RX12P	U31	V27	C207	1	2	SCD1U16V2ZY-2GP	PEG_TXP12
PCIE_RX12N	T31C	U27	C208	1	2	SCD1U16V2ZY-2GP	PEG_TXN12
PCIE_RX13P	T30	U25	C188	1	2	SCD1U16V2ZY-2GP	PEG_TXP13
PCIE_RX13N	R30C	J25	C189	1	2	SCD1U16V2ZY-2GP	PEG_TXN13
PCIE_RX14P	R32	T28	C205	1	2	SCD1U16V2ZY-2GP	PEG_TXP14
PCIE_RX14N	P32C	R28	C206	1	2	SCD1U16V2ZY-2GP	PEG_TXN14
PCIE_RX15P	P31	R27	C186	1	2	SCD1U16V2ZY-2GP	PEG_TXP15
PCIE_RX15N	N31C	P27	C187	1	2	SCD1U16V2ZY-2GP	PEG_TXN15



FOR M26X  
PCIE\_CALRN = 100R  
PCIE\_CALRP = 150R  
PCIE\_CALI = 10K  
FOR M52P, M54P, M56P  
PCIE\_CALRN = 2K  
PCIE\_CALRP = 562R  
PCIE\_CALI = 1.47K

MEM_ID0	MEM_ID1	MEM_ID2	MEM_ID3	MEM	SIZE	VENDOR	CHIPS
1	0	1	0	64M	16M*16	Infineon	x2
1	1	1	0	64M	16M*16	Hynix	x2
0	1	1	0	128M	16M*16	Samsung	x4
0	0	1	0	256M	32M*16	Infineon	x4
0	1	0	0	128M	16M*16	Infineon	x4
0	1	0	0	256M	32M*16	Infineon	x4
1	1	0	0	128M	16M*16	Hynix	x4
0	0	0	0	256M	32M*16	Hynix	x4

STRAPS	PIN	DESCRIPTION OF RECOMMENDED SETTING	RECOMMENDED
STRAP_B_PTX_PWRS_ENB	GPIO0	TRANSMITTER POWER SAVINGS ENABLE - FULL TX OUTPUT SWING	INSTALL 10K RESISTOR
STRAP_B_PTX_DEEMPH_EN	GPIO1	TRANSMITTER DE-EMPHASIS ENABLE DEPENDS ON PCIE CHIPSET BEING USED FOR M26X, M5X INSTALL WITH ATI RS480, RS400, RX480, RC410, RS482 CHIPSETS FOR M26X ONLY DO NOT INSTALL WITH INTEL 915PM CHIPSET	TBD
RSVD	GPIO(3:2)	NO ATI FEATURE ENABLED	DO NOT INSTALL 10K RESISTORS
REVERSE LANES	GPIO4	NOT REVERSED LANE (M26X)	DO NOT INSTALL 10K RESISTOR
DEBUG ACCESS	GPIO5	NO DEBUG ACCESS (M52P, M54P, M56P)	DO NOT INSTALL 10K RESISTORS
STRAP_FORCE_COMPLIANCE	GPIO5	DO NOT FORCE COMPLIANCE STATE QUICKLY (M26X) NO ATI FEATURE ENABLED (M52P, M54P, M56P)	INSTALL 10K RESISTORS
COMMON MODE RANGE	GPIO6	NORMAL RANGE (M26X)	DO NOT INSTALL 10K RESISTORS
RSVD	GPIO6	NO ATI FEATURE ENABLED (M52P, M54P, M56P)	DO NOT INSTALL 10K RESISTORS
DEBUG ACCESS	GPIO8	NO DEBUG ACCESS (M26X)	DO NOT INSTALL 10K RESISTORS
FORCE_COMPLIANCE	GPIO8	DON'T FORCE COMPLIANCE STATE (M52P, M54P, M56P)	DO NOT INSTALL 10K RESISTORS
ROMIDFCG(3:0)	GPIO[9,13:11]	SERIAL FLASH ROM TYPE (M26X, M52P, M54P, M56P) - SERIAL M25P10 ROM	1011
MEMORY APERTURE SIZE	GPIO[13:11]	IF NO ROM GPIO11 (M26X) AND GPIO12,13 (M52, M54, M56) SET MEMORY APERTURE SIZE - SEE M26X, M54X, M56X DATA BOOK FOR MEMORY, FRAME BUFFER APERTURE SETTINGS	TBD
MEM_TYPE	MEMID(3:0)	MEMORY TYPE AND SPEED SELECT	TBD
RSVD	H2SYNC V2SYNC GENERIC	ATI FEATURE NOT ENABLED (M52P, M54P, M56P)	DO NOT INSTALL 10K RESISTORS
NO STRAP FUNCTION	NO STRAP	NO STRAP (M26X)	
RSVD	PCIE_TEST	ATI FEATURE NOT ENABLED (M52P, M54P, M56P)	
NO STRAP FUNCTION	NO STRAP	NO STRAP (M26X)	



When no ROM is attached, GPIO[9] is set to 0.  
GPIO[13:12] is used to select the frame buffer aperture size.  
GPIO[13:12] = 00: 128M frame buffer, same as ROM strap 00  
GPIO[13:12] = 01: 256M frame buffer, same as ROM strap 01  
GPIO[13:12] = 10: 64M frame buffer, same as ROM strap 10  
GPIO[13:12] = 11: reserved, same as ROM strap 11

<Variant Name>

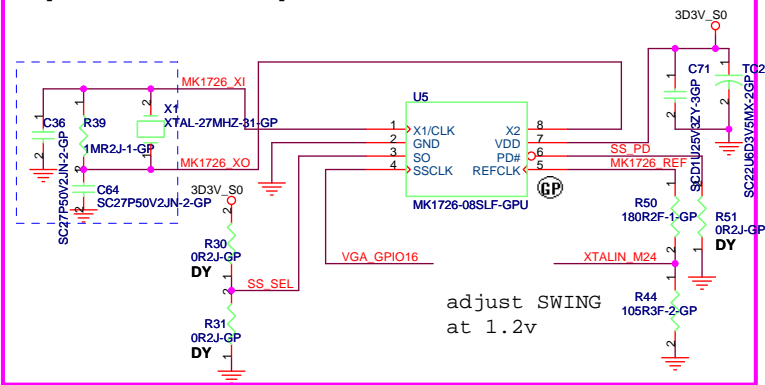
**緯創資通 Wistron Corporation**  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **ATI M5X-P PCIE 1/4**

Size: A3 Document Number: **AG1** Rev: SA

Date: Thursday, October 13, 2005 Sheet: 49 of 58

[USE ICS MK1726-08]



adjust SWING  
at 1.2v

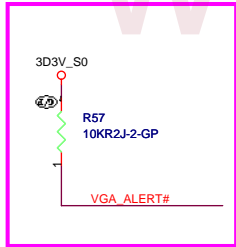
DVPCNTL,DVPDATA[23..0]  
ARE CONFIGURED FOR  
+3.3V SIGNALING MODE  
ON THIS DESIGN

Modulation Rate		
SEL1	SEL0	Center Spread
L	L	+/-0.5%
L	H	+/-1.0%
H	L	+/-1.5%
H	H	No Spread

FOR M26X  
CONNECT TO +1.8V OR VSS  
TO DEFINE DVO SIGNAL LEVEL  
FOR M52P,M54P,M56P  
NOT CONNECTED

ANY UNUSED GPIO CAN OPTIONALLY BE  
PANEL TYPE CONFIG STRAPS

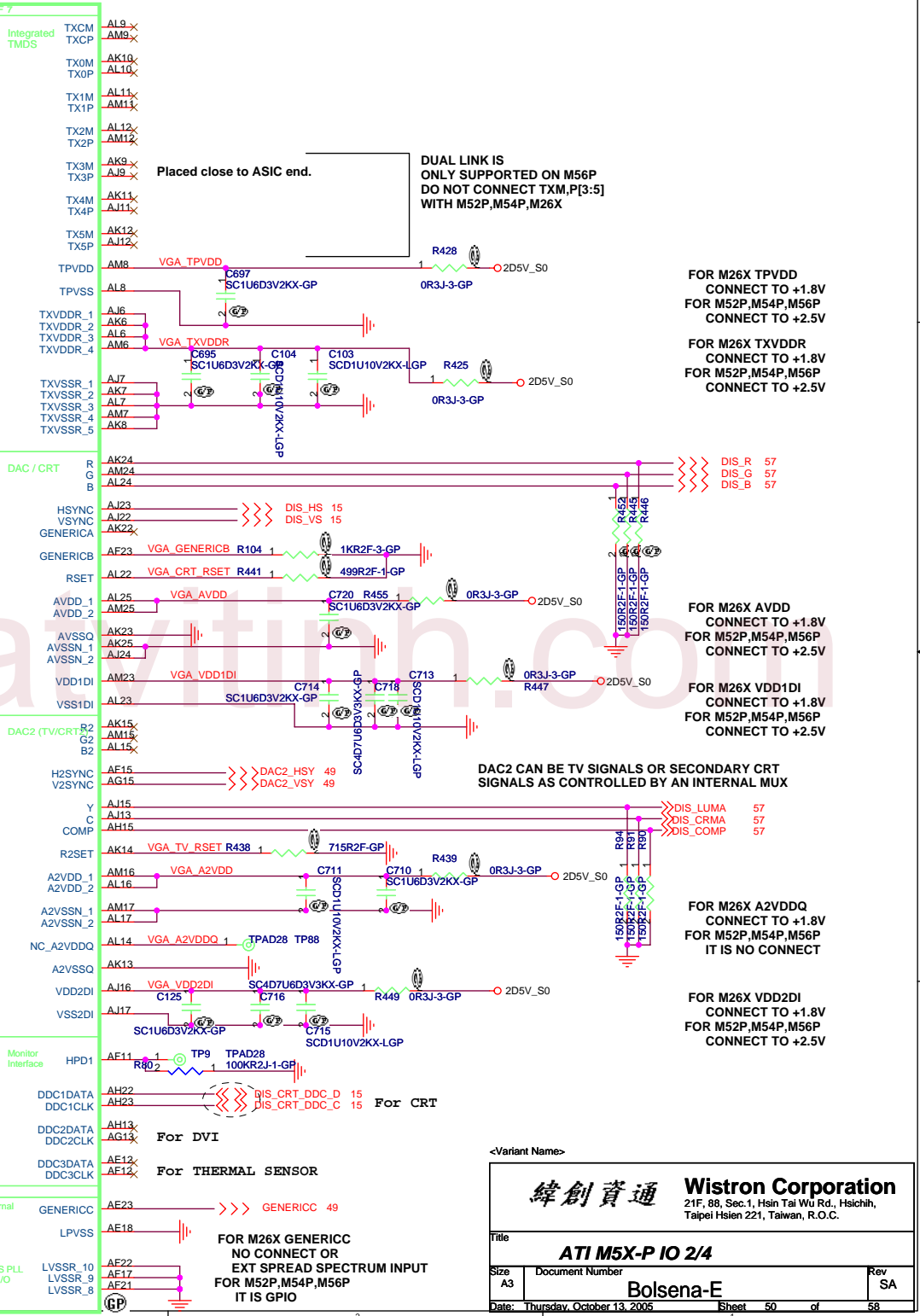
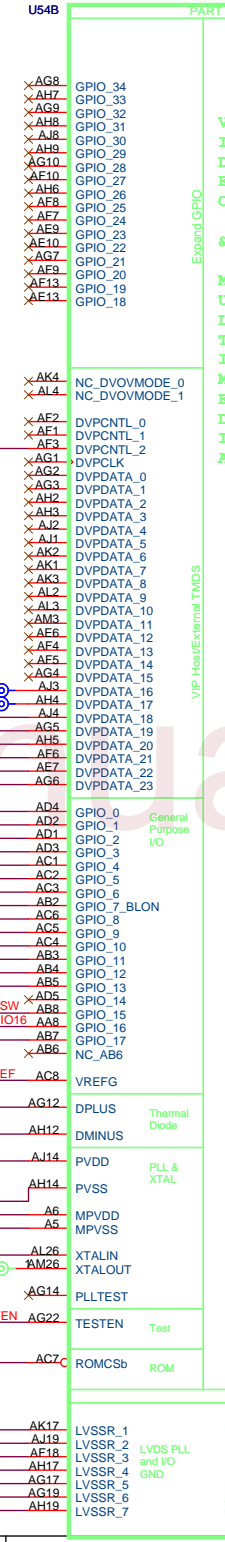
ANY UNUSED GPIO CAN OPTIONALLY BE  
MEMORY TYPE CONFIG STRAPS



FOR M26X PVDD  
CONNECT TO +1.8V  
FOR M52P,M54P,M56P  
CONNECT TO +2.5V

FOR M26X MPVDD  
CONNECT TO +1.8V  
FOR M52P,M54P,M56P  
CONNECT TO VDDC

VOLTAGE DIVIDER 3.3V MEM SS  
MODOUT TO 1.2V XTALIN/OUT  
adjust SWING at 1.2v



Placed close to ASIC end.  
DUAL LINK IS  
ONLY SUPPORTED ON M56P  
DO NOT CONNECT TXM,P[3:5]  
WITH M52P,M54P,M26X

FOR M26X TPVDD  
CONNECT TO +1.8V  
FOR M52P,M54P,M56P  
CONNECT TO +2.5V

FOR M26X TXVDDR  
CONNECT TO +1.8V  
FOR M52P,M54P,M56P  
CONNECT TO +2.5V

FOR M26X AVDD  
CONNECT TO +1.8V  
FOR M52P,M54P,M56P  
CONNECT TO +2.5V

FOR M26X VDD1DI  
CONNECT TO +1.8V  
FOR M52P,M54P,M56P  
CONNECT TO +2.5V

DAC2 CAN BE TV SIGNALS OR SECONDARY CRT  
SIGNALS AS CONTROLLED BY AN INTERNAL MUX

FOR M26X A2VDDQ  
CONNECT TO +1.8V  
FOR M52P,M54P,M56P  
IT IS NO CONNECT

FOR M26X VDD2DI  
CONNECT TO +1.8V  
FOR M52P,M54P,M56P  
CONNECT TO +2.5V

For CRT  
For DVI  
For THERMAL SENSOR

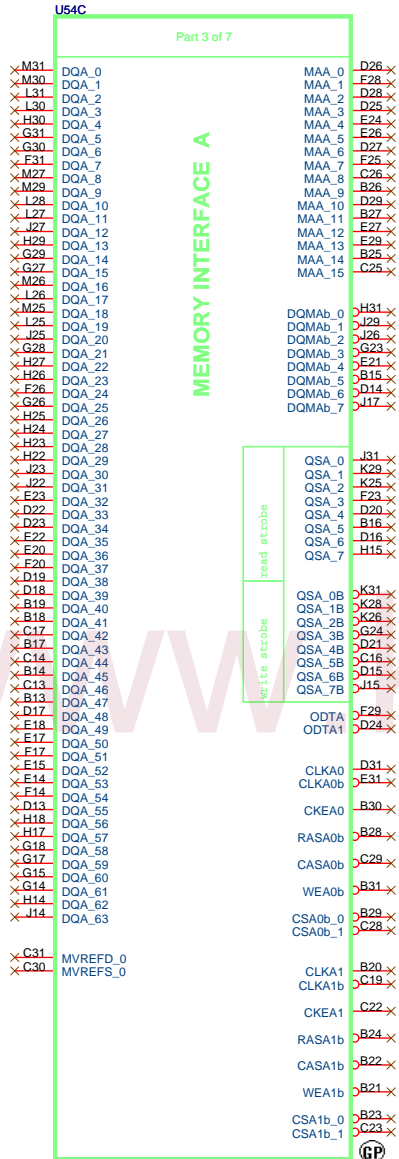
FOR M26X GENERICC  
NO CONNECT OR  
EXT SPREAD SPECTRUM INPUT  
FOR M52P,M54P,M56P  
IT IS GPIO

Wistron Corporation  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

ATI M5X-P IO 2/4

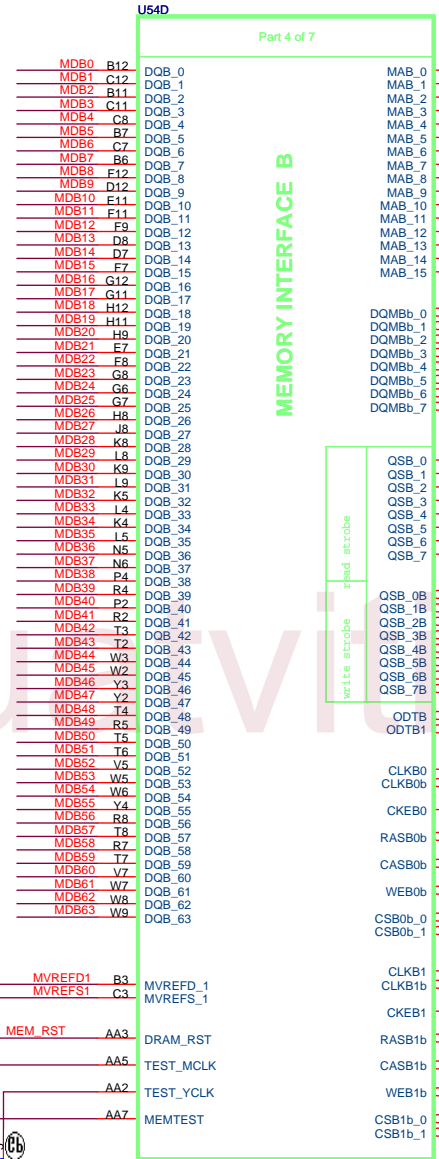
Bolsena-E

Date: Thursday, October 13, 2005 Sheet 50 of 58



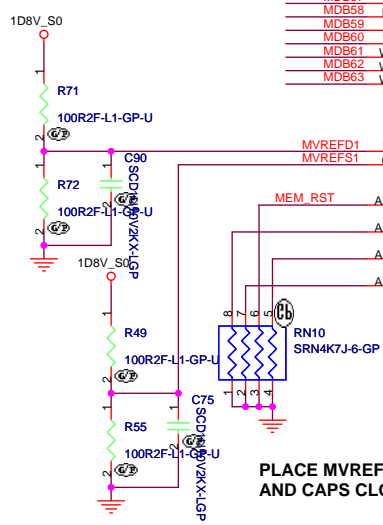
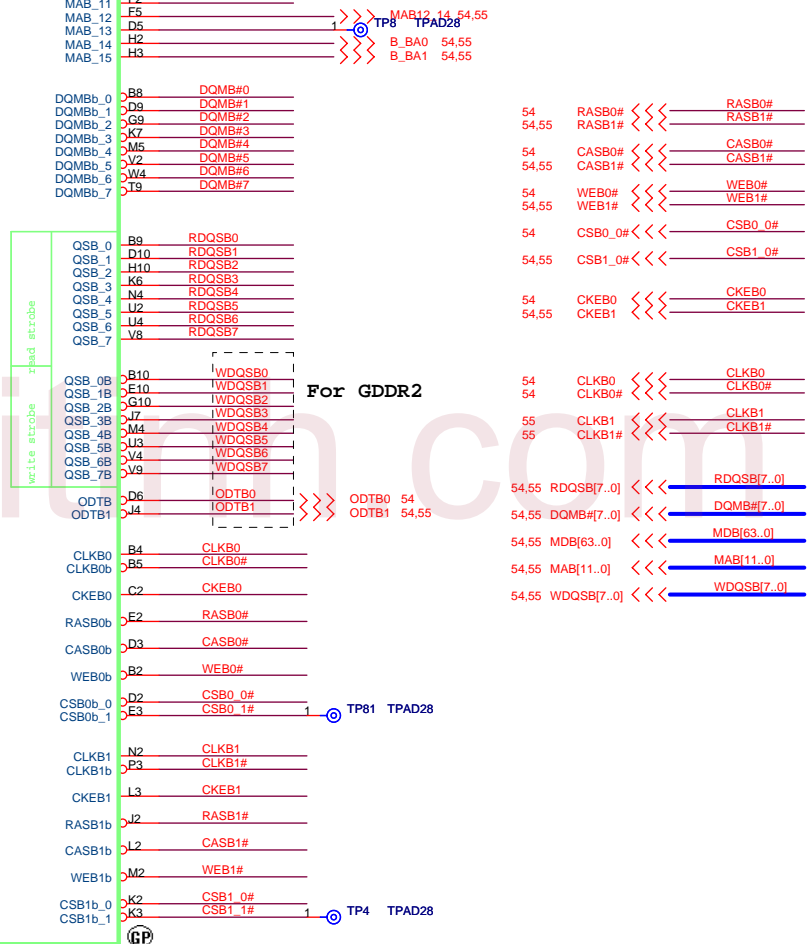
Ch-A  
FOR M52P,M54P,M26X  
PIN B25 IS MA12 (BA0)  
PIN C25 IS MA13 (BA1)  
PIN E29 IS MA15 (BA2)  
PIN E27 IS MA14

FOR M56P  
PIN B25 IS MA14 (BA0)  
PIN C25 IS MA15 (BA1)  
PIN E29 IS MA13 (BA2)  
PIN E27 IS MA12



Ch-B  
FOR M52P,M54P,M26X  
PIN H2 IS MAB12 (BA0)  
PIN H3 IS MAB15 (BA1)  
PIN D5 IS MAB15 (BA2)  
PIN F5 IS MAB14

FOR M56P  
PIN H2 IS MA14 (BA0)  
PIN H3 IS MA15 (BA1)  
PIN D5 IS MA13 (BA2)  
PIN F5 IS MAB12



PLACE MVREF DIVIDERS AND CAPS CLOSE TO ASIC

PLACE MVREF DIVIDERS AND CAPS CLOSE TO ASIC

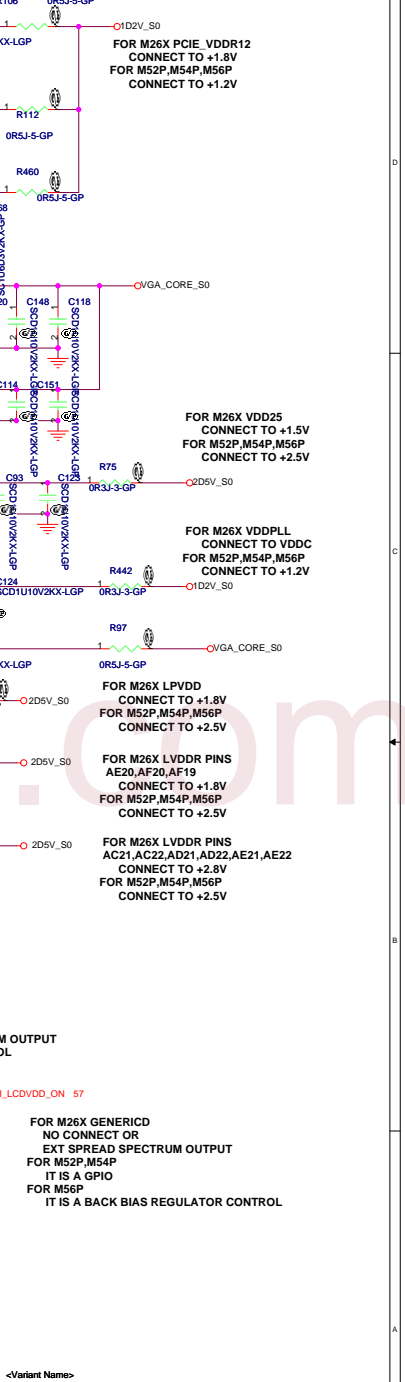
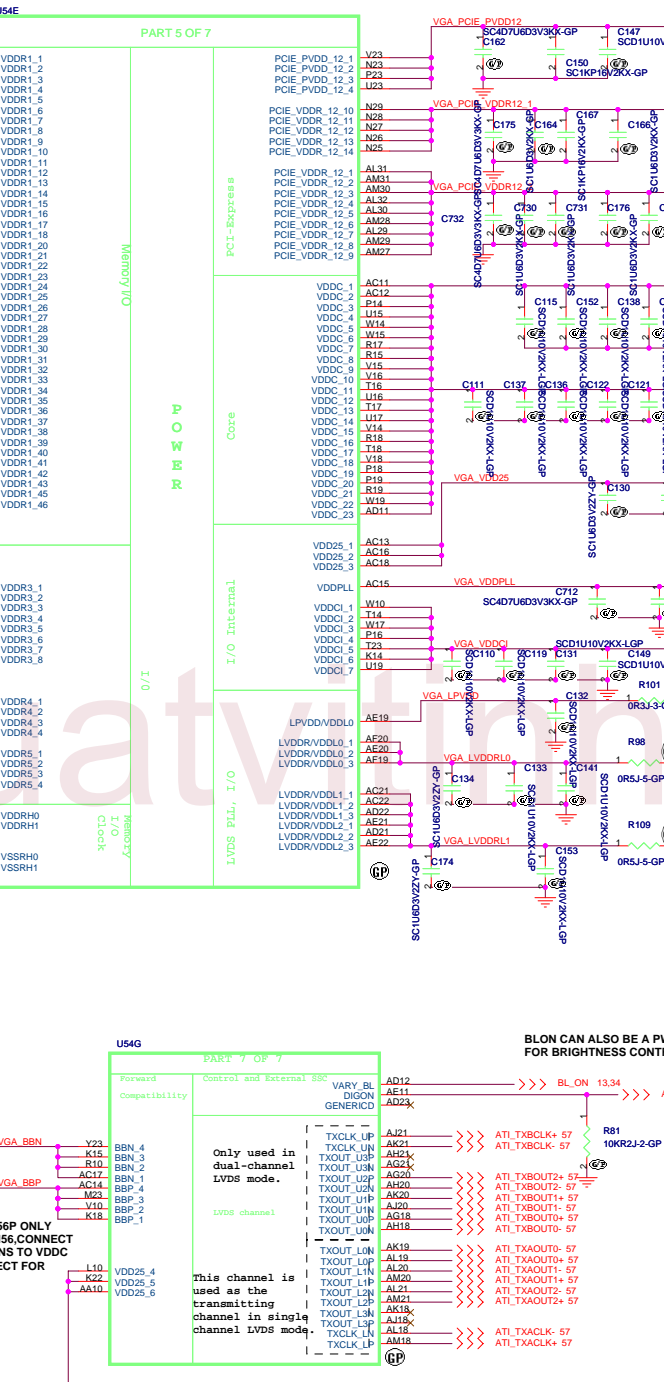
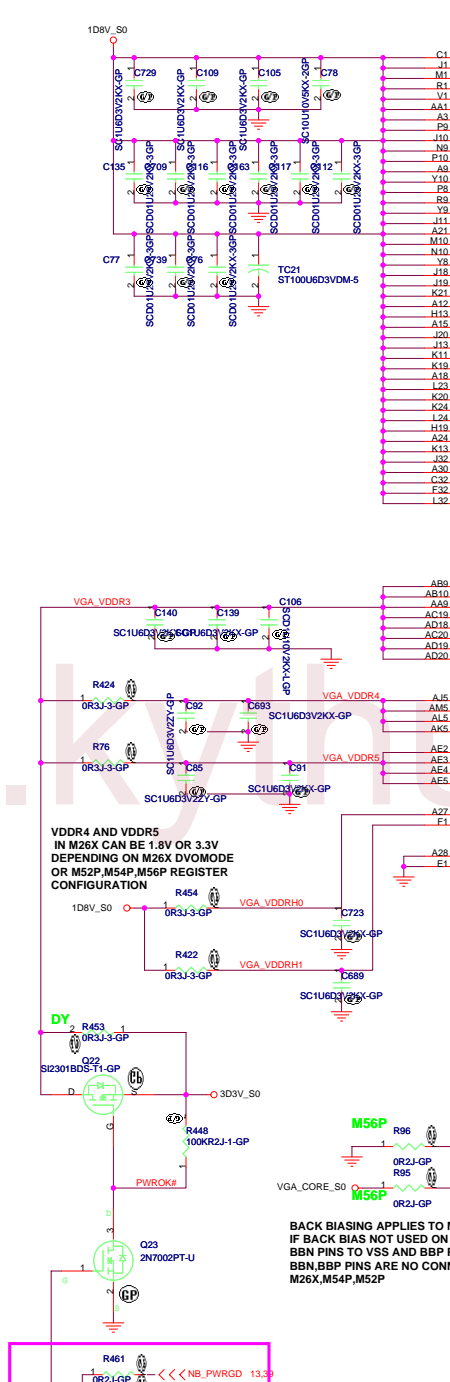
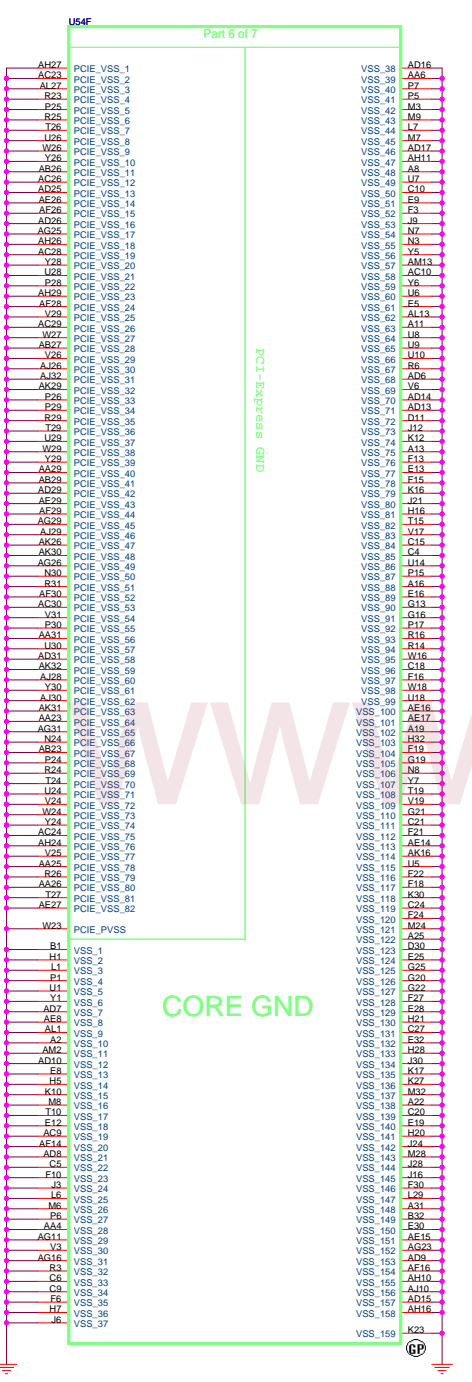
<Variant Name>

**緯創資通 Wistron Corporation**  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **ATI M5X-P MEM 3/4**

Size: A3 Document Number: **Bolsena-E** Rev: SA

Date: Thursday, October 13, 2005 Sheet: 51 of 58



**VDDR4 AND VDDR5 IN M26X CAN BE 1.8V OR 3.3V DEPENDING ON M26X DVOMODE OR M52P, M54P, M56P REGISTER CONFIGURATION**

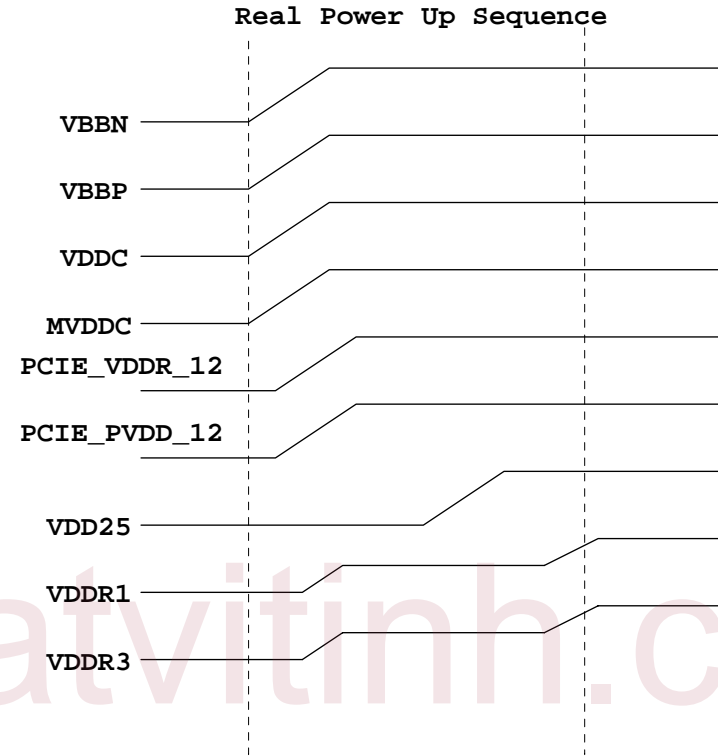
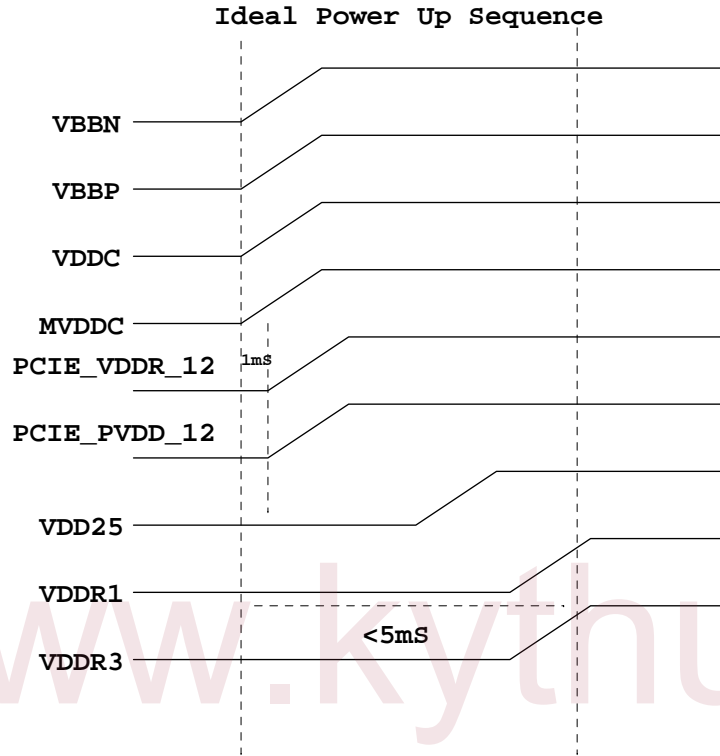
**BACK BIASING APPLIES TO M56P ONLY IF BACK BIAS NOT USED ON M56. CONNECT BBN, BBP PINS TO VSS AND BBP PINS ARE NO CONNECT FOR M26X, M54P, M52P**

**CONNECT THESE VDD25 PINS TO 2.5V FOR M52P, M54P, M56P THESE VDD25 PINS ARE NO CONNECT FOR M26X**

**BLON CAN ALSO BE A PWM OUTPUT FOR BRIGHTNESS CONTROL**

**FOR M26X GENERIC NO CONNECT OR EXT SPREAD SPECTRUM OUTPUT FOR M52P, M54P IT IS A GPIO FOR M56P IT IS A BACK BIAS REGULATOR CONTROL**





www.kythuathinh.com

**RESISTOR**

Symbol name	Value	Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1%)	Rating 0402=> 1/16W, 25V 0603 => 1/16W, 75V 0805 => 1/10W, 100V	Size 2=>0402, 3=>0603, 5=>0805 6=>1206, 0=>1210
10KR3	10K Ohm	If no letter, it means J: 5%	1/16W, 75V	0603
33D3R5	33.3 Ohm	If no letter, it means J: 5%	1/10W, 100V	0805
1KR3F	1K Ohm	F: 1%	1/16W, 75V	0603

The naming rule is value + R + size + tolerance  
 For the value, it can be read by the number before R. (R means resistor)  
 For the tolerance, it can be read from the last letter.  
 For the rating, we don't show on the symbol name.  
 For the size, R2=>0402, R3=>0603, R5=>0805,....

**General Guidelines:**

- BBN and BBP must ramp up before or at the same time as VDDC but not after.
- VDDC and MVDDC must be ramped up first, followed by PCIE\_VDDR\_12, PCIE\_PVDD12, VDD25, VDDR1 and VDDR3 (and other I/O powers).
- All powers must be ramped up within 5ms of each other (from the ramp of VDDC to 90% of VDDR3).
- VDD25 can be ramped with VDDC or VDDR1 but it cannot be ramped later than VDDR1.
- The power down is the opposite of the power on sequence: VDDR3/VDDR1 -> VDD25 ->VDDC/MVDDC/BBN/BBP

Due to the level shifter design in the memory I/Os, in order to avoid over-stressing the thin oxide transistors when VDDR1 is powered on but VDDC is not, VDDC must ramp up before VDDR1. Similarly, VDDC must ramp up before VDDR3. The level shifter design is a function of the transistor types used in 90nm technology and of the voltage level support. The drawback of ramping up VDDC before the I/O voltages (such as VDDR1 and VDDR3) is that parasitic P/N junctions are forward biased, thus creating a conduction path. These conduction paths will pump up VDDR1 (from the memory I/Os) and VDDR3 (from the GPIOs).

The real power up sequence will appear as follows:

Figure 2-2. Real Power Up Sequence

As long as MVDDC ramps up with VDDC, the pump voltage on VDDR1 should be all right since the DRAM spec will not be violated.

**CAPACITOR**

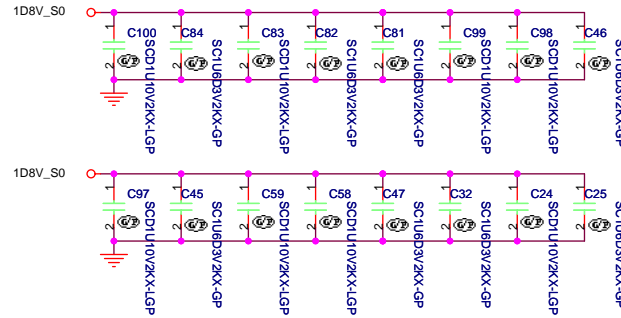
Symbol name	Value	Tolerance (J: +/-5, K: +/-10, M: +/-20, Z: +80/-20)	Rating ( X5R / X7R < 80%, Y5V/Y5U/Z5U < 1/3 )	Size 2=>0402, 3=>0603, 5=>0805 6=>1206, 0=>1210
SCD1U10V2MX-1	0.1uF	M/X5R	10V	0402
SC10U6D3V5MX	10uF	M/X5R	6.3V	0805
SC2D2U16V5ZY	2.2uF	Z/Y5V	16V	0805

The naming rule is Capacitor type + value + rating + size + tolerance + material  
 SCD1U10V2MX-1  
 SC=> SMT Ceramic, TC=> POS cap or SP cap  
 D1U => 0.1uF  
 10V => the voltage rating is 10V  
 2=> 0402, 3=>0603, 5=>0805  
 M=>tolerance J, K, M, Z  
 X=> X7R/X5R, Y=> Y5V  
 -1 => symbol version, nonsense to EE characteristic

<Variant Name>

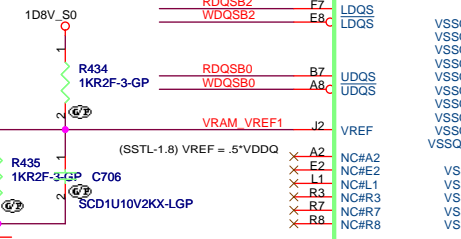
<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wji Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>ATI M5X-P POWER SEQUENCE</b>			
Size A3	Document Number	<b>Bolsena-E</b>	
Date: Thursday, October 13, 2005	Sheet 53	of	58

# CHAN B DDR2 84BGA 32MX16 MEMORY



51.55	B_BA0	L2	BA0
51.55	B_BA1	L3	BA1
51.55	MAB12_1D	R2	A12
		P7	A11
		M2	A10/AP
		P3	A9
		P8	A8
		P2	A7
		N7	A6
		N3	A5
		N8	A4
		N2	A3
		M7	A2
		M3	A1
		M8	A0

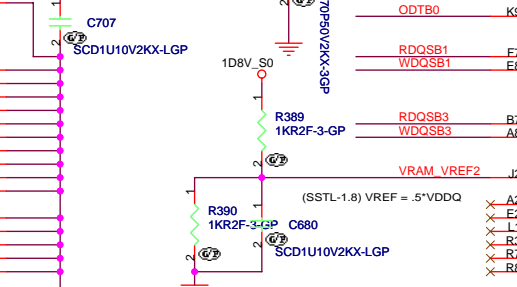
	CLKB0#	K8	CK
	CLKB0	J8	CK
	CKEB0	K2	CKE
	CSB0_0#	L8	CS
	WEB0#	K3	WE
	RASB0#	K7	RAS
	CASB0#	L7	CAS
	DQMB#2	F3	LDM
	DQMB#0	B3	UDM
	ODTB0	K9	ODT
	RDQSB2	F7	LDQS
	WDQSB2	E8	LDQS
	RDQSB0	B7	UDQS
	WDQSB0	A8	UDQS
	VRAM_VREF1	J2	VREF



HY5PS561621A-25GP  
72.55616.C0U

B_BA0	L2	BA0	DQ15
B_BA1	L3	BA1	DQ14
		D9	DQ13
		D1	DQ12
		D3	DQ11
		D7	DQ10
		C2	DQ9
		C8	DQ8
		F9	DQ7
		F1	DQ6
		H9	DQ5
		H3	DQ4
		H7	DQ3
		G2	DQ2
		G8	DQ1
		DQ0	DQ0

A9	VDDQ1	A8	VDDQ1
C1	VDDQ2	C3	VDDQ2
C7	VDDQ3	C9	VDDQ3
E9	VDDQ4	E7	VDDQ4
G1	VDDQ5	G3	VDDQ5
G7	VDDQ6	G9	VDDQ6
A1	VDDQ7	A3	VDDQ7
E1	VDDQ8	E3	VDDQ8
J9	VDDQ9	J7	VDDQ9
M9	VDDQ10	M7	VDDQ10
A7	VDDQ11	A5	VDDQ11
B2	VDDQ12	B4	VDDQ12
D8	VDDQ13	D6	VDDQ13
D2	VDDQ14	D4	VDDQ14
D6	VDDQ15	D4	VDDQ15
E7	VDDQ16	E5	VDDQ16
F2	VDDQ17	F4	VDDQ17
F8	VDDQ18	F6	VDDQ18
H2	VDDQ19	H4	VDDQ19
H8	VDDQ20	H6	VDDQ20
A2	VSSQ1	A4	VSSQ1
E2	VSSQ2	E4	VSSQ2
L1	VSSQ3	L3	VSSQ3
R3	VSSQ4	R2	VSSQ4
R7	VSSQ5	R6	VSSQ5
R8	VSSQ6	R7	VSSQ6
A2	VSSQ7	A4	VSSQ7
E2	VSSQ8	E4	VSSQ8
L1	VSSQ9	L3	VSSQ9
R3	VSSQ10	R2	VSSQ10
R7	VSSQ11	R6	VSSQ11
R8	VSSQ12	R7	VSSQ12
A2	VSSQ13	A4	VSSQ13
E2	VSSQ14	E4	VSSQ14
L1	VSSQ15	L3	VSSQ15
R3	VSSQ16	R2	VSSQ16
R7	VSSQ17	R6	VSSQ17
R8	VSSQ18	R7	VSSQ18

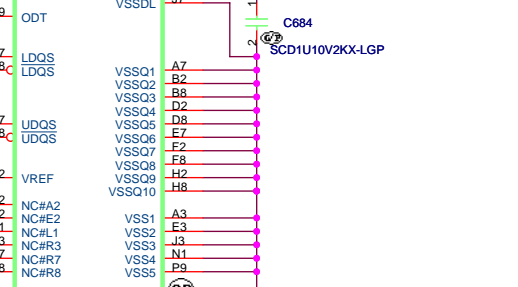


HY5PS561621A-25GP  
72.55616.C0U

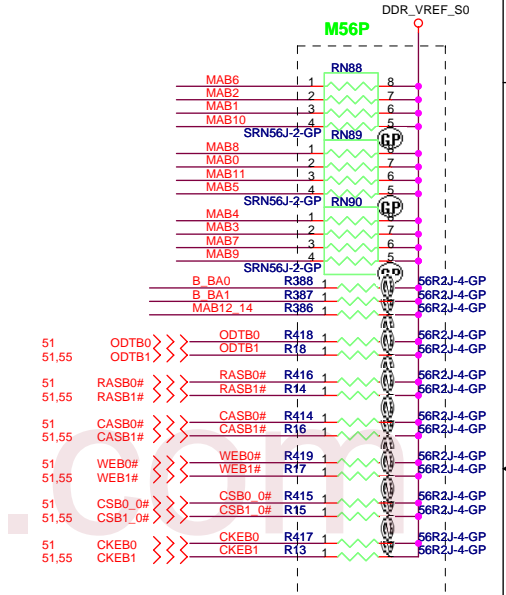
72.55616.C0U IC VRAM HY5PS561621AFP-25 FBGA(16M\*16, 400Mhz)  
72.51216.D0U IC VRAM HY5PS121621BFP-25 FBGA(32M\*16, 400Mhz)

B_BA0	L2	BA0	DQ15
B_BA1	L3	BA1	DQ14
		D9	DQ13
		D1	DQ12
		D3	DQ11
		D7	DQ10
		C2	DQ9
		C8	DQ8
		F9	DQ7
		F1	DQ6
		H9	DQ5
		H3	DQ4
		H7	DQ3
		G2	DQ2
		G8	DQ1
		DQ0	DQ0

A9	VDDQ1	A8	VDDQ1
C1	VDDQ2	C3	VDDQ2
C7	VDDQ3	C9	VDDQ3
E9	VDDQ4	E7	VDDQ4
G1	VDDQ5	G3	VDDQ5
G7	VDDQ6	G9	VDDQ6
A1	VDDQ7	A3	VDDQ7
E1	VDDQ8	E3	VDDQ8
J9	VDDQ9	J7	VDDQ9
M9	VDDQ10	M7	VDDQ10
A7	VDDQ11	A5	VDDQ11
B2	VDDQ12	B4	VDDQ12
D8	VDDQ13	D6	VDDQ13
D2	VDDQ14	D4	VDDQ14
D6	VDDQ15	D4	VDDQ15
E7	VDDQ16	E5	VDDQ16
F2	VDDQ17	F4	VDDQ17
F8	VDDQ18	F6	VDDQ18
H2	VDDQ19	H4	VDDQ19
H8	VDDQ20	H6	VDDQ20
A2	VSSQ1	A4	VSSQ1
E2	VSSQ2	E4	VSSQ2
L1	VSSQ3	L3	VSSQ3
R3	VSSQ4	R2	VSSQ4
R7	VSSQ5	R6	VSSQ5
R8	VSSQ6	R7	VSSQ6
A2	VSSQ7	A4	VSSQ7
E2	VSSQ8	E4	VSSQ8
L1	VSSQ9	L3	VSSQ9
R3	VSSQ10	R2	VSSQ10
R7	VSSQ11	R6	VSSQ11
R8	VSSQ12	R7	VSSQ12
A2	VSSQ13	A4	VSSQ13
E2	VSSQ14	E4	VSSQ14
L1	VSSQ15	L3	VSSQ15
R3	VSSQ16	R2	VSSQ16
R7	VSSQ17	R6	VSSQ17
R8	VSSQ18	R7	VSSQ18



HY5PS561621A-25GP  
72.55616.C0U



FOR M56P AT DDR2 MEMORY SPEEDS ABOVE 350MHZ  
MEMORY CONTROL SIGNALS WE,CAS,RAS,CS,CKE,ODT  
AND MEMORY ADDRESS SIGNALS REQUIRE 55 OHM PULLUP  
TO A VTT RAIL (50% OF VDDQ)

51	CLKB0	>>>	CLKB0
51	CLKB0#	>>>	CLKB0#
51,55	RDQSB[7..0]	>>>	RDQSB[7..0]
51,55	DQMB#[7..0]	>>>	DQMB#[7..0]
51,55	MDB[63..0]	>>>	MDB[63..0]
51,55	MAB[11..0]	>>>	MAB[11..0]
51,55	WDQSB[7..0]	>>>	WDQSB[7..0]

<Variant Name>

**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title: **VRAM 1/2**

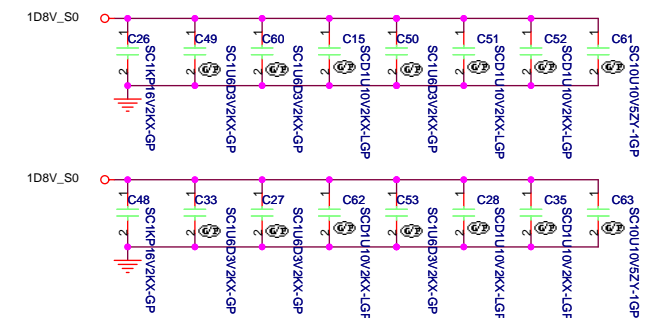
Size: A3 Document Number: **Bolsena-E** Rev: SA

Date: Thursday, October 13, 2005 Sheet: 54 of 58

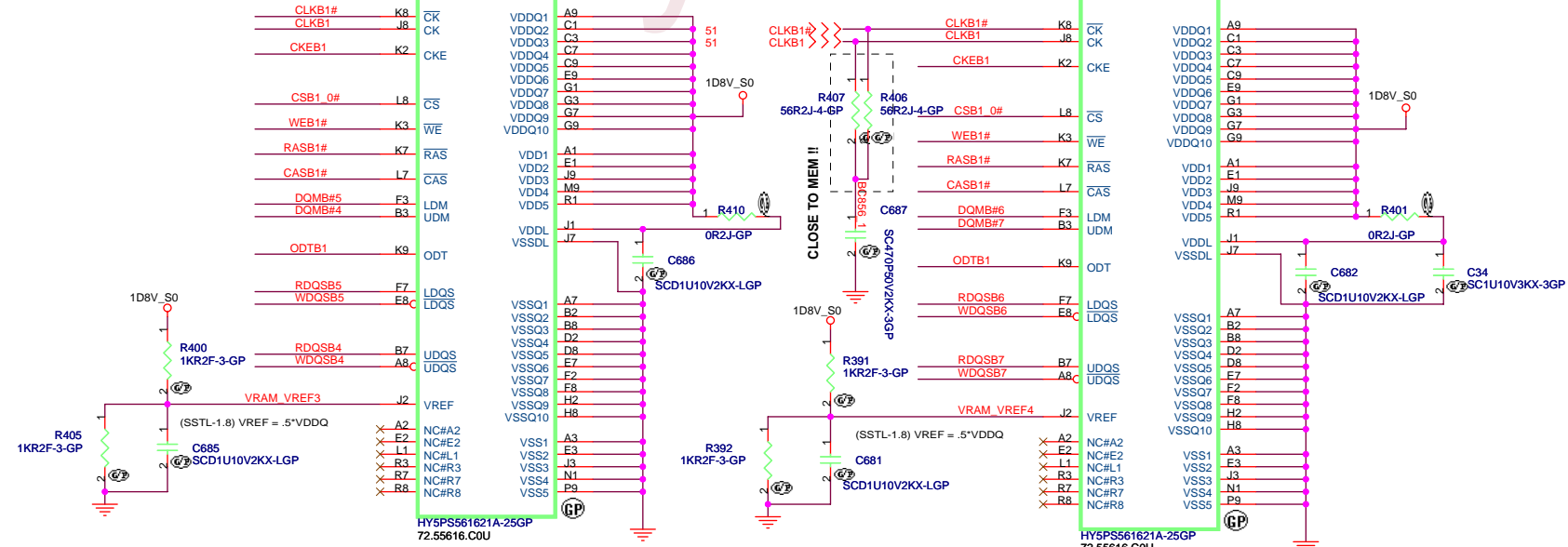


Pin	Signal	U50 Pin	U50 Label
51,54	B_BA0	L2	BA0
51,54	B_BA1	L3	BA1
51,54	MAB12_14	R2	A12
	MAB11	P7	A11
	MAB10	M2	A10/AP
	MAB9	P3	A9
	MAB8	P8	A8
	MAB7	P2	A7
	MAB6	N7	A6
	MAB5	N3	A5
	MAB4	N8	A4
	MAB3	N2	A3
	MAB2	M7	A2
	MAB1	M3	A1
	MAB0	M8	A0

Pin	Signal	U51 Pin	U51 Label
	B_BA0	L2	BA0
	B_BA1	L3	BA1
	MAB12_14	R2	A12
	MAB11	P7	A11
	MAB10	M2	A10/AP
	MAB9	P3	A9
	MAB8	P8	A8
	MAB7	P2	A7
	MAB6	N7	A6
	MAB5	N3	A5
	MAB4	N8	A4
	MAB3	N2	A3
	MAB2	M7	A2
	MAB1	M3	A1
	MAB0	M8	A0



- 51,54 RASB1# >>> RASB1#
- 51,54 CASB1# >>> CASB1#
- 51,54 WEB1# >>> WEB1#
- 51,54 CSB1\_0# >>> CSB1\_0#
- 51,54 CKEB1 >>> CKEB1
- 51,54 ODTB1 >>> ODTB1
- 51,54 RDQSB[7..0] >>> RDQSB[7..0]
- 51,54 DQMB[7..0] >>> DQMB[7..0]
- 51,54 MDB[63..0] >>> MDB[63..0]
- 51,54 MAB[11..0] >>> MAB[11..0]
- 51,54 WDQSB[7..0] >>> WDQSB[7..0]



<Variant Name>

**緯創資通 Wistron Corporation**  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

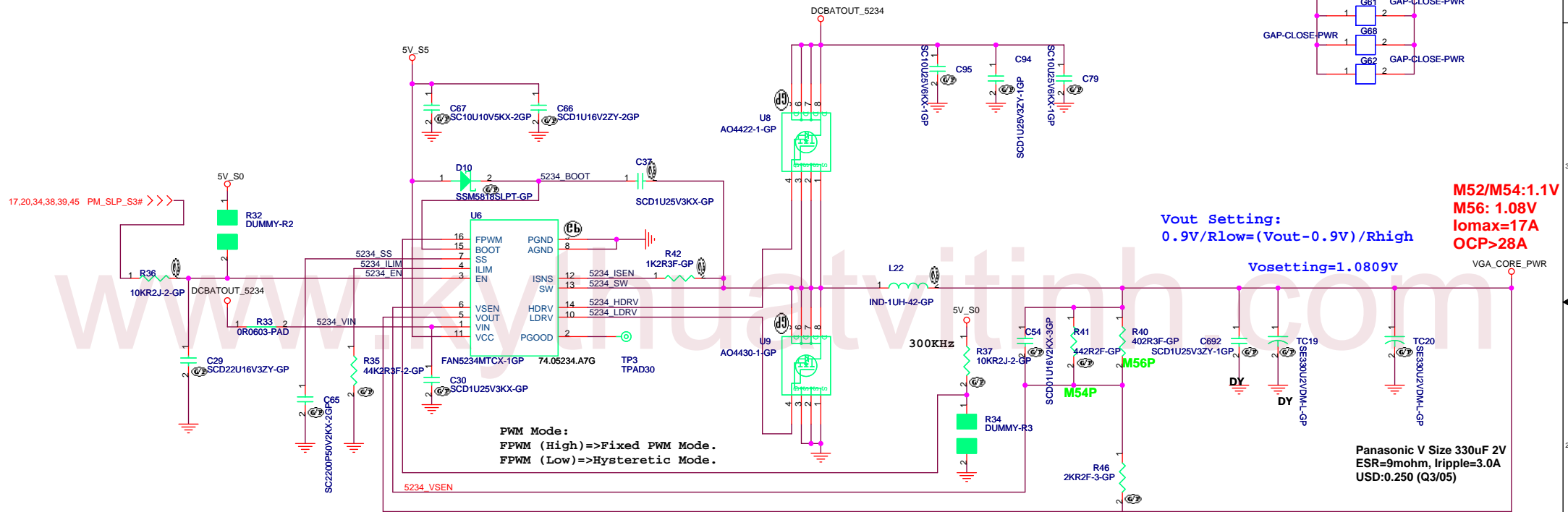
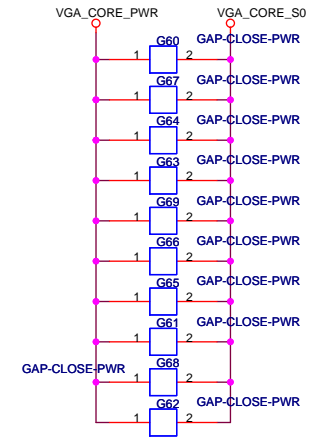
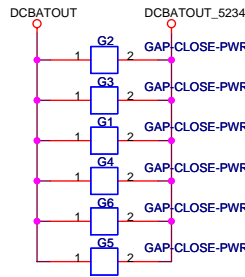
Title: **VRAM 2/2**

Size: A3	Document Number: Bolsena-E	Rev: SA
----------	----------------------------	---------

Date: Thursday, October 13, 2005 Sheet 55 of 58

# FAN5234 FOR VGA\_Core

Dummy when use 'UMA' (whole page)



Vout Setting:  
0.9V/Rlow=(Vout-0.9V)/Rhigh

Vosetting=1.0809V

M52/M54:1.1V  
M56: 1.08V  
Iomax=17A  
OCP>28A

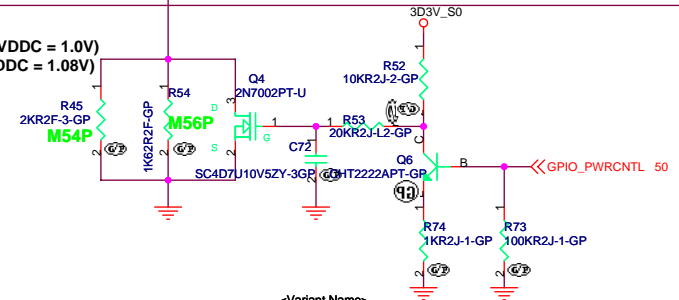
Panasonic V Size 330uF 2V  
ESR=9mohm, Iripple=3.0A  
USD:0.250 (Q3/05)

$$R_{ilim} = (11.2 / I_{ilim}) * ((100 + R_{sense}) / R_{dson})$$

### POWERPLAY:

high (3.3V) = set lower core voltage (e.g. VDDC = 1.0V)  
low (0V) = set higher core voltage (e.g. VDDC = 1.08V)

High : R800 + R59 set Vout to 1V.  
Low : R800 set Vout to 1.08V.



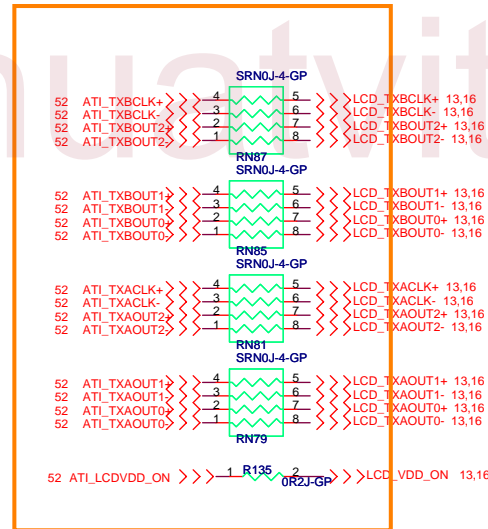
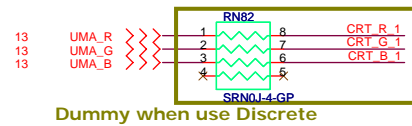
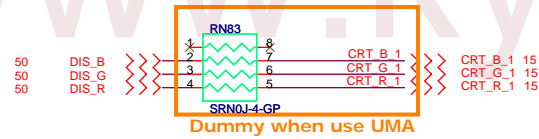
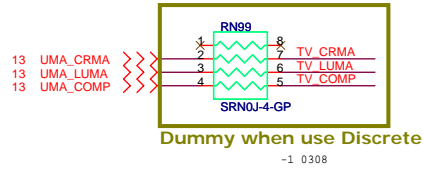
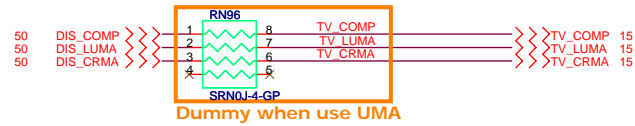
<Variant Name>

緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title <b>VGA CORE 1D1V</b>		
Size A3	Document Number <b>Bolsena-E</b>	Rev SA
Date: Thursday, October 13, 2005	Sheet 56 of	58

# TV SWITCH

Function	S
A to B0	L
A to B1	H



<Variant Name>

緯創資通

**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**VGA SELECTOR**

Size  
A3

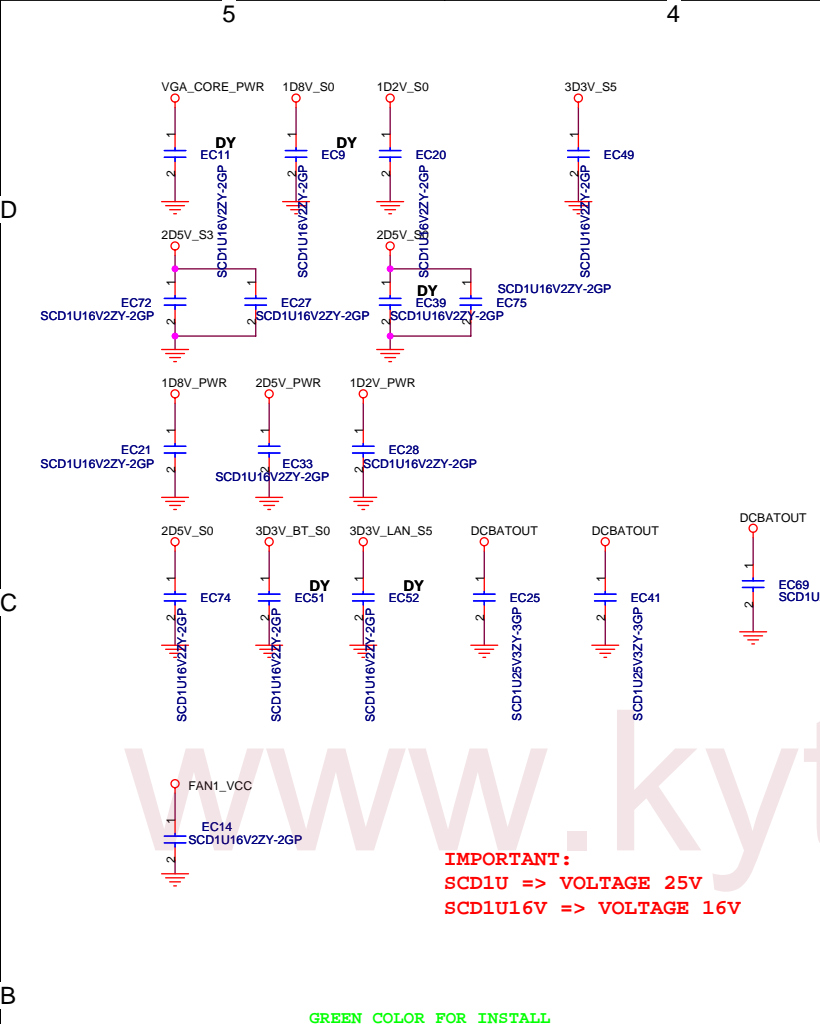
Document Number

**Bolsena-E**

Rev  
SA

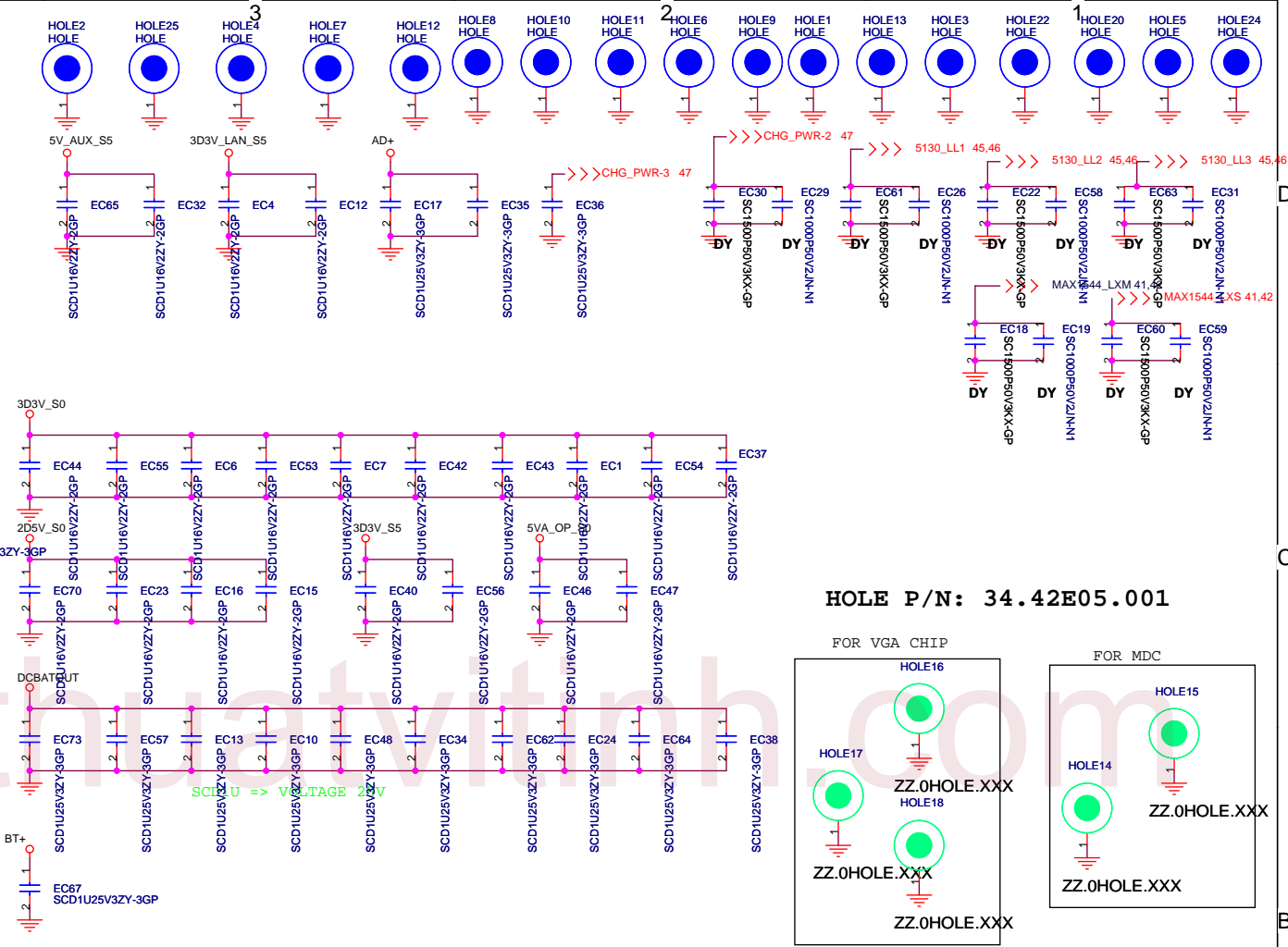
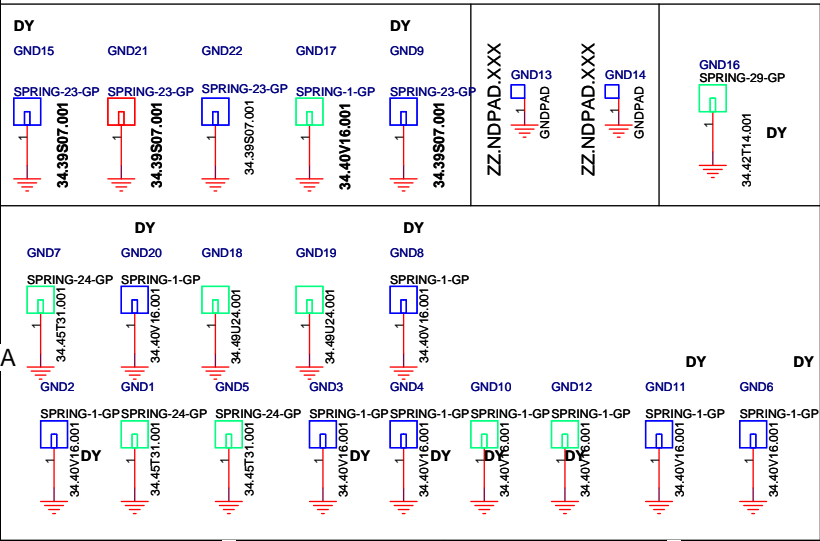
Date: Thursday, October 13, 2005

Sheet 57 of 58

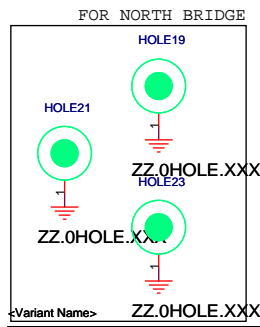
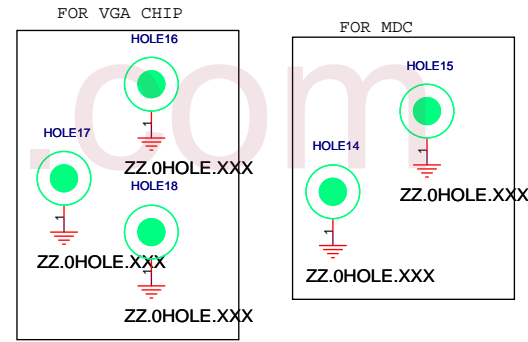


**IMPORTANT:**  
 SCD1U => VOLTAGE 25V  
 SCD1U16V => VOLTAGE 16V

GREEN COLOR FOR INSTALL



HOLE P/N: 34.42E05.001



Variant Name: ZZ.0HOLE.XXX

**緯創資通 Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **EMI**

Size: A3 Document Number: **Bolsena-E** Rev: SA

Date: Thursday, October 13, 2005 Sheet: 58 of 58