# Sonoma Dothan EAL50_1
# LA2362 Schematic

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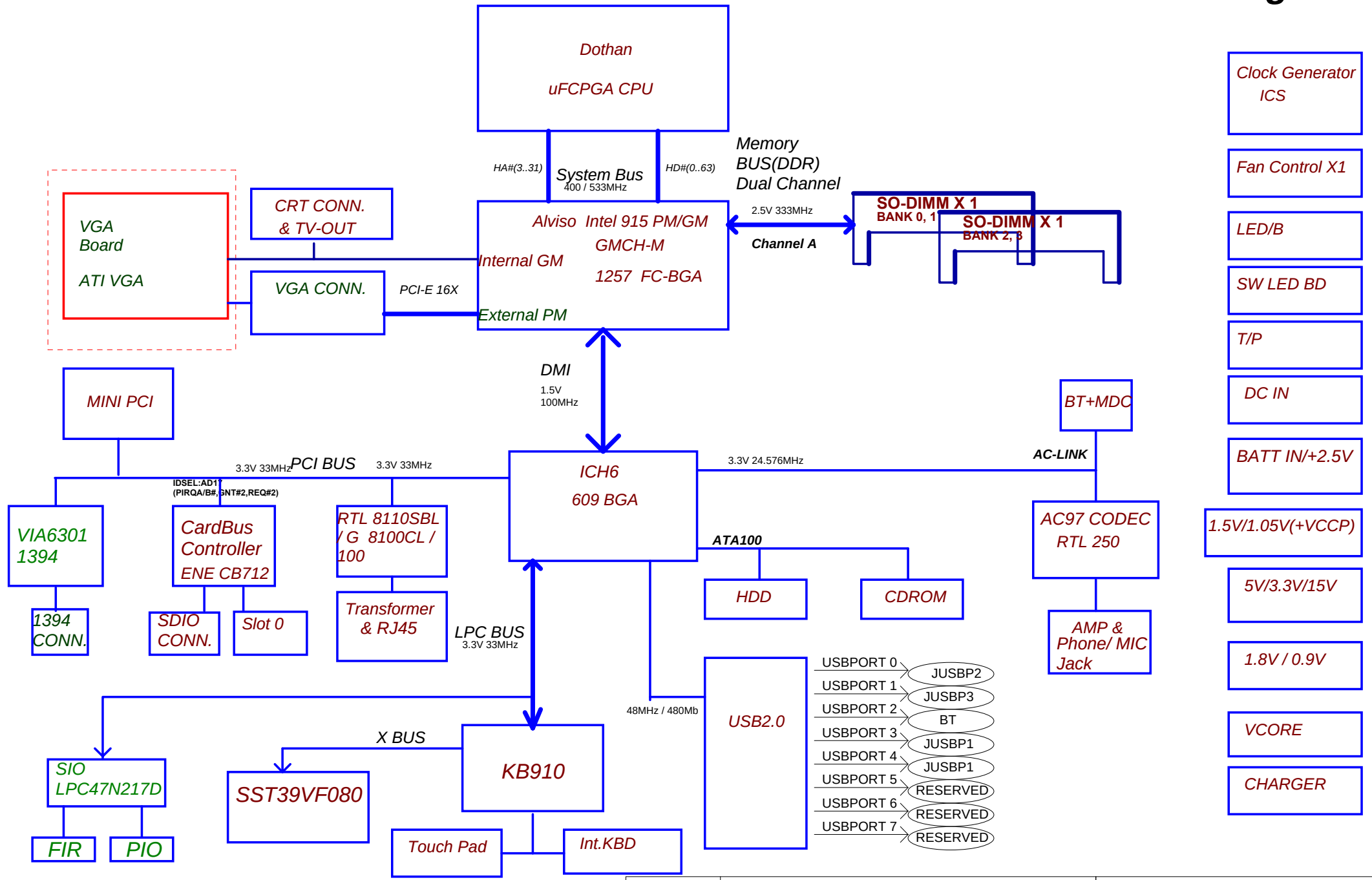
Title: <Title>

Size: Custom | Document Number: LA-2362 | Rev: 1

Date: Friday, March 11, 2005 | Sheet 1 of 52

# Compal confidential

# Block Diagram

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| Issued Date | 2005/03/01 | Deciphered Date | 2006/03/01 |



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| Title | <Title> | | |
| Size | Document Number | | Rev |
| CustomLA-2362 | | | 1 |
| Date: | Friday, March 11, 2005 | Sheet | 2 of 52 |

# I2C / SMBUS ADDRESSING

## External PCI Devices

| DEVICE | IDSEL # | REQ/GNT # | PIRQ |
|---|---|---|---|
| LAN | AD17 | 0 | F |
| CARD BUS | AD20 | 1 | A |
| Cardreader | | | B |
| 1394 | AD16 | 2 | E |
| Wireless LAN(MINI PCI) | AD18 | 3 | G,H |

**@ Depop**
**1@ EAL51**
**2@ EAL50**
**1@ EAL51 VALUE (DELETE SIO/1394)**

Power Managment table

| State \ Signal | +12VALW<br>+3VALW<br>+5VALW | +2.5V<br>+3V<br>+5V<br>+12V | +CPU_CORE<br>+VCCP<br>+5VS<br>+3VS<br>+2.5VS<br>+1.8VS<br>+1.25VS<br>+1.5VS |
|---|---|---|---|
| S0 | ON | ON | ON |
| S1 | ON | ON | ON |
| S3 | ON | ON | OFF |
| S5 S4/AC | ON | OFF | OFF |
| S5 S4/AC don't exist | OFF | OFF | OFF |

Ceramic Capacitor Spec Guide:

Temperature Characteristics:

| Symbol | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|---|
| CODE | Z5U | Z5V | Z5P | Y5U | Y5V | Y5P | X5R | X7R |

| 8 | 9 | A | B | C | D | E | F | G |
|---|---|---|---|---|---|---|---|---|
| NP0 | C0G | | BJ | CH | CJ | CK | SH | SJ |

| H | I | J | |
|---|---|---|---|
| UJ | UK | SL | |

Tolerance:

| Symbol | A | B | C | D | F | G | H | J |
|---|---|---|---|---|---|---|---|---|
| CODE | +-0.05PF | +-0.1PF | +-0.25PF | +-0.5PF | +-1PF | +-2% | +-3% | +-5% |

| K | M | N | P | Q | V | X | Z | |
|---|---|---|---|---|---|---|---|---|
| +-10% | +-20% | +-30% | +100,-0% | +30,-10% | +20,-10% | +40,-20% | +80,-20% | |

SMBUS Control Table

| | SOURCE | INVERTER | BATT | SERIAL EEPROM | THERMAL SENSOR (CPU) | THERMAL SENSOR (LM75) | SODIMM | CLK CHIP | MINI PCI | LCD | VGA Thermal ADM1032 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SMB_EC_CK1<br>SMB_EC_DA1 | PC87591L | √ | √ | √ | X | X | X | X | X | X | X |
| SMB_EC_CK2<br>SMB_EC_DA2 | PC87591L | X | X | X | √ | √ | X | X | X | X | √ |
| ICH_SMBCLK<br>ICH_SMBDATA | ICH6-M | X | X | X | X | X | √ | √ | X | X | X |
| LCD_DDCCLK<br>LCD_DDCDATA | Alviso GM-GP | X | X | X | X | X | X | X | X | √ | X |

| | PCB Rev | Data |
|---|---|---|
| Bringup-Build<br>SST-Build | 0.1 | |
| PT-Build | | |
| ST-Build | | |
| QT-Build | | |
| | | |
| | | |

SCHEMATICS VERSION LIST

| VERSION | ISSUE DATE | REMARK |
|---|---|---|
| 0.0A | | First Release |
| | | |
| | | |
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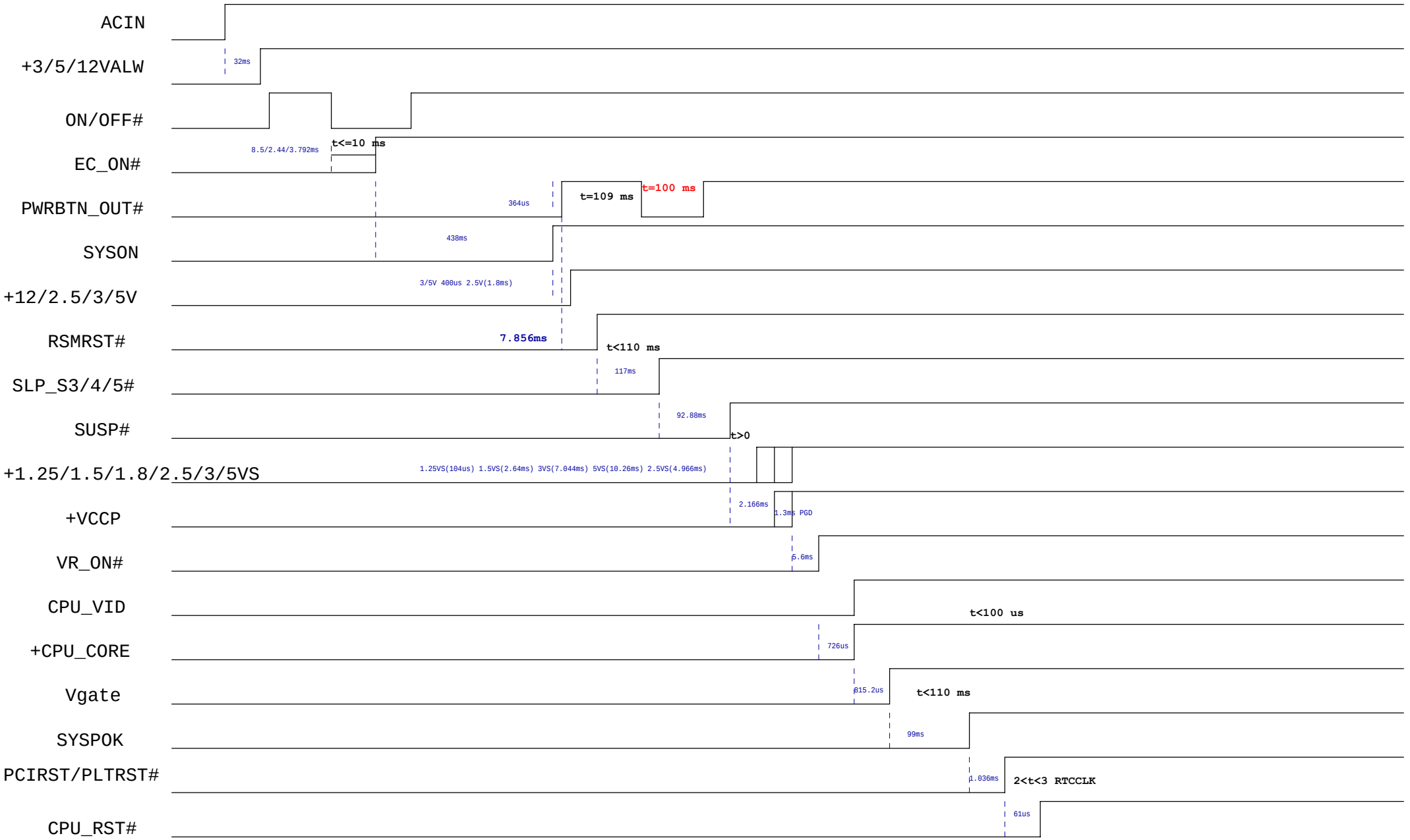
| Issued Date | 2005/03/01 | Deciphered Date | 2006/03/01 |

Title: <Title>
Size: C | Document Number: LA-2362 | Rev: 1
Date: Friday, March 11, 2005 | Sheet 3 of 52

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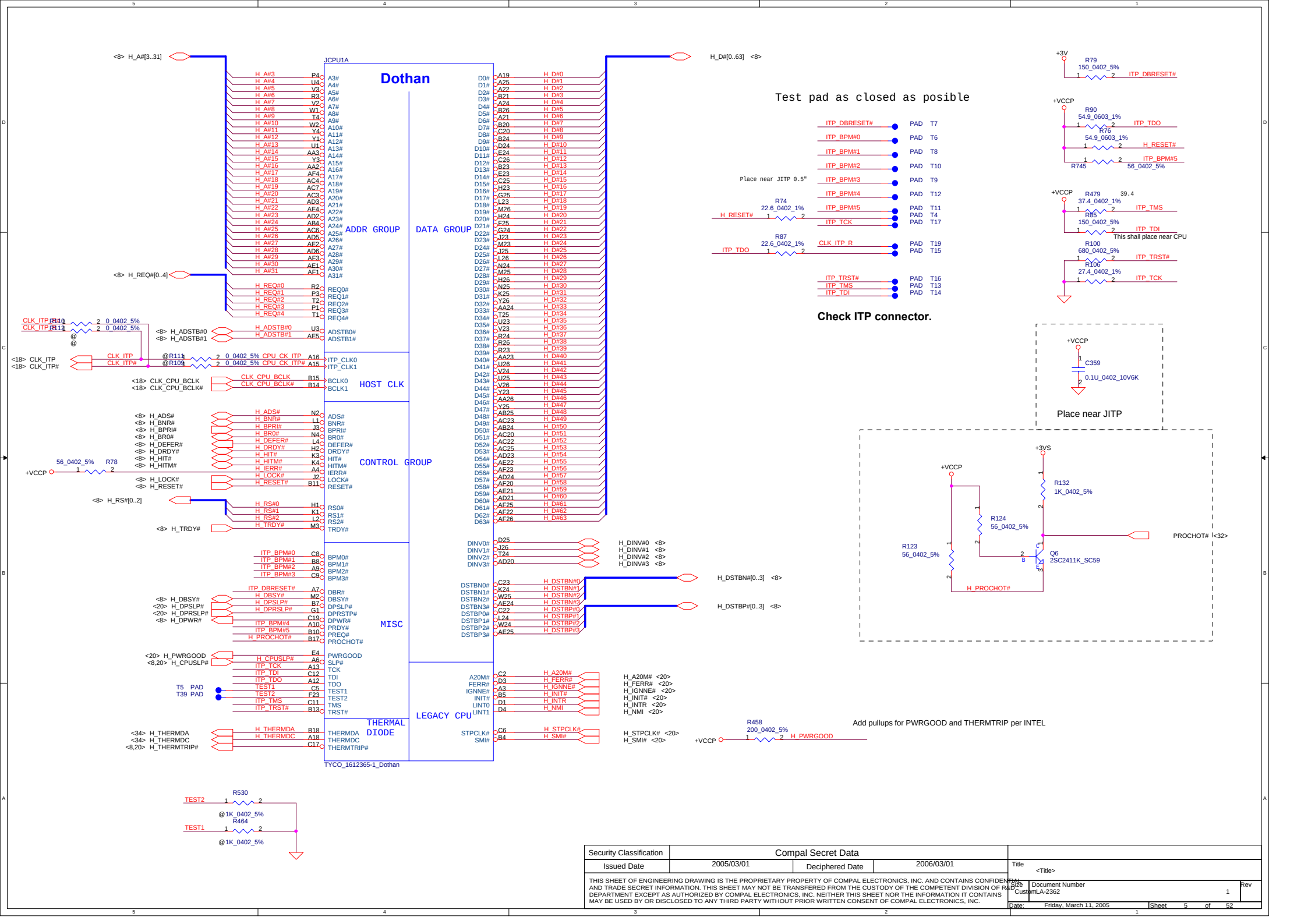
| Size | Document Number | | Rev |
| Custom | LA-2362 | | 1 |
| Date: | Friday, March 11, 2005 | Sheet | 4 of 52 |

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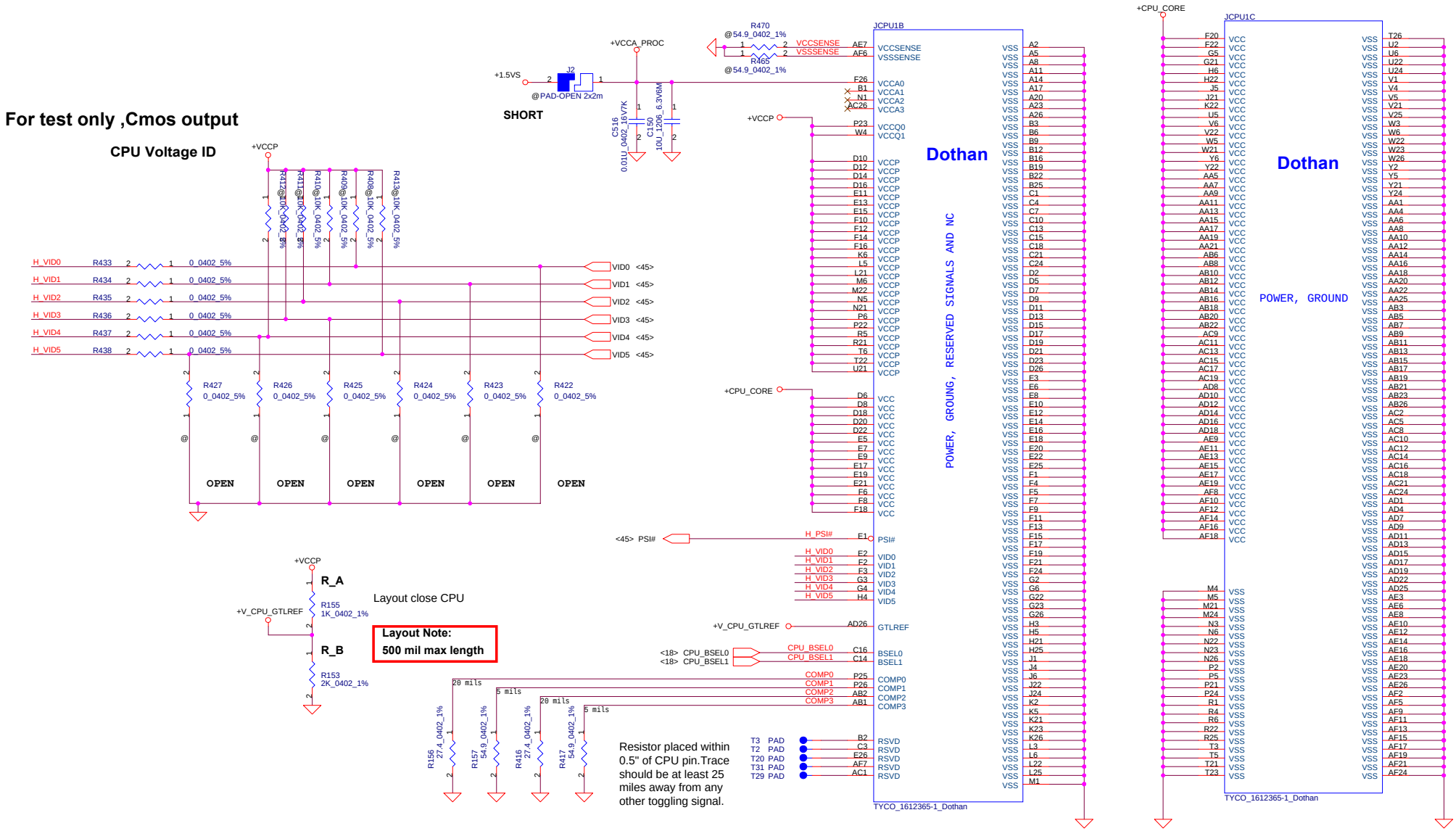
| Size | Document Number | | Rev |
| CustomLA-2362 | | | 1 |
| Date: | Friday, March 11, 2005 | Sheet | 5 of 52 |

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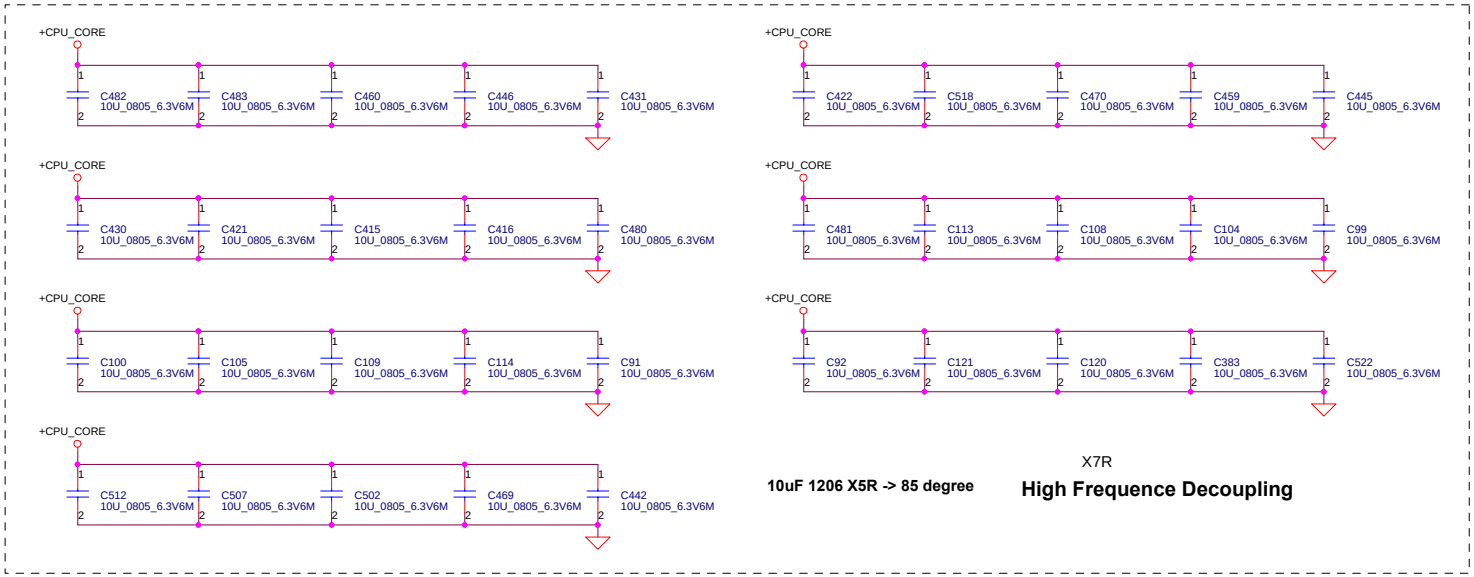
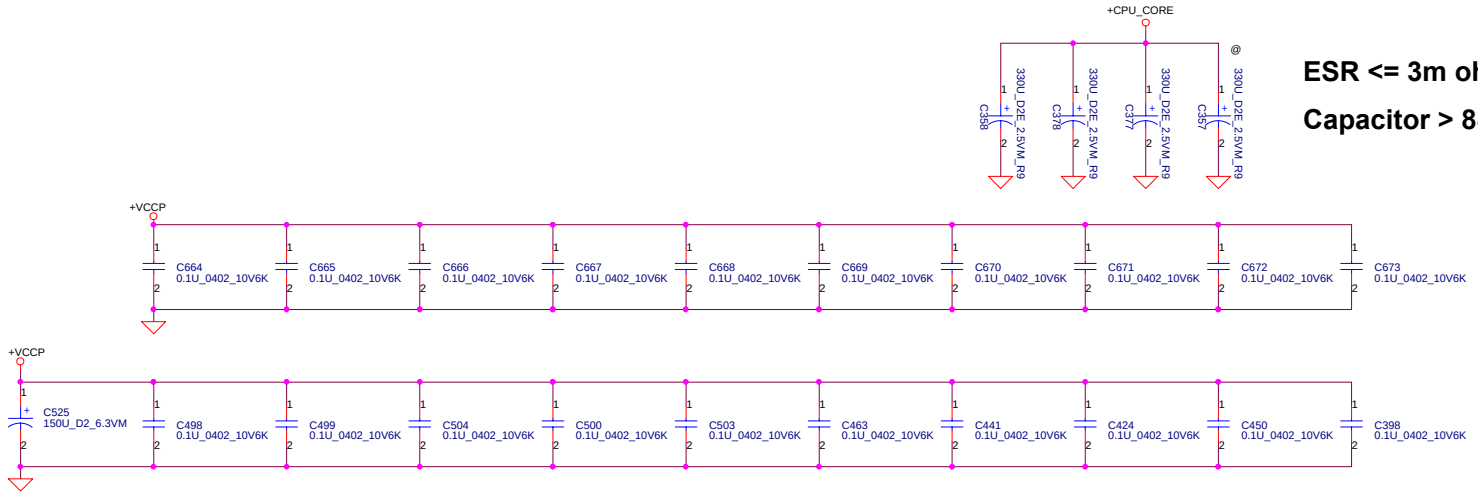
| Size | Document Number | | Rev |
| C | CustomLA-2362 | | 1 |
| Date: | Friday, March 11, 2005 | Sheet | 6 of 52 |




**Near VCORE regulator.**




**ESR <= 3m ohm**

**Capacitor > 880 uF**

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|---|---|---|---|
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| Issued Date | 2005/03/01 | Deciphered Date | 2006/03/01 |



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|---|---|---|---|
| Title | <Title> | | |
| Size: CustomLA-2362 | Document Number | | Rev: 1 |
| Date: Friday, March 11, 2005 | Sheet 7 of 52 | | |

Layout Guide will show these signals routed differentially.

Alviso CFG[17:3] has internal pull-up

**Layout Note: Rote as short as possible**

Layout Guide will show these signals routed differentially.

| | |
|---|---|
| **CFG[2:0]** | **Refer to sheet 6 for FSB frequency select** |
| **CFG5** | **Low = DMI x 2**<br>**High = DMI x 4** * |
| **CFG6** | **Low = DDR-II**<br>**High = DDR-I** * |
| **CFG7** | **Low = DT/Transportable CPU**<br>**High = Mobile CPU** * |
| **CFG9** | **Low = Reverse Lane**<br>**High = Normal Operation** * |
| **CFG[13:12]** | **00 = Reserved**<br>**01 = XOR Mode Enabled**<br>**10 = All Z Mode Enabled**<br>**11 = Normal Operation (Default)** * |
| **CFG16 (FSB Dynamic ODT)** | **Low = Disabled**<br>**High = Enabled** * |
| **CFG18 (VCC Select)** | **Low = 1.05V (Default)** *<br>**High = 1.5V** |
| **CFG19 (VTT Select)** | **Low = 1.05V (Default)** *<br>**High = 1.2V** |

CFG[17:3] have internal pull-up

CFG[19:18] have internal pull-down

**Note:**
**"Do not install R for Dothan-A, Install R97 for Dothan-B"**

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|---|---|---|---|
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| Issued Date | 2005/03/01 | Deciphered Date | 2006/03/01 |



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|---|---|---|---|
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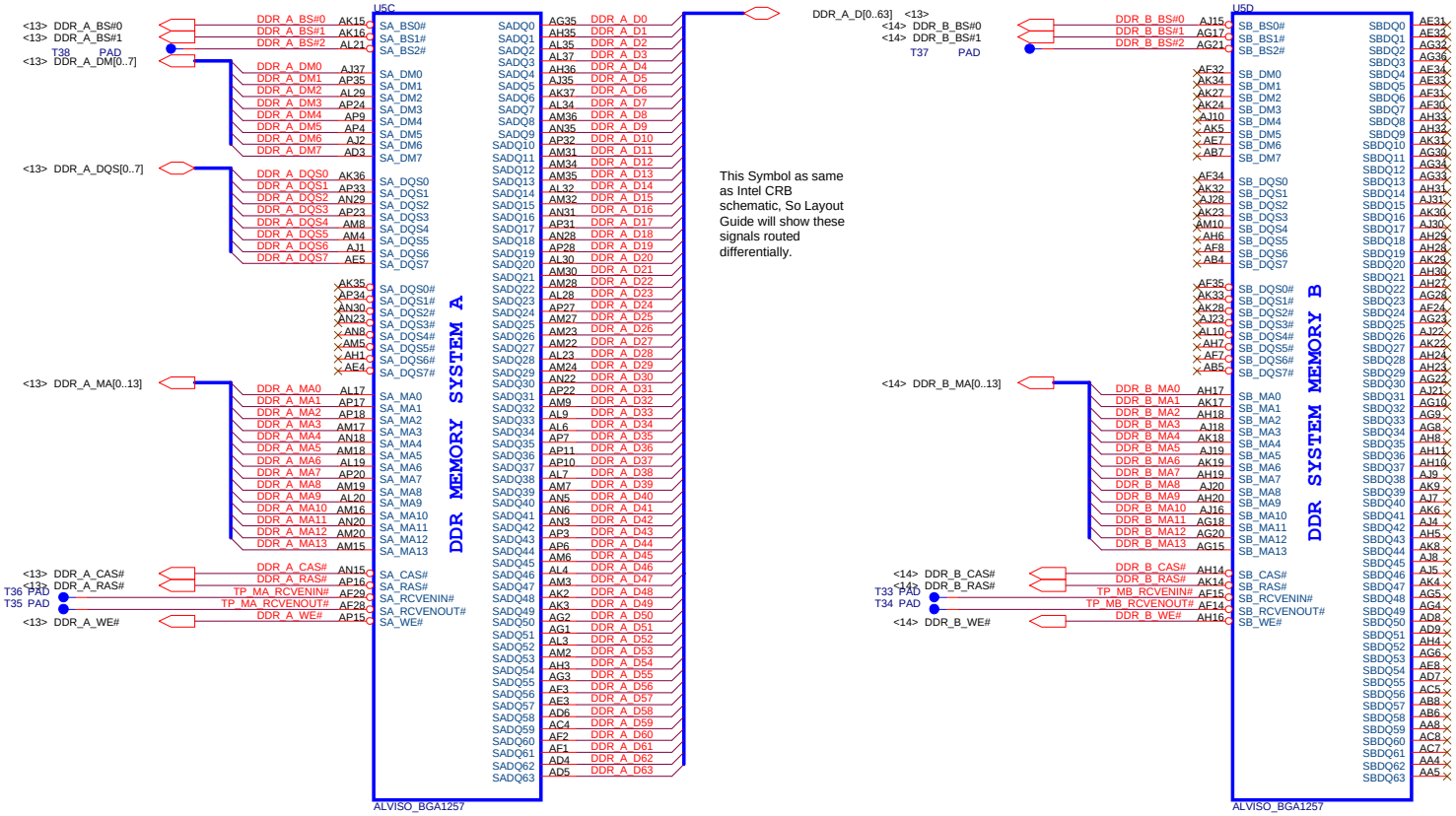
| Size | Document Number | | Rev |
| Custom | LA-2362 | | 1 |
| Date: | Friday, March 11, 2005 | Sheet | 8 of 52 |

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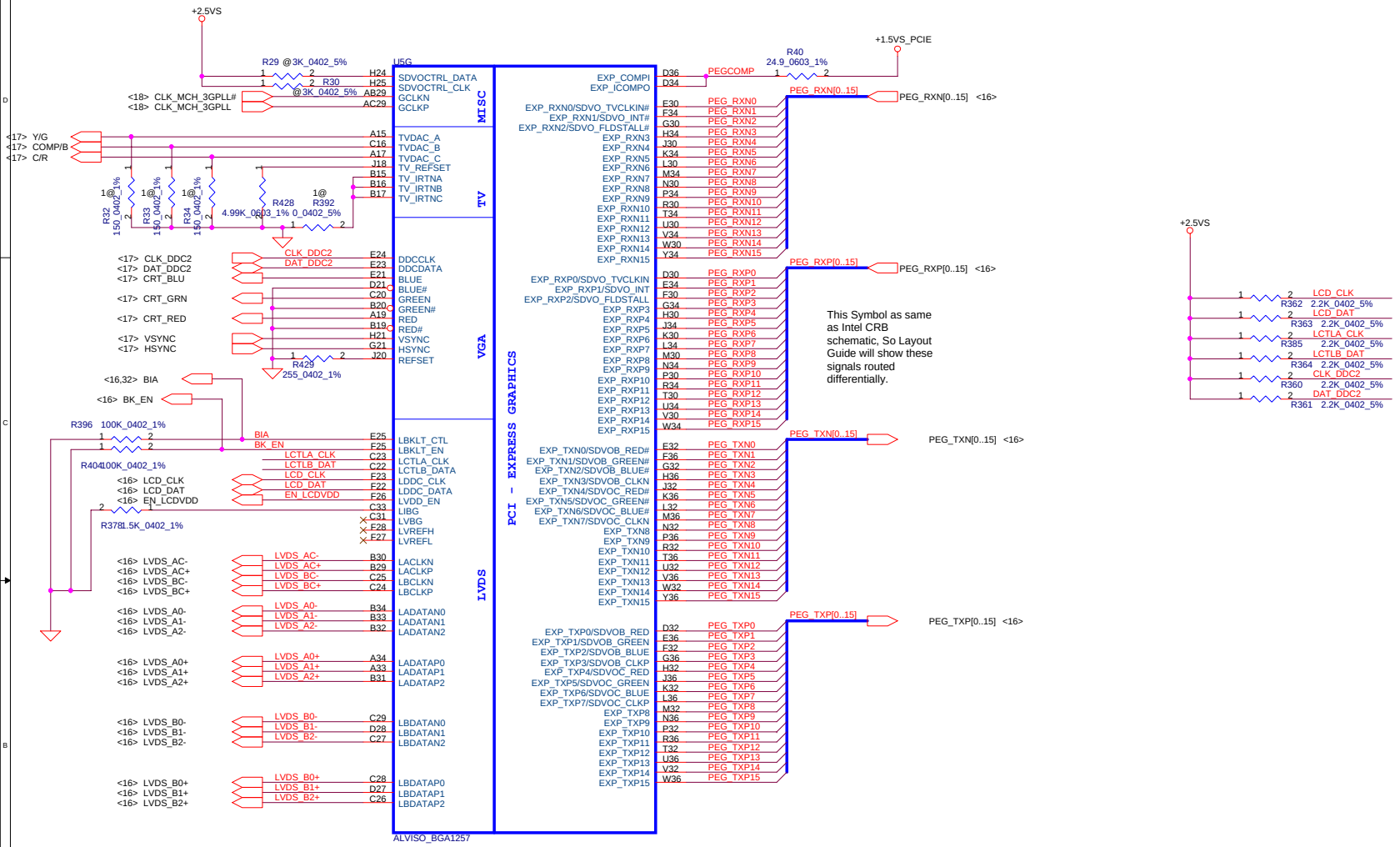
| Title | <Title> | | |
| Size | Document Number | | Rev |
| CustomLA-2362 | | 1 | |
| Date: | Friday, March 11, 2005 | Sheet 9 of 52 | |

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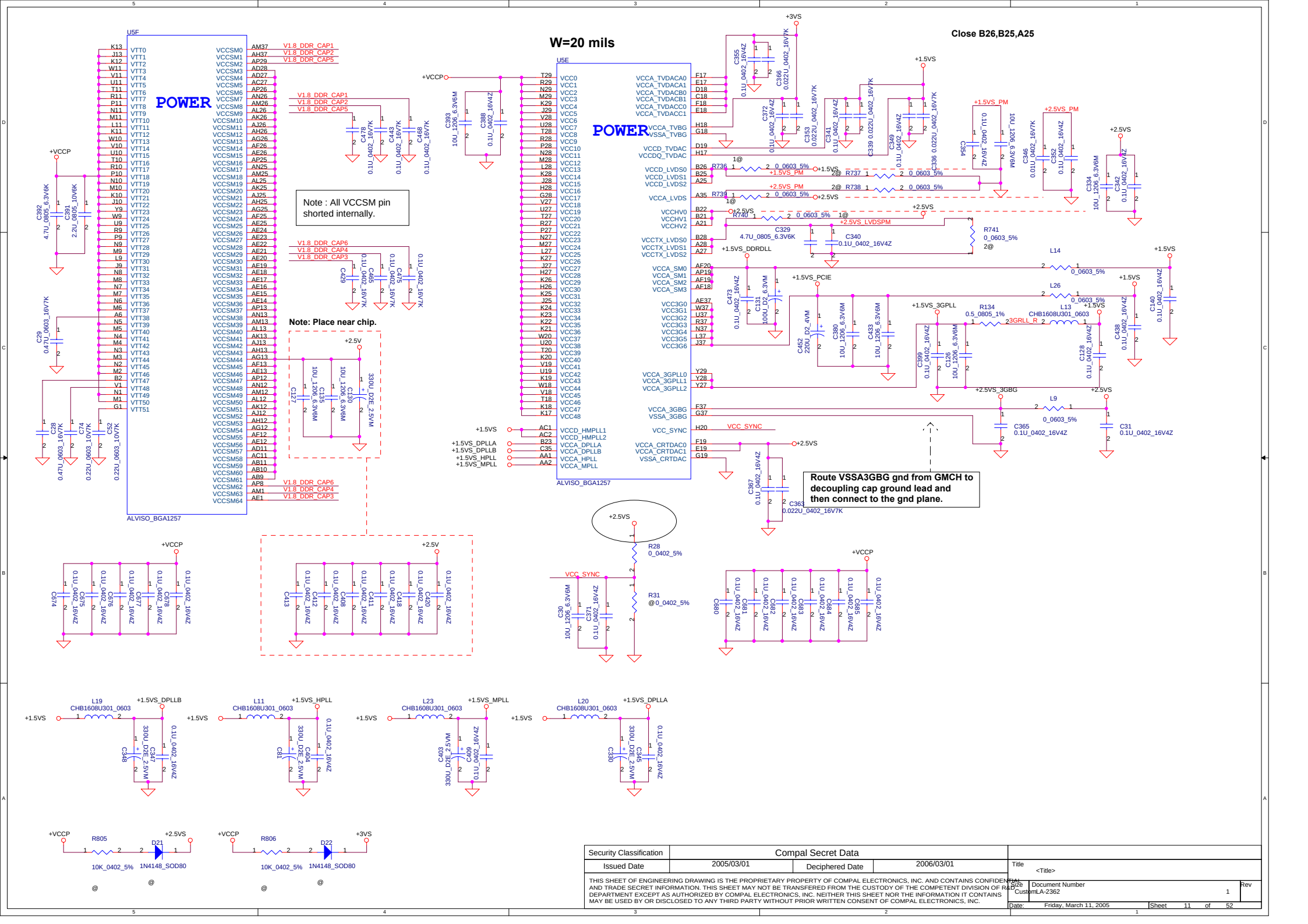
| Size: Custom | Document Number: LA-2362 | | Rev: 1 |
| Date: Friday, March 11, 2005 | Sheet 10 of 52 | | |

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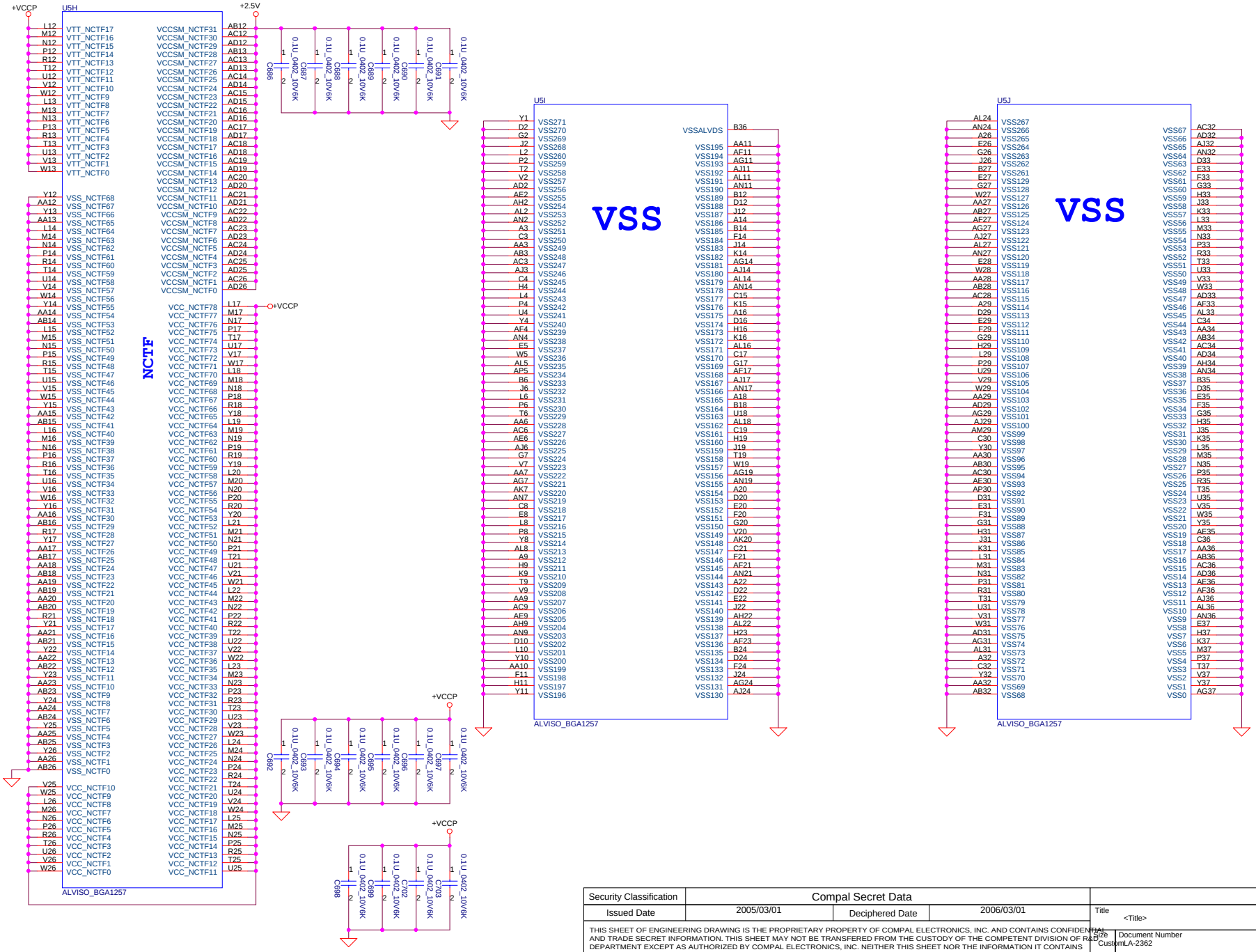
| Size | Document Number | | Rev |
| CustomLA-2362 | | | 1 |
| Date: | Friday, March 11, 2005 | Sheet | 11 of 52 |

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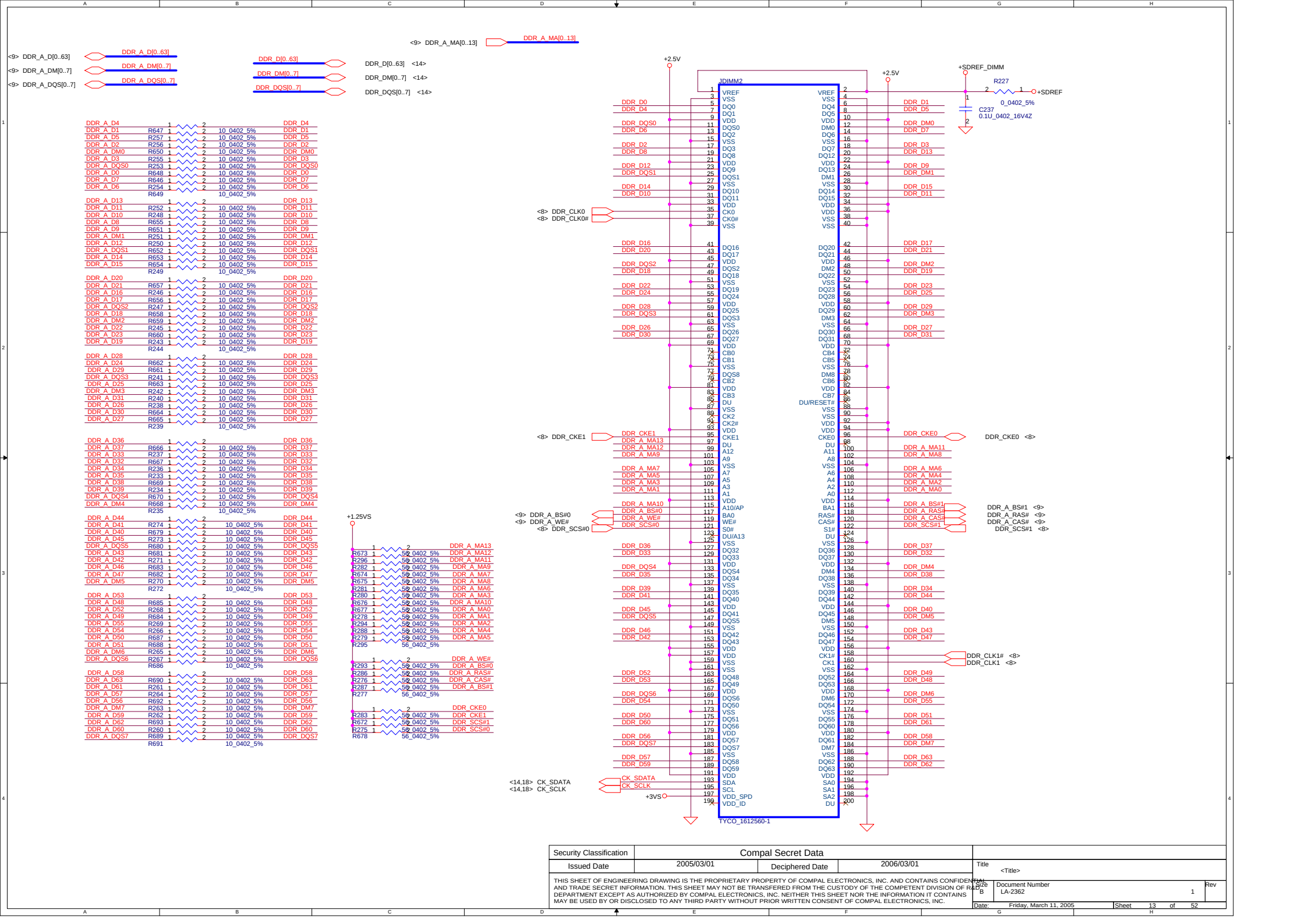
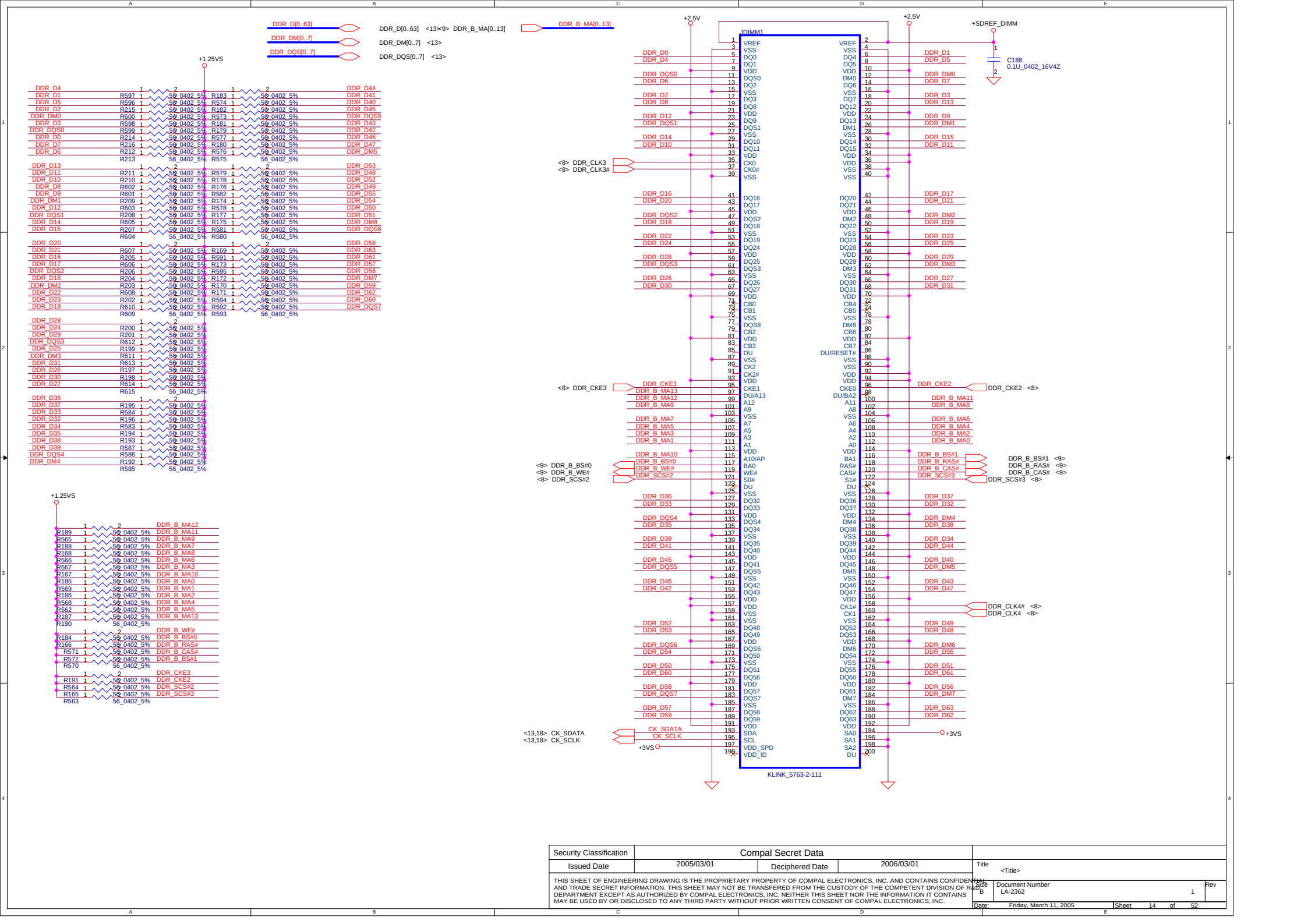
| Size | Document Number | | Rev |
| CustomLA-2362 | | 1 | |
| Date: | Friday, March 11, 2005 | Sheet 12 of 52 | |



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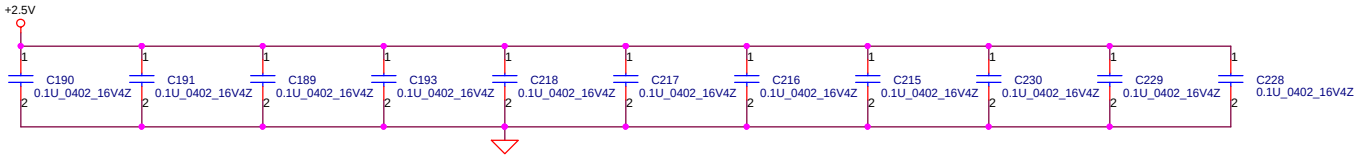
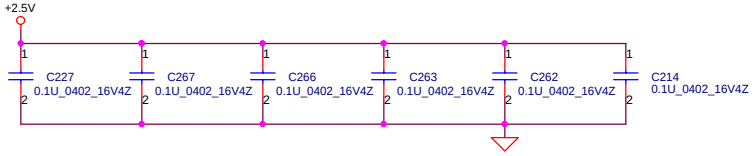
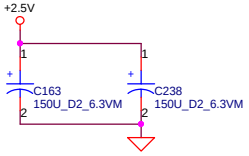
| Title | <Title> | | |
| Size B | Document Number LA-2362 | | Rev 1 |
| Date: Friday, March 11, 2005 | Sheet 14 of 52 | | |

**Layout note :**

**Distribute as close as possible to DDR-SODIMM.**

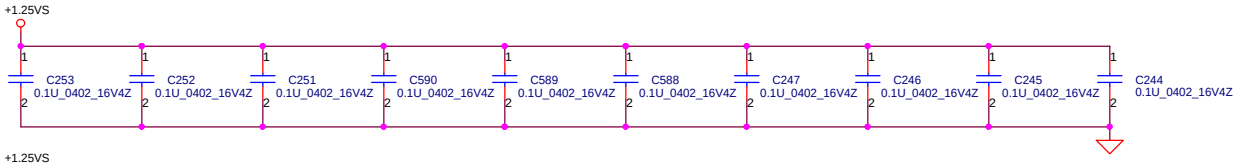


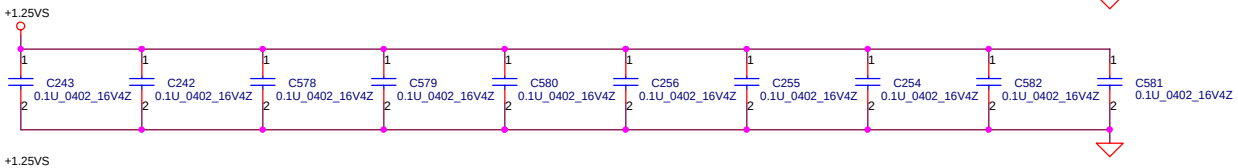



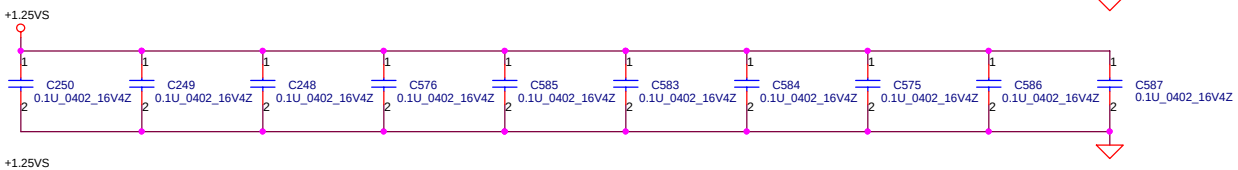



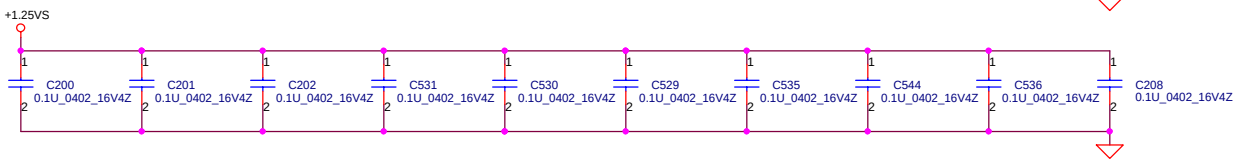

**Layout note :**

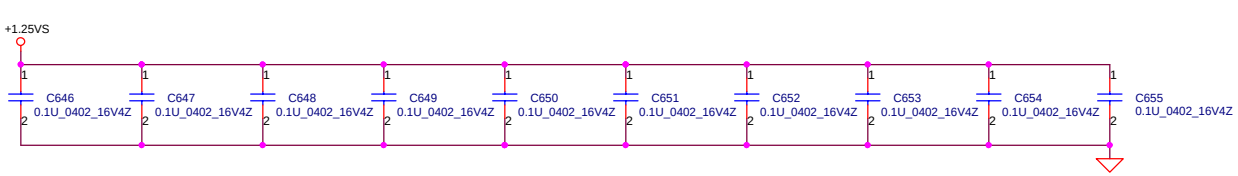
**Place one cap close to every 2 pull up resistors termination to +1.25V**

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| Security Classification | Compal Secret Data | | |
| Issued Date | 2005/03/01 | Deciphered Date | 2006/03/01 |



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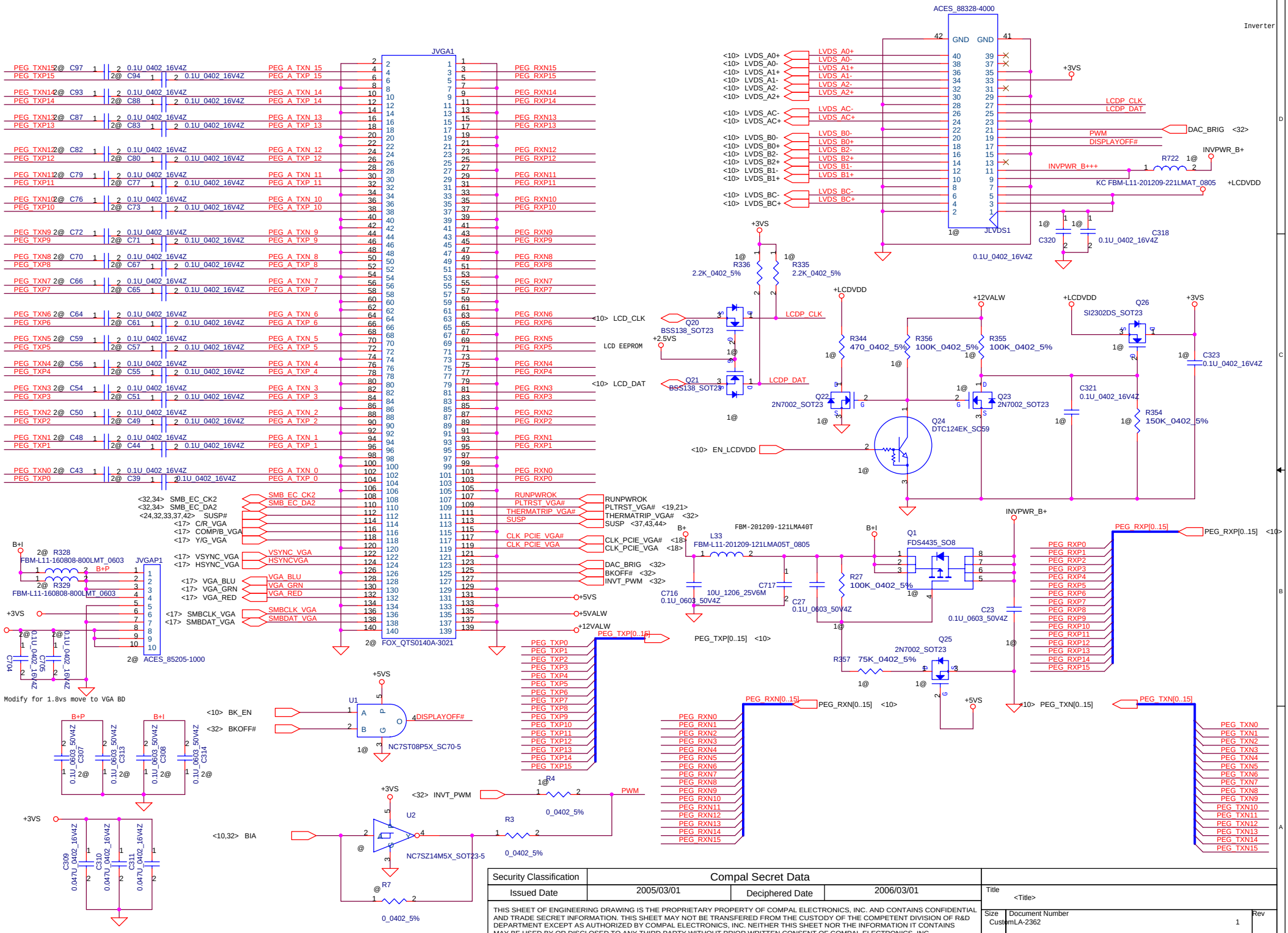
| Title | <Title> | |
| Size | Document Number | Rev |
| CustomLA-2362 | 1 | |
| Date: Friday, March 11, 2005 | Sheet 15 of 52 | |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FOX_QTS0140A-3021
ACES_88328-4000
JLVDS1
ACES_85205-1000
JVGAP1
Inverter
LCD EEPROM
Q20 BSS138_SOT23
Q21 BSS138_SOT23
Q22 2N7002_SOT23
Q23 2N7002_SOT23
Q24 DTC124EK_SC59
Q25 2N7002_SOT23
Q26 SI2302DS_SOT23
Q1 FDS4435_SO8
L33 FBM-L11-201209-121LMA05T_0805
FBM-L11-160808-800LMT_0603
FBM-201209-121LMA40T
U1 NC7ST08P5X_SC70-5
U2 NC7SZ14M5X_SOT23-5
Modify for 1.8vs move to VGA BD
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Document Number
LA-2362
Rev
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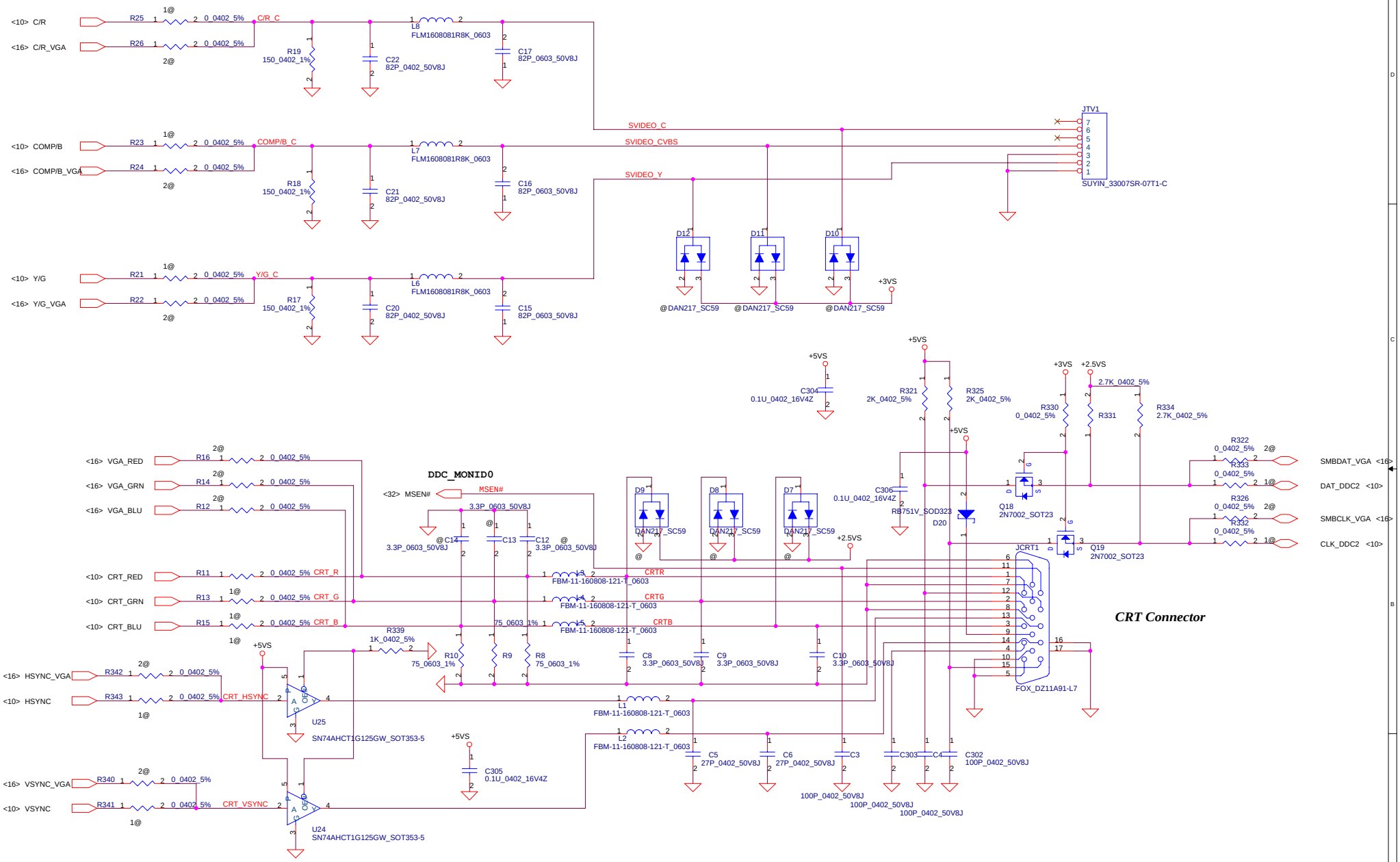
Date:
Friday, March 11, 2005
Sheet
16
of
52

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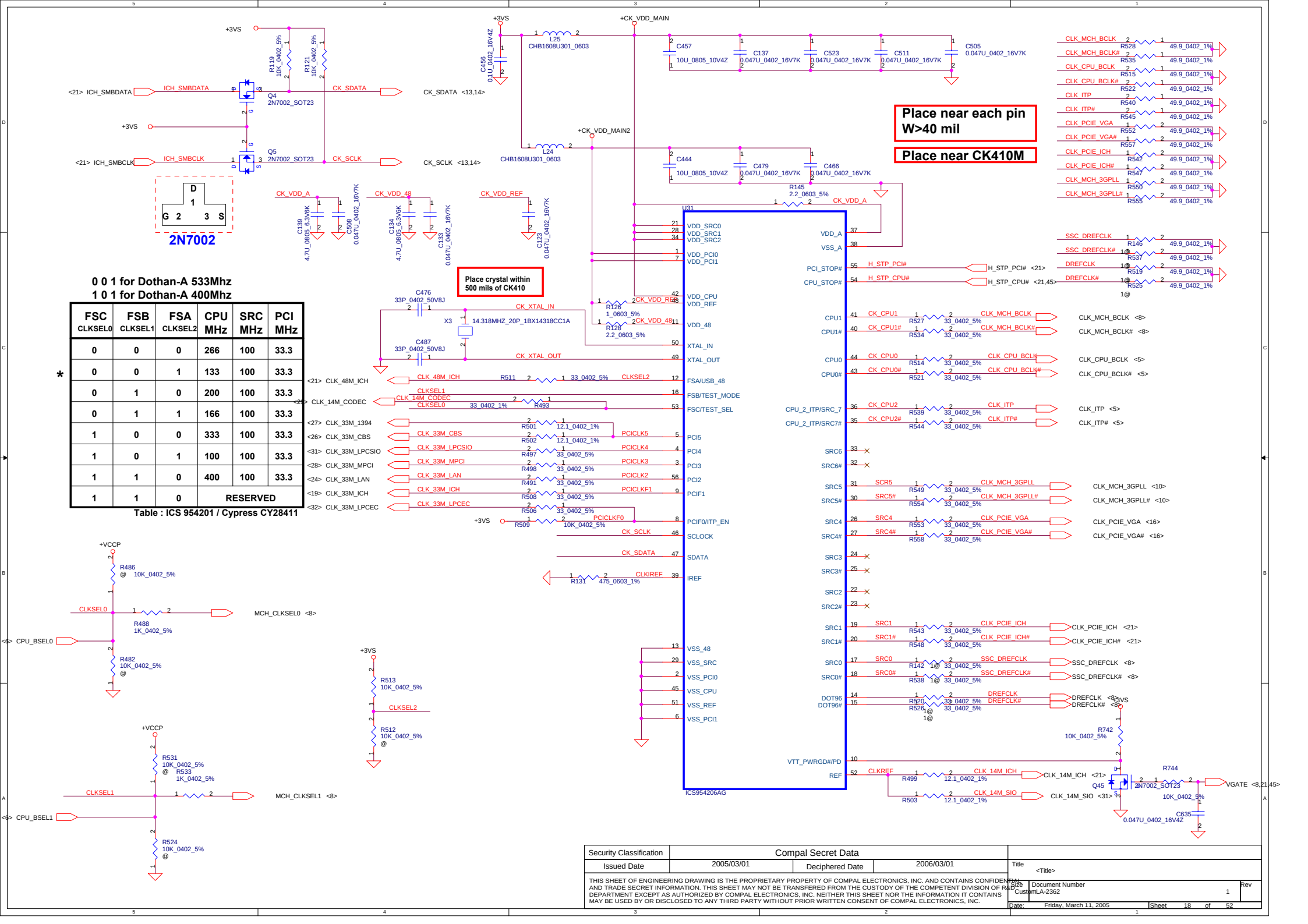
| Size | Document Number | | Rev |
| CustomLA-2362 | | 1 | |
| Date: Friday, March 11, 2005 | Sheet 17 of 52 | | |




| | FSC CLKSEL0 | FSB CLKSEL1 | FSA CLKSEL2 | CPU MHz | SRC MHz | PCI MHz |
|---|---|---|---|---|---|---|
| | 0 | 0 | 0 | 266 | 100 | 33.3 |
| * | 0 | 0 | 1 | 133 | 100 | 33.3 |
| | 0 | 1 | 0 | 200 | 100 | 33.3 |
| | 0 | 1 | 1 | 166 | 100 | 33.3 |
| | 1 | 0 | 0 | 333 | 100 | 33.3 |
| | 1 | 0 | 1 | 100 | 100 | 33.3 |
| | 1 | 1 | 0 | 400 | 100 | 33.3 |
| | 1 | 1 | 0 | RESERVED | | |

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|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2005/03/01 | Deciphered Date | 2006/03/01 |



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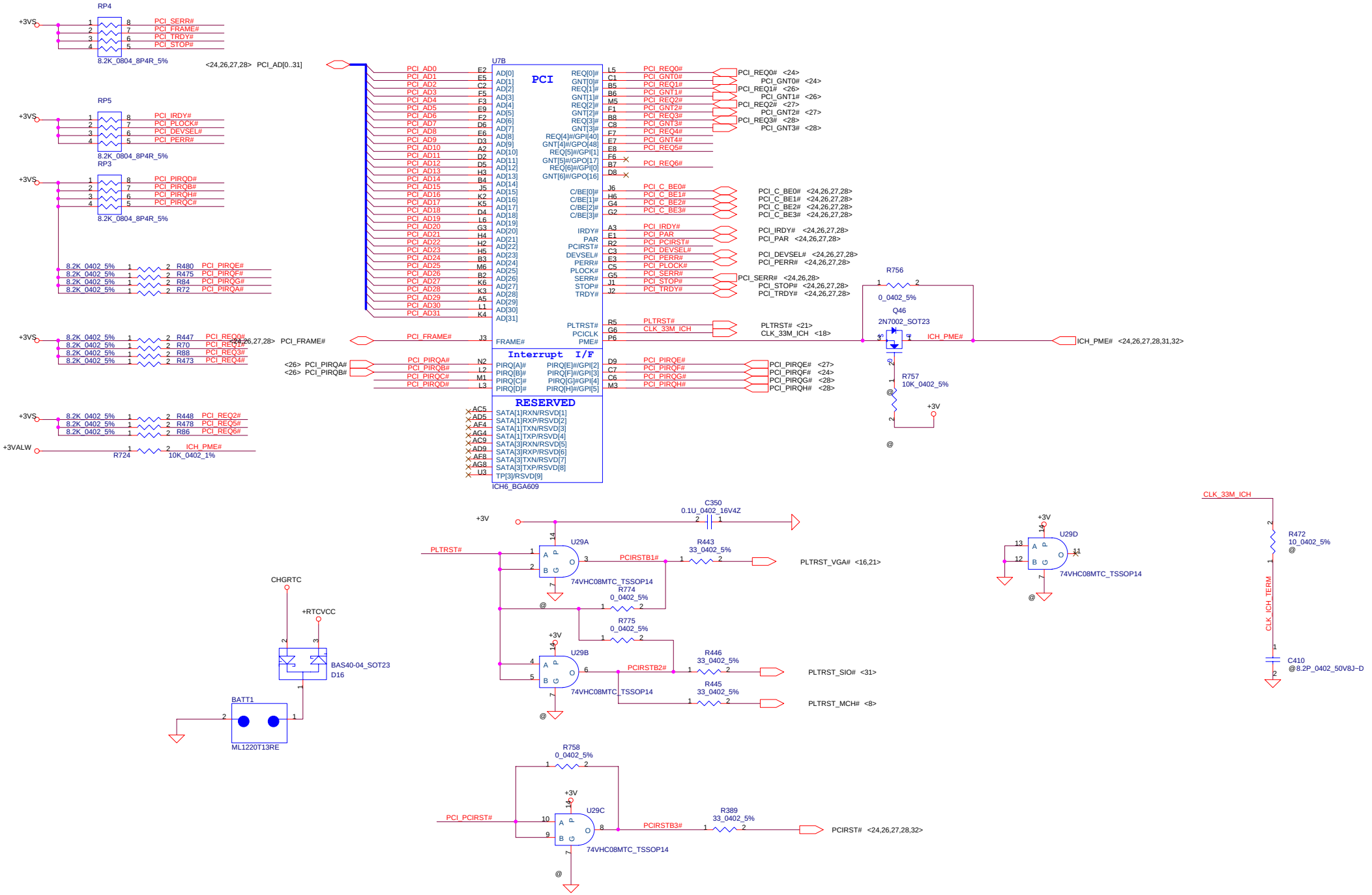
|---|---|---|---|
| Title | <Title> | | |
| Size | Document Number | | Rev |
| CustomLA-2362 | | | 1 |
| Date: | Friday, March 11, 2005 | Sheet | 18 of 52 |

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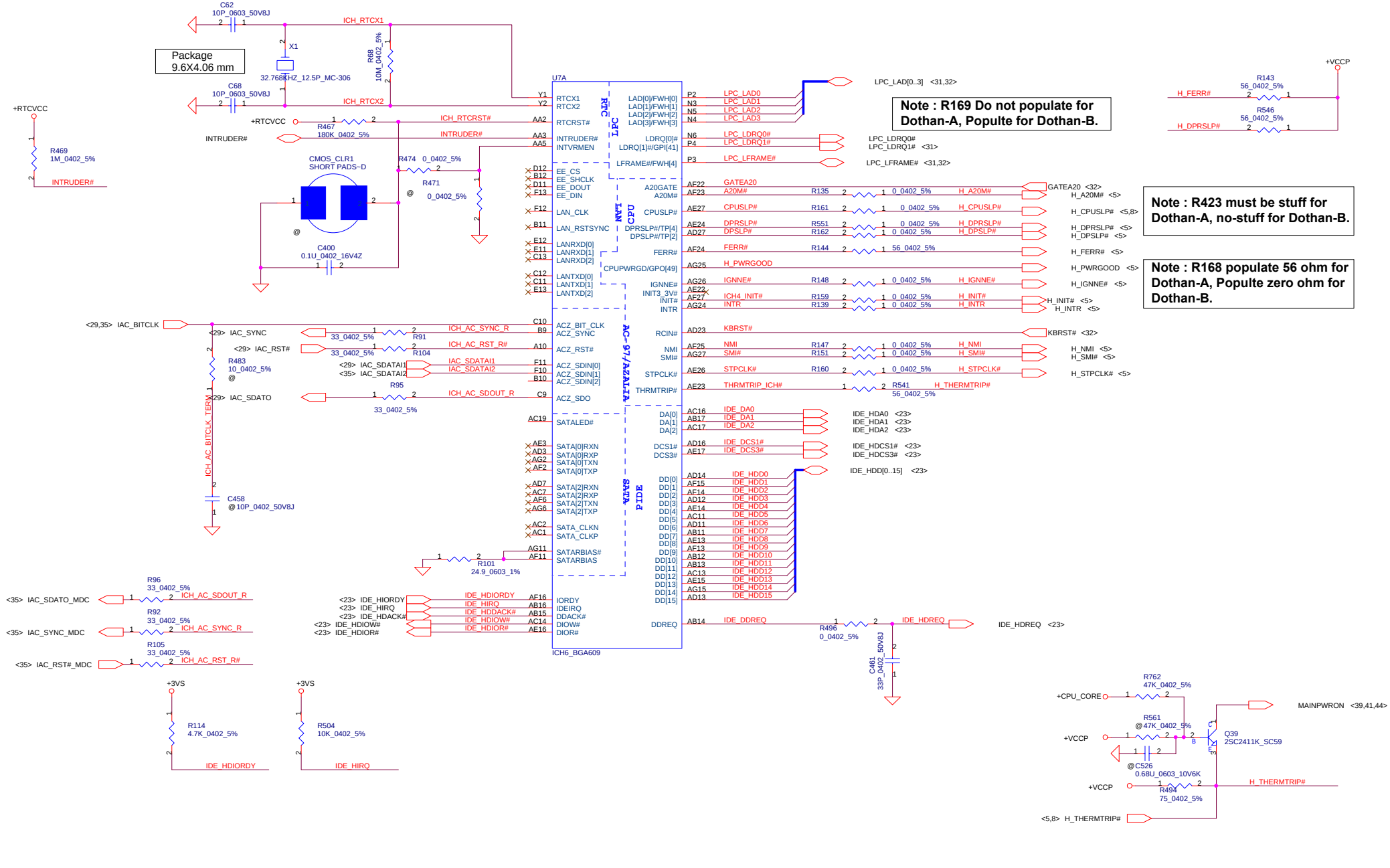
| Size | Document Number | | Rev |
| CustomLA-2362 | | | 1 |
| Date: Friday, March 11, 2005 | Sheet 19 of 52 | | |

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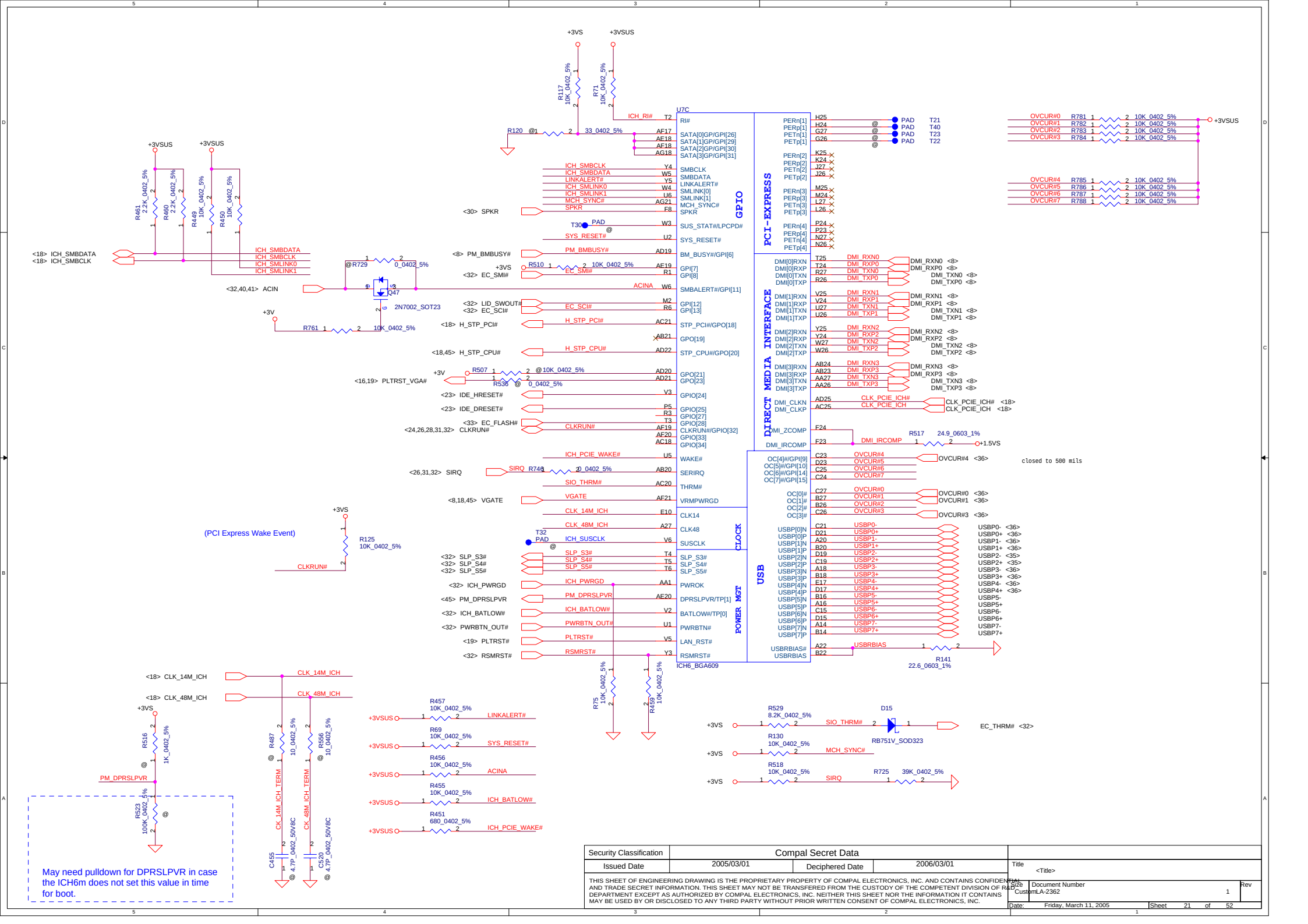
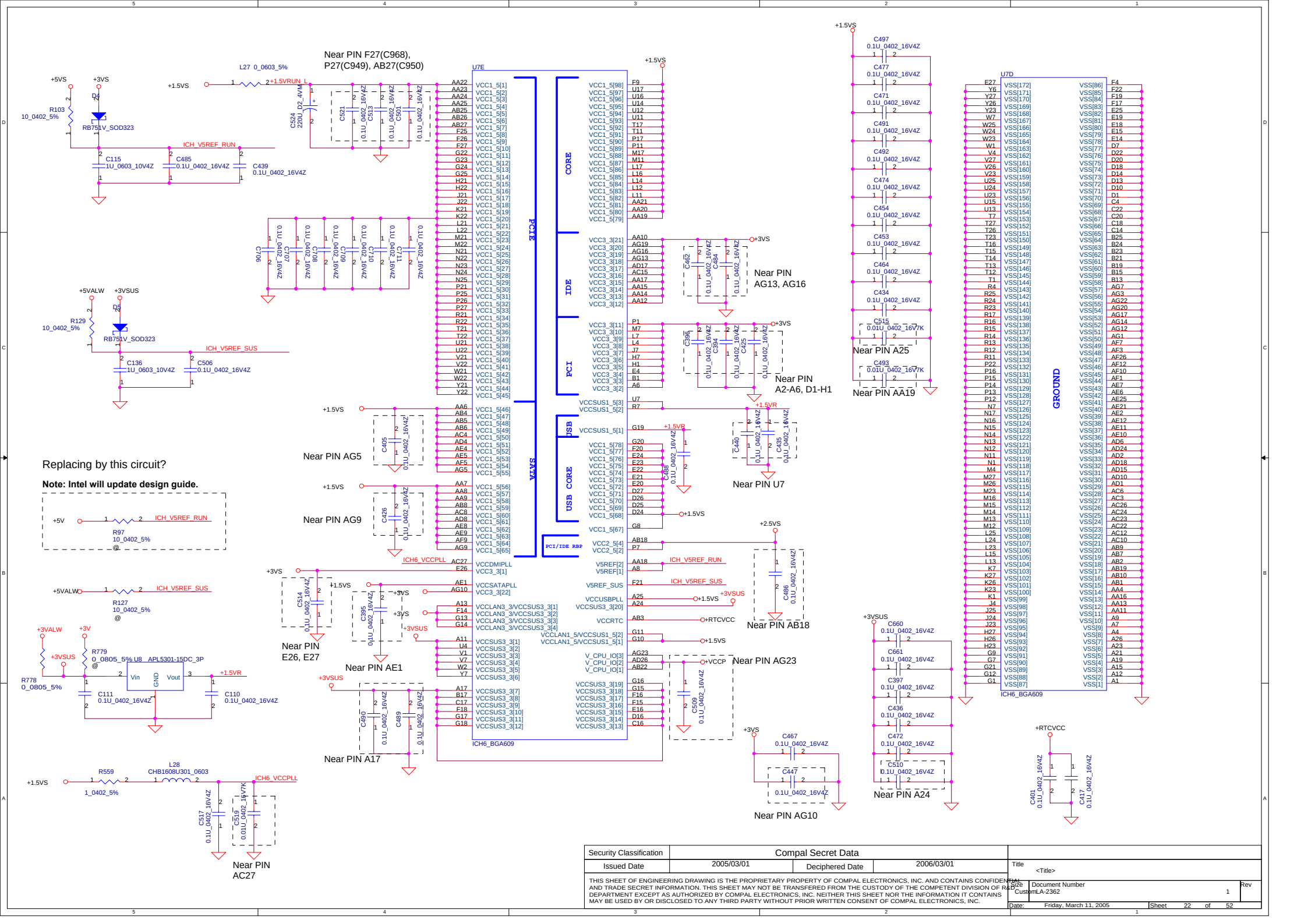
| Size | Document Number | | Rev |
| CustomLA-2362 | | | 1 |
| Date: | Friday, March 11, 2005 | Sheet | 20 of 52 |



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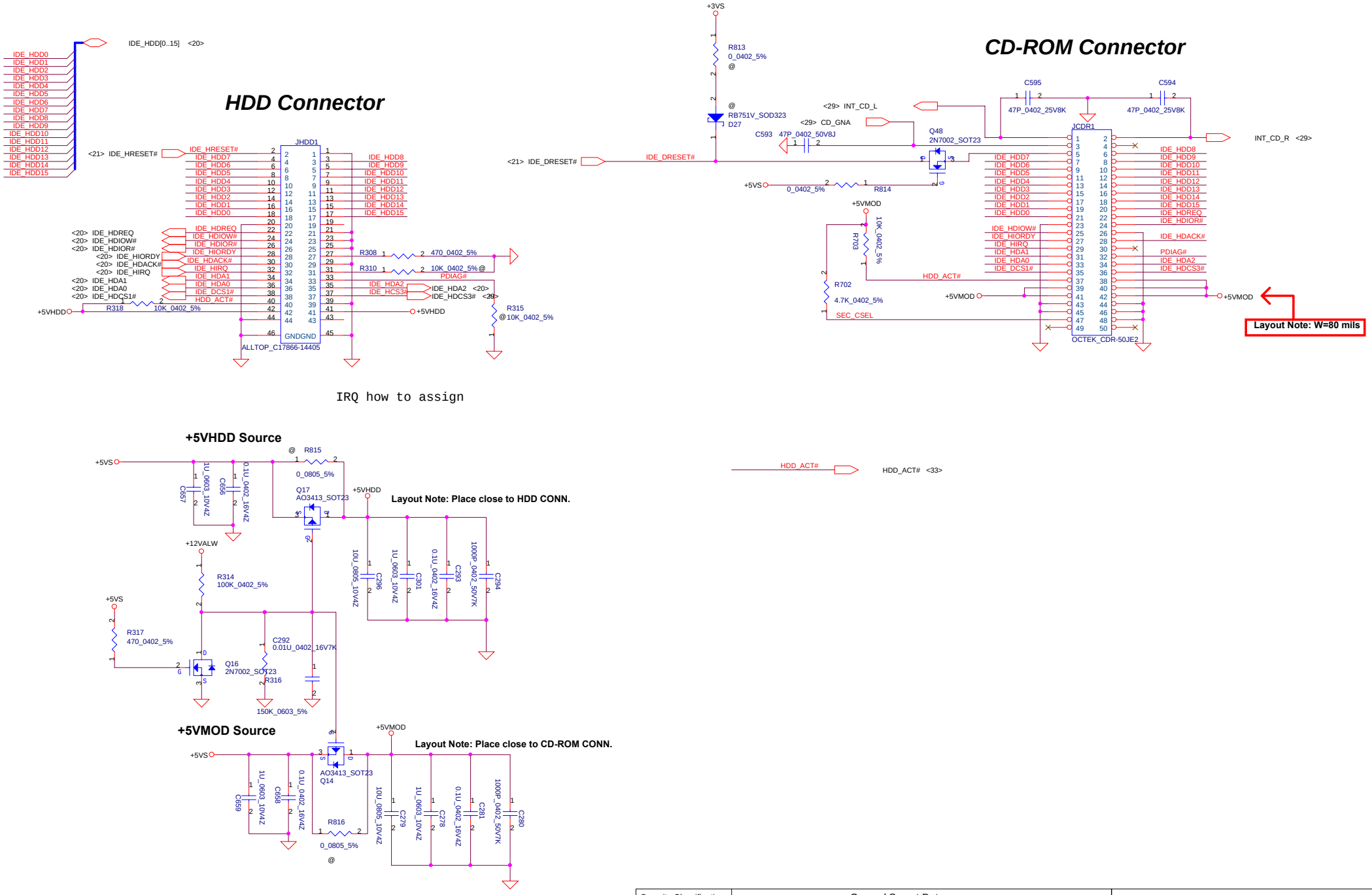
|---|---|---|---|
| Title | <Title> | | |
| Size | Document Number | | Rev |
| CustomLA-2362 | | 1 | |
| Date: | Friday, March 11, 2005 | Sheet | 22 of 52 |

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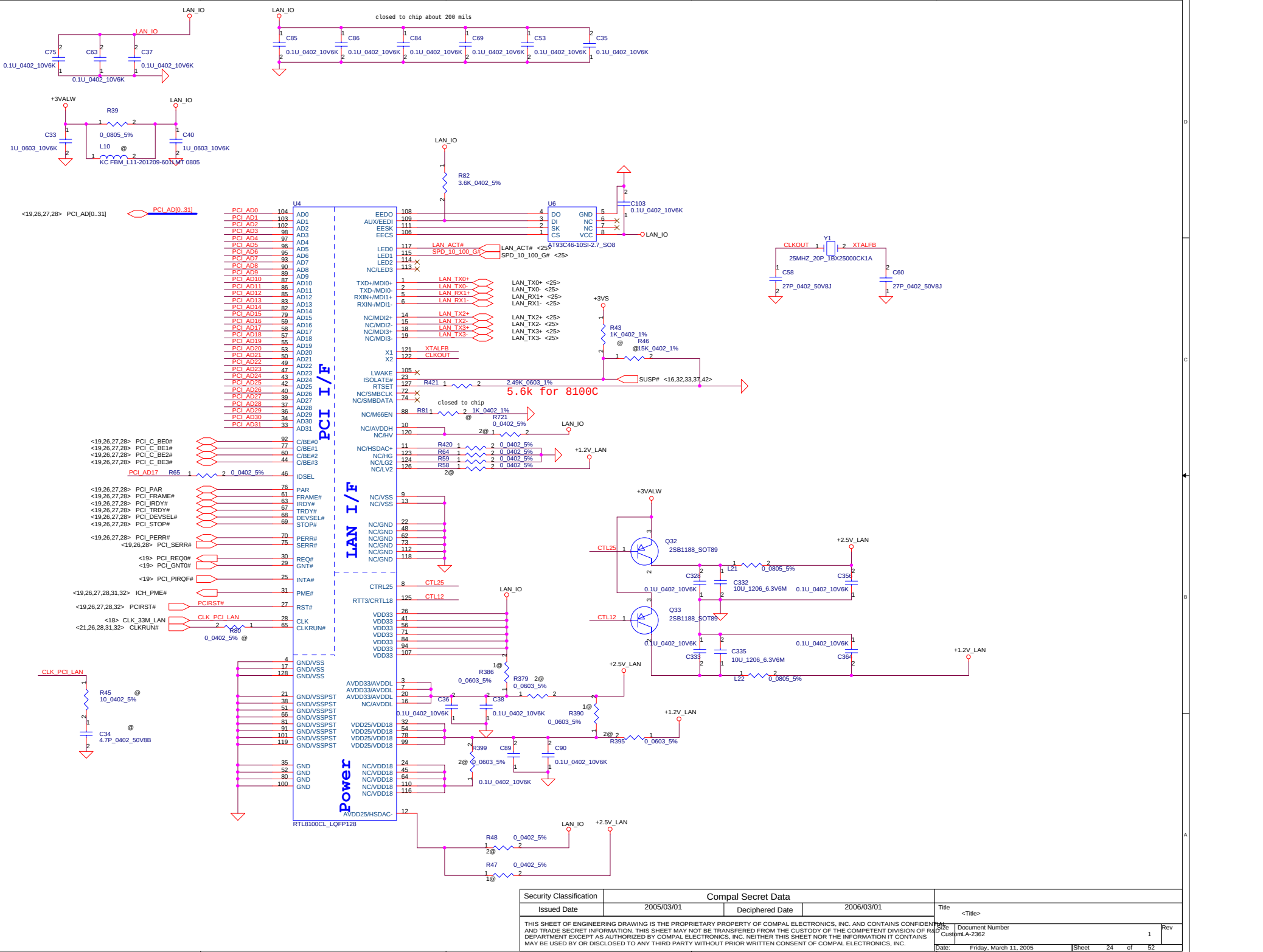
| Size | Document Number | | Rev |
| CustomLA-2362 | | 1 | |
| Date: Friday, March 11, 2005 | Sheet 23 of 52 | | |

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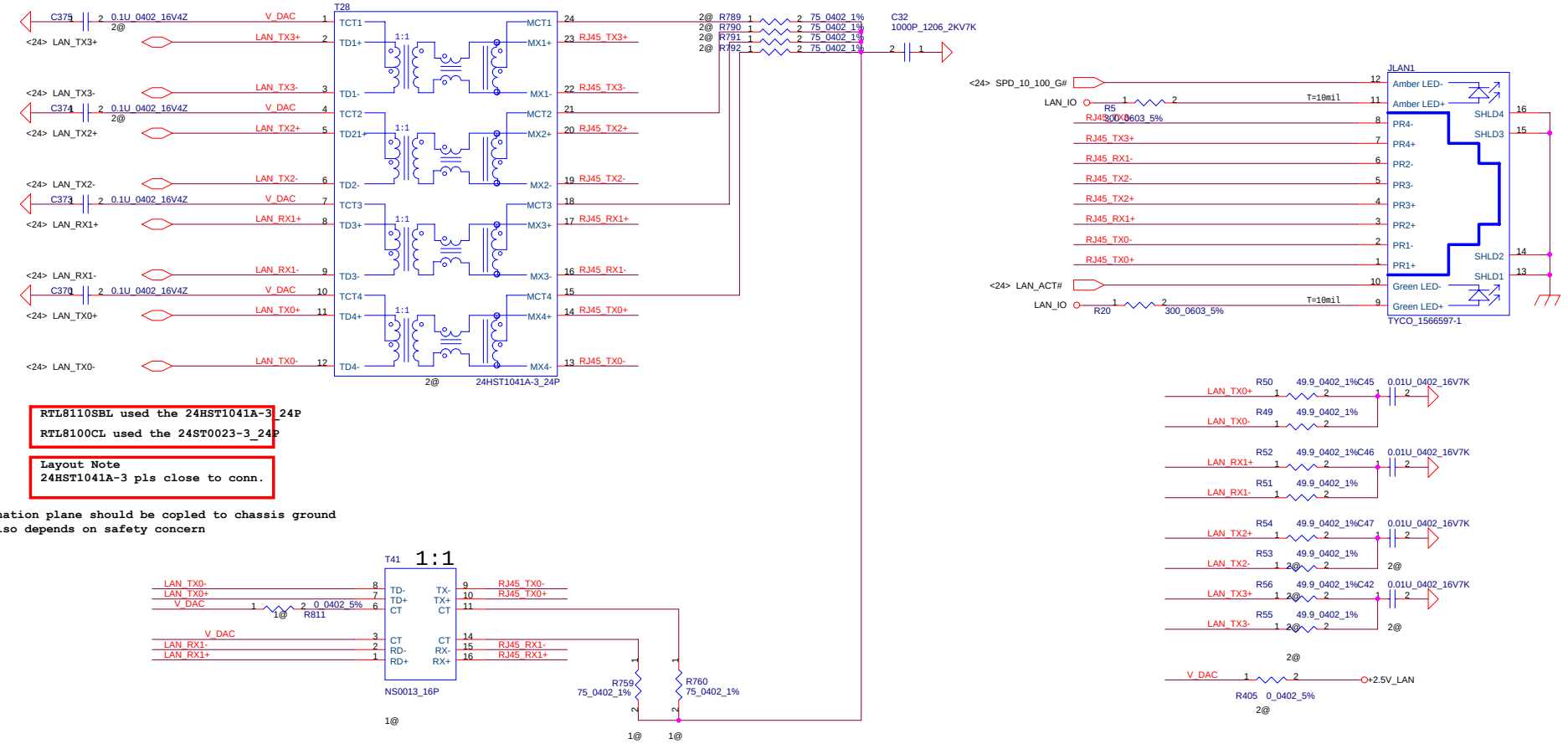



**RTL8110SBL used the 24HST1041A-3_24P**

**RTL8100CL used the 24ST0023-3_24P**

**Layout Note**
**24HST1041A-3 pls close to conn.**

**Termination plane should be copled to chassis ground and also depends on safety concern**



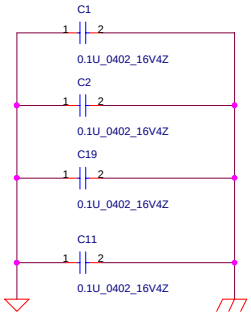







**Termination plane should be copled to chassis ground and also depends on safety concern**

**Please close to LAN IC**

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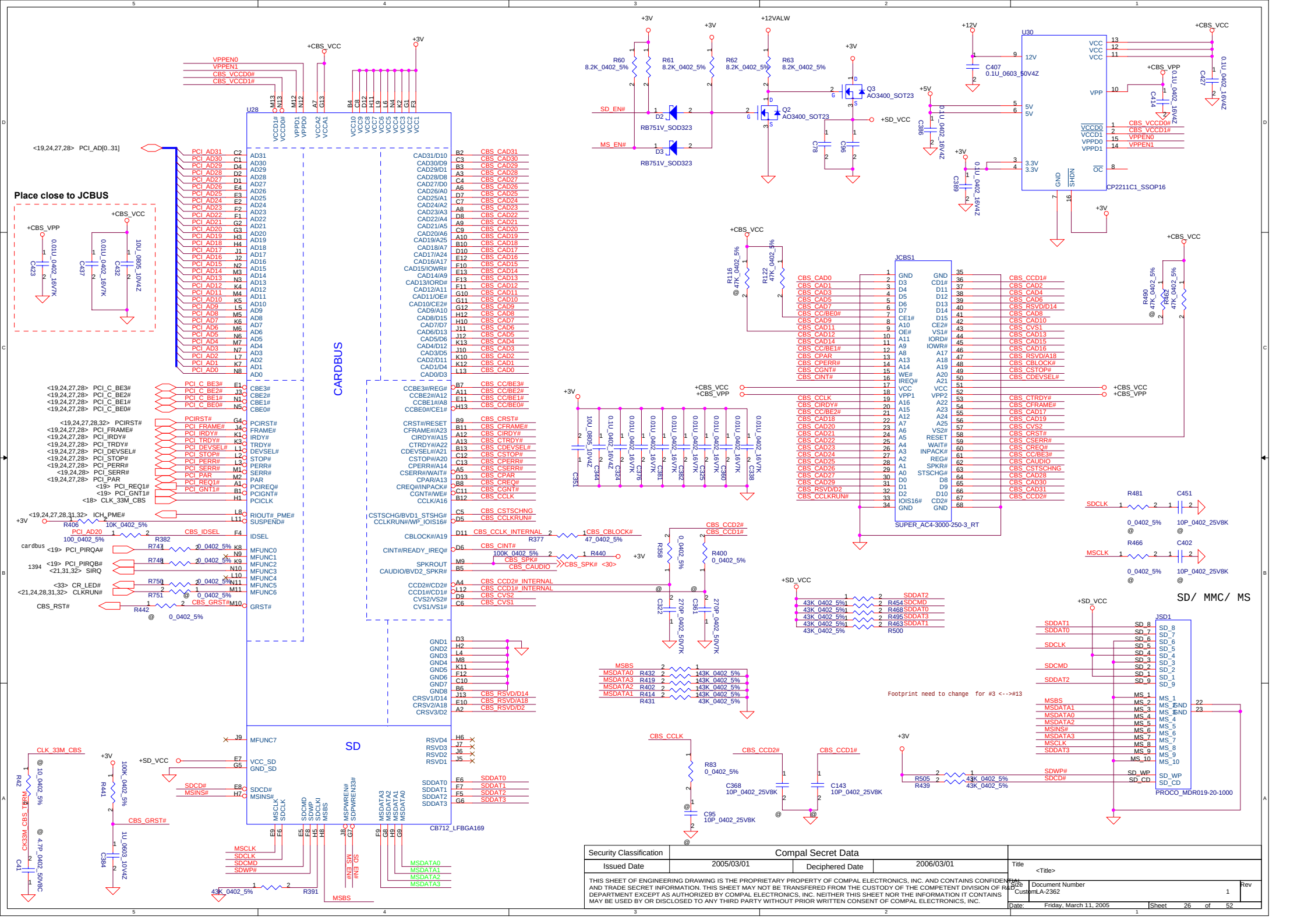
| Date: Friday, March 11, 2005 | Sheet 25 of 52 | | |


Place close to JCBUS
CARDBUS
SD
U28
CB712_LFBGA169
JCBS1
SUPER_AC4-3000-250-3_RT
U30
CP2211C1_SSOP16
JSD1
PROCO_MDR019-20-1000
SD/ MMC/ MS
Footprint need to change for #3 <-->#13
+CBS_VCC
+CBS_VPP
+3V
+5V
+12V
+12VALW
+SD_VCC
+SD_VCC
PCI_AD[0..31]
CBS_CAD[0..31]
SDDAT[0..3]
MSBS
CBS_RST#
CLK_33M_CBS
Security Classification
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Issued Date
2005/03/01
Deciphered Date
2006/03/01
Title
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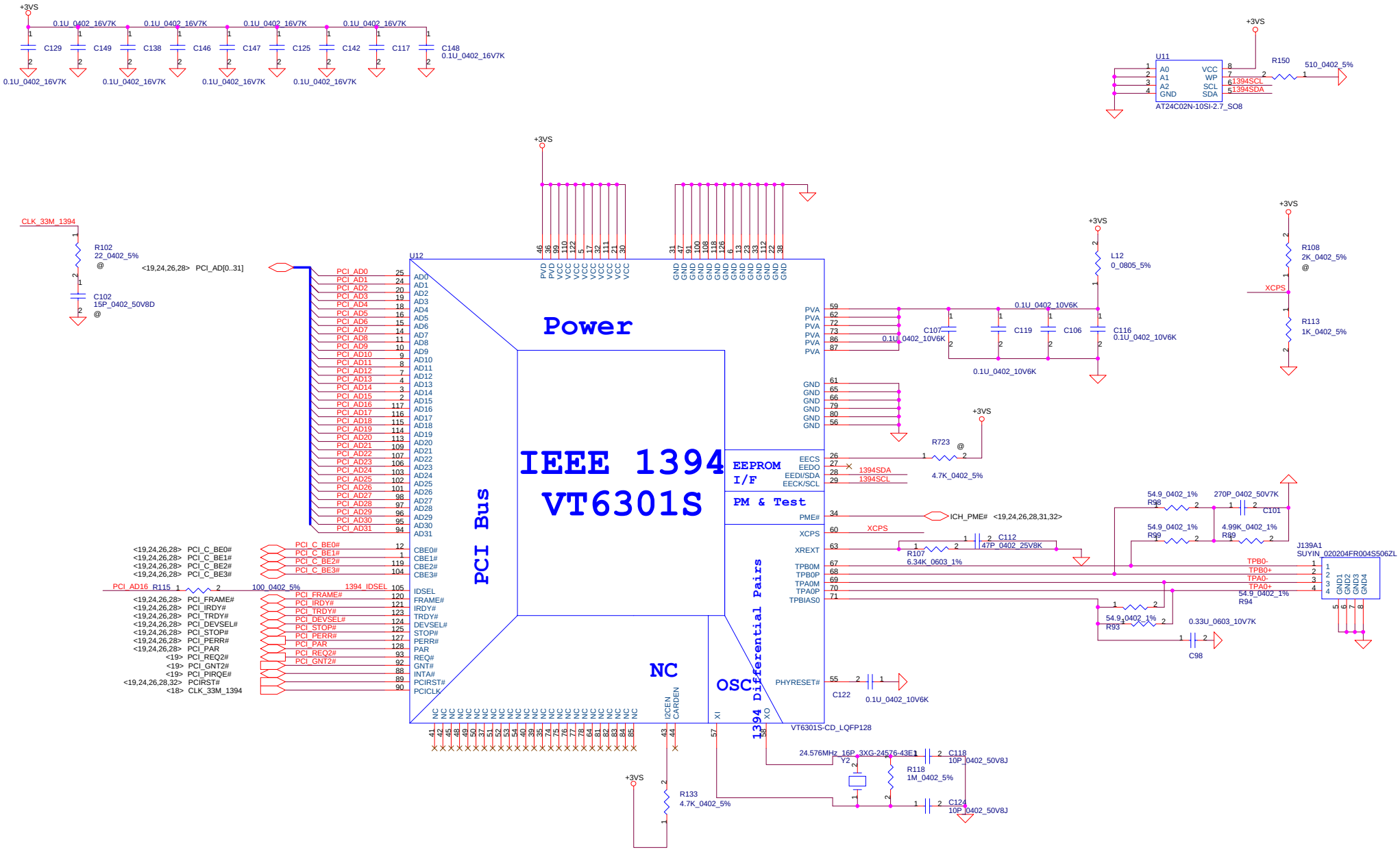
Size
CustomLA-2362
Document Number
Rev
Date:
Friday, March 11, 2005
Sheet
26
of
52

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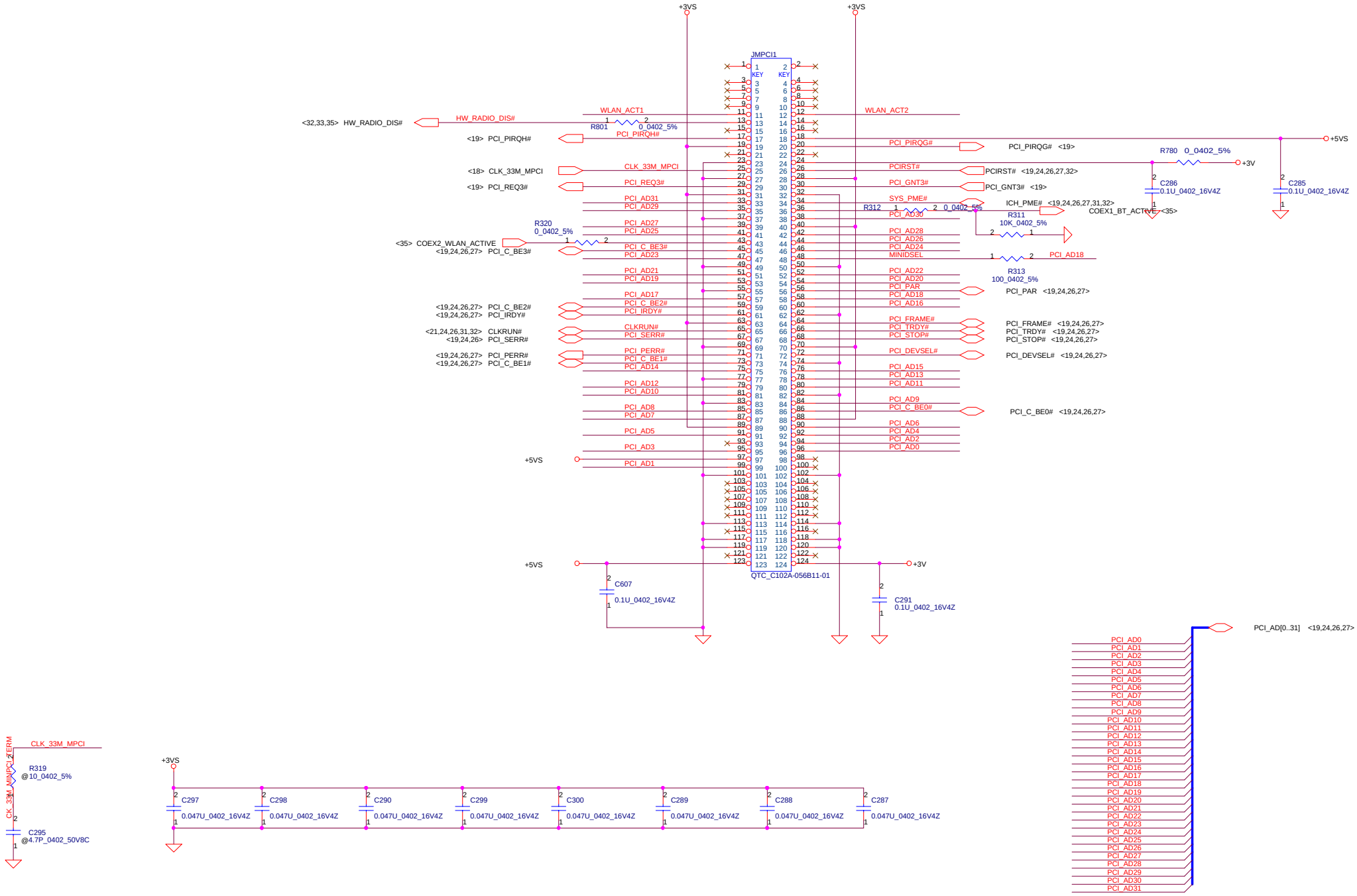
| Size | Document Number | | Rev |
| CustomLA-2362 | | 1 | |
| Date: | Friday, March 11, 2005 | Sheet 27 of 52 | |

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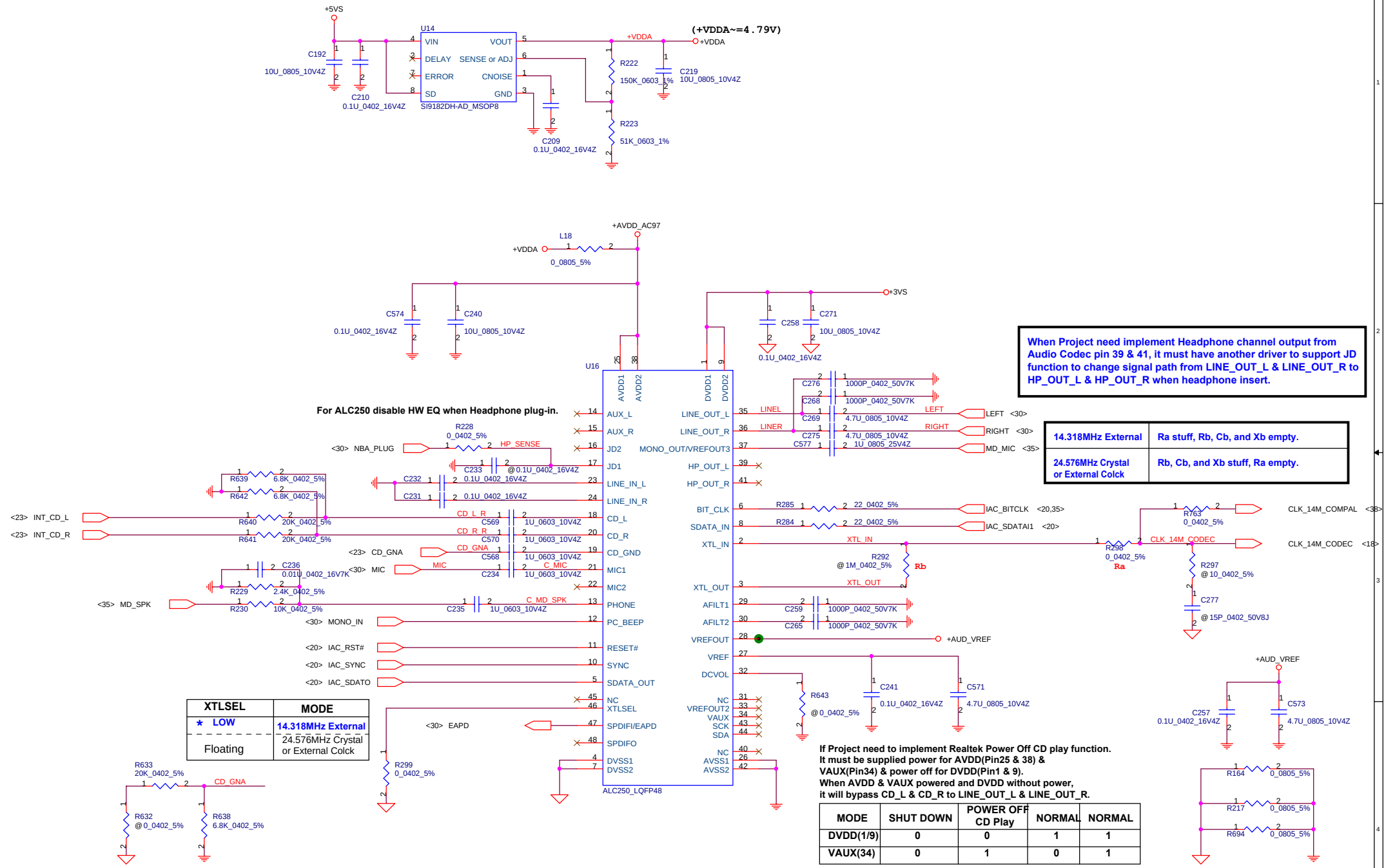
| Title | <Title> | | |
| Size | Document Number | | Rev |
| CustomLA-2362 | | | 1 |
| Date: | Friday, March 11, 2005 | Sheet | 28 of 52 |

# AC97 Codec

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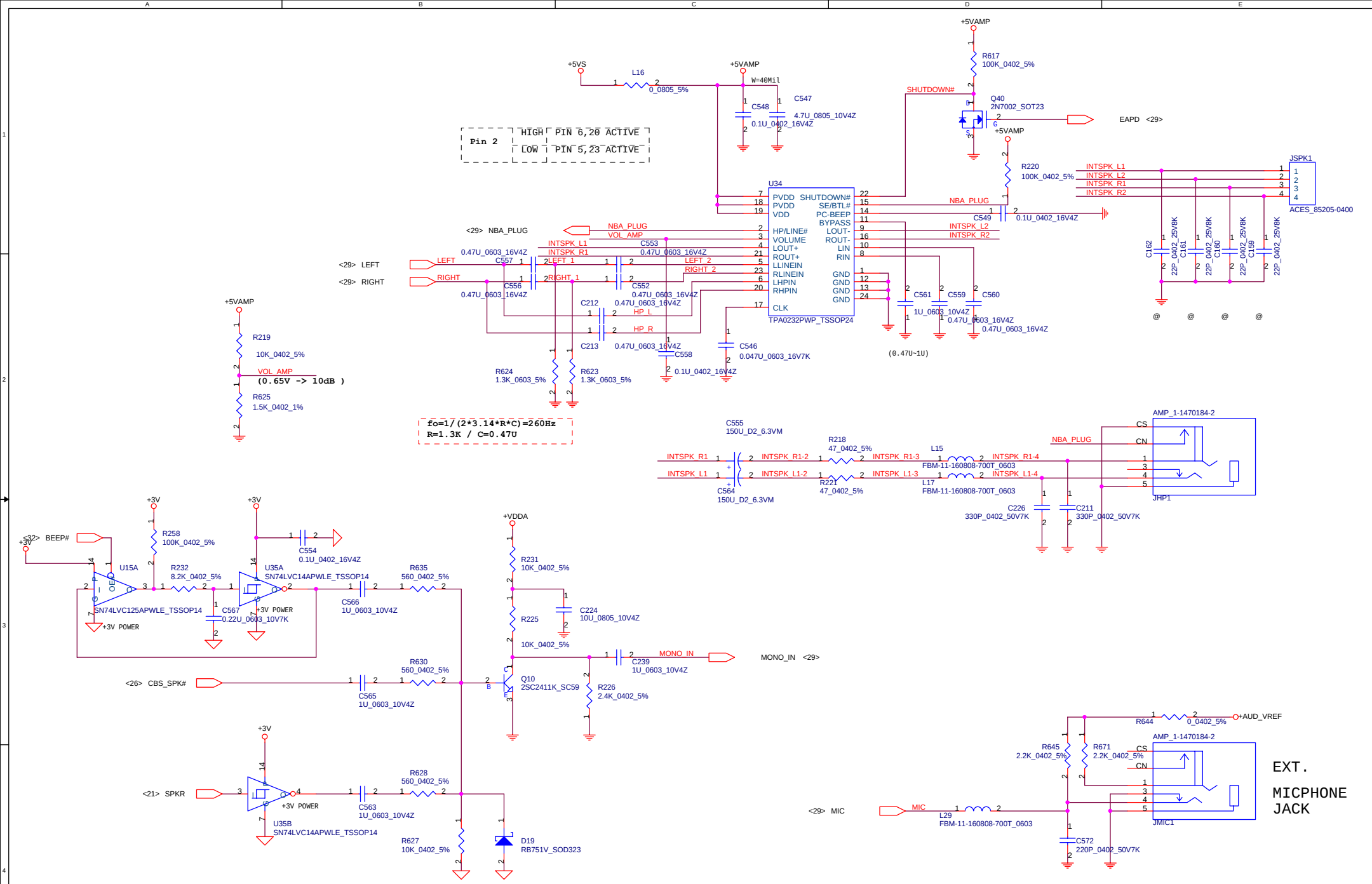
| CustomLA-2362 | | 1 | |
| Date: | Friday, March 11, 2005 | Sheet 29 of 52 | |

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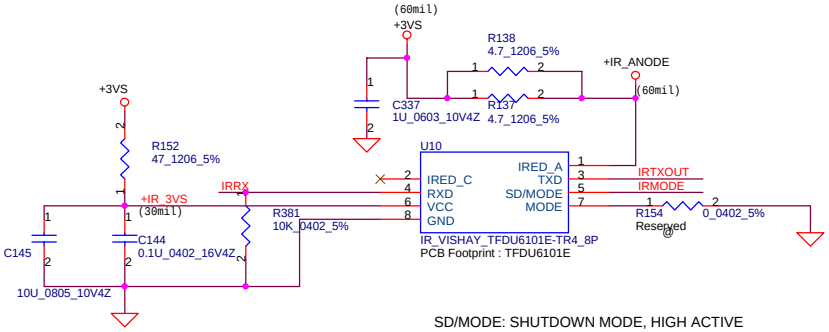
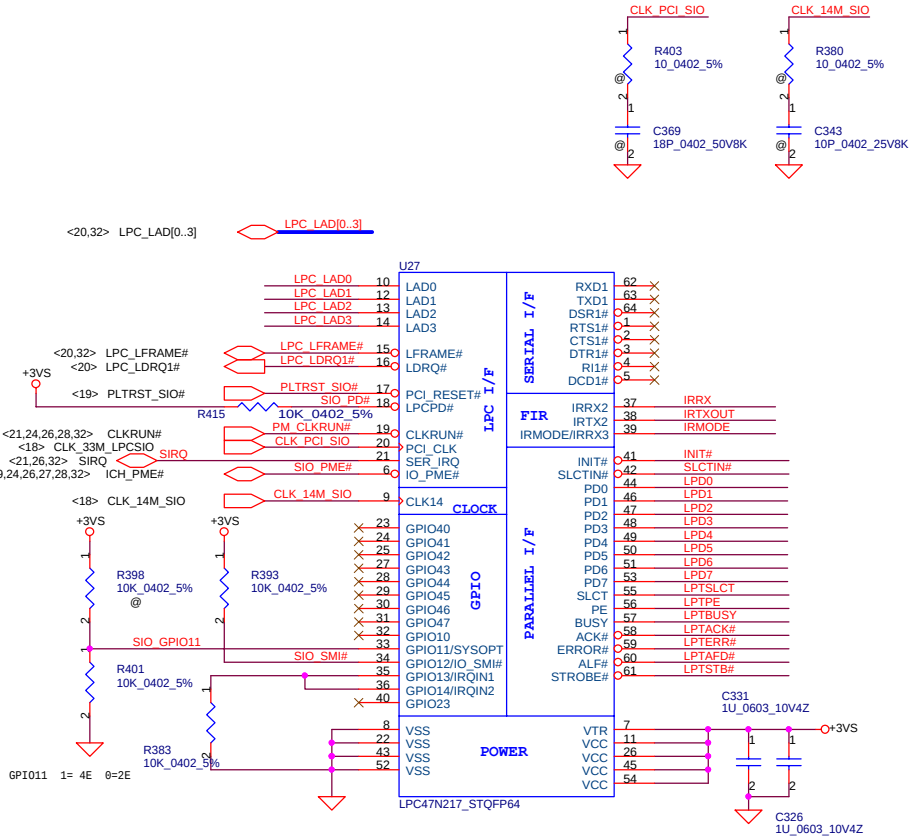
| Title | <Title> | | |
| Size | Document Number | | Rev |
| Custom | LA-2362 | | 1 |
| Date: | Friday, March 11, 2005 | Sheet | 30 of 52 |

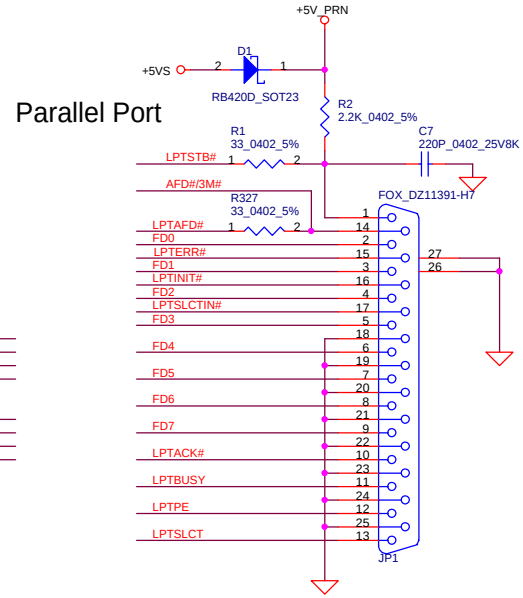
# FIR Module

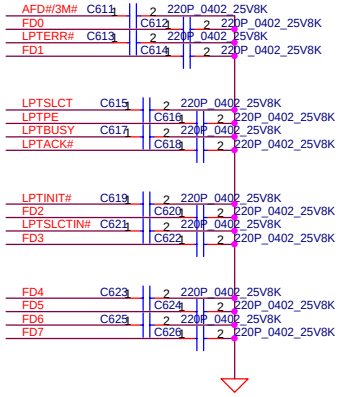


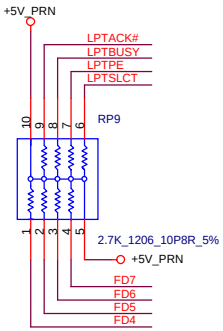

SD/MODE: SHUTDOWN MODE, HIGH ACTIVE
MODE: HIGH/LOW SPEED SELECT

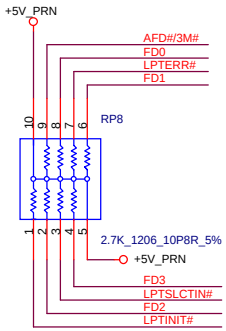


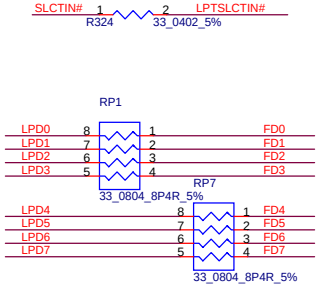

## Parallel Port

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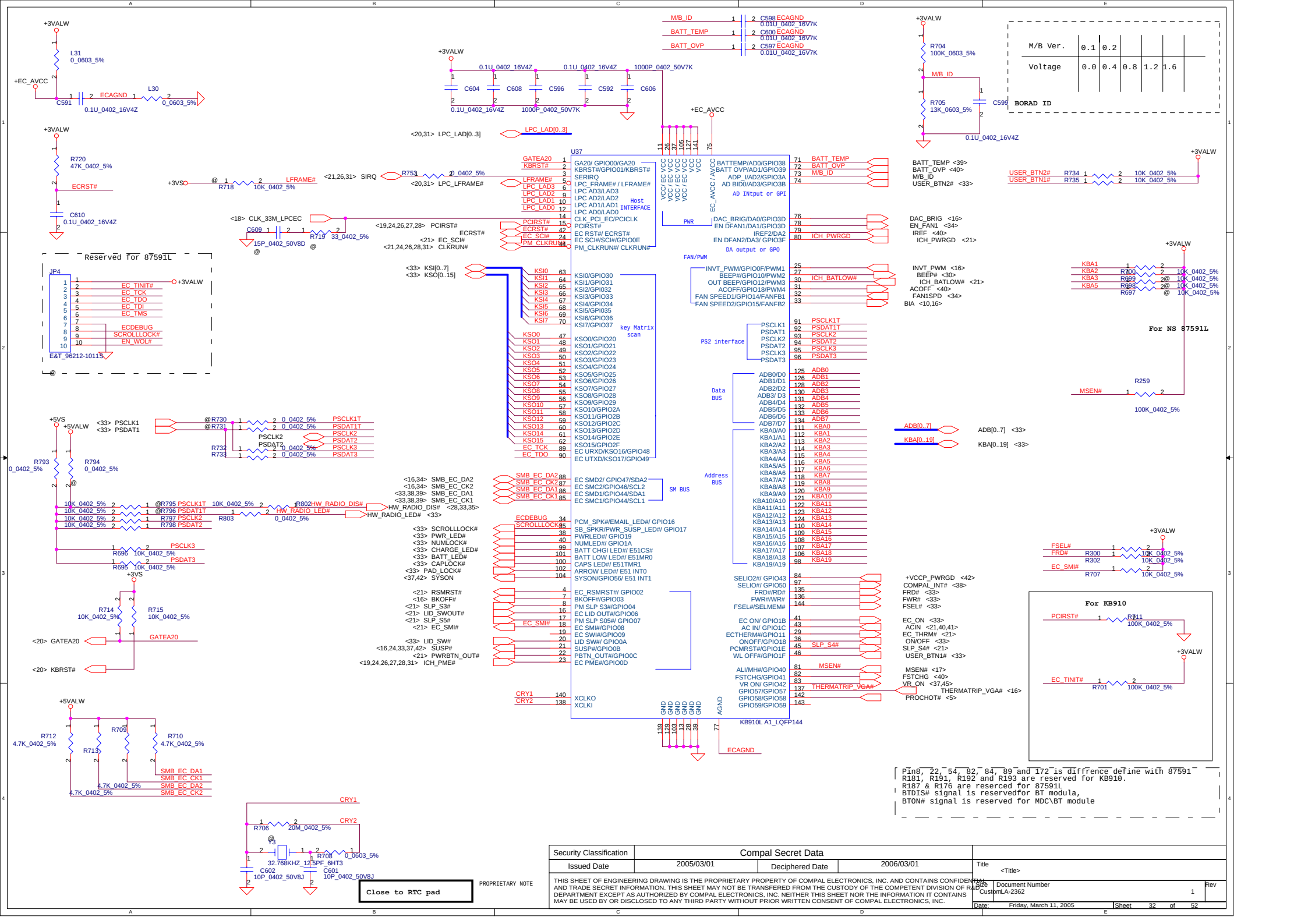
| Size | Document Number | | Rev |
| Custom | LA-2362 | | 1 |
| Date: | Friday, March 11, 2005 | Sheet | 31 of 52 |


+3VALW
+EC_AVCC
+5VS
+5VALW
+3VS
L31
0_0603_5%
L30
C591
0.1U_0402_16V4Z
ECAGND
M/B_ID
BATT_TEMP
BATT_OVP
C598 ECAGND 0.01U_0402_16V7K
C600 ECAGND 0.01U_0402_16V7K
C597 ECAGND 0.01U_0402_16V7K
C604
C608
C596
C592
C606
1000P_0402_50V7K
R704 100K_0603_5%
R705 13K_0603_5%
C599
BORAD ID
M/B Ver. 0.1 0.2
Voltage 0.0 0.4 0.8 1.2 1.6
R720 47K_0402_5%
ECRST#
C610 0.1U_0402_16V4Z
LPC_LAD[0..3]
U37
KB910L A1_LQFP144
GATEA20
KBRST#
LFRAME#
LPC_LAD3
LPC_LAD2
LPC_LAD1
LPC_LAD0
CLK_PCI_EC/PCICLK
PCIRST#
EC RST#/ ECRST#
EC SCI#/SCI#/GPIO0E
PM_CLKRUN#/ CLKRUN#
Host INTERFACE
PWR
FAN/PWM
DA output or GPO
AD INtput or GPI
key Matrix scan
PS2 interface
Data BUS
Address BUS
SM BUS
KSI[0..7]
KSO[0..15]
KSI0 KSI1 KSI2 KSI3 KSI4 KSI5 KSI6 KSI7
KSO0 KSO1 KSO2 KSO3 KSO4 KSO5 KSO6 KSO7 KSO8 KSO9 KSO10 KSO11 KSO12 KSO13 KSO14 KSO15
EC_TCK EC_TDO
SMB_EC_DA2 SMB_EC_CK2 SMB_EC_DA1 SMB_EC_CK1
ECDEBUG SCROLLLOCK#
EC_SMI#
CRY1 CRY2
XCLKO XCLKI
BATTEMP/AD0/GPIO3B
BATT OVP/AD1/GPIO39
ADP_I/AD2/GPIO3A
AD BID0/AD3/GPIO3B
DAC_BRIG/DA0/GPIO3D
EN DFAN1/DA1/GPIO3D
IREF2/DA2
EN DFAN2/DA3/ GPIO3F
INVT_PWM/GPIO0F/PWM1
BEEP#/GPIO10/PWM2
OUT BEEP/GPIO12/PWM3
ACOFF/GPIO18/PWM4
FAN SPEED1/GPIO14/FANFB1
FAN SPEED2/GPIO15/FANFB2
ICH_BATLOW#
ICH_PWRGD
PSCLK1T PSDAT1T PSCLK2 PSDAT2 PSCLK3 PSDAT3
ADB0 ADB1 ADB2 ADB3 ADB4 ADB5 ADB6 ADB7
KBA0 KBA1 KBA2 KBA3 KBA4 KBA5 KBA6 KBA7 KBA8 KBA9 KBA10 KBA11 KBA12 KBA13 KBA14 KBA15 KBA16 KBA17 KBA18 KBA19
SELIO2# GPIO43
SELIO# GPIO50
FRD#/RD#
FWR#/WR#
FSEL#/SELMEM#
EC ON/ GPIO1B
AC IN/ GPIO1C
ECTHERM#/GPIO11
ONOFF/GPIO18
PCMRST#/GPIO1E
WL OFF#/GPIO1F
SLP_S4#
ALI/MH#/GPIO40
FSTCHG/GPIO41
VR ON/ GPIO42
GPIO57/GPIO57
GPIO58/GPIO58
GPIO59/GPIO59
MSEN#
THERMATRIP_VGA#
GND GND GND GND GND GND GND
AGND
ECAGND
BATT_TEMP <39>
BATT_OVP <40>
M/B_ID
USER_BTN2# <33>
DAC_BRIG <16>
EN_FAN1 <34>
IREF <40>
ICH_PWRGD <21>
INVT_PWM <16>
BEEP# <30>
ICH_BATLOW# <21>
ACOFF <40>
FAN1SPD <34>
BIA <10,16>
ADB[0..7] <33>
KBA[0..19] <33>
+VCCP_PWRGD <42>
COMPAL_INT* <38>
FRD# <33>
FWR# <33>
FSEL# <33>
EC_ON <33>
ACIN <21,40,41>
EC_THRM# <21>
ON/OFF <33>
SLP_S4# <21>
USER_BTN1# <33>
MSEN# <17>
FSTCHG <40>
VR_ON <37,45>
THERMATRIP_VGA# <16>
PROCHOT# <5>
USER_BTN2# R734 10K_0402_5%
USER_BTN1# R735 10K_0402_5%
KBA1 KBA2 KBA3 KBA5 R700 R699 R698 R697 10K_0402_5%
For NS 87591L
R259 100K_0402_5%
MSEN#
FSEL# FRD# EC_SMI# R300 R302 R707 10K_0402_5%
For KB910
PCIRST# R711 100K_0402_5%
EC_TINIT# R701 100K_0402_5%
Reserved for 87591L
JP4
E&T_96212-1011S
EC_TINIT# EC_TCK EC_TDO EC_TDI EC_TMS ECDEBUG SCROLLLOCK# EN_WOL#
R718 10K_0402_5%
LFRAME#
R753 0_0402_5%
C609 15P_0402_50V8D
R719 33_0402_5%
PCIRST#
ECRST#
EC_SCI#
PM_CLKRUN#
R730 R731 R732 R733 0_0402_5%
PSCLK1T PSDAT1T PSCLK2 PSDAT2 PSCLK3 PSDAT3
R793 R794 0_0402_5%
R795 R796 R797 R798 10K_0402_5%
R802 HW_RADIO_DIS#
R803 0_0402_5%
HW_RADIO_LED#
R696 R695 10K_0402_5%
R714 R715 10K_0402_5%
GATEA20
KBRST#
R712 R713 R709 R710 4.7K_0402_5%
SMB_EC_DA1 SMB_EC_CK1 SMB_EC_DA2 SMB_EC_CK2
R706 20M_0402_5%
Y3 32.768KHZ_12.5PF_6HT3
R708 0_0603_5%
C602 C601 10P_0402_50V8J
Close to RTC pad
PROPRIETARY NOTE
Pin8, 22, 54, 82, 84, 89 and 172 is difference define with 87591
R181, R191, R192 and R193 are reserved for KB910.
R187 & R176 are reserved for 87591L
BTDIS# signal is reservedfor BT modula,
BTON# signal is reserved for MDC\BT module
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Title
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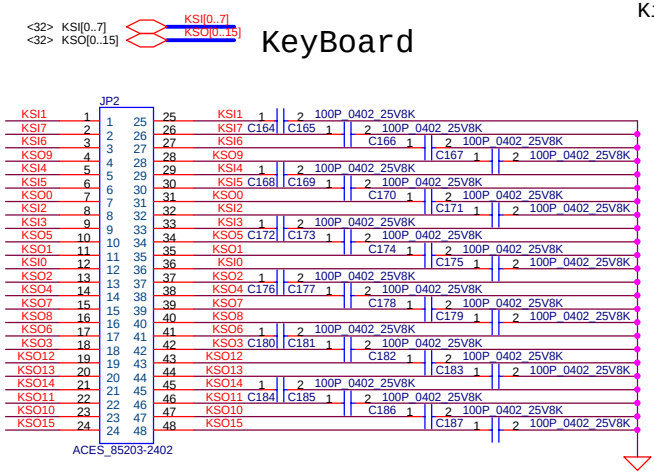
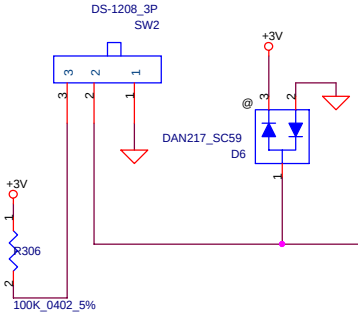
Size
Custom
Document Number
LA-2362
Rev
1
Date:
Friday, March 11, 2005
Sheet
32
of
52

# KeyBoard




# Killer switch

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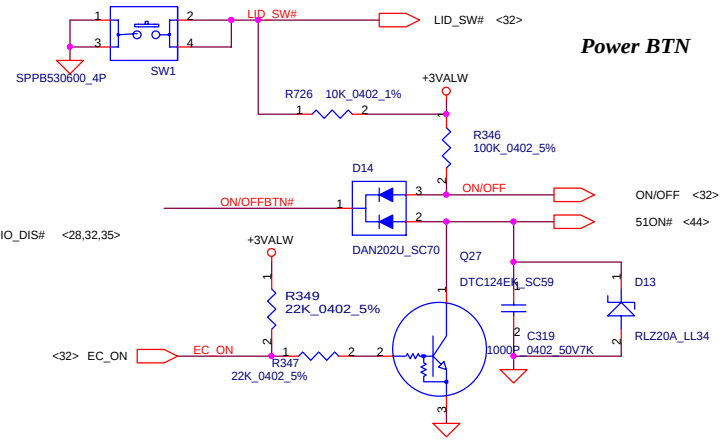
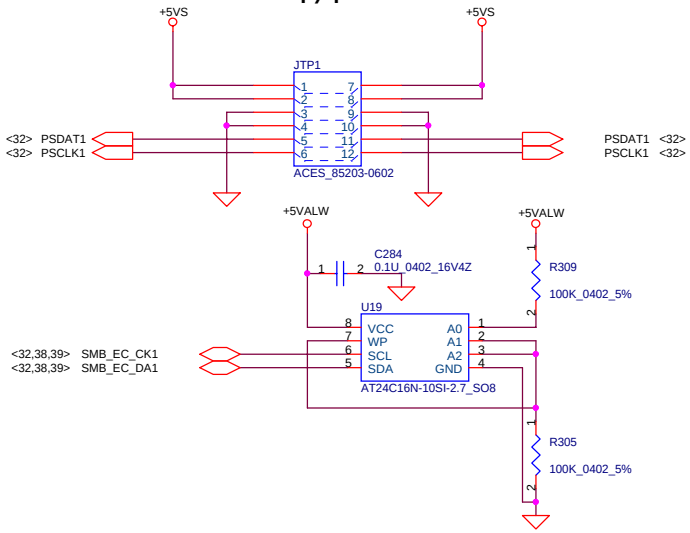


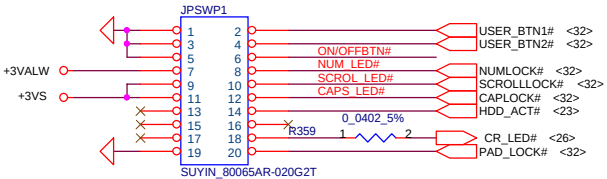

# T/P

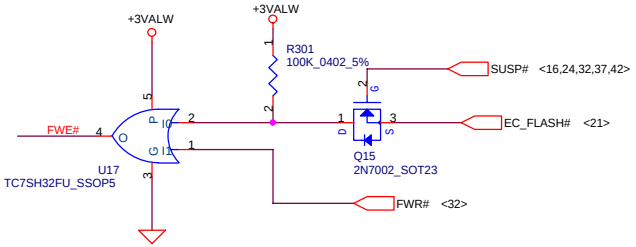


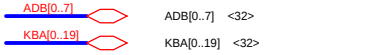


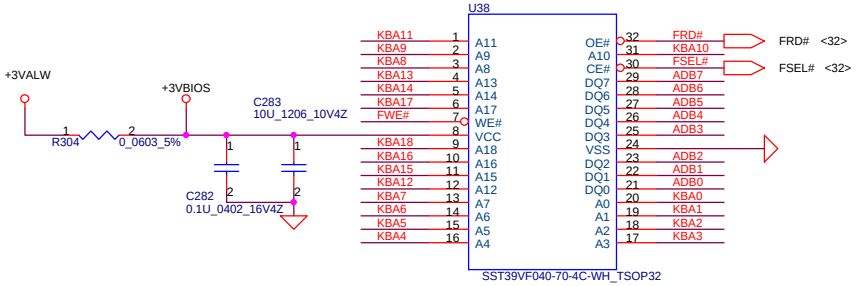


# SW Board

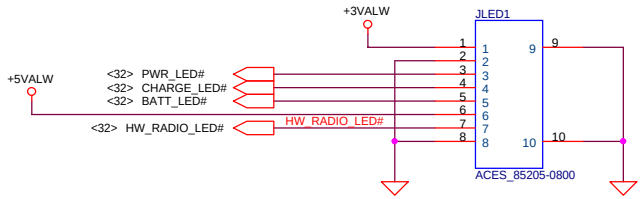



# LED Board

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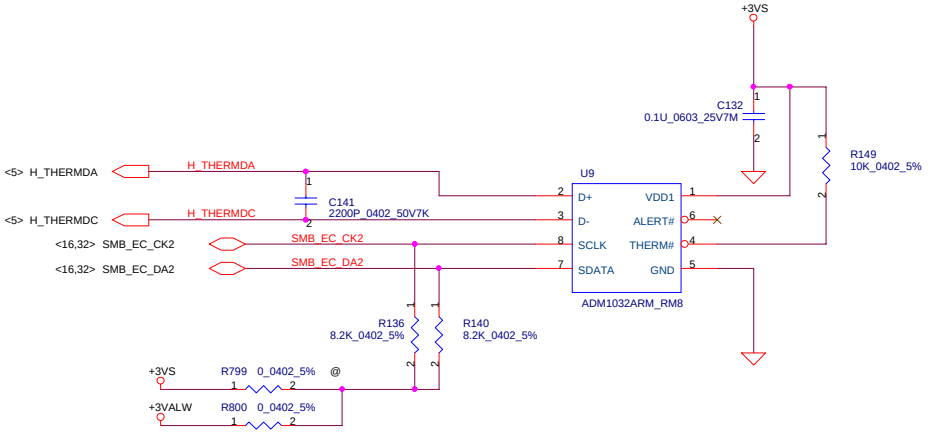
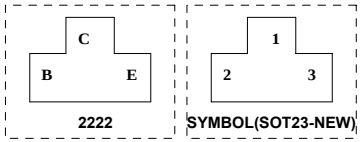
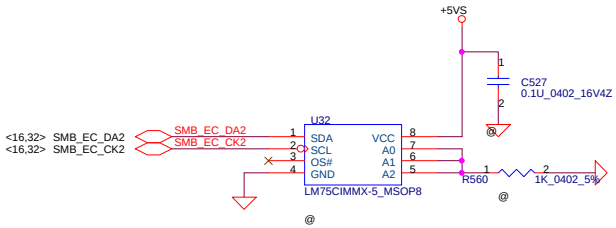
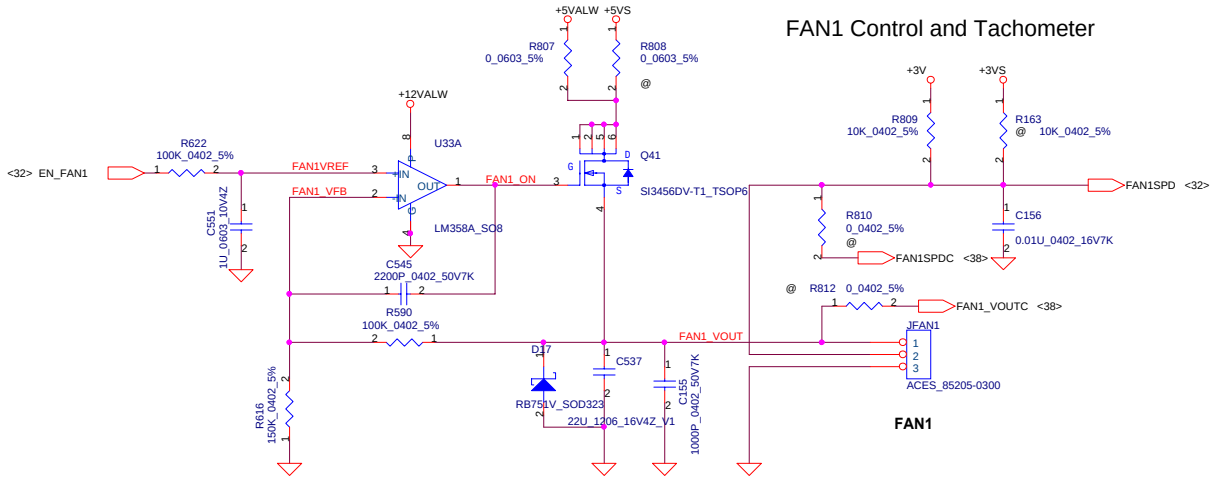
|---|---|---|---|
| Title | <Title> | | |
| Size | Document Number | | Rev |
| Custom | LA-2362 | | 1 |
| Date: | Friday, March 11, 2005 | Sheet | 33 of 52 |

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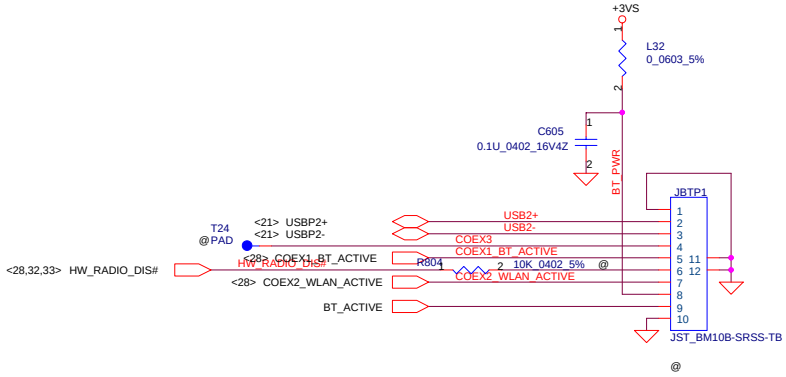
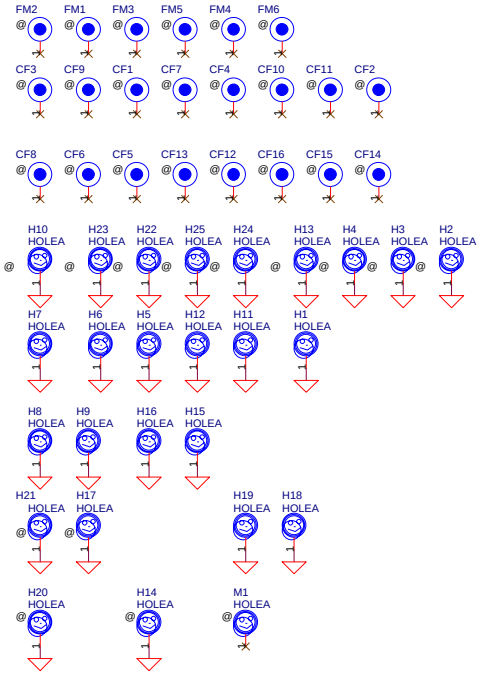
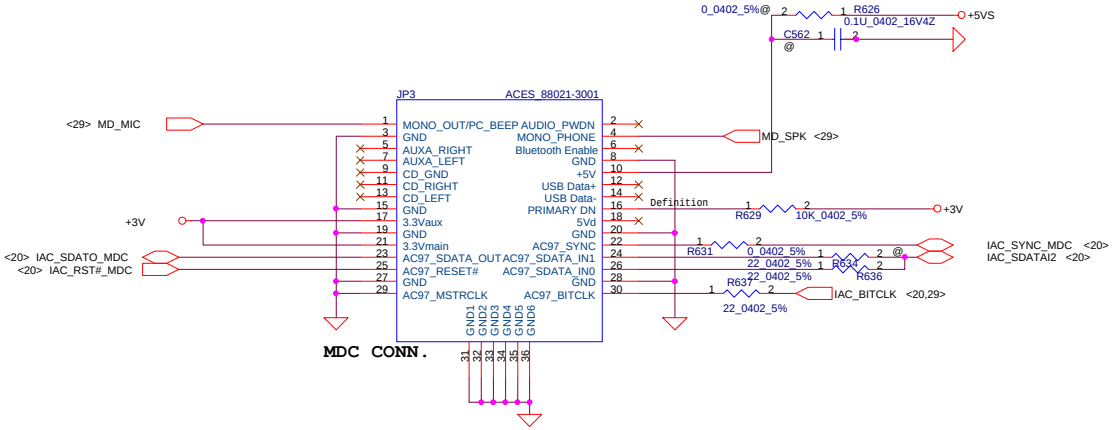
| Size | Document Number | | Rev |
| Custom | LA-2362 | | 1 |
| Date: | Friday, March 11, 2005 | Sheet 34 of 52 | |

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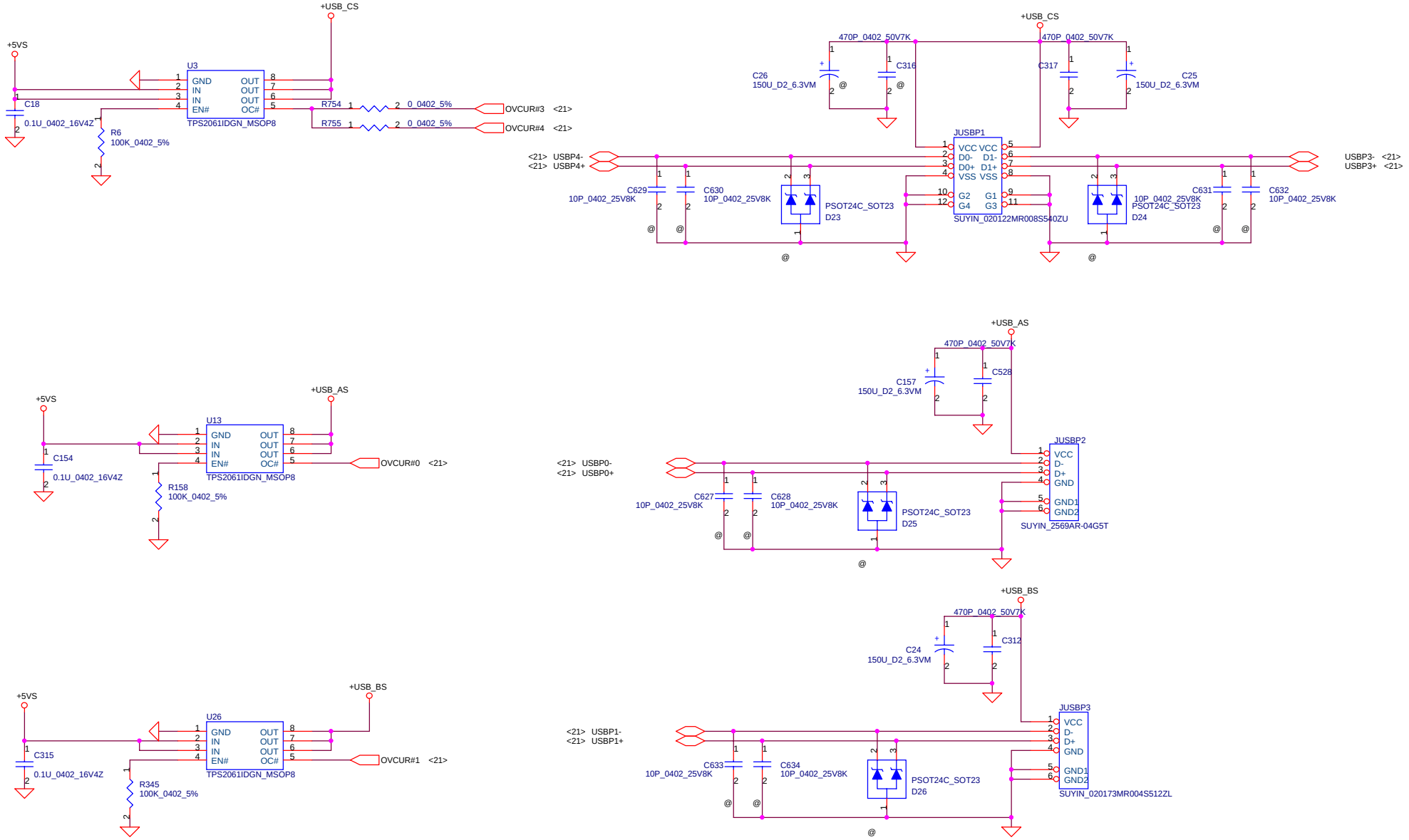
| Title | <Title> | | |
| Size: CustomLA-2362 | Document Number | | Rev: 1 |
| Date: Friday, March 11, 2005 | Sheet 35 of 52 | | |

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| Security Classification | Compal Secret Data | | |
| Issued Date | 2005/03/01 | Deciphered Date | 2006/03/01 |



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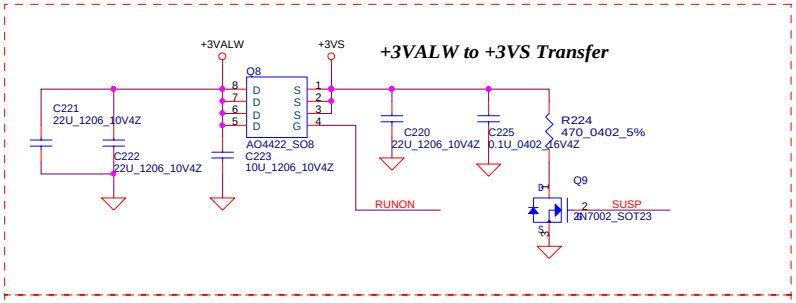
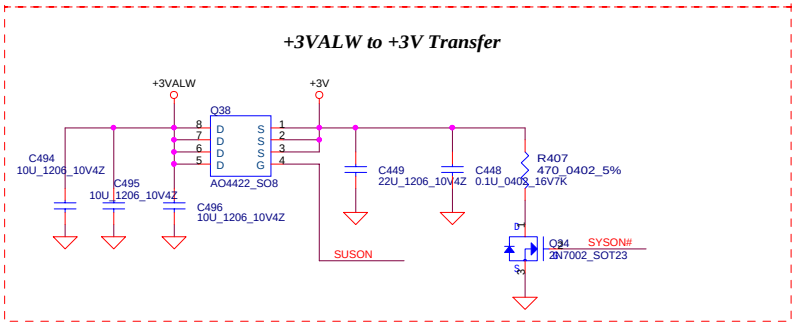
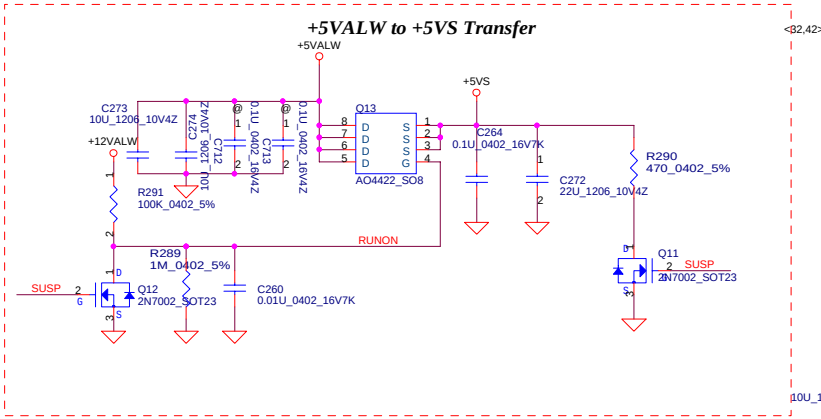
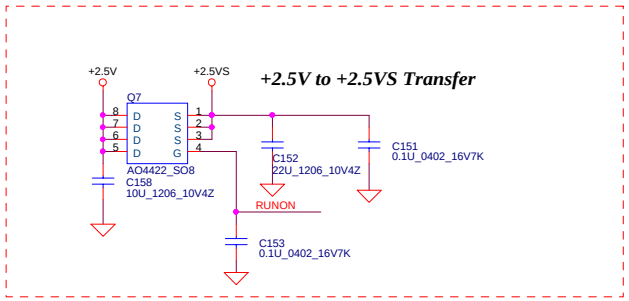
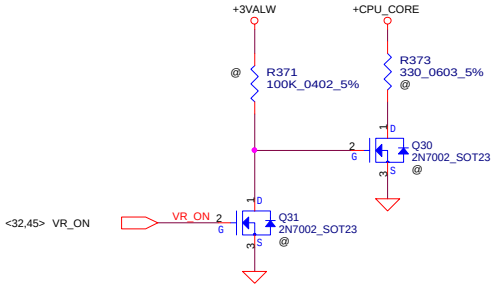
| Title | <Title> | | |
| Size | Document Number | | Rev |
| CustomLA-2362 | | 1 | |
| Date: | Friday, March 11, 2005 | Sheet 36 of 52 | |

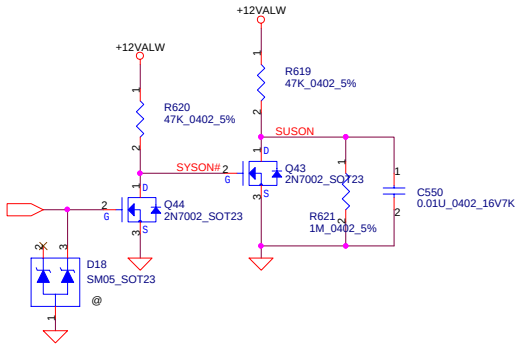


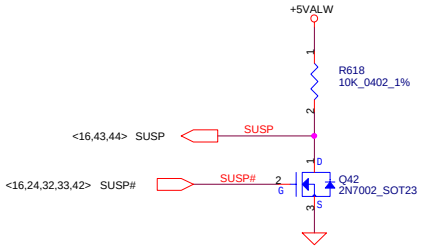



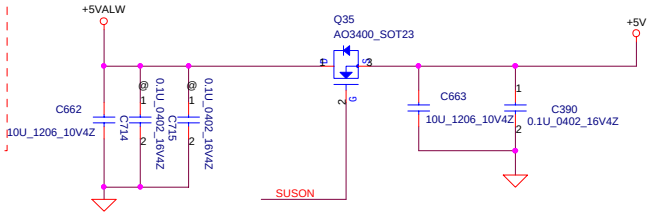



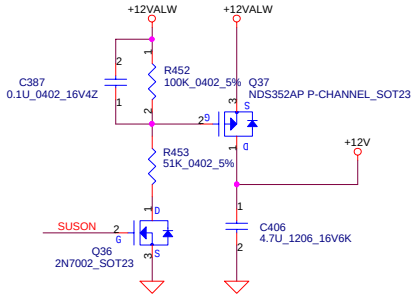

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| Security Classification | Compal Secret Data | | |
| Issued Date | 2005/03/01 | Deciphered Date | 2006/03/01 |



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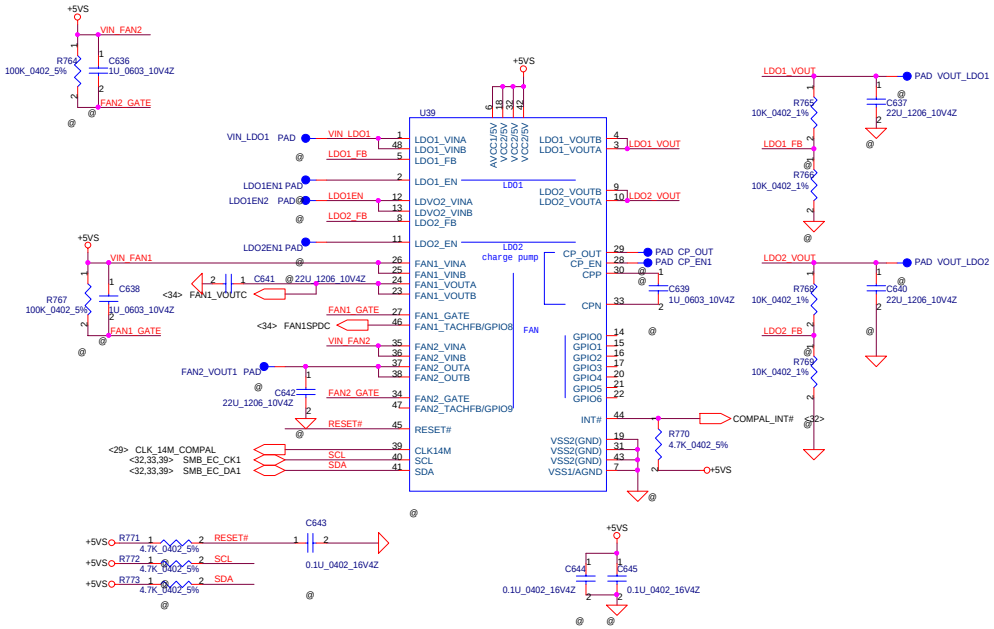
| Title | <Title> | | |
| Size: Custom | Document Number: LA-2362 | | Rev: 1 |
| Date: Friday, March 11, 2005 | Sheet 37 of 52 | | |

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| Security Classification | Compal Secret Data | | |
| Issued Date | 2005/03/01 | Deciphered Date | 2006/03/01 |



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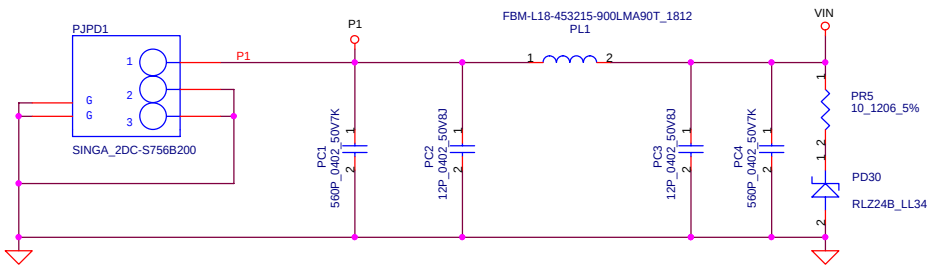
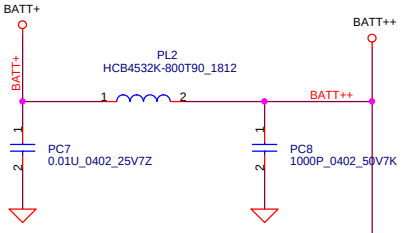
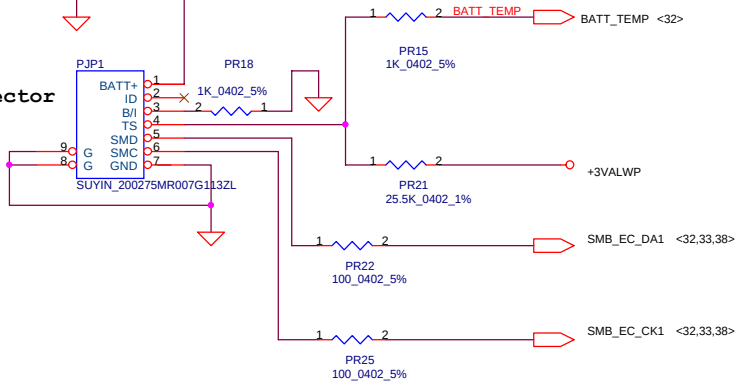
| Title | <Title> | | |
| Size C | Document Number LA-2362 | | Rev 1 |
| Date: Friday, March 11, 2005 | | Sheet 38 of 52 | |



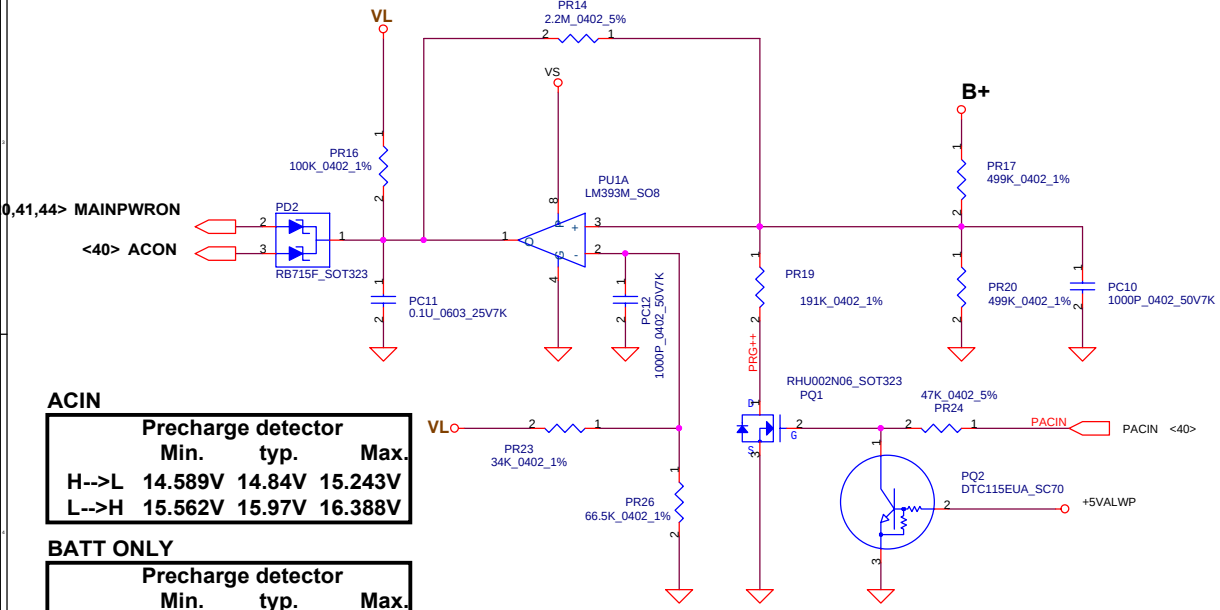



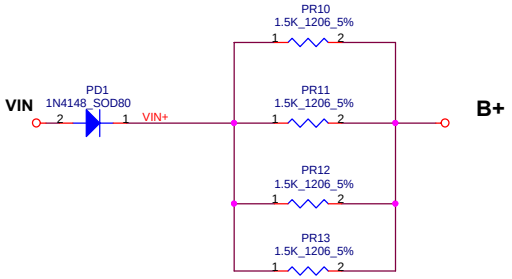




**PJPB1 battery connector**

**SMART Battery:**

**1.BAT+**
**2.ID**
**3.B/I**
**4.TS**
**5.SMD**
**6.SMC**
**7.GND**




**ACIN**

| Precharge detector | Min. | typ. | Max. |
|---|---|---|---|
| H-->L | 14.589V | 14.84V | 15.243V |
| L-->H | 15.562V | 15.97V | 16.388V |

**BATT ONLY**

| Precharge detector | Min. | typ. | Max. |
|---|---|---|---|
| H-->L | 6.138V | 6.214V | 6.359V |
| L-->H | 7.196V | 7.349V | 7.505V |



*Compal Electronics, Inc.*

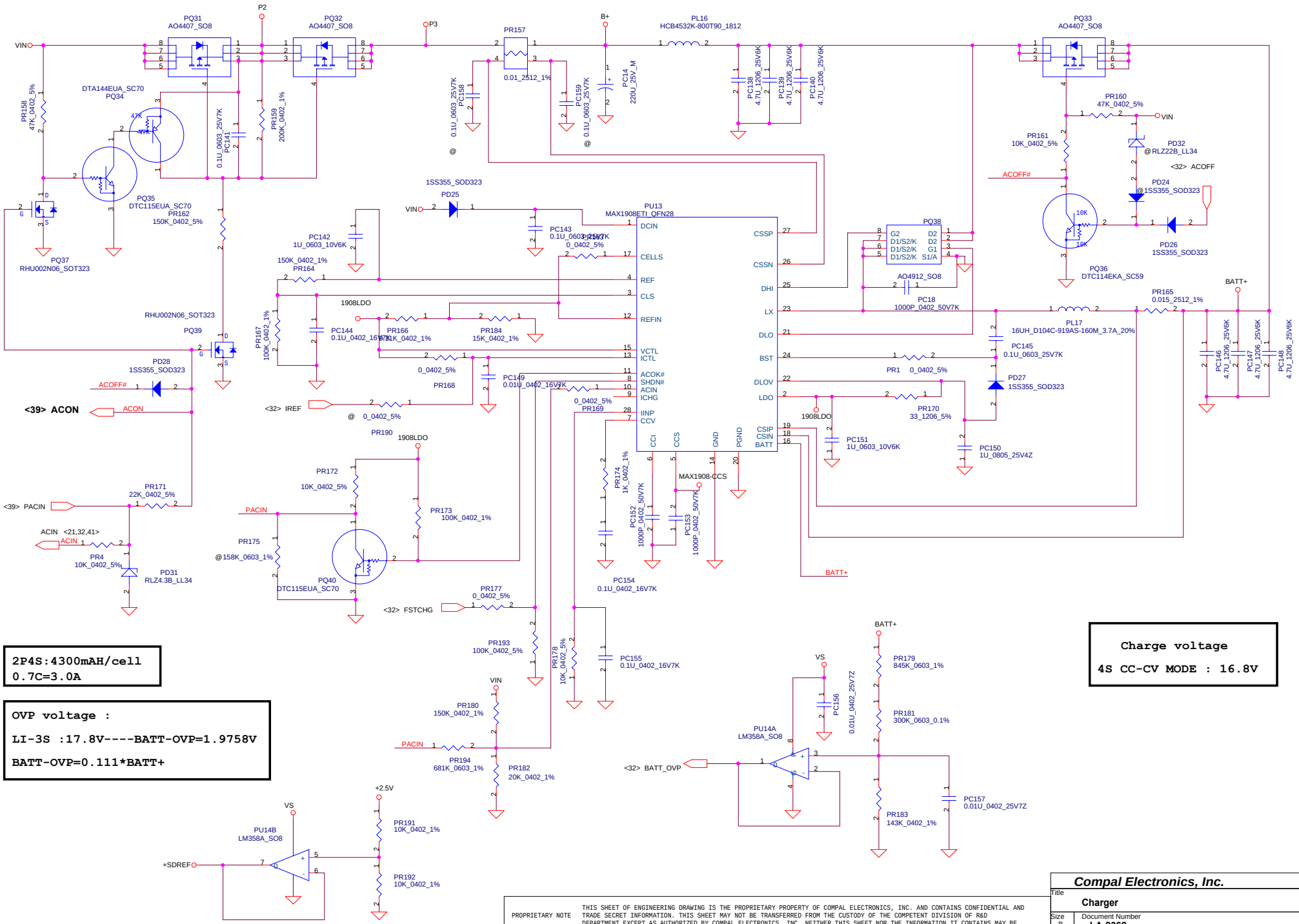
Title: **DCIN & DETECTOR & Precharge**

Size: B | Document Number: **LA-2362** | Rev: 1

Date: Friday, March 11, 2005 | Sheet 39 of 52

# Charger

**Iadp=0~3A(65W)**




**2P4S:4300mAH/cell**
**0.7C=3.0A**

**OVP voltage :**
**LI-3S :17.8V----BATT-OVP=1.9758V**
**BATT-OVP=0.111*BATT+**

**Charge voltage**
**4S CC-CV MODE : 16.8V**




Compal Electronics, Inc.

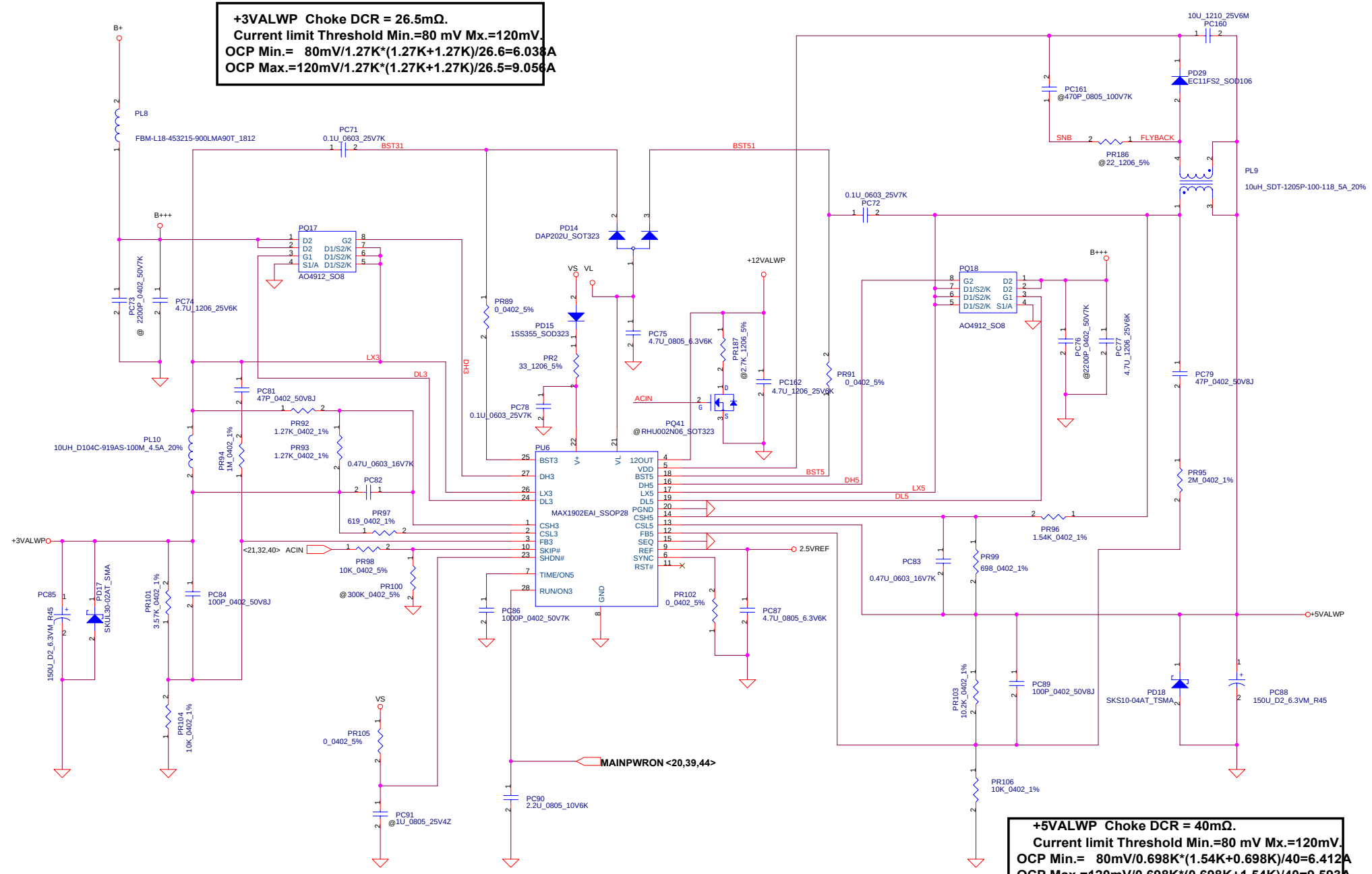
Title: Charger

Size: B | Document Number: LA-2362 | Rev: 1

Date: Friday, March 11, 2005 | Sheet 40 of 52

# +3.3V/+5V/+12V

**+3VALWP Choke DCR = 26.5mΩ.**
**Current limit Threshold Min.=80 mV Mx.=120mV.**
**OCP Min.= 80mV/1.27K*(1.27K+1.27K)/26.6=6.038A**
**OCP Max.=120mV/1.27K*(1.27K+1.27K)/26.5=9.056A**




**+5VALWP Choke DCR = 40mΩ.**
**Current limit Threshold Min.=80 mV Mx.=120mV.**
**OCP Min.= 80mV/0.698K*(1.54K+0.698K)/40=6.412A**
**OCP Max.=120mV/0.698K*(0.698K+1.54K)/40=9.593A**

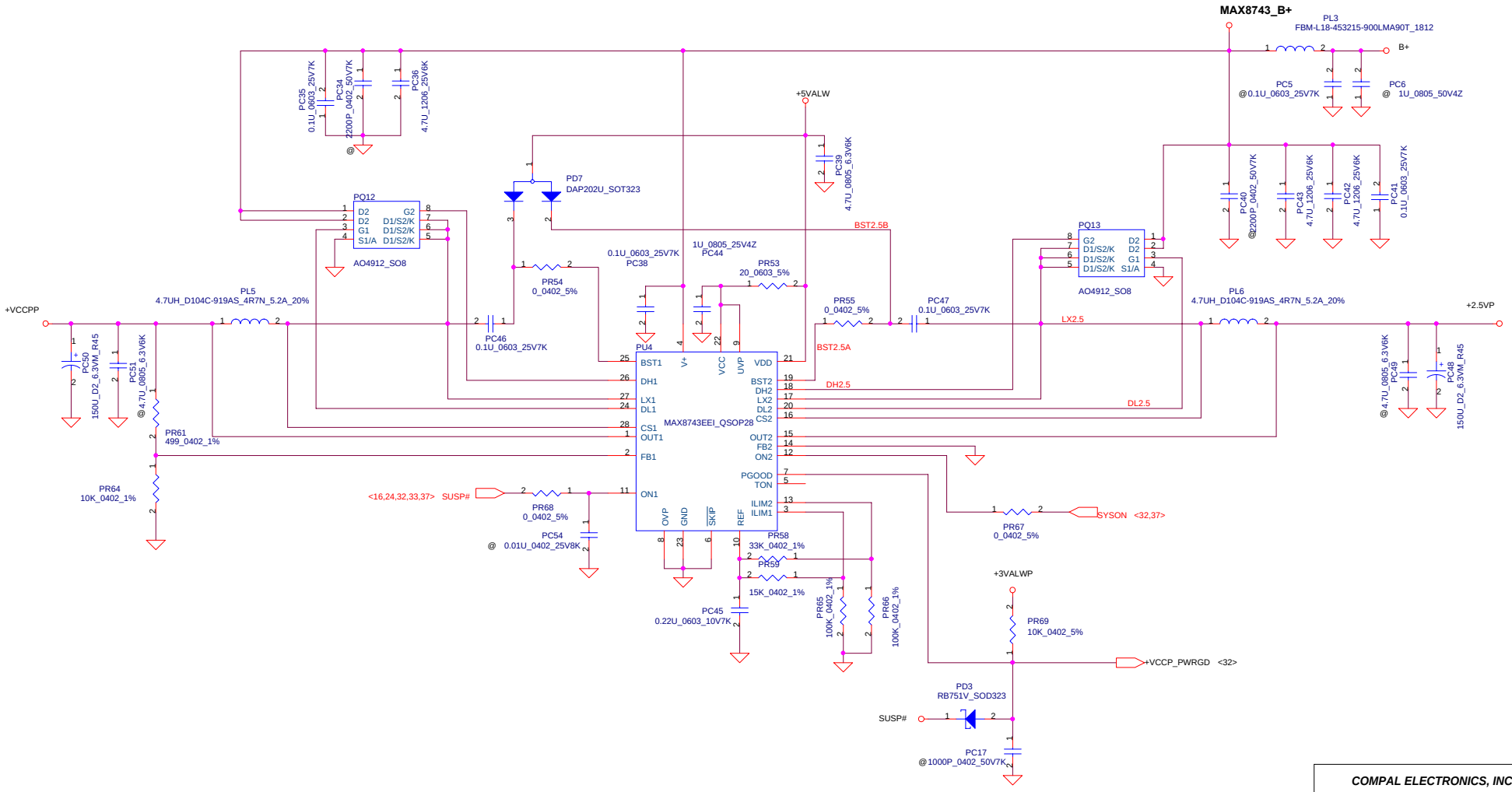
**RS2(PR64)=RS1(PR58)*RS3(PR61)/(RS1+RS3)**
**L/RL(DCR)=RS1*RS3(PR61)/(RS1+RS3)*Cs(PC56)**



| | |
|---|---|
| Compal Electronics, Inc. | |
| Title | 3.3V / 5V / 12V |
| Size: B | Document Number: LA-2362 |
| Rev | 0.1 |
| Date: Friday, March 11, 2005 | Sheet 41 of 52 |

Vin=19V,Vo=2.5V,Io=4.5A,Fs=345KHZ,L=4.7UH
Mosfet Rds(on) tpy.=19.7mΩ Max=24mΩ,Delta I =0.6118A
Iimit=ILIM(V)/10/Rds(on)+1/2 delta I
Iimit Min=1.98V*100K/(100K+15K)/10/31.2mΩ+0.3059=5.824A
Iimit Max=2.02V*100K/(100K+15K)/10/19.7mΩ+0.3059=9.821A
+VCCPP = 5.824A ~ 9.821A

Vin=19V,Vo=2.5V,Io=4.5A,Fs=255KHZ,L=4.7UH
Mosfet Rds(on) tpy.=19.7mΩ Max=24mΩ,Delta I =1.8115A
Iimit=ILIM(V)/10/Rds(on)+1/2 delta I
Iimit Min=1.98V*100K/(100K+33K)/10/31.2mΩ+0.905=5.6765A
Iimit Max=2.02V*100K/(100K+33K)/10/19.7mΩ+0.905=8.614A
+2.5VP = 5.6765A ~ 8.614A



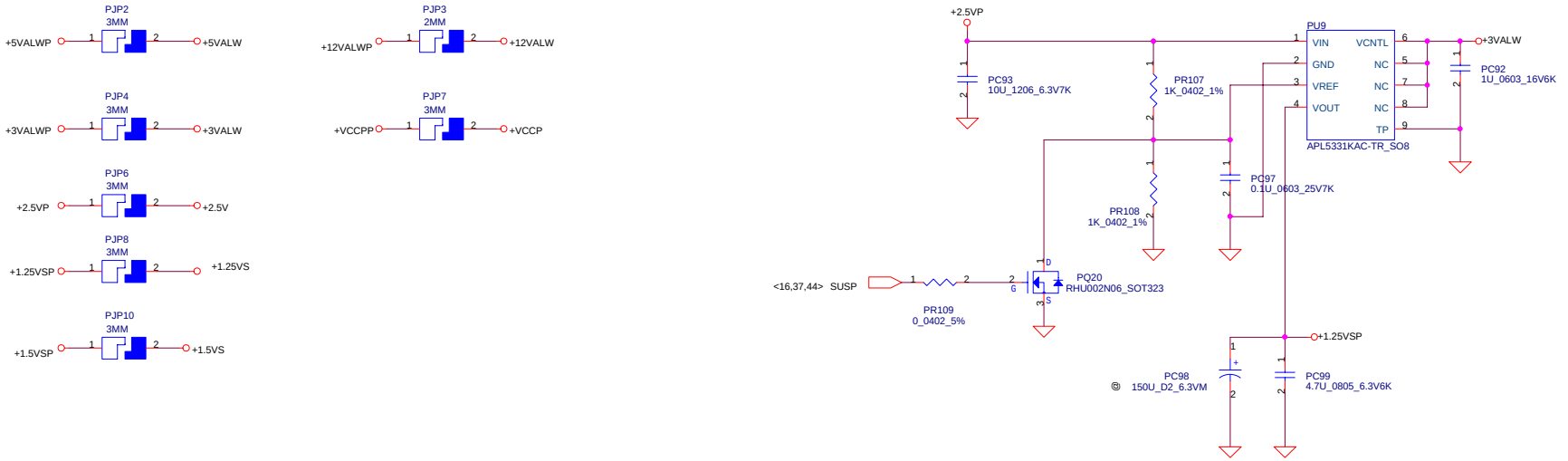



COMPAL ELECTRONICS, INC

Title: +2.5VP & +VCCPP

Size: B | Document Number: LA-2362 | Rev: 1

Date: Friday, March 11, 2005 | Sheet 42 of 52



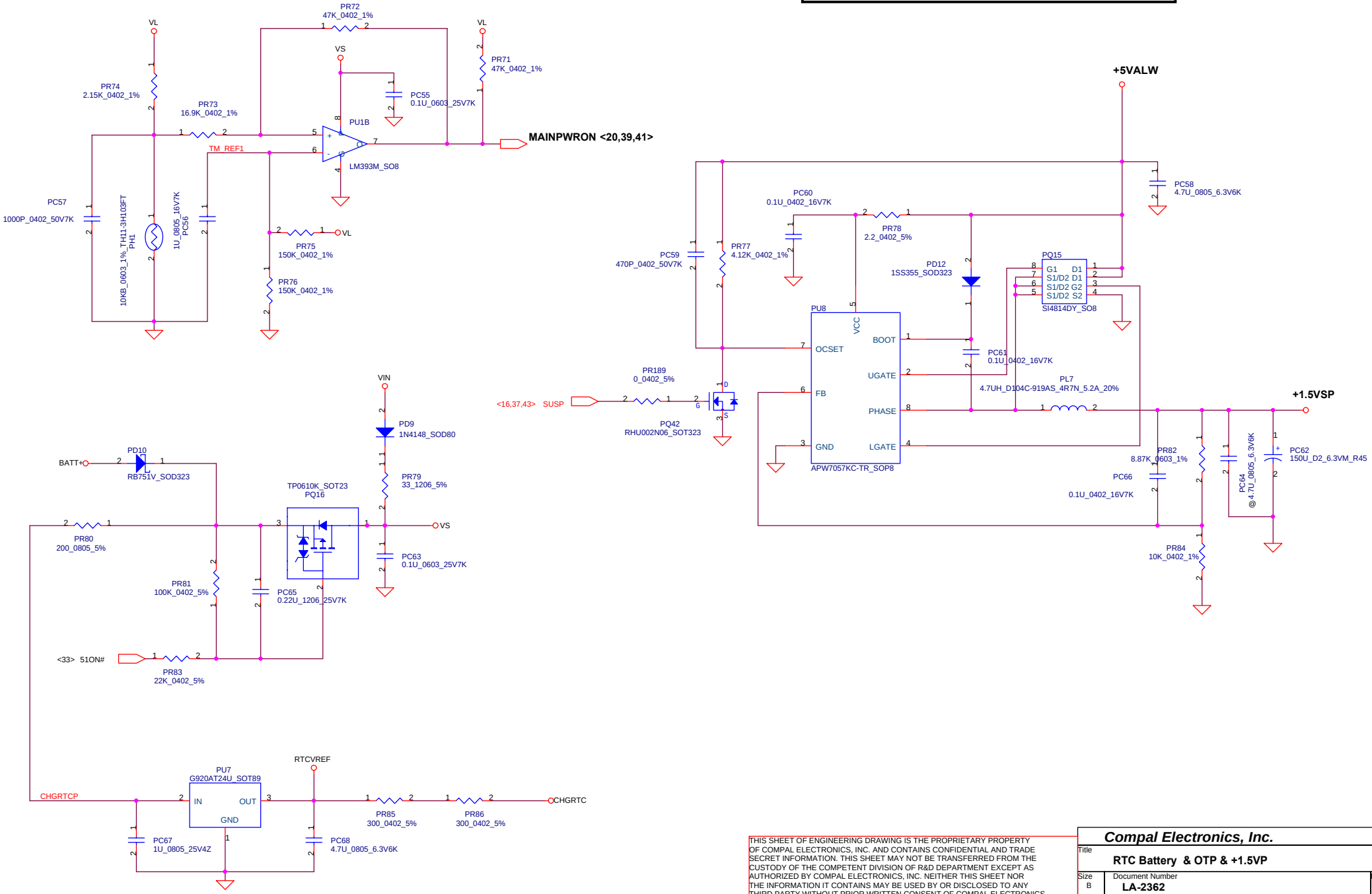



**Compal Electronics, Inc.**

| | | |
|---|---|---|
| Title | +1.25VSP | |
| Size: B | Document Number: LA-2362 | Rev: 1 |
| Date: Friday, March 11, 2005 | Sheet 43 of 52 | |

**PH2 under CPU botten side :**
CPU thermal protection at 80 degree C
Recovery at 44(45) degree C

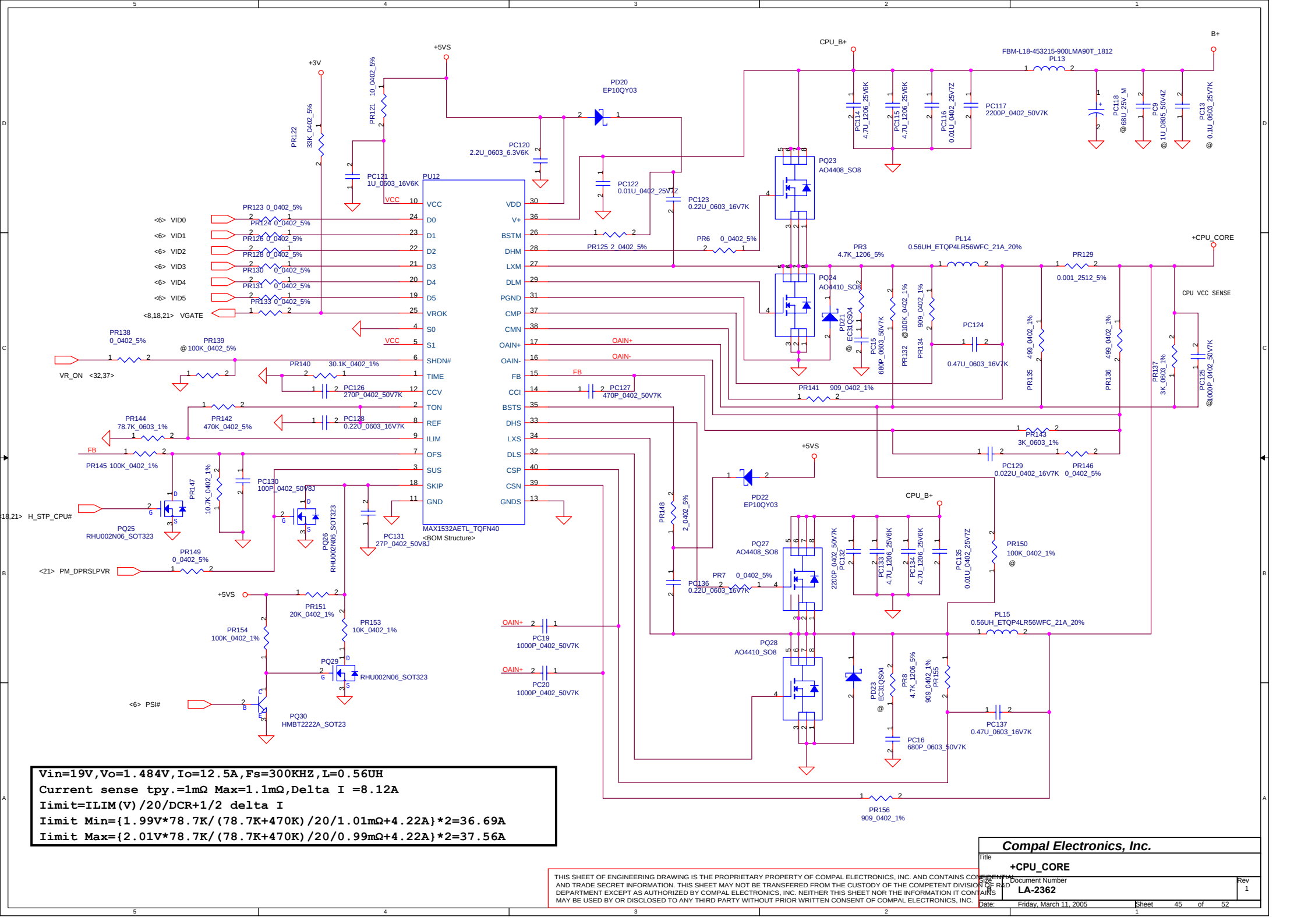
**Ipeak=Iocset*Rocset/RDS(ON)high side**
**Iocset=40uA, Pocset=4.12K RDS(on)=25.5mΩ**
**Ipeak min=40uA*4.12/(25.5*1.3)=4.97A**
**Ipeak max=40uA*4.12/25.5=6.46A**






**Compal Electronics, Inc.**

| | | |
|---|---|---|
| Title | RTC Battery & OTP & +1.5VP | |
| Size: B | Document Number: LA-2362 | Rev: 1 |
| Date: Friday, March 11, 2005 | Sheet 44 of 52 | |



## *Version change list (P.I.R. List)*



| Item | Fixed Issue | Reason for change | Rev. | PG# | Modify List | B.Ver# | Phase |
|---|---|---|---|---|---|---|---|
| 1 | | | | | ICH_PME# pull up +3VALW add R 10K | 0.2 | DVT |
| 2 | | | | | LID_SW# pull up +3VALW add R 10K | 0.2 | DVT |
| 3 | | | | | SB +1.5V regulator footprint error | 0.2 | DVT |
| 4 | | | | | SB +1.5V regulator footprint error U8 need to reverse | 0.2 | DVT |
| 5 | | | | | R76 take off | 0.2 | DVT |
| 6 | | | | | PR191 power plane 2.5vref change to +2.5V | 0.2 | DVT |
| 7 | | | | | R398 remove to R401 | 0.2 | DVT |
| 8 | | | | | H_DPRSLP# add pull up to +vccp power plane POP R546 | 0.2 | DVT |
| 9 | | | | | POP U9 for lose and foot print error | 0.2 | DVT |
| 10 | | | | | U3 pin6 & pin 7 need to swap | 0.2 | DVT |
| 11 | | | | | Add R476/7 40.2 Ohm for memory | 0.2 | DVT |
| 12 | | | | | R259 short | 0.2 | DVT |
| 13 | | | | | PR122 chang power plane to +3V for EC voltage leakage | 0.2 | DVT |
| 14 | | | | | Add R224/R290/R407 470ohm and Q34/9/11 2N7002 | 0.1 | DVT-2 |
| 15 | | | | | ADD R 39K//220p to GND at R518 for modify SIRQ | 0.1 | DVT-2 |
| 16 | | | | | Reverse the JHP1 & JMIC1 Symble error | 0.1 | DVT-2 |
| 17 | | | | | Modify NB FSB speed select for Dothan | 0.1 | DVT-2 |
| 18 | | | | | Modify ACIN for SB | 0.1 | DVT-2 |
| 19 | | | | | CardReader pin swap for flash memory | 0.1 | DVT-2 |
| 20 | | | | | Reverse the JHP1 & JMIC1 Symbl | 0.1 | DVT-2 |
| 21 | | | | | Add VCCP noise cap. at CPU C664/5/6/7/8/9 C670/1/2 | 0.2 | DVT-3 |
| 22 | | | | | Change R362/3 2.2K to 10K for Panel select | 0.2 | DVT-3 |

## *Version change list (P.I.R. List)*



| Item | Fixed Issue | Reason for change | Rev. | PG# | Modify List | B.Ver# | Phase |
|---|---|---|---|---|---|---|---|
| 23 | | | | | Add C674/5/6/7/8 C680/1/2/3/4/5 C686/7/8/9 C690/1/2/3/4/5/6/7/8/9 C702/3 for NB VCCP noise cap. | 0.2 | DVT-3 |
| 24 | | | | | ADD C646/7/8/9 C650/1/2/3/4/5 for DDR RAM 1.25V noise cap | 0.2 | DVT-3 |
| 25 | | | | | ADD C704/5 for JVGAP1 2.5V for noise | 0.2 | DVT-3 |
| 26 | | | | | Change R17/8/9 from 75 to 150 OHM for TV-out signal | 0.2 | DVT-3 |
| 27 | | | | | ADD R774/5 for cost down U29 parts | 0.2 | DVT-3 |
| 28 | | | | | Change SB(U5) sus power from V plane to Always power plane and R457 R69 R456 R455 R456 R451 U7.T2 +1.5VR | 0.2 | DVT-3 |
| 29 | | | | | R154 remove for FIR function | 0.2 | DVT-3 |
| 30 | | | | | ADD C656/7 C659/8 for +5VS HDD CDROM power noise | 0.2 | DVT-3 |
| 31 | | | | | U9 replace the new package to RM8 and remove to TOP | 0.2 | DVT-3 |
| 32 | | | | | ADD C706/7/8/9/10/11 for SB 1.5Vrun noise | 0.2 | DVT-3 |
| 33 | | | | | R129 change to +5VALW | 0.2 | DVT-3 |
| 34 | | | | | Q3 cahnge to AO3400 for current rating not enough | 0.2 | DVT-3 |
| 35 | | | | | JMPCI1 P.24 change to +3V for wireless power | 0.2 | DVT-3 |
| 36 | | | | | Remove KB910 & 39VF080 ROM | 0.2 | DVT-3 |
| 37 | | | | | R705 change to 13K for MB ID | 0.2 | DVT-3 |
| 38 | | | | | Change the Killer switch circuit for EC detect method then light on the LED | 0.2 | DVT-3 |
| 39 | | | | | Move U32 to near NB | 0.2 | DVT-3 |
| 40 | | | | | ADD 5VALW noise cap. C714/5/2/3, | 0.2 | DVT-3 |
| 41 | | | | | | | |
| 42 | | | | | | | |
| 43 | | | | | | | |
| 44 | | | | | | | |

# Version change list (P.I.R. List)



| Item | Fixed Issue | Reason for change | Rev. | PG# | Modify List | B.Ver# | Phase |
|---|---|---|---|---|---|---|---|
| 1 | Delete the charge circuit. | Delete the charge circuit. | 0.2 | 38 | 1.Delete the PU5 IC LM393M (SM).<br>2.Delete PD1 S DIO 1N4148 (SM).<br>3.Delete PR10,PR11,PR12,PR13 S RES 1/4W 1.5K +-5% 1206. | 0.2 | DVT |
| 2 | Change the CPU OTP circuit from active H to active L. | Change the CPU OTP circuit from active H to active L. | 0.2 | 43 | 1.Delete PQ14 S TR DTC115EUA NPN (UMT3).<br>2..Delete PD8 S DIO 1SS355.<br>3.Change PR75 and PR76 from S RES 1/16W 100K +-1% 0402 to S RES 1/16W 150K +-1% 0402.<br>4.Change PR73 from S RES 1/16W 15K +-1% 0402 to S RES 1/16W 16.9K +-1% 0402.<br>5.Change PC56 from S CER CAP .22U 16V K X7R 0603 to S CER CAP 1U 16V K X7R 0805<br>6.Change PR74 from S RES 1/16W 3.4K +-1% 0402 to S S RES 1/16W 2.15K +-1% 0402. | 0.2 | DVT |
| 3 | For cost down solution. | To cost down for +1.5VP. | 0.2 | 43 | 1.Change the PD12 from DIO 1N4148 (SM) to DIO 1SS355. | 0.2 | DVT |
| 4 | For cost down solution. | To cost down for RTC charge circuit.. | 0.2 | 43 | 1.Delete the PD33 S ZEN DIO RLZ4.3B (LL-34). | 0.2 | DVT |
| 5 | To prevent the KB-910 damag. | To prevent the KB-910 damag. | 0.2 | 40 | 1.Change the PD17 from SCH DIO SKS10-04AT TSMA to SCH DIO SKUL30-02AT THIN SMA. | 0.2 | DVT |
| 6 | For cost down solution. | To cost down for +1.5VP for +12VALWP circuit. | 0.2 | 40 | 1.Delete PR187 S RES 1/8W 2.7K +-5% 1206 S7. | 0.2 | DVT |
| 7 | For cost down solution. | To cost down for DDR 2.5V. | 0.2 | 41 | 1.Delete PR62 S RES 1/16W 0 +-5% 0402. | 0.2 | DVT |
| 8 | For cost down solution. | To cost down for CPU_CORE. | 0.2 | 44 | 1.Delete PR127 and PR152 S RES 1/16W 0 +-5% 0402. | 0.2 | DVT |
| 9 | For cost down solution. | To cost down for snubber circuit. | 0.2 | 40 | 1.Deete PR127 and PR152 S RES 1/16W 0 +-5% 0402.<br>2.Delete the PC161 S CER CAP 470P 100V K X7R 0805. | 0.2 | DVT |
| 10 | For cost down solution. | To cost down for EMI capacitor. | 0.2 | 39<br>40<br>41 | 1.Delete PC41,PC158 and PC159 S CER CAP .1U 25V K X7R 0603.<br>2.Delete PC40,PC73 and PC76 CER CAP 2200P 50V K X7R 0402. | 0.2 | DVT |
| 10 | Don't has pull high resister on VGATE pin. | Add pull high resister on VGATE pin. | 0.2 | 44 | 1.Add the S RES 1/16W 100K +-5% 0402. | 0.2 | DVT |
| 10 | VCCPP output voltage has error. | Adjustment resistor divider. | 0.2 | 41 | 1.Change the PR60 from S RES 1/16W 681 +-1% 0402 to S RES 1/16W 1.69K +-1% 0603. | 0.2 | DVT |
| 11. | Choke Rating not enough for +1.5VP. | Choke Rating not enough for +1.5VP. | 0.2 | 43 | 1.Change PL7 from 4.7UH_FDV0630-4.7UH_5.5A_20% to 4.7UH_D104C-919AS_4R7N_5.2A_20%. | 0.2 | DVT |

# Version change list (P.I.R. List)



| Item | Fixed Issue | Reason for change | Rev. | PG# | Modify List | B.Ver# | Phase |
|---|---|---|---|---|---|---|---|
| 1 | Don't has pull down resister on SHDN# pin for charger. | Add pull down resister on SHDN# pin. | 0.2 | 39 | 1.Add PR193 the S RES 1/16W 100K +-5% 0402. | 0.2 | DVT |
| 2 | Change the Vin Detector from LM393 to charger ACOK#. | Change the Vin Detector from LM393 to charger ACOK#. | 0.2 | 38,39 | 1.Add the PQ40 S TR DTC115EUA NPN (UMT3).<br>2.Delete the PR3,PR4,PR8 and PR9 RES 1/16W 10K +-1% 0402.<br>3.Add the PR193,PR172 and PR173 RES 1/16W 100K +-5% 0402.<br>4.Delete PR6 the S RES 1/16W 22K +-1% 0402.<br>5.Delete PR1 the S RES 1/16W 1M +-1% 0402.<br>6.Change PR182 from S RES 1/16W 150K +-1% 0402 to S S RES 1/16W 20K +-1% 0402.<br>7.Delete the PR7 S RES 1/16W 20K +-1% 0402.<br>8.Delete the PR2 S RES 1/16W 84.5K +-1% 0402.<br>9.Add the PR175 S RES 1/16W 158K +-1% 0402.<br>10.Add the PR175 S RES 1/16W 681K +-1% 0402.<br>11.Delete PC6 from S CER CAP .1U 25V K X7R 0603.<br>12..Delete PC5 from S CER CAP 1000P 50V +-10% X7R 0402. | 0.2 | DVT |
| 3 | For ACIN pin, | ACIN pin don't have connect to system. | 0.2 | 39 | 1.Add PR4 the 10K +-5% 0402 | 0.2 | DVT |
| 4 | +1.8VSP power rating not enough. | +1.8VSP power rating isnot enough. | 0.2 | 42 | 1.Change PU10 from S IC G965-18P1U SOP-8L REG to S IC APW7057KC-TR SOP-8 PWM.<br>2.Add PR197 S RES 1/16W 12.7K +-1% 0402.<br>3.Add the PQ44 S TR RHU002N06 1N SOT323<br>4.Delete PQ43 the S TR AO4912 2N SO8 W/D<br>5.Add PD33 the S DIO 1SS355.<br>6.Add PR195 the S RES 1/16W 2.2 +-5% 0402<br>7.Add PR198 the S RES 1/16W 10K +-1% 0402.<br>8.Add PR196 the S RES 1/16W 4.12K +-1% 0402<br>9.Add the PC167 the S CER CAP 4.7U 10V Z Y5V 0805.<br>10.Add the PC164 S CER CAP 470P 50V +-10% X7R 0402.<br>11.Add the PC163,PC165 and PC168 S CER CAP .1U 16V +-10% X7R 0402<br>12.Delete PC96 the S CER CAP 10U 6.3V K X7R 1206.<br>13.Add the PC166 S POLY CAP 150U 6.3V M V(D2) T520 LESR.<br>14.Add PL18 the S COIL 5.0UH +-20% TPRH6D38-5R0M-N 2.9A. | 0.2 | DVT |
| 5 | VCCP's transients cannot meet spec. | VCCP's transients cannot meet spec. | 0.2 | 41 | 1.Change PC50 from S POLY CAP 150U 6.3V M V(D2) T520 LESR to S POLY C 220U 4V M V(D2) T520 LESR.<br>2.Change PL6 from S COIL 4.7UH +-20% D104C-919AS-4R7M 5.2A to S COIL 1.8UH +-30% D104C-919AS-1R8N 9.5A. | 0.2 | DVT |
| 6 | For CPU_CORE's EMI, | For CPU_CORE's EMI, | 0.2 | 44 | 1.Change the PR125 and PR148 from S RES 1/16W 0 +-5% 0402S to RES 1/16W 2 +-5% 0402. | 0.2 | DVT |

# Version change list (P.I.R. List)



| Item | Fixed Issue | Reason for change | Rev. | PG# | Modify List | B.Ver# | Phase |
|---|---|---|---|---|---|---|---|
| 1. | CPU's transients cannot meet spec. | Add one current sense on phase 2. | 0.2 | 44 | 1.Delete PC124 and PC137 the S CER CAP 0.47U 16V +-10% X7R 0603.<br>2.Delete PR134,PR141,PR155 and PR156 the S RES 1/16W 909+-1% 0402.<br>3.Add PR134 S RES 1W 0.01 +-1%2512. | 0.2 | DVT |
| 2. | PACIN pin's high level is only 2.3V. | To adjust PACIN pin's level. | 0.2 | 39 | 1.Delete PR175 the S RES 1/16W 158K+-1% 0402.<br>2.Change the PR172 from S RES 1/16W 100K +-1% 0402 S to RES 1/16W 10K +-1% 0402. | 0.2 | DVT |
| 3. | The 5VALWP rising time is faster than PACIN's. | To delay timer of 5VALWP. | 0.3 | 40 | 1.Change the PR105 from S RES 1/16W 47K +-1% 0402 S to RES 1/16W 100K +-1% 0402.<br>2.Change the PC91 from S CER CAP .047U 25V M X7R 0603 to CAP 1U 25V Z F Y5V 0805.. | 0.3 | DVT2 |
| 4. | The charge has error on change mode. | To adjust input and output current regulation loop compensation. | 0.3 | 39 | 1.Change PC152 and PC153 from the S CER CAP 0.01U 16V +-10% X7R to CER CAP 0.001U 16V +-10% X7R. | 0.3 | DVT2 |
| 5. | For cost down solution. | For cost down solution. | 0.3 | 42<br>43 | 1.Change PC58,PC68,PC95 and PC99 from the S CER CAP 4.7U 25V K X5R 1206 to CAP 4.7U 10V K X7R 0805. | 0.3 | DVT2 |
| 6. | The charger has EMI issue. | Add a resistor on charger's boost for EMI. | 0.3 | 39 | 1.Add the PR1 S RES 1/16W 0 +-5% 0402. | 0.3 | DVT2 |
| 7. | Change the current limit's from sense DRC to resister. | To adjust current limit point for CPU_CORE. | 0.3 | 44 | 1.Change the PR142 from S RES 1/16W 200K +-5% 0402 to S RES 1/16W 470K +-5% 0402. | 0.3 | DVT2 |
| 8. | To preven in-rush current for B+ of MAX1902. | To preven in-rush current for B+ of MAX1902. | 0.3 | 40 | 1.Add PR2 S RES 1/8W 33 +-5% 1206. | 0.3 | DVT2 |
| 9. | The CPU's dual choke will shortage. | Change to single choke. | 0.3 | 44 | 1.Add PQ26 SB502060000 S TR RHU002N06 1N SOT323.<br>2.Add PR134,PR141,PR155,PR156 S RES 1/16W 909 +-1% 0402.<br>3.Delete PL14 S COIL .5UH +-30% CXZT1050-R50 28A.<br>4.Add the PL14,PL15 S COIL .56UH +-20% ETQP4LR56 WFC 21A.<br>5.Add the PC124,PC137 0.47U 16V +-10% X7R 0603 S8.<br>4.Add the PL14,PL15 S COIL .56UH +-20% ETQP4LR56 WFC 21A. | 0.3 | DVT2 |
| 10. | Delete the +1.8VSP on M/B. | Delete the +1.8VSP on M/B. | 0.3 | 42 | 1.Delete the PU10 S IC APW7057KC-TR SOP-8 PWM.<br>2.Delete the PQ43 S TR AO4912 2N SO8 W/D.<br>3.Delete the PR188 S RES 1/16W 0 +-5% 0402.<br>4.Delete the PR195 S RES 1/16W 2.2 +-5% 0402<br>5.Delete the PR196 S RES 1/16W 4.12K +-1% 0402<br>6.Delete the PR198 S RES 1/16W 10K +-1% 0402<br>7.Delete the PR197 S RES 1/16W 12.7K +-1% 0402.<br>8.Delete the PL18 S COIL 5.0UH +-20% TPRH6D38-5R0M-N 2.9A.<br>9.Delete the PC166 S POLY CAP 150U 6.3V M V(D2) T520 LESR.<br>10.Change the PC75 and PC87 from S CER CAP 4.7U 10V Z Y5V 0805 to S CER CAP 4.7U 6.3V +-10% X5R 0805<br>11.Delete PC95 S CER CAP 4.7U 10V Z Y5V 0805.<br>12.Delete PC163,PC165,PC168 .1U 16V +-10% X7R 0402.<br>13.Delete PC164 S CER CAP 470P 50V +-10% X7R 0402.<br>14.Delete PD33 S DIO 1SS355. | 0.3 | DVT2 |

# Version change list (P.I.R. List)



| Item | Fixed Issue | Reason for change | Rev. | PG# | Modify List | B.Ver# | Phase |
|---|---|---|---|---|---|---|---|
| 1. | Max1902 protect When power cord fast plug-out and plug-in. | Add the pre-chagre circuit. | 0.3 | 38 | 1.Add PQ1 SB502060000 S TR RHU002N06 1N SOT323.<br>2.Add PQ2 S TR DTC115EUA NPN (UMT3).<br>3.Add PD2 S SCH DIO RB715F UMD3.<br>4.Add PD1 S DIO 1N4148 (SM)<br>5.Add PR10,PR11,PR12 and PR13 S RES 1/4W 1.5K +-5% 1206.<br>6.Add PR16 S RES 1/16W 100K +-1% 0402.<br>7.Add PR17 and PR20 S RES 1/16W 499K +-1% 0402.<br>8.Add PR19 S RES 1/16W 191K +-1% 0402.<br>9.Add PR23 S RES 1/16W 34K +-1% 0402.<br>10.Add PR26 S RES 1/16W 66.5K +-1% 0402.<br>11.Add PR14 S RES 1/16W 2.2M +-5% 0402.<br>12.Add PR24 S RES 1/16W 47K +-5% 0402.<br>13.Add PC10 and PC12 S CER CAP 1000P 50V +-10% X7R 0402.<br>14.Add PC11 S CER CAP .1U 25V K X7R 0603. | 0.3 | DVT2 |
| 2. | The 5VALWP choke rating is not enough. | Change the choke. | 0.3 | 40 | 1.Change the PL9 from S COIL 10UH +-30% SDT-1050P-100-118 3.5A to S COIL 10uH +-20% SDT-1205P-100-118. | 0.3 | DVT2 |
| 3. | TP0610T will EOL. | Change the part. | 0.3 | 43 | 1.Change the PQ16 S TR TP0610T 1P SOT-23 to.S TR TP0610K 1P SOT-23 | 0.3 | DVT2 |

# Version change list (P.I.R. List)



| Item | Fixed Issue | Reason for change | Rev. | PG# | Modify List | B.Ver# | Phase |
|---|---|---|---|---|---|---|---|
| 1. | To adjust sequence for +5VALWP and +3VALWP. | To adjust sequence for +5VALWP and +3VALWP. | LA-2362-0.2 | 41 | 1.Change PC90 from .47U 16V X7R 0603 to 2.2U 10V X5R 0805. | LA-2362-0.2 | DVT3 |
| 2. | Change the pull-high resistor for VGTE pin. | For HW request. | LA-2362-0.2 | 45 | 1.Change PR122 from 100K 0402 to 10K 0402. | LA-2362-0.2 | DVT3 |
| 3. | The system has re-boot issue when running the 3D mark. | The HW has noise by interference from B+. | LA-2362-0.2 | 42 | 1.Add the PL3 FBL-18-453215-900LM90T_1812.<br>2.Add the PC35 and PC41 0.1U 25V X7R 0603, | LA-2362-0.2 | DVT3 |
| 4. | The CPU's B+ has nosie issue when system into C3/C4. | The CPU's B+ has nosie issue when system into C3/C4. | LA-2362-0.2 | 45 | 1.Add the PC14  220U 25V. | LA-2362-0.2 | DVT3 |
| 5. | To cost down for 150uf/6.3V. | To cost down for 150uf/6.3V. | LA-2362-0.2 | 41,45 | 1.Change the vendor form KEMET to EPCOS. | LA-2362-0.2 | DVT3 |
| 6. | Change the IC solution from ISL6227 to MAX8743 for +2.5V and +VCCPP. | The ISL6227 has shut down issue when windows idle. | LA-2362-0.2 | 42 | | LA-2362-0.2 | DVT3 |