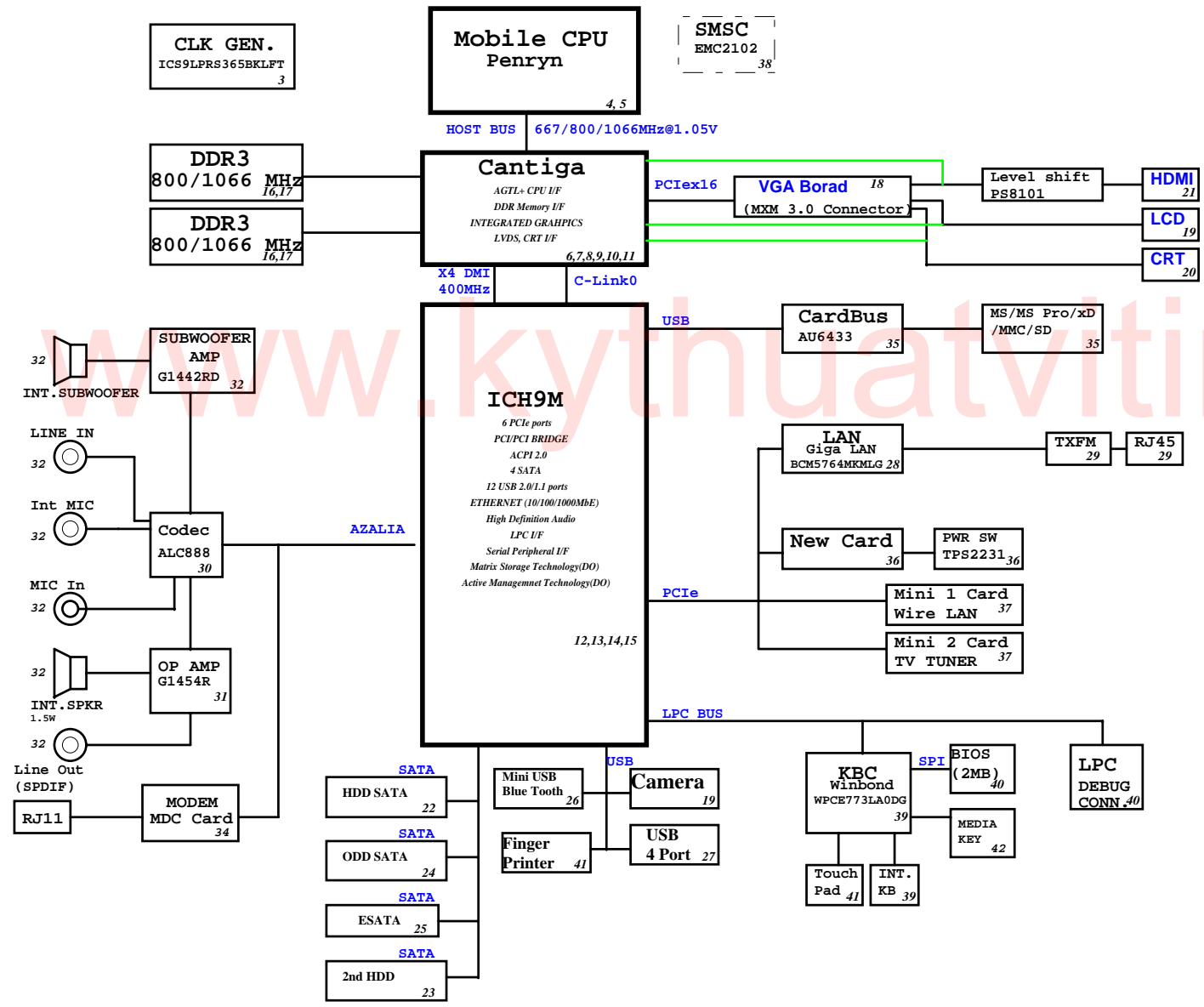
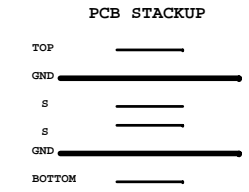


JM70 -MV Block Diagram



SYSTEM DC/DC ISL62392 46	
INPUTS	OUTPUTS
DCBATOUT	5V_S5(6A) 3D3V_S5(7A) 5V_AUX_S5 3D3V_AUX_S5
SYSTEM DC/DC TPS51124 46	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0(10A) 1D5V_S3(10A)
RT9026 49	
1.5V_S3	DDR_VREF_S3 (1.2A)
G9198-15 14	
3D3V_S5	1D5V_S5 (300mA)
CHARGER ISL88731A 50	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 1.8V 6.0A
CPU DC/DC ADP3208C 51	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0-1.3V 38A
GFX DC/DC ISL6263 48	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE 0-1.3V 6.5A



ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5 page 92

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIe Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIe config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/GPIO53	PCIe config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#/GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resistor.

ICH9M Integrated Pull-up and Pull-down Resistors

ICH9 EDS 642879 Rev.1.5

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSPLVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 0.5 page 218

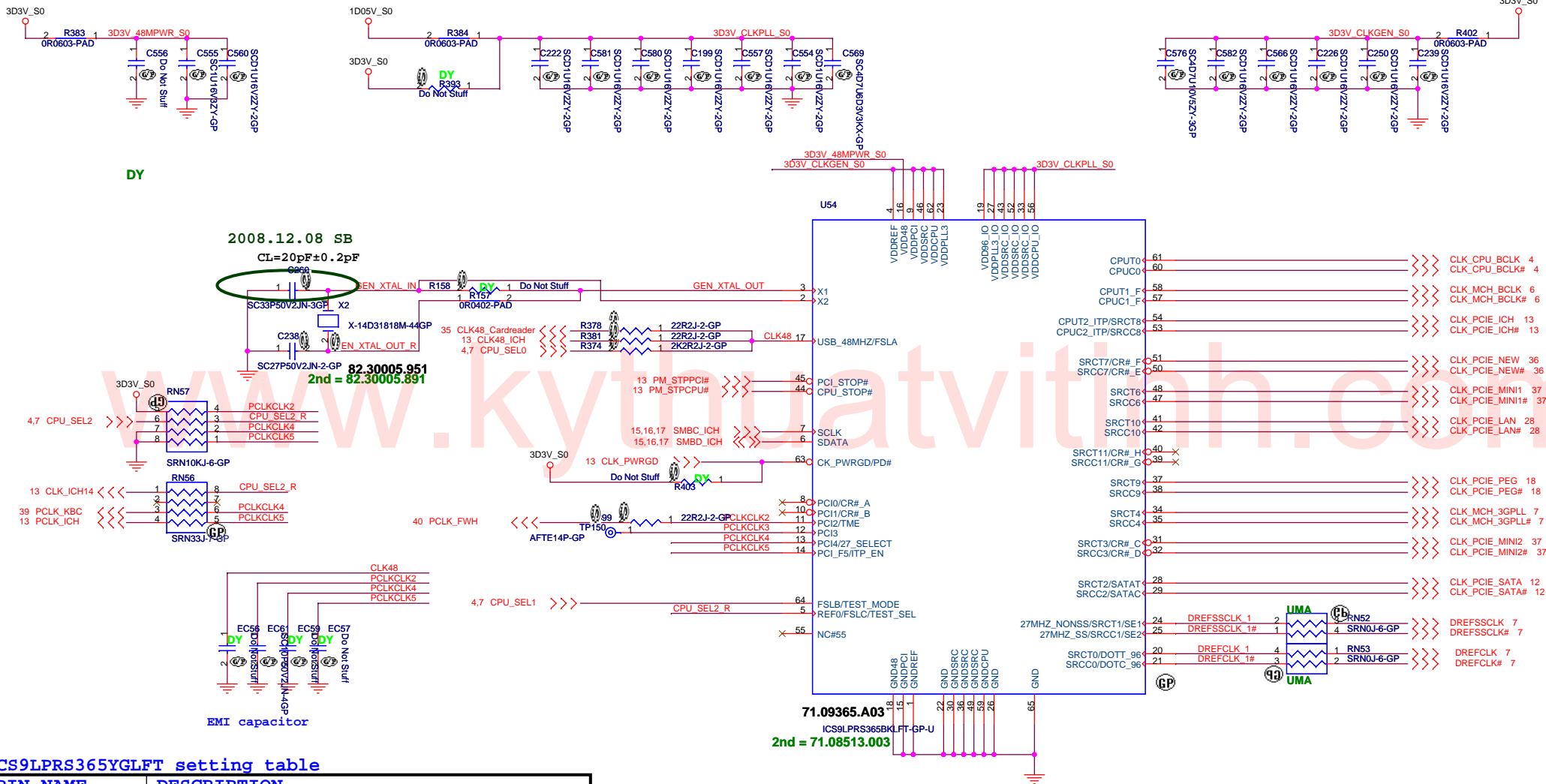
Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) 1=The iTPM Host Interface is disabled(default)
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality 1 = TLS cipher suite with confidentiality (default)
CFG9	PCIe Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. 1= Normal operation(Default):Lane Numbered in order
CFG10	PCIe Loopback enable	0 = Enable (Note 3) 1= Disabled (default)
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) 11 = Disabled (default)
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG19	DMI Lane Reversal	0 = Normal operation(Default): Lane Numbered in Order 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3 DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/IHDMI) Concurrent with PCIe	0 = Only Digital Display Port or PCIe is operational (Default) 1 = Digital display Port and PCIe are operating simultaneously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 =No SDVO Card Present (Default) 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (Default) 1= LFP Card Present; PCIe disabled

NOTE:

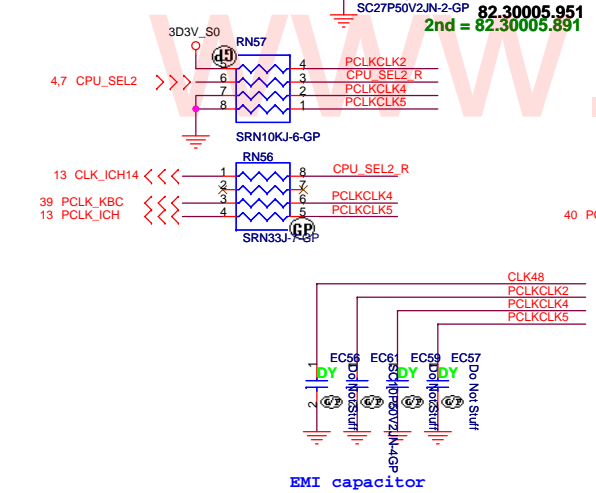
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6. Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

UMA

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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Reference			
Title	Document Number		Rev
	JM70-MV		SB
Size A3	Date: Saturday, December 20, 2008		Sheet 2 of 55



2008.12.08 SB
 CL=20pF±0.2pF
 SC33P50V2JN-3GP X2
 X-14D31818M-44GP
 SC27P50V2JN-2GP
 82.30005.951
 2nd = 82.30005.891



ICS9LPRS365YGLFT setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1 = CR#A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1 = CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1 = CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1 = CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3	
PCI4/27M_SEL	0 = Pin17 as SRC-1, Pin18 as SRC-1#, Pin13 as DOT96, Pin14 as DOT96# 1 = Pin17 as 27MHz, Pin 18 as 27MHz_SS, Pin13 as SRC-0, Pin14 as SRC-0#
PCI_F5/ITP_EN	0 = SRC8/SRC8# 1 = ITP/ITP#
SRCT3/CR#_C	Byte 5, bit 3 0 = SRC3 enabled (default) 1 = CR#_C enabled. Byte 5, bit 2 controls whether CR#_C controls SRC0 or SRC2 pair Byte 5, bit 2 0 = CR#_C controls SRC0 pair (default), 1 = CR#_C controls SRC2 pair

PIN NAME	DESCRIPTION
SRCC3/CR#_D	Byte 5, bit 1 0 = SRC3 enabled (default) 1 = CR#_D enabled. Byte 5, bit 0 controls whether CR#_D controls SRC1 or SRC4 pair Byte 5, bit 0 0 = CR#_D controls SRC1 pair (default) 1 = CR#_D controls SRC4 pair
SRCC7/CR#_E	Byte 6, bit 7 0 = SRC7 enabled (default) 1 = CR#_F controls SRC6
SRCT7/CR#_F	Byte 6, bit 6 0 = SRC7 enabled (default) 1 = CR#_F controls SRC8
SRCC11/CR#_G	Byte 6, bit 5 0 = SRC11# enabled (default) 1 = CR#_G controls SRC9
SRCT11/CR#_H	Byte 6, bit 4 0 = SRC11 enabled (default) 1 = CR#_H controls SRC10

SEL2	SEL1	SEL0	CPU	FSB
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1067M

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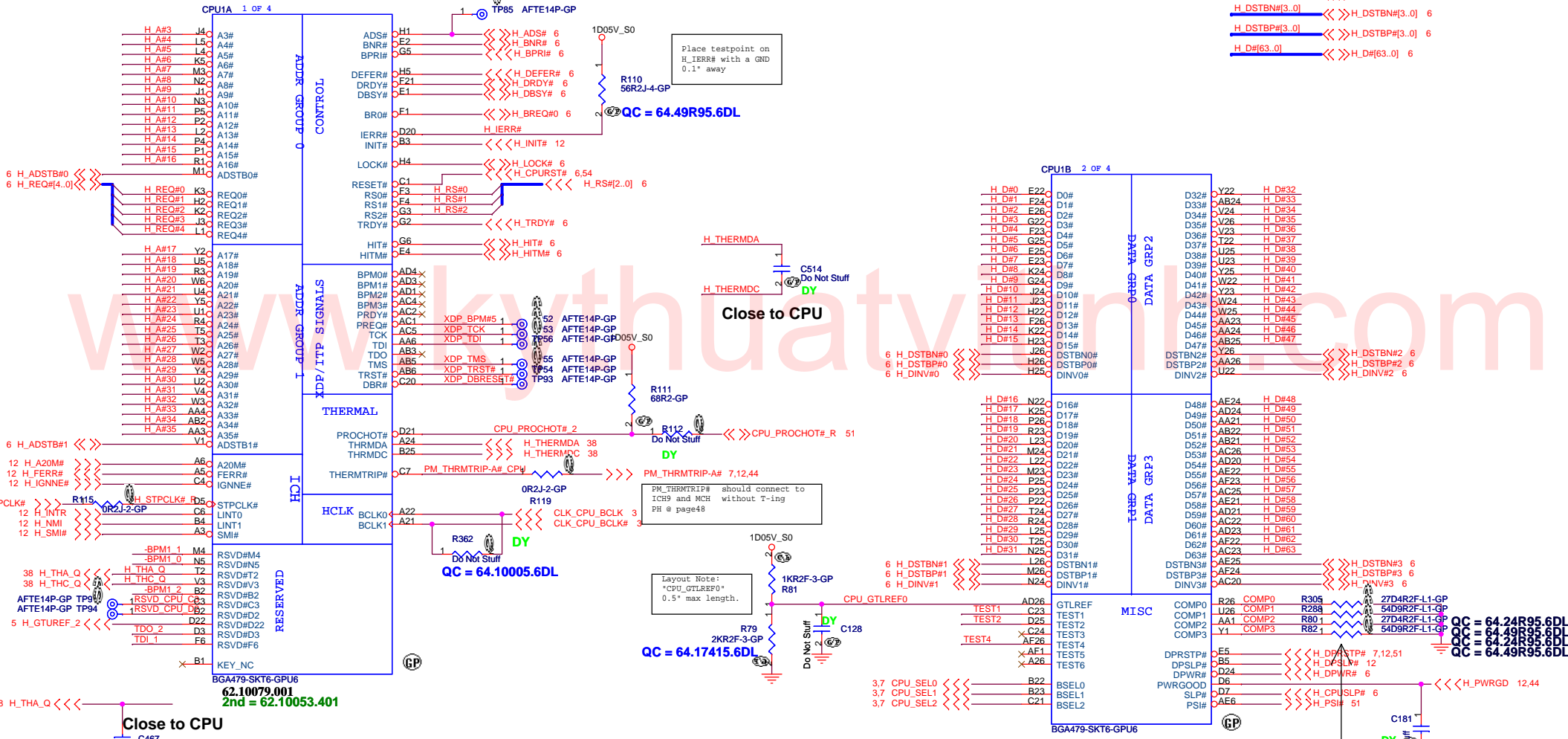
Title: **Clock Generator**

Size: Document Number **JM70-MV** Rev **SB**

Date: Saturday, December 20, 2008 Sheet 3 of 55

6 H_A#(35..3) <<< H_A#(35..3)

H_DIN#(3..0) <<< H_DIN#(3..0) 6
H_DSTBN#(3..0) <<< H_DSTBN#(3..0) 6
H_DSTBP#(3..0) <<< H_DSTBP#(3..0) 6
H_D#(63..0) <<< H_D#(63..0) 6



Place testpoint on H_IERR# with a GND 0.1" away

Close to CPU

PM_THRMTRIP# should connect to ICH9 and MCH without T-ing PH @ page48

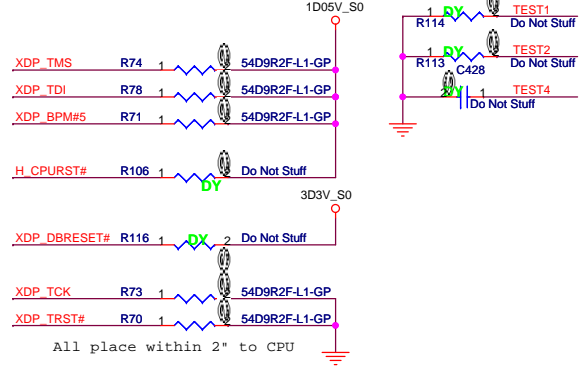
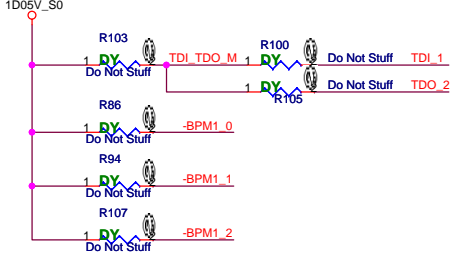
Layout Note: "CPU_GTLREF0" 0.5" max length.

Net "TEST4" as short as possible, make sure "TEST4" routing is reference to GND and away other noisy signals

Place these TP on button-side, easy to measure.

Layout Note: Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5". Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5".

XDP FOR QUAD CORE CPU

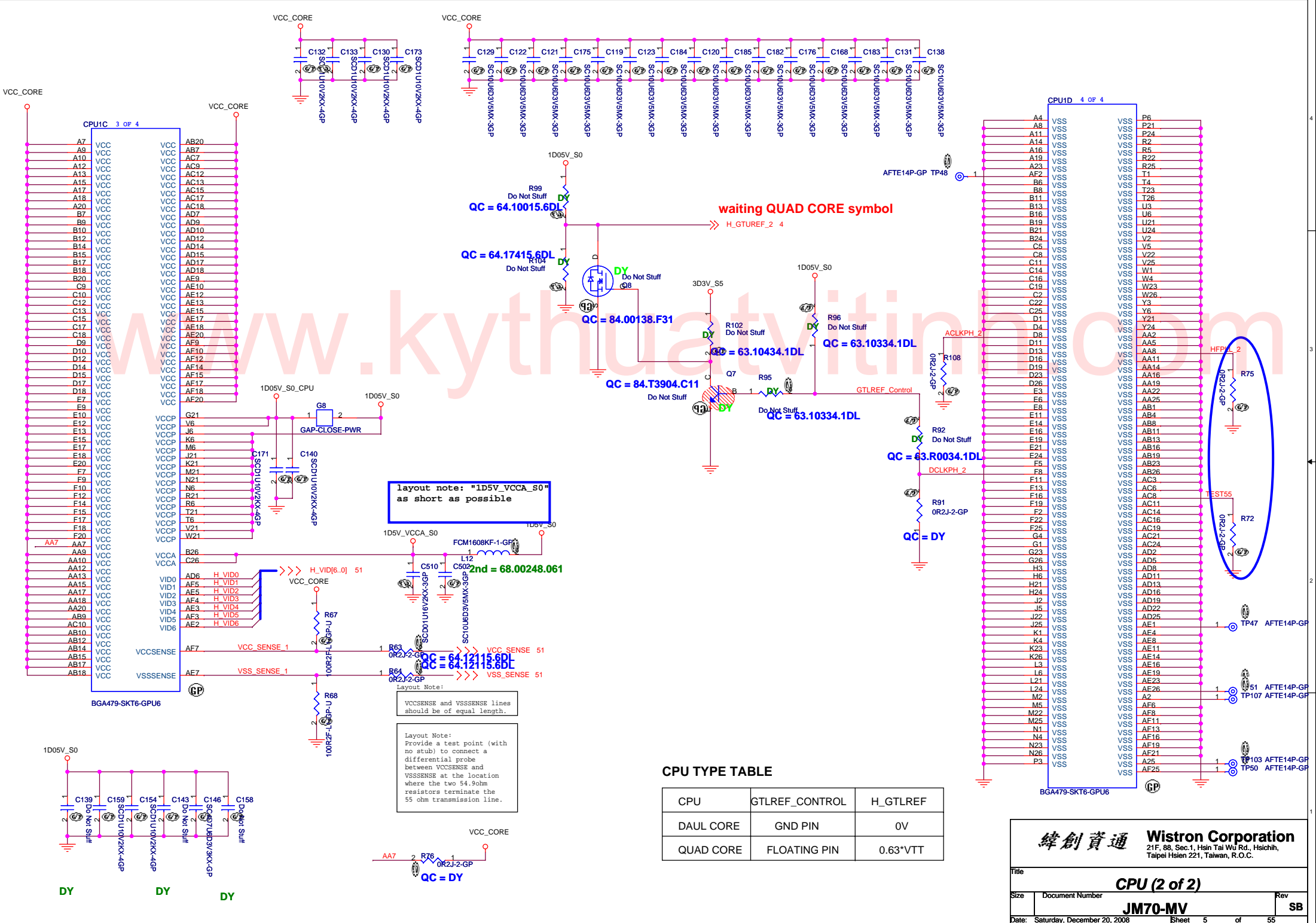


All place within 2" to CPU

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Title			CPU (1 of 2)
Size	Document Number	JM70-MV	
Date: Saturday, December 20, 2008	Sheet	4	of 55



CPU TYPE TABLE

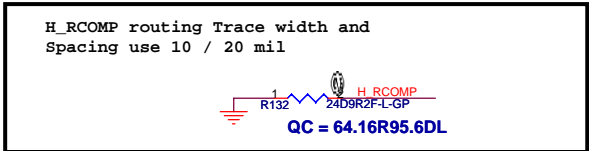
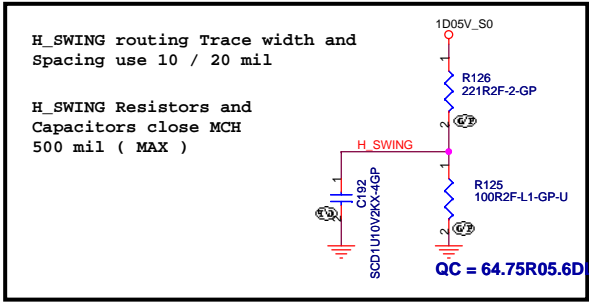
CPU	GTLREF_CONTROL	H_GTLREF
DAUL CORE	GND PIN	0V
QUAD CORE	FLOATING PIN	0.63*VTT

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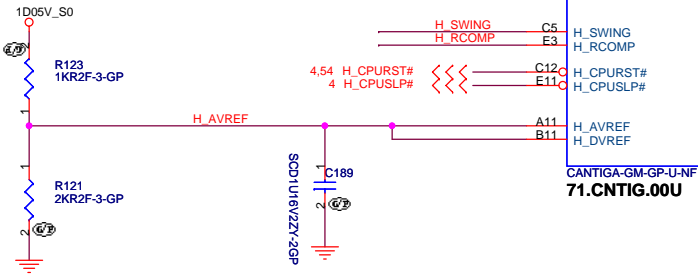
Title: **CPU (2 of 2)**

Size: Document Number: **JM70-MV** Rev: **SB**

Date: Saturday, December 20, 2008 Sheet 5 of 55



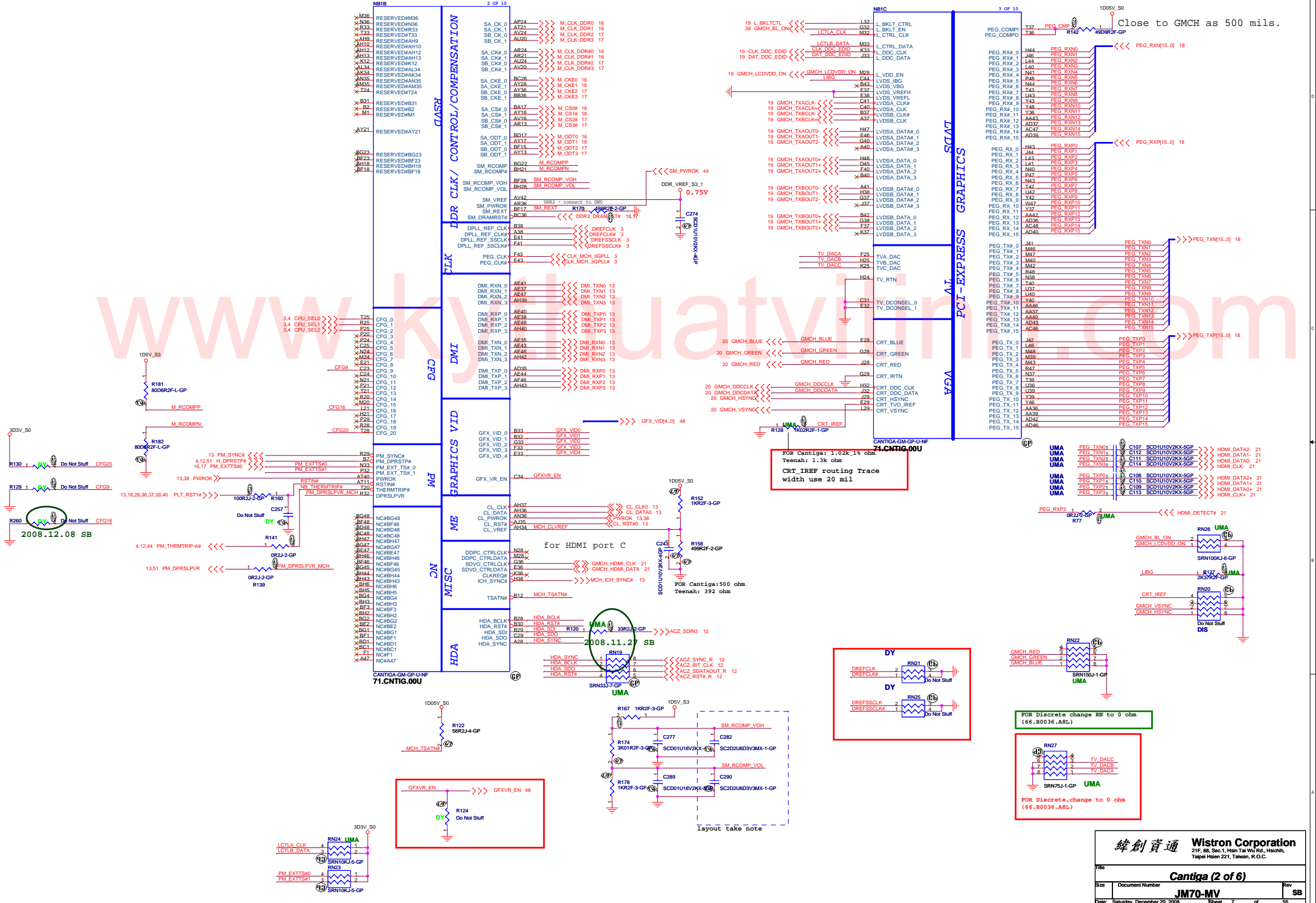
Place them near to the chip (< 0.5")



NB1A		1 OF 10	
H_D#0	F2	H_A#_3	A14
H_D#1	G8	H_A#_4	C15
H_D#2	F8	H_A#_5	H13
H_D#3	F6	H_A#_6	C18
H_D#4	G2	H_A#_7	M16
H_D#5	H6	H_A#_8	J13
H_D#6	F6	H_A#_9	P16
H_D#7	F2	H_A#_10	R16
H_D#8	D4	H_A#_11	N17
H_D#9	H3	H_A#_12	M13
H_D#10	M9	H_A#_13	E17
H_D#11	M11	H_A#_14	P17
H_D#12	J1	H_A#_15	E17
H_D#13	J2	H_A#_16	C20
H_D#14	N12	H_A#_17	B19
H_D#15	J6	H_A#_18	J16
H_D#16	P2	H_A#_19	E20
H_D#17	L2	H_A#_20	H16
H_D#18	R2	H_A#_21	J20
H_D#19	N9	H_A#_22	L17
H_D#20	L6	H_A#_23	A17
H_D#21	M5	H_A#_24	B17
H_D#22	I3	H_A#_25	L16
H_D#23	N2	H_A#_26	C21
H_D#24	R1	H_A#_27	J17
H_D#25	N5	H_A#_28	H20
H_D#26	N6	H_A#_29	B18
H_D#27	P13	H_A#_30	K17
H_D#28	N8	H_A#_31	B20
H_D#29	L7	H_A#_32	F21
H_D#30	N10	H_A#_33	K21
H_D#31	M3	H_A#_34	L20
H_D#32	I3	H_A#_35	H_A#35
H_D#33	AD14		
H_D#34	Y6	H_ADS#	H12
H_D#35	Y10	H_ADSTB#	B16
H_D#36	Y12	H_ADSTB#	G17
H_D#37	Y14	H_BNR#	A9
H_D#38	Y7	H_BNR#	E11
H_D#39	W2	H_BPRI#	G12
H_D#40	AA8	H_BREQ#	E3
H_D#41	Y9	H_DEFER#	B10
H_D#42	AA13	H_DBSY#	AH7
H_D#43	AA9	HPLL_CLK#	AH6
H_D#44	AA11	H_DPWR#	J11
H_D#45	AD11	H_DRDY#	E9
H_D#46	AD10	H_HIT#	H9
H_D#47	AD13	H_HITM#	E12
H_D#48	AE12	H_LOCK#	H11
H_D#49	AE9	H_TRDY#	C3
H_D#50	AA2		
H_D#51	AD8		
H_D#52	AD3		
H_D#53	AD3		
H_D#54	AD7		
H_D#55	AE14		
H_D#56	AF3		
H_D#57	AC1		
H_D#58	AE3		
H_D#59	AC3		
H_D#60	AE11		
H_D#61	AE8		
H_D#62	AG2		
H_D#63	AD6		

HOST

H_A#35.3	<<<>>>	H_A#35.3	4
H_A#3		H_A#4	
H_A#4		H_A#5	
H_A#5		H_A#6	
H_A#6		H_A#7	
H_A#7		H_A#8	
H_A#8		H_A#9	
H_A#9		H_A#10	
H_A#10		H_A#11	
H_A#11		H_A#12	
H_A#12		H_A#13	
H_A#13		H_A#14	
H_A#14		H_A#15	
H_A#15		H_A#16	
H_A#16		H_A#17	
H_A#17		H_A#18	
H_A#18		H_A#19	
H_A#19		H_A#20	
H_A#20		H_A#21	
H_A#21		H_A#22	
H_A#22		H_A#23	
H_A#23		H_A#24	
H_A#24		H_A#25	
H_A#25		H_A#26	
H_A#26		H_A#27	
H_A#27		H_A#28	
H_A#28		H_A#29	
H_A#29		H_A#30	
H_A#30		H_A#31	
H_A#31		H_A#32	
H_A#32		H_A#33	
H_A#33		H_A#34	
H_A#34		H_A#35	
H_A#35			
H_ADS#		H_ADS#	4
H_ADSTB#_0		H_ADSTB#0	4
H_ADSTB#_1		H_ADSTB#1	4
H_BNR#		H_BNR#	4
H_BPRI#		H_BPRI#	4
H_BREQ#		H_BREQ#	4
H_DEFER#		H_DEFER#	4
H_DBSY#		H_DBSY#	4
HPLL_CLK#		GLK_MCH_BCLK#	3
HPLL_CLK#		GLK_MCH_BCLK#	3
H_DPWR#		H_DPWR#	4
H_DRDY#		H_DRDY#	4
H_HIT#		H_HIT#	4
H_HITM#		H_HITM#	4
H_LOCK#		H_LOCK#	4
H_TRDY#		H_TRDY#	4
H_DINV#_0		H_DINV#3.0	4
H_DINV#_1		H_DINV#3.0	4
H_DINV#_2		H_DINV#3.0	4
H_DINV#_3		H_DINV#3.0	4
H_DSTBN#_0		H_DSTBN#3.0	4
H_DSTBN#_1		H_DSTBN#3.0	4
H_DSTBN#_2		H_DSTBN#3.0	4
H_DSTBN#_3		H_DSTBN#3.0	4
H_DSTBP#_0		H_DSTBP#3.0	4
H_DSTBP#_1		H_DSTBP#3.0	4
H_DSTBP#_2		H_DSTBP#3.0	4
H_DSTBP#_3		H_DSTBP#3.0	4
H_REQ#_0		H_REQ#0	4
H_REQ#_1		H_REQ#1	4
H_REQ#_2		H_REQ#2	4
H_REQ#_3		H_REQ#3	4
H_REQ#_4		H_REQ#4	4
H_RS#_0		H_RS#0	2
H_RS#_1		H_RS#1	2
H_RS#_2		H_RS#2	2



Close to GMCH as 500 mils.

FOR Cantiga: 1.02k_1 ohm
Teenah: 1.3k ohm
CRT IRREF routing Trace
width use 20 mil

71.CNTIG.00U

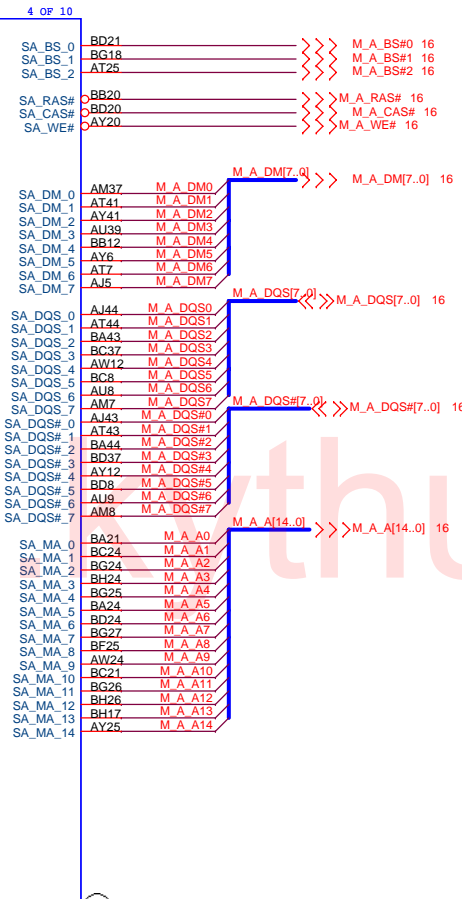
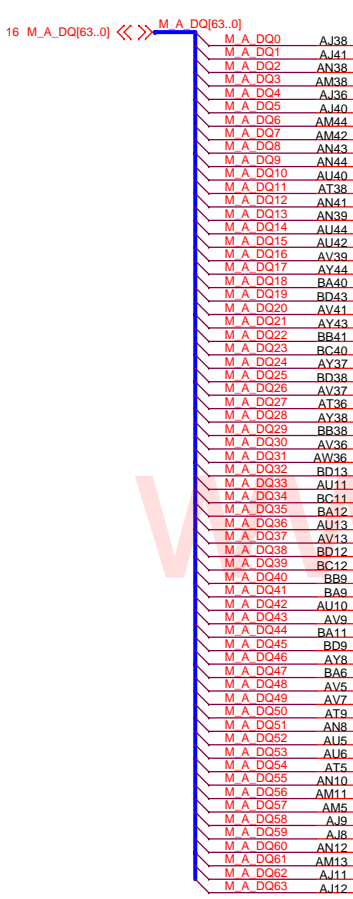
FOR Discrete change RN to 0 ohm
(66.R0036.AB1)

FOR Discrete, change to 0 ohm
(66.R0036.AB1)

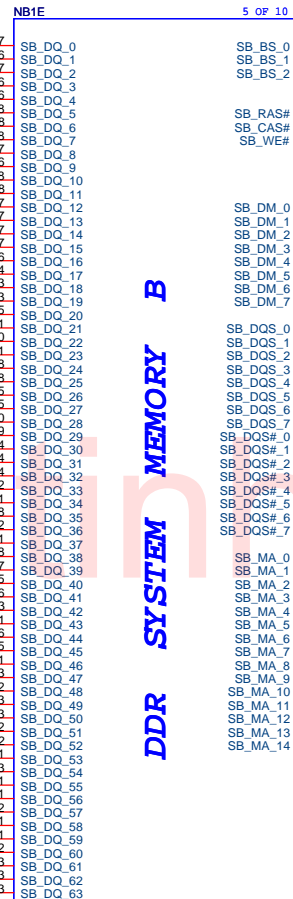
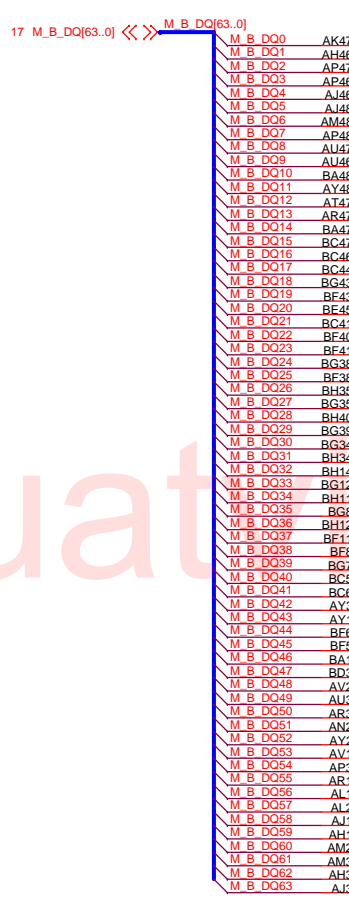
layout take note

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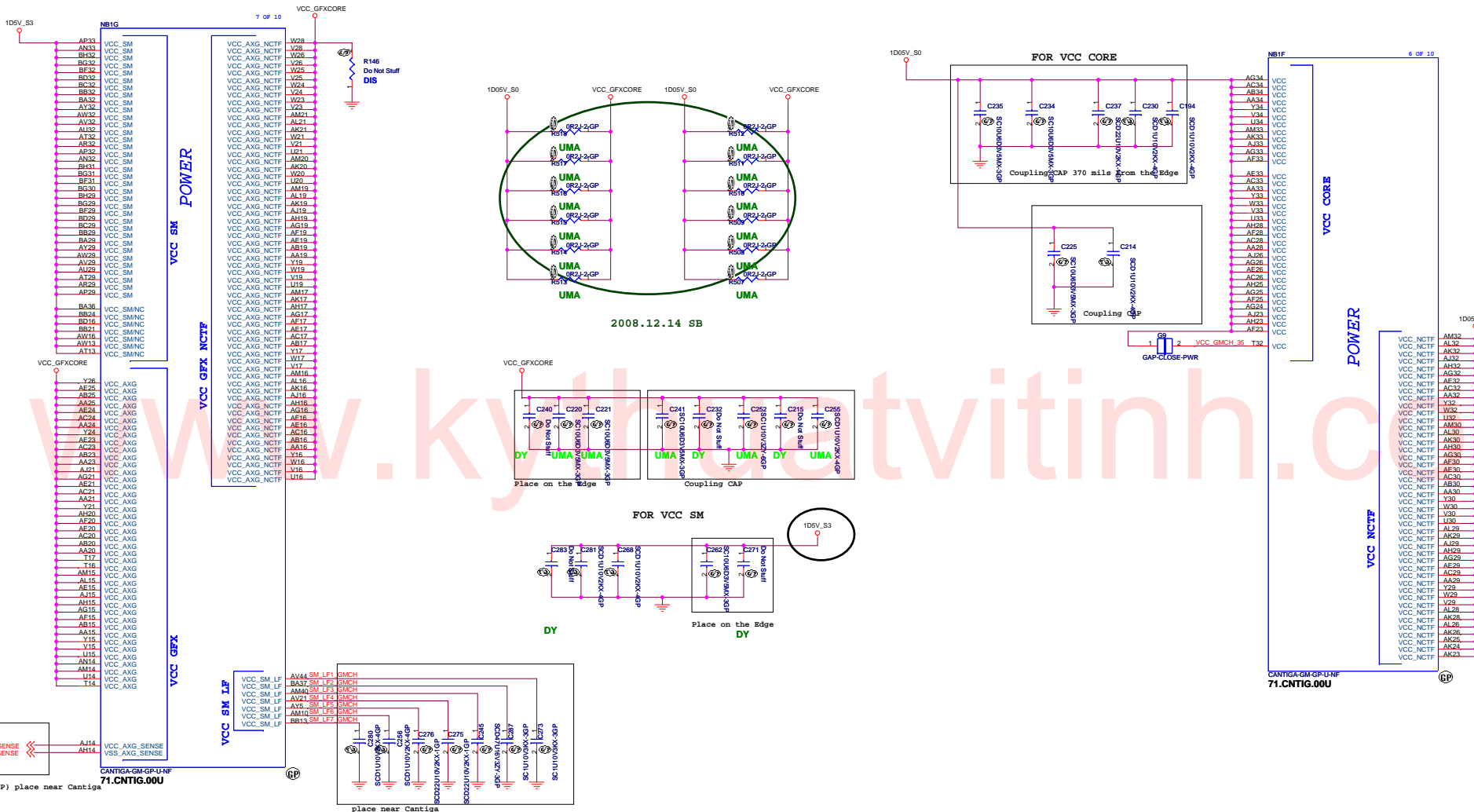
File: **Cantiga (2 of 6)**
 Size: Document Number: **JM70-MV** Rev: **SB**
 Date: **Saturday, December 20, 2008** Sheet: **7** of **55**



CANTIGA-GM-GP-U-NF
71.CNTIG.00U

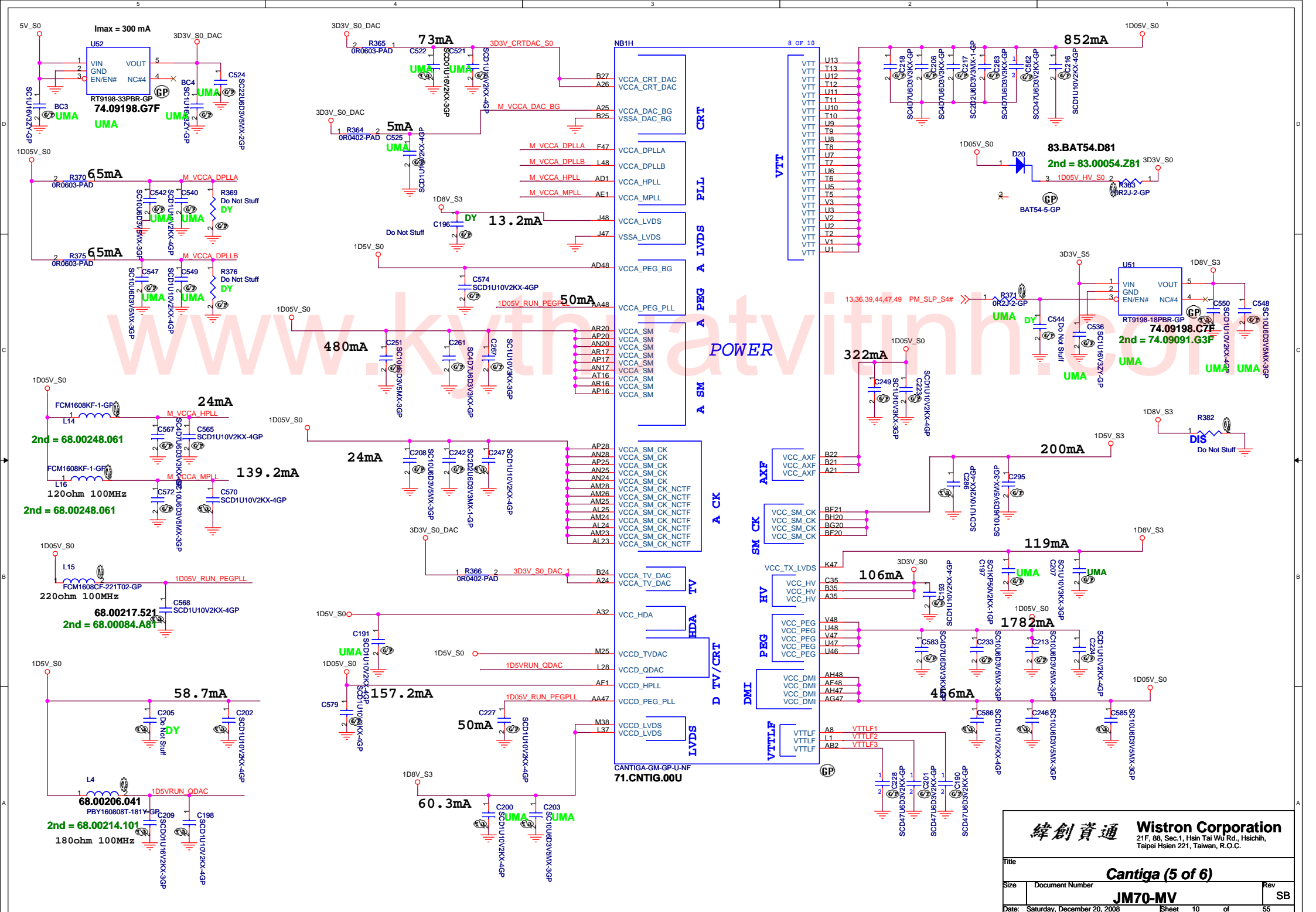


CANTIGA-GM-GP-U-NF
71.CNTIG.00U



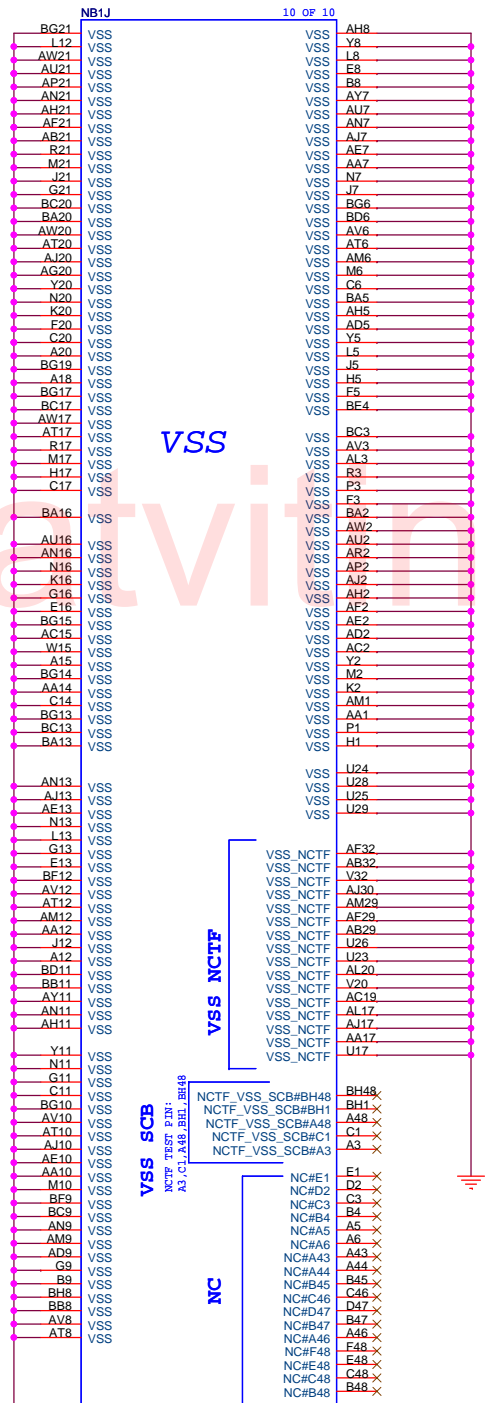
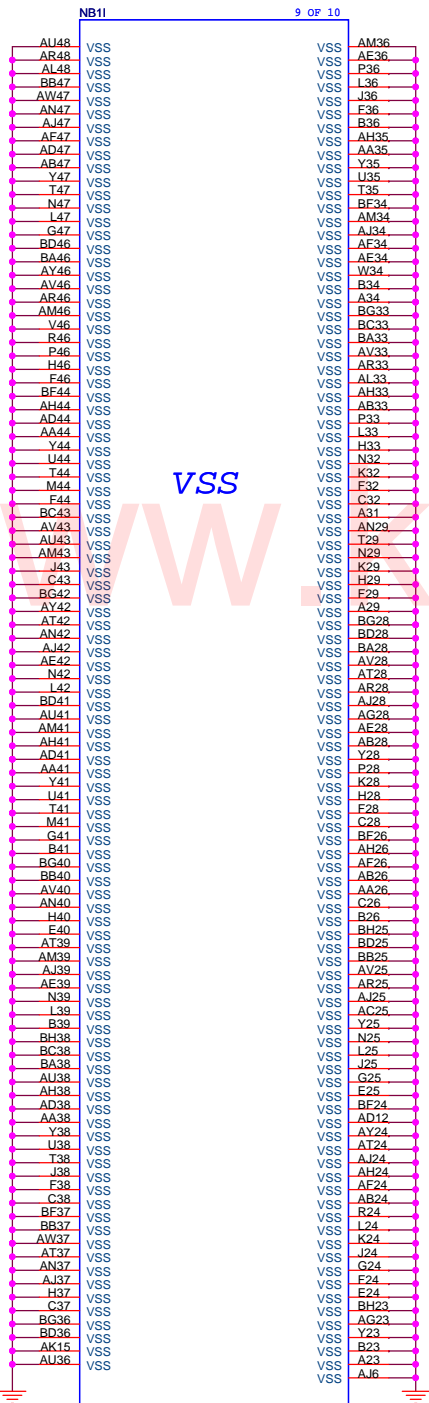
U60 (I8L263AKRZ-T-GP) place near Cantiga 71.CNTIG.000

place near Cantiga



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Title		
Cantiga (5 of 6)		
Size	Document Number	Rev
JM70-MV		SB
Date: Saturday, December 20, 2008	Sheet 10	of 55

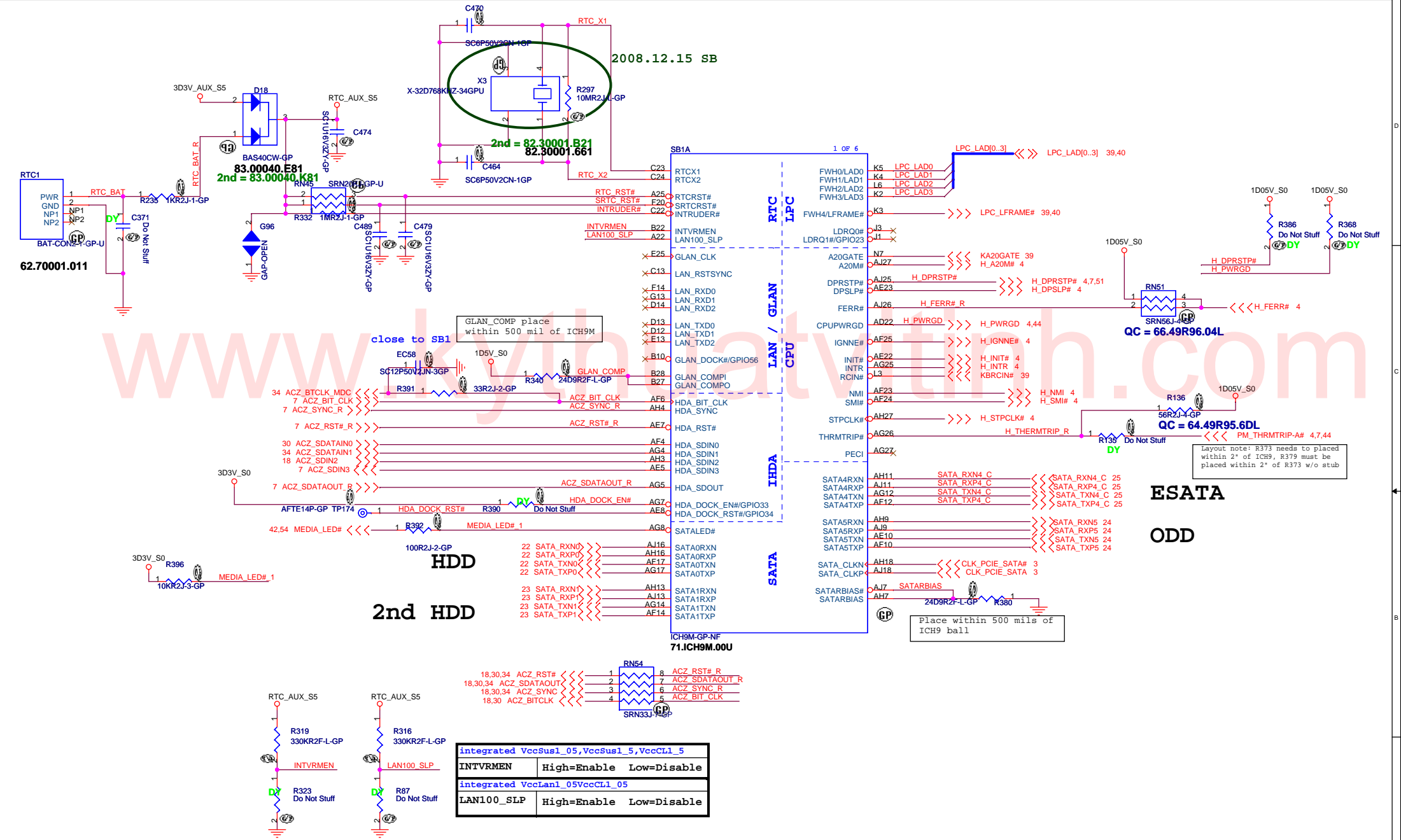


緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Cantiga (6 of 6)**

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2008.12.15 SB

62.70001.011

83.0040.E81
2nd = 83.0040.K81

2nd = 82.30001.B21
82.30001.661

close to SB1
GLAN_COMP place within 500 mil of ICH9M

Layout note: R373 needs to be placed within 2" of ICH9, R379 must be placed within 2" of R373 w/o stub

integrated VccSus1_05,VccSus1_5,VccCLI_5	
INTVRMEN	High=Enable Low=Disable
integrated VccLan1_05VccCLI_05	
LAN100_SLP	High=Enable Low=Disable

ESATA
ODD

UMA

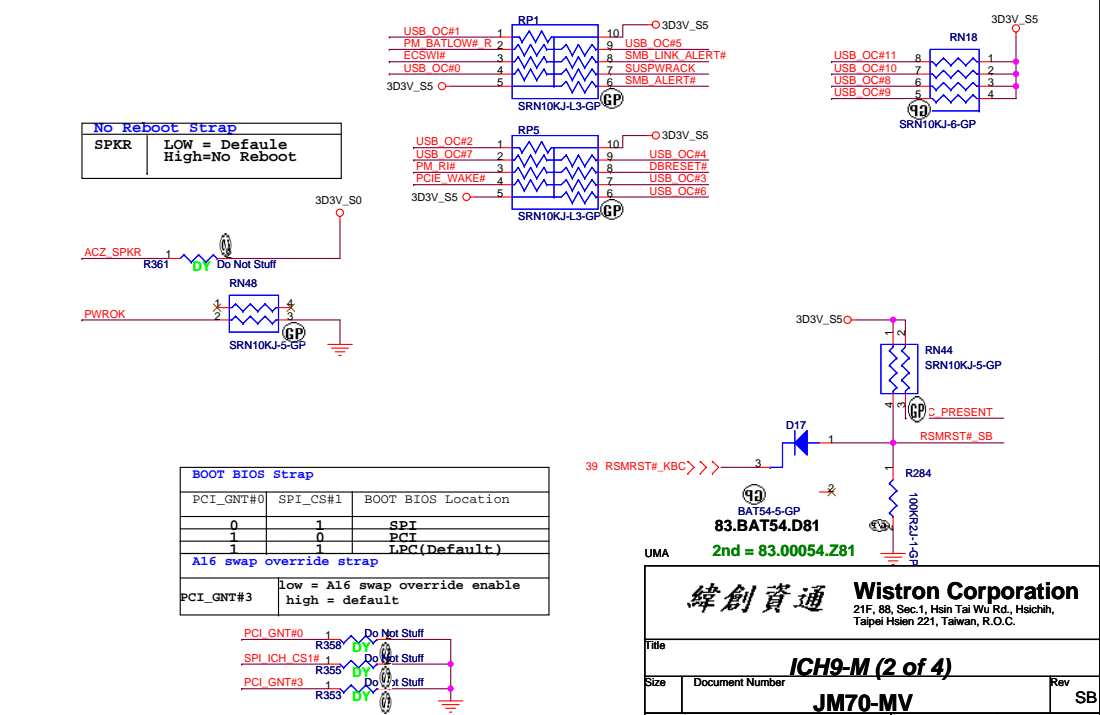
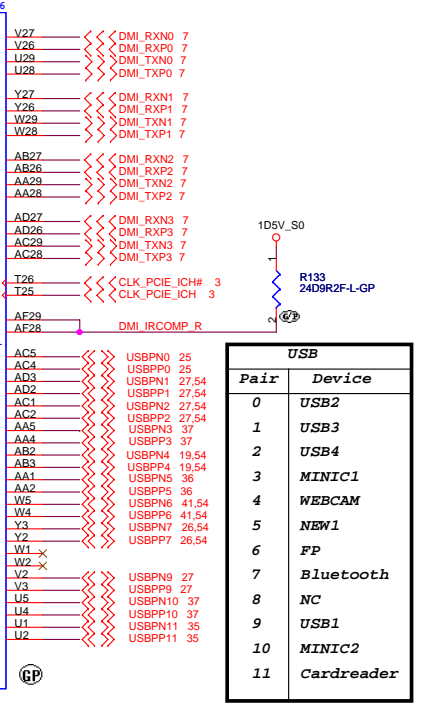
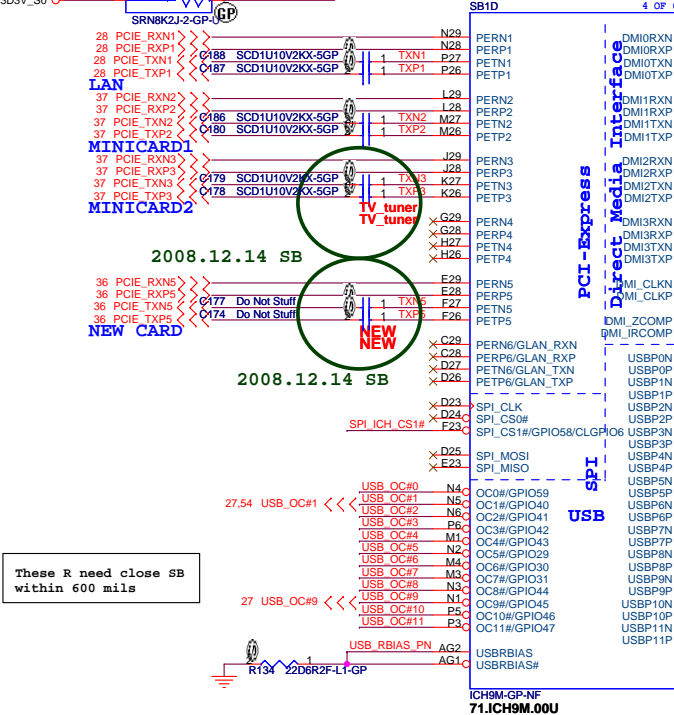
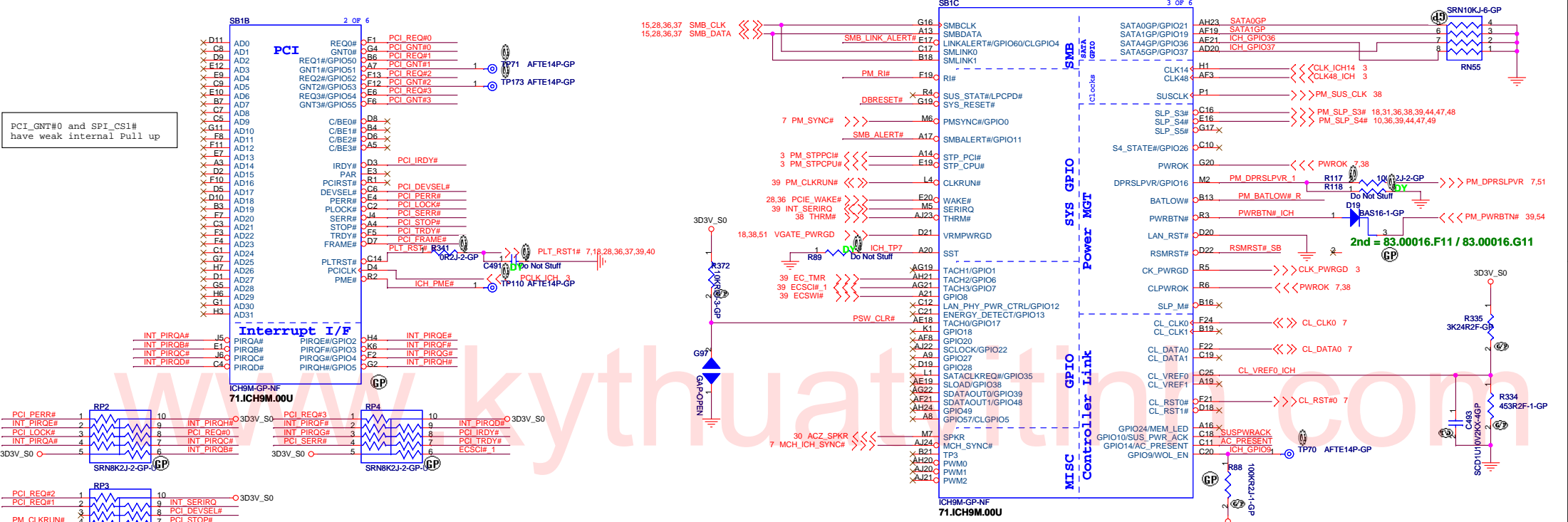
緯創資通 Wistron Corporation
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Title: **ICH9-M (1 of 4)**

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PCI_GNT#0 and SPI_CS1# have weak internal Pull up



Pair	Device
0	USB2
1	USB3
2	USB4
3	MINIC1
4	WEBCAM
5	NEW1
6	FP
7	Bluetooth
8	NC
9	USB1
10	MINIC2
11	Cardreader

Pair	Device
0	USB2
1	USB3
2	USB4
3	MINIC1
4	WEBCAM
5	NEW1
6	FP
7	Bluetooth
8	NC
9	USB1
10	MINIC2
11	Cardreader

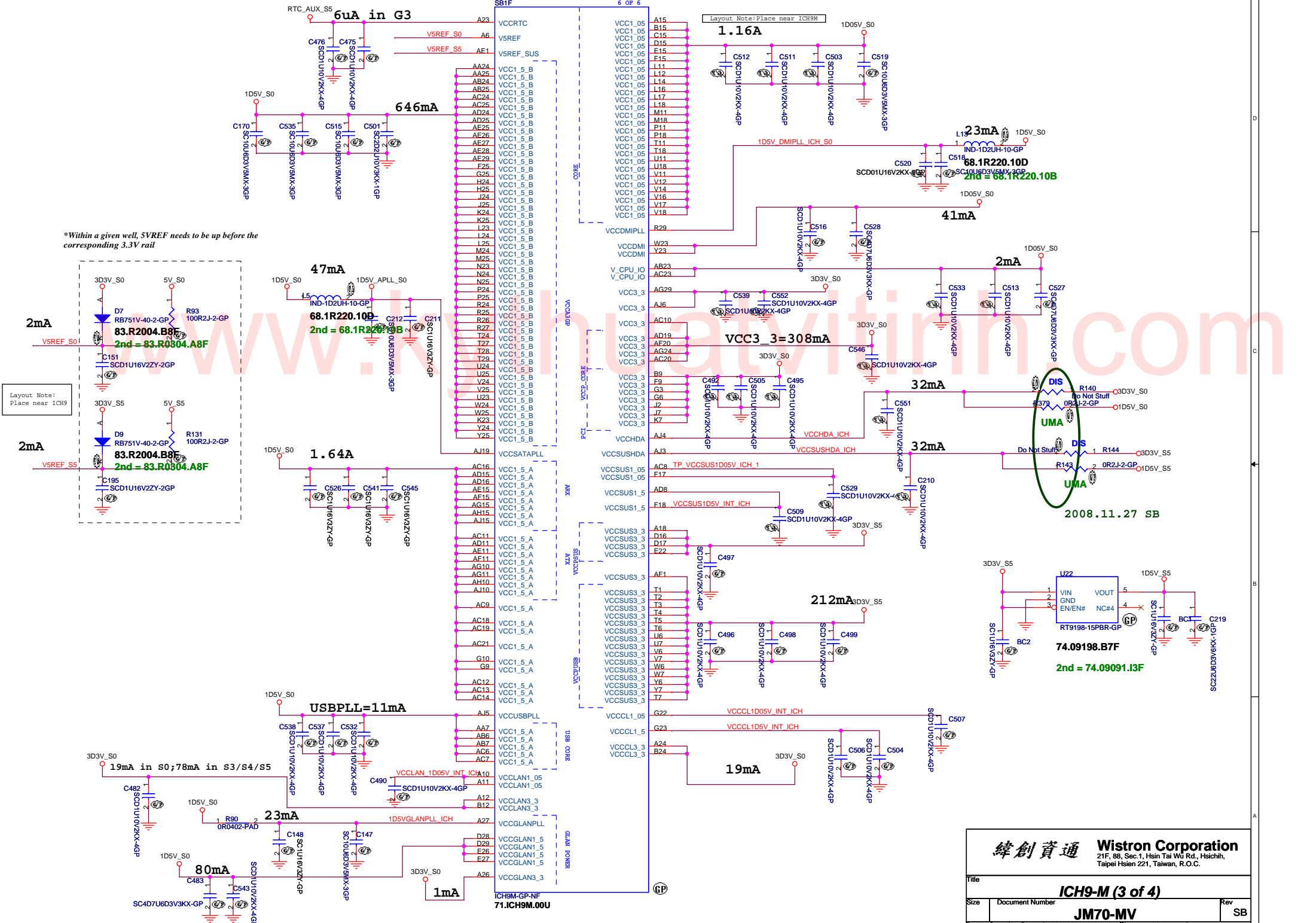
Pair	Device
0	USB2
1	USB3
2	USB4
3	MINIC1
4	WEBCAM
5	NEW1
6	FP
7	Bluetooth
8	NC
9	USB1
10	MINIC2
11	Cardreader

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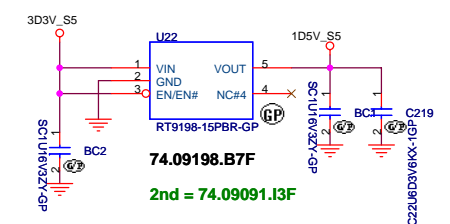
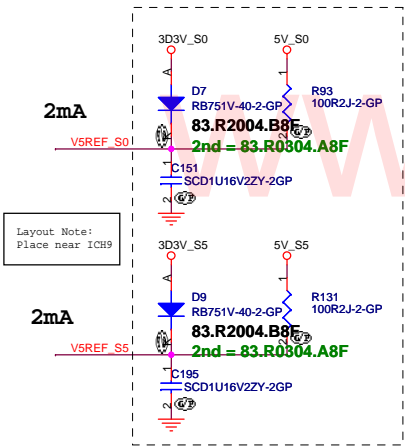
83.BAT54.D81
2nd = 83.00054.281

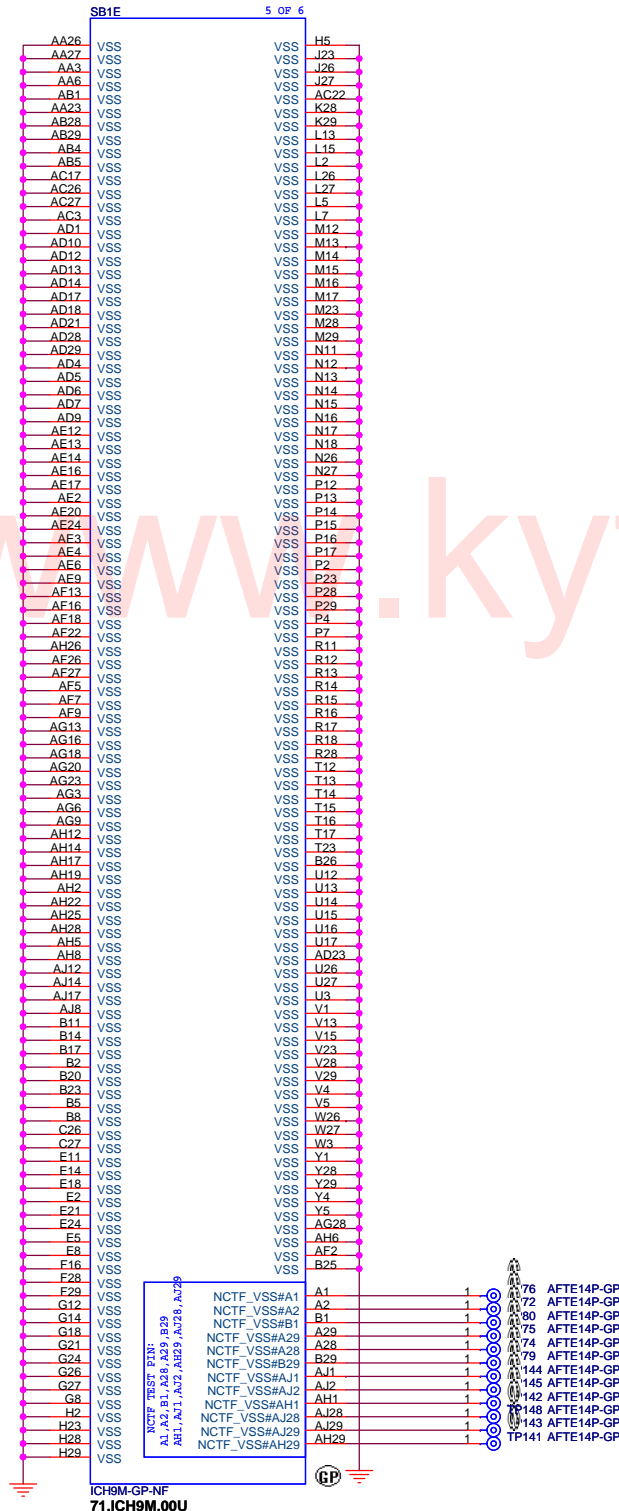
ICH9-M (2 of 4)
JM70-MV

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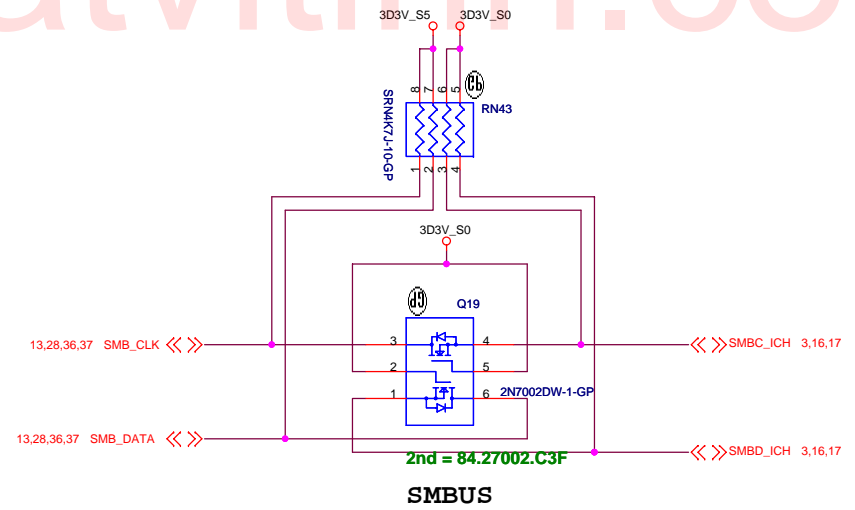
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail





ICH9M-GP-NF
71.ICH9M.00U

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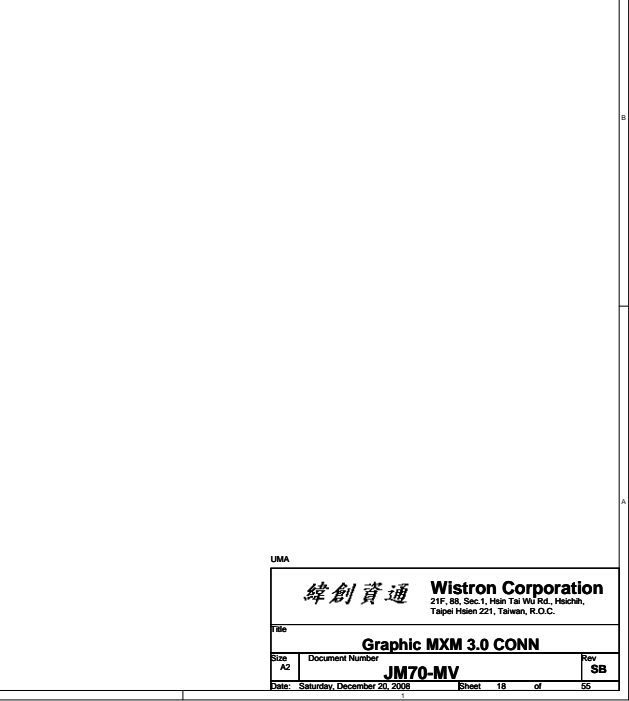
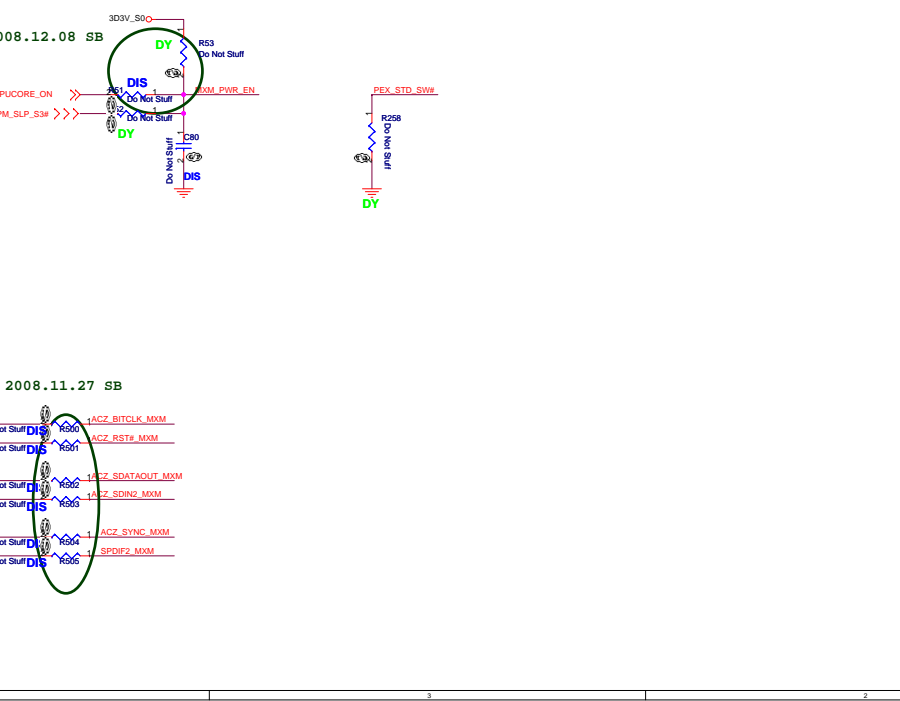
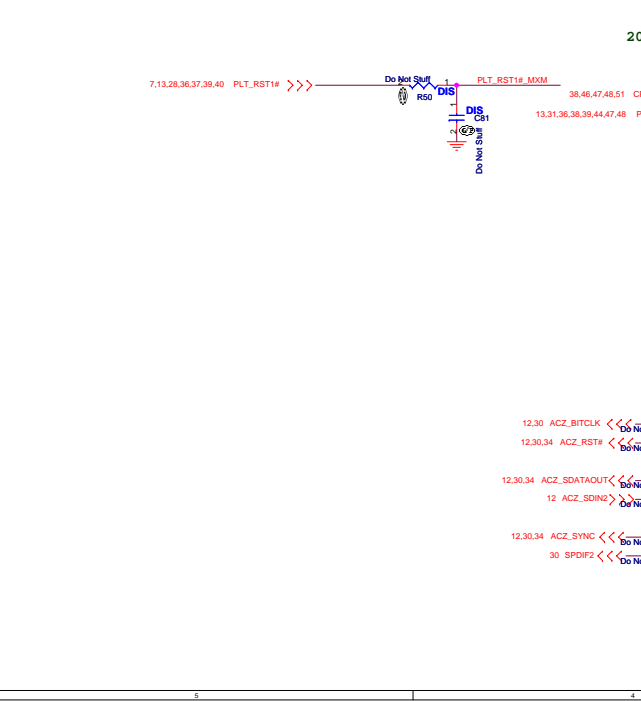
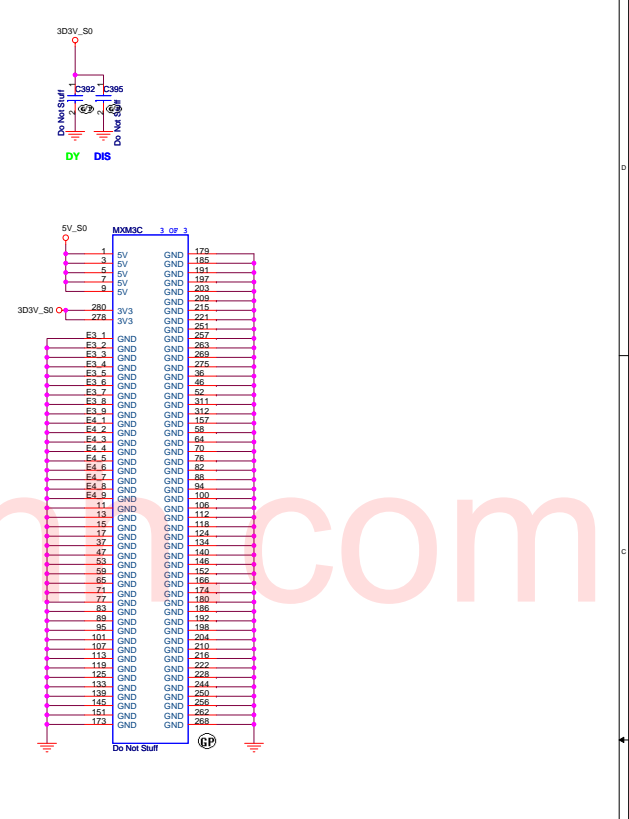
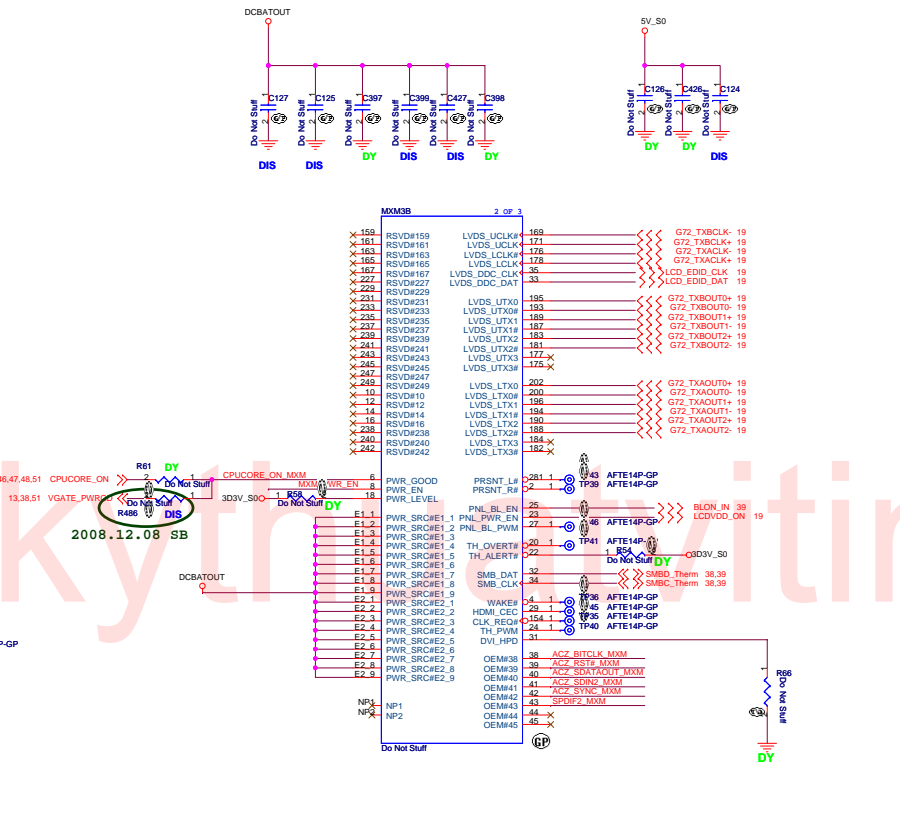


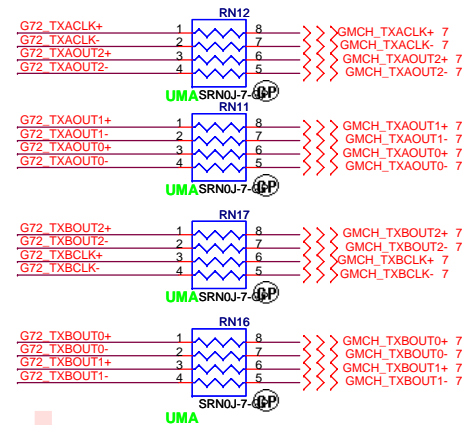
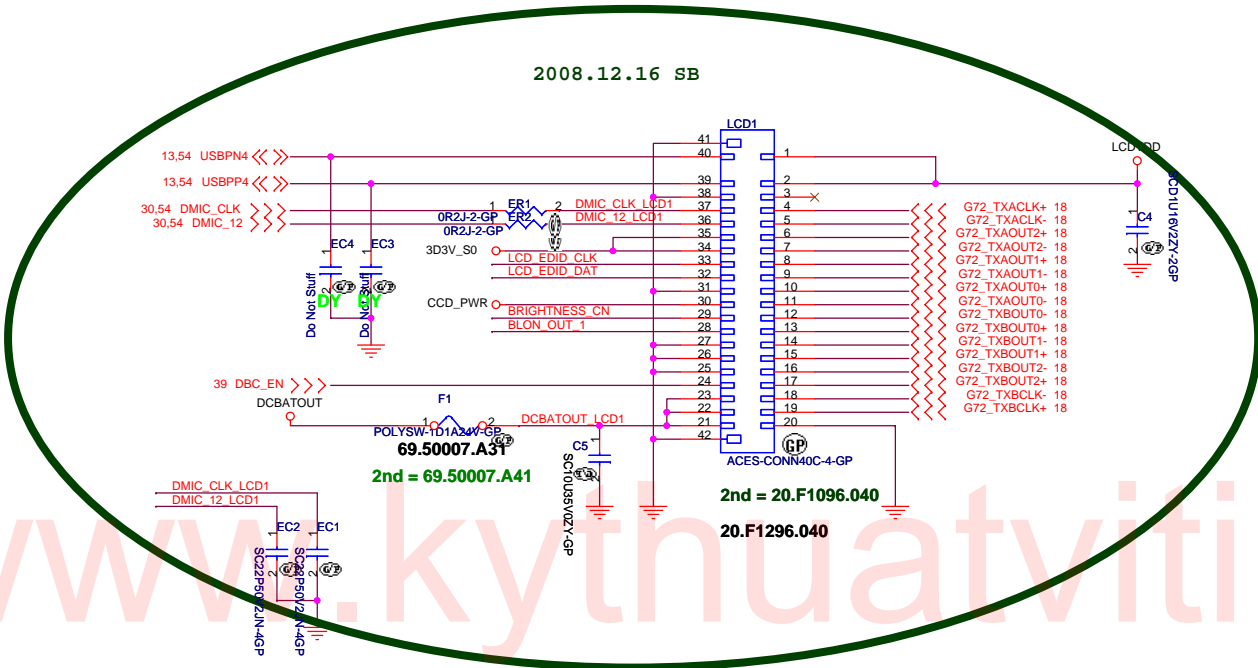
SMBUS

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ICH9-M (4 of 4)			
Title			Rev
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Date:	Saturday, December 20, 2008	Sheet	15 of 55

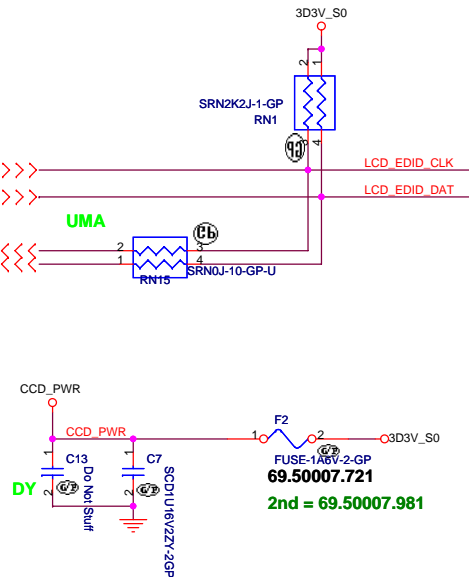
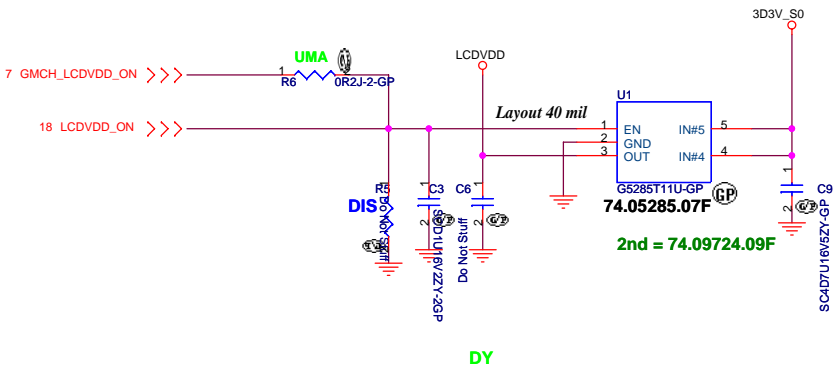
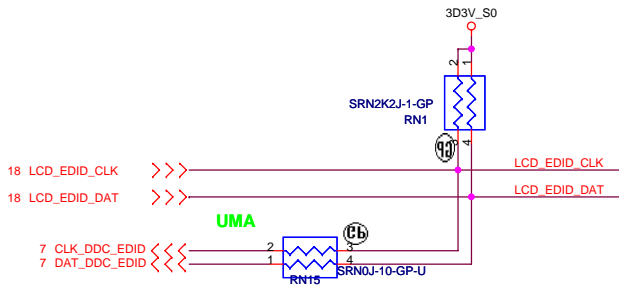
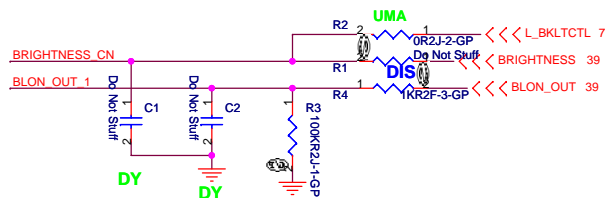
7 PEG_TXP[15..0] <<<< DIS
 7 PEG_TXN[15..0] <<<< DIS
 7 PEG_RXP[15..0] <<<< DIS
 7 PEG_RXN[15..0] <<<< DIS

MXM3A 1 of 3		MXM3B 2 of 3	
PEG_RXP0 Do Not Stuff	C452 DIS GRXP0 149	PEG_RX0	DP_A_AUX4 277
PEG_RXN0 Do Not Stuff	C451 DIS GRXN0 147	PEG_RX08	DP_A_AUX 279
PEG_RXP1 Do Not Stuff	C443 DIS GRXP1 143	PEG_RX1	DP_A_HPD 276
PEG_RXN1 Do Not Stuff	C444 DIS GRXN1 141	PEG_RX14	
PEG_RXP2 Do Not Stuff	C442 DIS GRXP2 137	PEG_RX2	DP_A_L0# 263
PEG_RXN2 Do Not Stuff	C441 DIS GRXN2 135	PEG_RX28	DP_A_L0 265
PEG_RXP3 Do Not Stuff	C434 DIS GRXP3 123	PEG_RX3	DP_A_L1# 269
PEG_RXN3 Do Not Stuff	C435 DIS GRXN3 121	PEG_RX34	DP_A_L1 261
PEG_RXP4 Do Not Stuff	C450 DIS GRXP4 117	PEG_RX38	DP_A_L2# 265
PEG_RXN4 Do Not Stuff	C449 DIS GRXN4 115	PEG_RX44	DP_A_L2 267
PEG_RXP5 Do Not Stuff	C439 DIS GRXP5 111	PEG_RX48	DP_A_L3# 271
PEG_RXN5 Do Not Stuff	C446 DIS GRXN5 109	PEG_RX54	DP_A_L3 273
PEG_RXP6 Do Not Stuff	C438 DIS GRXP6 105	PEG_RX6	
PEG_RXN6 Do Not Stuff	C436 DIS GRXN6 103	PEG_RX68	
PEG_RXP7 Do Not Stuff	C440 DIS GRXP7 99	PEG_RX7	DP_B_AUX4 270
PEG_RXN7 Do Not Stuff	C439 DIS GRXN7 97	PEG_RX74	DP_B_AUX 272
PEG_RXP8 Do Not Stuff	C438 DIS GRXP8 93	PEG_RX8	DP_B_HPD 274
PEG_RXN8 Do Not Stuff	C437 DIS GRXN8 91	PEG_RX88	
PEG_RXP9 Do Not Stuff	C430 DIS GRXP9 87	PEG_RX98	DP_B_L0# 246
PEG_RXN9 Do Not Stuff	C429 DIS GRXN9 85	PEG_RX988	DP_B_L0 248
PEG_RXP10 Do Not Stuff	C448 DIS GRXP10 81	PEG_RX10	DP_B_L1# 252
PEG_RXN10 Do Not Stuff	C447 DIS GRXN10 79	PEG_RX10#	DP_B_L1 254
PEG_RXP11 Do Not Stuff	C439 DIS GRXP11 75	PEG_RX11#	DP_B_L2# 258
PEG_RXN11 Do Not Stuff	C431 DIS GRXN11 73	PEG_RX11	DP_B_L2 260
PEG_RXP12 Do Not Stuff	C458 DIS GRXP12 69	PEG_RX12#	DP_B_L3# 264
PEG_RXN12 Do Not Stuff	C454 DIS GRXN12 67	PEG_RX12	DP_B_L3 266
PEG_RXP13 Do Not Stuff	C425 DIS GRXP13 63	PEG_RX13	
PEG_RXN13 Do Not Stuff	C424 DIS GRXN13 61	PEG_RX13#	
PEG_RXP14 Do Not Stuff	C421 DIS GRXP14 57	PEG_RX14#	DP_C_AUX4 223
PEG_RXN14 Do Not Stuff	C420 DIS GRXN14 55	PEG_RX14#	DP_C_AUX 225
PEG_RXP15 Do Not Stuff	C423 DIS GRXP15 51	PEG_RX15#	DP_C_HPD 234
PEG_RXN15 Do Not Stuff	C422 DIS GRXN15 49	PEG_RX15#	DP_C_L0# 199
PEG_TXP0 Do Not Stuff	C103 DIS GTXP0 150	PEG_TX0	DP_C_L0 201
PEG_TXN0 Do Not Stuff	C102 DIS GTXN0 148	PEG_TX0#	DP_C_L1# 207
PEG_TXP1 Do Not Stuff	C106 DIS GTXP1 144	PEG_TX1	DP_C_L1 209
PEG_TXN1 Do Not Stuff	C105 DIS GTXN1 142	PEG_TX1#	DP_C_L2# 211
PEG_TXP2 Do Not Stuff	C104 DIS GTXP2 138	PEG_TX2	DP_C_L2 213
PEG_TXN2 Do Not Stuff	C099 DIS GTXN2 136	PEG_TX2#	DP_C_L3# 217
PEG_TXP3 Do Not Stuff	C100 DIS GTXP3 132	PEG_TX3	DP_C_L3 219
PEG_TXN3 Do Not Stuff	C101 DIS GTXN3 130	PEG_TX3#	
PEG_TXP4 Do Not Stuff	C075 DIS GTXP4 116	PEG_TX4	
PEG_TXN4 Do Not Stuff	C074 DIS GTXN4 114	PEG_TX4#	DP_D_AUX4 230
PEG_TXP5 Do Not Stuff	C088 DIS GTXP5 110	PEG_TX5	DP_D_AUX 232
PEG_TXN5 Do Not Stuff	C087 DIS GTXN5 108	PEG_TX5#	DP_D_HPD 228
PEG_TXP6 Do Not Stuff	C078 DIS GTXP6 104	PEG_TX6#	
PEG_TXN6 Do Not Stuff	C077 DIS GTXN6 102	PEG_TX6	DP_D_L0# 208
PEG_TXP7 Do Not Stuff	C076 DIS GTXP7 98	PEG_TX7#	DP_D_L0 208
PEG_TXN7 Do Not Stuff	C077 DIS GTXN7 96	PEG_TX7#	DP_D_L1# 212
PEG_TXP8 Do Not Stuff	C074 DIS GTXP8 92	PEG_TX8#	DP_D_L1 214
PEG_TXN8 Do Not Stuff	C072 DIS GTXN8 90	PEG_TX8	DP_D_L2# 220
PEG_TXP9 Do Not Stuff	C073 DIS GTXP9 88	PEG_TX9#	DP_D_L2 222
PEG_TXN9 Do Not Stuff	C065 DIS GTXN9 84	PEG_TX9	DP_D_L3# 226
PEG_TXP10 Do Not Stuff	C083 DIS GTXP10 80	PEG_TX10#	DP_D_L3 226
PEG_TXN10 Do Not Stuff	C082 DIS GTXN10 78	PEG_TX10#	
PEG_TXP11 Do Not Stuff	C091 DIS GTXP11 74	PEG_TX11#	VGA_DISABLE# 241
PEG_TXN11 Do Not Stuff	C090 DIS GTXN11 72	PEG_TX11#	VGA_DDC_DAT 160
PEG_TXP12 Do Not Stuff	C090 DIS GTXP12 68	PEG_TX12#	VGA_DDC_CLK# 160
PEG_TXN12 Do Not Stuff	C089 DIS GTXN12 66	PEG_TX12#	CRT_DDCCLK 20
PEG_TXP13 Do Not Stuff	C088 DIS GTXP13 62	PEG_TX13#	VGA_VSYNC 164
PEG_TXN13 Do Not Stuff	C087 DIS GTXN13 60	PEG_TX13#	VGA_HSYNC 164
PEG_TXP14 Do Not Stuff	C086 DIS GTXP14 58	PEG_TX14#	VGA_RED 168
PEG_TXN14 Do Not Stuff	C085 DIS GTXN14 54	PEG_TX14	CRT_RED 20
PEG_TXP15 Do Not Stuff	C084 DIS GTXP15 50	PEG_TX15#	VGA_GREEN 170
PEG_TXN15 Do Not Stuff	C083 DIS GTXN15 46	PEG_TX15#	CRT_GREEN 20
		PEG_TX15#	CRT_BLUE 20



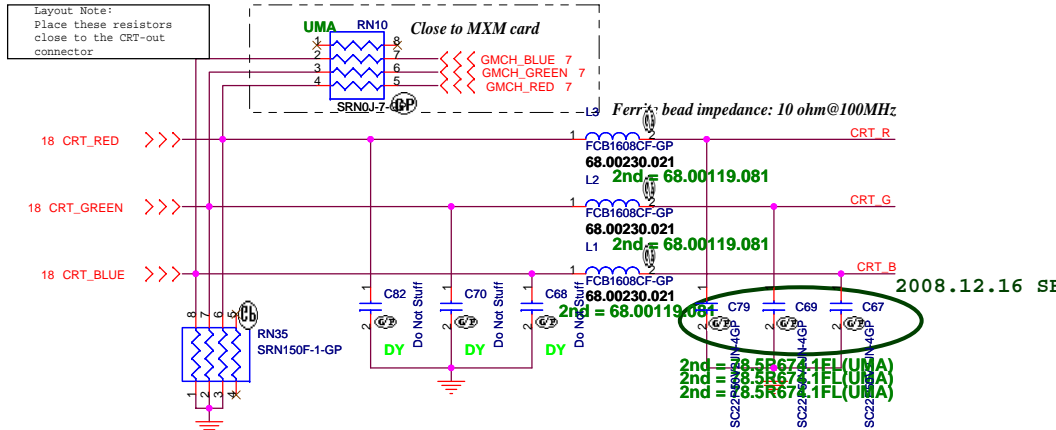


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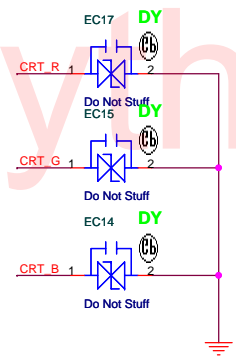


		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
LCD CONN		
File	JM70-MV	
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		SB
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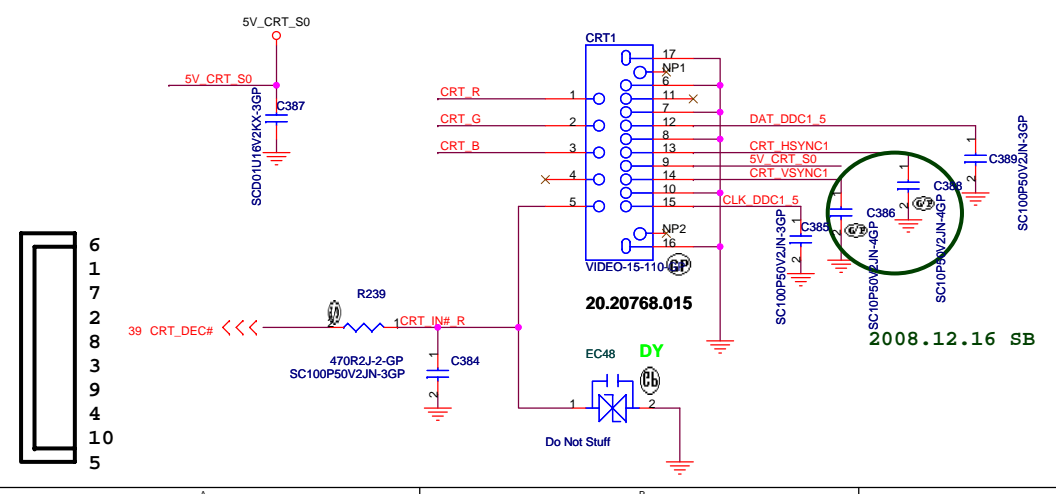
Layout Note:
Place these resistors close to the CRT-out connector



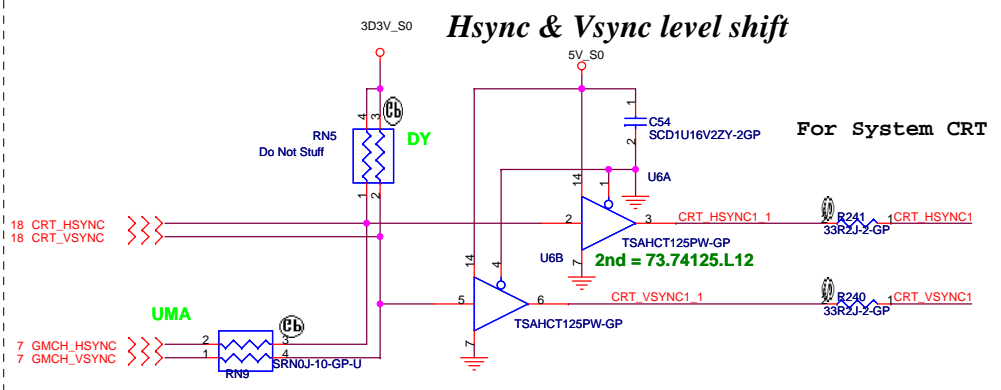
Layout Note:
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.



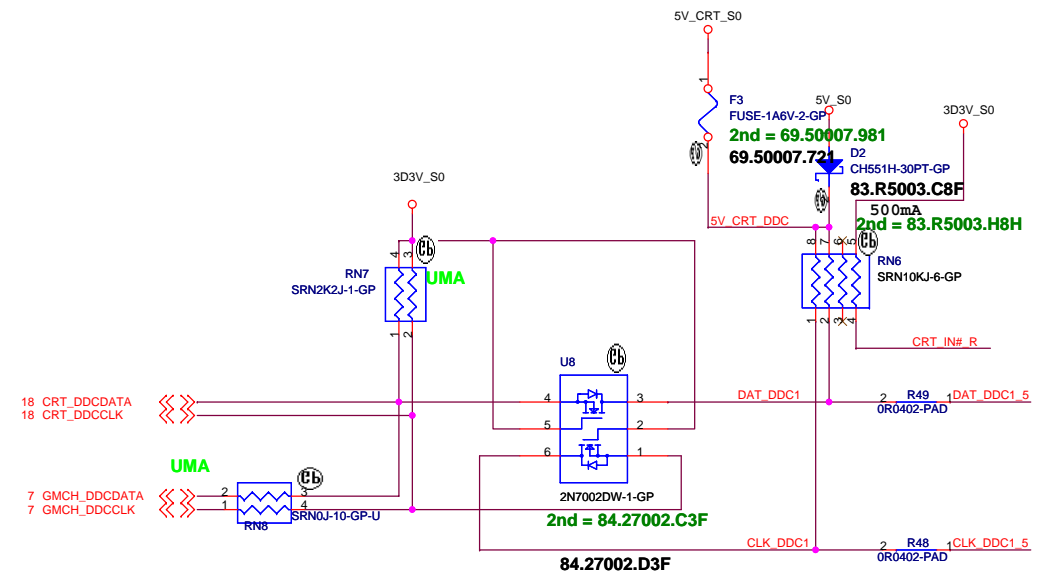
CRT I/F & CONNECTOR



Hsync & Vsync level shift

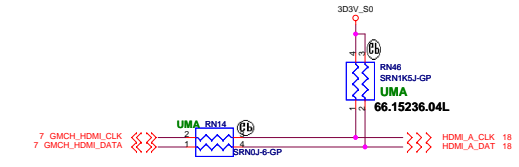
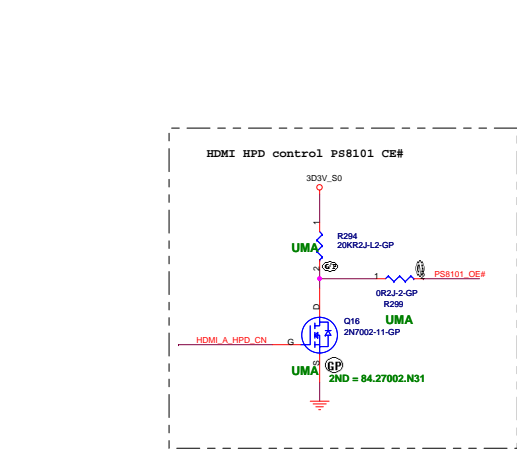
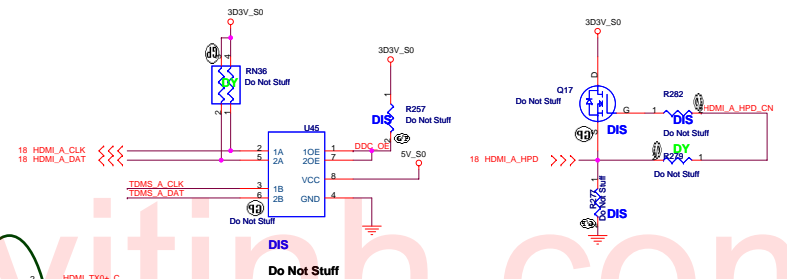
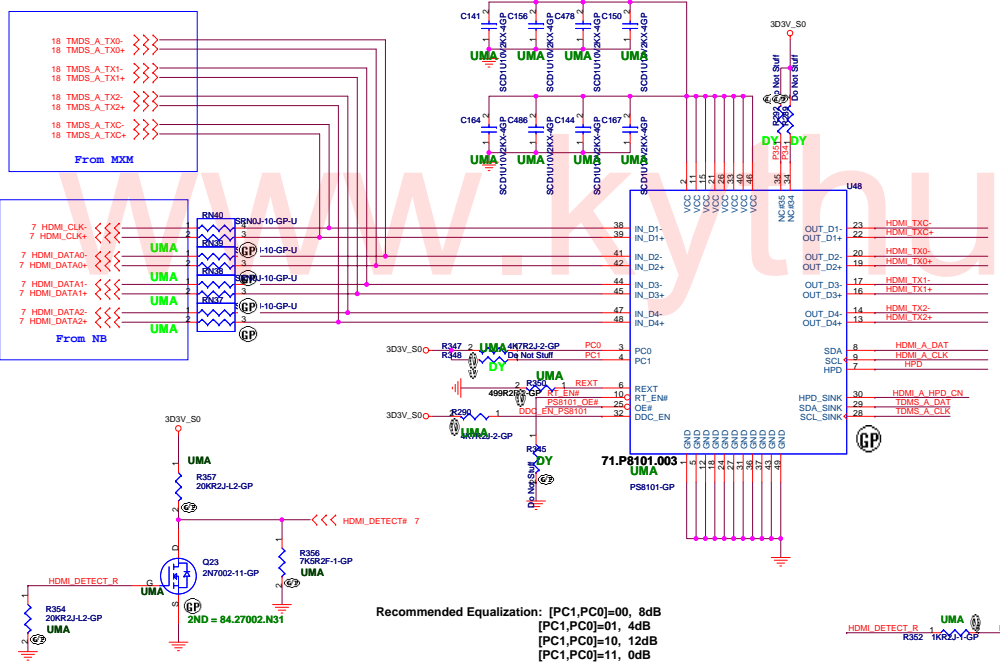
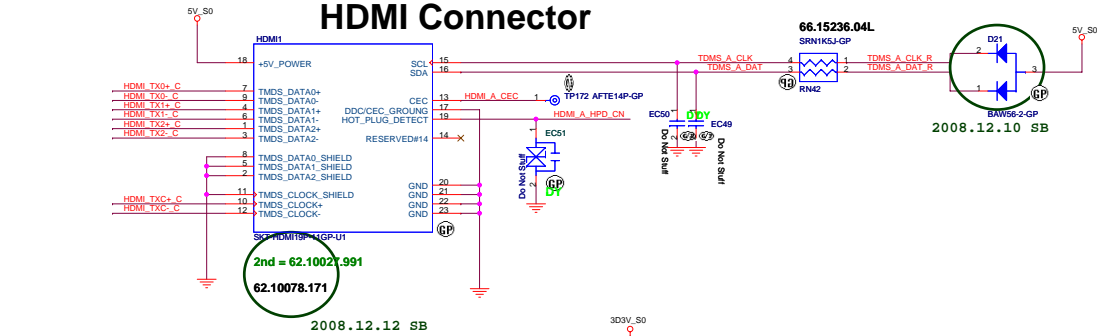


DDC_CLK & DATA level shift



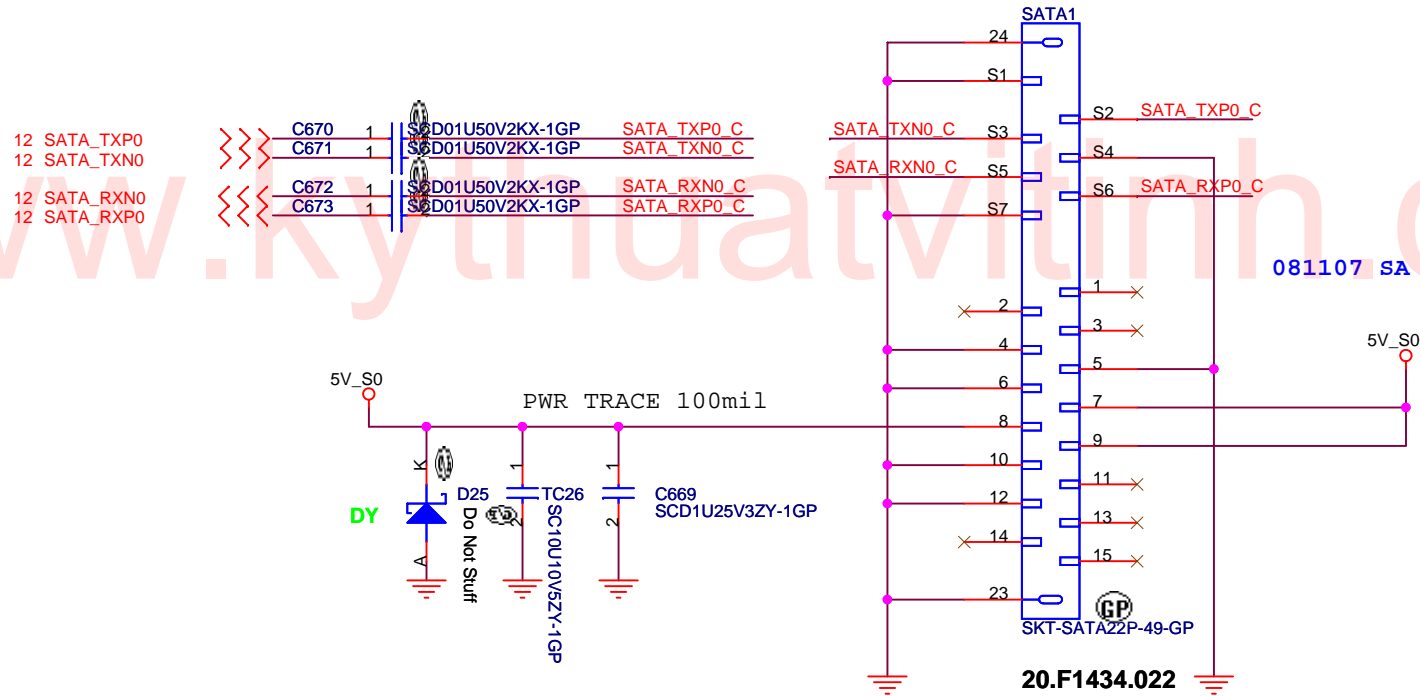
緯創資通		Wistron Corporation	
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
CRT CONN			
Title	Document Number	Rev	SB
JM70-MV			
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HDMI Connector



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SATA Connector



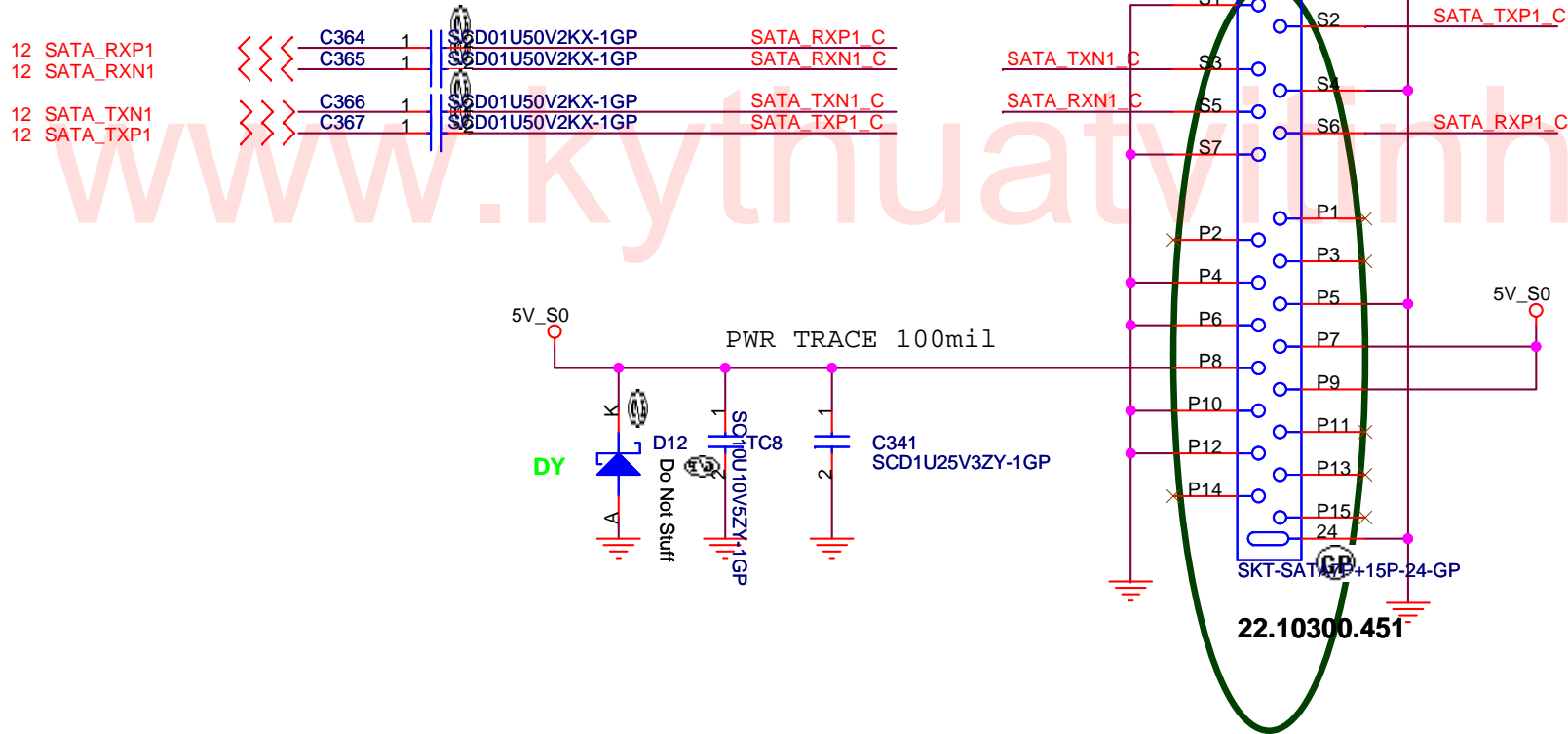
UMA

緯創資通 **Wistron Corporation**
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

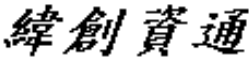
Title			HDD CONN		
Size	Document Number				Rev
	JM70-MV				SB
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2nd HDD SATA Connector

2008.12.12 SB

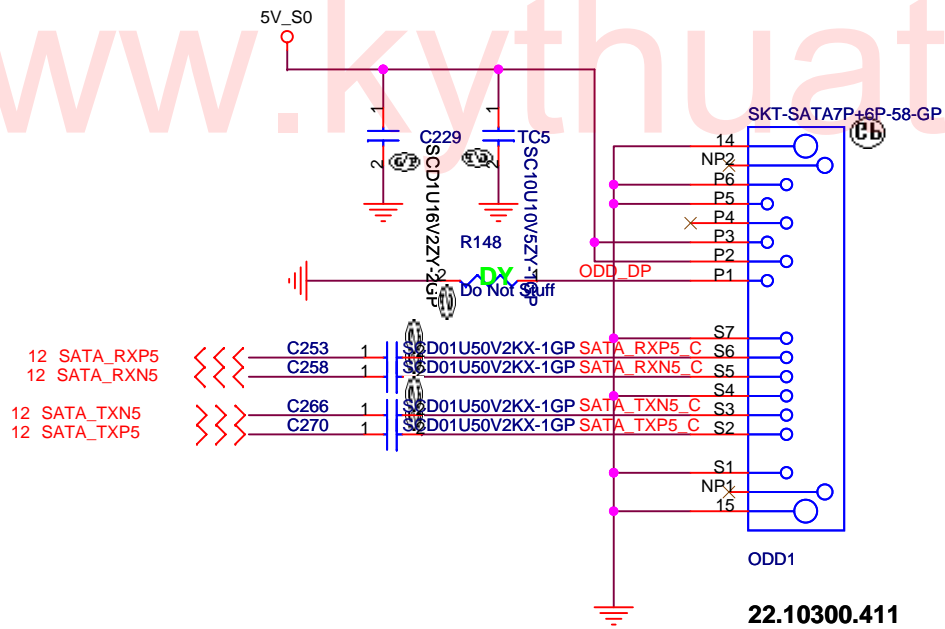


UMA

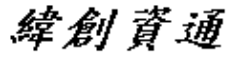
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title 2nd HDD			
Size	Document Number		Rev
	JM70-MV		SB
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ODD Connector

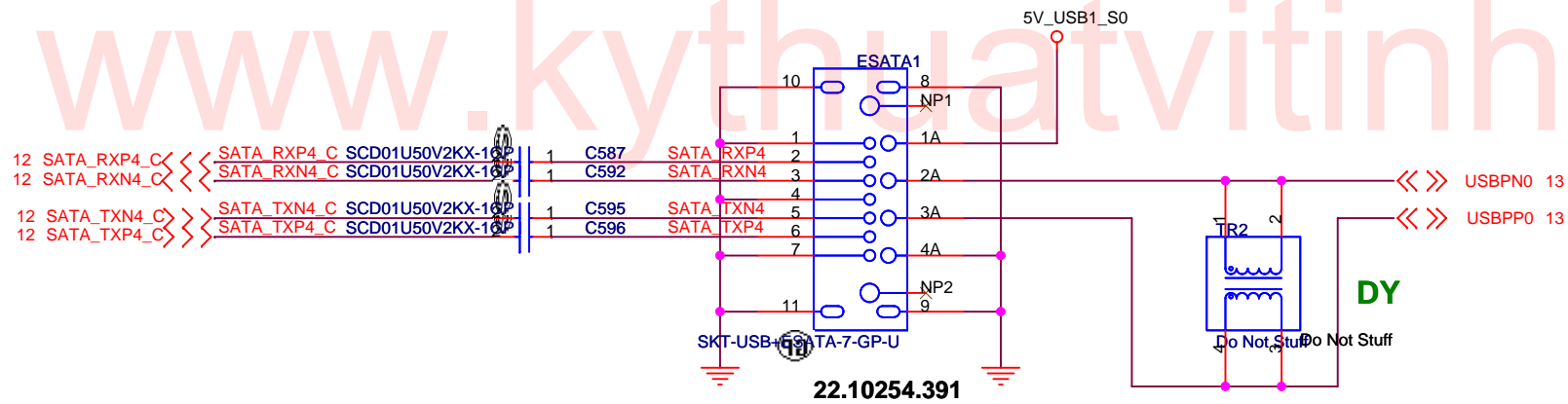
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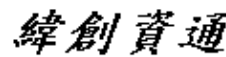
UMA

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Title <h2 style="margin: 0;">ODD</h2>	
Size Document Number <h2 style="margin: 0;">JM70-MV</h2>	Rev SB
Date: Saturday, December 20, 2008	
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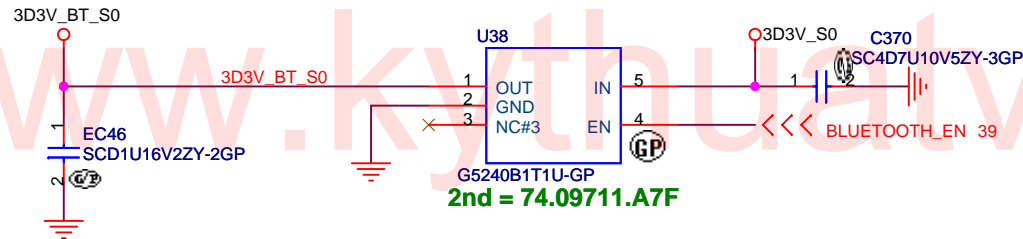
ESATA Connector



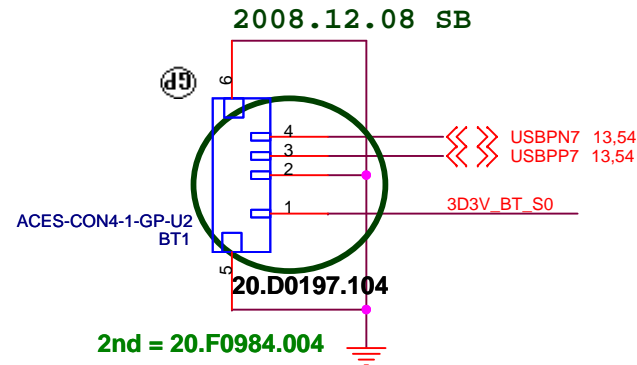
UMA

 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title ESATA	
Size A4	Document Number JM70-MV
Rev SB	
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BLUETOOTH MODULE



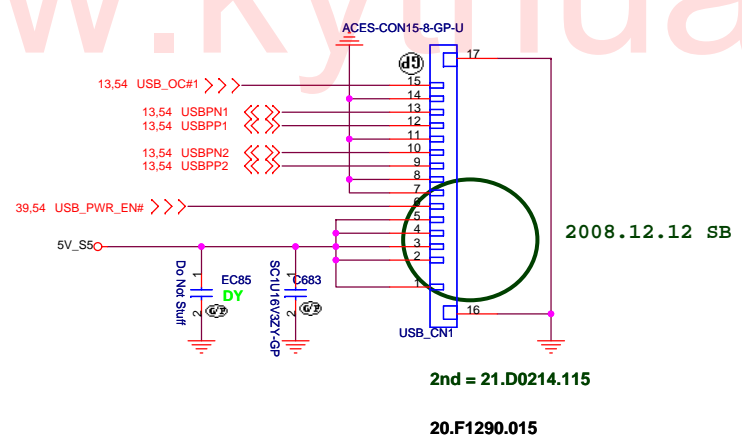
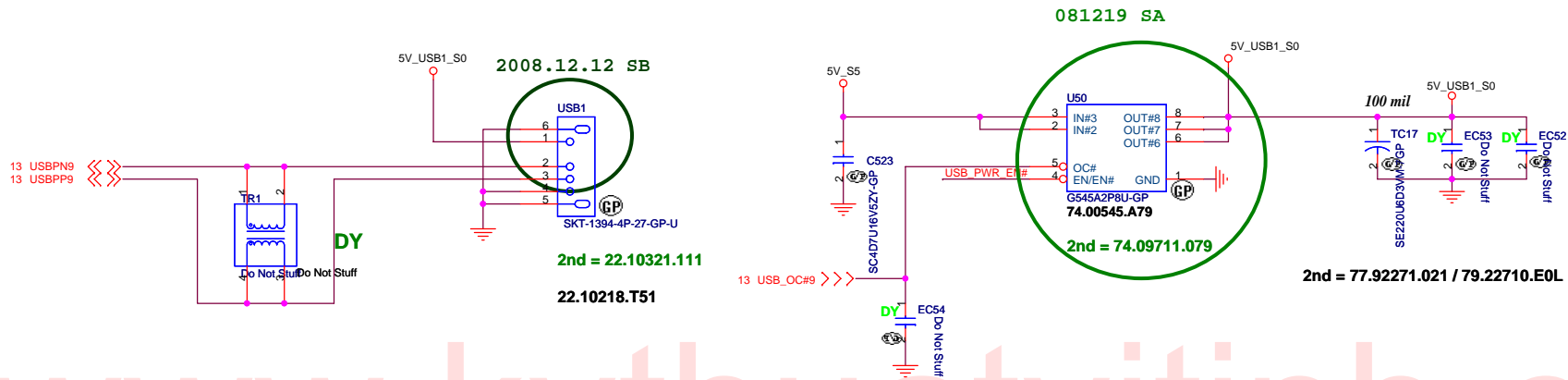
EC20 put near
BLUE1 / all
USB put one
choke near
connector by
EMI request



UMA

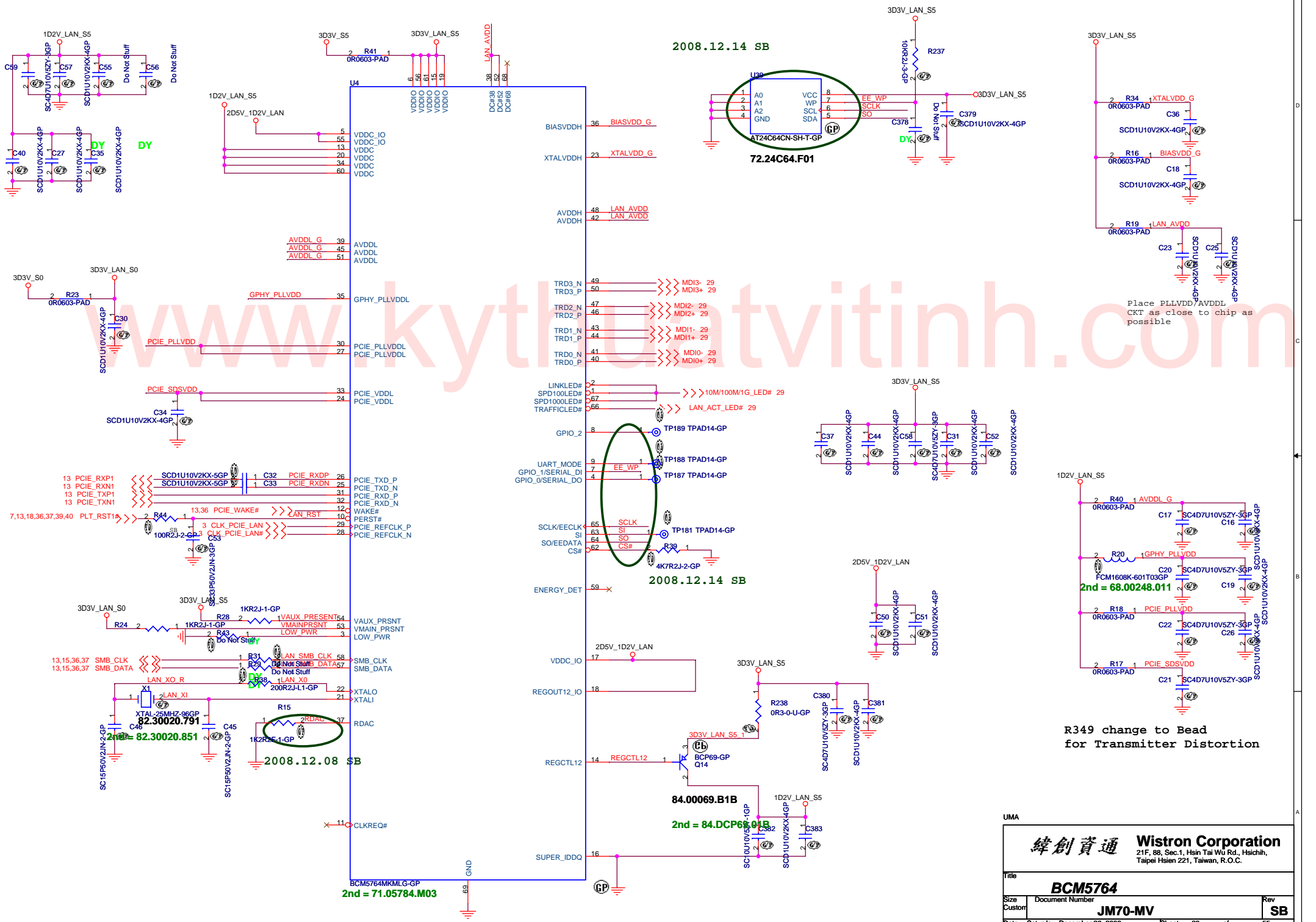
 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title BLUETOOTH	
Size	Document Number
JM70-MV	
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USB1 Connector



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UMA	
Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title USB CONN	
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2008.12.14 SB

2008.12.14 SB

2008.12.08 SB

R349 change to Bead for Transmitter Distortion

Place PLLVDD/AVDDL CKT as close to chip as possible

UMA

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 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **BCM5764**

Size Custom	Document Number	Rev
	JM70-MV	SB

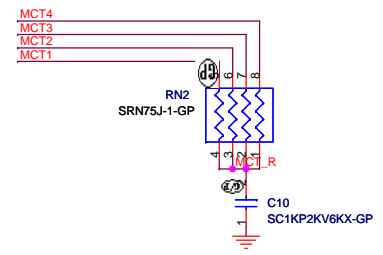
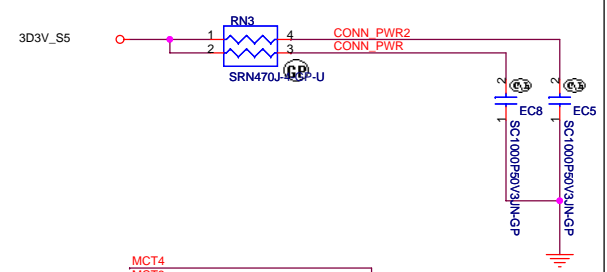
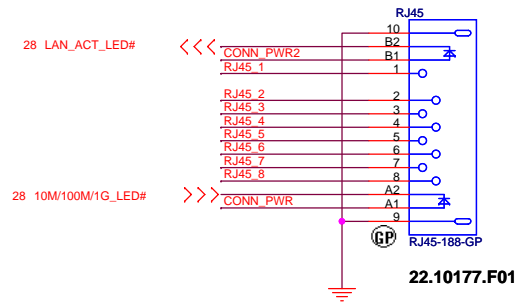
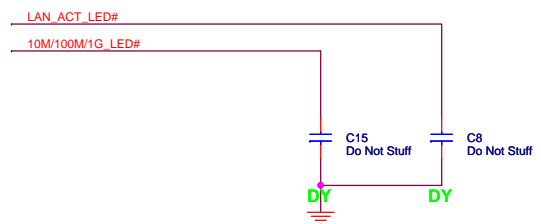
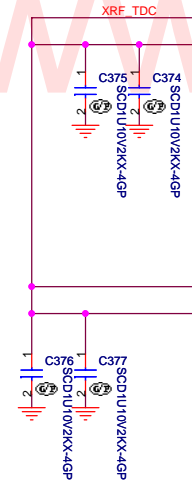
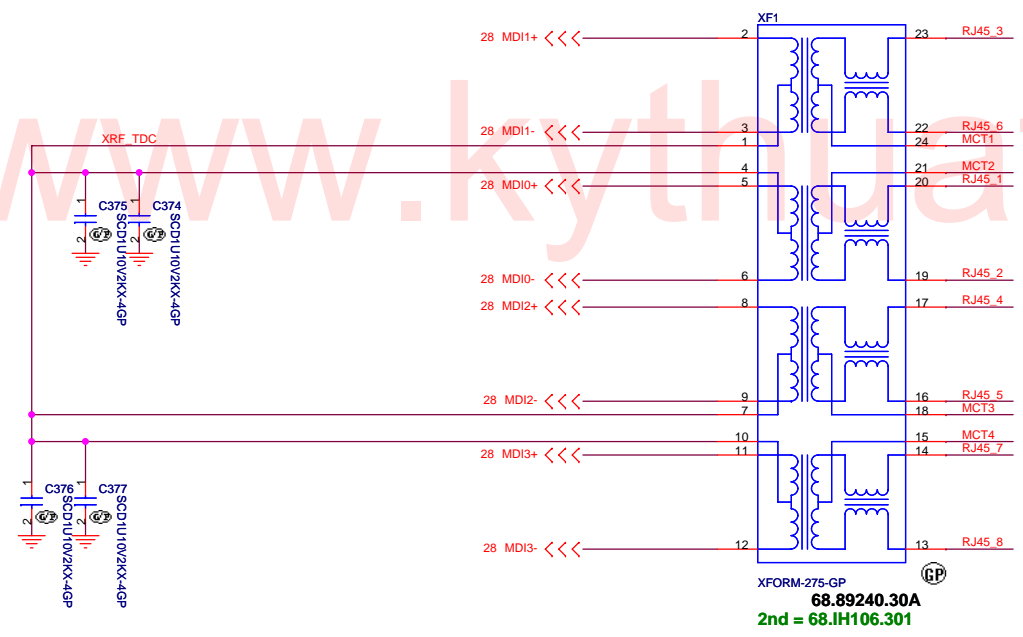
Date: Saturday, December 20, 2008 Sheet 28 of 55

- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.

LAN Connector

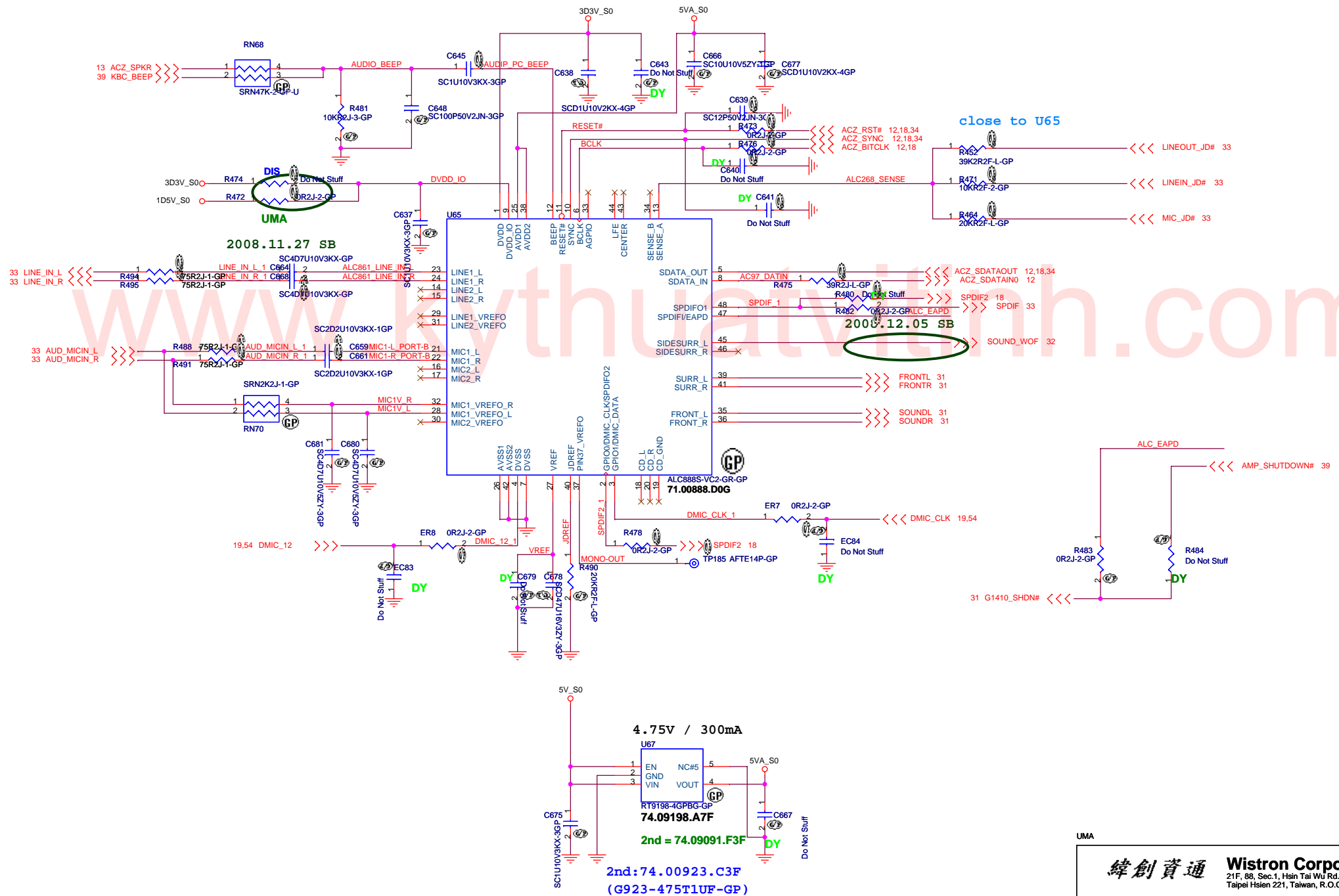
LAN Connector

GIGA Lan Transformer



UMA

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
LAN CONN	
Title LAN CONN	Rev SB
Size A3	Document Number JM70-MV
Date: Saturday, December 20, 2008	Sheet 29 of 55



2008.11.27 SB

2008.12.05 SB

4.75V / 300mA

2nd: 74.00923.C3F
(G923-475T1UF-GP)

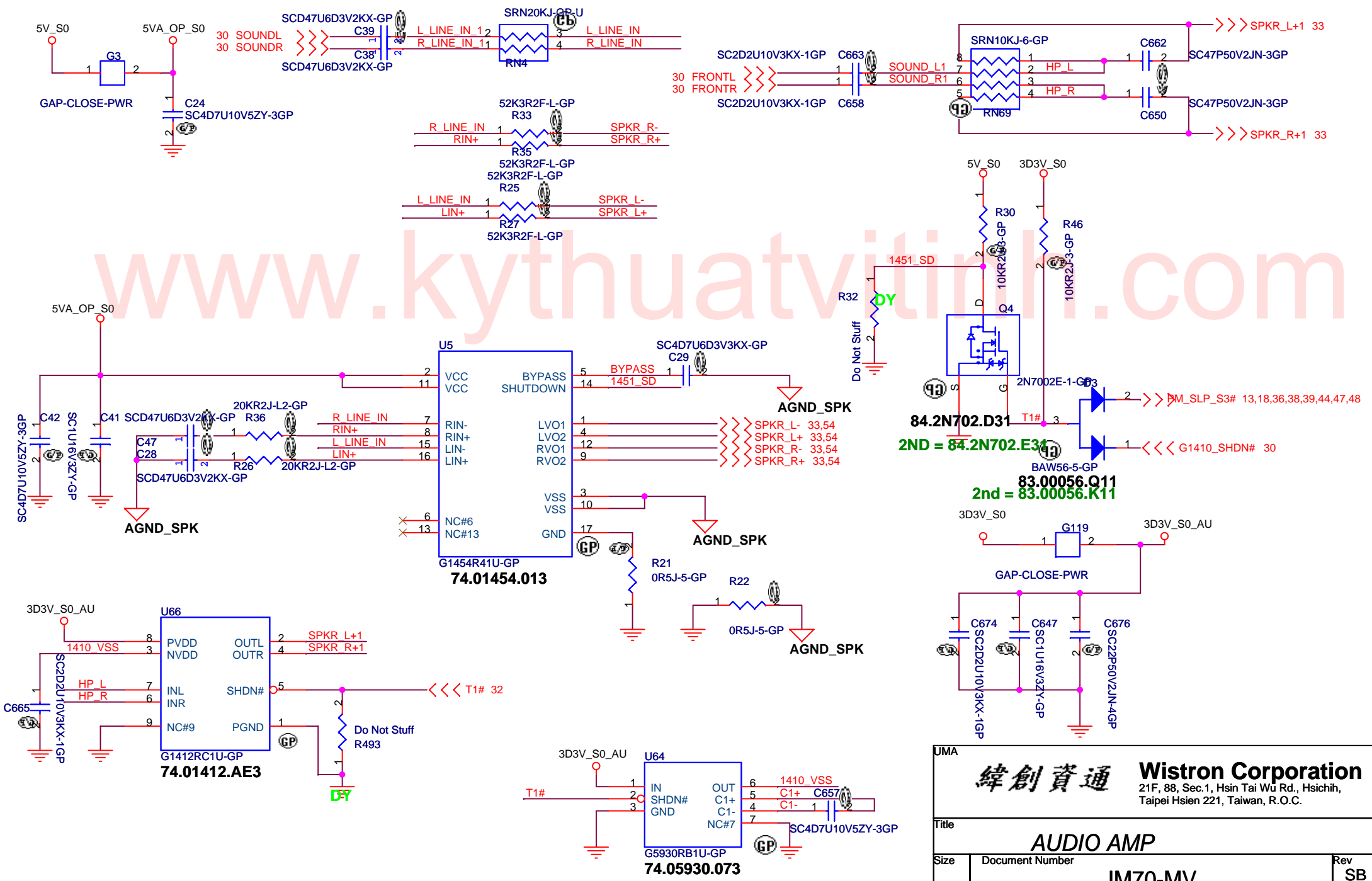
UMA

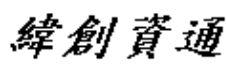
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

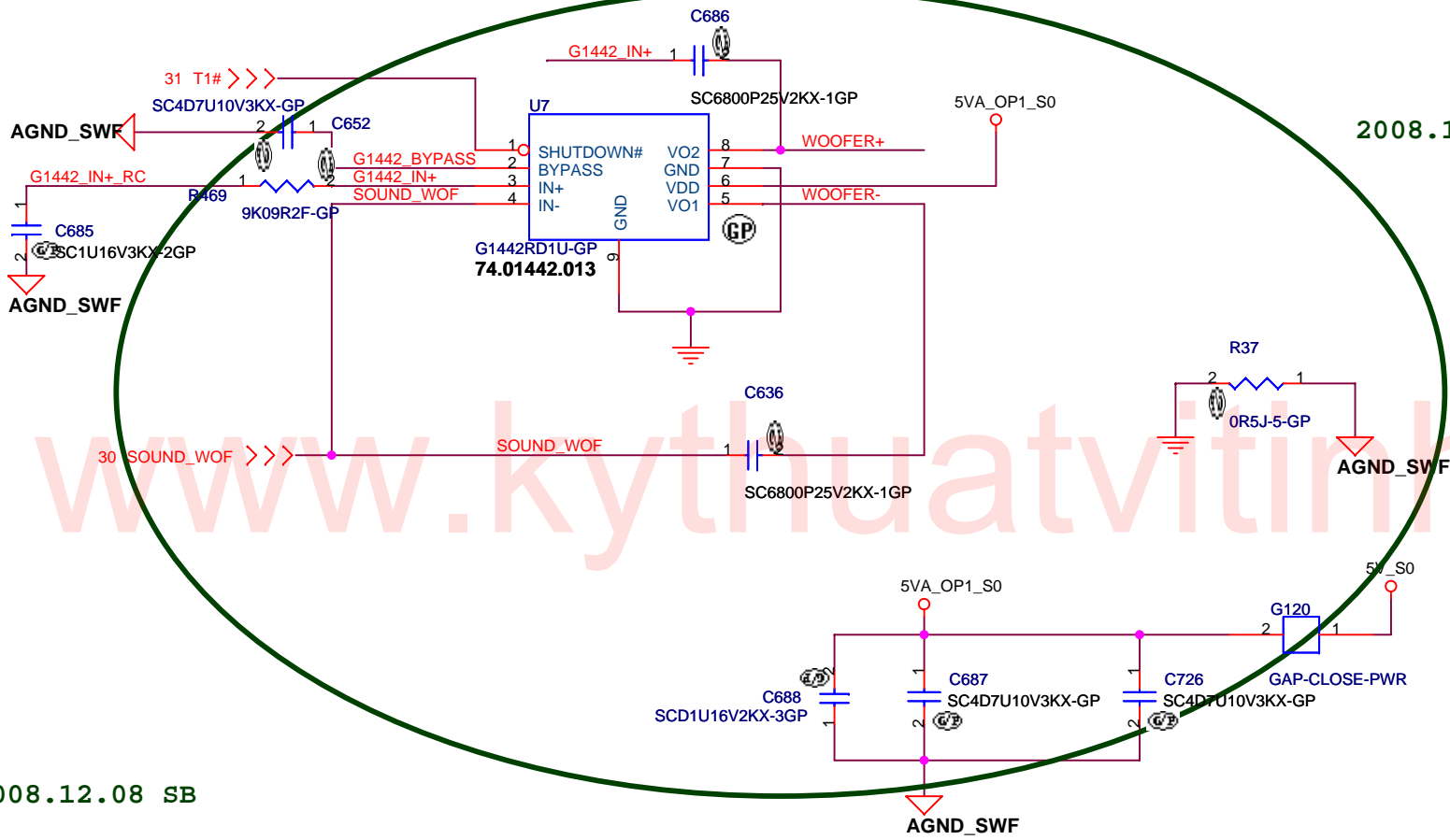
Title: **Azalia codec ALC888**

Size A3	Document Number JM70-MV	Rev SB
Date: Saturday, December 20, 2008	Sheet 30	of 55

AUDIO OP AMPLIFIER



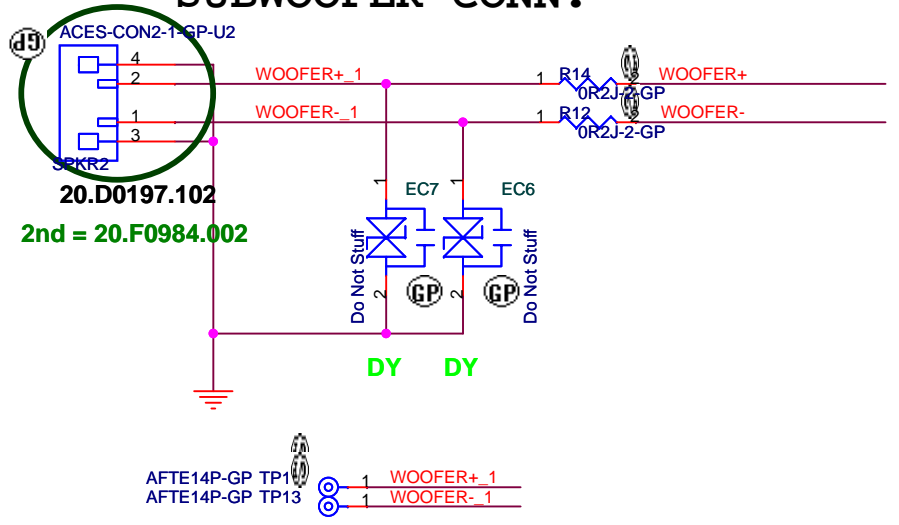
 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
AUDIO AMP	
Size	Document Number
JM70-MV	
Date	Rev
Saturday, December 20, 2008	SB
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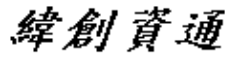


2008.12.14 SB

2008.12.08 SB

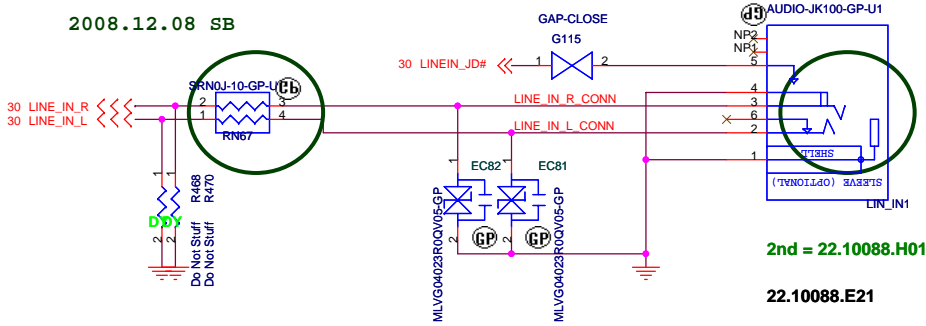
SUBWOOFER CONN.



UMA	
 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
SUBWOOFER CONN.	
Size	Document Number
JM70-MV	
Date: Saturday, December 20, 2008	Rev SB
Sheet 32	of 55

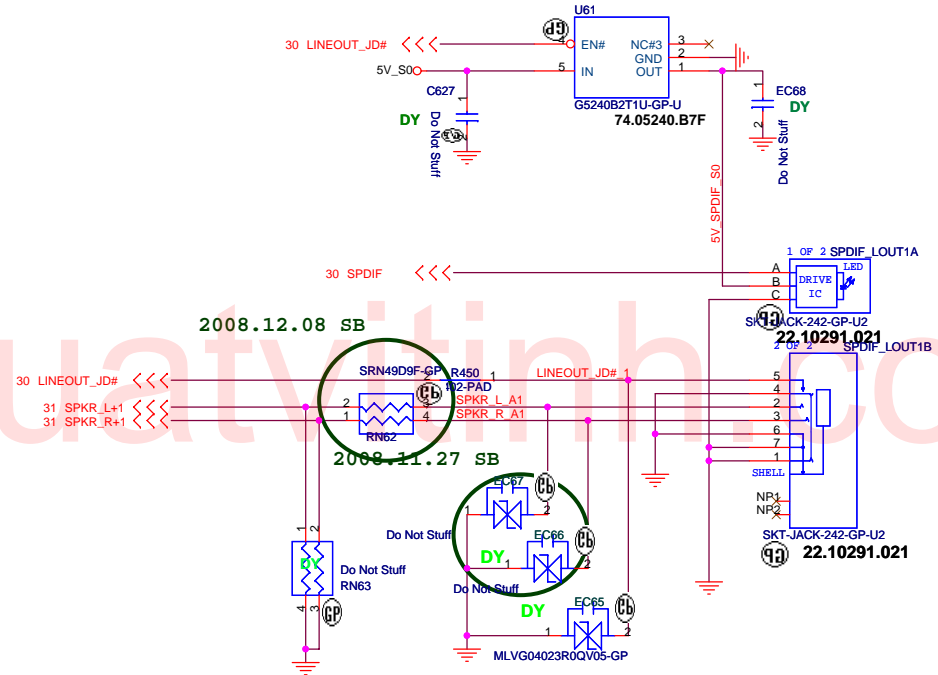
LINE IN

2008.12.08 SB



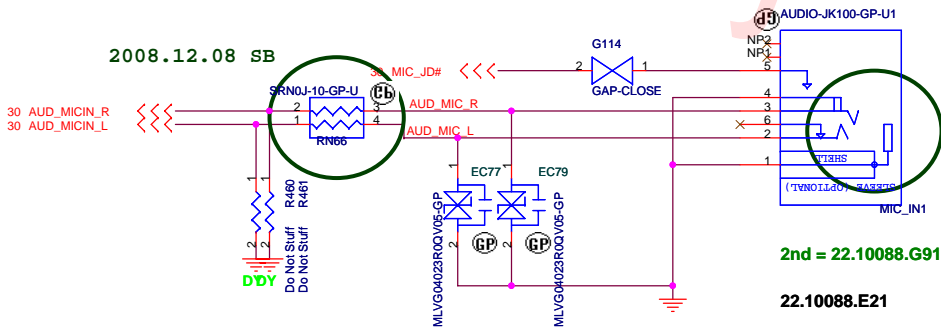
LINE OUT / SPDIF

2008.12.08 SB



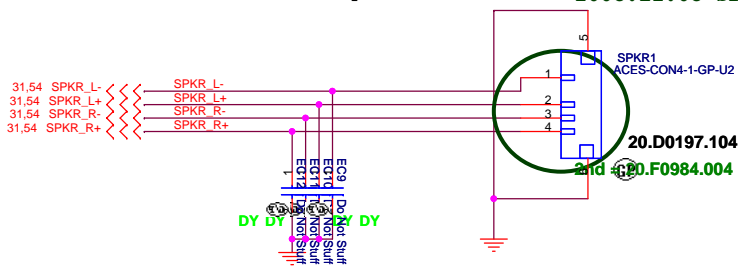
MIC IN

2008.12.08 SB



Internal Speaker

2008.12.08 SB

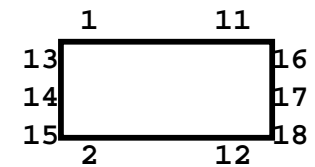
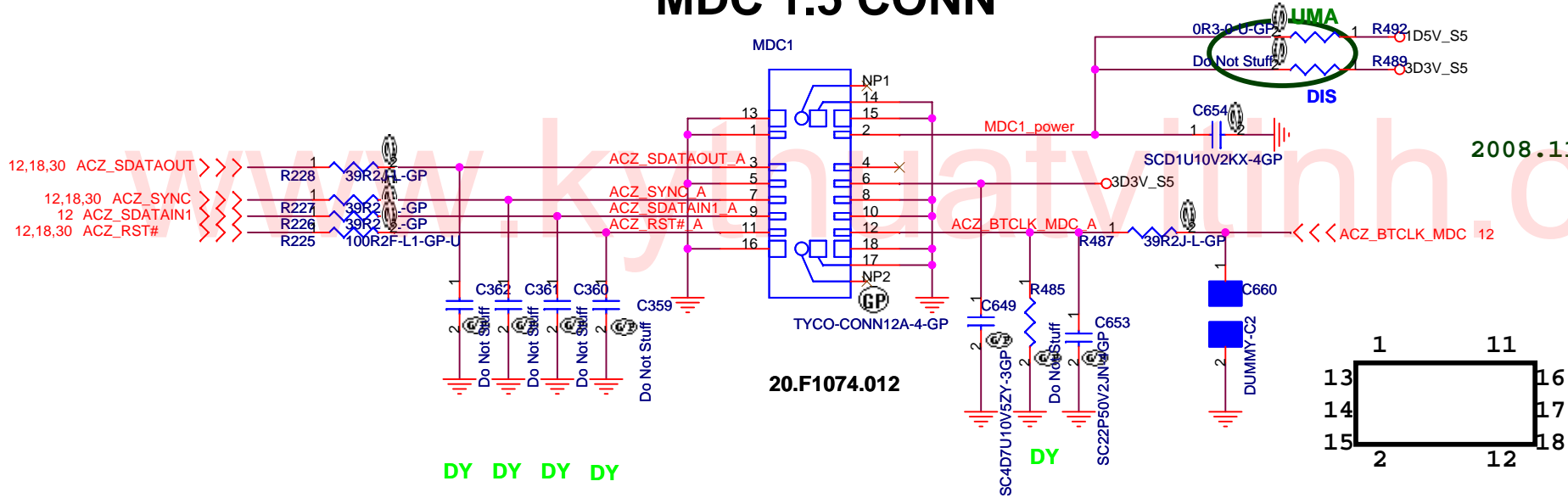


UMA


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Taipei Hsien 221, Taiwan, R.O.C.

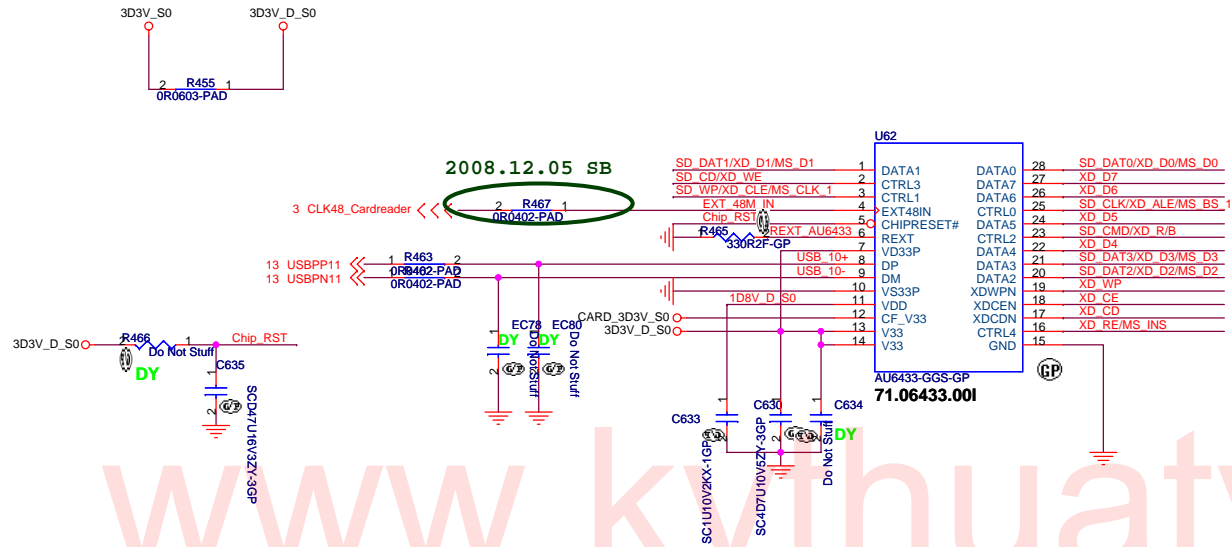
Title		
AUDIO jack		
Size	Document Number	Rev
	JM70-MV	SB
Date: Saturday, December 20, 2008	Sheet 33 of 55	

MDC 1.5 CONN



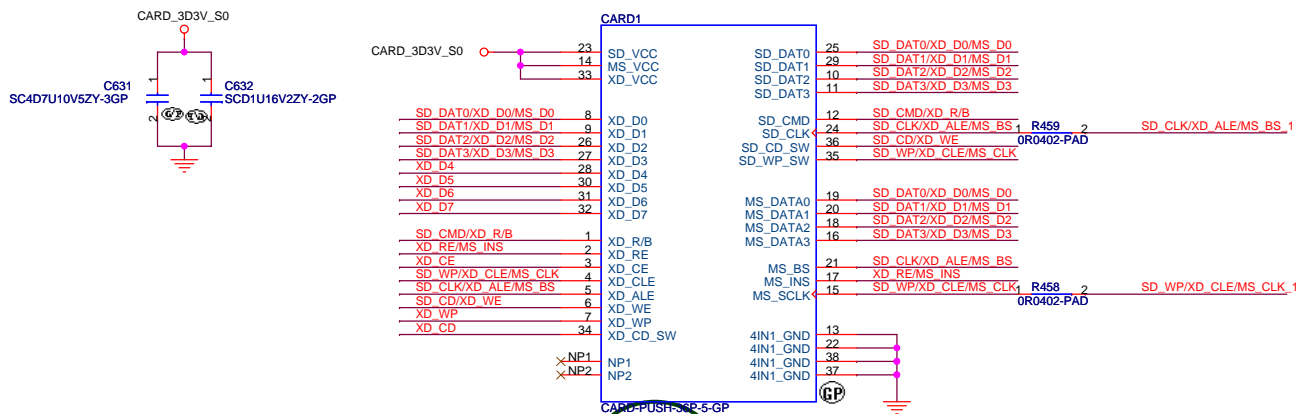
UMA

 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
MDC	
Size	Document Number
	JM70-MV
Date: Saturday, December 20, 2008	Rev SB
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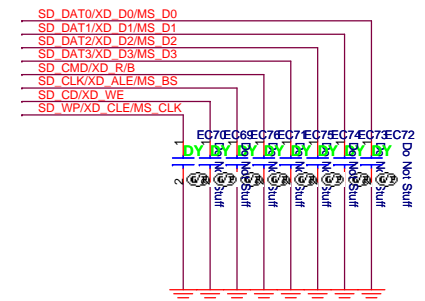
www.kyathuatvithinh.com

5 IN1 CARD-READER (SD/MMC/MS/MS PRO/XD)



2nd = 20.10079.011
20.10081.011

EMI capacitor

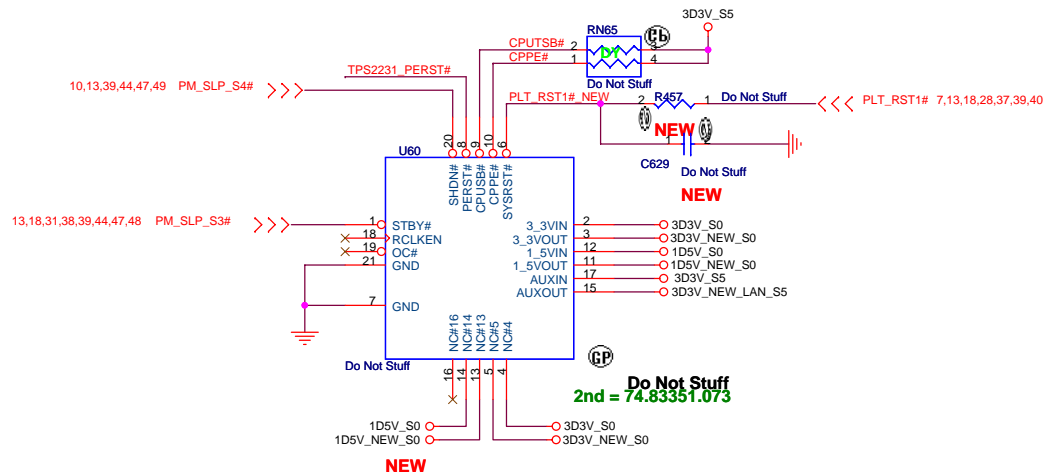
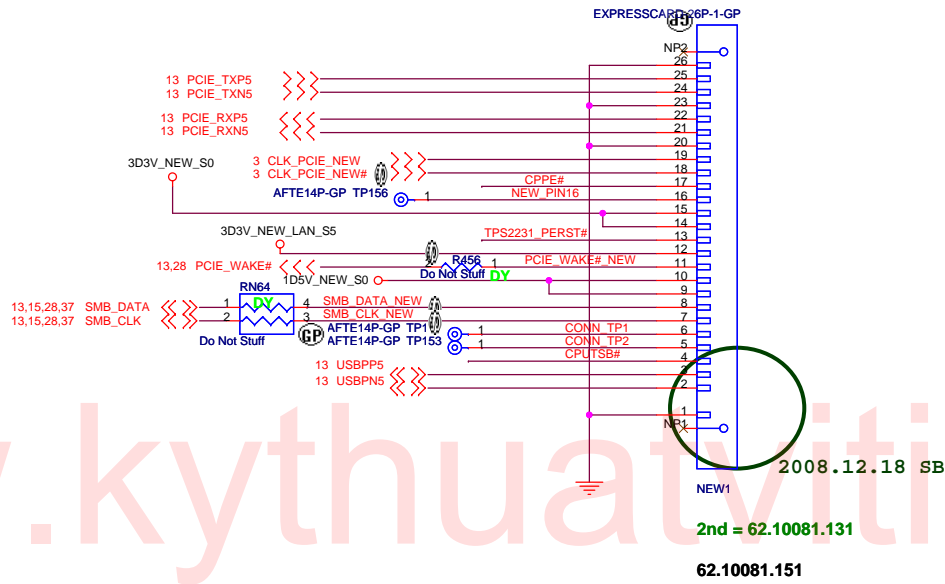


UMA

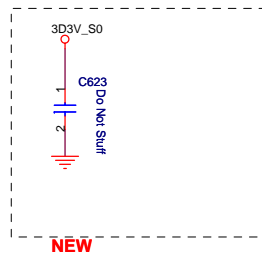
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Cardreader**

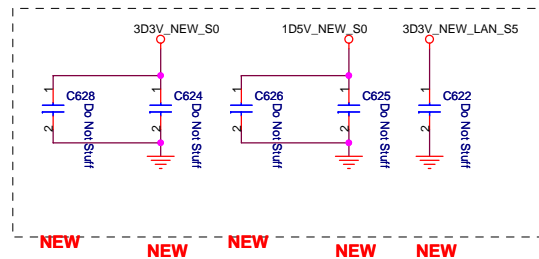
Size	Document Number	Rev
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Date: Saturday, December 20, 2008	Sheet 35 of 55	



Place them Near to Chip



Place them Near to Connector



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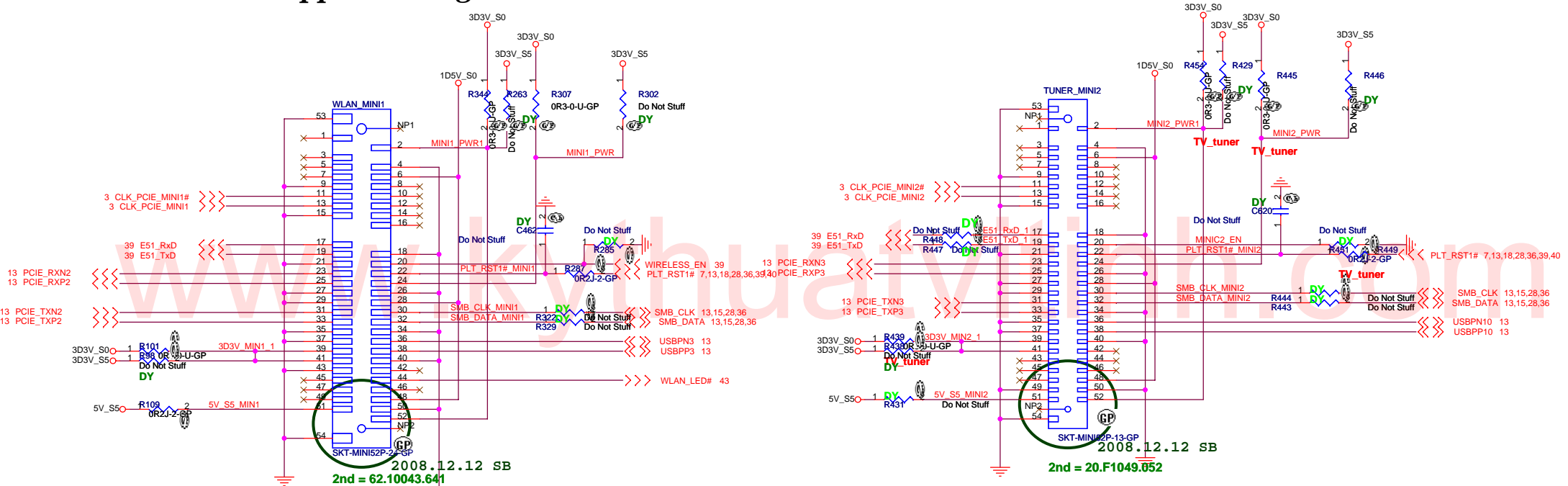
Title: **NEW CARD**

Size	Document Number	Rev
	JM70-MV	SB

Date: Saturday, December 20, 2008 Sheet 36 of 55

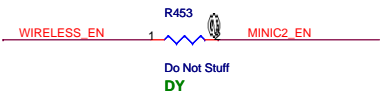
Mini1 Card Connector(WLAN) Support debug-card

Mini2 Card Connector(TV tuner)

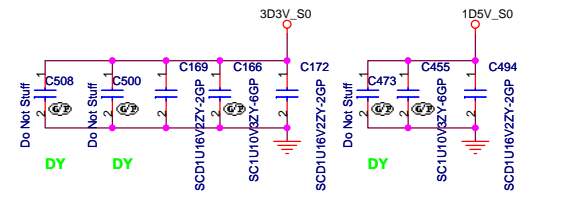


2008.12.12 SB
2nd = 62.10043.641
62.10043.611

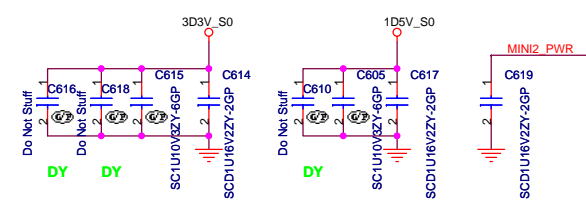
2008.12.12 SB
2nd = 20.F1049.652
62.10043.461



Place near MINI1



Place near MINIC2



UMA

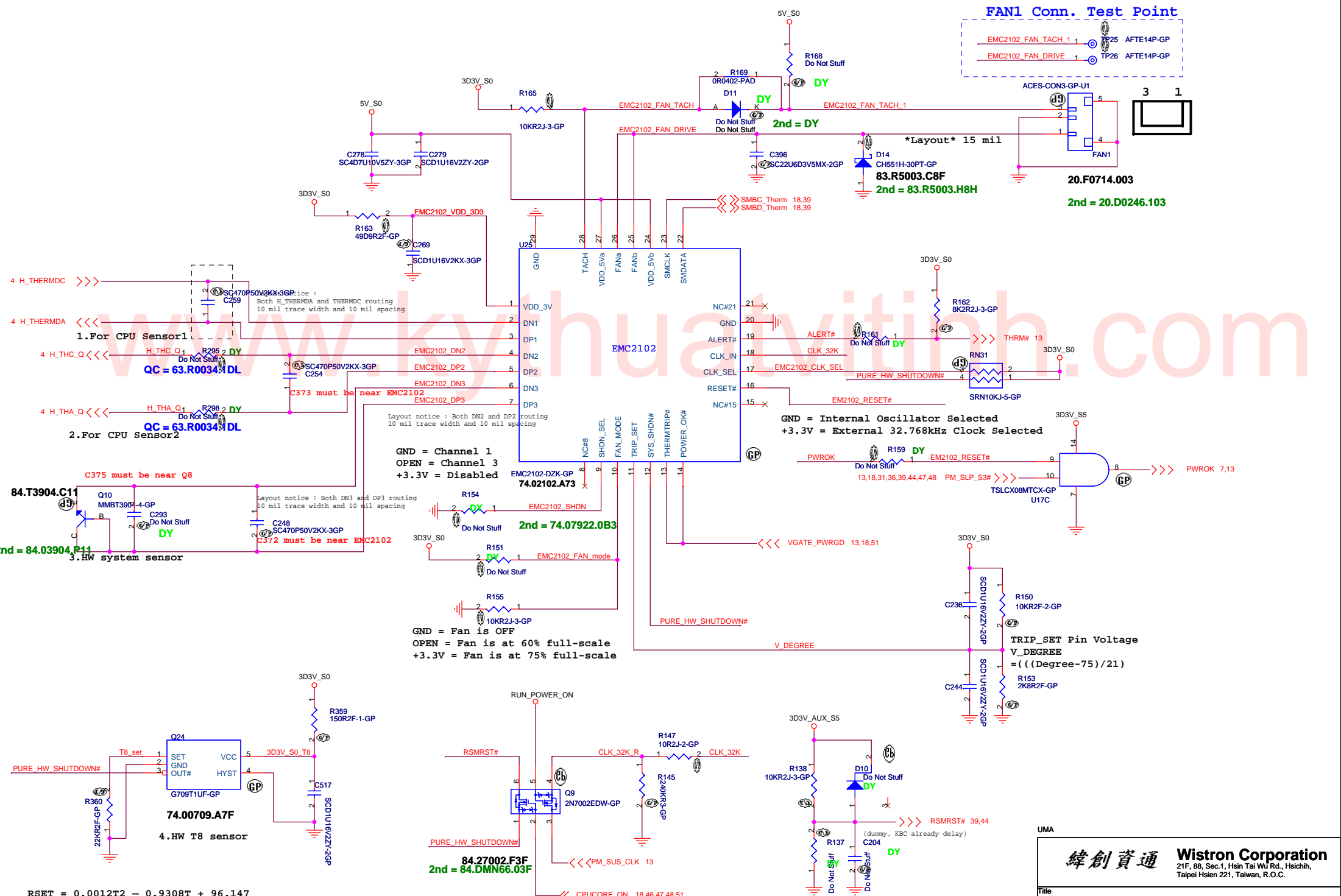
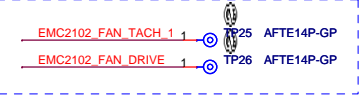
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **MINI CARD**

Size A3	Document Number JM70-MV	Rev SB
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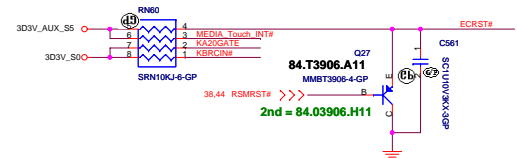
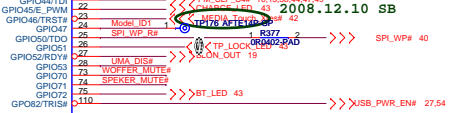
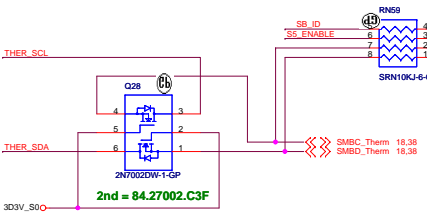
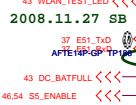
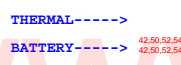
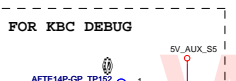
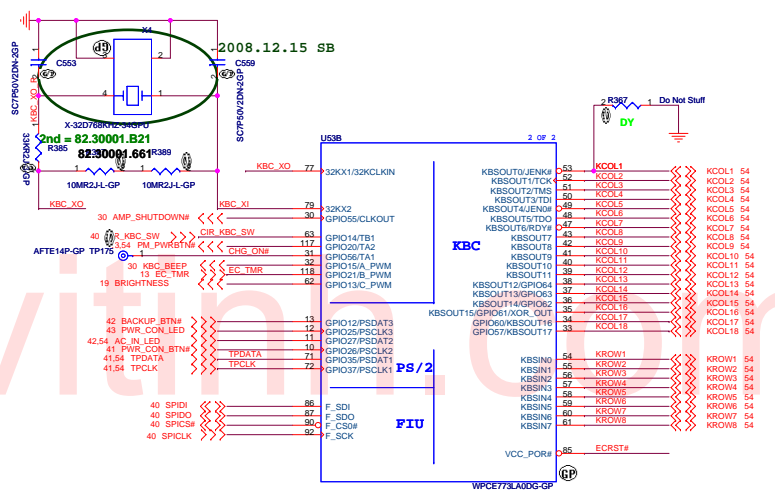
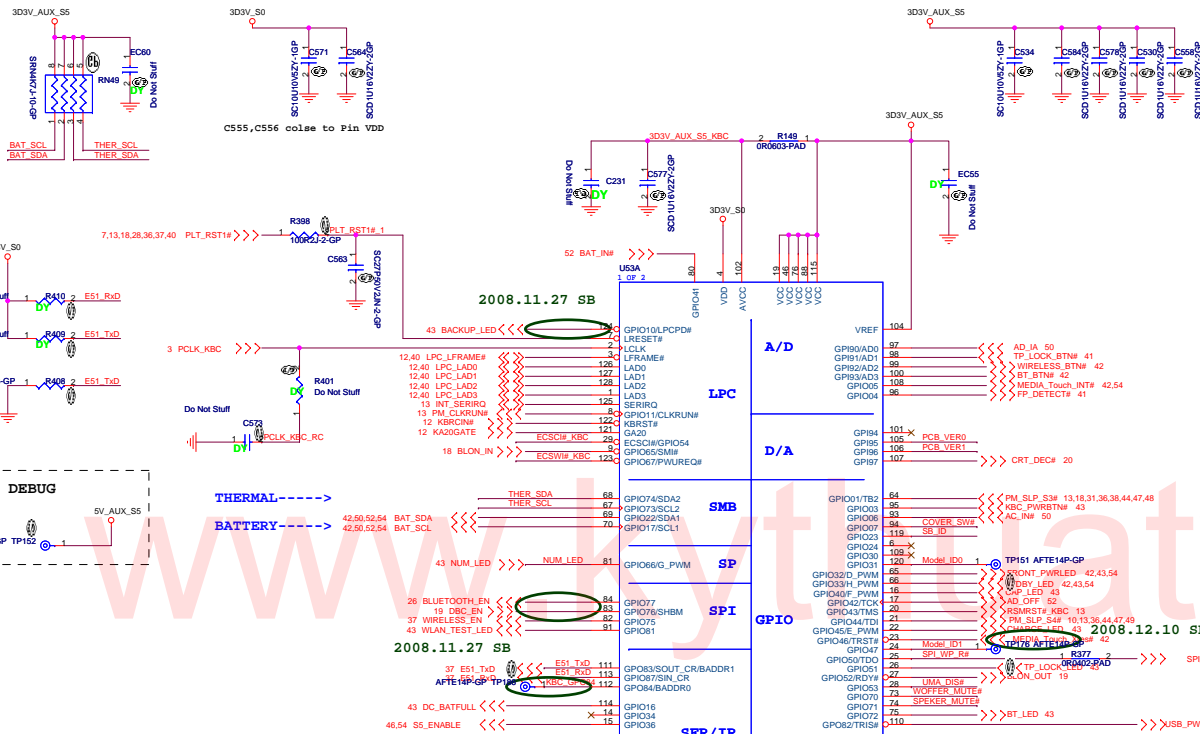
Date: Saturday, December 20, 2008 Sheet 37 of 55

FAN1 Conn. Test Point

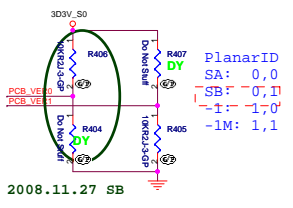
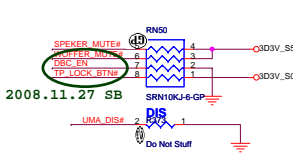
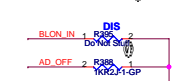
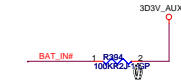
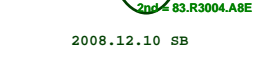
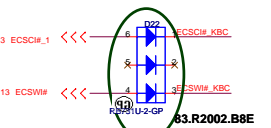
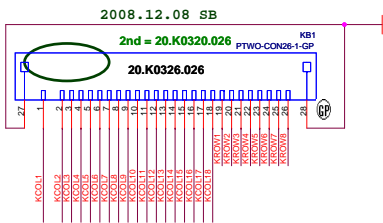


RSET = 0.0012T2 - 0.9308T + 96.147
T8 setting 90 degree

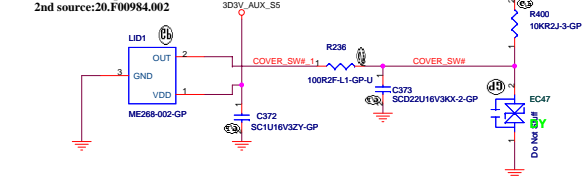
Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Thermal/Fan Controller	
Size	Document Number
JM70-MV	
Date: Saturday, December 20, 2008	Sheet 38 of 55



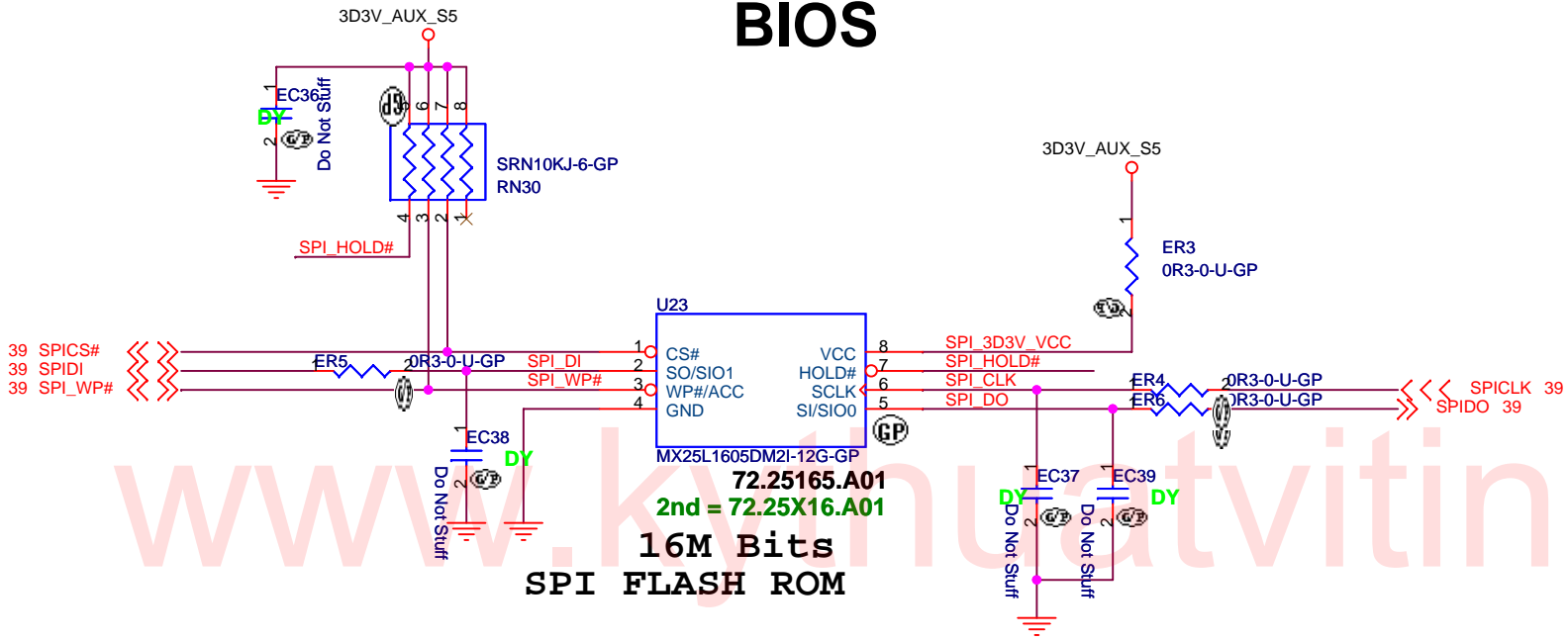
Internal Keyboard Connector



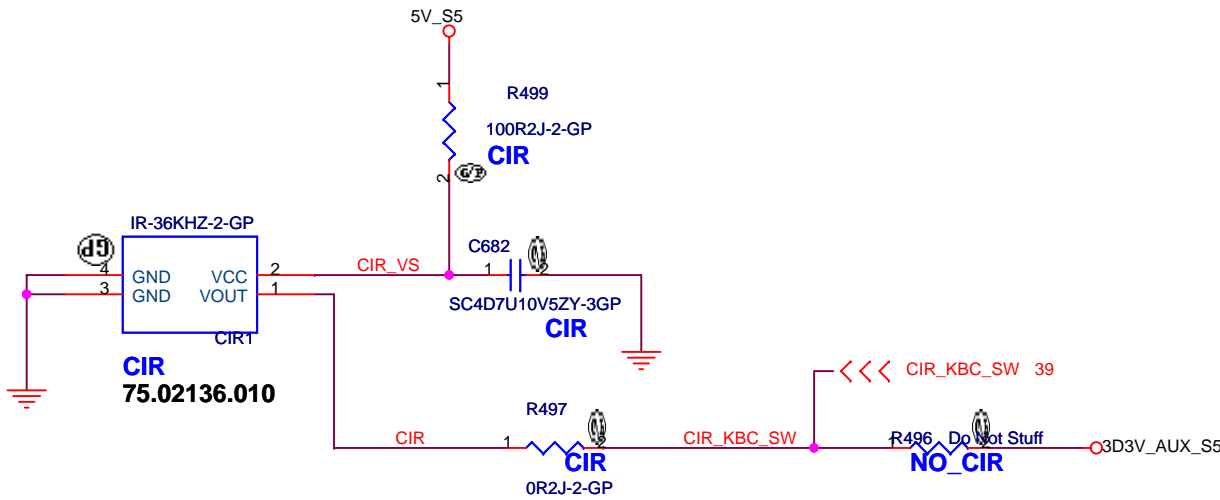
Cover Up Switch



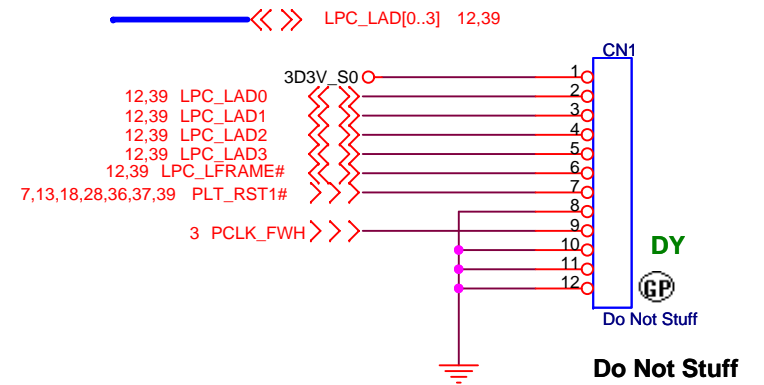
BIOS




VISHAY CIR Module



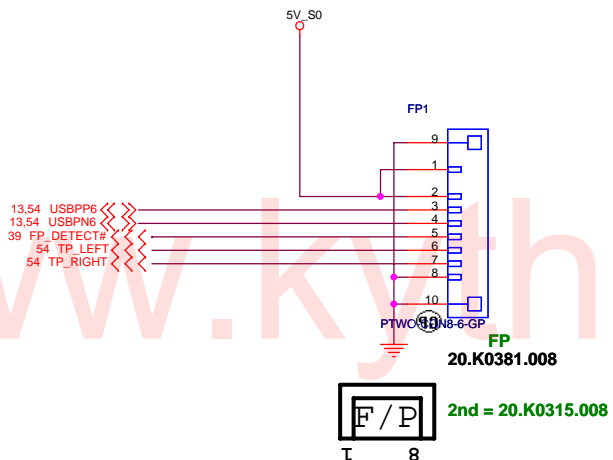
GOLDEN FINGER FOR DEBUG BOARD



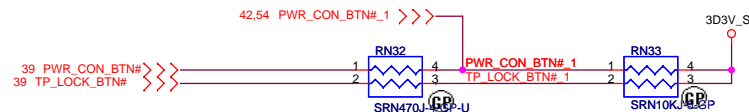
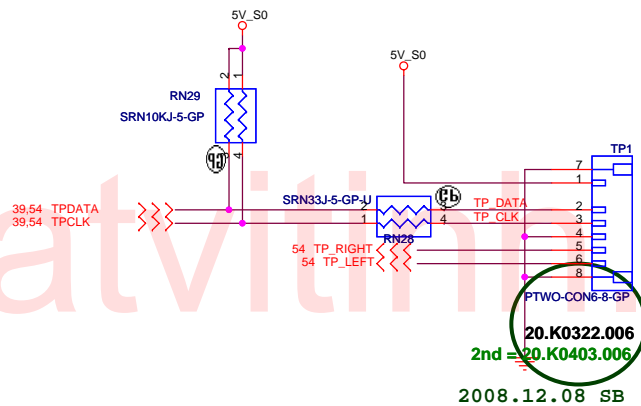
UMA

 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
BIOS		
Size	Document Number	Rev
	JM70-MV	SB
Date: Saturday, December 20, 2008		Sheet 40 of 55

Finger printer

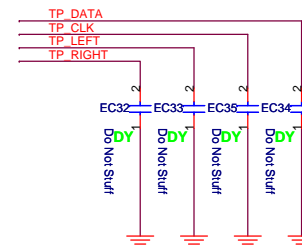
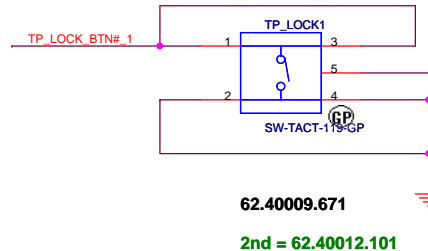


Touch Pad



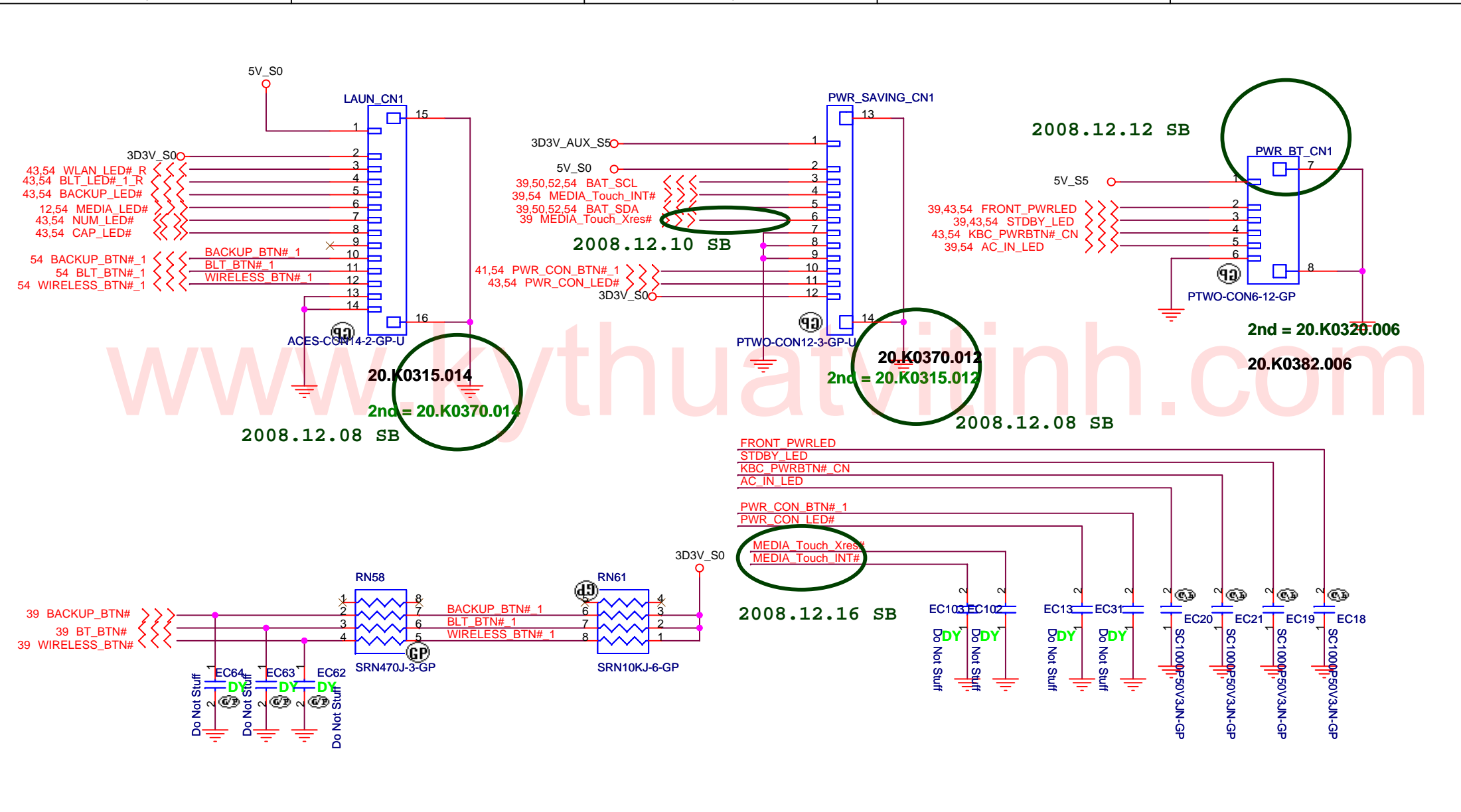
TP_LOCK key

Note. main with 2nd symbol pin define different



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Title			
Touch PAD and FP			
Size	Document Number		Rev
	JM70-MV		SB
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2008.12.08 SB

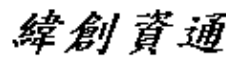
2008.12.10 SB

2008.12.08 SB

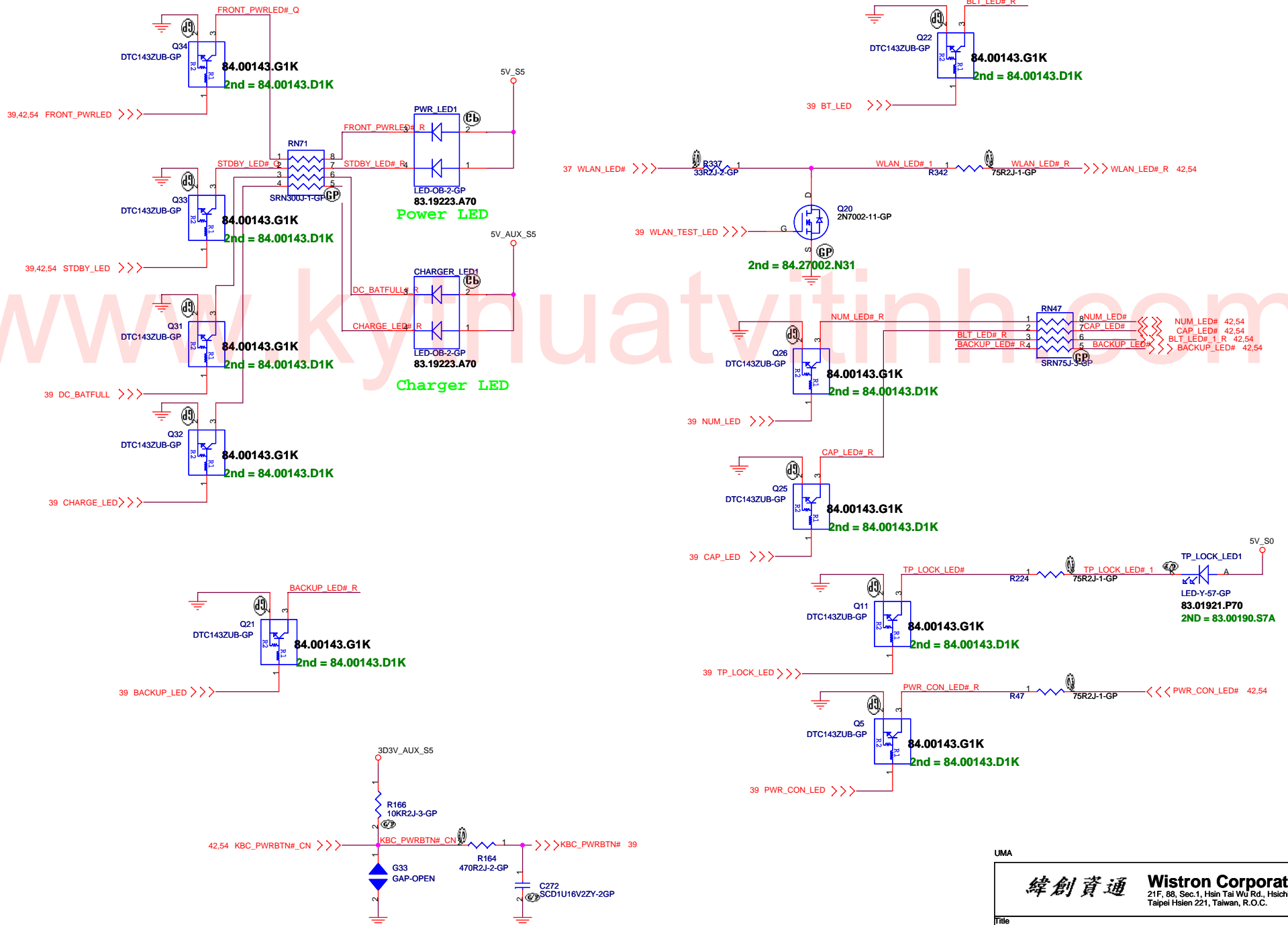
2008.12.12 SB

2008.12.16 SB

UMA

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Title Launch CN		
Size A4	Document Number JM70-MV	Rev SB
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LED



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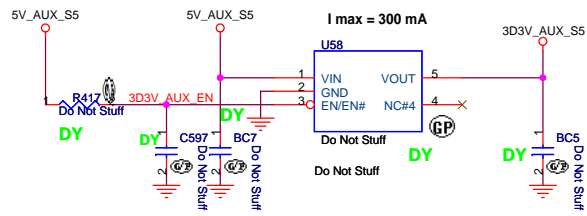
Title: **LED&POWERBD CONN**

Size: Document Number: **JM70-MV** Rev: SB

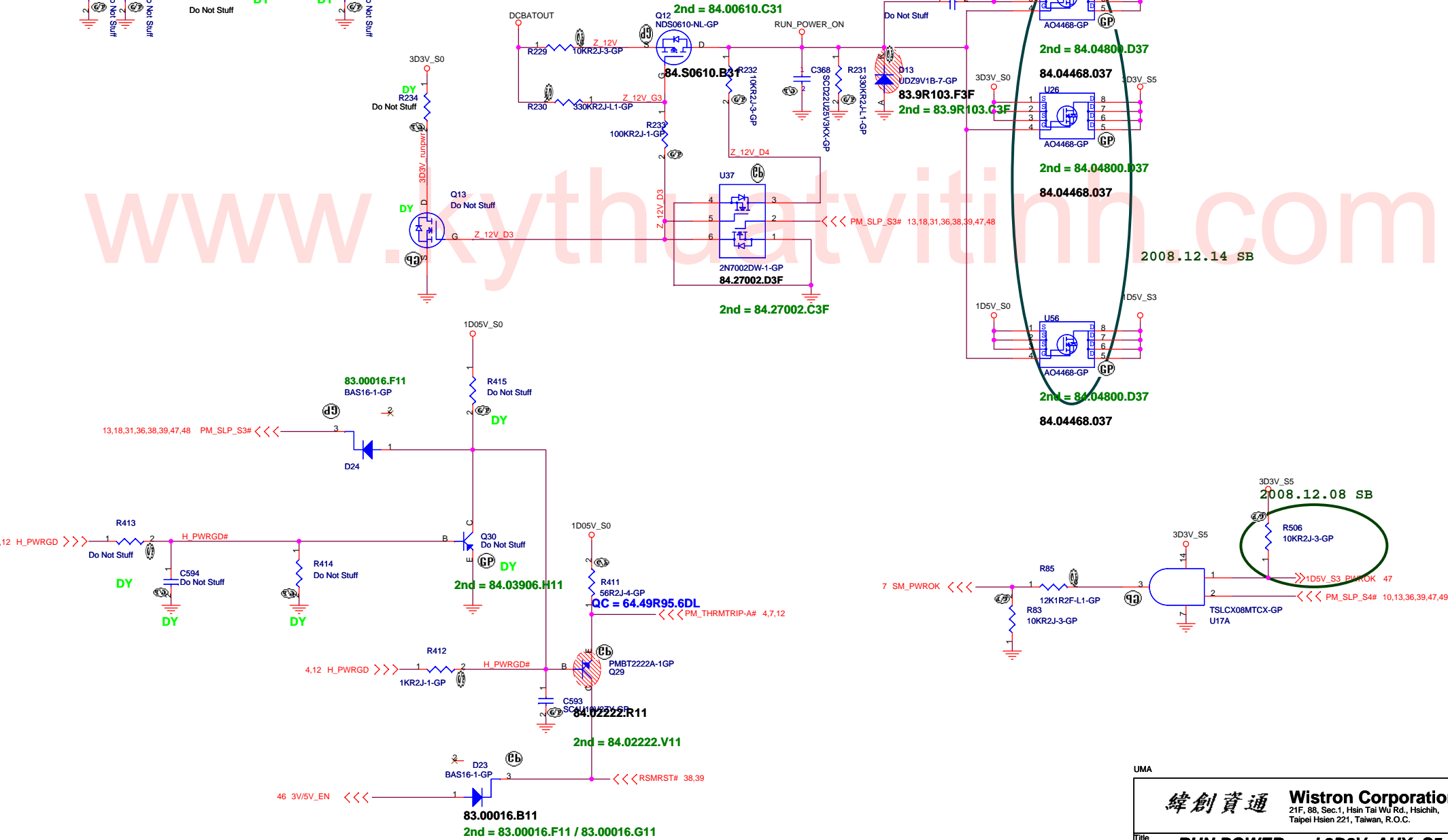
Date: Saturday, December 20, 2008 Sheet 43 of 55

Aux Power

3D3V_AUX_S5



Run Power



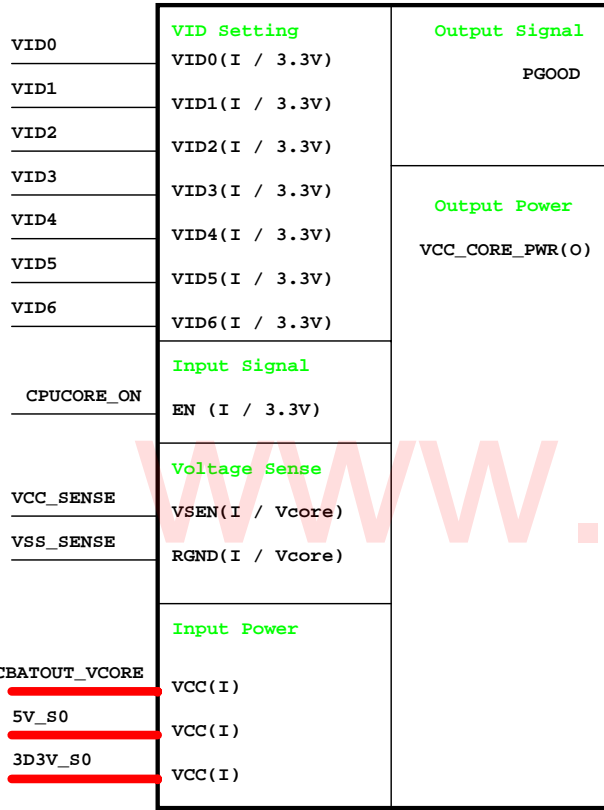
www.kyathvith.com

2008.12.14 SB

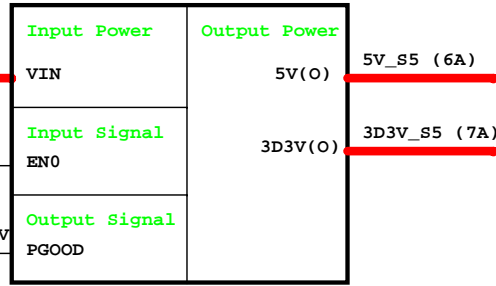
2008.12.08 SB

UMA	
Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
RUN POWER and 3D3V_AUX_S5	
Title	
Size	Document Number
JM70-MV	
Date:	Saturday, December 20, 2008
Sheet	44 of 55
Rev	SB

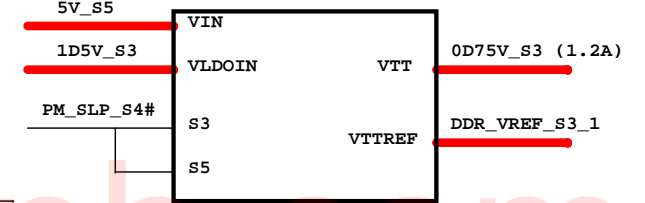
CPU_CORE
ADP3208C



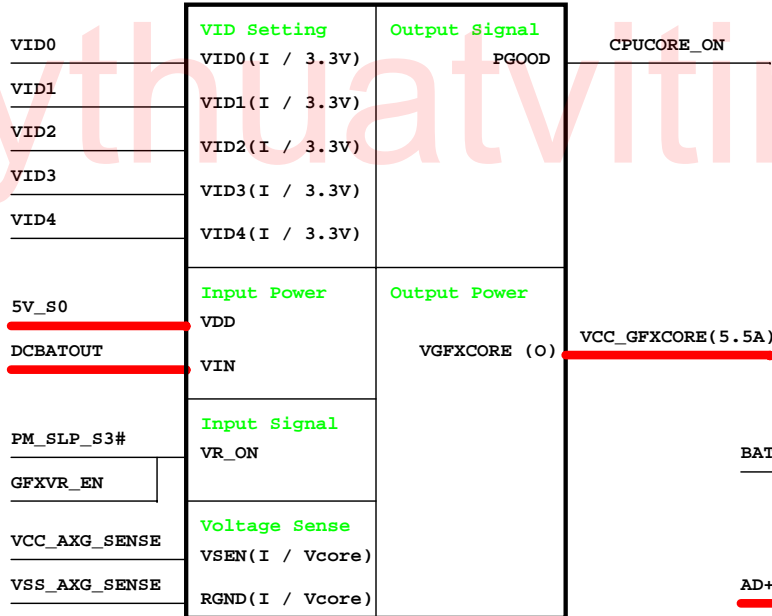
ISL62392
5V/3D3V



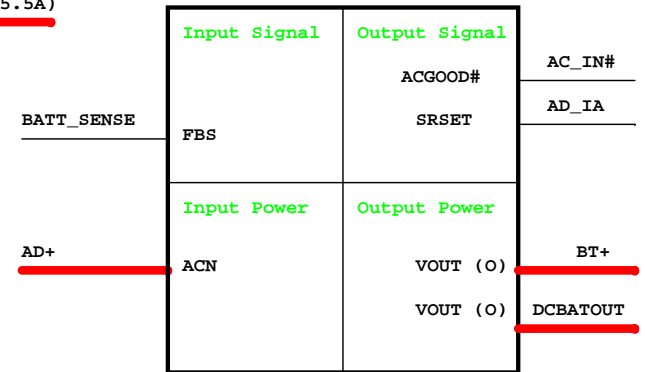
DDR 3.0
RT9026 0D75V_S0



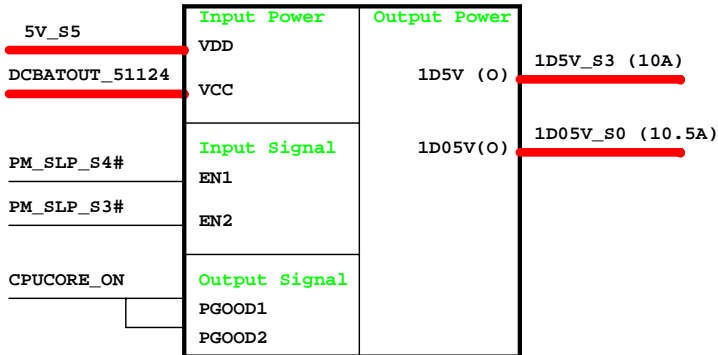
GFX_CORE
ISL6263A



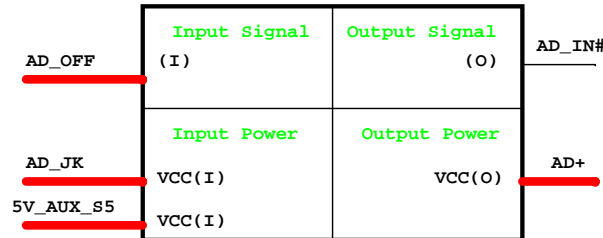
Charger ISL88731A



TPS51124
1D5V/1D05V

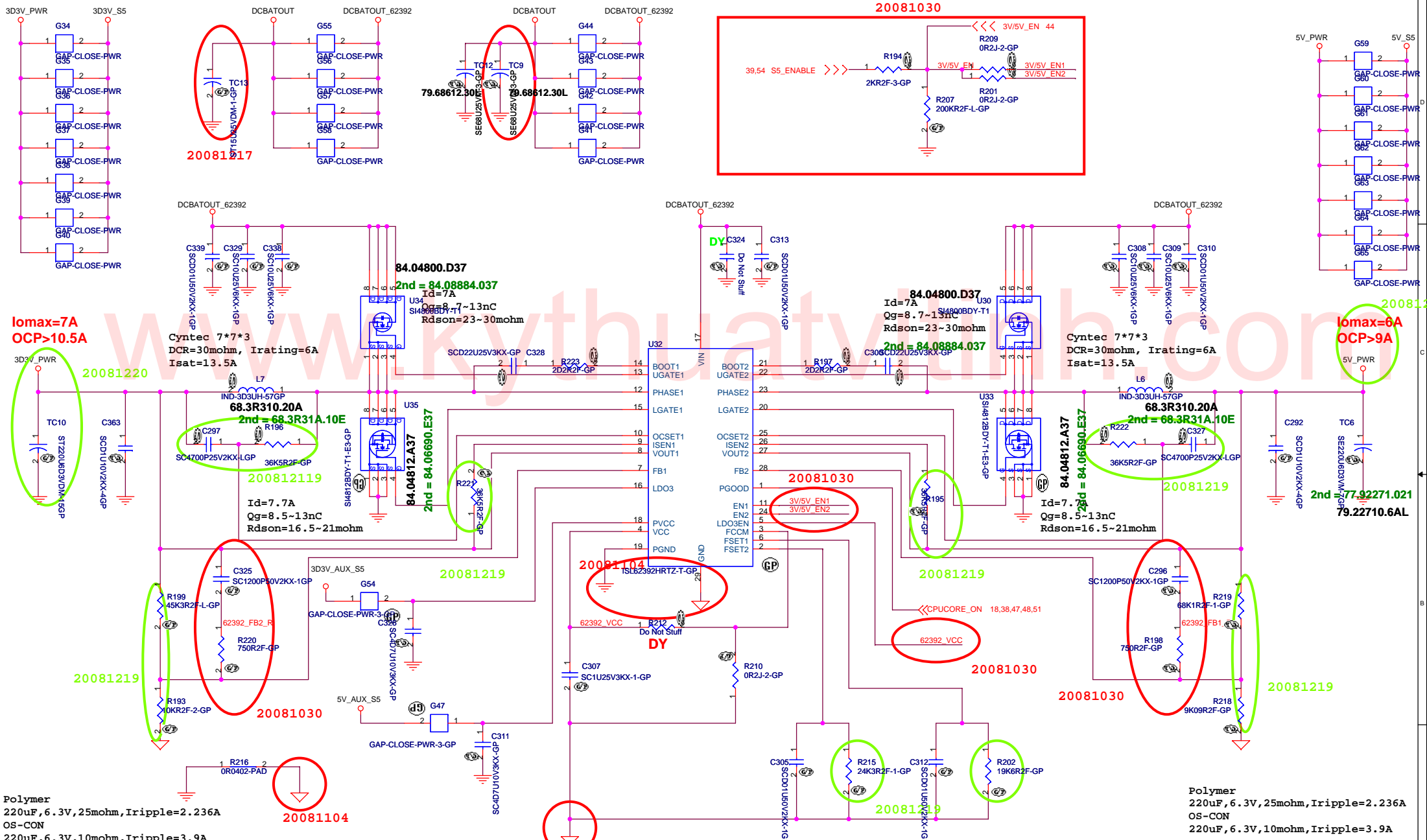


Adapter



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Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Block Diagram**
Size B Document Number: **JM70-MV** Rev SB
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**Iomax=7A
OCP>10.5A**

**Iomax=6A
OCP>9A**

Polymer
220uF, 6.3V, 25mohm, Irripple=2.236A
OS-CON
220uF, 6.3V, 10mohm, Irripple=3.9A

Polymer
220uF, 6.3V, 25mohm, Irripple=2.236A
OS-CON
220uF, 6.3V, 10mohm, Irripple=3.9A

$$V_{out} = 0.6 * (1 + R1/R2)$$

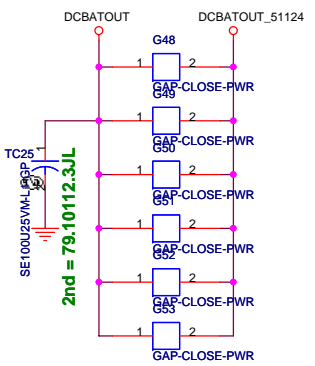
UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **ISL62392 5V/3D3V**

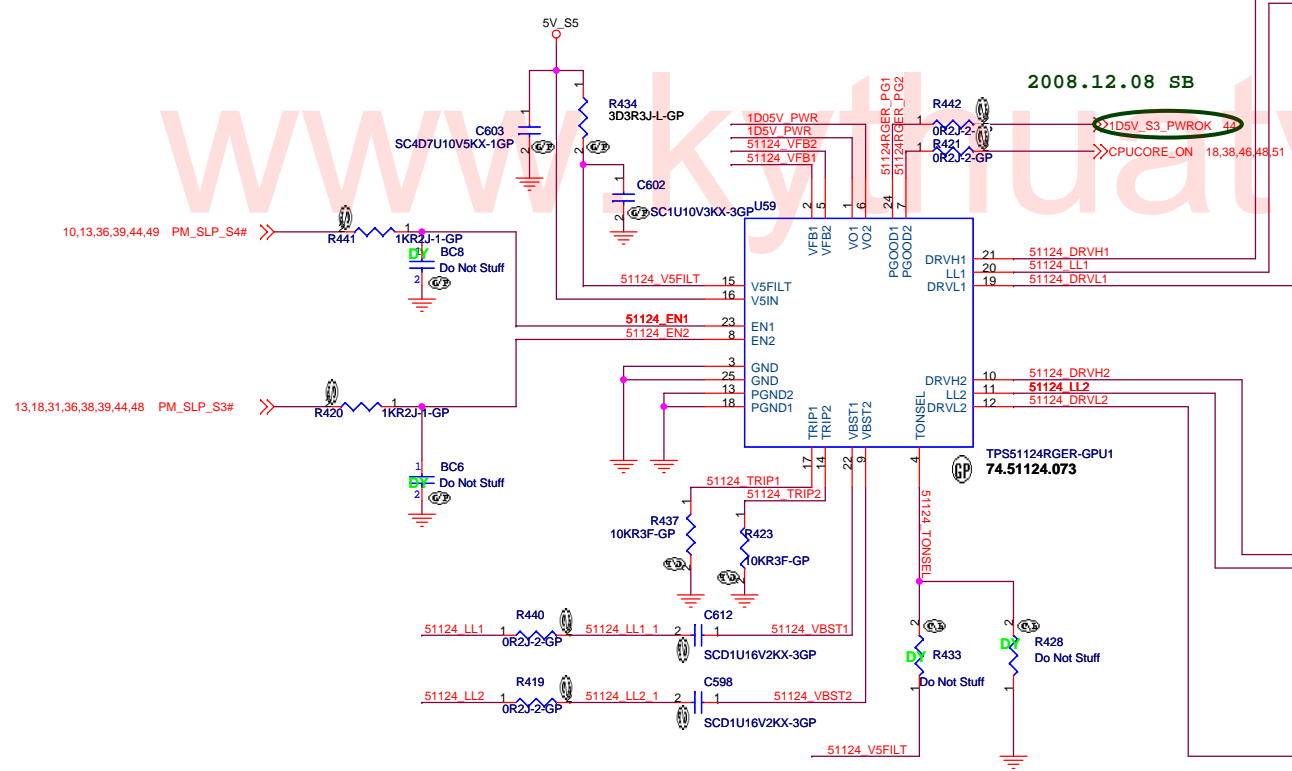
Size A3 Document Number **JM70-MV** Rev **SB**

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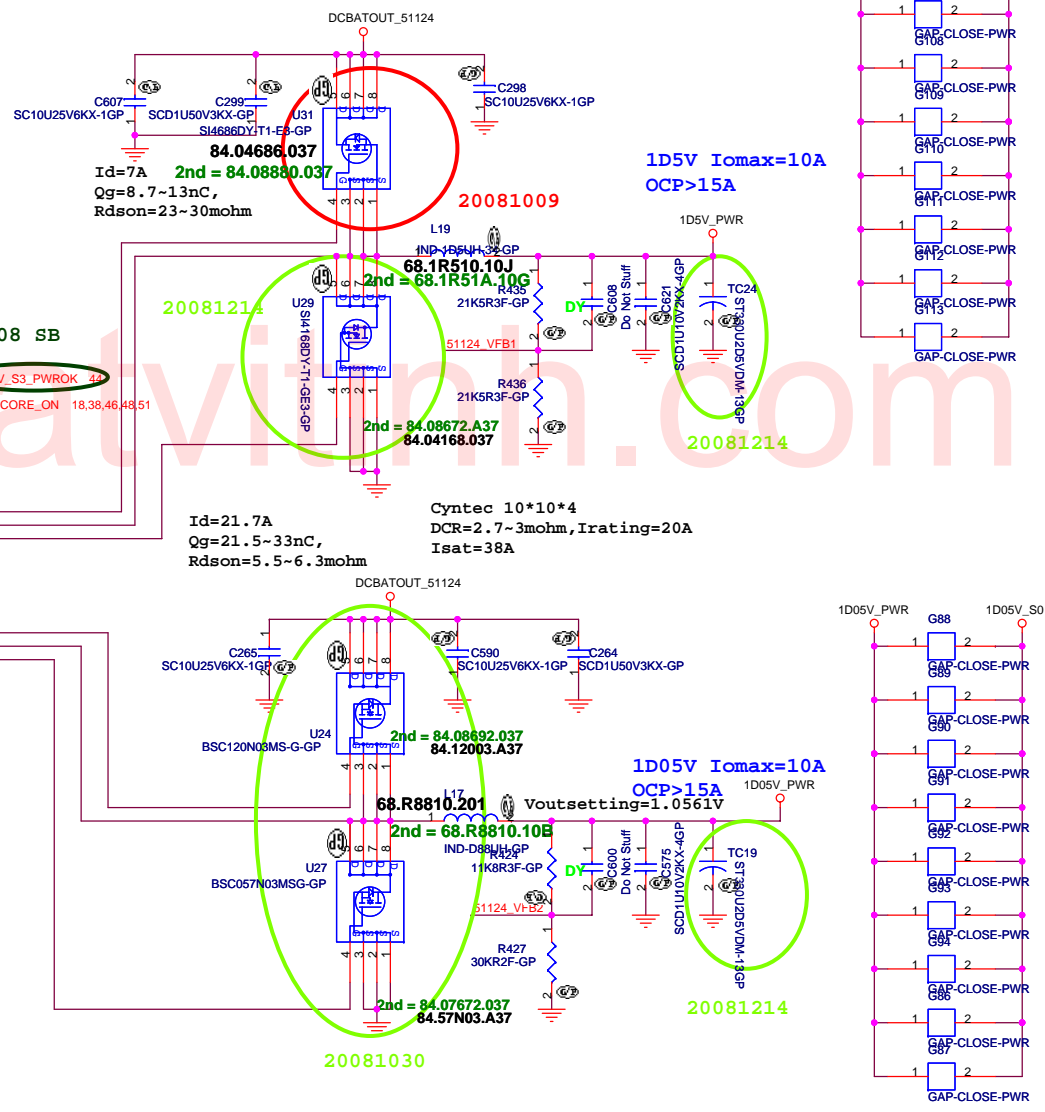
$$V_{trip}(mV) = R_{trip}(Kohm) * I_0(uA)$$

$$I_{ocp} = (V_{trip}/R_{dson}) + ((1/(2*L*f)) * ((V_{in}-V_{out}) * V_{out}) / V_{in})$$



	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

$V_{out} = 0.758V * (R1+R2) / R2$ --> PWM mode
 $V_{out} = 0.764V * (R1+R2) / R2$ --> Skip Mode



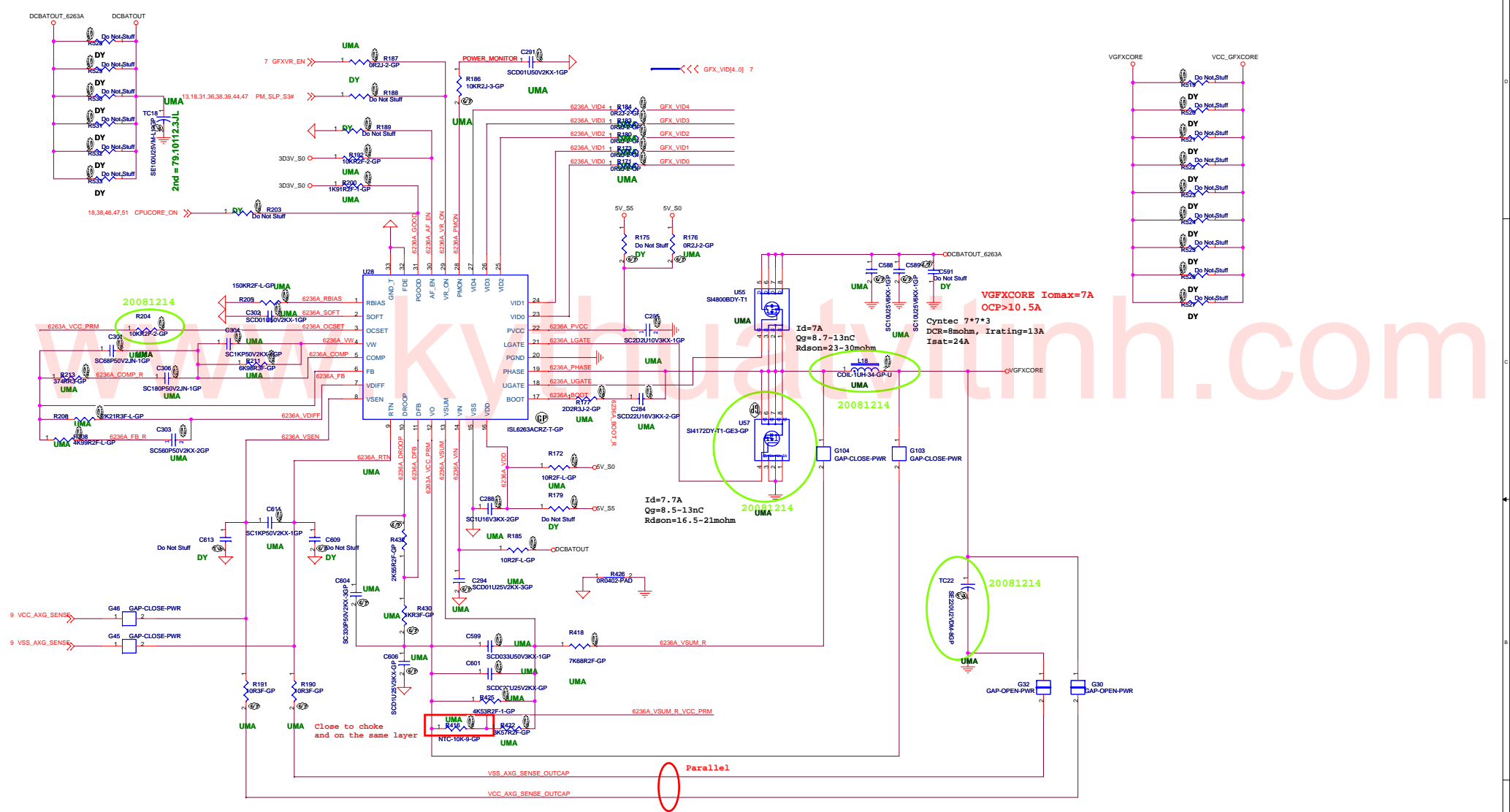
UMA

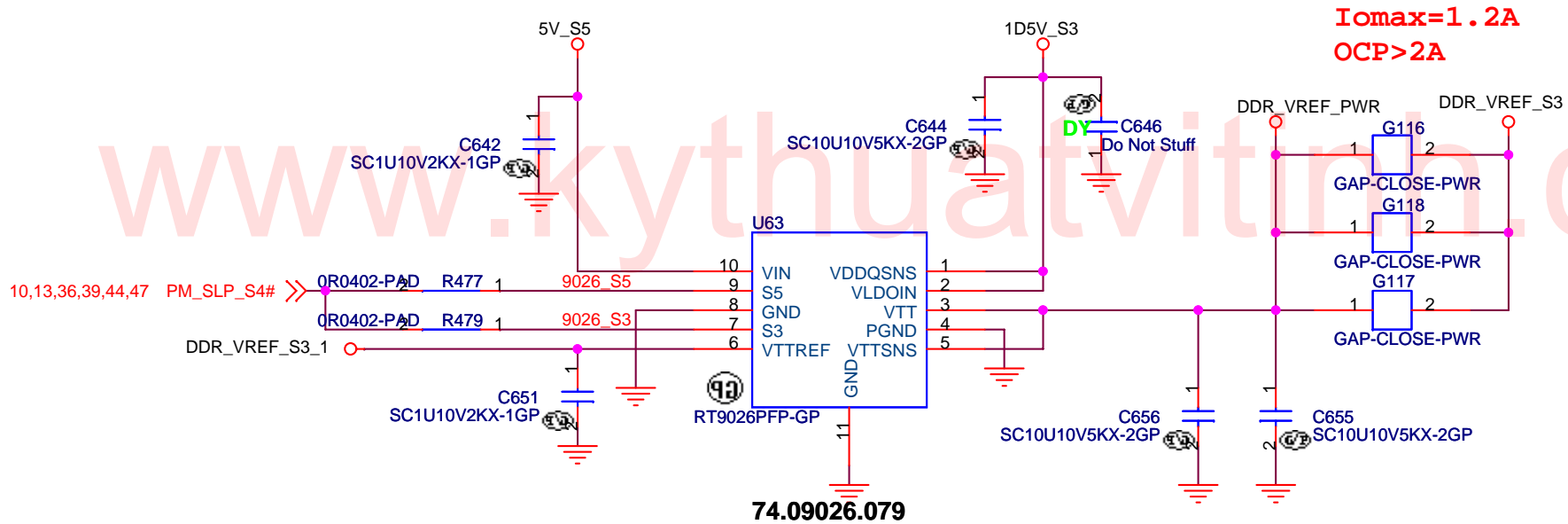
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Title: **TPS51124 1D5V 1D05V**

Size A3 Document Number **JM70-MV** Rev **SB**

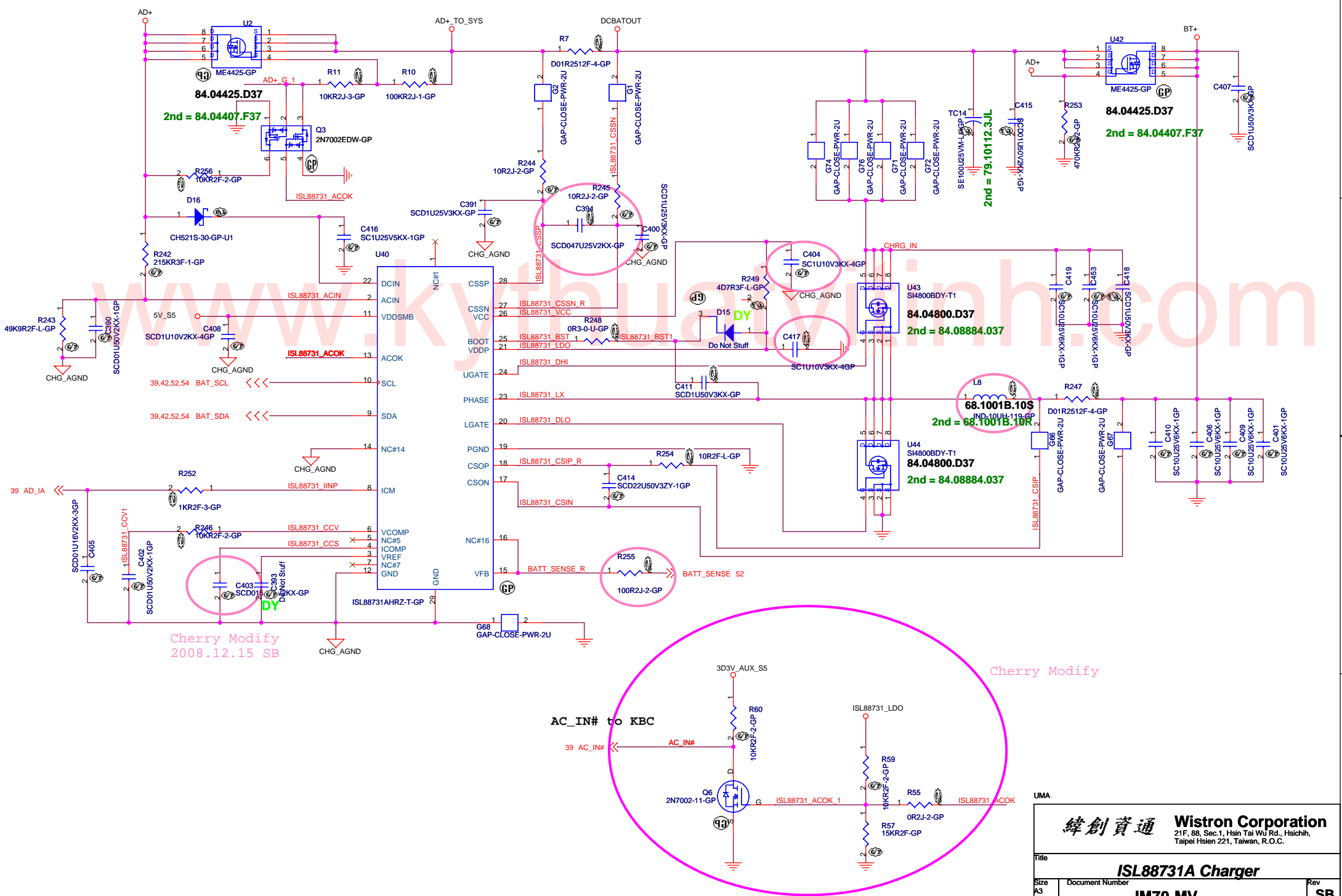
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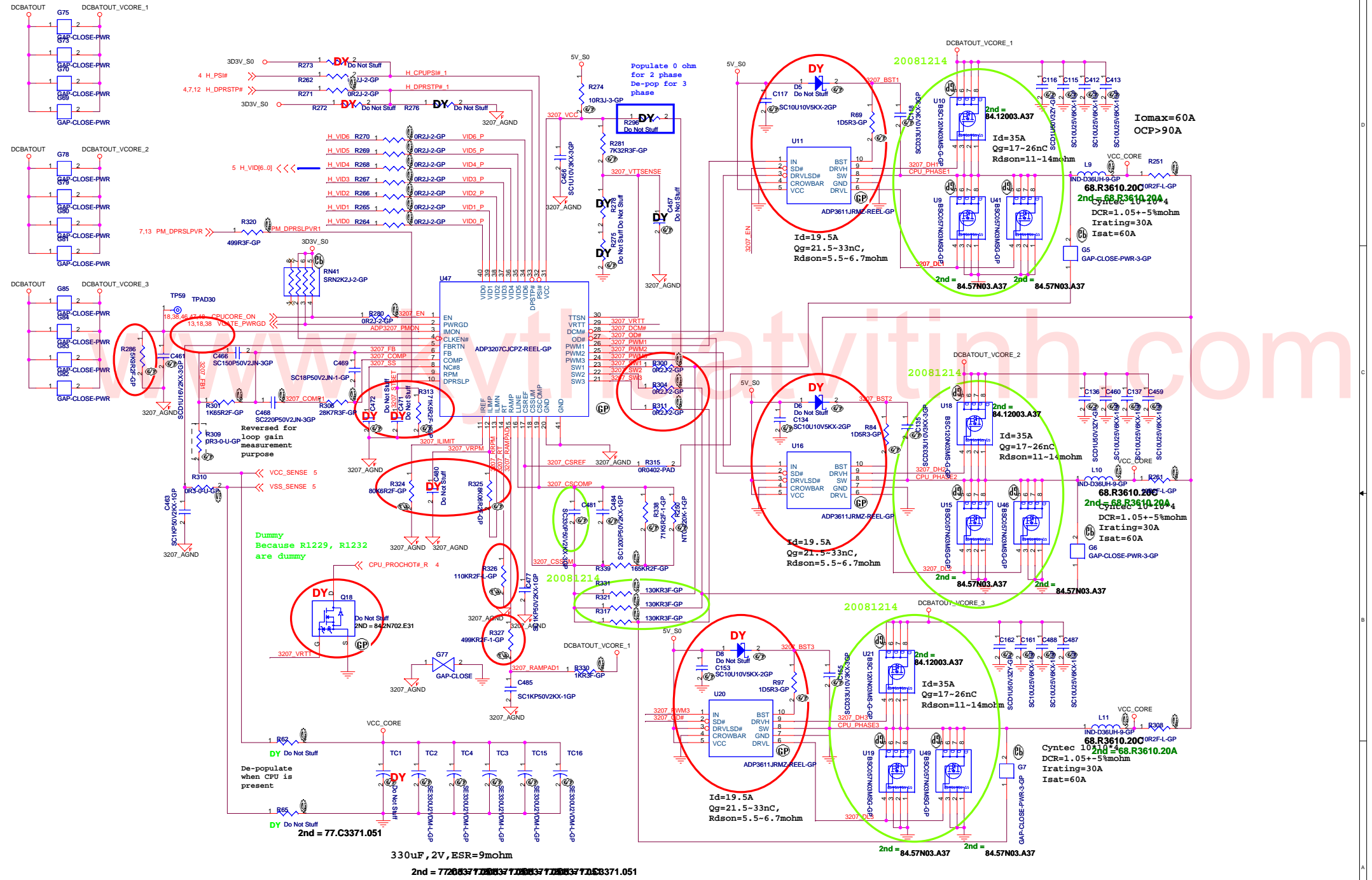




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Title	
0D75V	
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Dummy
Because R1229, R1232
are dummy

De-populate
when CPU is
present

330uF, 2V, ESR=9mohm
2nd = 77.C3371.051

ADP3611JRMZ-REEL-GP
Id=19.5A
Qg=21.5-33nC,
Rdson=5.5-6.7mohm

ADP3611JRMZ-REEL-GP
Id=19.5A
Qg=21.5-33nC,
Rdson=5.5-6.7mohm

ADP3611JRMZ-REEL-GP
Id=19.5A
Qg=21.5-33nC,
Rdson=5.5-6.7mohm

ADP3611JRMZ-REEL-GP
Id=19.5A
Qg=21.5-33nC,
Rdson=5.5-6.7mohm

ADP3611JRMZ-REEL-GP
Id=19.5A
Qg=21.5-33nC,
Rdson=5.5-6.7mohm

Cyntec 10.41
2nd = 68.R3610.20A
DCR=1.05+-5mohm
Irating=30A
Isat=60A

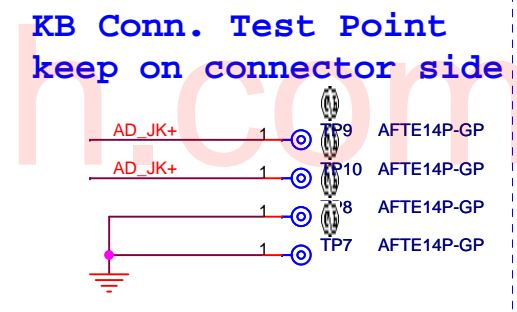
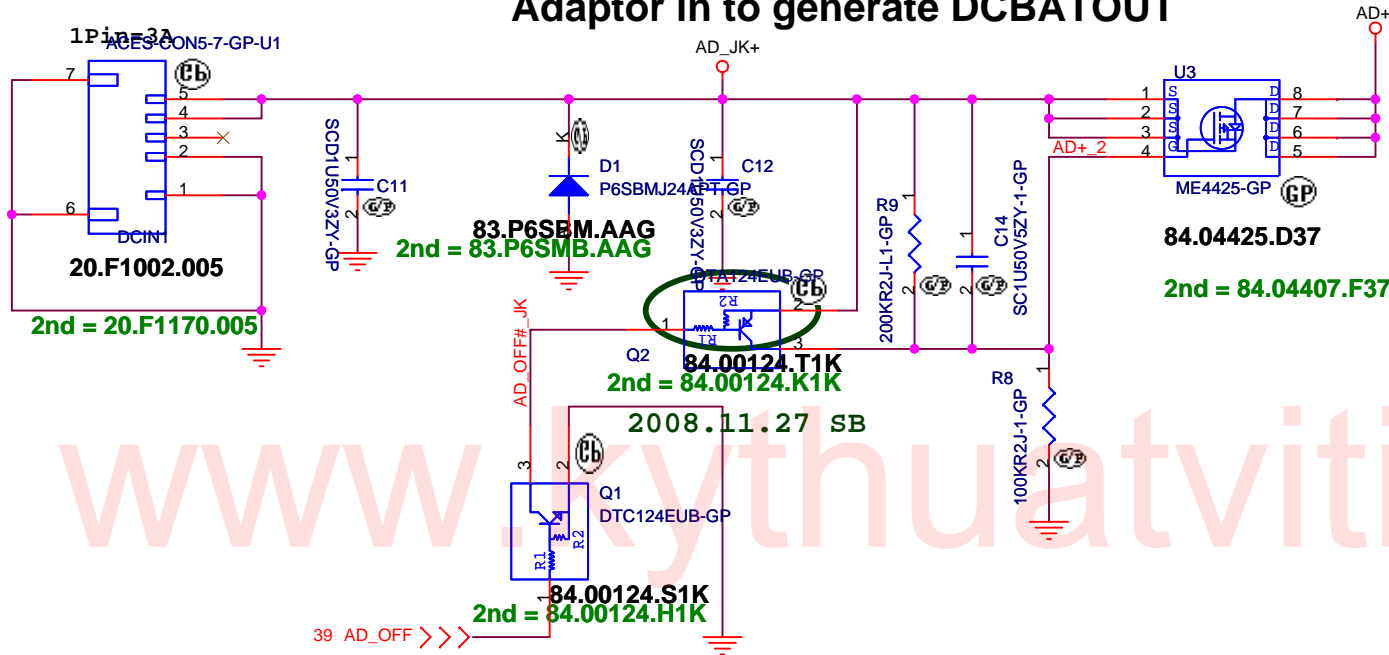
Cyntec 10.41
2nd = 68.R3610.20A
DCR=1.05+-5mohm
Irating=30A
Isat=60A

Cyntec 10.41
2nd = 68.R3610.20A
DCR=1.05+-5mohm
Irating=30A
Isat=60A

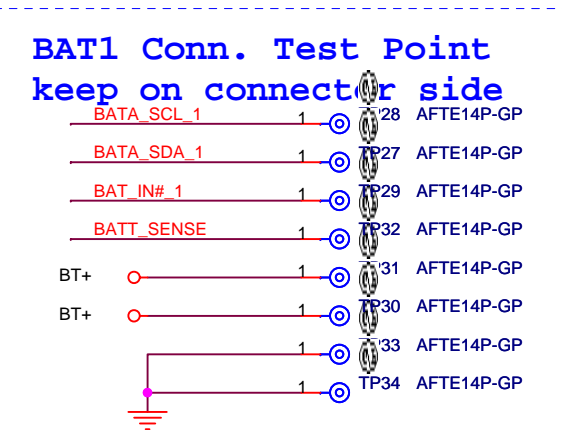
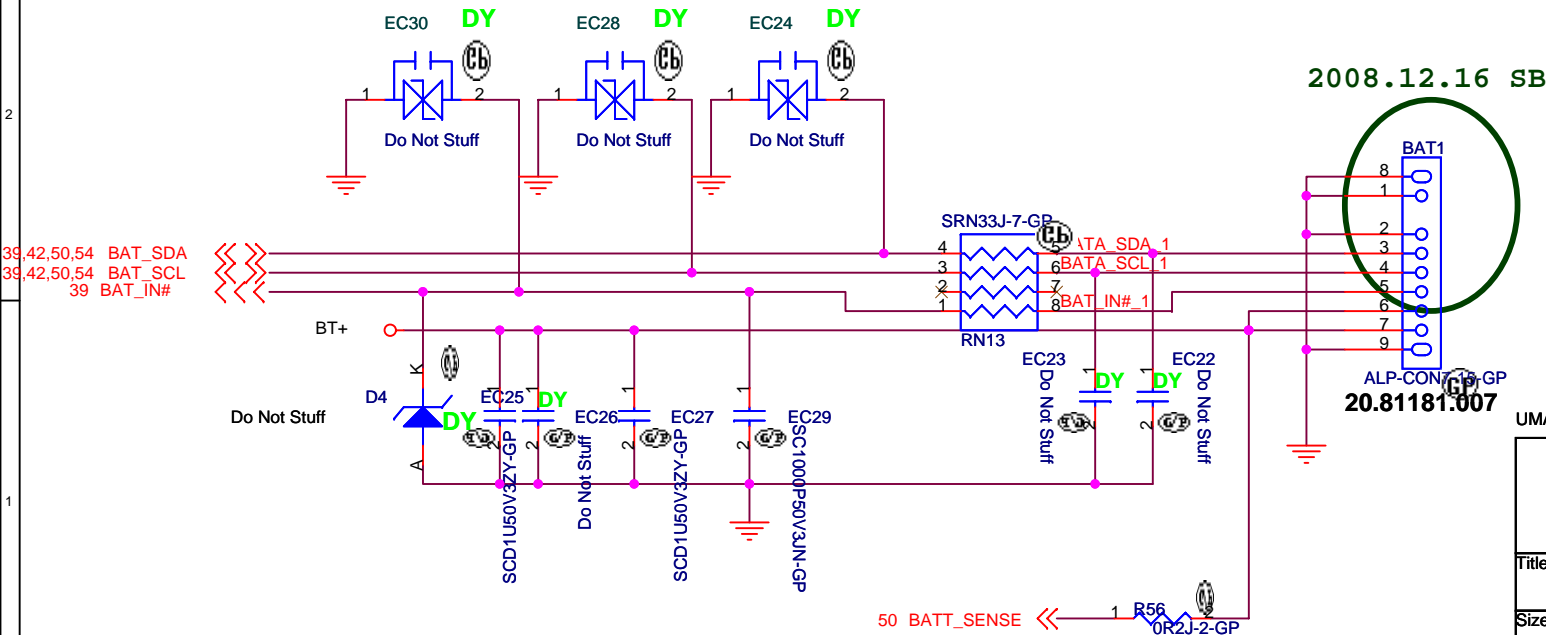
I_{comax}=60A
OCP>90A

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Title ADP3207C CPU CORE		
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Adaptor in to generate DCBATOUT



MAIN BATTERY CONNECTOR



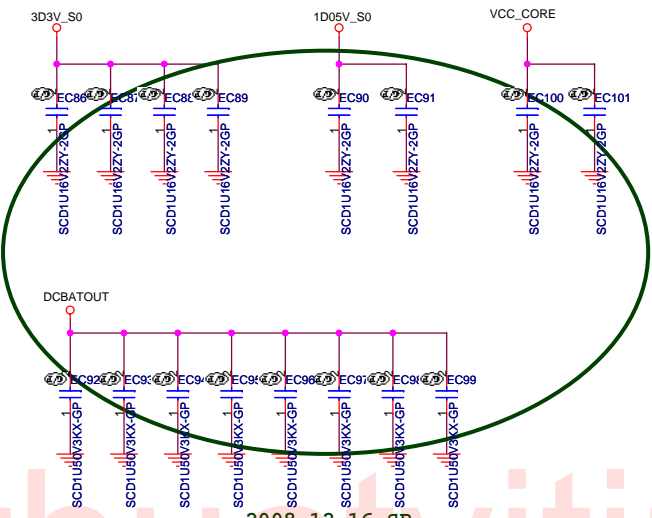
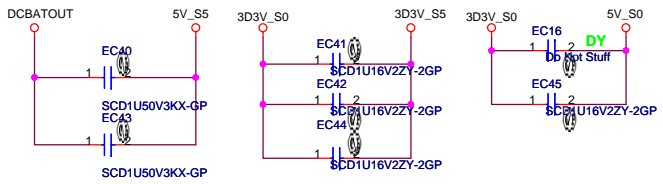
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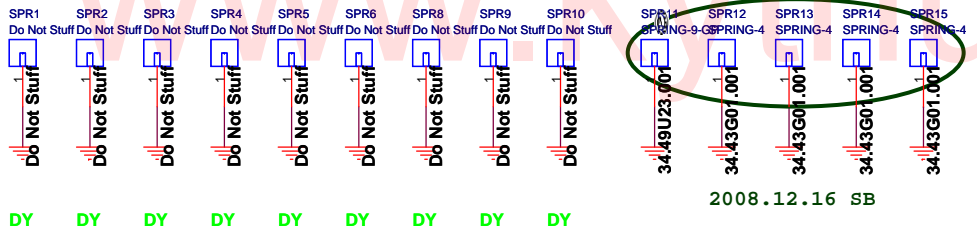
Title: **AD&BTY CONNECTER**

Size: Document Number **JM70-MV** Rev: **SB**

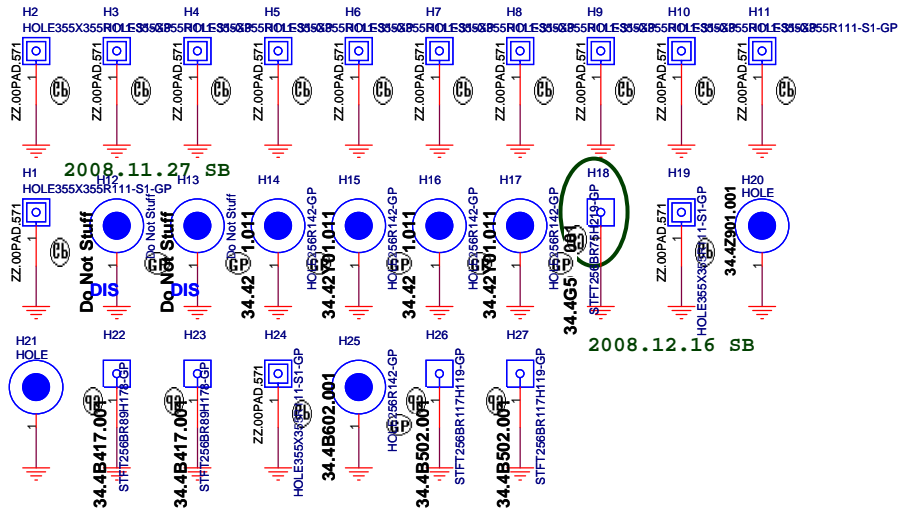
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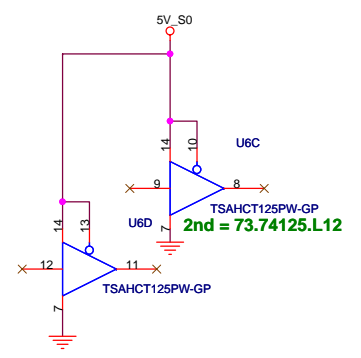
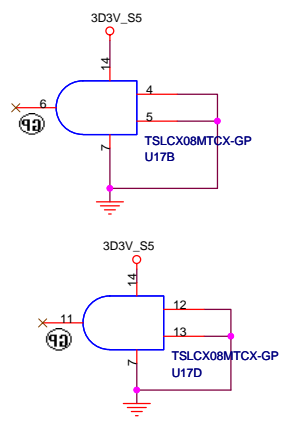
2008.12.16 SB



2008.12.16 SB



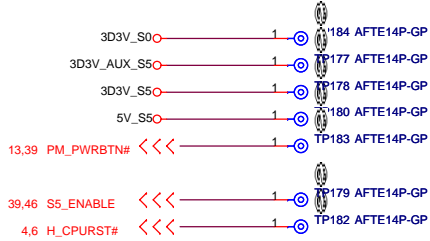
2008.12.16 SB



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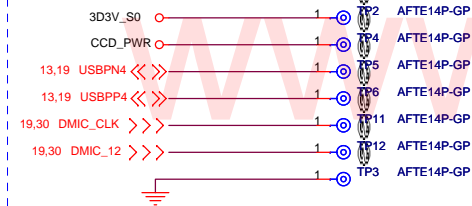
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	EMI/Spring/Boss	
Size	Document Number	Rev
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Check test point

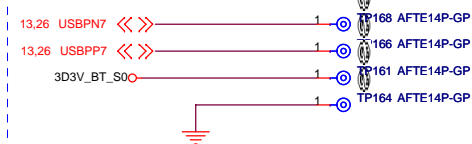


Test Point放在Dimm Door打開可量測處

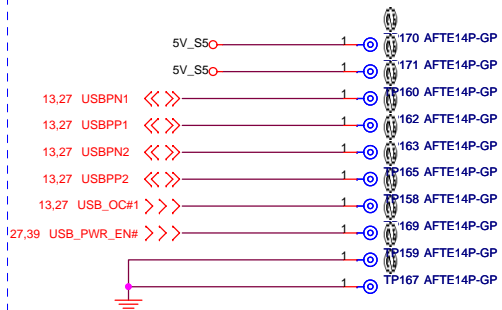
CCD_DMIC_CN1 Conn. Test Point keep on connector side



BT Conn. Test Point keep on connector side



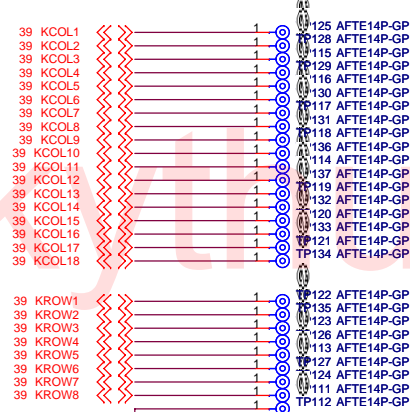
USB_CN1 Conn. Test Point keep on connector side



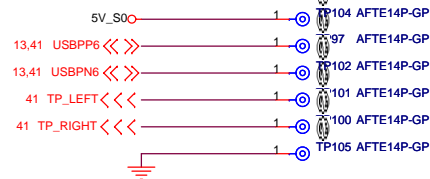
SPKR1 Conn. Test Point keep on connector side



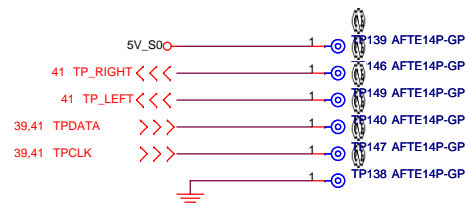
KBI Conn. Test Point keep on connector side



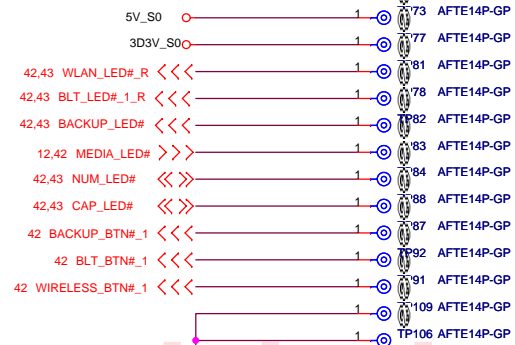
FP test Point keep on connector side



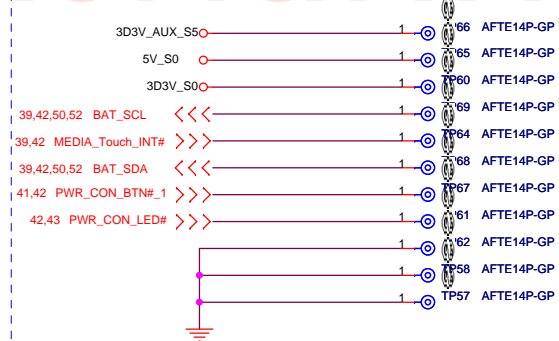
TOUCH PAD Conn. Test Point keep on connector side



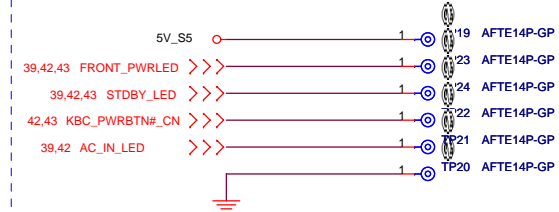
LAUN_CN1 Conn. Test Point keep on connector side



PWR_SAVING_CN1 Conn. Test Point keep on connector side



PWR_BT_CN1 Conn. Test Point keep on connector side



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Title			AFTE TP		
Size	Document Number				Rev
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HISTORY	
File	
Size	Document Number
K2	JM70-MV
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