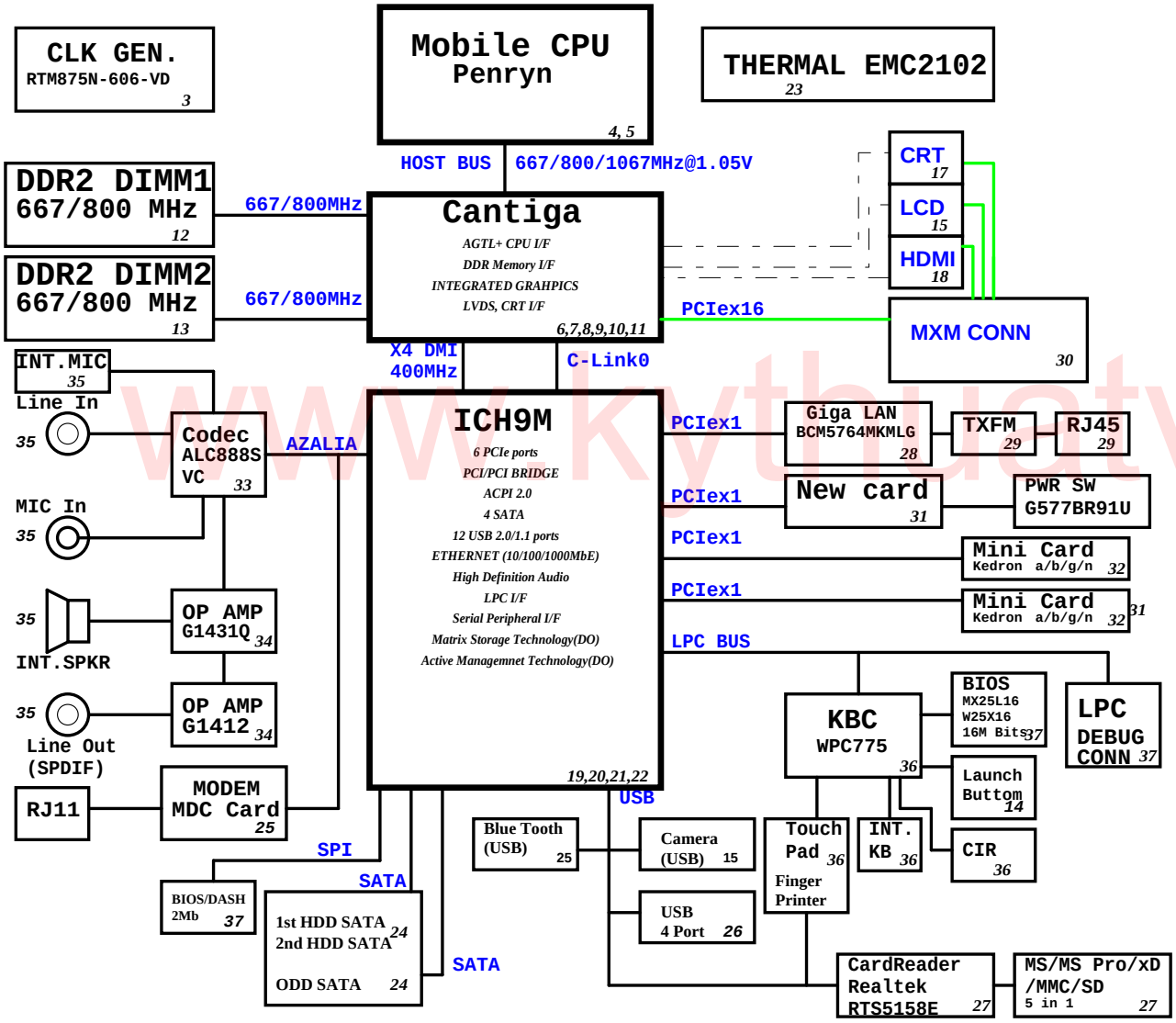
Big Bear 2 Block Diagram

Project code: 91.4AV01.001
PCB P/N : 48.4AV01.
REVISION : -1



PCB STACKUP

TOP	
VCC	
S	
S	
GND	
BOTTOM	

SYSTEM DC/DC TPS51125 43	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5

SYSTEM DC/DC TPS51124 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D8V_S3

RT9026 44	
1D8V_S3	DDR_VREF_S0 DDR_VREF_S3

RT9018A 44	
1D8V_S3	1D5V_S0

G9131 44	
3D3V_S0	2D5V_S0

GFXCORE DC/DC ISL6263 46	
INPUTS	OUTPUTS
DCBATOUT	VGFXCORE 0.7~1.25V

CPU DC/DC ISL6266A 42	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0.35~1.5V

CHARGER BQ24745 47	
INPUTS	OUTPUTS
DCBATOUT	BT+ DCBATOUT

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DN: cn=dddddddddd, email=dddd@yahoo.com, c=US
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Title: BLOCK DIAGRAM
Size: Custom | Document Number: Big Bear 2 | Rev: -1
Date: Wednesday, October 22, 2008 | Sheet 1 of 50

ICH9M Functional Strap Definitions

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#/ GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resister.

ICH9M Integrated Pull-up and Pull-down Resistors

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) **1=The iTPM Host Interface is disalbed(default)**
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality **1 = TLS cipher suite with confidentiality (default)**
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG10	PCIE Loopback enable	0 = Enable (Note 3) **1= Disabled (default)**
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) **11 = Disabled (default)**
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG19	DMI Lane Reversal	**0 = Normal operation(Default): Lane Numbered in Order** 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	**0 = Only Digital Display Port or PCIE is operational (Default)** 1 =Digital display Port and PCIe are operting simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	**0 =No SDVO Card Present (Default)** 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	**0 = LFP Disabled (Default)** 1= LFP Card Present; PCIE disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG/12/CFG13 straps can be enabled at any time.

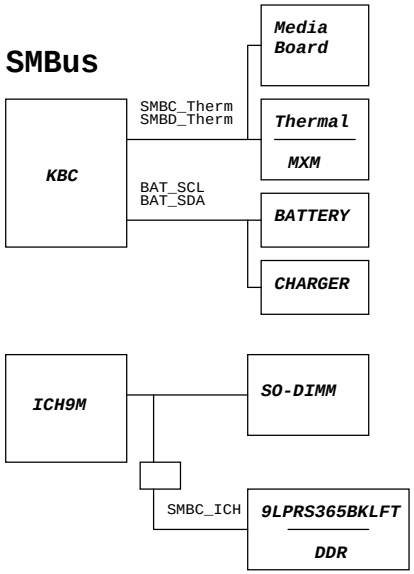
PCIE Routing

LANE1	LAN MARVELL 88E8071
LANE2	MiniCard WLAN
LANE3	MiniCard WWAN/TV
LANE4	JMB385 Card Reader
LANE5	NewCard
LANE6	*NC*

USB Table

USB	
Pair	*Device*
0	*USB1*
1	*USB4*
2	*USB2*
3	*USB5(DOCK)*
4	*USB3*
5	*Bluetooth*
6	*FP*
7	*MINIC1*
8	*WEBCAM*
9	*NEW1*
10	*MINIC2*
11	*NC*

SMBus



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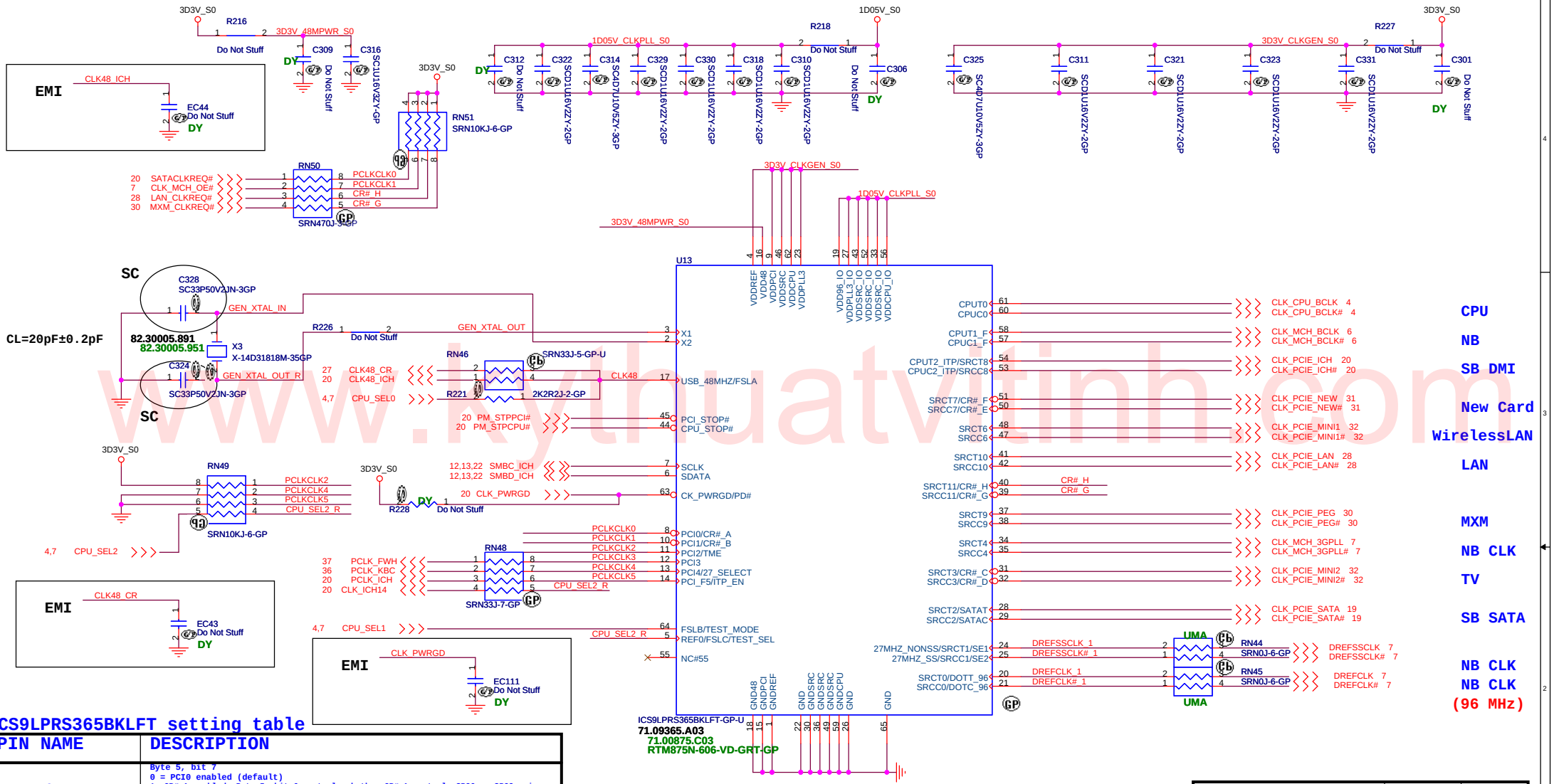
Title: **Reference**

Size: A3 | Document Number: **Big Bear 2** | Rev: **-1**

Date: Wednesday, October 22, 2008 | Sheet 2 of 50



ICS9LPRS365BKLFT setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3	3.3V PCI clock output
PCI4/27M_SEL	0 = Pin24 as SRC-1, Pin25 as SRC-1#, Pin20 as DOT96, Pin21 as DOT96# 1 = Pin24 as 27MHz, Pin25 as 27MHz_SS, Pin20 as SRC-0, Pin21 as SRC-0#
PCI_F5/ITP_EN	0 =SRC8/SRC8# 1 = ITP/ITP#
SRCT3/CR#_C	Byte 5, bit 3 0 = SRC3 enabled (default) 1= CR#_C enabled. Byte 5, bit 2 controls whether CR#_C controls SRC0 or SRC2 pair Byte 5, bit 2 0 = CR#_C controls SRC0 pair (default), 1= CR#_C controls SRC2 pair

PIN NAME	DESCRIPTION
SRCC3/CR#_D	Byte 5, bit 1 0 = SRC3 enabled (default) 1= CR#_D enabled. Byte 5, bit 0 controls whether CR#_D controls SRC1 or SRC4 pair Byte 5, bit 0 0 = CR#_D controls SRC1 pair (default) 1= CR#_D controls SRC4 pair
SRCC7/CR#_E	Byte 6, bit 7 0 = SRC7# enabled (default) 1= CR#_F controls SRC6
SRCT7/CR#_F	Byte 6, bit 6 0 = SRC7 enabled (default) 1= CR#_F controls SRC8
SRCC11/CR#_G	Byte 6, bit 5 0 = SRC11# enabled (default) 1= CR#_G controls SRC9
SRCT11/CR#_H	Byte 6, bit 4 0 = SRC11 enabled (default) 1= CR#_H controls SRC10

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1066M

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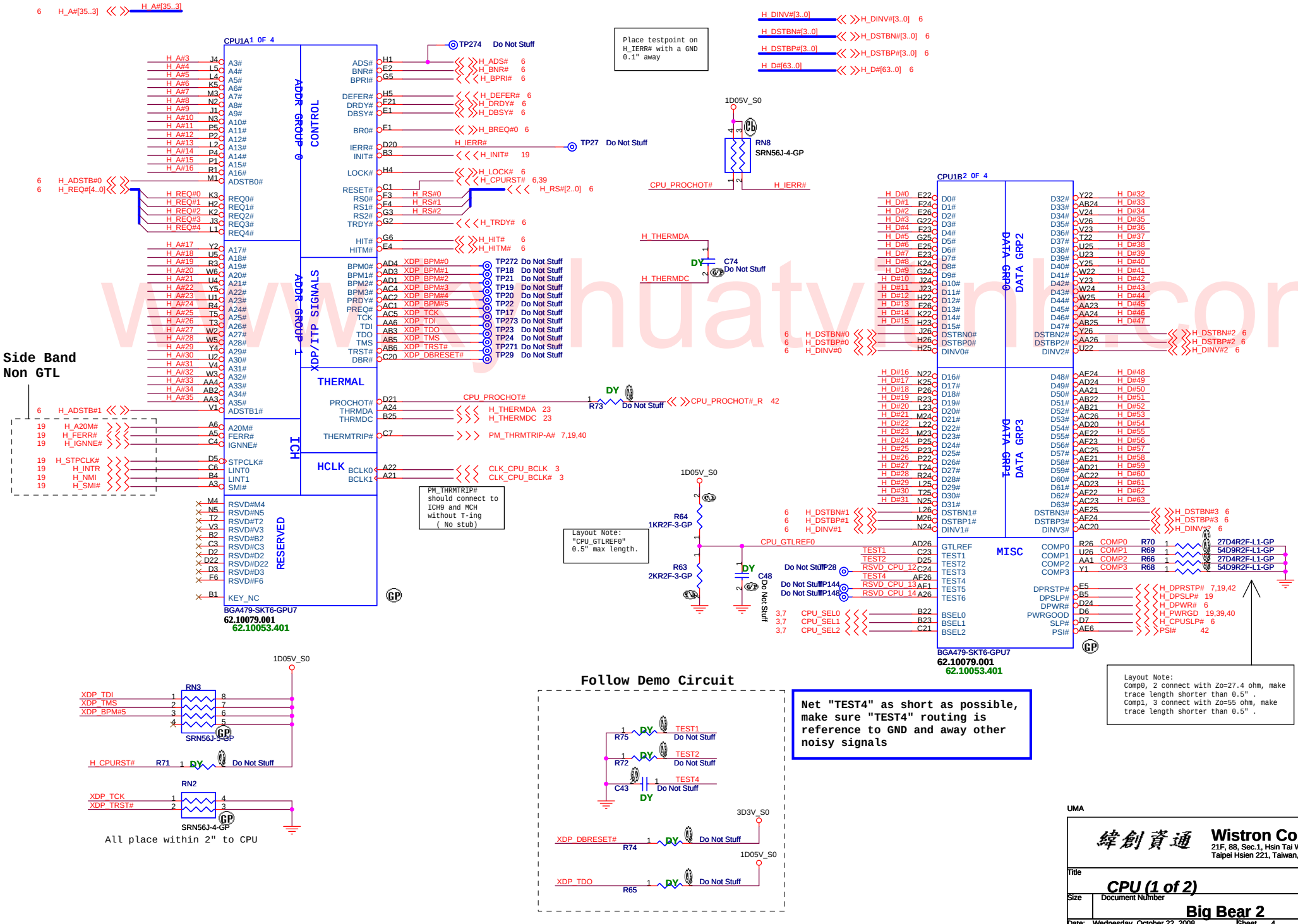
Title: Clock Generator

Size | Document Number: Big Bear 2 | Rev: -1

Date: Wednesday, October 22, 2008 | Sheet 3 of 50


CPU1A 1 OF 4
ADDR GROUP 0
ADDR GROUP 1
CONTROL
XDP/ITP SIGNALS
THERMAL
HCLK
RESERVED
ICH
BGA479-SKT6-GPU7
62.10079.001
62.10053.401
Side Band
Non GTL
Place testpoint on H_IERR# with a GND 0.1" away
CPU1B 2 OF 4
DATA GRP0
DATA GRP2
DATA GRP1
DATA GRP3
MISC
RN8
SRN56J-4-GP
C74
Do Not Stuff
R73
CPU_PROCHOT#_R
PM_THRMTRIP# should connect to ICH9 and MCH without T-ing (No stub)
Layout Note: "CPU_GTLREF0" 0.5" max length.
R64
1KR2F-3-GP
R63
2KR2F-3-GP
C48
RN3
SRN56J-5-GP
R71
RN2
SRN56J-4-GP
All place within 2" to CPU
Follow Demo Circuit
R75
R72
C43
R74
R65
Net "TEST4" as short as possible, make sure "TEST4" routing is reference to GND and away other noisy signals
Layout Note: Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5" . Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5" .
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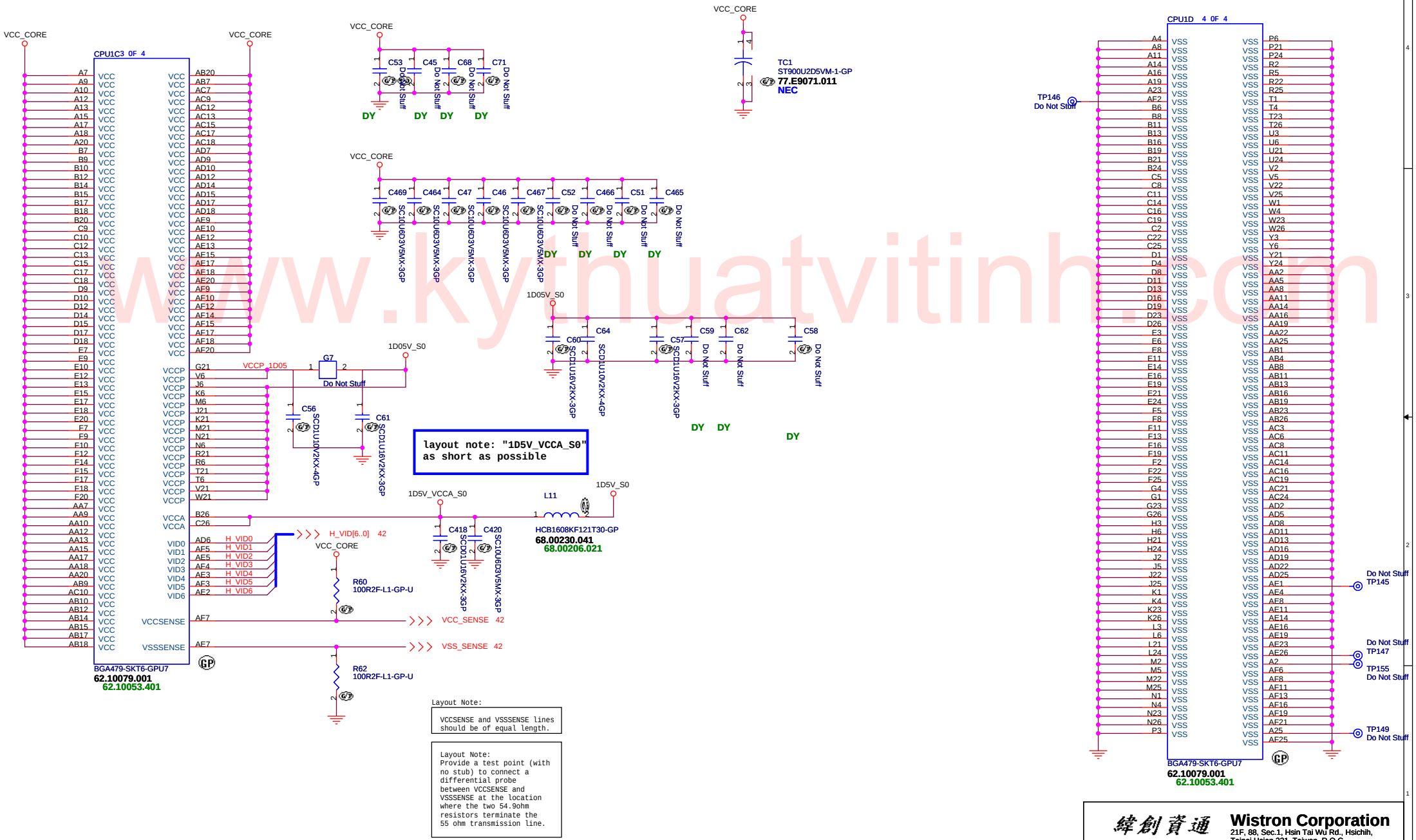
CPU (1 of 2)
Big Bear 2
-1
Wednesday, October 22, 2008
Sheet 4 of 50


VCC_CORE
CPU1C3 0F 4
BGA479-SKT6-GPU7
62.10079.001
62.10053.401
C53
C45
C68
C71
Do Not Stuff
DY
TC1
ST900U2D5VM-1-GP
77.E9071.011
NEC
C469
C464
C47
C46
C467
C52
C466
C51
C465
SC10U6D3V5MX-3GP
1D05V_S0
C60
C64
C57
C59
C62
C58
SCD1U16V2KX-3GP
SCD1U10V2KX-4GP
VCCP_1D05
G7
Do Not Stuff
C56
C61
SCD1U10V2KX-4GP
SCD1U6V2KX-3GP
layout note: "1D5V_VCCA_S0" as short as possible
1D5V_VCCA_S0
L11
HCB1608KF121T30-GP
68.00230.041
68.00206.021
C418
C420
SCD01U16V2KX-3GP
SC10U6D3V5MX-3GP
H_VID[6..0]
42
R60
100R2F-L1-GP-U
R62
VCC_SENSE
VSS_SENSE
Layout Note:
VCCSENSE and VSSSENSE lines should be of equal length.
Layout Note:
Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.
CPU1D 4 0F 4
TP146
TP145
TP147
TP155
TP149
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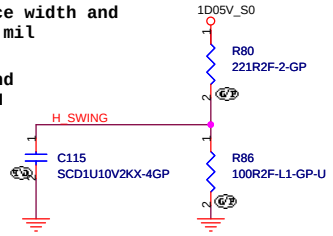
Title
CPU (2 of 2)
Size
Document Number
Big Bear 2
Rev
-1
Date: Wednesday, October 22, 2008
Sheet 5 of 50

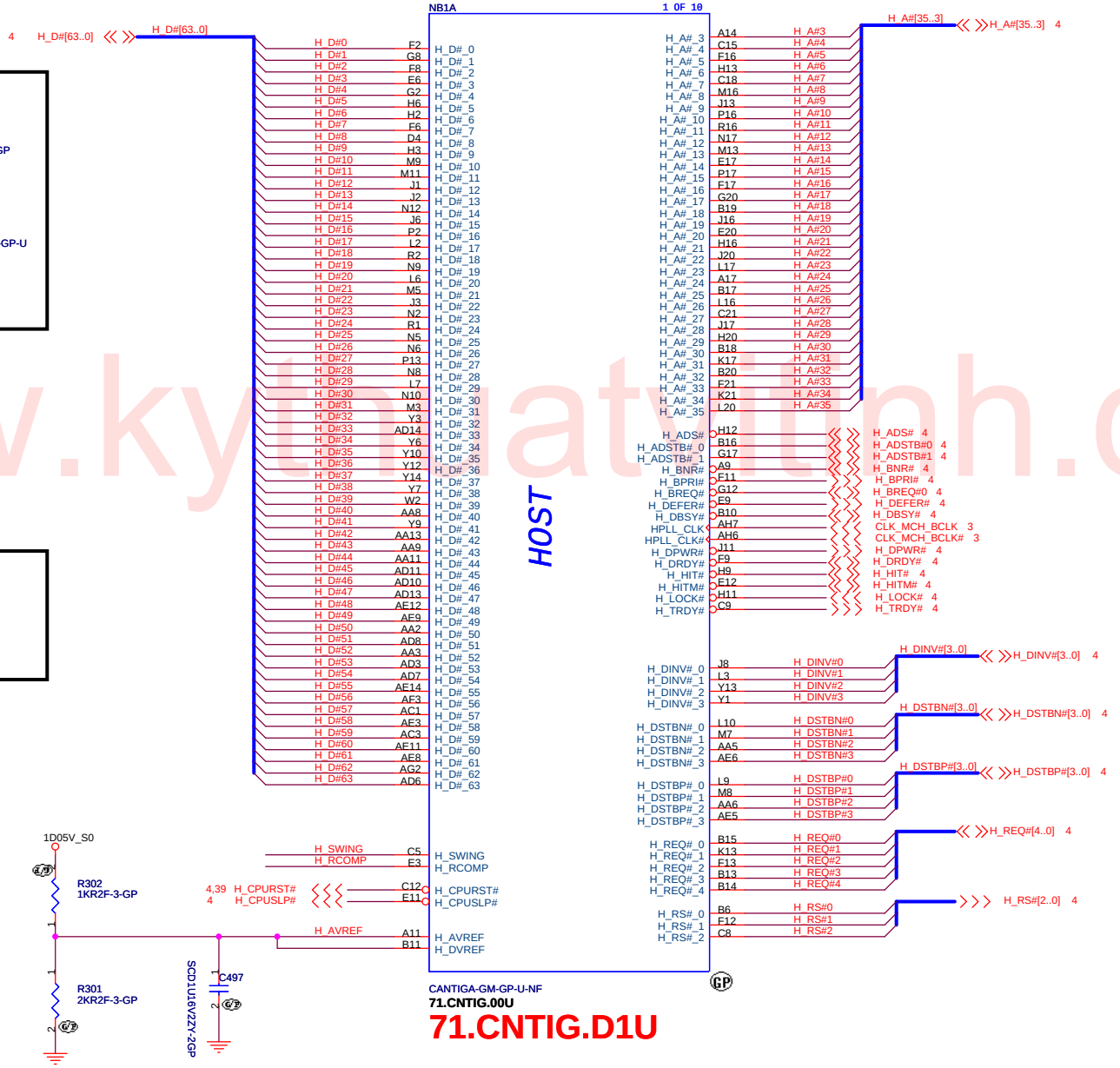
H_SWING routing Trace width and Spacing use 10 / 20 mil

H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



H_RCOMP routing Trace width and Spacing use 10 / 20 mil

Place them near to the chip (< 0.5")



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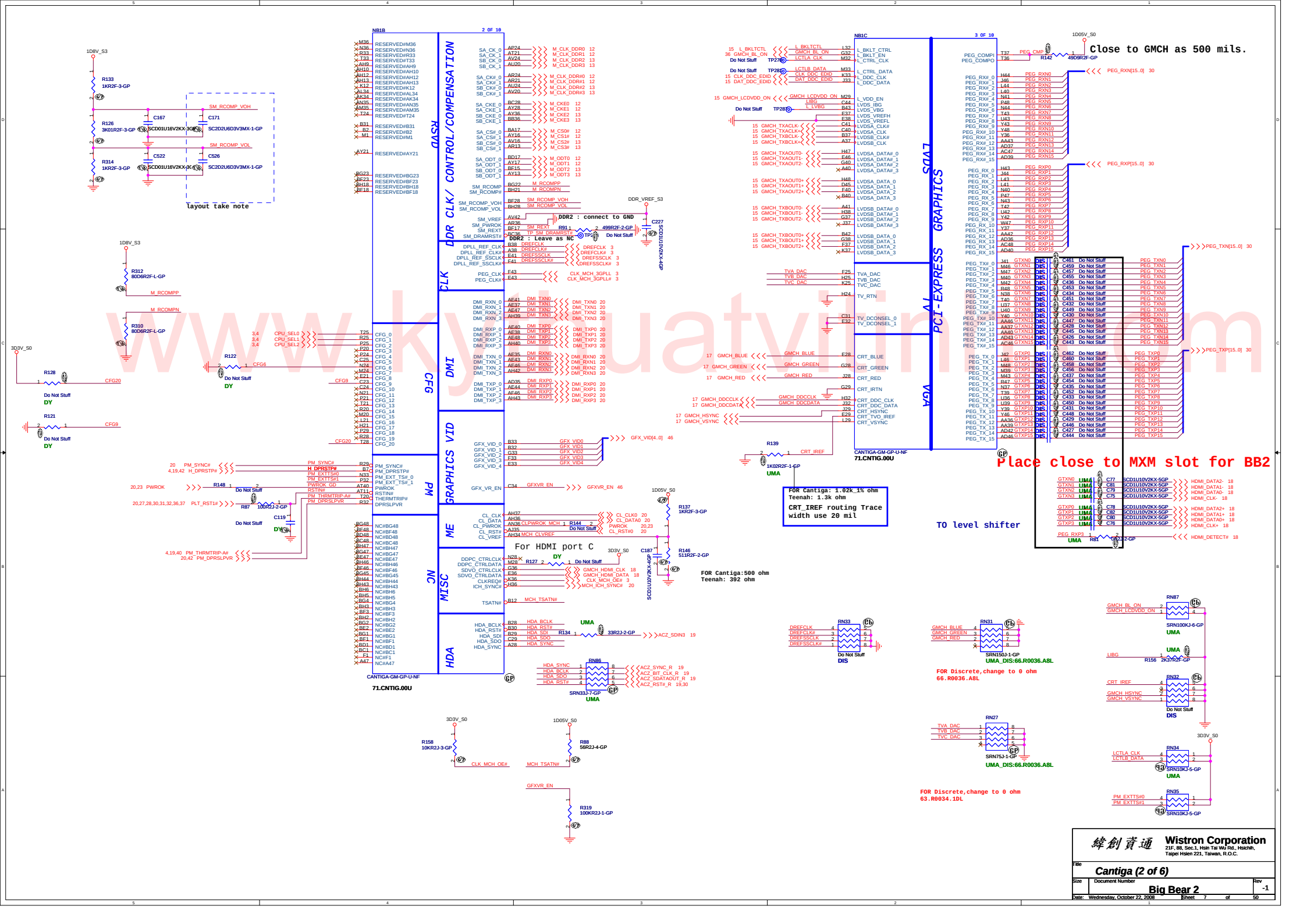
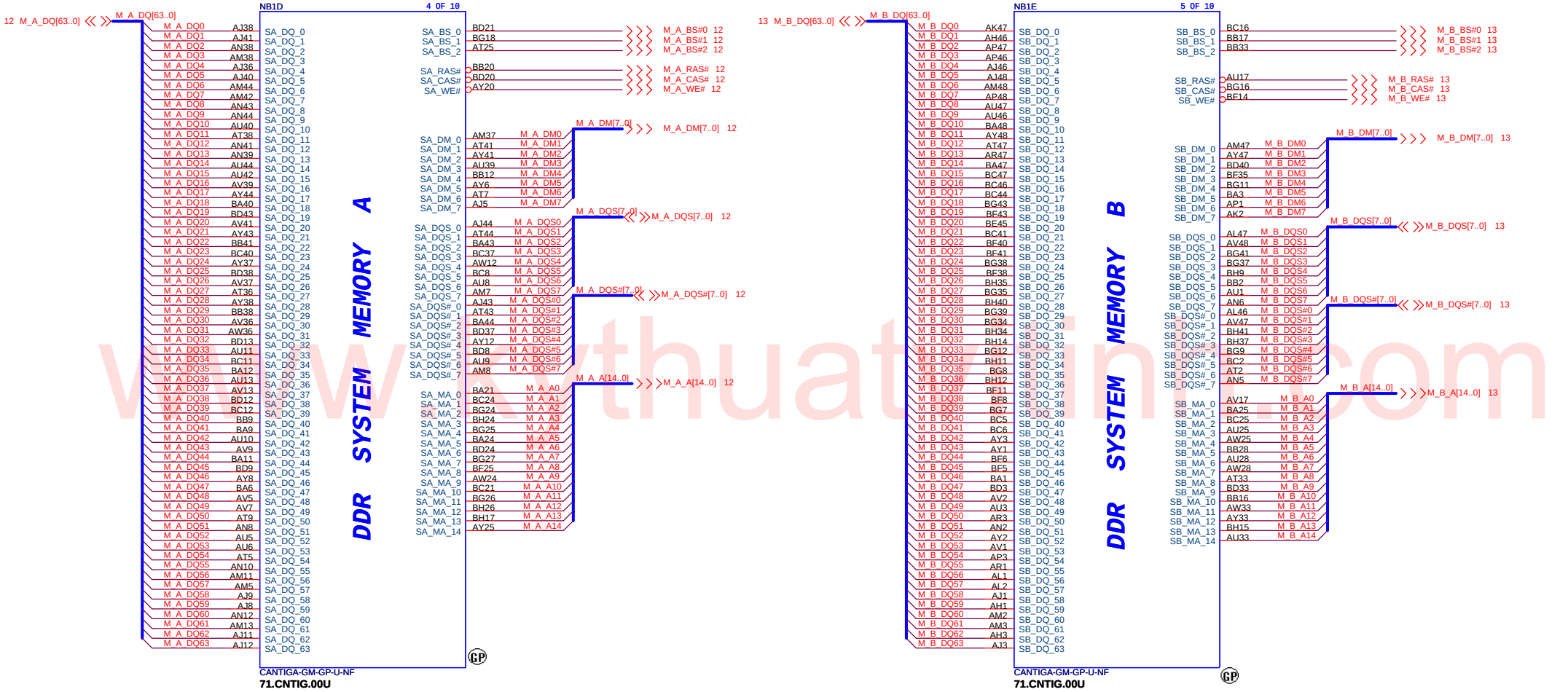
Title: ***Cantiga (1 of 6)***

Size | Document Number: **Big Bear 2** | Rev: -1

Date: Wednesday, October 22, 2008 | Sheet 6 of 50





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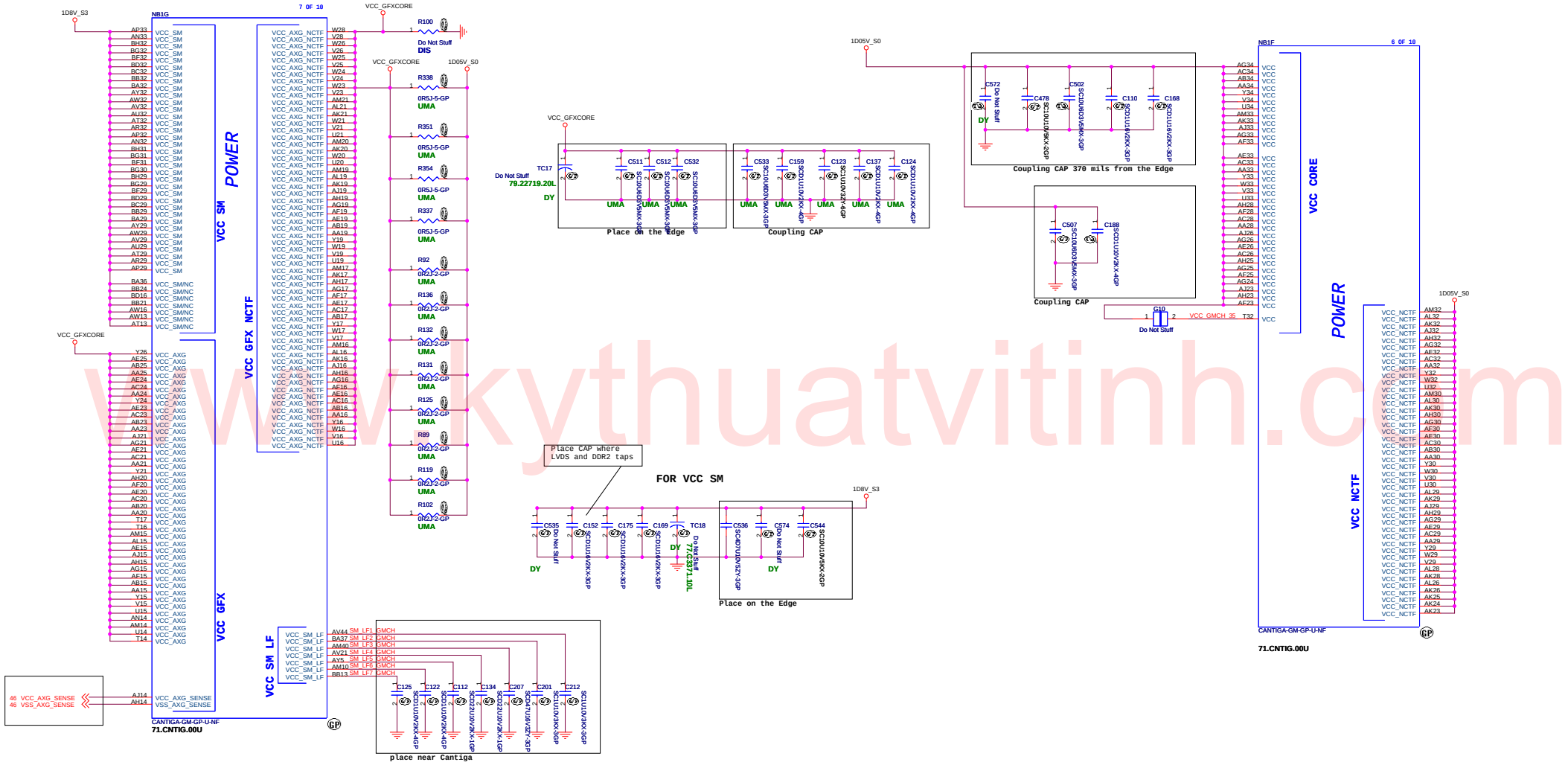
Title: Cantiga (3 of 6)

Size | Document Number: Big Bear 2 | Rev: -1

Date: Wednesday, October 22, 2008 | Sheet 8 of 50



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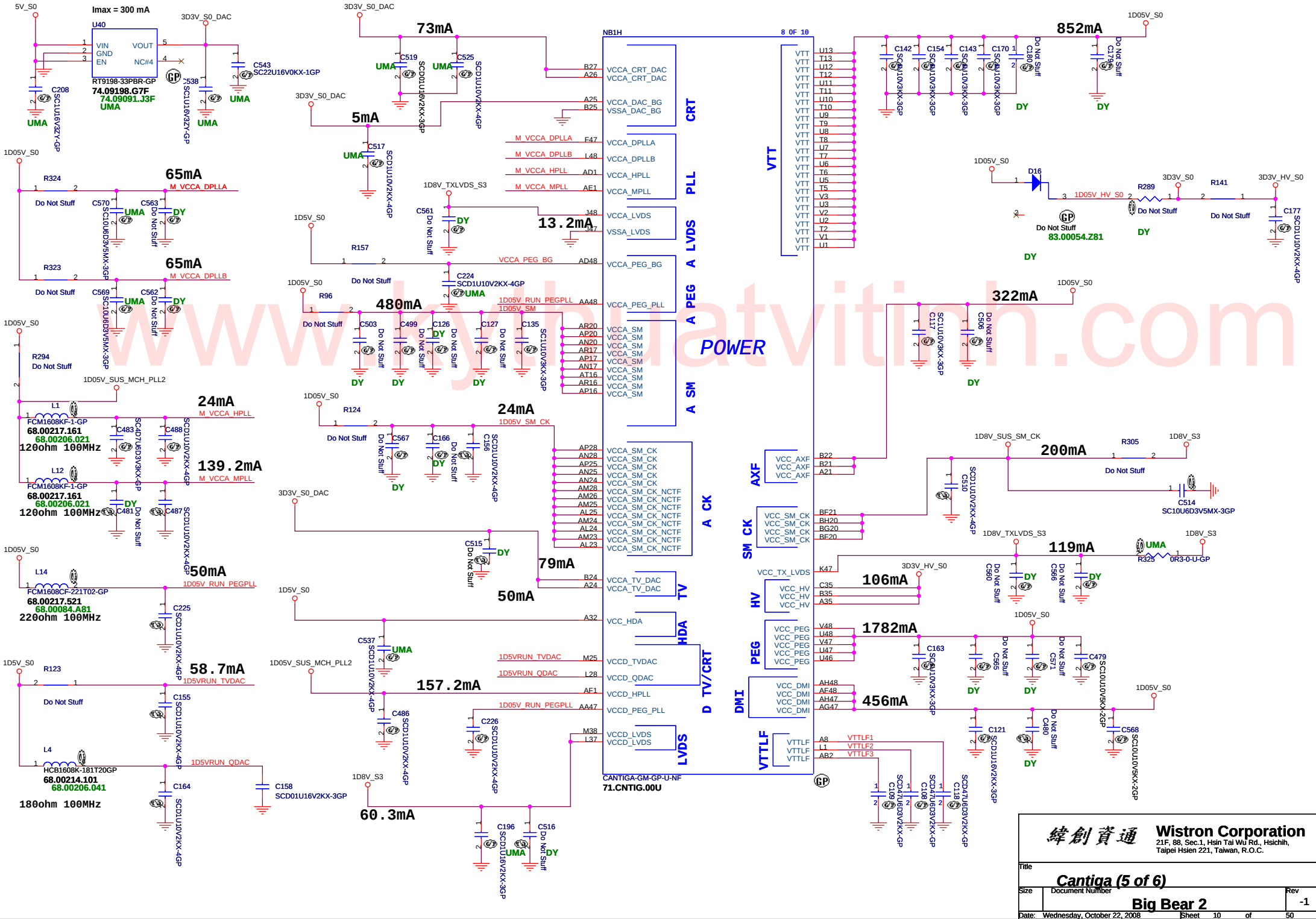
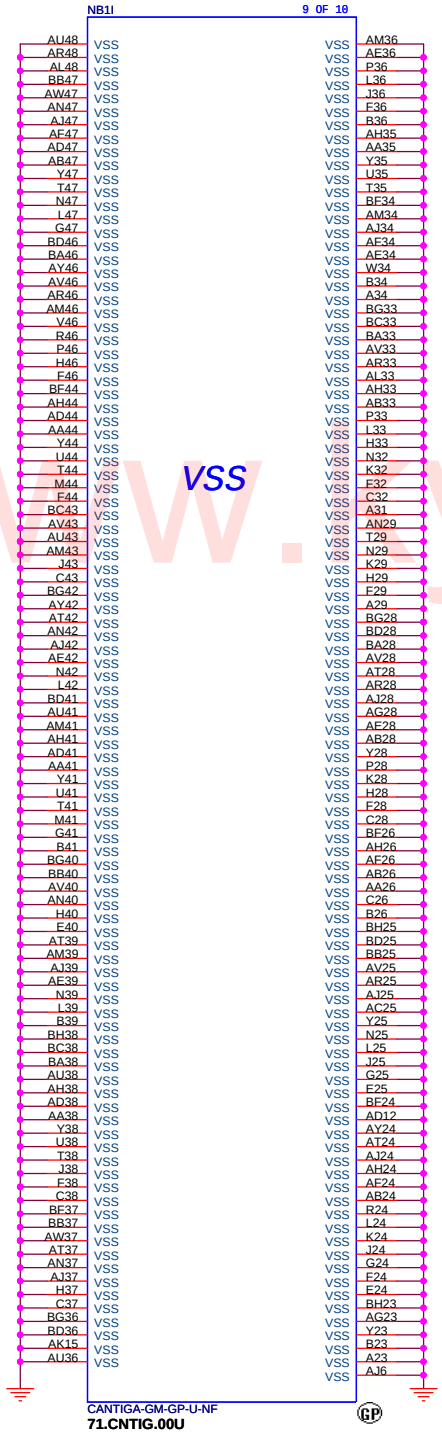
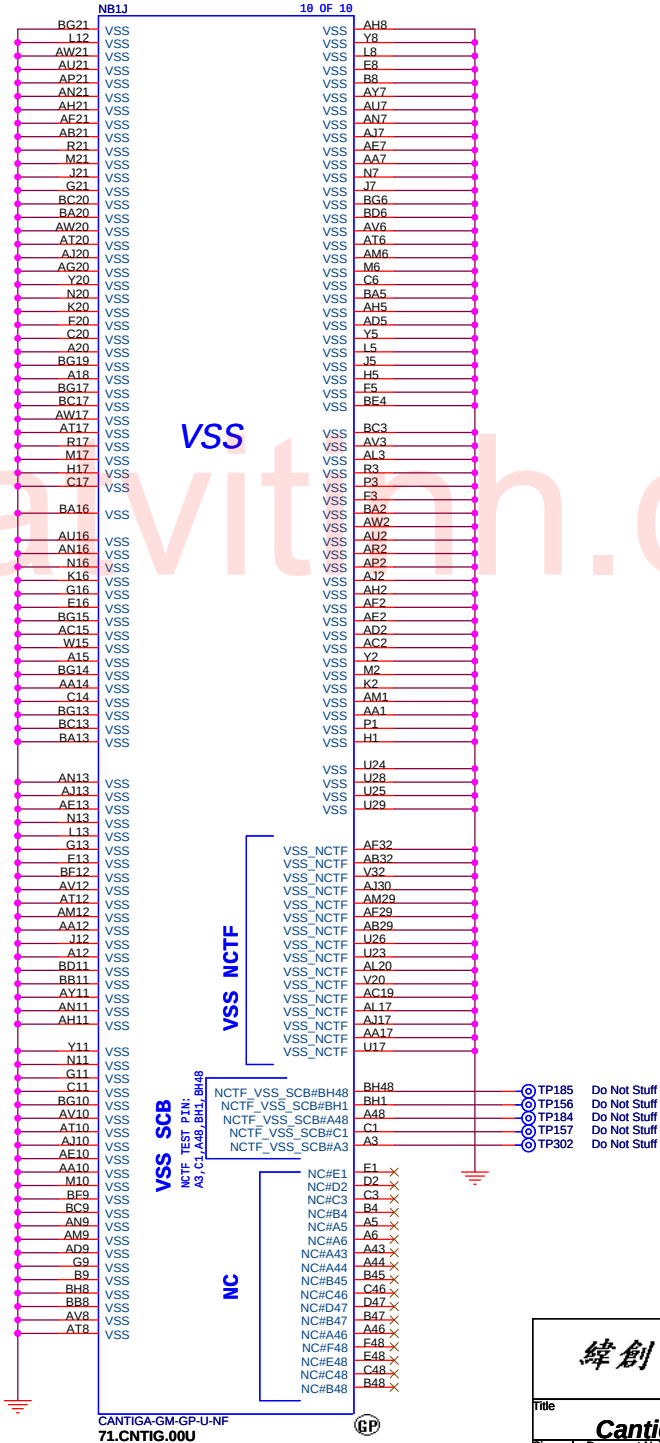
Title	Cantiga (4 of 6)	
Size	Document Number	Rev
	Big Bear 2	-1
Date: Wednesday, October 22, 2008	Sheet 9 of 50	







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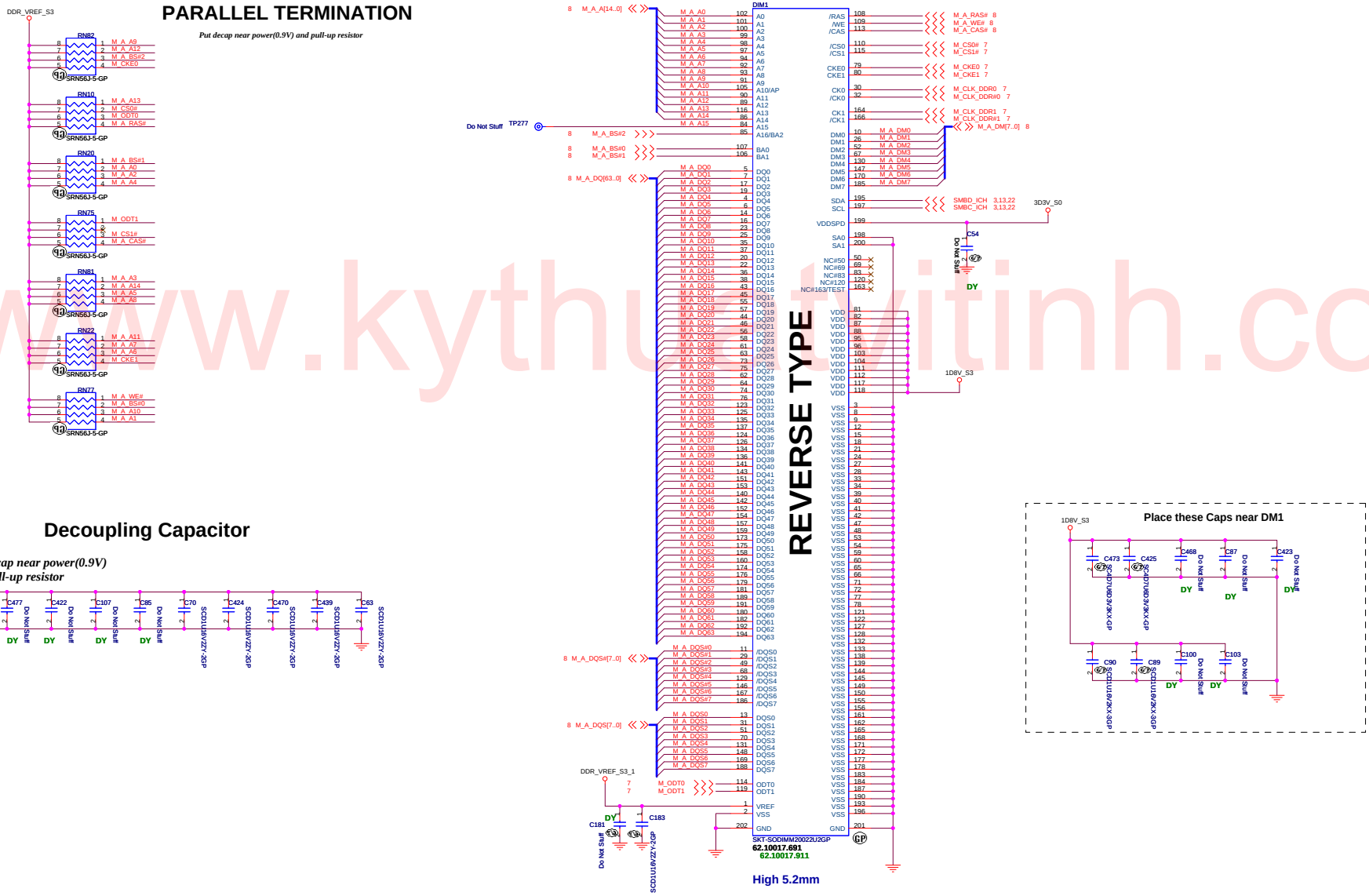
Size | Document Number: **Big Bear 2** | Rev: -1

Date: Wednesday, October 22, 2008 | Sheet 11 of 50



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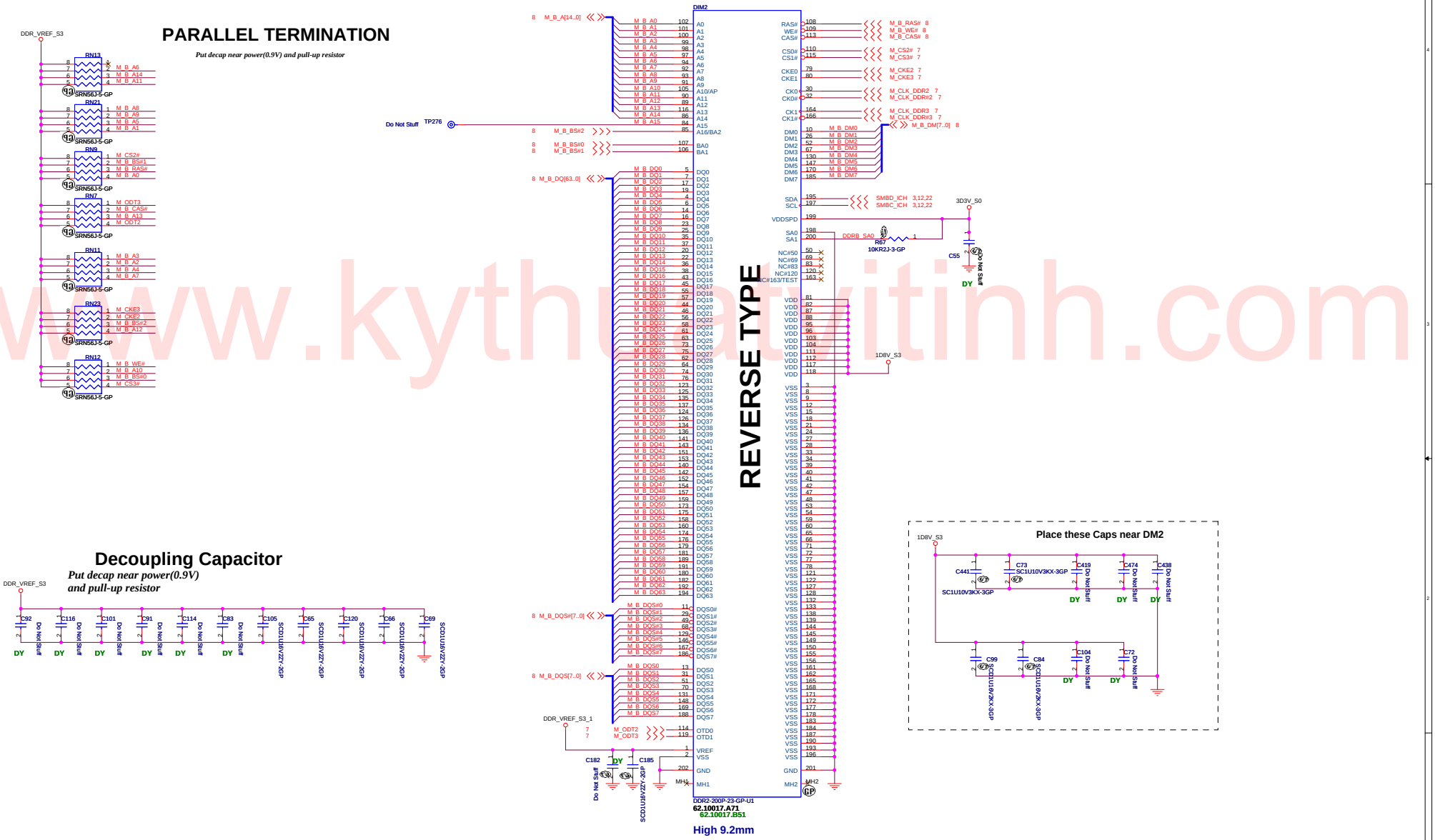
Title: DDR2 Socket 0 (DM1)
Size: | Document Number: Big Bear 2 | Rev: -1
Date: Wednesday, October 22, 2008 | Sheet 12 of 50



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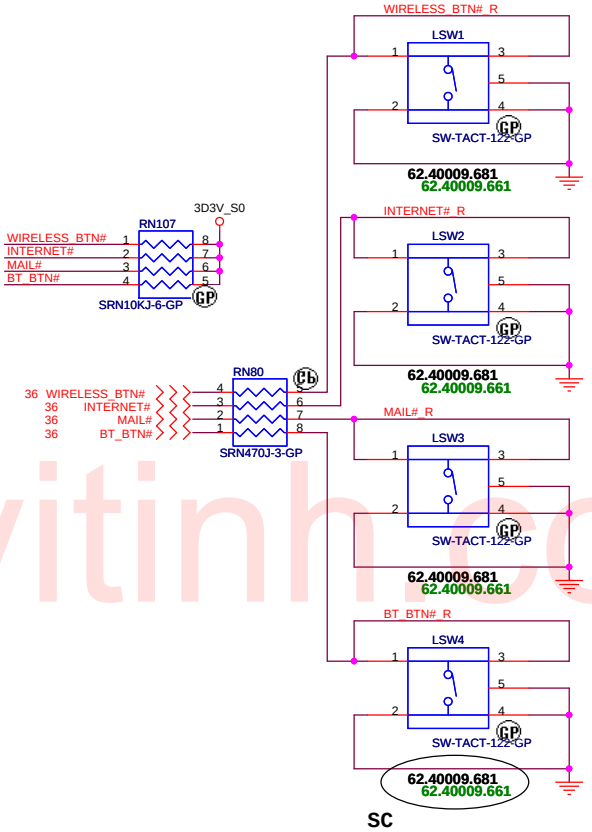
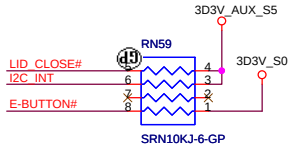
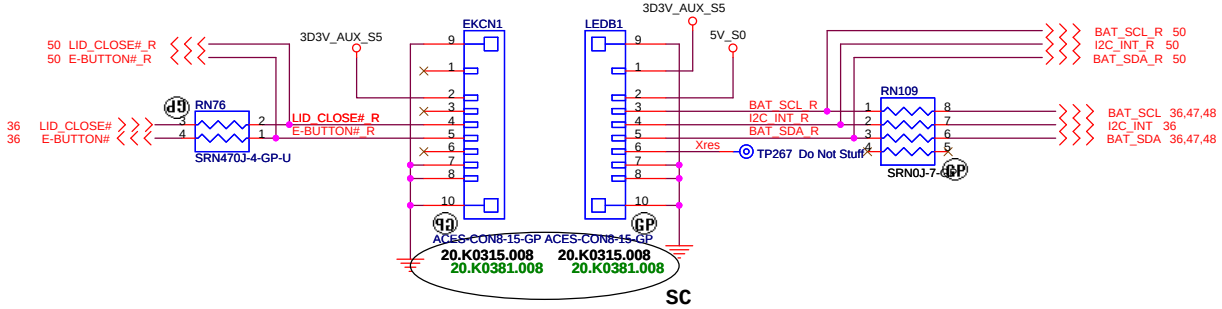
Title: **DDR2 Socket 1 (DM2)**

Size | Document Number: **Big Bear 2** | Rev: -1

Date: Wednesday, October 22, 2008 | Sheet 13 of 50







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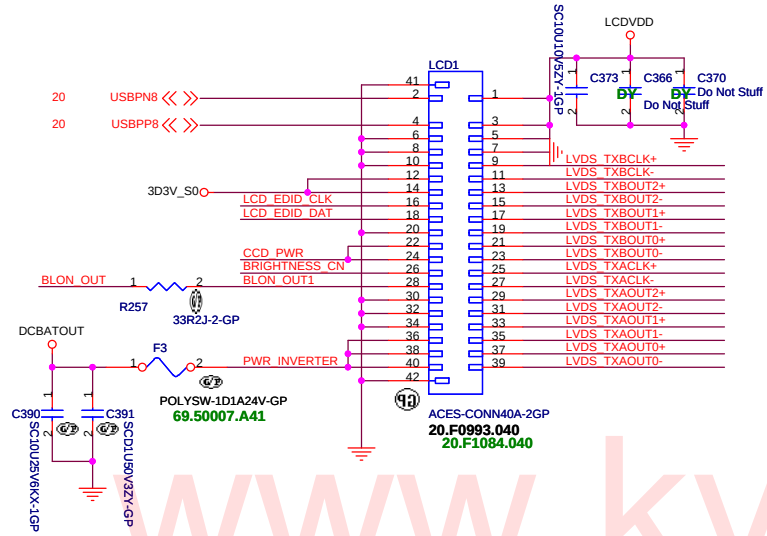
Title	***LAUNCH***	
Size	Document Number **Big Bear 2**	Rev -1
Date: Wednesday, October 22, 2008	Sheet 14 of 50	

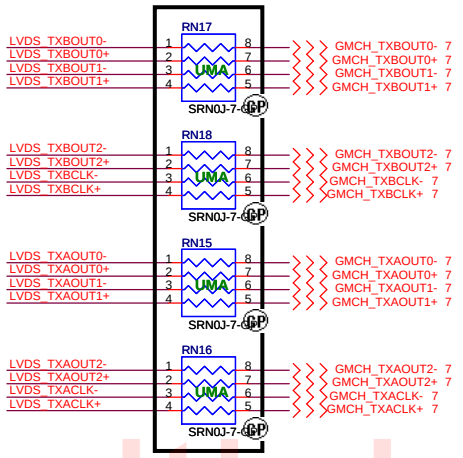
LCD/INVERTER/CCD CONN

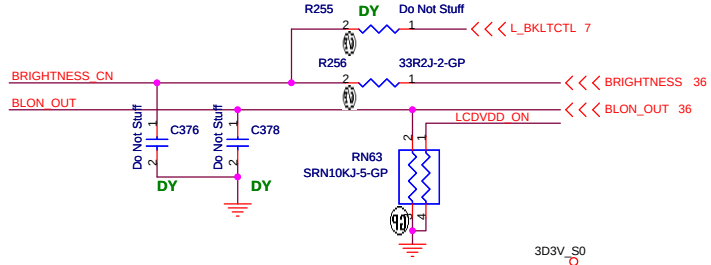
Place close to MXM slot for BB2

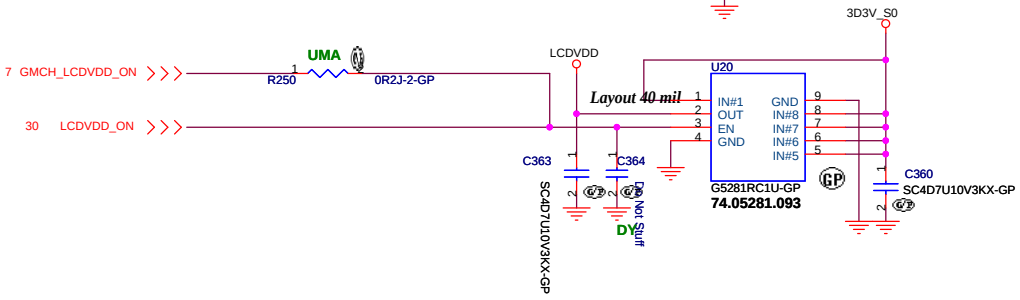


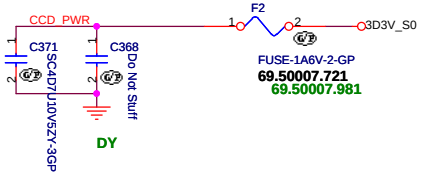
Inverter Pin	
Pin	Symbol
1	Vin
2	Vin
3	Brightness
4	BLON
5	GND
6	GND

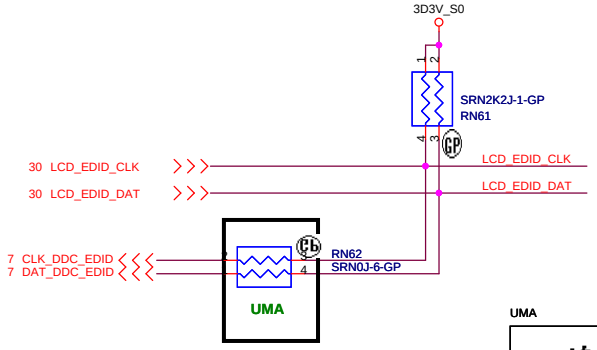
CCD Pin	
Pin	Symbol
1	CCD_PWR
2	USB-
3	USB+
4	GND
5	GND











Place close to MXM slot for BB2

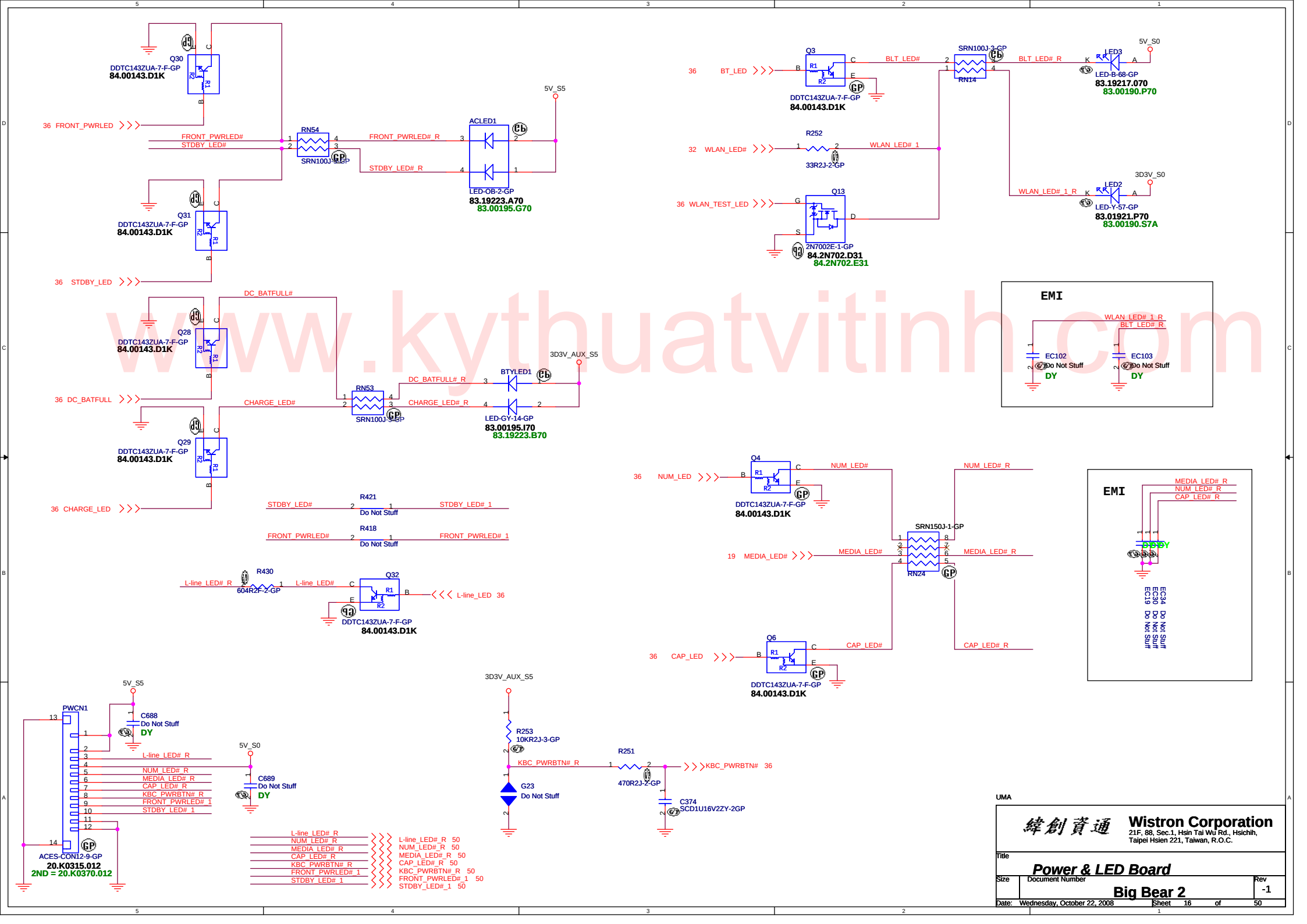
UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD CONN

Size | Document Number: Big Bear 2 | Rev: -1

Date: Wednesday, October 22, 2008 | Sheet 15 of 50



Layout Note:
Place these resistors close to the CRT-out connector

Ferrite bead impedance: 10 ohm@100MHz

CRT_R_SYS → L9 FCB1608CF-GP 68.00230.021 68.00119.081 → CRT_R
CRT_G_SYS → L8 FCB1608CF-GP 68.00230.021 68.00119.081 → CRT_G
CRT_B_SYS → L7 FCB1608CF-GP 68.00230.021 68.00119.081 → CRT_B

R267 150R2J-L1-GP-U
R269 150R2J-L1-GP-U
R272 150R2J-L1-GP-U
C404 Do Not Stuff DY
C398 Do Not Stuff DY
C396 Do Not Stuff DY
C401 SC15P50V2JN-2-GP
C397 SC6D8P50V2DN-GP
C395 SC6D8P50V2DN-GP

RN73 SRN0J-7-GP
30 CRT_RED
30 CRT_GREEN
30 CRT_BLUE
CRT_R_SYS
CRT_G_SYS
CRT_B_SYS
Do Not Stuff
DIS

RN6 SRN0J-7-GP
7 GMCH_BLUE
7 GMCH_GREEN
7 GMCH_RED
CRT_B_SYS
CRT_G_SYS
CRT_R_SYS
UMA

5V_S0
D10 CRT_R DY Do Not Stuff Do Not Stuff 83.00099.K11
D8 CRT_G DY Do Not Stuff Do Not Stuff 83.00099.K11
D7 CRT_B DY Do Not Stuff Do Not Stuff 83.00099.K11

Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

Hsync & Vsync level shift

5V_S0
C50 SCD1U16V2KX-3GP
CRT_HSYNC → U6A TSAHCT125PW-GP 73.74125.L13 73.74125.L12 → R57 Do Not Stuff → CRT_HSYNC2 → CRT_HSYNC1
CRT_VSYNC → U6B TSAHCT125PW-GP 73.74125.L13 73.74125.L12 → R56 Do Not Stuff → CRT_VSYNC2 → CRT_VSYNC1

For UMA CRT

7 GMCH_HSYNC
7 GMCH_VSYNC
RN72 SRN0J-6-GP UMA
CRT_HSYNC
CRT_VSYNC

For DIS CRT

30 CRT_HSYNC
30 CRT_VSYNC
CRT_HSYNC
CRT_VSYNC

5V_S0
U6C TSAHCT125PW-GP 73.74125.L13 73.74125.L12
U6D TSAHCT125PW-GP 73.74125.L13 73.74125.L12

CRT I/F & CONNECTOR

CRT1 VIDEO-15-42-GP-U 20.20378.015 20.20775.015
CRT_R
CRT_G
CRT_B
DAT_DDC1_5
CRT_HSYNC1
CRT_VSYNC1
CLK_DDC1_5
5V_CRT_S0
C27 SCD01U16V2KX-3GP
C393 SC100P50V2JN-3GP
C26 SC18P50V2JN-1-GP
C25 SC18P50V2JN-1-GP
C394 SC100P50V2JN-3GP

R265 470R2J-2-GP
36 CRT_DEC#
CRT_IN#_R
C392 Do Not Stuff DY
D5 Do Not Stuff 83.00099.K11
5V_S0

6 1 7 2 8 3 9 4 10 5

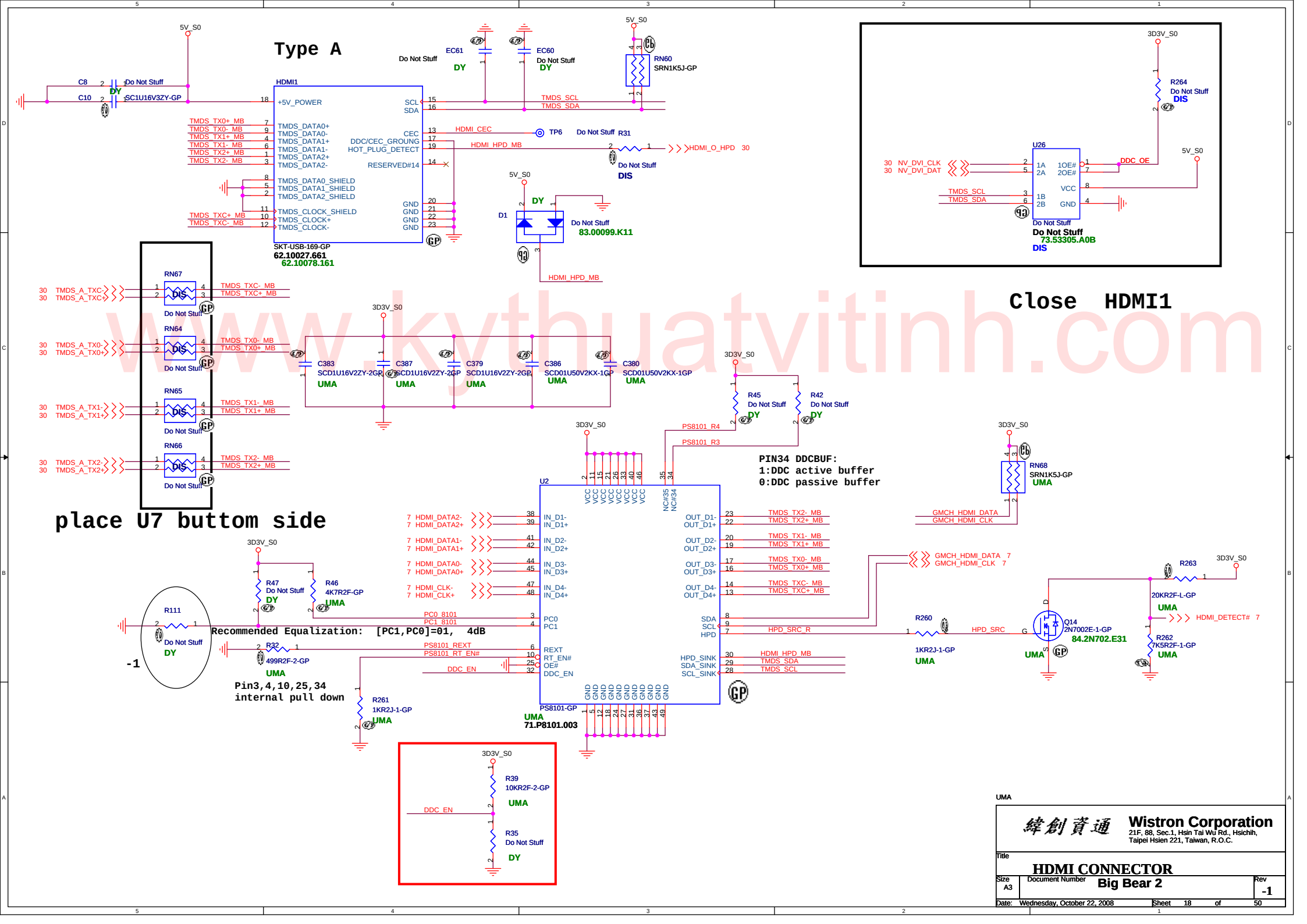
DDC_CLK & DATA level shift

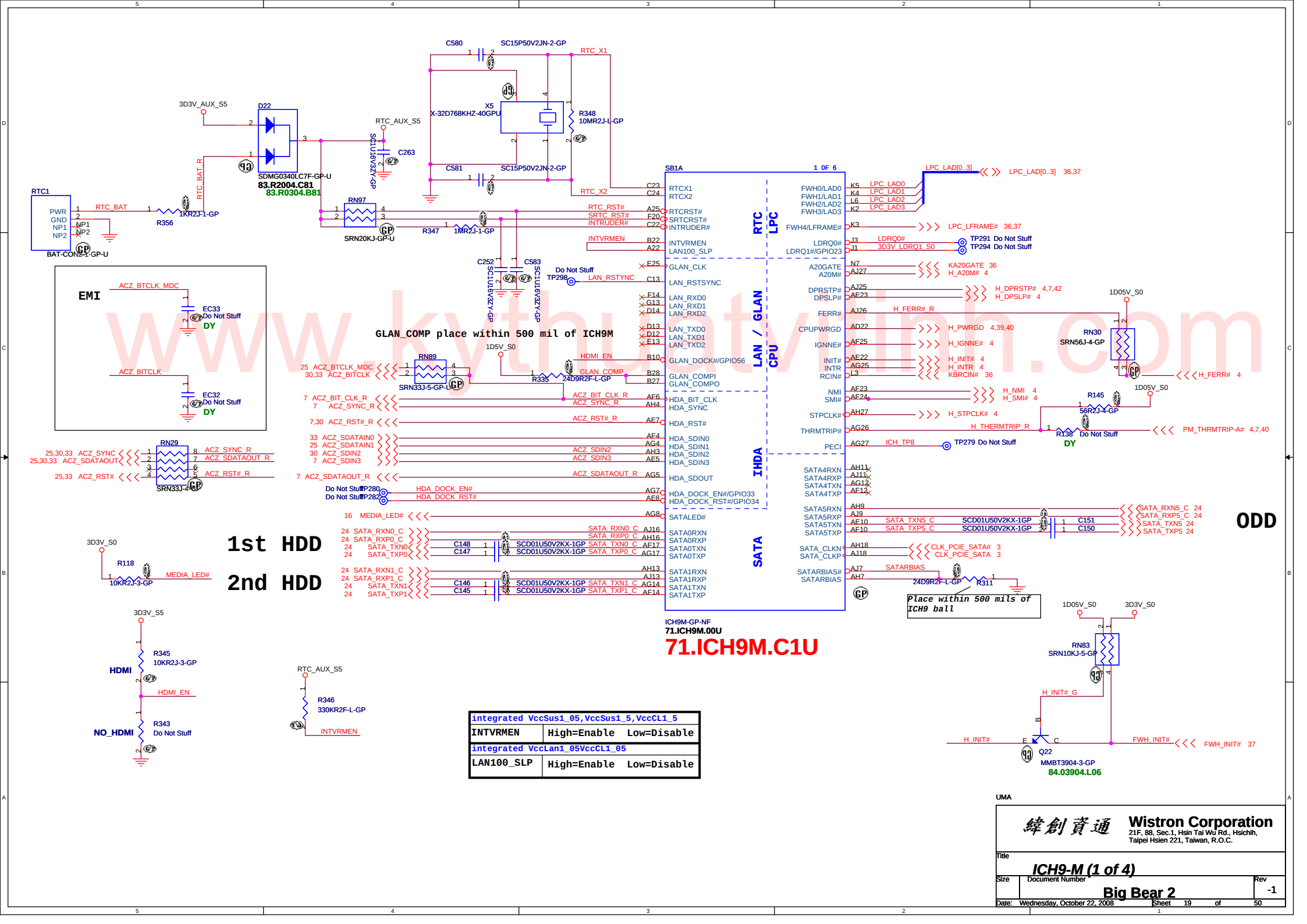
3D3V_S0
5V_CRT_S0
5V_S0
D6 CH551H-30PT-GP 83.R5003.H8H
F1 FUSE-1DTA6V-4GP-U 69.50007.691 69.50007.771
5V_CRT_DDC
RN70 SRN2K2J-1-GP
RN69 SRN2KJ-2-GP
Q15 2N7002EDW-GP 84.DMN66.03F
CRT_IN#_R
DAT_DDC1_5
CLK_DDC1_5
7 GMCH_DDCDATA
7 GMCH_DDCCLK
RN1 SRN0J-6-GP UMA
30 CRT_DDCDATA
30 CRT_DDCCLK

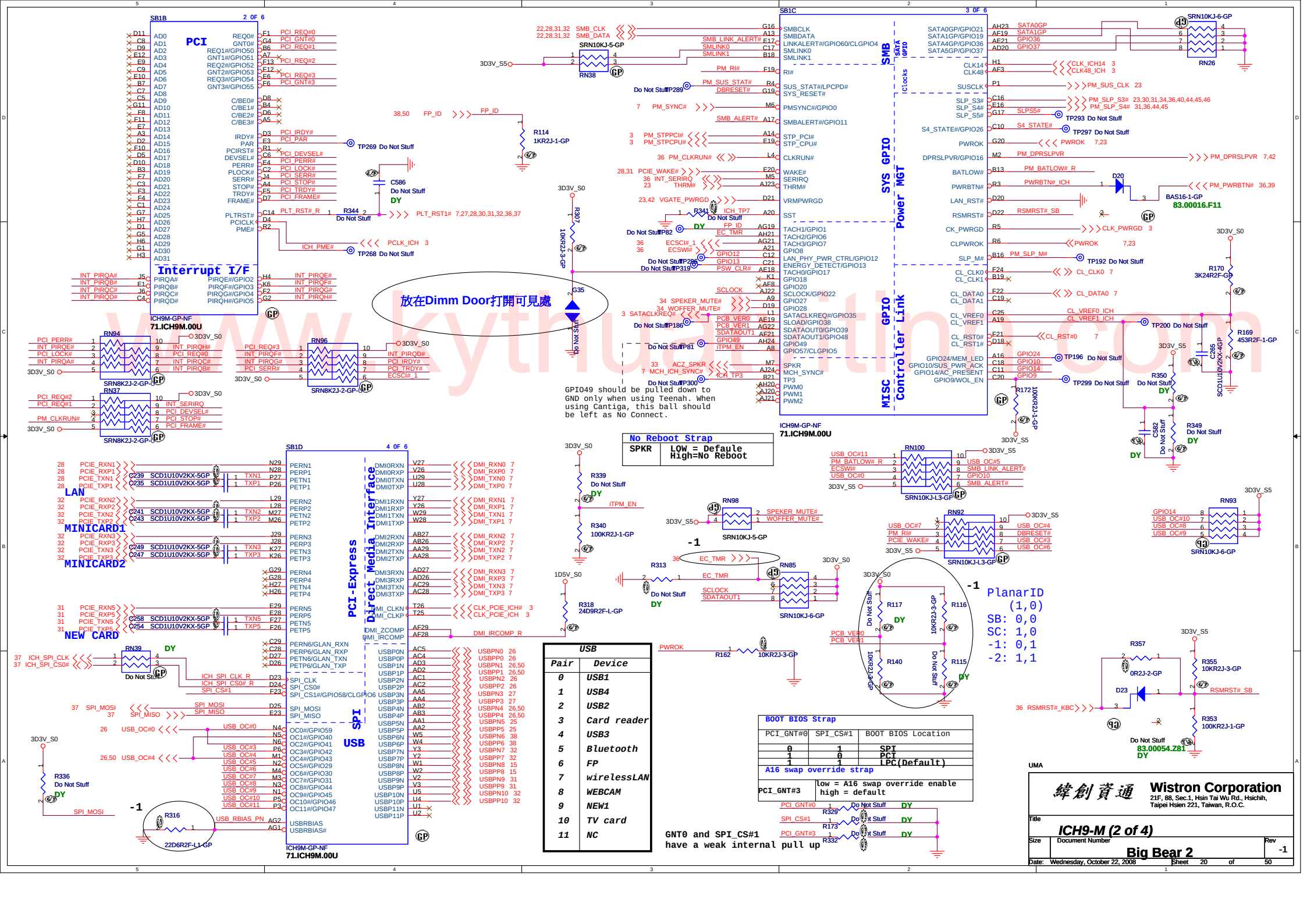
UMA

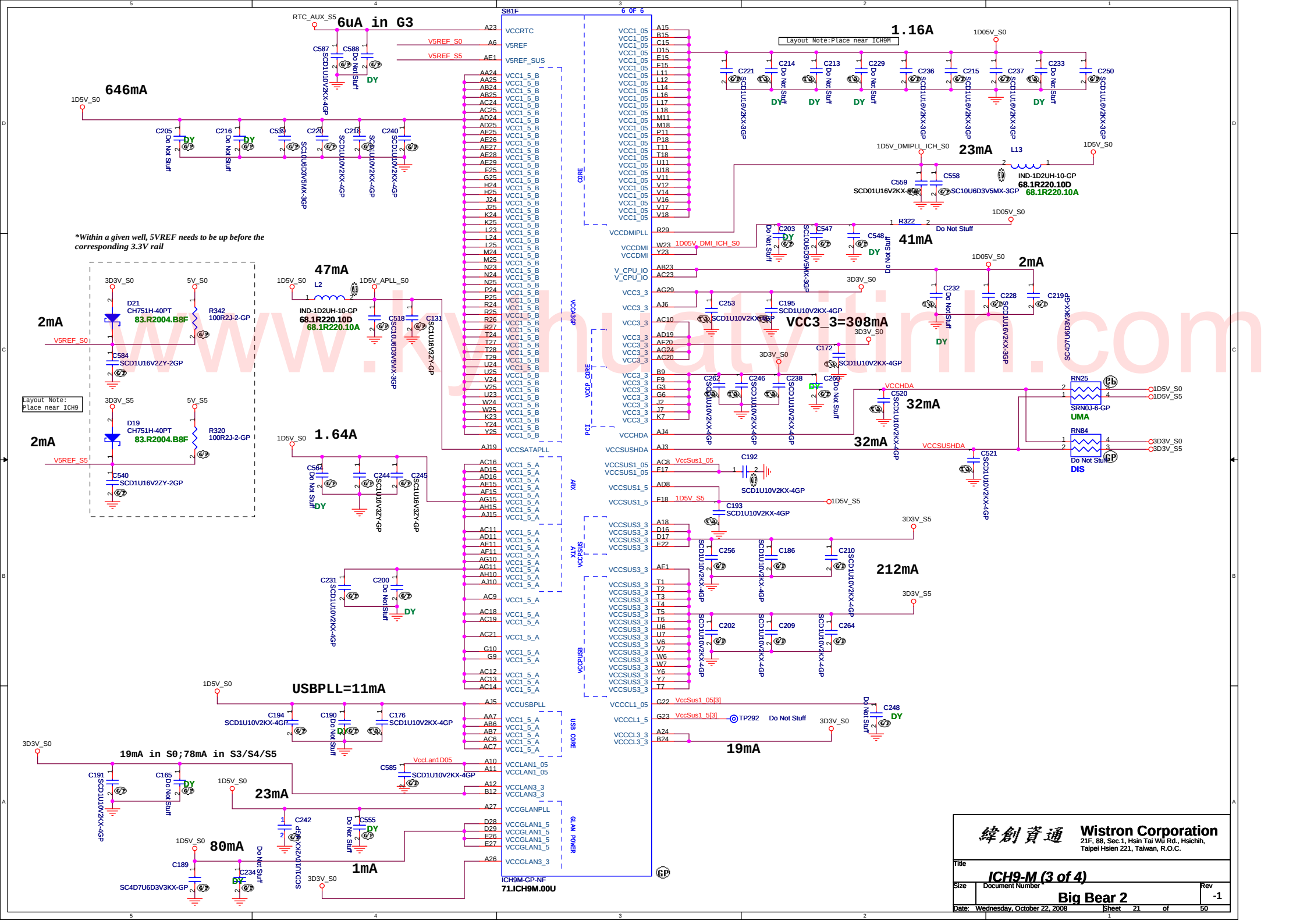
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

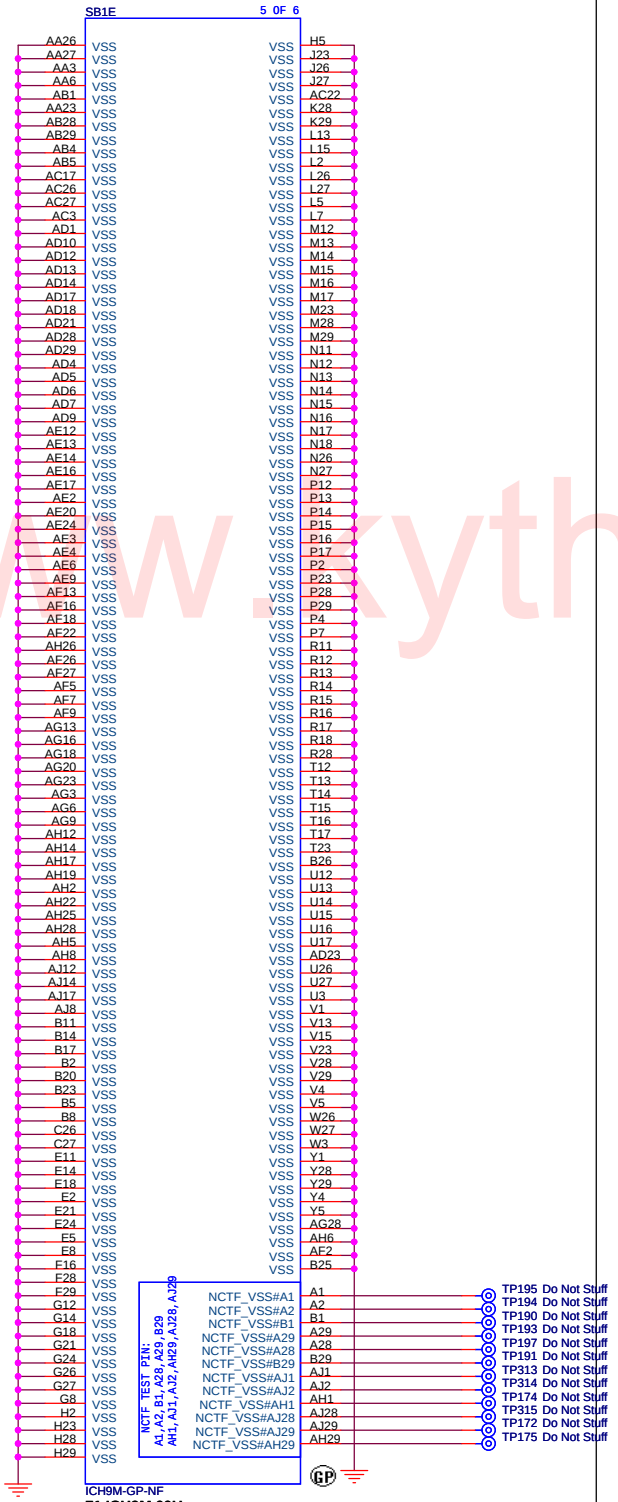
Title	***CRT Connector***	
Size	Document Number **Big Bear 2**	Rev -1
Date: Wednesday, October 22, 2008	Sheet 17 of 50	

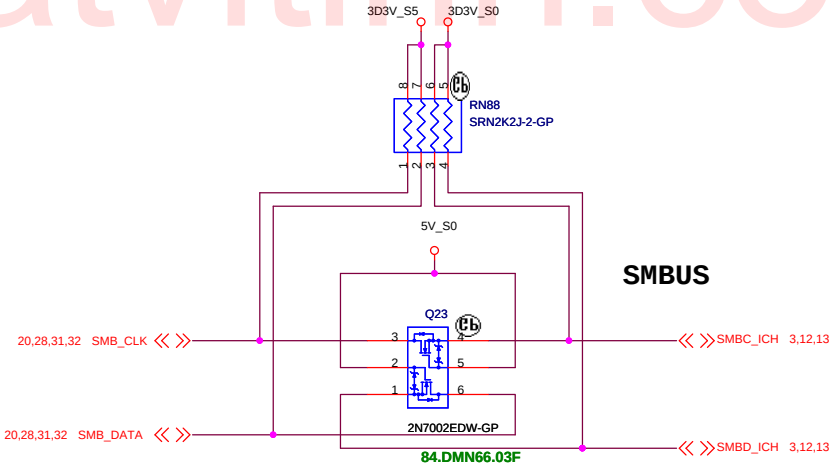



RTC1
BAT-CON2-1-GP-U
RTC_BAT
R356
1KR2J-1-GP
RTC_BAT_R
D22
SDMG0340LC7F-GP-U
83.R2004.C81
83.R0304.B81
3D3V_AUX_S5
RTC_AUX_S5
C263
SCU16V32Y-GP
C580
C581
SC15P50V2JN-2-GP
X5
X-32D768KHZ-40GPU
R348
10MR2J-L-GP
RTC_X1
RTC_X2
RN97
SRN20KJ-GP-U
R347
1MR2J-1-GP
RTC_RST#
SRTC_RST#
INTRUDER#
INTVRMEN
C252
C583
SCU16V32Y-GP
Do Not Stuff
TP298
LAN_RSTSYNC
EMI
EC33
EC32
Do Not Stuff
DY
ACZ_BTCLK_MDC
ACZ_BITCLK
GLAN_COMP place within 500 mil of ICH9M
RN89
SRN33J-5-GP-U
R335
24D9R2F-L-GP
HDMI_EN
GLAN_COMP
RN29
SRN33J-4-GP
ACZ_SYNC_R
ACZ_SDATAOUT_R
ACZ_RST#_R
ACZ_BIT_CLK_R
ACZ_SDIN2
ACZ_SDIN3
HDA_DOCK_EN#
HDA_DOCK_RST#
MEDIA_LED#
R118
10KR2J-3-GP
1st HDD
2nd HDD
SCD01U50V2KX-1GP
C148
C147
C146
C145
SATA_RXN0_C
SATA_RXP0_C
SATA_TXN0
SATA_TXP0
SATA_RXN1_C
SATA_RXP1_C
SATA_TXN1
SATA_TXP1
SB1A
1 OF 6
RTC
LPC
LAN / GLAN
CPU
IHDA
SATA
RTCX1
RTCX2
RTCRST#
SRTCRST#
INTRUDER#
INTVRMEN
LAN100_SLP
GLAN_CLK
LAN_RSTSYNC
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
GLAN_DOCK#/GPIO56
GLAN_COMPI
GLAN_COMPO
HDA_BIT_CLK
HDA_SYNC
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDOUT
HDA_DOCK_EN#/GPIO33
HDA_DOCK_RST#/GPIO34
SATALED#
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
FWH0/LAD0
FWH1/LAD1
FWH2/LAD2
FWH3/LAD3
FWH4/LFRAME#
LDRQ0#
LDRQ1#/GPIO23
A20GATE
A20M#
DPRSTP#
DPSLP#
FERR#
CPUPWRGD
IGNNE#
INIT#
INTR
RCIN#
NMI
SMI#
STPCLK#
THRMTRIP#
PECI
SATA4RXN
SATA4RXP
SATA4TXN
SATA4TXP
SATA5RXN
SATA5RXP
SATA5TXN
SATA5TXP
SATA_CLKN
SATA_CLKP
SATARBIAS#
SATARBIAS
LPC_LAD[0..3]
LPC_LFRAME#
LDRQ0#
3D3V_LDRQ1_S0
TP291 Do Not Stuff
TP294 Do Not Stuff
KA20GATE
H_A20M#
H_DPRSTP#
H_DPSLP#
H_FERR#_R
H_PWRGD
H_IGNNE#
H_INIT#
H_INTR
KBRCIN#
H_NMI
H_SMI#
H_STPCLK#
H_THERMTRIP_R
ICH_TP8
TP279 Do Not Stuff
SCD01U50V2KX-1GP
C151
C150
SATA_TXN5_C
SATA_TXP5_C
CLK_PCIE_SATA#
CLK_PCIE_SATA
SATARBIAS
24D9R2F-L-GP
R311
Place within 500 mils of ICH9 ball
1D05V_S0
3D3V_S0
RN30
SRN56J-4-GP
R145
56R2J-4-GP
R138
Do Not Stuff
DY
PM_THRMTRIP-A#
RN83
SRN10KJ-5-GP
H_INIT# G
Q22
MMBT3904-3-GP
84.03904.L06
FWH_INIT#
ODD
SATA_RXN5_C
SATA_RXP5_C
SATA_TXN5
SATA_TXP5
HDMI
NO_HDMI
R345
10KR2J-3-GP
R343
Do Not Stuff
R346
330KR2F-L-GP
INTVRMEN
integrated VccSus1_05,VccSus1_5,VccCL1_5
INTVRMEN
High=Enable Low=Disable
integrated VccLan1_05VccCL1_05
LAN100_SLP
High=Enable Low=Disable
ICH9M-GP-NF
71.ICH9M.00U
71.ICH9M.C1U
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH9-M (1 of 4)
Size
Document Number
Big Bear 2
Rev
-1
Date: Wednesday, October 22, 2008
Sheet 19 of 50


SB1B
2 0F 6
PCI
Interrupt I/F
ICH9M-GP-NF
71.ICH9M.00U
SB1C
3 0F 6
SMB
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
ICH9M-GP-NF
71.ICH9M.00U
SB1D
4 0F 6
PCI-Express
Direct Media Interface
SPI
USB
ICH9M-GP-NF
71.ICH9M.00U
放在Dimm Door打開可見處
GPIO049 should be pulled down to GND only when using Teenah. When using Cantiga, this ball should be left as No Connect.
No Reboot Strap
SPKR
LOW = Defaule
High=No Reboot
USB
Pair
Device
0
USB1
1
USB4
2
USB2
3
Card reader
4
USB3
5
Bluetooth
6
FP
7
wirelessLAN
8
WEBCAM
9
NEW1
10
TV card
11
NC
GNT0 and SPI_CS#1 have a weak internal pull up
BOOT BIOS Strap
PCI_GNT#0
SPI_CS#1
BOOT BIOS Location
0
1
SPI
1
0
PCI
1
1
LPC(Default)
A16 swap override strap
PCI_GNT#3
low = A16 swap override enable
high = default
PlanarID
(1,0)
SB: 0,0
SC: 1,0
-1: 0,1
-2: 1,1
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH9-M (2 of 4)
Size
Document Number
Big Bear 2
Rev
-1
Date: Wednesday, October 22, 2008
Sheet 20 of 50


6uA in G3
646mA
1.16A
23mA
41mA
2mA
47mA
1.64A
VCC3_3=308mA
32mA
212mA
USBPLL=11mA
19mA in S0;78mA in S3/S4/S5
80mA
1mA
19mA
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
Layout Note:Place near ICH9M
Layout Note: Place near ICH9
Do Not Stuff
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
ICH9-M (3 of 4)
Big Bear 2
Wednesday, October 22, 2008
71.ICH9M.00U



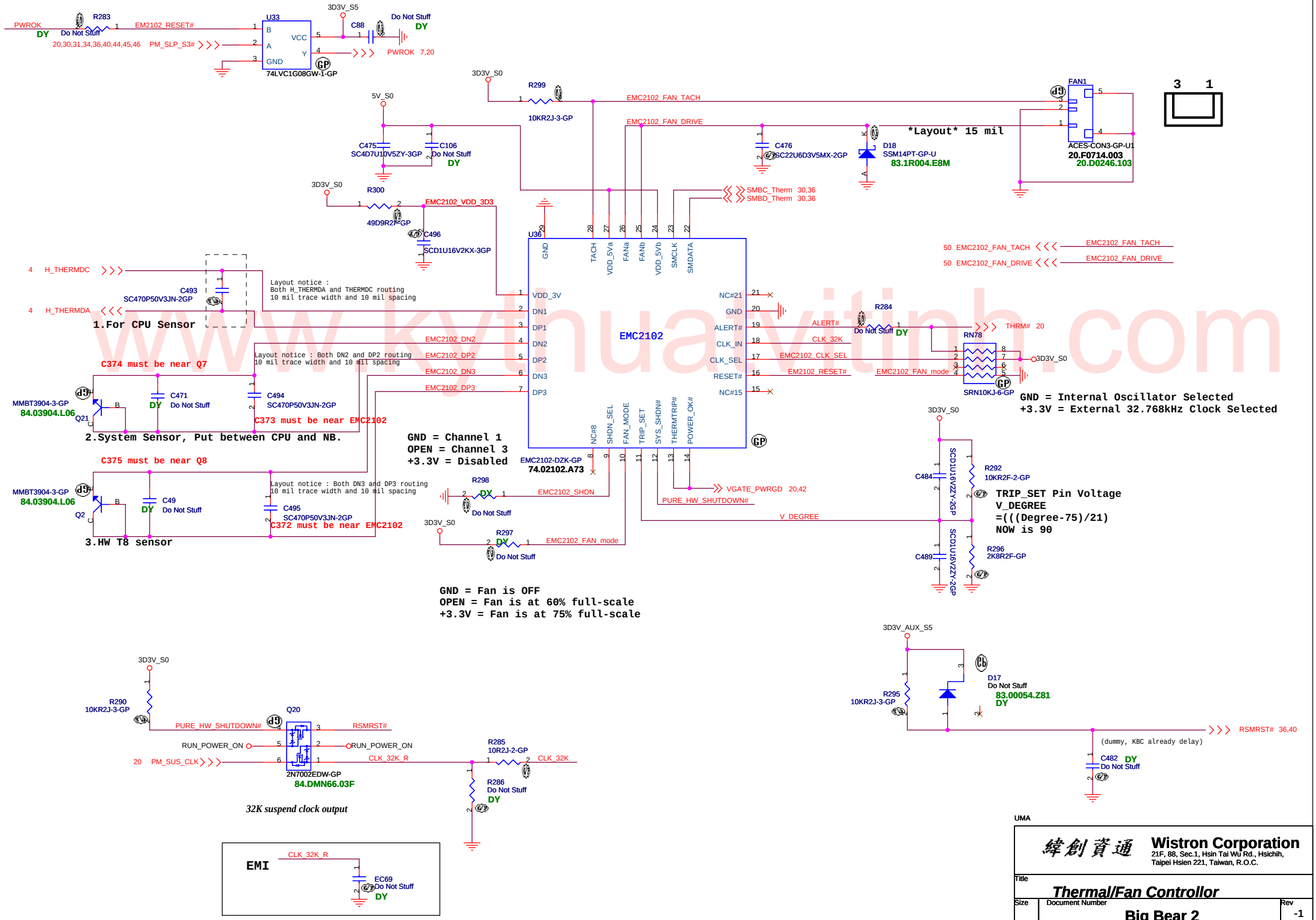


緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***ICH9-M (4 of 4)***

Size | Document Number: **Big Bear 2** | Rev: -1

Date: Wednesday, October 22, 2008 | Sheet 22 of 50



UMA

緯創資通 **Wistron Corporation**
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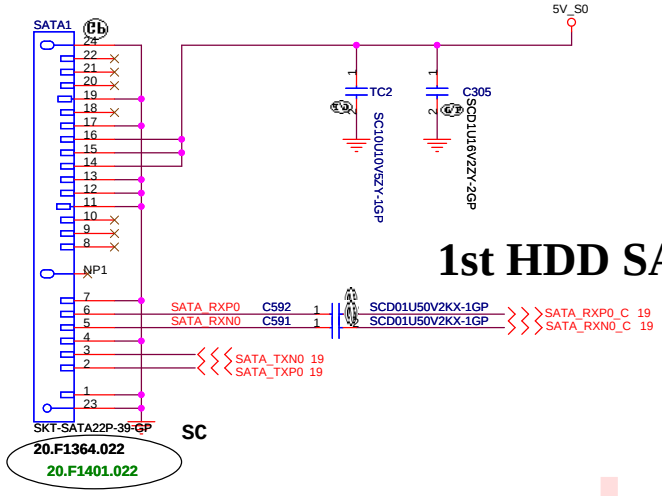
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Thermal/Fan Controllor***

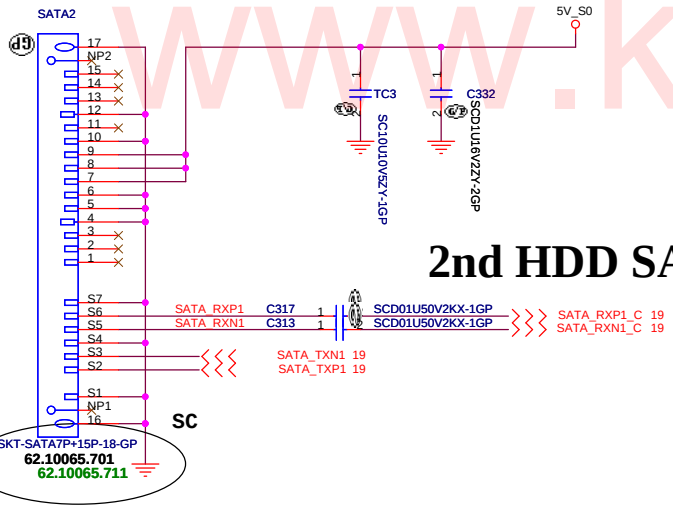
Size	Document Number	Rev
	Big Bear 2	-1

Date: Wednesday, October 22, 2008 Sheet 23 of 50

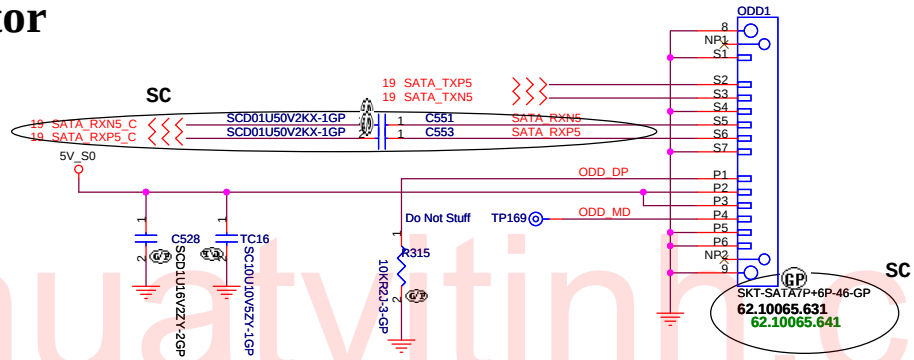
SATA ODD Connector



1st HDD SATA Connector



2nd HDD SATA Connector

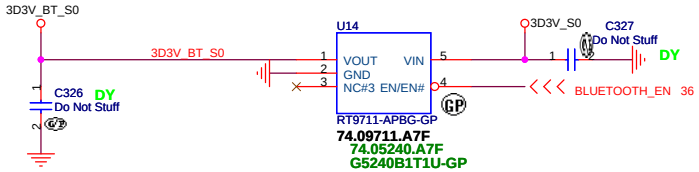


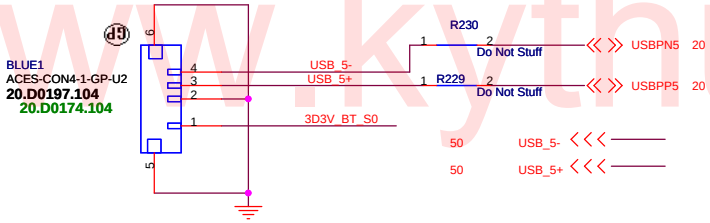
UMA

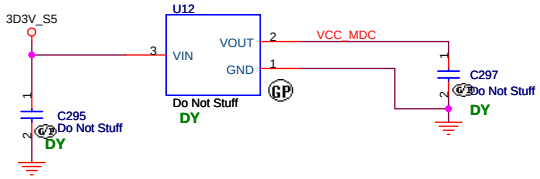
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: HDD & ODD		
Size	Document Number: Big Bear 2	Rev: -1
Date: Wednesday, October 22, 2008	Sheet 24 of 50	

BLUETOOTH MODULE

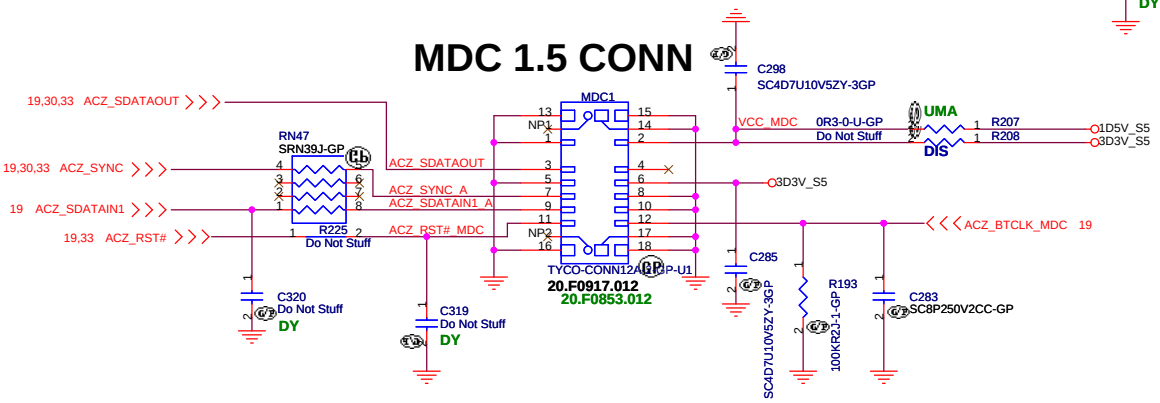
1.5A / High Active Voltage 2V

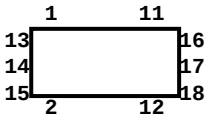






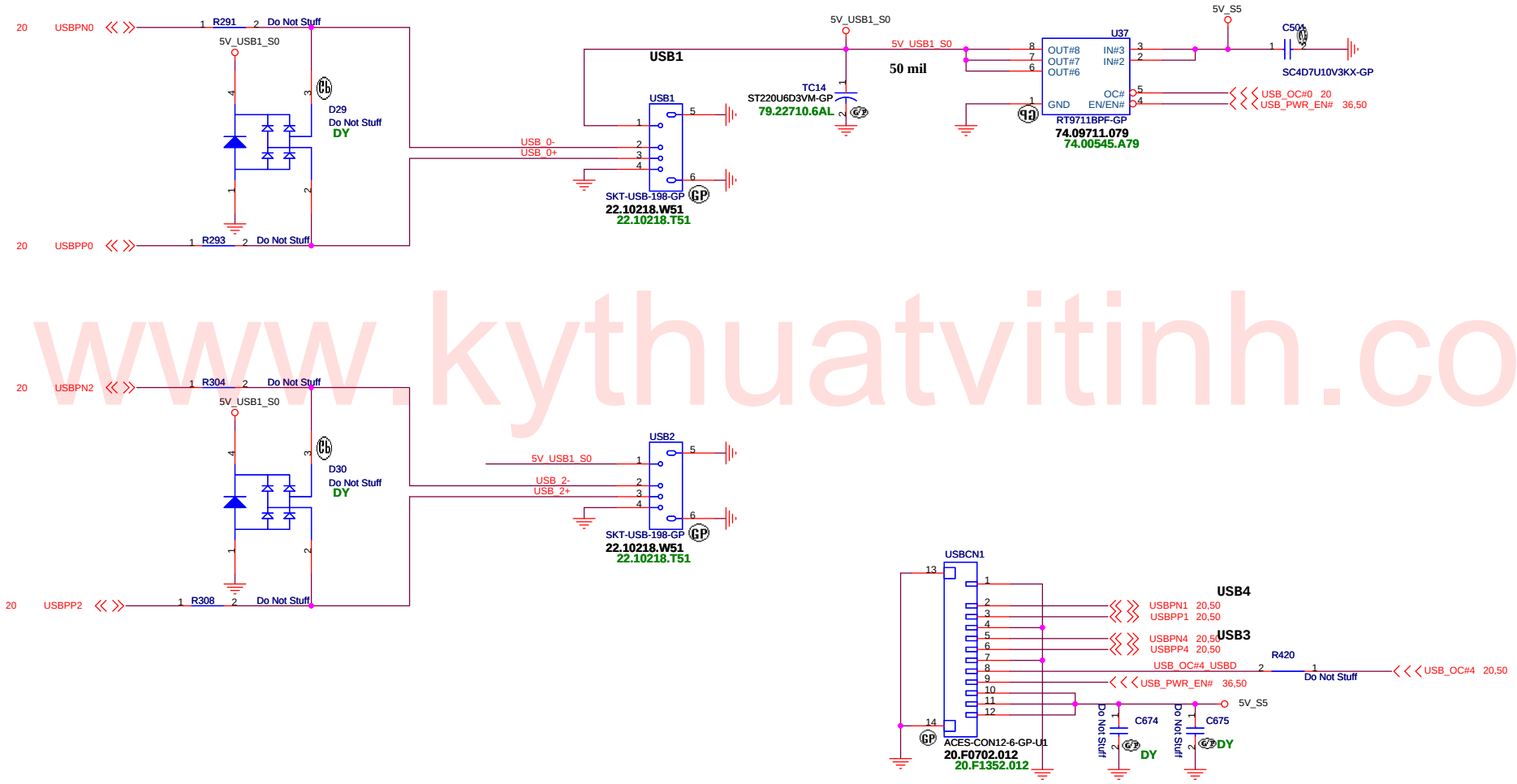
MDC 1.5 CONN





UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***BLUETOOTH & MDC***	
Size	Document Number **Big Bear 2**	Rev -1
Date: Wednesday, October 22, 2008	Sheet 25 of 50	



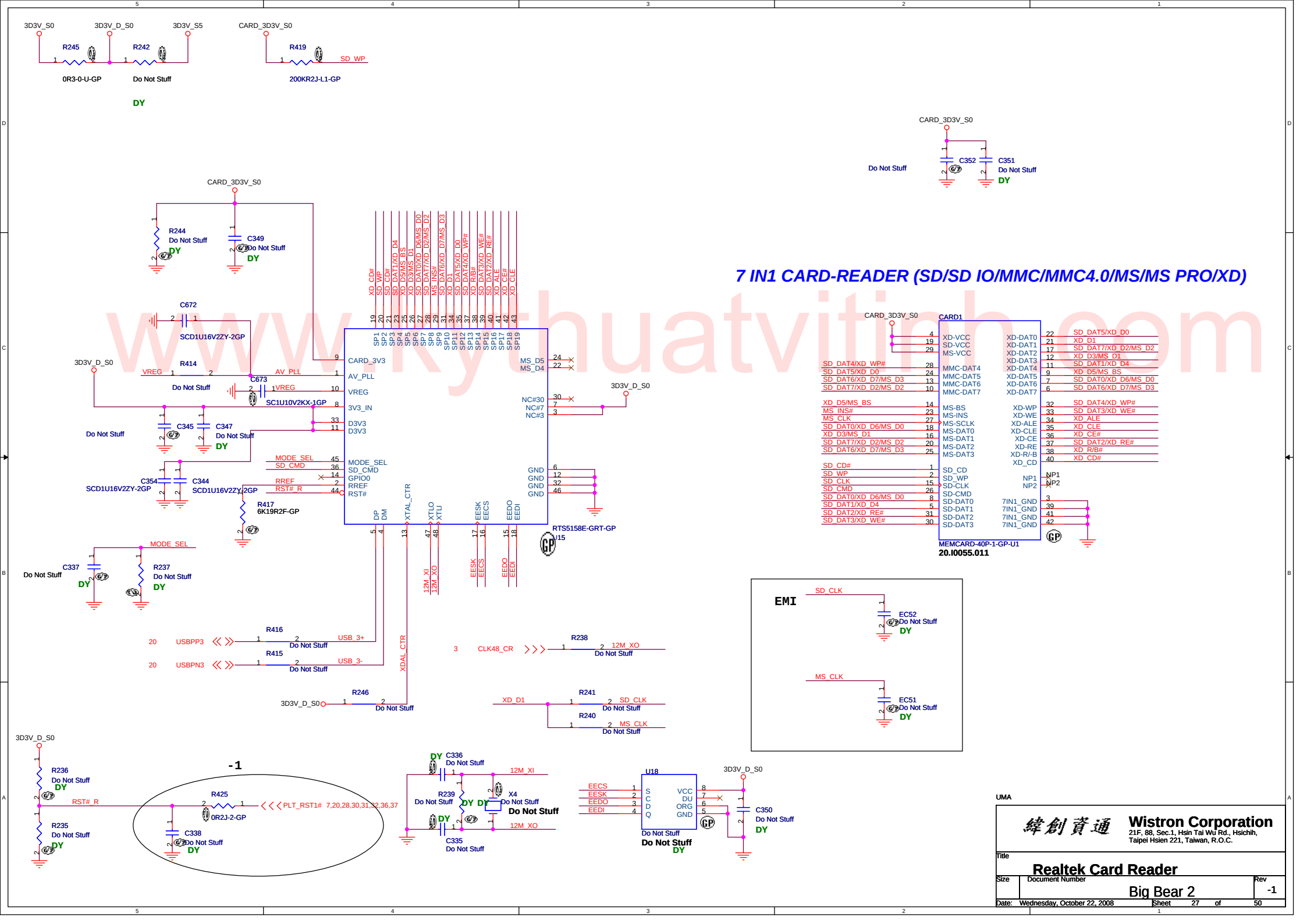
UMA

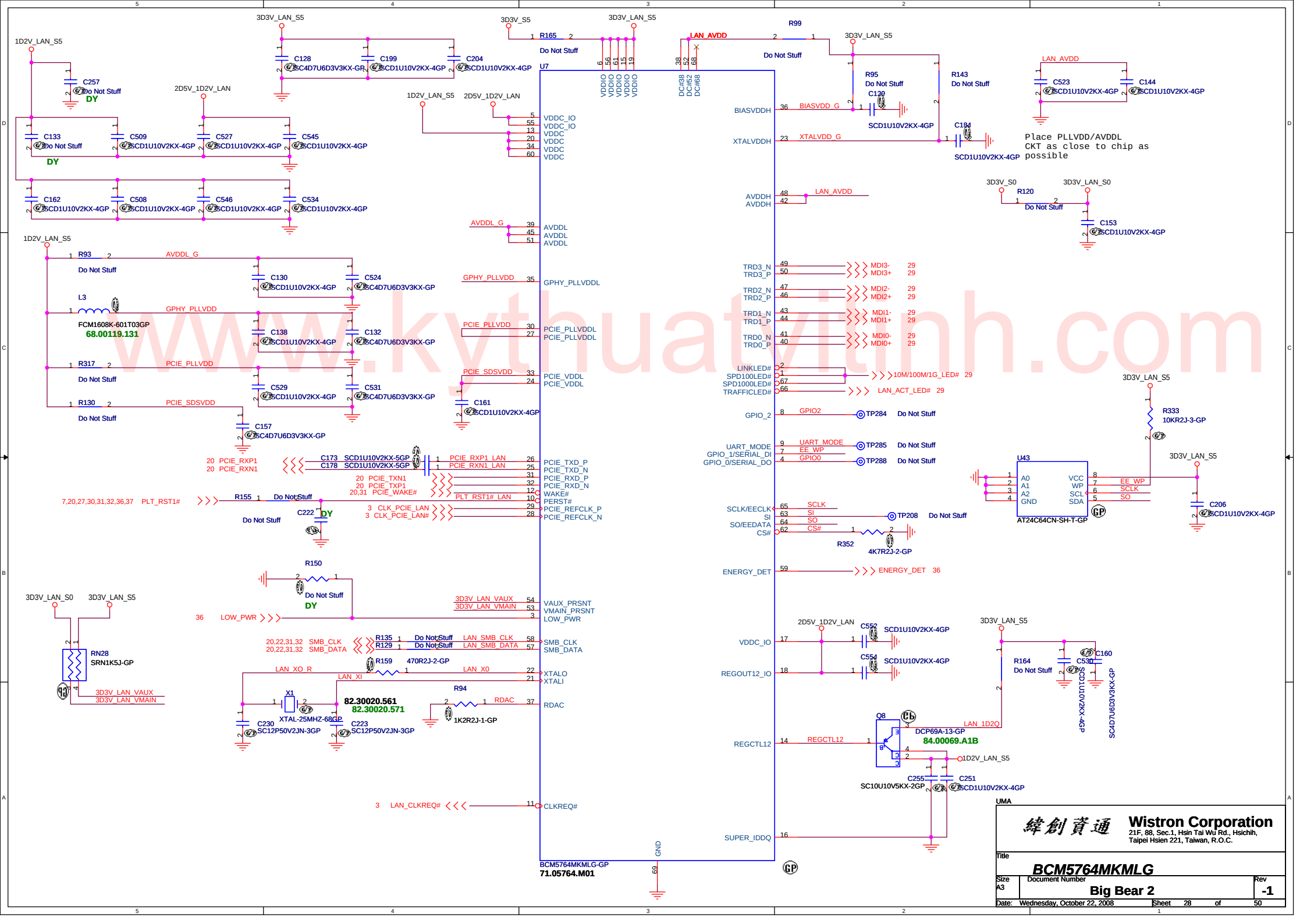
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB connector**

Size	Document Number	Rev
	Big Bear 2	-1

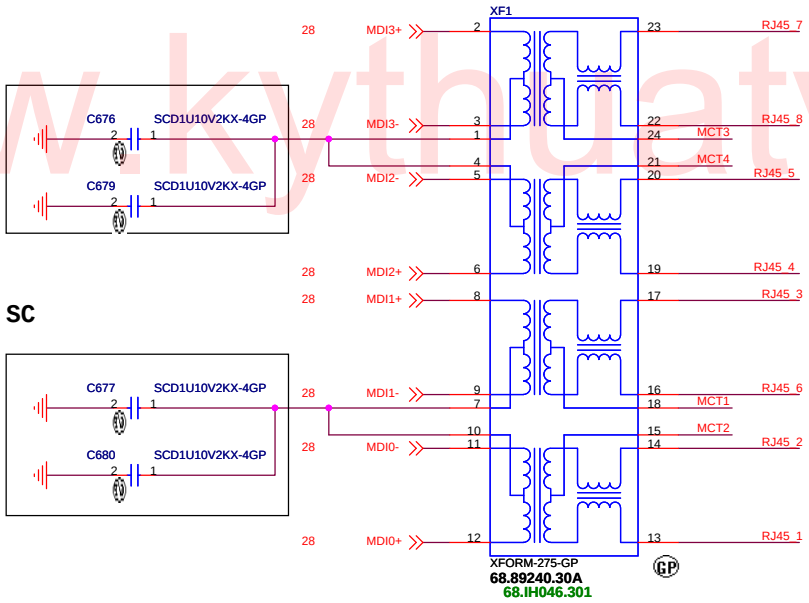
Date: Wednesday, October 22, 2008 Sheet 26 of 50

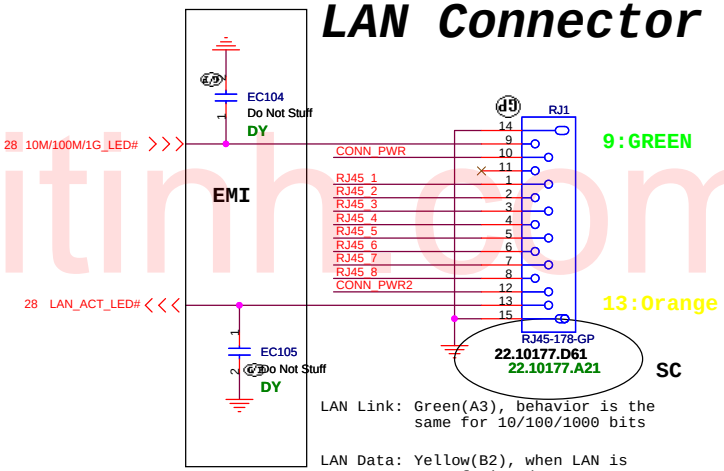

7 IN1 CARD-READER (SD/SD IO/MMC/MMC4.0/MS/MS PRO/XD)
www.kythuatvitinh.com
RTS5158E-GRT-GP
MEMCARD-40P-1-GP-U1
20.I0055.011
EMI
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Realtek Card Reader
Big Bear 2
Wednesday, October 22, 2008

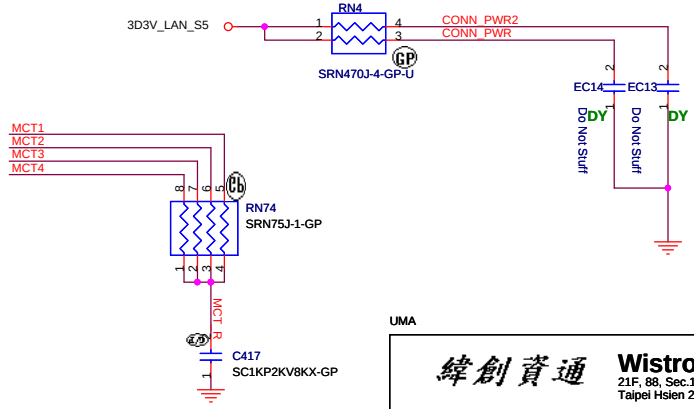


LAN Connector

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.







UMA

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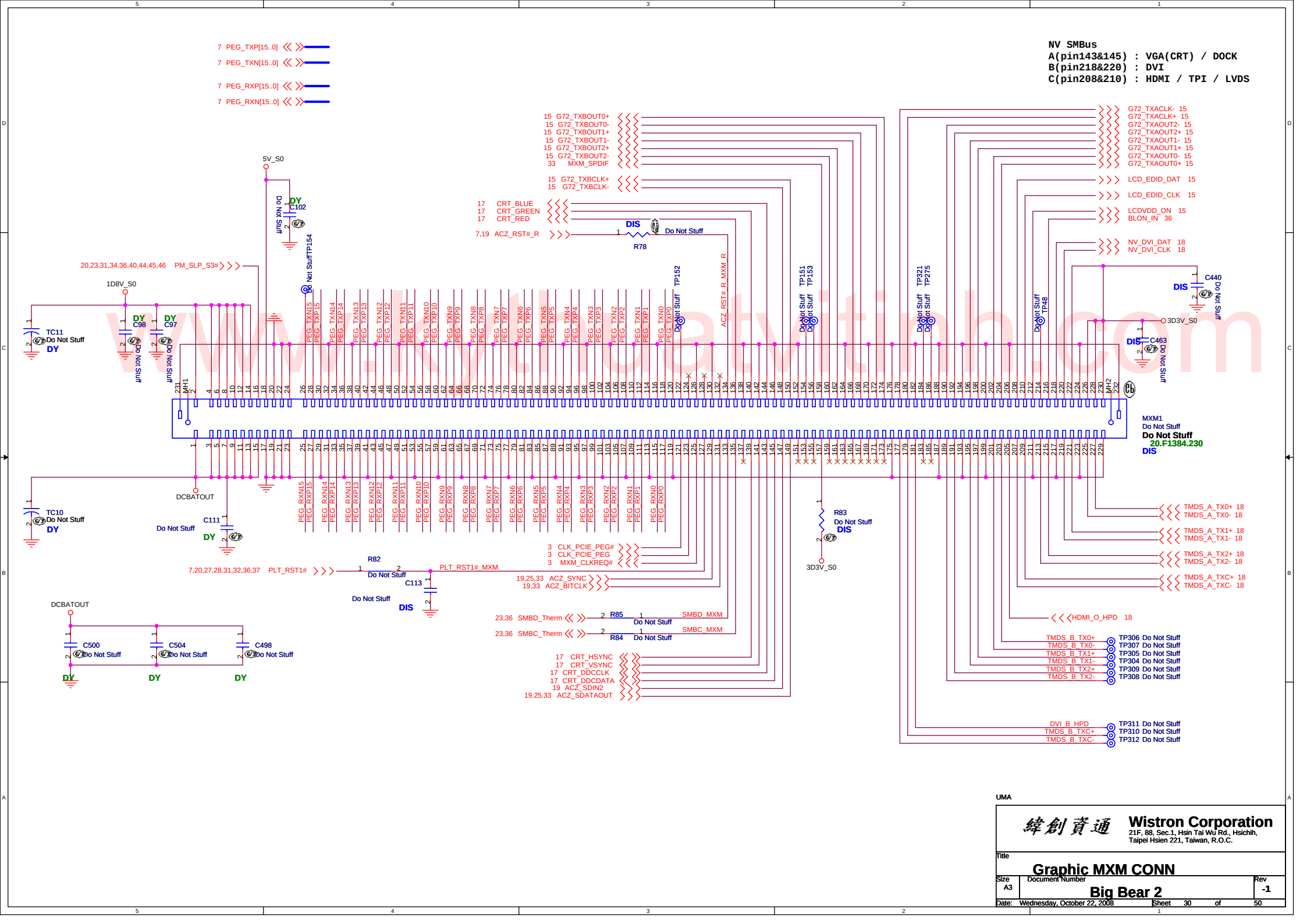
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

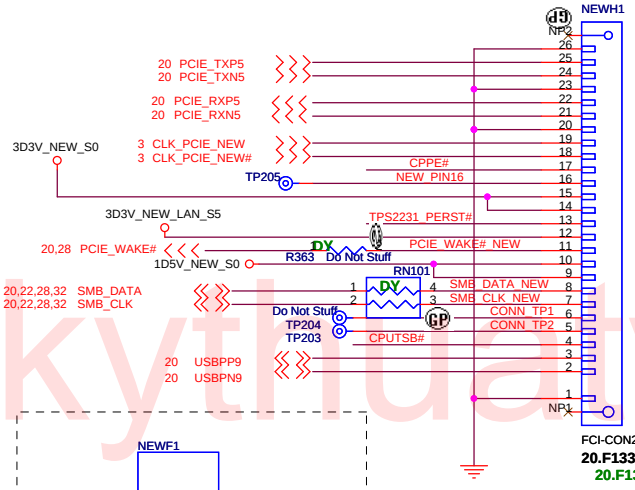
Title		
LAN CONN		
Size: A3	Document Number: Big Bear 2	Rev: -1
Date: Wednesday, October 22, 2008	Sheet 29 of 50	

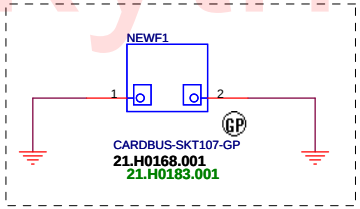

NV SMBus
A(pin143&145) : VGA(CRT) / DOCK
B(pin218&220) : DVI
C(pin208&210) : HDMI / TPI / LVDS
7 PEG_TXP[15..0]
7 PEG_TXN[15..0]
7 PEG_RXP[15..0]
7 PEG_RXN[15..0]
5V_S0
1D8V_S0
3D3V_S0
DCBATOUT
UMA
MXM1
Do Not Stuff
20.F1384.230
DIS
DY
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Graphic MXM CONN
Big Bear 2
Size A3
Rev -1
Date: Wednesday, October 22, 2008
Sheet 30 of 50

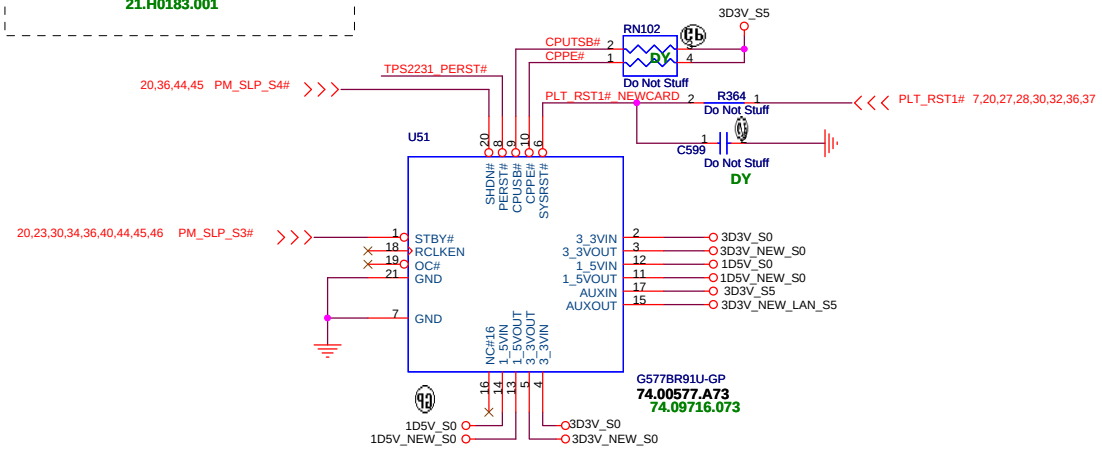
NEWCARD Connector

Reserve the symbol
for bottom side
connector

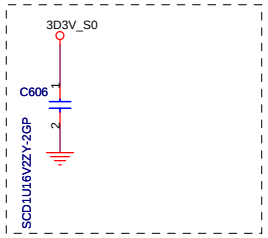
TOP VIEW



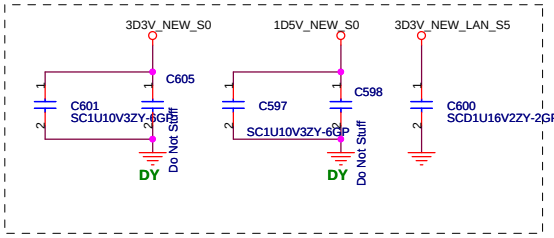




Place them Near to Chip



Place them Near to Connector



UMA

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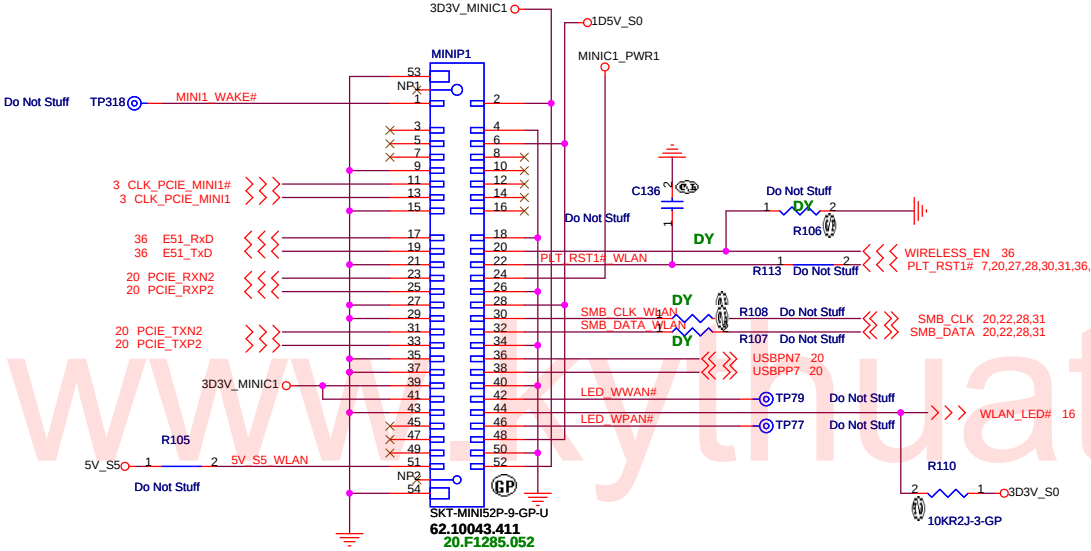
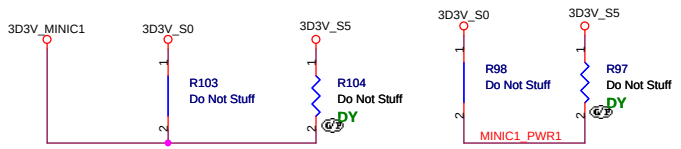
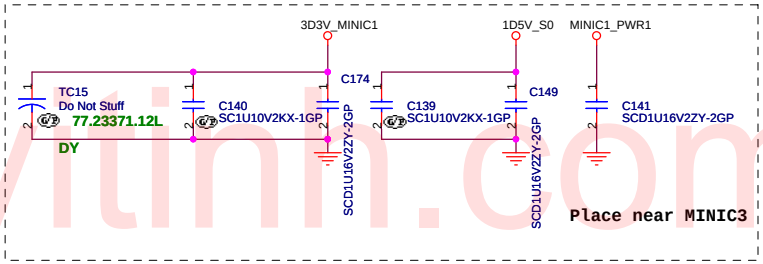
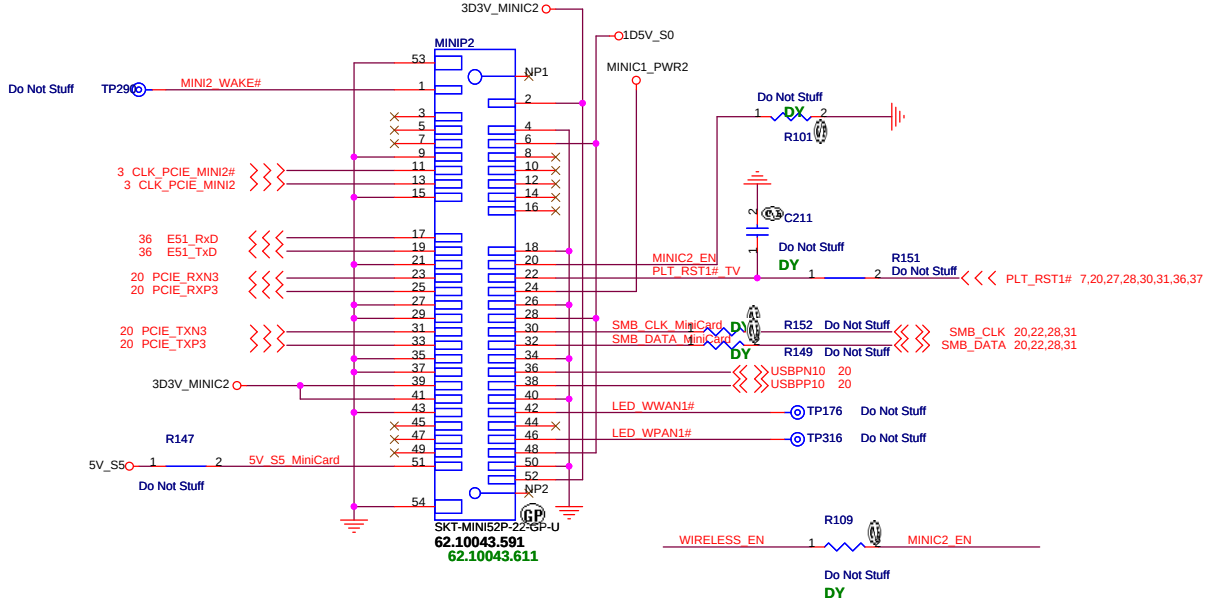
Title: NEW CARD	
Size	Document Number: Big Bear 2 — Rev: -1
Date: Wednesday, October 22, 2008	Sheet 31 of 50

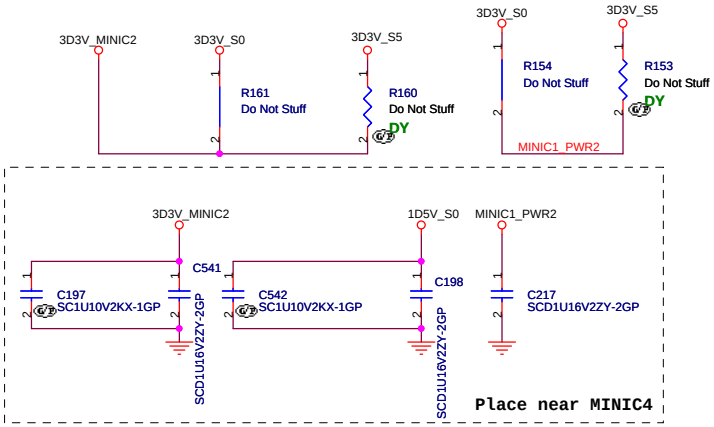
Mini Card Connector(WLAN)











UMA

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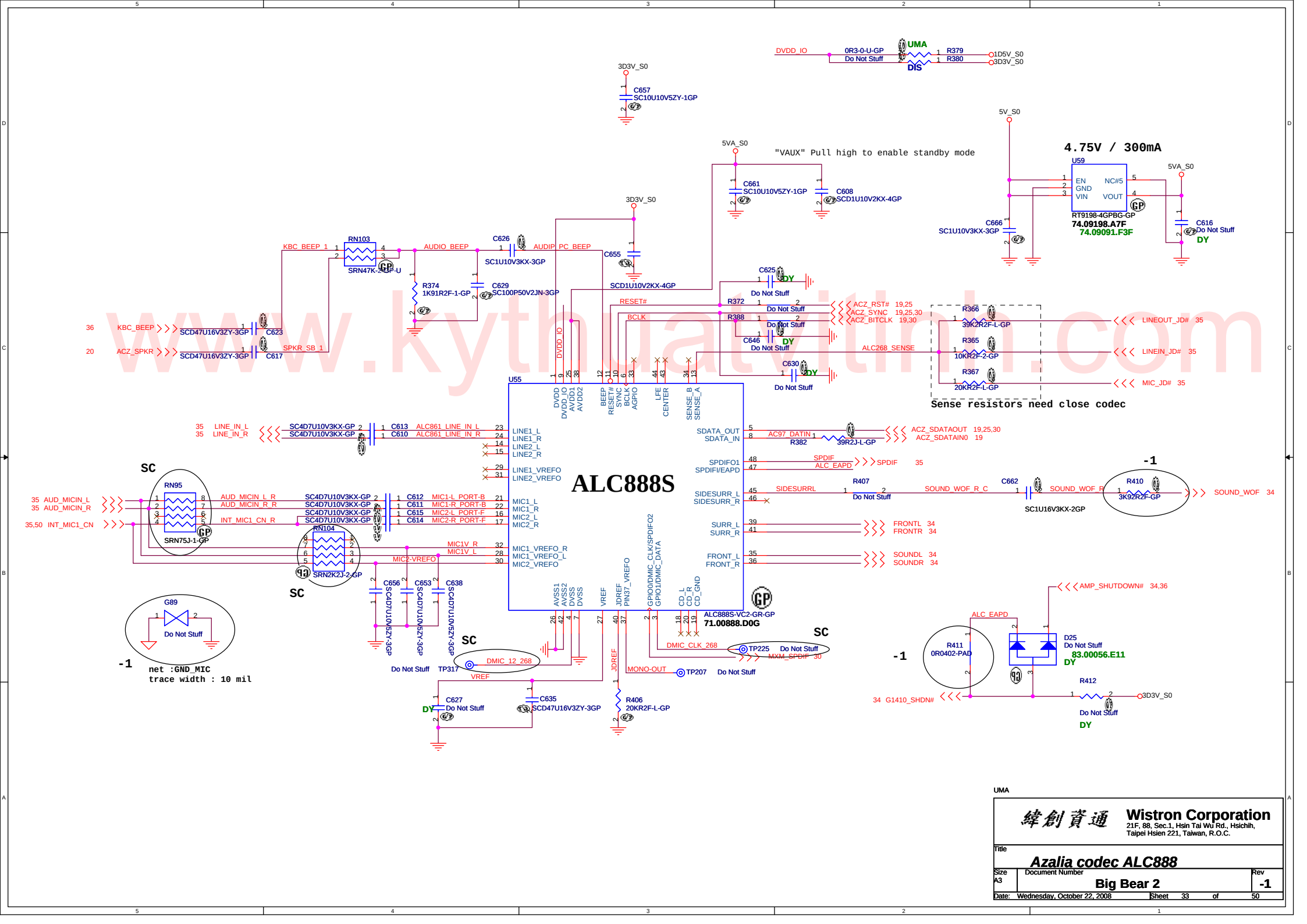
Taipei Hsien 221, Taiwan, R.O.C.

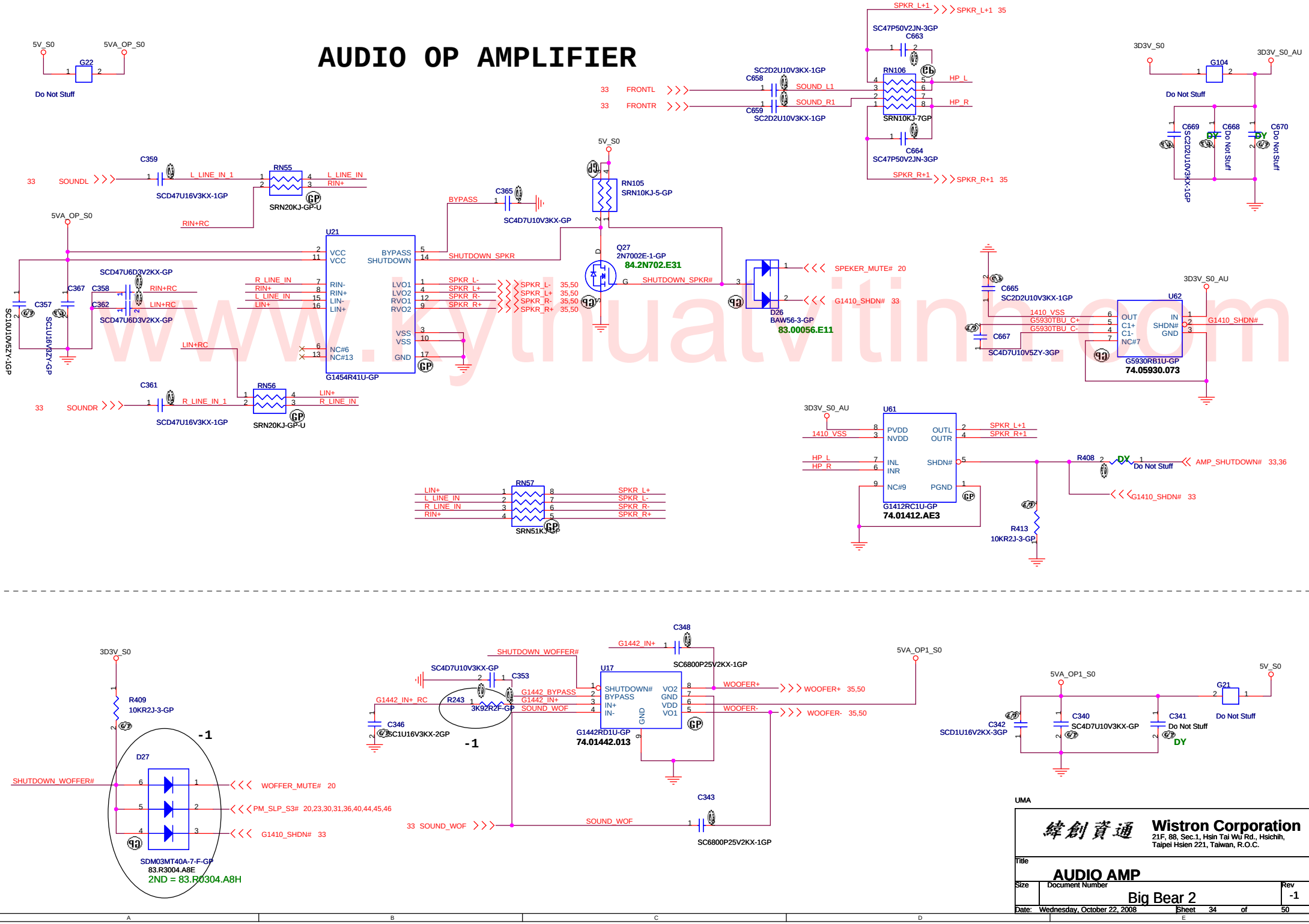
Title: **MINI CARD**

Size: A3 | Document Number: **Big Bear 2** | Rev: **-1**

Date: Wednesday, October 22, 2008 | Sheet 32 of 50


ALC888S
U55
ALC888S-VC2-GR-GP
71.00888.D0G
"VAUX" Pull high to enable standby mode
4.75V / 300mA
U59
RT9198-4GPBG-GP
74.09198.A7F
74.09091.F3F
Sense resistors need close codec
net :GND_MIC
trace width : 10 mil
UMA
DIS
SC
DY
-1
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Azalia codec ALC888
Big Bear 2
Wednesday, October 22, 2008
Sheet 33 of 50

AUDIO OP AMPLIFIER



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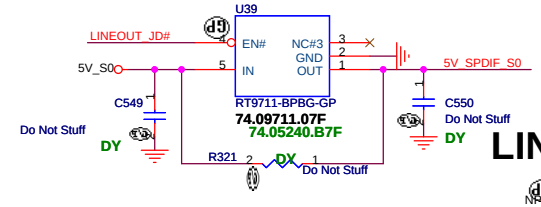
Taipei Hsien 221, Taiwan, R.O.C.

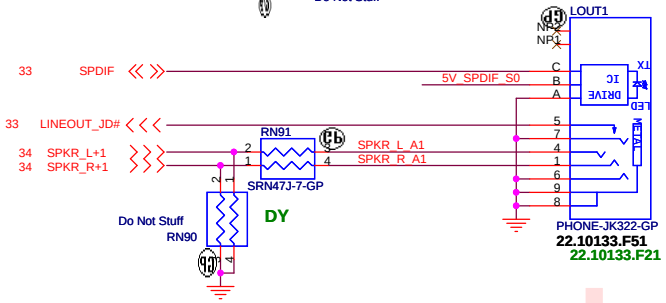
Title: **AUDIO AMP**

Size	Document Number	Rev
	Big Bear 2	-1

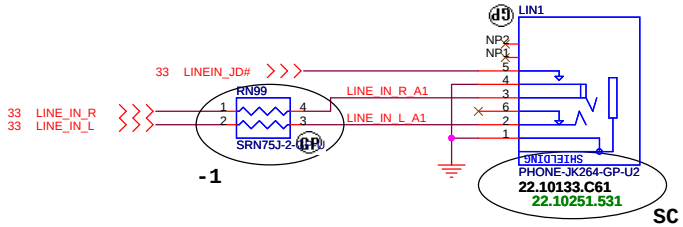
Date: Wednesday, October 22, 2008 Sheet 34 of 50

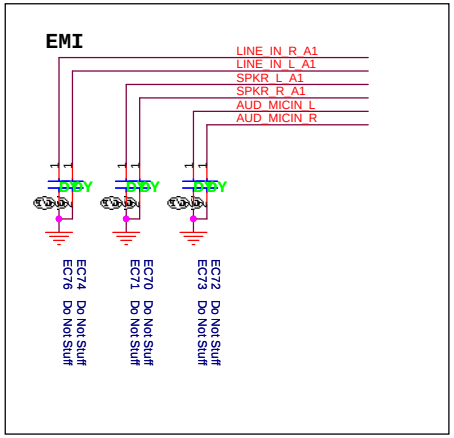


LINE OUT

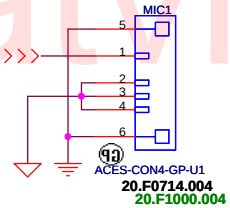


LINE IN

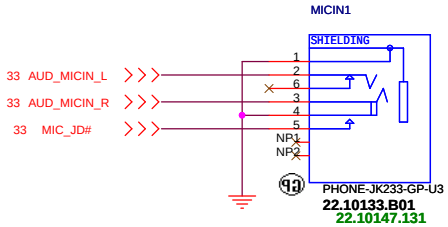




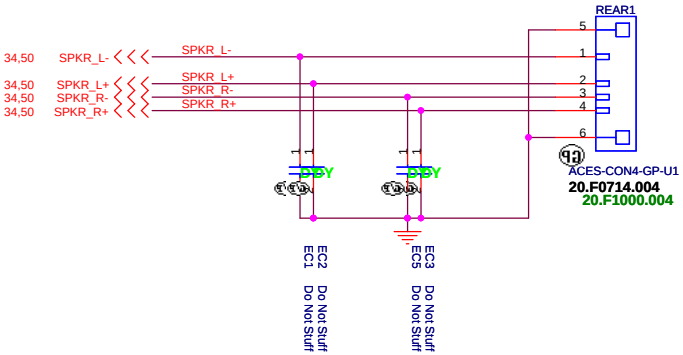
INT. MIC



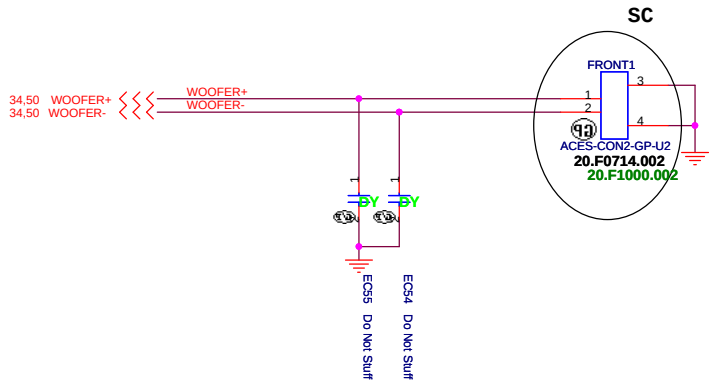
MIC IN



REAR Speaker

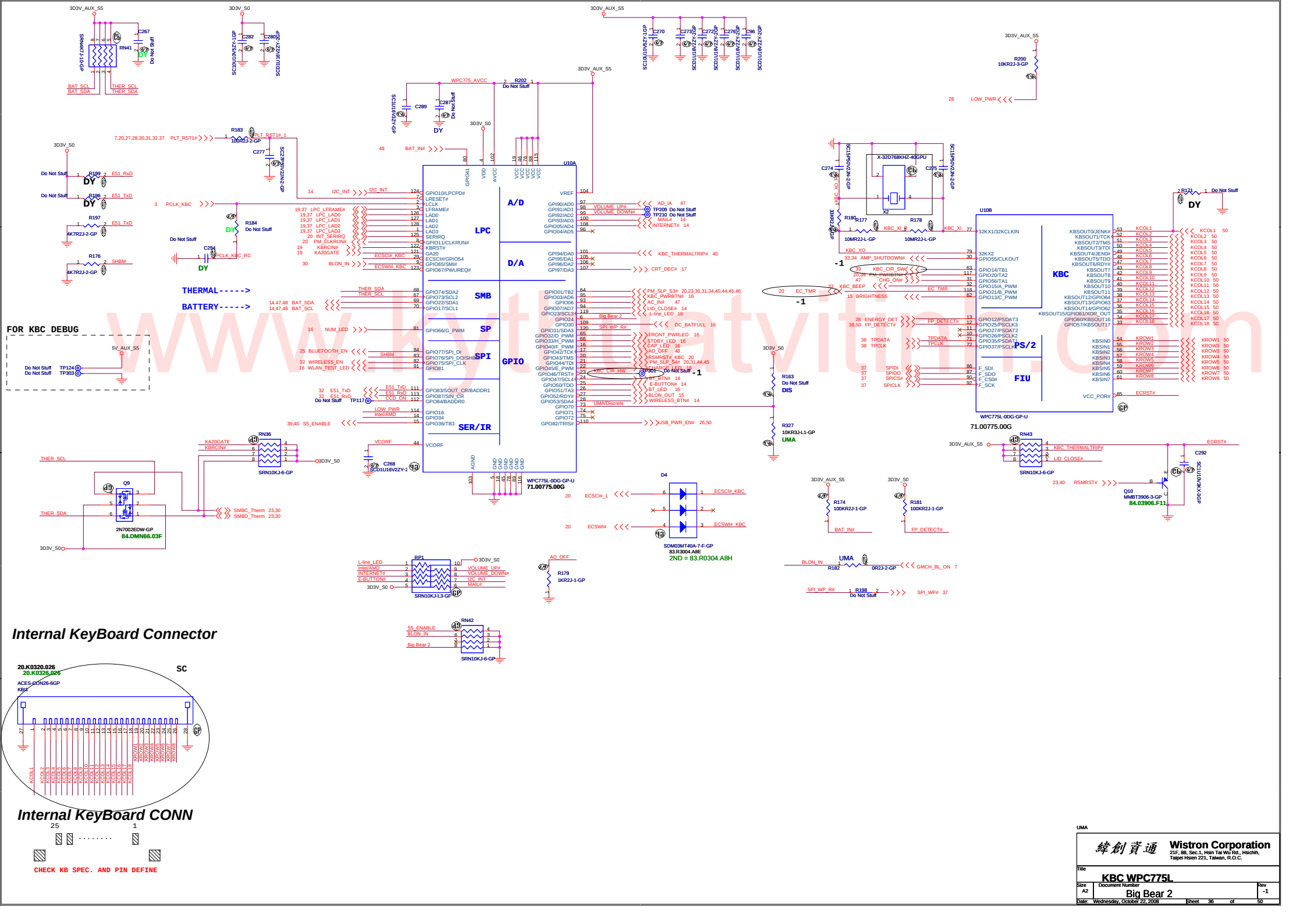


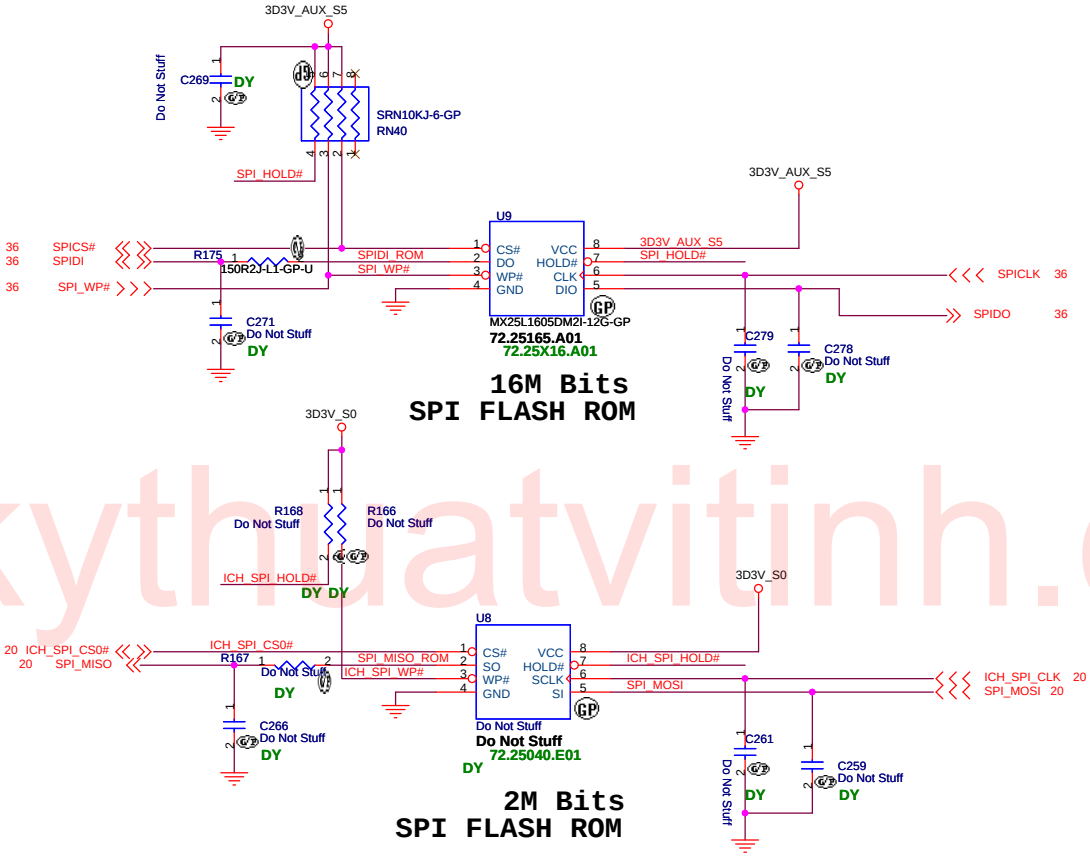
SUBWOOFER



UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**AUDIO_JACK**	
Size	Document Number: Big Bear 2	Rev: -1
Date: Wednesday, October 22, 2008	Sheet 35 of 50	

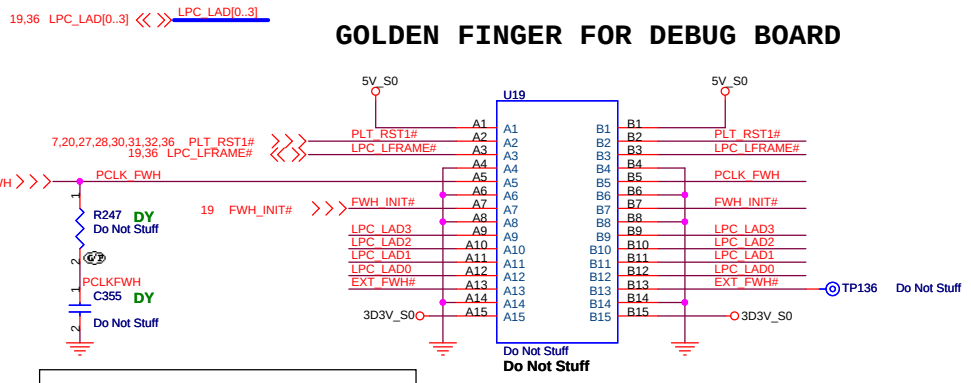


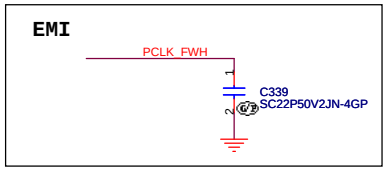


TOP VIEW

A15	(B1)
A14	(B2)
⋮	⋮
A2	(B14)
A1	(B15)

(BOTTOM VIEW)





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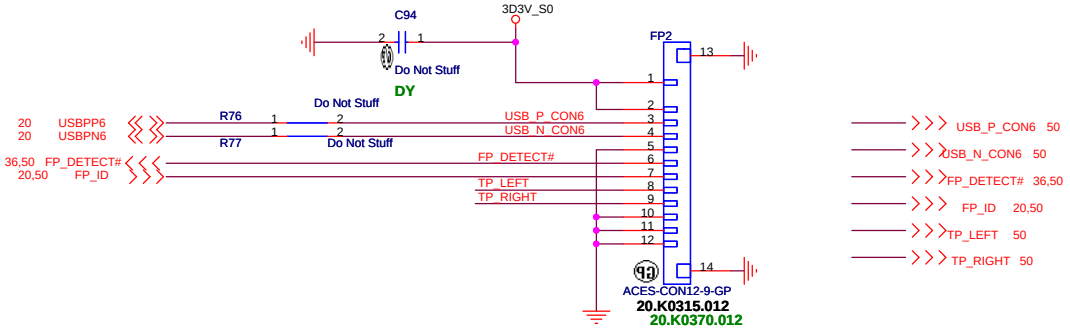
Taipei Hsien 221, Taiwan, R.O.C.

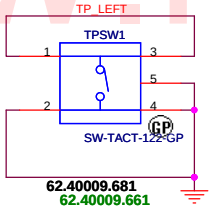
Title: **BIOS**

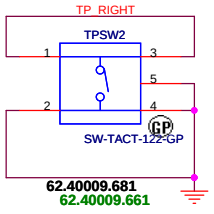
Size	Document Number	Rev
	Big Bear 2	-1

Date: Wednesday, October 22, 2008 Sheet 37 of 50

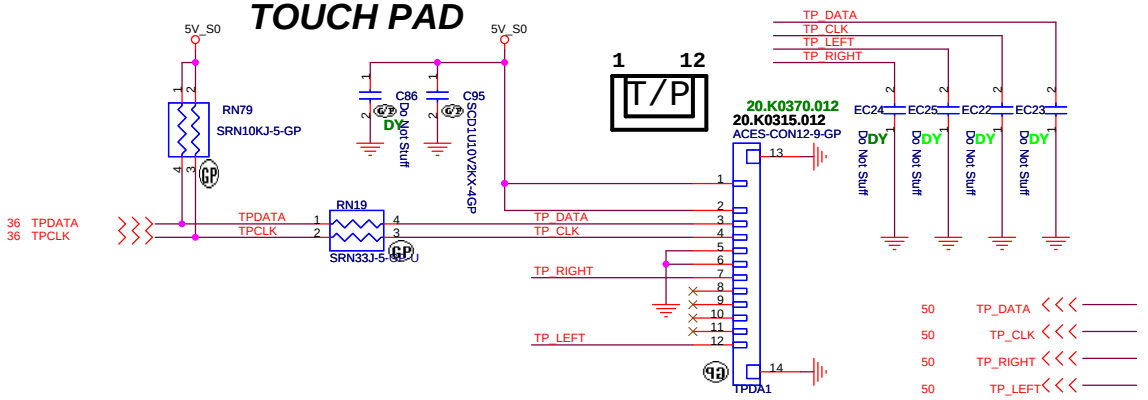
Finger printer







TOUCH PAD



UMA

緯創資通 **Wistron Corporation**
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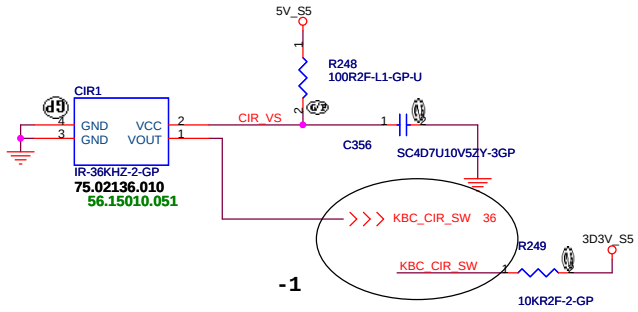
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Finger Printer and Touch PAD**

Size	Document Number	Rev
A3	Big Bear 2	-1

Date: Wednesday, October 22, 2008 Sheet 38 of 50

CIR Module



Check test point

Test Point放在Dimm Door打開可量測處

UMA

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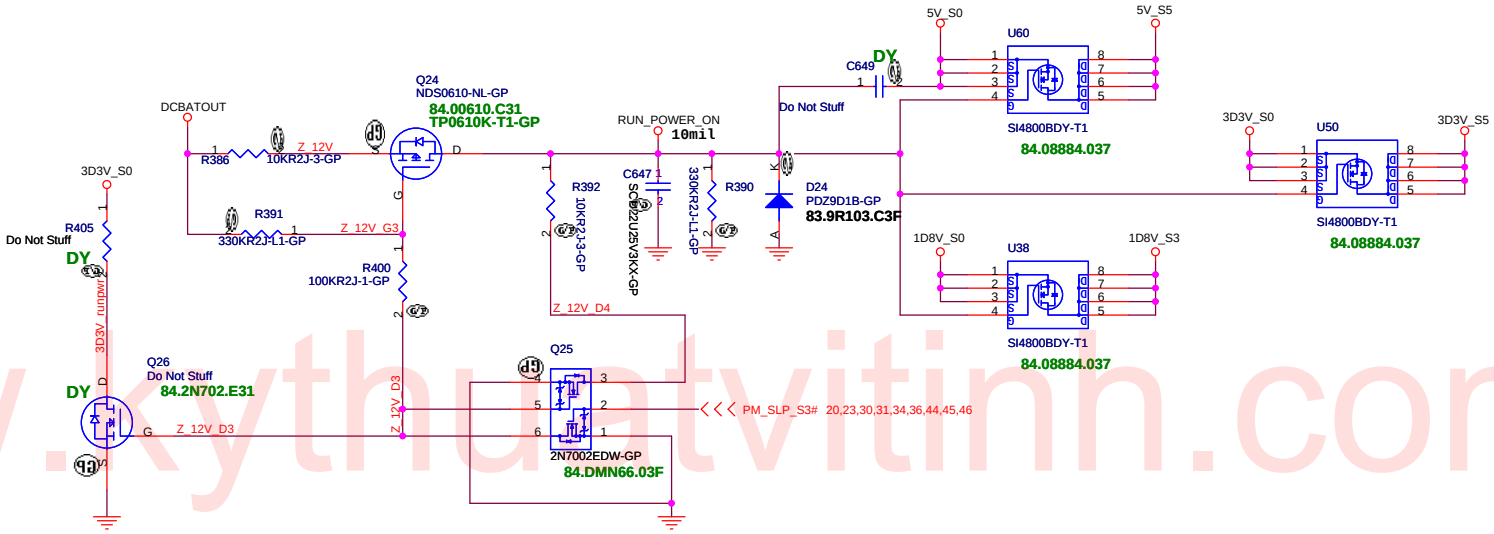
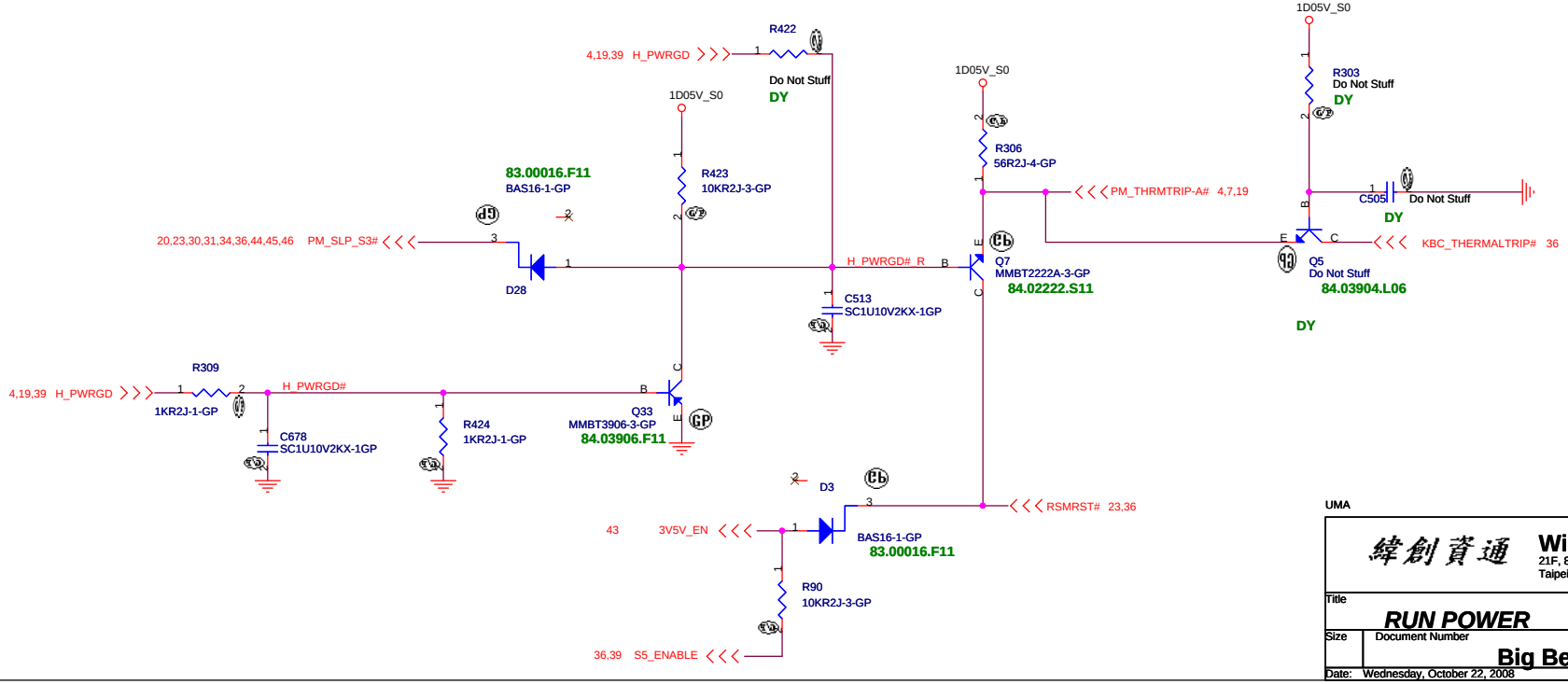
Title: CIR & test point		
Size: A3	Document Number: Big Bear 2	Rev: -1
Date: Wednesday, October 22, 2008	Sheet 39 of 50	

Run Power





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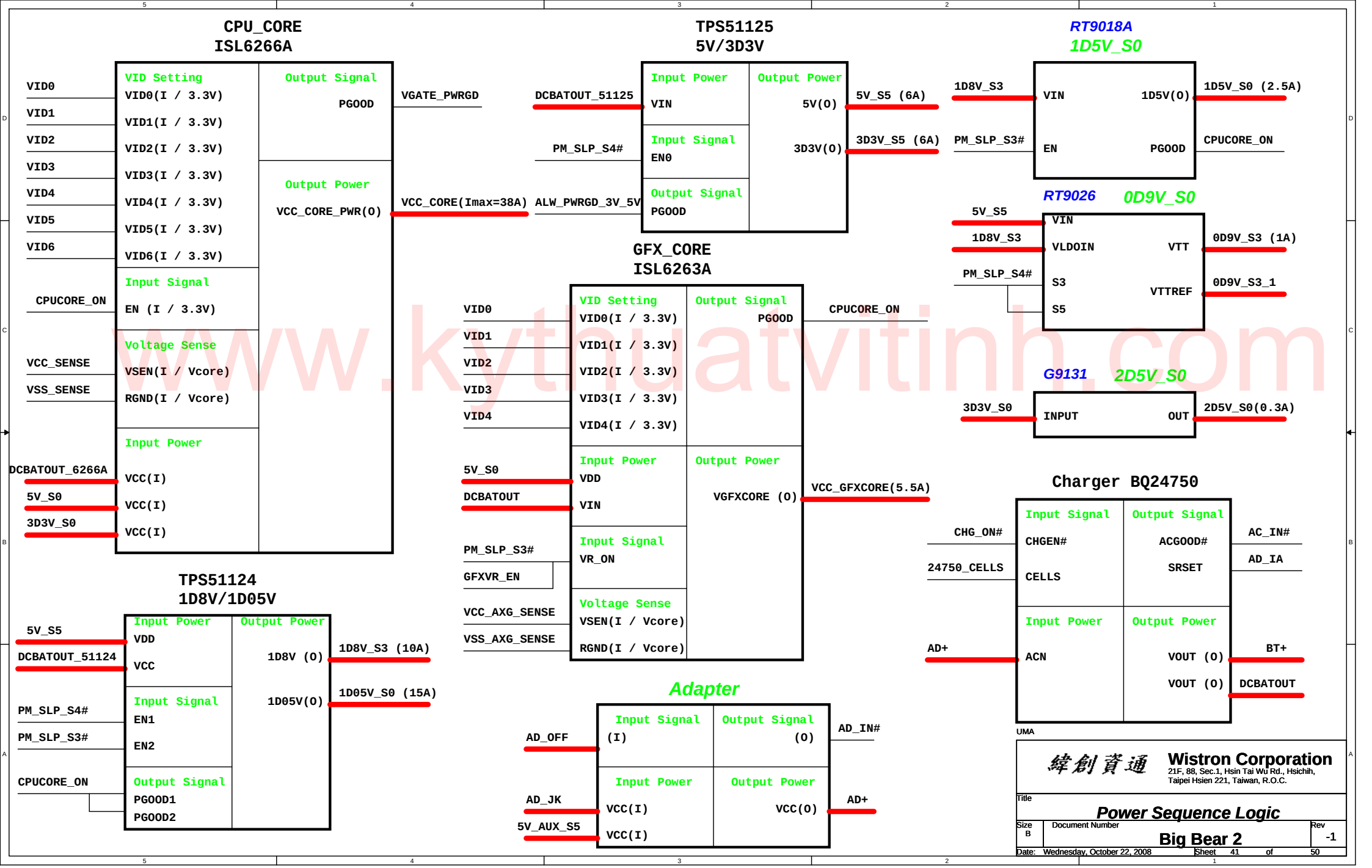
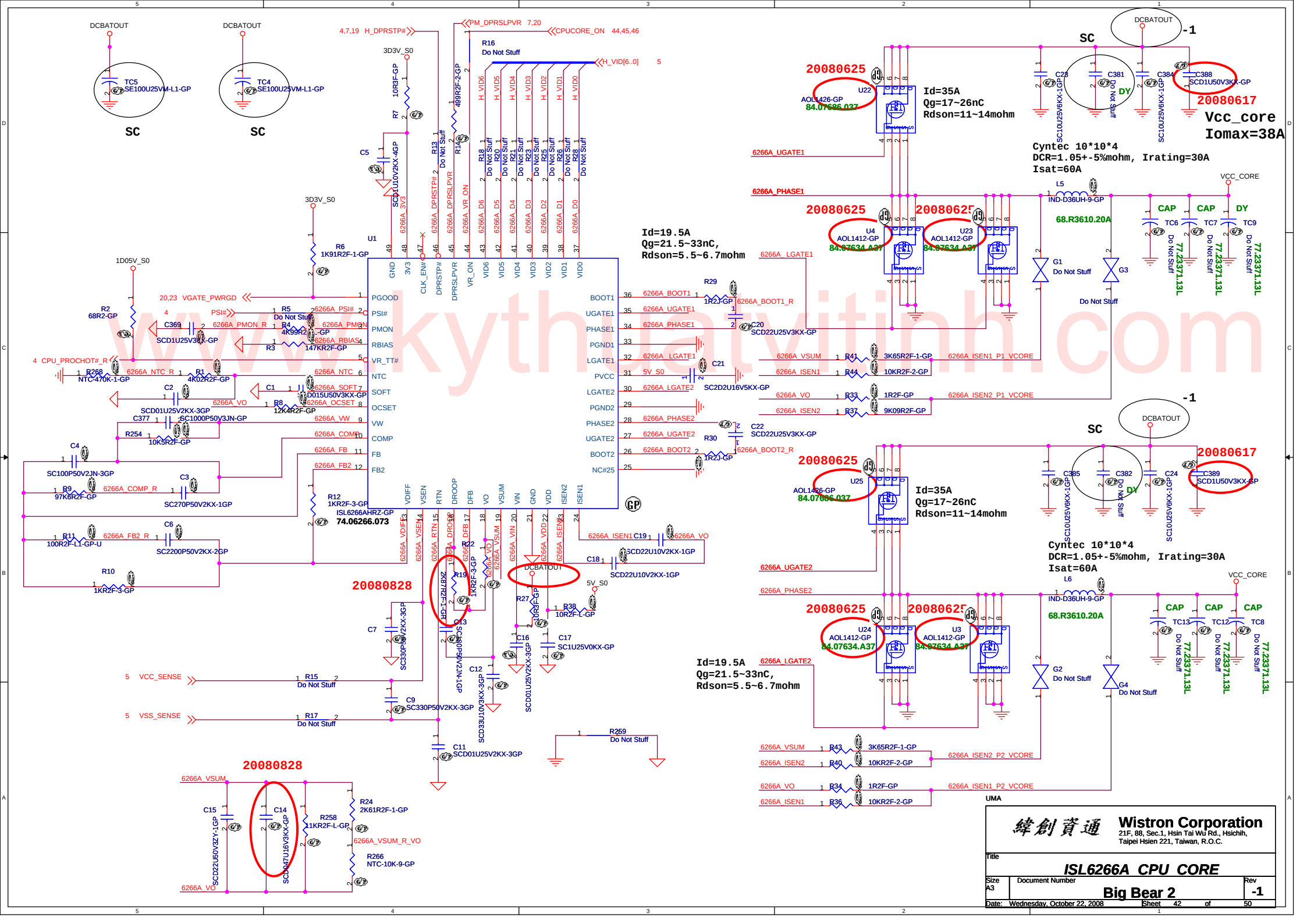
Taipei Hsien 221, Taiwan, R.O.C.

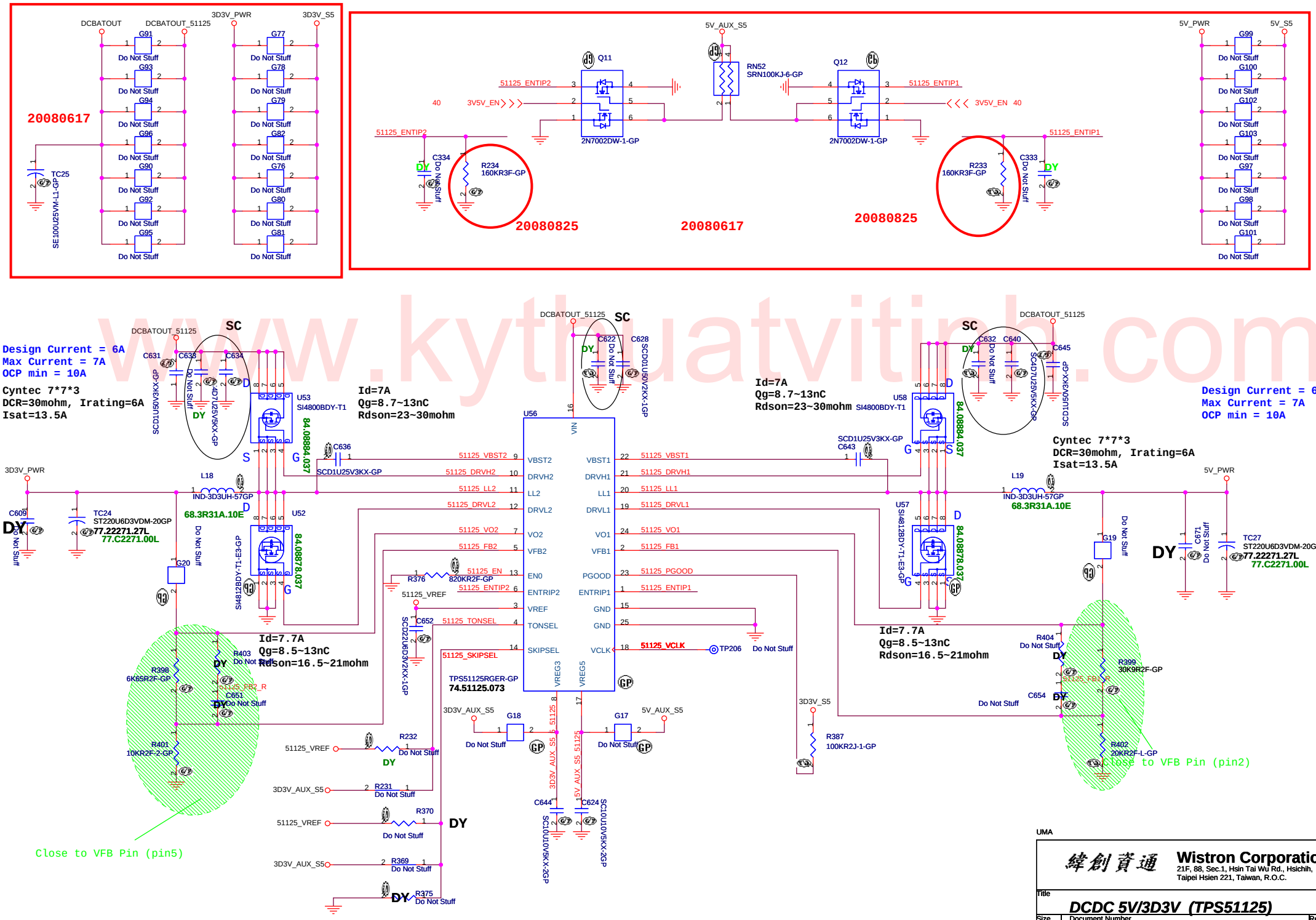
Title: RUN POWER

Size	Document Number	Rev
	Big Bear 2	-1

Date: Wednesday, October 22, 2008 Sheet 40 of 50






20080617
20080825
20080617
20080825
Design Current = 6A
Max Current = 7A
OCP min = 10A
Cyntec 7*7*3
DCR=30mohm, Irating=6A
Isat=13.5A
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm
TPS51125RGER-GP
74.51125.073
Close to VFB Pin (pin5)
Close to VFB Pin (pin2)
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
DCDC 5V/3D3V (TPS51125)
Big Bear 2
Wednesday, October 22, 2008

1D5V_S0
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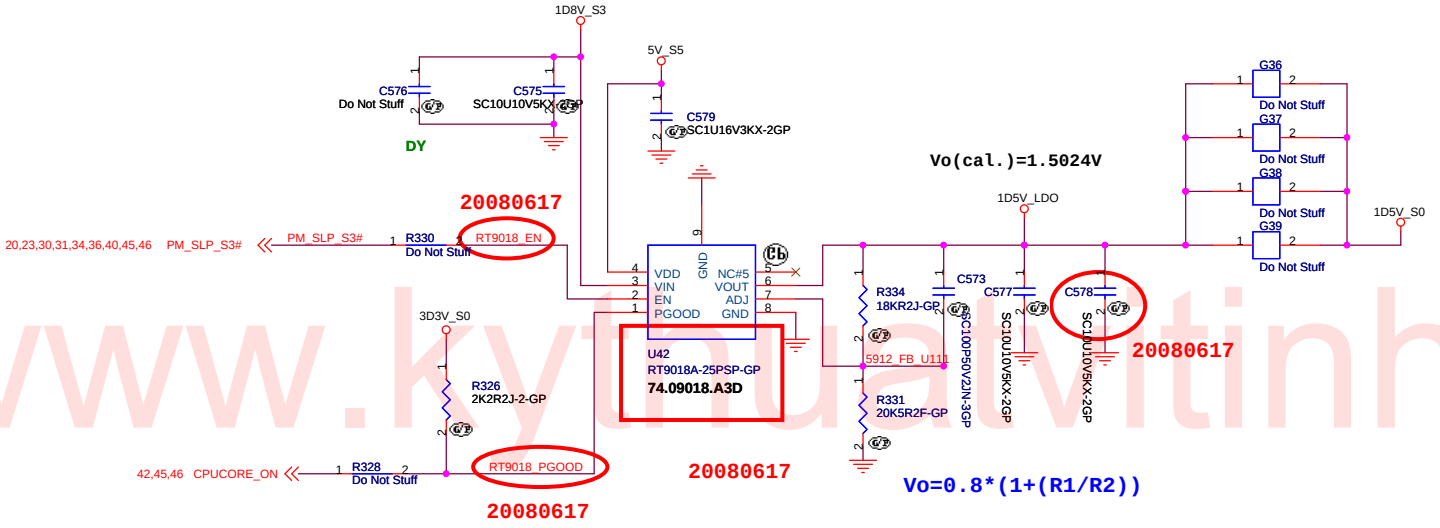
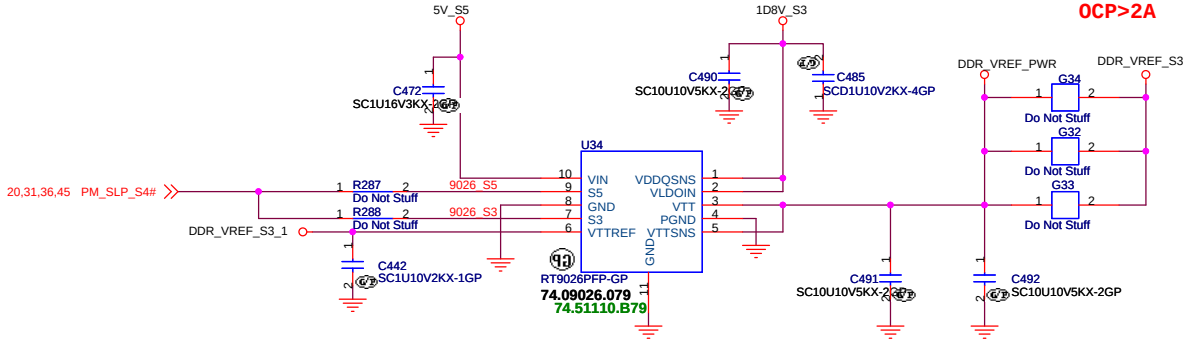
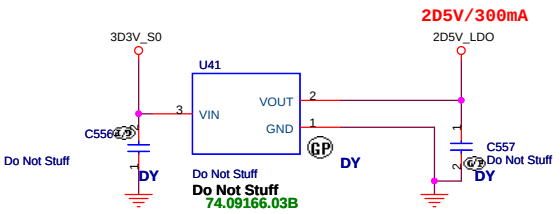


Iomax=1A
OCP>2A



2D5V_S0
Iomax=0.3A



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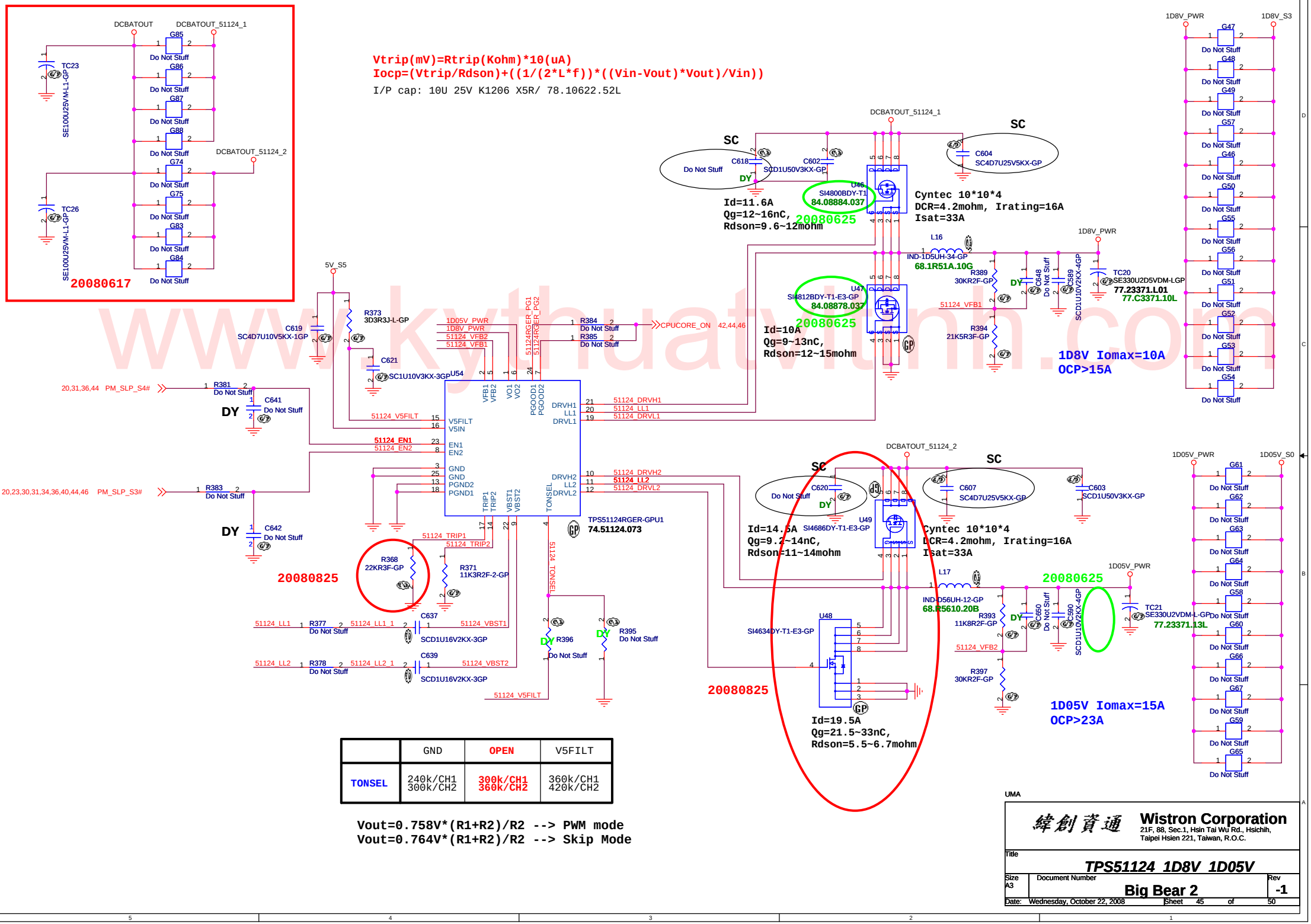
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *1D5V & 0D9V & 2D5V*		
Size: A3	Document Number: Big Bear 2	Rev: -1
Date: Wednesday, October 22, 2008	Sheet 44 of 50	



	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

UMA

緯創資通 Wistron Corporation
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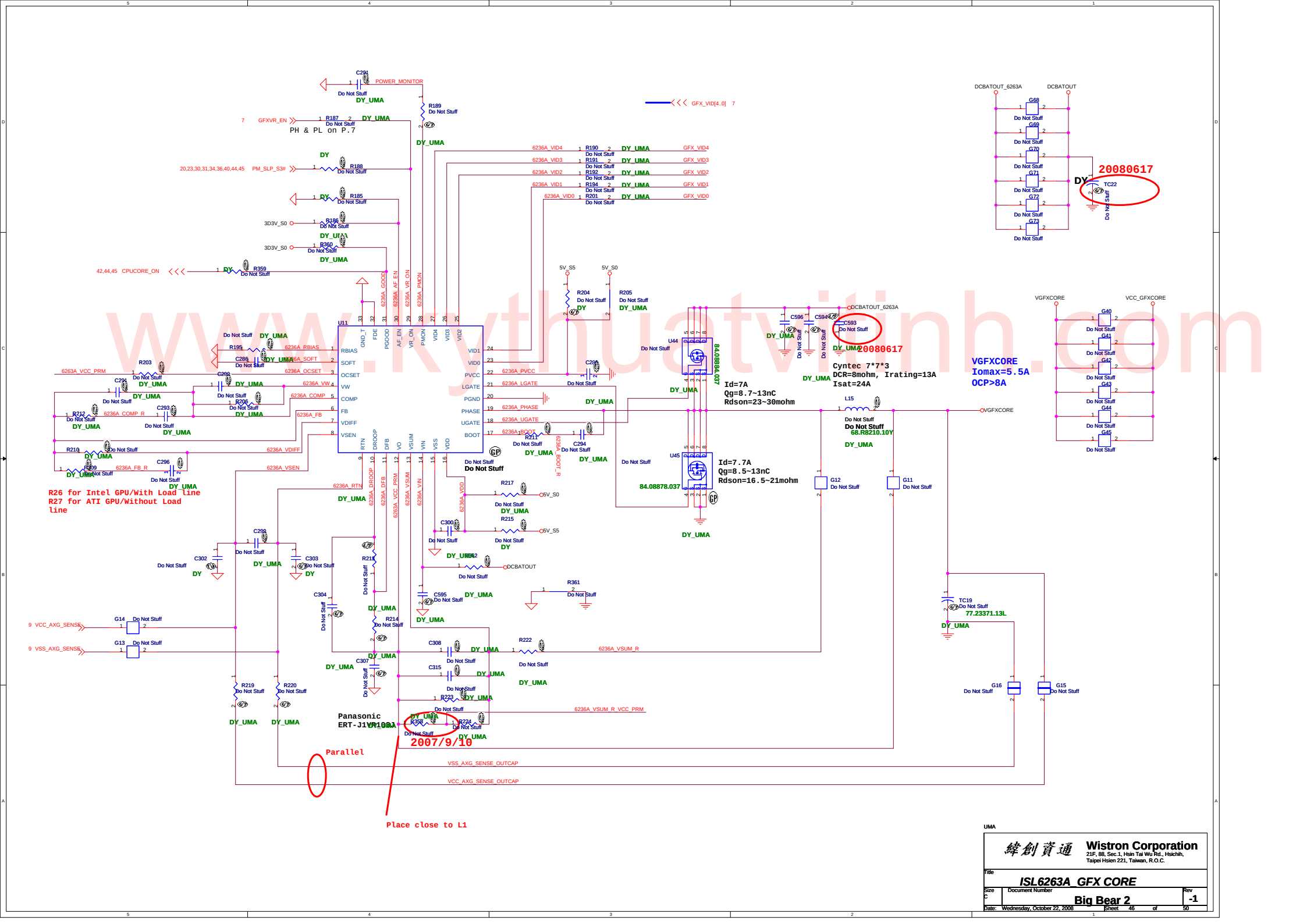
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51124_1D8V_1D05V

Size	Document Number	Rev
A3	Big Bear 2	-1

Date: Wednesday, October 22, 2008 Sheet 45 of 50



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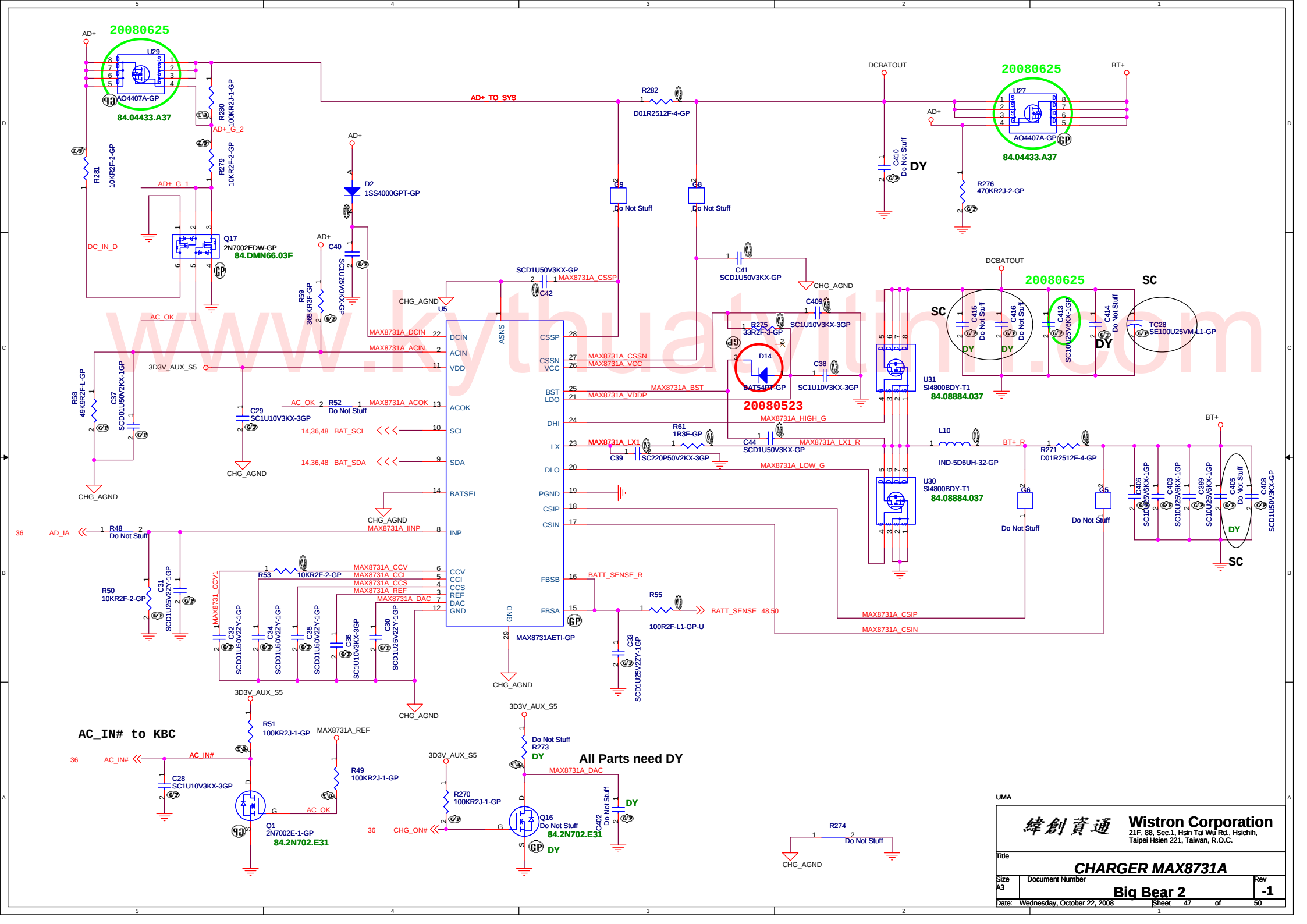
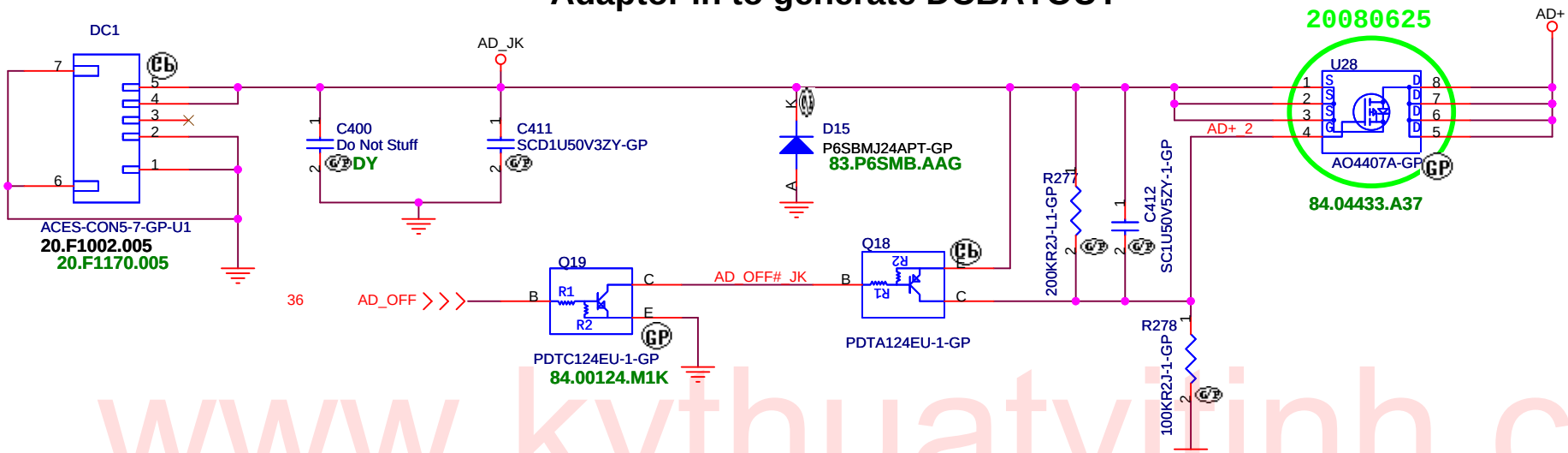
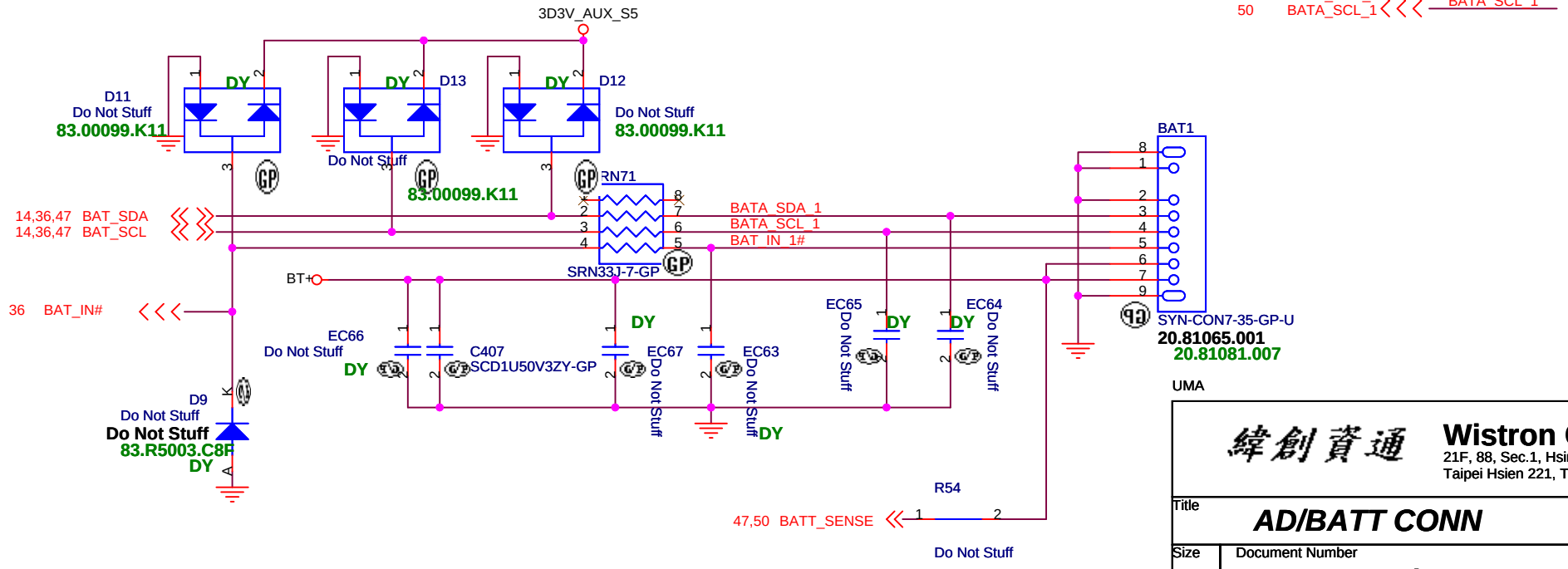
Title	ISL6263A_GFX CORE
Size: C	Document Number: Big Bear 2
Rev	-1
Date: Wednesday, October 22, 2008	Sheet 46 of 50



Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



47,50 BATT_SENSE — BATT_SENSE
50 BAT_IN_1# — BAT_IN_1#
50 BATA_SDA_1 — BATA_SDA_1
50 BATA_SCL_1 — BATA_SCL_1

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Title	AD/BATT CONN
Size	Document Number: Big Bear 2
Rev	-1
Date	Wednesday, October 22, 2008
Sheet	48 of 50

STAND OFF

SPRING ON BOTTOM

CPU & NB

H31 HOLE 34.42Y01.011
H32 HOLE 34.42Y01.011
H33 HOLE 34.42Y01.011
H34 HOLE 34.42Y01.011

MDC

H21 HOLE 34.42Y01.011
H22 HOLE 34.42Y01.011

Mini Card

H35 HOLE 34.4Z402.001
H36 HOLE 34.4Z402.001
H37 HOLE 34.4AJ01.001
H38 HOLE 34.4AJ01.001

MXM

H14 Do Not Stuff DIS_34.4Z401.001
H17 Do Not Stuff DIS_34.4Z401.001

DIMM

GND1 Do Not Stuff Do Not Stuff DY

Touch Pad

SC

MXM SPRING

S1 Do Not Stuff DIS
S3 Do Not Stuff DIS
S2 Do Not Stuff DIS

H1 H2 H3 H4 H5 H6 H7 H8 H9 H10 H13 H18 PAD1 Do Not Stuff

GND2 Do Not Stuff Do Not Stuff DY
GND3 Do Not Stuff Do Not Stuff DY

H39 H40 Do Not Stuff

EMI

DCBATOUT
EC6 SCD1U50V3ZY-GP DY
EC15 Do Not Stuff DY
EC16 SCD1U50V3ZY-GP DY
EC50 Do Not Stuff DY
EC53 Do Not Stuff DY
EC41 Do Not Stuff DY
EC31 Do Not Stuff DY
EC12 Do Not Stuff DY
EC11 Do Not Stuff DY
EC10 SCD1U50V3ZY-GP DY
EC9 SCD1U50V3ZY-GP DY

DCBATOUT
EC7 Do Not Stuff DY
EC8 SCD1U50V3ZY-GP DY

5V_USB1_S0
EC29 Do Not Stuff DY

1D8V_S3
EC17 Do Not Stuff DY
EC77 Do Not Stuff DY
EC20 Do Not Stuff DY

3D3V_S0
EC38 Do Not Stuff DY
EC40 Do Not Stuff DY
EC45 Do Not Stuff DY
EC42 Do Not Stuff DY
EC47 SCD1U50V3ZY-GP DY
EC35 Do Not Stuff DY
EC62 Do Not Stuff DY

3D3V_S0
EC81 Do Not Stuff DY
EC79 Do Not Stuff DY
EC59 Do Not Stuff DY
EC21 Do Not Stuff DY
EC58 Do Not Stuff DY

1D05V_S0
EC27 Do Not Stuff DY

1D05V_S0
EC75 Do Not Stuff DY
EC39 Do Not Stuff DY

5V_S0
EC83 Do Not Stuff DY
EC84 Do Not Stuff DY

5V_S0
EC28 Do Not Stuff DY
EC26 Do Not Stuff DY
EC68 Do Not Stuff DY
EC4 Do Not Stuff DY
EC18 Do Not Stuff DY
EC82 Do Not Stuff DY
EC37 Do Not Stuff DY
EC80 Do Not Stuff DY

BT+
EC100 Do Not Stuff DY
EC99 Do Not Stuff DY

5V_S5
EC49 Do Not Stuff DY
EC57 Do Not Stuff DY

3D3V_S5
EC46 Do Not Stuff DY
EC56 Do Not Stuff DY
EC78 Do Not Stuff DY
EC48 Do Not Stuff DY
EC36 Do Not Stuff DY

1D8V_S3
EC86 Do Not Stuff DY
EC85 Do Not Stuff DY
EC87 Do Not Stuff DY
EC89 Do Not Stuff DY
EC88 Do Not Stuff DY
EC90 Do Not Stuff DY

AD_JK
EC101 Do Not Stuff DY

1D05V_S0
EC93 Do Not Stuff DY
EC92 Do Not Stuff DY
EC91 Do Not Stuff DY
EC95 Do Not Stuff DY
EC94 Do Not Stuff DY

5V_S0
EC97 Do Not Stuff DY
EC96 Do Not Stuff DY

DCBATOUT
EC98 Do Not Stuff DY

VCC_GFXCORE
EC106 Do Not Stuff DY
EC107 Do Not Stuff DY
EC108 Do Not Stuff DY

DCBATOUT
EC109 SCD1U50V3ZY-GP DY
EC110 Do Not Stuff DY

Near H38

S4 Do Not Stuff DY
S5 SPRING-7

Near SB

S6 Do Not Stuff DY
S7 Do Not Stuff DY

Near CRT

S8 Do Not Stuff DY
S9 Do Not Stuff DY

USB port

S10 Do Not Stuff DY
S11 Do Not Stuff DY
S12 Do Not Stuff DY

HDMI

S13 Do Not Stuff DY

SC

UMA

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Title: EMI/Spring/Boss
Size: Document Number: Big Bear 2
Rev: -1
Date: Wednesday, October 22, 2008 Sheet 49 of 50

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Title: AFTE

Size	Document Number	Rev
A3	Big Bear 2	-1

Date: Wednesday, October 22, 2008 Sheet 50 of 51

Big Bear 2 Schematic EC Tracking Record LAB 0911 , 2008
EC #/ Page / Description / Part Affected

EC SC01/20/Change R316 to 20R2F(For USB eye diagram)
EC SC02/24/Swap net SATA_RXN5 SATA_RXP5
EC SC03/29/Add C679 C680 for XF1(For IEEE common voltage channel D fail)
EC SC04/33/Add RN95 RN104(vendor realtek request)
EC SC05/36/Swap KBI1 pin definition

UMA

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Size | Document Number: **Big Bear 2** | Rev: -1

Date: Wednesday, October 22, 2008 | Sheet 51 of 51