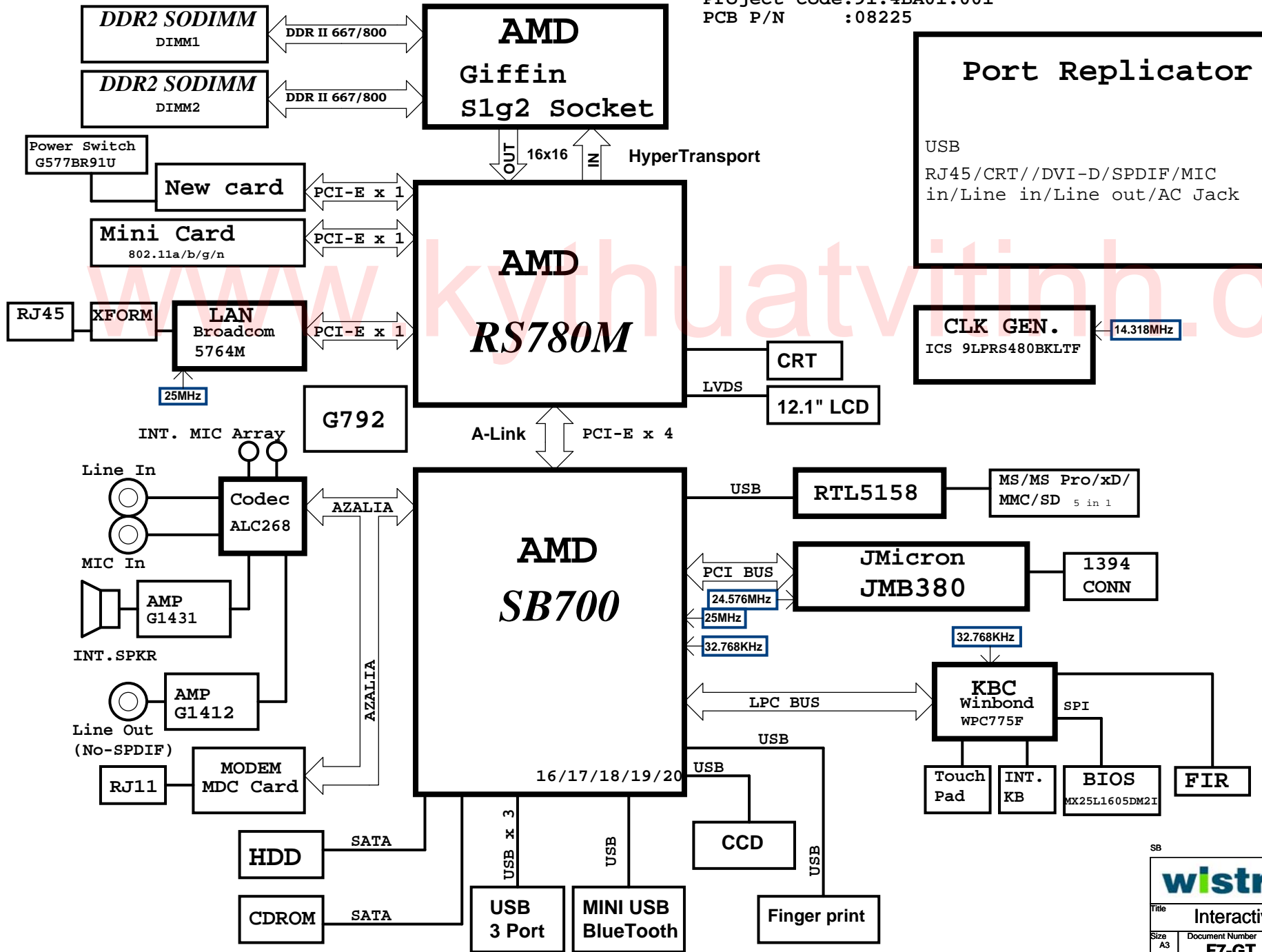


Ferrari 7 GT Block Diagram

2008/09/01

Project code: 91.4BA01.001
PCB P/N : 08225



PCB Layer Stackup

- L1: Component
- L2: GND
- L3: Signal
- L4: VCC
- L5: GND
- L6: Signal
- L7: GND
- L8: Component

CPU V_CORE

ISL6265HR 37

INPUT	OUTPUT
DCBATOUT	VCC_CORE_S0

SYSTEM DC/DC

TPS51124 38

INPUT	OUTPUT
DCBATOUT	ID2V_S0 ID1V_S0

TPS51120 40

INPUT	OUTPUT
DCBATOUT	5V_S5 3D3V_S5

TPS51117 39

INPUT	OUTPUT
DCBATOUT	ID8V_S3

SYSTEM LDO

G2997 41

INPUT	OUTPUT
1D8V_S3	0D9V_S3

G9161

INPUT	OUTPUT
3D3V_S5	ID2V_S5

G9166

INPUT	OUTPUT
3D3V_S0	2D5V_S0

G957

INPUT	OUTPUT
3D3V_S0	ID5V_S0

Battery Charger

MAX8371 43

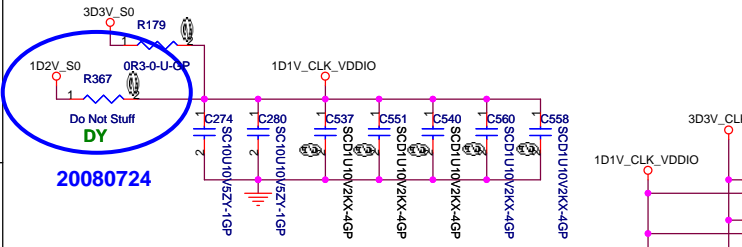
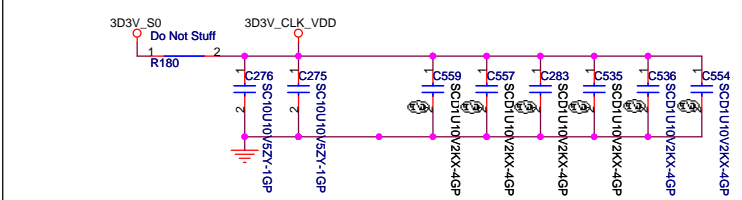
INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT

wistron Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

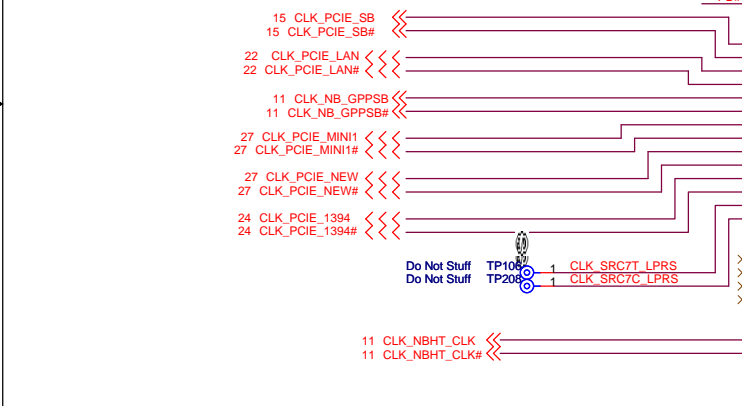
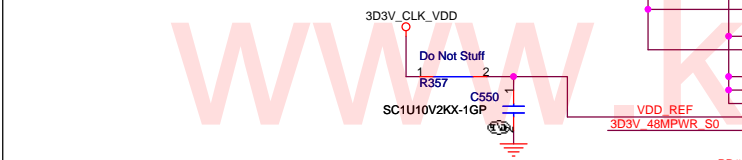
Title: Interactive Circuit Map

Size: A3 Document Number: F7-GT Rev: SB

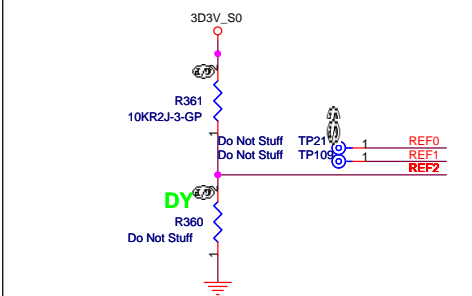
Date: Monday, September 01, 2008 Sheet: 1 of 47



20080724



20080716



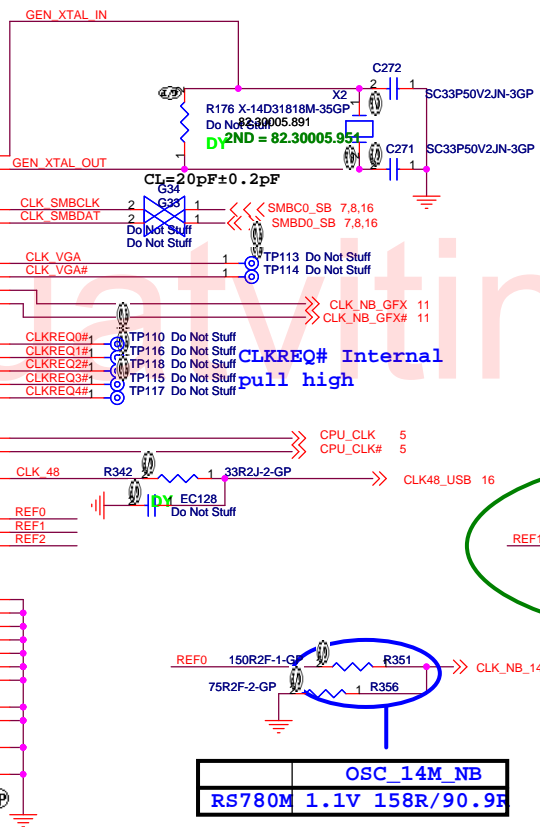
SEL_SATA	1	100 MHz non-spreading differential SRC clock
REF1	0*	100 MHz spreading differential SRC clock
SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
REF0	0*	100 MHz differential HTT clock

* default

CPU_CLK (200MHz)

Olan -1 change to 71.09480.A03

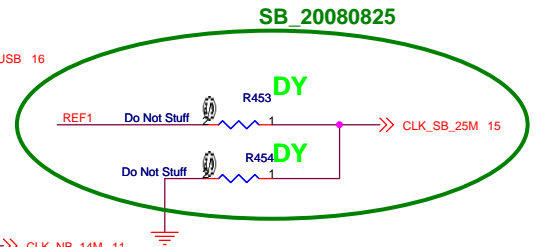
ICS9LPRS480BKLF-T-GP
71.09480.A03



OSC_14M_NB
RS780M 1.1V 158R/90.9F

Due to PLL issue on current clock chip, the SBlink clock need to come from SRC clocks for RS740 and RS780. Future clock chip revision will fix this.

Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.



SB 20080825

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	66M SE(SINGLE END)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	NC	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF

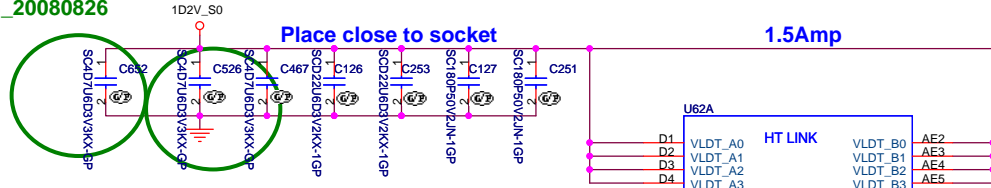
* RS780 can be used as clock buffer to output two PCIe reference clocks. By default, chip will configured as input mode, BIOS can program it to output mode.

SB

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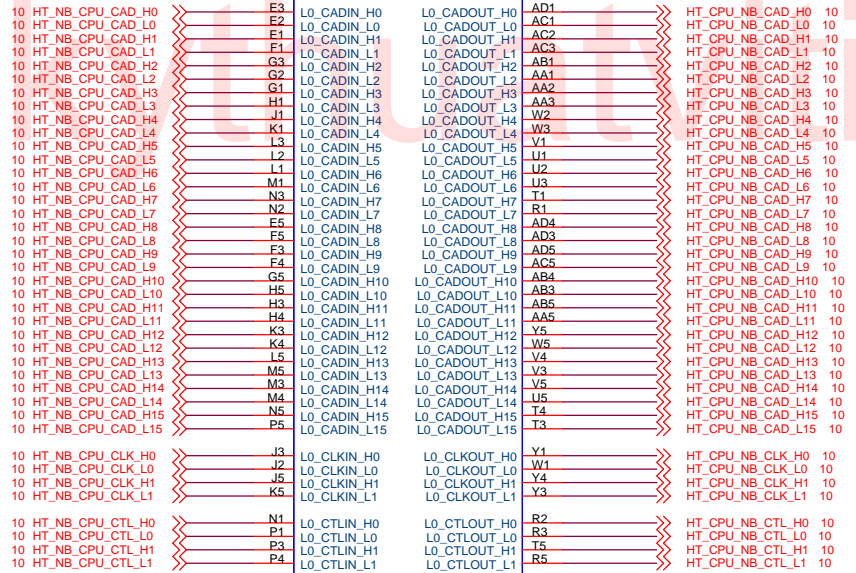
Title CLKGEN_ICS9LPRS480		
Size A3	Document Number F7-GT	Rev SB
Date Friday, August 29, 2008	Sheet 2	of 47

SB_20080826

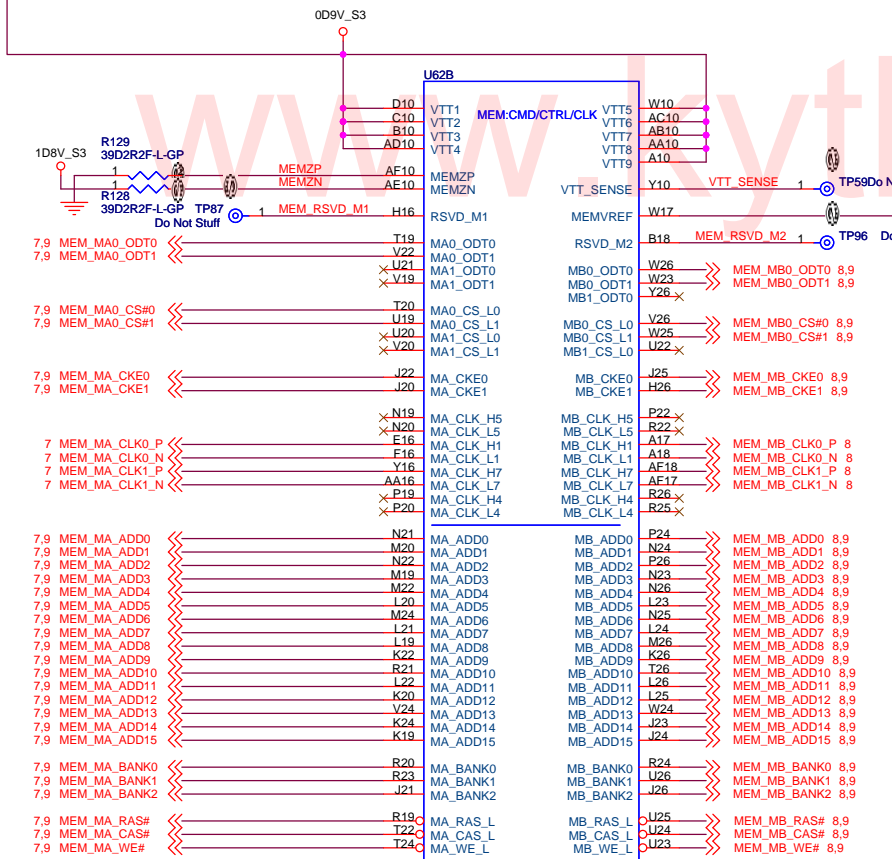
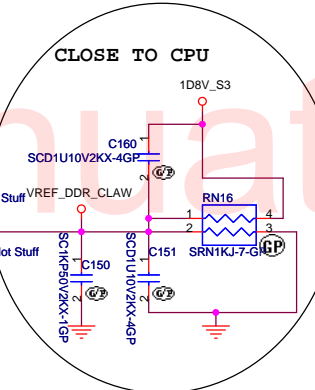
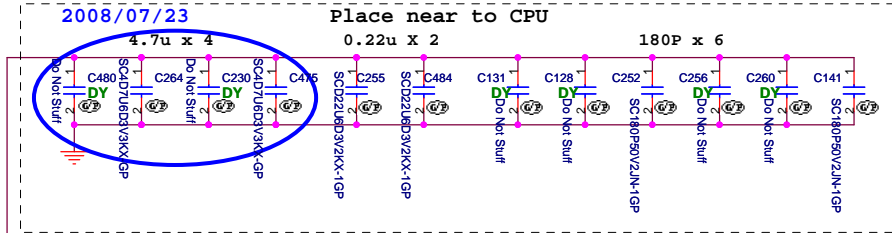


2008/07/23

State	Specification	Notes	2M200100M2303
S0.C0.Px	Tcase Max	3	TBD
	NB COF	1	400 MHz
	VID_VDDNB Min	2	0.950 V
	VID_VDDNB Max	2	0.950 V
	Startup P-state		
S0.C0.P0	CPU COF	1	2000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	IDD Max	3	TBD
S0.C0.P1	CPU COF	1	1800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	IDD Max	3	TBD
S0.C0.P2	CPU COF	1	1500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	IDD Max	3	TBD
S0.C0.P3	CPU COF	1	1300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	IDD Max	3	TBD
S0.C0.P4	CPU COF	1	1000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	IDD Max	3	TBD
S0.C0.P5	CPU COF	1	800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	IDD Max	3	TBD
S0.C0.P6	CPU COF	1	500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	IDD Max	3	TBD
S0.C0.P7	CPU COF	1	300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	IDD Max	3	TBD

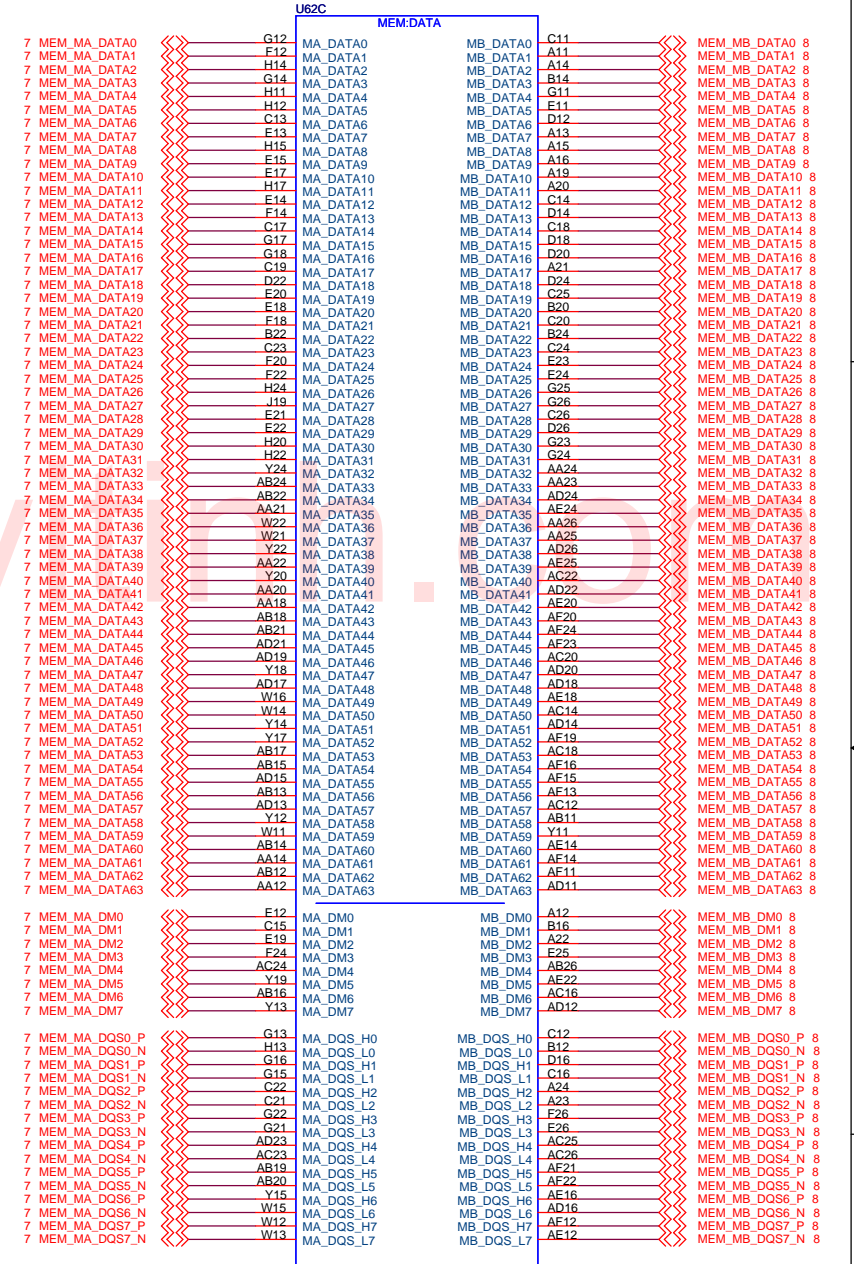


SKT-CPU638P-GP-U2
 62.10055.111 2ND = 62.10055.251
 SKT-BGA638H176



SKT-CPU638P-GP-U2
62.10055.111

2ND = 62.10055.251



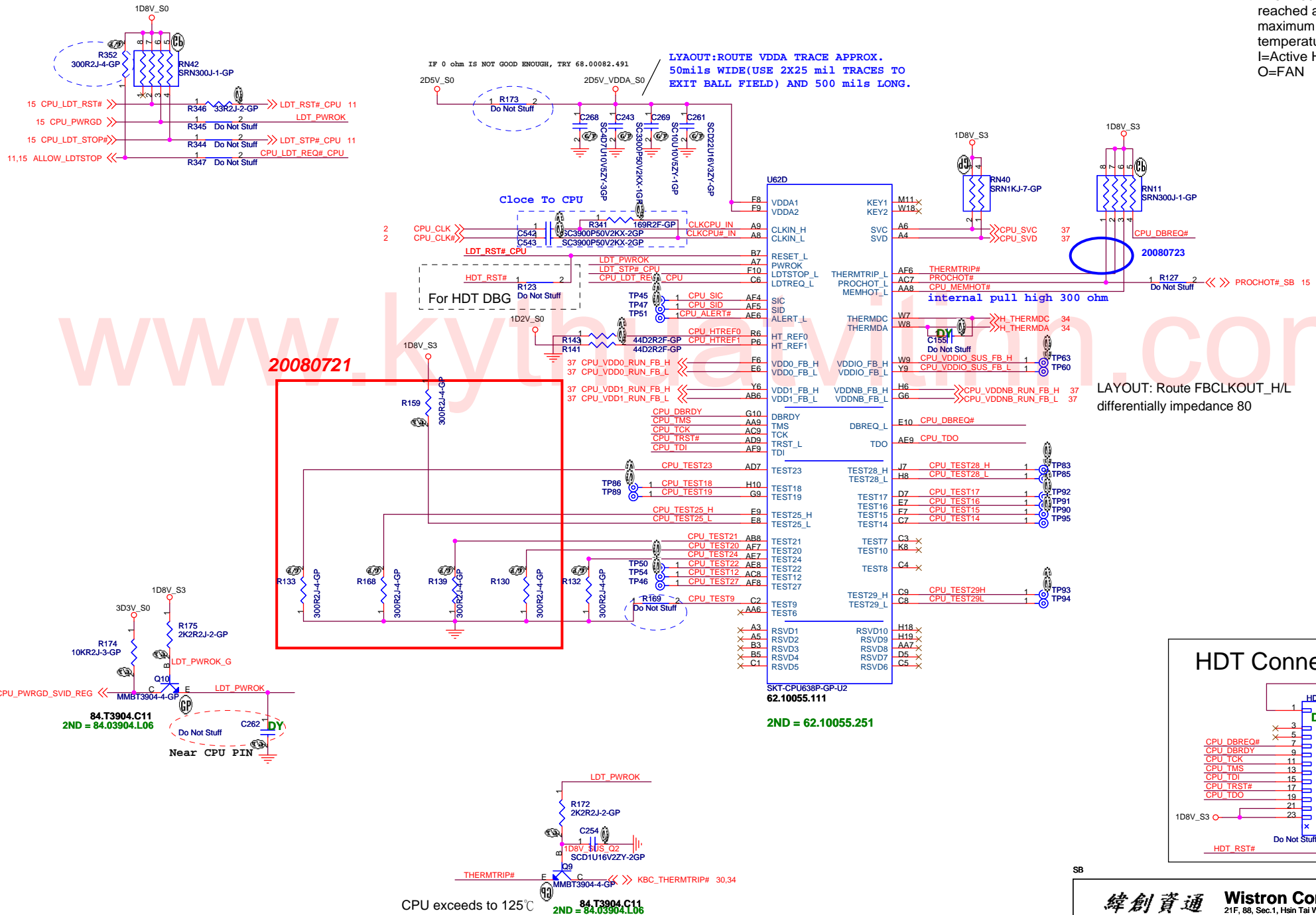
SKT-CPU638P-GP-U2
62.10055.111

2ND = 62.10055.251

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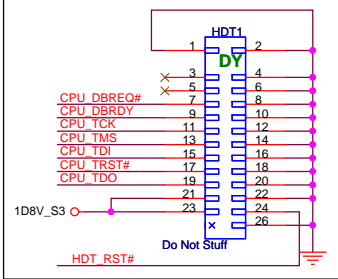
Title			CPU_DDR (2/4)		
Size	Document Number	Rev			
A3	F7-GT	SB			
Date:	Friday, August 29, 2008	Sheet	4	of	47

The Processor has reached a preset maximum operating temperature. 100°C
 I=Active HTC
 O=FAN



LAYOUT: Route FBCLKOUT_H/L differentially impedance 80

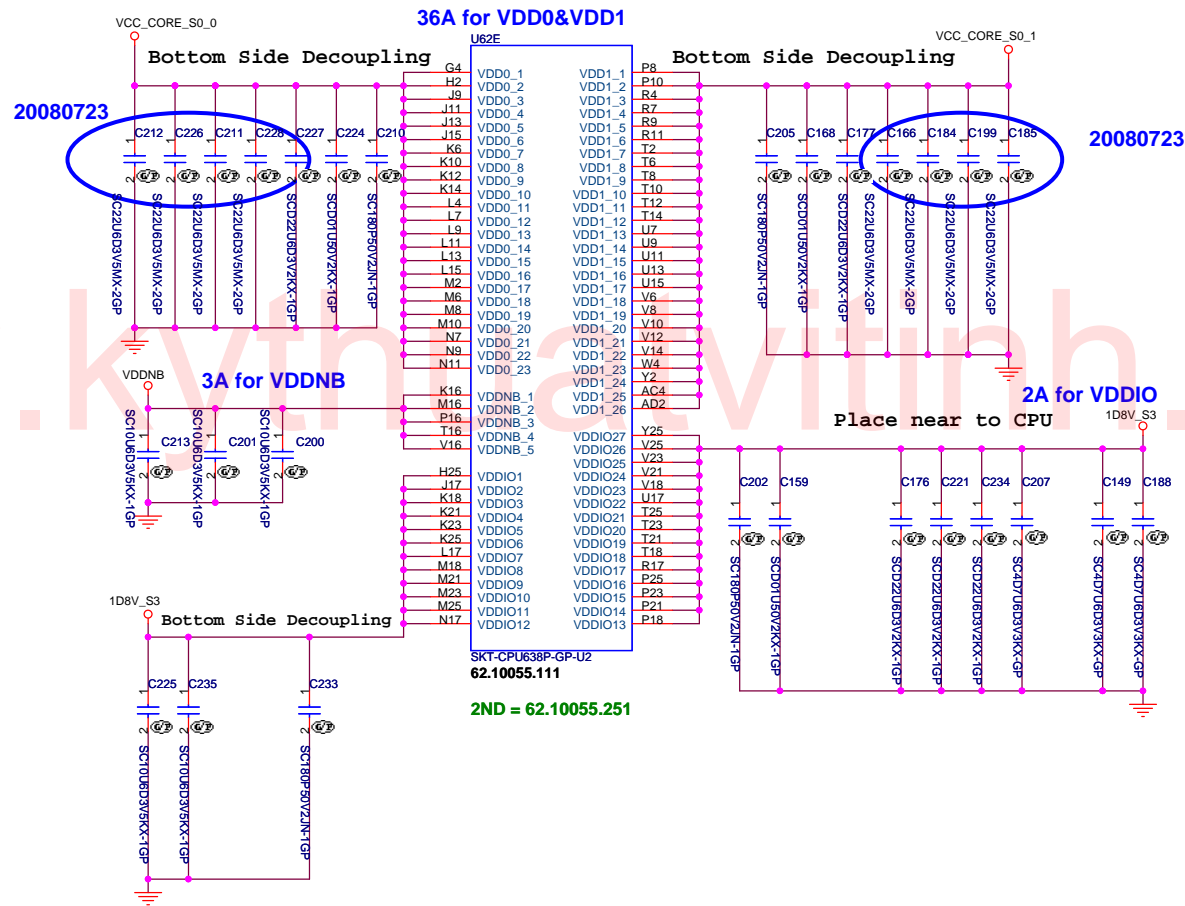
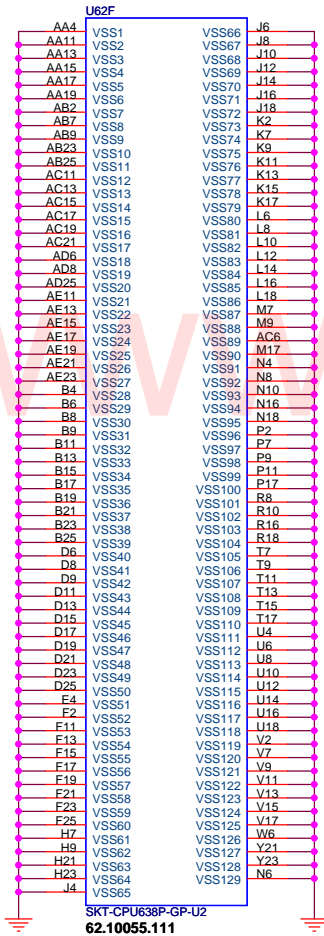
HDT Connectors

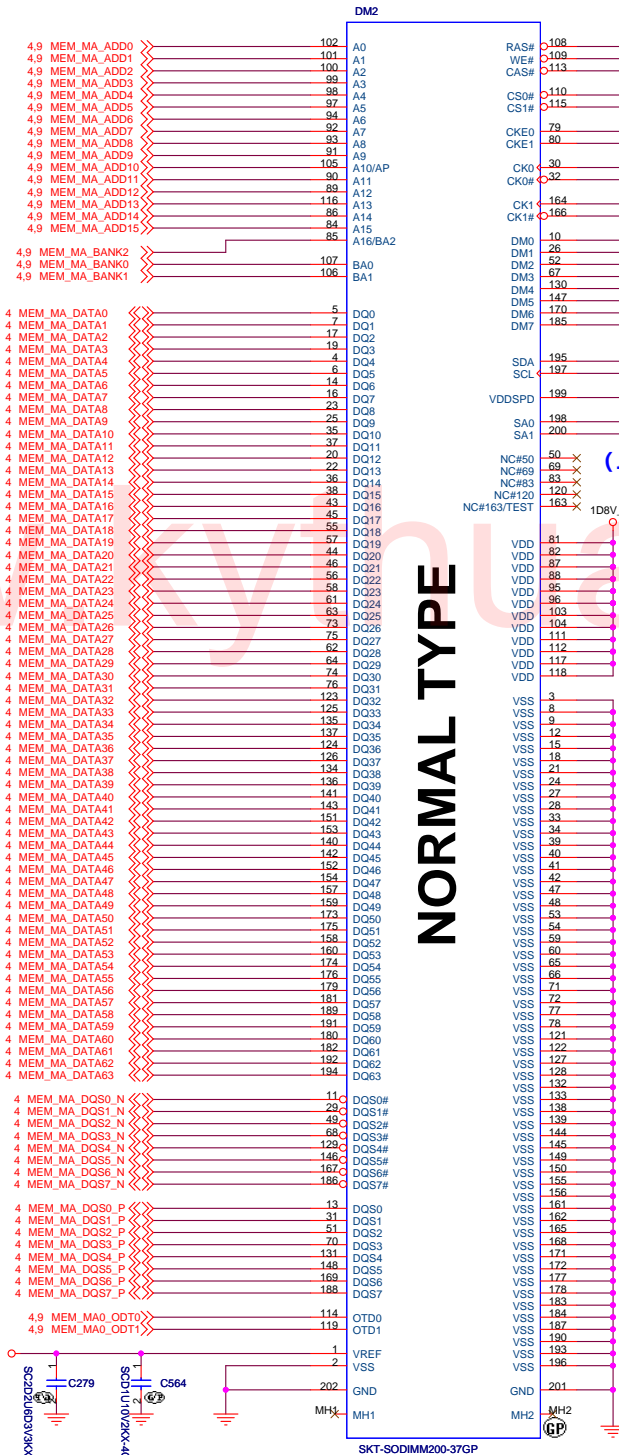


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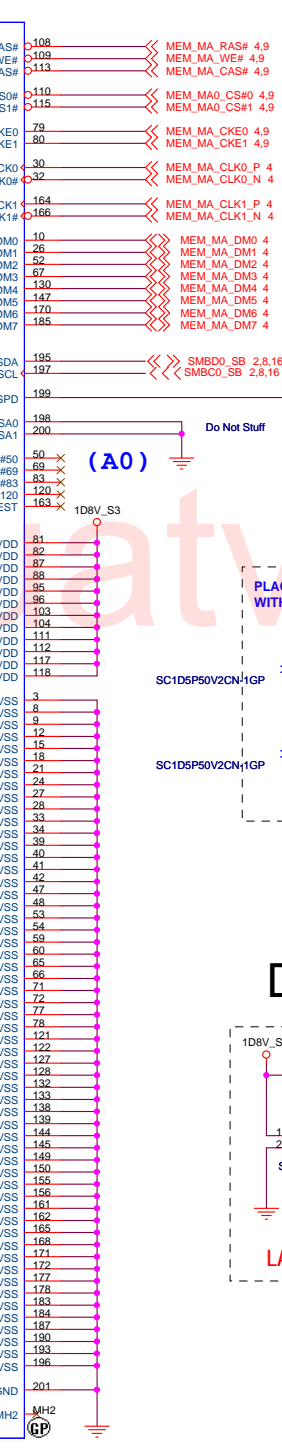
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Size: A3	Document Number: F7-GT	Rev: SB
Date: Friday, August 29, 2008	Sheet 5 of 47	

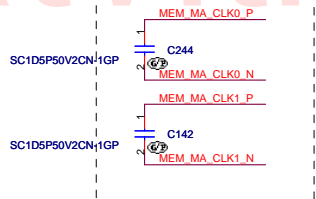




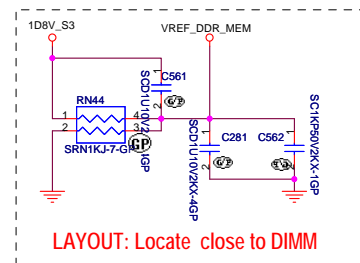
NORMAL TYPE



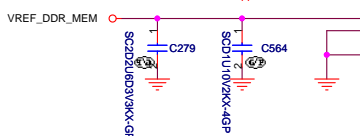
PLACE CLOSE TO PROCESSOR WITHIN 1.5 INCH



DDR_VREF

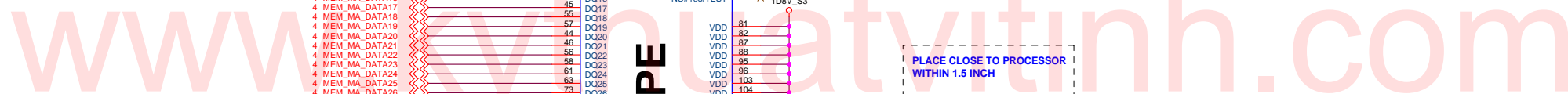


LAYOUT: Locate close to DIMM

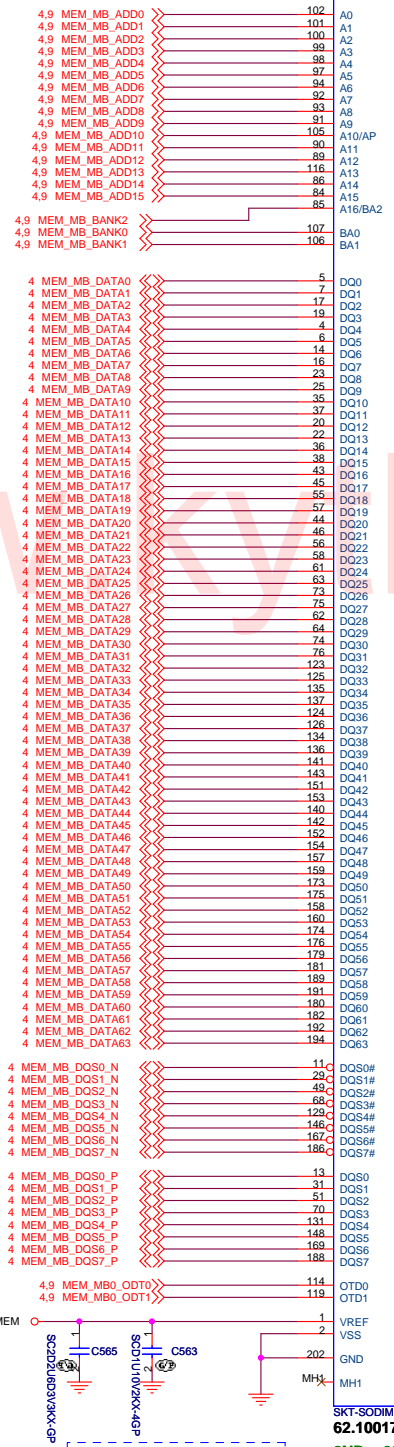


Place C2.2uF and 0.1uF < 500mils from DDR connector

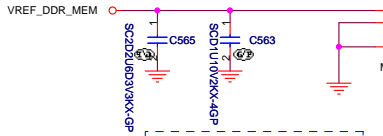
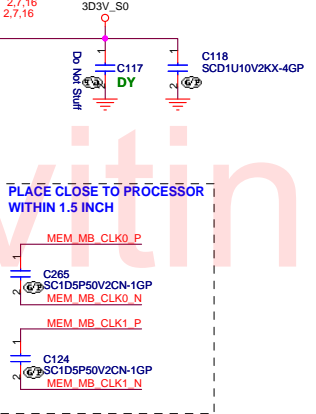
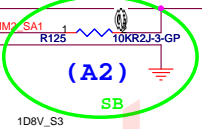
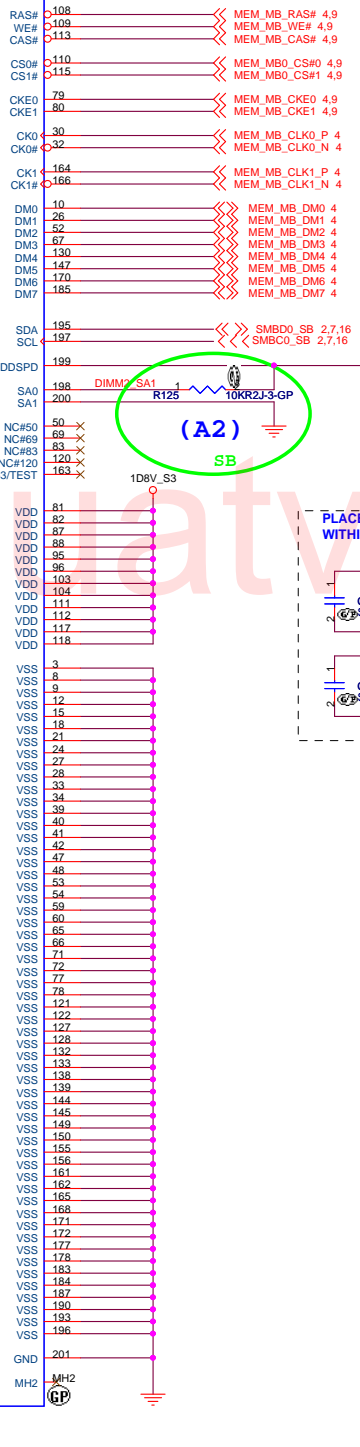
HI 9.2mm
62.10017.E21
2ND = 62.10017.A51



Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
DDR_SO-DIMM SKT_1	
Title DDR_SO-DIMM SKT_1	Rev SB
Size Custom	Document Number F7-GT
Date: Wednesday, September 03, 2008 Sheet 7 of 47	



REVERSE TYPE



SKT-SODIMM2002U3GP
62.10017.661
2N2 = 62.10017.A41
LOW 5.2 mm

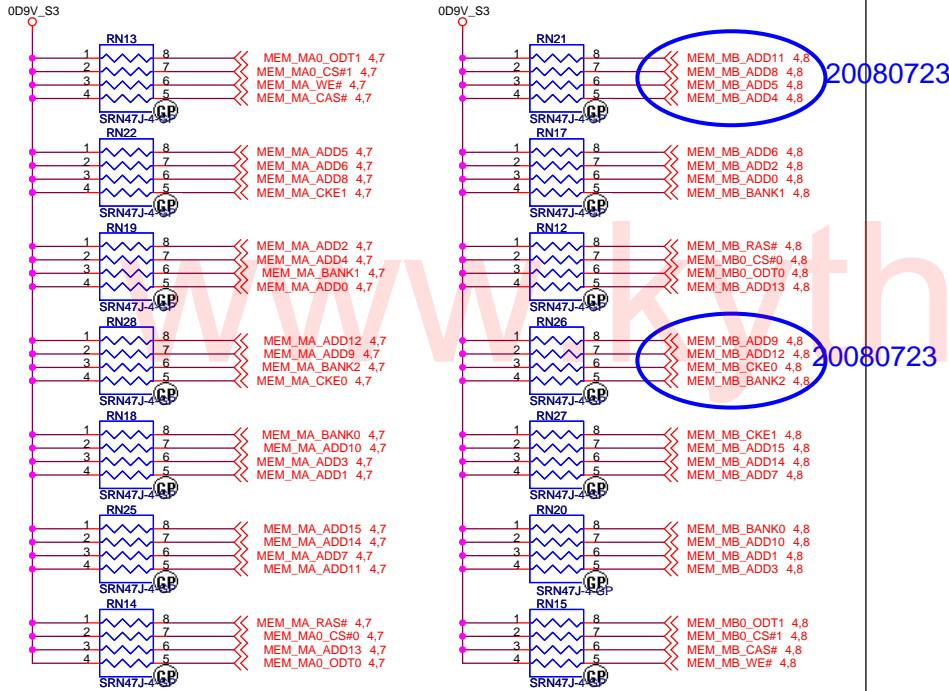
SB

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Title		
DDR_SO-DIMM SKT_2		
Size	Document Number	Rev
Custom	F7-GT	SB
Date: Friday, August 29, 2008	Sheet 8	of 47

PARALLEL TERMINATION

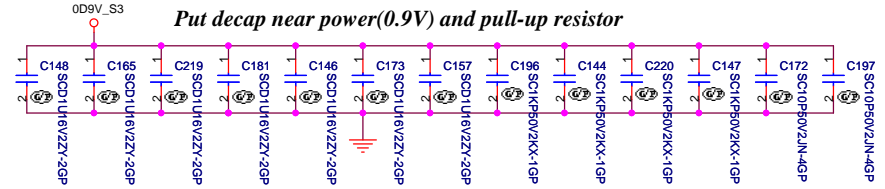
Put decap near power(0.9V) and pull-up resistor



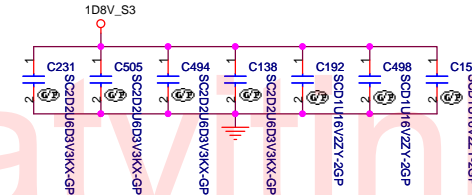
Do not share the Term resistor between the DDR address and Control Signals.

Decoupling Capacitor

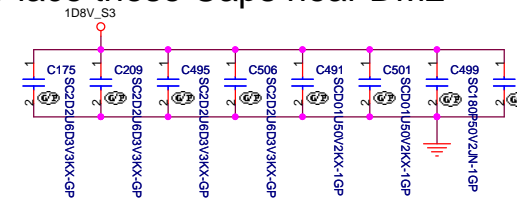
Put decap near power(0.9V) and pull-up resistor



Place these Caps near DM1



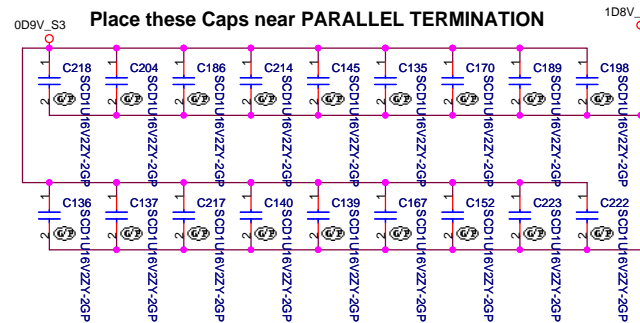
Place these Caps near DM2

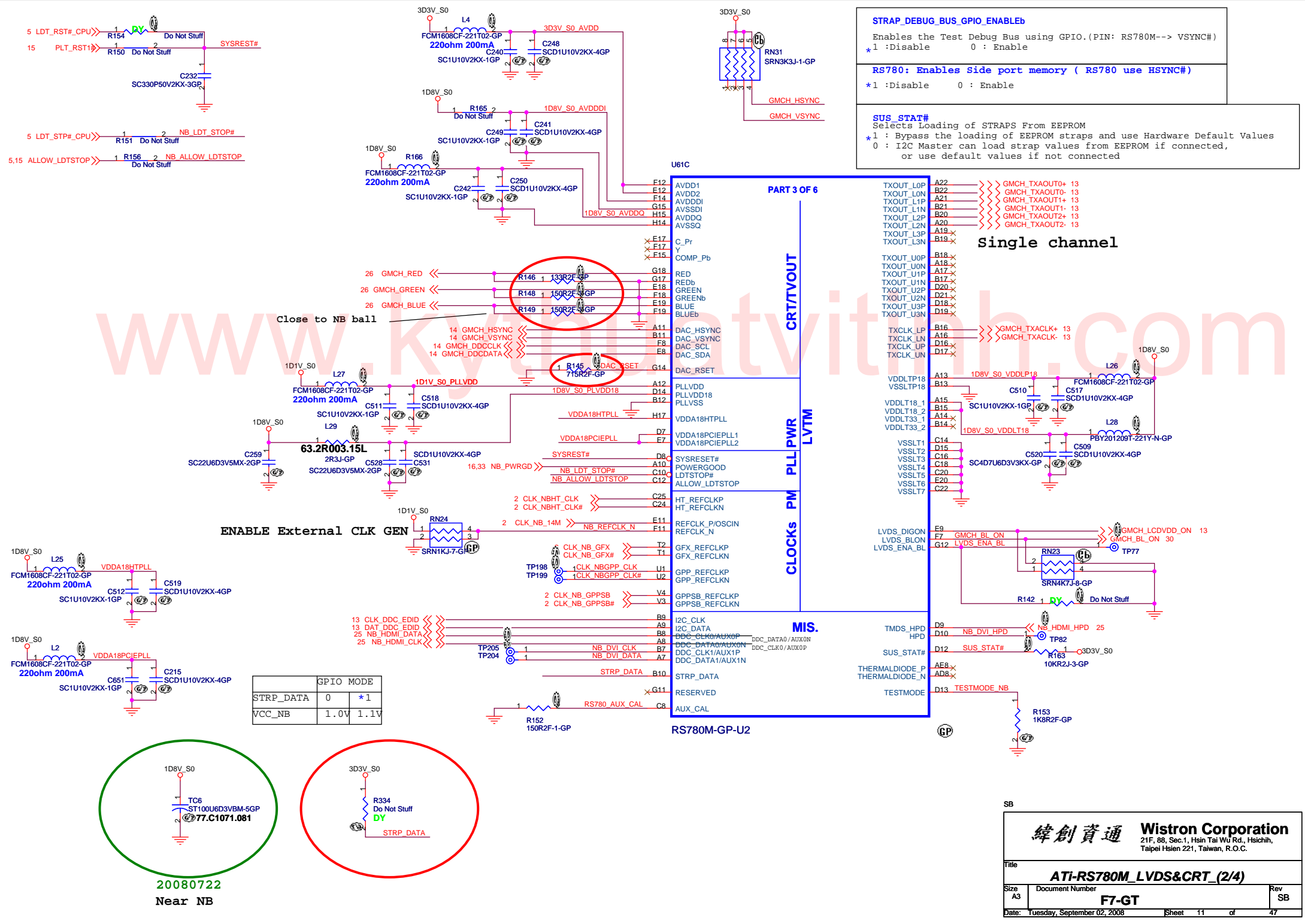


Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3

Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3

Place these Caps near PARALLEL TERMINATION





STRAP_DEBUG_BUS_GPIO_ENABLEb
 Enables the Test Debug Bus using GPIO.(PIN: RS780M--> VSYNC#)
 *1 :Disable 0 : Enable

RS780: Enables Side port memory (RS780 use HSYNC#)
 *1 :Disable 0 : Enable

SUS_STAT#
 Selects Loading of STRAPS From EEPROM
 *1 : Bypass the loading of EEPROM straps and use Hardware Default Values
 0 : I2C Master can load strap values from EEPROM if connected,
 or use default values if not connected

Single channel

	GPIO MODE	
STRP_DATA	0	* 1
VCC_NB	1.0V	1.1V

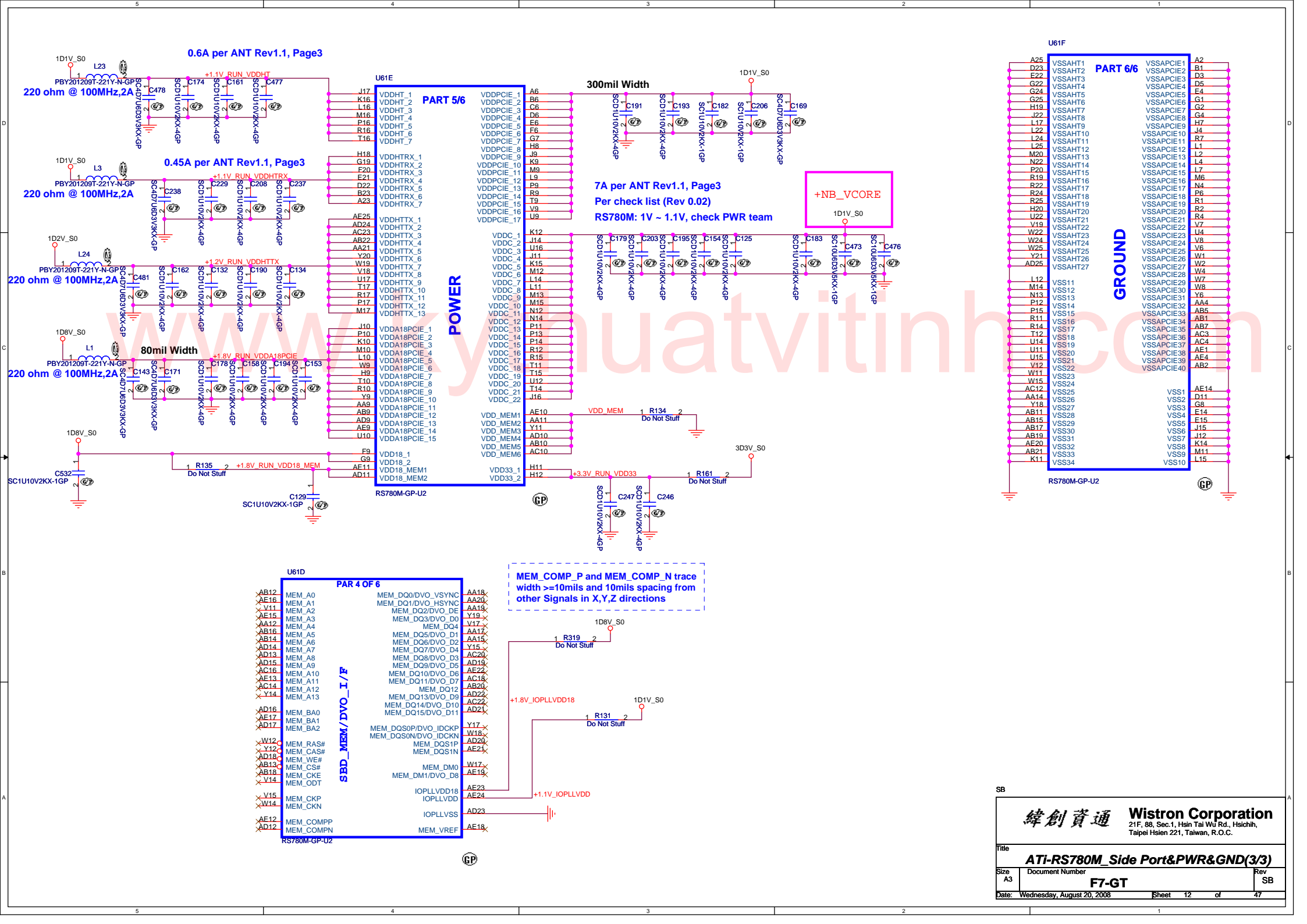
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **ATI-RS780M_LVDS&CRT (2/4)**

Size A3 Document Number **F7-GT** Rev SB

Date: Tuesday, September 02, 2008 Sheet 11 of 47

20080722
Near NB



0.6A per ANT Rev1.1, Page3

0.45A per ANT Rev1.1, Page3

80mil Width

300mil Width

7A per ANT Rev1.1, Page3
Per check list (Rev 0.02)
RS780M: 1V ~ 1.1V, check PWR team

+NB_VCORE

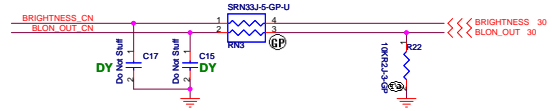
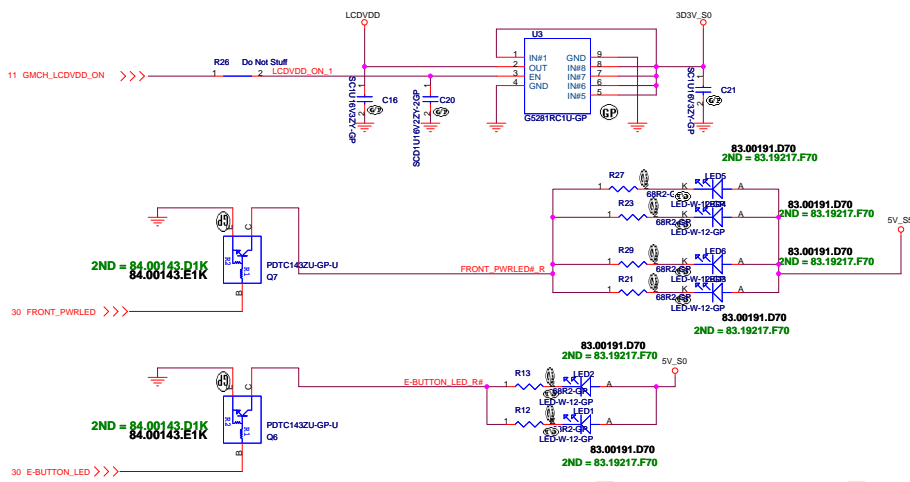
POWER

GROUND

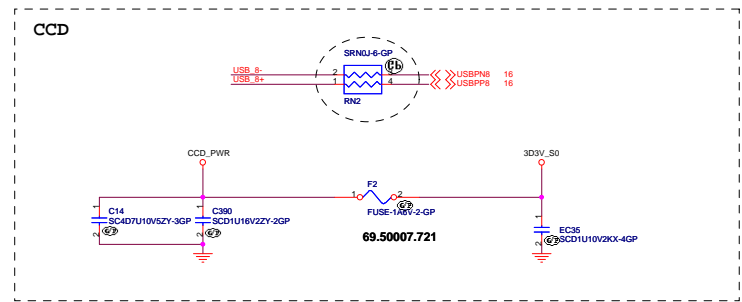
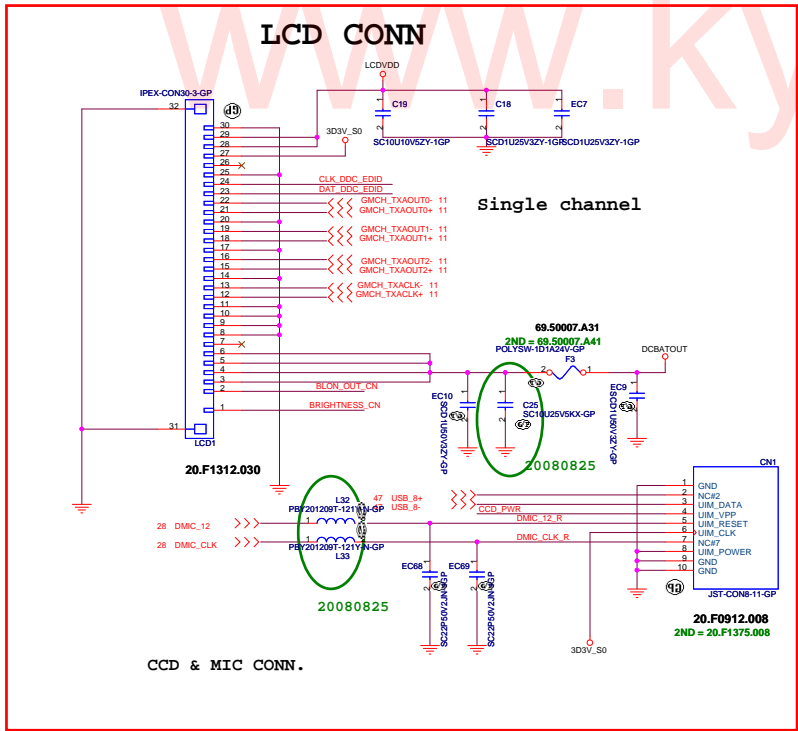
MEM_COMP_P and MEM_COMP_N trace width >=10mils and 10mils spacing from other Signals in X,Y,Z directions

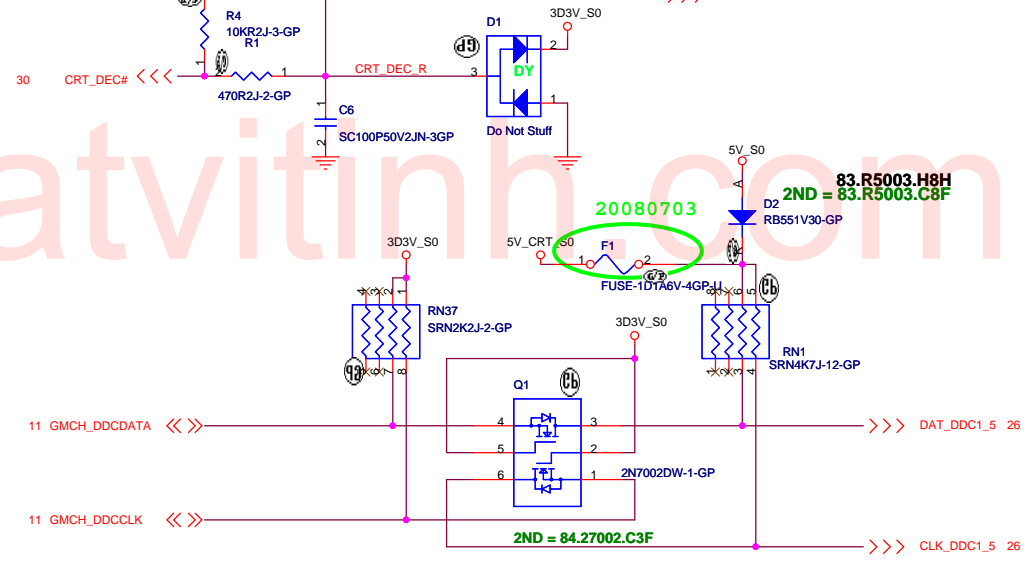
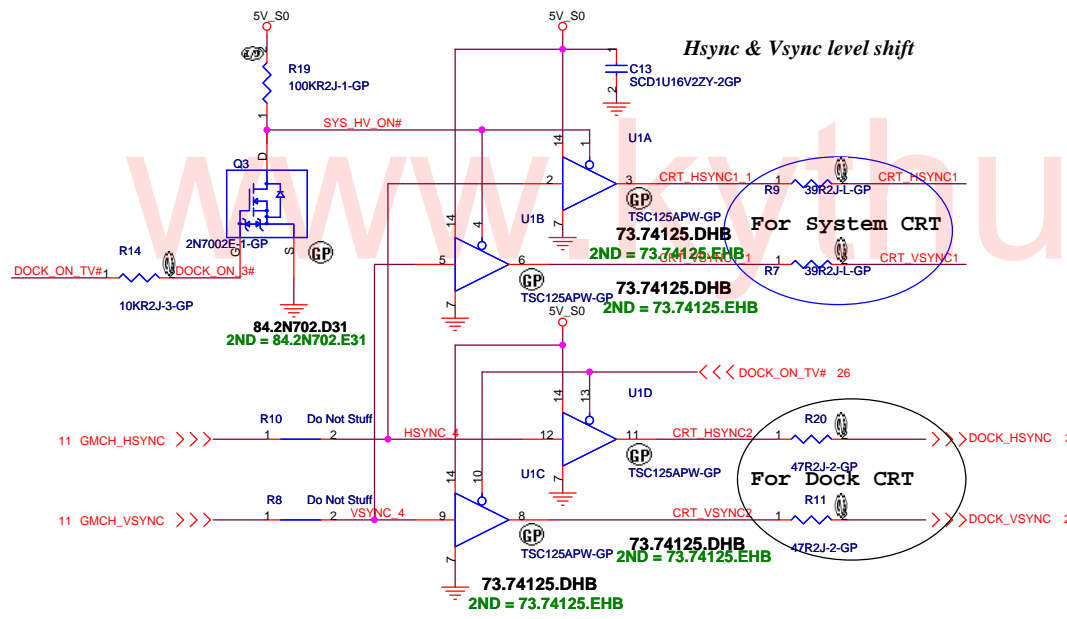
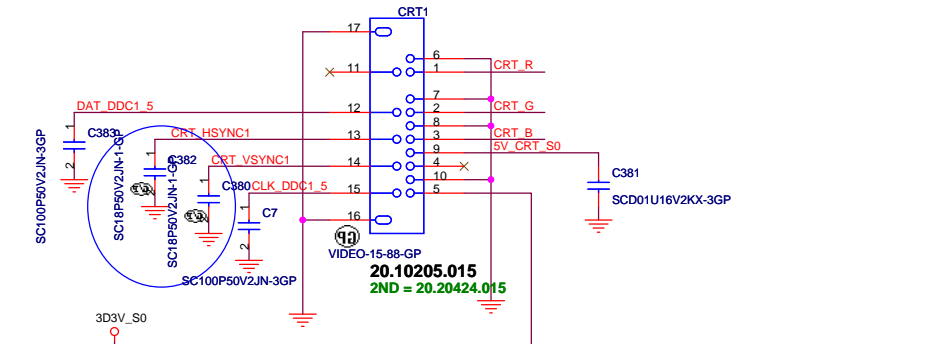
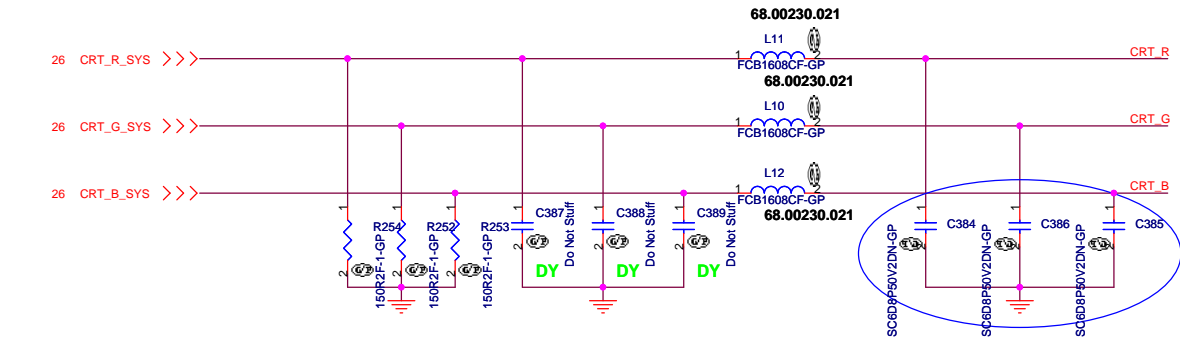
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

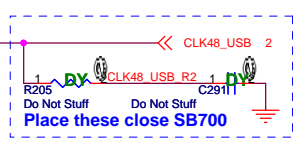
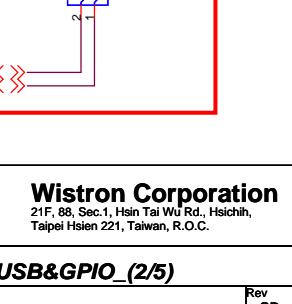
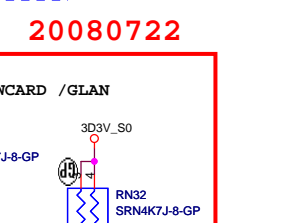
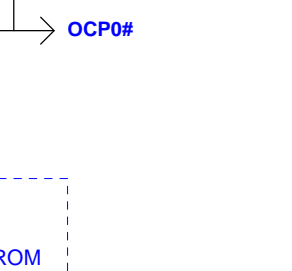
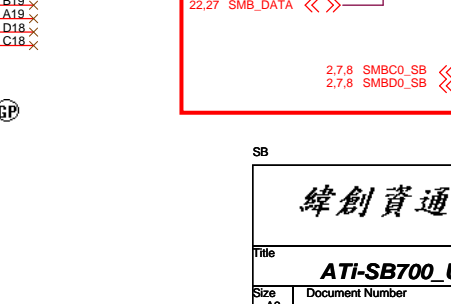
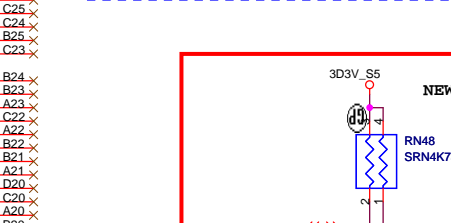
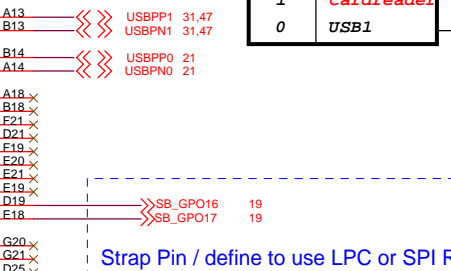
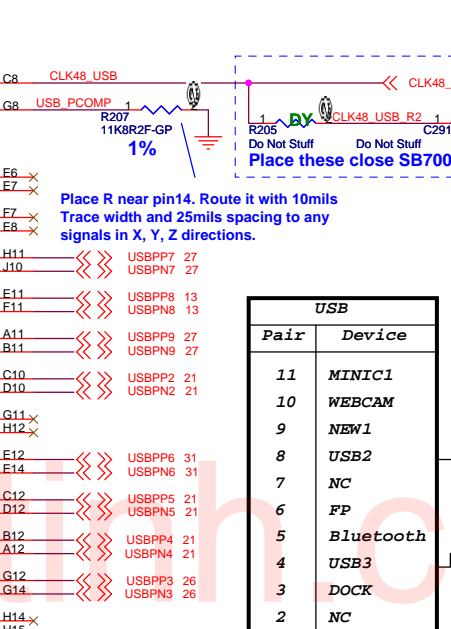
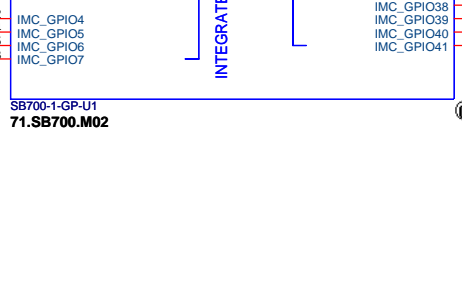
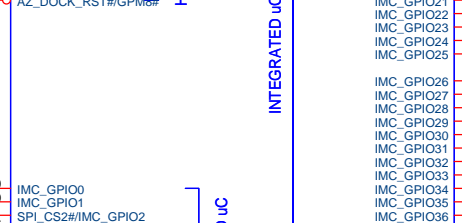
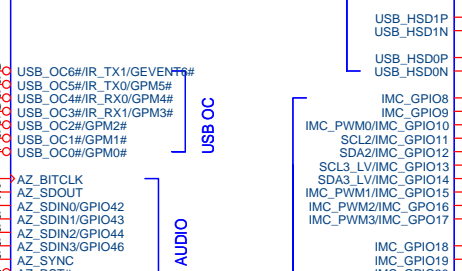
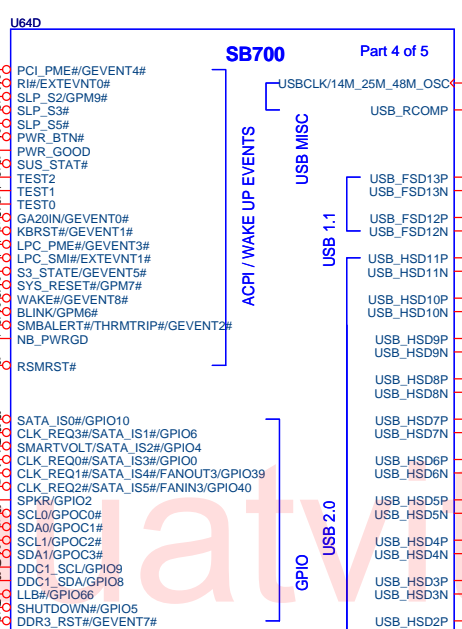
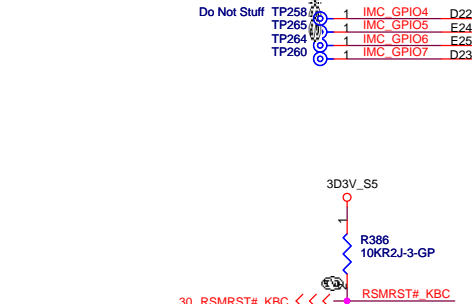
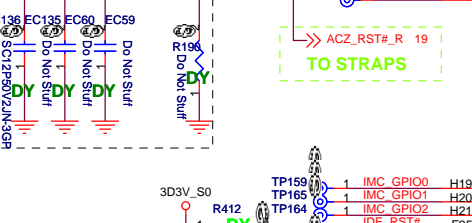
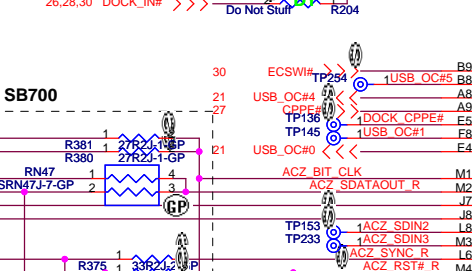
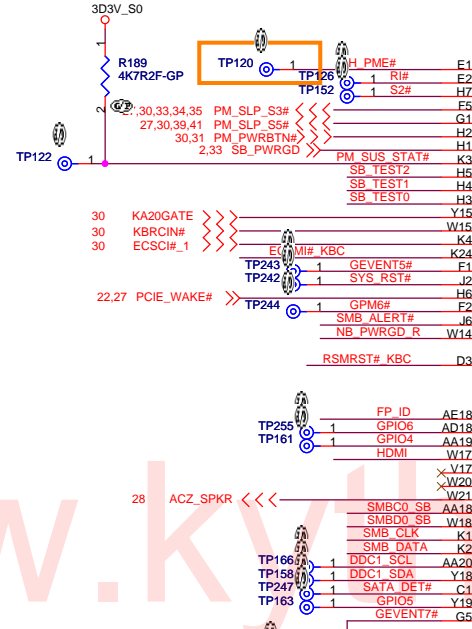
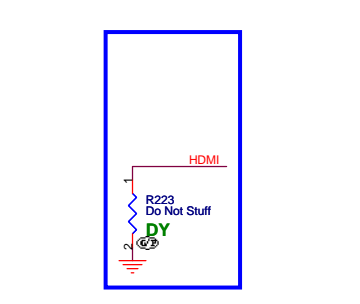
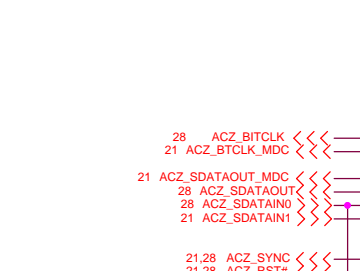
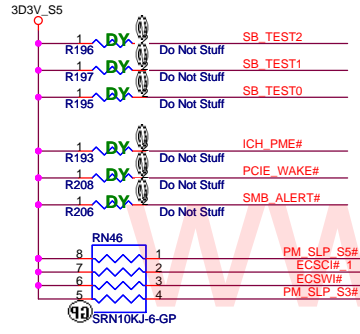
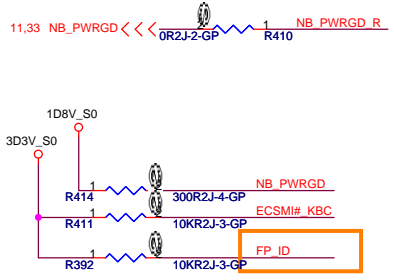
Title	ATI-RS780M_Side Port&PWR&GND(3/3)		
Size	Document Number	F7-GT	Rev
A3			SB
Date:	Wednesday, August 20, 2008	Sheet	12 of 47



20080731 change connect





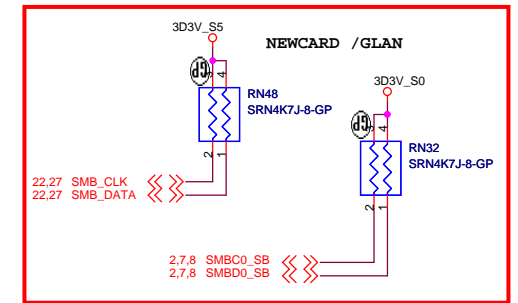


Place R near pin14. Route it with 10mils Trace width and 25mils spacing to any signals in X, Y, Z directions.

Pair	Device
11	MINIC1
10	WEBCAM
9	NEW1
8	USB2
7	NC
6	FP
5	Bluetooth
4	USB3
3	DOCK
2	NC
1	Cardreader
0	USB1

OCP4#
OCP0#

Strap Pin / define to use LPC or SPI ROM



20080722

SB700-1-GP-U1
71.SB700.M02

SB

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **ATI-SB700_USB&GPIO_(2/5)**

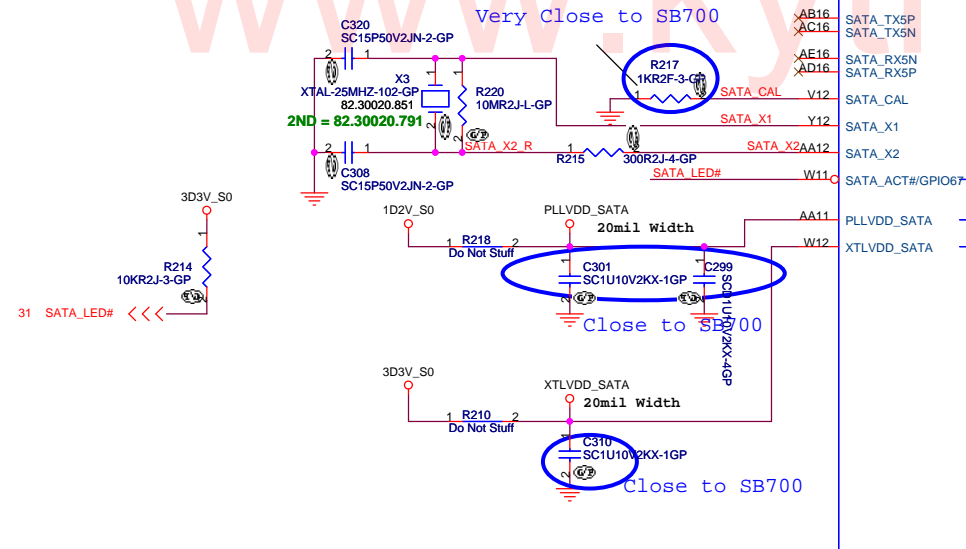
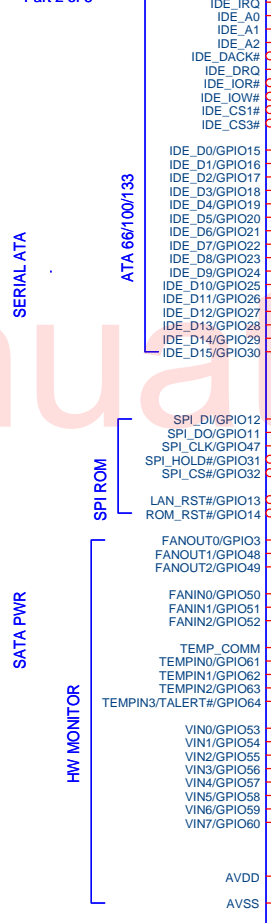
Size: A3 Document Number: **F7-GT** Rev: SB

Date: Friday, August 29, 2008 Sheet 16 of 47

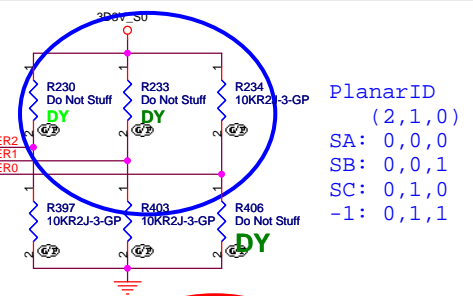
PLACE SATA AC DECOUPLING CAPS CLOSE TO SB700



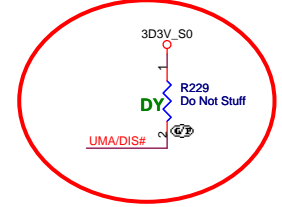
SB700
Part 2 of 5



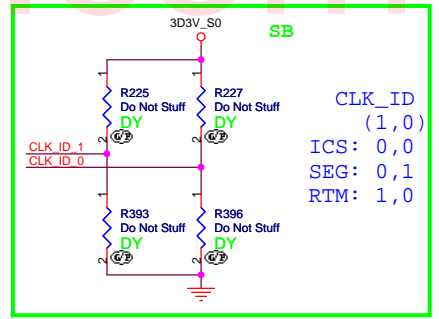
20080825



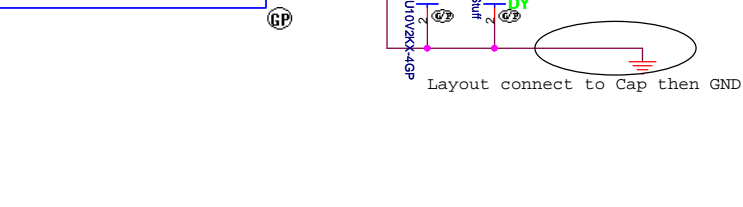
PlanarID
(2,1,0)
SA: 0,0,0
SB: 0,0,1
SC: 0,1,0
-1: 0,1,1



20080722



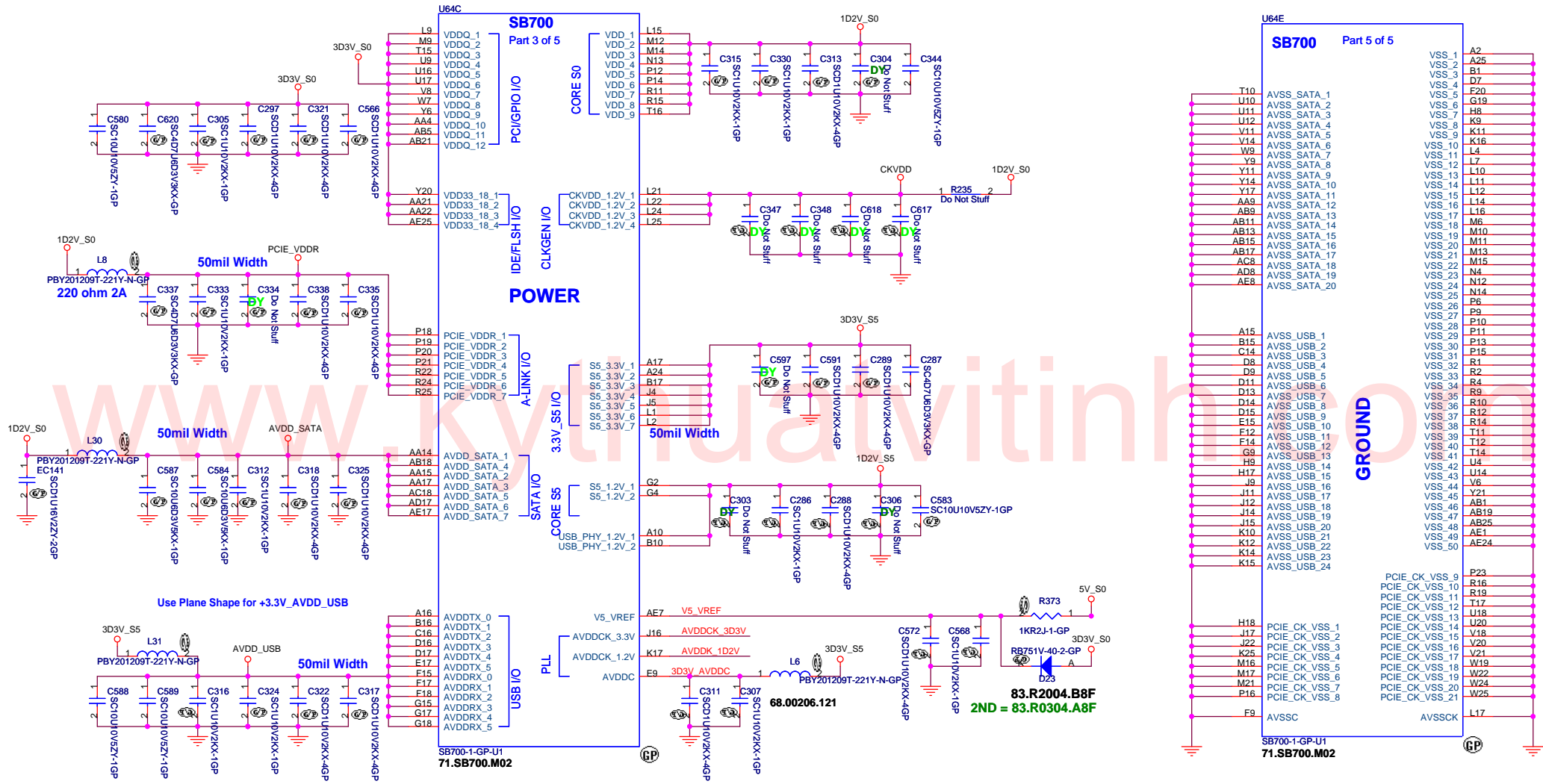
CLK_ID
(1,0)
ICS: 0,0
SEG: 0,1
RTM: 1,0



SB

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title ATI-SB700 SATA-IDE (3/5)		
Size A3	Document Number F7-GT	Rev SB
Date: Friday, August 29, 2008	Sheet 17 of 47	



SB

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

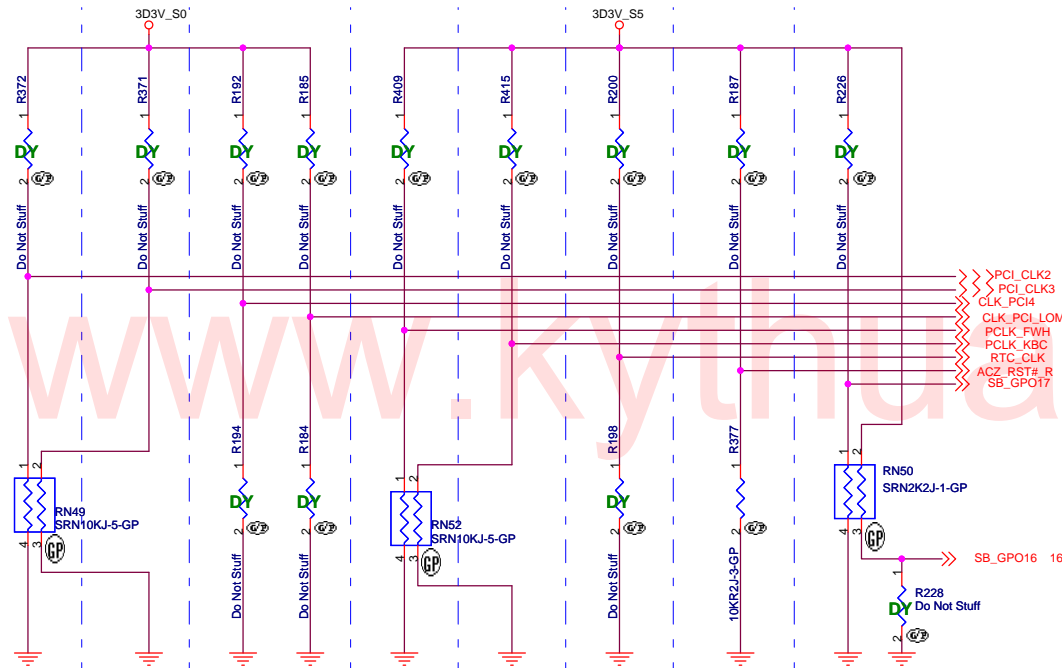
Title: **ATI-SB700 POWER&GND (4/5)**

Size: **A3** Document Number: **F7-GT** Rev: **SB**

Date: Tuesday, August 26, 2008 Sheet 18 of 47

REQUIRED STRAPS

REQUIRED SYSTEM STRAPS



- PCI_CLK2 15
- PCI_CLK3 15
- CLK_PCI4 15
- CLK_PCI_LOM 15
- PCLK_FWH 15,32
- PCLK_KBC 15,30
- RTC_CLK 15,34
- AZ_RST#_R 16
- SB_GPO17 16

DEBUG STRAPS

- TP230 1 PCI_AD23 15
- TP229 1 PCI_AD24 15
- TP128 1 PCI_AD24 15
- TP240 1 PCI_AD25 15
- TP124 1 PCI_AD26 15
- TP239 1 PCI_AD27 15
- TP228 1 PCI_AD28 15
- TP238 1 PCI_AD29 15
- TP238 1 PCI_AD30 15

	PCI_CLK2	PCI_CLK3	CLK_PCI_LOM CLK_PCI4	PCLK_FWH	PCLK_KBC	RTCCLK	AZ_RST#	SB_GPO17 , SB_GPO16
PULL HIGH	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	RESERVED	IMC ENABLED	CLKGEN ENABLED (Use Internal)	INTERNAL RTC DEFAULT	ENABLE PCI ROM BOOT	H, H = Reserved H, L = SPI ROM DEFAULT
PULL LOW	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT		IMC DISABLED DEFAULT	CLKGEN DISABLED (Use External) DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI ROM BOOT DEFAULT	L, H = LPC ROM L, L = FWH ROM

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTCCLK

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23	PCI_AD30 PCI_AD29
PULL HIGH	USE LONG RESET (DEFAULT)	USE PCI PLL (DEFAULT)	USE ACPI BCLK (DEFAULT)	USE IDE PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Reserved (DEFAULT)	Reserved
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved	Reserved

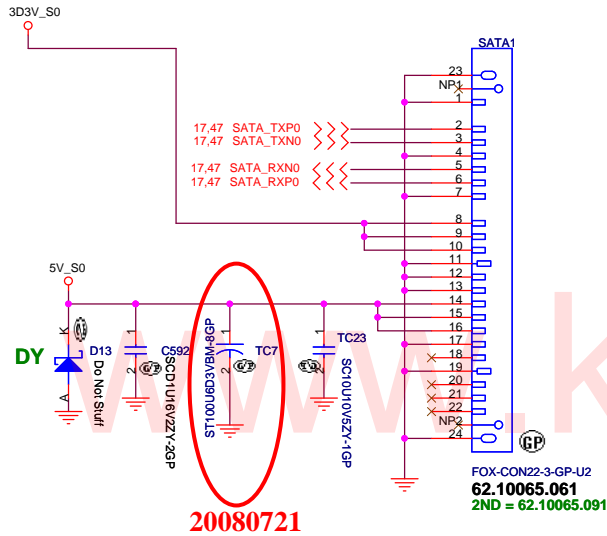
Note: SB700 has 15K internal PU FOR PCI_AD[30:23]

緯創資通 **Wistron Corporation**
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

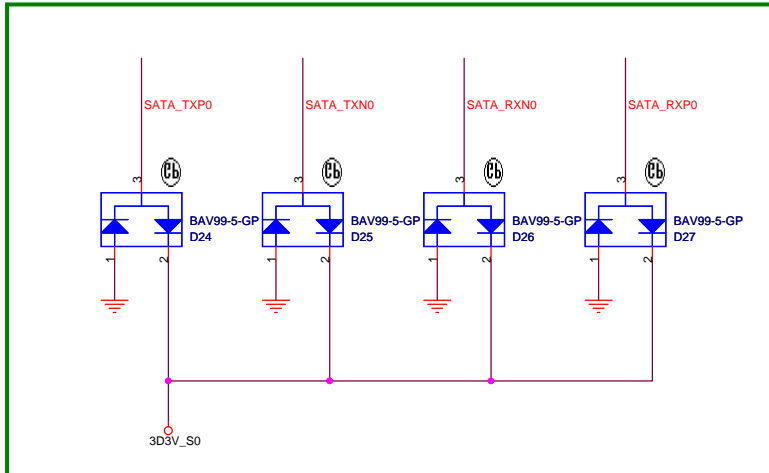
Title: **ATI-SB700 STRAPPING (5/5)**

Size: A3	Document Number: F7-GT	Rev: SB
Date: Friday, August 29, 2008	Sheet: 19 of 47	

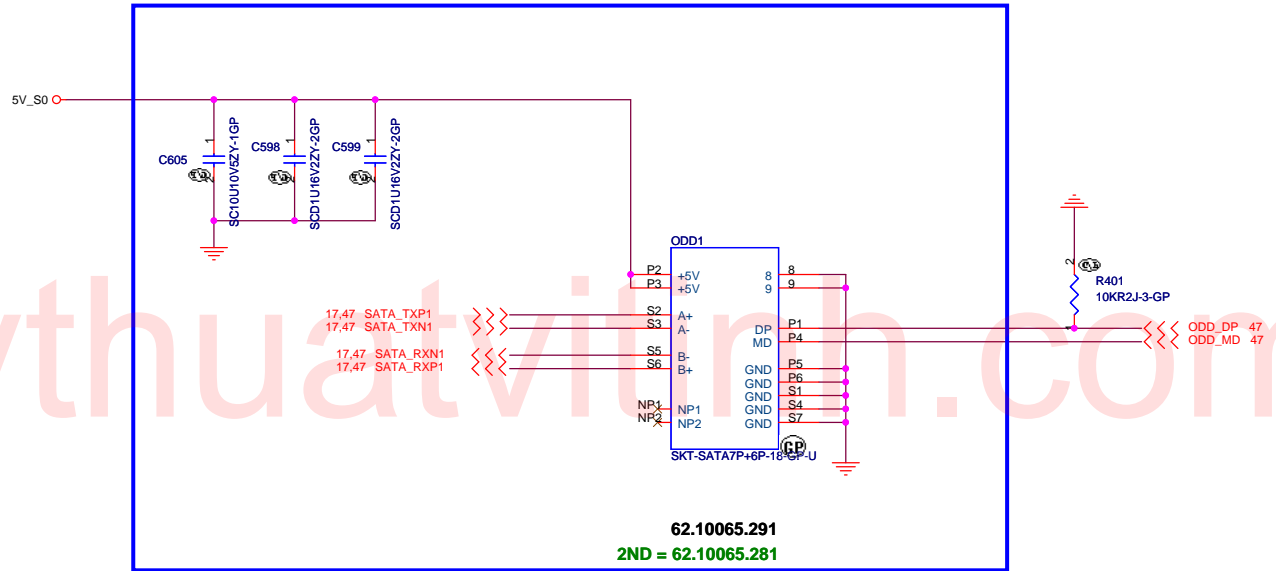
SATA HDD Connector



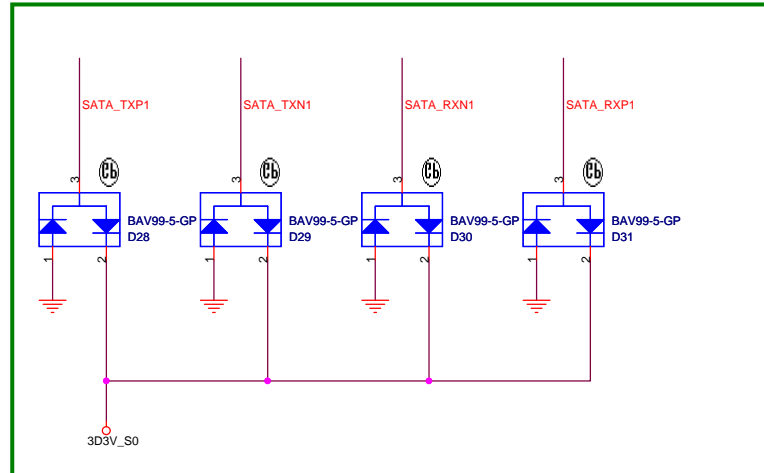
For HDD

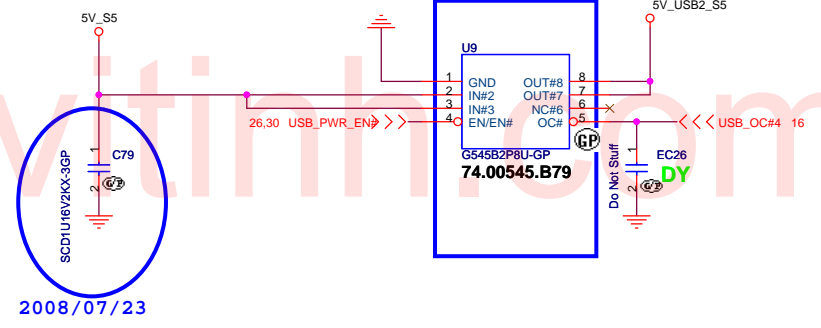
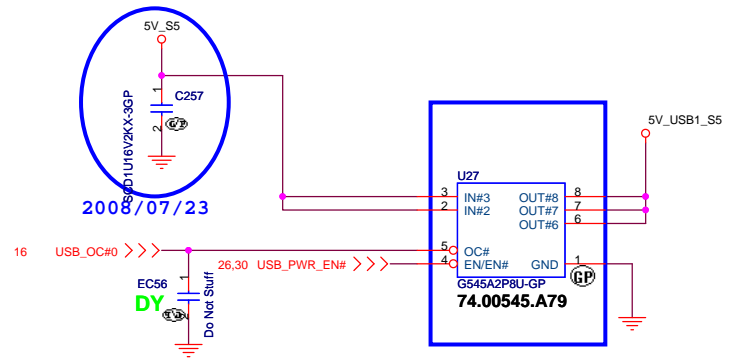
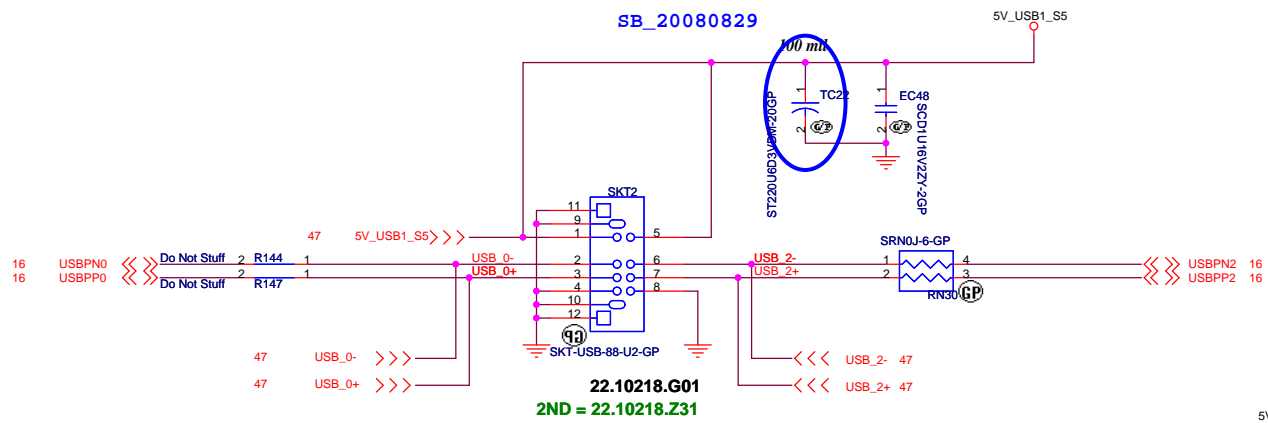


20080714 SATA ODD Connector



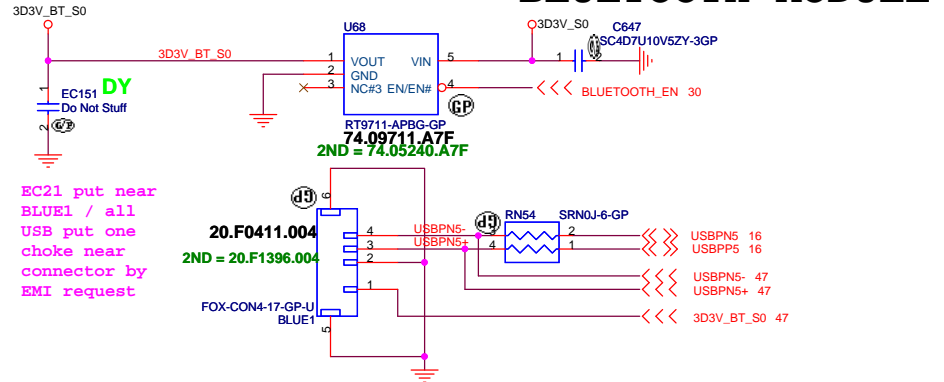
For ODD





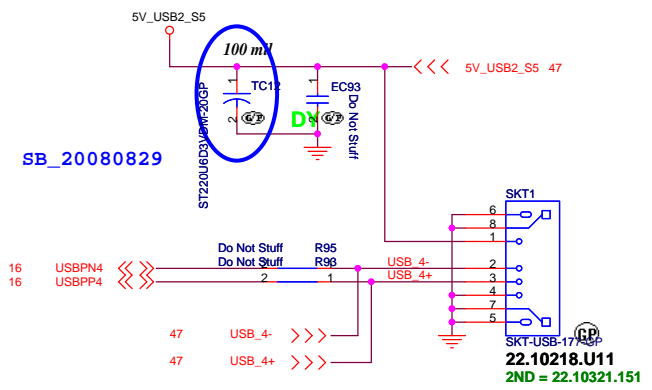
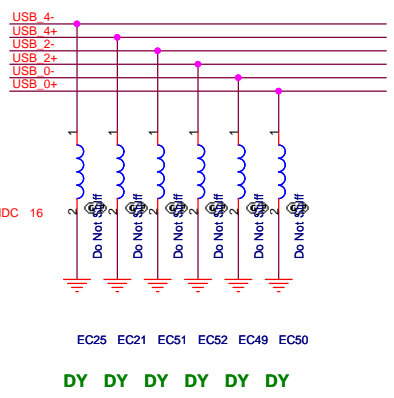
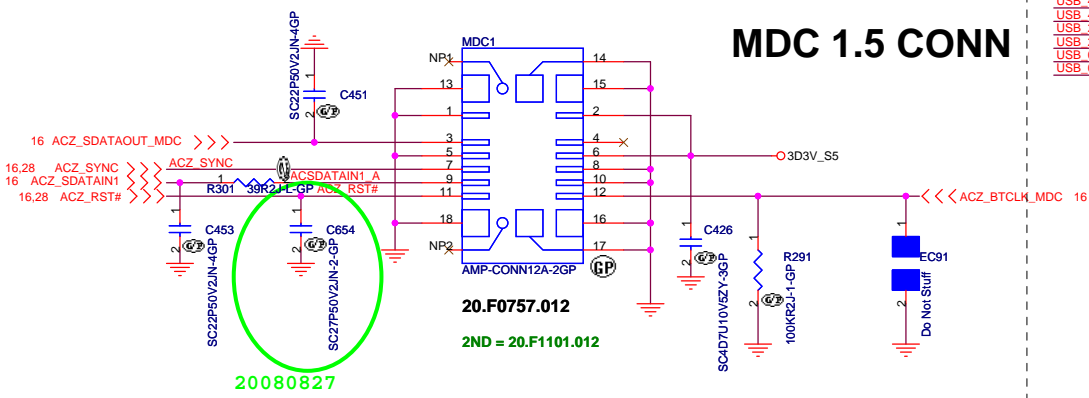
www.kythuatuatv.com

BLUETOOTH MODULE



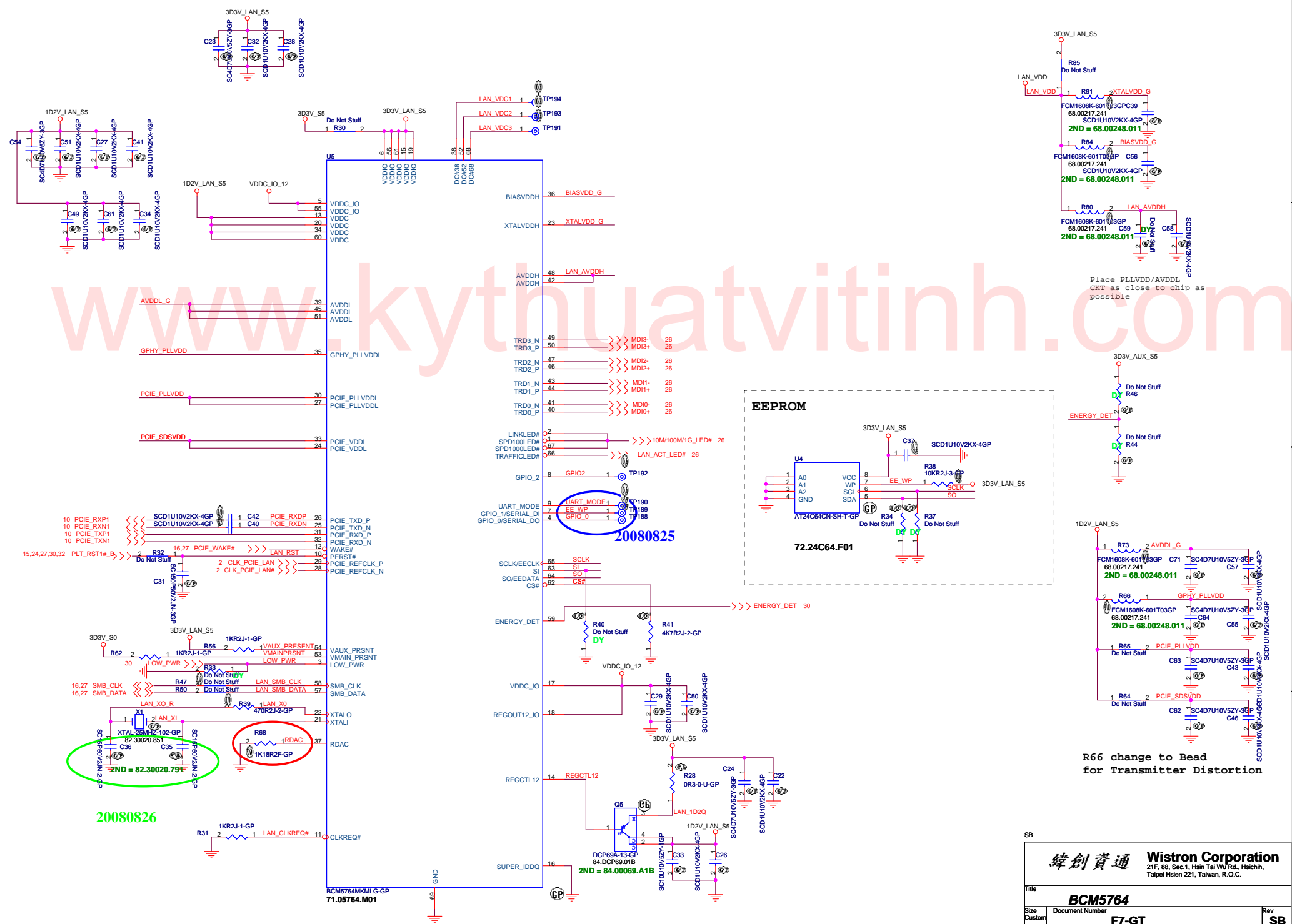
EC21 put near BLUE1 / all USB put one choke near connector by EMI request

MDC 1.5 CONN



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USB / MDC / BLUETOOTH			
Title	Document Number		Rev
	F7-GT		SB
Date: Friday, August 29, 2008	Sheet 21	of	47

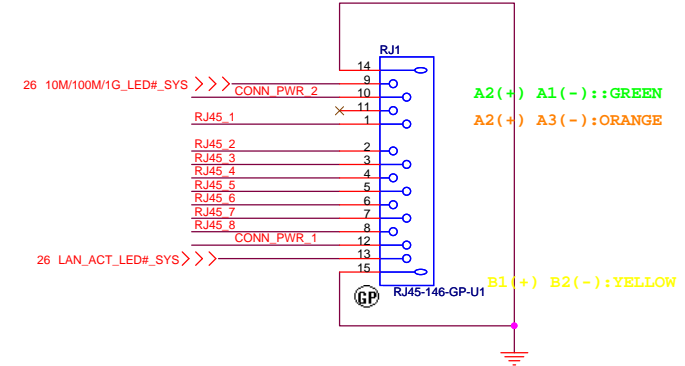
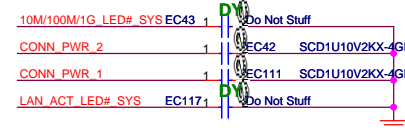
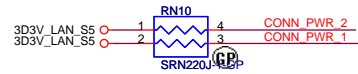
www.kythuathatvithinh.com



Place PLLVDD/AVDDL CKT as close to chip as possible

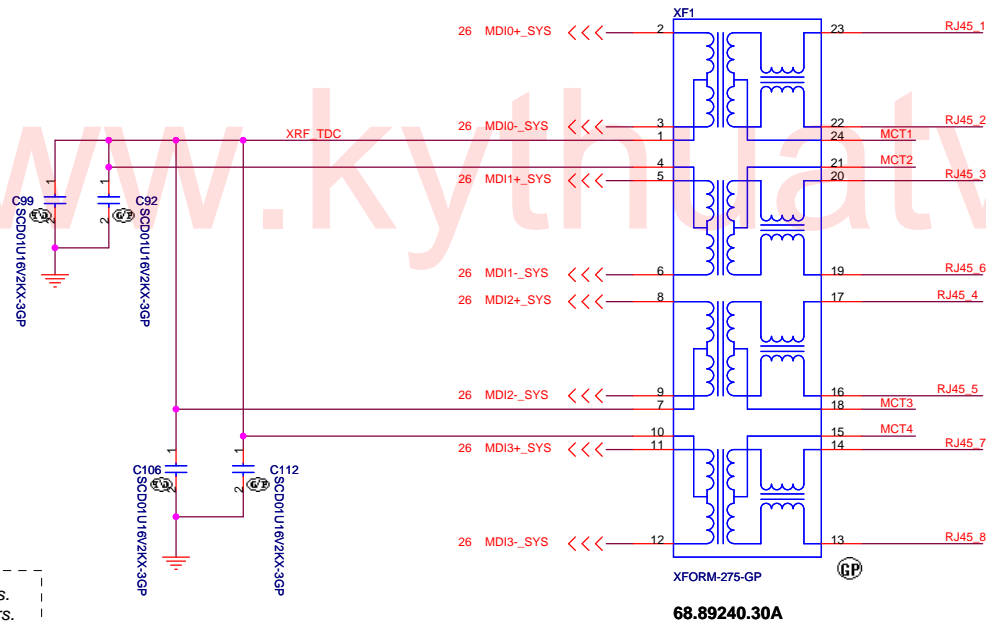
R66 change to Bead for Transmitter Distortion

LAN Connector



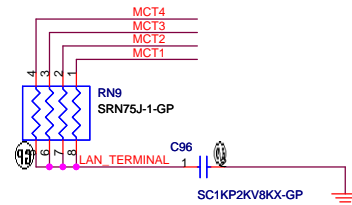
22.10245.R11
2ND = 22.10245.X61

GIGA Lan Transformer



68.89240.30A

- 1. route on bottom as differential pairs.
- 2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3. No vias, No 90 degree bends.
- 4. pairs must be equal lengths.
- 5. 5.6mil trace width, 12mil separation.
- 6. 3.6mil between pairs and any other trace.
- 7. Must not cross ground moat, except RJ-45 moat.



10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

www.kytronic.com

SB

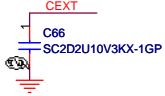
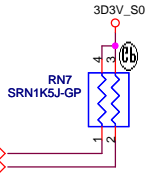
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN Connector**

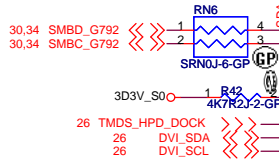
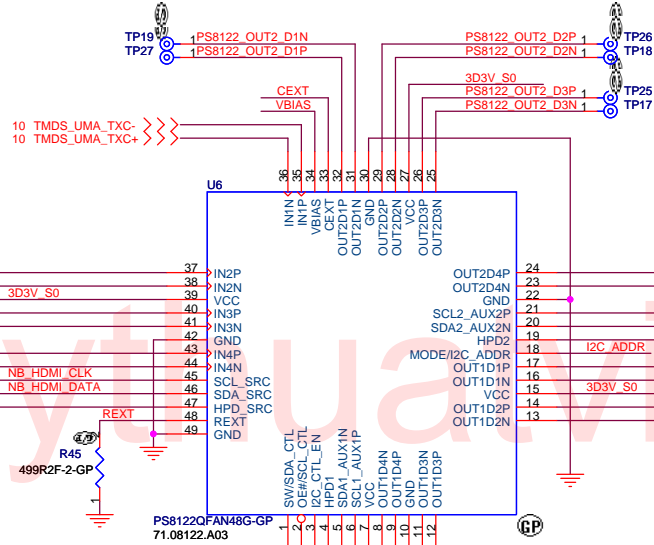
Size A3 Document Number **F7-GT** Rev **SB**

Date: Friday, August 29, 2008 Sheet 23 of 47

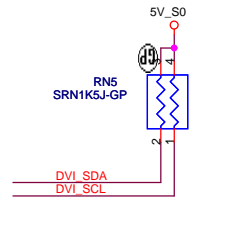
11 NB_HDMI_DATA
11 NB_HDMI_CLK



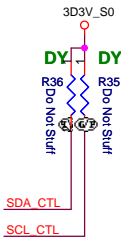
10 TMDS_UMA_TX0-
10 TMDS_UMA_TX0+
10 TMDS_UMA_TX1-
10 TMDS_UMA_TX1+
10 TMDS_UMA_TX2-
10 TMDS_UMA_TX2+
11 NB_HDMI_HPD



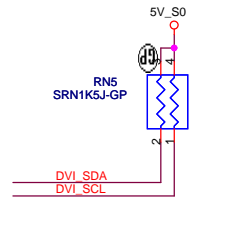
30,34 SMBD_G792
30,34 SMBC_G792



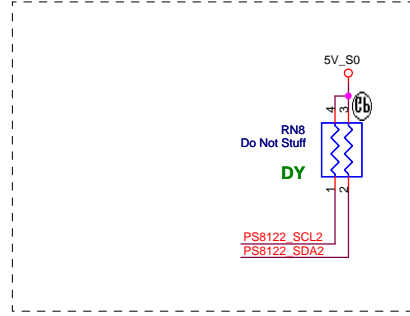
26 TMDS_HPD_DOCK
26 DVI_SDA
26 DVI_SCL



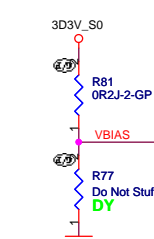
SDA_CTL
SCL_CTL



DVI_SDA
DVI_SCL

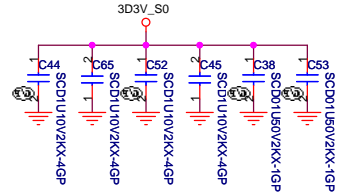


PS8122_SCL2
PS8122_SDA2



I2C_ADDR

3D3V_S0
R81 0R2J-2-GP
VBIAS
R77 Do Not Stuff
DY



PS8122_OUT2_D1N
PS8122_OUT2_D1P
PS8122_OUT2_D2P
PS8122_OUT2_D2N
PS8122_OUT2_D3P
PS8122_OUT2_D3N

PS8122_OUT2_D4P
PS8122_OUT2_D4N
PS8122_SCL2
PS8122_SDA2
PS8122_HPD2

TMDS_A_TXC- 26
TMDS_A_TXC+ 26
TMDS_A_TX0- 26
TMDS_A_TX0+ 26

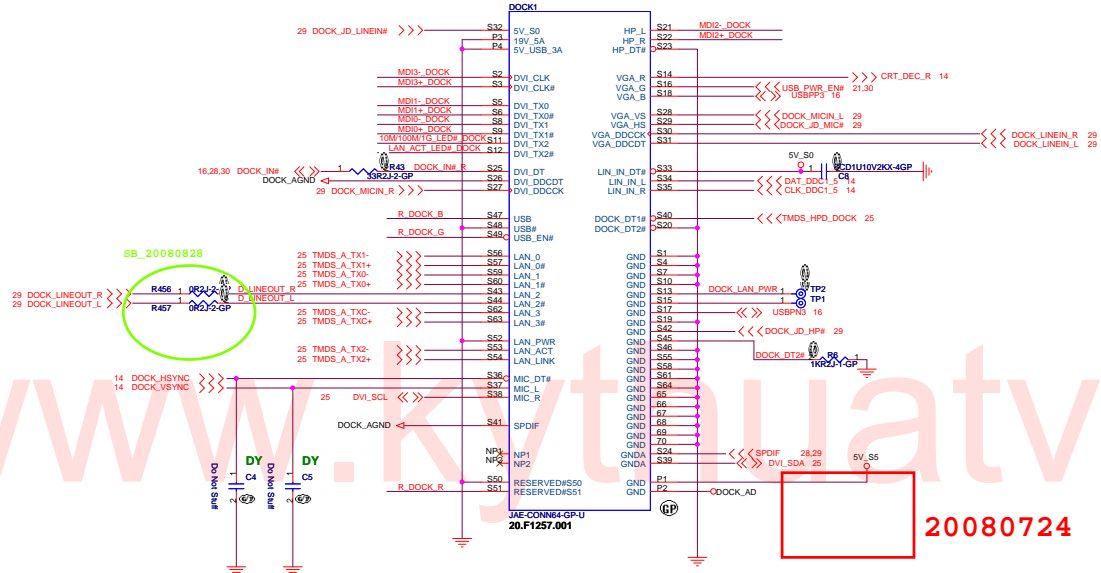
TMDS_A_TX1- 26
TMDS_A_TX1+ 26
TMDS_A_TX2- 26
TMDS_A_TX2+ 26

SB

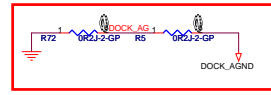
		緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title PS8122			
Size	Document Number	Rev	
	F7-GT	SB	
Date: Friday, August 29, 2008	Sheet	25	of 47

20080709 change to Port Replicator

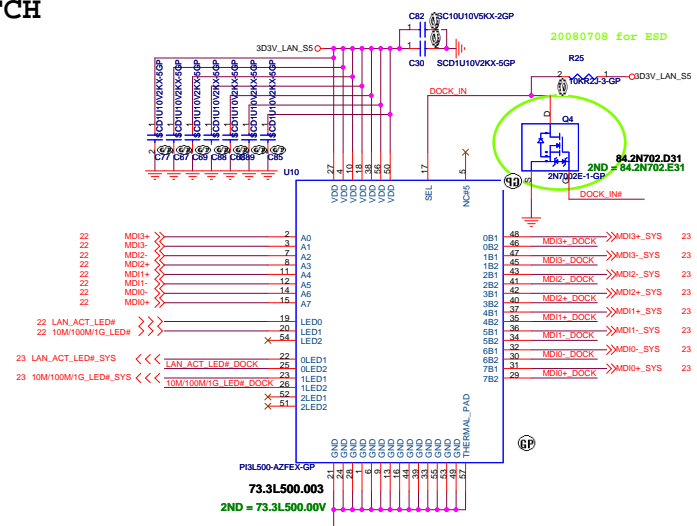
DOCK



20080724

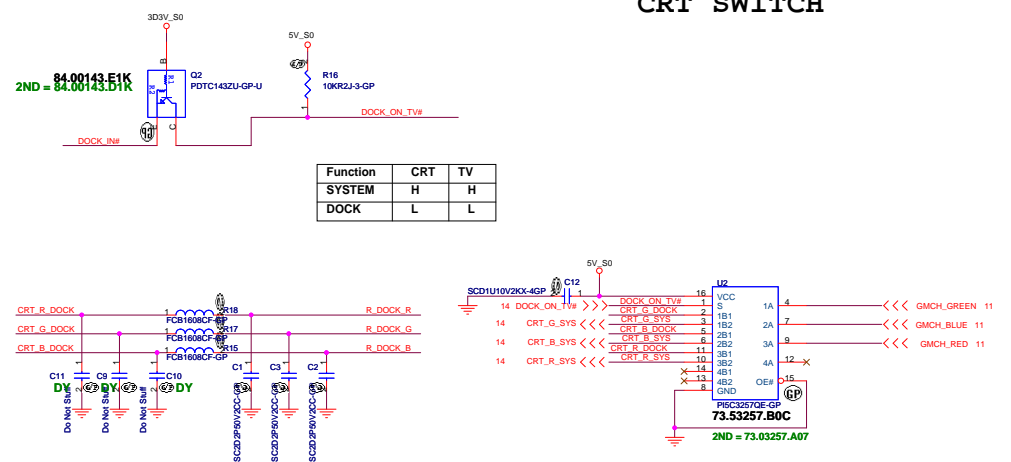


LAN SWITCH



Function	LAN
SYSTEM	L
DOCK	H

CRT SWITCH

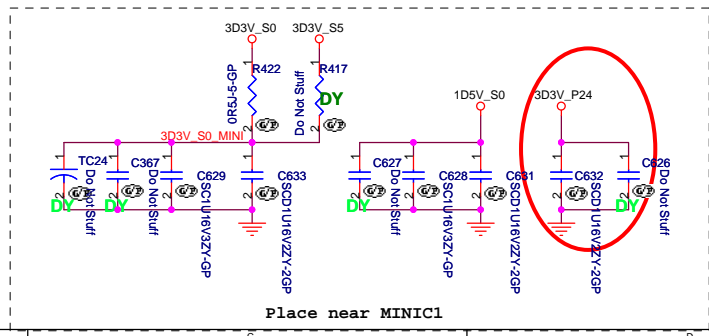
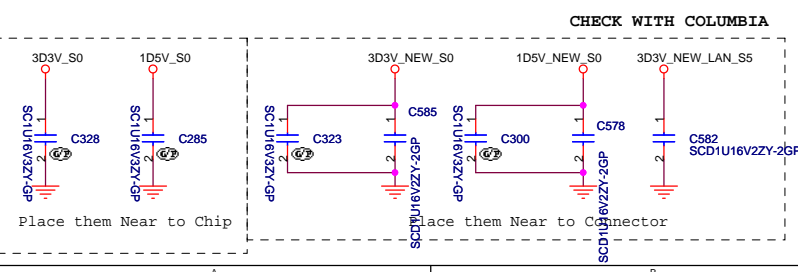
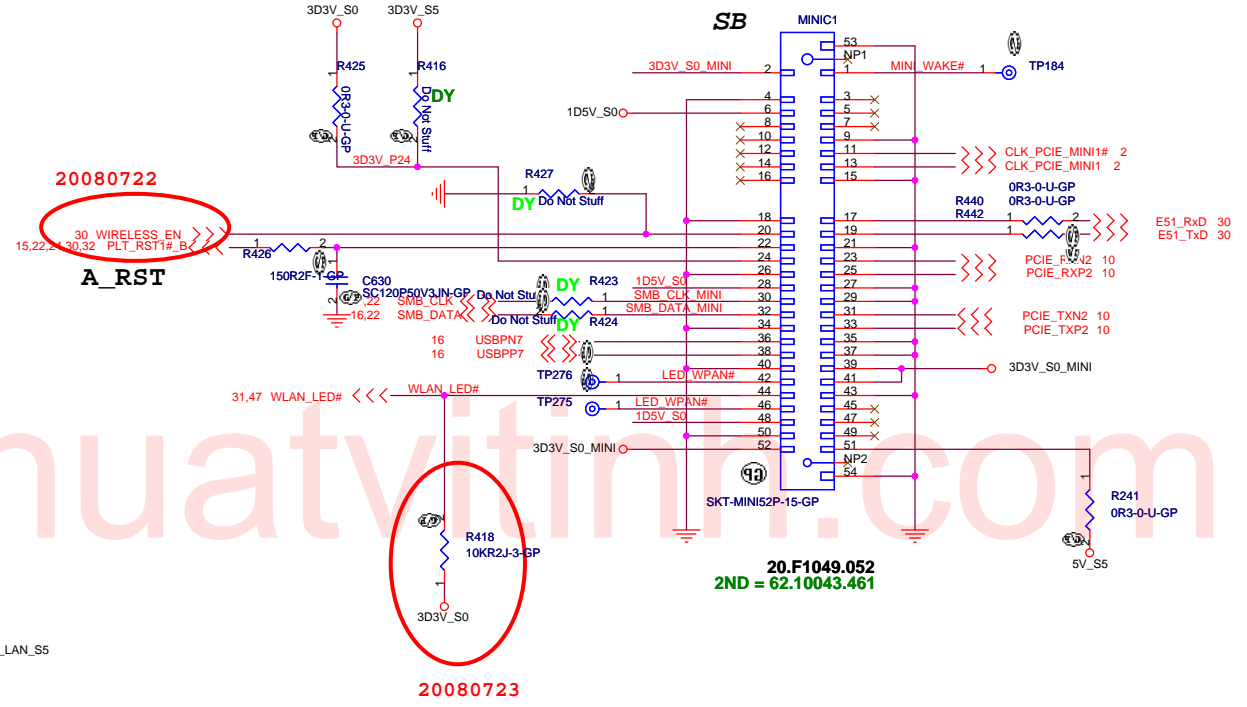
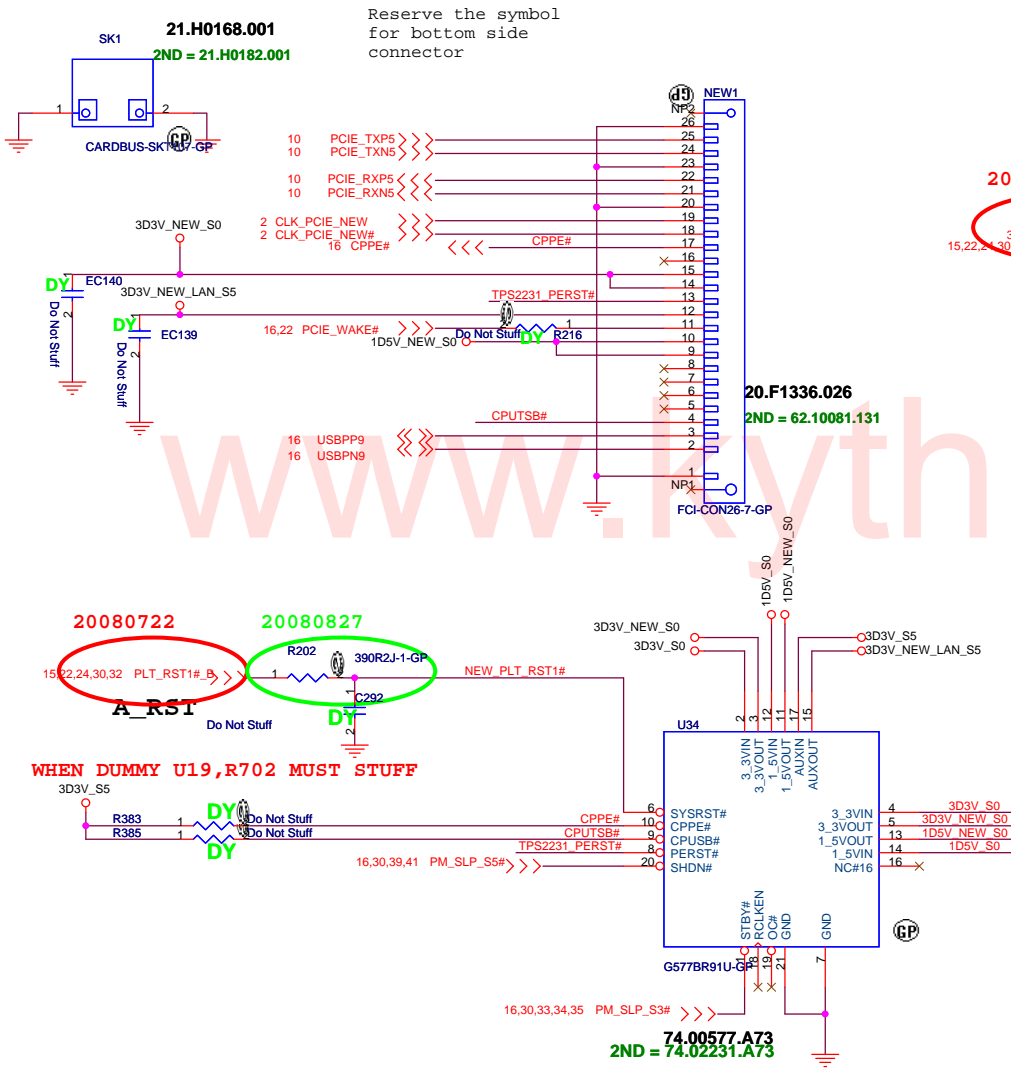


Function	CRT	TV
SYSTEM	H	H
DOCK	L	L

NEWCARD Connector

Mini Card Connector

CHECK / POWER PIN



SB

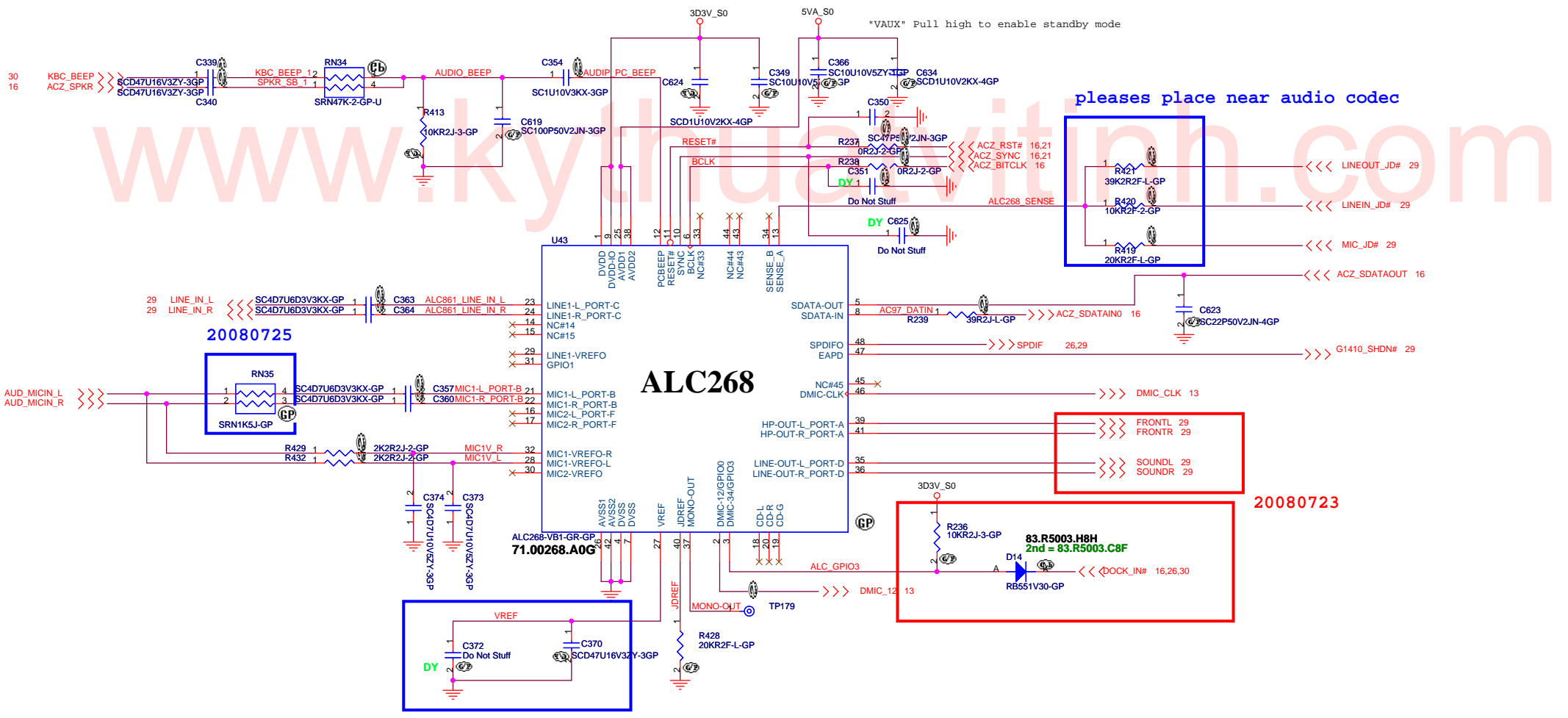
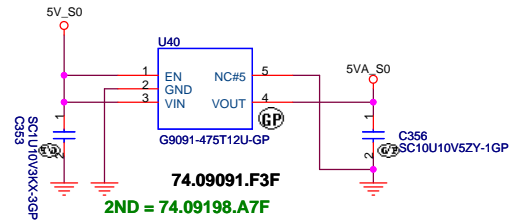
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **MINI CARD / NEW CARD**

Size: Document Number

Rev: SB

Date: Tuesday, September 02, 2008 Sheet 27 of 47



please place near audio codec

please place near audio codec

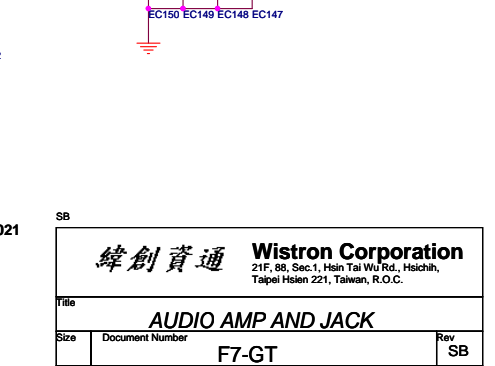
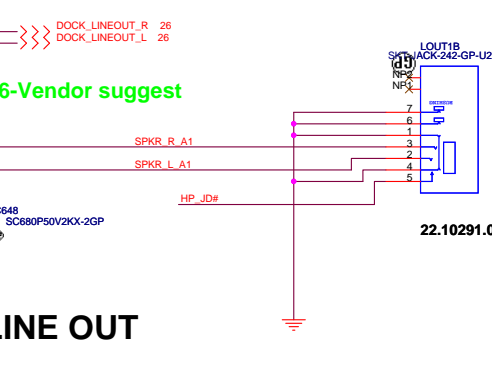
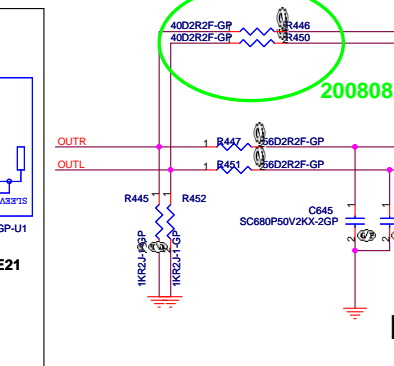
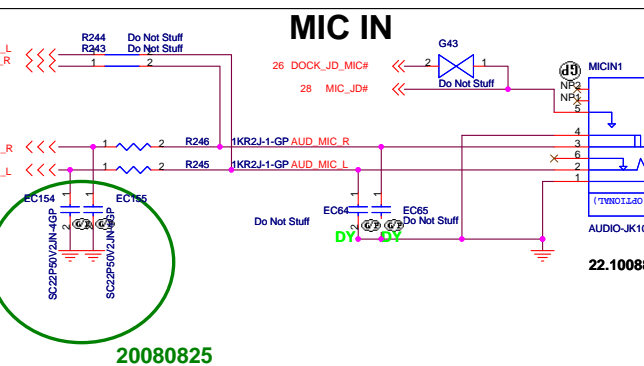
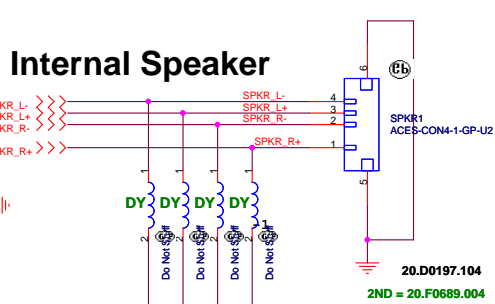
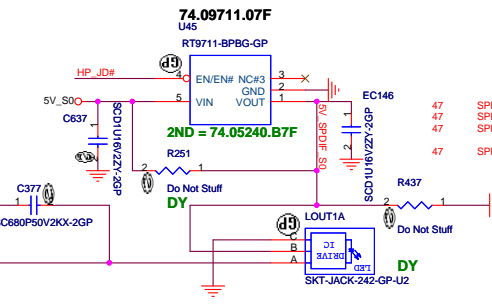
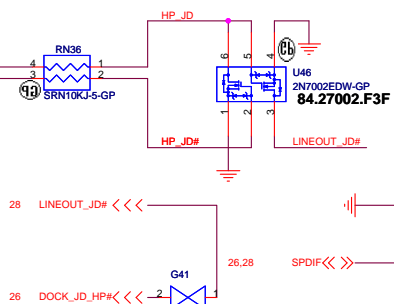
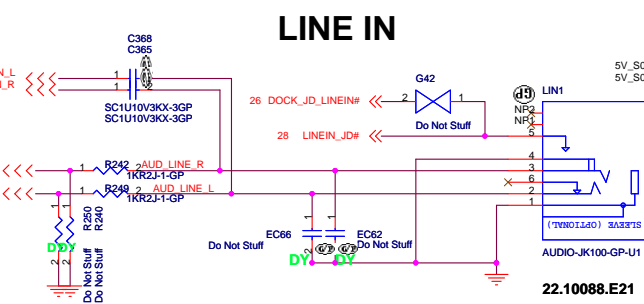
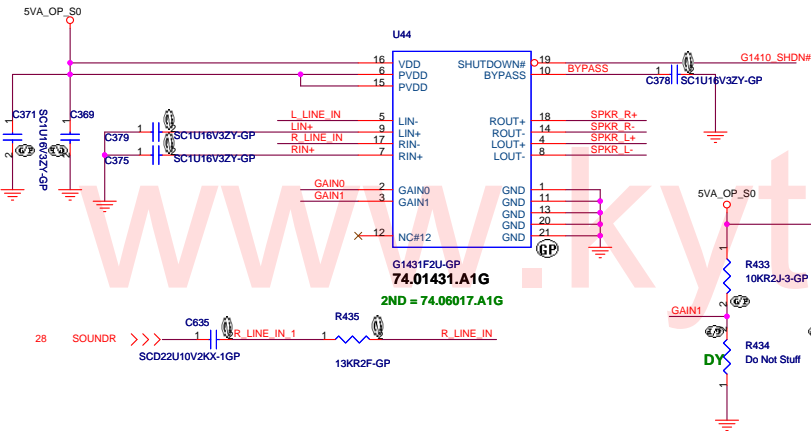
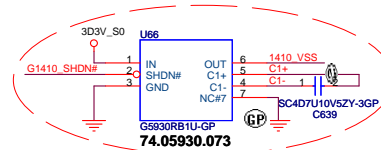
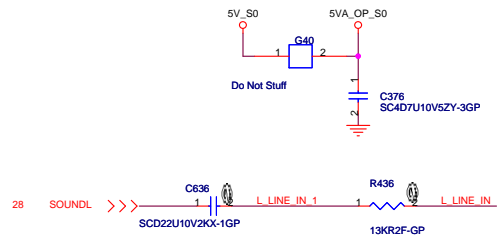
SB

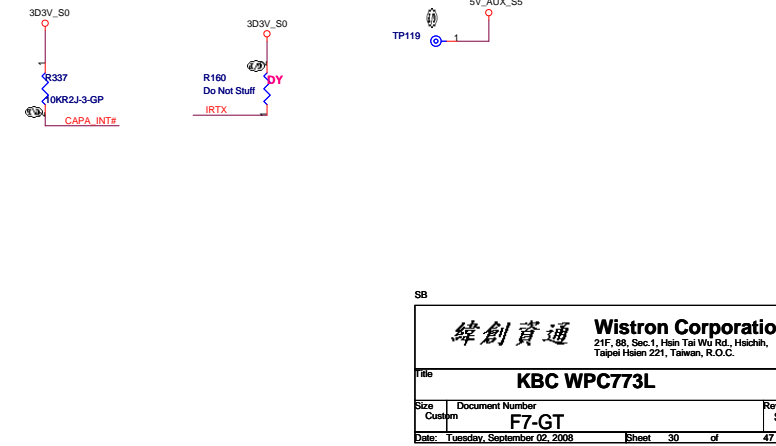
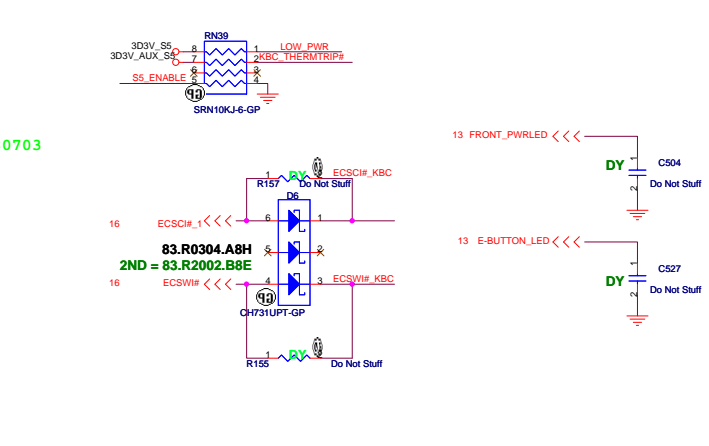
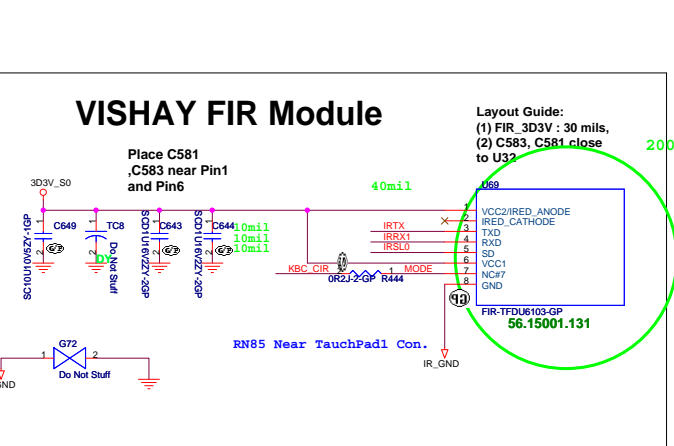
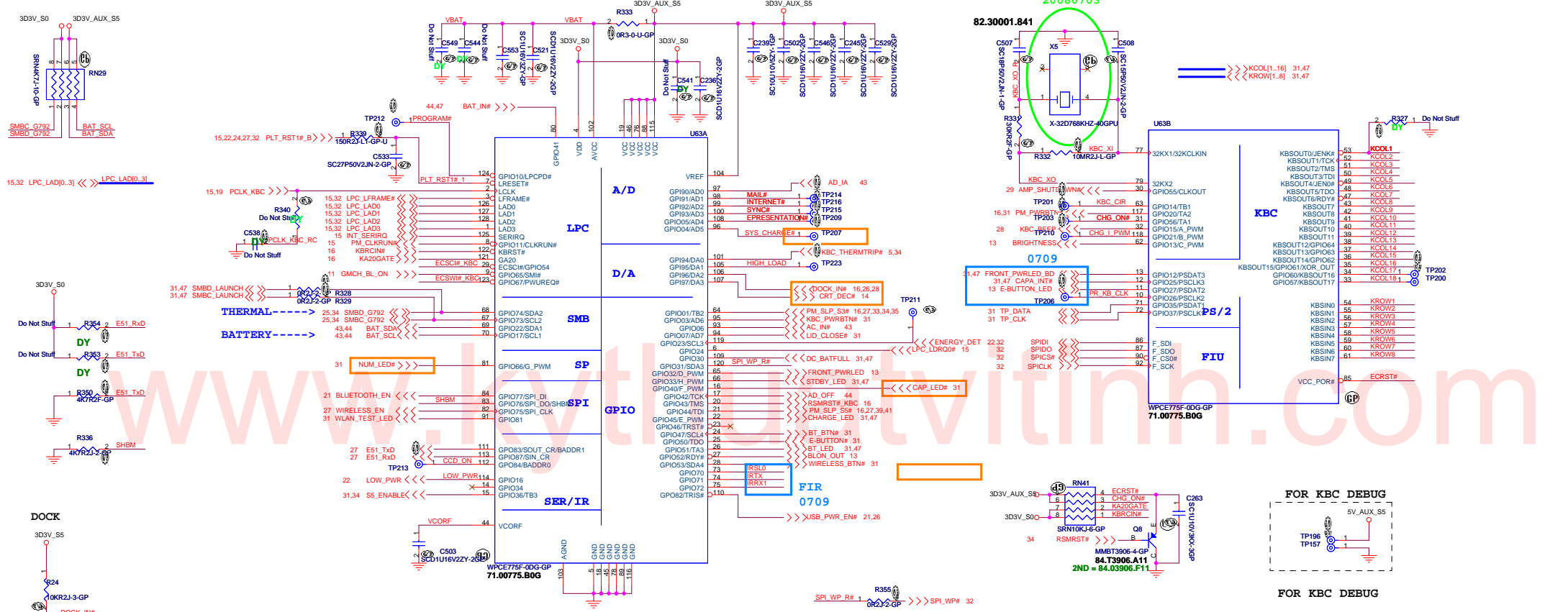
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Title: **AZALIA CODEC - ALC268**

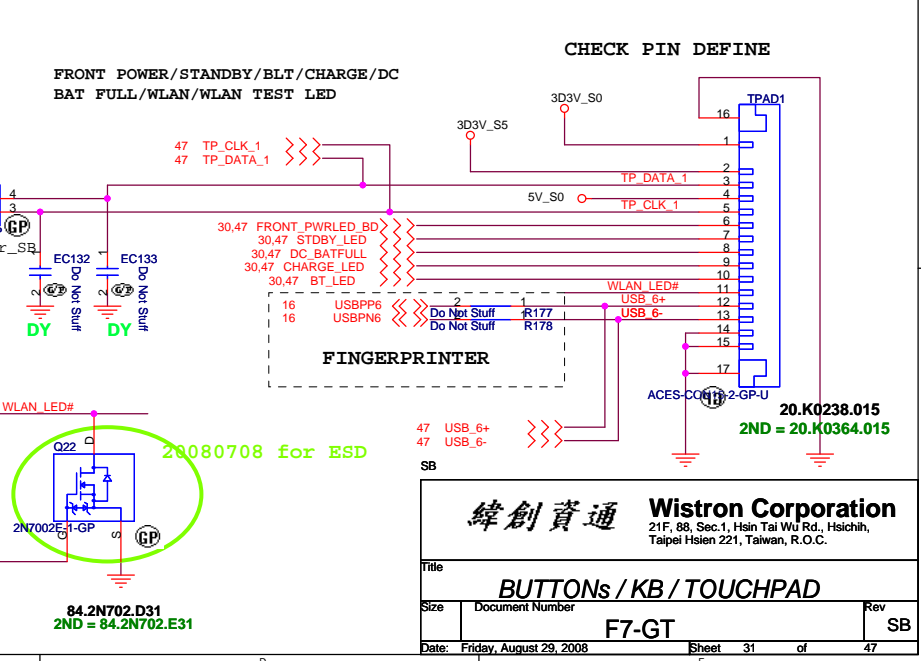
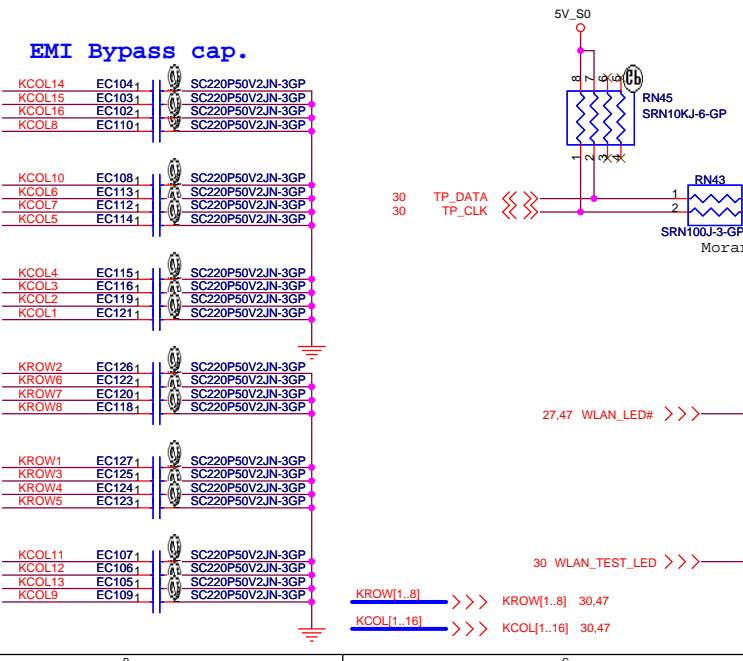
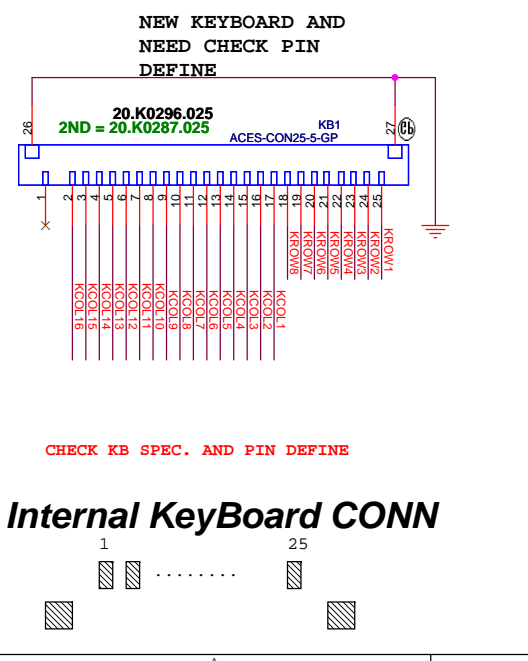
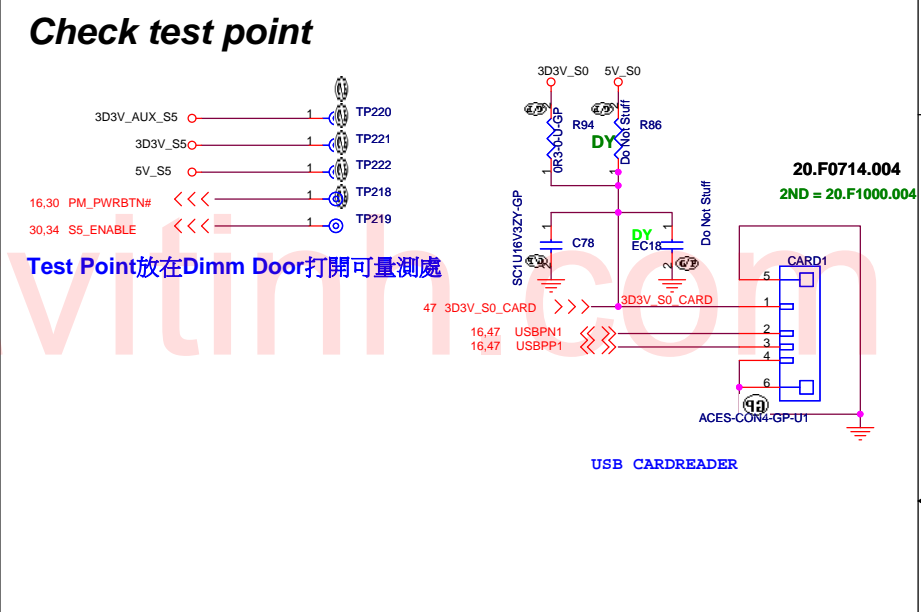
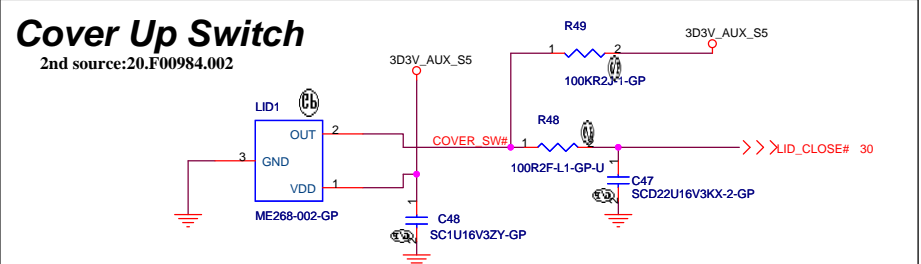
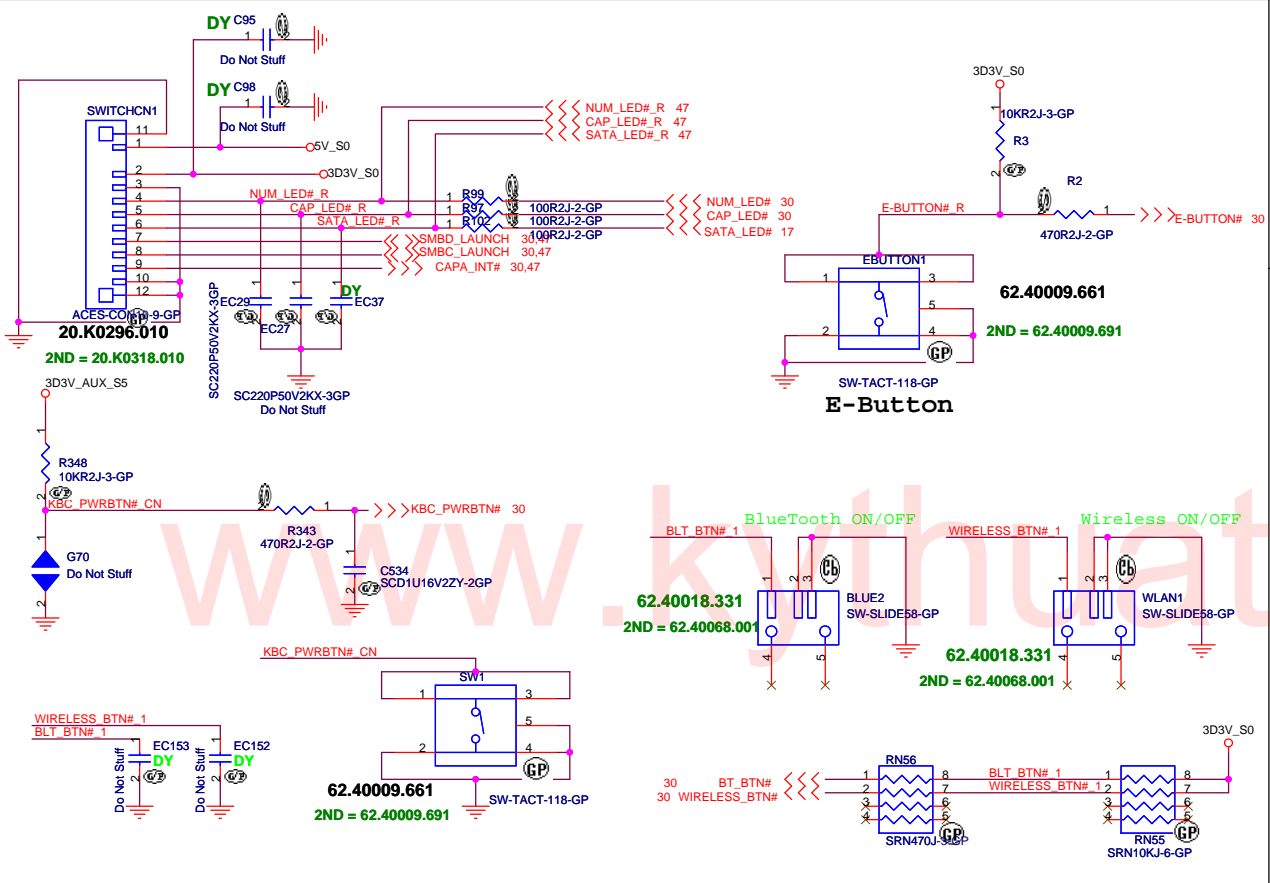
Size: Document Number **F7-GT** Rev: **SB**

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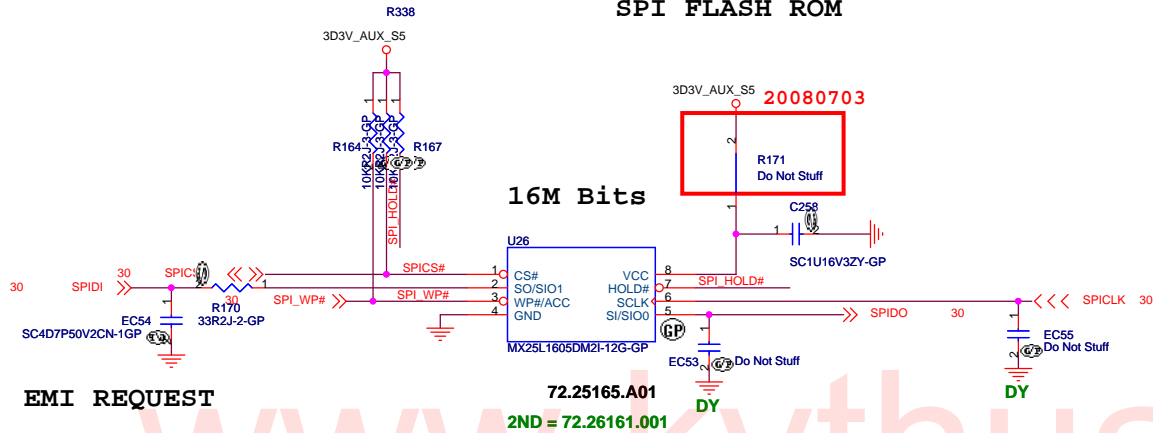




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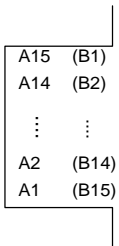


SPI FLASH ROM



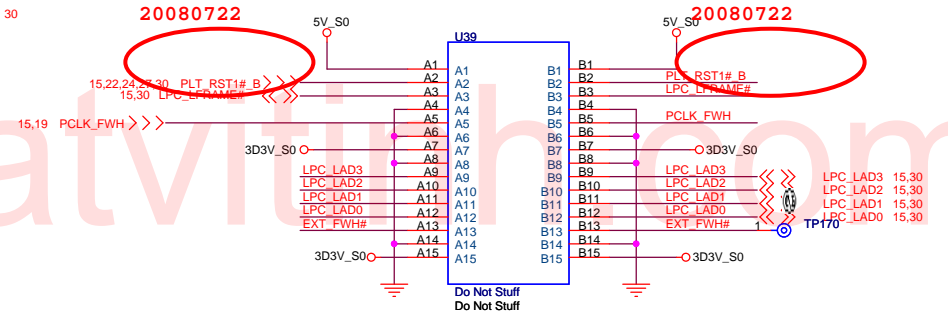
EMI REQUEST

TOP VIEW

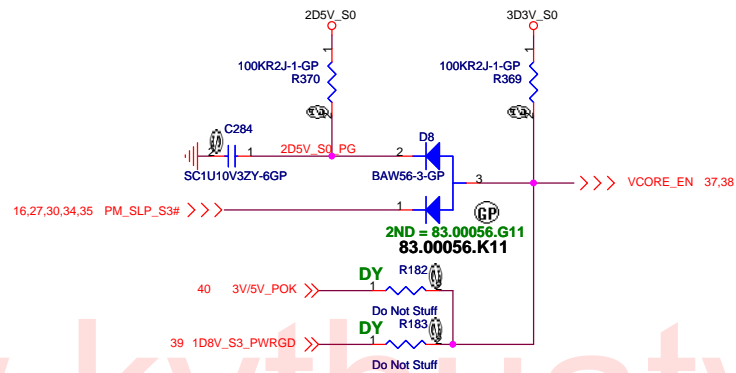


(BOTTOM VIEW)

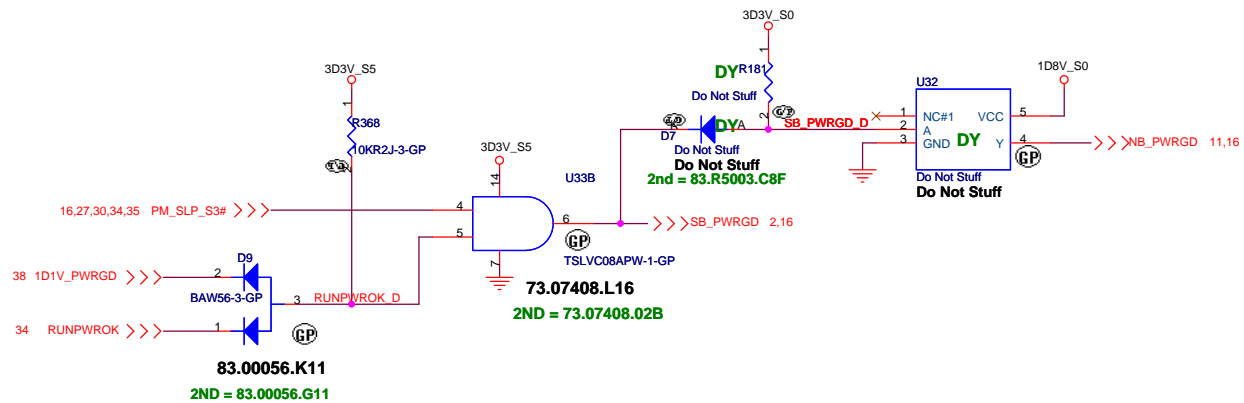
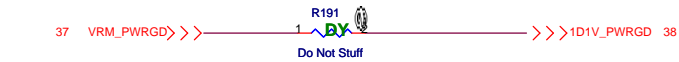
GOLDEN FINGER FOR DEBUG BOARD

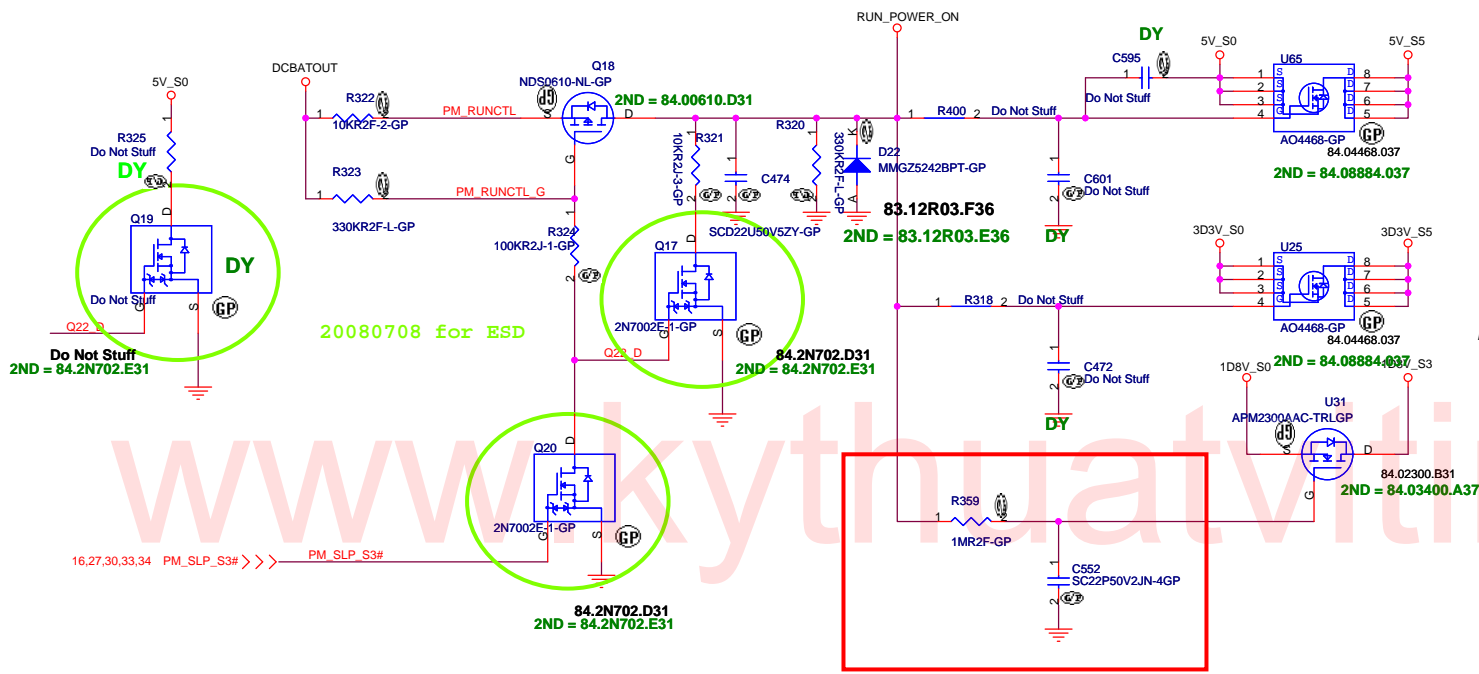


SB



P/H @ 1D8V_S3 PAGE





20080708 for ESD

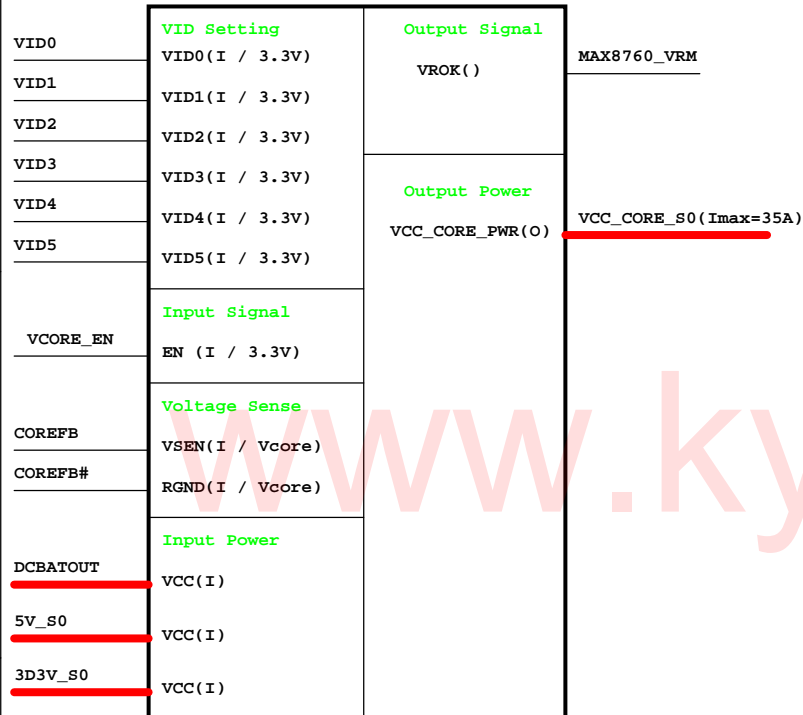
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Run Power

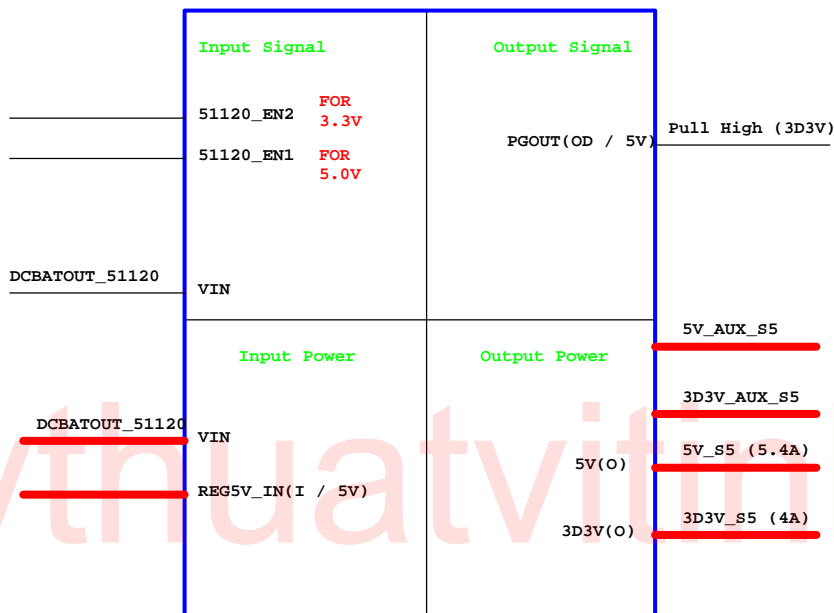
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Title PWR CTL LOGIC / PWR PLANE			
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CPU_CORE
ISL6264CRZ



TI TPS51120
3D3V/5V



2D5V_S0



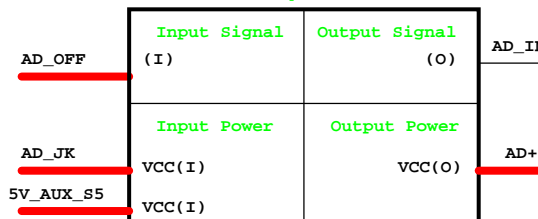
APL5913

1D8V_S5

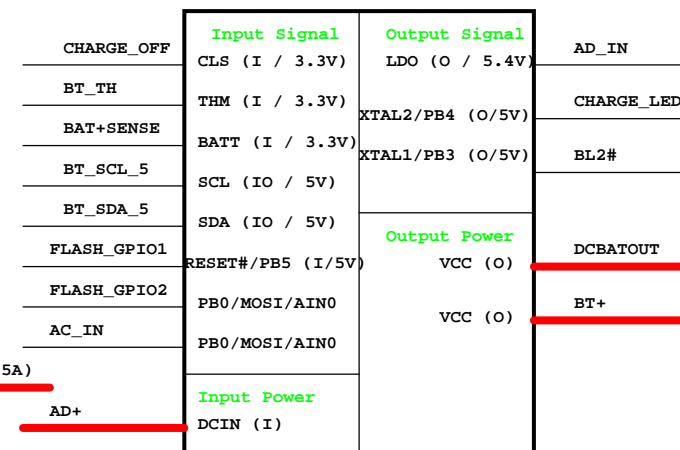


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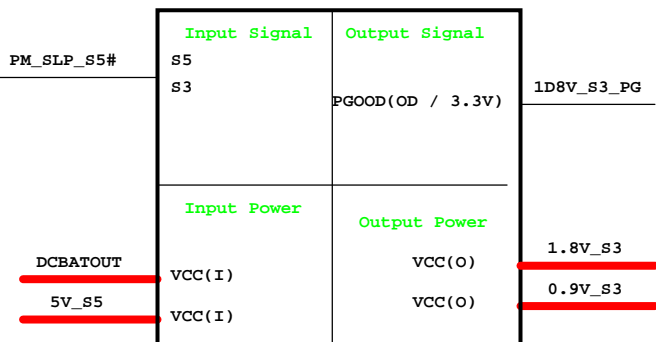
Adapter



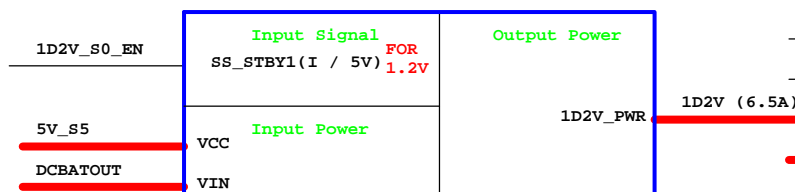
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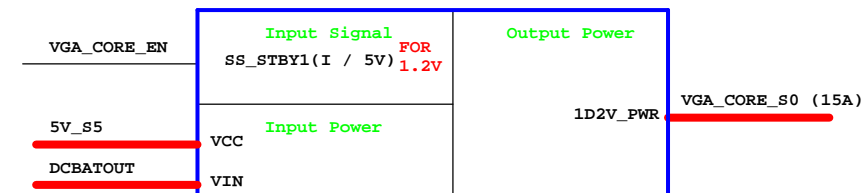
TI TPS51116
1.8V / 0.9V



ISL6268_1D2V



ISL6268_VGA_CORE



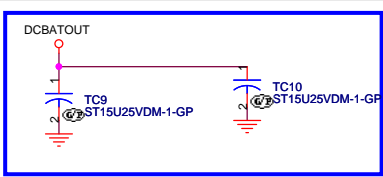
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Title: **Power Block Diagram**

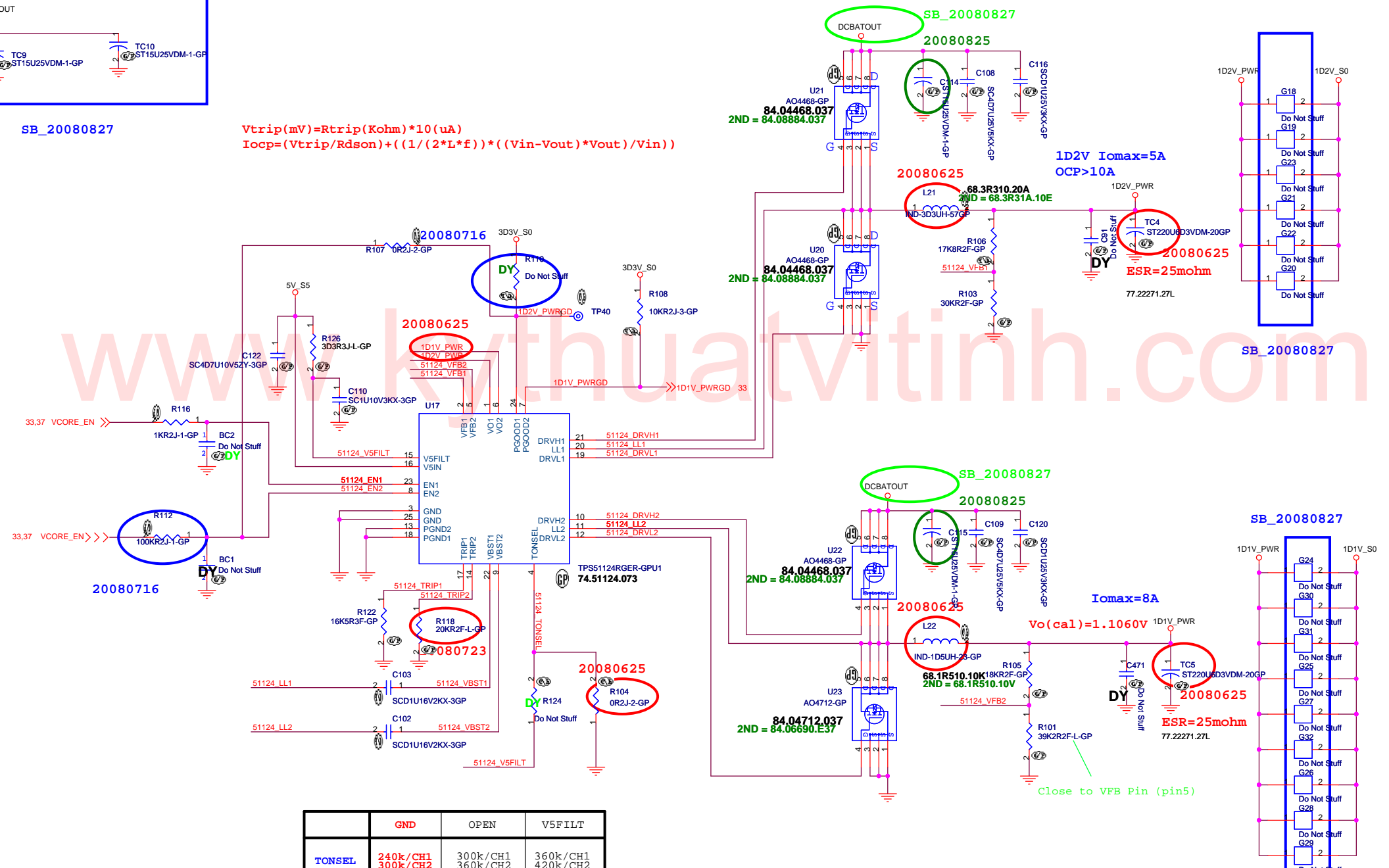
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$V_{trip}(mV) = R_{trip}(Kohm) * 10(uA)$
 $I_{ocp} = (V_{trip}/R_{dson}) + ((1/(2*L*F)) * ((V_{in}-V_{out}) * V_{out}) / V_{in})$



	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

$V_{out} = 0.758V * (R1+R2)/R2$ --> PWM mode
 $V_{out} = 0.764V * (R1+R2)/R2$ --> Skip Mode

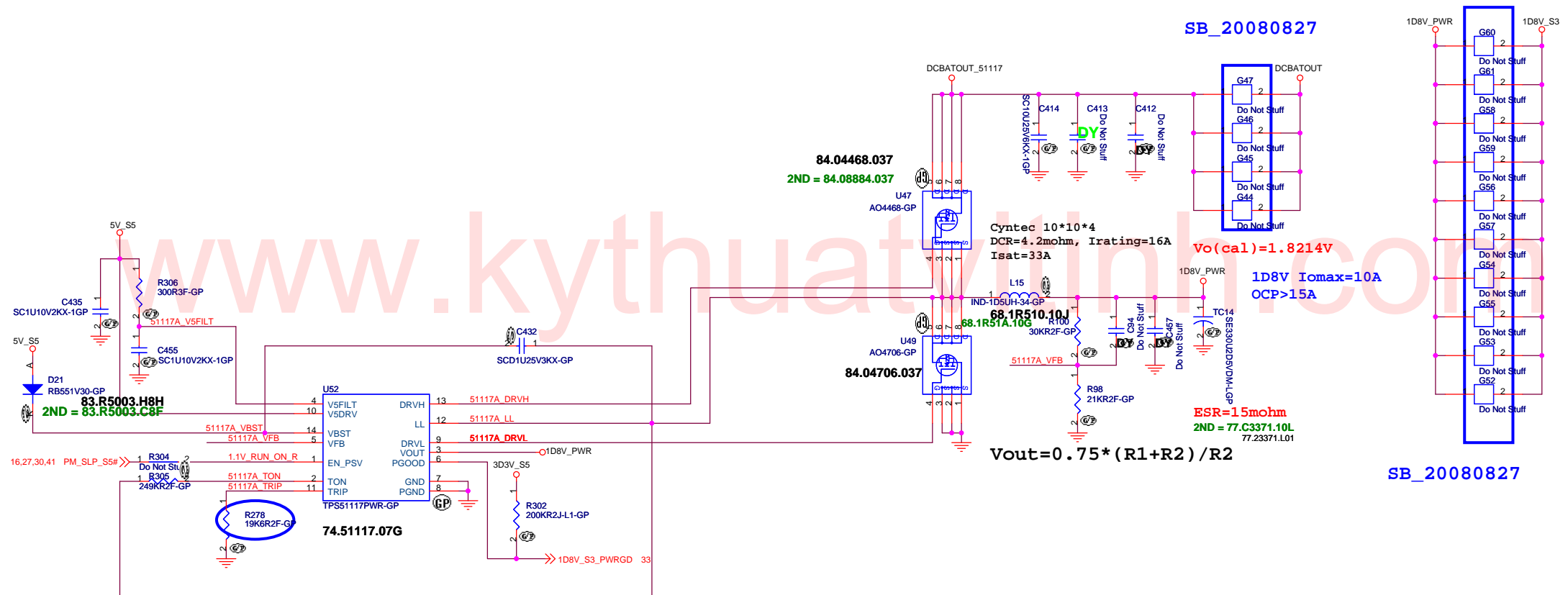
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Title: **TPS51124 1D1V 1D2V**

Size: A3	Document Number: F7-GT	Rev: SB
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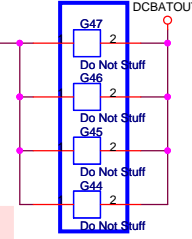
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84.04468.037
2ND = 84.08884.037

Cyntec 10*10*4
DCR=4.2mohm, Irating=16A
Isat=33A



Vo(cal)=1.8214V

1D8V Iomax=10A
OCP>15A

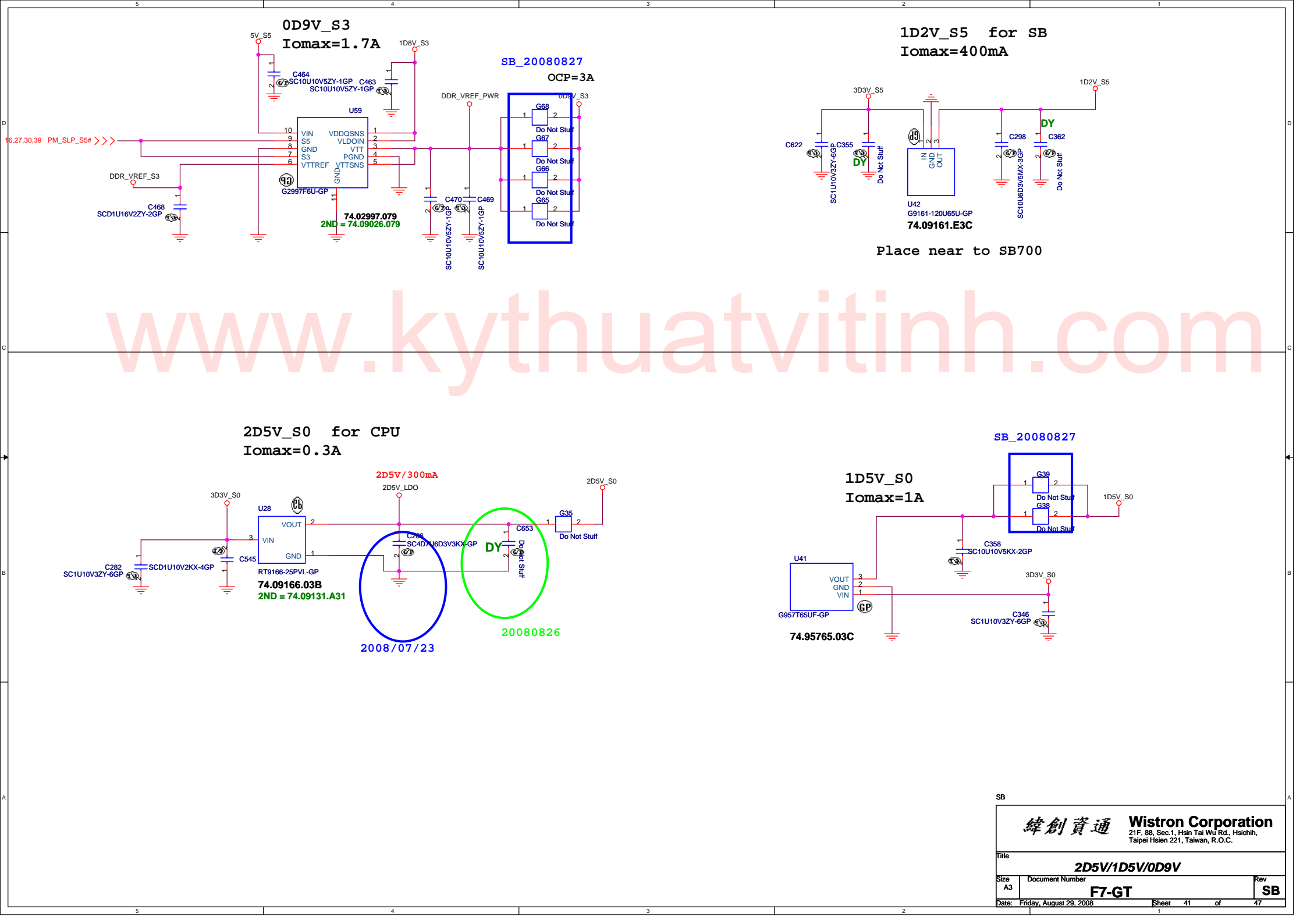
84.04706.037

ESR=1.5mohm
2ND = 77.C3371.10L
77.23371.L01

$$V_{out} = 0.75 * (R1 + R2) / R2$$

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0D9V_S3
Iomax=1.7A

SB_20080827
OCP=3A

1D2V_S5 for SB
Iomax=400mA

2D5V_S0 for CPU
Iomax=0.3A

SB_20080827

1D5V_S0
Iomax=1A

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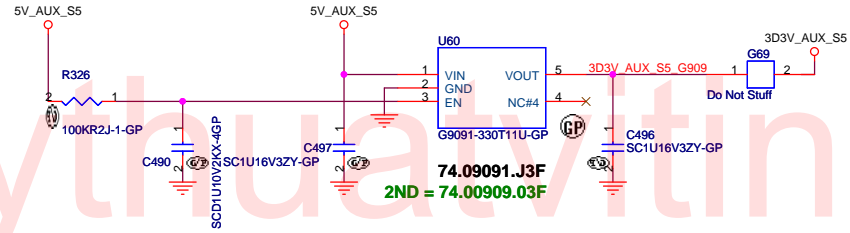
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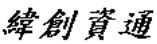
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **2D5V/1D5V/0D9V**

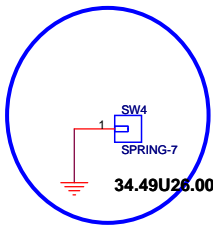
Size: A3	Document Number: F7-GT	Rev: SB
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Aux Power 3D3V_AUX_S5

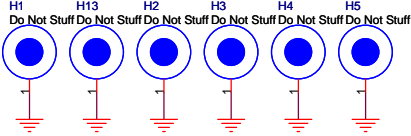


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Title	
3D3V AUX	
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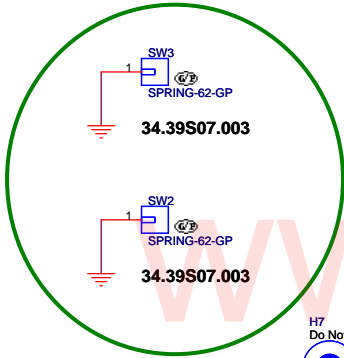
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34.49U26.001

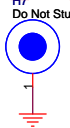
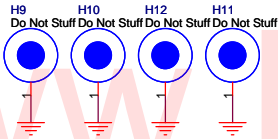
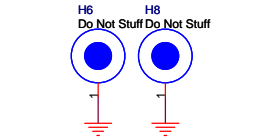


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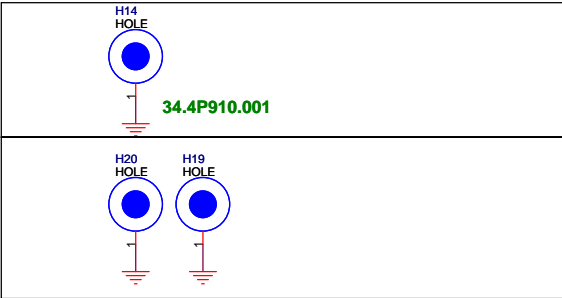
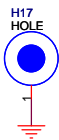
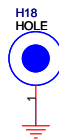
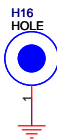
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34.39S07.003



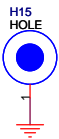
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34.41Q08.011 34.41Q08.011



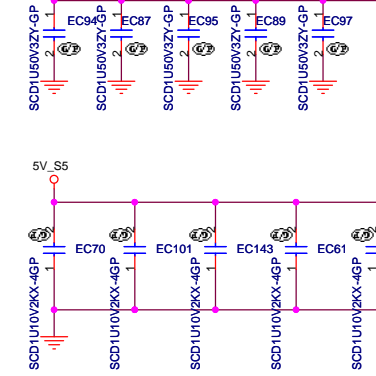
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34.4G502.011 34.4G502.011

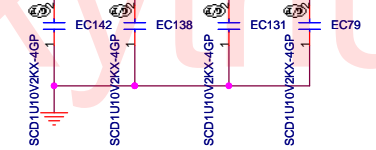


34.41Q08.011

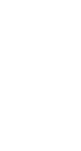
DCBATOUT



5V_S5



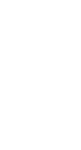
CCD_PWR



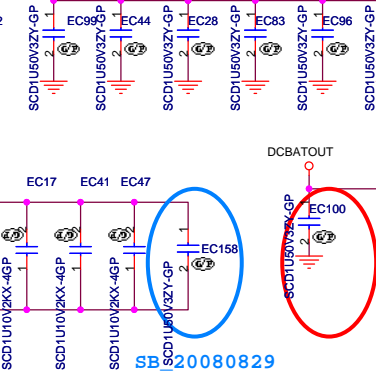
1D2V_S0



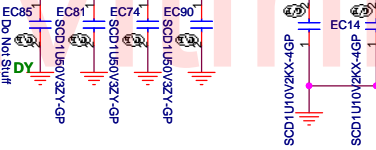
3D3V_S0



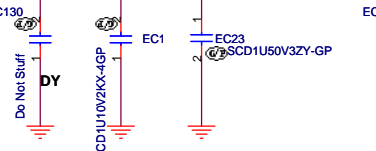
DCBATOUT



5V_S0



DOCK_AD+



3D3V_LAN_S5



3D3V_CLK_VDD



5V_CRT_S0



AD+

1D8V_S3

DOCK_AD


20080702

SB_20080828

SB_20080829

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CCD Test Point



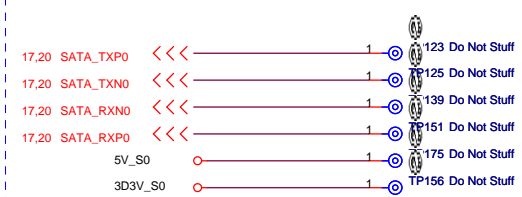
RTC1 CN Test Point



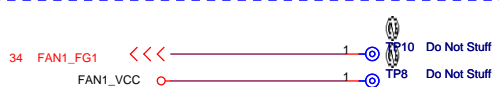
ODD1 Conn. Test Point



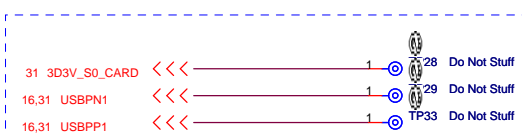
HDD Conn. Test Point



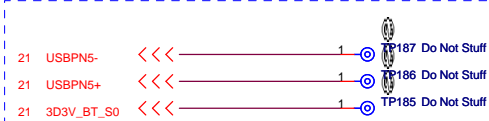
FAN1 Conn. Test Point



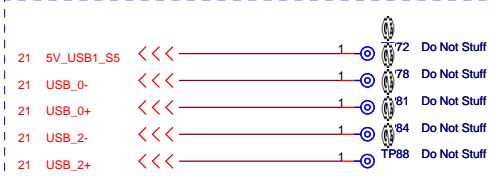
CARD1 Conn. Test Point



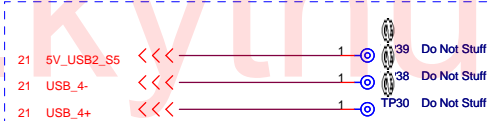
BT Conn. Test Point



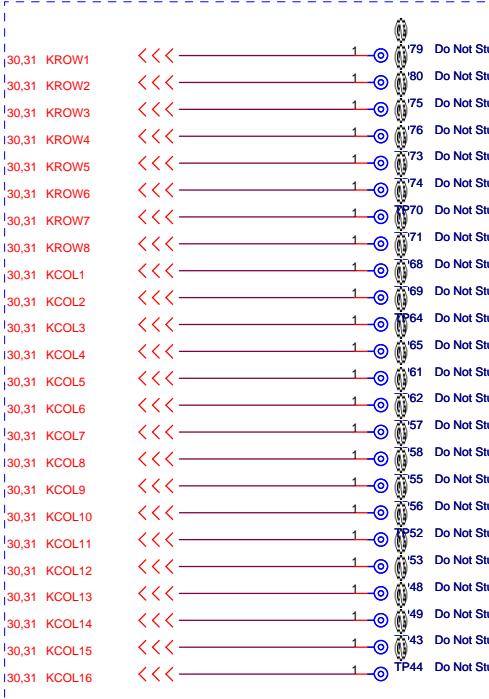
USB Conn2. Test Point



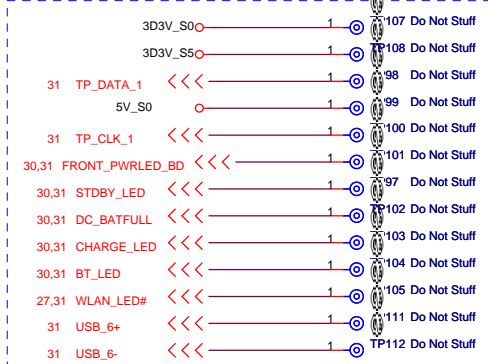
USB Conn1. Test Point



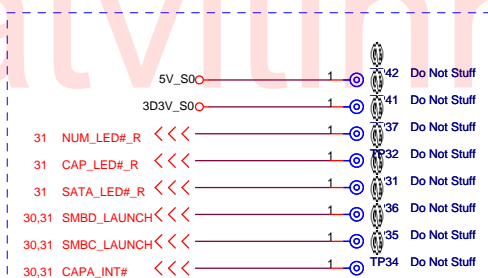
KB Conn1. Test Point



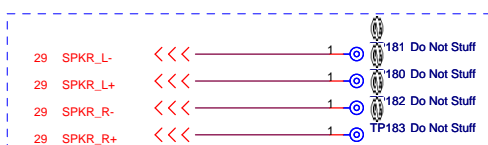
TPAD1 Conn. Test Point



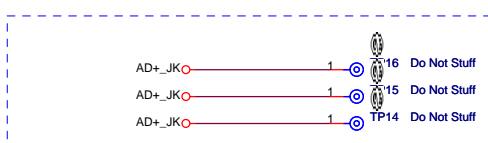
SWITCH Conn. Test Point



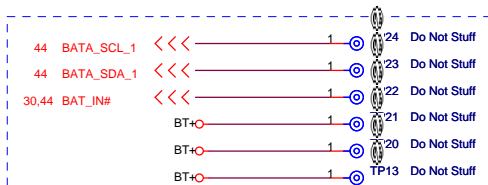
SPKR1 Conn. Test Point



DC1 Conn. Test Point



BAT1 Conn. Test Point



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