

# Compal Confidential

## HBL50 Schematics Document

**Intel Yonah Processor with 945GM/945PM + DDRII + ICH7M  
(With nVIDIA G73M/72MV)**

**2005-11-08**

**REV: 0.3**

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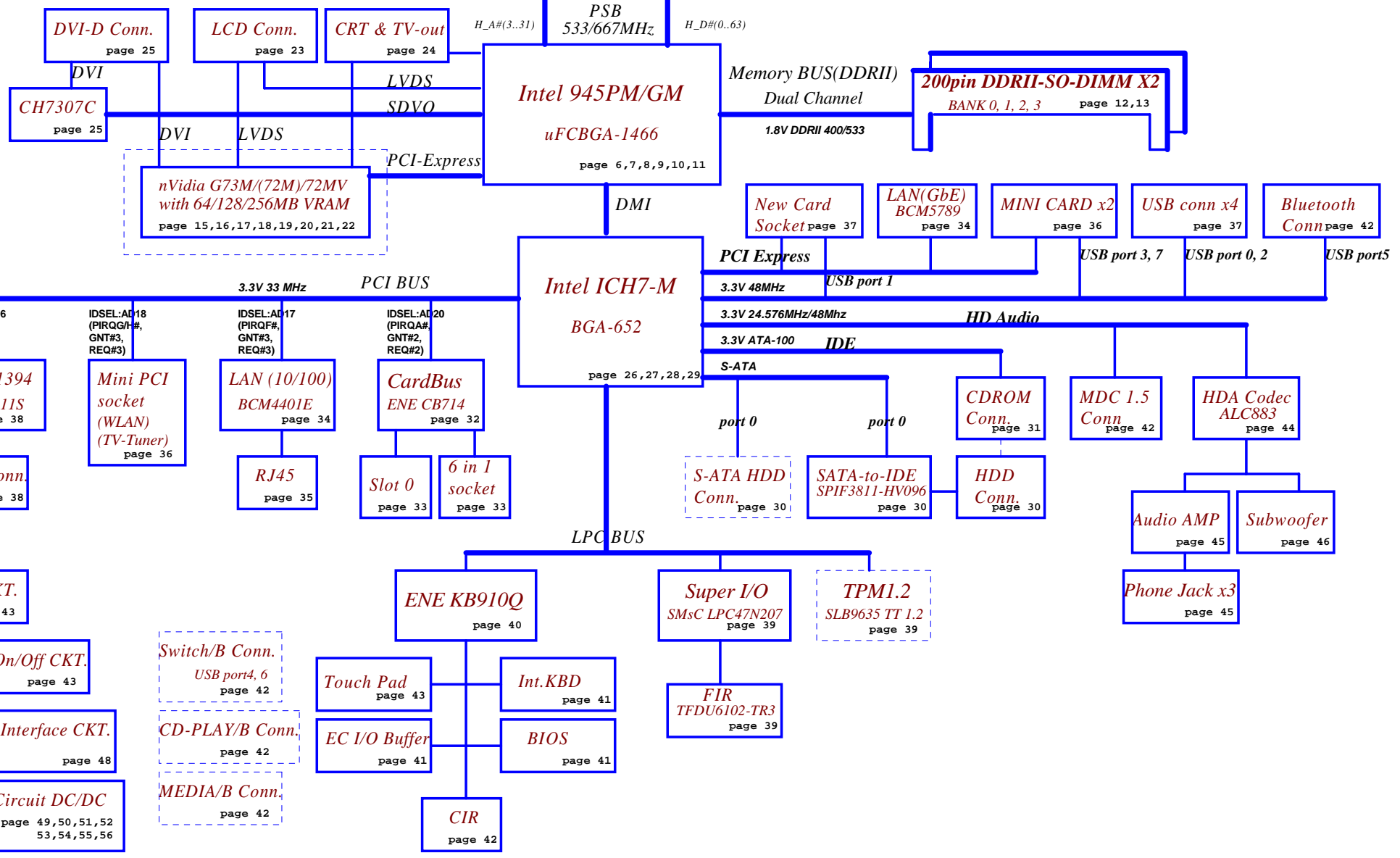
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File Name : LA-2921

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## Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	NA	NA	NA
B+	AC or battery power rail for power circuit.	NA	NA	NA
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

## External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus(SD)	AD20	2	PIRQA/PIRQB
1394	AD16	0	PIRQE
LAN(10/100)	AD17	3	PIRQF
Mini-PCI(WLAN/TV-Tuner)	AD18	1	PIRQG/PORQH

## EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	Fintek F75383M	1001 100X b
EEPROM(24C16/02)	1010 000X b		
GMT G781-1	1001 101X b		

## EC SM Bus2 address

## ICH7M SM Bus address

Device	Address
Clock Generator (ICS9LPRS325AKLFT_MLF72)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

## Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

## BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

## SKU ID Table

SKU ID	SKU
0	PM
1	GM
2	
3	
4	
5	
6	
7	

## BTO Option Table

BTO Item	BOM Structure
VGA	PM@ + VGA@
UMA	GM@
UMA's DVI	7307@
LAN(10/100)	4401@
LAN(GIGA)	5789@
MINI CARD1	MINI1@
MINI CARD2	MINI2@
SATA-to-IDE	3811@
PATA	PATA@
GRAPEVINE	GRA@
G72MV Only	G72@
G73 Only	G73@
VRAM	X76@
VRAM 64M	64@
VRAM 128M	64@+128@
VRAM 256M	64@+128@+256@
MEDIA/B	MEDIA@
CIR	CIR@
FIR	FIR@
GENEVA	GEN@
LCM	LCM@
Sub-woofer	SUB@

5789&5787	8789@
4401&5789	0189@
VP1020	VP1020@
INTERNAL MIC	INTMIC@
1394	1394@
SATA HDD	SATA@

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6 H\_A# [3..31] H\_A# [3..31]

JP18A

**YONAH**

H\_A#3 J4 A3#  
 H\_A#4 L4 A4#  
 H\_A#5 M3 A5#  
 H\_A#6 K5 A6#  
 H\_A#7 M1 A7#  
 H\_A#8 N2 A8#  
 H\_A#9 J1 A9#  
 H\_A#10 N3 A10#  
 H\_A#11 P5 A11#  
 H\_A#12 P2 A12#  
 H\_A#13 L1 A13#  
 H\_A#14 P4 A14#  
 H\_A#15 P1 A15#  
 H\_A#16 R1 A16#  
 H\_A#17 Y2 A17#  
 H\_A#18 U5 A18#  
 H\_A#19 K3 A19#  
 H\_A#20 W6 A20#  
 H\_A#21 U4 A21#  
 H\_A#22 Y5 A22#  
 H\_A#23 U2 A23#  
 H\_A#24 R4 A24#  
 H\_A#25 T5 A25#  
 H\_A#26 U3 A26#  
 H\_A#27 W5 A27#  
 H\_A#28 Y4 A28#  
 H\_A#29 Y4 A29#  
 H\_A#30 W2 A30#  
 H\_A#31 Y1 A31#

ADDR GROUP DATA GROUP

D0# E22 H\_D#0  
 D1# E24 H\_D#1  
 D2# E26 H\_D#2  
 D3# H22 H\_D#3  
 D4# E23 H\_D#4  
 D5# G25 H\_D#5  
 D6# E25 H\_D#6  
 D7# E27 H\_D#7  
 D8# K24 H\_D#8  
 D9# G24 H\_D#9  
 D10# J24 H\_D#10  
 D11# J23 H\_D#11  
 D12# H26 H\_D#12  
 D13# E28 H\_D#13  
 D14# K22 H\_D#14  
 D15# H22 H\_D#15  
 D16# K25 H\_D#16  
 D17# P26 H\_D#17  
 D18# R23 H\_D#18  
 D19# R25 H\_D#19  
 D20# L22 H\_D#20  
 D21# M23 H\_D#21  
 D22# L23 H\_D#22  
 D23# P25 H\_D#23  
 D24# P22 H\_D#24  
 D25# P23 H\_D#25  
 D26# P23 H\_D#26  
 D27# T24 H\_D#27  
 D28# R24 H\_D#28  
 D29# L26 H\_D#29  
 D30# T25 H\_D#30  
 D31# N24 H\_D#31  
 D32# AA23 H\_D#32  
 D33# AB24 H\_D#33  
 D34# V24 H\_D#34  
 D35# V26 H\_D#35  
 D36# U25 H\_D#36  
 D37# U23 H\_D#37  
 D38# U25 H\_D#38  
 D39# U22 H\_D#39  
 D40# AB25 H\_D#40  
 D41# W22 H\_D#41  
 D42# V23 H\_D#42  
 D43# AA26 H\_D#43  
 D44# Y26 H\_D#44  
 D45# Y22 H\_D#45  
 D46# AC26 H\_D#46  
 D47# AA24 H\_D#47  
 D48# AC22 H\_D#48  
 D49# AC23 H\_D#49  
 D50# AB22 H\_D#50  
 D51# AA21 H\_D#51  
 D52# AB21 H\_D#52  
 D53# AC25 H\_D#53  
 D54# AD20 H\_D#54  
 D55# AE22 H\_D#55  
 D56# AE23 H\_D#56  
 D57# AD24 H\_D#57  
 D58# AE21 H\_D#58  
 D59# AD21 H\_D#59  
 D60# AE25 H\_D#60  
 D61# AE25 H\_D#61  
 D62# AE22 H\_D#62  
 D63# AF26 H\_D#63

6 H\_REQ# [0..4] H\_REQ# [0..4]

H\_REQ#0 K3 REQ0#  
 H\_REQ#1 H2 REQ1#  
 H\_REQ#2 K2 REQ2#  
 H\_REQ#3 J3 REQ3#  
 H\_REQ#4 L5 REQ4#

6 H\_ADSTB# [0..1] L2 ADSTB0#  
V4 ADSTB1#

14 CLK\_CPU\_BCLK A22 BCLK0  
14 CLK\_CPU\_BCLK# A21 BCLK1

HOST CLK

6 H\_ADS# H1 ADS#  
 6 H\_BNR# E2 BNR#  
 6 H\_BR# G5 BR#  
 6 H\_BR# F1 BR0#  
 6 H\_DEFER# H5 DEFER#  
 6 H\_DRDY# F2 DRDY#  
 6 H\_HIT# G6 HIT#  
 6 H\_HIT# E4 HITM#  
 6 H\_LOCK# H IERR#  
 6 H\_RESET# H4 LOCK#  
 6 H\_RESET# B1 RESET#

CONTROL

6 H\_RS# [0..2] H\_RS# [0..2]

H\_RS#0 E3 RS0#  
 H\_RS#1 F4 RS1#  
 H\_RS#2 G3 RS2#  
 6 H\_TRDY# G2 TRDY#

T5 PAD ITP\_BPM#0 AD4 BPM0#  
 T3 PAD ITP\_BPM#1 AD3 BPM1#  
 T1 PAD ITP\_BPM#2 AD4 BPM2#  
 T4 PAD ITP\_BPM#3 AD4 BPM3#

28 ITP\_DBRESET# C20 DBR#  
 6 H\_DBSY# E1 DBSY#  
 27 H\_DPSLP# E5 DPSTP#  
 27,56 H\_DPRSTP# E5 DPRSTP#  
 6 H\_DPWR# D24 DPWR#  
 T2 PAD ITP\_BPM#4 AC2 PRDY#  
 ITP\_BPM#5 AC1 PREQ#  
 H\_PROCHOT# D21 PROCHOT#

MISC

27 H\_PWRGOOD D6 PWRGOOD  
 6 H\_CPUSLP# D7 SLP#  
 ITP\_TCK AC5 TCK  
 ITP\_TDI AA6 TDI  
 ITP\_TDO AB3 TDO  
 TEST1 C26 TEST1  
 TEST2 D25 TEST2  
 ITP\_TMS AB5 TMS  
 ITP\_TRST# AB6 TRST#

LEGACY CPU

6,27 H\_THERMTRIP# THERMDA A24 THERMDA  
 THERMDC A25 THERMDC  
 THERMTRIP# C7 THERMTRIP#

THERMAL DIODE

FOX\_P247903-2741-42\_YONAH

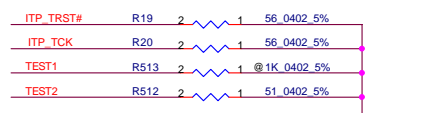
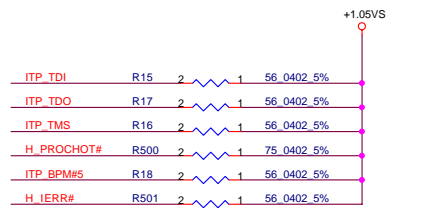
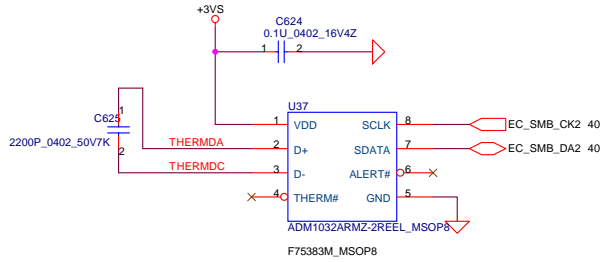
H\_D# [0..63] H\_D# [0..63] 6

DINV0# J26 H\_DINV#0 6  
 DINV1# M26 H\_DINV#1 6  
 DINV2# V23 H\_DINV#2 6  
 DINV3# AC20 H\_DINV#3 6

DSTBN0# H23 H\_DSTBN#0 6  
 DSTBN1# M24 H\_DSTBN#1 6  
 DSTBN2# V24 H\_DSTBN#2 6  
 DSTBN3# AD23 H\_DSTBN#3 6  
 DSTBP0# G22 H\_DSTBP#0 6  
 DSTBP1# N25 H\_DSTBP#1 6  
 DSTBP2# Y25 H\_DSTBP#2 6  
 DSTBP3# AE24 H\_DSTBP#3 6

A20M# A6 H\_A20M# 27  
 FERR# A5 H\_FERR# 27  
 IGNNE# C4 H\_IGNNE# 27  
 INT# B3 H\_INT# 27  
 LINT0 C6 H\_INTR# 27  
 LINT1 B4 H\_NMI# 27

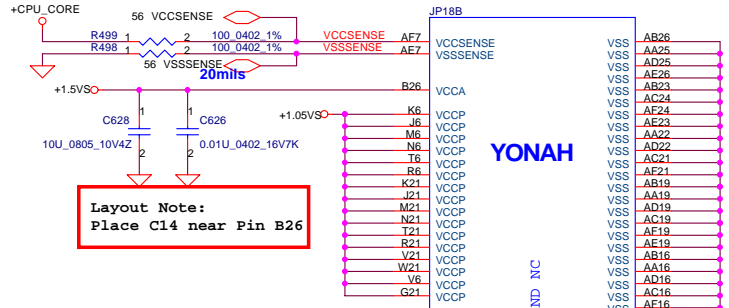
STPCLK# D5 H\_STPCLK# 27  
 SM# A3 H\_SM# 27



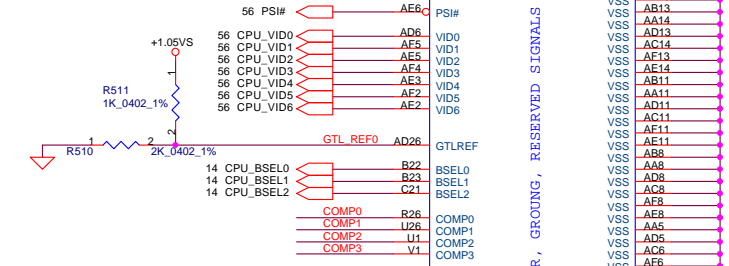
**Layout Note:**  
 THERMDA & THERMDC Trace / Space = 10 / 10 mil

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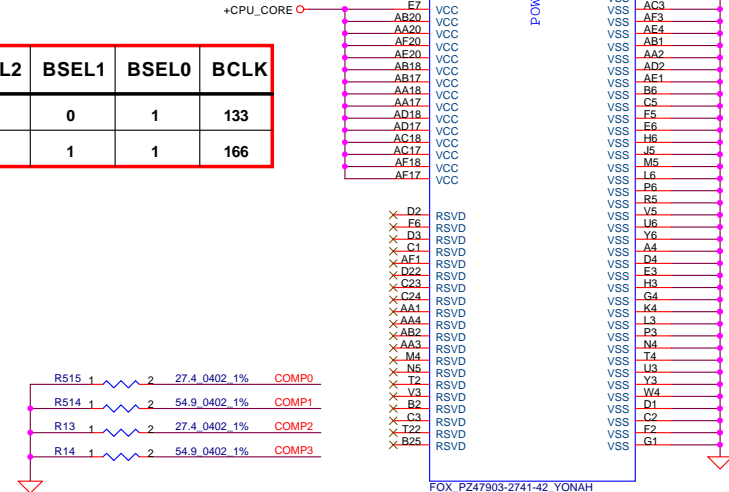
**Layout Note:**  
Route VCCSENSE and VSSSENSE traces at 27.4ohms with 50 mil spacing.  
Place PU and PD within 1 inch of CPU.



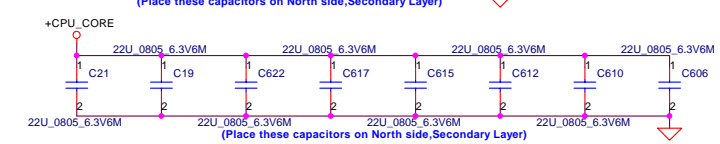
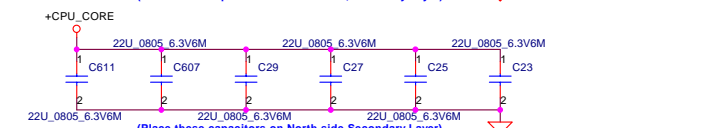
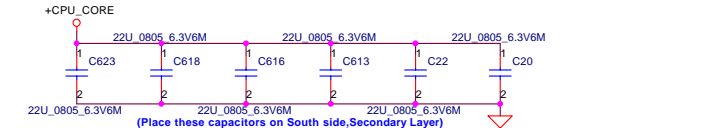
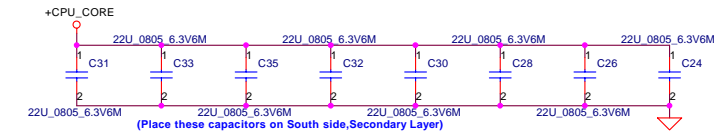
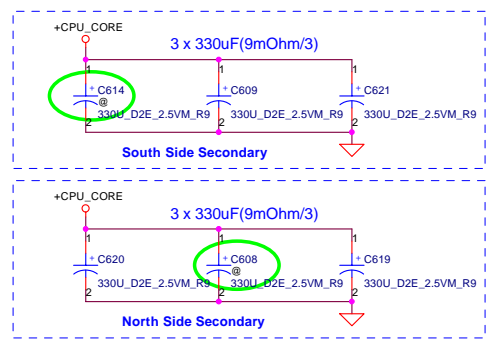
**Layout Note:**  
Place C14 near Pin B26



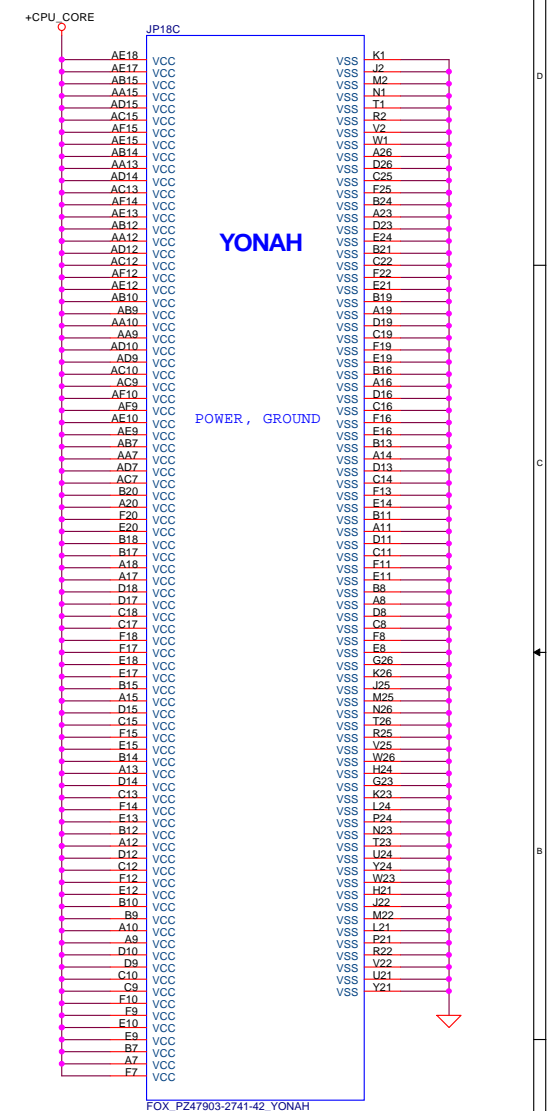
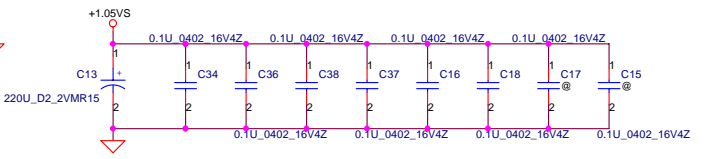
BSEL2	BSEL1	BSEL0	BCLK
0	0	1	133
0	1	1	166

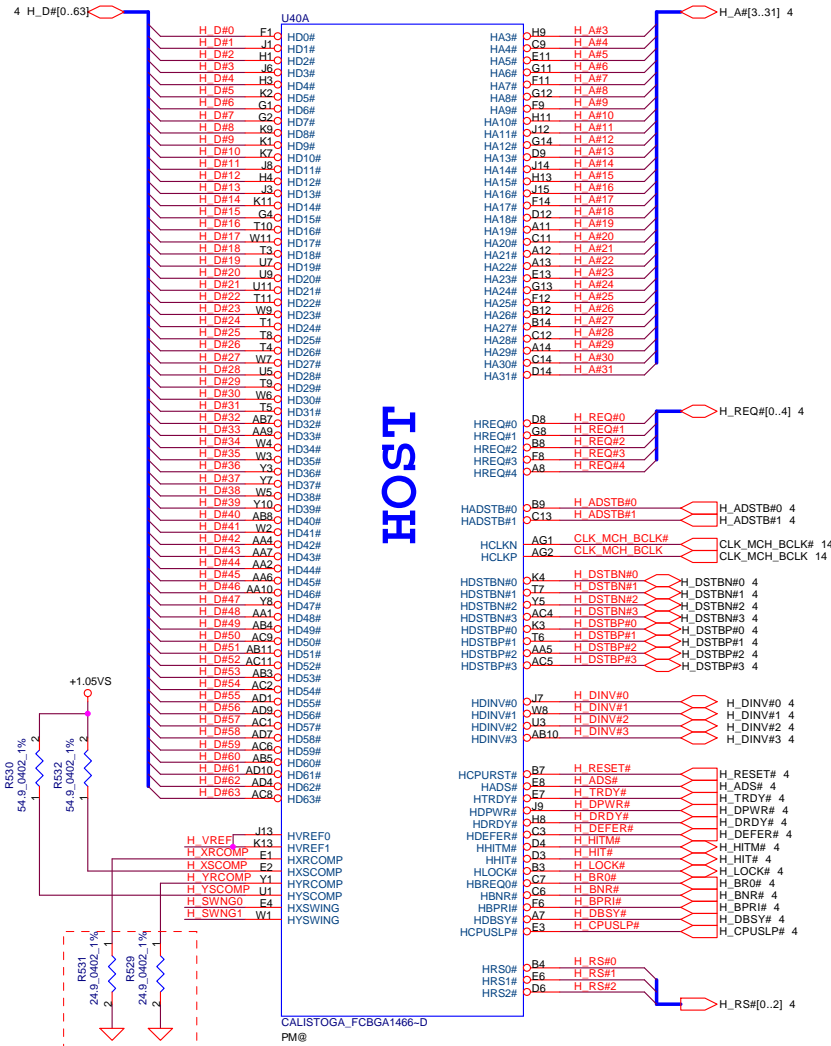


**TRACE CLOSELY CPU < 0.5'**  
COMP0, COMP2 layout : Width 18mils and Space 25mils (27.4ohms)  
COMP1, COMP3 layout : Space 25mils (55ohms)

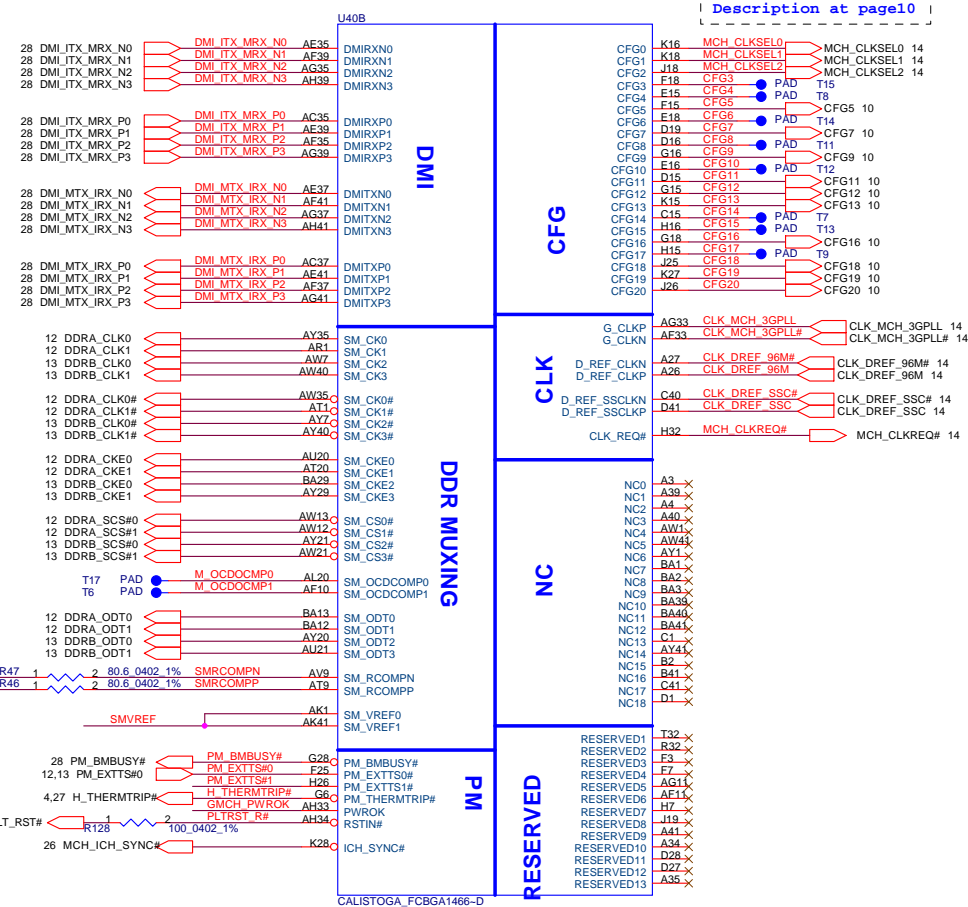
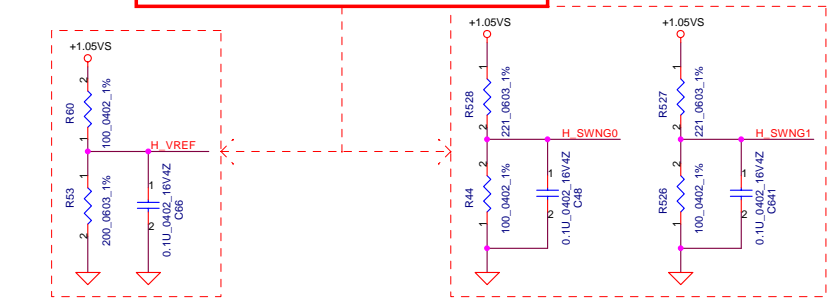


+CPU-CORE Decoupling	C,uF	ESR, mohm	ESL,nH
SPCAP, Polymer	6X330uF	9m ohm/6	1.8nH/6
MLCC 0805 X5R	32X22uF	3m ohm/32	0.6nH/32

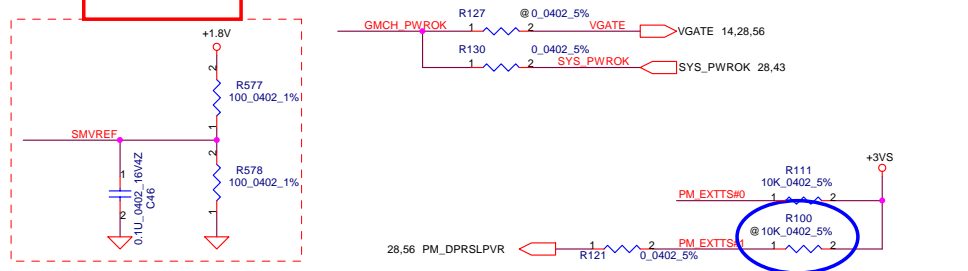




**Layout Note:**  
 H\_XRCOMP / H\_YRCOMP / H\_VREF / H\_SWNG0 /  
 H\_SWNG1 trace width and spacing is 10/20.

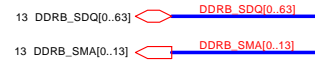
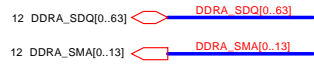


**Layout Note:**  
 SMVREF trace  
 width and spacing  
 is 20/20.

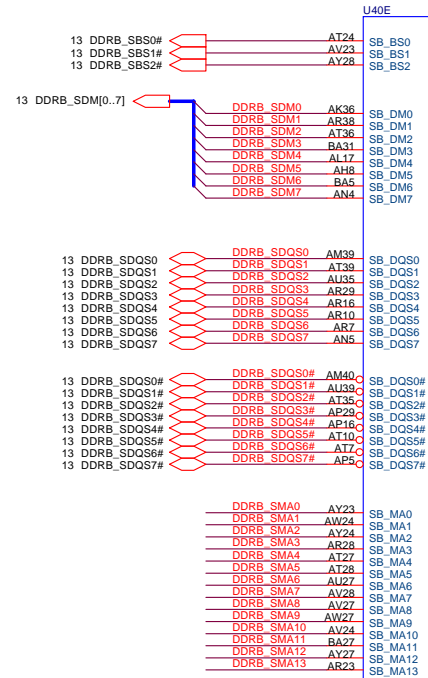
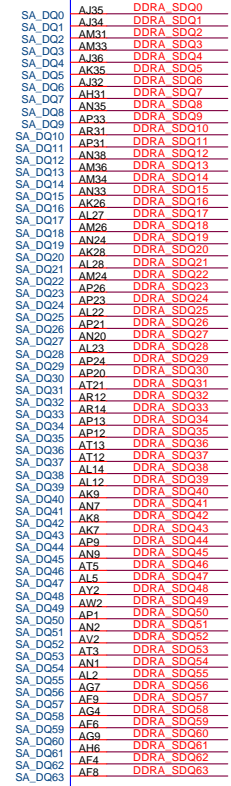


2005/09/20

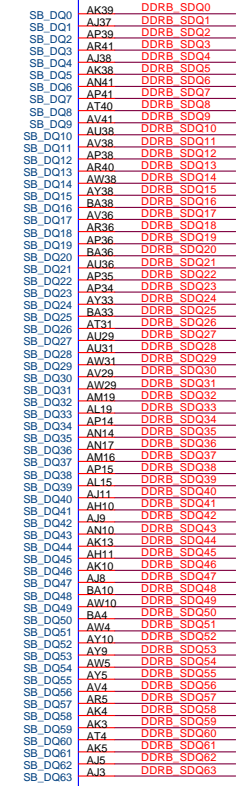
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DDR SYS MEMORY A



DDR SYS MEMORY B



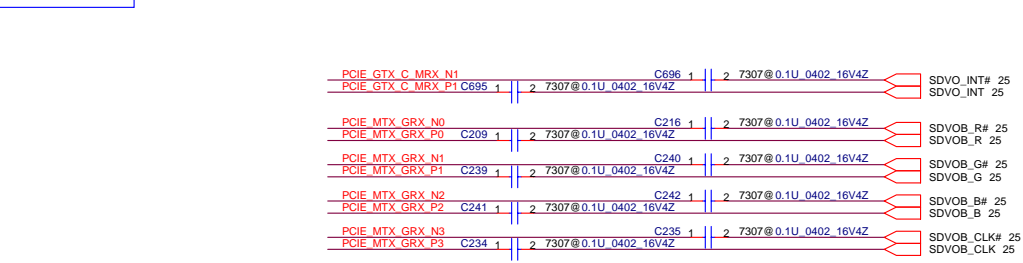
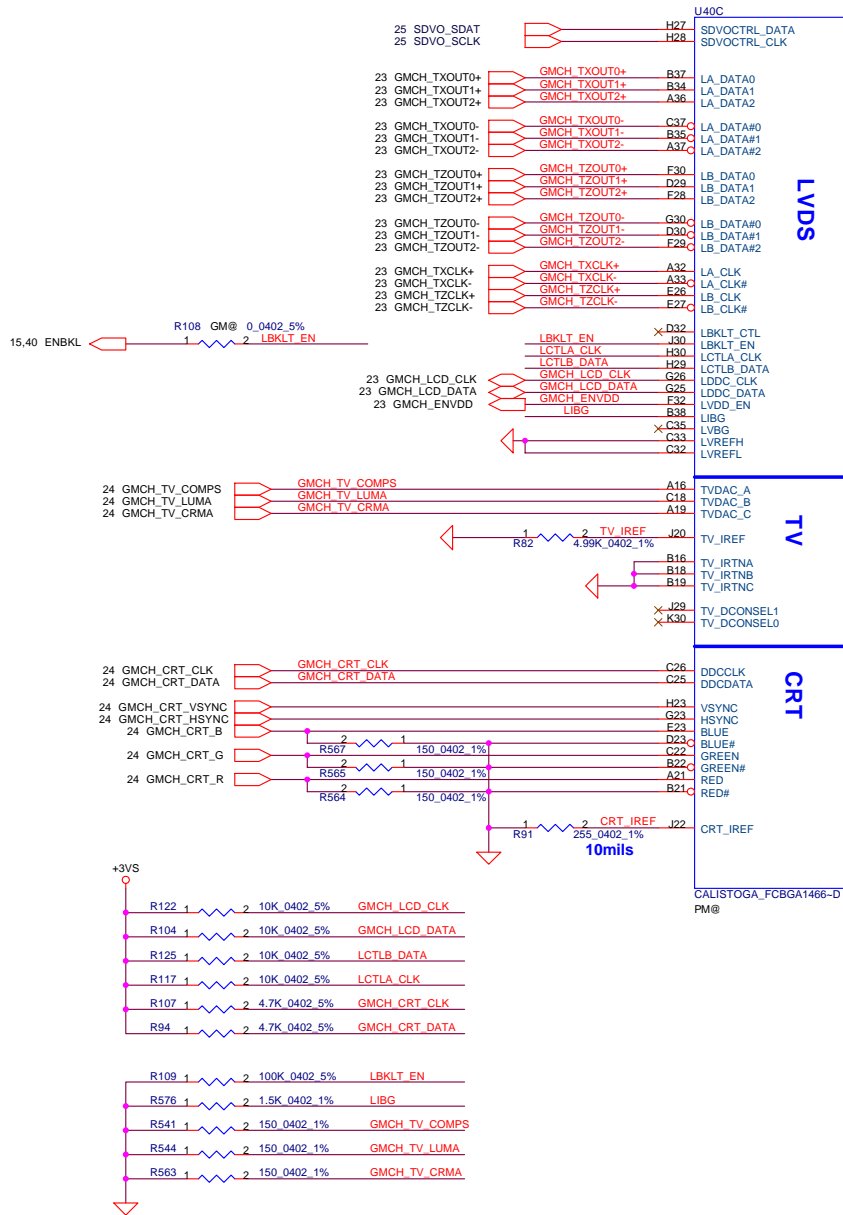
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CALISTOGA\_FCBGA1466-D  
PM@

CALISTOGA\_FCBGA1466-D  
PM@

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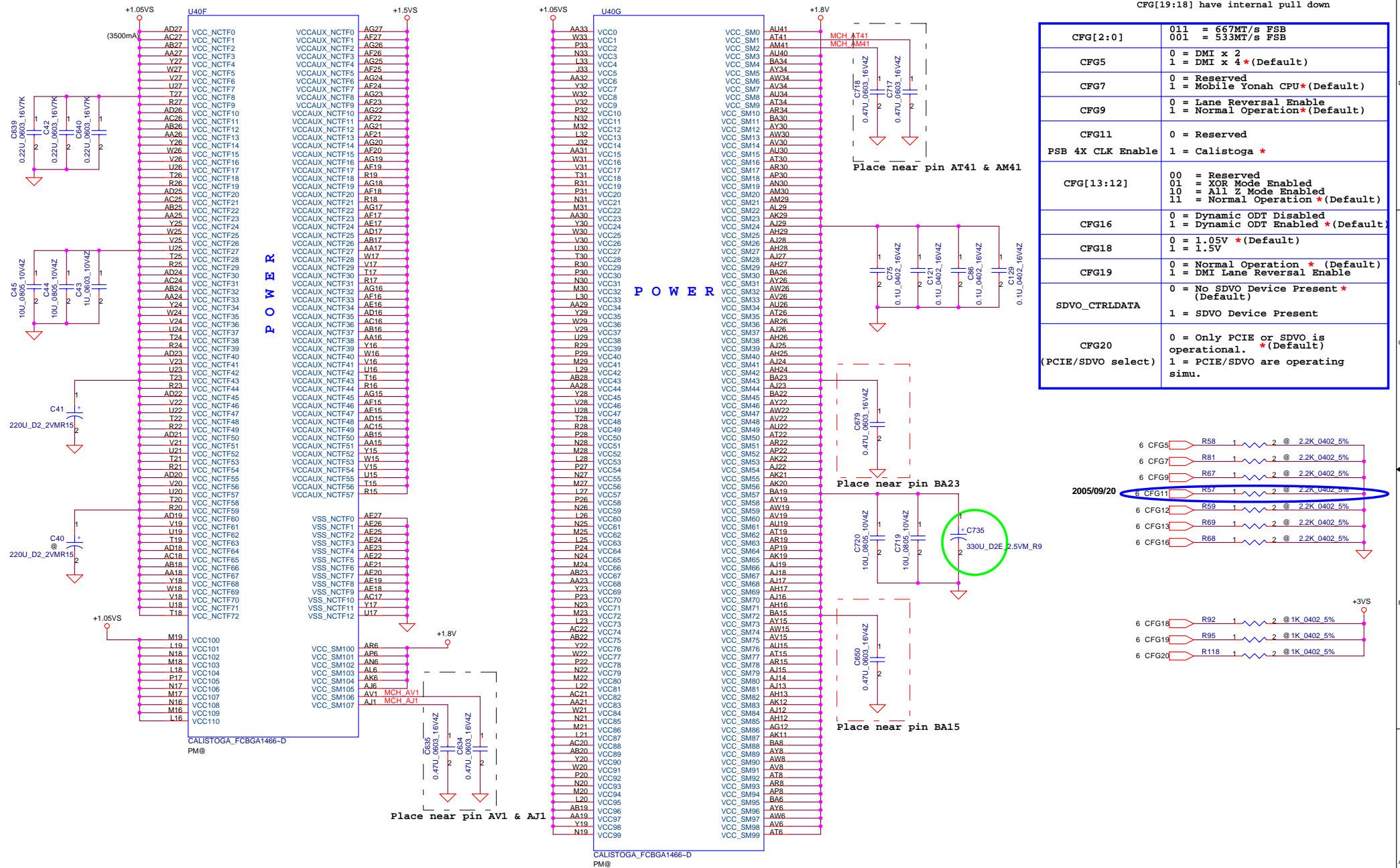




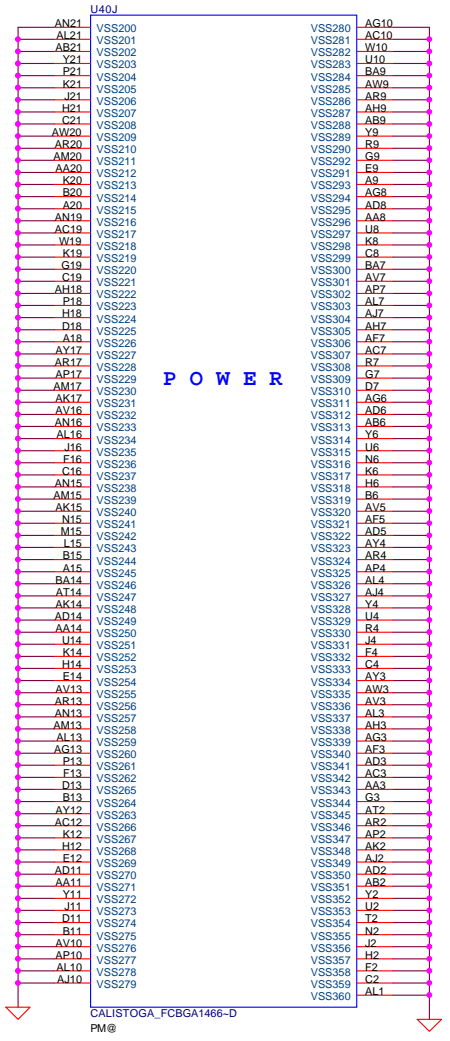
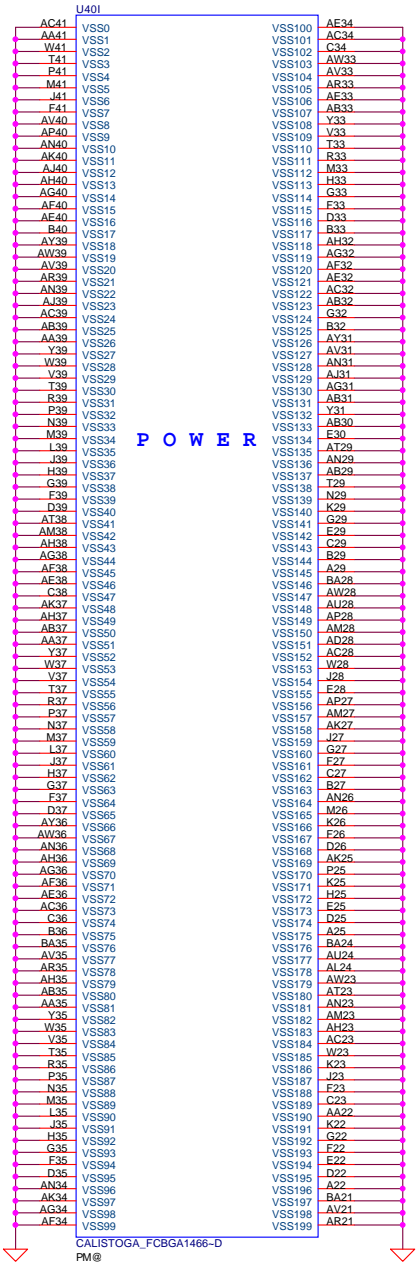
# Strap Pin Table

CFG[3:17] have internal pull up  
CFG[19:18] have internal pull down

CFG[2:0]	011 = 667MT/s FSB 001 = 533MT/s FSB
CFG5	0 = DMI x 2 1 = DMI x 4 *(Default)
CFG7	0 = Reserved 1 = Mobile Yonah CPU*(Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation*(Default)
CFG11	0 = Reserved
PSB 4X CLK Enable	1 = Calistoga *
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation *(Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled *(Default)
CFG18	0 = 1.05V *(Default) 1 = 1.5V
CFG19	0 = Normal Operation *(Default) 1 = DMI Lane Reversal Enable
SDVO_CTRLDATA	0 = No SDVO Device Present *(Default) 1 = SDVO Device Present
CFG20 (PCIE/SDVO select)	0 = Only PCIE or SDVO is operational. *(Default) 1 = PCIE/SDVO are operating simu.



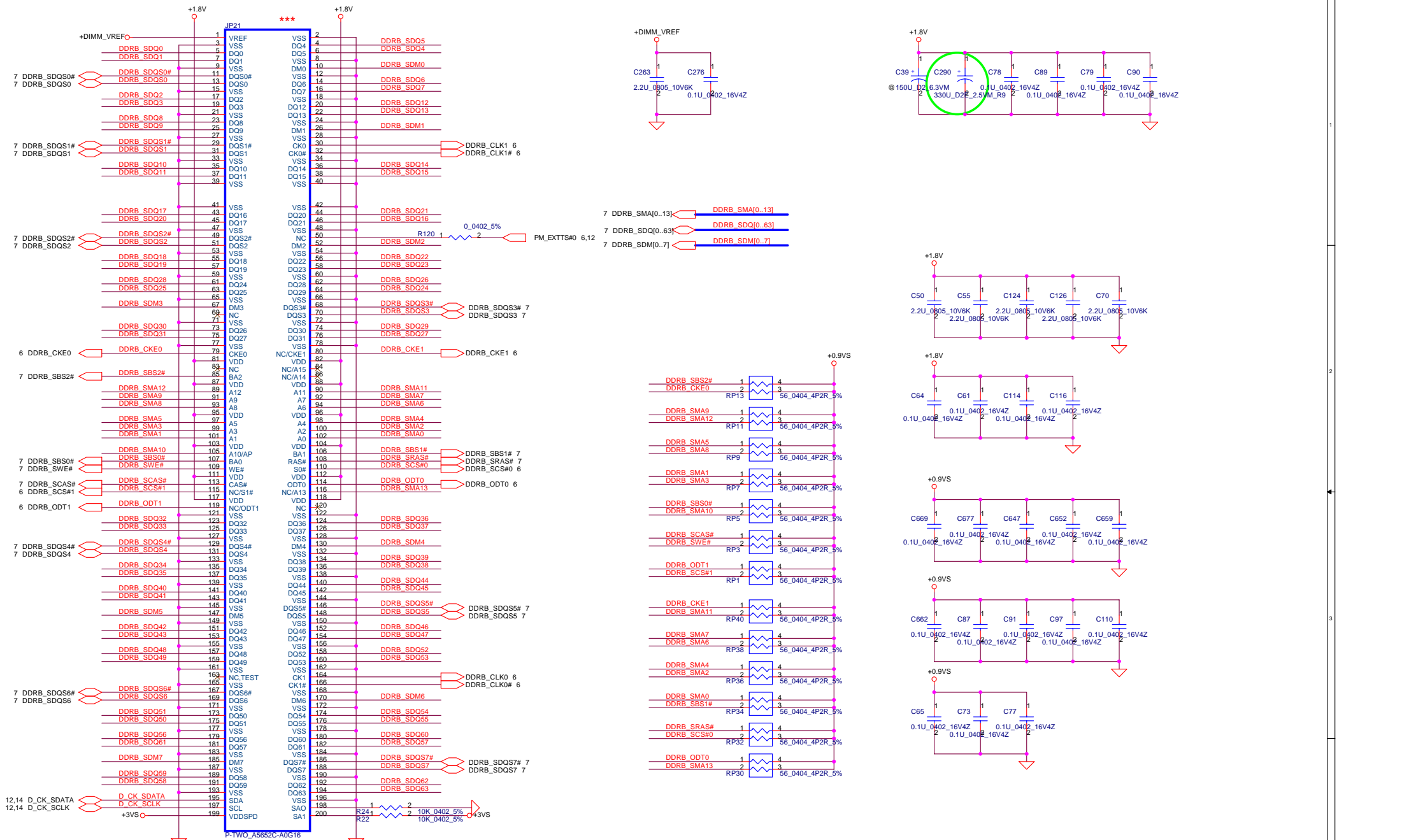
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POWER

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				Calistoga (6/6)
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**DIMM1 STD H:5.2mm (BOT)**

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**Compal Electronics, Inc.**

**DDR II-SODIMM1**

**HBL50 LA-2921P**

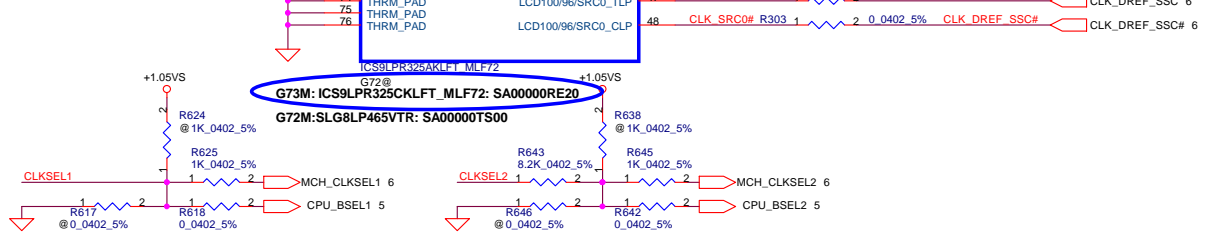
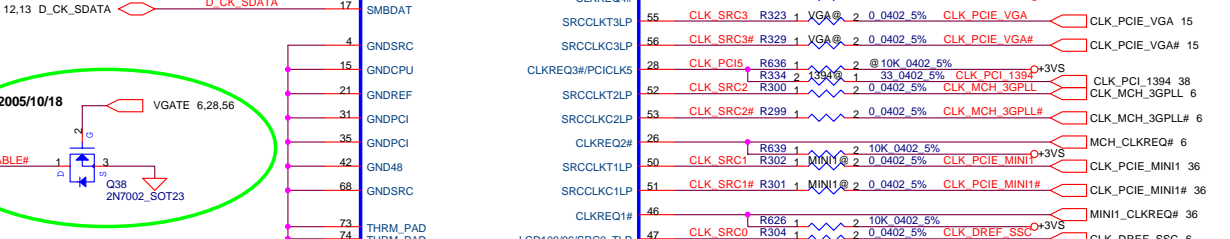
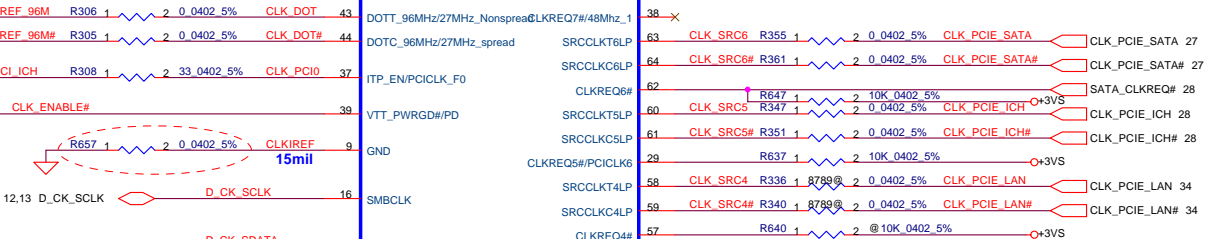
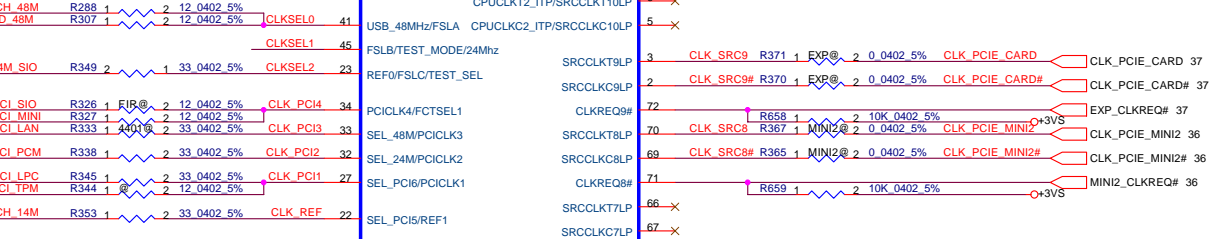
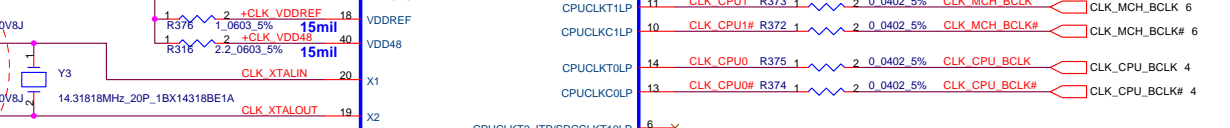
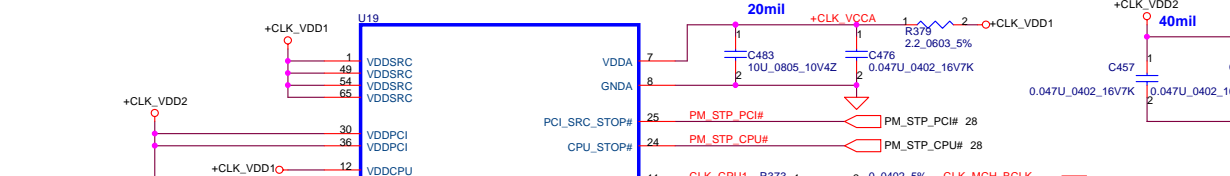
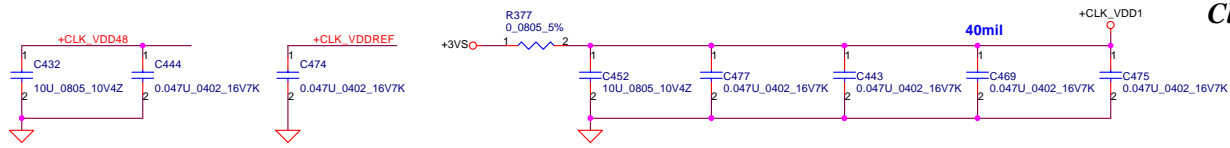
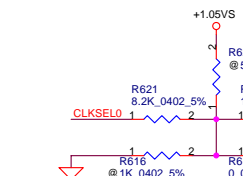
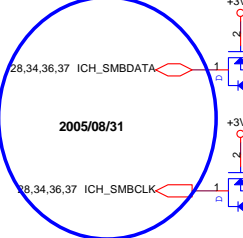
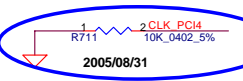
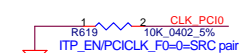
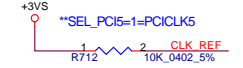
FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	0	1	133	100	33.3
0	1	1	166	100	33.3

Table : ICS9LPR325

	0	1
**SEL_PCI5/REF1	CLKREQ3#	33.3MHz PCICLK5
**SEL_PCI6/PCICLK1	CLKREQ5#	33.3MHz PCICLK6
**SEL_24M/PCICLK2	TESTMODE	24MHz Output
**SEL_48M/PCICLK3	CLKREQ7#	48MHz_1 Output
ITP_EN/PCICLK_F0	SRC pair	CPU_ITP pair

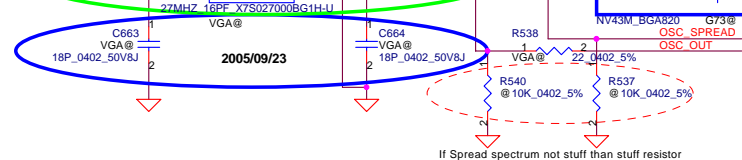
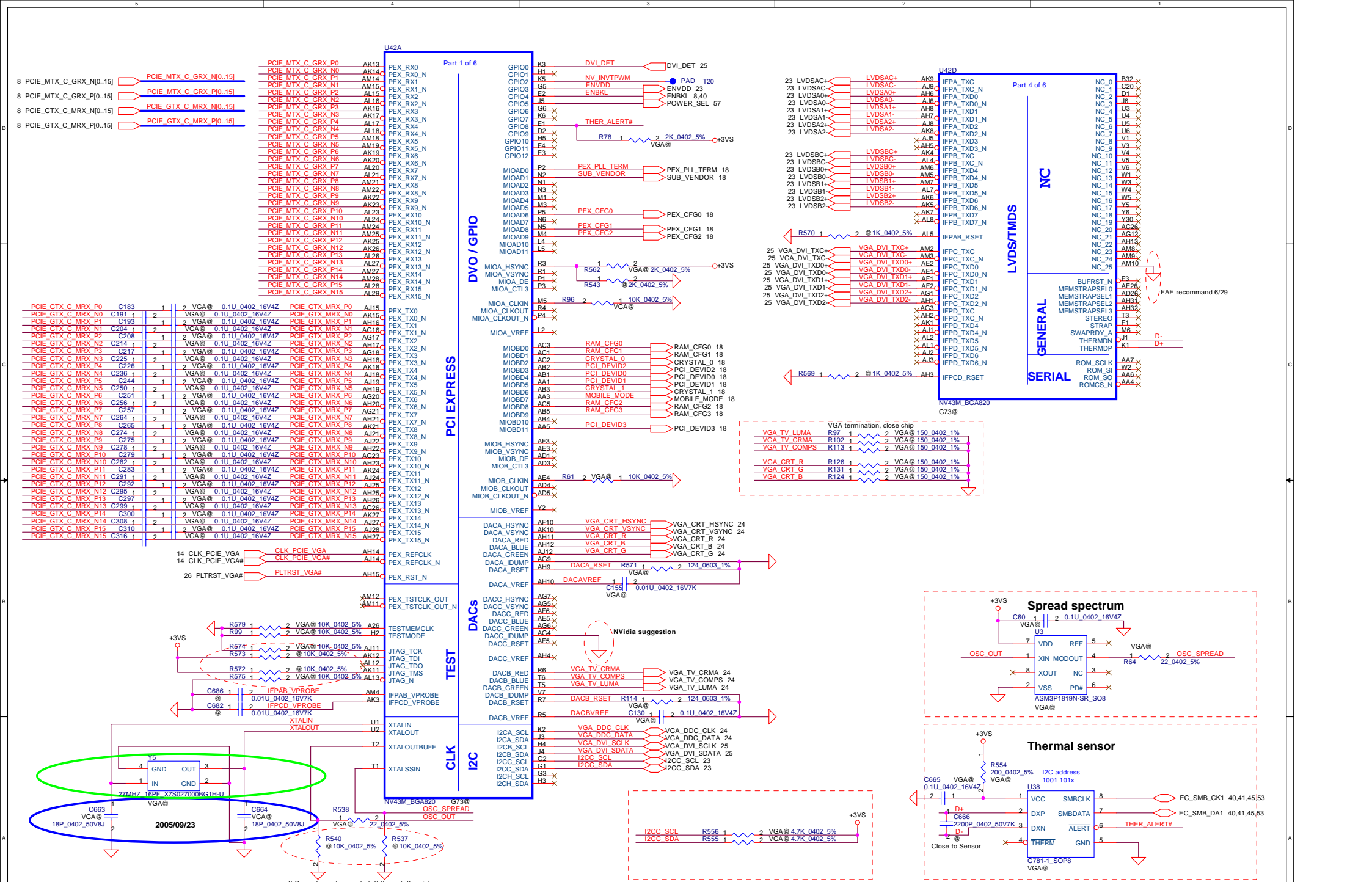
\*\*SEL\_24M/PCICLK2=0=TESTMODE  
\*\*SEL\_PCI6/PCICLK1=0=CLKREQ5#

\*\*SEL\_PCI5=1=PCICLK5  
ITP\_EN/PCICLK\_F0=0=SRC pair

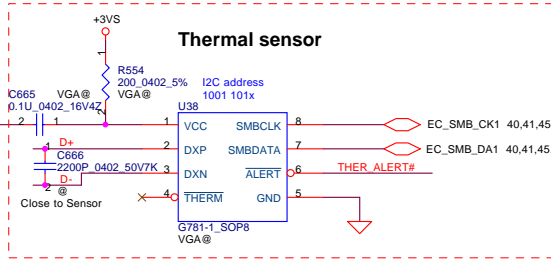
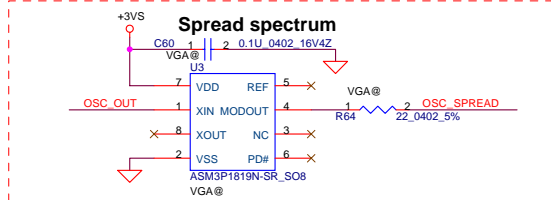


# Clock Generator

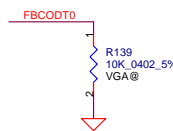
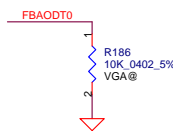
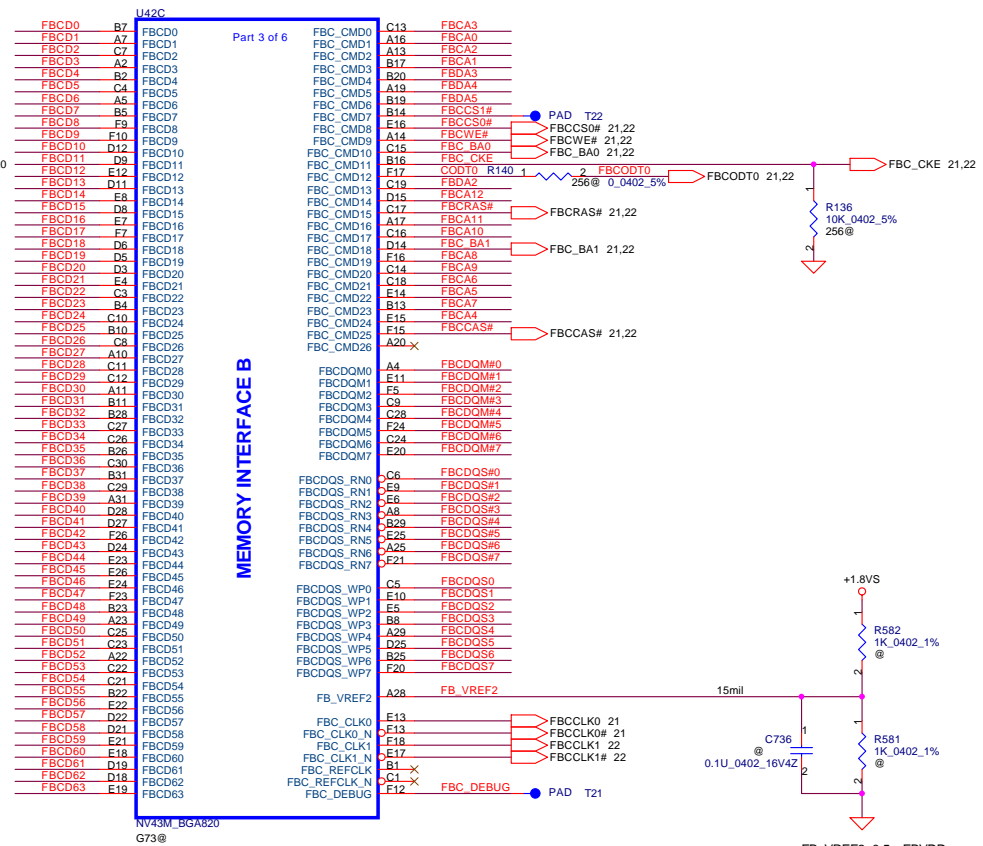
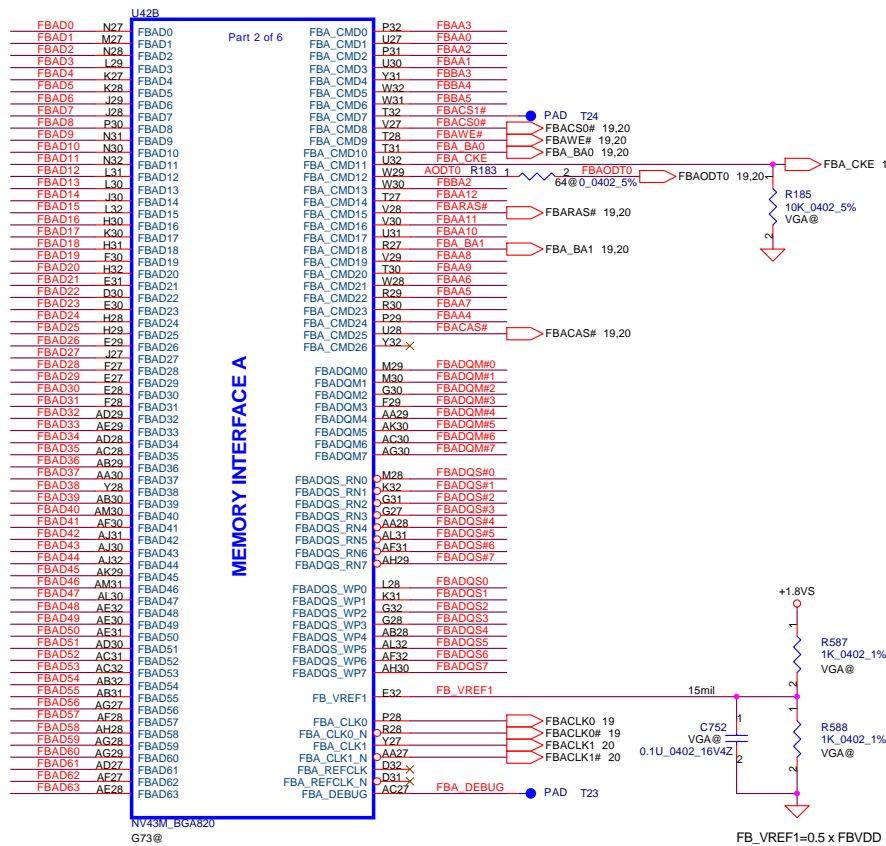
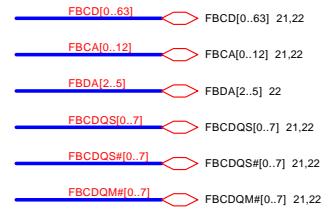
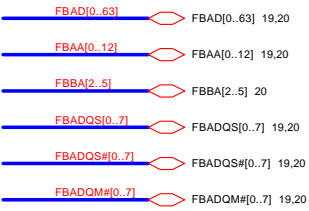
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		59		



If Spread spectrum not stuff than stuff resistor

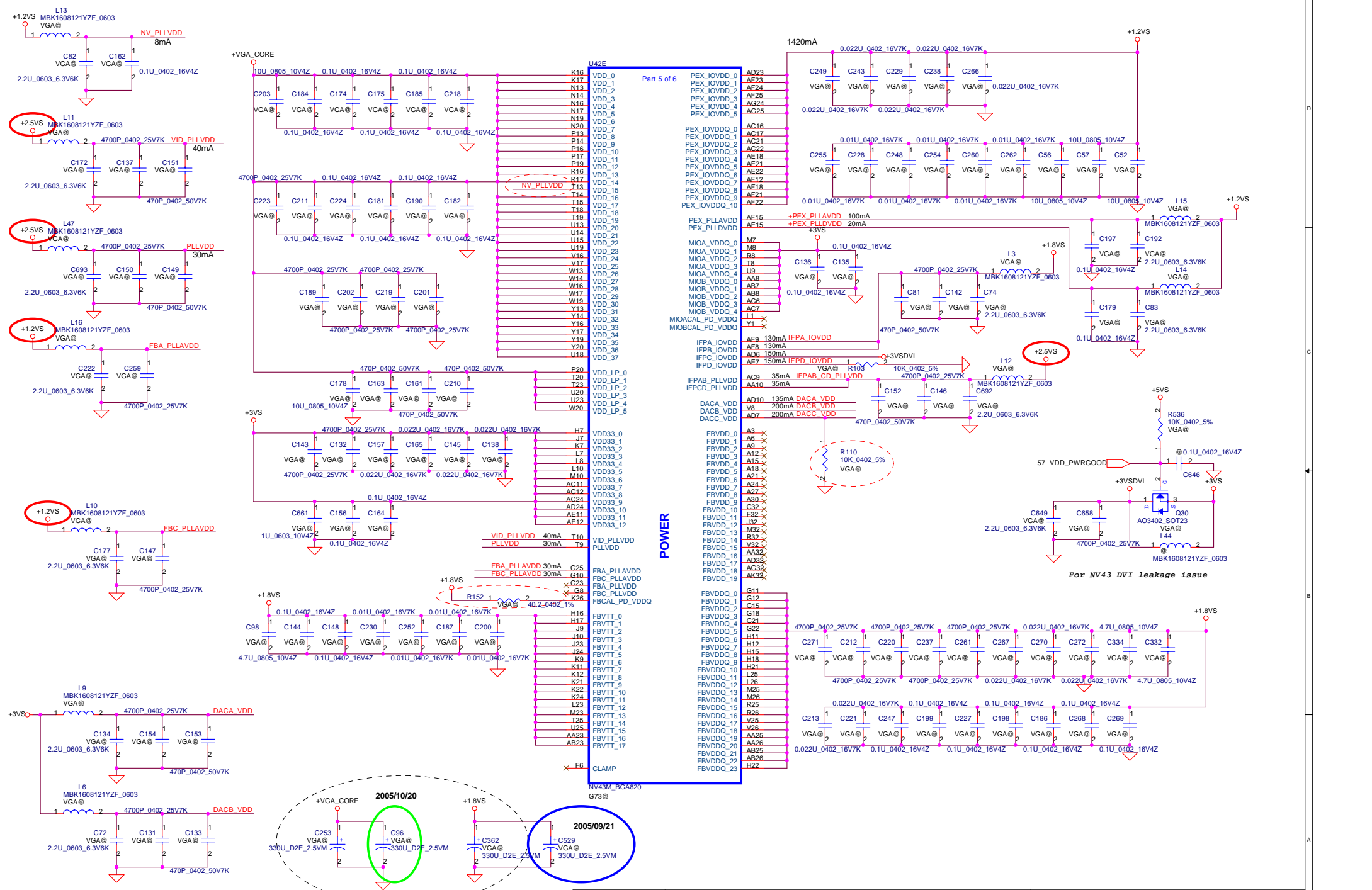


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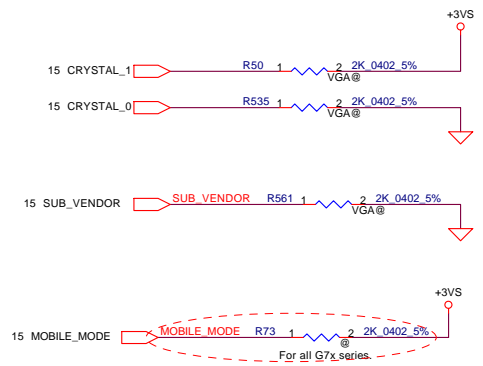
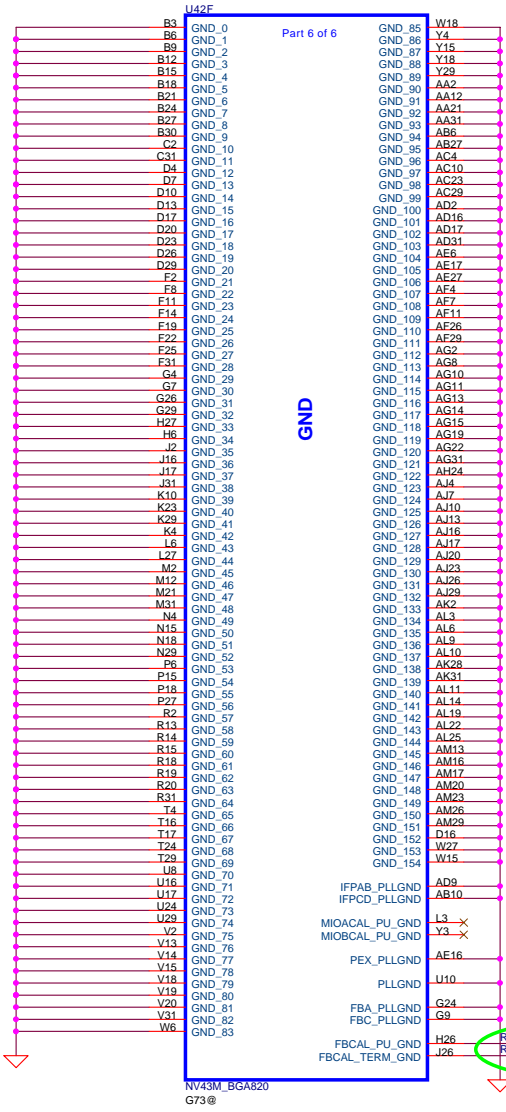




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Compal Electronics, Inc.		
Title <b>G72/G73 Power</b>		
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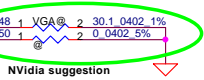
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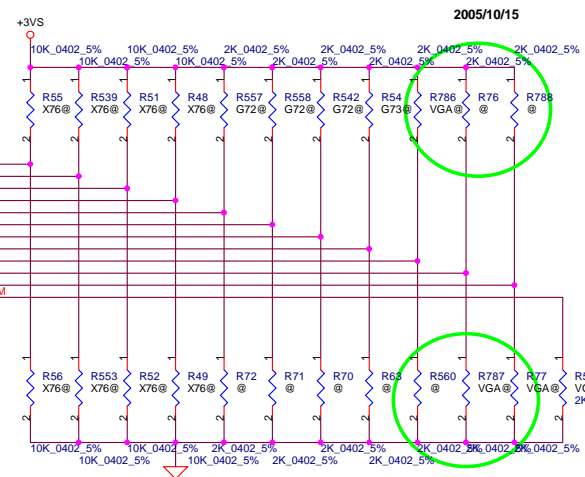
G73M : SA00000QZ00  
 G72M : SA00000QY00  
 G72MV : SA00000QY20

STRAPS	PIN	DESCRIPTION	Value	Value
CRYSTAL[1:0]	MIOBD[6,2]	27MHz=10, 14.318MHz=01, 13.5MHz=00	10	
ROM_TYPE[1:0]	MIOBD [11:10]	Parallel=00, SERIAL M25P10=01, Serial SST45VF=10	01	
SUB_VENDOR	MIOAD1	VBIOs on card (pull high) VBIOs with system BIOS (pull down)	0	
PEX_PLL_TERM	MIOAD0		0	
PEX_CFG[2:0]	MIOAD [9,8,6]	Recommended for G7x	010	
RAM_CFG[3:0]	MIOAD[5:2]	16Mx16x4 1.8V (128bit G73M)	0001	Samsung
		16Mx16x4 1.8V (128bit G73M)	0011	Hynix
		16Mx16x4 1.8V (64bit G73M)	1001	Samsung
		16Mx16x4 1.8V (64bit G73M)	1011	Hynix
		16Mx16x4 1.8V (64bit G72MV)	0001	Samsung
		16Mx16x4 1.8V (64bit G72MV)	0011	Hynix
PCI_DEVID[3:0]	VIPD[5:3] MIOA_HSYNC	G73M-xxxxx8 G72M-0x01D8	1000	
		G72MV-0x01D7 TBD/TBD	0111	
MOBILE_MODE	MIOBD7	For NV44M/G7x		0

RAM\_CFG[1:0]  
 (Manufacture)  
 (01=Sam, 10=Inf, 11=Hyn)  
 RAM\_CFG[2] (0=16M or 1=32M)  
 RAM\_CFG[3] (Bandwidth 0=Full, 1=Half)

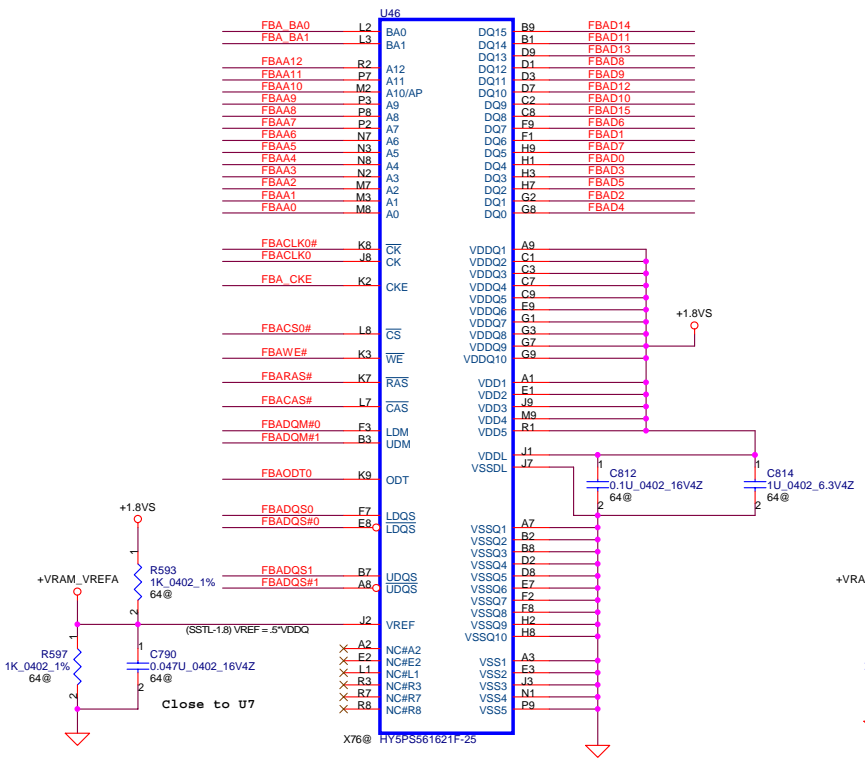


Bandwidth	RAM Type	Vendor
FULL	R49 32M R51	Samsung R553, R55
HALF	R48 16M R52	Hynix R539, R55
		Infineon R553, R56

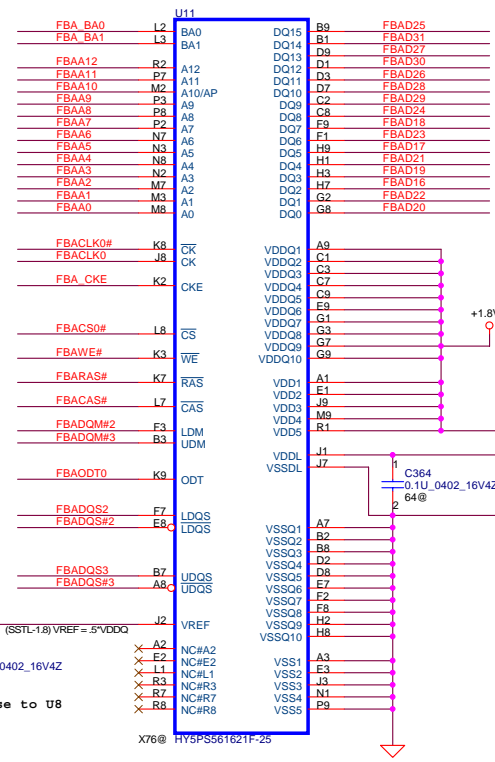


Package	Part Number	Part Number
(10*12.5)	Infineon GDDR2(400): SA00000S800 (HYB18T256161AFL-25)	Infineon GDDR2(350): SA00000T700 (HYB18T256161AF-28)
(11*13)	Samsung GDDR2 (400): SA00000FG10 (K4N56163QF-ZC25)	Samsung GDDR2 (350): SA00000TB00 (K4N56163QF-ZC2A)
(8*13)	Hynix GDDR2 (400): SA00000FF10 (HY5PS561621AFP-25)	Hynix GDDR2 (350): SA00000TJ00 (HY5PS561621AFP-28)

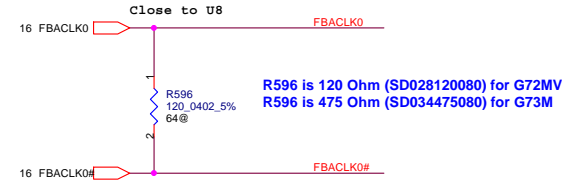
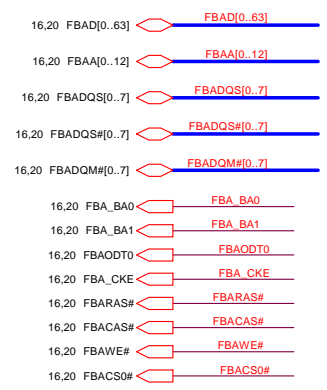
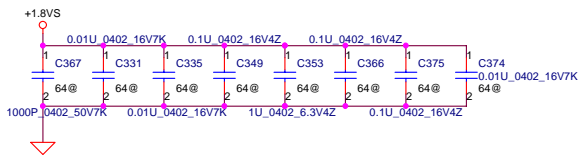
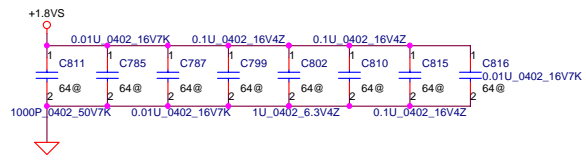
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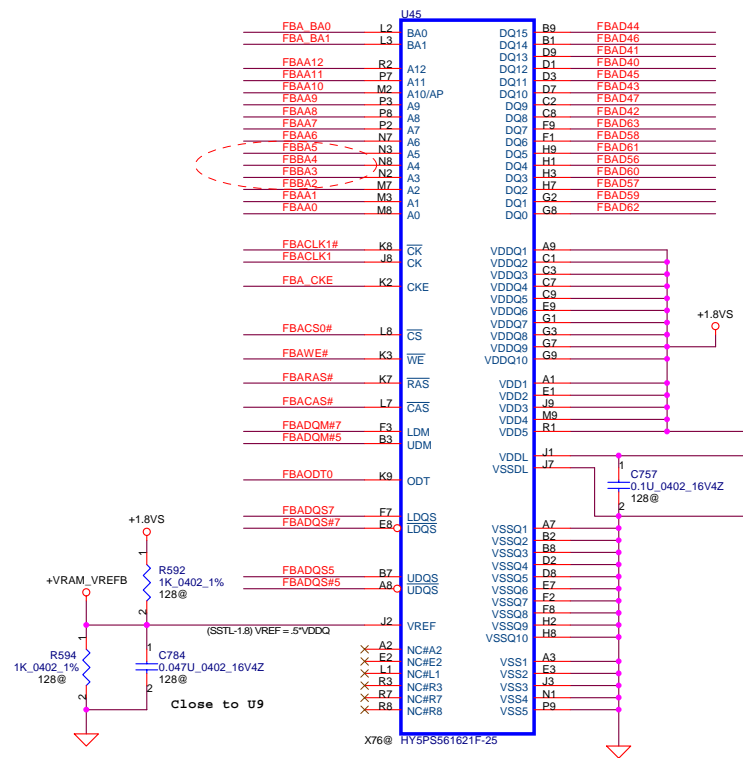
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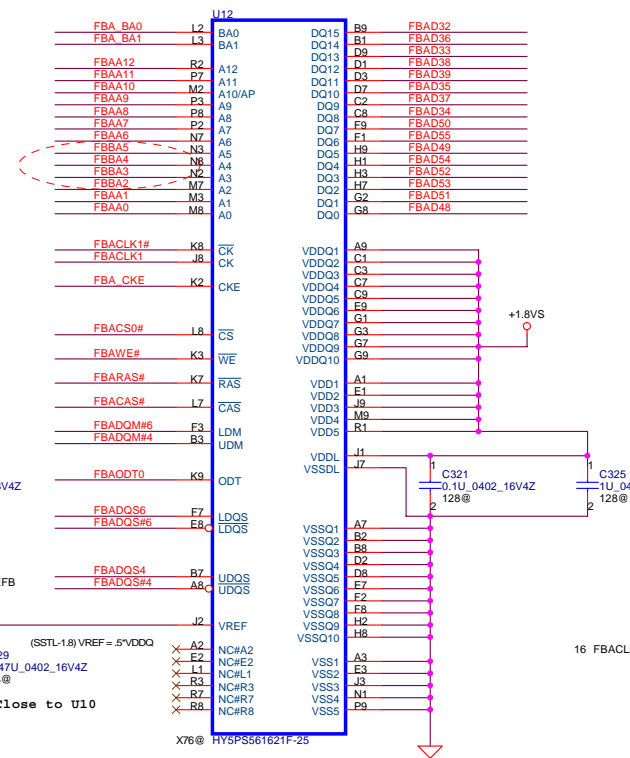
DDR2 BGA MEMORY



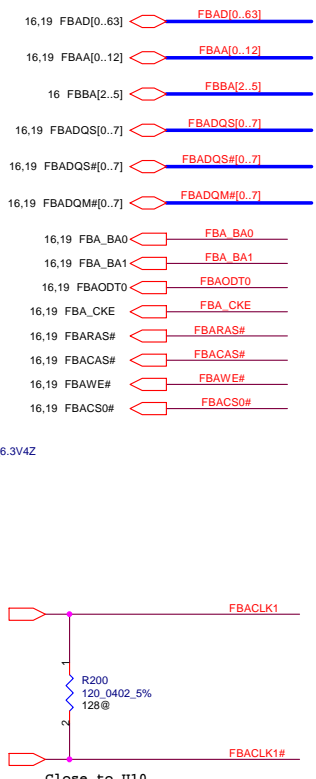
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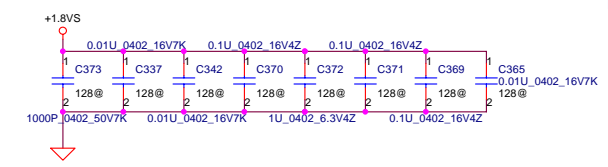
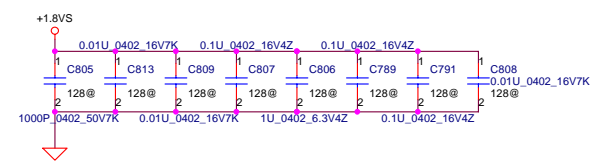
DDR2 BGA MEMORY



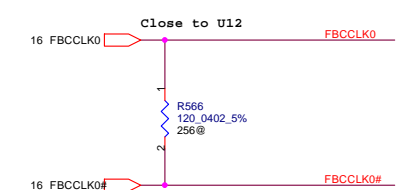
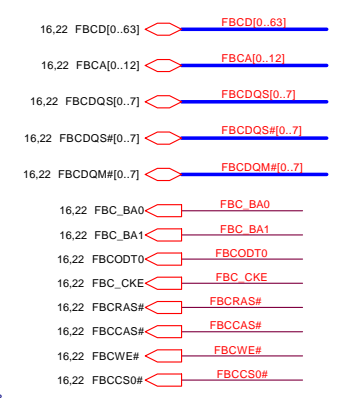
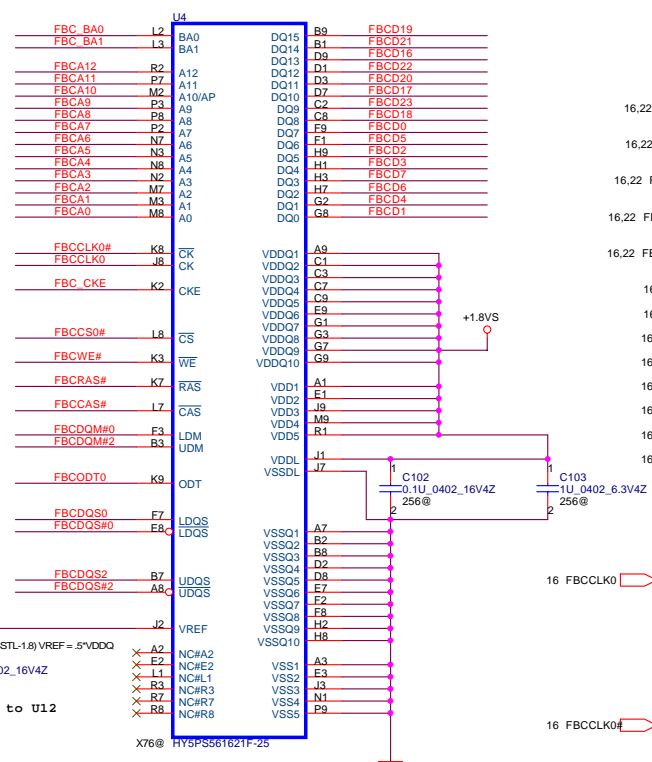
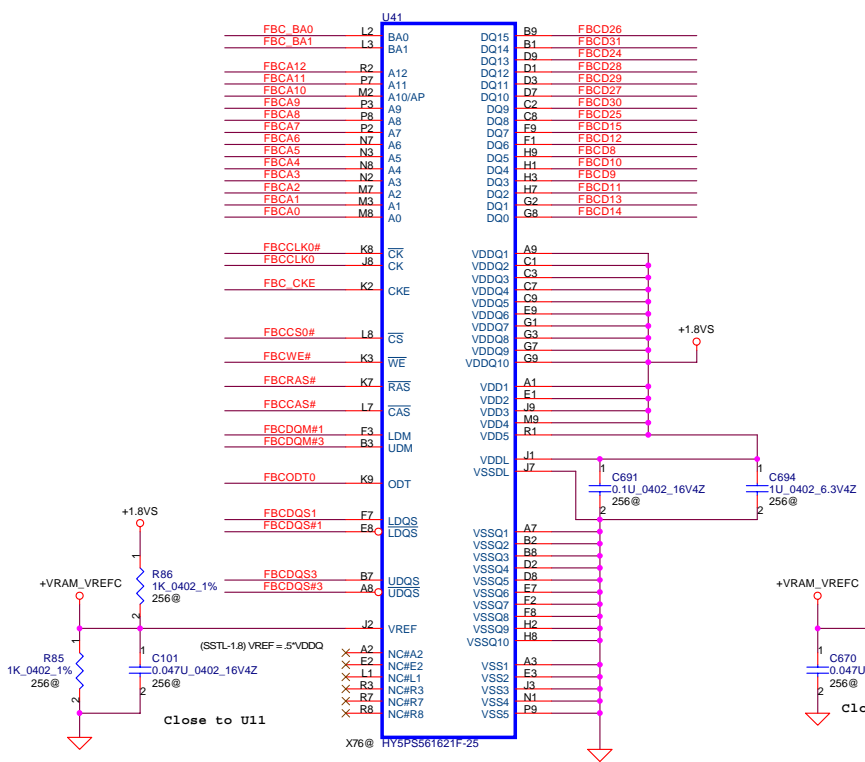
DDR2 BGA MEMORY



R200 is 120 Ohm (SD028120080) for G72MV  
R200 is 481 Ohm (SD00000CA80) for G73M



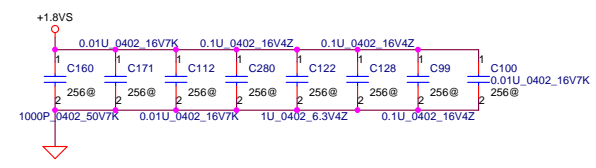
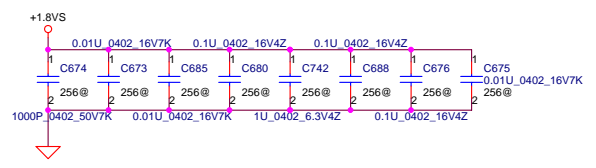
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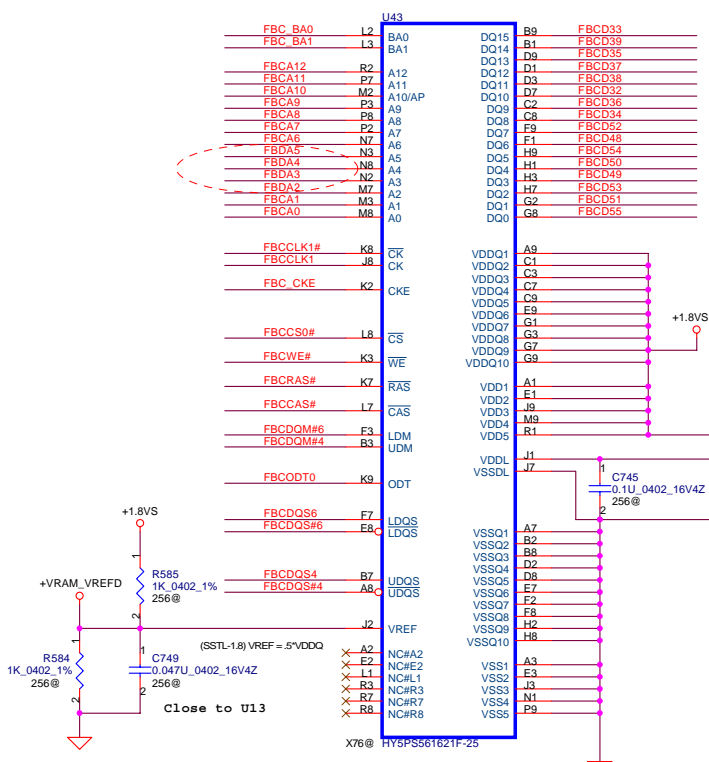
R566 is 120 Ohm (SD028120080) for G72MV  
R566 is 481 Ohm (SD00000CA80) for G73M

DDR2 BGA MEMORY

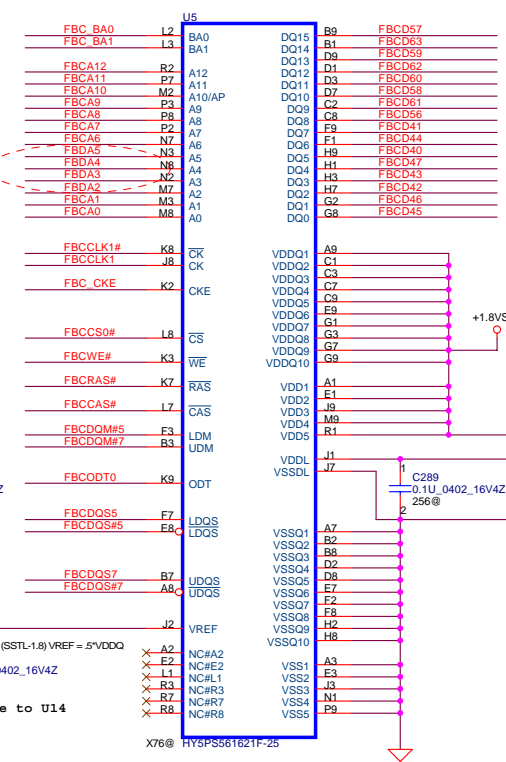
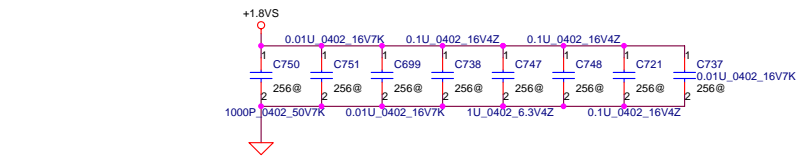
DDR2 BGA MEMORY



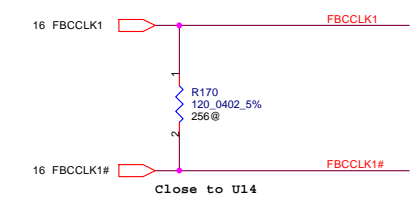
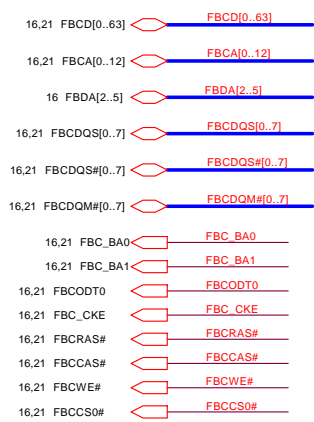
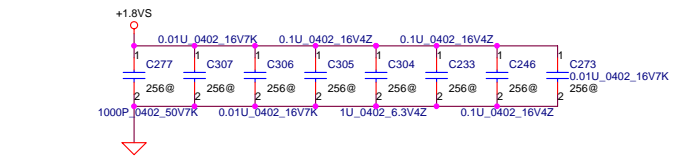
Security Classification	Compal Secret Data		Title	
Issued Date	2005/06/20	Deciphered Date	2006/06/20	VRAM DDRC
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DDR2 BGA MEMORY



DDR2 BGA MEMORY

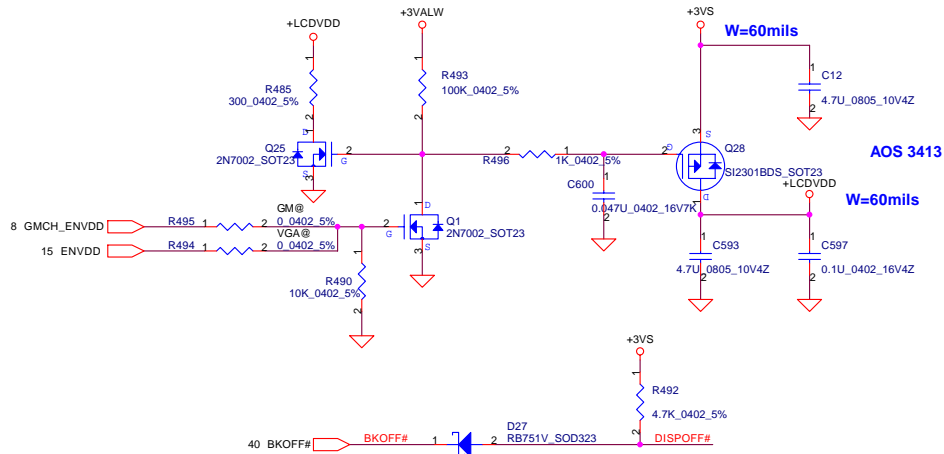


R170 is 120 Ohm (SD028120080) for G72MV  
R170 is 481 Ohm (SD00000CA80) for G73M

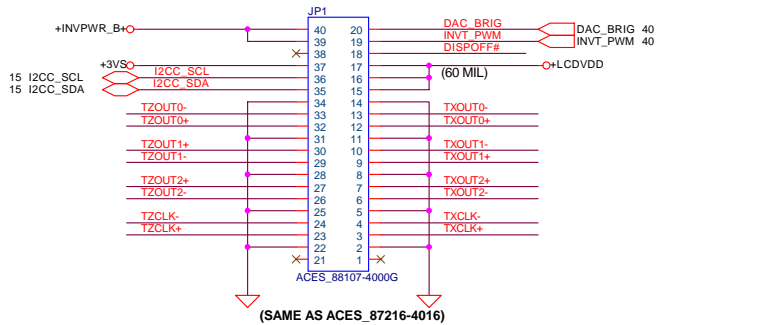
Security Classification	Compal Secret Data	
Issued Date	2005/06/20	Deciphered Date
		2006/06/20
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Compal Electronics, Inc.		
Title		
VRAM DDRD		
Size	Document Number	Rev
Custom	HBL50 LA-2921P	0.3
Date:	Friday, November 11, 2005	Sheet 22 of 59

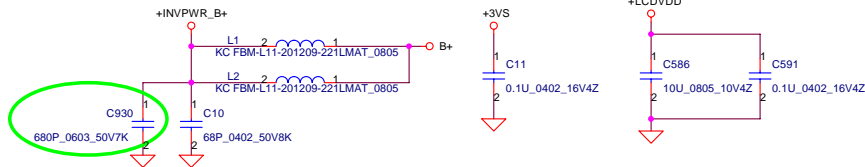
# LCD POWER CIRCUIT



## LCD/PANEL BD. Conn.



(SAME AS ACES\_87216-4016)

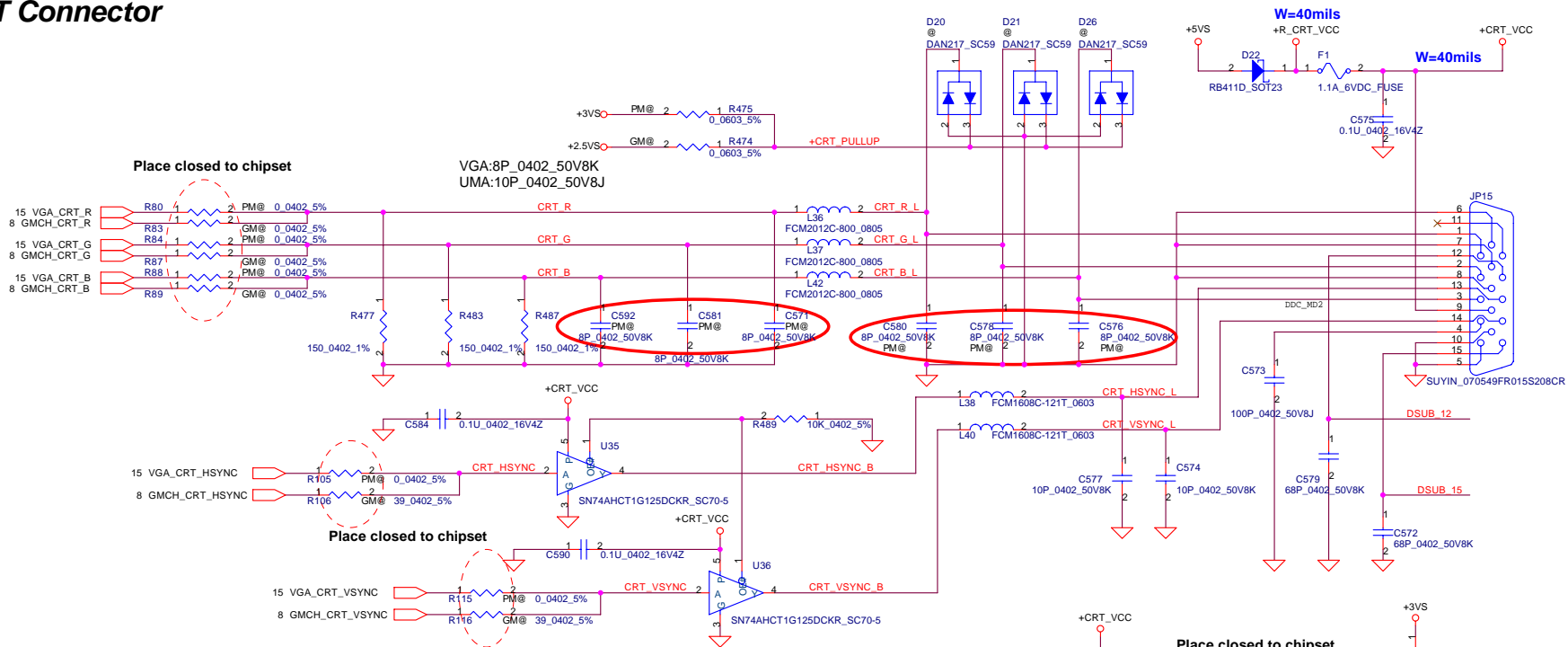


TXOUT0-	R25	1	2	VGA@ 0.0402 5%	LVDSA0-	LVDSA0-	15
TXOUT0+	R26	1	2	VGA@ 0.0402 5%	LVDSA0+	LVDSA0+	15
TXOUT1-	R27	1	2	VGA@ 0.0402 5%	LVDSA1-	LVDSA1-	15
TXOUT1+	R28	1	2	VGA@ 0.0402 5%	LVDSA1+	LVDSA1+	15
TXOUT2-	R29	1	2	VGA@ 0.0402 5%	LVDSA2-	LVDSA2-	15
TXOUT2+	R30	1	2	VGA@ 0.0402 5%	LVDSA2+	LVDSA2+	15
TXCLK-	R31	1	2	VGA@ 0.0402 5%	LVDSAC-	LVDSAC-	15
TXCLK+	R32	1	2	VGA@ 0.0402 5%	LVDSAC+	LVDSAC+	15
TZOUT0-	R33	1	2	VGA@ 0.0402 5%	LVDSB0-	LVDSB0-	15
TZOUT0+	R34	1	2	VGA@ 0.0402 5%	LVDSB0+	LVDSB0+	15
TZOUT1-	R35	1	2	VGA@ 0.0402 5%	LVDSB1-	LVDSB1-	15
TZOUT1+	R36	1	2	VGA@ 0.0402 5%	LVDSB1+	LVDSB1+	15
TZOUT2-	R37	1	2	VGA@ 0.0402 5%	LVDSB2-	LVDSB2-	15
TZOUT2+	R38	1	2	VGA@ 0.0402 5%	LVDSB2+	LVDSB2+	15
TZCLK-	R39	1	2	VGA@ 0.0402 5%	LVDSBC-	LVDSBC-	15
TZCLK+	R40	1	2	VGA@ 0.0402 5%	LVDSBC+	LVDSBC+	15
I2CC_SCL	R41	1	2	GM@ 0.0402 5%	GMCH_LCD_CLK	GMCH_LCD_CLK	8
I2CC_SDA	R42	1	2	GM@ 0.0402 5%	GMCH_LCD_DATA	GMCH_LCD_DATA	8
TXOUT0-	R509	1	2	GM@ 0.0402 5%	GMCH_TXOUT0-	GMCH_TXOUT0-	8
TXOUT0+	R508	1	2	GM@ 0.0402 5%	GMCH_TXOUT0+	GMCH_TXOUT0+	8
TXOUT1-	R507	1	2	GM@ 0.0402 5%	GMCH_TXOUT1-	GMCH_TXOUT1-	8
TXOUT1+	R506	1	2	GM@ 0.0402 5%	GMCH_TXOUT1+	GMCH_TXOUT1+	8
TXOUT2-	R505	1	2	GM@ 0.0402 5%	GMCH_TXOUT2-	GMCH_TXOUT2-	8
TXOUT2+	R504	1	2	GM@ 0.0402 5%	GMCH_TXOUT2+	GMCH_TXOUT2+	8
TXCLK-	R503	1	2	GM@ 0.0402 5%	GMCH_TXCLK-	GMCH_TXCLK-	8
TXCLK+	R502	1	2	GM@ 0.0402 5%	GMCH_TXCLK+	GMCH_TXCLK+	8
TZOUT0-	R525	1	2	GM@ 0.0402 5%	GMCH_TZOUT0-	GMCH_TZOUT0-	8
TZOUT0+	R524	1	2	GM@ 0.0402 5%	GMCH_TZOUT0+	GMCH_TZOUT0+	8
TZOUT1-	R523	1	2	GM@ 0.0402 5%	GMCH_TZOUT1-	GMCH_TZOUT1-	8
TZOUT1+	R522	1	2	GM@ 0.0402 5%	GMCH_TZOUT1+	GMCH_TZOUT1+	8
TZOUT2-	R521	1	2	GM@ 0.0402 5%	GMCH_TZOUT2-	GMCH_TZOUT2-	8
TZOUT2+	R520	1	2	GM@ 0.0402 5%	GMCH_TZOUT2+	GMCH_TZOUT2+	8
TZCLK-	R519	1	2	GM@ 0.0402 5%	GMCH_TZCLK-	GMCH_TZCLK-	8
TZCLK+	R518	1	2	GM@ 0.0402 5%	GMCH_TZCLK+	GMCH_TZCLK+	8

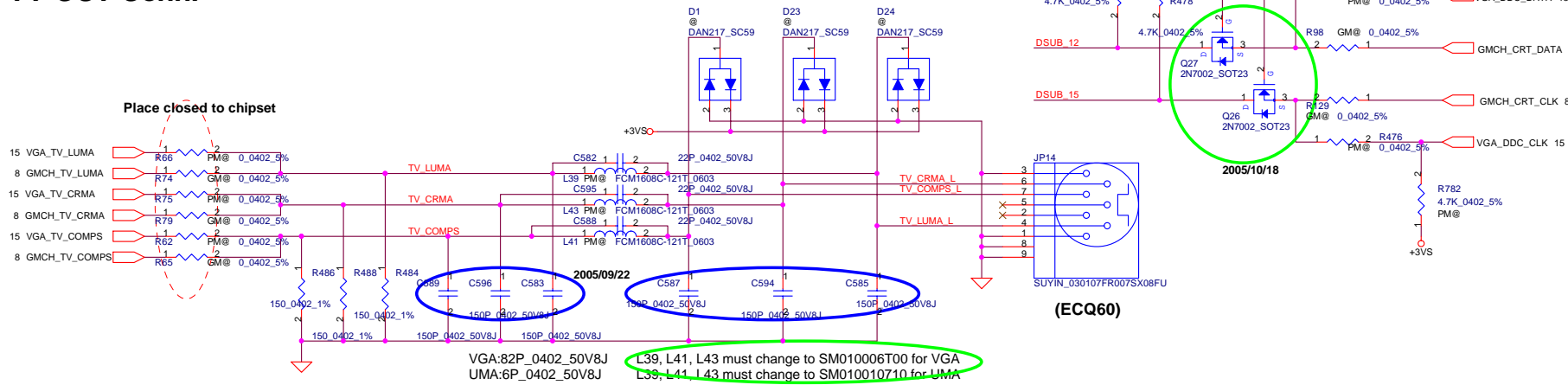
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Issued Date	2005/06/20	Deciphered Date	2006/06/20	Title	
				LCD Connector	
				Size	Document Number
				B	HBL50 LA-2921P
				Rev	0.3
				Date:	Friday, November 11, 2005
				Sheet	23 of 59

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# CRT Connector

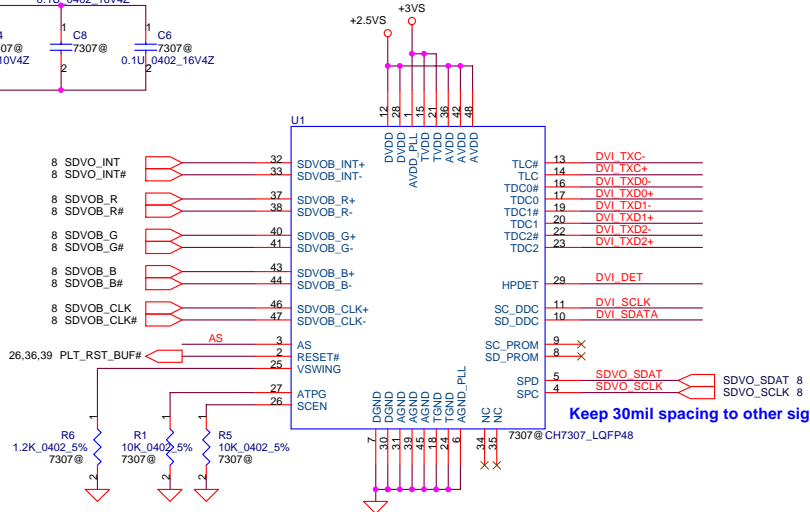
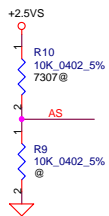
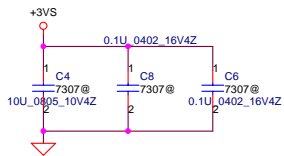
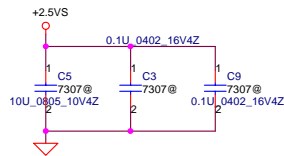


# TV-OUT Conn.

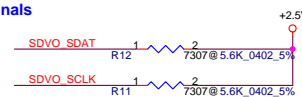


Security Classification		Compal Secret Data		Title	
Issued Date	2005/06/20	Deciphered Date	2006/06/20	Compal Electronics, Inc.	
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Size	Document Number	Rev		Date	
B	HBL50 LA-2921P	0.3		Friday, November 11, 2005	
				Sheet	24 of 59

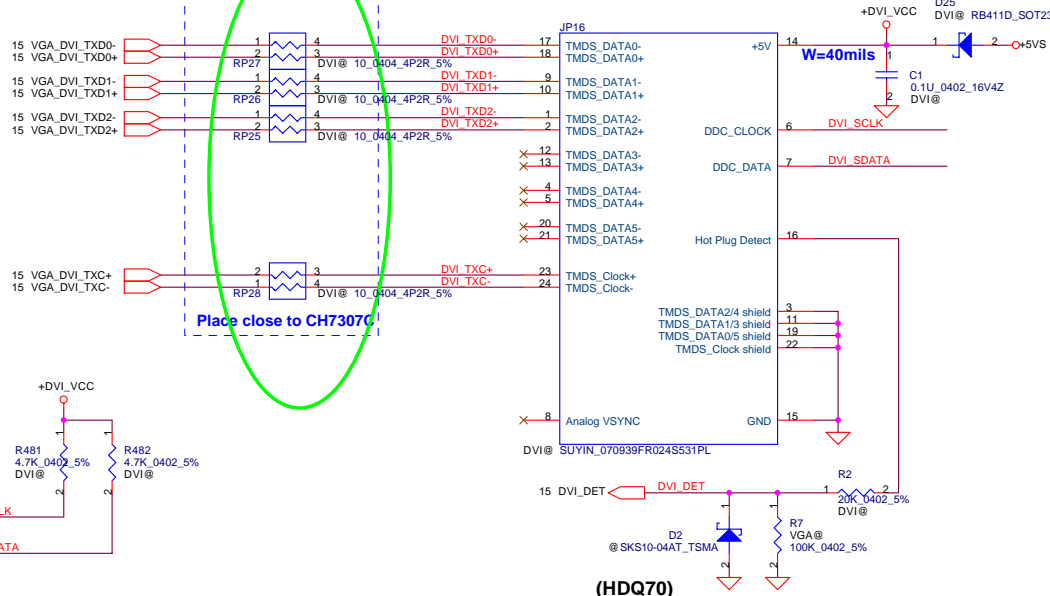




BOM structure	DVI from SDVO	DVI from Discrete VGA
7307@	Stuff	No_Stuff
VGA@	No_Stuff	Stuff
@	No_Stuff	No_Stuff

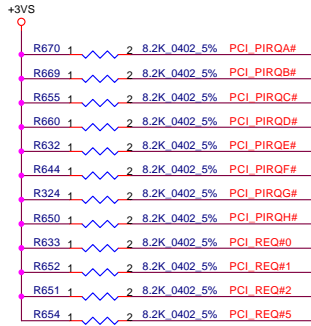
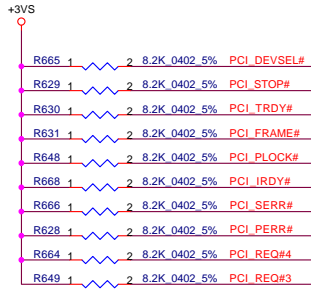


### DVI-D Connector

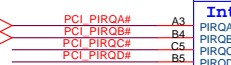
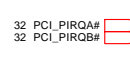
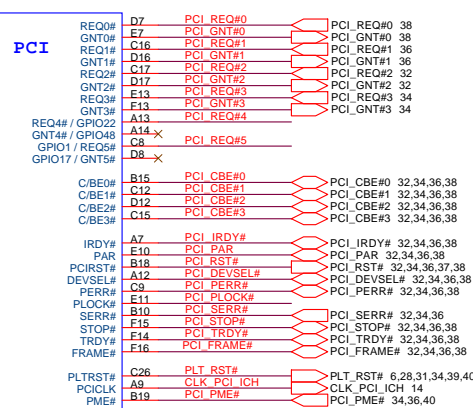
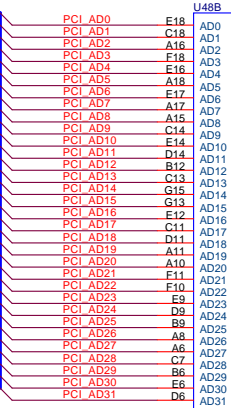


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				Date:	Friday, November 11, 2005	Sheet 25 of 59

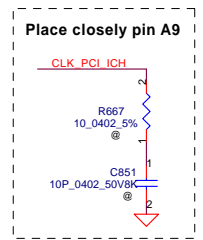
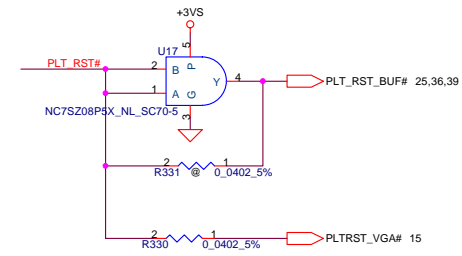
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 ICH7M-DH(B-0) (QK17) [QS]:SA00000JK60



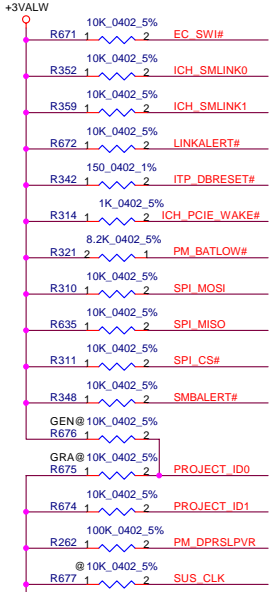
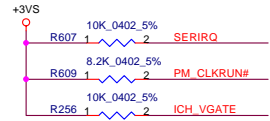
32,34,36,38 PCI\_AD[0..31]



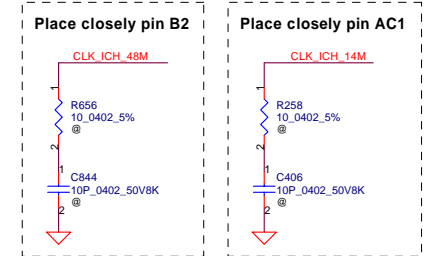
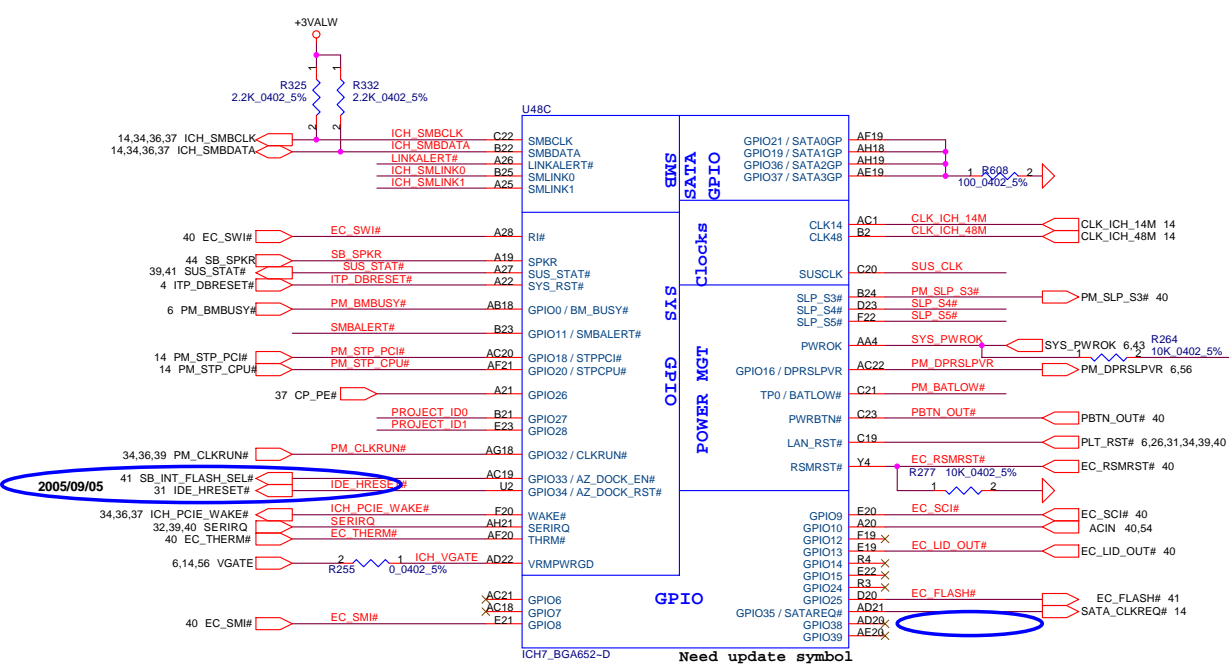
CH7\_BGA652-D



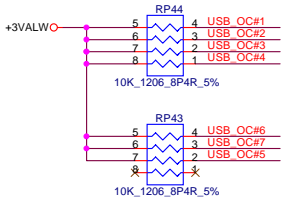
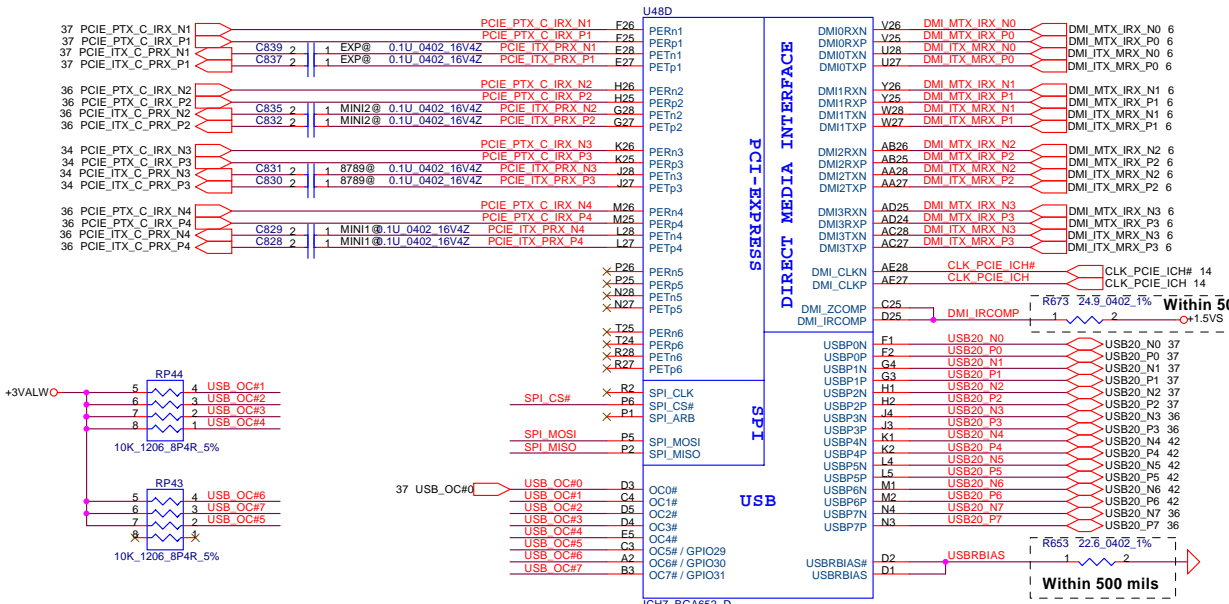
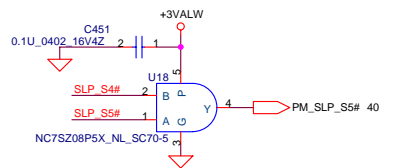




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01	= Geneva

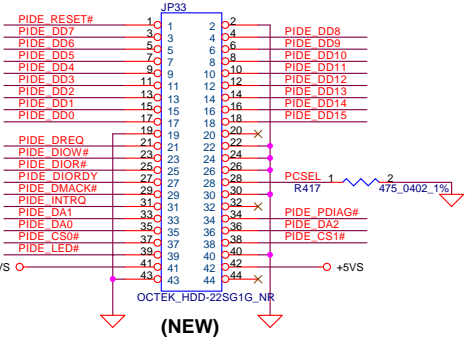
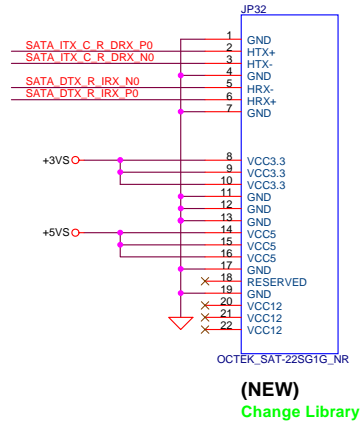
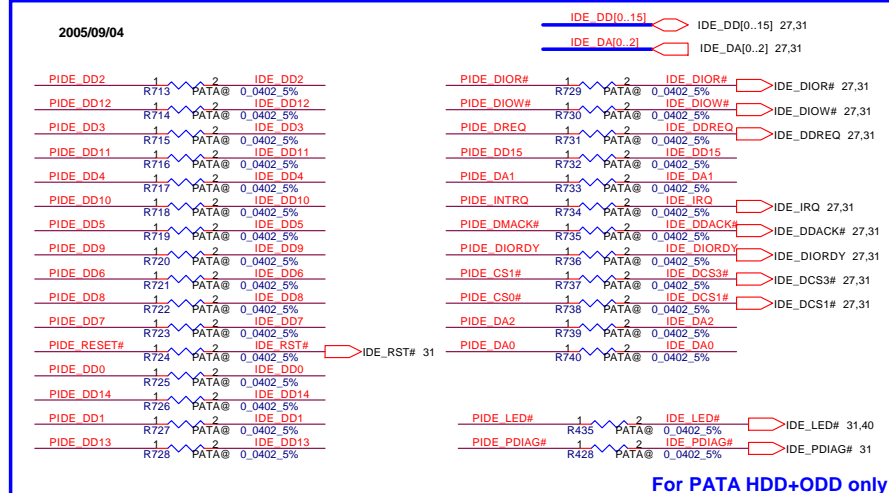
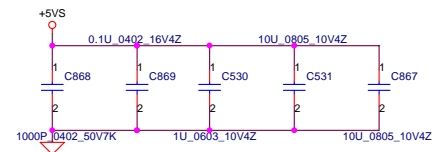
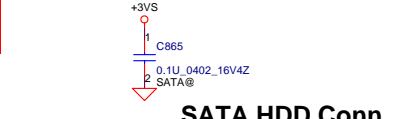
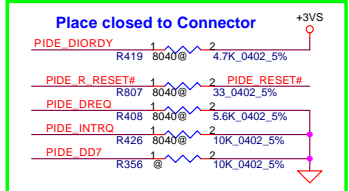
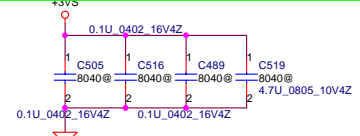
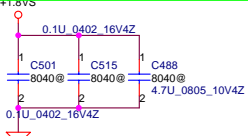
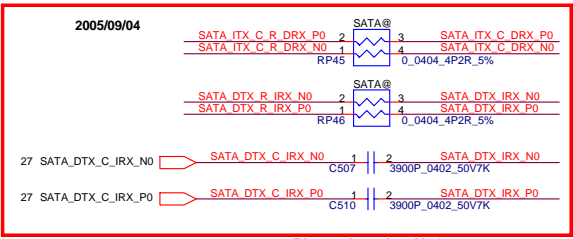
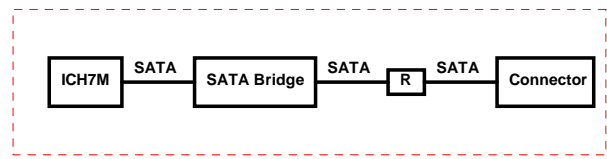
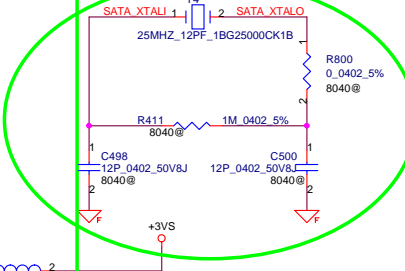
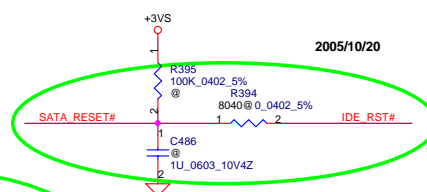
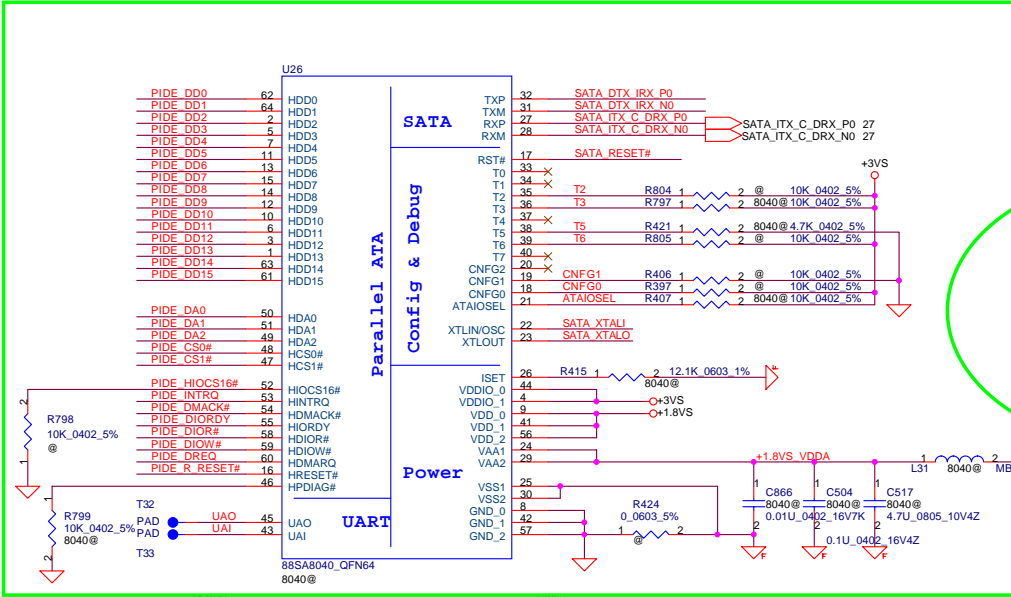


PM\_DPRSPLVPR : Need to series a 500Ohm resistor to IMVP6



Security Classification	Compal Secret Data		Title	
Issued Date	2005/06/20	Deciphered Date	2006/06/20	<b>ICH7-M(3/4)</b>
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Size	Document Number	Rev		
Custom	HBL50 LA-2921P	0.3		
Date:	Friday, November 11, 2005	Sheet	28	of 59

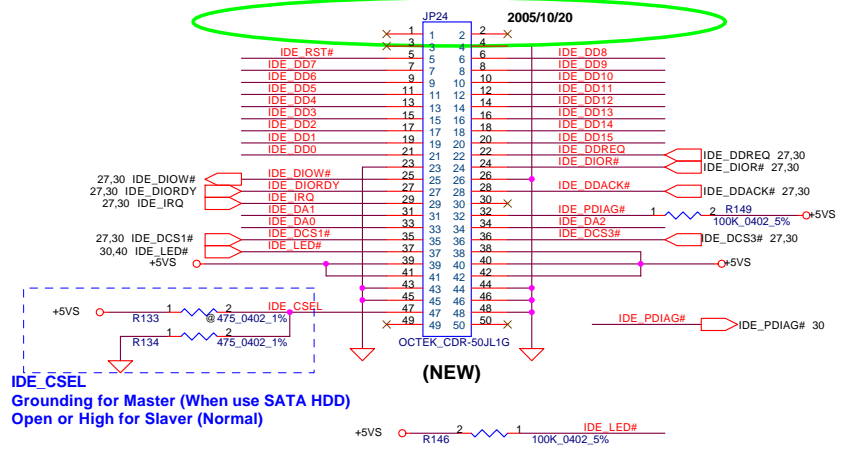
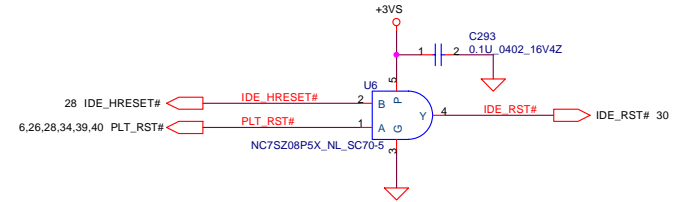
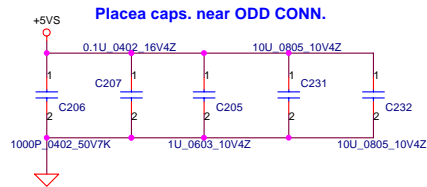




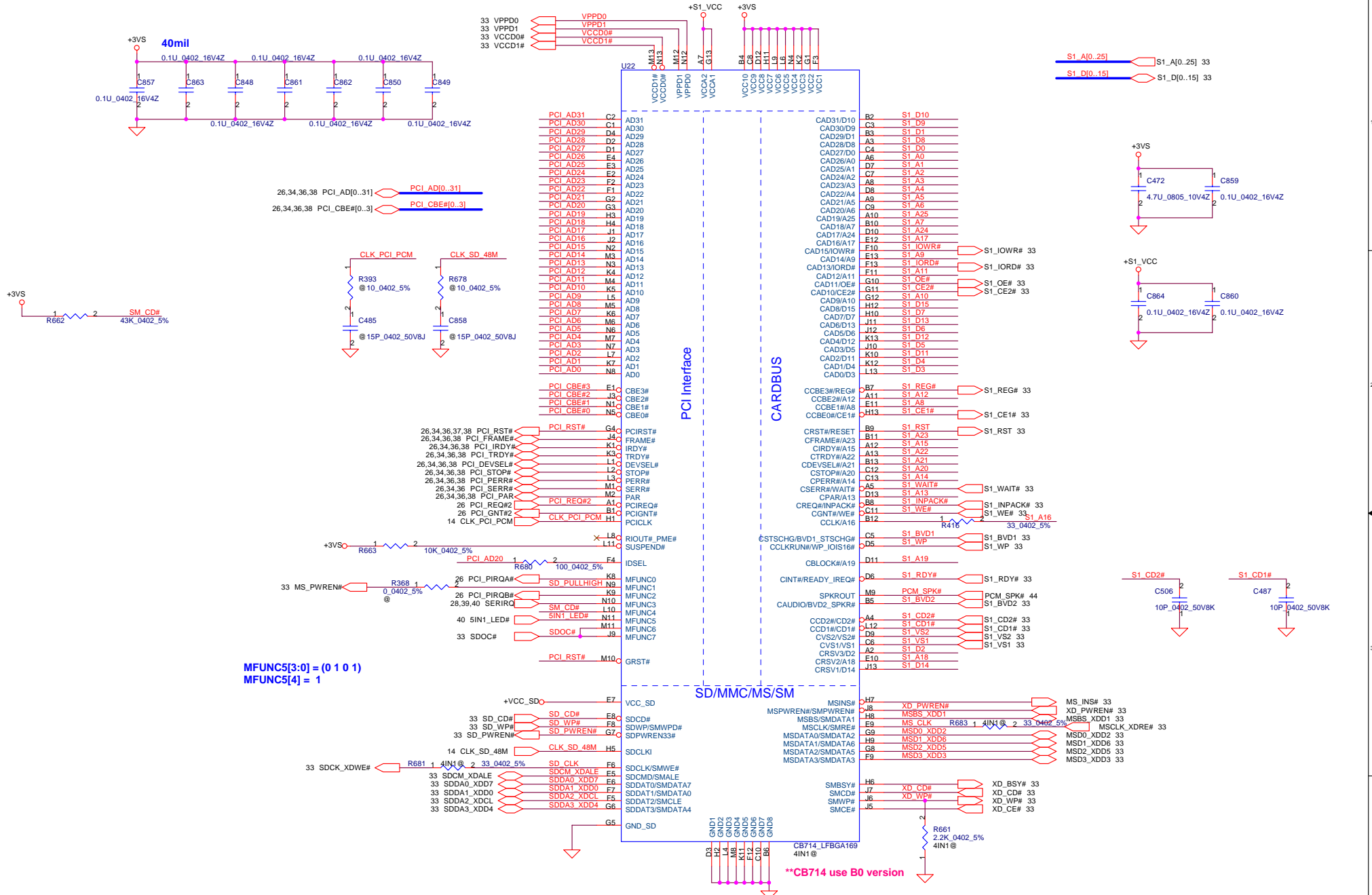
Security Classification	Compal Secret Data	
Issued Date	2005/06/20	Deciphered Date
		2006/06/20

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Compal Electronics, Inc.		
Title		
SATA Bridge		
Size	Document Number	Rev
B	HBL50 LA-2921P	0.3
Date:	Friday, November 11, 2005	Sheet 30 of 59



Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2005/06/20	Deciphered Date	2006/06/20	Title
				ODD & SATA HDD Connector
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			Document Number	Rev
			HBL50 LA-2921P	0.3
			Date: Friday, November 11, 2005	Sheet 31 of 59



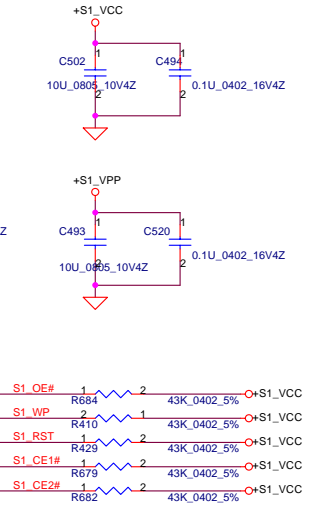
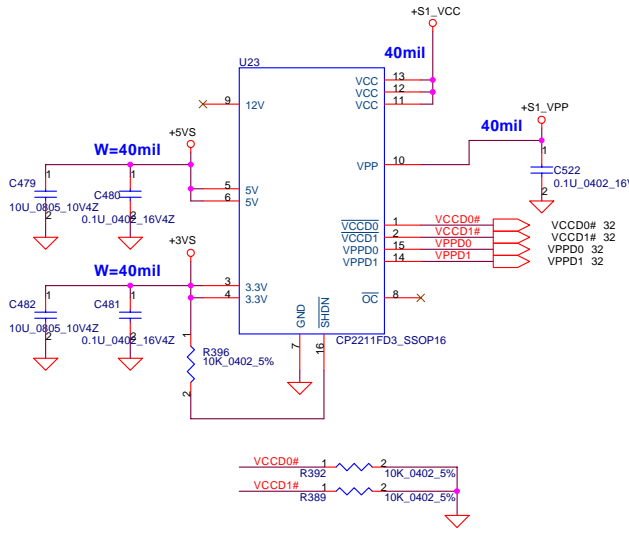
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**CB1410 P/N: SA014100310**

**\*\*CB714 use B0 version**

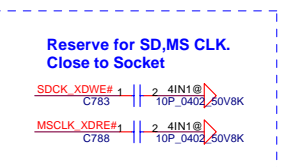
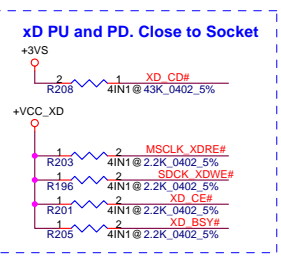
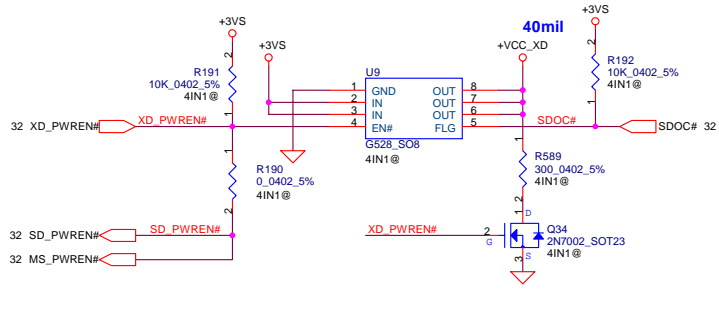
Security Classification	Compal Secret Data		Title	
Issued Date	2005/06/20	Deciphered Date	2006/06/20	Cardbus Controller CB714
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Date:	Friday, November 11, 2005	Sheet	32 of 59	Rev 0.3



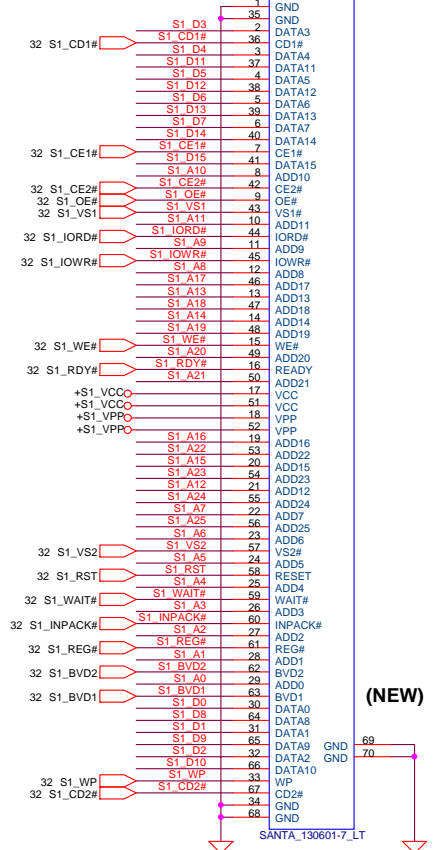
### PCMCIA Power Control



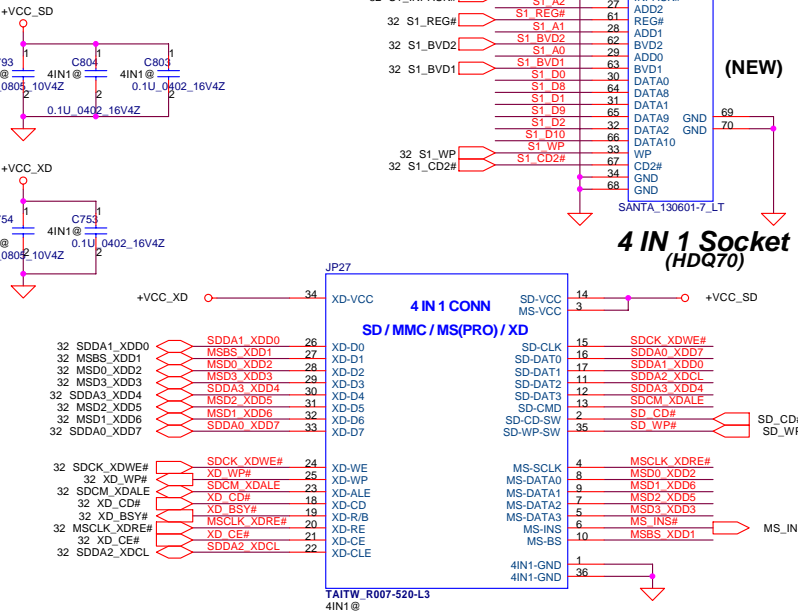
### SD/MS Power Control XD Power Control



### PCMCIA Socket



### 4 IN 1 Socket (HDQ70)



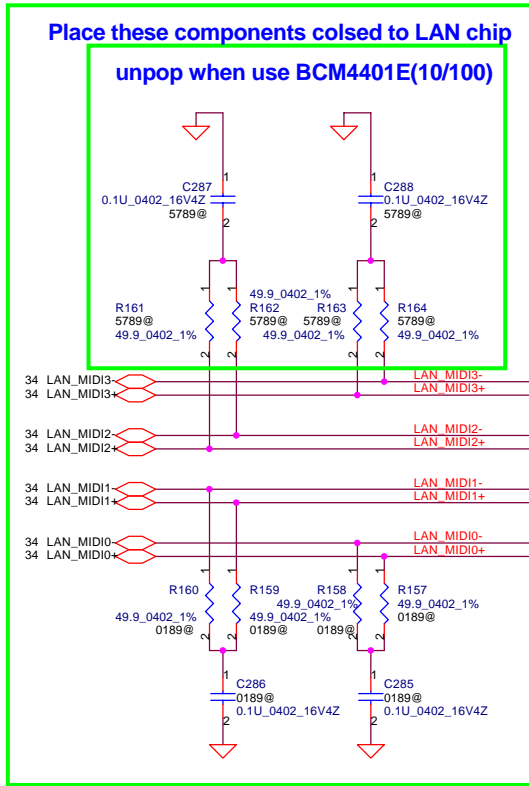
Security Classification	Compal Secret Data		Title	
Issued Date	2005/06/20	Deciphered Date	2006/06/20	PCMCIA Socket
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Document Number			Rev	0.3
HBL50 LA-2921P			Date:	Friday, November 11, 2005
Sheet 33 of 59				



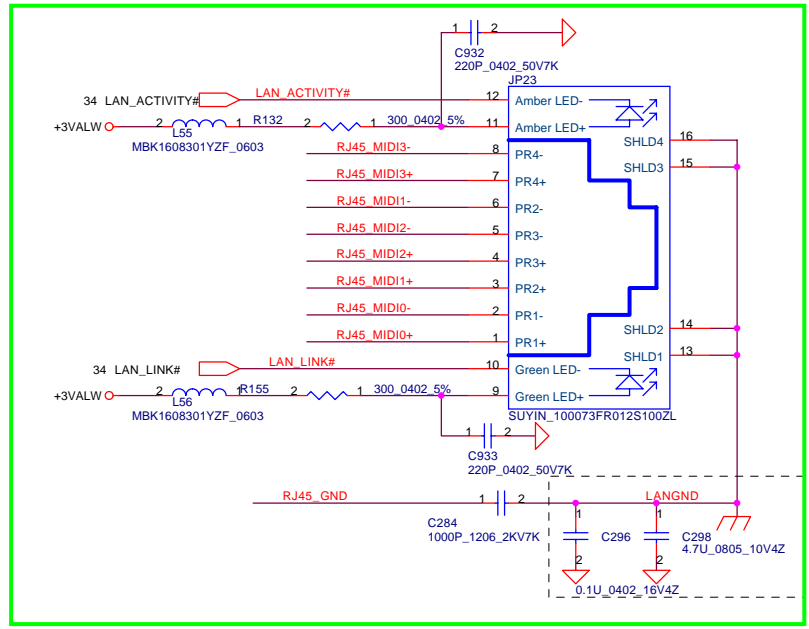
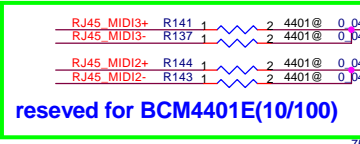
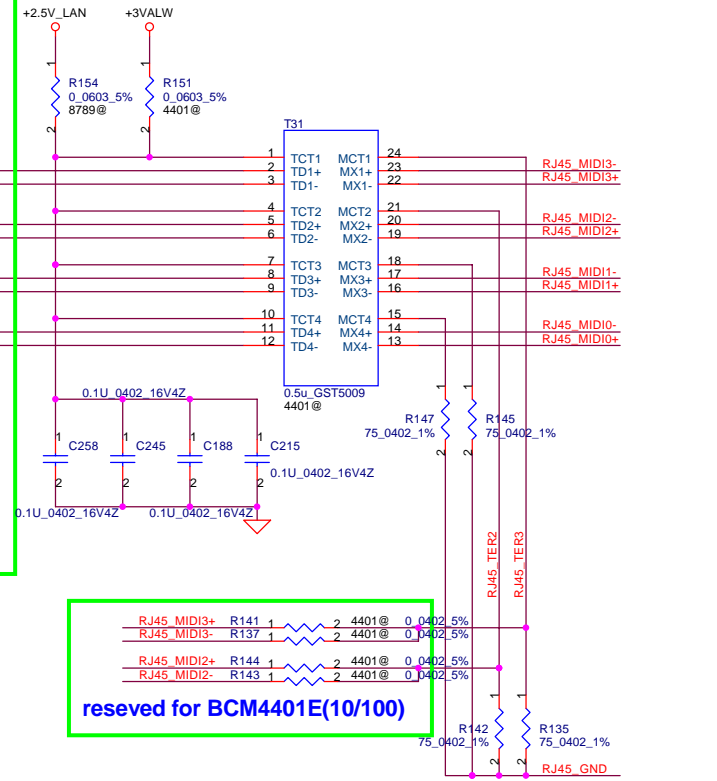
# LAN BCM4401E/ BCM5789

Place these components colsed to LAN chip

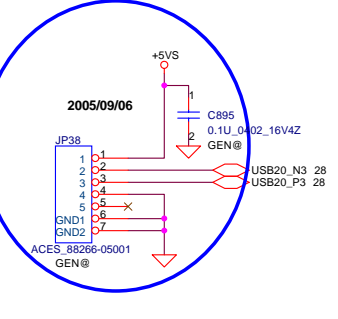
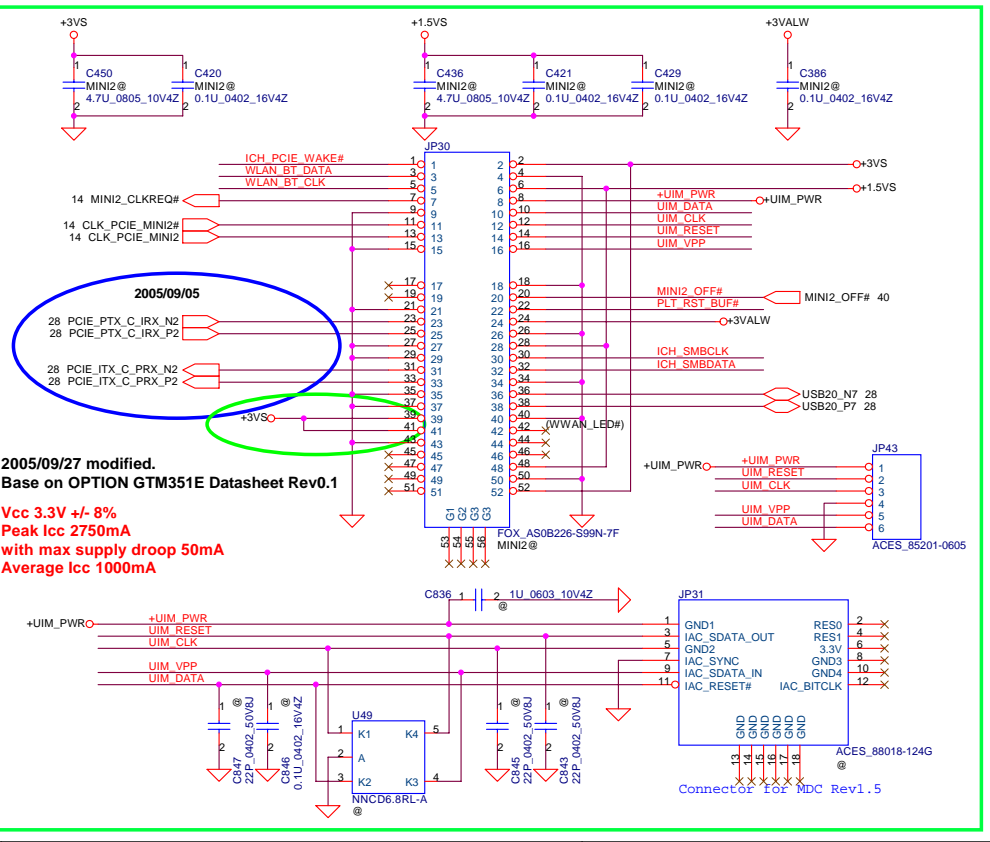
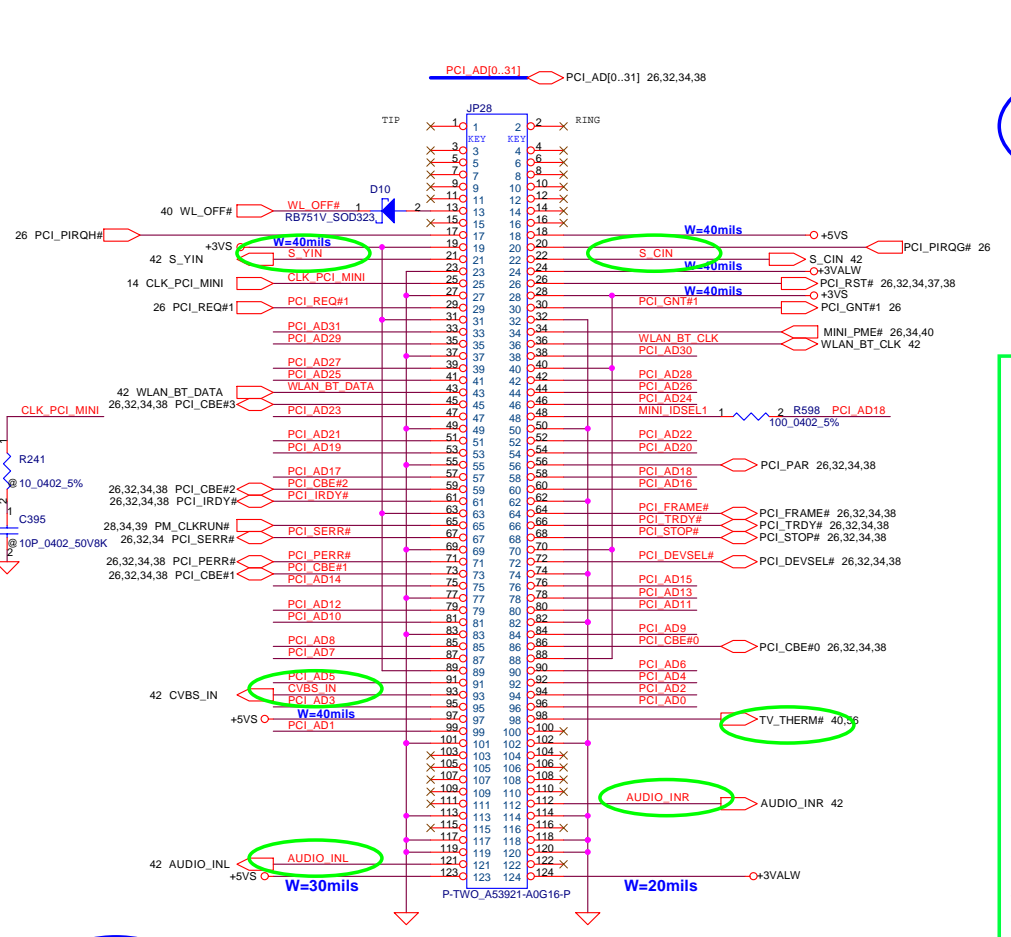
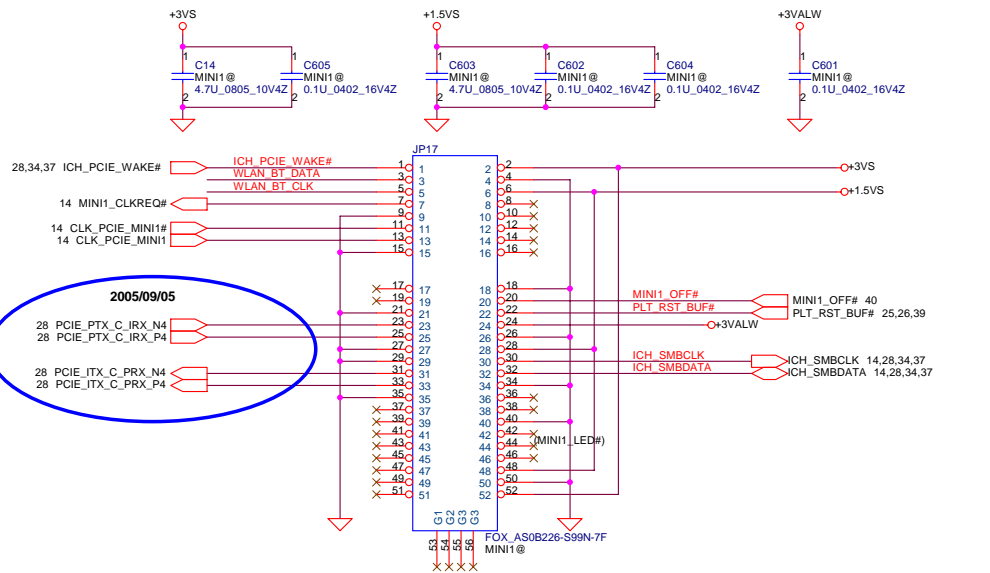
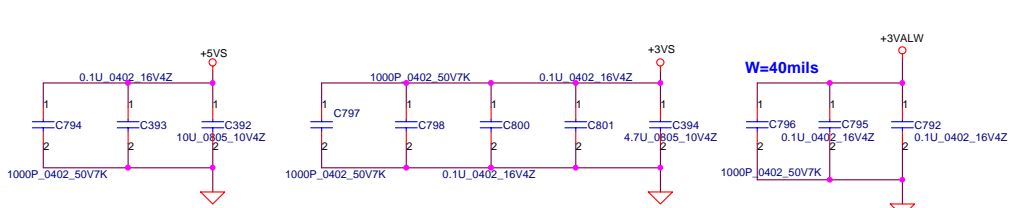
unpop when use BCM4401E(10/100)



GbE Transformer: GST5009 (SP050005610)  
10/100 Transformer : TST1284-LF (SP050001X10)



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Size	Document Number			Rev	
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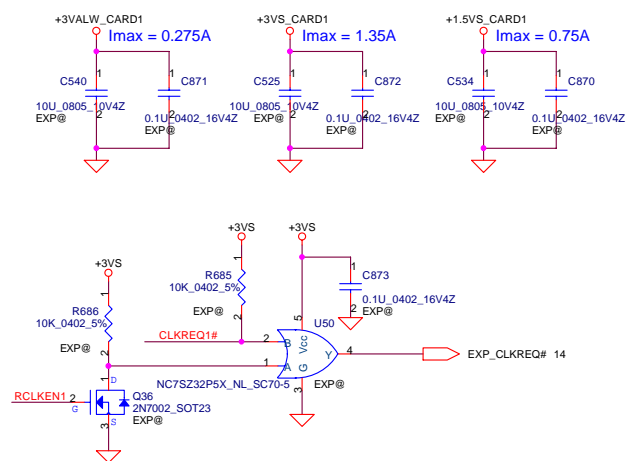
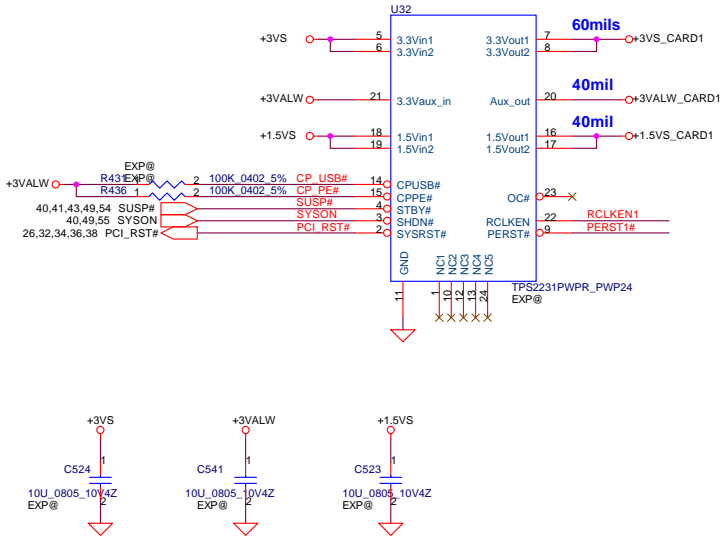


**Mini Card Power Rating**

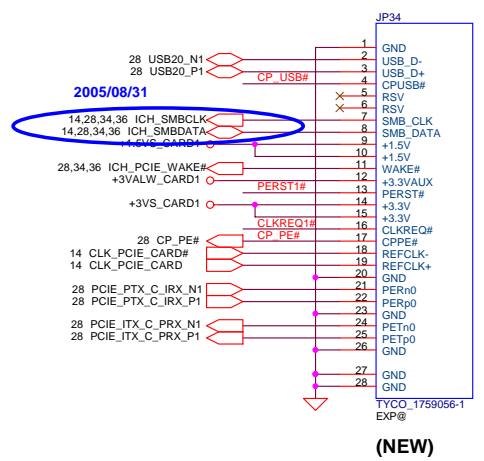
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	Normal
+3VALW	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

2005/09/27 modified.  
 Base on OPTION GTM351E Datasheet Rev0.1  
**Vcc 3.3V +/- 8%**  
**Peak Icc 2750mA**  
**with max supply droop 50mA**  
**Average Icc 1000mA**

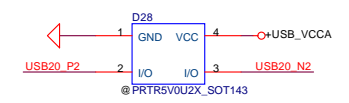
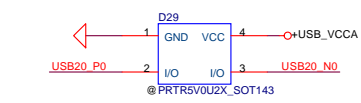
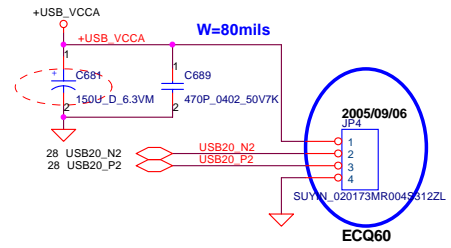
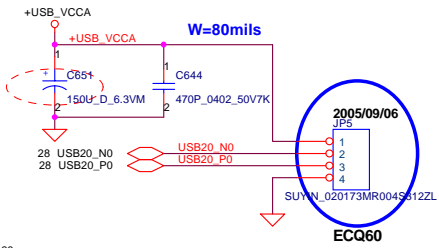
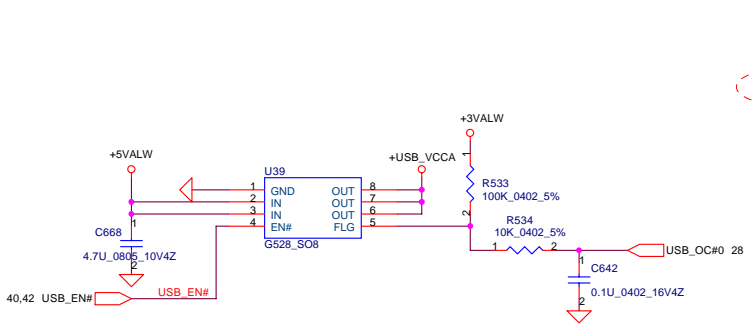
# New Card Power Switch



# New Card Socket (Left)



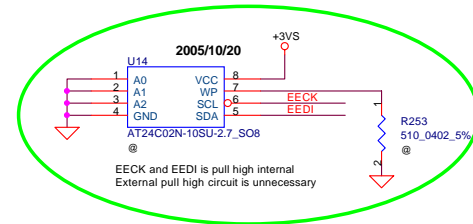
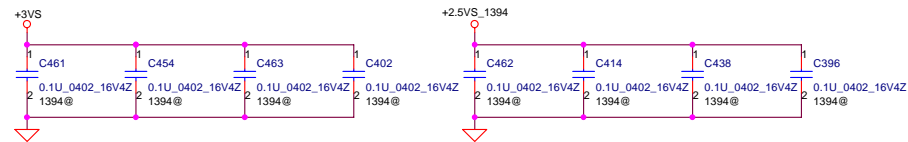
# USB CONN. 1 & 2



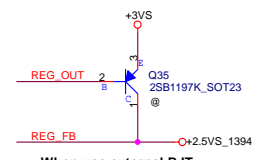
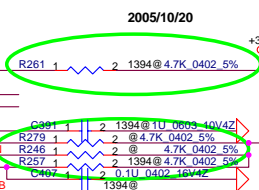
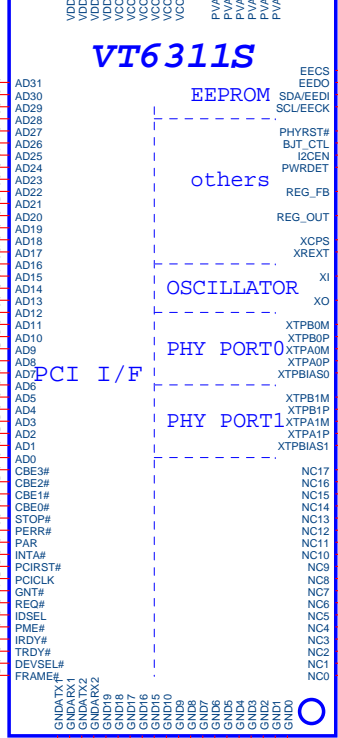
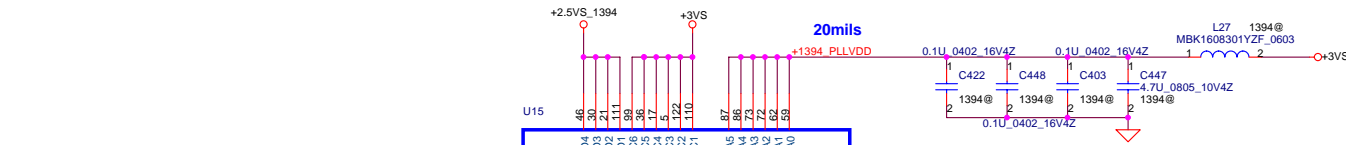
SUYIN\_020173MR004G533ZR\_4P

SUYIN\_020173MR004G533ZR\_4P

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Size	Document Number		Rev	
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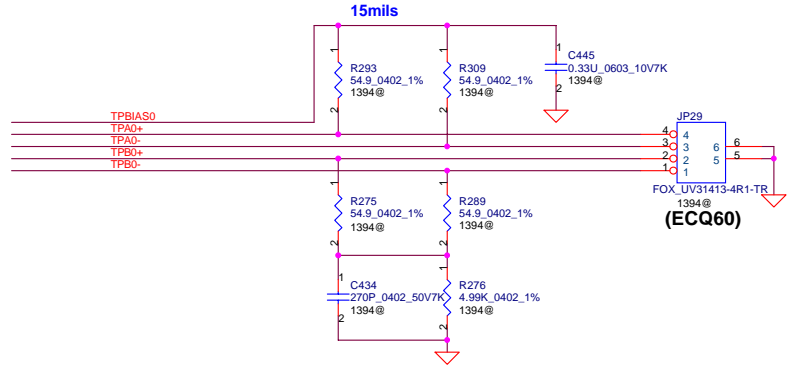
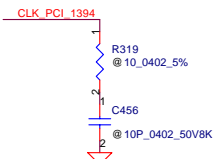
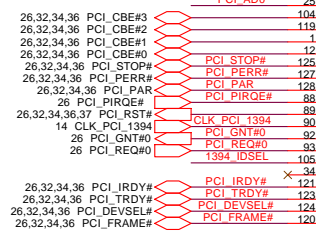
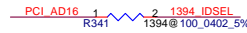
When use external EEPROM  
Populate U14, R246, R253  
Un-populate R261



When use external BJT  
Populate Q35, R279



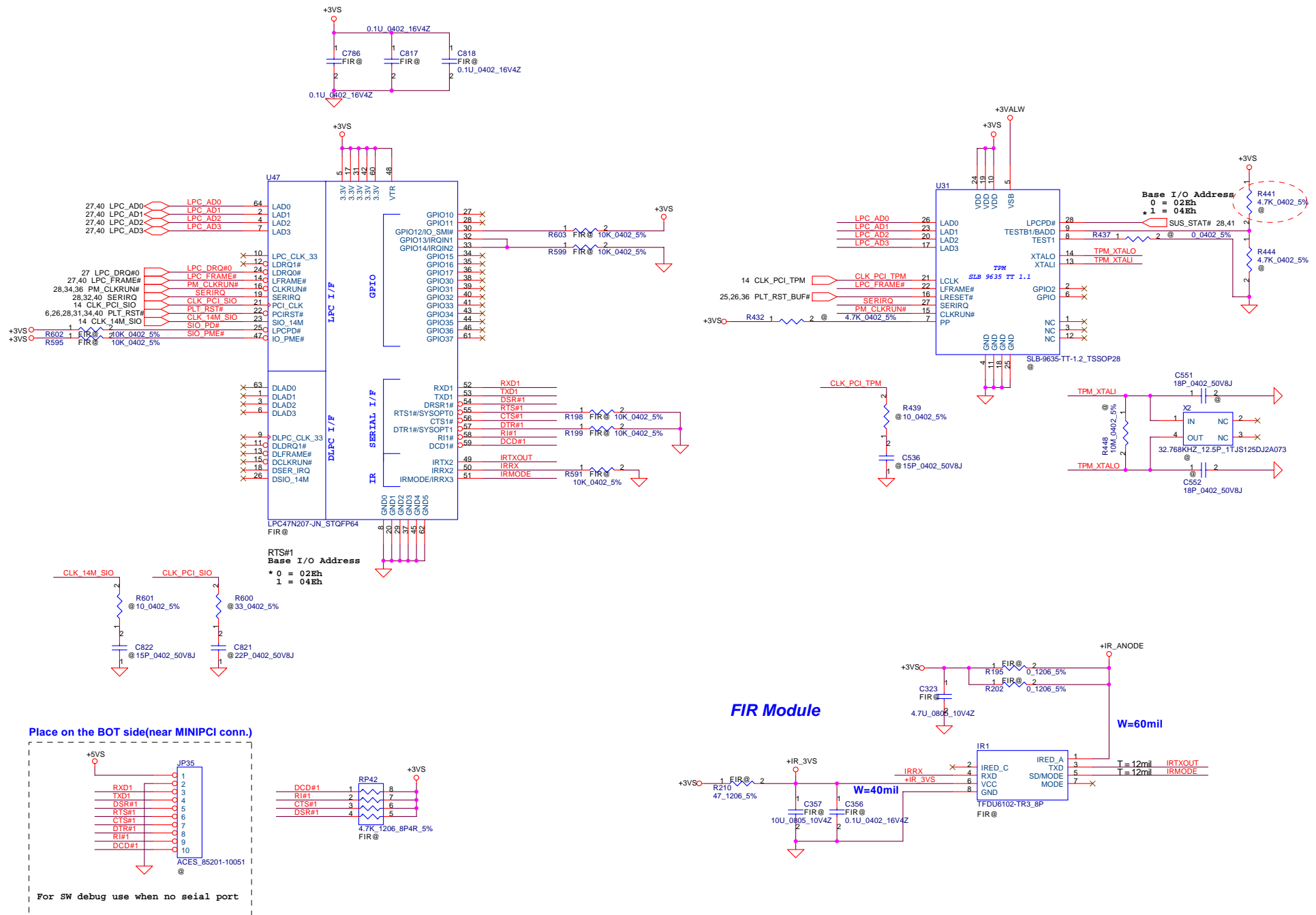
IDSEL:PCI\_AD16



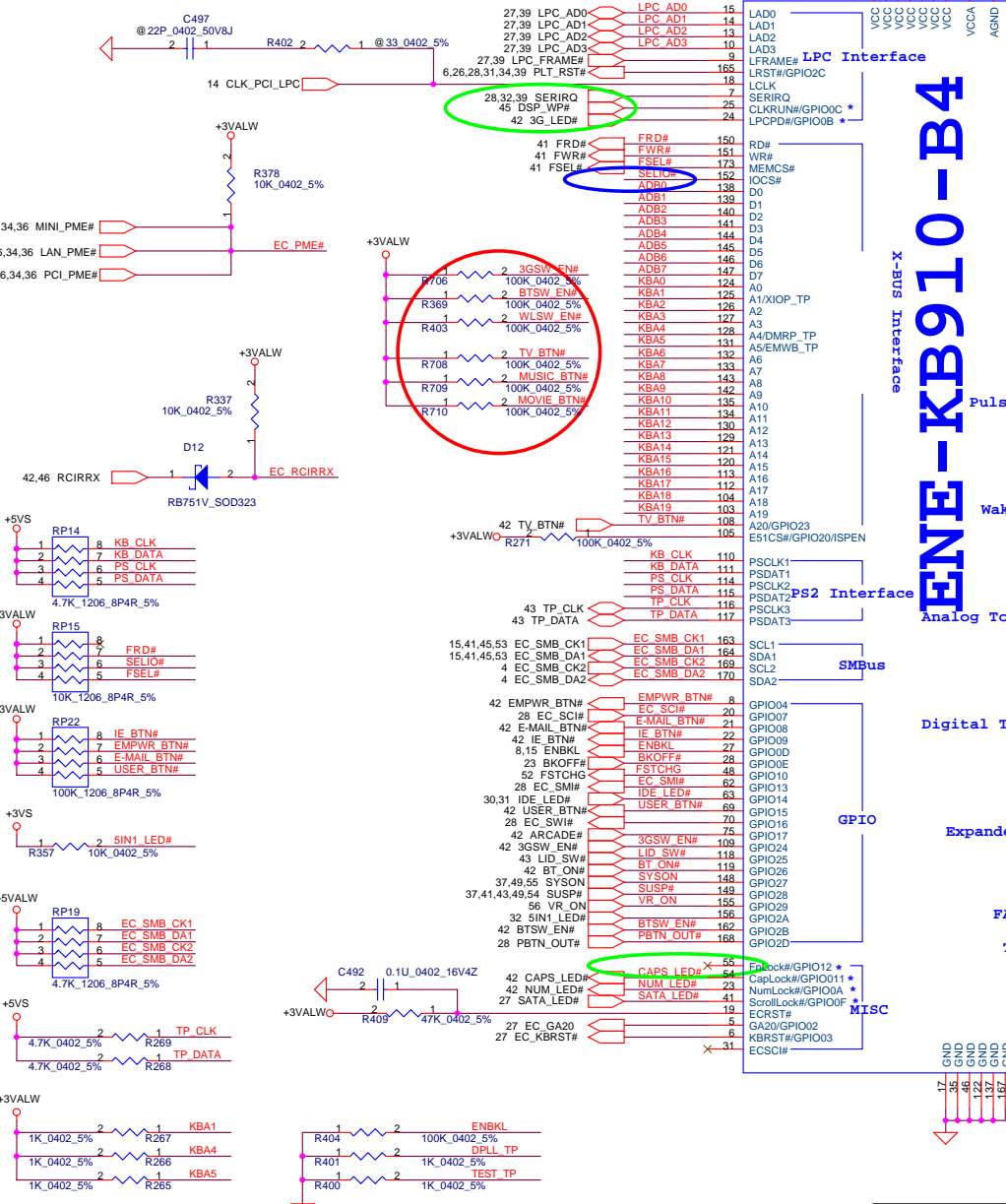
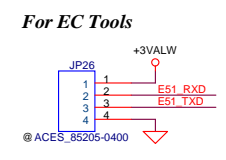
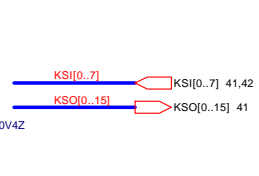
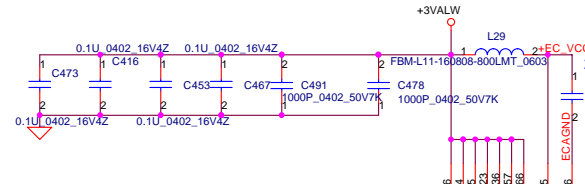
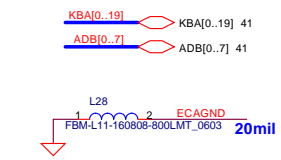
(ECQ60)

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# SUPER I/O SMsC LPC47N207



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**ENE-KB910-B4**

**Internal Keyboard**

**Wake Up Pin**

**Analog To Digital**

**Digital To Analog**

**Expanded I/O**

**FAN**

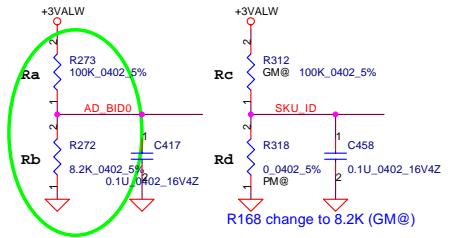
**Timer Pin**

**MISC**

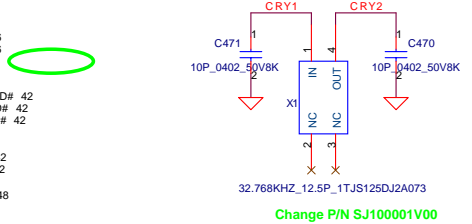
KB910Q B4\_LQFP176

Analog Board ID definition,  
Please see page 3.

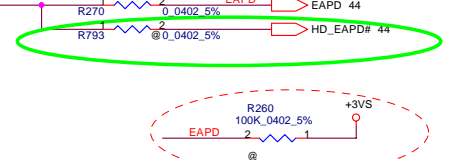
SKU ID definition,  
Please see page 3.



R168 change to 8.2K (GM@)

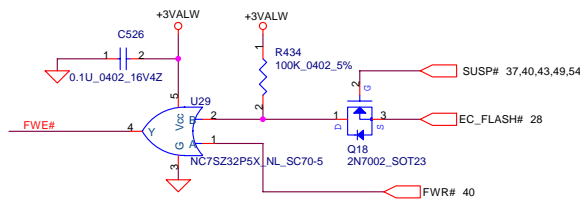


Change P/N SJ100001V00

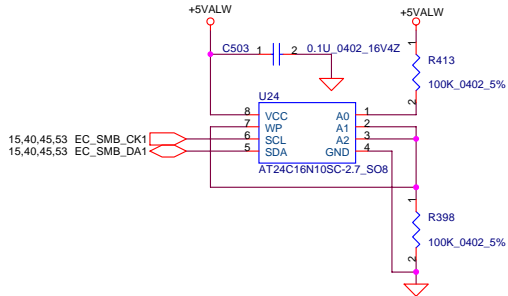


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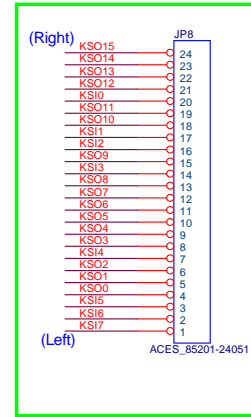
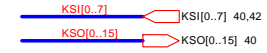




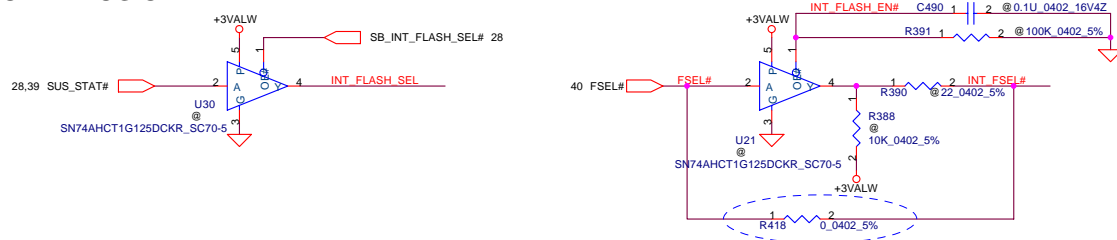
Check PCB Footprint



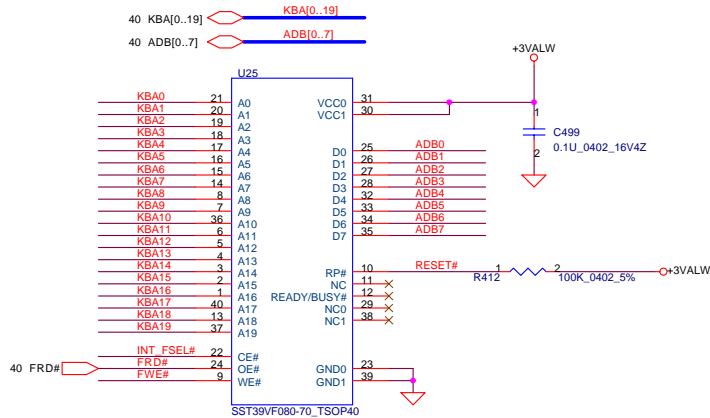
INT\_KBD Conn.



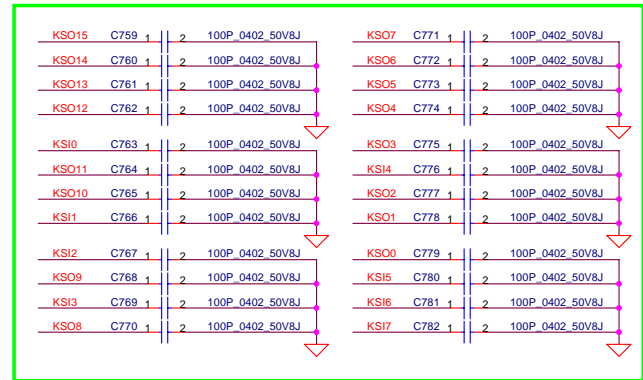
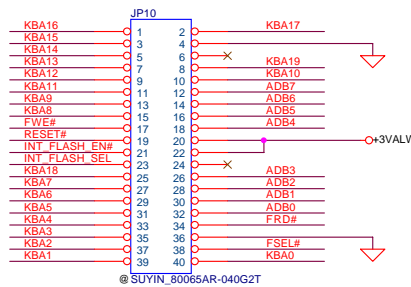
FOR DEBUG ONLY



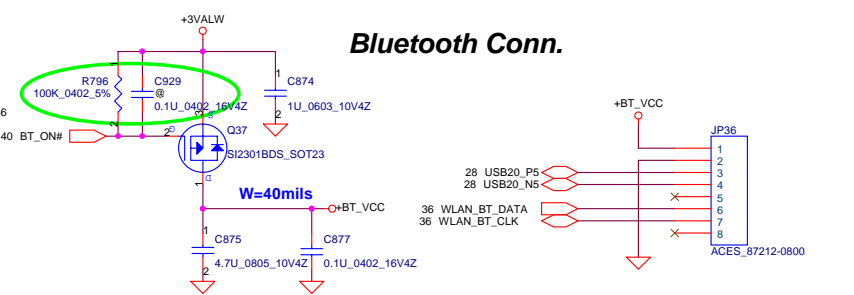
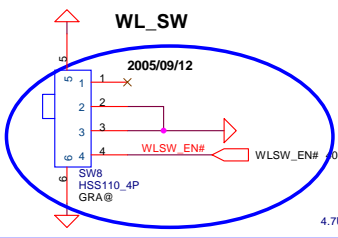
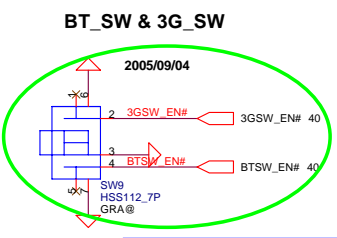
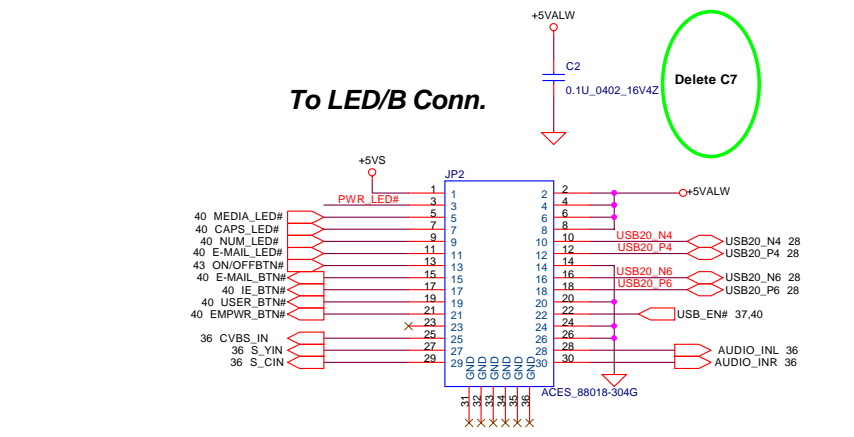
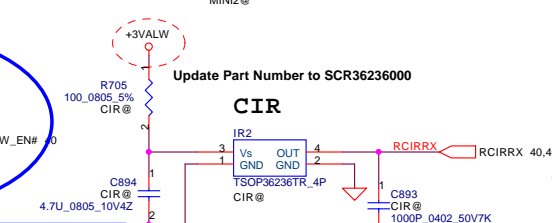
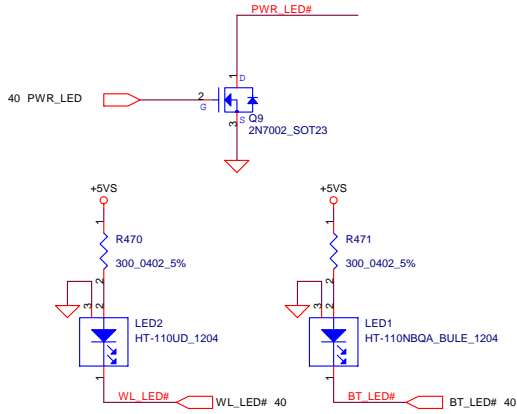
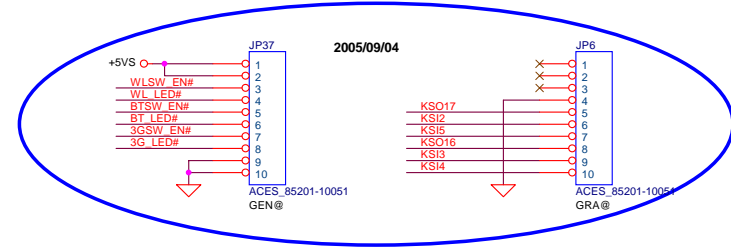
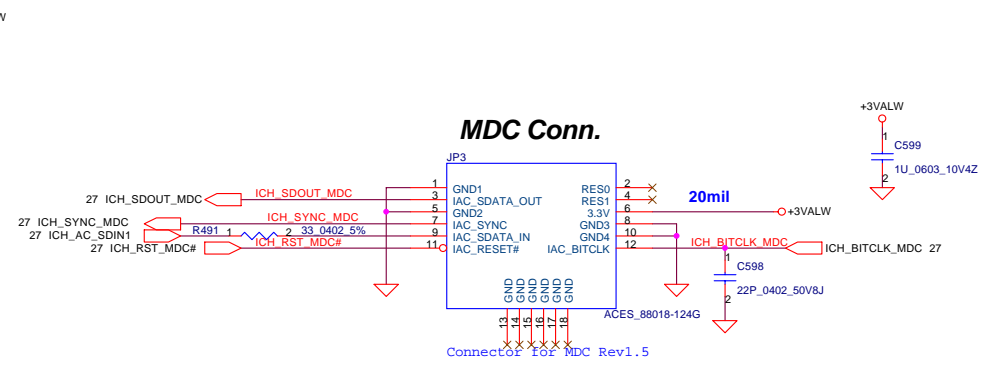
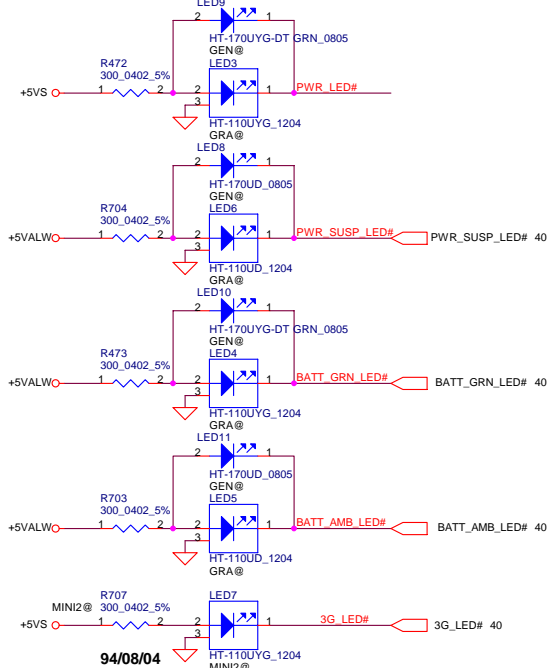
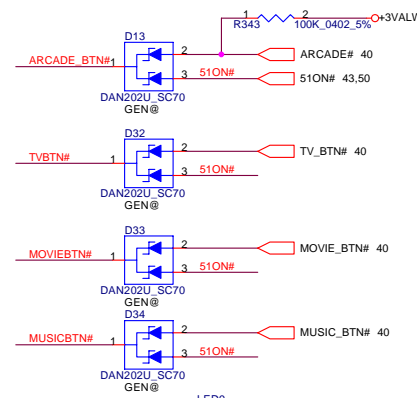
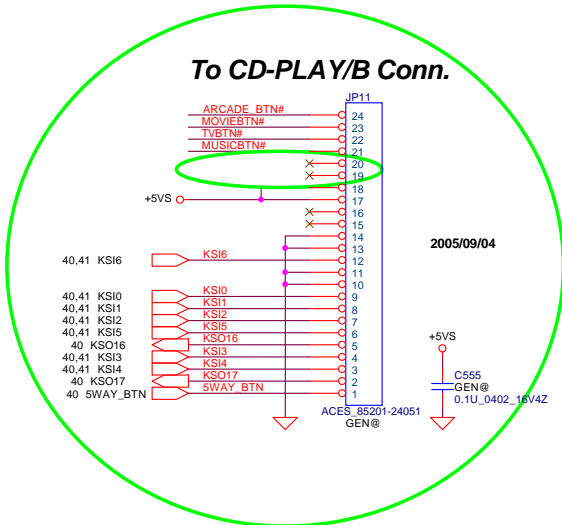
1MB Flash ROM



1MB ROM Socket

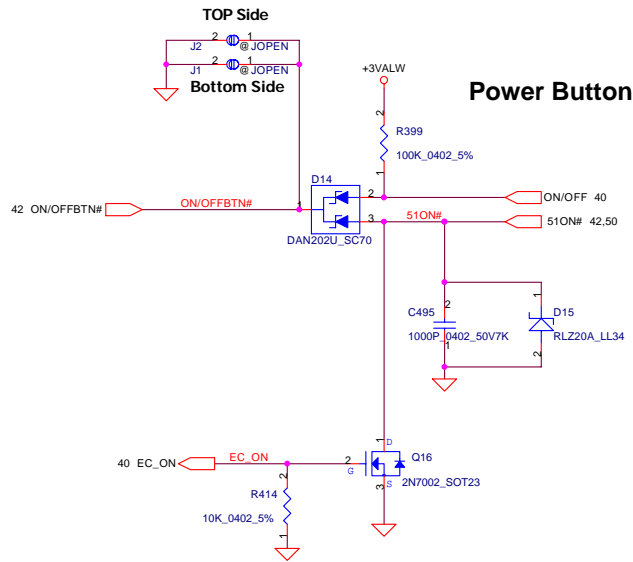


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Size	Document Number	Rev.		Date:	
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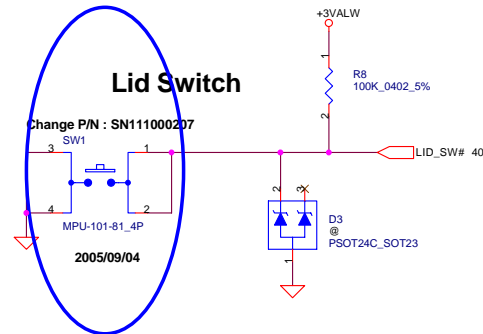
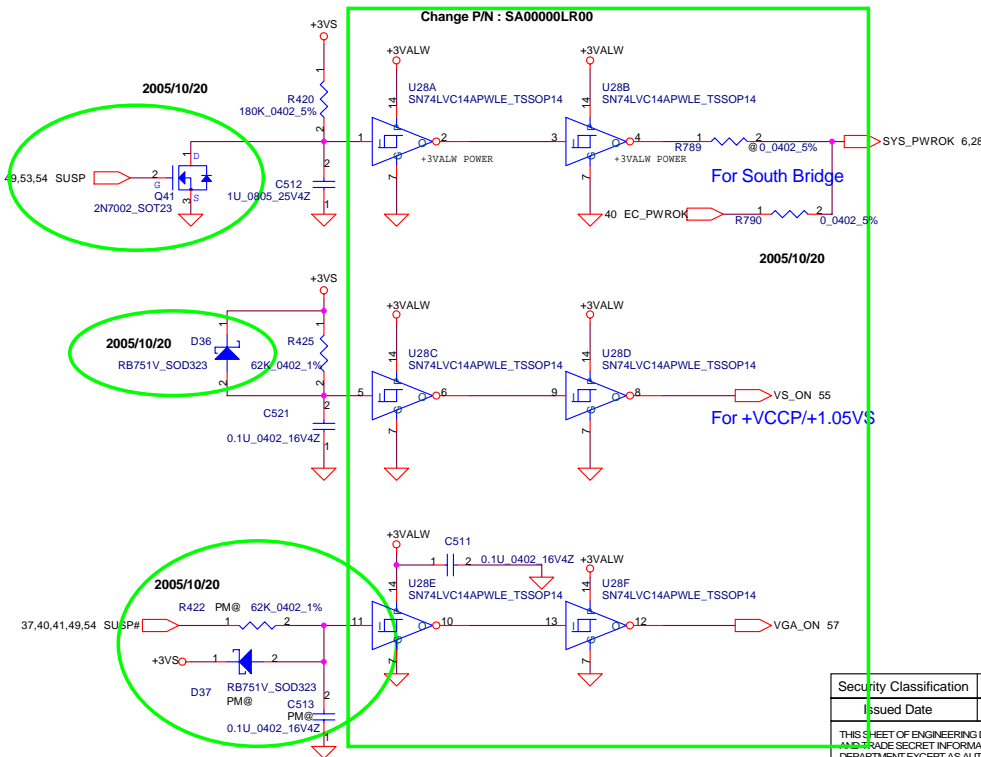


Geneva		Grapevine	
KSO10	KSO16	KSO16	KSO17
KSI0	VOL_UP		
KSI1	RIGHT		
KSI2	PLAY	KSI2	PLAY
KSI3	STOP	KSI3	STOP
KSI4	NEXT	KSI4	NEXT
KSI5	REV	KSI5	REV
KSI6			ARCANE_TV
			ARCANE_TV

**ON/OFF switch**

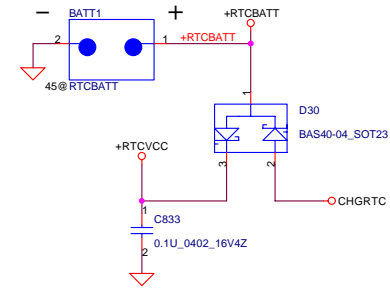


**Power ON Circuit**

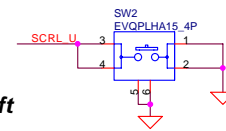


Change BATT1 P/N : SP093PA0200 (Panasonic)  
SP093MX0000 (MAXELL)

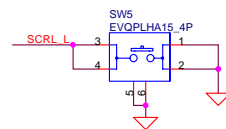
**RTC Battery**



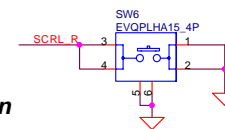
**Scroll Up**



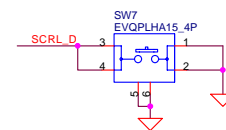
**Scroll Left**



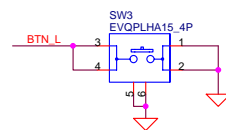
**Scroll Right**



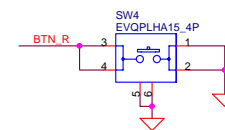
**Scroll Down**



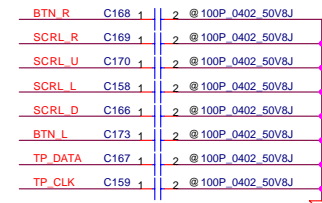
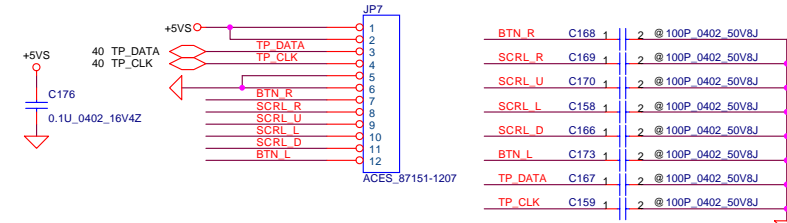
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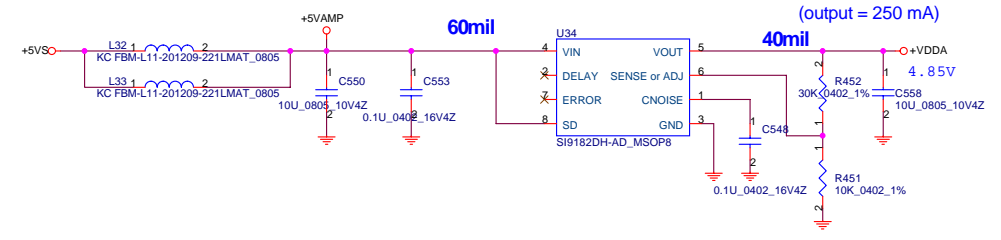
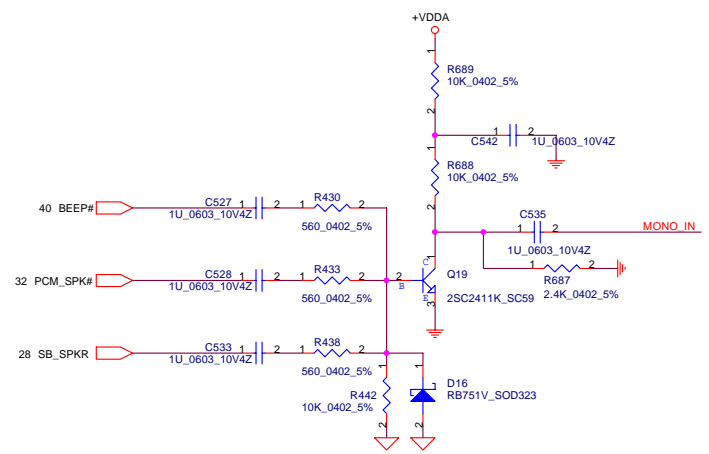
**Right**



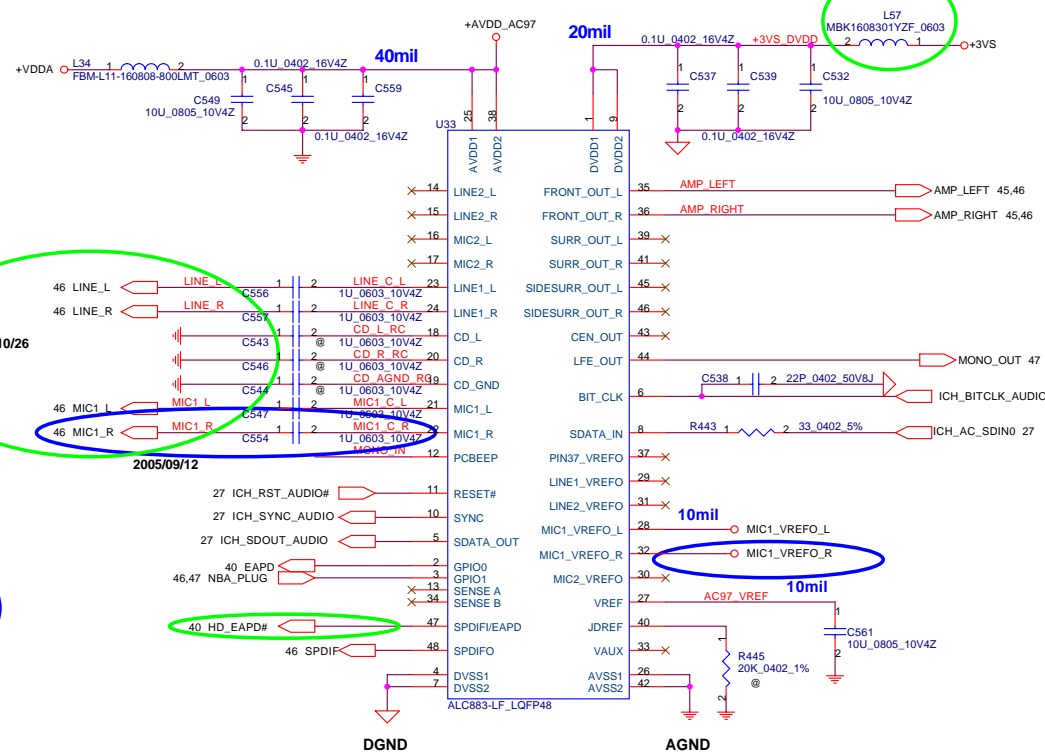
**To TP/B Conn.**



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Issued Date	2005/06/20	Deciphered Date	2006/06/20	Power OK, Reset and RTC Circuit, TP
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Date: Friday, November 11, 2005				Sheet 43 of 59

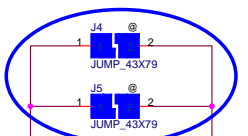


### HD Audio Codec

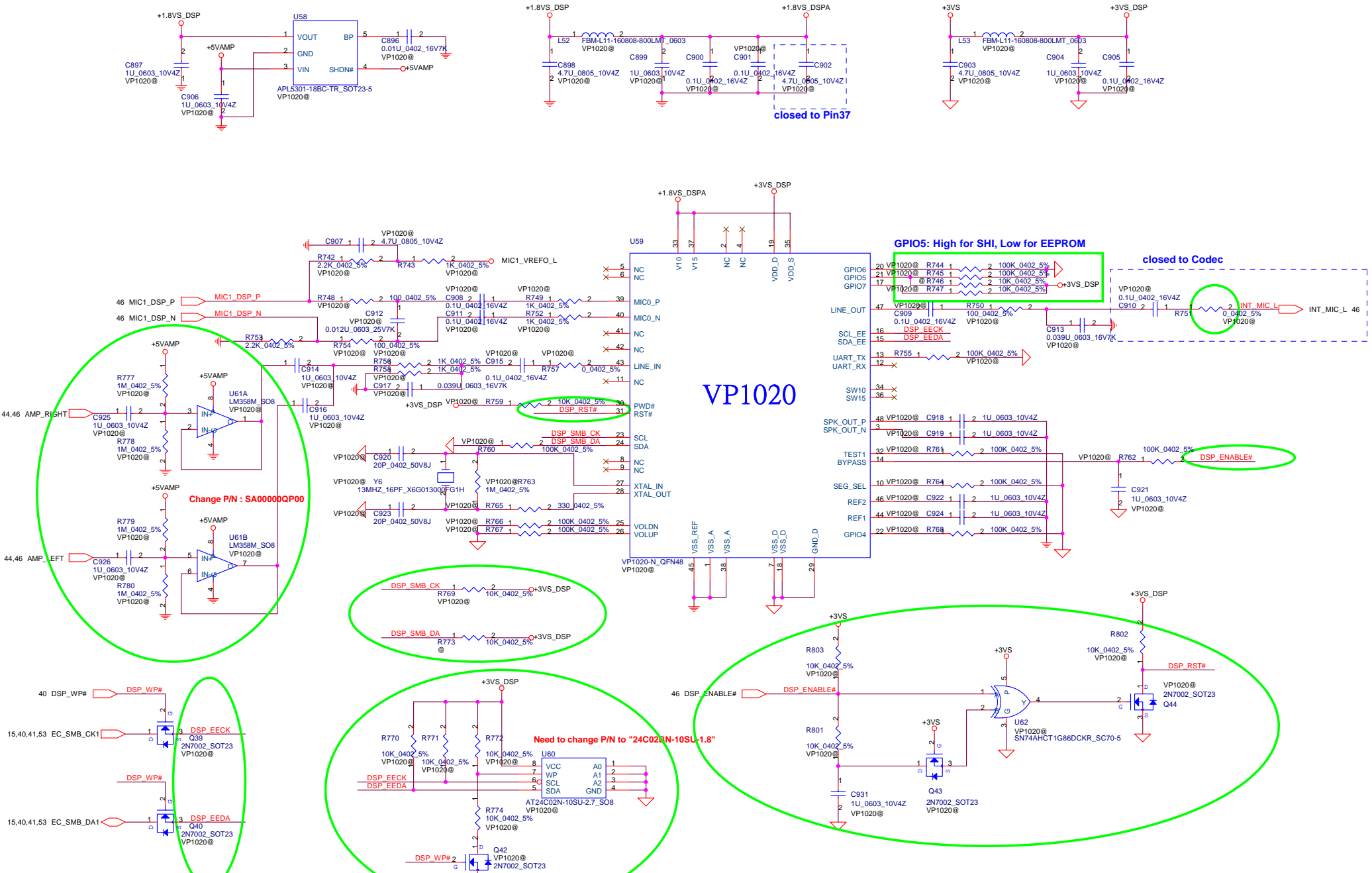


2005/10/26

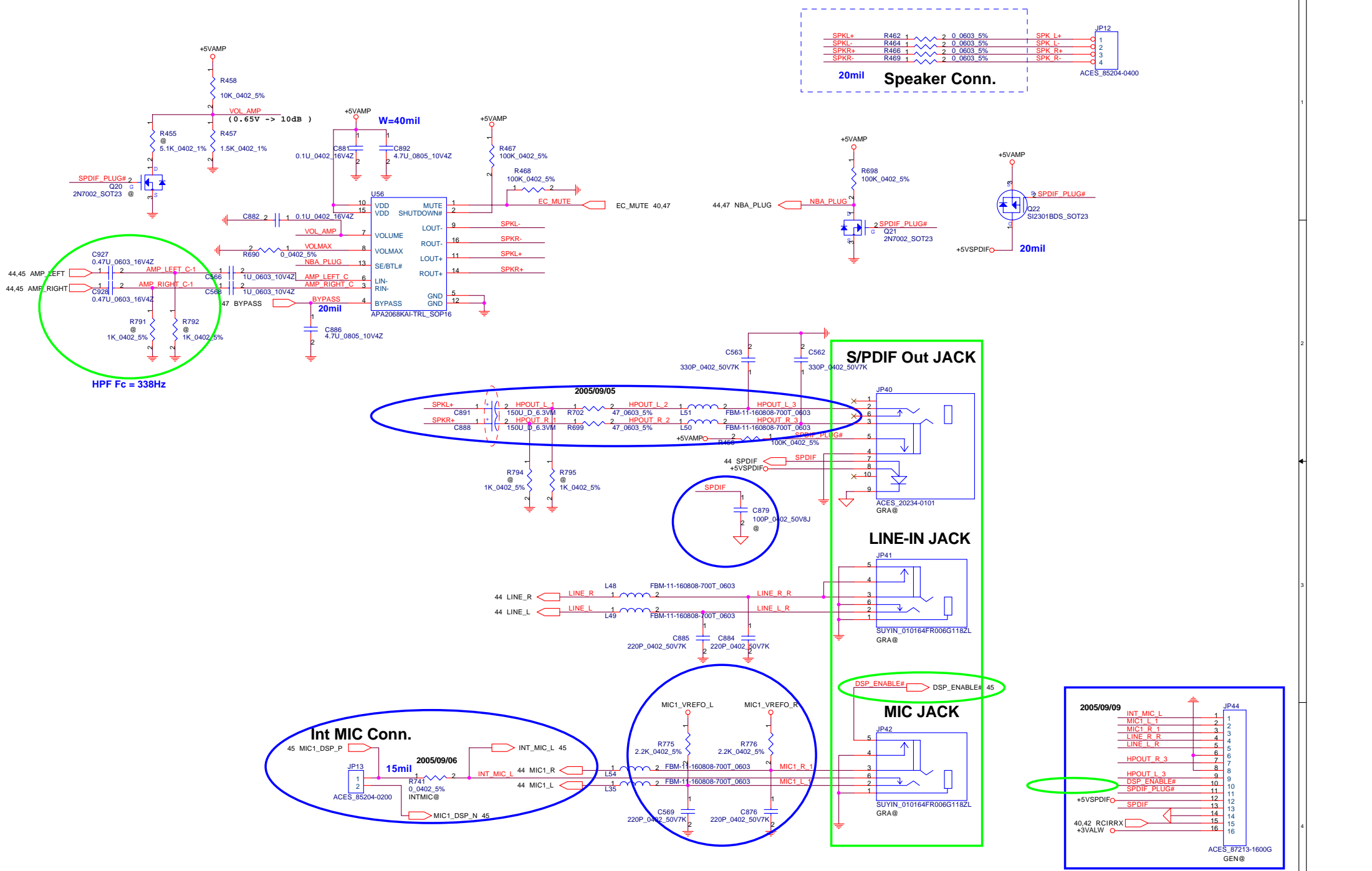
2005/09/12



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Size B	Document Number	Rev		
	HBL50 LA-2921P	0.3		
Date:	Friday, November 11, 2005	Sheet	44	of 59

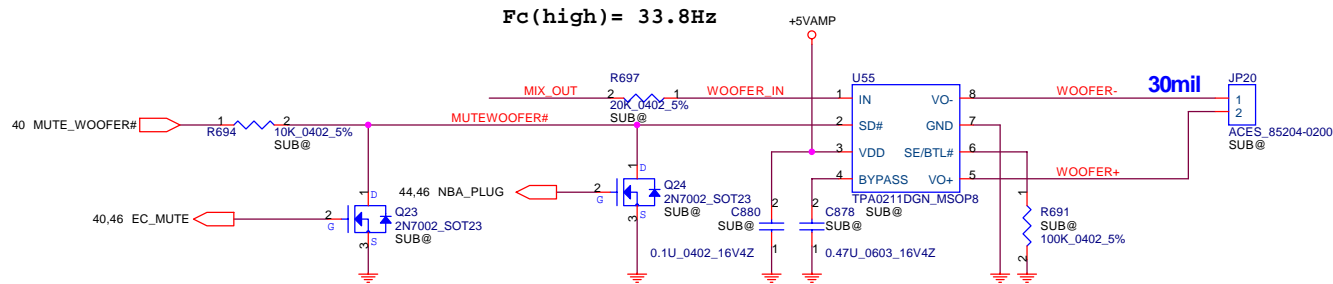
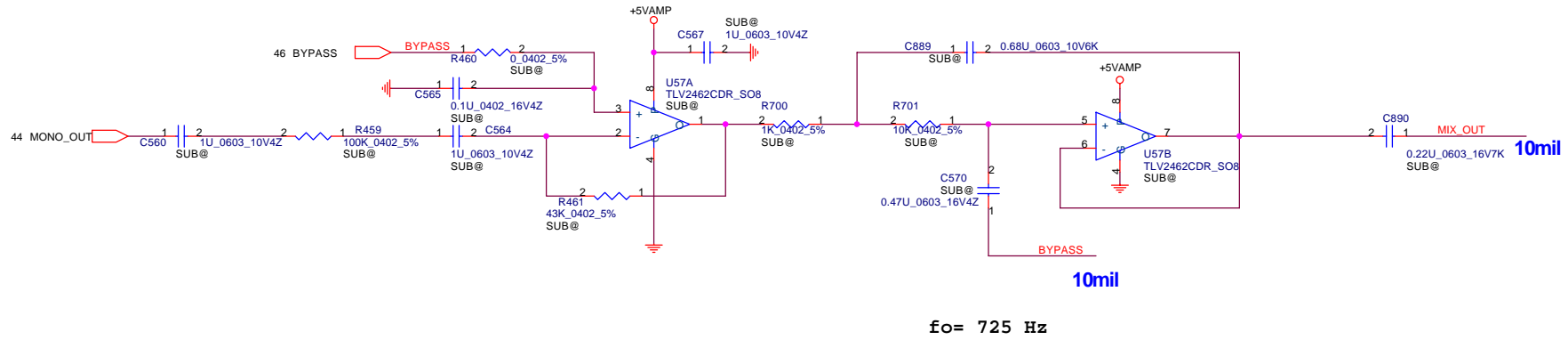


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Issued Date	2005/06/20	Deciphered Date	2006/06/20	Echo Cancellation	
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				Date: Friday, November 11, 2005	Sheet 45 of 59



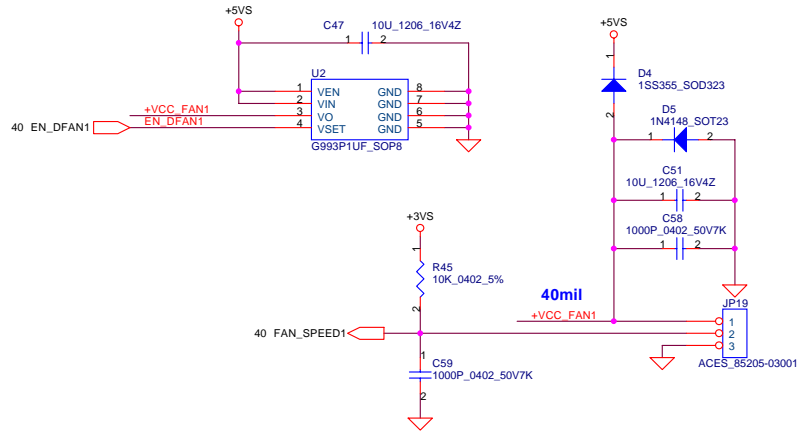
Security Classification		Compal Secret Data	
Issued Date	2005/06/20	Deciphered Date	2006/06/20
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Compal Electronics, Inc.			
Title Amplifier & Audio Jack			
Size B	Document Number HBL50 LA-2921P	Rev 0.3	
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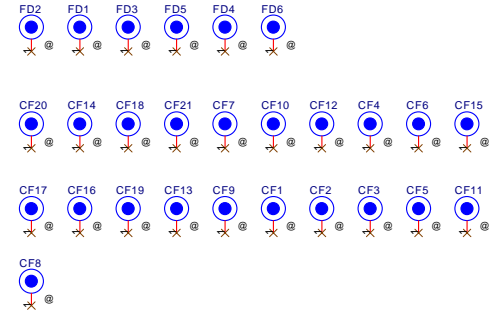
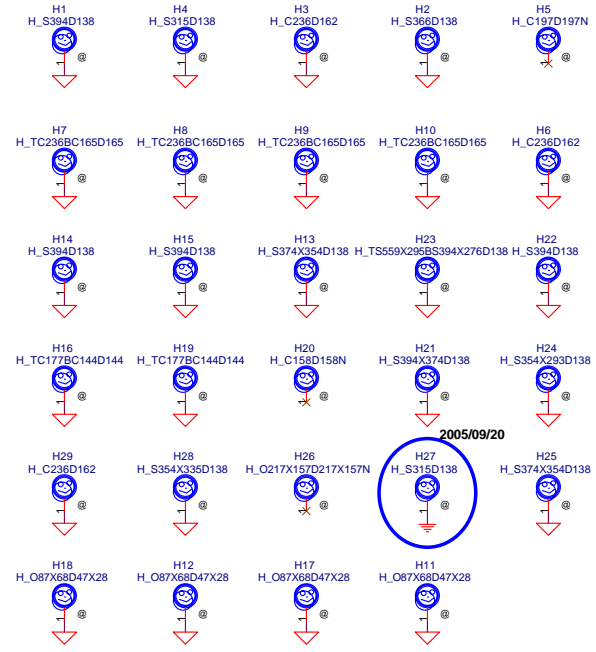
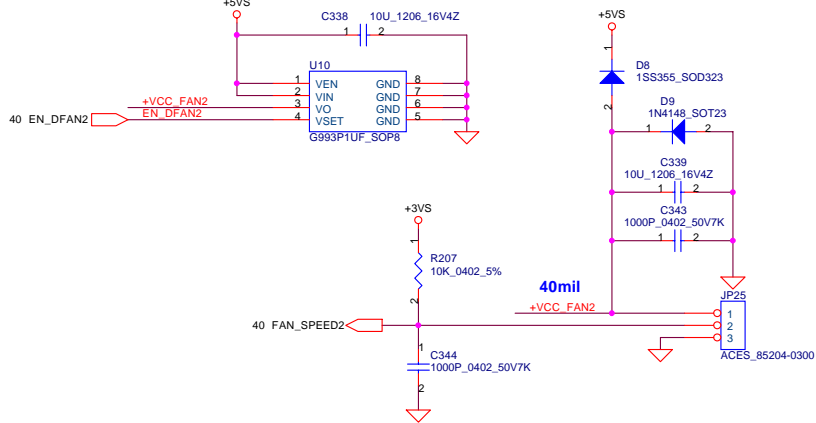


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Issued Date	2005/06/20	Deciphered Date	2006/06/20	Title	
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Size	Document Number			Rev	
B	HBL50 LA-2921P			0.3	
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### FAN1 Conn

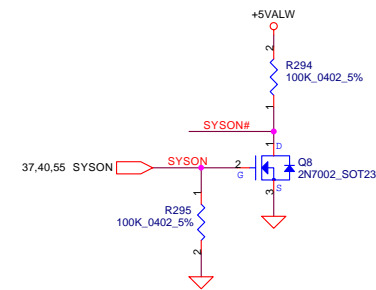
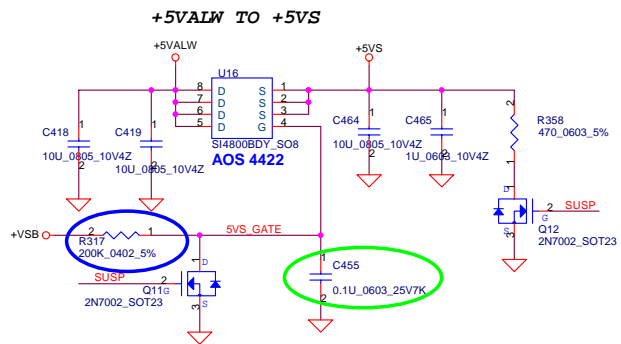


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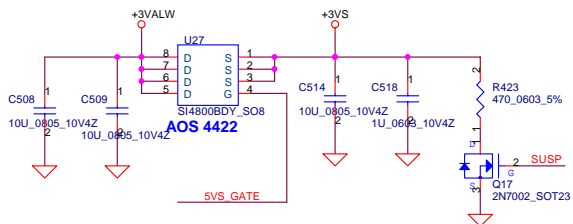


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Issued Date	2005/06/20	Deciphered Date	2006/06/20	Title	
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Size	B	Document Number	HBL50 LA-2921P	Rev.	0.3
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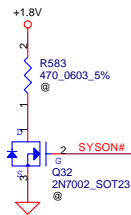
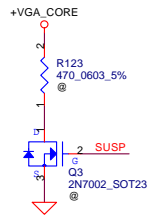
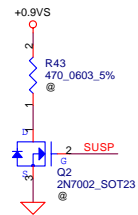
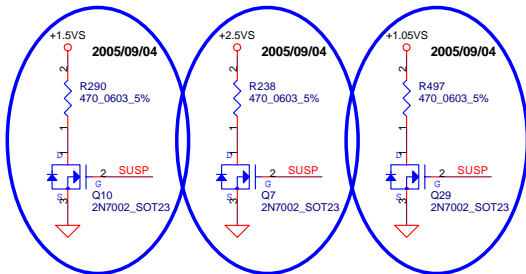
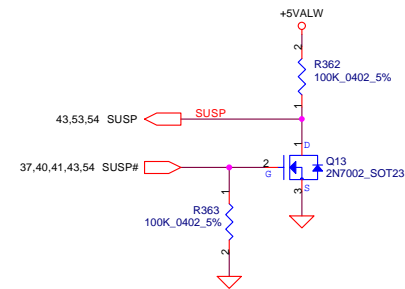
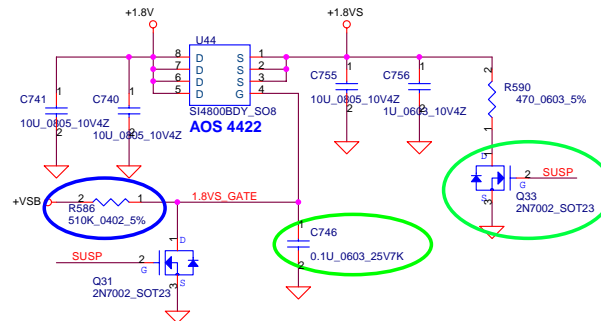




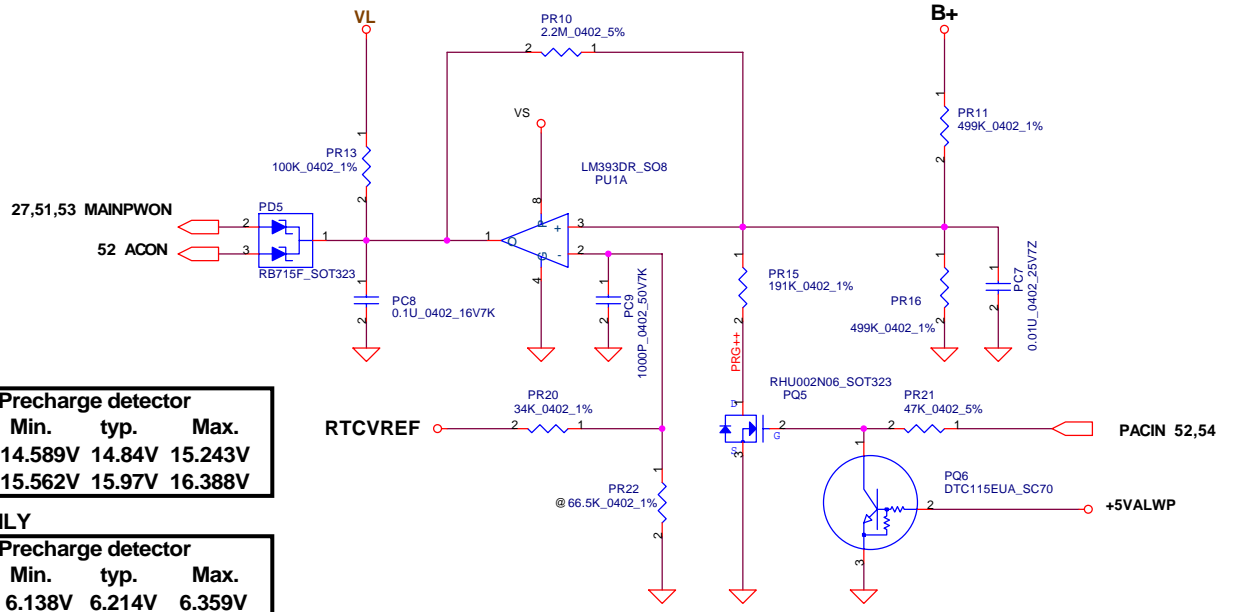
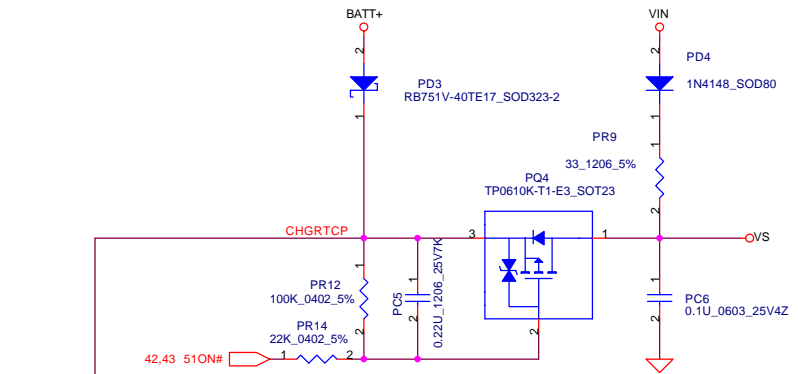
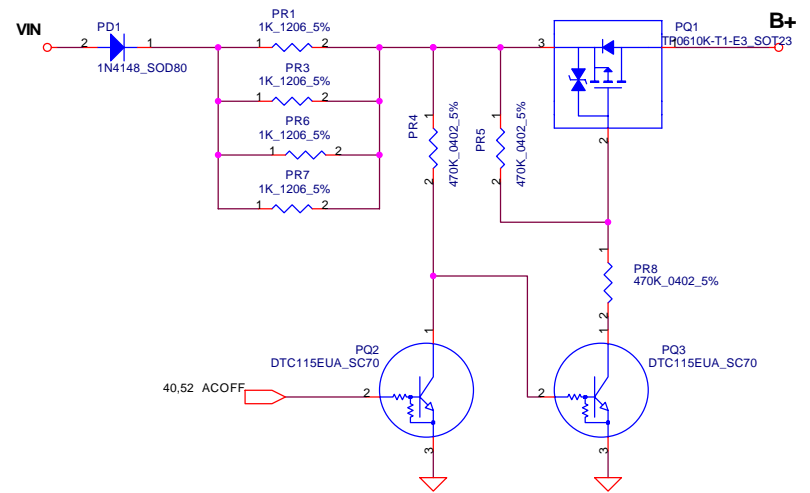
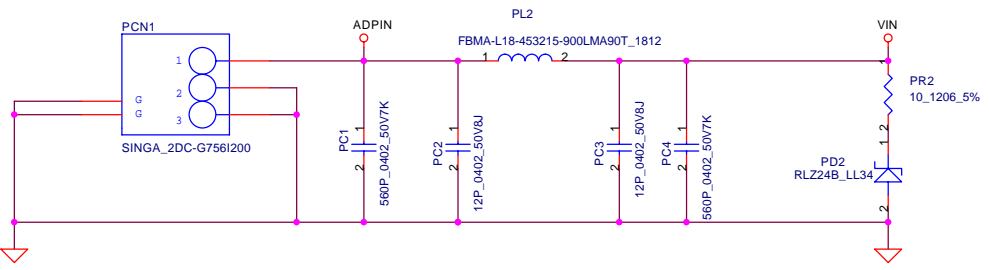
**+3VALW TO +3VS**



**+1.8V to +1.8VS**



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Issued Date	2005/06/20	Deciphered Date	2006/06/20	DC Interface
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Date: Friday, November 11, 2005				Sheet 49 of 59

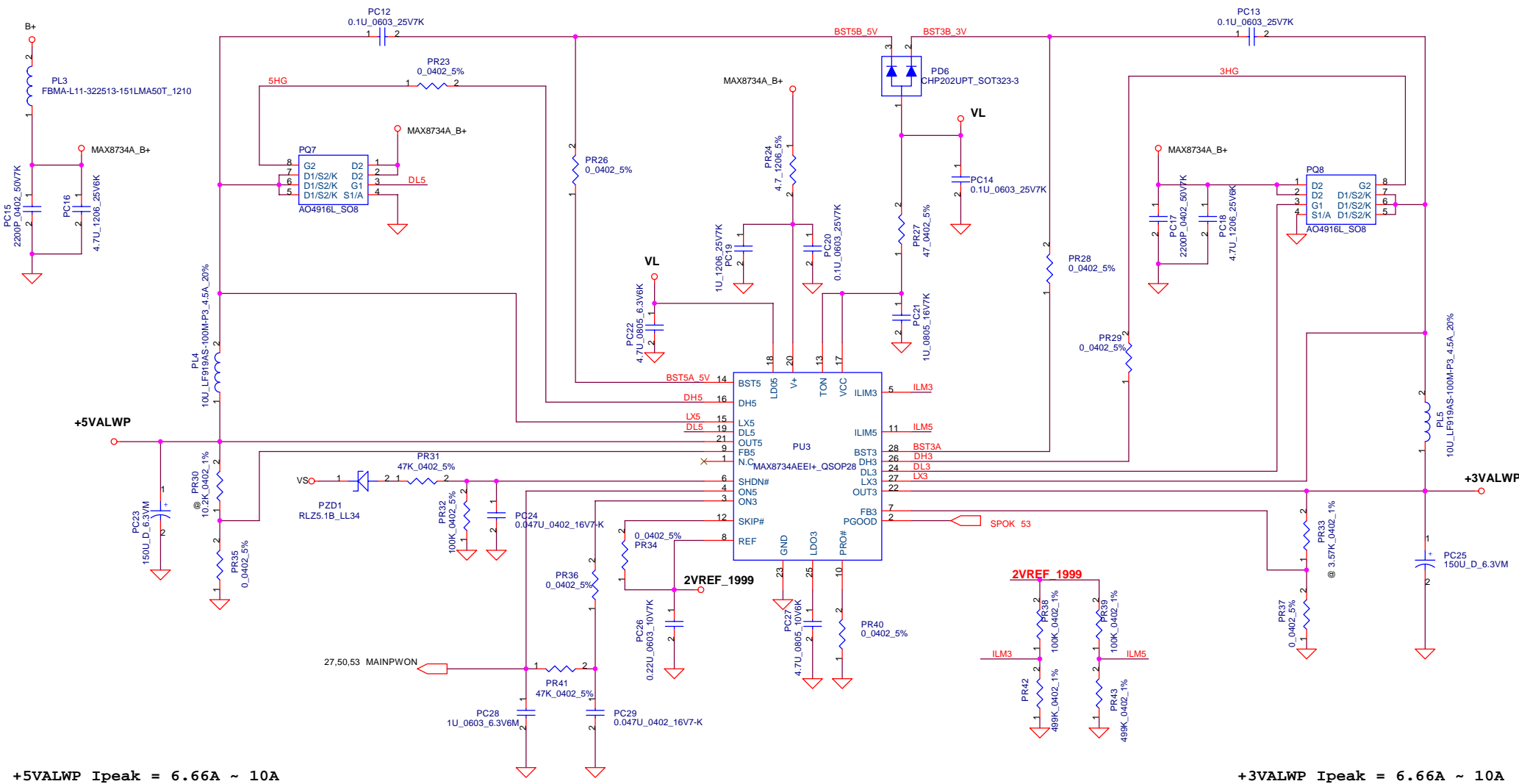


ACIN			
Precharge detector			
	Min.	typ.	Max.
H->L	14.589V	14.84V	15.243V
L->H	15.562V	15.97V	16.388V

BATT ONLY			
Precharge detector			
	Min.	typ.	Max.
H->L	6.138V	6.214V	6.359V
L->H	7.196V	7.349V	7.505V

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				HBL50 LA-2921P
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				Date: Friday, November 11, 2005
				Sheet 50 of 59

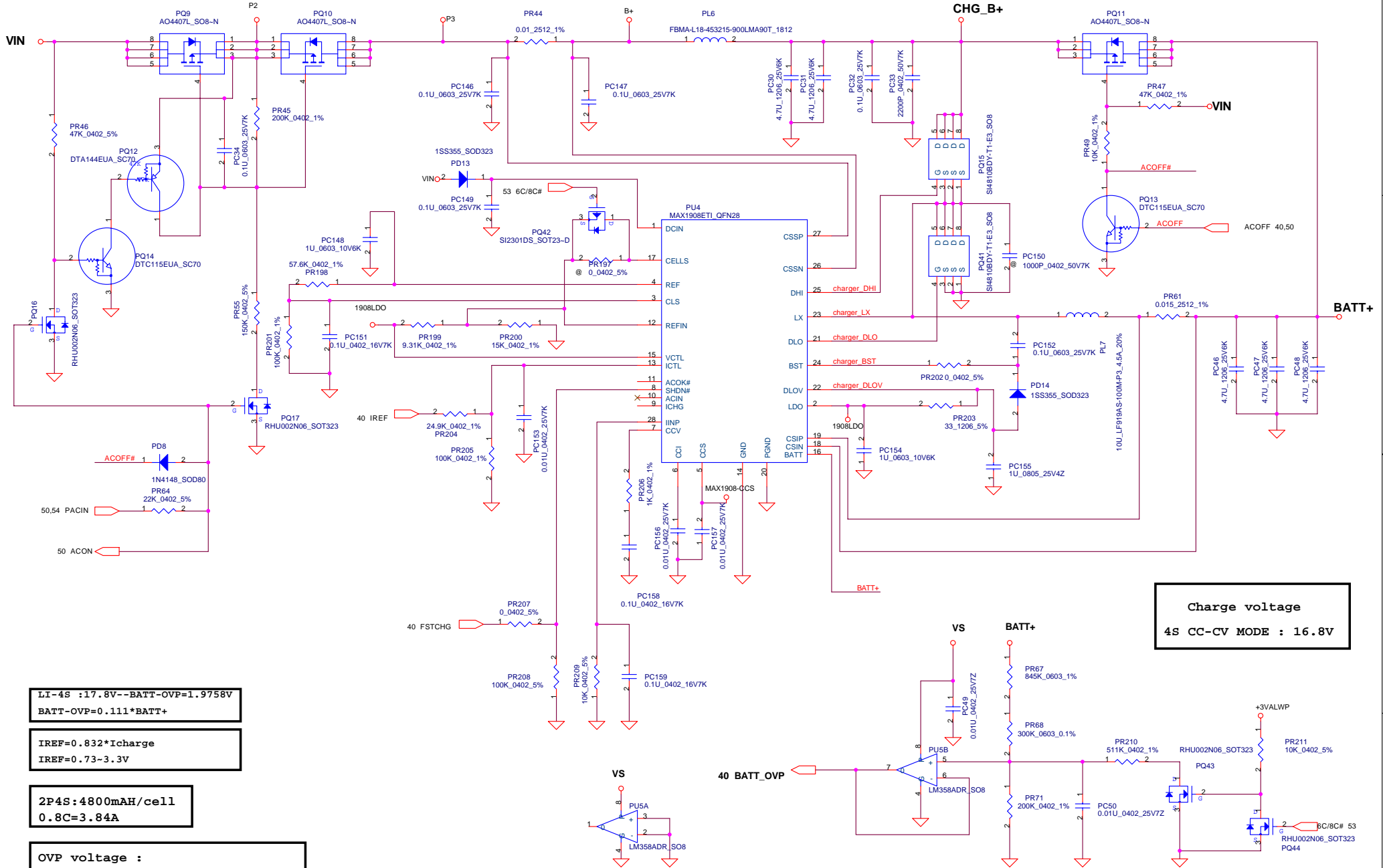


**+5VALWP Ipeak = 6.66A ~ 10A**

**+3VALWP Ipeak = 6.66A ~ 10A**

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I<sub>adp</sub>=0~4.74A(90W)



Charge voltage  
4S CC-CV MODE : 16.8V

LI-4S : 17.8V--BATT-OVP=1.9758V  
BATT-OVP=0.111\*BATT+

IREF=0.832\*Icharge  
IREF=0.73~3.3V

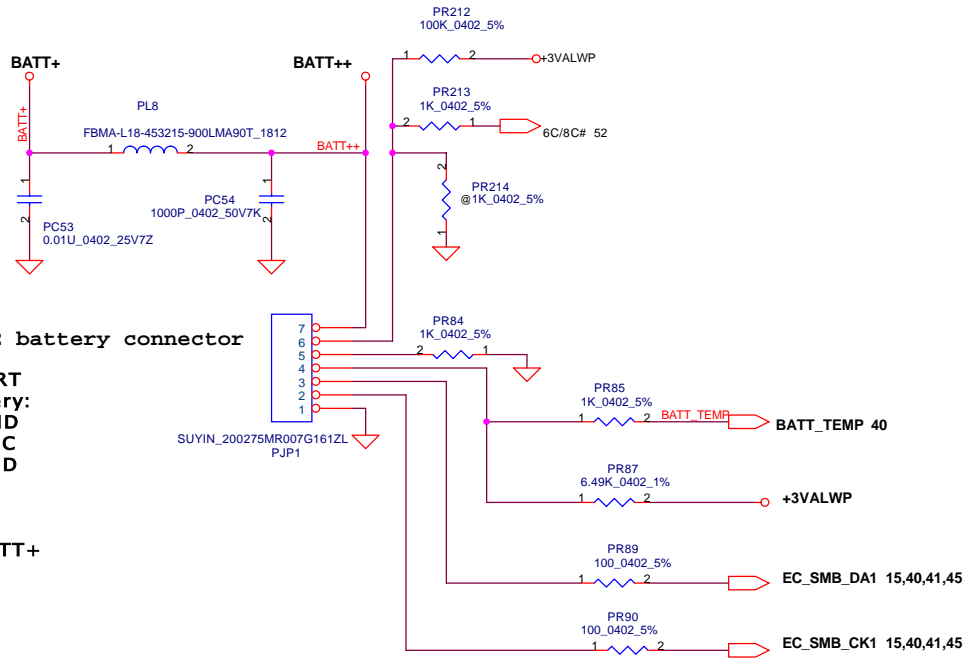
2P4S:4800mAh/cell  
0.8C=3.84A

OVP voltage :  
LI-3S : 17.8V---BATT-OVP=1.9758V  
BATT-OVP=0.111\*BATT+

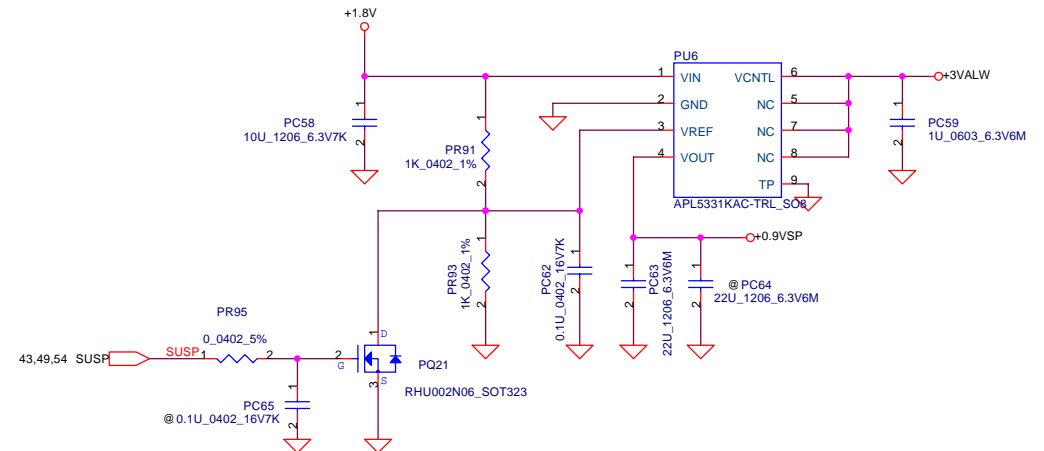
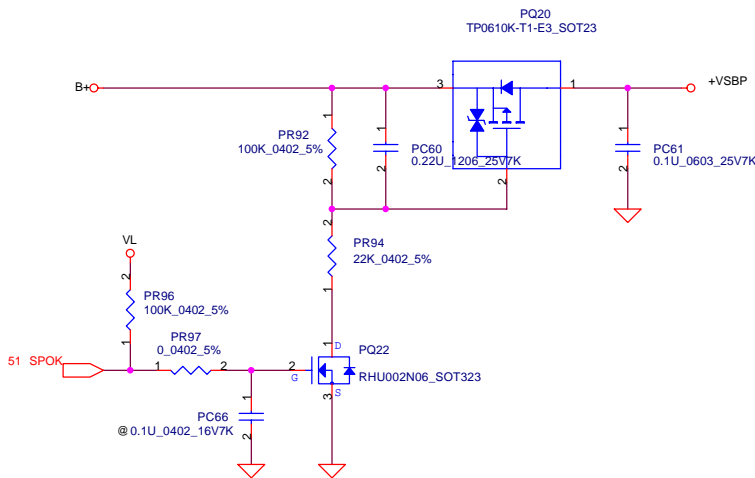
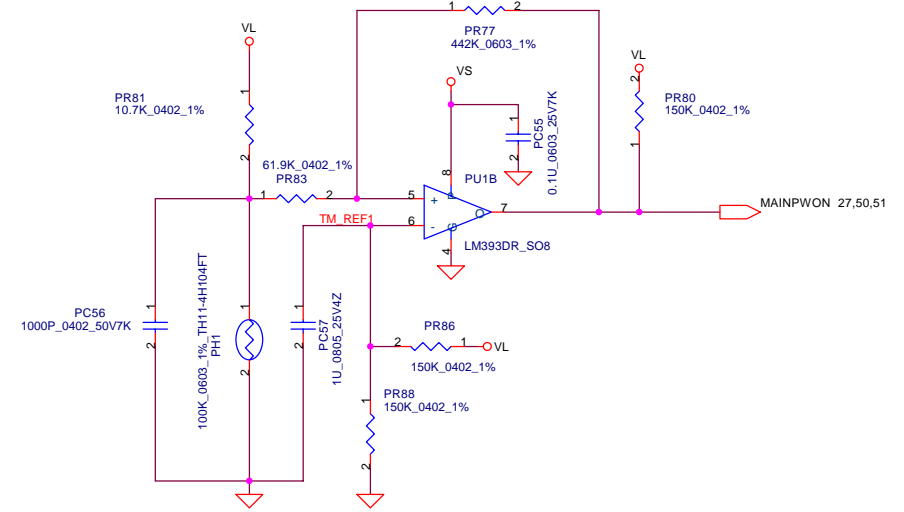
Security Classification	Compal Secret Data		Title	Compal Electronics, Inc.	
Issued Date	2005/06/20	Deciphered Date	2006/06/20	Charger	
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Size	Document Number	Rev		Date	
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**PJP2 battery connector**

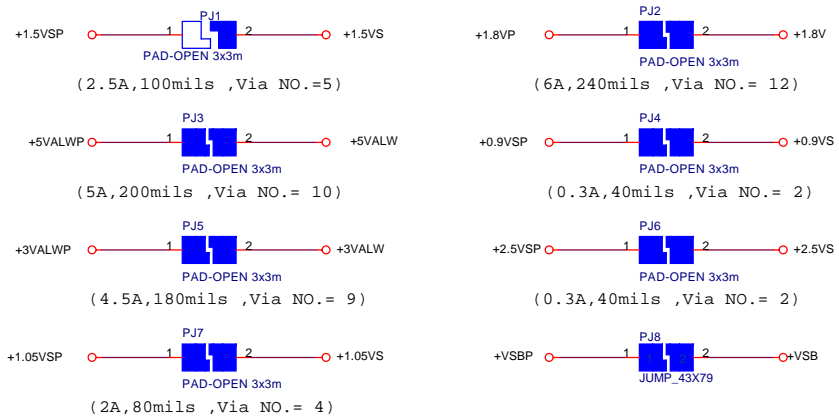
- SMART Battery:**  
 1.GND  
 2.SMC  
 3.SMD  
 4.TS  
 5.B/I  
 6.ID  
 7.BATT+



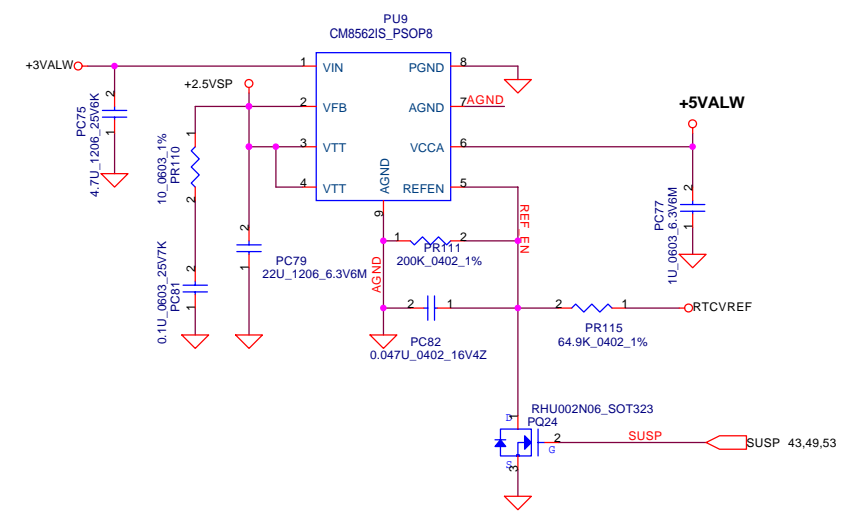
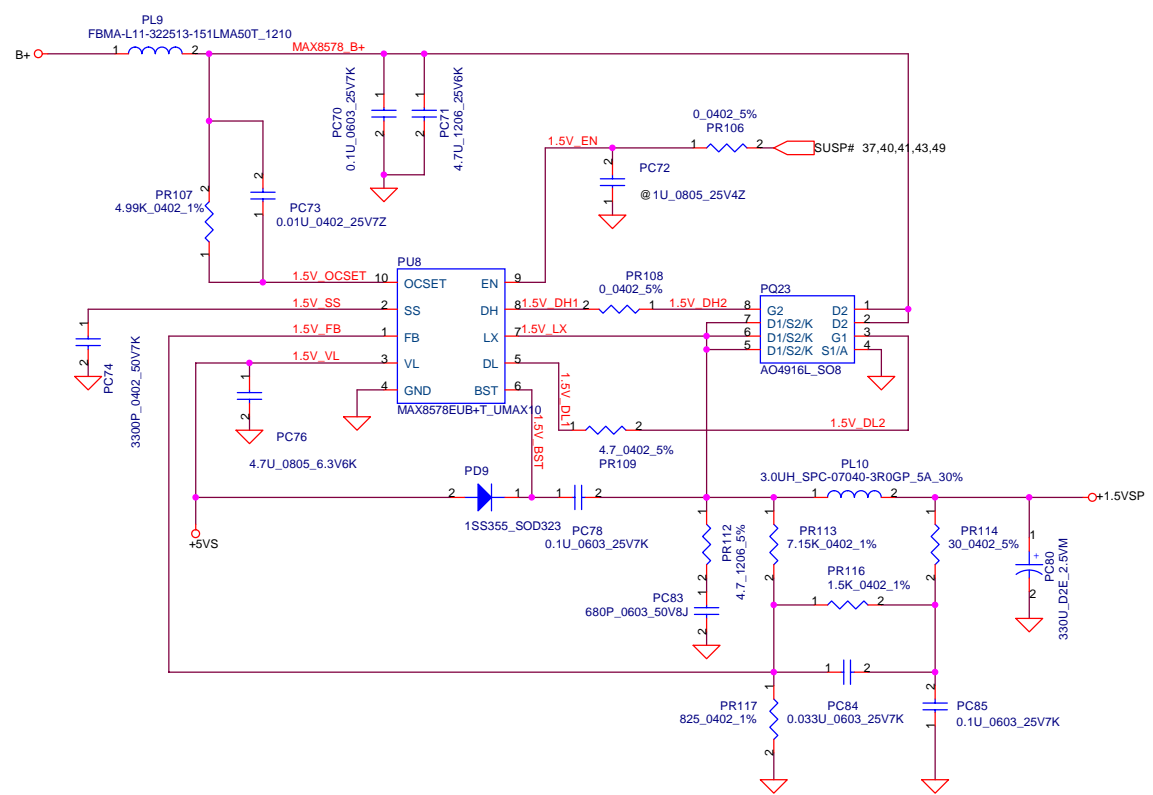
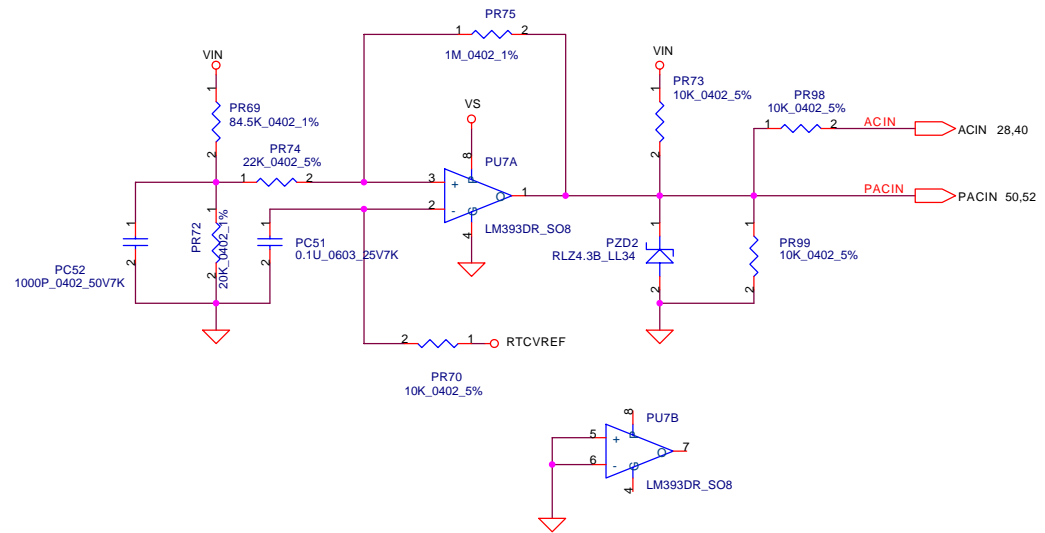
**PH1 under CPU bottom side :**  
 CPU thermal protection at 80 degree C  
 Recovery at 44(45) degree C



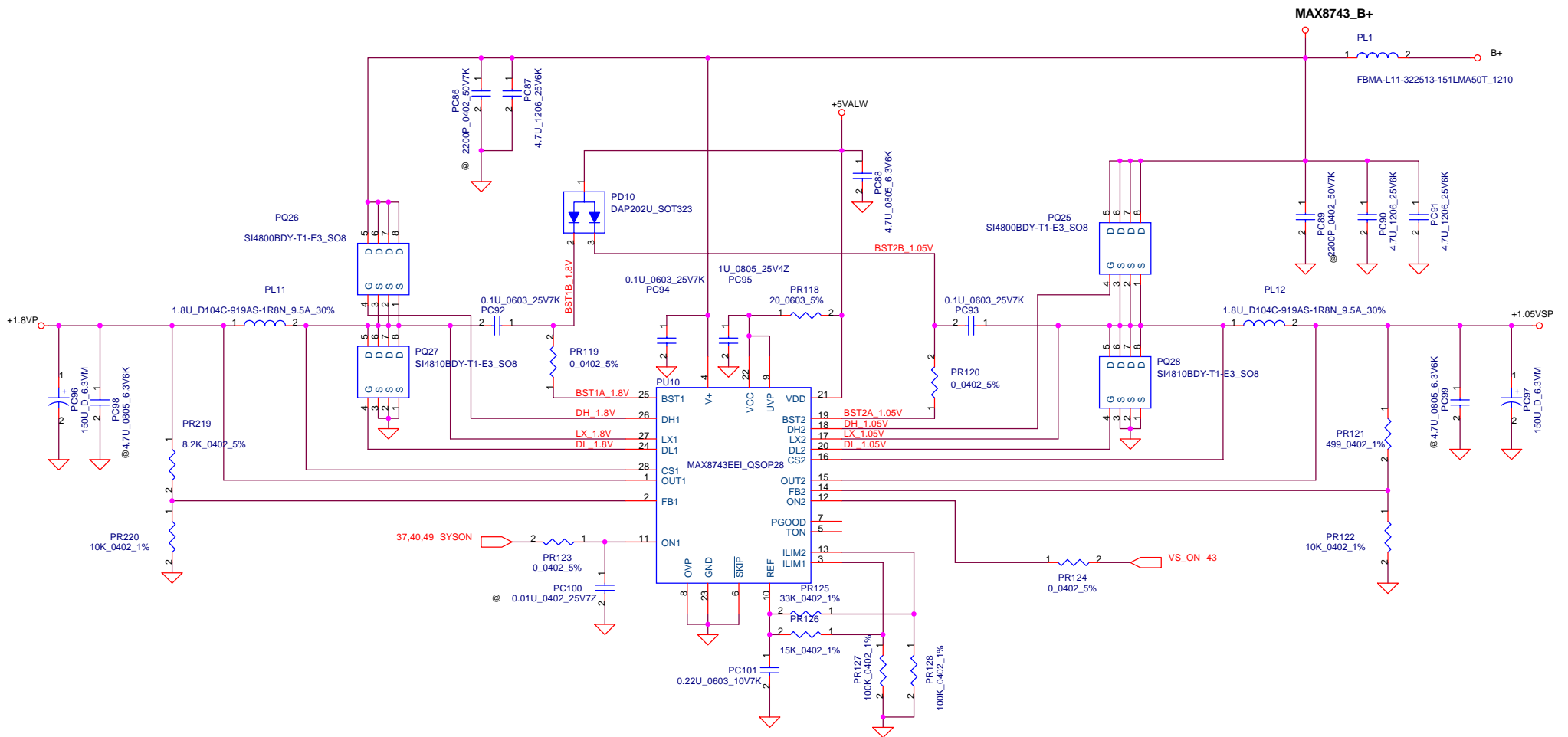
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2005/06/20	Deciphered Date	2006/06/20	Title	<b>BATTERY CONN. / OTP/+0.9VSP</b>
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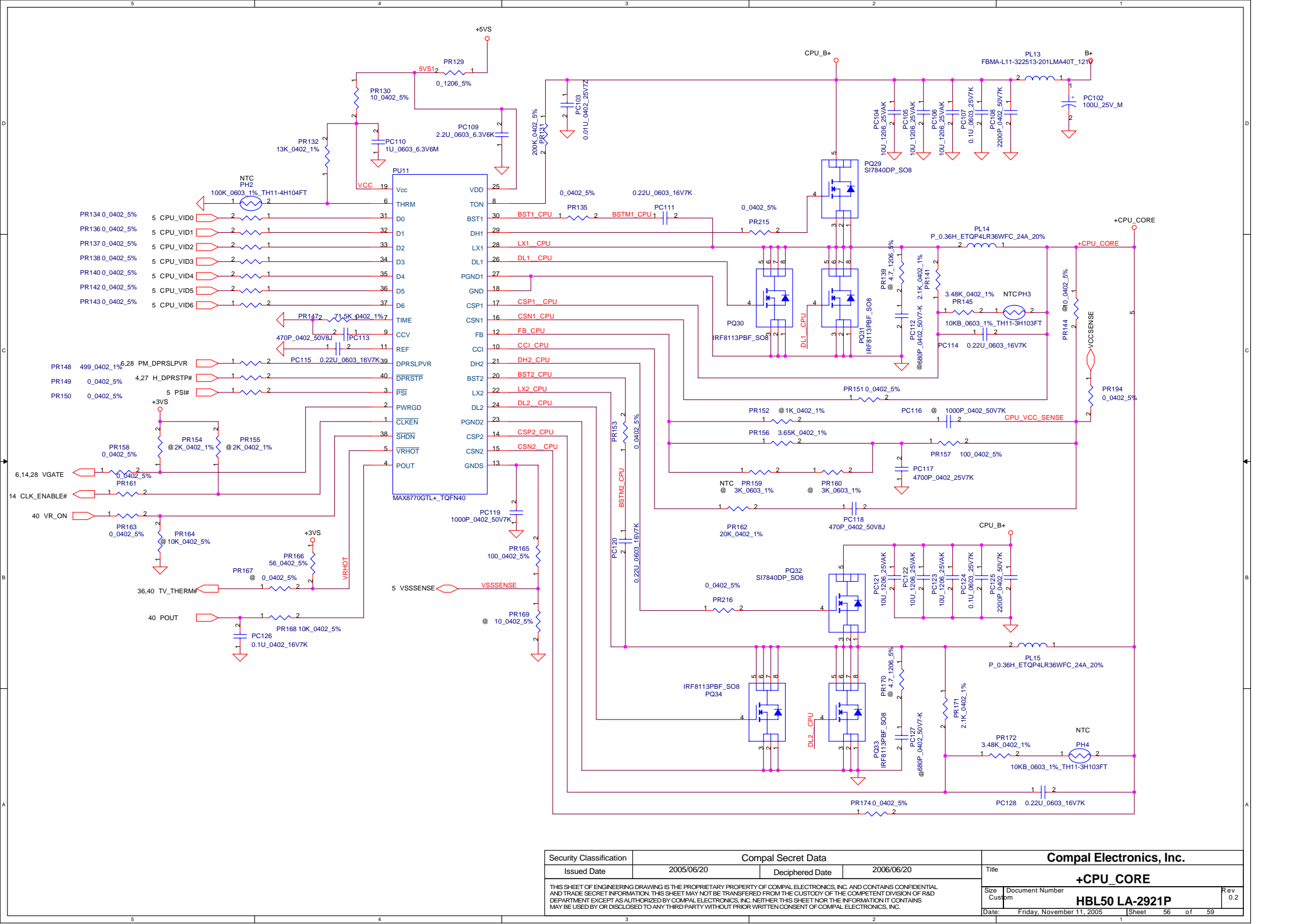
**Vin Detector**  
17.90V/17.24V



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Size	Document Number			Rev	
B	HBL50 LA-2921P			0.2	
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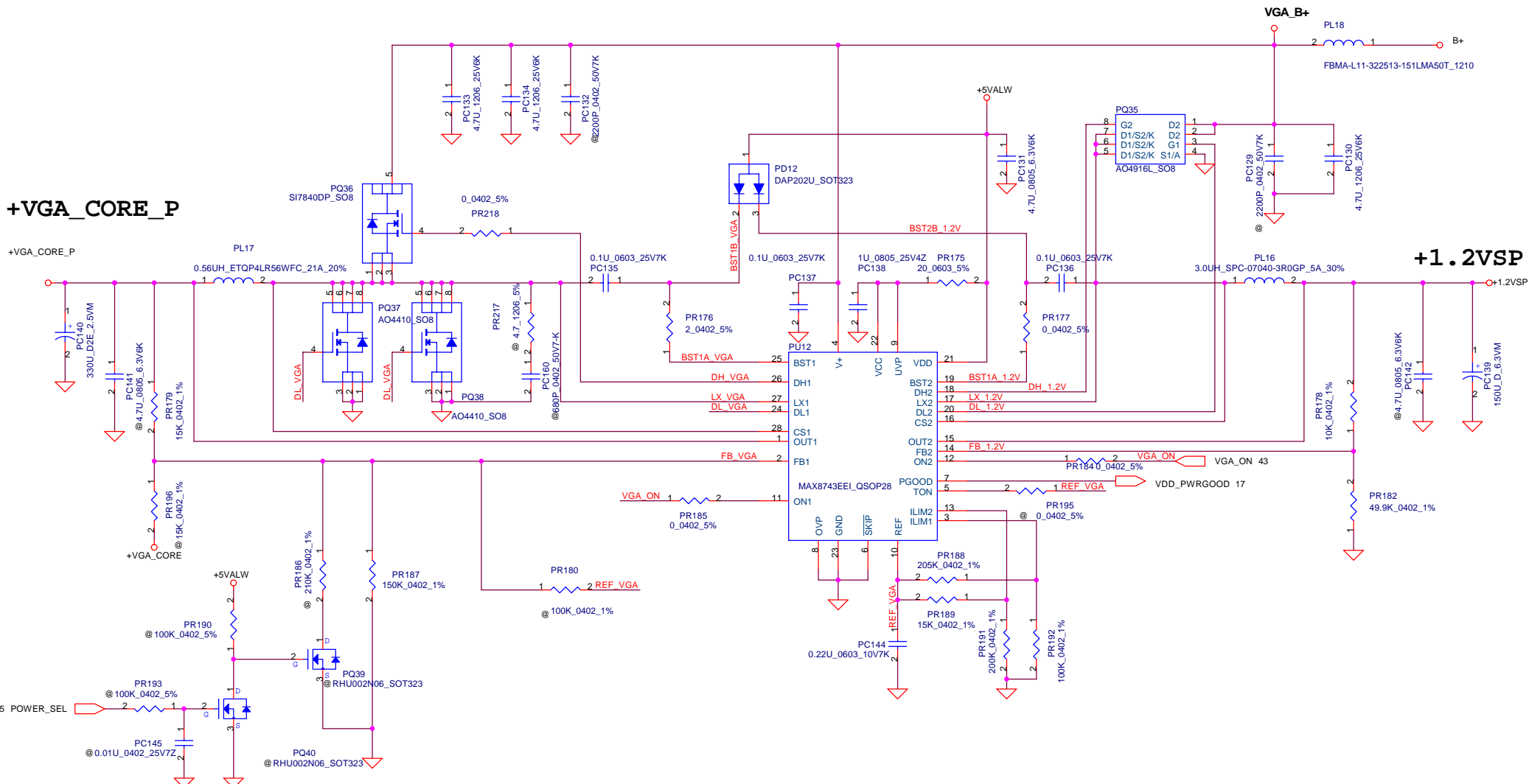
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Title	+CPU_CORE			
Size	Document Number	HBL50 LA-2921P		Rev
Custom			56	0.2
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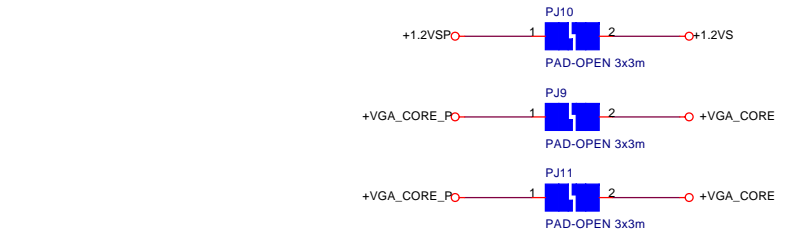


POWER_SEL	H	L
+VGA_CORE FOR G73.	+0.95V(VGA@+G72@)	+1.025V
+VGA_CORE FOR G72.	+1.1V(VGA@)	



**+VGA\_CORE\_P**

**+1.2VSP**



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Compal Electronics, Inc.			
Title: <b>+VGA_CORE_P/+1.2VSP</b>			
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## A --> B Change List

1. Page06 : No stuff R100 10K\_0402\_5%
2. Page09 : Add C49 & C887 220U\_D2\_4VMM
3. Page10 : No stuff R57 2.2K\_0402\_5%
4. Page14 : Add R711 10K\_0402\_5% to set 96MHz output  
Change Q14 & Q15 pin1 net name to connect to ICH7M  
Change U19 ICS9LPRS325CKLFT part number to SA00000RE20
5. Page15 : Change C663, C664 from 22P\_0402\_50V8J to 18P\_0402\_50V8J.
6. Page18 : Modify VGA Device ID for G72MV & G73.
7. Page24 : Change VGA\_DDC\_CLK & VGA\_DDC\_DATA to Q26 & Q27 Level shift.  
Add R781 & R782 4.7K\_0402\_5%  
Change C589, C596, C583, C587, C594, C585 to 150P\_0402\_50V8J
8. Page28 : Change SB\_INT\_FLASH\_SEL# from ICH7M GPIO38 to GPIO33.
9. Page29 : Change C437 from 0.1U\_0402\_16V4Z to 1U\_0402\_6.3V4Z
10. Page30 : Change PATA HDD+ODD select resistor form RP to R\_0402 (0\_0402\_5%)
11. Page34 : Stuff R175 & no stuff R182 (0\_0402\_5%) for BCM4401E/BCM5789M/BCM5787M
12. Page35 : Modify LAN\_ACTIVITY# & LAN\_LINK# LED color
13. Page 36 : Add JP38 & C895 for CAMERA.  
Swap JP17 PCIE TX & RX Signal.  
Swap JP30 PCIE TX & RX Signal.
14. Page37 : Connect JP34 SMBus interface to ICH7M  
Change JP4 & JP5 USB connector to BOTTOM.
15. Page38 : Add 1394 @ BOM Structure.
16. Page41 : Delete LCM interface Extension I/O.  
No stuff R390 & Stuff R418 for Flash ROM interface.
17. Page42 : Change JP11 from 34 pin to 24 pin.  
Change SW8 & SW9.  
Add JP37.
18. Page43 : Change U28 Part Number.  
Change SW1 Part Number.  
Change R425 from 10K\_0402\_5% to 62K\_0402\_1%  
Change R422 from 10K\_0402\_5% to 62K\_0402\_1% & add C513 0.1U\_0402\_16V4Z
19. Page44 : Add C554 for MIC\_R  
Add R440, R695 (0\_0603\_5%) & J4, J5 for EMI request.
20. Page45 : Add Echo Cancellation function.
21. Page46 : Correct Headphone L & R signal.  
Reserved C879 for EMI request  
Modify MIC Jack circuit. add R741, R775, R776, L54, C876  
Change JP44 from 14 pin to 16 pin
22. Page48 : H27 connect to GNDA.
23. Page49 : Add R290, R238, R497, Q10, Q7, Q29  
Change R317 to 200K\_0402\_5%  
Change R586 to 510K\_0402\_5%

## B --> C Change List

1. Page05 : No stuff C608, C614
2. Page12 : Change JP22 Footprint
3. Page14 : Change R620 from 2K\_0402\_5% to 10K\_0402\_5% & add Q38
4. Page15 : Delete DVI pull high resistor
5. Page17 : AddC96 330U for +VGA\_CORE
6. Page18 : Modify PEX\_CFG[0..2] setting from 02 to 01.
7. Page30 : Delete R395 & C486, add R394 for SATA bridge reset timing  
Modify SATA HDD connector library
8. Page31 : Delete IDE\_CD\_L, IDE\_CD\_R & CD\_GNDA
9. Page34 : Add R783, R784, R785 for BCM5787M, stuff R214 when use BCM4401E,  
Del R168, change Q5 P/N
10. Page36 : Add +3VS, GND at JP30 for 3G device
11. Page38 : No stuff U14, R253, R246 & stuff R261
12. Page40 : Reserved R793 for ALC883 pin47 EAPD, & define KB910 Pin174 as EC\_PWROK
13. Page41 : No stuff U21, U30, C490, R391, R390, R388 & stuff R418
14. Page42 : Modify SW9 Pin1, Pin5 as NC, no stuff C7
15. Page43 : Modify Power OK circuit. add R790 for EC\_PWROK, reserved Q41, R420, C512  
add D35, D37, Change BATT1 P/N to SP093PA0200
16. Page44 : Delete ALC883 CD input circuit, add HD\_EAPD# signal
17. Page46 : Add C927, C928, reserved R791, R792
18. Page49 : Stuff Q33

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