MYALL Block Diagram (Ref. rename from 12/6)

Project Code: 91.4G501.001

PCB: 05244-Rev.

CLK GEN.
IDT CV125 3

Mobile CPU
Dothan 4, 5

G792 19

HOST BUS 400MHz

DDR II 400 MHz 11,12 — 400MHz

DDR II 400 MHz 11,12 — 400MHz

Intel 910GM (UMA)
Intel 915PM (DIS) 6,7,8,9,10

DMI I/F 100MHz

RGB → CRT 14

LVDS → LCD 13

Nvidia G72M-V 24,25 — VRAMx4 24,25

Line In 27
Mic In 27
Int. MIC In 27
Line Out 27
Codec ALC861 26
Azalia

INT.SPKR 27 — OP AMP G1421B 27

MODEM MDC Card 21

ICH6-M 15,16,17,18

PCI BUS

ENE CB1410 24,25 — PWR SW CP2211 25 — PCMCIA ONE SLOT 25

Mini-PCI 802.11A/B/G 28

LAN 10/100 RTL8110CL 22, 23 — TXFM 23 — RJ45 23

PCIE X1 — PCI MINI CARD 25

LPC BUS

Golden Finger 30

KBC ENE KB3910 29 — Xbus — BIOS ROM 512 K PM39LV040-70JCE 31

Touch Pad 30

INT_KB 30

SATA

SATA 24,25

HDD 20

SATA 24,25

(co-lay)

PATA

CDROM 20

USB

USB 5 PORT 21

MINI USB 21
BlueTooth

LED BDx1
(another circuit)

CPU DC/DC ISL6218CV-T 34

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0.844~1.3V 27A

SYSTEM DC/DC TPS51120 35

INPUTS	OUTPUTS
DCBATOUT	3D3V_S5 5V_S5

APL5912-LAC APL5308-25AC 36

INPUTS	OUTPUTS
5V_S5 3D3V_S0	1D5V_S0 2D5V_S0

SYSTEM DC/DC ISL6227 37

INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S3

TPS51100DGQ 37

5V_S5	DDR_VREF DDR_VREF_S3

CHARGER ISL6255 38

INPUTS	OUTPUTS
DCBATOUT	BT+ 16.8V 3A

PCB Layer Stackup

L1: Signal 1
L2:VCC
L3: Signal 2
L4: Signal 3
L5: GND
L6: Signal 4

<Core Design>
Wistron Corporation
DN: cn=dd, o=dd, ou
email=dddd@yahoo.
c=US
Date: 2009.11.29 07:5
+07'00'
Rev SA

Alviso Strapping Signals and Configuration

page 7

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = Reserved 001 = FSB533 010 = FSB800 011-111 = Reversed
CFG[3:4]	Reversed	
CFG5	DMI x2 Select	0 = DMI x2 **1 = DMI x4** (Default)
CFG6	DDR I / DDR II	0 = DDR II 1 = DDR I
CFG7	CPU Strap	0 = Prescott **1 = Dothan** (Default)
CFG[8:11]	Reversed	
CFG[12:13]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled **11 = Normal Operation** (Default)
CFG[14:15]	Reversed	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled** (Default)
CFG17	Reversed	
CFG18	CPU core VCC Select	**0 = 1.05V** (Default) 1 = 1.5V
CFG19	CPU VTT Select	**0 = 1.05V** (Default) 1 = 1.2V
CFG20	Reversed	
SDVOCRTL _DATA	SDVO Present	**0 = No SDVO device present** (Default) 1= SDVO device present

NOTE: All strap signals are sampled with respect to the leading edge of the Alviso GMCH PWORK In signal.

PCI Routing

	IDSEL	IRQ	REQ/GNT
1410	25	B.F.G	0
MiniPCI	21	F	1
LAN	23	E	2

ICH6-M Integrated Pull-up and Pull-down Resistors

ICH6-M EDS 14308 0.8V1

ACZ_BIT_CLK, DPRSLP#, EE_DIN, EE_DOUT, GNT[5]#/GPO[17], GNT[6]#/GPO[16], LDRQ[1]/GPI[41], LAD[3:0]#/FB[3:0]#, LDRQ[0], PME#, PWRBTN#, TP[3]	ICH6 internal 20K pull-ups
LAN_RXD[2:0]	ICH6 internal 10K pull-ups
ACZ_RST#, ACZ_SDIN[2:0], ACZ_SYNC, ACZ_SDOUT, ACZ_BITCLK, DPRSLPVR, SPKR, EE_CS,	ICH6 internal 20K pull-downs
USB[7:0][P,N]	ICH6 internal 15K pull-downs
DD[7], SDDREQ	ICH6 internal 11.5K pull-downs
LAN_CLK	ICH6 internal 100K pull-downs

ICH6-M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm

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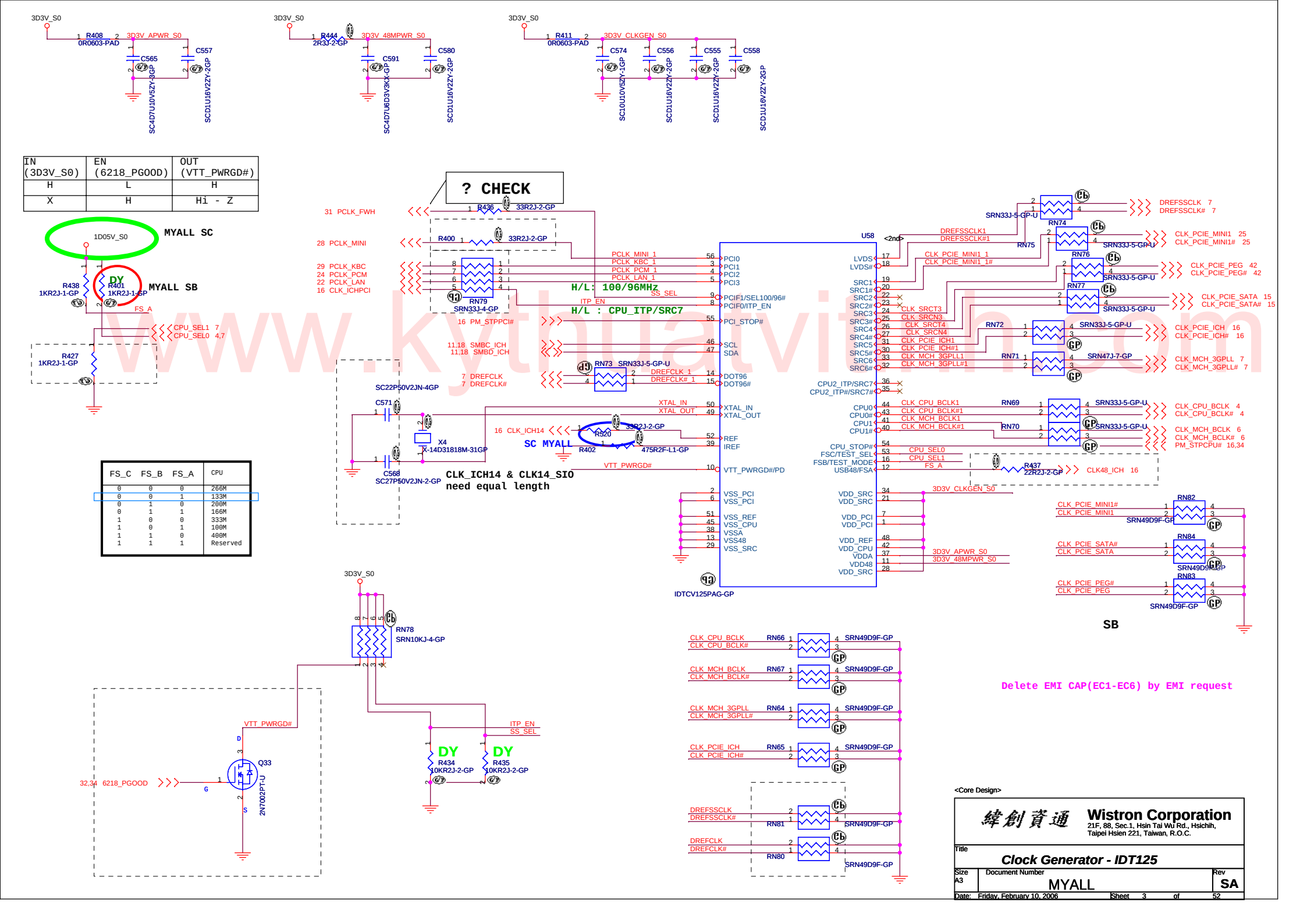
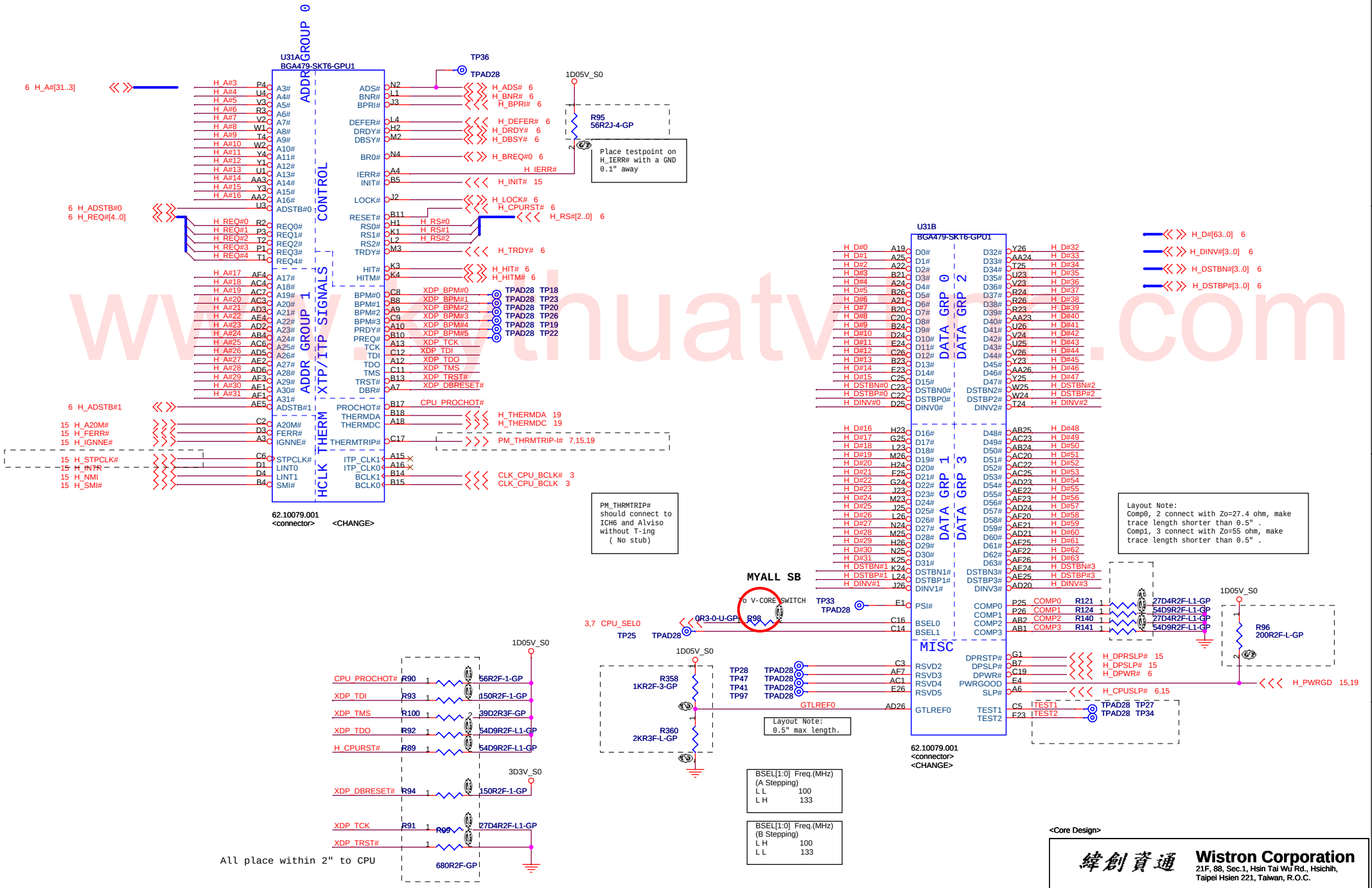
Title: Memo

Size: A3 | Document Number: MYALL | Rev: SA

Date: Friday, February 10, 2006 | Sheet 2 of 52





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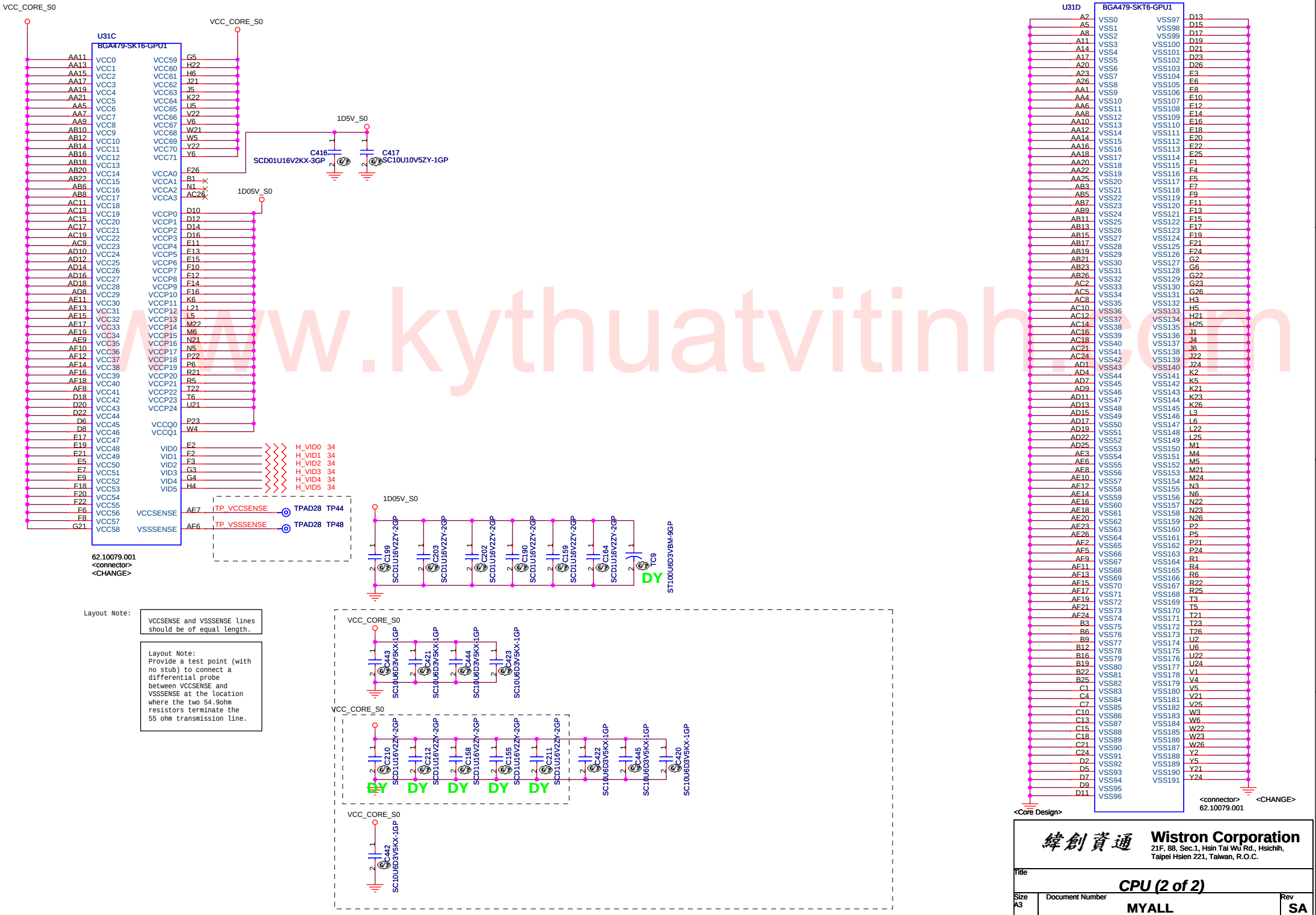
Title: CPU (1 of 2)

Size: A3 | Document Number: MYALL | Rev: SA

Date: Friday, February 10, 2006 | Sheet 4 of 52



Layout Note:

VCCSENSE and VSSSENSE lines should be of equal length.

Layout Note:
Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.

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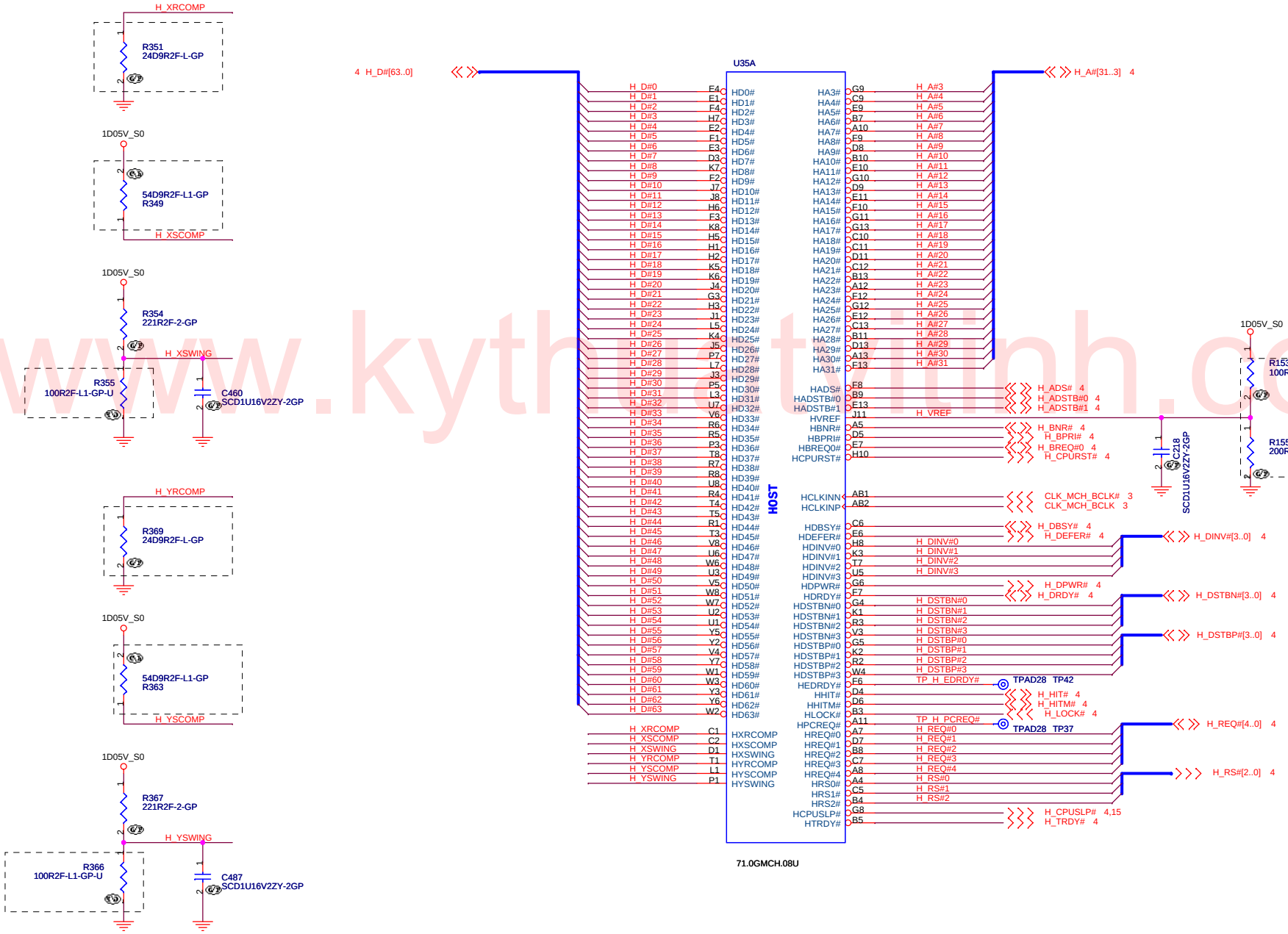
Title: **CPU (2 of 2)**

Size	Document Number	Rev
A3	MYALL	SA

Date: Friday, February 10, 2006 Sheet 5 of 52



Place them near to the chip

<Core Design>

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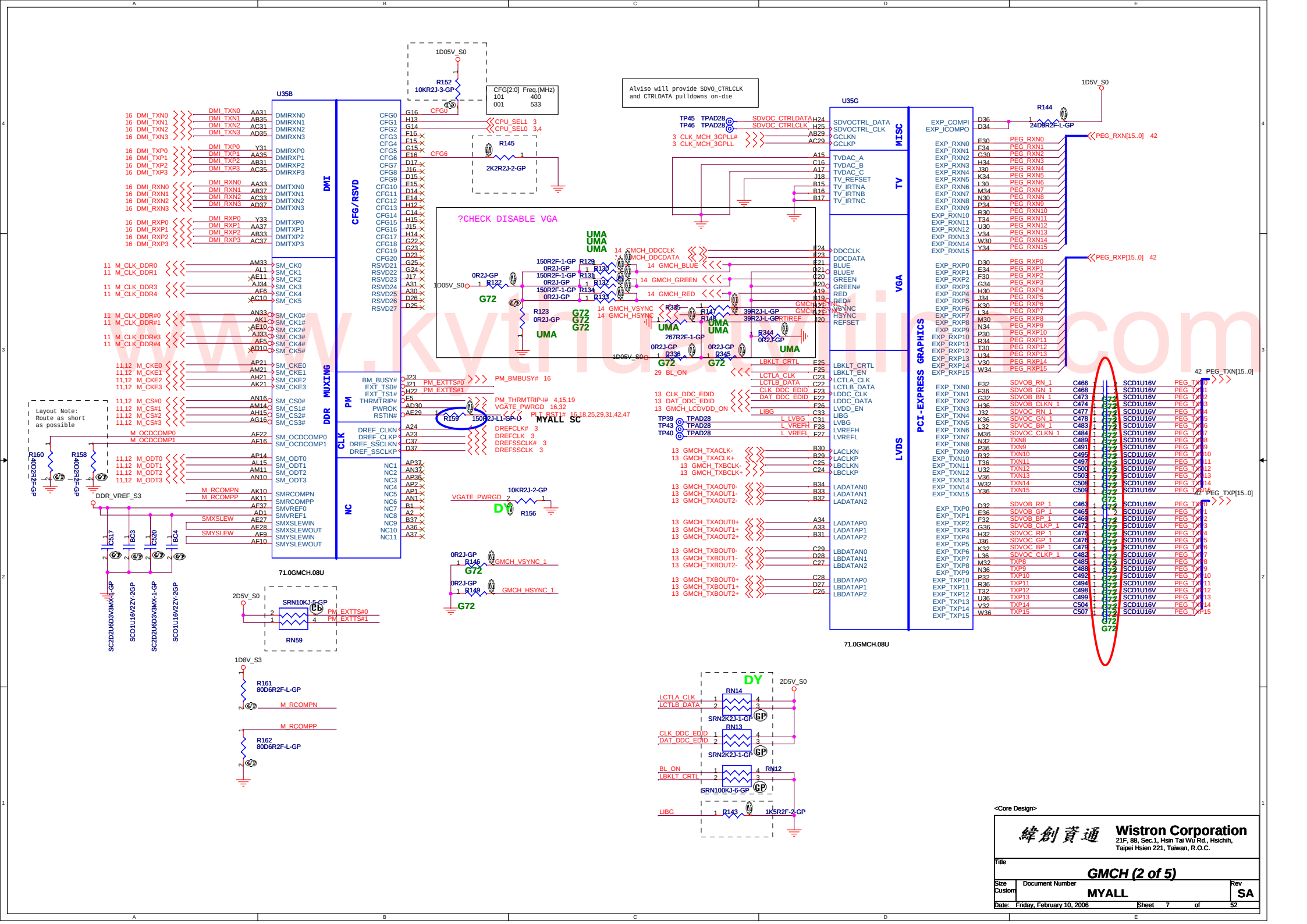
Title: GMCH (1 of 5)

Size: A3 | Document Number: MYALL | Rev: SA

Date: Friday, February 10, 2006 | Sheet 6 of 52


U35B
DMI
CFG/RSVD
MUXING
DDR
PM
CLK
NC
U35G
MISC
TV
VGA
LVDS
PCI-EXPRESS GRAPHICS
?CHECK DISABLE VGA
Alviso will provide SDVO_CTRLCLK and CTRLDATA pulldowns on-die
CFG[2:0] Freq.(MHz)
101 400
001 533
Layout Note: Route as short as possible
71.0GMCH.08U
MYALL SC
<Core Design>
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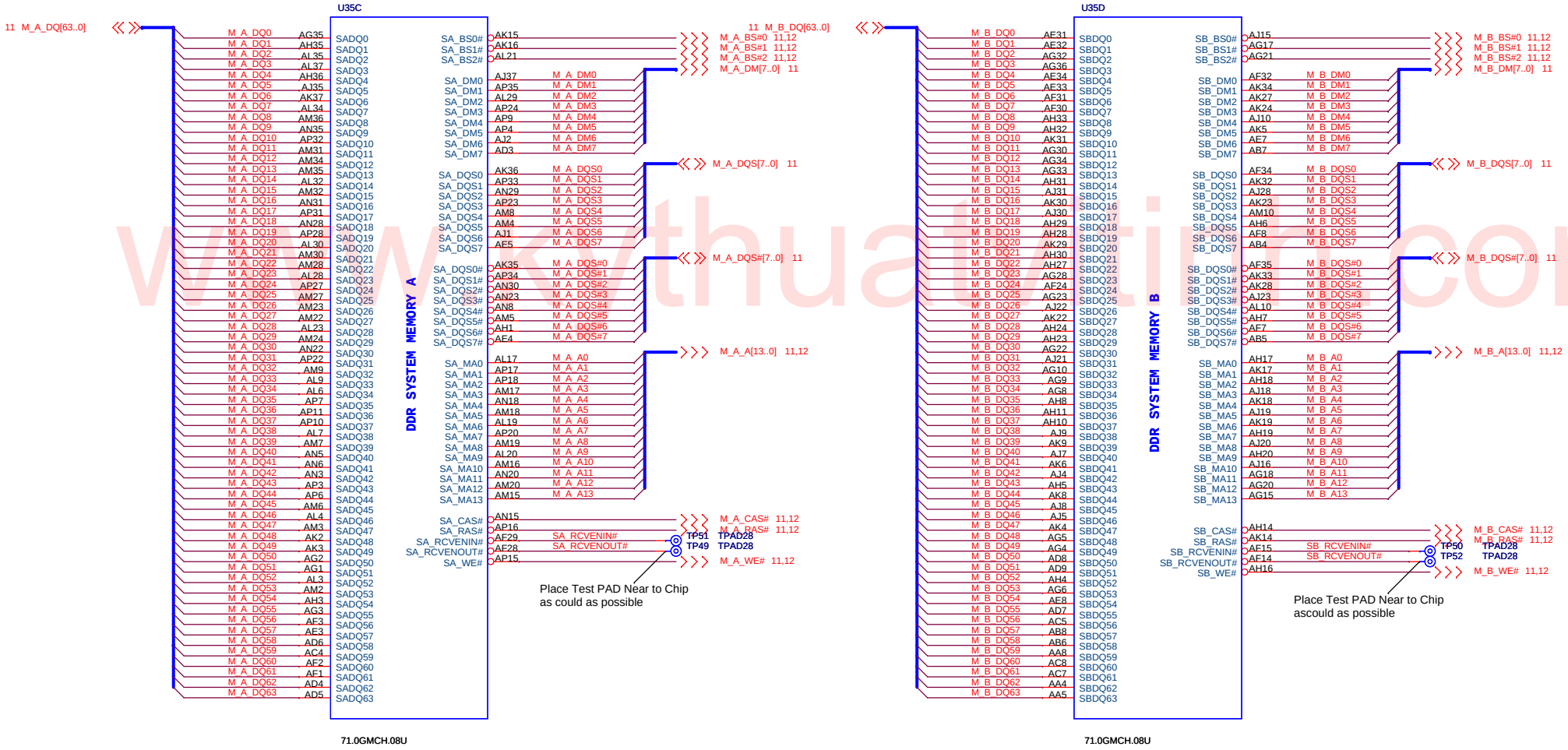
GMCH (2 of 5)
MYALL
SA
Date: Friday, February 10, 2006
Sheet 7 of 52



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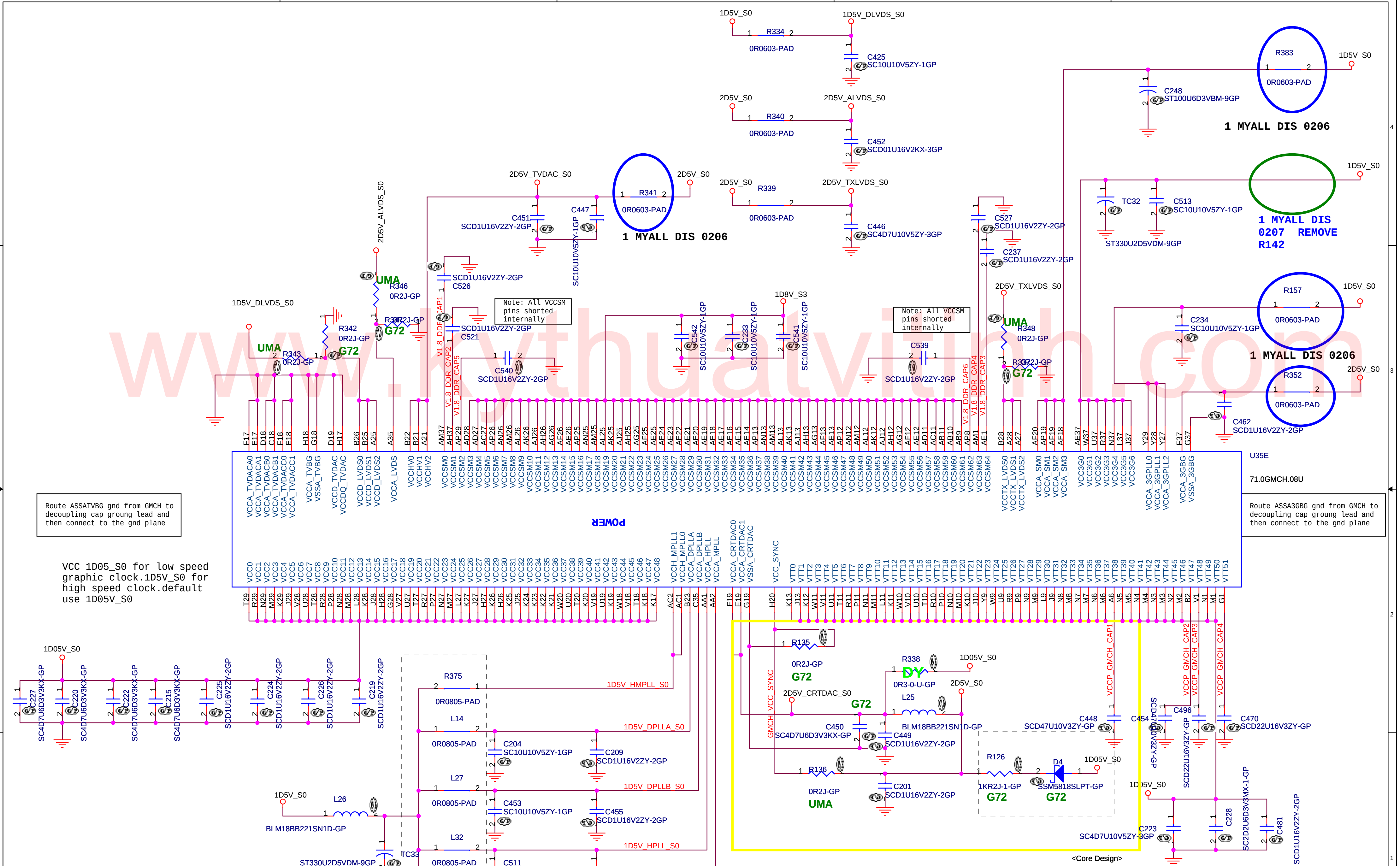
Title: ***GMCH (3 of 5)***

Size	Document Number	Rev
A3	MYALL	SA

Date: Friday, February 10, 2006 Sheet 8 of 52



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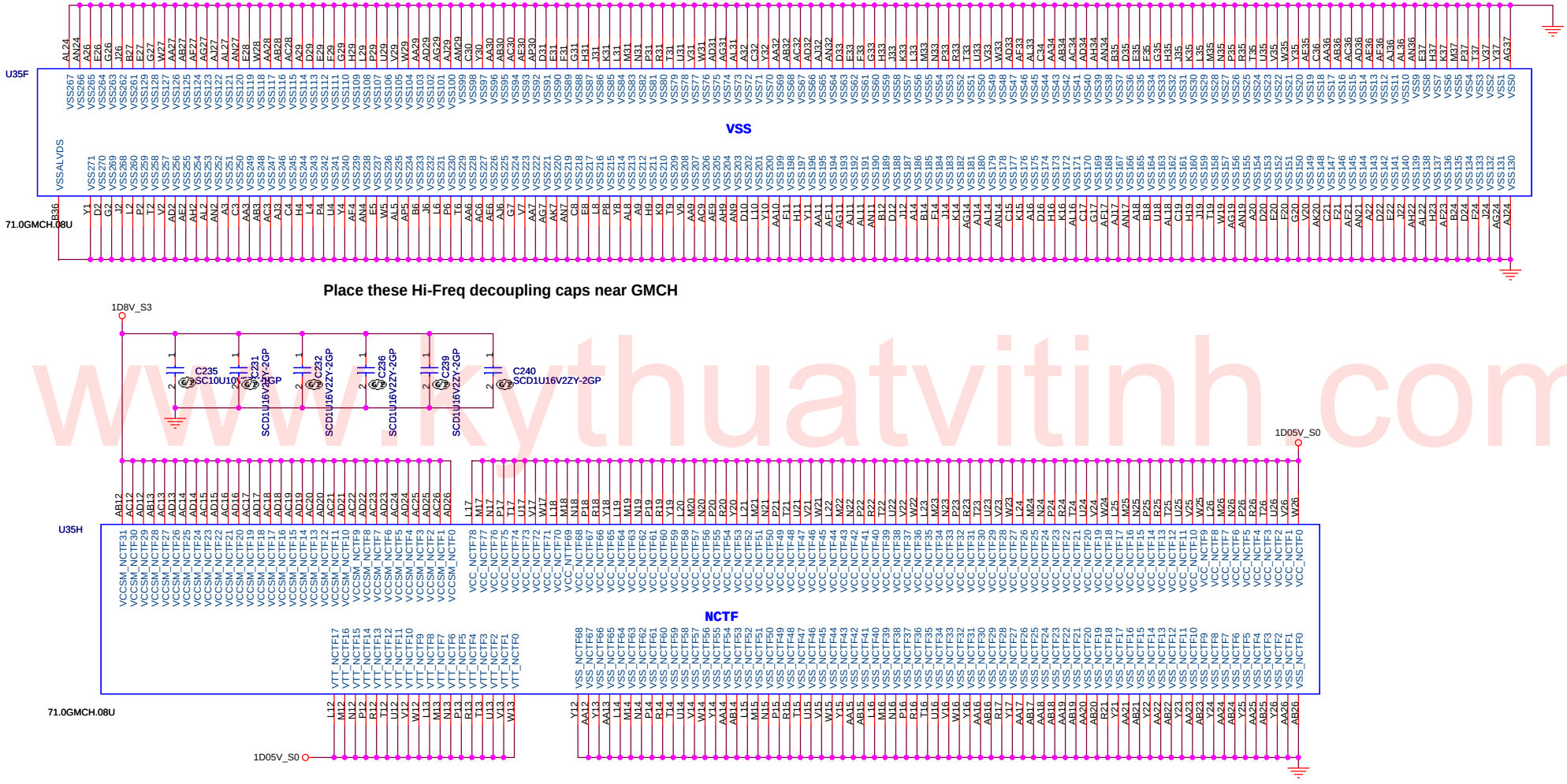
Title	GMCH (4 of 5)	
Size A3	Document Number: MYALL	Rev SA
Date: Friday, February 10, 2006	Sheet 9 of 52	



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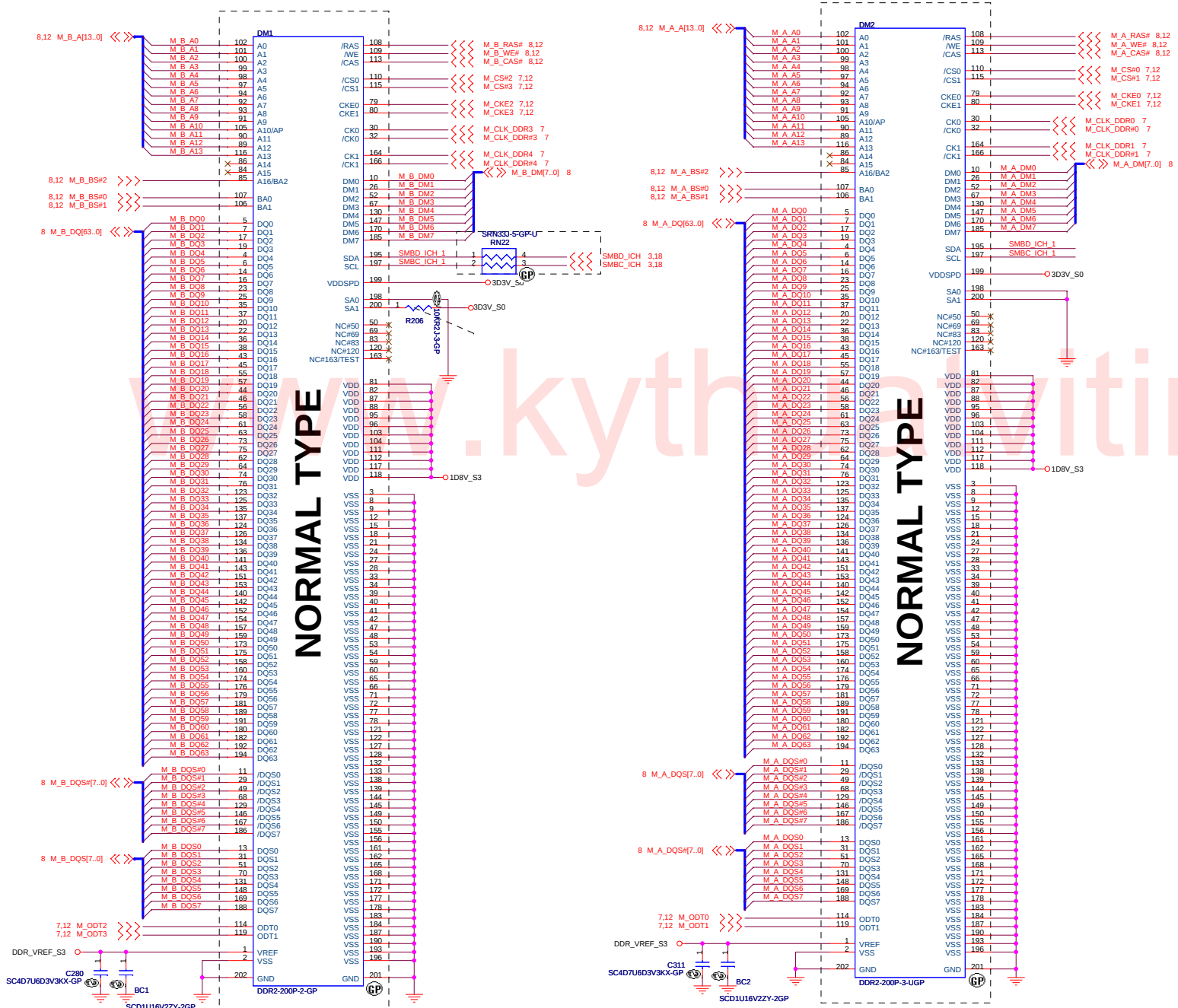
Title	***GMCH (5 of 5)***
Size A3	Document Number: **MYALL**
Rev	**SA**
Date: Friday, February 10, 2006	Sheet 10 of 52



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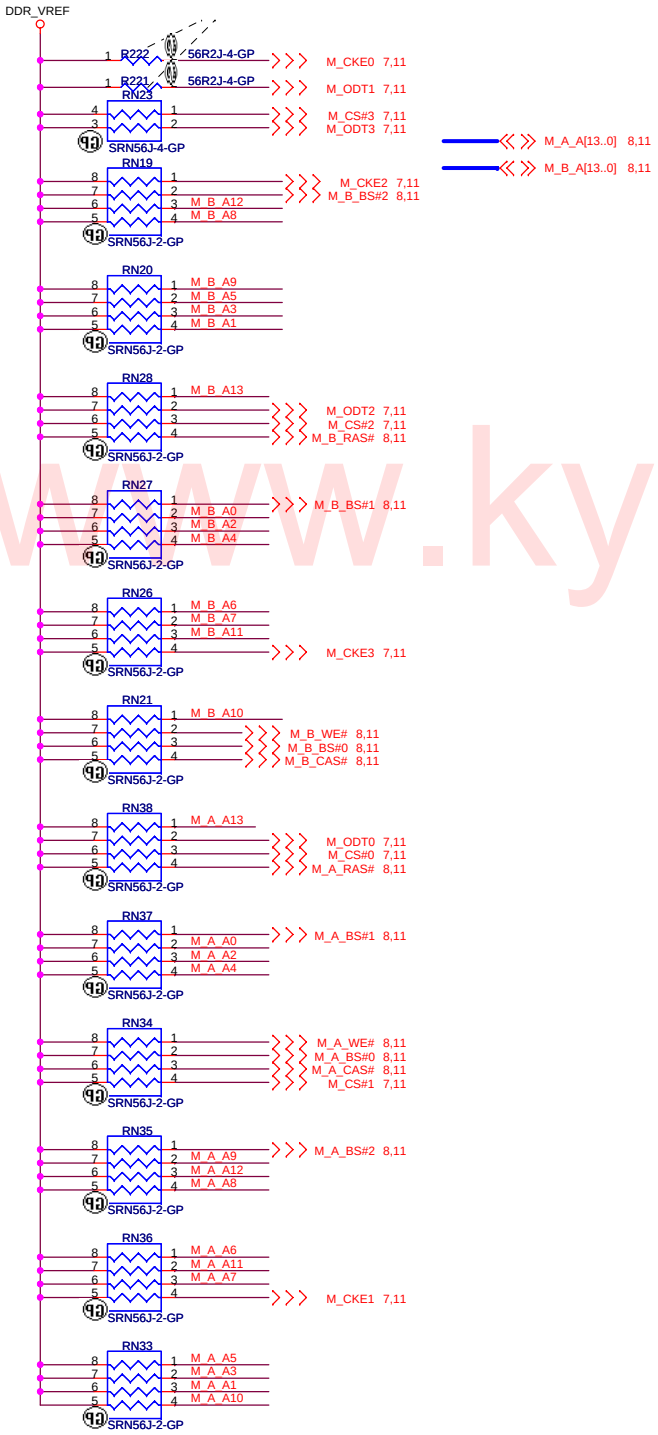
Title: DDR Socket

Size	Document Number	Rev
Custom	MYALL	SA

Date: Friday, February 10, 2006 Sheet 11 of 52

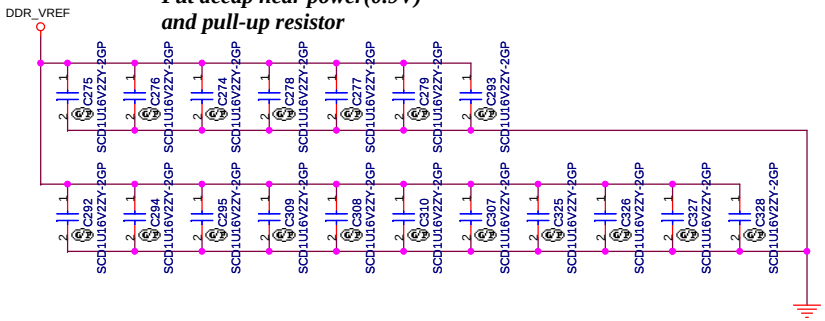
PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

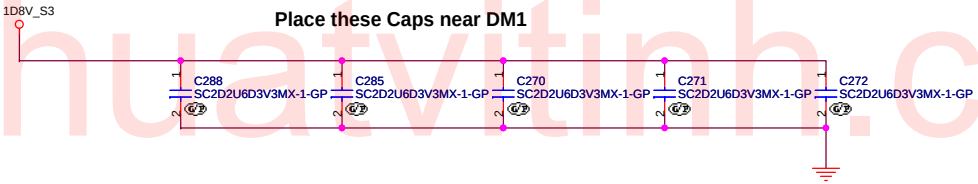


Decoupling Capacitor

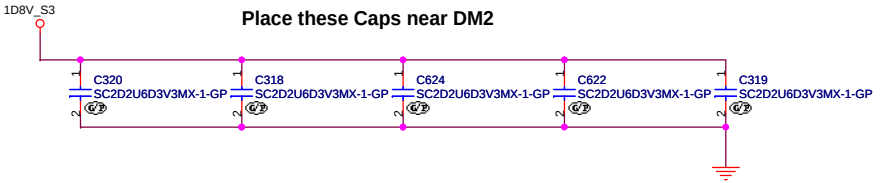
Put decap near power(0.9V) and pull-up resistor



Place these Caps near DM1



Place these Caps near DM2



<Core Design>

緯創資通 **Wistron Corporation**
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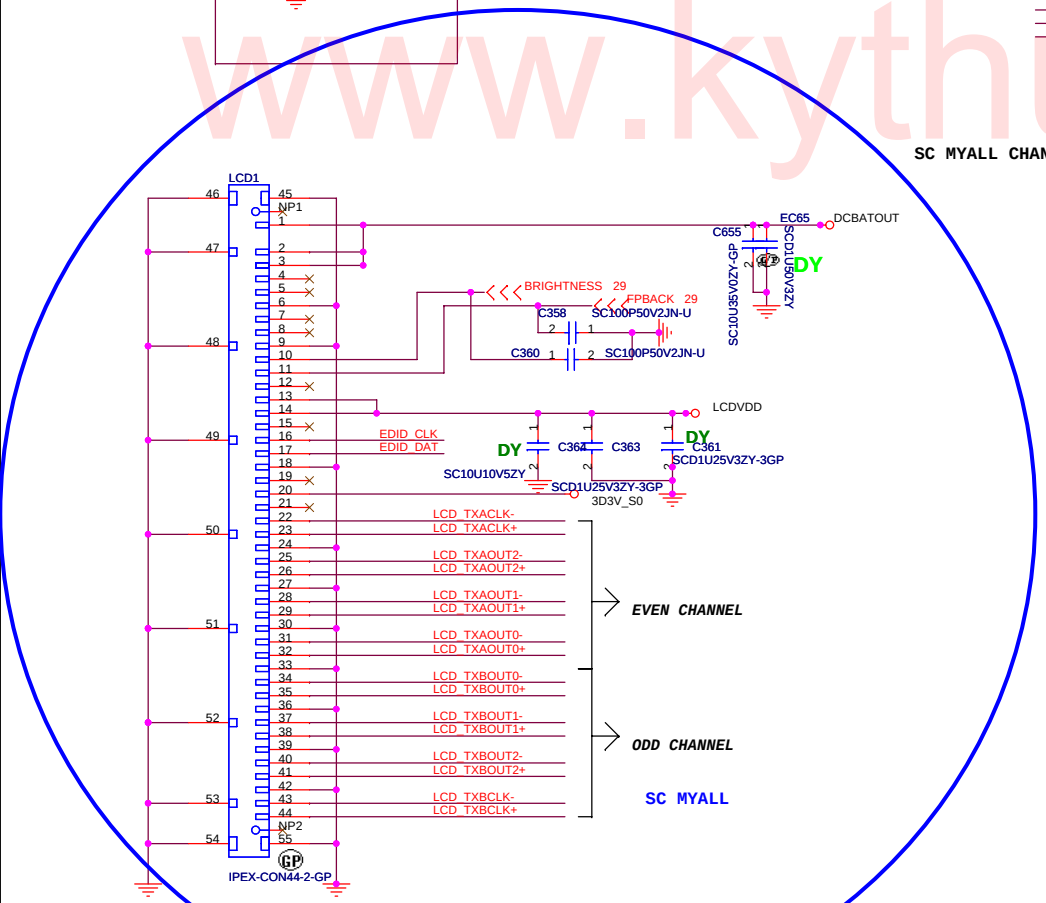
Title: ***DDR2 Termination Resistor***

Size	Document Number	Rev
A3	MYALL	SA

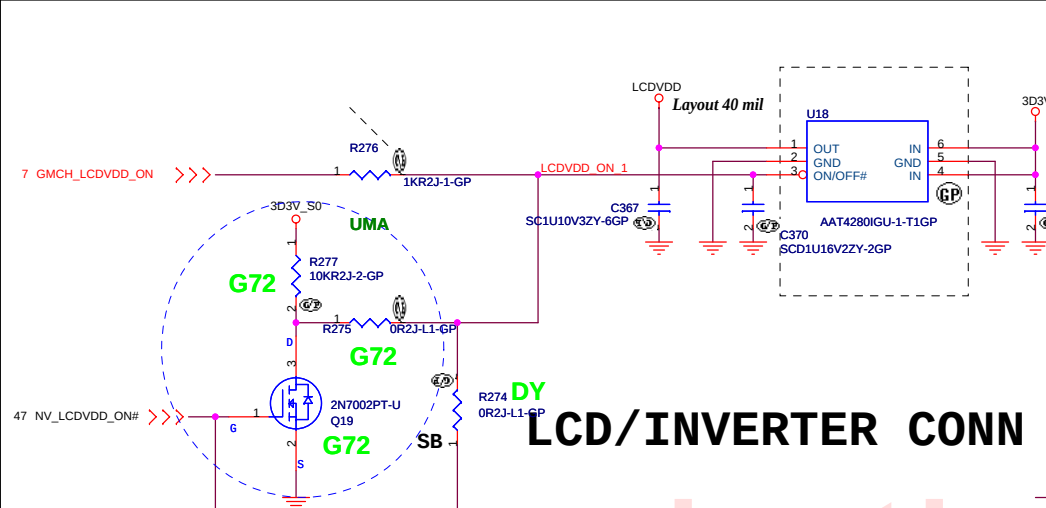
Date: Friday, February 10, 2006 Sheet 12 of 52

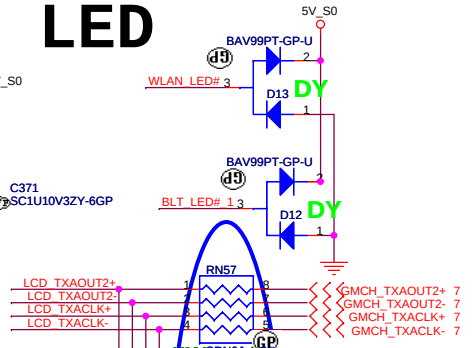
LED

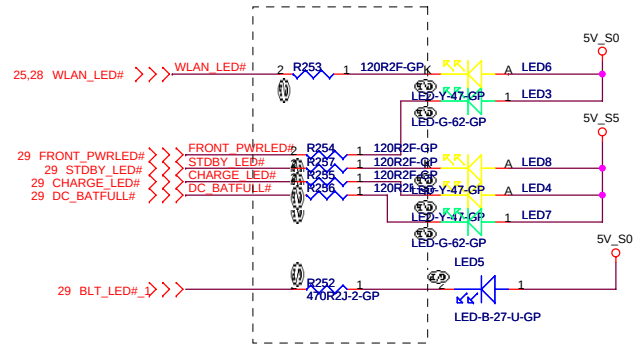
LCD/INVERTER CONN



SC MYALL CHANGE 2006.01.11

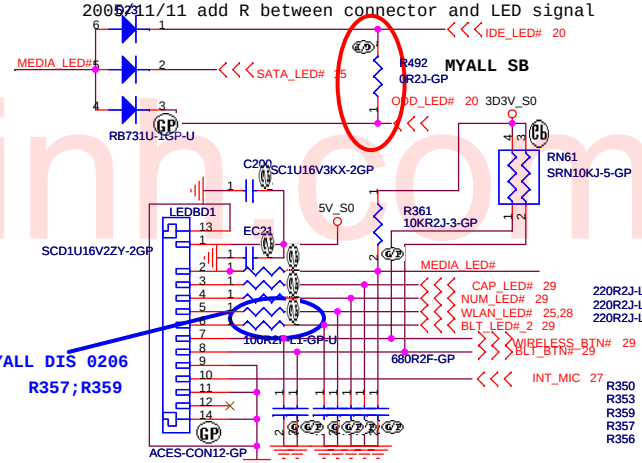




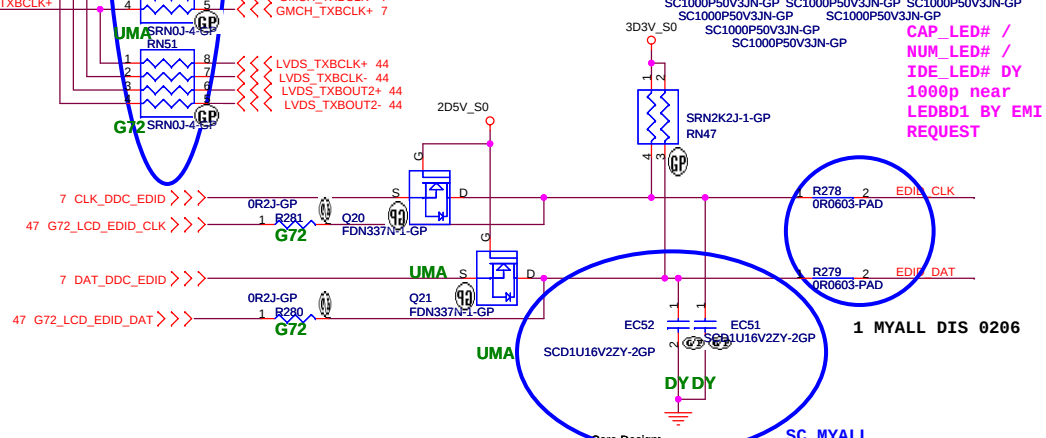


LED BD CONN

2005/11/11 add R between connector and LED signal



1 MYALL DIS 0206
R357;R359



CAP_LED# / NUM_LED# / IDE_LED# DY 1000p near LEDBD1 BY EMI REQUEST

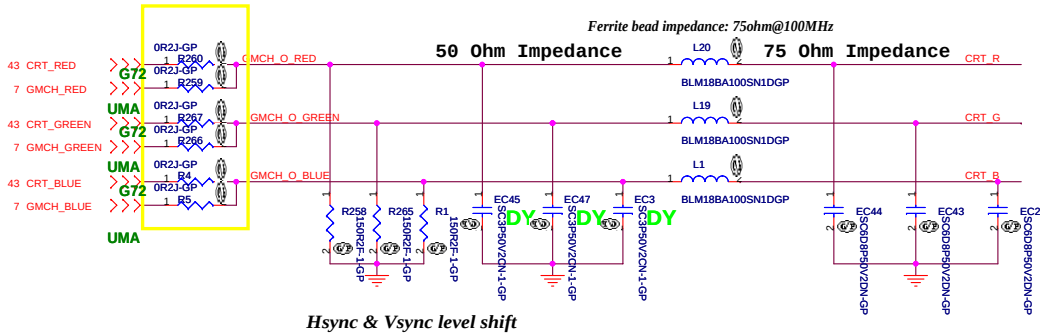
1 MYALL DIS 0206

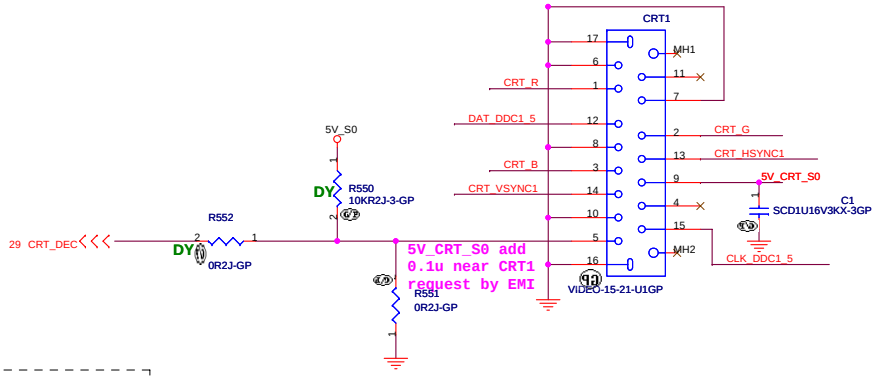
SC MYALL

<Core Design>

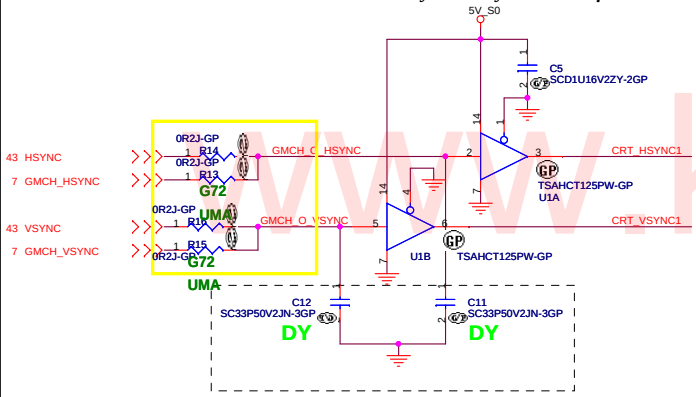
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: LCD CONN & LED		
Size: A3	Document Number: MYALL	Rev: SA
Date: Friday, February 10, 2006	Sheet 13 of 52	

CRT CONNECTOR

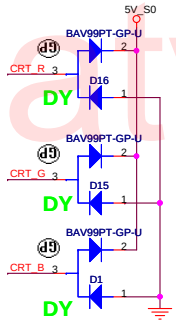


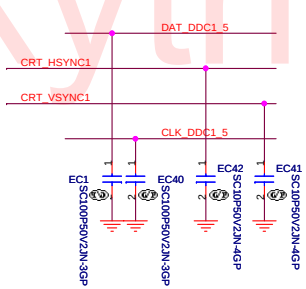


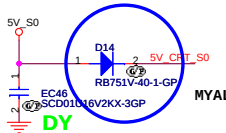
Hsync & Vsync level shift



ESD Protection Diode

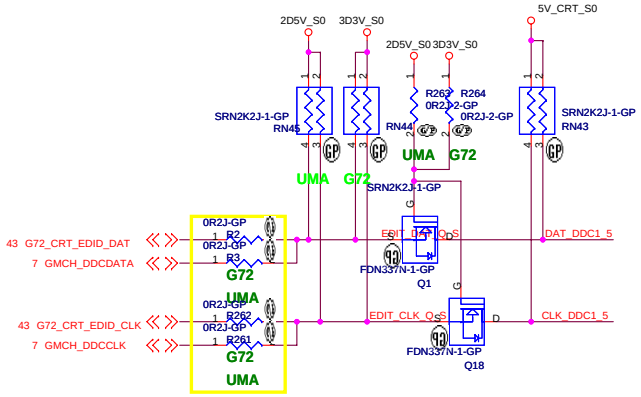






MYALL SC CHANGE

DDC_CLK & DATA level shift



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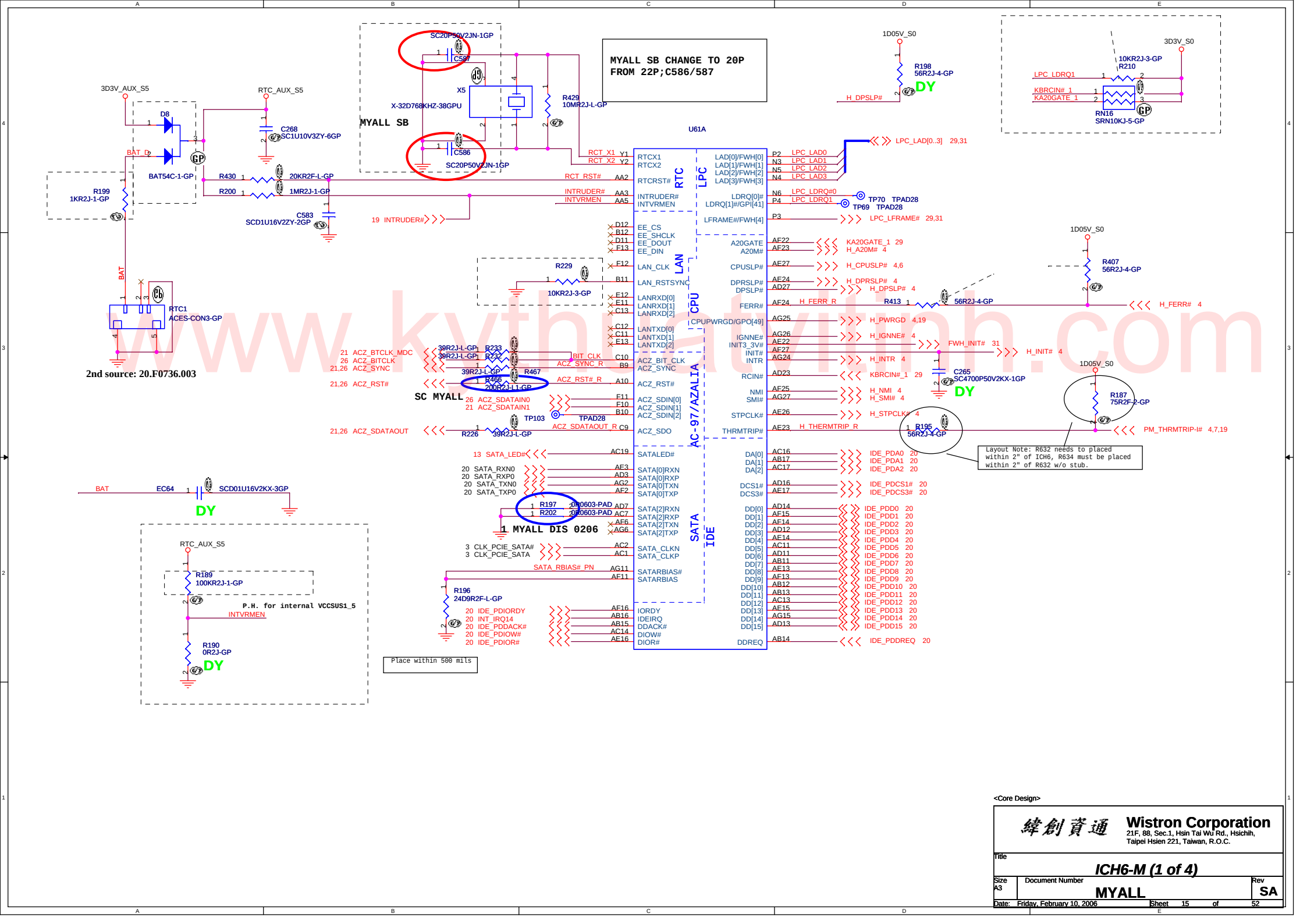
Title: CRT Connector		
Size: Custom	Document Number: MYALL	Rev: SA
Date: Friday, February 10, 2006	Sheet 14 of 52	



<Core Design>

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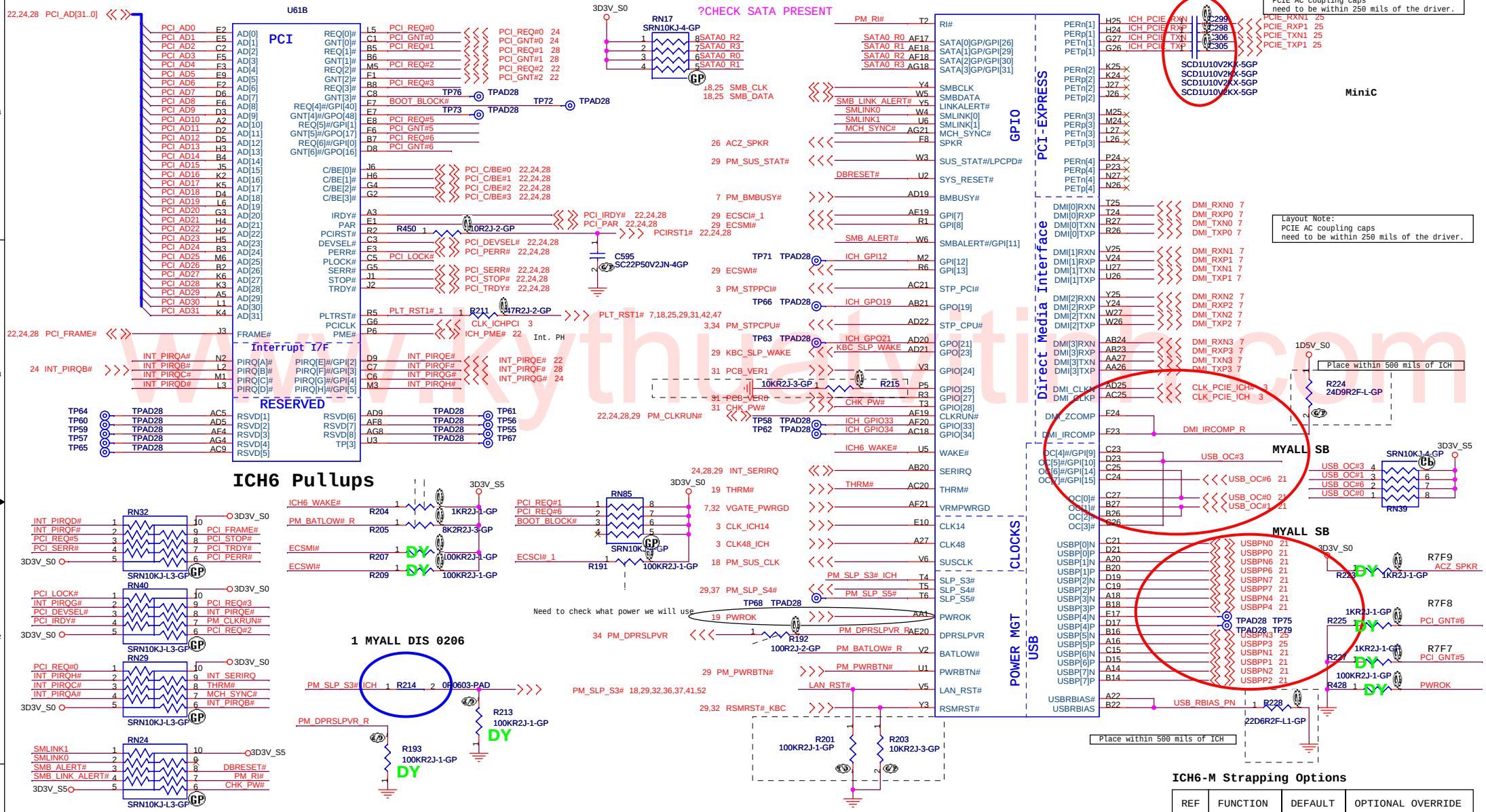
Title: ICH6-M (1 of 4)

Size	Document Number	Rev
A3	MYALL	SA

Date: Friday, February 10, 2006 Sheet 15 of 52



ICH6-M Strapping Options

REF	FUNCTION	DEFAULT	OPTIONAL OVERRIDE
R7F9	No Reboot	NO_STUFF	STUFF
R7F8	A16 Swap Override	NO_STUFF	STUFF
R7F7	Boot BIOS	NO_STUFF	STUFF

<Core Design>

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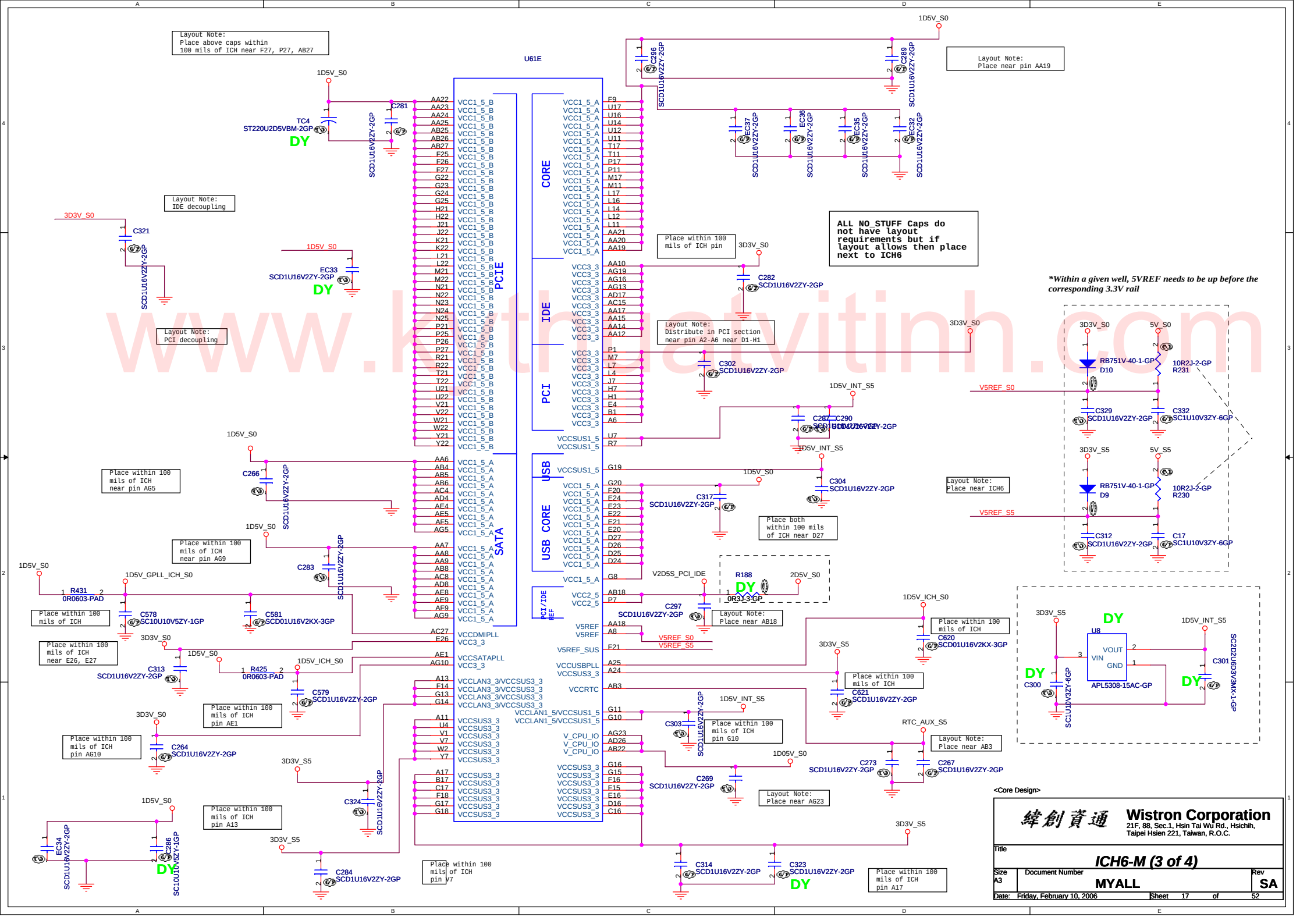
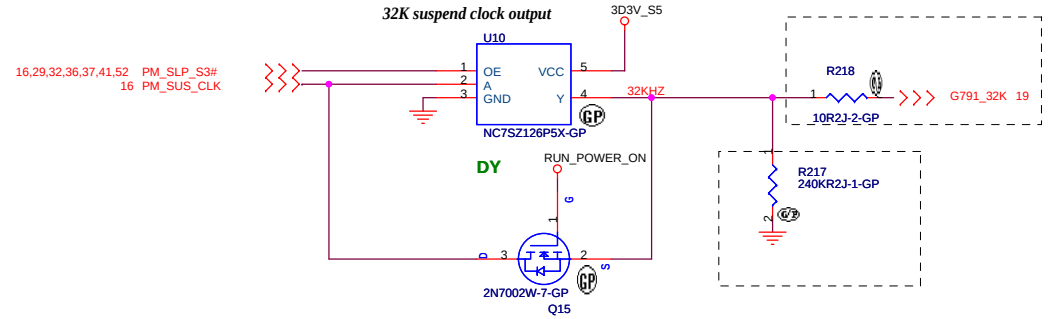
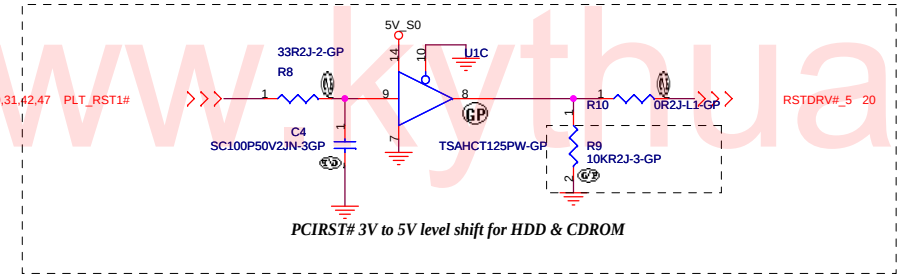
Title: ICH6-M (2 of 4)

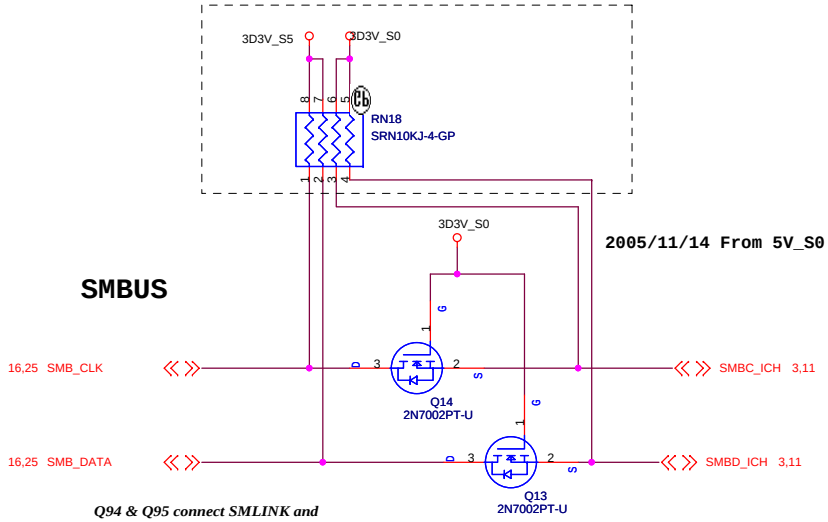
Size: A3 | Document Number: MYALL | Rev: SA

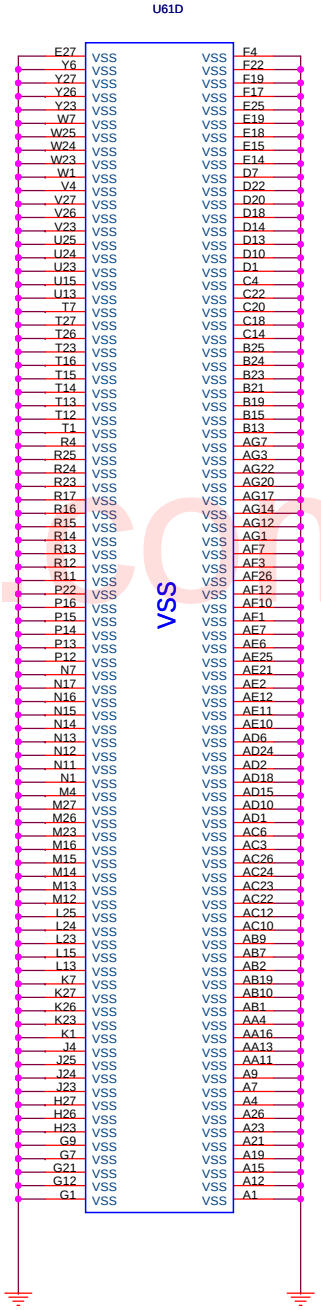
Date: Friday, February 10, 2006 | Sheet 16 of 52


U61E
PCIE
SATA
CORE
IDE
PCI
USB
USB CORE
PCI/IDE REF
Layout Note: Place above caps within 100 mils of ICH near F27, P27, AB27
Layout Note: IDE decoupling
Layout Note: PCI decoupling
Layout Note: Place near pin AA19
ALL NO_STUFF Caps do not have layout requirements but if layout allows then place next to ICH6
Place within 100 mils of ICH pin
Layout Note: Distribute in PCI section near pin A2-A6 near D1-H1
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
Layout Note: Place near ICH6
Place within 100 mils of ICH near pin AG5
Place within 100 mils of ICH near pin AG9
Place within 100 mils of ICH near E26, E27
Place within 100 mils of ICH pin AE1
Place within 100 mils of ICH pin AG10
Place within 100 mils of ICH pin A13
Place within 100 mils of ICH pin V7
Place within 100 mils of ICH pin G10
Place within 100 mils of ICH pin A17
Place within 100 mils of ICH
Place both within 100 mils of ICH near D27
Layout Note: Place near AB18
Layout Note: Place near AB3
Layout Note: Place near AG23
Place within 100 mils of ICH
Place within 100 mils of ICH
Place within 100 mils of ICH
Place within 100 mils of ICH
Place within 100 mils of ICH
Place within 100 mils of ICH
1D5V_S0
3D3V_S0
5V_S0
1D5V_INT_S5
3D3V_S5
5V_S5
1D5V_ICH_S0
1D5V_GPLL_ICH_S0
V2D5S_PCI_IDE
2D5V_S0
1D05V_S0
RTC_AUX_S5
V5REF_S0
V5REF_S5
V5REF_SUS
V_CPU_IO
TC4 ST220U2D5VBM-2GP DY
EC33 SCD1U16V2ZY-2GP DY
C321 SCD1U16V2ZY-2GP
C281 SCD1U16V2ZY-2GP
C296 SCD1U16V2ZY-2GP
C289 SCD1U16V2ZY-2GP
EC37 SCD1U16V2ZY-2GP
EC36 SCD1U16V2ZY-2GP
EC35 SCD1U16V2ZY-2GP
EC32 SCD1U16V2ZY-2GP
C282 SCD1U16V2ZY-2GP
C302 SCD1U16V2ZY-2GP
C287 C290
C304 SCD1U16V2ZY-2GP
C317 SCD1U16V2ZY-2GP
C266 SCD1U16V2ZY-2GP
C283 SCD1U16V2ZY-2GP
R431 0R0603-PAD
C578 SC10U10V5ZY-1GP
C581 SCD01U16V2KX-3GP
R425 0R0603-PAD
C313 SCD1U16V2ZY-2GP
C579 SCD1U16V2ZY-2GP
C264 SCD1U16V2ZY-2GP
C324 SCD1U16V2ZY-2GP
C284 SCD1U16V2ZY-2GP
EC34 SCD1U16V2ZY-2GP
C286 SC10U10V5ZY-1GP
R188 0R3J-3-GP DY
C297 SCD1U16V2ZY-2GP
C303 SCD1U16V2ZY-2GP
C269 SCD1U16V2ZY-2GP
C314 SCD1U16V2ZY-2GP
C323 SCD1U16V2ZY-2GP DY
C620 SCD01U16V2KX-3GP
C621 SCD1U16V2ZY-2GP
C273 SCD1U16V2ZY-2GP
C267 SCD1U16V2ZY-2GP
RB751V-40-1-GP D10
10R2J-2-GP R231
C329 SCD1U16V2ZY-2GP
C332 SC1U10V3ZY-6GP
RB751V-40-1-GP D9
10R2J-2-GP R230
C312 SCD1U16V2ZY-2GP
C17 SC1U10V3ZY-6GP
U8 APL5308-15AC-GP
C300 SC1U10V3ZY-6GP DY
C301 SC2D2U6D3V3MX-1-GP DY
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH6-M (3 of 4)
Size A3
Document Number MYALL
Rev SA
Date: Friday, February 10, 2006
Sheet 17 of 52









<Core Design>

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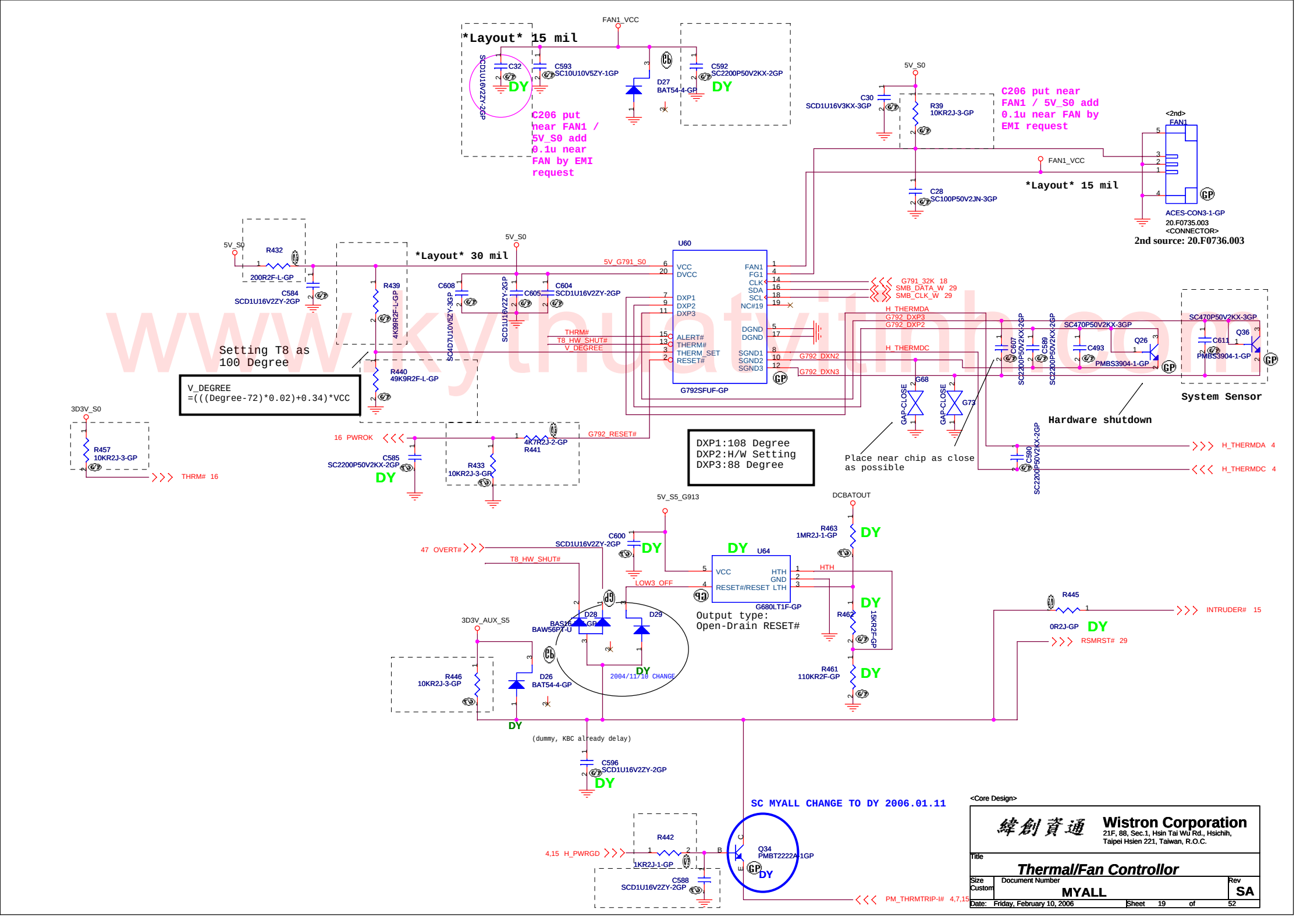
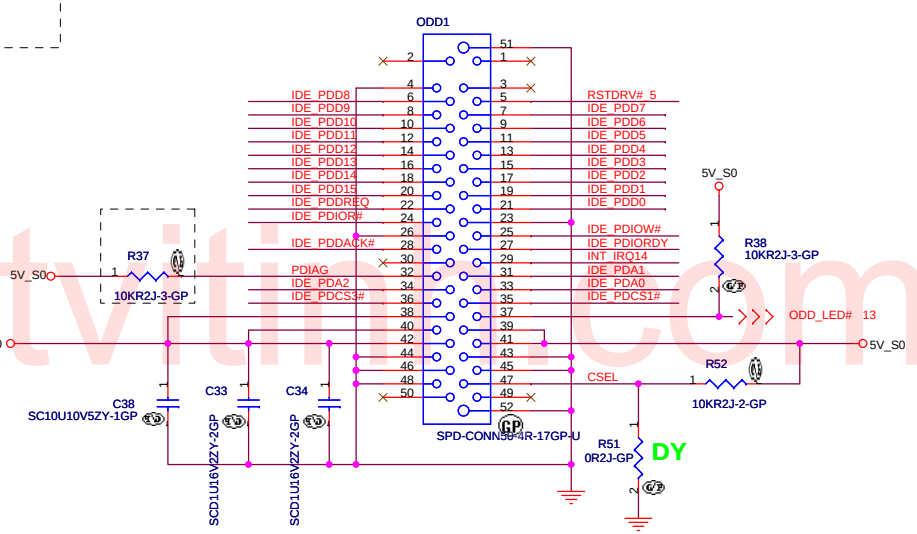
Title: ICH6-M (4 of 4)

Size	Document Number	Rev
A3	MYALL	SA

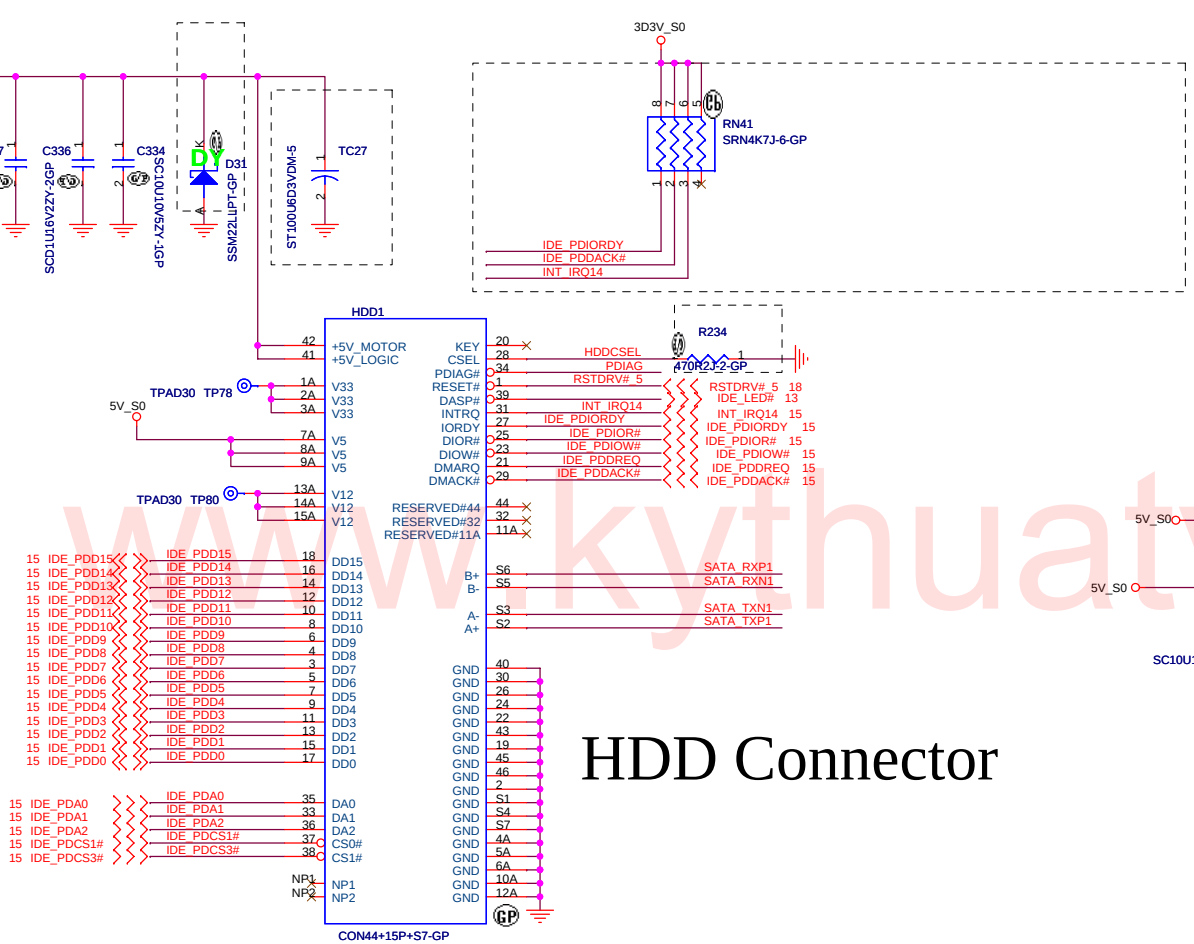
Date: Friday, February 10, 2006 Sheet 18 of 52



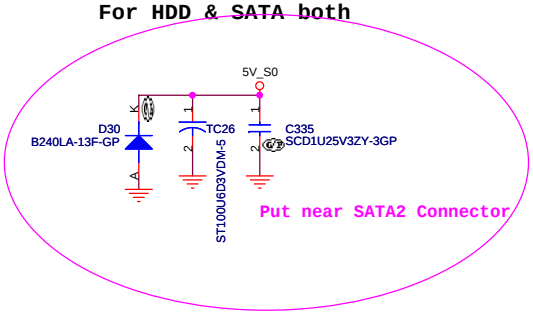
CD-ROM Connector



HDD Connector



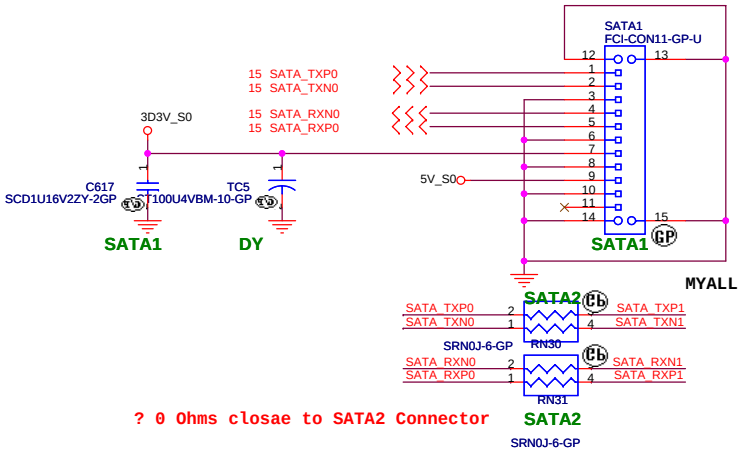
For HDD & SATA both



TC33 CLOSE BETWEEN HDD1 AND SATA1 CONNECTOR.

SATA Connector

PWR TRACE 100mil



MYALL SB RELOAD SYMBOL ADD PIN 12~15

Dummy when use IDE

? 0 Ohms closae to SATA2 Connector

ME : 20.F0777.022

<Core Design>

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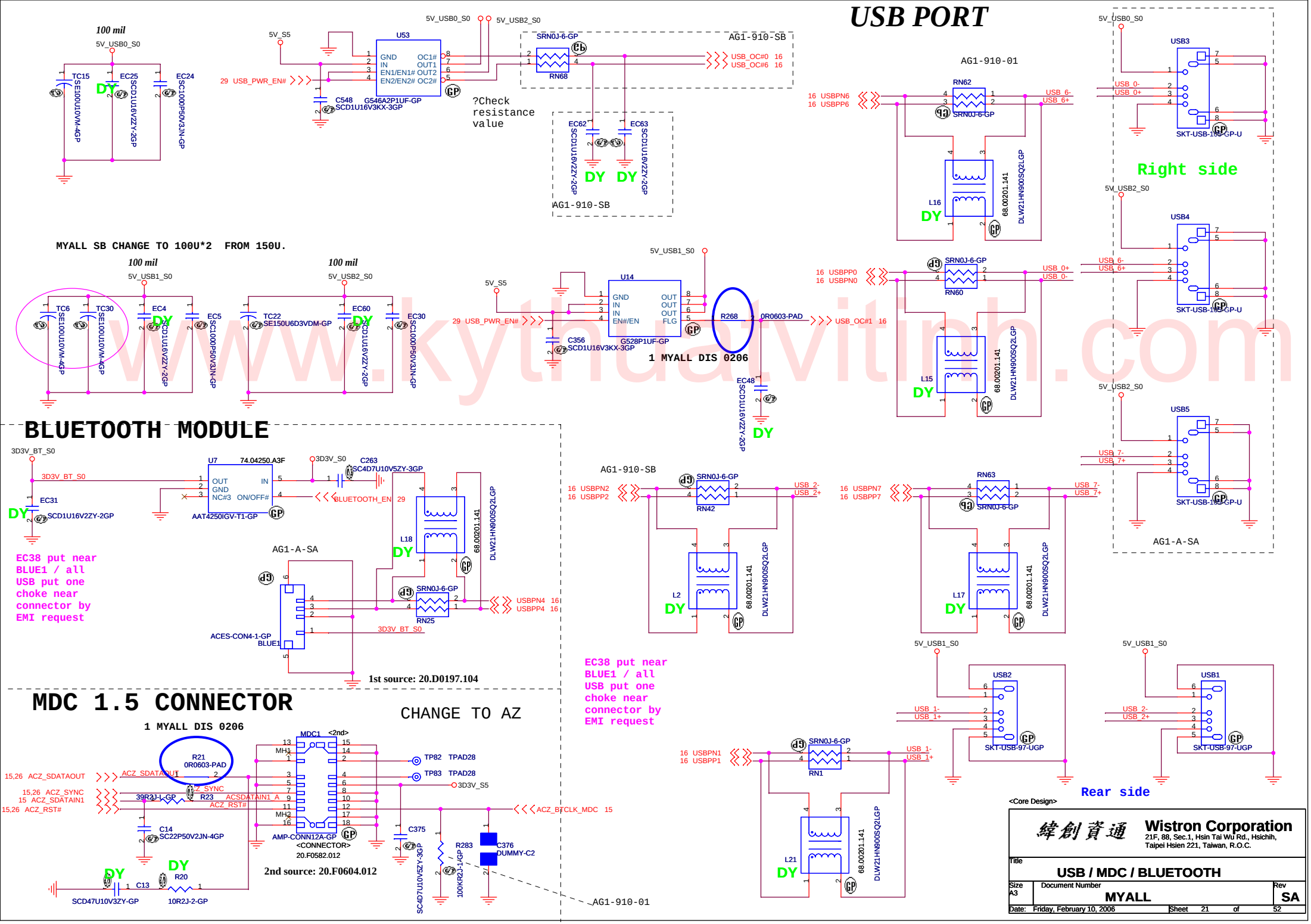
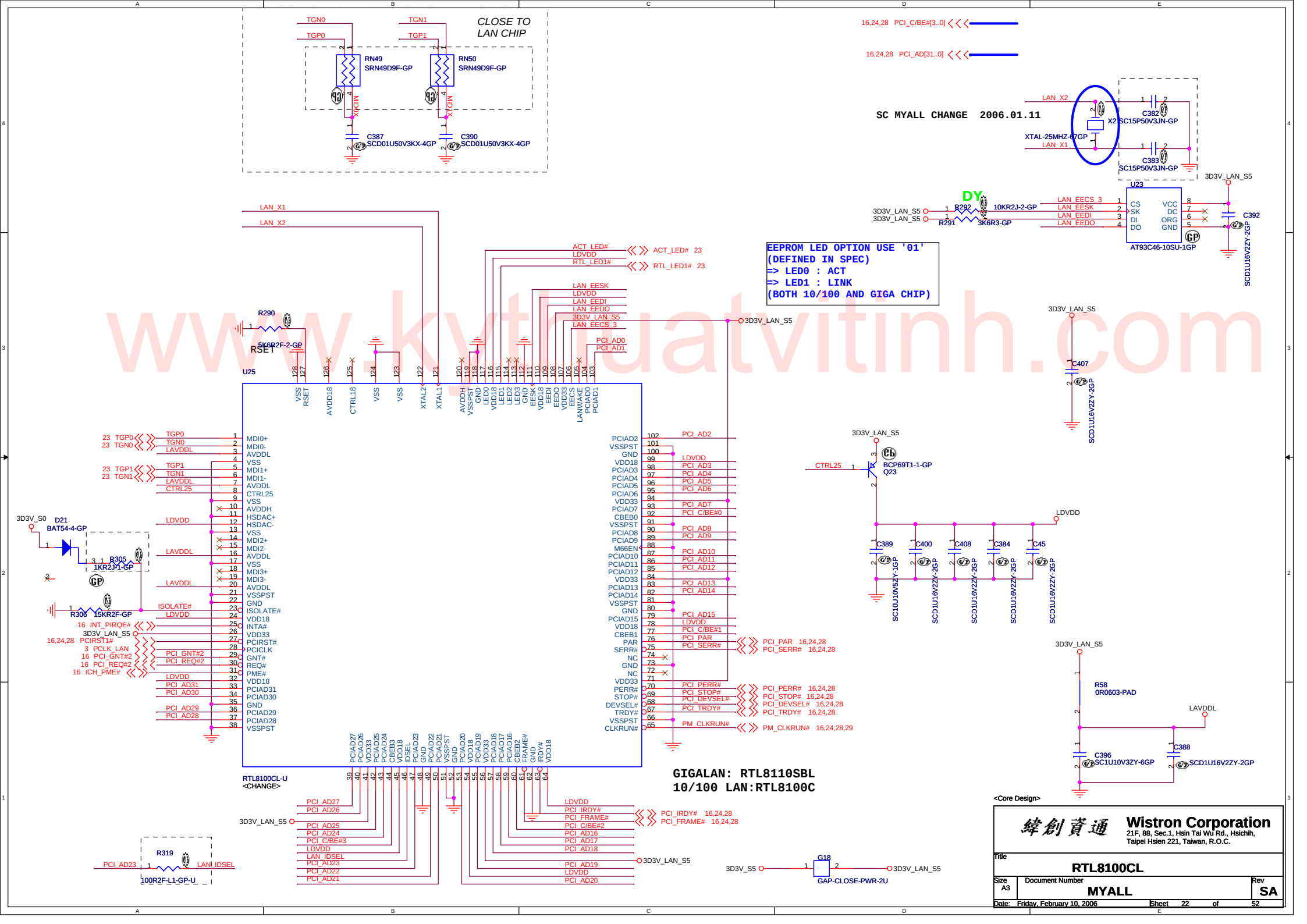
Title: HDD and CDROM

Size	Document Number	Rev
A3	MYALL	SA

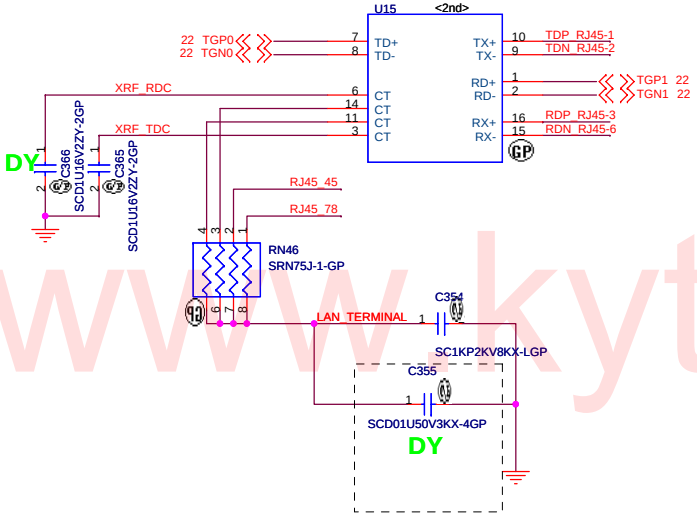
Date: Monday, February 13, 2006 Sheet 20 of 52

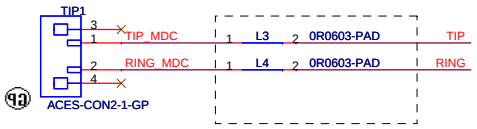
USB PORT





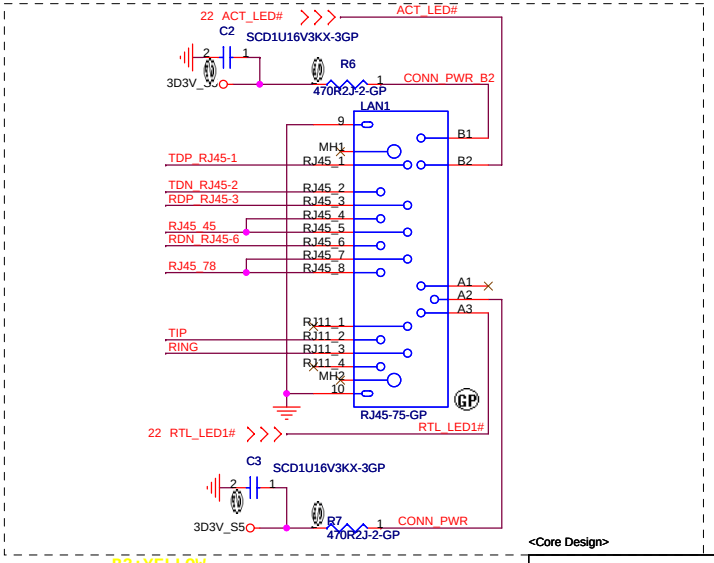
10/100M Lan Transformer





LAN Connector

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.



<Core Design>

B2:YELLOW
A1:ORANGE
A3:GREEN

3D3V_S5 add 0.1u near LAN1 by EMI request

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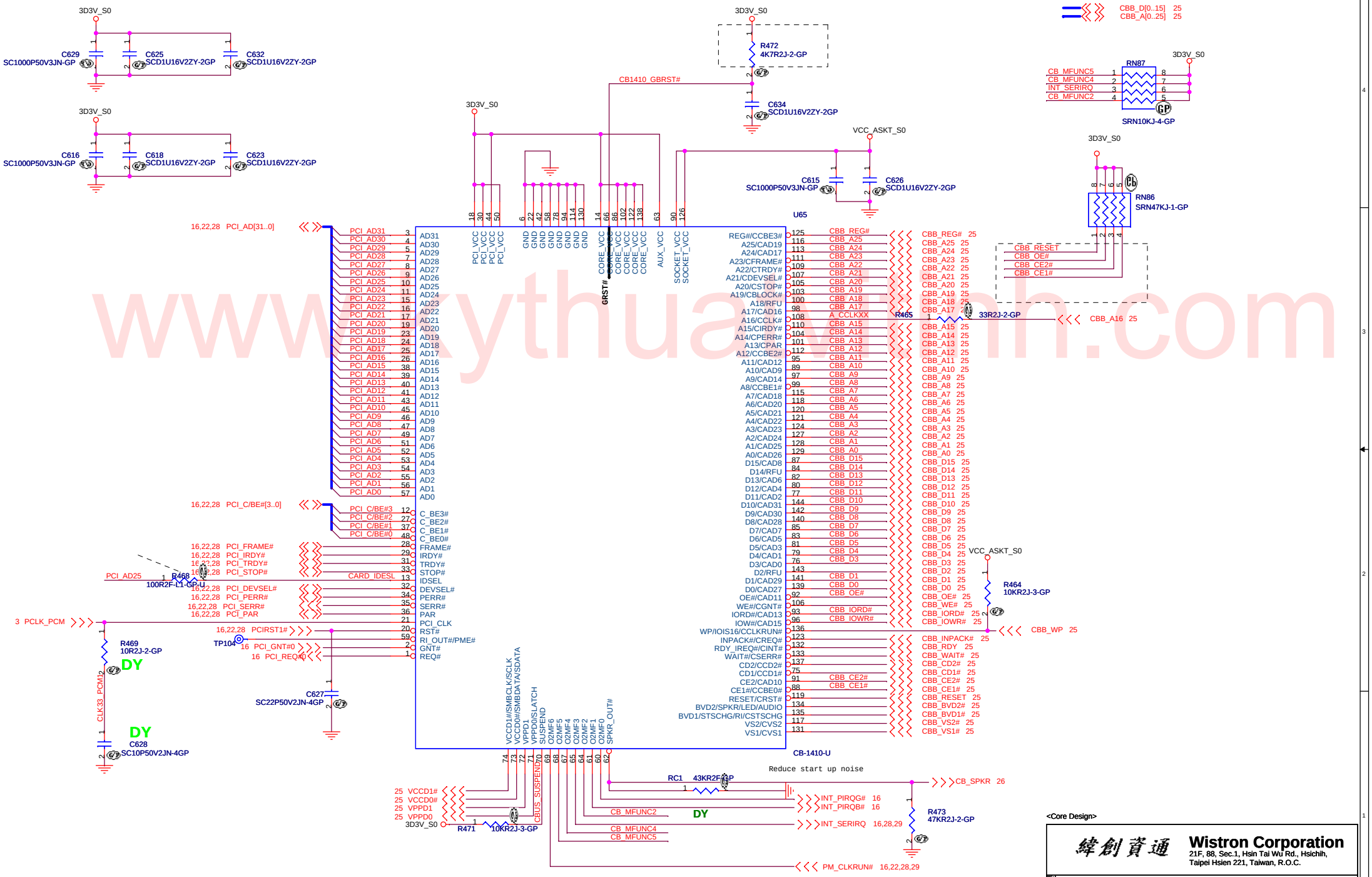
Title	LAN CONN	
Size A3	Document Number MYALL	Rev SA
Date: Friday, February 10, 2006	Sheet 23 of 52	



<Core Design>

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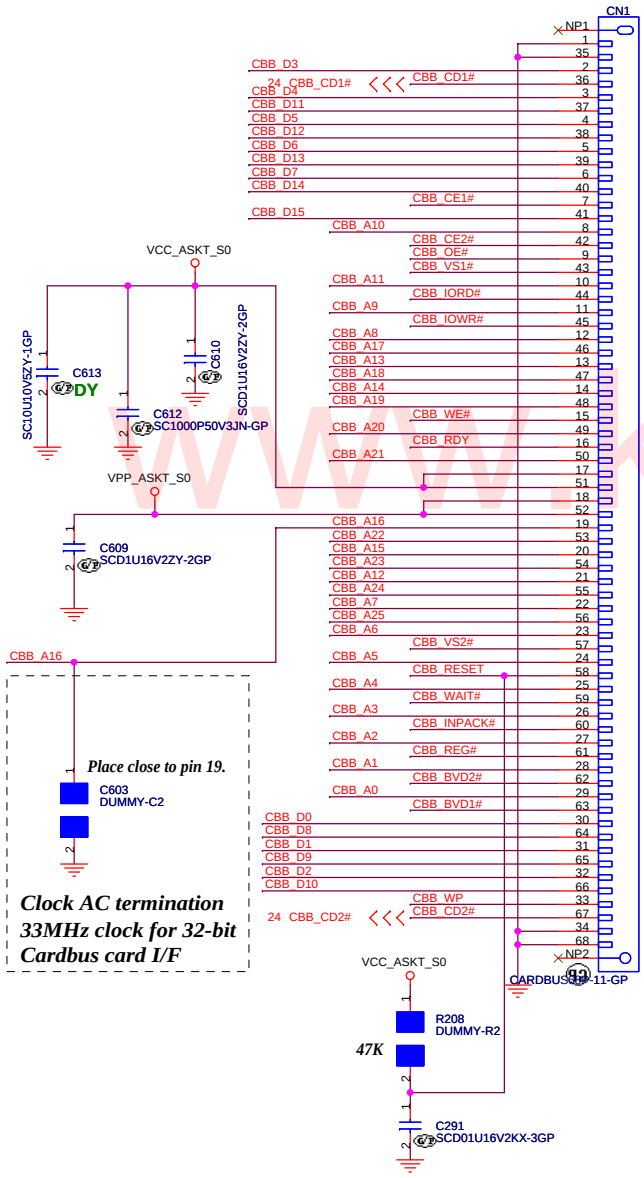
Taipei Hsien 221, Taiwan, R.O.C.

Title: CardBus_ENE CB1410

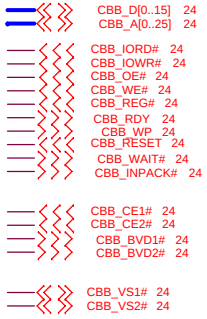
Size	Document Number	Rev
A3	MYALL	SA

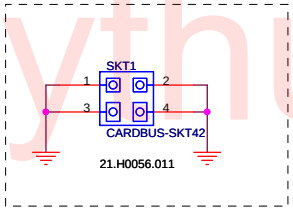
Date: Friday, February 10, 2006 Sheet 24 of 52

PCMCIA Socket

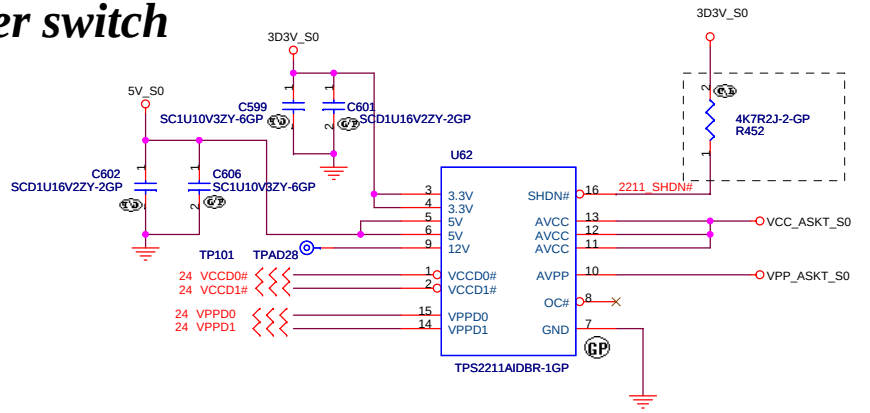


Cardbus I/F

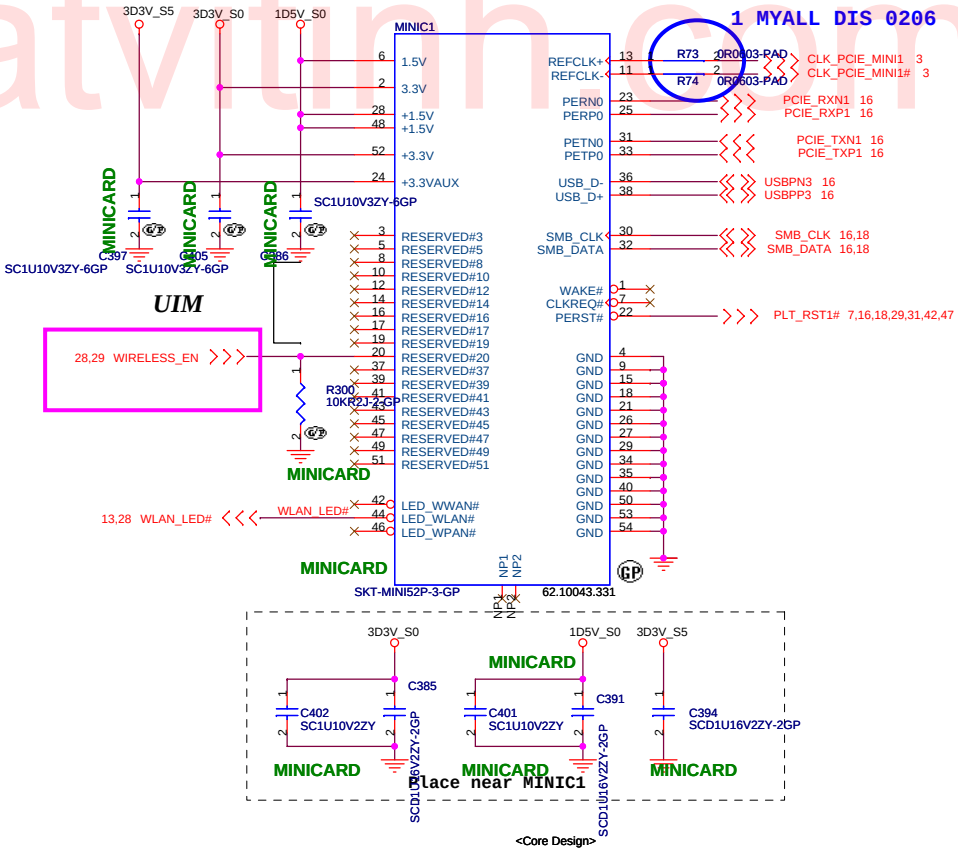




Power switch



Mini Card Connector



<Core Design>

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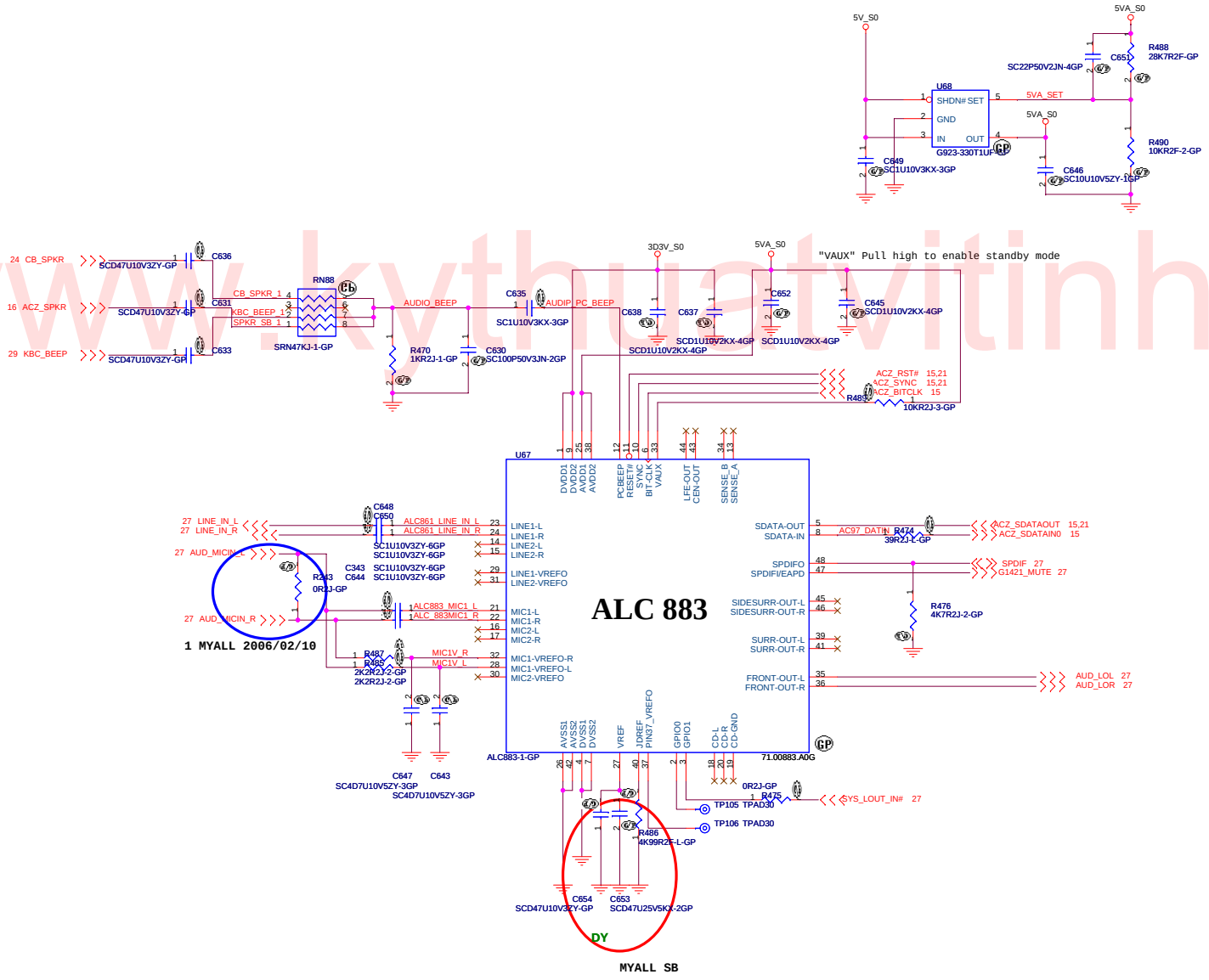
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCMCIA /PCIE MINI CARD

Size	Document Number	Rev
A3	MYALL	SA

Date: Friday, February 10, 2006 Sheet 25 of 52



<Core Design>

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Title: AZALIA CODEC - ALC883

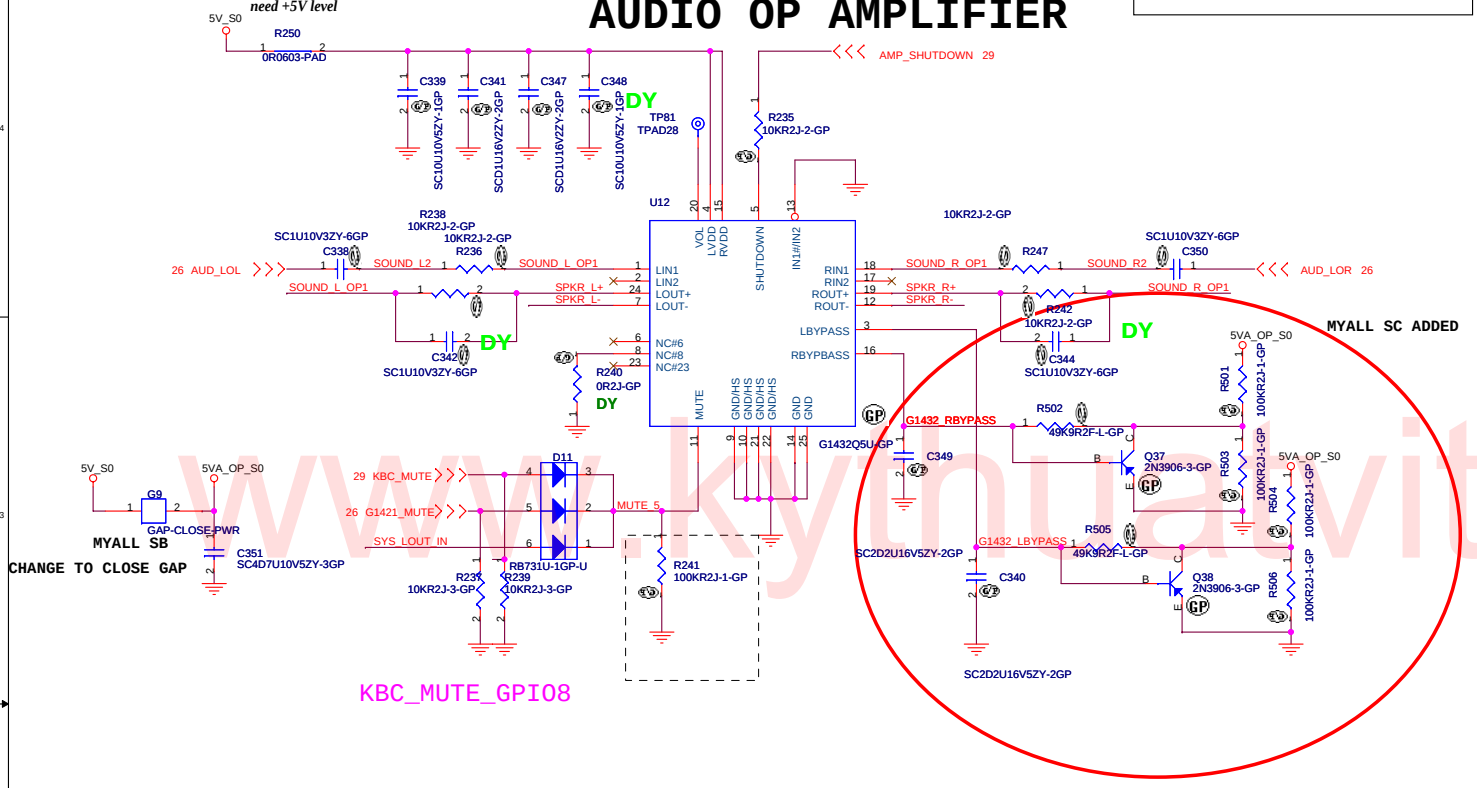
Size	Document Number	Rev
Custom	MYALL	SA

Date: Friday, February 10, 2006 Sheet 26 of 52

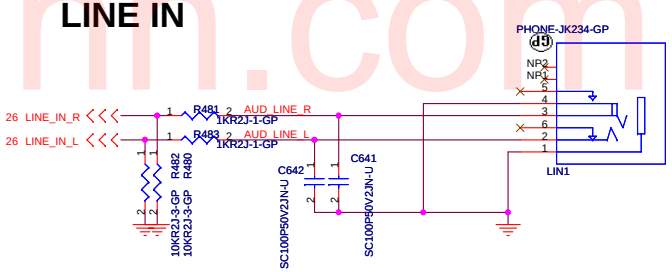
AUDIO OP AMPLIFIER

MYALL SB DELETE GAP

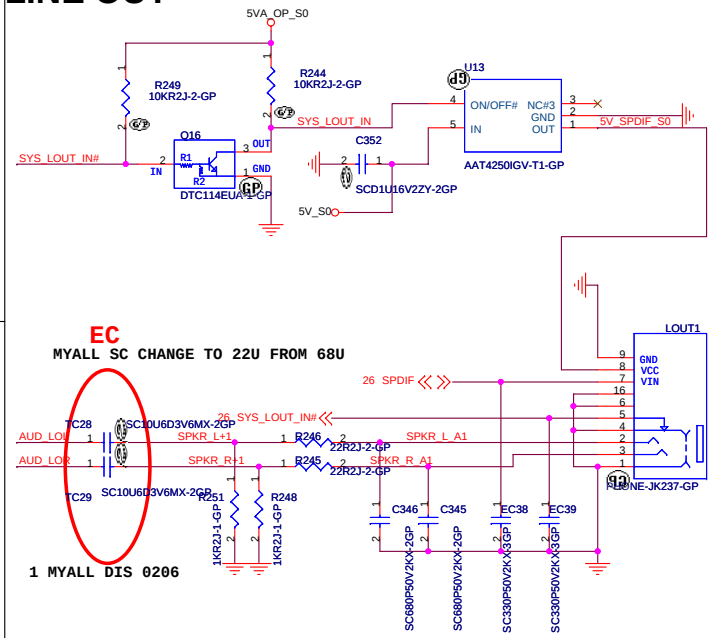
I/P signal level need +5V level



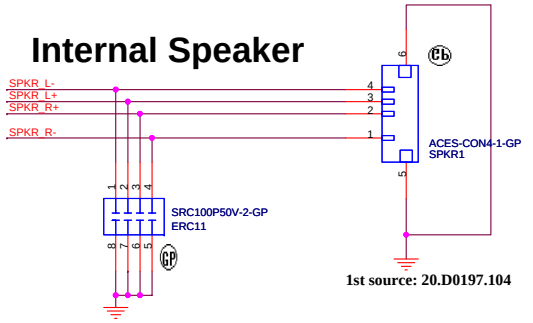
LINE IN



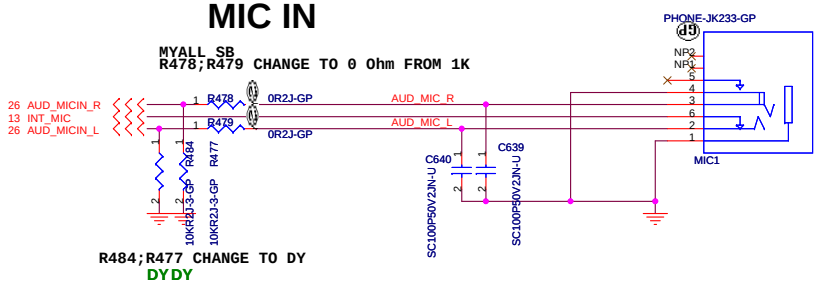
LINE OUT



Internal Speaker



MIC IN



<Core Design>

緯創資通 **Wistron Corporation**
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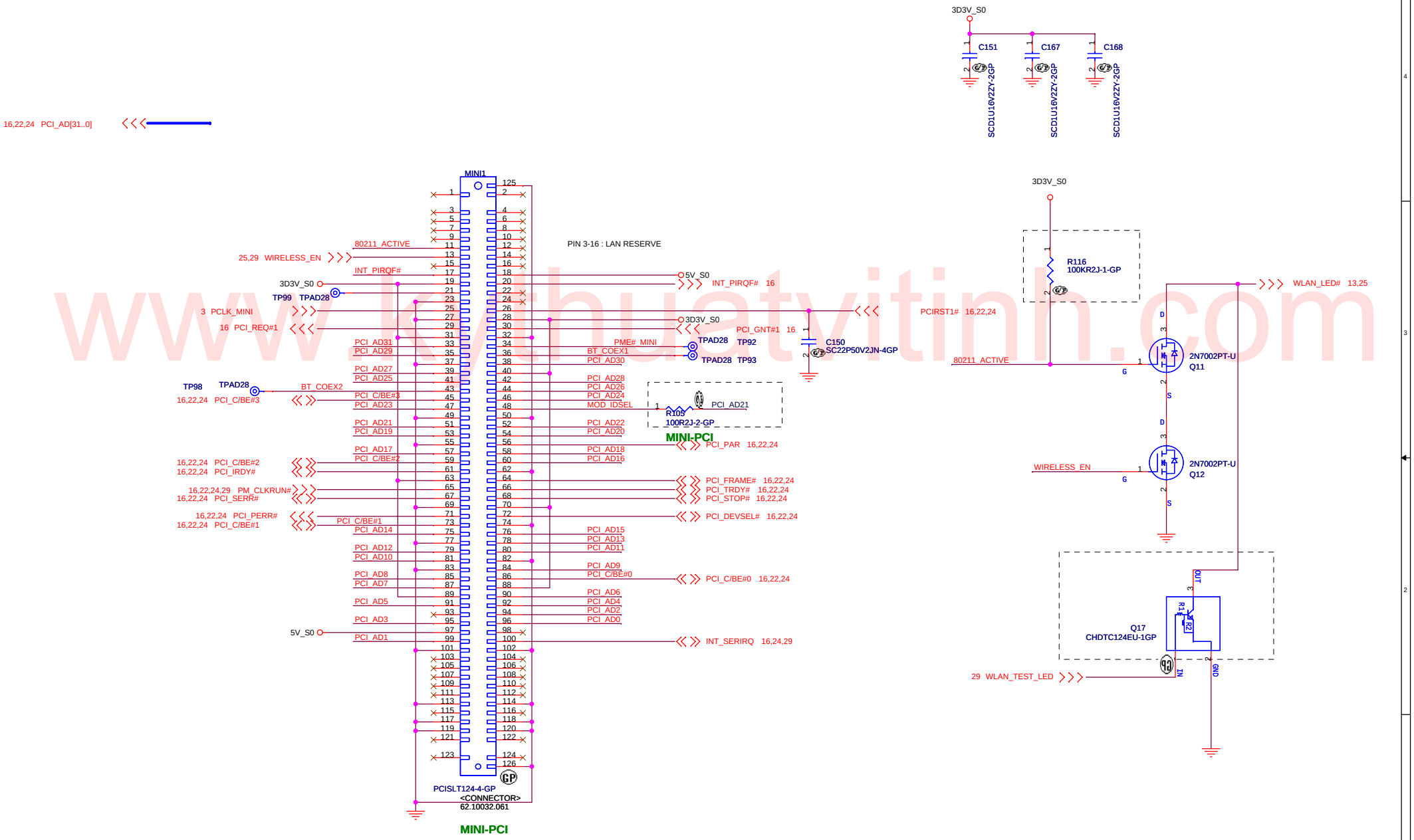
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO AMP AND JACK

Size: | Document Number: MYALL | Rev: SA

Date: Friday, February 10, 2006 Sheet 27 of 52



<Core Design>

緯創資通 Wistron Corporation
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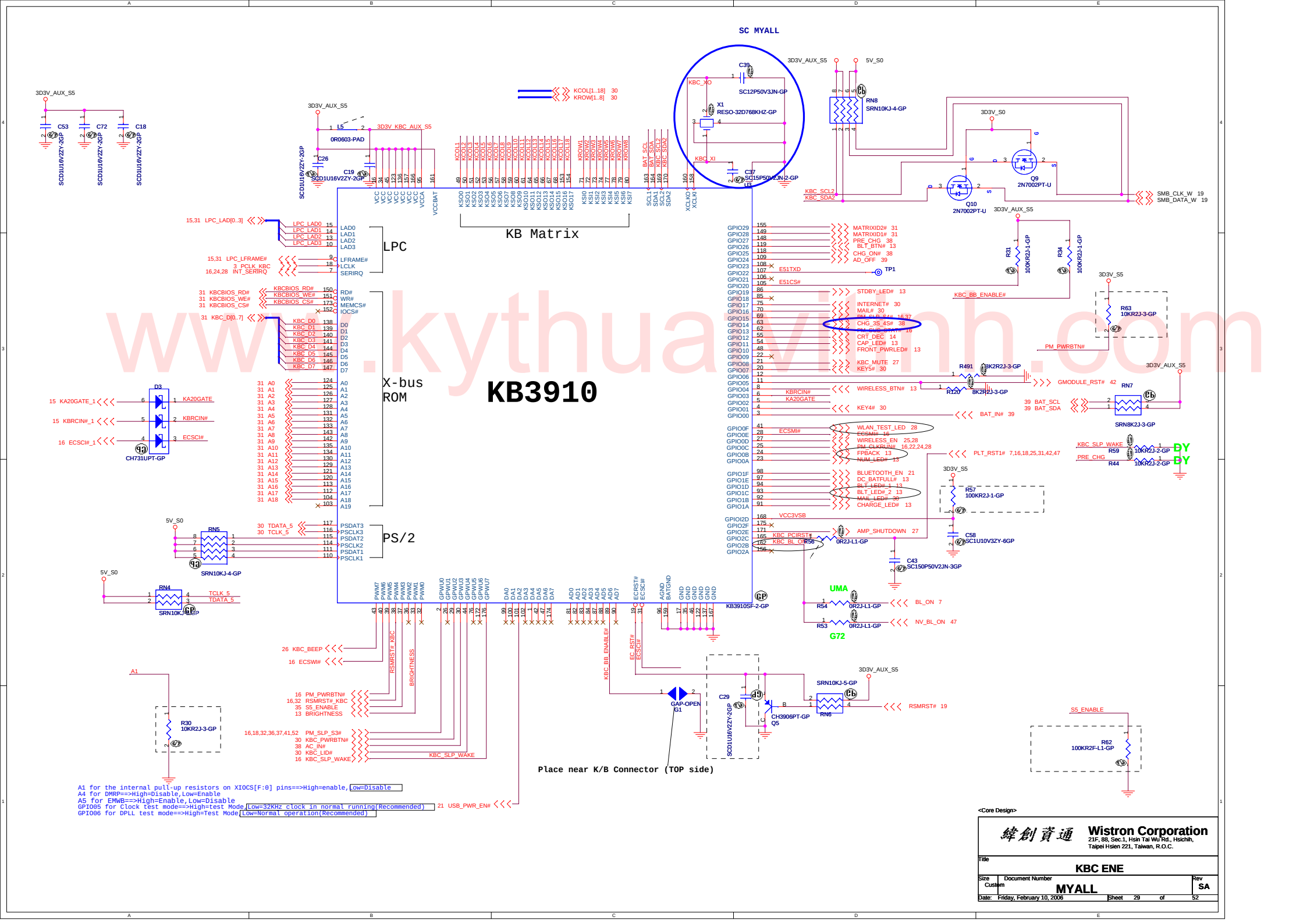
Taipei Hsien 221, Taiwan, R.O.C.

Title: MINI-PCI

Size	Document Number	Rev
A3	MYALL	SA

Date: Friday, February 10, 2006 Sheet 28 of 52


SC MYALL
KB3910
LPC
KB Matrix
X-bus
ROM
PS/2
KB3910SF-2-GP
Place near K/B Connector (TOP side)
A1 for the internal pull-up resistors on XIOCS[F:0] pins==>High=enable,Low=Disable
A4 for DMRP==>High=Disable,Low=Enable
A5 for EMWB==>High=Enable,Low=Disable
GPIO05 for Clock test mode==>High=test Mode,Low=32KHz clock in normal running(Recommended)
GPIO06 for DPLL test mode==>High=Test Mode,Low=Normal operation(Recommended)
UMA
G72
Wistron Corporation
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KBC ENE
MYALL
Date: Friday, February 10, 2006
Sheet 29 of 52

LAUNCH BD CONN

Internet Button

Mail Button

Power Button

2nd source: 20.K0185.012

Program Button

E-Button

POWER LED FOR BUTTON SIDE

MAIL LED FOR BUTTON SIDE

SC MYALL

SC MYALL

Cover Up Switch

TOUCH PAD

2nd source: 62.40009.341

Internal KeyBoard CONN

CHECK KB SPEC. AND PIN DEFINE

EMI Bypass cap.

<Core Design>

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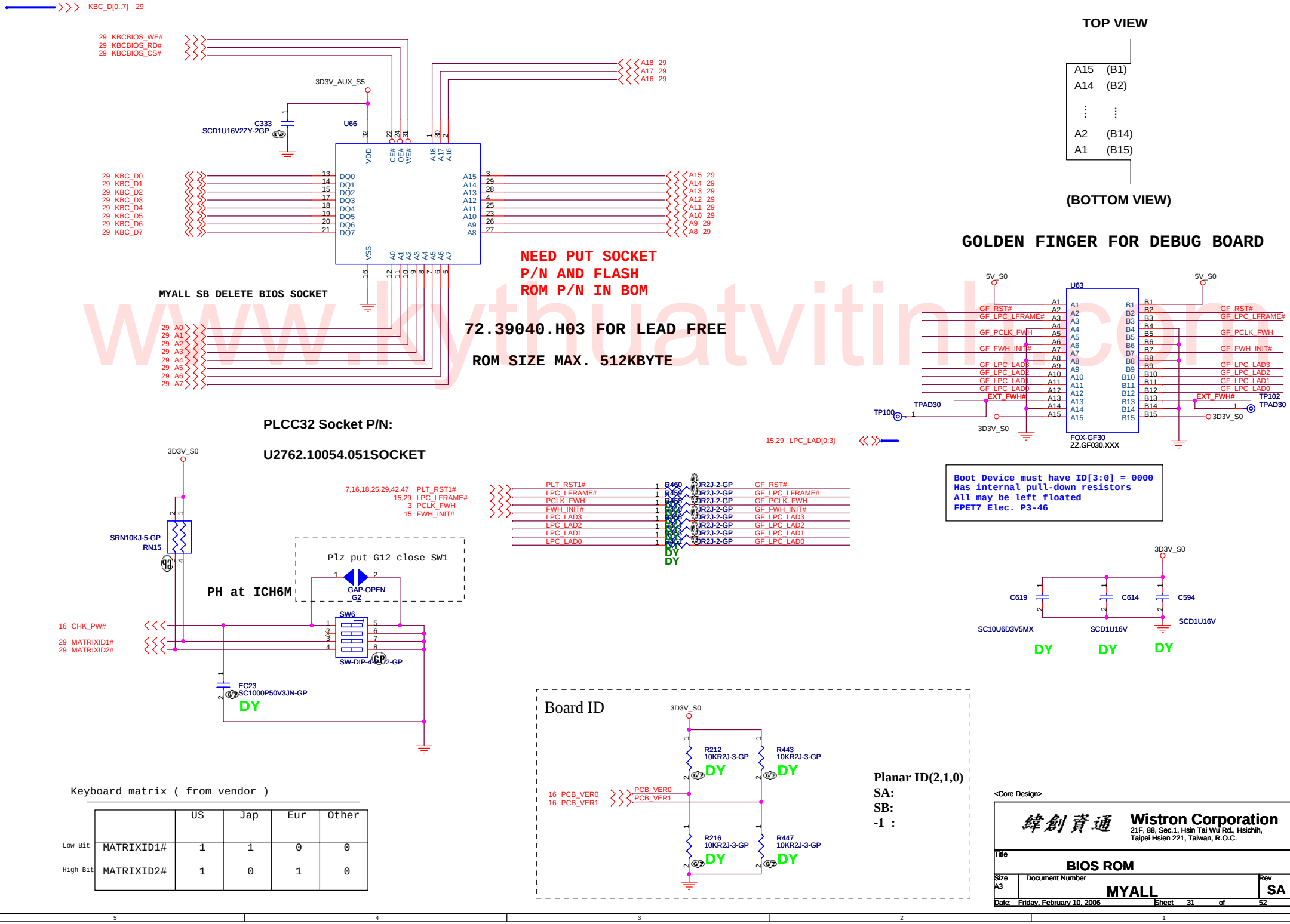
Title: BUTTONs / KB / TOUCHPAD

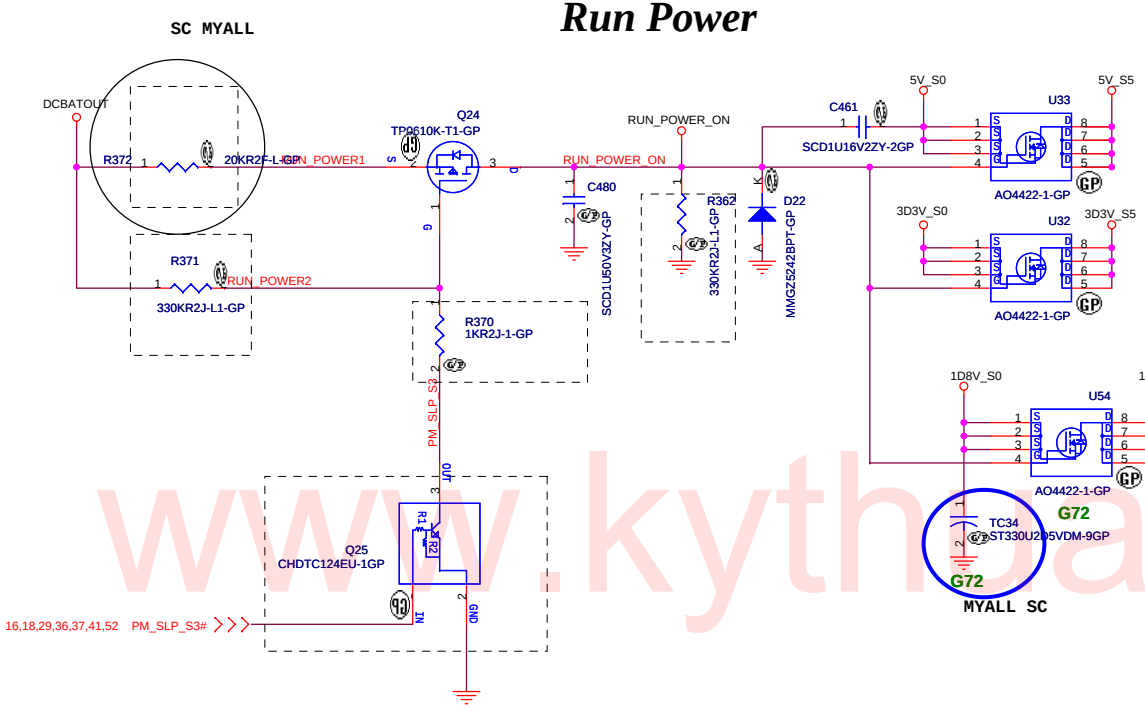
Size: A3 | Document Number: MYALL | Rev: SA

Date: Friday, February 10, 2006 | Sheet 30 of 52

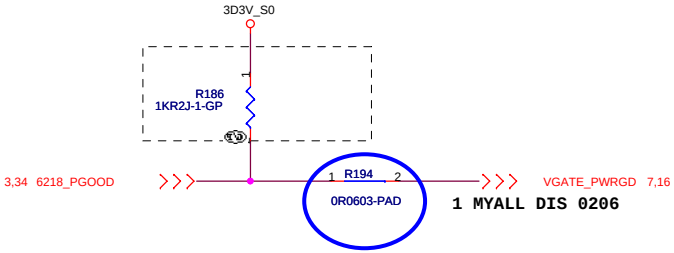


		US	Jap	Eur	Other
Low Bit	MATRIXID1#	1	1	0	0
High Bit	MATRIXID2#	1	0	1	0

Run Power

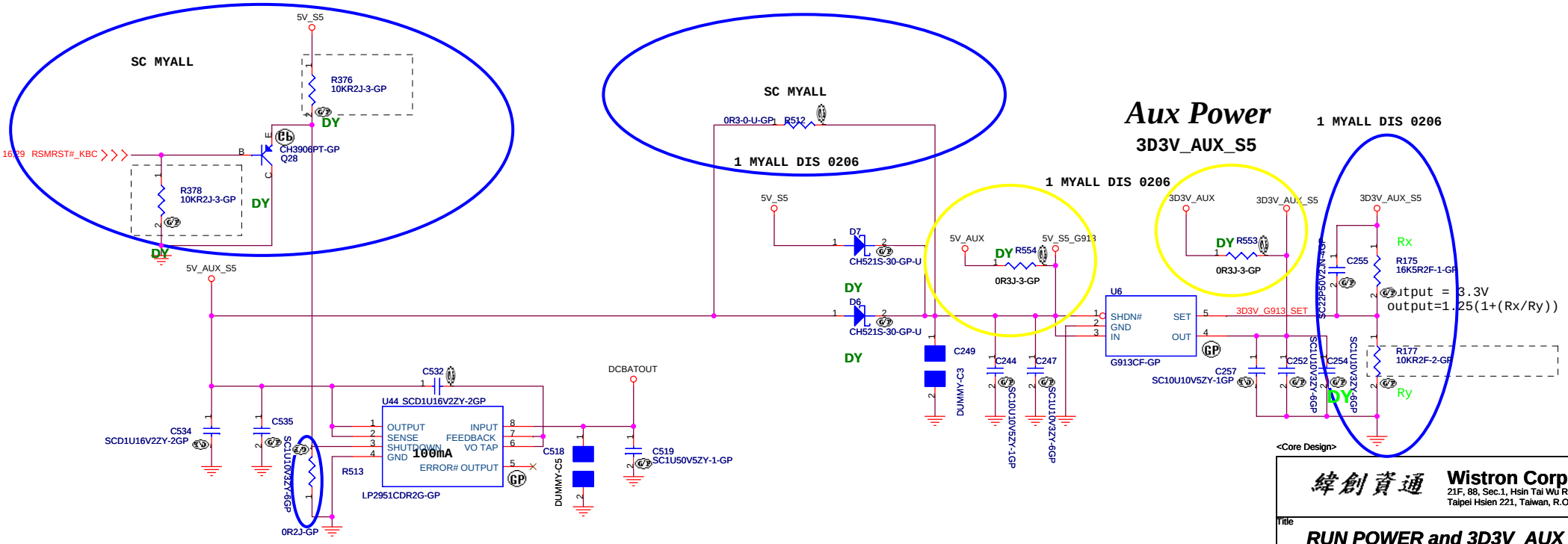


PWRGD for NB and SB



PWRGD to Turn on CPU_Core_Power

Aux Power



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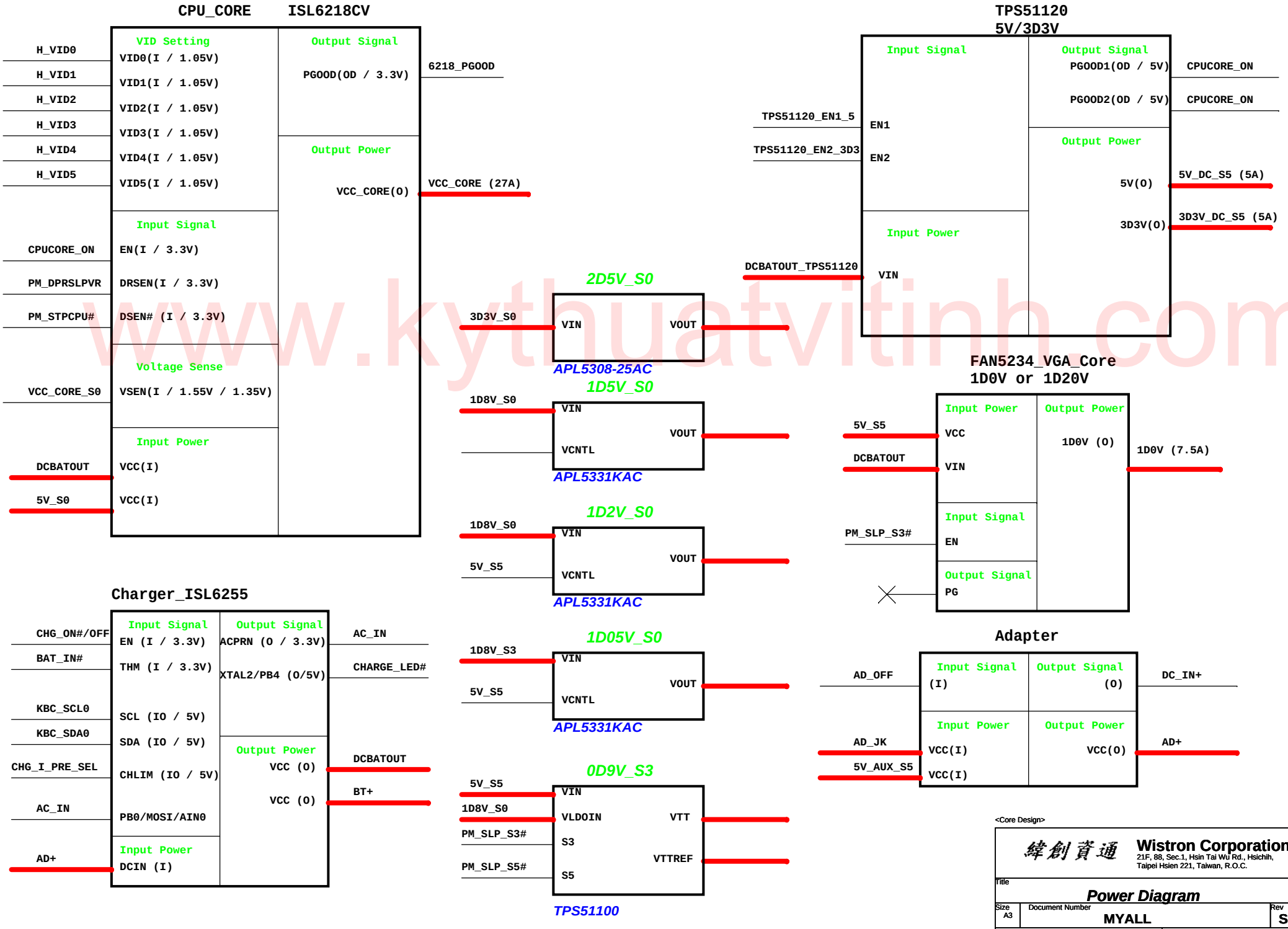
Taipei Hsien 221, Taiwan, R.O.C.

Title	RUN POWER and 3D3V_AUX_S5	
Size A3	Document Number MYALL	Rev SA
Date: Tuesday, February 14, 2006	Sheet 32 of 52	



<Core Design>

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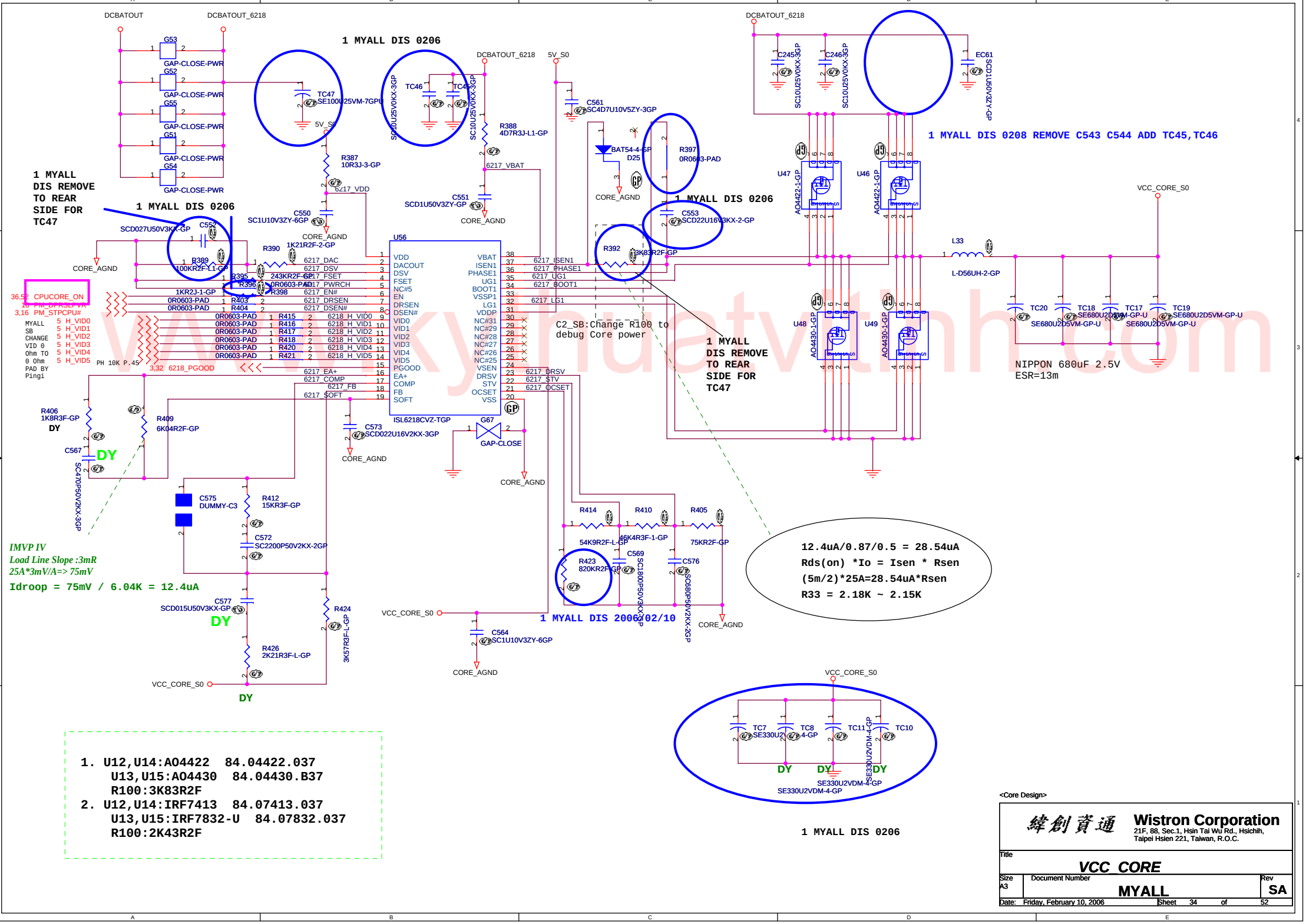
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Diagram

Size: A3 | Document Number: MYALL | Rev: SA

Date: Friday, February 10, 2006 | Sheet 33 of 52



<Core Design>
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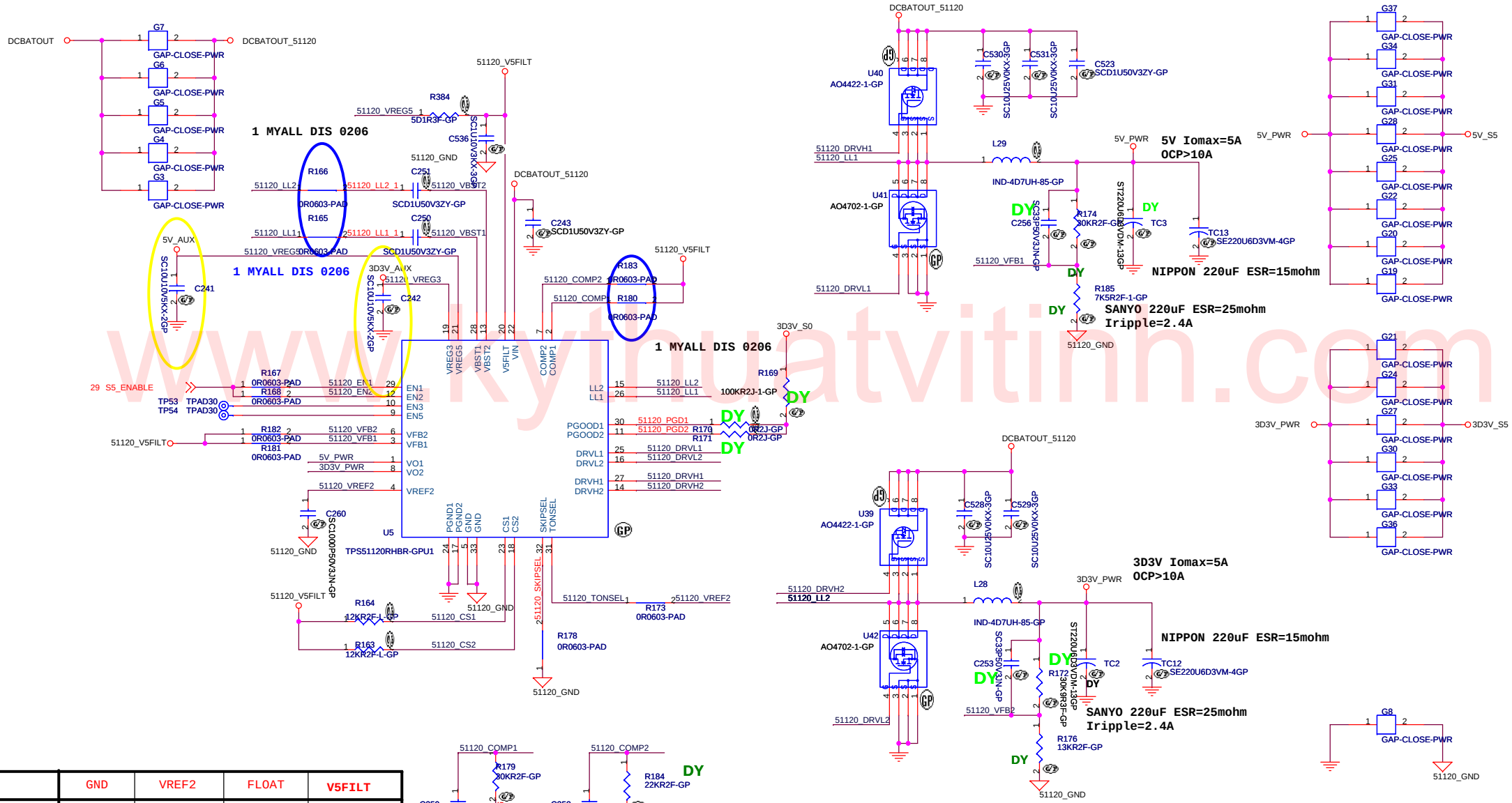
Taipei Hsien 221, Taiwan, R.O.C.

Title: VCC_CORE

Size	Document Number	Rev
A3	MYALL	SA

Date: Friday, February 10, 2006 Sheet 34 of 52



	GND	VREF2	FLOAT	V5FILT
SKIPSEL	**AUTOSKIP**	AUTOSKIP /FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	**D-Cap MODE**
TONSEL	380k/CH1 590k/CH2	**290k/CH1 440k/CH2**	220k/CH1 330k/CH2	180k/CH1 280k/CH2
VFB1	N/A	not use	ADJ.	**5V Fixed Output**
VFB2	N/A	not use	ADJ.	**3.3V Fixed Output**
EN1,EN2	Switcher OFF	not use	**Swithchr ON**	**Switcher ON**
EN3,EN5	LDO OFF	not use	**LDO ON**	VREG3 on

For TPS51120,
Vout=5V
1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.

Vout=3.3V
1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
3. If you use a 2.5uH inductor, the minimum ESR is 27m ohm.

<Core Design>

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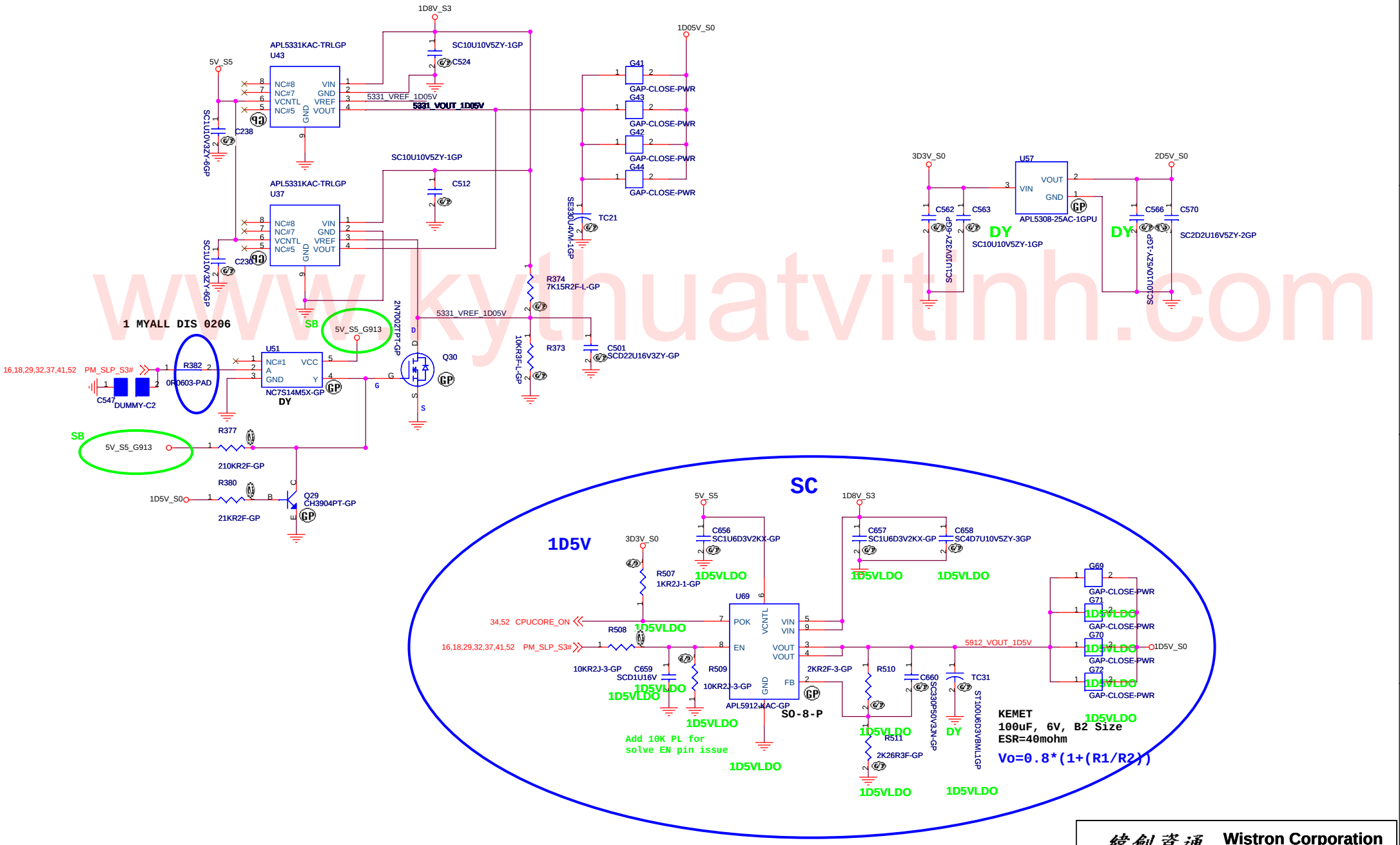
Title: TPS51120 / 3D3V / 5V

Size: A3 | Document Number: MYALL | Rev: SC

Date: Friday, February 10, 2006 | Sheet 35 of 52



Wistron Corporation	緯創資通
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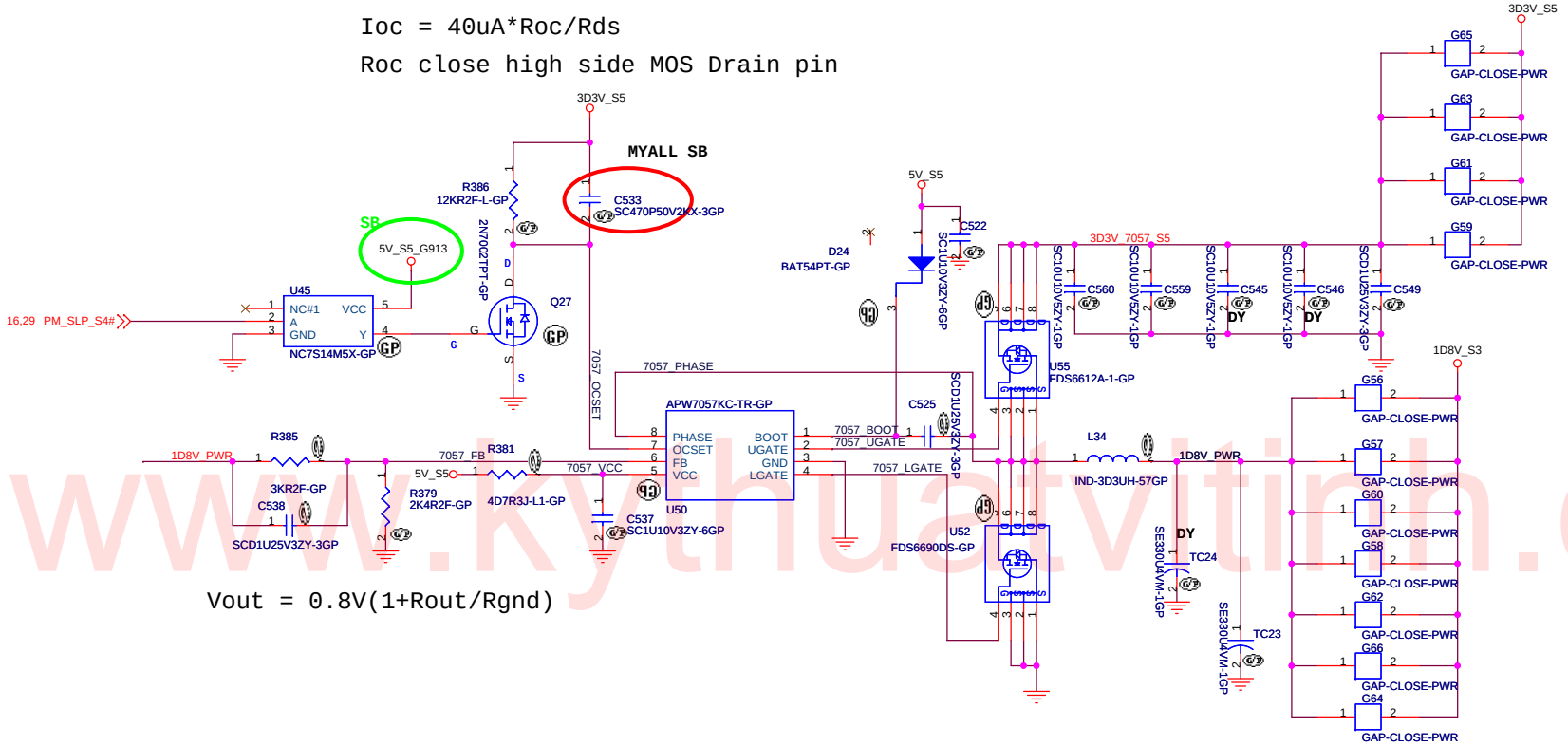
Title	1D5V / 1D05V / 2D5V
Size A3	Document Number MYALL
Rev	SA
Date: Friday, February 10, 2006	Sheet 36 of 52

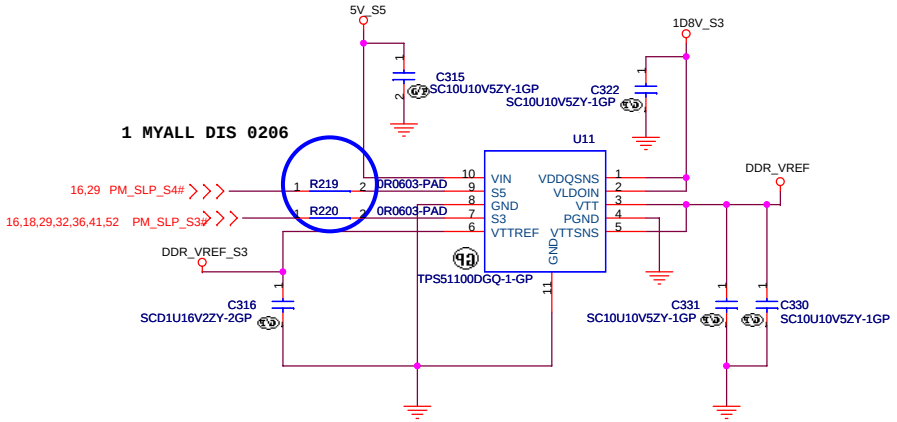
Ioc = 40uA*Roc/Rds

Roc close high side MOS Drain pin



Vout = 0.8V(1+Rout/Rgnd)

0D9V



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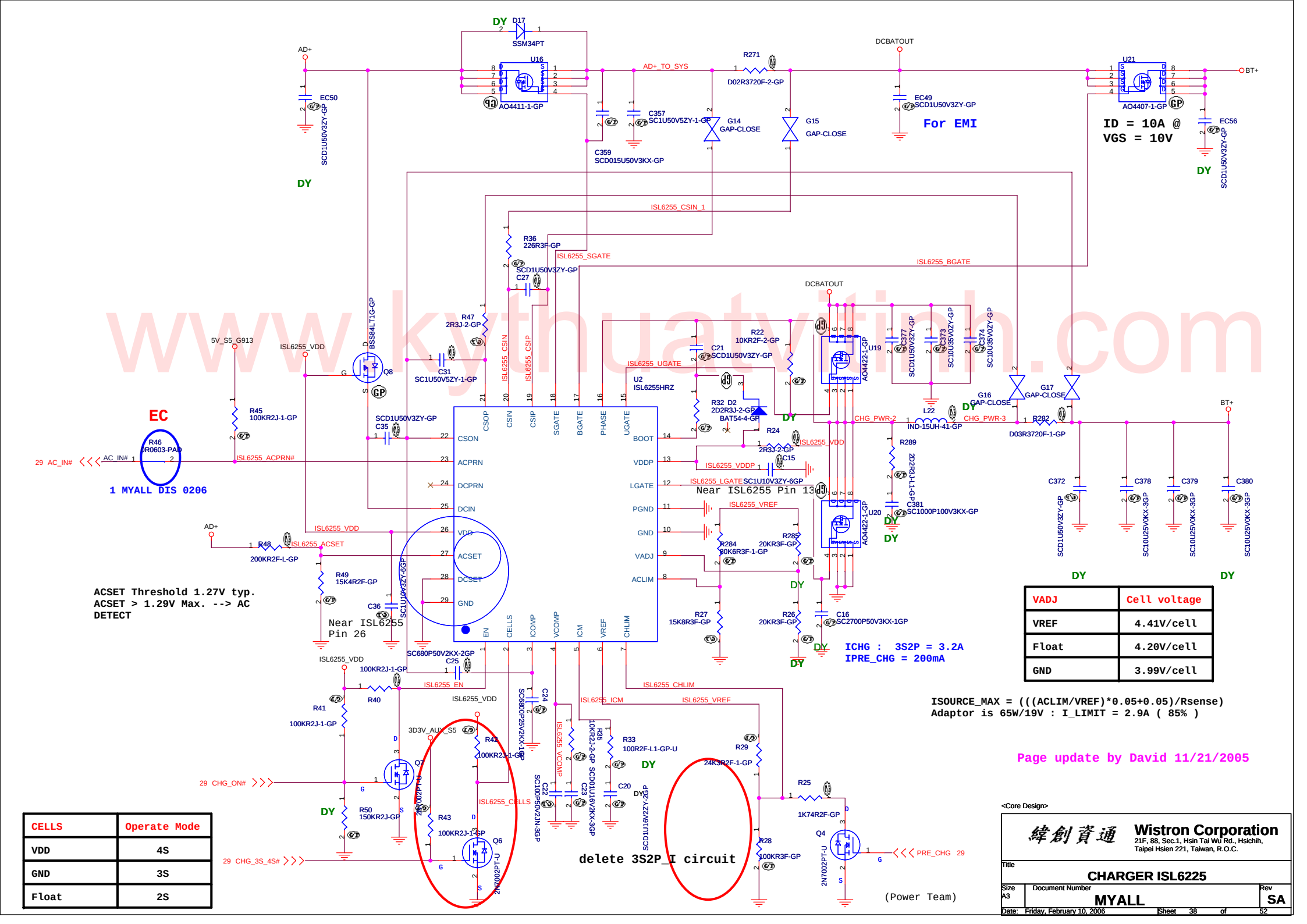
Title	APW7057 / 1D8V/0D9V	
Size A3	Document Number MYALL	Rev SA
Date: Friday, February 10, 2006	Sheet 37 of 52	



VADJ	Cell voltage
VREF	4.41V/cell
Float	4.20V/cell
GND	3.99V/cell

CELLS	Operate Mode
VDD	4S
GND	3S
Float	2S

ISOURCE_MAX = (((ACLIM/VREF)*0.05+0.05)/Rsense)
Adaptor is 65W/19V : I_LIMIT = 2.9A (85%)

Page update by David 11/21/2005

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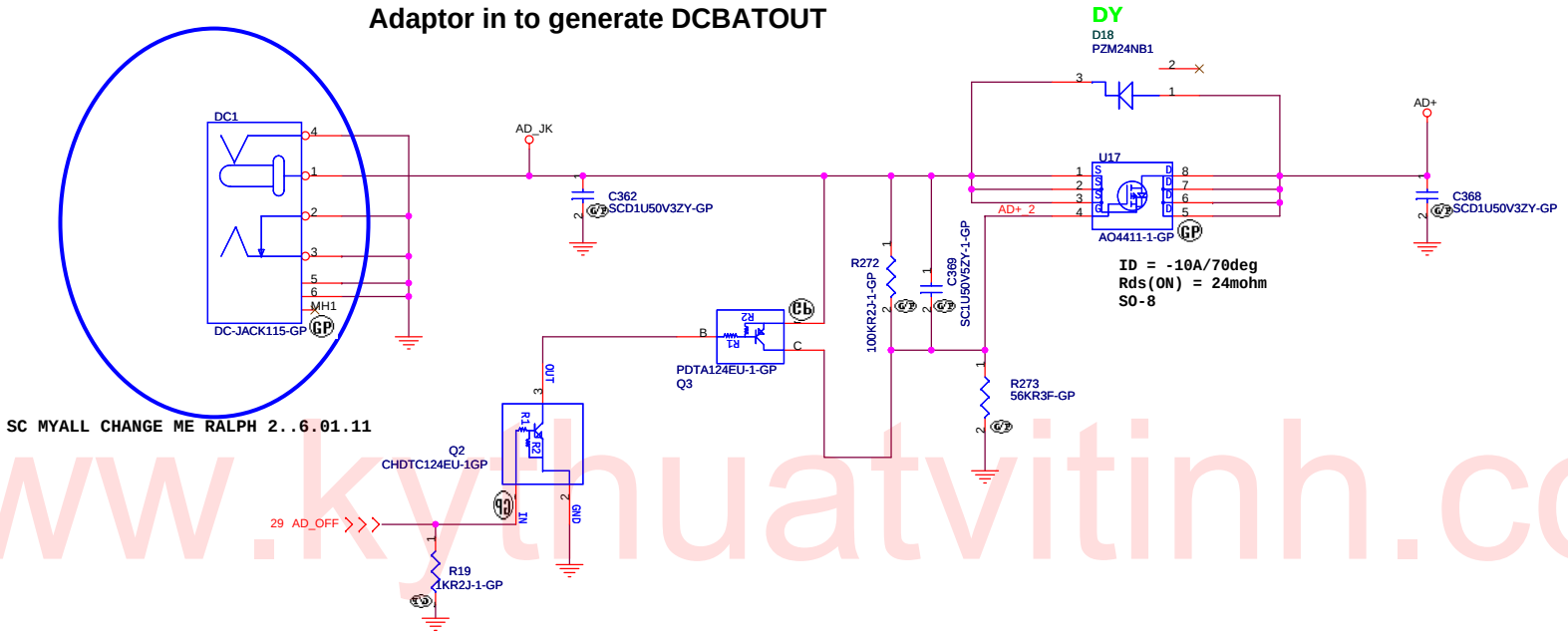
Title: CHARGER ISL6225

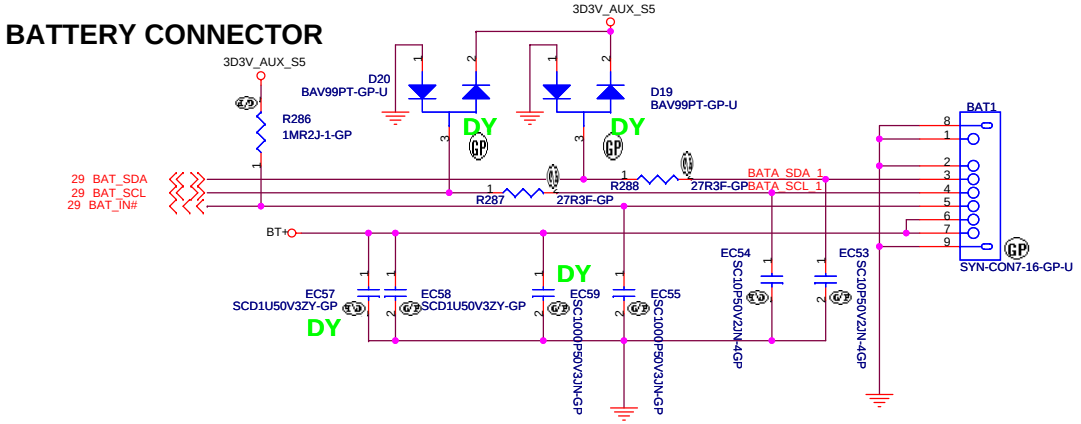
Size: A3 | Document Number: MYALL | Rev: SA

Date: Friday, February 10, 2006 | Sheet 38 of 52

Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



Page update by David 11/21/2005

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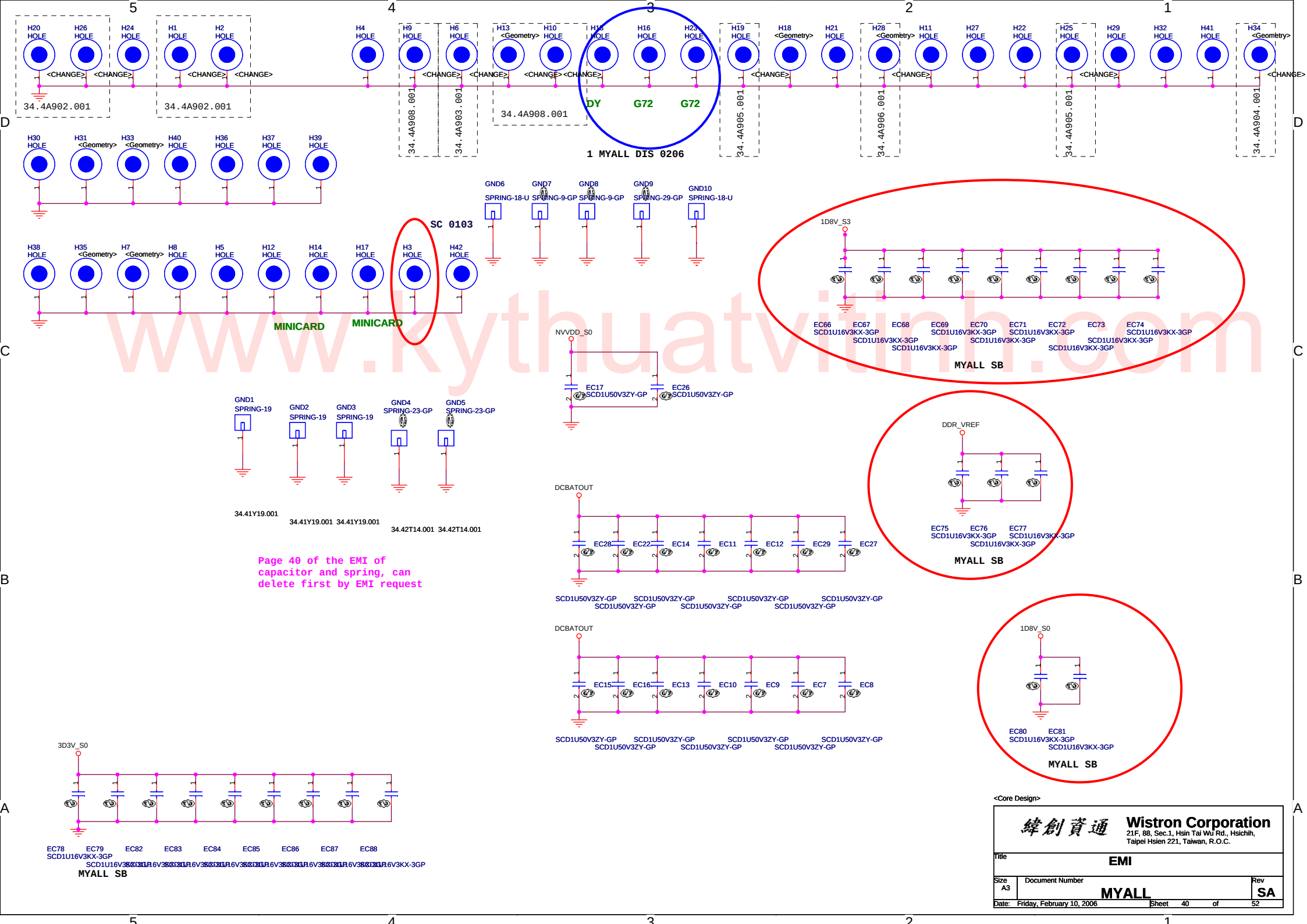
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**AD/BATT CONN**
Size: A3	Document Number: **MYALL** Rev: **SA**
Date: Friday, February 10, 2006	Sheet 39 of 52



Page 40 of the EMI of capacitor and spring, can delete first by EMI request

<Core Design>

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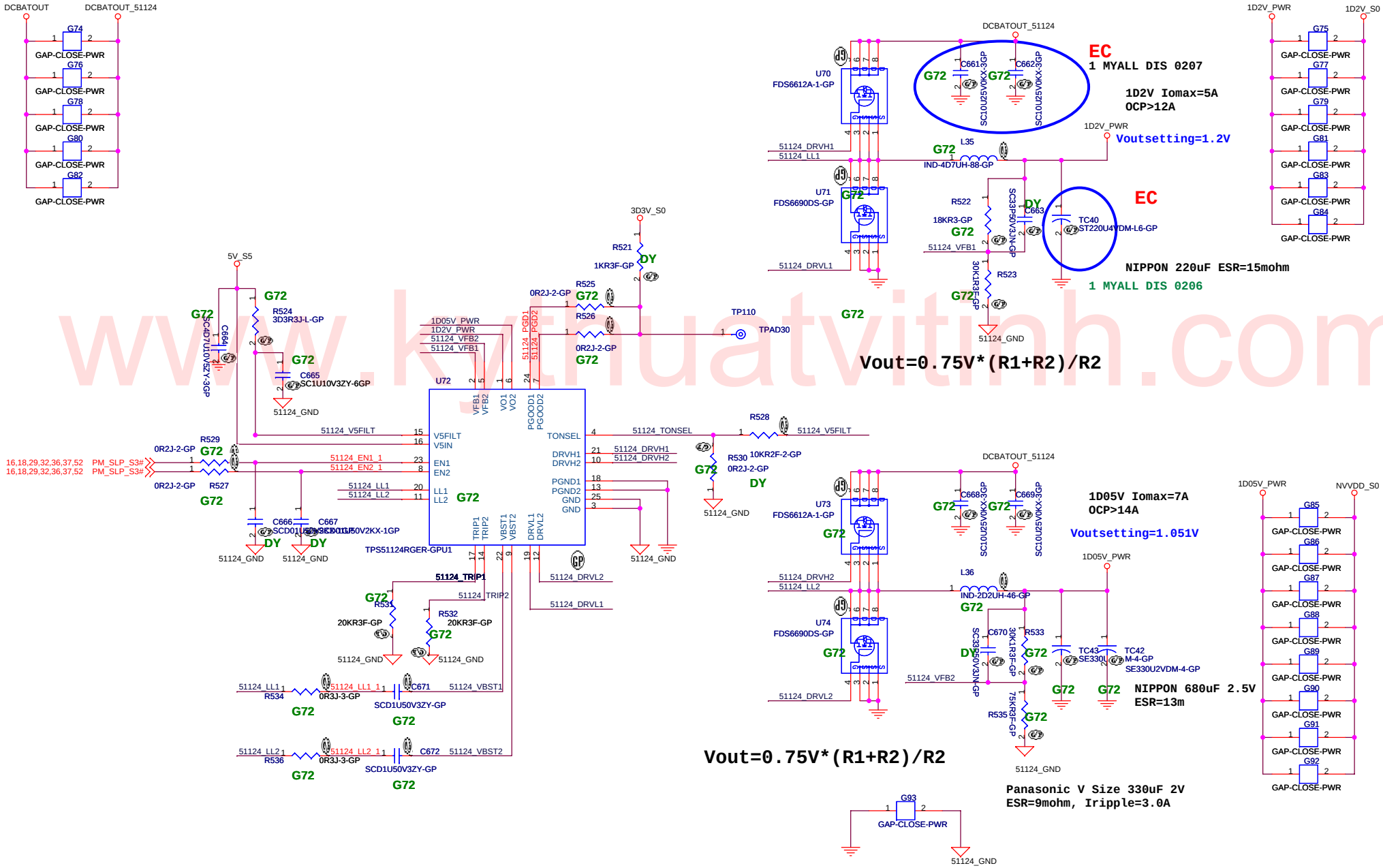
Taipei Hsien 221, Taiwan, R.O.C.

Title	EMI	
Size A3	Document Number MYALL	Rev SA
Date: Friday, February 10, 2006	Sheet 40 of 52	



	GND	OPEN	V5FILT
TONSEL	230k/CH1 283k/CH2	283k/CH1 346k/CH2	346k/CH1 423k/CH2

<Core Design>

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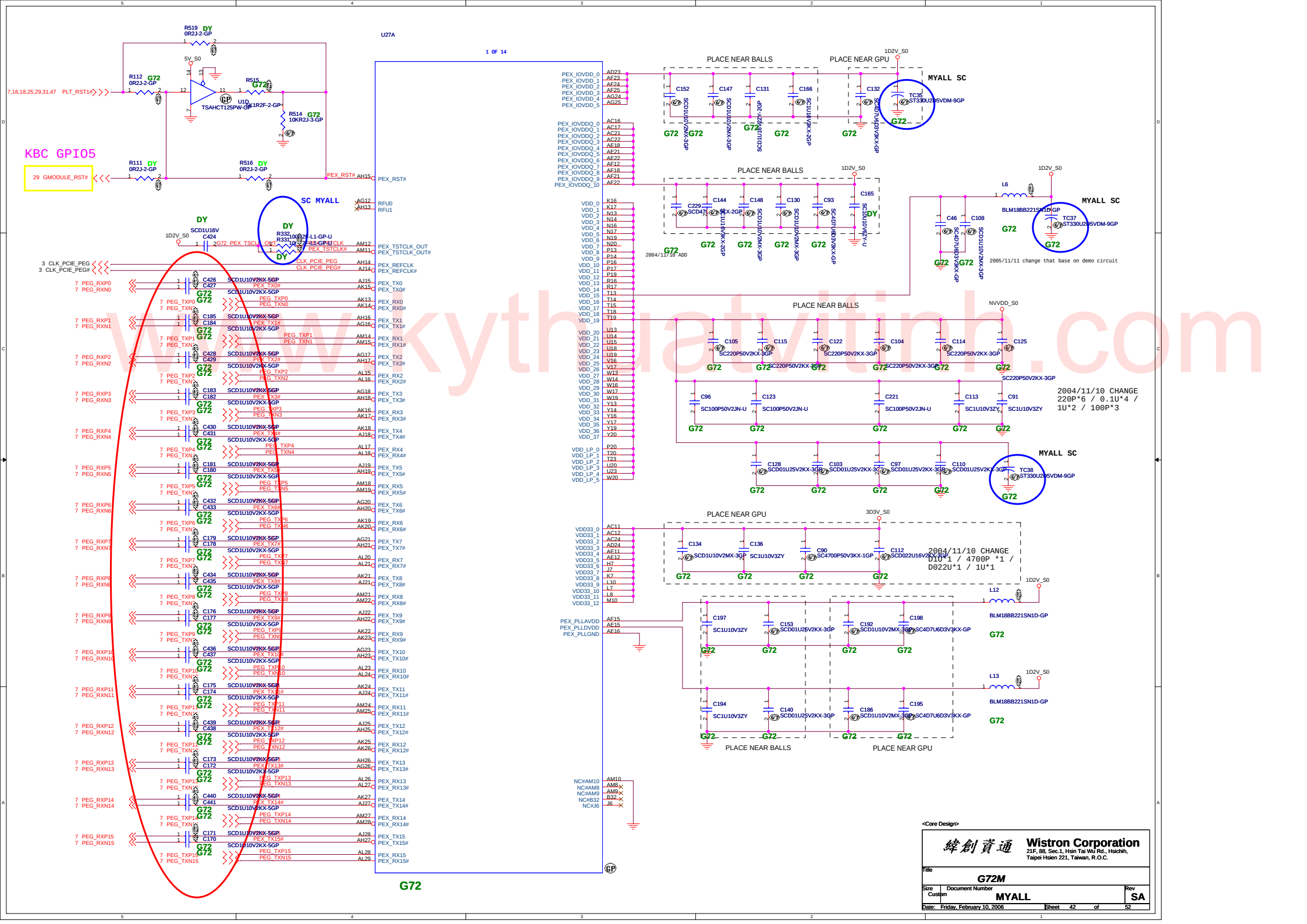
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51124 / NVDD/1D2V

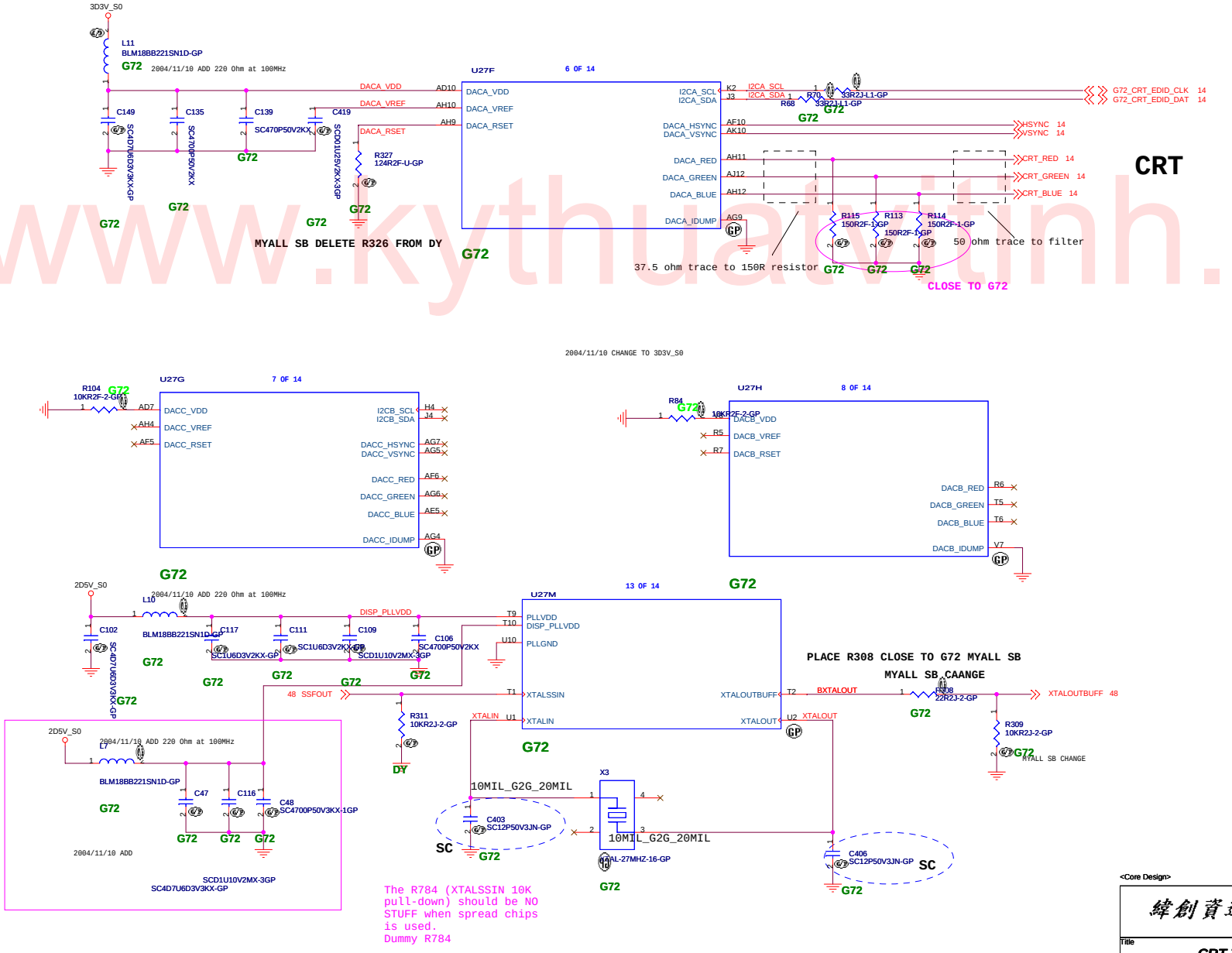
Size: A3 | Document Number: MYALL | Rev: SC

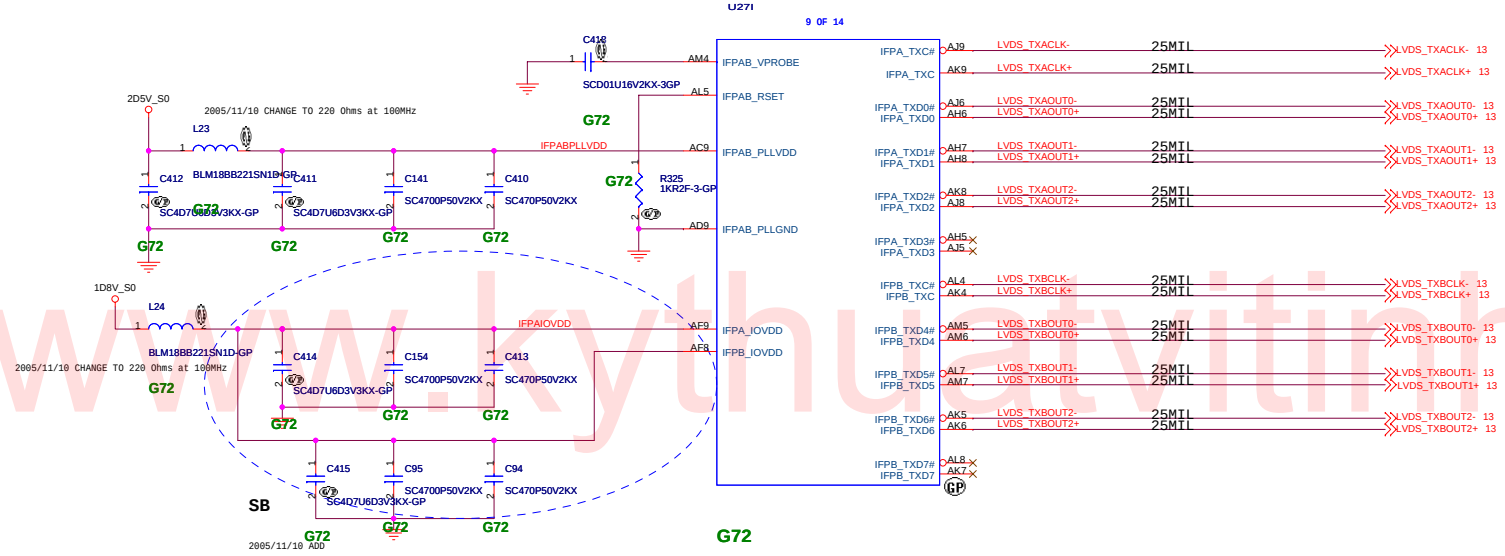
Date: Friday, February 10, 2006 | Sheet 41 of 52

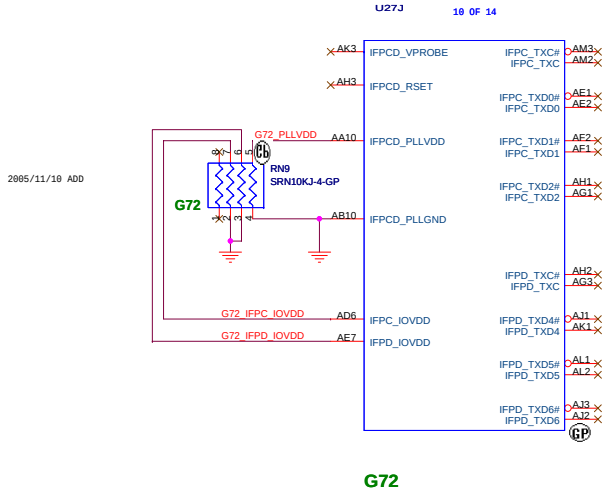


<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	G72M		
Size: Custom	Document Number: MYALL		Rev: SA
Date: Friday, February 10, 2006	Sheet 42 of 52		







<Core Design>

緯創資通 **Wistron Corporation**
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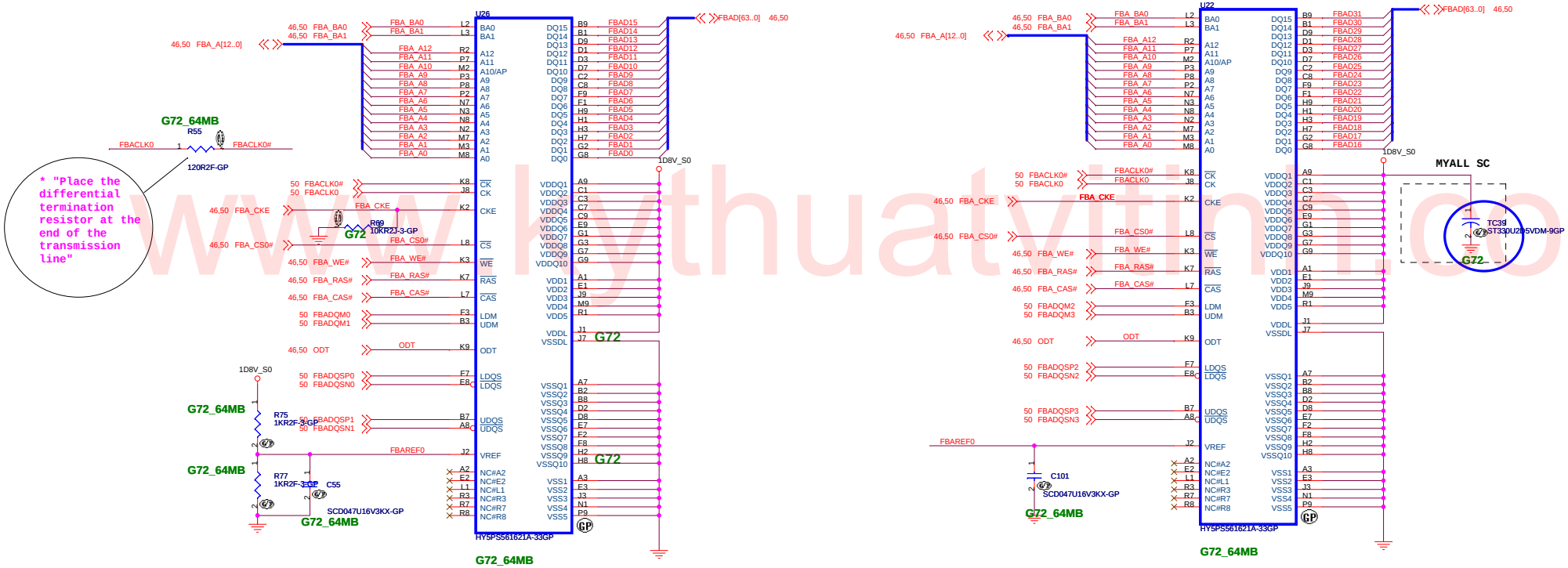
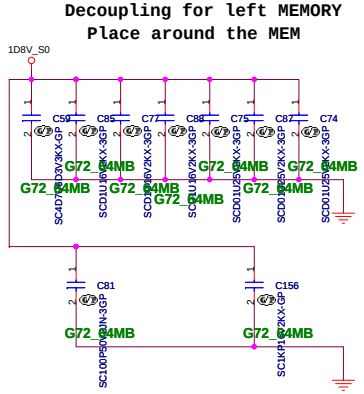
Taipei Hsien 221, Taiwan, R.O.C.

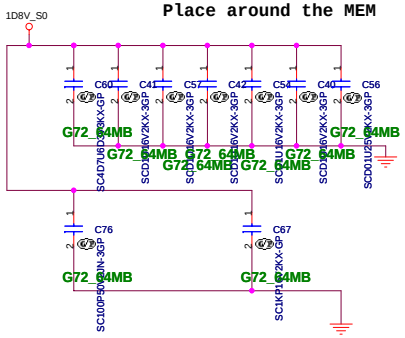
Title: **LVDS,TMDS**

Size	Document Number	Rev
Custom	MYALL	SA

Date: Friday, February 10, 2006 Sheet 44 of 52







<Core Design>

緯創資通 Wistron Corporation
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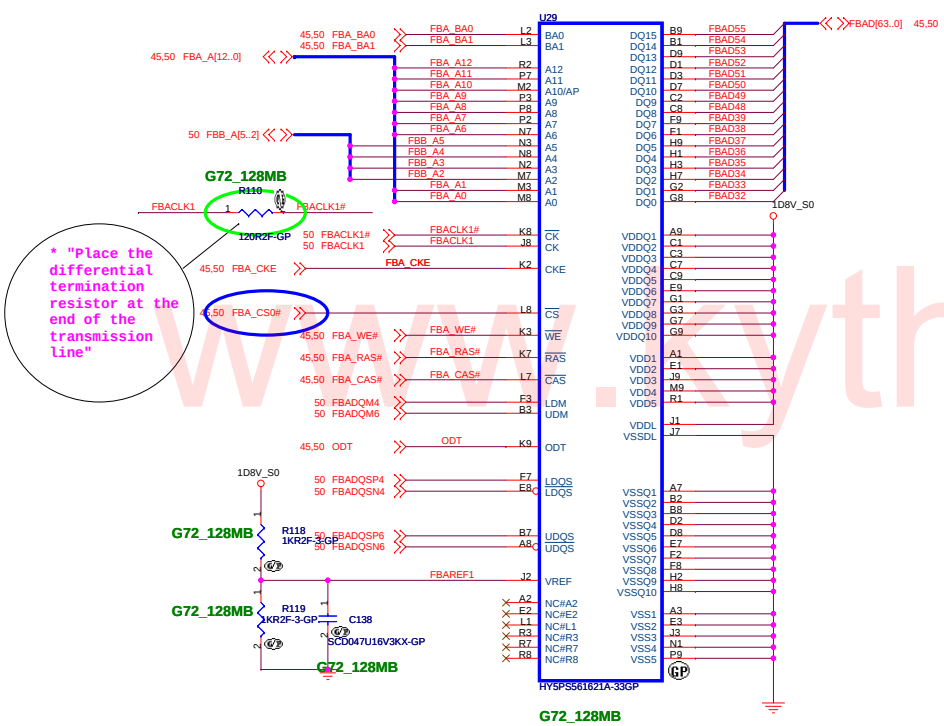
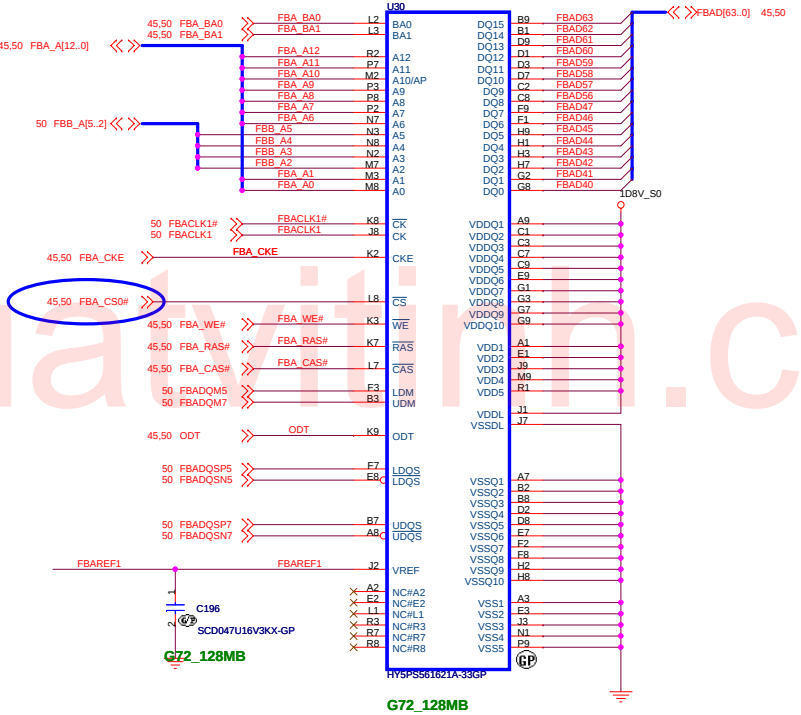
Taipei Hsien 221, Taiwan, R.O.C.

Title: VRAM (1ST 1/2)

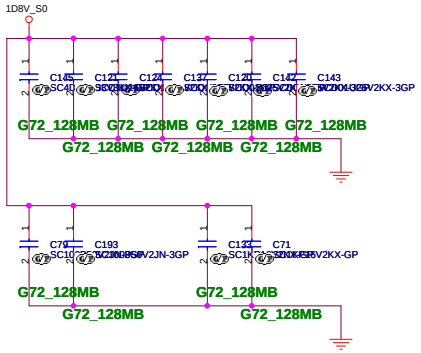
Size	Document Number	Rev
Custom	MYALL	SA

Date: Friday, February 10, 2006 Sheet 45 of 52

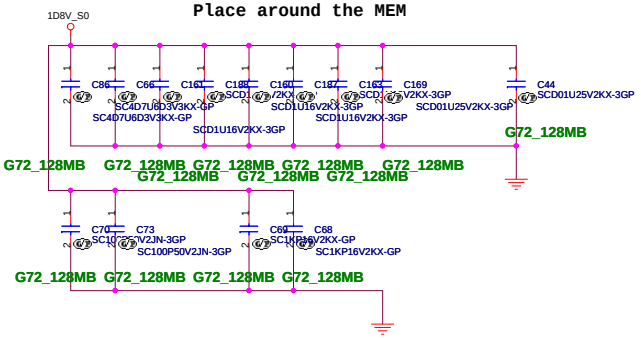




Decoupling for left MEMORY
Place around the MEM



Decoupling for right MEMORY
Place around the MEM



<Core Design>

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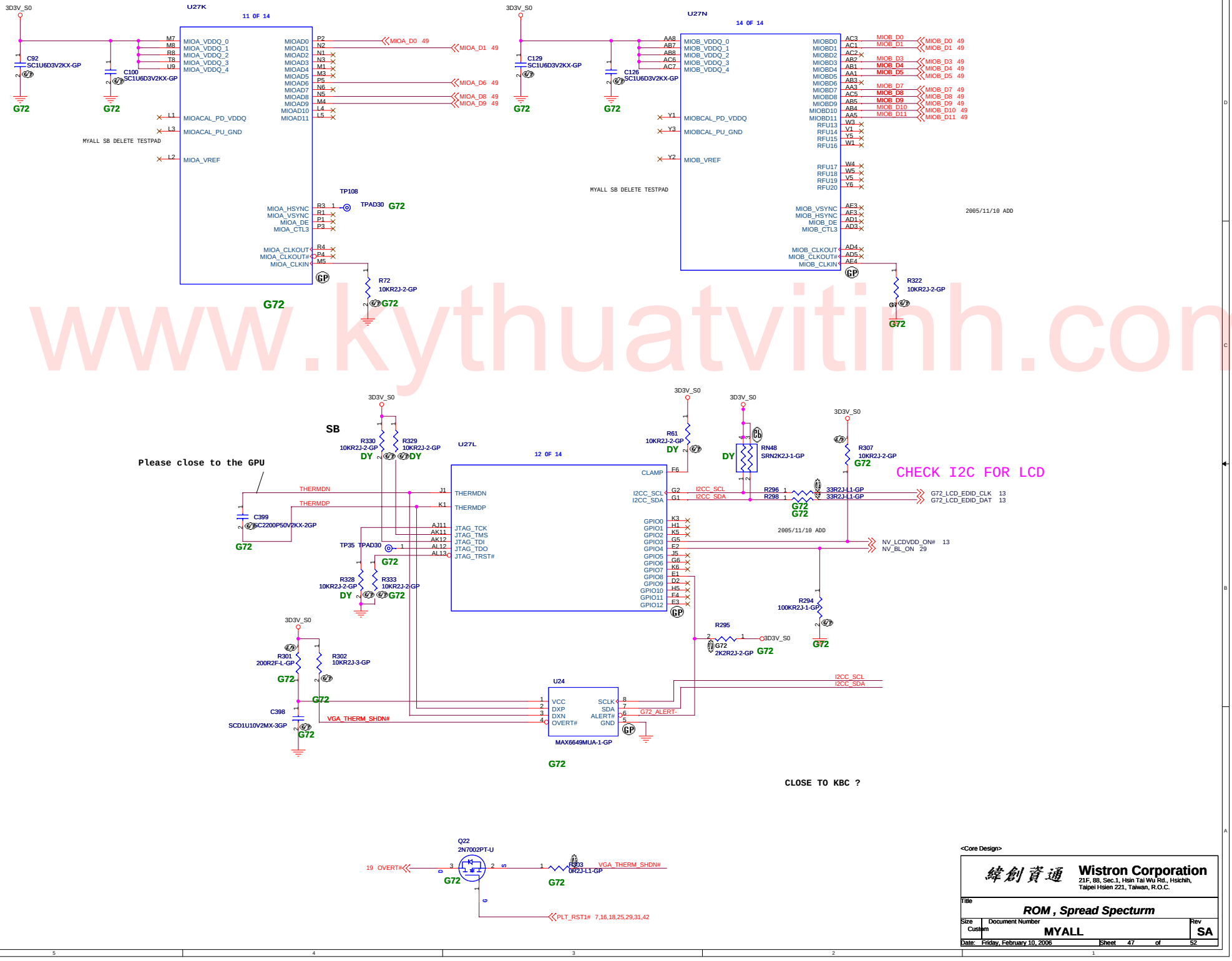
Title: VRAM (1ST 2/2)

Size	Document Number	Rev
Custom	MYALL	SA

Date: Friday, February 10, 2006 Sheet 46 of 52



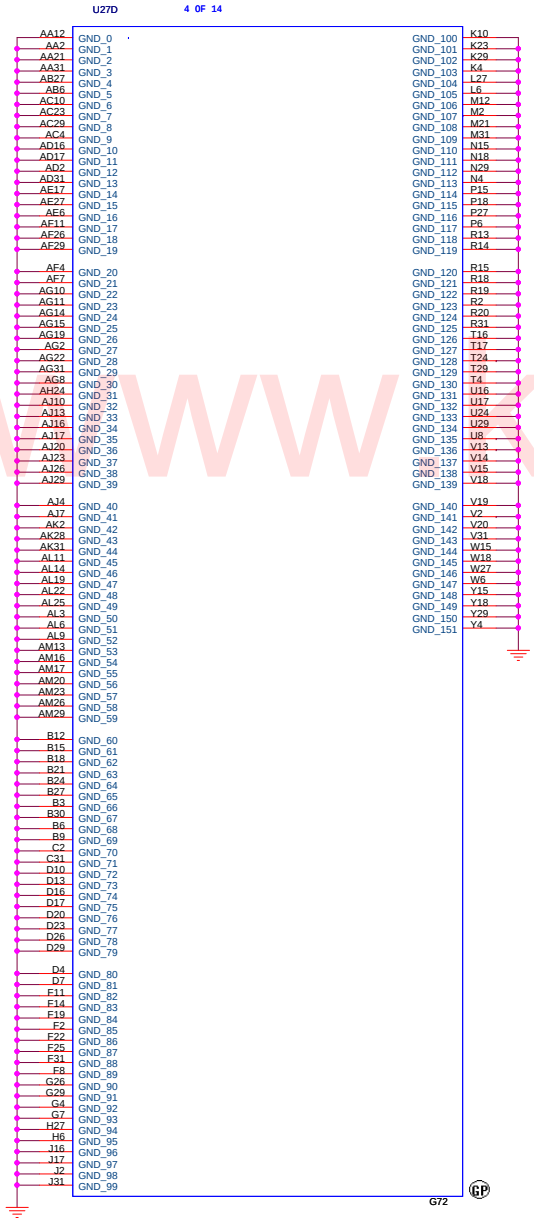
<Core Design>

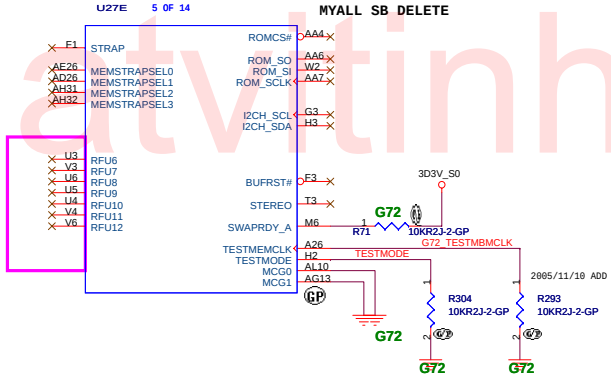
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

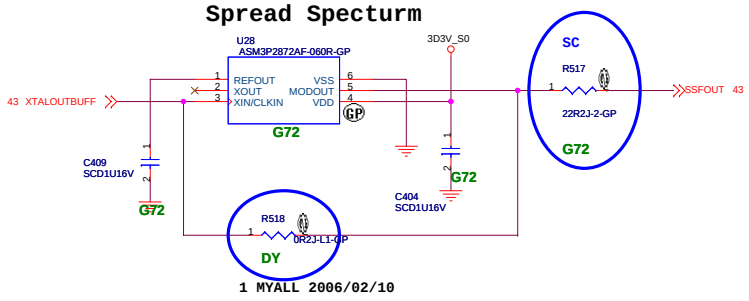
Title: ROM , Spread Specturm

Size	Document Number	Rev
Custom	MYALL	SA

Date: Friday, February 10, 2006 Sheet 47 of 52







<Core Design>

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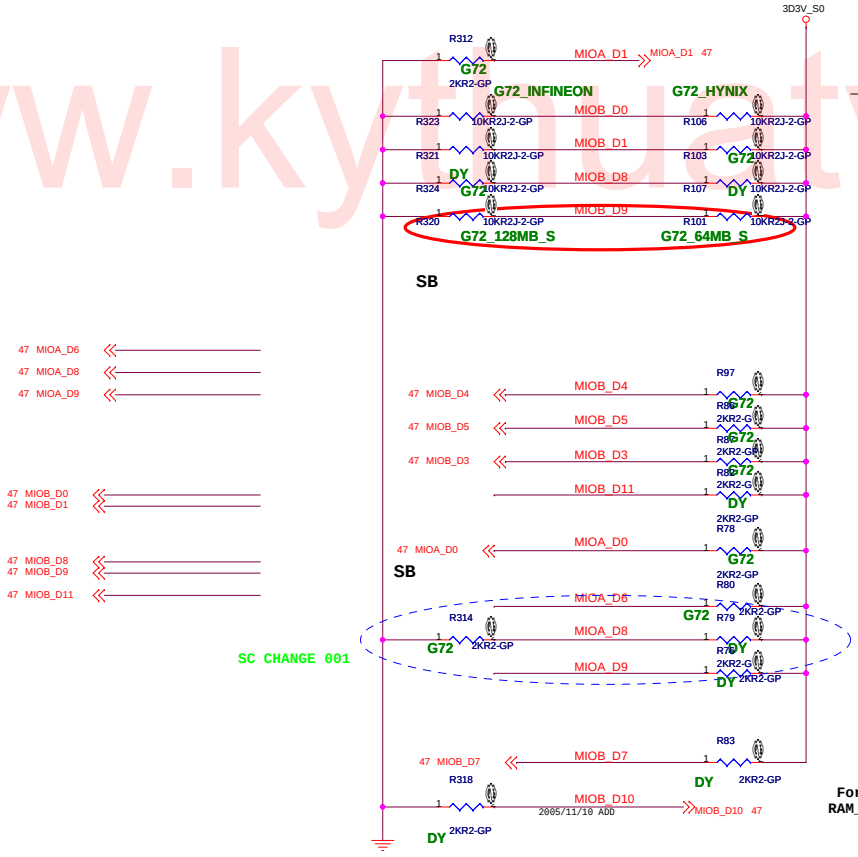
Title: ROM , Spread Specturm

Size	Document Number	Rev
Custom	MYALL	SA

Date: Friday, February 10, 2006 Sheet 48 of 52

STRAPS, Mechanical Parts



	Bit Signal	Values
MIOA_D1:	SUB_VENDOR	0 NO_BIOS 1 READ FROM BIOS
MIOB_D0: MIOB_D1: MIOB_D8: MIOB_D9:	RAM_CFG_0 RAM_CFG_1 RAM_CFG_2 RAM_CFG_3	0000 RFU 1000 RFU 0001 8Mx32 BGA 1.8V 1001 RFU 0010 RFU 1010 RFU 0011 RFU 1011 RFU 0100 4Mx32 BGA 1.8V 1100 RFU 0101 RFU 1101 RFU 0110 RFU 1110 RFU 0111 RFU 1111 RFU 0011 16MX16
MIOB_D2: MIOB_D6:	CRYSTAL_0 CRYSTAL_1	00 13.500 MHz 01 14.31818 MHz 10 27.000 MHz 11 UNKNOWN
MIOA_D7: MIOA_D10:	TV_MODE_0 TV_MODE_1	00 SECAM 01 NTSC 10 PAL 11 CRT
MIOB_D4: MIOB_D5: MIOB_D3: MIOB_D11:	PCI_DEVID_0 PCI_DEVID_1 PCI_DEVID_2 PCI_DEVID_3	1000 (default 0x00FC) 0111 G72MV
MIOA_D0:	PEX_PLL_EN_TERM100	0 ENABLED 1 DISABLED
MIOA_D6: MIOA_D8: MIOA_D9:	3GIO_PADCFG_LUT_ADDR[0] 3GIO_PADCFG_LUT_ADDR[1] 3GIO_PADCFG_LUT_ADDR[2]	0 DESKTOP 1 MOBILE 010 DEFAULT
MIOB_D7:	MOBILE_GPIO	0 GPIO_PULLDN 1 GPIO_FLOAT

SC CHANGE 001

For MEM strapping, Please use below table,

RAM_CFG[3:0]	Config	FB Bus Width	Definitions
0000	16Mx16 DDR2	64-bit	Elpida
0001	16Mx16 DDR2	64-bit	Samsung
0010	16Mx16 DDR2	64-bit	Infineon
0011	16Mx16 DDR2	64-bit	Hynix

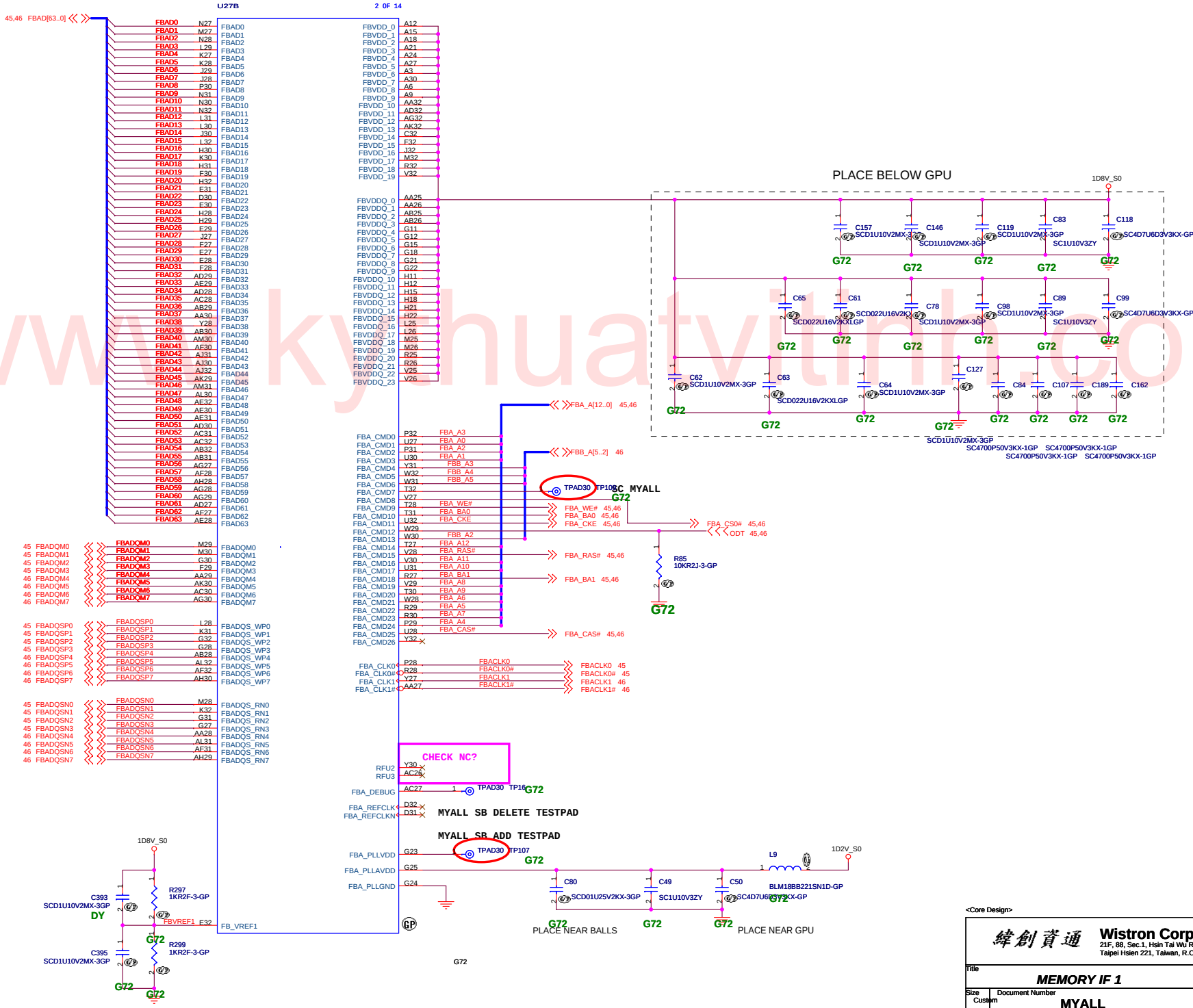
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ROM,Spread Specturn

Size: Custom | Document Number: MYALL | Rev: SA

Date: Friday, February 10, 2006 | Sheet 49 of 52



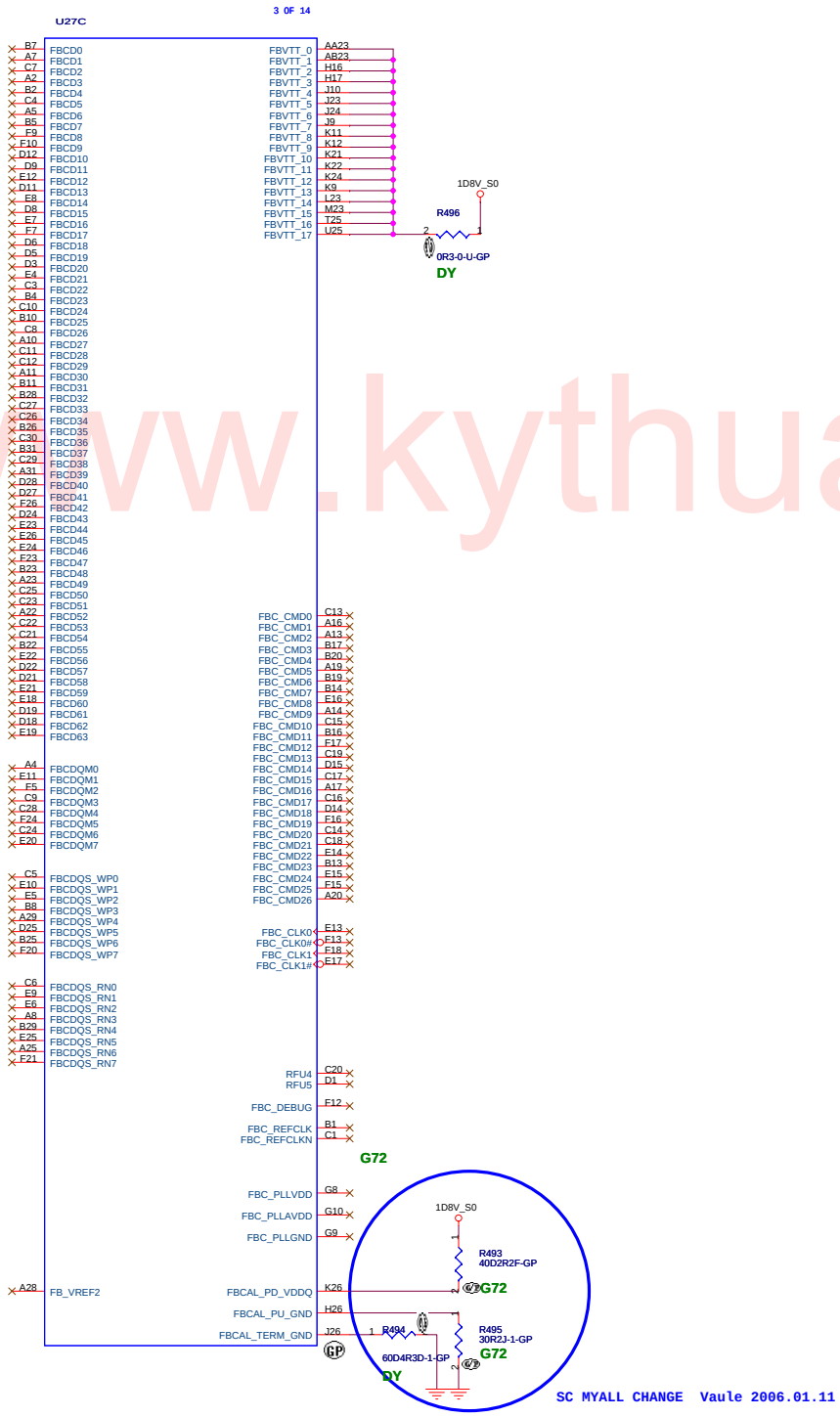
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MEMORY IF 1

Size	Document Number	Rev
Custom	MYALL	SA

Date: Friday, February 10, 2006 Sheet 50 of 52



SC MYALL CHANGE Vaule 2006.01.11

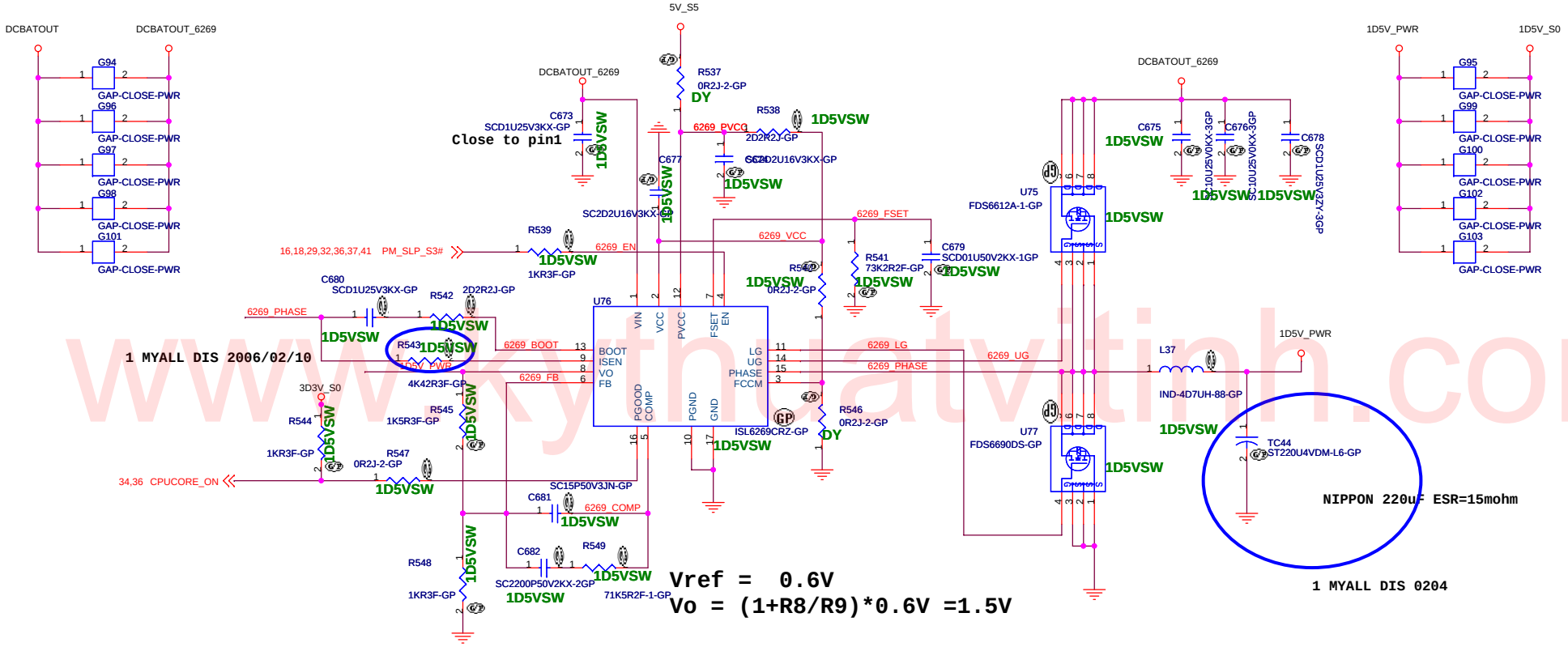
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MEMORY IF 2

Size: Custom | Document Number: MYALL | Rev: SA

Date: Friday, February 10, 2006 | Sheet 51 of 52



緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	ISL6269/1D5V
Size: A3	Document Number: MYALL
Rev	SC
Date: Friday, February 10, 2006	Sheet 52 of 52