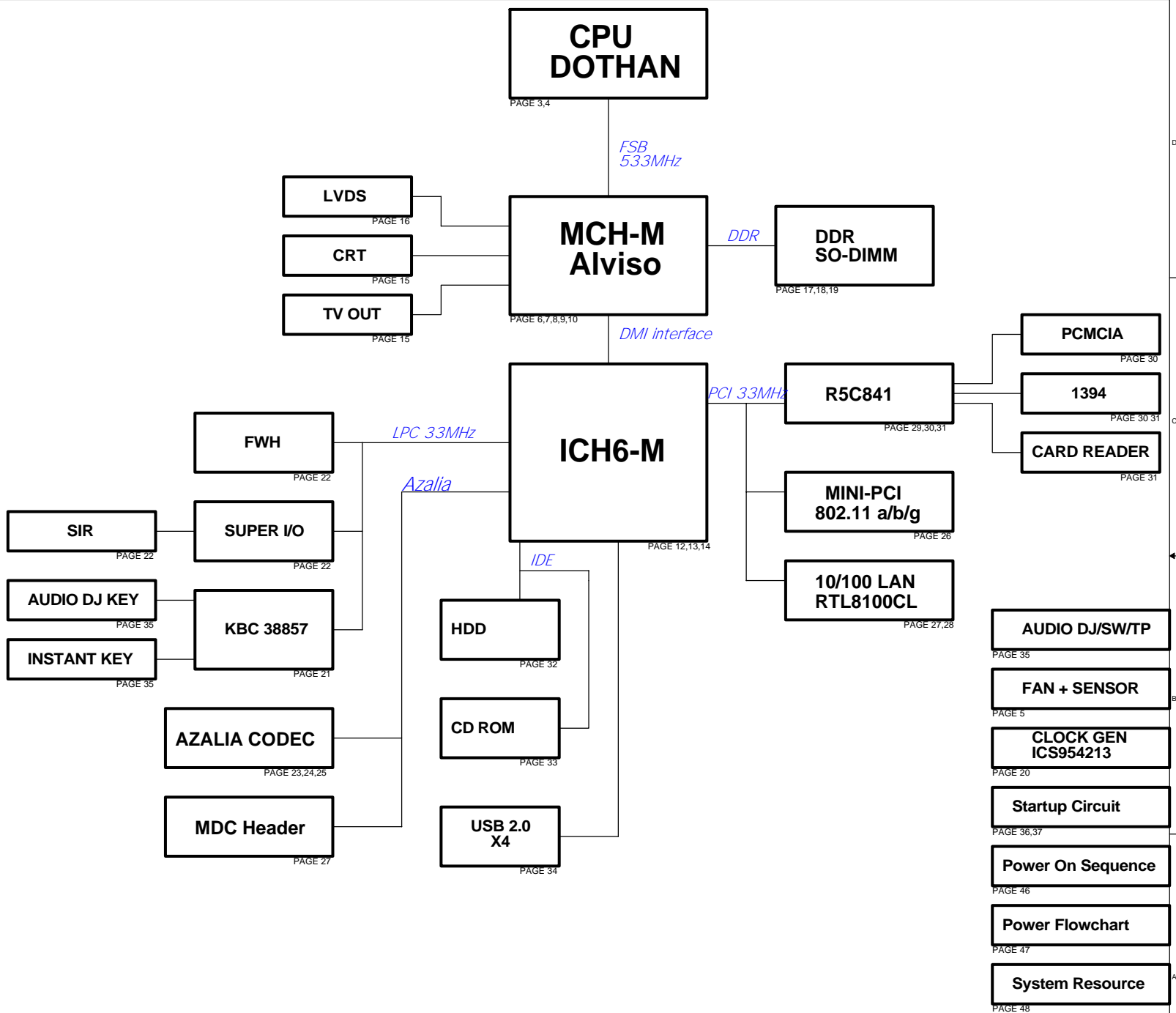


A3E CONTEXT

- 01_BLOCK DIAGRAM
- 02_REVISION LIST
- 03_DOYHAN CPU(1)
- 04_DOTHAN CPU(2)
- 05_THERMAL SENSOR,FAN
- 06_ALVISO GMCH(1)
- 07_ALVISO PCIE(2)
- 08_ALVISO DDR SLOT(3)
- 09_ALVISO POWER(4)
- 10_ALVISO GND(5)
- 11_GMCH STRAPPING/LVDS TRANS
- 12_ICH6M SATA,LPC,IDE(1)
- 13_ICH6M USB,PCI/E,PMIO(2)
- 14_ICH6M PWR,GND(3)
- 15_CRT&TV OUT CONN
- 16_LVDS&INVERTER(CAMERA,WLAN)
- 17_DDR SODIMM
- 18_DDR DATA TERMINATION
- 19_DDR ADDRESS TERMINATION
- 20_CLOCK GEN ICS954213
- 21_KBC M38857
- 22_FWH,SIO,SIR
- 23_AZALIA ALC880
- 24_AMPLIFIER 2 CHANNEL
- 25_MIC,LINE-IN JACK
- 26_MINI-PCI
- 27_LAN RTL8100CL
- 28_RJ11/45,MDC,PRN
- 29_PCI CARDBUS R5C841
- 30_PCI PCMCIA SOCKET A
- 31_PCI IEEE1394A,3IN1 CON
- 32_HDD CONNECTOR
- 33_Q/SW,CD-ROM CONNECTOR
- 34_USB CONNECTOR
- 35_DJ BOARD/SW/TP
- 36_STARTUP CIRCUIT(1)
- 37_STARTUP CIRCUIT(2)
- 38_VCORE
- 39_SYSTEM(3V,5V)
- 40_2.5V,1.5V,1.8V,1.05V
- 41_VCCA,DDR(1.25VS)
- 42_PIC/BAT CONN/PWOK/THERM PT
- 43_CHARGE
- 44_BATLOW/SD#
- 45_LOAD SWITCH
- 46_POWER ON SEQUENCE
- 47_SYSTEM RESOURCE
- 48_Power Flowchart
- 49_EE HISTORY
- 50_PWR HISTORY



		Title : BLOCK DIAGRAM	
ASUSTeK COMPUTER INC		Engineer: Quan-Tai Lin	
Size	Project Name	Rev	
Custom	A3E	2.2	
Date: Thursday, May 05, 2005		Sheet	1 of 51

REVISION LIST

R1.0 2005/01/10

POWER INTERFACE

SIGNALS TYPE POWER

PM_PSI#	O	+VCCP
VR_VID[5:0]	O	+VCCP
VRON	O	+3.3V
PM_DPRSLPVR	O	+3.3V
CPU_STP#	O	+3.3V
RST_BTN#	O	+3.3V
CLK_EN#	I	+3.3V
DELAY_VR_PWRGD	I	+3.3V
OTP_RESET#	I	+3.3V
SHUT_DOWN#	I	+3.3V
BAT_LEARN	I	+3.3V
BAT_LLOW#_OC	I	+3.3V
BAT_IN#_OC	I	+3.3V
CHG_EN#	I	+3.3V
CHG_FULL_OC	I	+3.3V
CHG_LED_UP	I	+3.3V
SMCLK_BAT1	IO	+3.3V
SMDATA_BAT1	IO	+3.3V
SUSB#	O	+3.3V
SUSC#	O	+3.3V
1.8V_PWRGD	I	+3.3V
1.5VS_PWRGD	I	+3.3V
VSUS_ON	O	+3.3V
ACIN_OC	I	+3.3V
ACIN#	I	AC_BAT_SYS
+3VA	PWR	+3.3V
+5VA	PWR	+5V
+5VLCM	PWR	+5VLCM
A/D_DOCK_IN	PWR	DC
AC_BAT_SYS	PWR	DC

POWER PLANE

POWER	VOLTAGE	CURRENT
+VCORE	0.7 - 1.77V	27A
+VCCP	1.05 - 1.2V	3.95A
+VCC_GMCH	1.05V	4.12A
+0.9VS	1.25V	0.85A
+1.5VS	1.5V	4.33A
+1.5V	1.5V	300 mA
+1.5VSUS	1.5V	270 mA
+2.5V	2.5V	6.68A
+2.5VS	2.5V	0.3 A
+3VS	3.3V	1.732A
+3V	3.3V	1.515A
+3VSUS	3.3V	540 mA
+5VS	5V	4.1A
+5V	5V	0.5A
+5VSUS	5V	0.5A
+12V	12V	0.25A
+12VS	12V	0.25A

IMPEDENCE

Single-Ended

27.4 OHM WIDTH
TOP/BOT 18 mils

37.5 OHM WIDTH
TOP/BOT 11 mils
IN1/IN2 9.5 mils

50 OHM WIDTH
TOP/BOT 6 mils
IN1/IN2 5 mils

55 OHM WIDTH
TOP/BOT 5.5 mils
IN1/IN2 4.5 mils

75 OHM WIDTH
TOP/BOT 4 mils
IN1/IN3 3.5 mils

Differential

85 OHM WIDTH/SPACE
TOP/BOT 5.5 mils/ 4 mils
IN1/IN2 4.5 mils/ 4 mils

90 OHM WIDTH/SPACE
TOP/BOT 5.5 mils/ 5 mils
IN1/IN2 4.5 mils/ 5 mils

100 OHM WIDTH/SPACE
TOP/BOT 6 mils/ 11 mils
IN1/IN2 5 mils/ 12 mils

110 OHM WIDTH/SPACE
TOP/BOT 5 mils/ 13 mils
IN1/IN2 4 mils/ 12 mils

PCI INTERFACE

PCI_REQ#

MINIPCI **PCI_REQ#3**
10/100 **PCI_REQ#2**
CB&1394 **PCI_REQ#1**

IDSEL

MINIPCI **PCI_AD19**
10/100 **PCI_AD16**
CB&1394 **PCI_AD17**

PCB STACK-UP

PCB THICKNESS: 1.6 mm

- L1 TOP
- L2 GND
- L3 IN1
- L4 IN2
- L5 GND
- L6 BOT

PAGE 38

SIGNAL IN: VR_VID[0..5]
PM_DPRSLPVR
STP_CPU#
PM_PSI#
CPU_VRON
MCH_OK

OUT: DELAY_VR_PWRGD
CLK_PWR_GD#

POWER IN: AC_BAT_SYS
+5VO
~~+3VO~~

OUT: +VCORE

PAGE 39

SIGNAL IN: ~~SUSC#_PWR~~
VSUS_ON

POWER IN: AC_BAT_SYS

OUT: +12VO
+3VO
+5VO

PAGE 40

SIGNAL IN: SUSB#_PWR
SUSC#_PWR
CPU_VRON

POWER IN: AC_BAT_SYS
+5VO

OUT: +1.8V
+1.5VS
+2.5VS
+VCC_GMCH_CORE
+5VALWAYS
+3VALWAYS
+VCCP

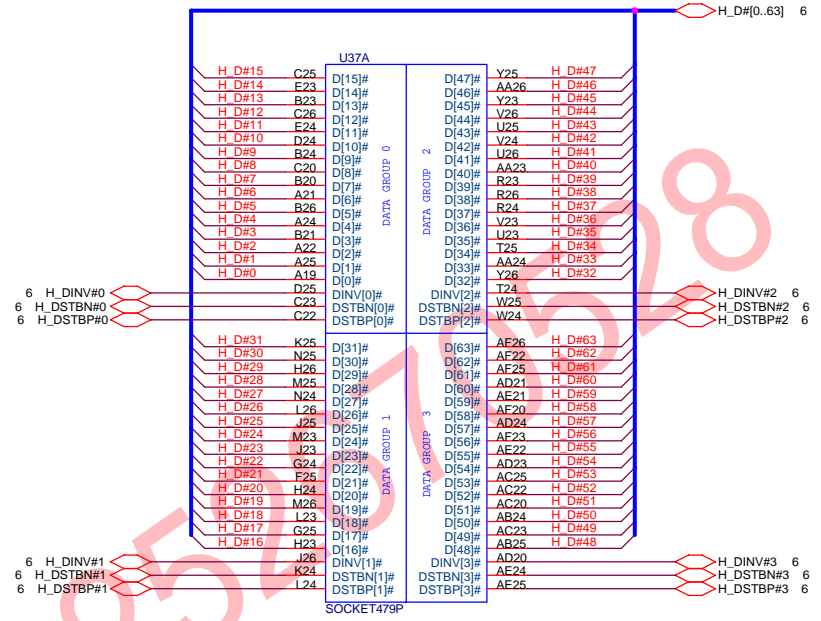
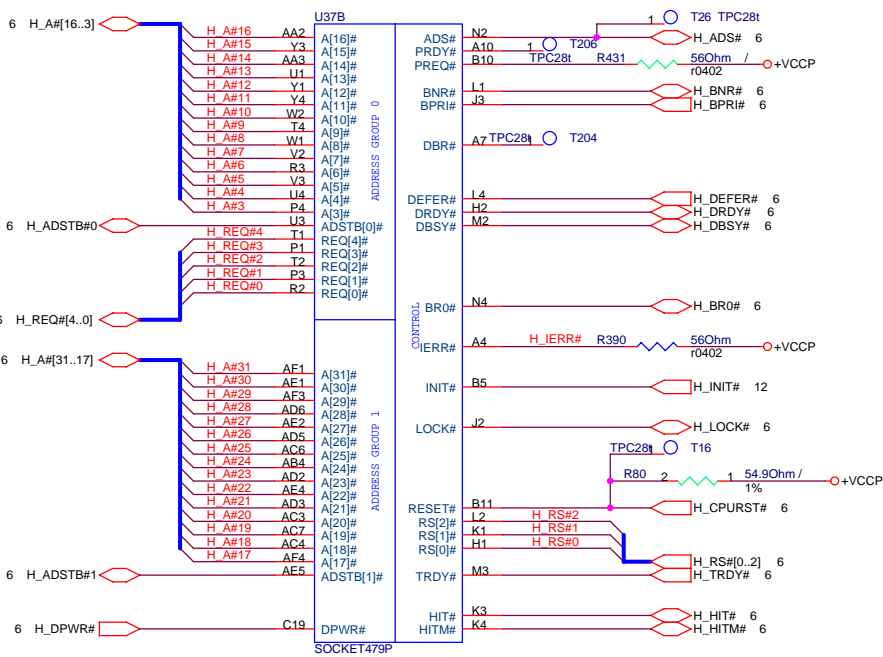
PAGE 41

SIGNAL IN: SUSB#_PWR

POWER IN: +3V
+1.8V

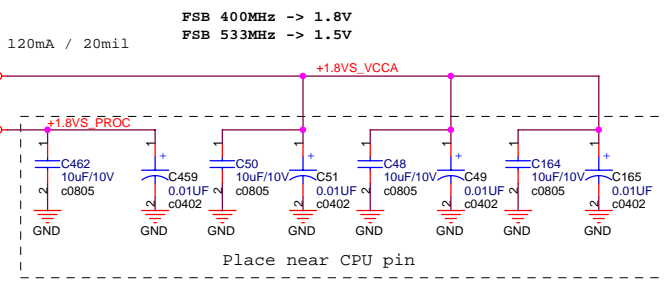
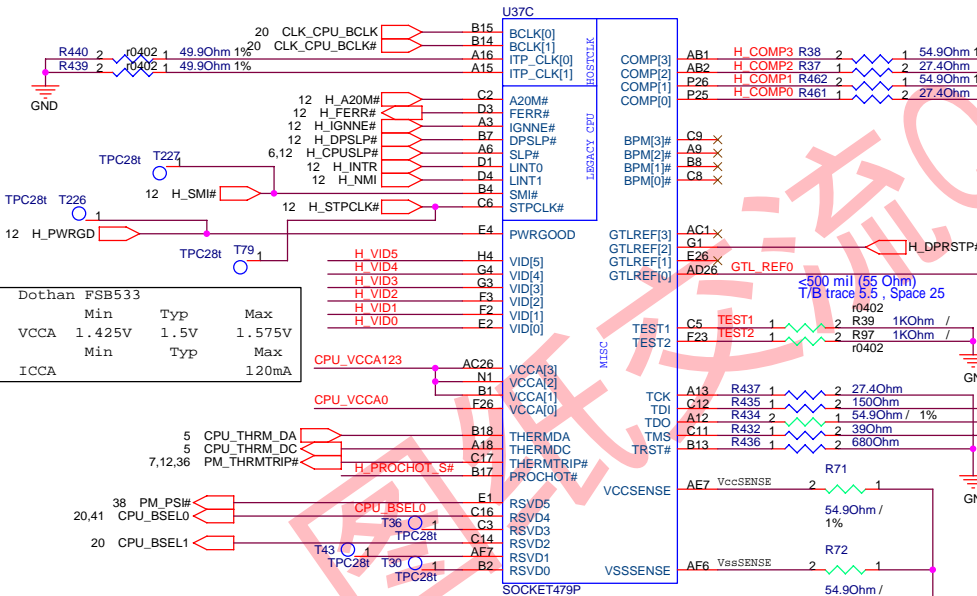
OUT: +0.9VS

		Title : REVISION LIST	
ASUSTeK COMPUTER INC		Engineer: Quan-Tai Lin	
Size	Project Name	Date	Rev
Custom	A3E	Thursday, May 05, 2005	2.2
Date: Thursday, May 05, 2005		Sheet	2 of 51



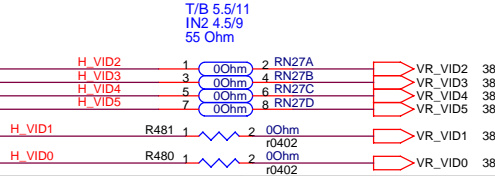
Layout note:
 COMP0 and COMP2 need to be Zo=27.4ohm traces.
 Best estimate is 18mil wide trace for outer layers and 14mil if on internal layer. See RDDP of Banias.
 Traces should be shorter than 0.5". Refer to latest CS layout

COMP1, COMP3 should be routed as Zo=55ohm traces shorter than 0.5"



Dothan FSB533			
Min	Typ	Max	
VCCA	1.425V	1.5V	1.575V
ICCA			
Min	Typ	Max	
			120mA

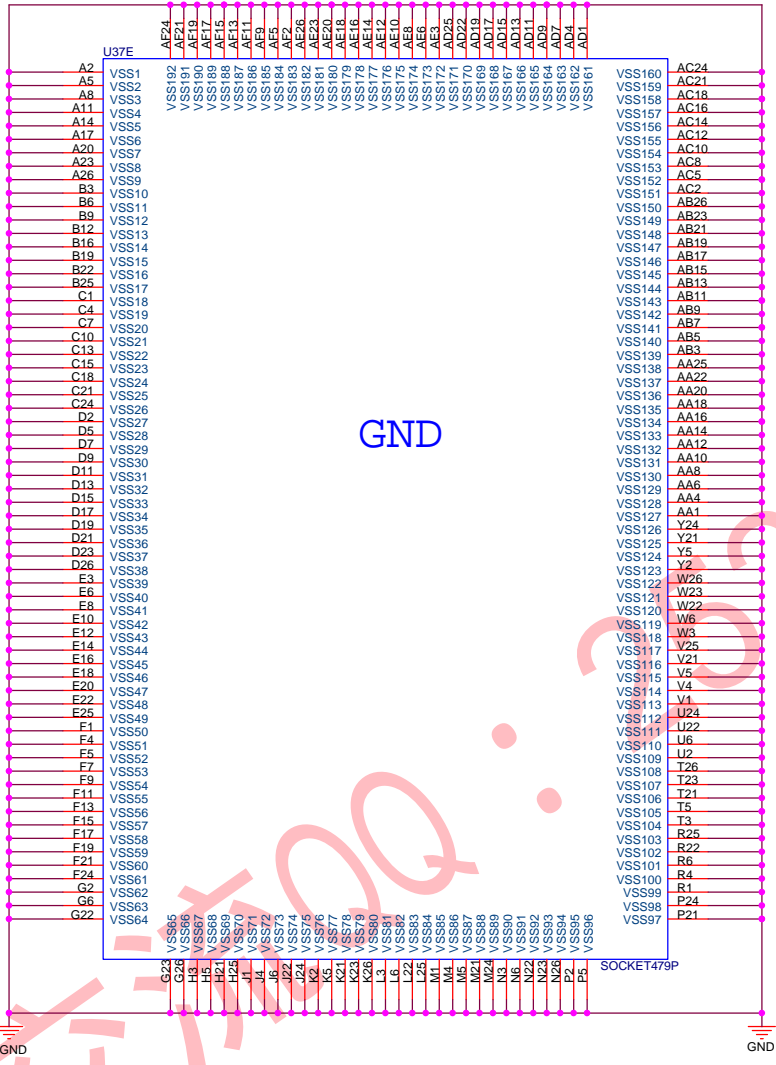
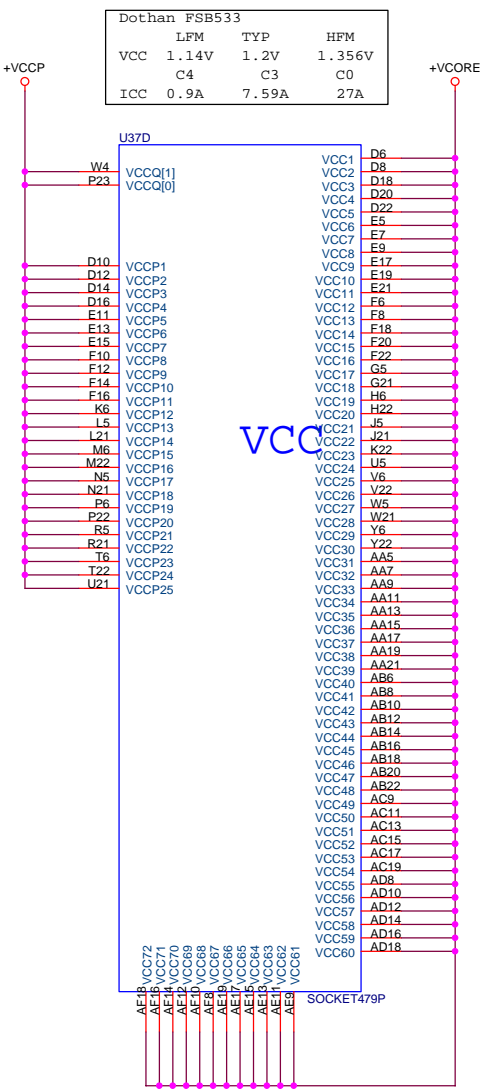
B-STEP			
Bclk	FSB	BSEL1	BSEL0
100	400	0	1
133	533	0	0



ASUS Title : **DOTHAN CPU (1)**
 ASUSTek COMPUTER INC Engineer: **Quan-Tai Lin**

Size	Project Name	Rev
Custom	A3E	2.2

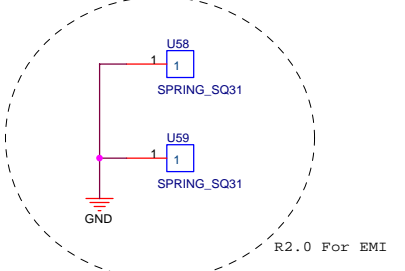
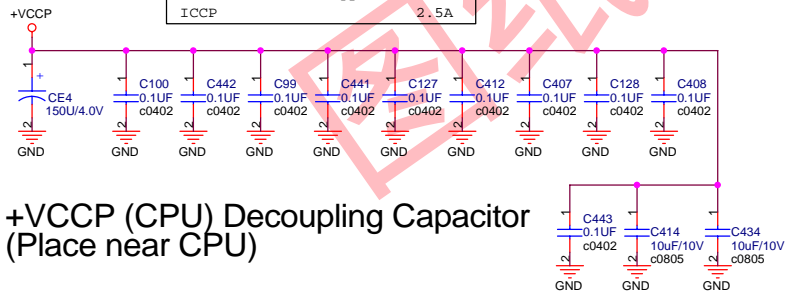
Date: Thursday, May 05, 2005 Sheet 3 of 51



MOBILE DOTHAN VID TABLE

VID[5..0]	Voltage	VID[5..0]	Voltage
000000	1.708V	100000	1.196V
000001	1.692V	100001	1.180V
000010	1.676V	100010	1.164V
000011	1.660V	100011	1.148V
000100	1.644V	100100	1.132V
000101	1.628V	100101	1.116V
000110	1.612V	100110	1.100V
000111	1.596V	100111	1.084V
001000	1.580V	101000	1.068V
001001	1.564V	101001	1.052V
001010	1.548V	101010	1.036V
001011	1.532V	101011	1.020V
001100	1.516V	101100	1.004V
001101	1.500V	101101	0.988V
001110	1.484V	101110	0.972V
001111	1.468V	101111	0.956V
010000	1.452V	110000	0.940V
010001	1.436V	110001	0.924V
010010	1.420V	110010	0.908V
010011	1.404V	110011	0.892V
010100	1.388V	110100	0.876V
010101	1.372V	110101	0.860V
010110	1.356V	110110	0.844V
010111	1.340V	110111	0.828V
011000	1.324V	111000	0.812V
011001	1.308V	111001	0.796V
011010	1.292V	111010	0.780V
011011	1.276V	111011	0.764V
011100	1.260V	111100	0.748V
011101	1.244V	111101	0.732V
011110	1.228V	111110	0.716V
011111	1.212V	111111	0.700V

Dothan FSB533			
Min	Typ	Max	
VCCP 0.997V	1.05V	1.102V	
ICC		2.5A	



Fan Speed Control

When fan speed is very slow, after RC integrator the level of FANSP1 will be very low that may make south bridge do the wrong detection.

CPU FAN

KBC will issue a analog (a voltage level) signal.

SW: FAN_DA1 must be low during S3

Using a OP AMP and fine-tuning the level, we can improve the fan speed accuracy.

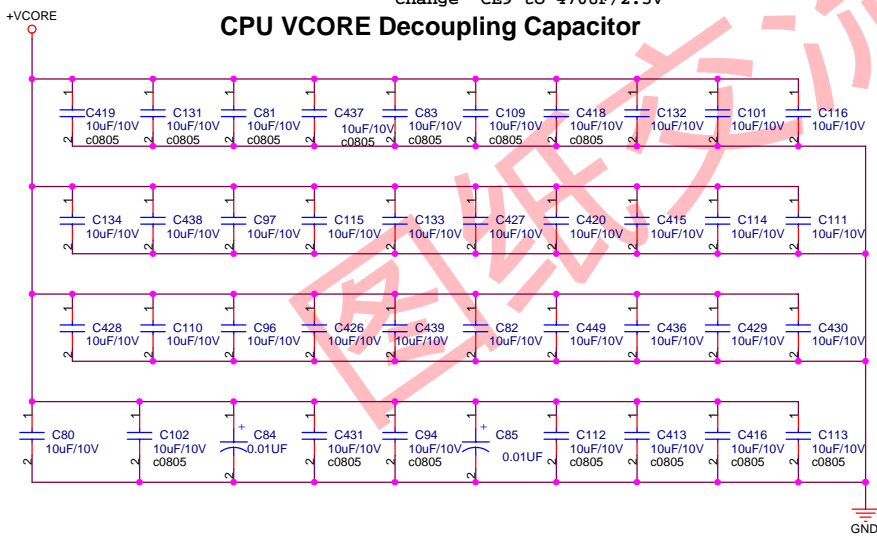
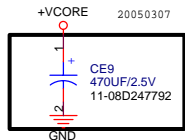
P/N change to 06-010112010 for cost down

U6 output maximum will be 10.5V (VCC-1.5V) which will damage south bridge. Add a MOS to transfer it to +3V level.

- CPU FAN will be forced on:
- 1) Thermal Sensor Over-temperature
 - 2) PROCHOT asserted(CPU)
 - 3) WATCHDOG asserted(KBC)

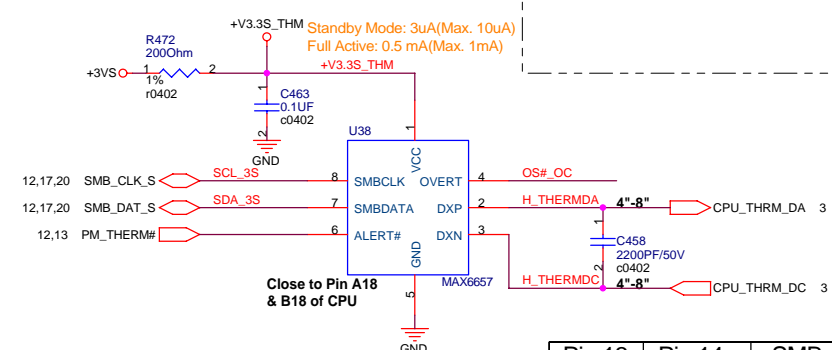
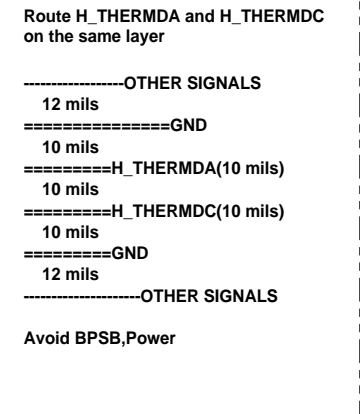
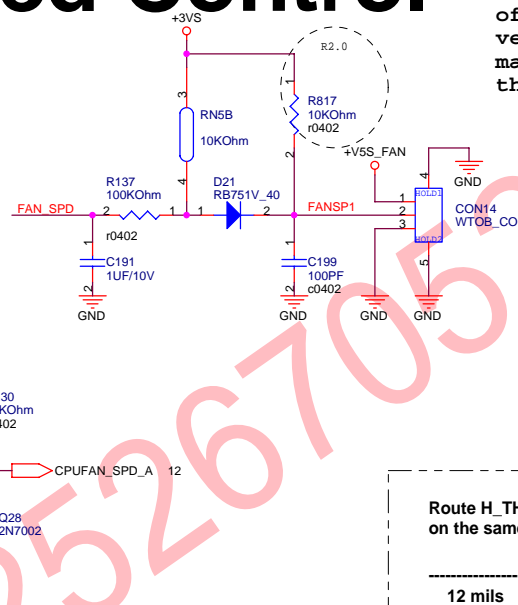
CPU VCORE Decoupling Capacitor

Change CE10 to power and change CE9 to 470UF/2.5V

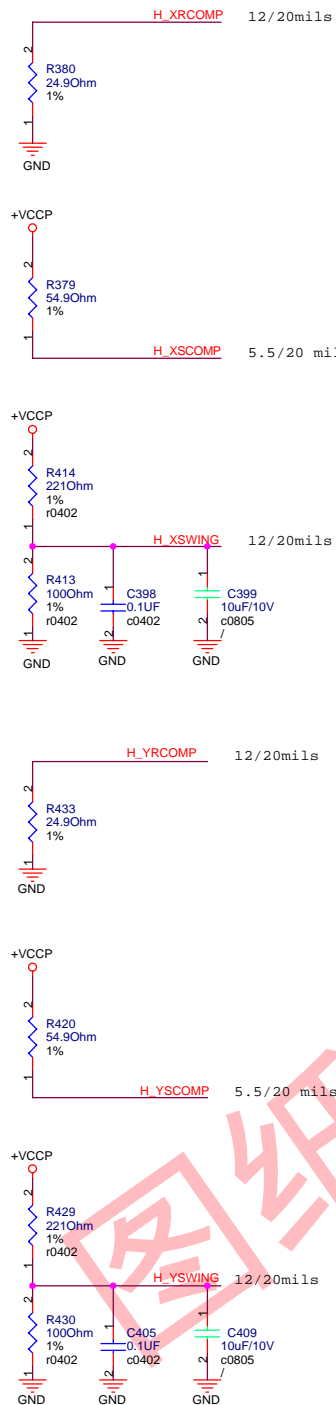


- Mid Frequency Decoupling (Place around Processor)
- High Frequency Decoupling (Place underneath Processor) using 10uF/6.3V X5R
- +VCORE Bulk Decoupling

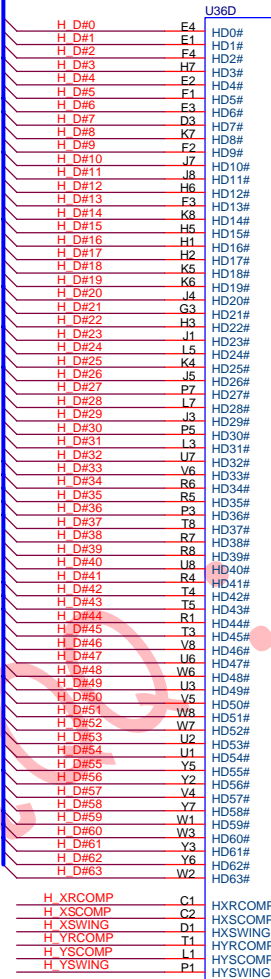
Four 200 uF are located in IMVP4



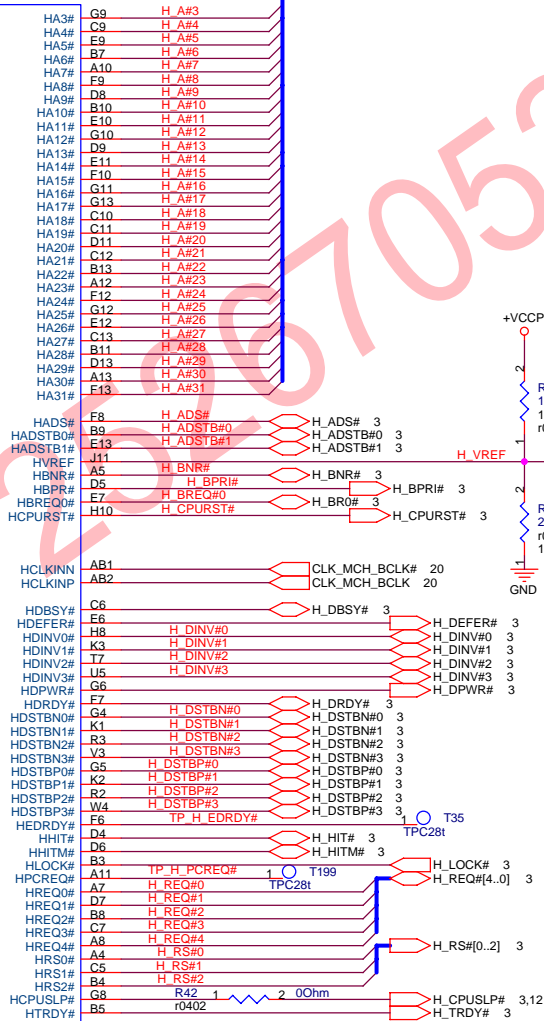
Pin 13	Pin 14	SMB Addr
1	X	5C **
0	1	5A
0	0	58



3 H_D#[0..63]



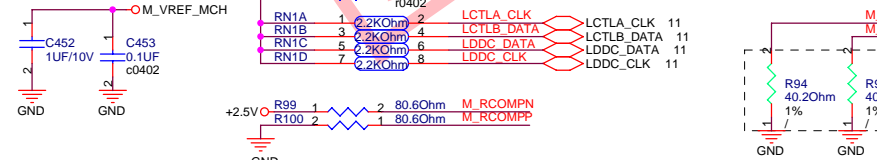
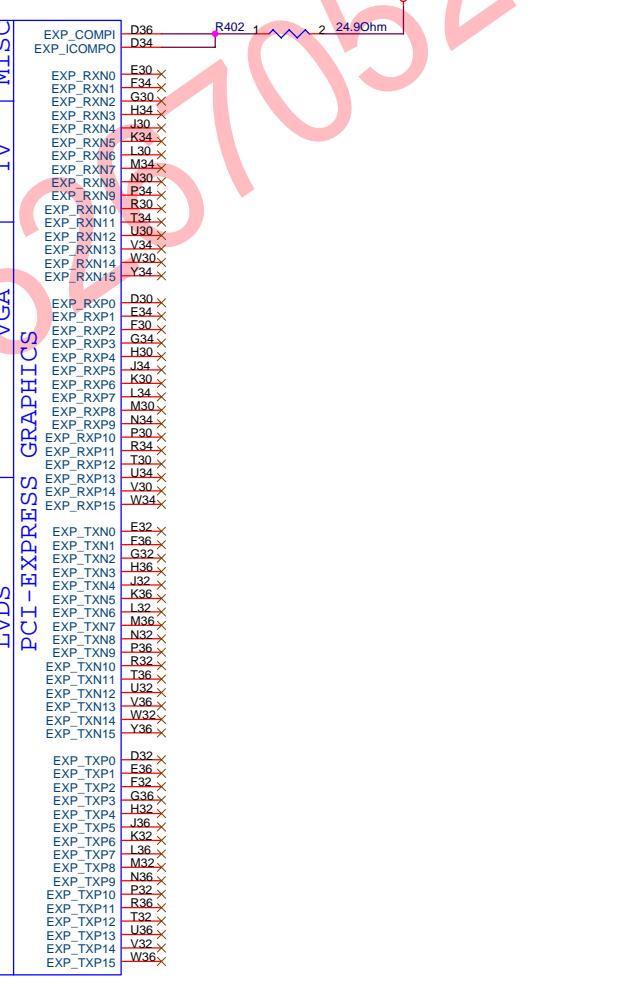
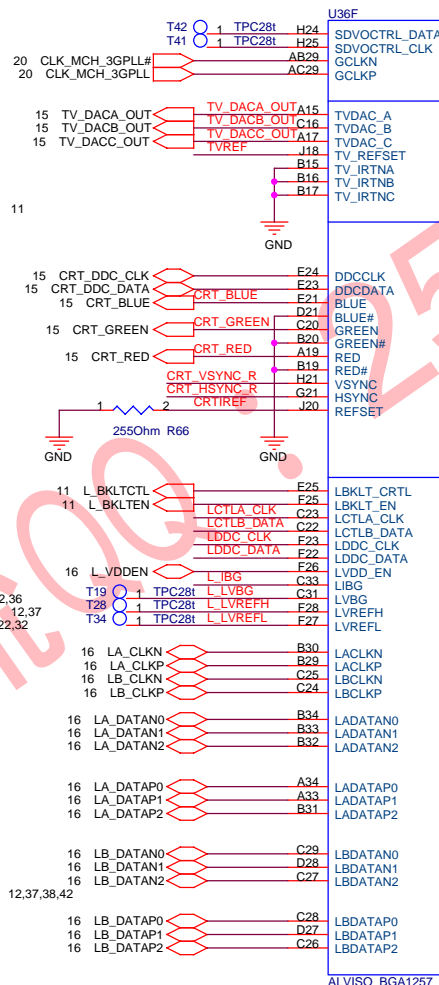
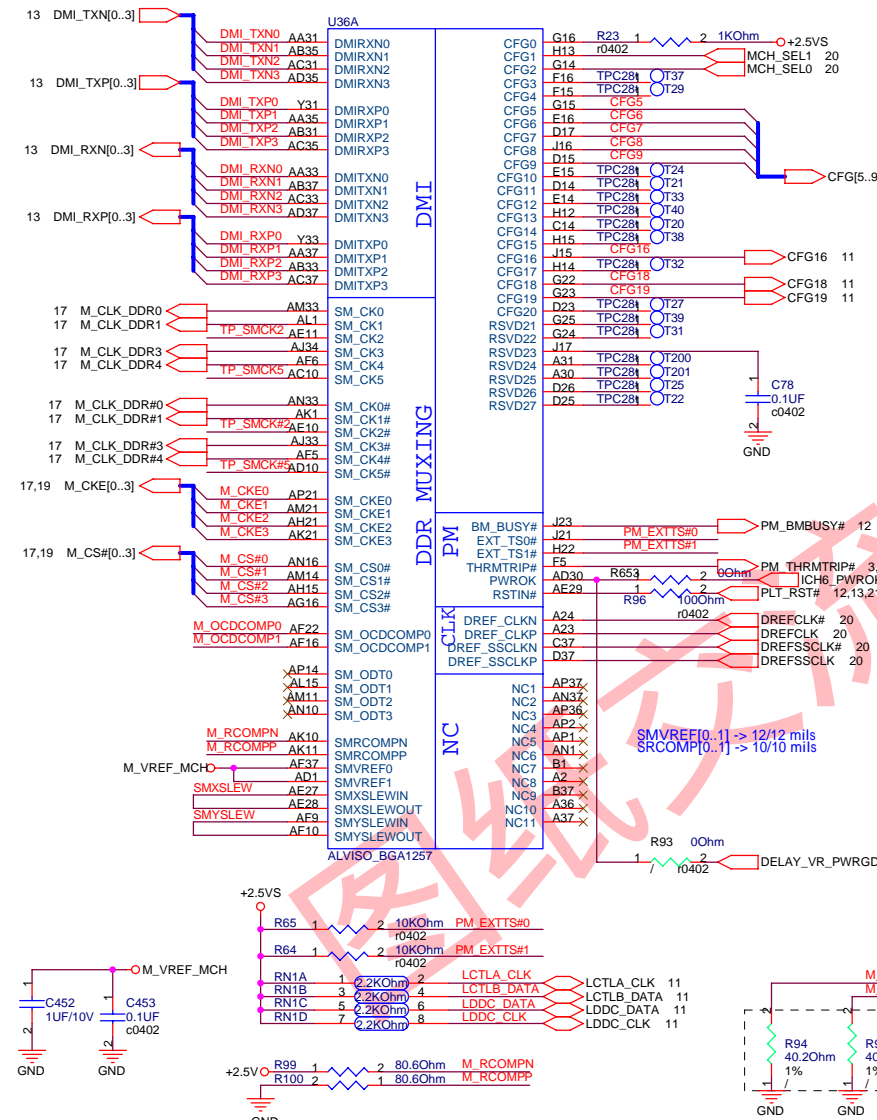
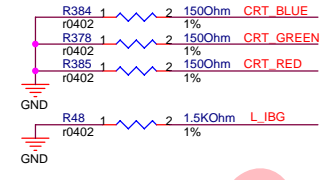
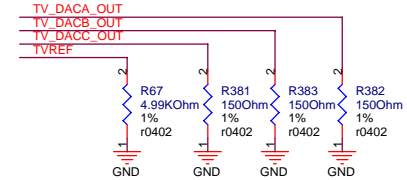
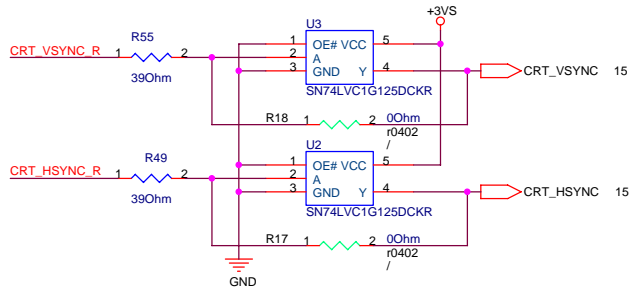
HOST



Dothan A : R282
NO STUFF

In OrCAD circuit,ALVISO PM P/N :02-010002600
But we have to use ALVISO GM P/N : 02-010002610 in BOM list

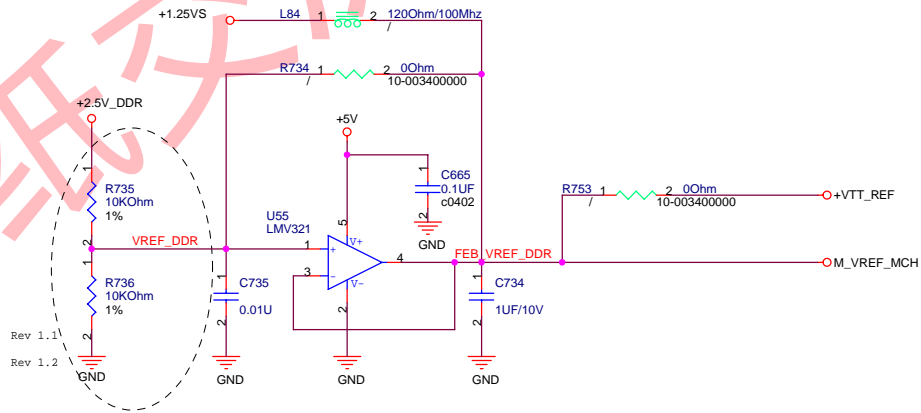
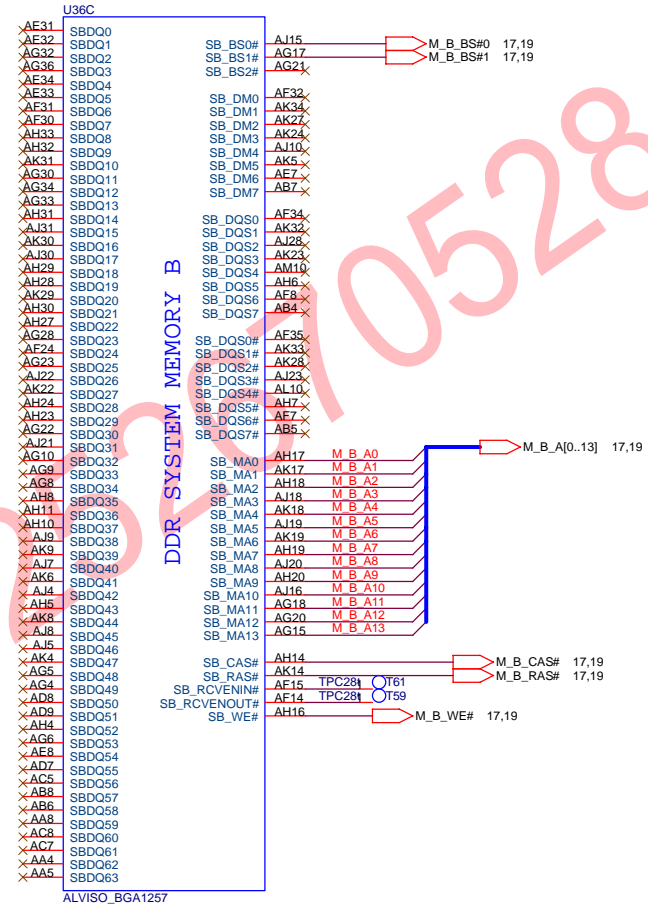
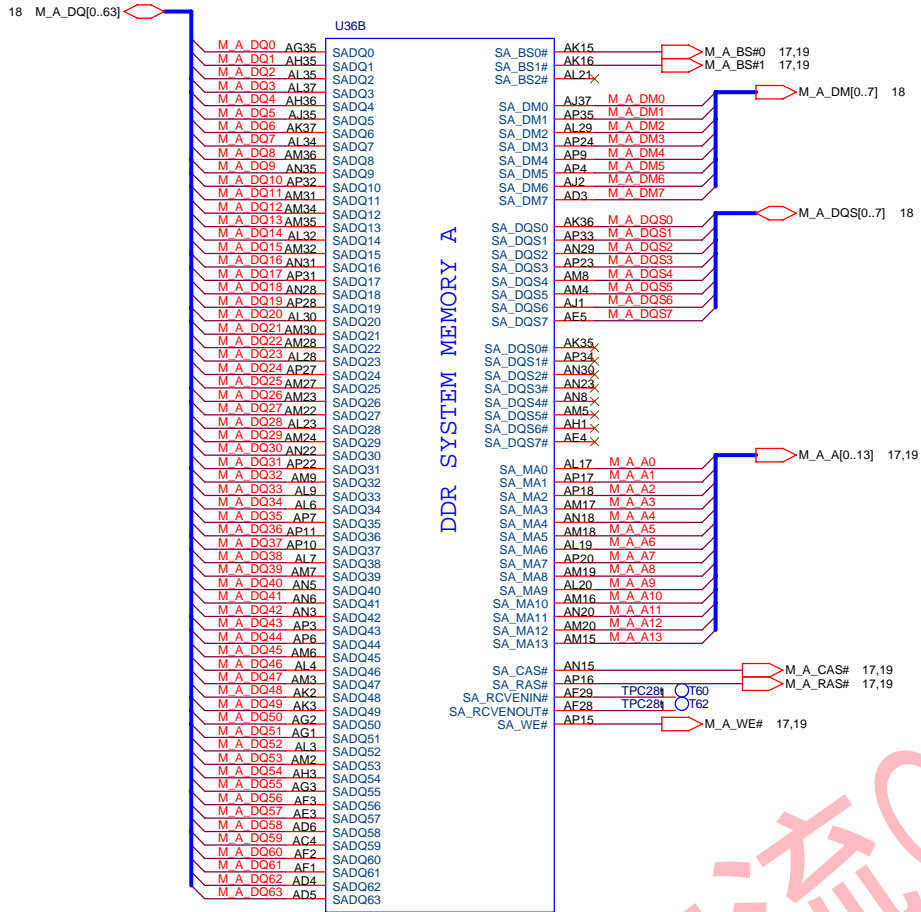
Near Alviso 0.5" ← → Near CRT Bead 0.5"



Layout Note:
Route as short as possible.

ASUS Title : Alviso GMCH (2)
 ASUSTek COMPUTER INC Engineer: Quan-Tai Lin
 Size Project Name
 Custom A3E
 Date: Thursday, May 05, 2005 Sheet 7 of 51

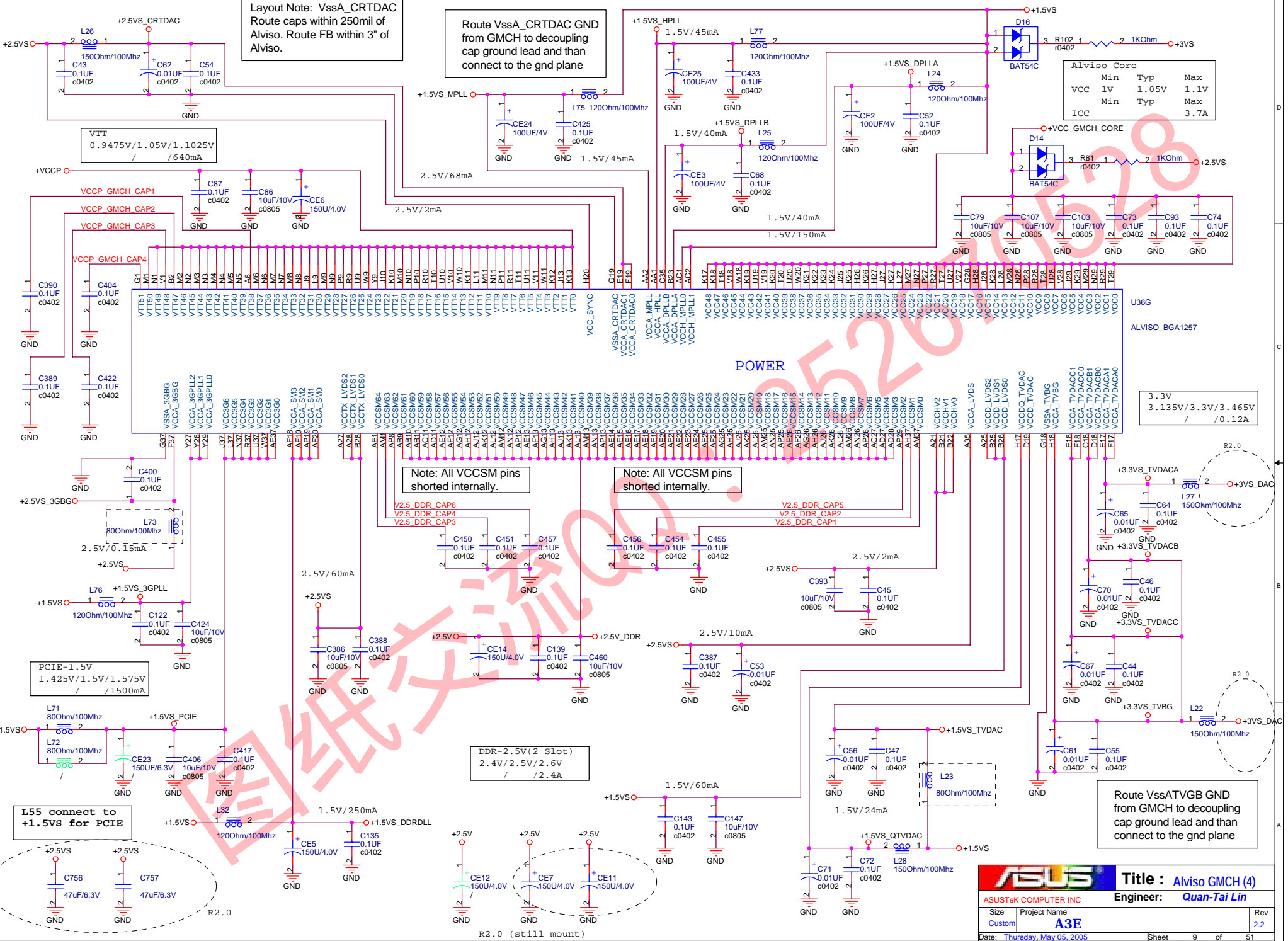
- T63 0 1 TPC281 TP_SMCK2
- T57 0 1 TPC281 TP_SMCK5
- T58 0 1 TPC281 TP_SMCK#2
- T54 0 1 TPC281 TP_SMCK#5



Layout Note: VssA_CRTDAC
Route caps within 250mil of Alviso. Route FB within 3" of Alviso.

Route VssA_CRTDAC GND from GMCH to decoupling cap ground lead and then connect to the gnd plane

Alviso Core			
	Min	Typ	Max
VCC	1V	1.05V	1.1V
ICC			3.7A



Note: All VCCSM pins shorted internally.

Note: All VCCSM pins shorted internally.

DDR-2.5V (2 Slot)
2.4V / 2.5V / 2.6V
/ / 2.4A

Route VssATVGB GND from GMCH to decoupling cap ground lead and then connect to the gnd plane

ASUS		Title : Alviso GMCH (4)	
ASUSTek COMPUTER INC		Engineer: Quan-Tai Lin	
Size Custom	Project Name A3E	Rev 2.2	
Date: Thursday, May 05, 2005		Sheet 9 of 51	



VSSA

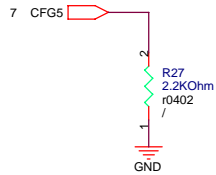
NCTF

		Title : Alviso GMCH (5)	
ASUSTek COMPUTER INC		Engineer: Quan-Tai Lin	
Size Custom	Project Name A3E		Rev 2.2
Date: Thursday, May 05, 2005		Sheet 10 of 51	

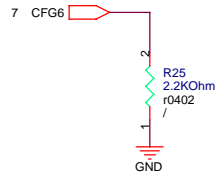
CFG[2:0] are HVMOS (+2.5VS)
 CFG[17..3] have internal pullup resistors. /AGTL+(VCCP)/
 CFG[19..18] have internal pulldown resistors. /HVMOS(+2.5VS)/
 SDVOCRTL_DATA has internal pulldown resistors.

SDVOCRTL_DATA :
 LOW = No SDVO device present (Default)

CFG5 : LOW = DMI X 2
 HIGH = DMI X 4 (Default)

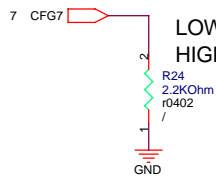


CFG6 : LOW = DDR2 SDRAM
 HIGH = DDR SDRAM (Default)



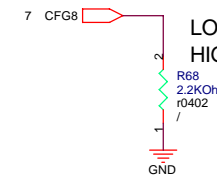
CFG7 : CPU STRAP

LOW = Mobile Prescott
 HIGH = Dothan CPU (Default)



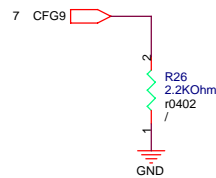
CFG8 : PCI-X POWER Saving

LOW = PCI-X POWER Saving
 HIGH (Default)



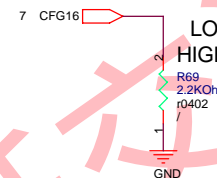
CFG9 : PCIE GRAPHIC LANE

LOW = REVERSE LANE
 HIGH = NORMAL OPERATION (Default)



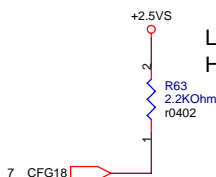
CFG16 : FSB DYNAMIC ODT

LOW = Dynamic ODT Disabled
 HIGH = Dynamic ODT Enabled (Default)



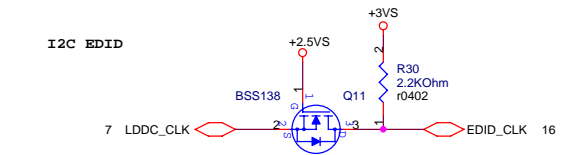
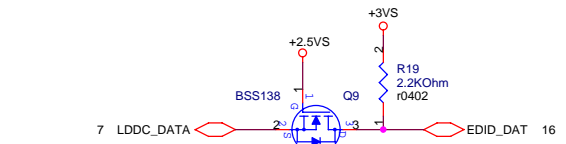
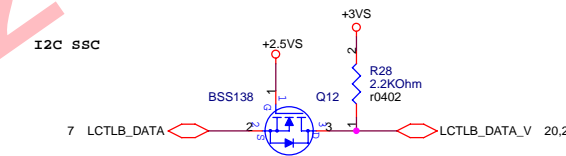
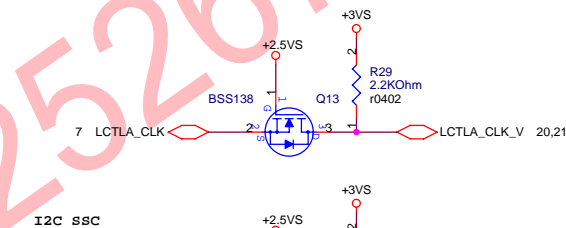
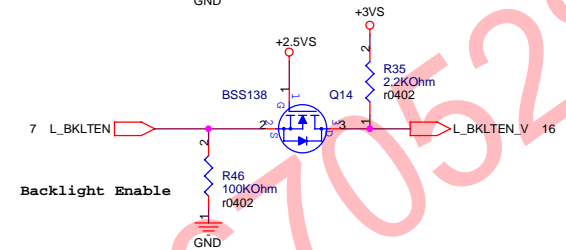
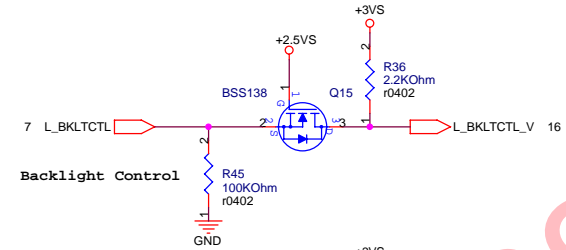
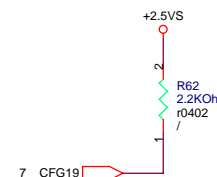
CFG18 : VCC SELECT

LOW = 1.05V (Default)
 HIGH = 1.5V



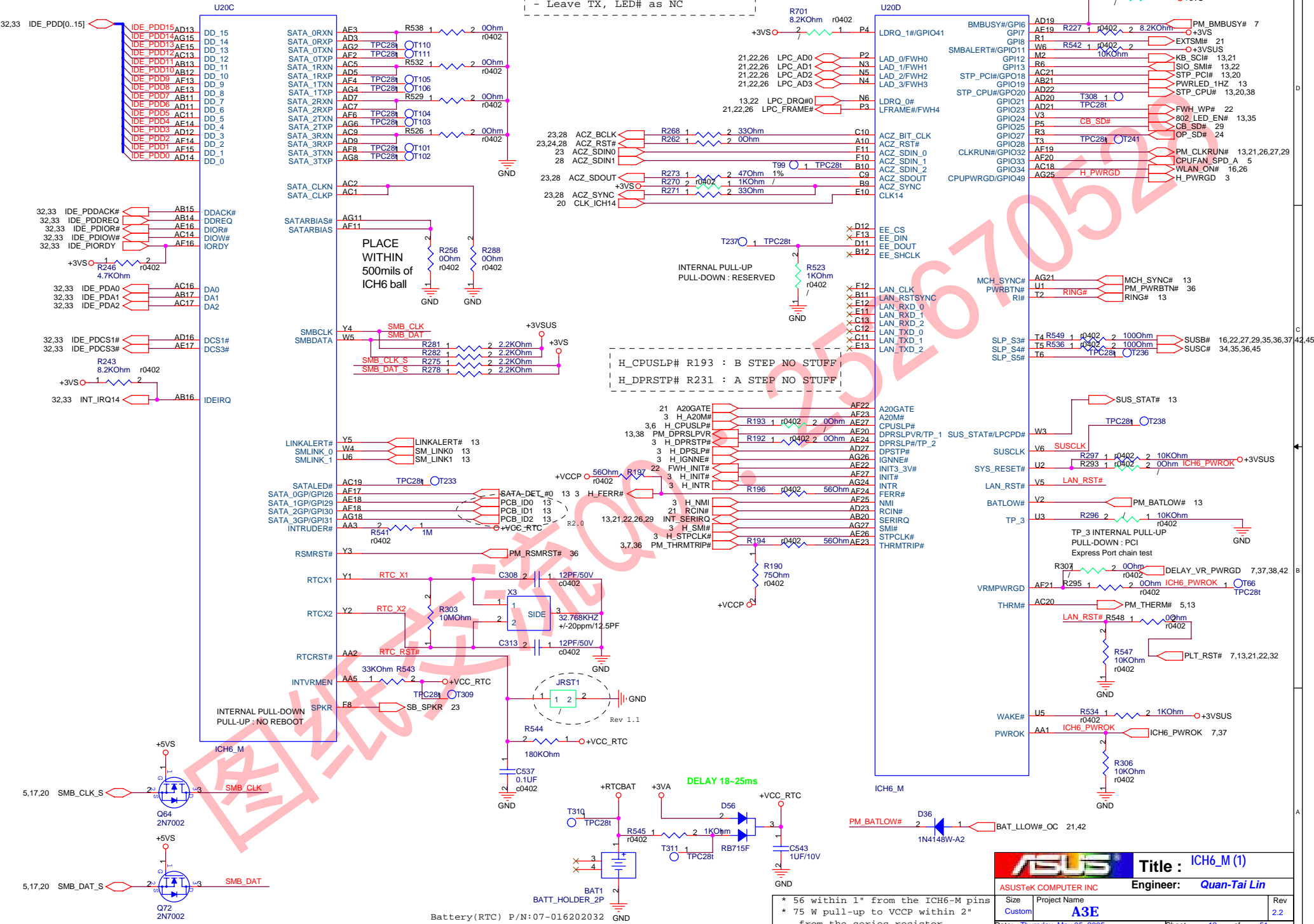
CFG19 : VTT SELECT

LOW = 1.05V (Default)
 HIGH = 1.2V



ICH6-M from 02-010002500 change to 02-010004402 on bom list

Unused SATA pin
- Connect RX, RBIAS, CLK to GND
- Leave TX, LED# as NC

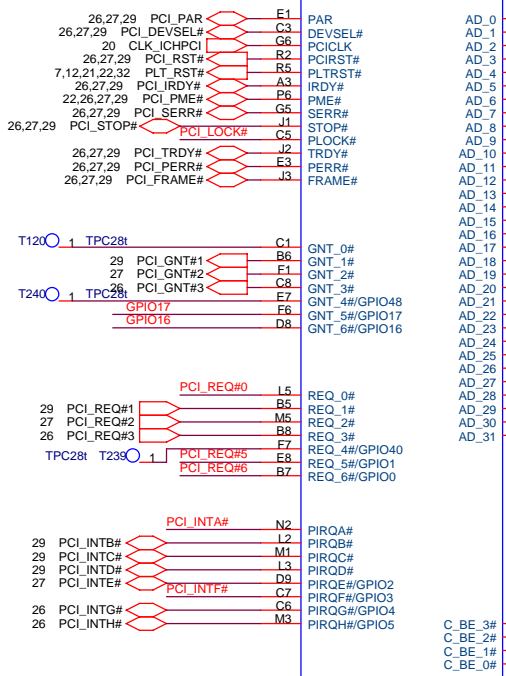


ASUS Title : ICH6_M (1)
 ASUSTek COMPUTER INC Engineer: Quan-Tai Lin
 Size Project Name
 Custom A3E
 Date: Thursday, May 05, 2005 Sheet 12 of 51

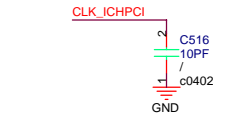
* 56 within 1" from the ICH6-M pins
 * 75 W pull-up to VCCP within 2" from the series resistor

Battery (RTC) P/N: 07-016202032

U20A

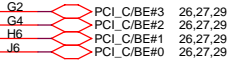
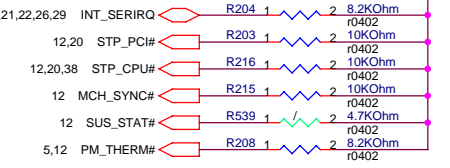
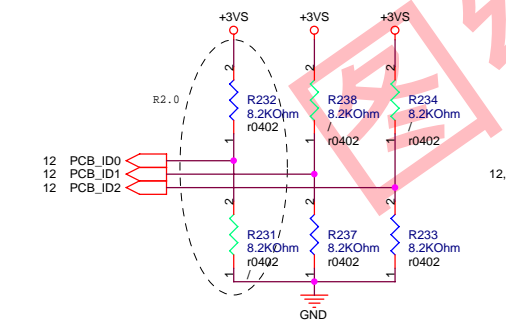


ICH6_M



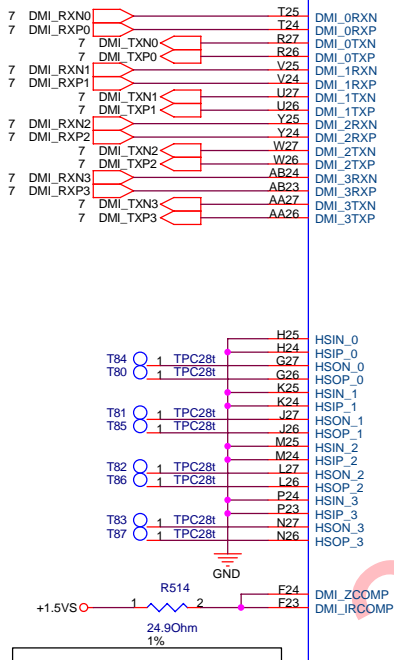
PCB_VID 0 1 2
MB_V1.0 0 0 0

PCB_VID3 : PROJECT CODE

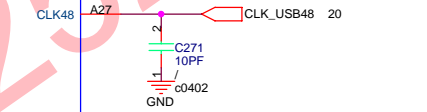
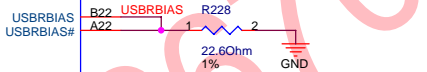
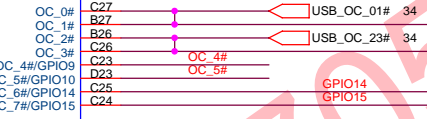
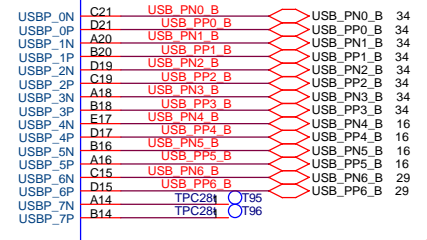
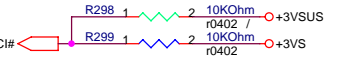
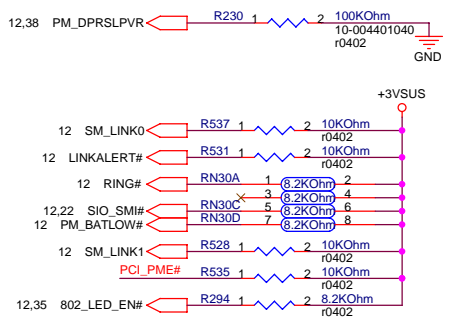


PLACE within 500mils of ICH. 5.5mil/8mil

U20B



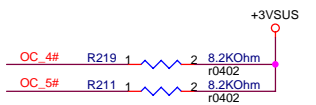
ICH6_M



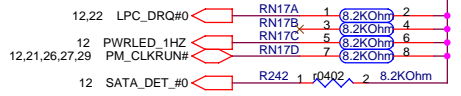
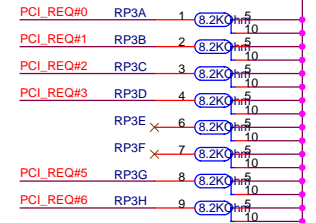
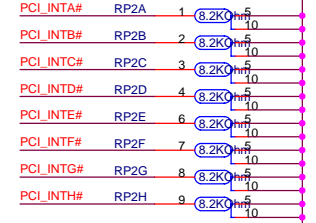
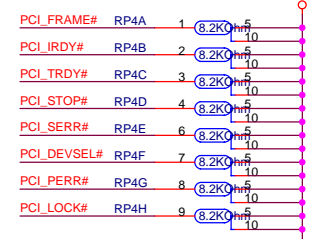
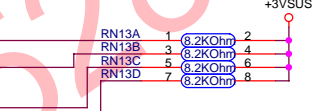
PLACE within 500mils of ICH.

INTERNAL PULL-DOWN SIGNALS :
AC_BITCLK, AC_RST#, AC_SDIN[2:0],
AC_SDOUT, AC_SYNC, DPSPVPR,
LAN_CLK, PDD[7], SDD[7],
PDDREQ, SDDREQ, SPKR,
USB[7:0][P,N]

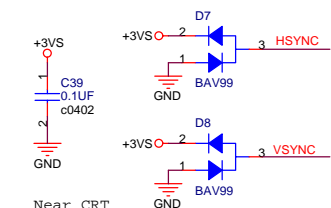
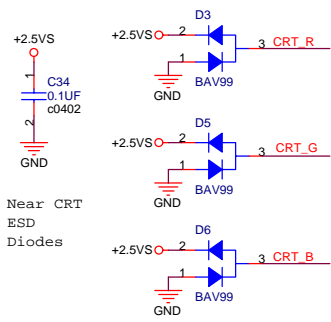
INTERNAL PULL-UP SIGNALS :
EE_DIN, EE_DOUT,
GNT[B:A]#, GNT[5]#,
GPIO[17:16], LAD[3:0]#,
LDRQ[1:0], LAN_RXD[2:0],
PME#, PWRBTN#



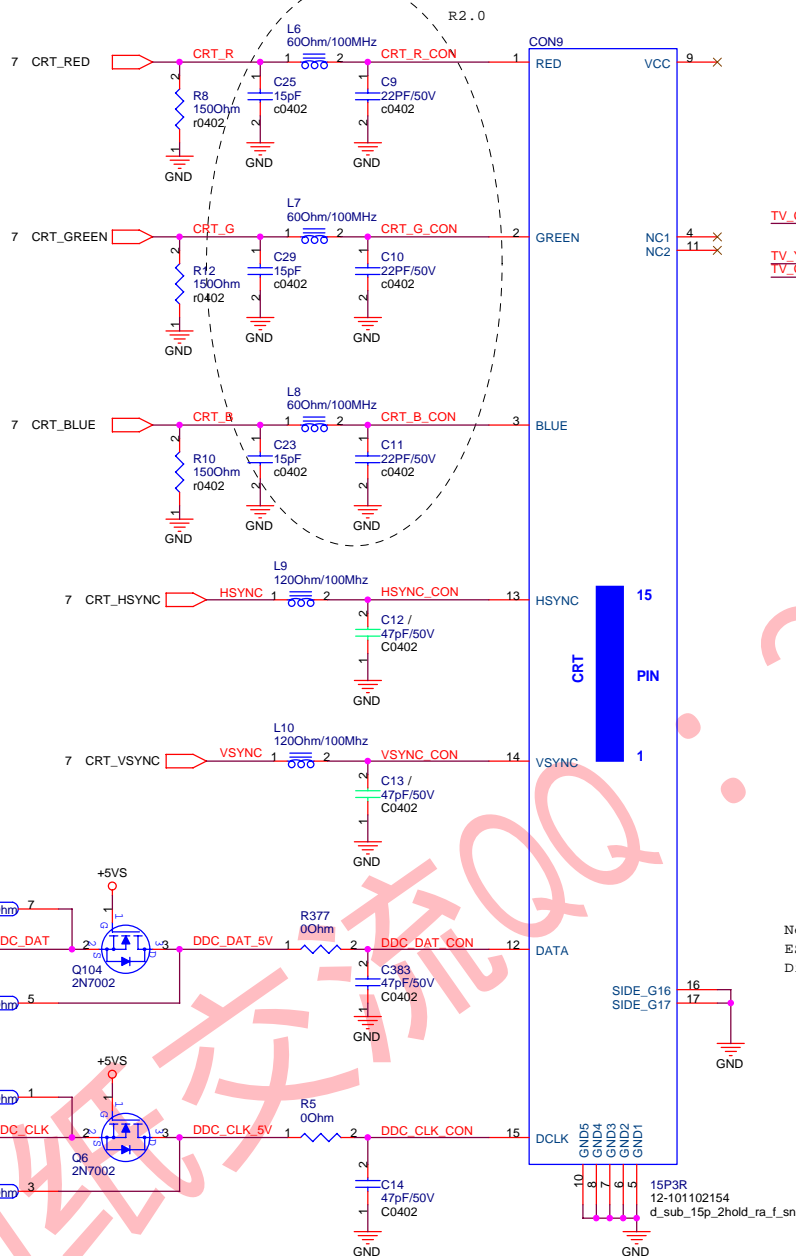
(USB 4 for CAMERA)
(USB 5 for WLAN)



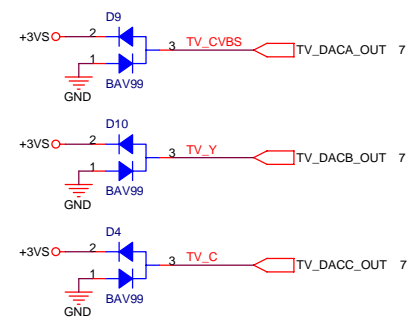
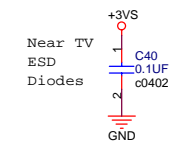
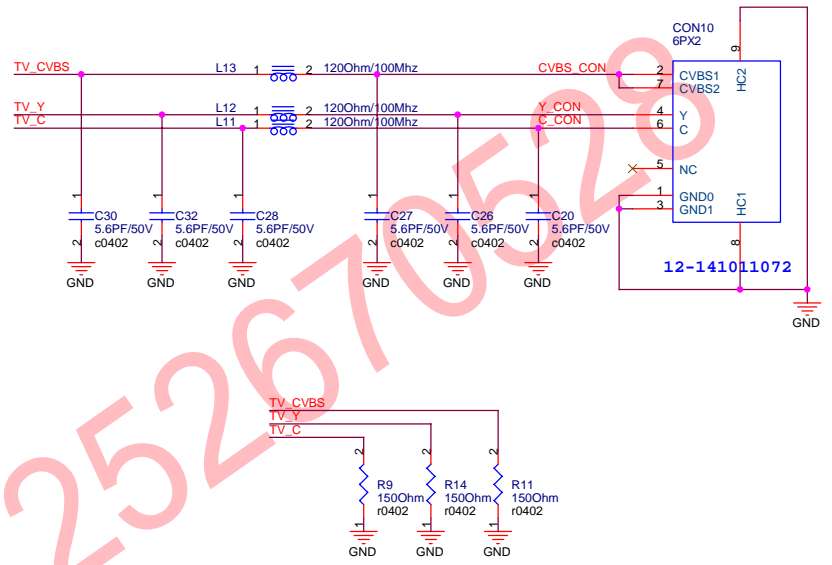
ASUS Title : ICH6_M (2)
ASUSTek COMPUTER INC Engineer: Quan-Tai Lin
Size Project Name
Custom A3E
Date: Thursday, May 05, 2005 Sheet 13 of 51



PLACE ESD Diodes near VGA port

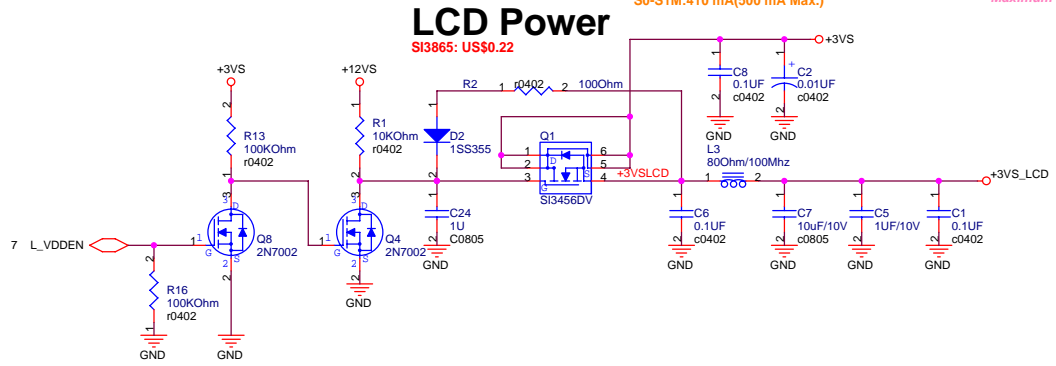


Note: CRT_Red, CRT Green, CRT Blue are ground reference.



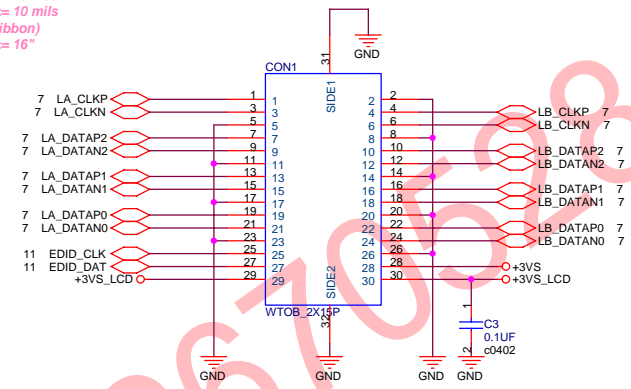
PLACE ESD Diodes near TV port

LCD Backlight Control

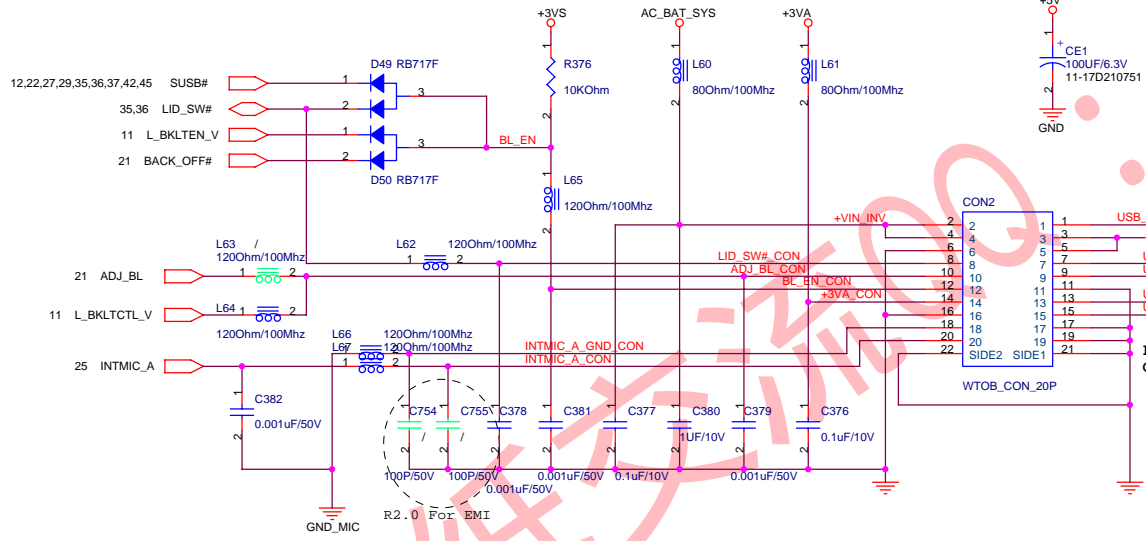


LCD LVDS Interface

Cable Requirement:
Impedance: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"

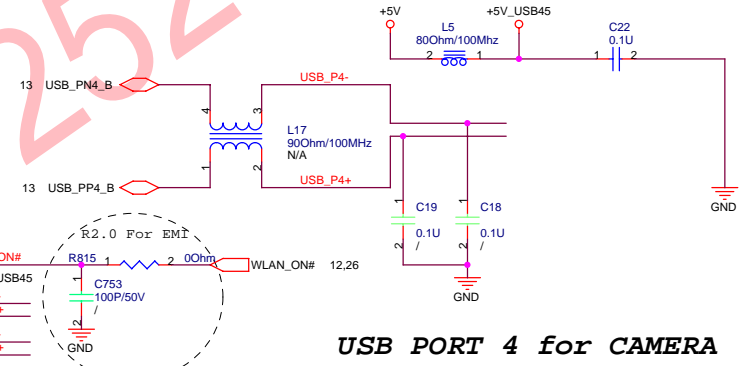


INVERTER Interface

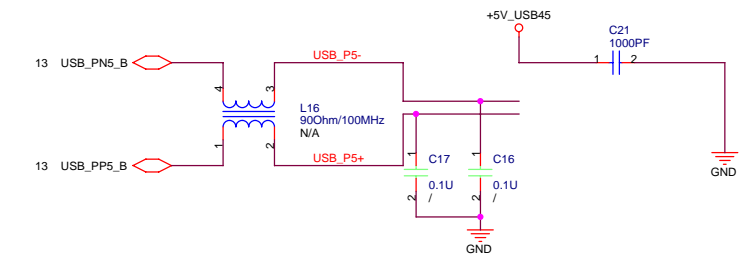


BIOS
ADJ_BL: KBC output D/A signal (adjust voltage level) to adjust Back light.

BIOS
BACK_OFF#:When user push "Fn+F7" button, BIOS active this pin to turn off back light.

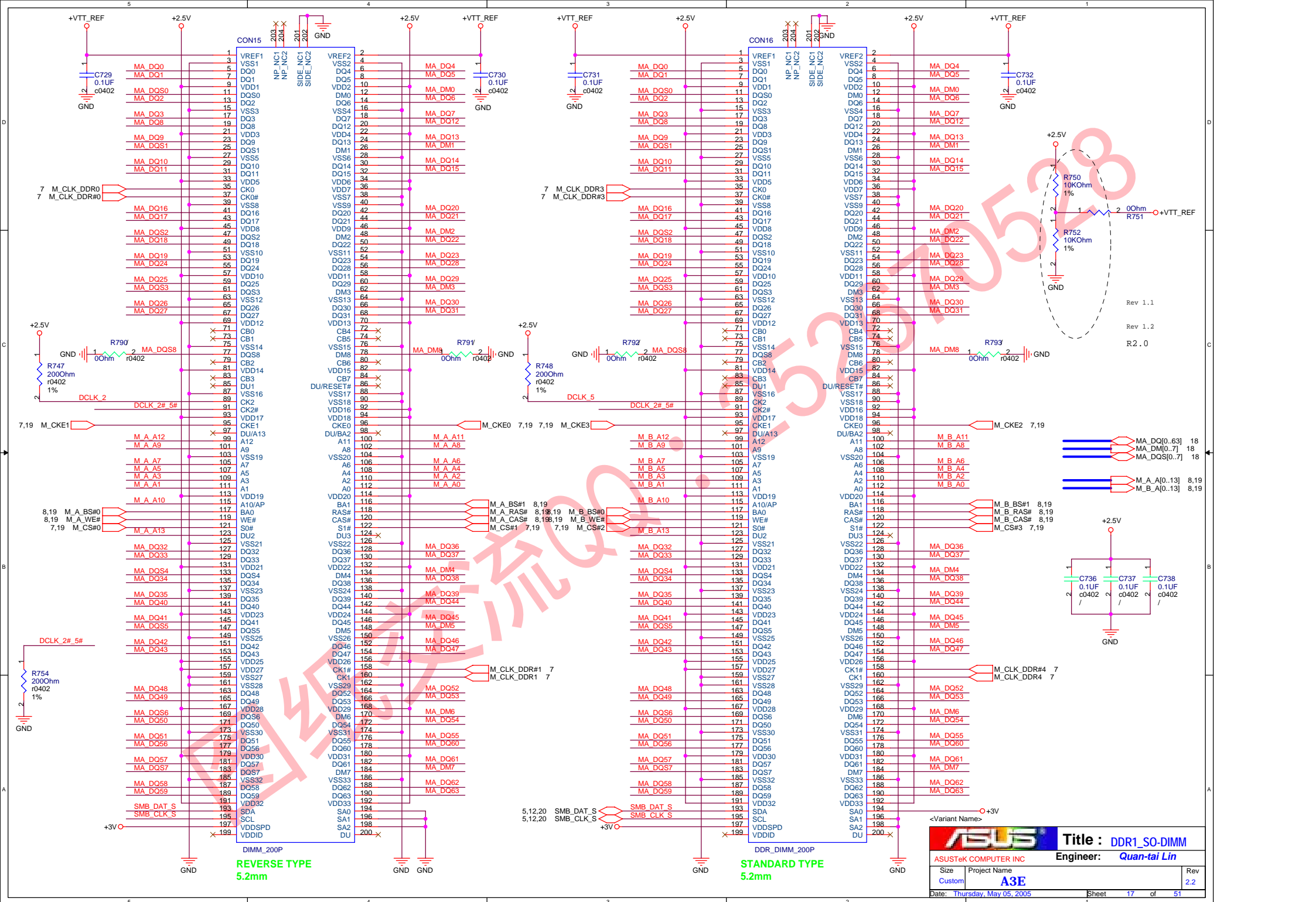


Pin 19 : Add a USB 2.0 Shielding GND cable to USB module.



700Vrms@5 mAms
(Min. 3 mAms)6 mAms(Max. 6.5 mAms)

ASUS		Title : LVDS & INVERTER	
ASUSTeK COMPUTER INC		Engineer: Quan-Tai Lin	
Size	Project Name	Rev	
Custom	A3E	2.2	
Date: Thursday, May 05, 2005	Sheet	16	of 51



ASUS
ASUSTek COMPUTER INC
Title : DDR1_SO-DIMM
Engineer: *Quan-tai Lin*

Size	Project Name	Rev
Custom	A3E	2.2

Date: Thursday, May 05, 2005 Sheet 17 of 51

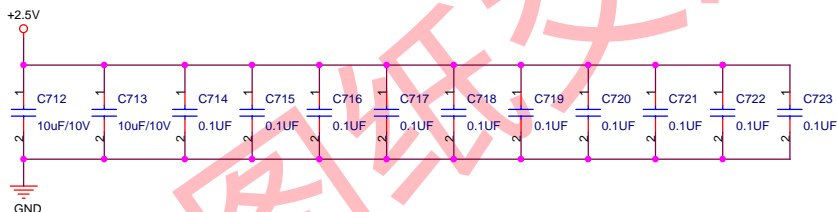
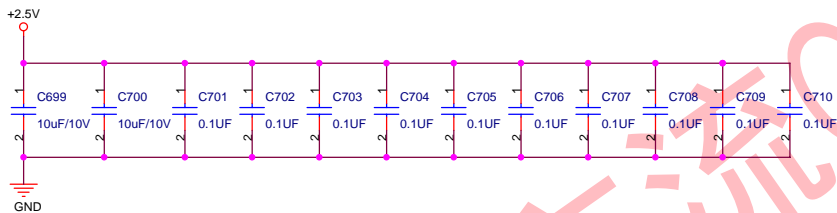
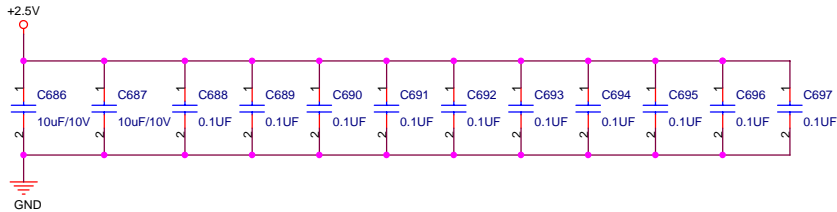
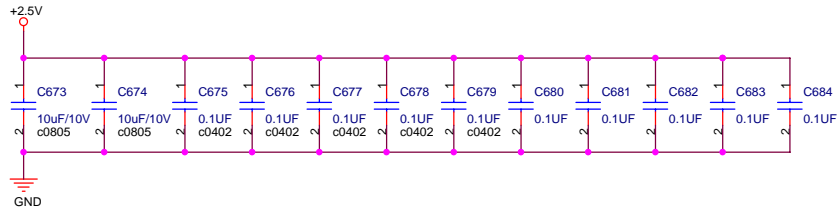
M_A_DQ[0..63] 8
M_A_DQS[0..7] 8
M_A_DM[0..7] 8

MA_DQ[0..63] 17
MA_DQS[0..7] 17
MA_DM[0..7] 17



<Variant Name>

ASUS		Title DDR DATA TERMINATION	
ASUSTek COMPUTER INC		Engineer: <i>Quan-tai Lin</i>	
Size	Project Name		Rev
Custom	A3E		2.2
Date: Thursday, May 05, 2005		Sheet	18 of 51



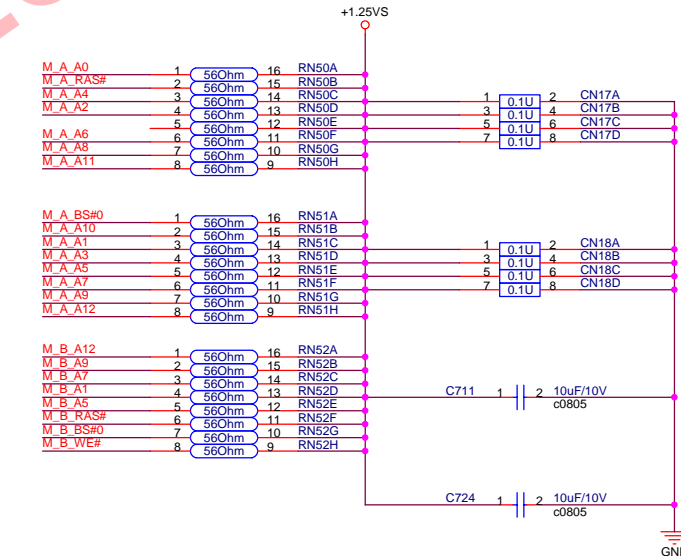
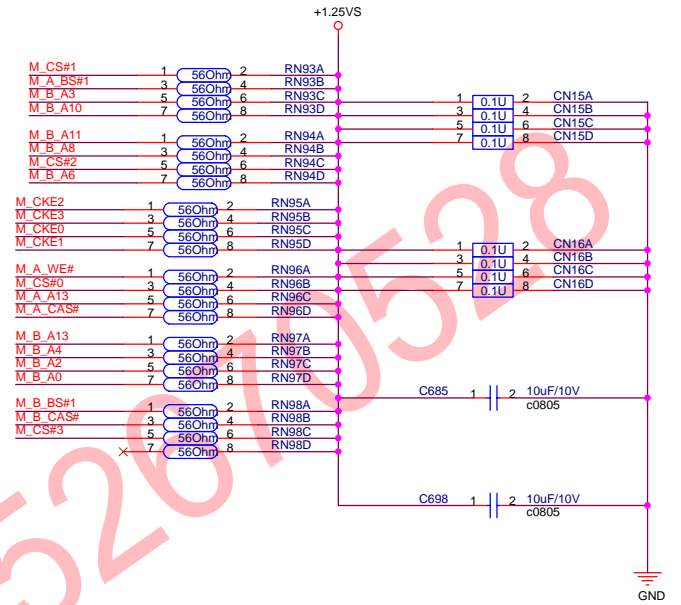
- M_A_A[0..13] 8,17
- M_B_A[0..13] 8,17
- M_CKE[0..3] 7,17
- M_CS[0..3] 7,17

- M_B_RAS# 8,17
- M_B_CAS# 8,17
- M_B_WE# 8,17

- M_A_RAS# 8,17
- M_A_CAS# 8,17
- M_A_WE# 8,17

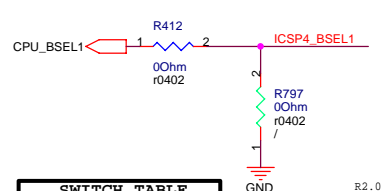
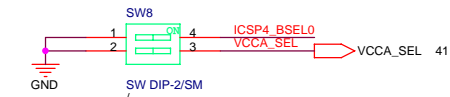
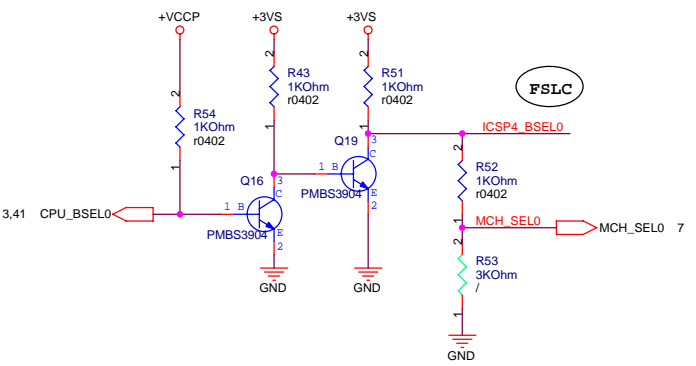
- M_A_BS#0 8,17
- M_A_BS#1 8,17

- M_B_BS#0 8,17
- M_B_BS#1 8,17

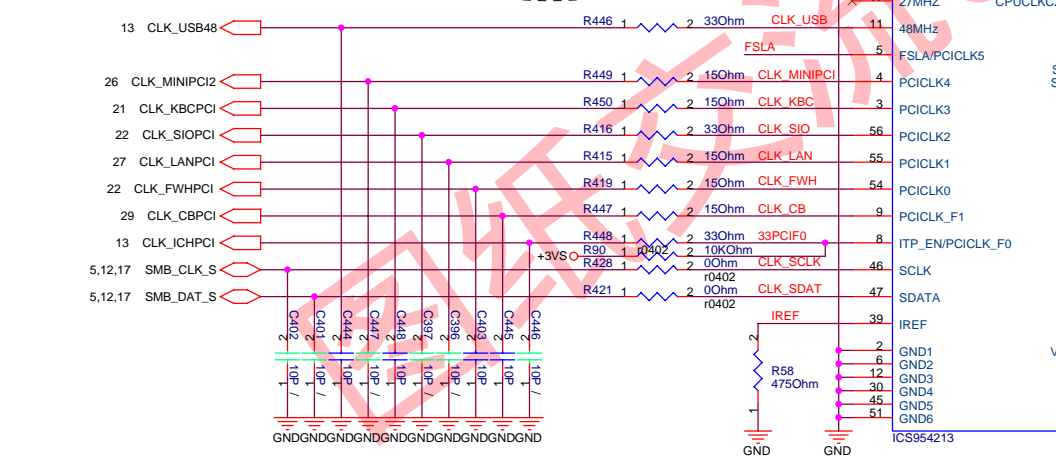


<Variant Name>

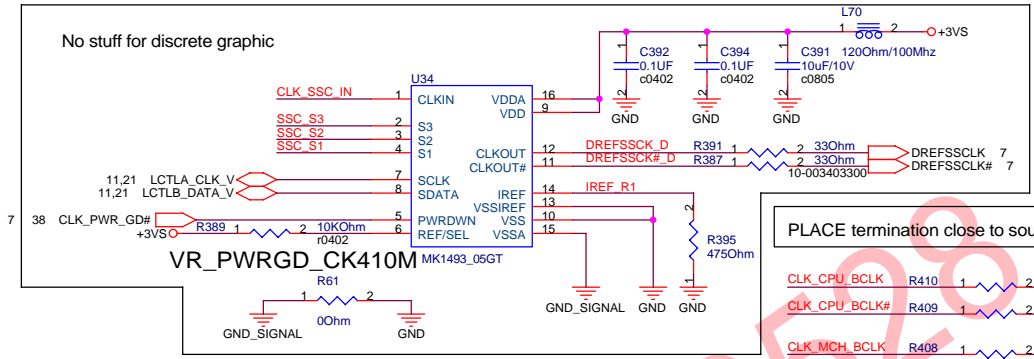
Bus	Rate	Rate	CPU	SBC	SATA	PCI
FSLC	FSLA	FSLA	200.00	100.00	100.00	33.33
0	0	1	133.33	100.00	100.00	33.33
0	1	0	200.00	100.00	100.00	33.33
0	1	1	133.33	100.00	100.00	33.33
1	0	0	333.33	100.00	100.00	33.33
1	0	1	133.33	100.00	100.00	33.33
1	1	0	400.00	100.00	100.00	33.33



SWITCH TABLE		
	1or4	2or3
Dothan 533	4	3
Dothan 400	1	2
Celeron	1	2
Banias	1	2

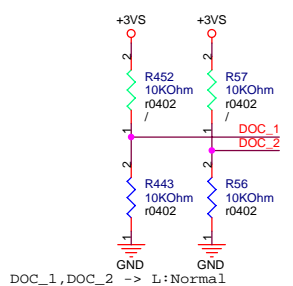
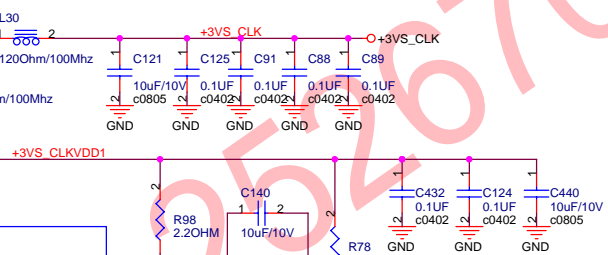


R441 10K pull up to +3VS for CPUCLK2_ITP
 R442 10K pull down to GND for SRC5

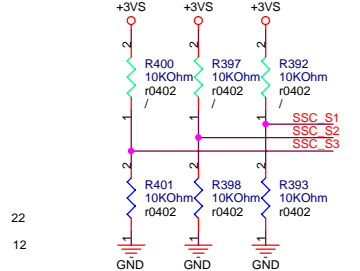


PLACE termination close to source IC

- CLK_CPU_BCLK R410 1 2 49.0Ohm r0402
- CLK_CPU_BCLK# R409 1 2 49.0Ohm r0402
- CLK_MCH_BCLK R408 1 2 49.0Ohm r0402
- CLK_MCH_BCLK# R407 1 2 49.0Ohm r0402
- DREFCLK R454 1 2 49.0Ohm r0402
- DREFCLK# R453 1 2 49.0Ohm r0402
- CLK_PCIE_ICH R455 1 2 49.0Ohm r0402
- CLK_PCIE_ICH# R456 1 2 49.0Ohm r0402
- CLK_MCH_3GPLL R406 1 2 49.0Ohm r0402
- CLK_MCH_3GPLL# R405 1 2 49.0Ohm r0402
- DREFSSCLK R396 1 2 49.0Ohm r0402
- DREFSSCLK# R388 1 2 49.0Ohm r0402



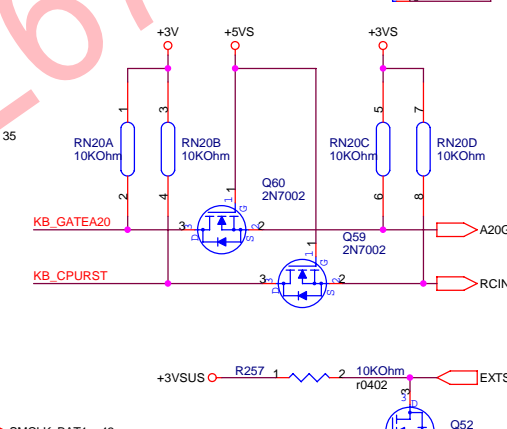
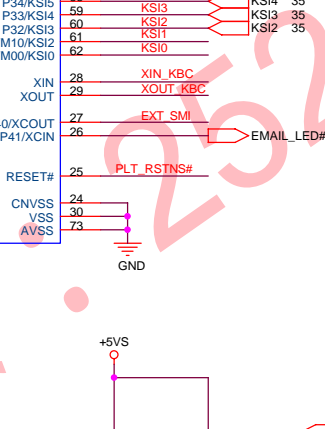
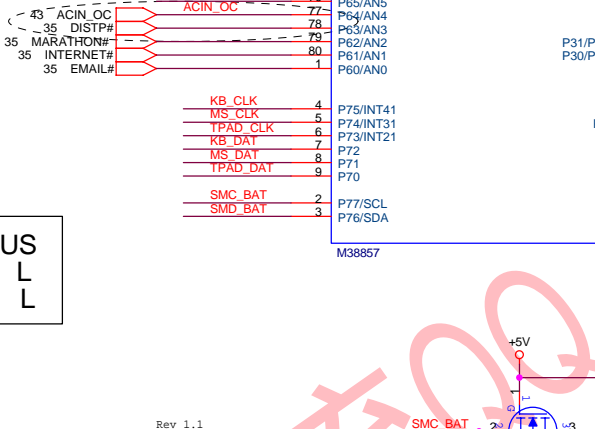
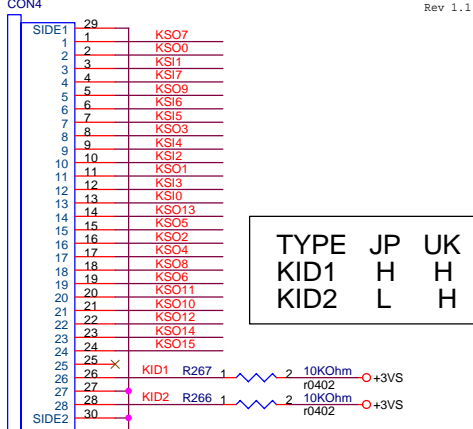
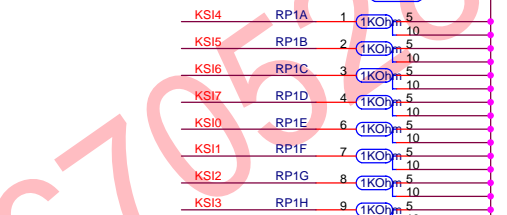
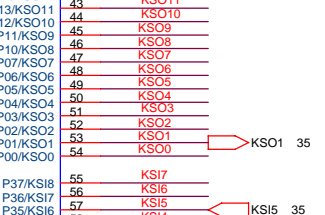
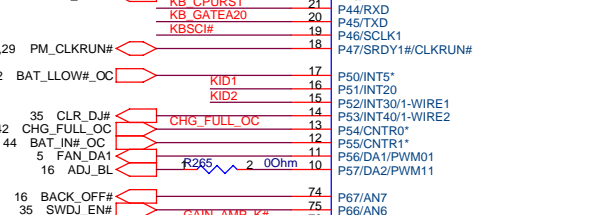
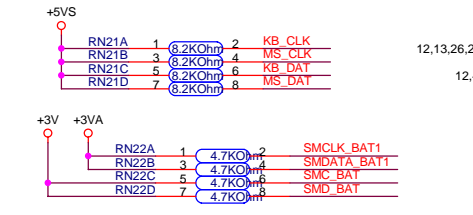
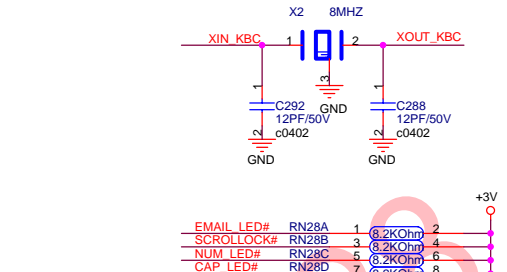
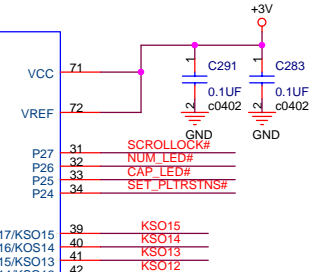
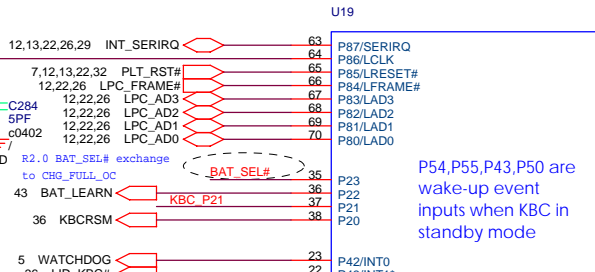
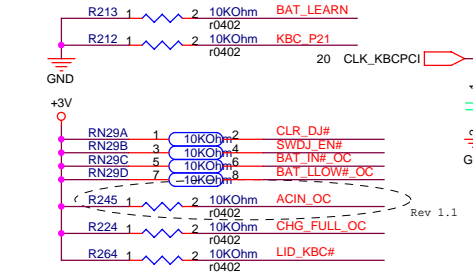
H: Freq will jump to a preprogrammed value in the I2C



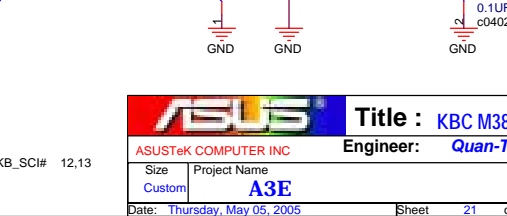
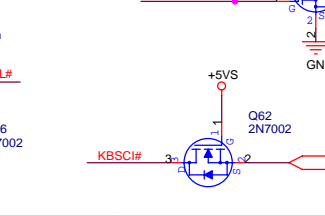
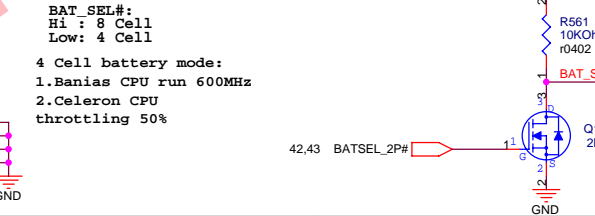
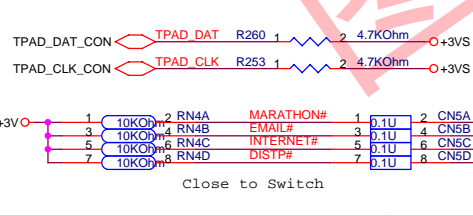
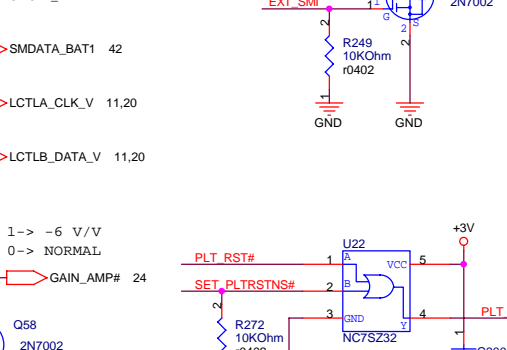
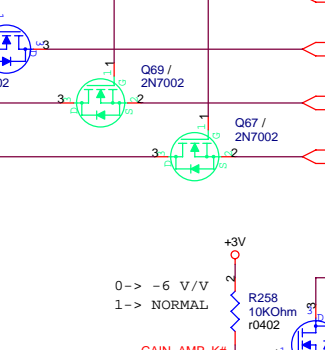
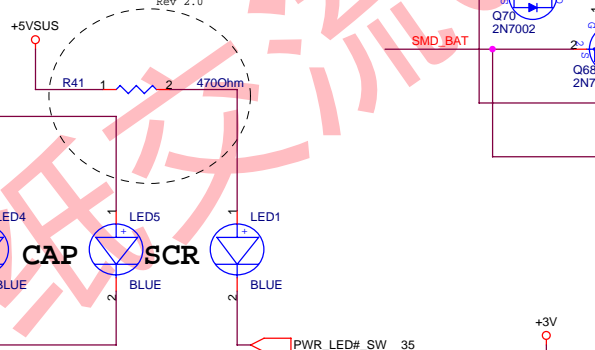
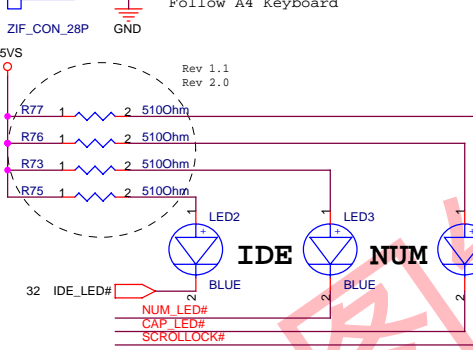
ASUS Title: **CLOCK GEN**
 ASUSTek COMPUTER INC Engineer: **Quan-Tai Lin**

Size	Project Name	Rev
Custom	A3E	2.2

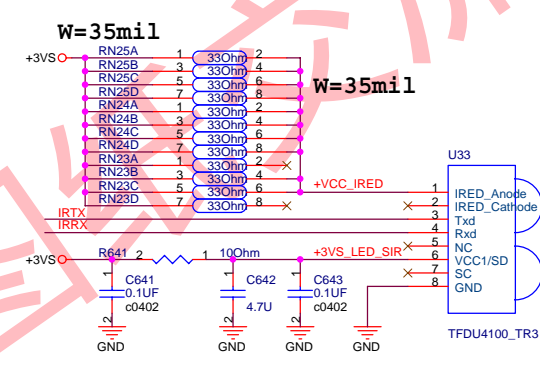
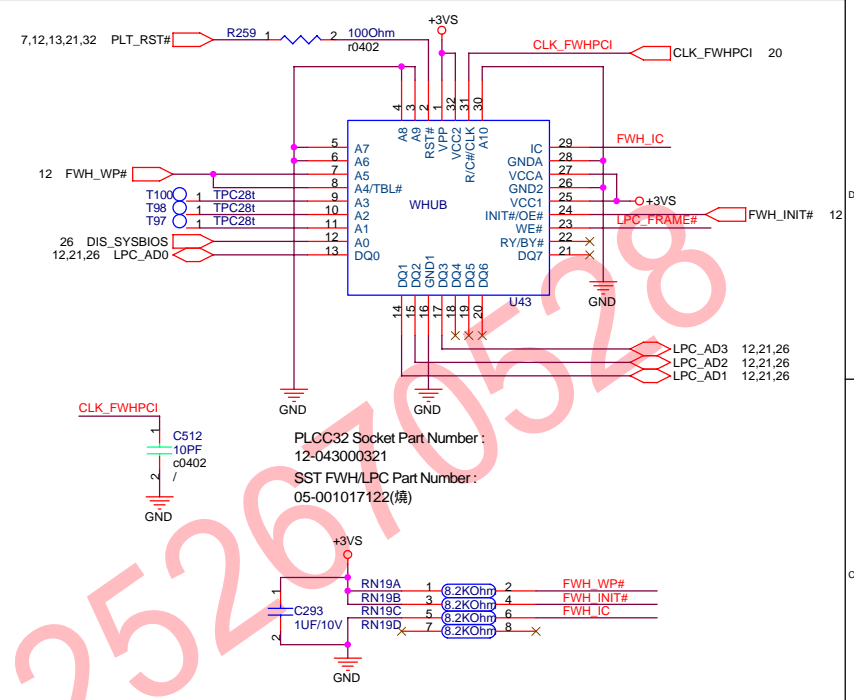
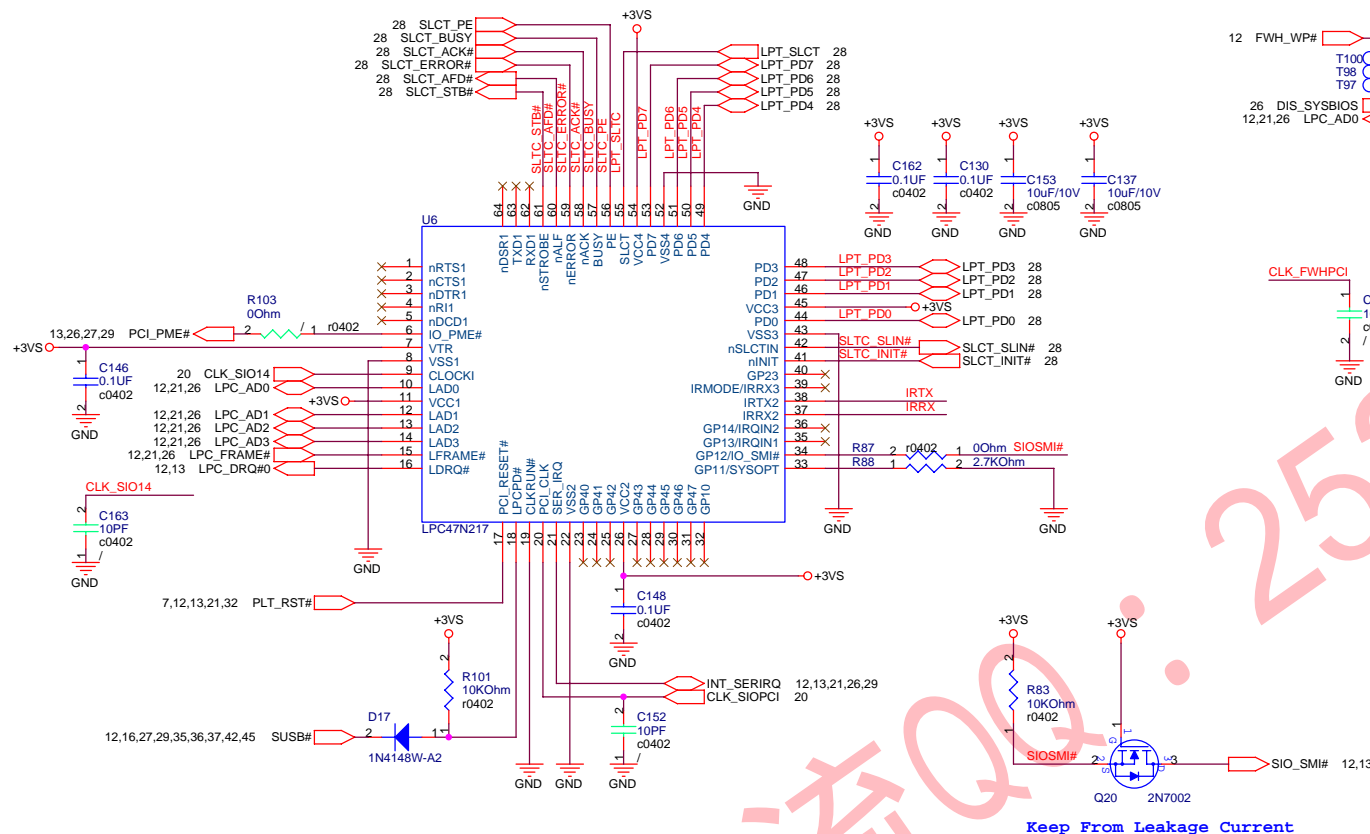
Date: Thursday, May 05, 2005 Sheet 20 of 51



TYPE	JP	UK	US
KID1	H	H	L
KID2	L	H	L

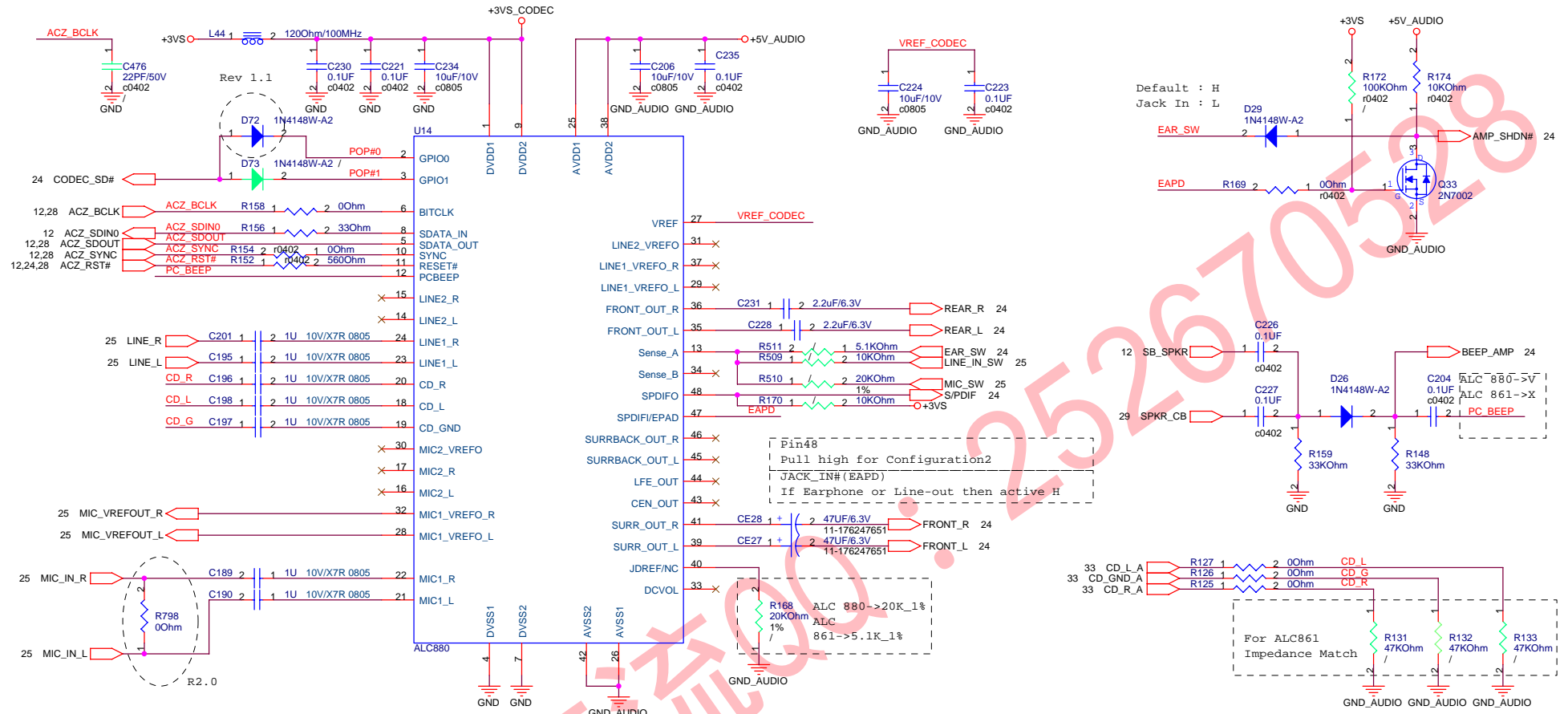


Super I/O

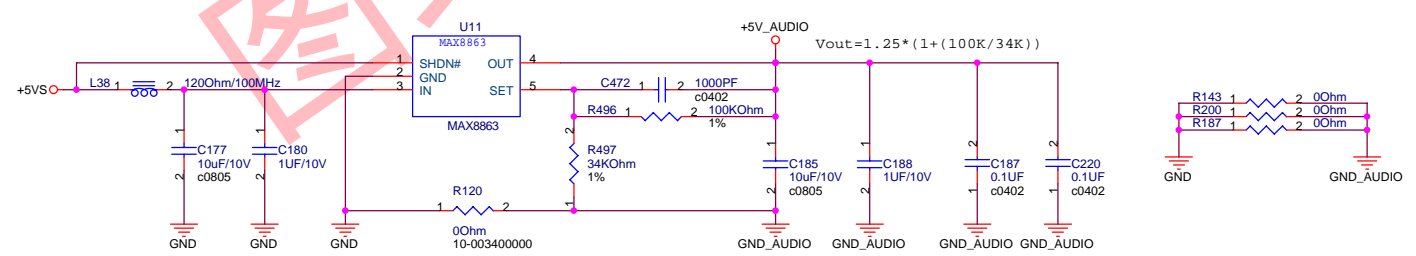
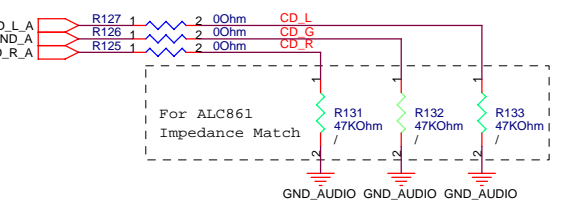
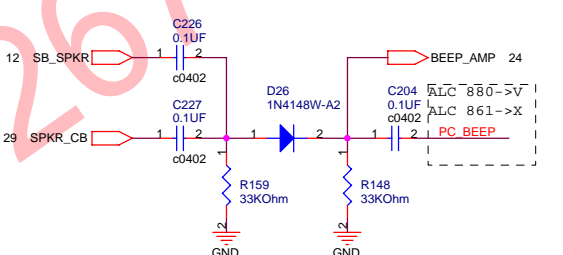
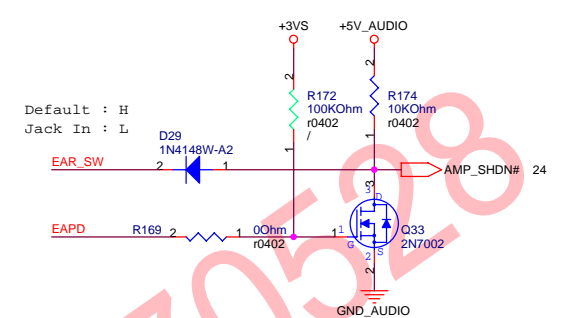


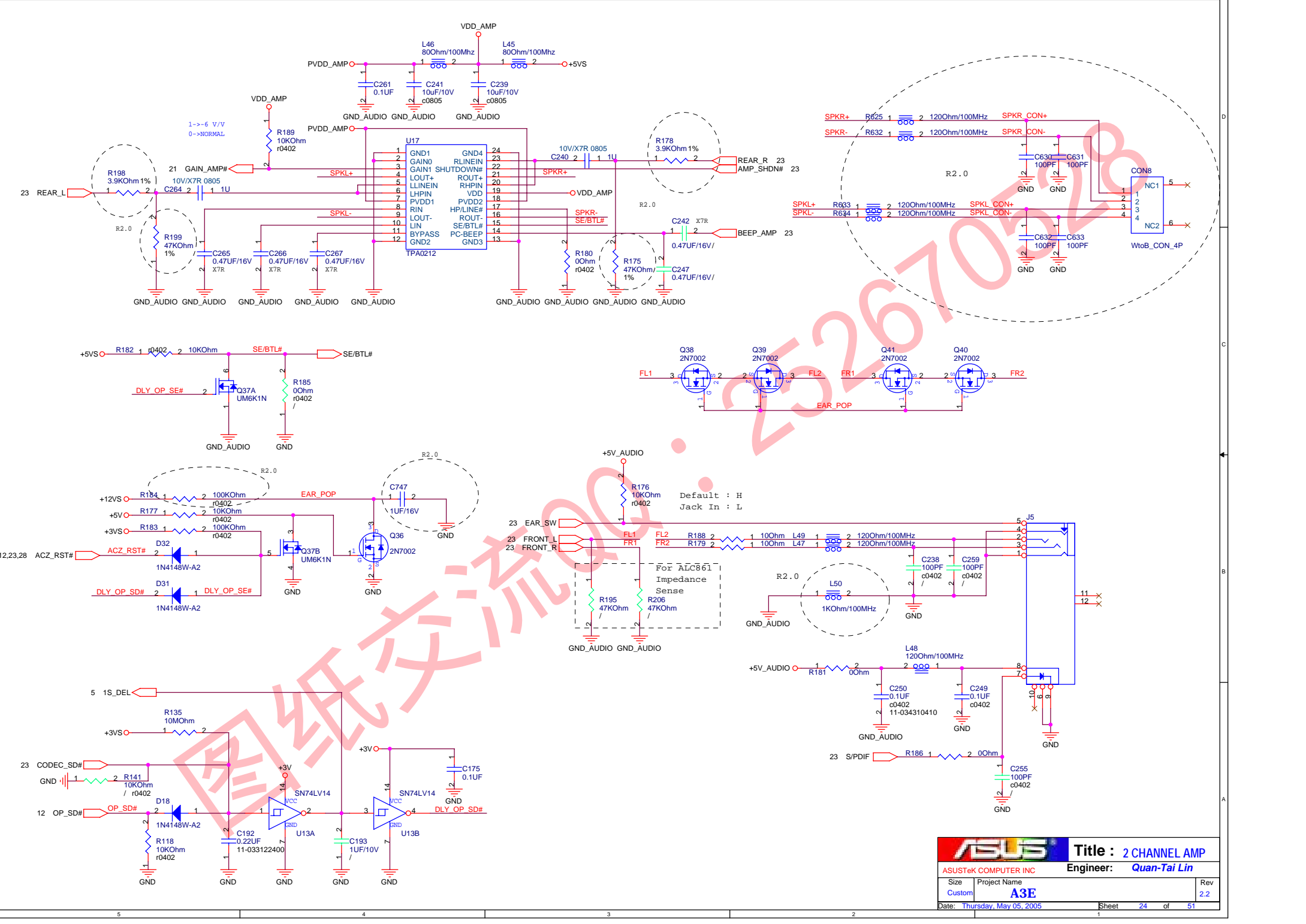
Keep From Leakage Current

ASUS		Title : FWH / SIO / SIR	
ASUSTek COMPUTER INC		Engineer: Quan-Tai Lin	
Size	Project Name	Rev	
Custom	A3E	2.2	
Date: Thursday, May 05, 2005		Sheet	22 of 51

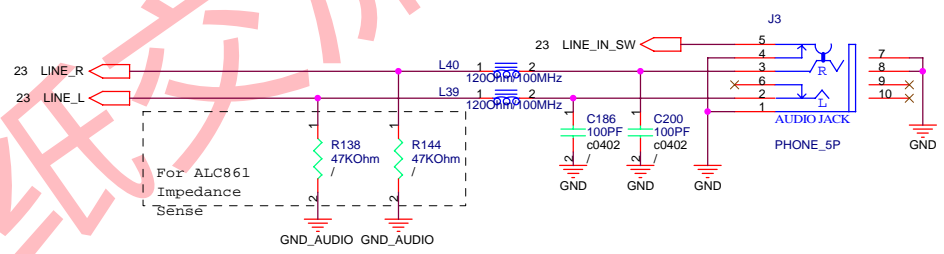
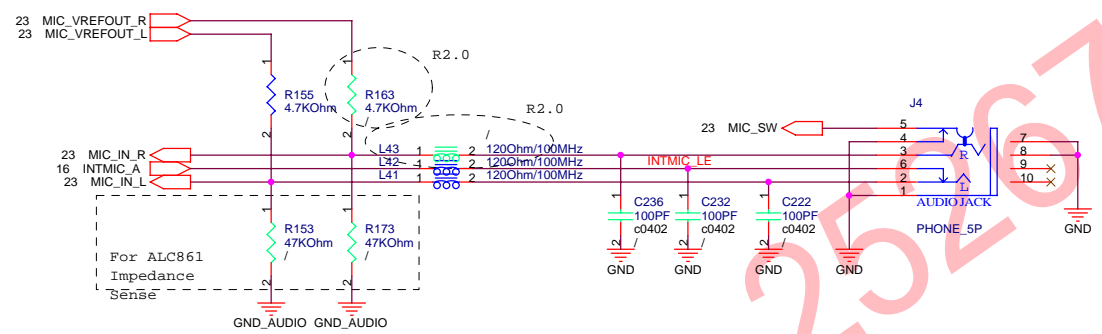
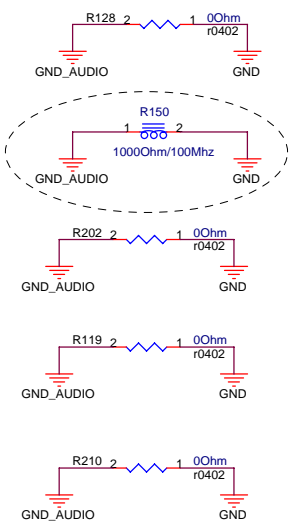
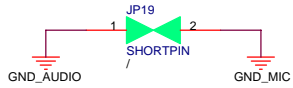


ALC880/ALC861
 Circuit P/N : 02-611000400
 ,BOM P/N : 02-611000413



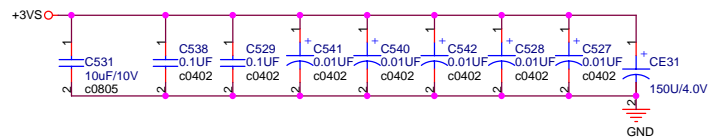
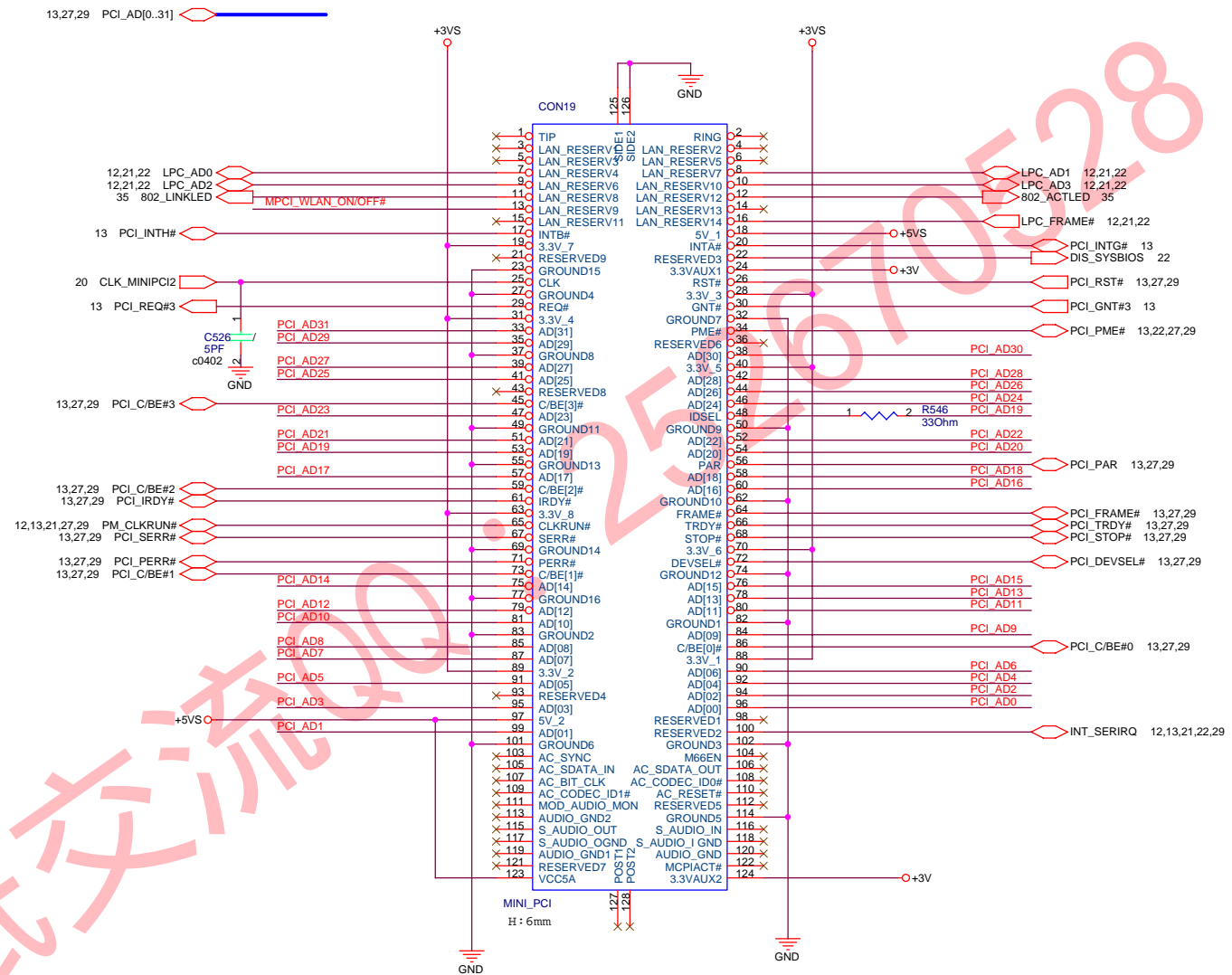
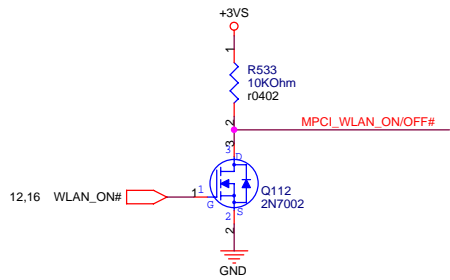


INTMIC_A:GND_AUDIO
: W/P/X = 12/5/15mils



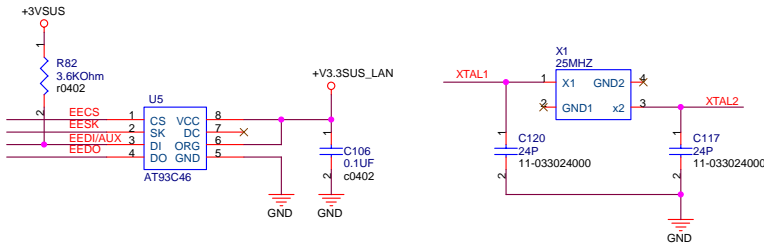
252670528
 图纸交流QQ

		Title : MIC / Line-IN Jack	
ASUSTek COMPUTER INC		Engineer: <i>Quan-Tai Lin</i>	
Size	Project Name		Rev
Custom	A3E		2.2
Date: Thursday, May 05, 2005		Sheet	25 of 51

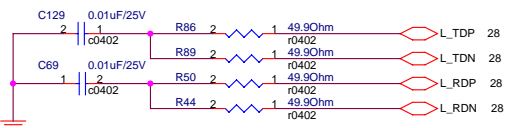


25670128
 图纸交流

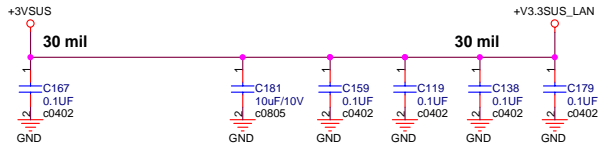
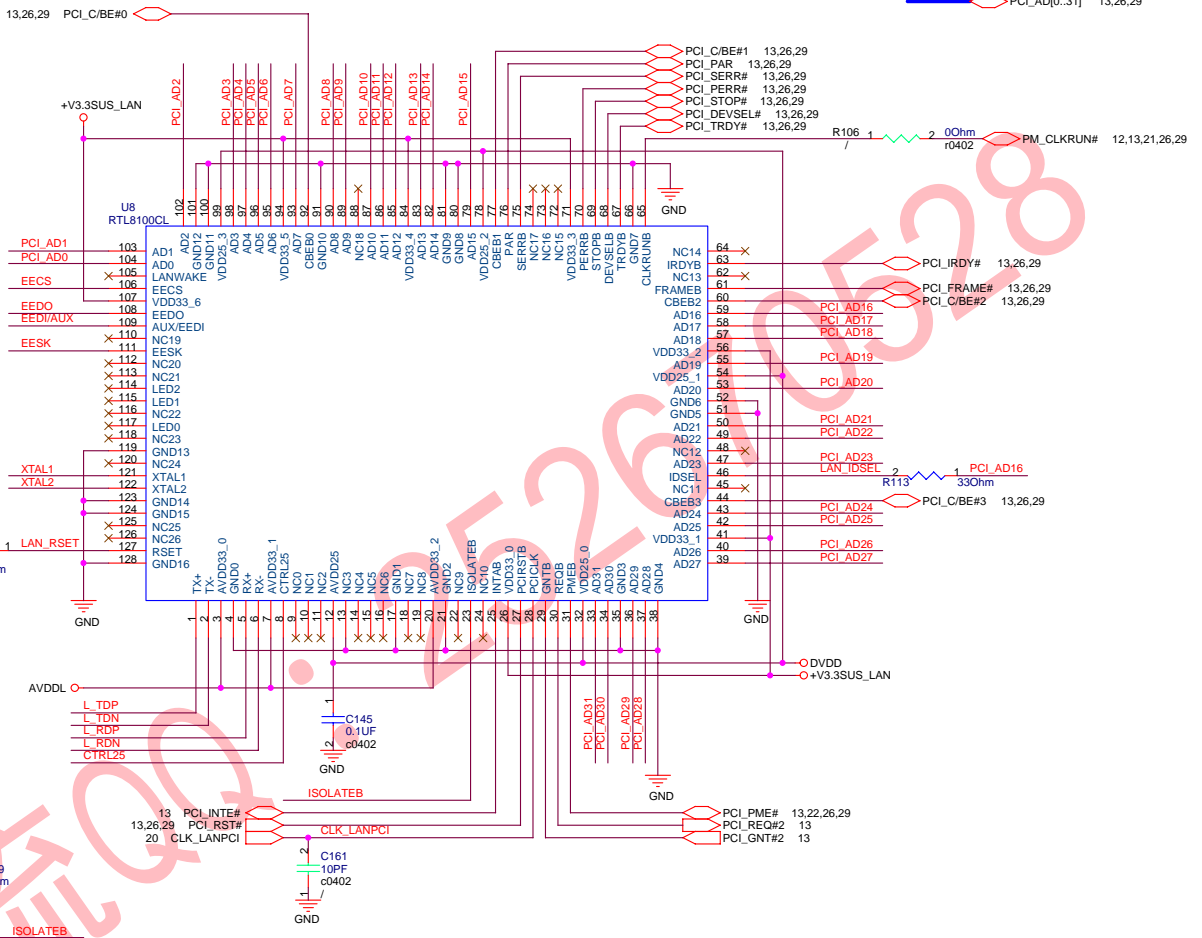
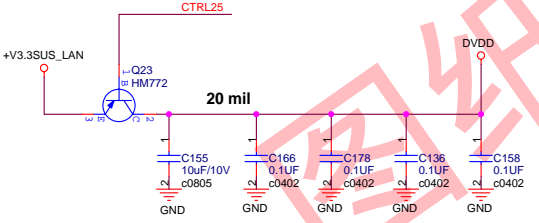
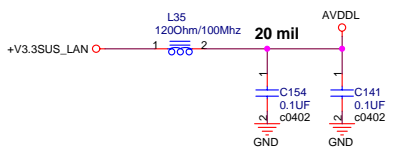
ASUS		Title : MINIPCI (802.11)	
ASUSTek COMPUTER INC		Engineer: Quan-Tai Lin	
Size	Project Name	Rev	
Custom	A3E		2.2
Date: Thursday, May 05, 2005		Sheet	26 of 51



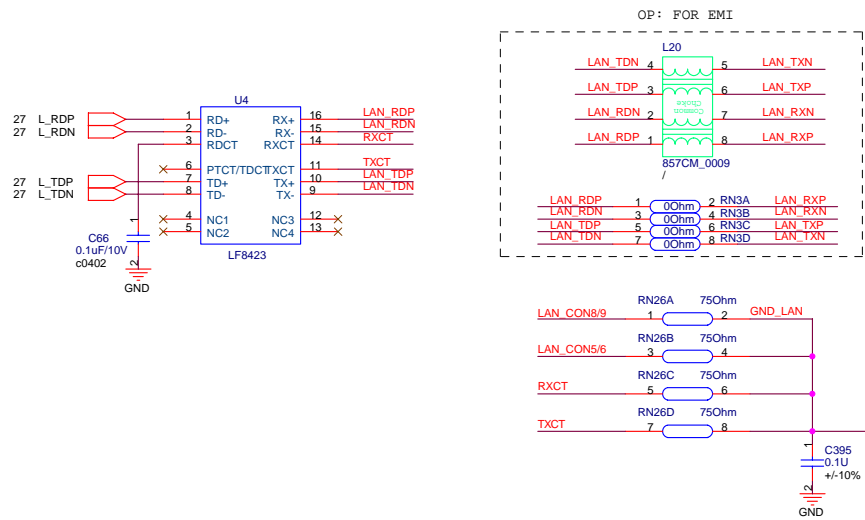
L_TDP ,L_TDN termination resistors should be near chip



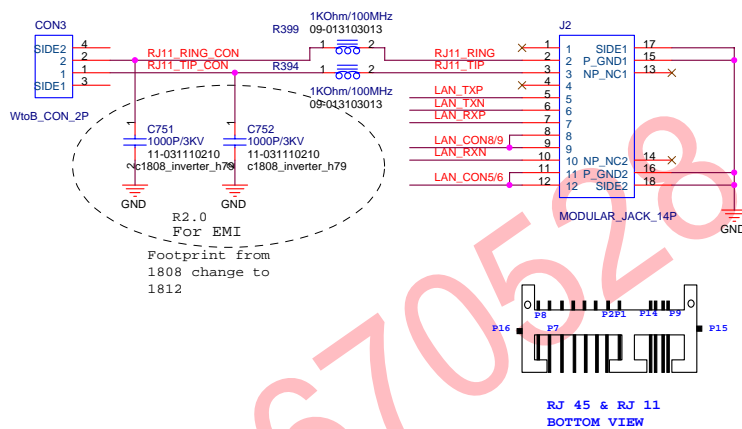
L_RDP ,L_RDN termination resistors should be near transformer-U32



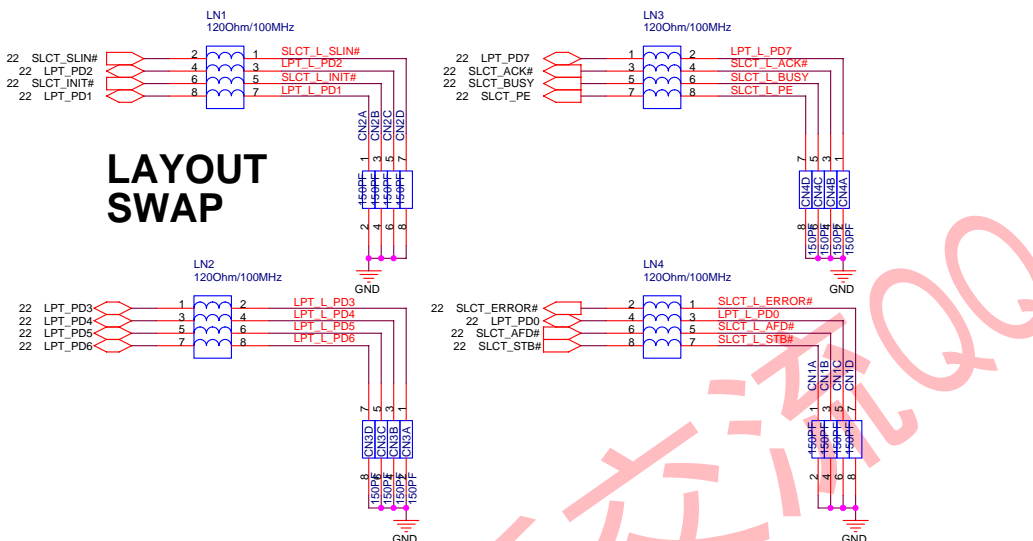
LAN PORT



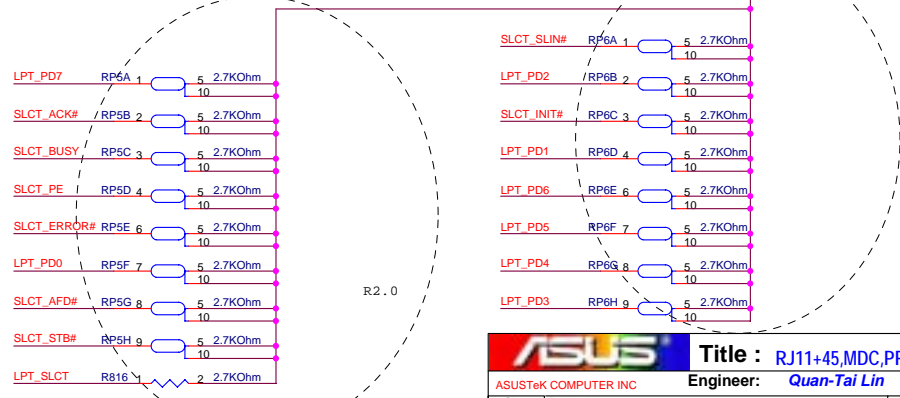
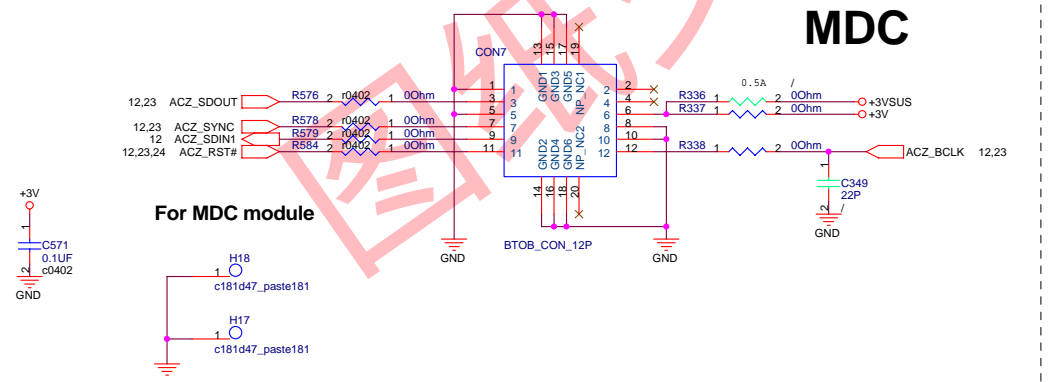
PRINT PORT

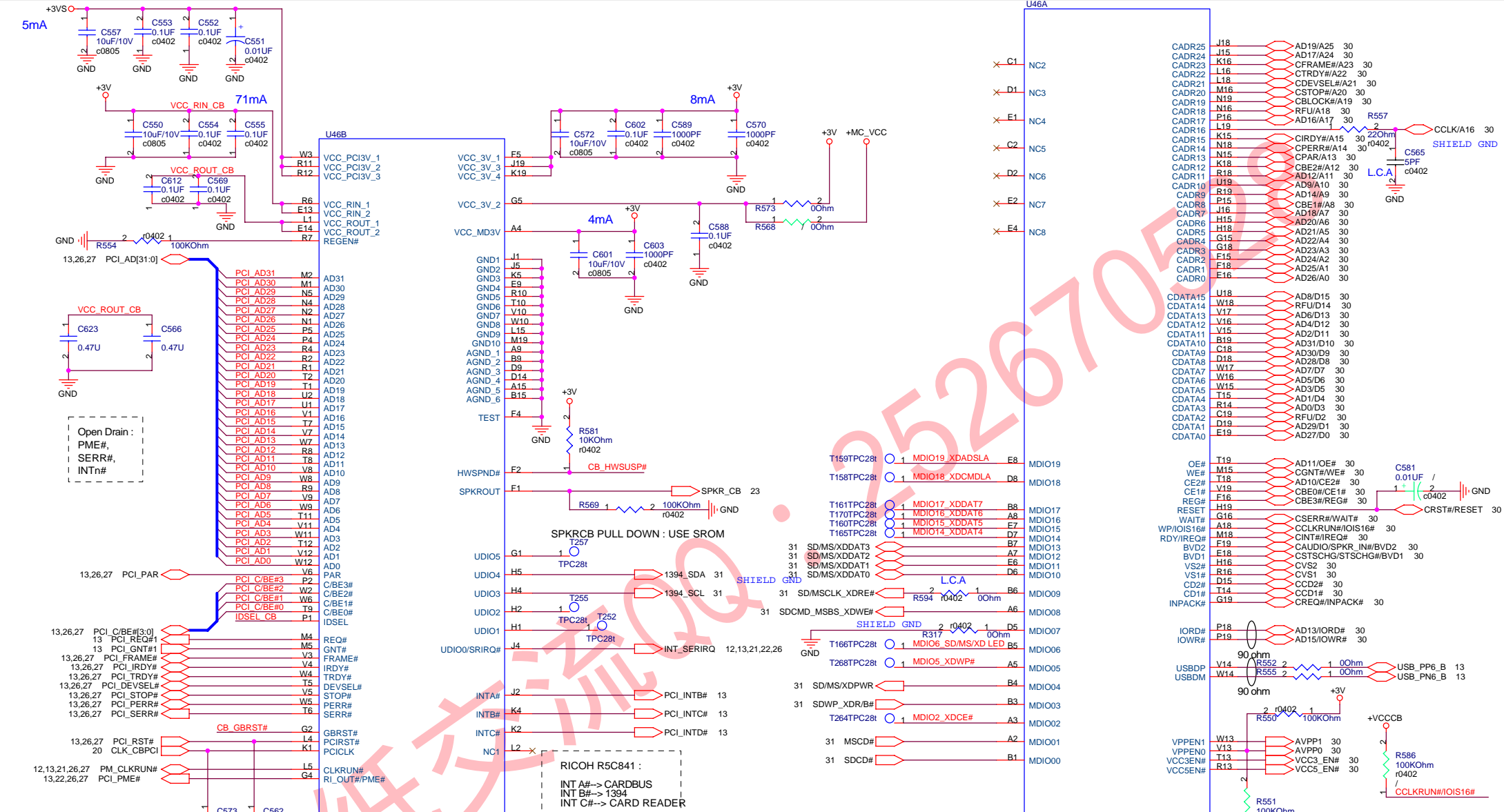


LAYOUT SWAP



MDC

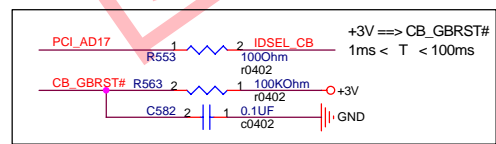




VCC_3V POWER :
 PME#, SPKROUT, RI_OUT#
 HWSUSP#, GBRST#, IRQn
 CCD1#, CCD2#, VS1#, VS2#
 TEST, VCC5EN#, VCC3EN#
 VPPEN0, VPPEN1, SD/MS I/F

VCCPCI POWER :
 PCI BUS

VCC_SLOT POWER :
 CARD_BUS,
 CAUDIO, CSTSCHG



RICOH R5C841 :
 INT A#--> CARDBUS
 INT B#--> 1394
 INT C#--> CARD READER

MDIO00--> SD Card Detect
 MDIO01--> MS Card Detect
 MDIO02--> XD Card Enable
 MDIO03--> SD Write Protect XD Card Ready/Busy#
 MDIO04--> SD/MS/XD Card Power0 Control
 MDIO05--> XD Card Write Protect
 MDIO06--> SD/MSXD LED
 MDIO07--> SD/MS External Clock
 MDIO08--> SD Command/MS Bus State /XD Card Write Enable
 MDIO09--> SD/MS Clock /XD Card Read Enable
 MDIO10--> SD/MS/XD Data 0
 MDIO11--> SD/MS/XD Data 1
 MDIO12--> SD/MS/XD Data 2
 MDIO13--> SD/MS/XD Data 3
 MDIO14--> XD Data 4
 MDIO15--> XD Data 5
 MDIO16--> XD Data 6
 MDIO17--> XD Data 7
 MDIO18--> XD Card Command Latch
 MDIO19--> XD Card Address Latch

GBRST# POWER SEQ
 $+3V \Rightarrow$ (GBRST#/CB_HWSUSP#) \Rightarrow PCIRST#

H/W SUSPEND# POWER SEQ :
 SUSPEND : CB_HWSUSP# LO \Rightarrow PCIRST# LO \Rightarrow +3VS
 RESUME : +3VS ON \Rightarrow PCIRST# HI \Rightarrow CB_HWSUSP# H

U46A
 NC2
 NC3
 NC4
 NC5
 NC6
 NC7
 NC8

CADR25	J18	AD19/A25	30
CADR24	J15	AD17/A24	30
CADR23	K16	CFRAME#/A23	30
CADR22	L16	CTRDY#/A22	30
CADR21	L18	CDEVSEL#/A21	30
CADR20	M16	CSTOP#/A20	30
CADR19	N19	CBLOCK#/A19	30
CADR18	N16	RFU/A18	30
CADR17	P16	AD16/A17	30
CADR16	L19		
CADR15	K15	CIRDY#/A15	30
CADR14	N18	CPERR#/A14	30
CADR13	K18	CPAR/A13	30
CADR12	R18	CBE2#/A12	30
CADR11	L18	AD12/A11	30
CADR10	U19	AD9/A10	30
CADR9	R19	AD14/A9	30
CADR8	P15	AD18/A8	30
CADR7	H16	AD20/A6	30
CADR6	H18	AD21/A5	30
CADR5	G15	AD22/A4	30
CADR4	G18	AD23/A3	30
CADR3	F15	AD24/A2	30
CADR2	F18	AD25/A1	30
CADR1	F16	AD26/A0	30
CDATA15	U18	AD8/D15	30
CDATA14	W18	RFU/D14	30
CDATA13	V17	AD6/D13	30
CDATA12	V16	AD4/D12	30
CDATA11	B19	AD2/D11	30
CDATA10	C18	AD3/D10	30
CDATA9	D18	AD30/D9	30
CDATA8	D18	AD2/D8	30
CDATA7	W17	AD7/D7	30
CDATA6	W16	AD5/D6	30
CDATA5	T15	AD3/D5	30
CDATA4	R14	AD1/D4	30
CDATA3	C19	AD0/D3	30
CDATA2	C19	RFU/D2	30
CDATA1	D19	AD29/D1	30
CDATA0	E19	AD27/D0	30

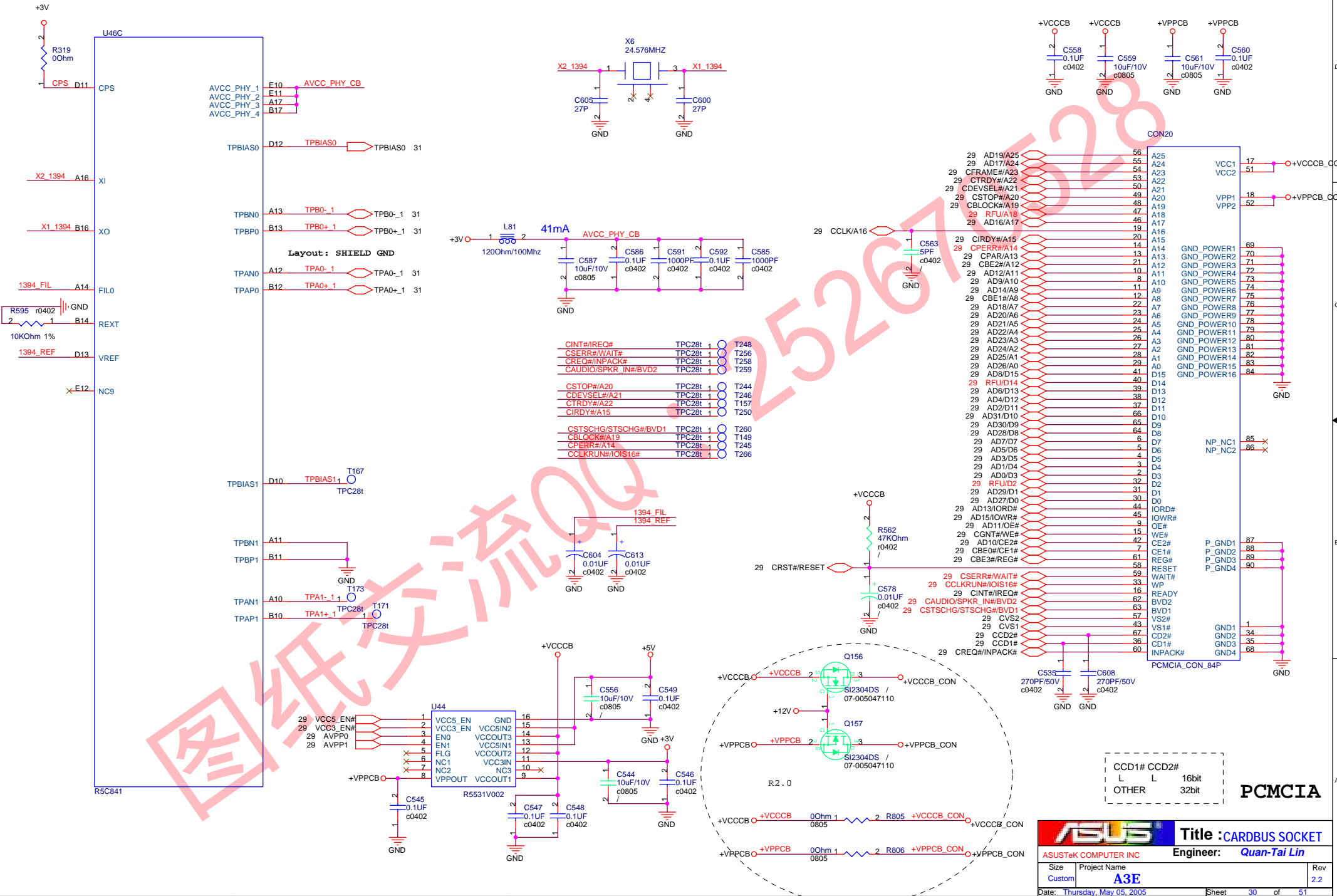
OE#	T19	AD11/OE#	30
WE#	M15	CGNT#/WE#	30
CE2#	T18	AD10/CE2#	30
CE1#	V19	CBE#/CE1#	30
REG#	F16	CBE#/REG#	30
RESET	H19		
WAIT#	G16	CSERR#/WAIT#	30
WP#/IOIS16#	M18	CCLKRUN#/IOIS16#	30
RDY#/IREQ#	M18		
BVD2	E19	CAUDIO/SPKR IN#/BVD2	30
BVD1	E18	CSTSCHG/STSCHG#/BVD1	30
VS2#	R16	CVS2	30
VS1#	H16	CVS1	30
D15	D15	CCD1#	30
CD2#	T14	CCD2#	30
CD1#	G19	CCD1#	30
INPACK#	G19	CREQ#/INPACK#	30
IORD#	P18	AD13/IORD#	30
IOWR#	P19	AD15/IOWR#	30
USBDP	V14		
USBDM	W14		
VPPEN1	W13	AVPP1	30
VPPEN0	V13	AVPP0	30
VCC3EN#	T13	VCC3_EN#	30
VCC5EN#	R13	VCC5_EN#	30

ASUS Title : RICOH R5C841

Engineer: Quan-Tai Lin

Project Name: A3E

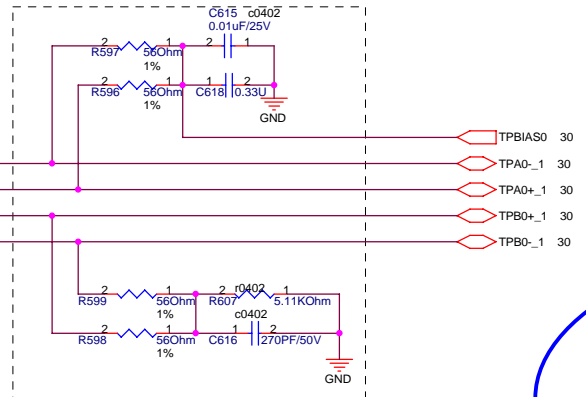
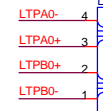
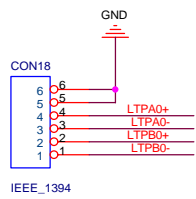
Date: Thursday, May 05, 2005 Sheet 29 of 51



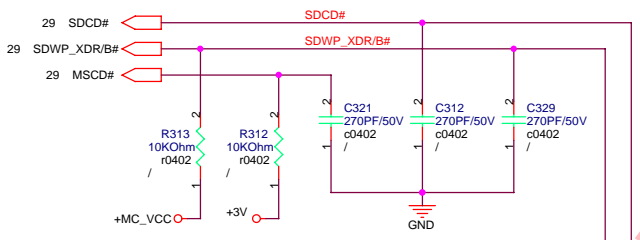
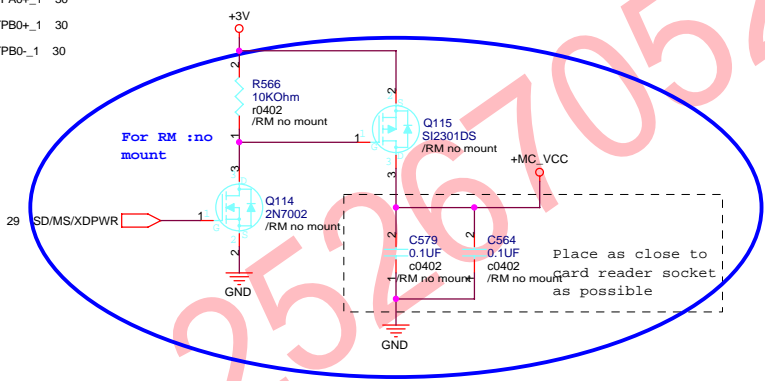
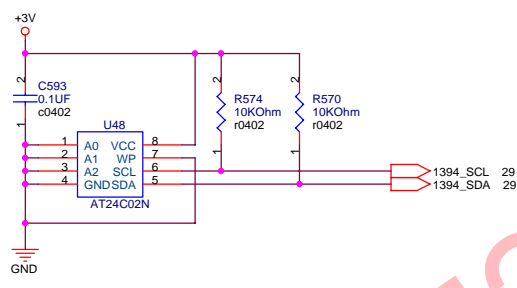
CCD1#	CCD2#	16bit
L	L	
OTHER		

PCMCIA

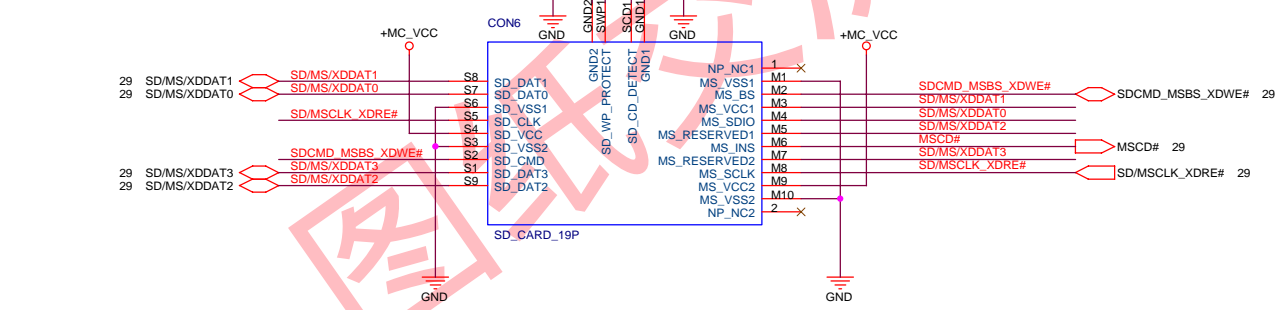
ASUS Title : **CARDBUS SOCKET**
 ASUSTek COMPUTER INC Engineer: **Quan-Tai Lin**
 Size Project Name
 Custom **A3E**
 Date: Thursday, May 05, 2005 Sheet 30 of 51

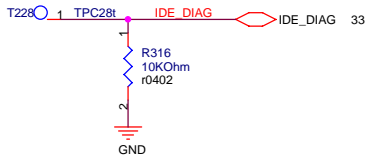


1. CLOSE TO R5C841
2. The area is as compact as possible, length < 10 mm
3. TPA Pair and TPB pair mismatch < 2.5mm
4. No via recommend , maxmium is one.
5. Total length < 50 mm
6. Differential impedance is 110+/- 6 ohm
7. TPA Pair trace or TPB pair trace mismatch < 1.25mm

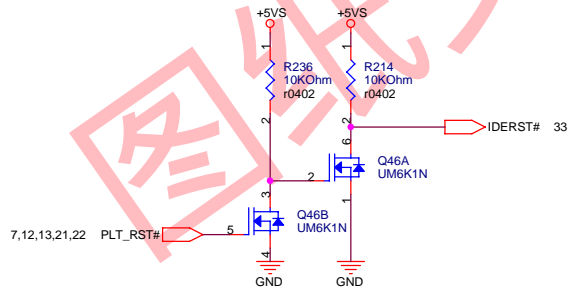
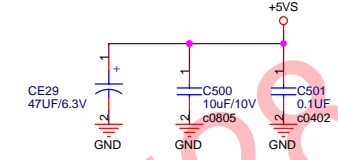
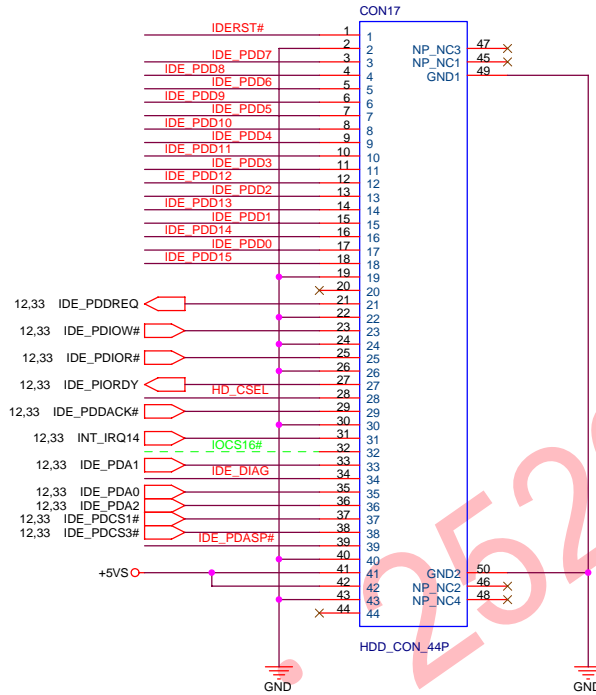
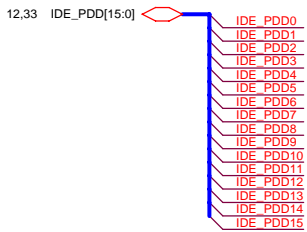
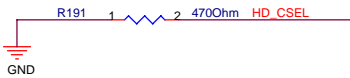


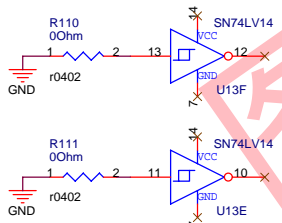
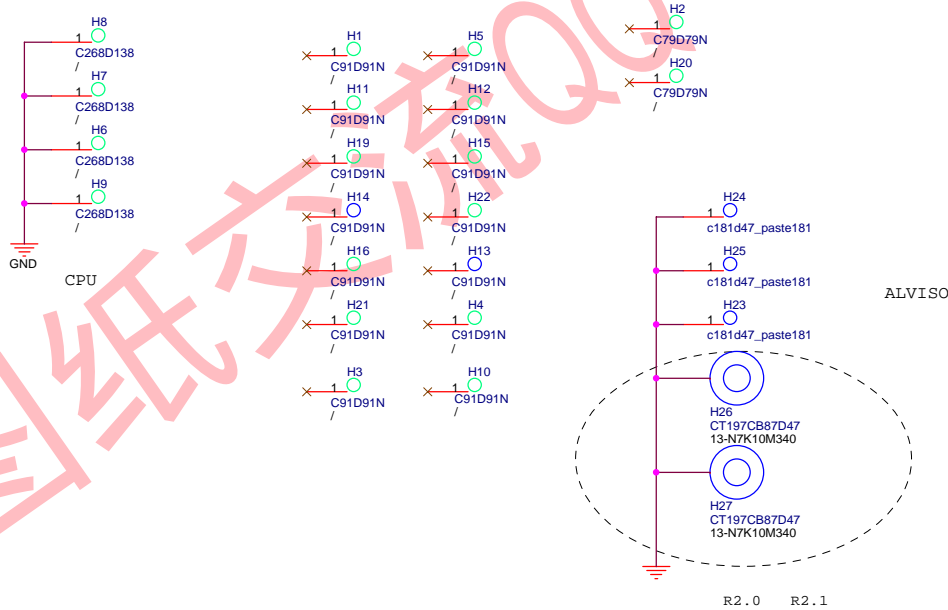
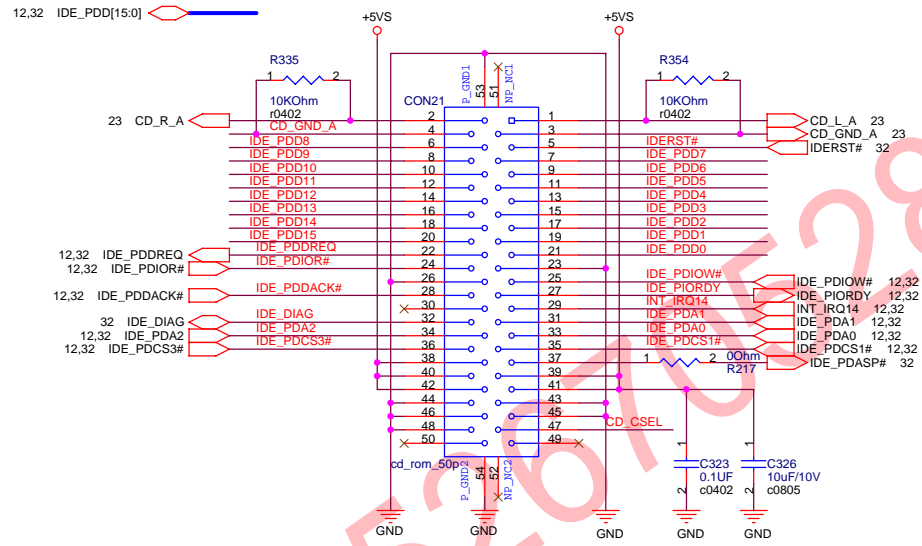
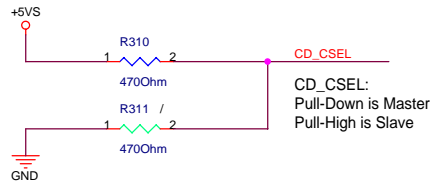
Layout: SHIELD GND





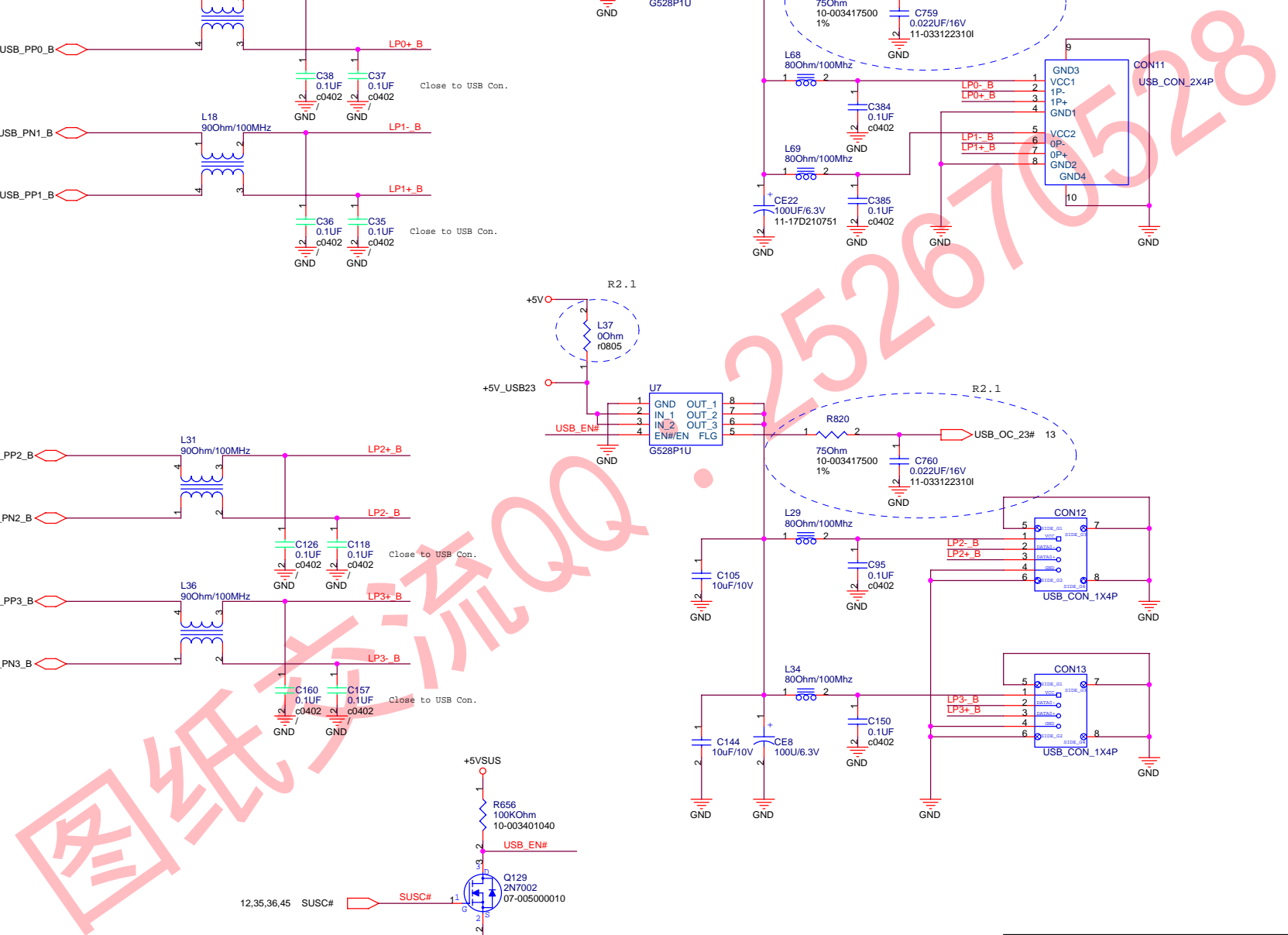
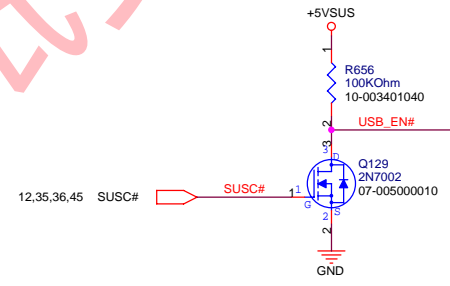
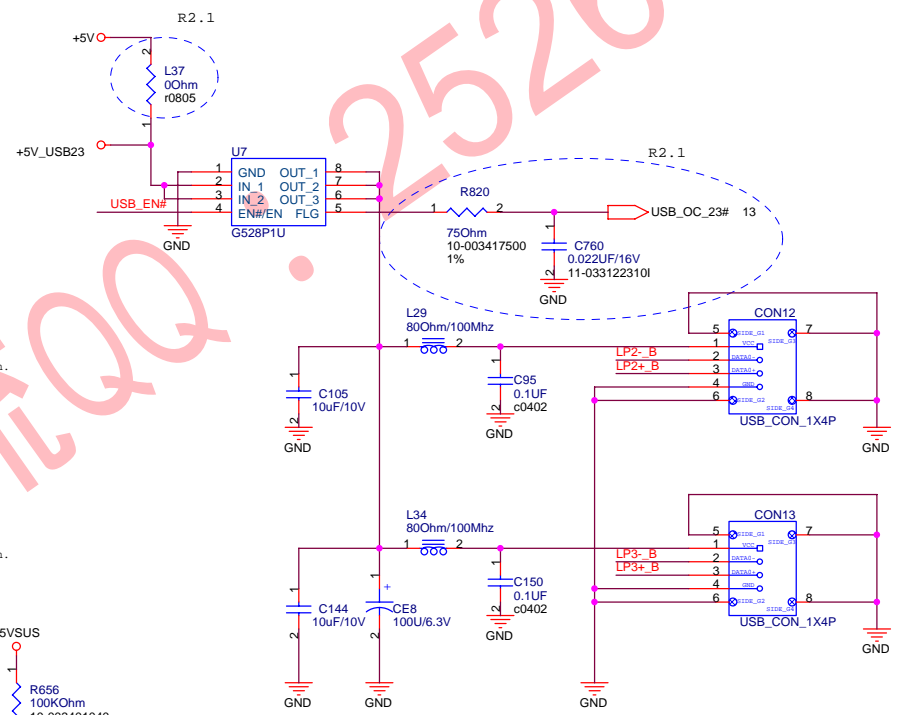
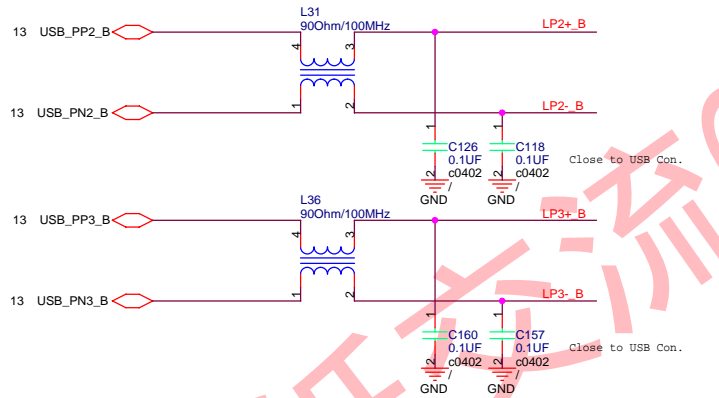
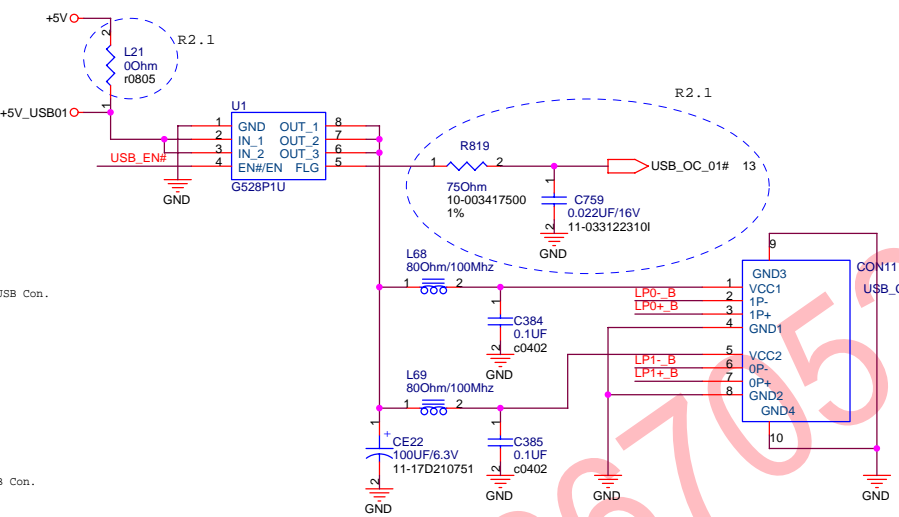
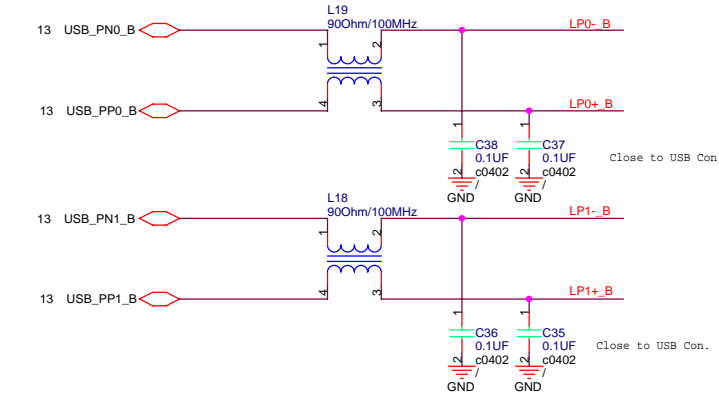
HD_CSEL : Pull-Down, HDD as Master



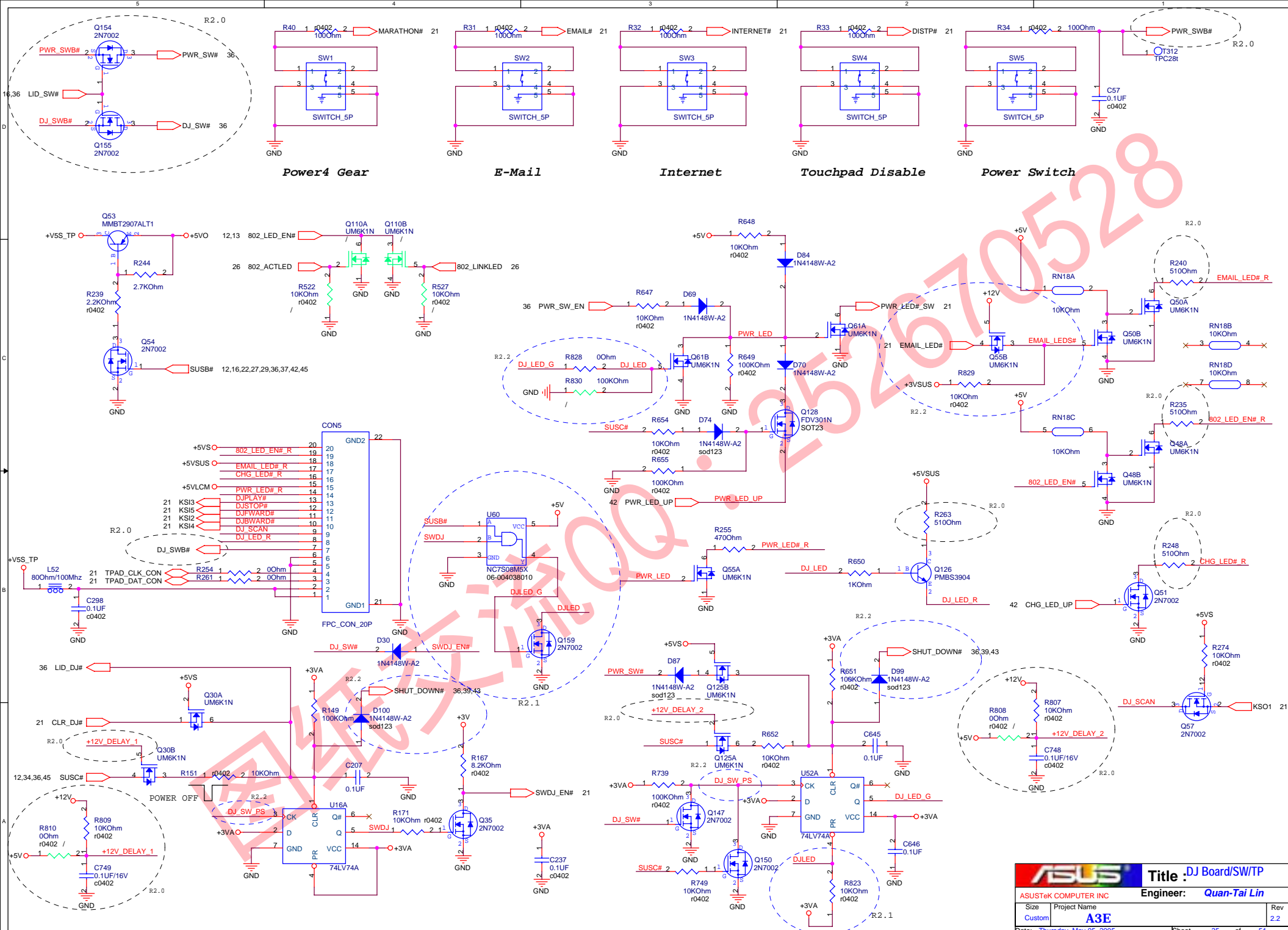


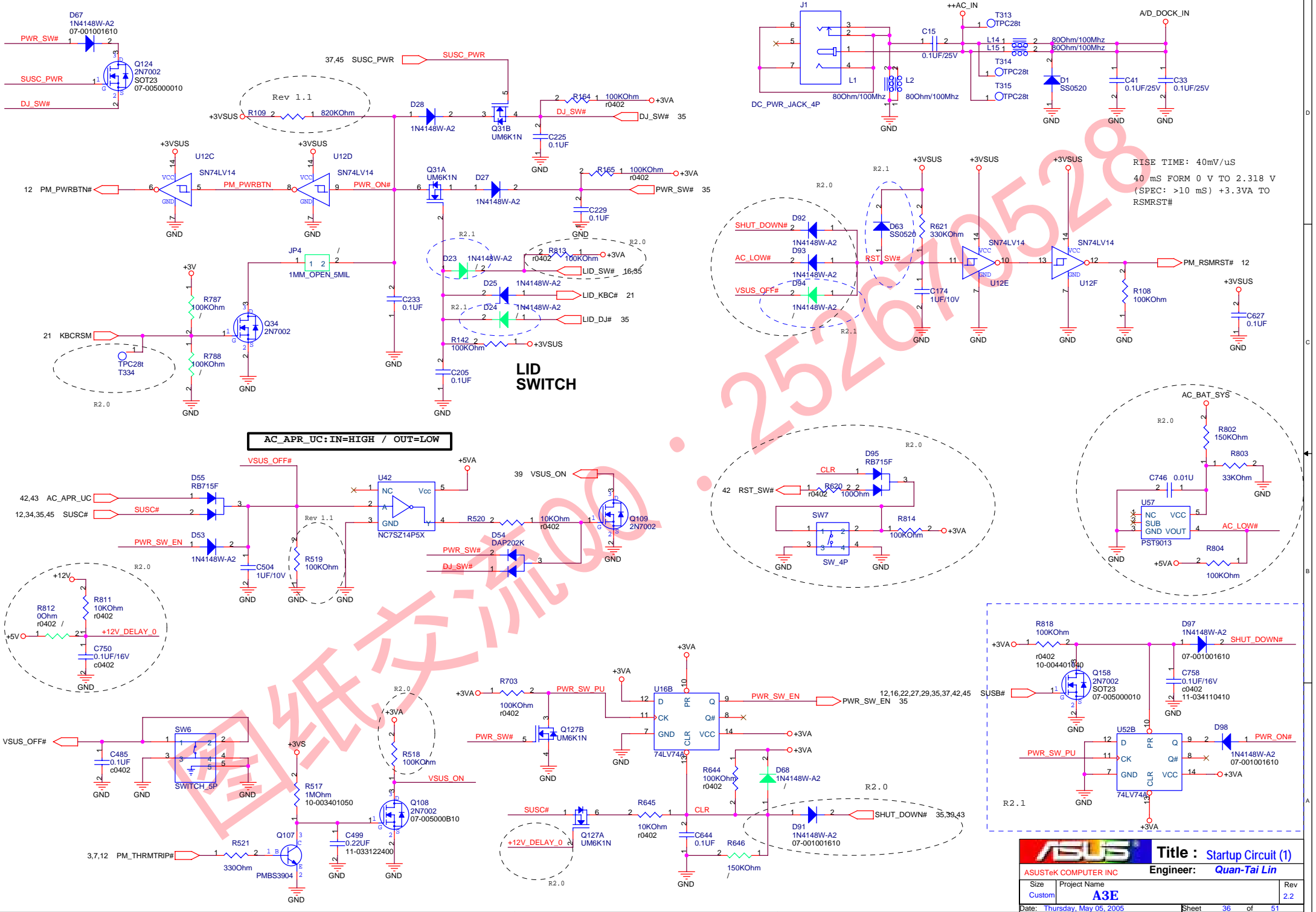
ASUS		Title : CDROM	
ASUSTek COMPUTER INC		Engineer: Quan-Tai Lin	
Size	Project Name	Rev	
Custom	A3E	2.2	
Date: Thursday, May 05, 2005		Sheet	33 of 51

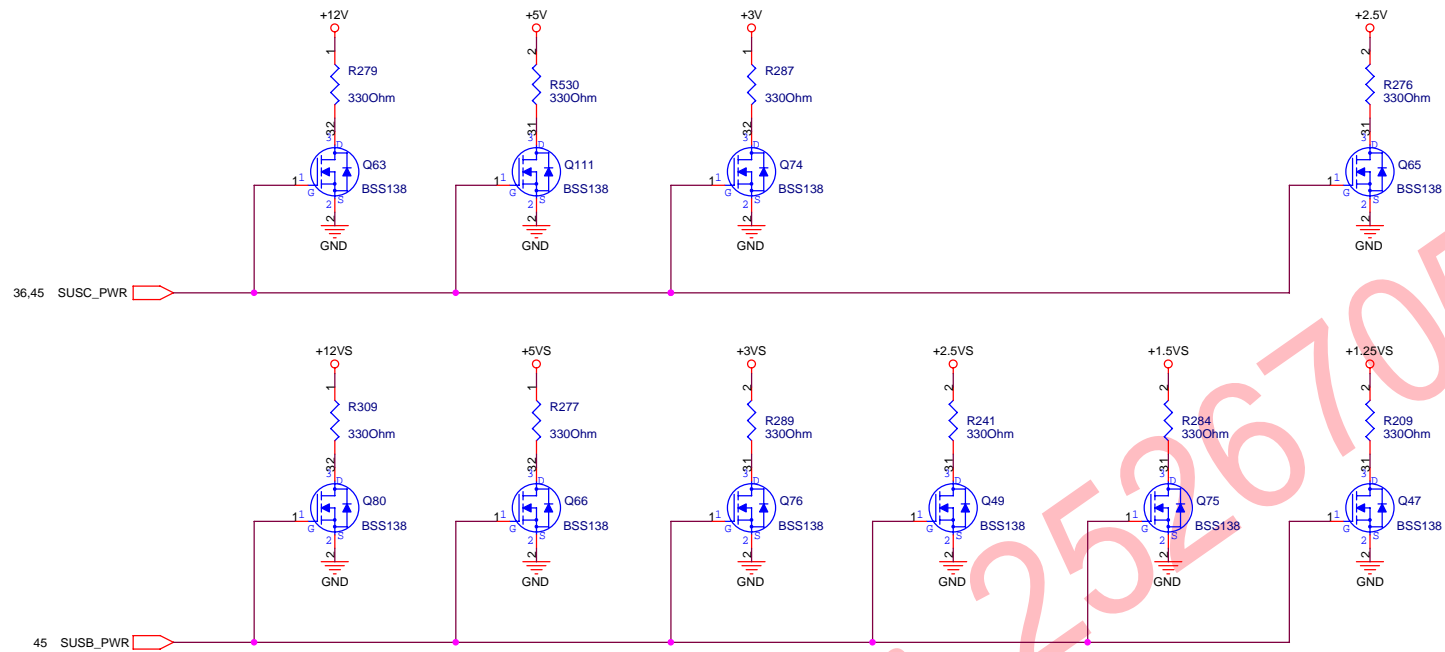
USB



ASUS		Title : USB CONN	
ASUSTek COMPUTER INC		Engineer: Quan-Tai Lin	
Size	Project Name	Rev	
Custom	A3E	2.2	
Date: Thursday, May 05, 2005	Sheet	34	of 51

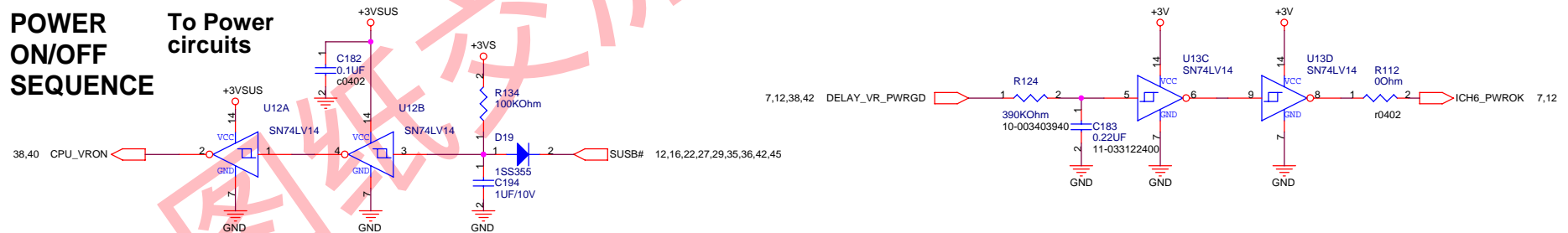


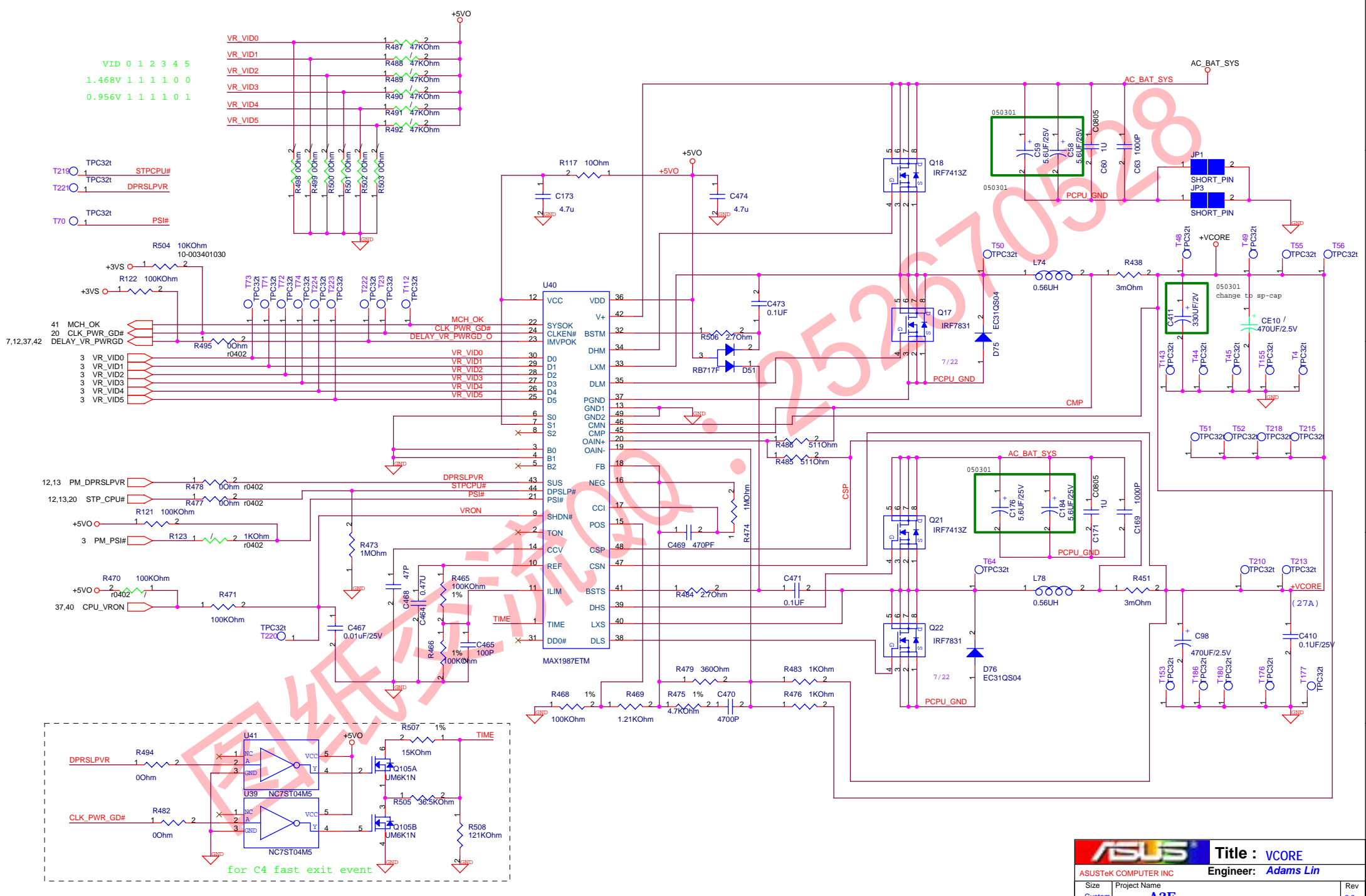




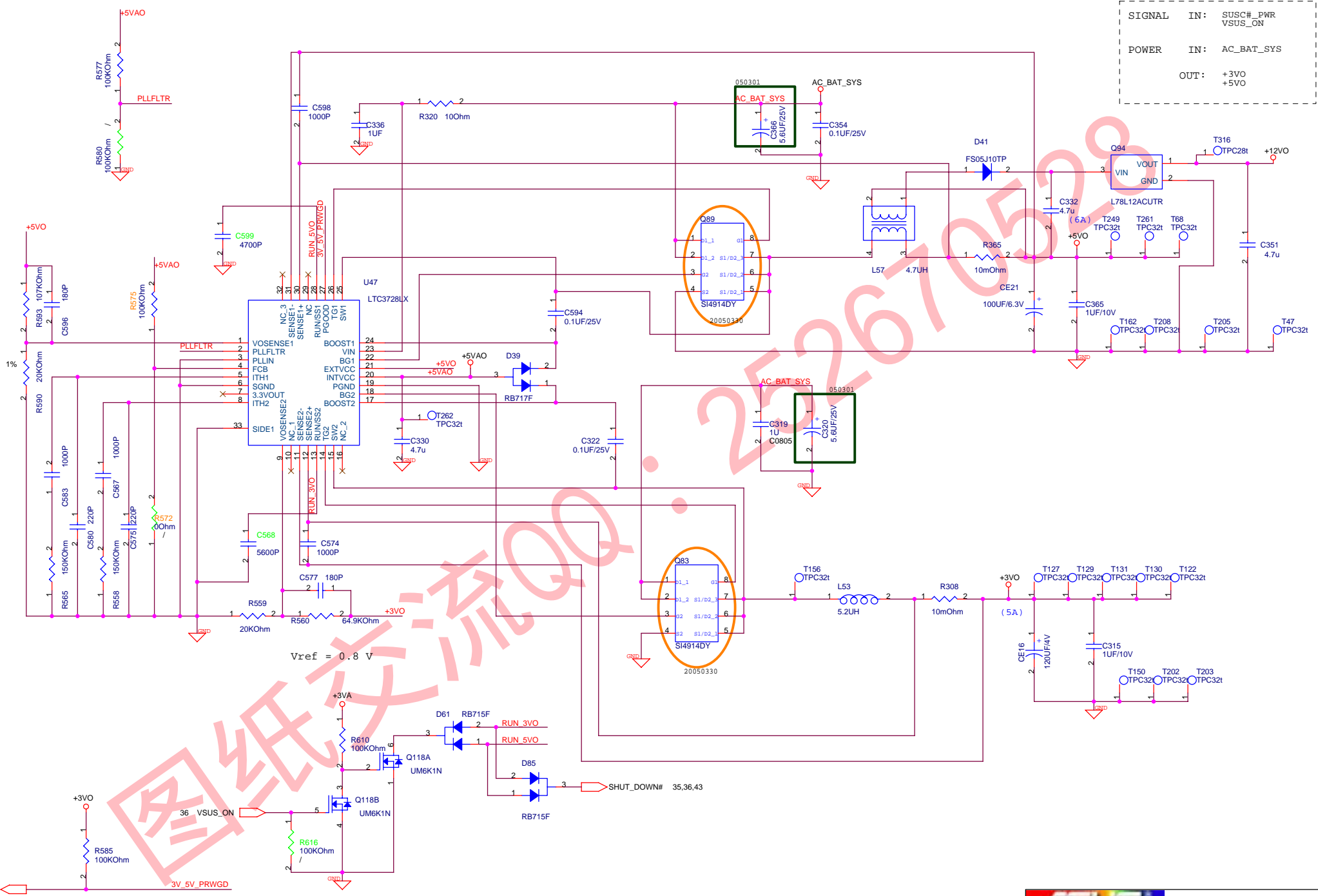
POWER ON/OFF SEQUENCE

To Power circuits

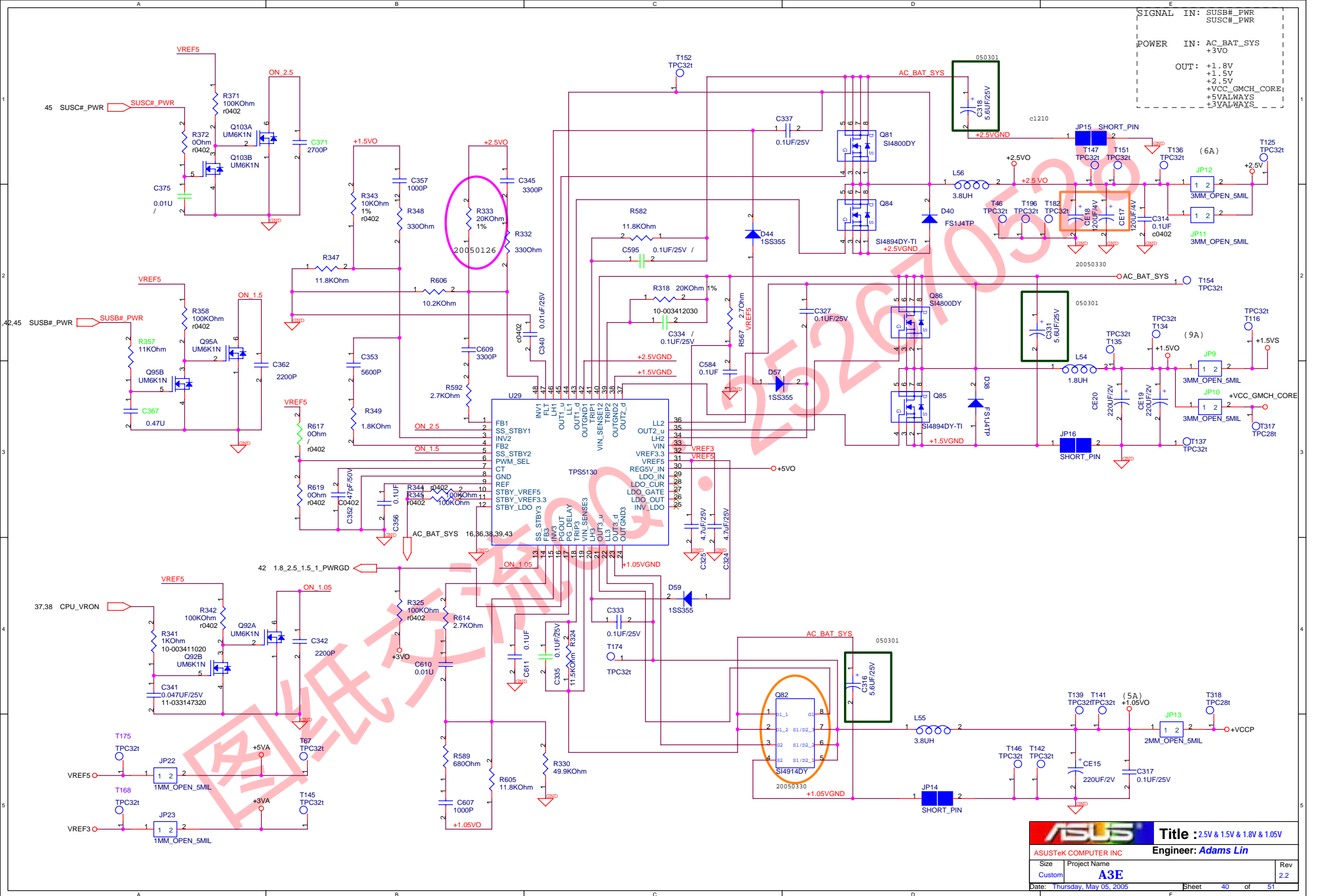




SIGNAL	IN:	SUSC#_PWR
		VSUS_ON
POWER	IN:	AC_BAT_SYS
	OUT:	+3VO
		+5VO



Vref = 0.8 V



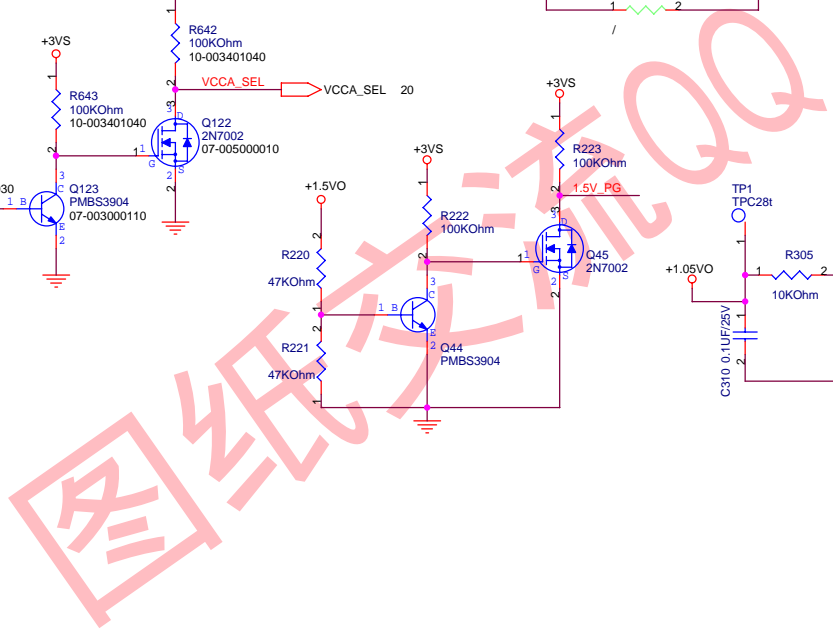
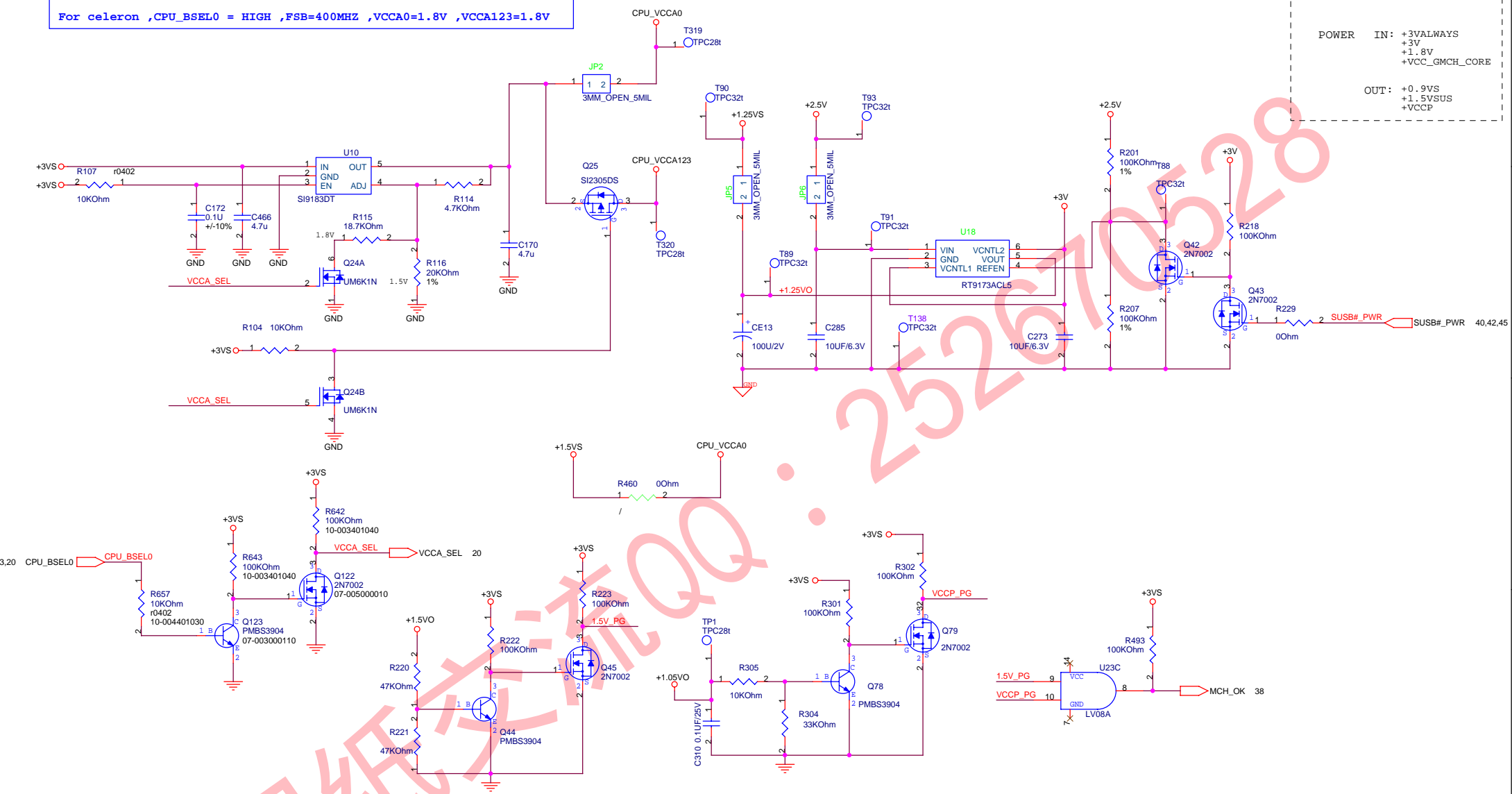
SIGNAL IN: SUSB#_PWR
 SUSC#_PWR

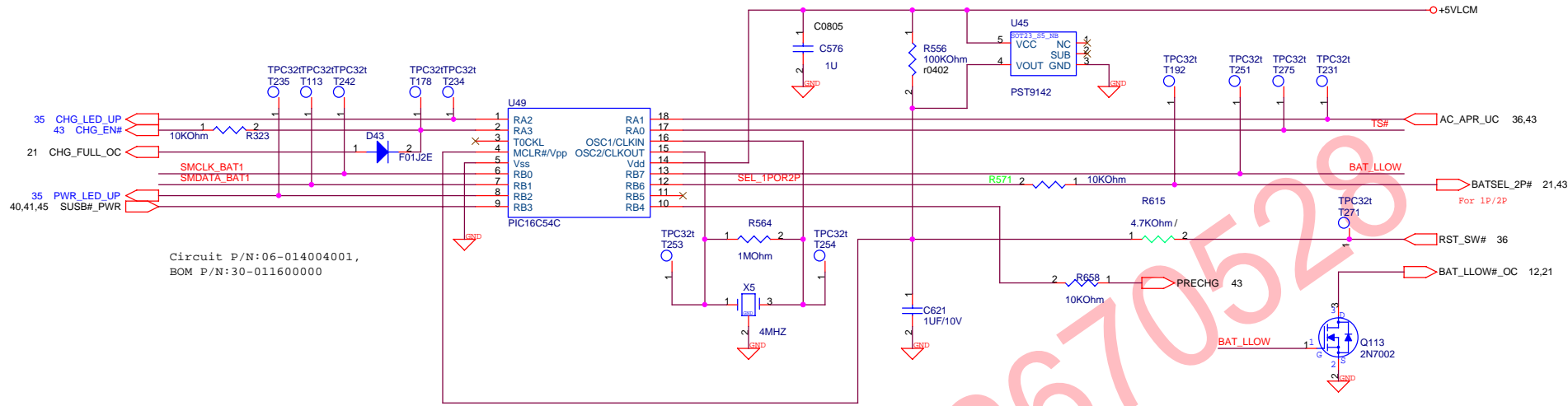
POWER IN: AC_BAT_SYS
 +3VO

OUT: +1.8V
 +1.5V
 +2.5V
 +VCC_GMCH_CORE
 +5VALWAYS
 +3VALWAYS

For Duthon ,CPU_BSEL0 = LOW ,FSB=533MHZ ,VCCA0=1.5V ,VCCA123=0V
 For celeron ,CPU_BSEL0 = HIGH ,FSB=400MHZ ,VCCA0=1.8V ,VCCA123=1.8V

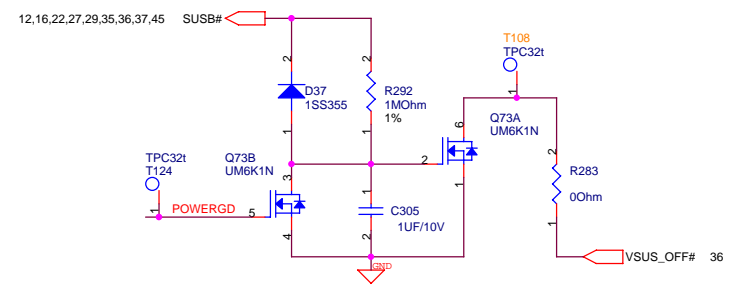
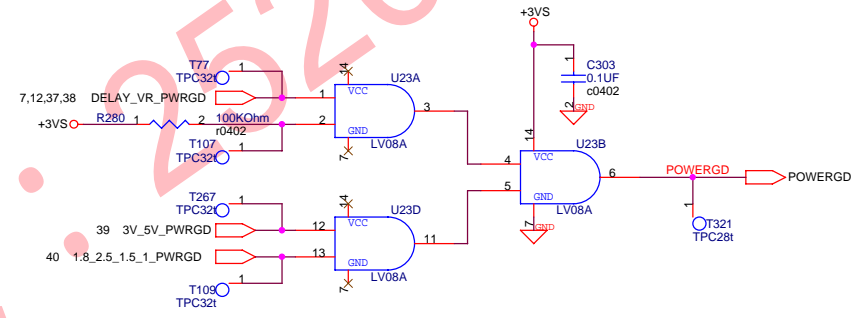
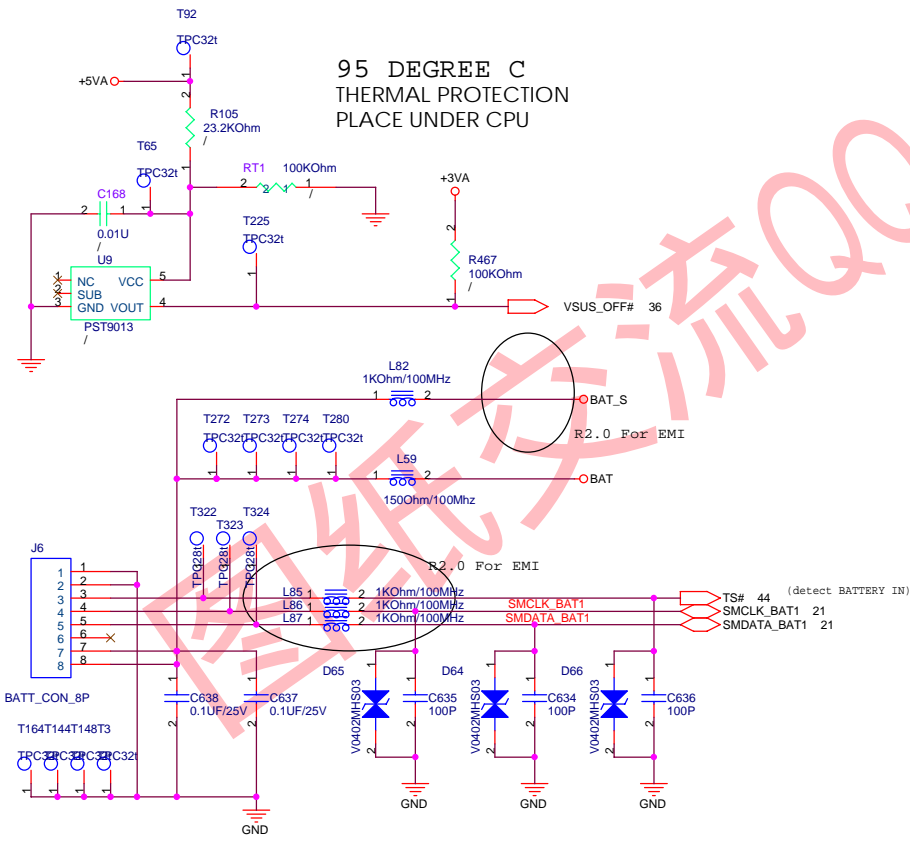
SIGNAL IN: SUSB#_PWR
 CPU_VRON
 POWER IN: +3VALWAYS
 +3V
 +1.8V
 +VCC_GMCH_CORE
 OUT: +0.9VS
 +1.5VSUS
 +VCCP

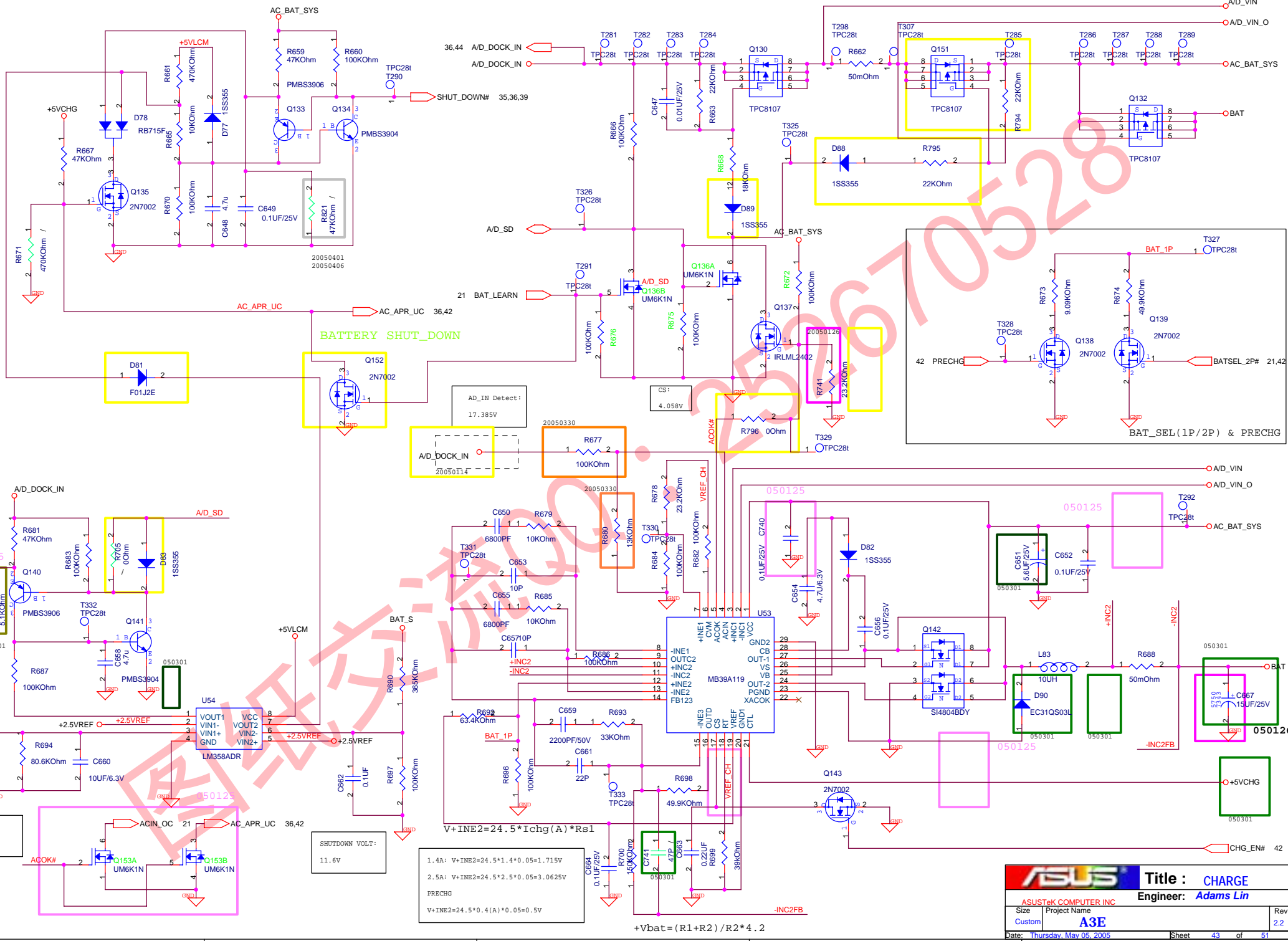




Circuit P/N:06-014004001,
BOM P/N:30-011600000

95 DEGREE C
THERMAL PROTECTION
PLACE UNDER CPU





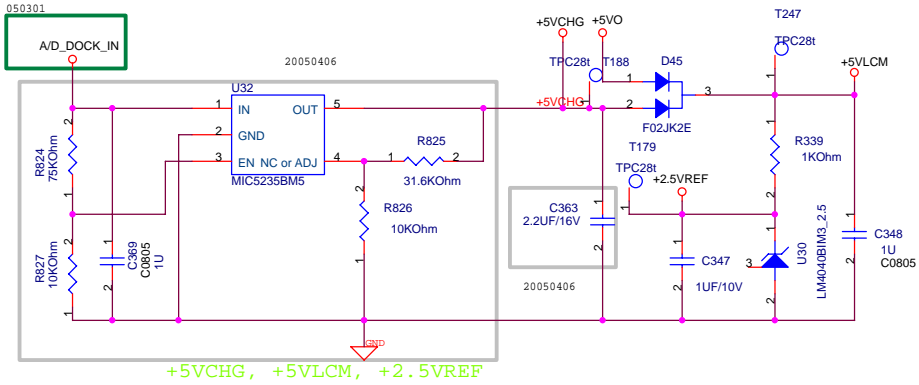
OVP VOLT: 17.146V

SHUTDOWN VOLT: 11.6V

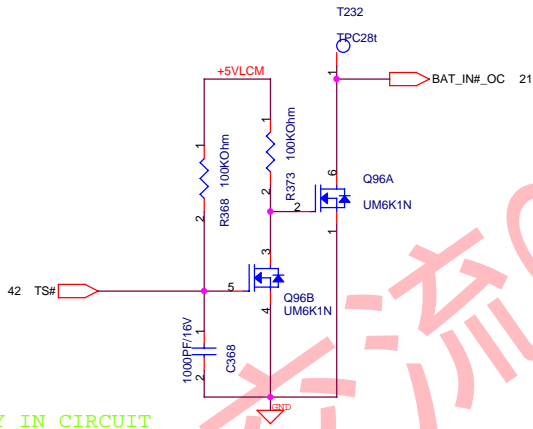
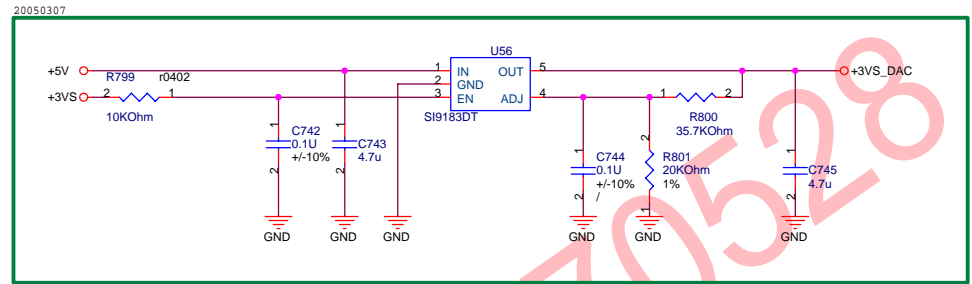
$V+INE2=24.5 * 1.4 * 0.05 = 1.715V$
 $PRECHG$
 $V+INE2=24.5 * 0.4(A) * 0.05 = 0.5V$

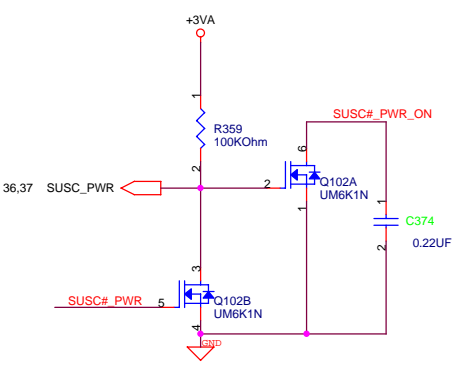
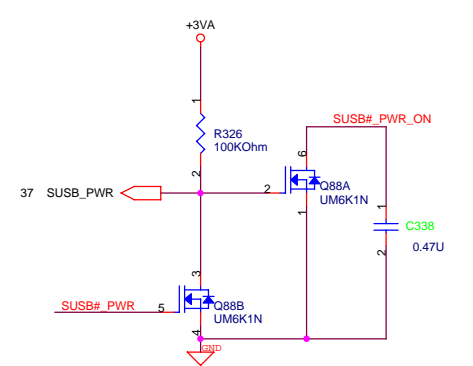
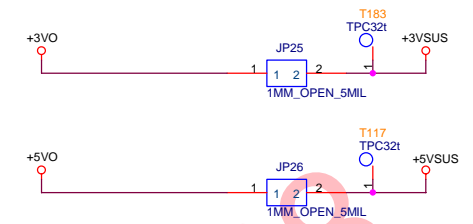
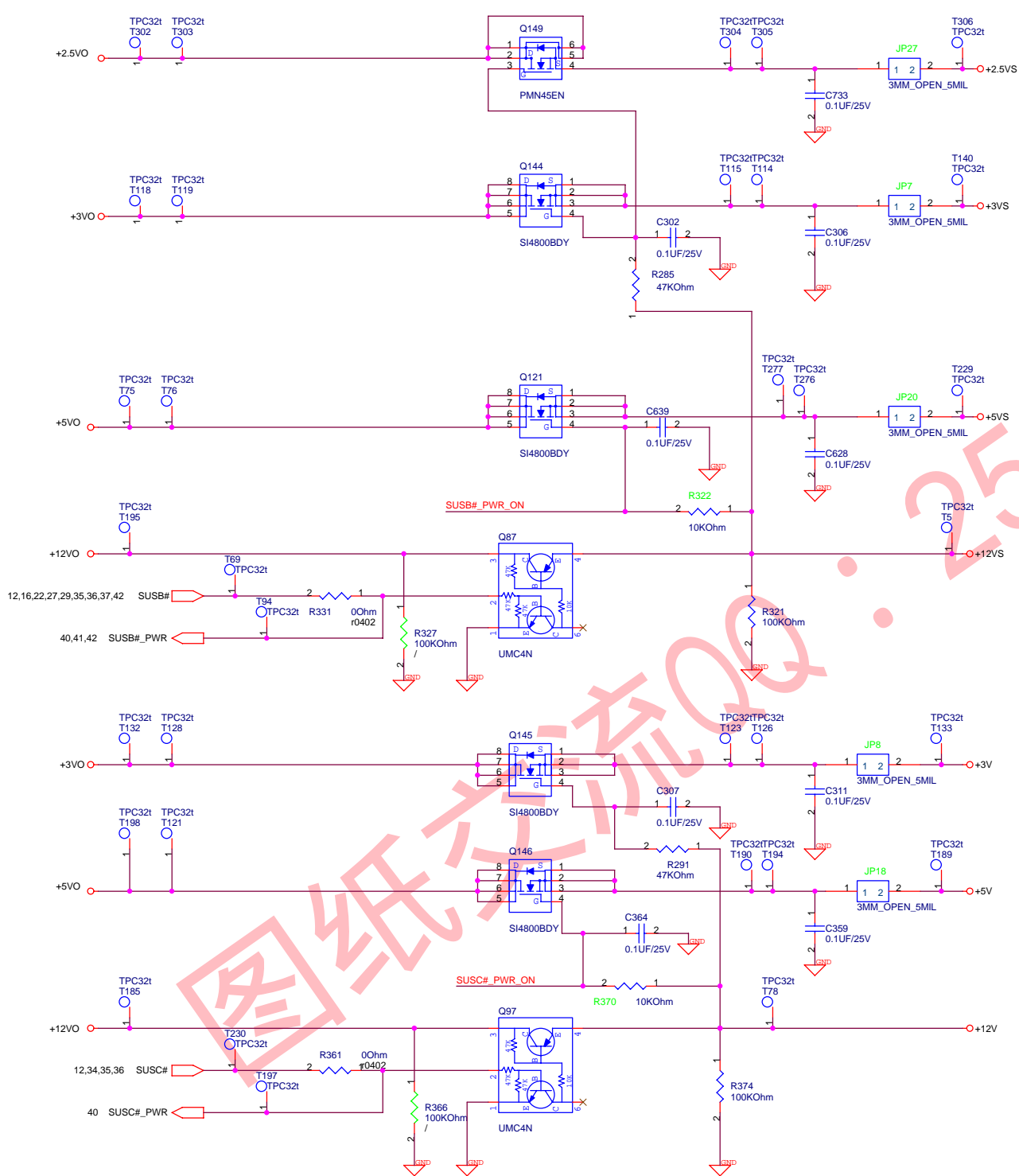
$+Vbat = (R1+R2) / R2 * 4.2$

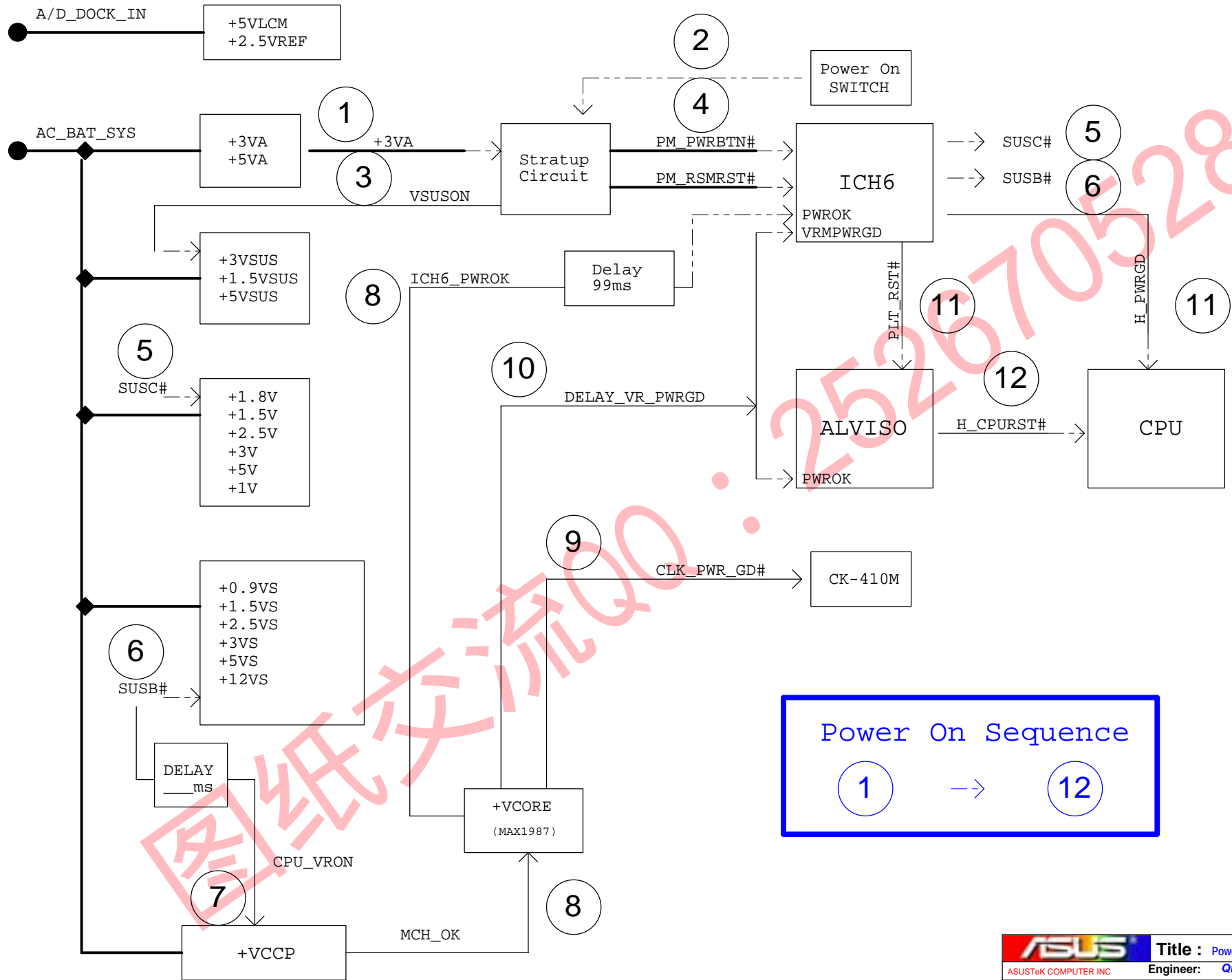
ASUS		Title : CHARGE	
ASUSTeK COMPUTER INC		Engineer: Adams Lin	
Size Custom		Project Name	
A3E		Rev 2.2	
Date: Thursday, May 05, 2005		Sheet 43 of 51	



Ref: 1.24V
ON: EN>2V
OFF: EN<0.6V

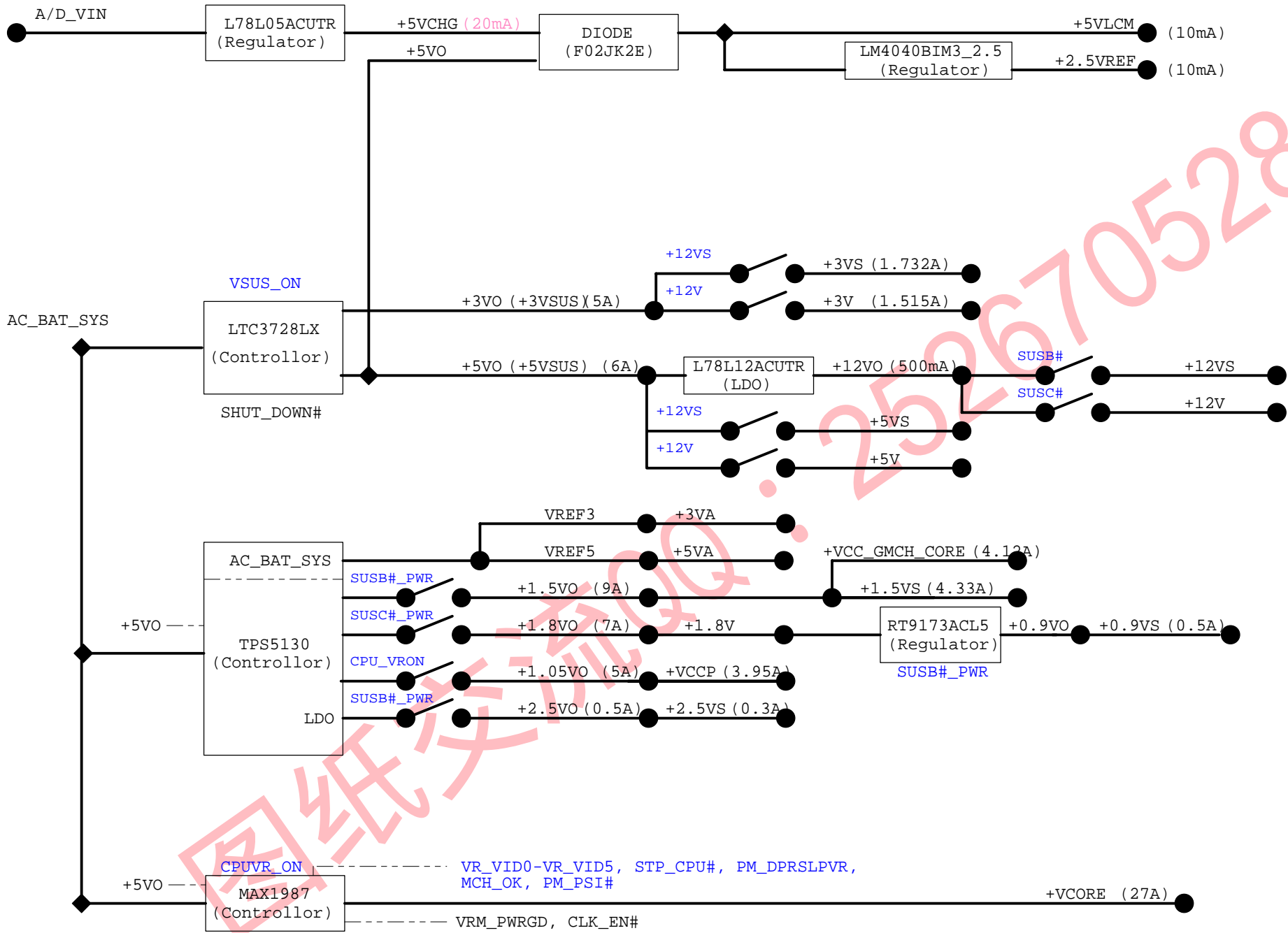






Power On Sequence

① → ⑫



PCI Device	IDSEL#	REQ/GNT#	Interrupts
10/100 RTL8100CL	AD16	2	E
CARD READER	AD17	1	B
CARDBUS	AD17	1	C
1394	AD17	1	D
MINIPCI (802.11a/b/g)	AD19	3	G,H

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	0101110x (5C)
PIC	1001001x (92)

ICH6-M GPIO	A5V	Note	Volt
GPI 0			+3VS
GPI 1			+3VS
GPI 2			+3VS
GPI 3			+3VS
GPI 4			+3VS
GPI 5			+3VS
GPI 7			+3VS
GPI 8	EXTSMI#		+3VSUS
GPI 11	LID_ICH#		+3VSUS
GPI 12	KB_SCI#		+3VSUS
GPI 13	SIO_SMI#		+3VSUS
GPI 14			+3VSUS
GPI 15			+3VSUS
GPO 16			
GPO 17			
GPO 19	PWRLED_1HZ		+3VS
GPO 21	BACK_OFF#		+3VS
GPO 23	FWH_WP#		+3VS
GPO 24	802_LED_EN#		+3VSUS
GPI 26	SATA_DET#0	Unused pull-up to Vcc3_3	+3VS
GPI 27			+3VSUS
GPI 28			+3VSUS
GPI 29	PCB_ID2	Default : 0	+3VS
GPI 30	PCB_ID0	Default : 0	+3VS
GPI 31	PCB_ID1	Default : 0	+3VS
GPI 33	CPUFAN_SPD_A		+3VS
GPO 34	WLAN_ON#		+3VS
GPI 40	PANEL_ID0		+3VS
GPI 41	PANEL_ID1		+3VS
GPO 48			
GPO 49			
GPIO 25	CB_SD#	Diode	+3V

KBC GPIO	A5V	Note
P23(Pin 35)	CHG_FULL_OC	
P22(Pin 36)	BAT_LEARN	
P21(Pin 37)	KBC_P21	
P20(Pin 38)	KBCRSM	
P42(Pin 23)	WATCHDOG	
P43(Pin 22)	OP_SD#	POSTCode前拉Low,ACPI前拉High,ACPI後放掉
P44(Pin 21)	KB_CPURST	
P45(Pin 20)	KB_GATEA20	
P46(Pin 19)	KBCSCI	
P47(Pin 18)	PM_CLKRUN#	
P50(Pin 17)	BAT_LLOW#_OC	
P51(Pin 16)	KID1	
P52(Pin 15)	KID2	
P53(Pin 14)	CLR_DJ#	
P54(Pin 13)	BAT_SEL#	
P55(Pin 12)	BAT1_IN#_OC	
P56(Pin 11)	FAN_DA1	
P57(Pin 10)	ADJ_BL	
P67(Pin 74)	DJ_LED#	
P66(Pin 75)	SWDJ_EN#	
P65(Pin 76)	GAIN_AMP_K#	0->-6 V/V 1->NORMAL
P64(Pin 77)	ACIN_OC	
P63(Pin 78)	DISTP#	
P62(Pin 79)	MARATHON#	
P61(Pin 80)	INTERNET#	
P60(Pin 1)	EMAIL#	
P75(Pin 4)	KB_CLK	
P74(Pin 5)	MS_CLK	
P73(Pin 6)	TPAD_CLK	
P72(Pin 7)	KB_DAT	
P71(Pin 8)	MS_DAT	
P70(Pin 9)	TPAD_DAT	
P77(Pin 2)	SMC_BAT	
P76(Pin 3)	SMD_BAT	
P27(Pin 31)	SCROLL_LED#	
P26(Pin 32)	NUM_LED#	
P25(Pin 33)	CAP_LED#	
P24(Pin 34)	SET_PLTRSTNS#	
P40(Pin 27)	EXT_SMI	
P41(Pin 26)	EMAIL_LED#	

Rev.	Data	Description
1.0	05'01/06	Initial release
2005/01/21-1140		R735.R736.R750.R752 footprint change to 0603
		JP28 for CMOS clear renames to JRST1 and no mount U19.77 signal changes to ACIN_OC and R245 still mount R73.R75.R76.R77 value change to 470ohm and R41 is 330ohm R519 value changes to 100Kohm
2005/01/24-1035		Add SW8 ,R797 but no mount
2005/01/26-0945		R109 value changes to 820Kohm D72 mount
2005/02/01-1300		R735.R736.R750.R752 tolerance change to 1%
2005/02/21-1300		Add test point :T309(+Vcc_RTC).T310(+RTCBAT).T311(R545.2). T312(PWR_SW#).T313.T314.T315(++AC_IN)
2005/03/01-1130		Add R798 to connect signal MIC_IN_R and MIC_IN_L R163. L43 no mount Add Q154 .Q155 to let LID_SW# to control PWR_SWB# and DJ_SWB# to be on or off Add D91 to connect to SHUT_DOWN# signal
2005/03/04-1600		U19.13 exchange to U19.35 (BAT_SEL# exchange to CHG_FULL_OC) GPIO29=PCB_ID0,GPIO30=PCB_ID1,GPIO31=PCB_ID2 PCB_ID0=1,PCB_ID1=0,PCB_ID2=0
2005/03/07-1500		R518 change to 100Kohm to prevent from +3VA sinking too much current Change CE10 to power and change CE9 to 470UF/2.5V L27.2 and L22.2 change to +3VS_DAC
2005/03/08-0950		Add D92.D93.D94,U57,C746,R802.R803.R804 to prevent from abnormal shut down in startup circuit Change R41 value to 470ohm,R77.R75.R76.R73.R240.R235.R248.R263 to 510ohm Change R184 to 100Kohm and add C747 1uF/10V Add T334 to R788.1 for KBCRSM signal
2005/03/10-1128		Colay Q156, R805and Q157,R806 for keep from PCMCIA device current leakage Q125,Q30,Q127 turn on voltage change to a RC delay +12V Add R811.C750.R812 for +12V_DELAY_0 signal Add R809.C749.R810 for +12V_DELAY_1 signal Add R807.C748.R808 for +12V_DELAY_2 signal
2005/03/11-1120		Add C751.C752 for EMI(P.28) Add C754.C755 100PF for EMI(P.16) Add C753 100PF. R815 0ohm for EMI(P.16) Add U58.U59 for EMI(P.4) Add R813 to pull up LID_SW# to +3VA Add D95.R814 to make RESET button (SW7) function to be ok
2005/03/14-1040		Delete T53.T207.T217.T214.T211.T212.T209.T216 Add C756.C757 47UF/6.3V 1206 to +2.5VS on page 9 Add D96.RP5.RP6.R816 and pull to +5VS for LPT C751.C752 footprint change to 1812_h71 Add H26.H27
2005/03/15-2050		Add R817 10Kohm to pull high to +3VS on page 5

Rev.	Data	Description
2005/03/16-1600		R178.R198 value change to 3.9Kohm 1% C630.C631.C632.C633 still mount C751.C752 still mount R625.R632.R633.R634 change to 120ohm/100MHZ bead R175.R199 still mount L50.R150 change to 1Kohm/100MHZ bead L6.L7.L8 change to 60ohm /100MHZ bead R162 change value to 4.7Kohm 1% CE9 change to 470UF/2.5V
Rev 2.1		
2005/03/29-1710		Add D63 back and D94 is no mount
2005/04/01-1228		Add U52B,D98,D97,R818,C758,Q158 for start up circuit D23.D24 no mount Add R819.C759 between U1.5 (FLG) and USB_OC_01# Add R820.C760 between U7.5 (FLG) and USB_OC_23# C751.C752 footprint changes to C1808 inverter_h79
2005/04/06		L21.L37 change to 0ohm resistance (0805) Add U60.R822.R823.Q159 for LED signal

Rev.	Data	Description
For RM:		
2005/01/24-1035		Page 31 no mount : R566,Q114,Q115,C579,C564 Page 20 no mount : R54,R43,Q16,Q19,R412 Page 41 no mount : R657,R643,Q122,Q123 Mount SW8 ,R797 Add SWITCH TABLE for CPU frequency select

Rev.	Data	Description

图纸交流QQ : 252670528

Rev.	Data	Description
1.0	05'01/06	Initial release
2005/01/21-1200		Add 22Kohm R794.R795 , P-MOS Q151 , diode D88.D89
2005/01/21-1200		Add capacitor C739,resistor R796,N-MOS Q152,diode D90
2005/01/21-1200		R677 value is from 110Kohm to 107Kohm and R677.1 connect to A/D_DOCK_IN
2005/01/21-1200		R680 value is from 14Kohm to 13.7Kohm and D81 changes to F01J2E
2005/01/21-1200		D83 mount and R705 no mount and R725 mount
2005/01/26-0945		R333 value changes to 20Kohm
2005/01/26-0945		Add Q153 for ACIN_OC and AC_APR_UC signals and delete D90
2005/01/26-0945		Change U53.18 and U53.19 for signal VREF_CH
2005/01/26-0945		Delete JP24 and add a cap C740 0.1UF
2005/01/26-0945		C725 still mount and R706 no mount
2005/01/26-0945		R741 value changes to 23.2K ohm
2005/01/26-1250		C666 changes to connect to L83.2
2005/01/28-1200		C666 no mount
2005/02/21-1300		Add test point : T316(+12VO).T317(+VCC_GMCH_CORE).T318(+VCCP). T319(CPU_VCCA0).T320(CPU_VCCA123).T322(R631.1).T323(R630.1). T324(R629.1).T321(POWERGD).T329(R796.2).T326(A/D_SD).T325(D88.2). T332(C658.1).T330(R684.2).T333(C661.1).T327(BAT_1P).T331(C653.2). T328(PRECHG)
2005/03/01-1800		Change C59, C58, C176, C184, C366, C320, C318, C331, C316, C651 to POSCAP 5.6UF/25V Add D90 for Charger noise(P. 43) Remove C666, R705, R689 Change r706 to 5.1Kohm Change U53 Pin 21 connector to +5VCHG Change U32 Pin 1 connector to A/D_DOCK_IN Change C441 to 330UF/2V SP-CAP Change C98 to 470UF/2.5V POSCAP Add C741 47PF/50V with R700(P.43) Change C667 to 15UF/2.5V POSCAP
2005/03/30-1124		Change R677 to 100Kohm Change R680 to 13Kohm Change CE17,CE18 to 220UF/4V Mount R283 Change Q82, Q83, Q89 to SI4914
2005/04/01-1640		Change CE17,CE18 to 120UF/4V Add R821 47Kohm for boot issue

Rev.	Data	Description
2005/04/06-1524		Change U32 to MIC5235BM5 Add R824=75K, R827=10K, R825=31.6K, R826=10K Change C363 to 2.2UF/16V Change R821 to unmount