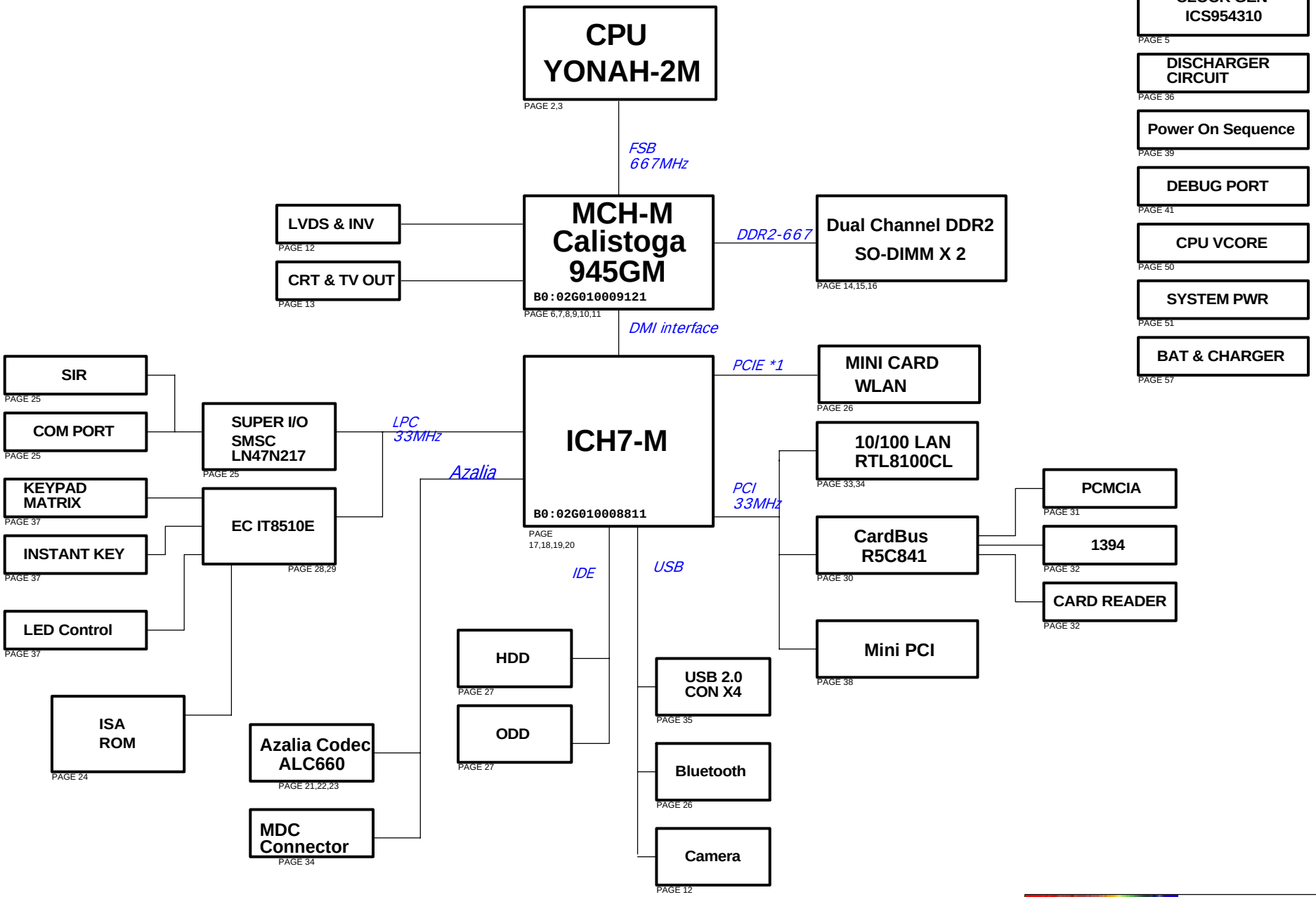
A3F Block Diagram



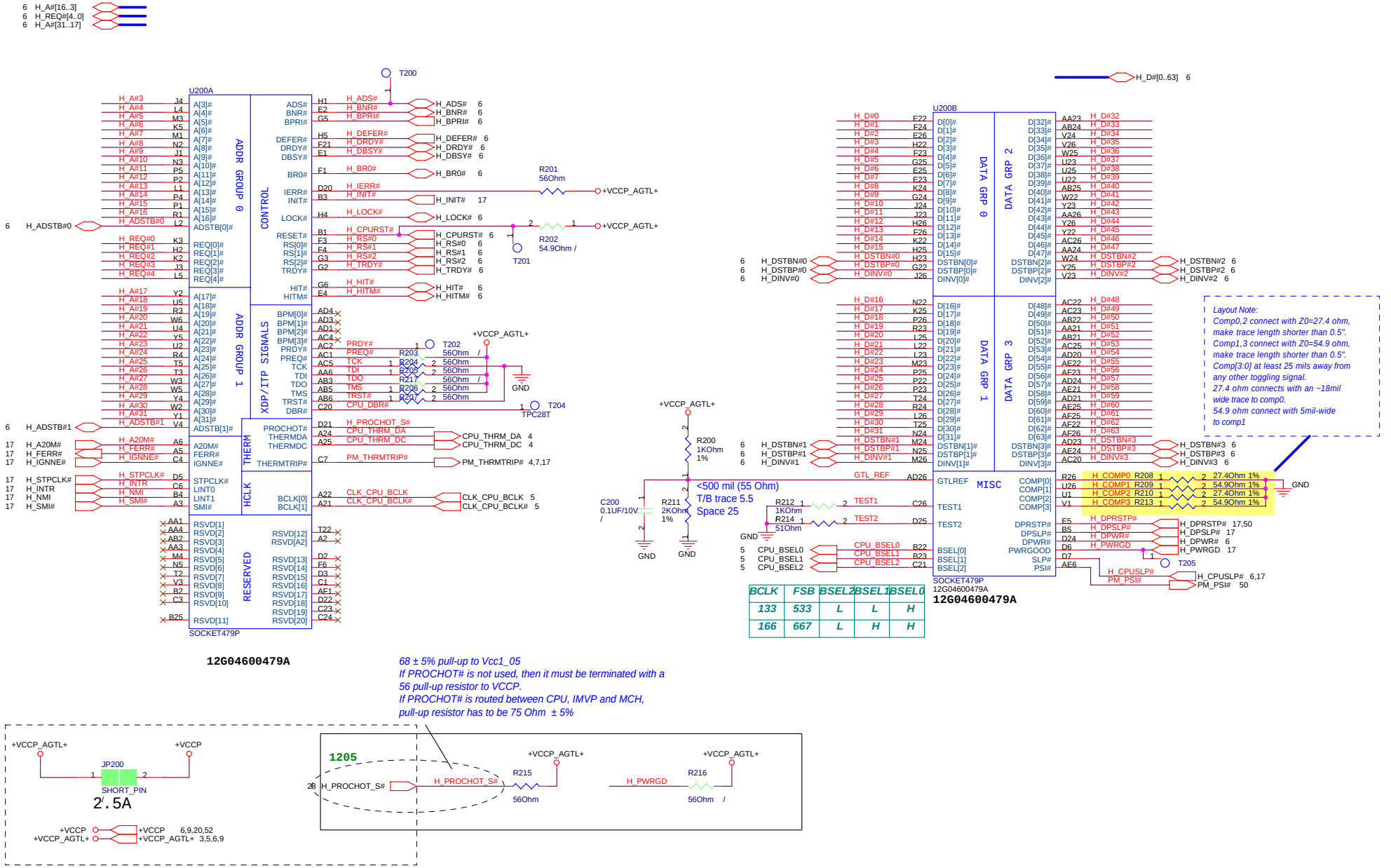
Title : BLOCK DIAGRAM

Engineer: Ping-Yen Tsai

ASUSTeK COMPUTER INC

Size	Project Name	Rev
Custom	A3F	2.0

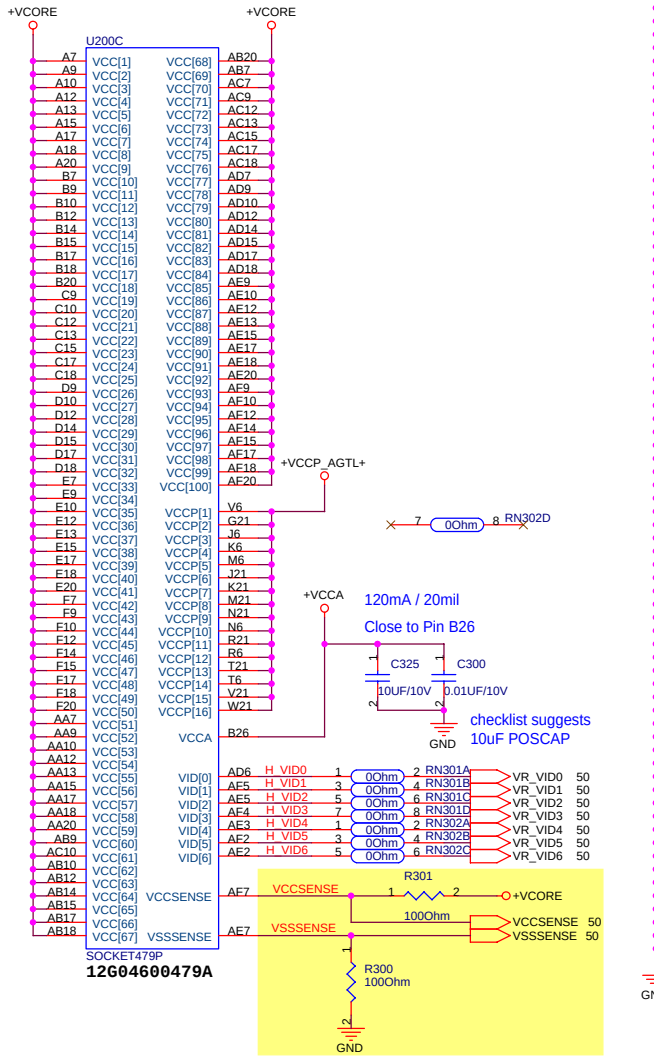
Date: Wednesday, January 18, 2006 Sheet 1 of 63

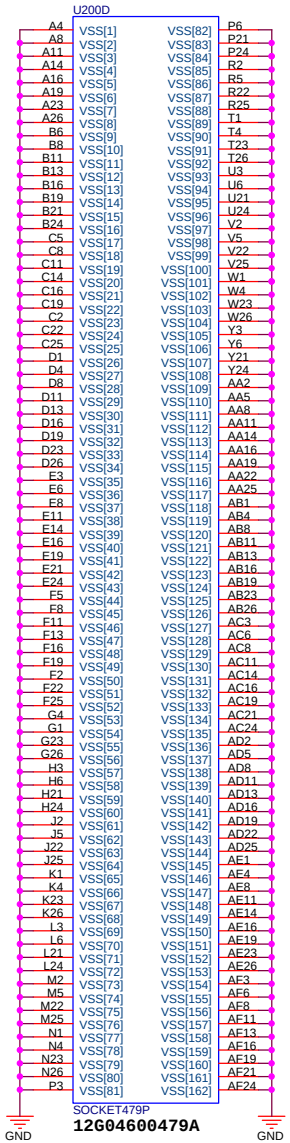


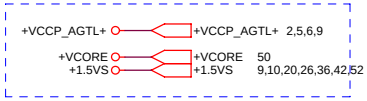
Title :	YONAH CPU (1)
ASUSTeK COMPUTER INC	Engineer: Ping-Yen Tsai
Size: Custom	Project Name: A3F
Rev: 2.0	
Date: Wednesday, January 18, 2006	Sheet 2 of 63

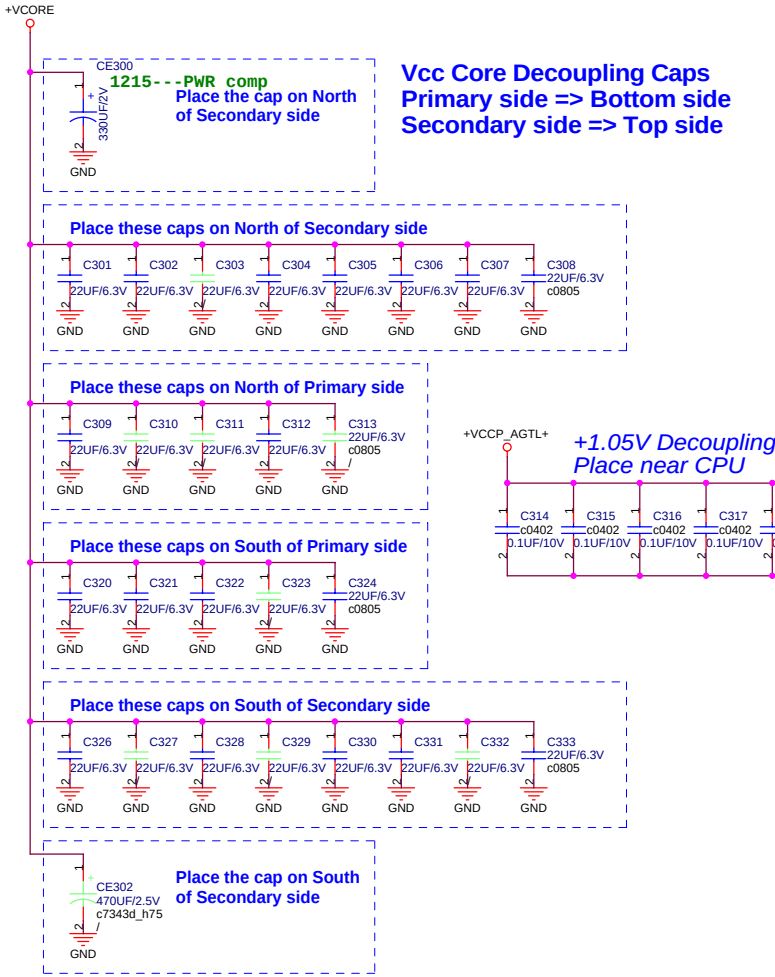
YUNAH FSB667			
	LFM	TYP	HFM
VCC	1.14V	1.2V	1.356V
	C4	C3	C0
ICC	0.9A	7.59A	27A

YUNAH FSB667			
	Min	Typ	Max
VCCP	0.997V	1.05V	1.102V
	Min	Typ	Max
ICCP			2.5A









Layout Note:
VCCSENSE/VSSSENSE lines between the CPU and the VR should have a trace width of 18 mils on 7 mils spacing, with trace impedance of Zo=27.4 Ohm.
The VCCSENSE/VSSSENSE should be length matched to within 25 mils.
These resistors should be placed within 2 inch of the CPU.

ASUSTeK COMPUTER INC	Title : Yonah CPU (2)	
	Engineer: *Ping-Yen Tsai*	
Size: A3	Project Name: A3F	Rev: 2.0
Date: Wednesday, January 18, 2006	Sheet 3 of 63	

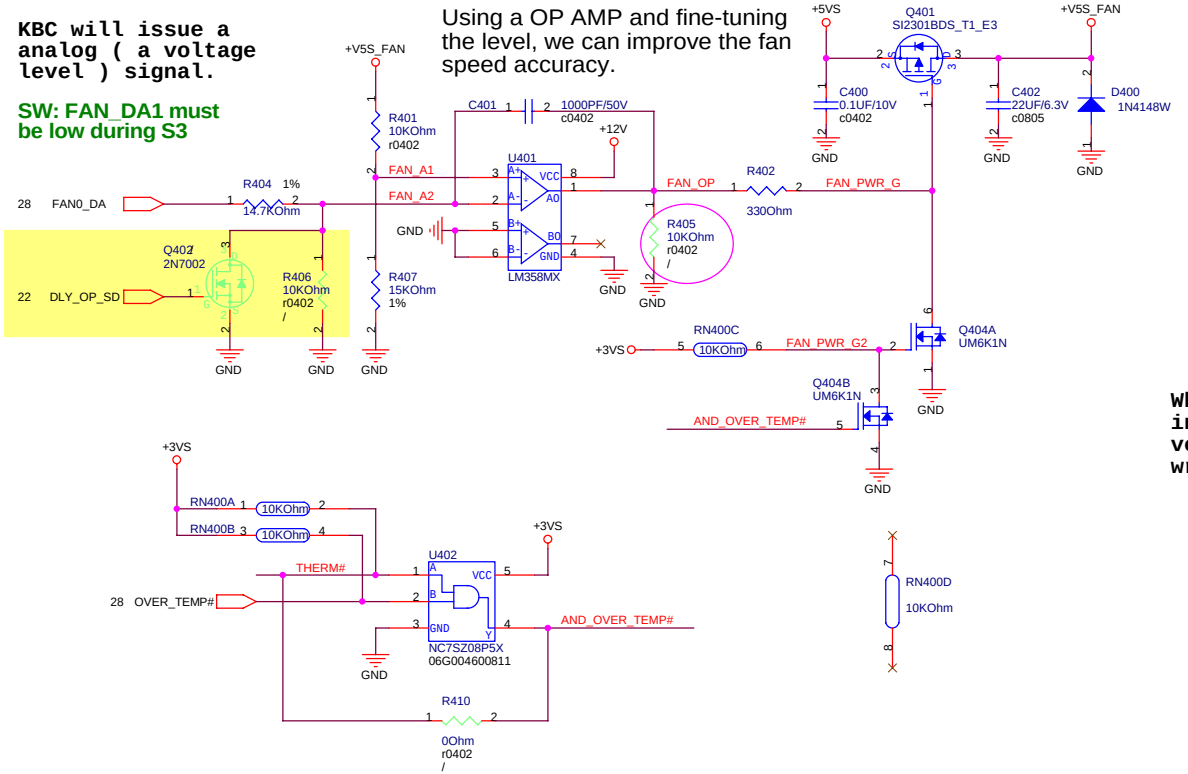
Fan Speed Control

+12V	+12V	35,36,61
+5VS	+5VS	13,19,20,21,22,27,28,36,37,38,44,50,61
+3VS	+3VS	5,7,9,11,12,13,14,15,19,20,21,22,25,26,27,28,30,36,38,39,42,50,52,60,61
+3VA	+3VA	12,20,28,37,39,54,59,63

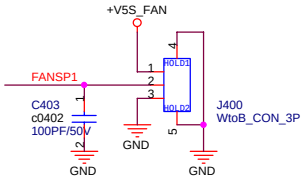
KBC will issue a analog (a voltage level) signal.

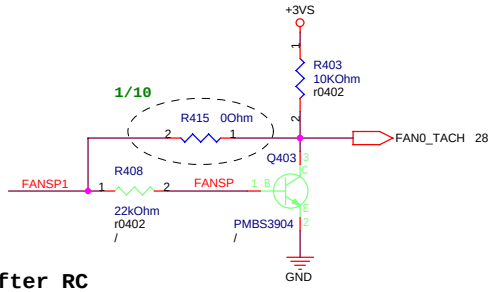
SW: FAN_DA1 must be low during S3

Using a OP AMP and fine-tuning the level, we can improve the fan speed accuracy.

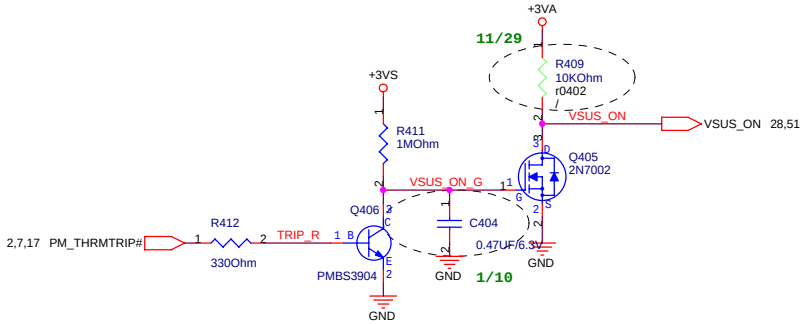


CPU FAN





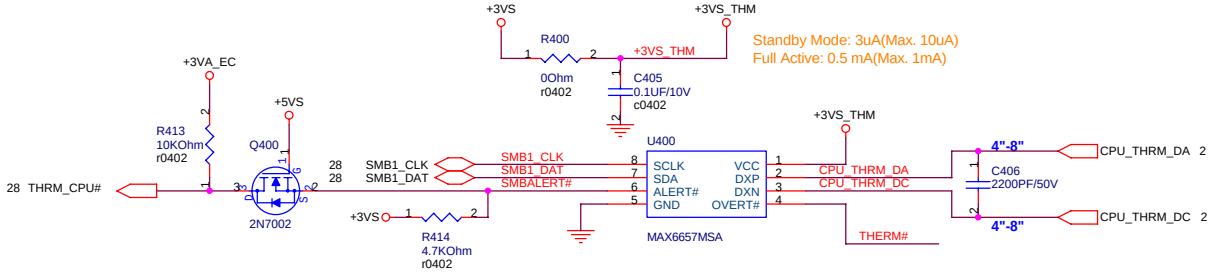
When fan speed is very slow, after RC integrator the level of FANSP1 will be very low that may make south bridge do the wrong detection.



Route H_THERMDA and H_THERMDC on the same layer

----------OTHER SIGNALS
12 mils
==========GND
10 mils
=========H_THERMDA(10 mils)
10 mils
=========H_THERMDC(10 mils)
10 mils
=========GND
12 mils
----------OTHER SIGNALS

Avoid BPSB,Power



ASUSTeK COMPUTER INC

Title : THER-SENSOR,FAN

Engineer: *Ping-Yen Tsai*

Size	Project Name	Rev
A3	A3F	2.0

Date: Wednesday, January 18, 2006 Sheet 4 of 63

Request	Control net	Net name
PCIE_REQ1#	PCIE0(#),PCIE6(#)	None
PCIE_REQ2#	PCIE1(#),PCIE8(#)	None
PCIE_REQ3#	PCIE2(#),PCIE4(#)	CLK_PCIE_MINICARD(#)
PCIE_REQ4#	PCIE3(#),PCIE5(#), PCIE7(#)	CLK_MCH_3GPLL(#)

Bclk	FSB	FSLC BSEL2	FSLB BSEL1	FSLA BSEL0
133	533	L	L	H
166	667	L	H	H

+VCCP_AGTL+ — +VCCP_AGTL+ 2,3,6,9

+3VS — +3VS 4,7,9,11,12,13,14,15,19,20,21,22,25,26,27,28,30,36,38,39,42,50,52,60,61

Layout Note:
Place termination close to source IC

Pin34 is PWRSAVE#

PREQ#1
0=PCIEX 6/0 Not Controlled
1=PCIEX 6/0 Controlled

PREQ#2
0=PCIEX 8/1 Not Controlled
1=PCIEX 8/1 Controlled

PREQ#3
0=PCIEX 4/2 Not Controlled
1=PCIEX 4/2 Controlled

PREQ#4
0=PCIEX 7/5/3 Not Controlled
1=PCIEX 7/5/3 Controlled

SELPCIE0_LCD#:
0-->pin17,pin18=LCDCLK(96MHz) or 27M/27M_SS

SELLCD_27#/PCICLK_F1:
1-->pin17,pin18=LCDCLK(96MHz)

PCICLK2/REQ_SEL:
1-->pin40,pin41=PREQ1#,PREQ2#

ITP_EN/PCICLK_F0:
1-->CPU_ITP pair

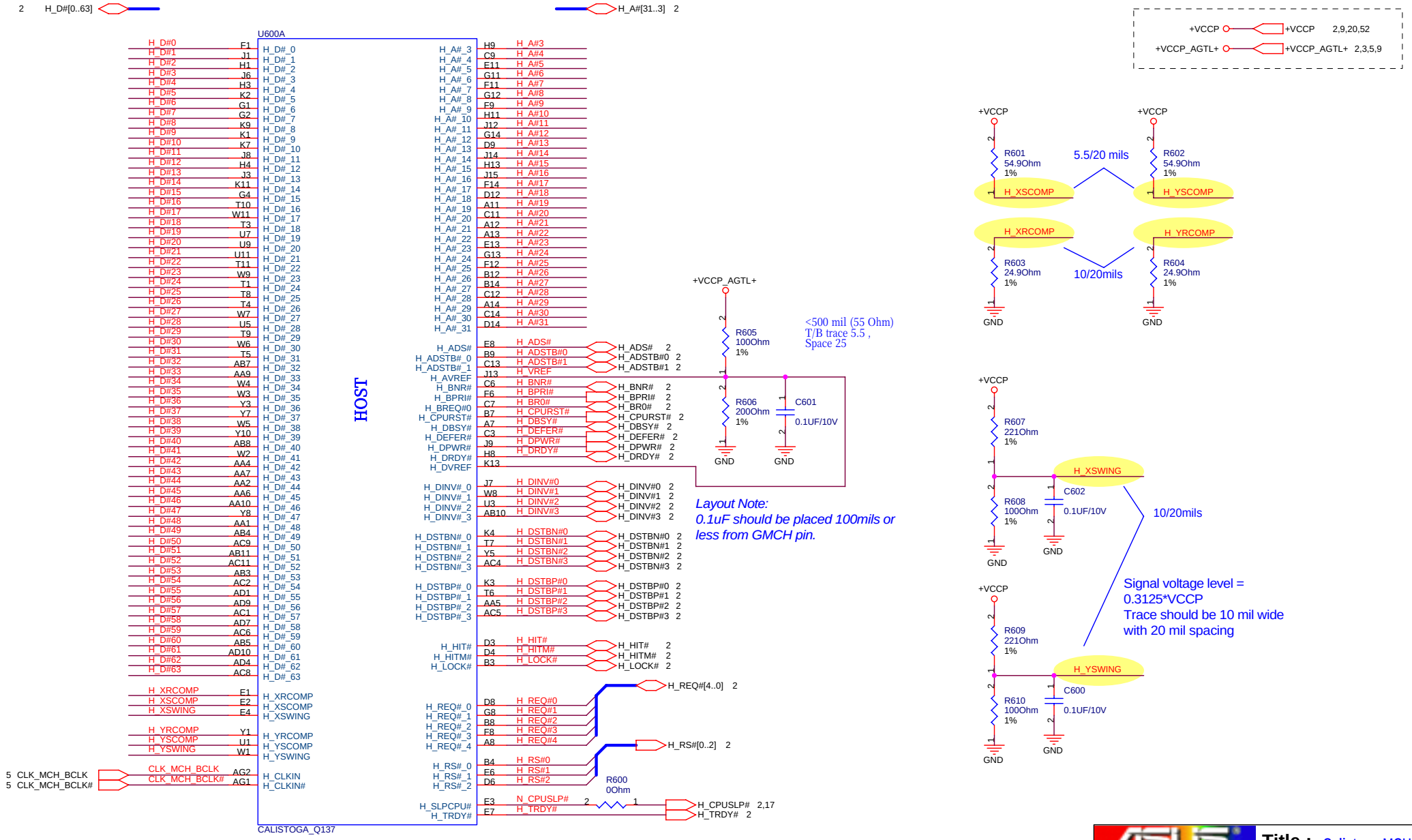
Realtek:Mount R519,Remove R550 R534

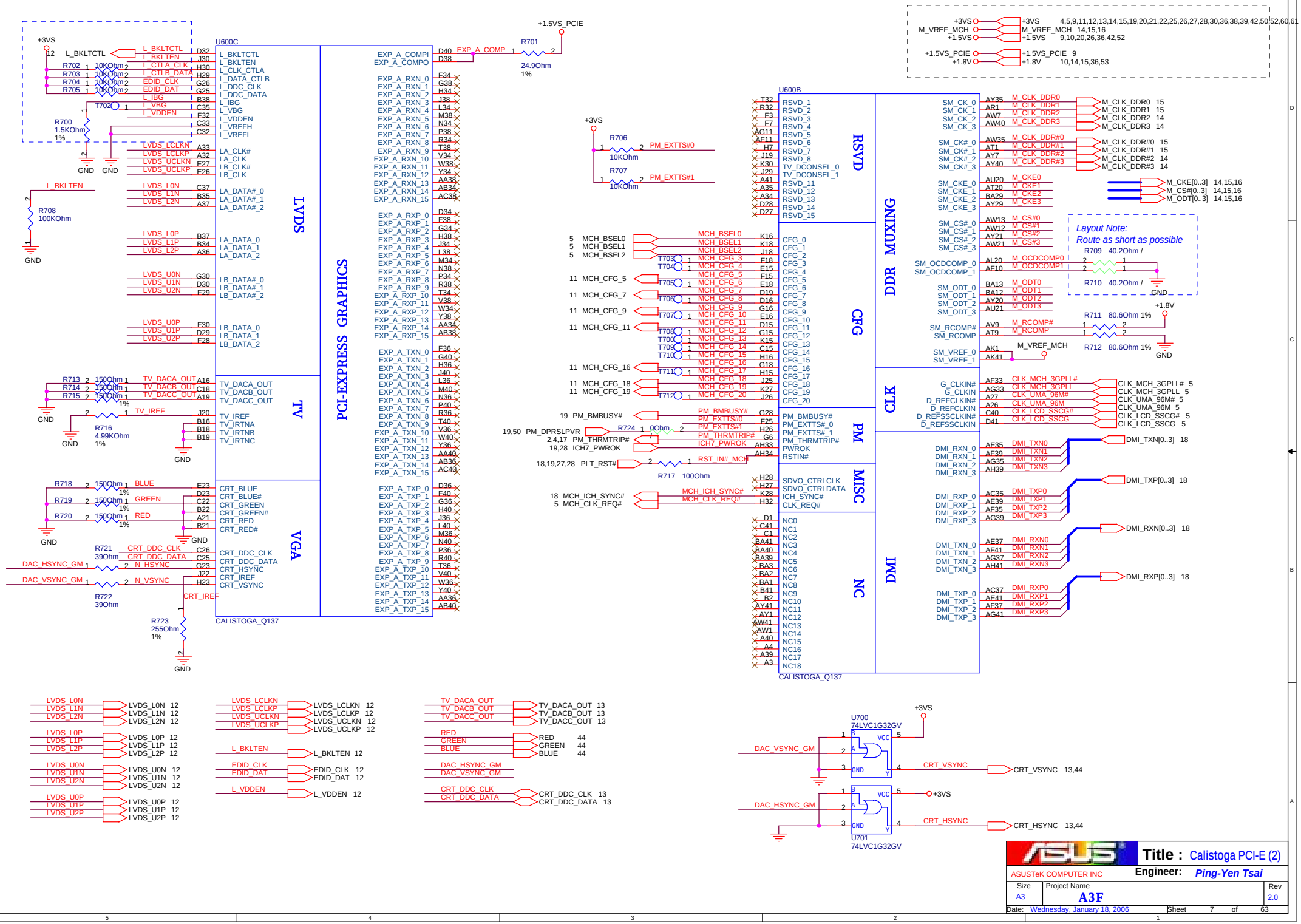
Internal Pull-Up Resistor

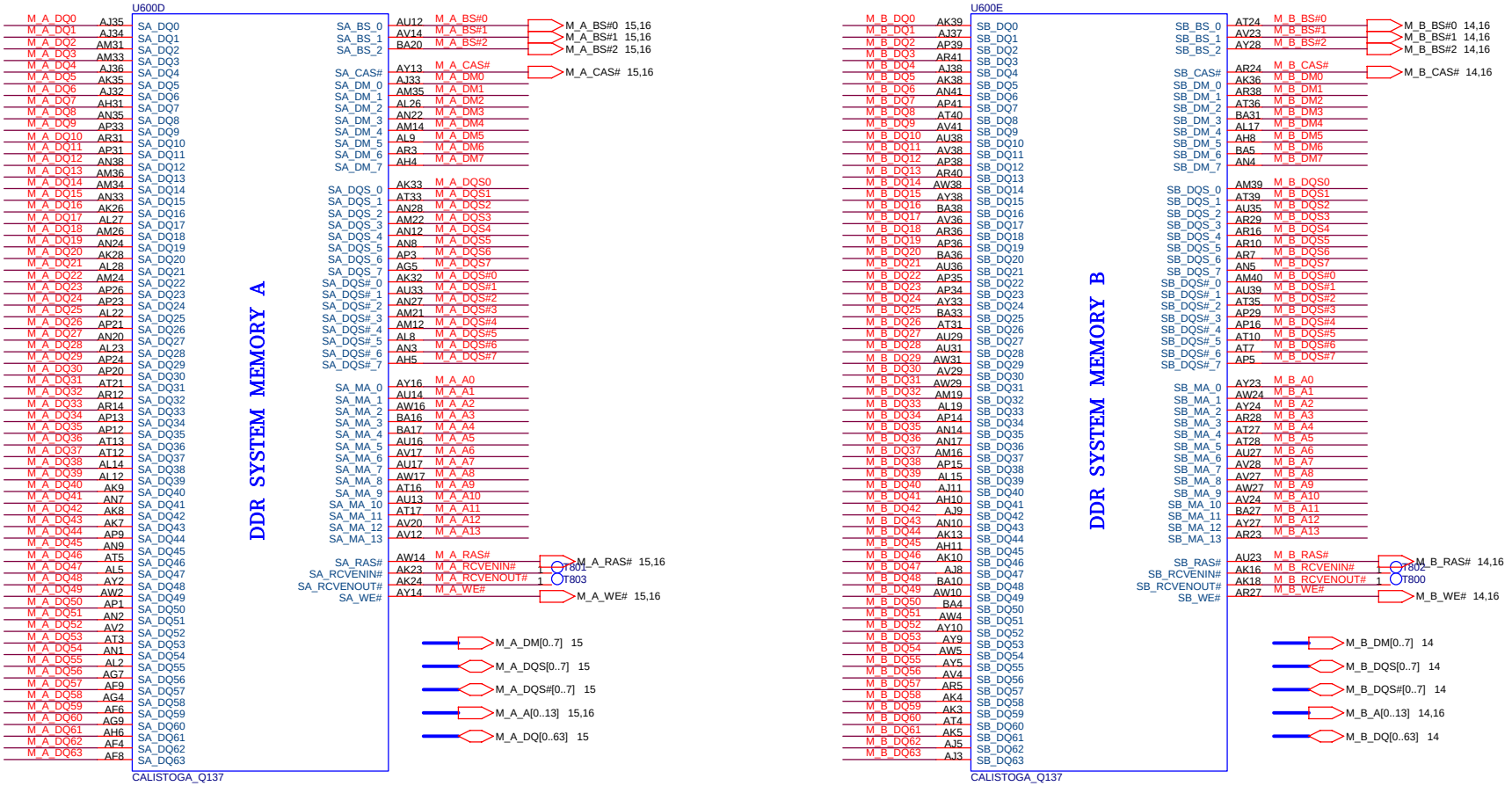
Internal Pull-Down Resistor

ICS954310BGLFT

Title :	CLOCK GEN	
ASUSTeK COMPUTER INC	Engineer:	Ping-Yen Tsai
Size: Custom	Project Name: A3F	Rev: 2.0
Date: Wednesday, January 18, 2006	Sheet 5 of 63	


2 H_D#[0..63]
H_A#[31..3] 2
+VCCP +VCCP 2,9,20,52
+VCCP_AGTL+ +VCCP_AGTL+ 2,3,5,9
U600A
HOST
CALISTOGA_Q137
+VCCP_AGTL+
R605 100Ohm 1%
R606 200Ohm 1%
C601 0.1UF/10V
GND
<500 mil (55 Ohm) T/B trace 5.5 , Space 25
Layout Note:
0.1uF should be placed 100mils or less from GMCH pin.
R600 0Ohm
+VCCP
R601 54.9Ohm 1%
R602 54.9Ohm 1%
5.5/20 mils
H_XSCOMP
H_YSCOMP
H_XRCOMP
H_YRCOMP
R603 24.9Ohm 1%
R604 24.9Ohm 1%
10/20mils
R607 221Ohm 1%
R608 100Ohm 1%
C602 0.1UF/10V
H_XSWING
10/20mils
Signal voltage level = 0.3125*VCCP
Trace should be 10 mil wide with 20 mil spacing
R609 221Ohm 1%
R610 100Ohm 1%
C600 0.1UF/10V
H_YSWING
5 CLK_MCH_BCLK
5 CLK_MCH_BCLK#
H_REQ#[4..0] 2
H_RS#[0..2] 2
H_CPUSLP# 2,17
H_TRDY# 2
Title : Calistoga MCH (1)
ASUSTeK COMPUTER INC
Engineer: Ping-Yen Tsai
Size B
Project Name A3F
Rev 2.0
Date: Wednesday, January 18, 2006
Sheet 6 of 63


+3VS
+3VS 4,5,9,11,12,13,14,15,19,20,21,22,25,26,27,28,30,36,38,39,42,50,52,60,61
M_VREF_MCH
M_VREF_MCH 14,15,16
+1.5VS
+1.5VS 9,10,20,26,36,42,52
+1.5VS_PCIE
+1.5VS_PCIE 9
+1.8V
+1.8V 10,14,15,36,53
U600C
L_BKLTCTL
L_BKLTEN
L_CTLA_CLK
L_CTLB_DATA
EDID_CLK
EDID_DAT
L_IBG
L_VBG
L_VDDEN
L_VREFH
L_VREFL
LVDS_LCLKN
LVDS_LCLKP
LVDS_UCLKN
LVDS_UCLKP
LVDS_L0N
LVDS_L1N
LVDS_L2N
LVDS_L0P
LVDS_L1P
LVDS_L2P
LVDS_U0N
LVDS_U1N
LVDS_U2N
LVDS_U0P
LVDS_U1P
LVDS_U2P
LVDS
TV_DACA_OUT
TV_DACB_OUT
TV_DACC_OUT
TV_IREF
TV_IRTNA
TV_IRTNB
TV_IRTNC
TV
CRT_BLUE
CRT_BLUE#
CRT_GREEN
CRT_GREEN#
CRT_RED
CRT_RED#
CRT_DDC_CLK
CRT_DDC_DATA
CRT_HSYNC
CRT_IREF
CRT_VSYNC
VGA
CALISTOGA_Q137
PCI-EXPRESS GRAPHICS
EXP_A_COMPI
EXP_A_COMPO
EXP_A_COMP
R701
24.9Ohm
1%
+1.5VS_PCIE
EXP_A_RXN_0
EXP_A_RXN_1
EXP_A_RXN_2
EXP_A_RXN_3
EXP_A_RXN_4
EXP_A_RXN_5
EXP_A_RXN_6
EXP_A_RXN_7
EXP_A_RXN_8
EXP_A_RXN_9
EXP_A_RXN_10
EXP_A_RXN_11
EXP_A_RXN_12
EXP_A_RXN_13
EXP_A_RXN_14
EXP_A_RXN_15
EXP_A_RXP_0
EXP_A_RXP_1
EXP_A_RXP_2
EXP_A_RXP_3
EXP_A_RXP_4
EXP_A_RXP_5
EXP_A_RXP_6
EXP_A_RXP_7
EXP_A_RXP_8
EXP_A_RXP_9
EXP_A_RXP_10
EXP_A_RXP_11
EXP_A_RXP_12
EXP_A_RXP_13
EXP_A_RXP_14
EXP_A_RXP_15
EXP_A_TXN_0
EXP_A_TXN_1
EXP_A_TXN_2
EXP_A_TXN_3
EXP_A_TXN_4
EXP_A_TXN_5
EXP_A_TXN_6
EXP_A_TXN_7
EXP_A_TXN_8
EXP_A_TXN_9
EXP_A_TXN_10
EXP_A_TXN_11
EXP_A_TXN_12
EXP_A_TXN_13
EXP_A_TXN_14
EXP_A_TXN_15
EXP_A_TXP_0
EXP_A_TXP_1
EXP_A_TXP_2
EXP_A_TXP_3
EXP_A_TXP_4
EXP_A_TXP_5
EXP_A_TXP_6
EXP_A_TXP_7
EXP_A_TXP_8
EXP_A_TXP_9
EXP_A_TXP_10
EXP_A_TXP_11
EXP_A_TXP_12
EXP_A_TXP_13
EXP_A_TXP_14
EXP_A_TXP_15
U600B
RSVD
CFG
PM
MISC
NC
DDR MUXING
CLK
DMI
CALISTOGA_Q137
M_CLK_DDR0
M_CLK_DDR1
M_CLK_DDR2
M_CLK_DDR3
M_CKE0
M_CKE1
M_CKE2
M_CKE3
M_CS#0
M_CS#1
M_CS#2
M_CS#3
M_ODCDCOMP0
M_ODCDCOMP1
M_ODT0
M_ODT1
M_ODT2
M_ODT3
M_RCOMP#
M_RCOMP
M_VREF_MCH
CLK_MCH_3GPLL#
CLK_MCH_3GPLL
CLK_UMA_96M#
CLK_UMA_96M
CLK_LCD_SSCG#
CLK_LCD_SSCG
DMI_TXN[0..3]
DMI_TXP[0..3]
DMI_RXN[0..3]
DMI_RXP[0..3]
Layout Note:
Route as short as possible
R709 40.2Ohm /
R710 40.2Ohm /
R711 80.6Ohm 1%
R712 80.6Ohm 1%
M_CLK_DDR[0..3] 15
M_CLK_DDR[0..3] 14
M_CKE[0..3] 14,15,16
M_CS#[0..3] 14,15,16
M_ODT[0..3] 14,15,16
MCH_BSEL0
MCH_BSEL1
MCH_BSEL2
MCH_CFG_3
MCH_CFG_4
MCH_CFG_5
MCH_CFG_6
MCH_CFG_7
MCH_CFG_8
MCH_CFG_9
MCH_CFG_10
MCH_CFG_11
MCH_CFG_12
MCH_CFG_13
MCH_CFG_14
MCH_CFG_15
MCH_CFG_16
MCH_CFG_17
MCH_CFG_18
MCH_CFG_19
MCH_CFG_20
PM_BMBUSY#
PM_EXTTS#0
PM_EXTTS#1
PM_THRMTRIP#
ICH7_PWROK
RST_IN#_MCH
R724 0Ohm
R717 100Ohm
SDVO_CTRLCLK
SDVO_CTRLDATA
ICH_SYNC#
MCH_ICH_SYNC#
MCH_CLK_REQ#
R706 10KOhm
R707 10KOhm
PM_EXTTS#0
PM_EXTTS#1
R700 1.5KOhm 1%
R702 10KOhm
R703 10KOhm
R704 10KOhm
R705 10KOhm
R708 100KOhm
R713 150Ohm 1%
R714 150Ohm 1%
R715 150Ohm 1%
R716 4.99KOhm 1%
R718 150Ohm 1%
R719 150Ohm 1%
R720 150Ohm 1%
R721 39Ohm
R722 39Ohm
R723 255Ohm 1%
T702
GND
LVDS_L0N 12
LVDS_L1N 12
LVDS_L2N 12
LVDS_L0P 12
LVDS_L1P 12
LVDS_L2P 12
LVDS_U0N 12
LVDS_U1N 12
LVDS_U2N 12
LVDS_U0P 12
LVDS_U1P 12
LVDS_U2P 12
LVDS_LCLKN 12
LVDS_LCLKP 12
LVDS_UCLKN 12
LVDS_UCLKP 12
L_BKLTEN 12
EDID_CLK 12
EDID_DAT 12
L_VDDEN 12
TV_DACA_OUT 13
TV_DACB_OUT 13
TV_DACC_OUT 13
RED 44
GREEN 44
BLUE 44
CRT_DDC_CLK 13
CRT_DDC_DATA 13
U700
74LVC1G32GV
U701
74LVC1G32GV
CRT_VSYNC 13,44
CRT_HSYNC 13,44
Title : Calistoga PCI-E (2)
ASUSTeK COMPUTER INC
Engineer: Ping-Yen Tsai
Size A3
Project Name A3F
Rev 2.0
Date: Wednesday, January 18, 2006
Sheet 7 of 63



ASUSTeK COMPUTER INC

Title : Calistoga DDR2 (3)

Engineer: *Ping-Yen Tsai*

Size	Project Name	Rev
A3	A3F	2.0

Date: Wednesday, January 18, 2006 Sheet 8 of 63

Layout Note:
Place filter components close to GMCH

Layout Note:
Caps should be on Top layer

+1.5VS_PCIE

VCC3G

+1.5VS_3GPLL

1500 mA

L901 120Ohm/100Mhz
CE900 150UF/4V
C901 10UF/10V
C902 10UF/10V

L902 30Ohm/100Mhz
C903 0.1UF/10V
C904 10UF/10V
VCCA_3GPLL

+1.5VS_VCCAUX

L900 80Ohm/100Mhz
CE902 470UF/2.5V
C908 0.1UF/10V
VCCAUX
1900 mA

+1.5VS_DPLLA

L903 30Ohm/100Mhz
CE903 470UF/2.5V
C911 0.1UF/10V
VCCA_DPLLA
50 mA

+1.5VS_DPLLB

L905 30Ohm/100Mhz
CE904 470UF/2.5V
C917 0.1UF/10V
VCCA_DPLLB
50 mA

+1.5VS_HPLL

L906 120Ohm/100Mhz
C922 22UF/6.3V
C923 0.1UF/10V
VCCA_HPLL
45 mA

+1.5VS_MPLL

L907 120Ohm/100Mhz
C926 22UF/6.3V
C927 0.1UF/10V
VCCA_MPLL
45 mA

Layout Note:
0.1uF caps in 1.5VS_xPLL need to be located as edge caps within 200 mils.

GMCH VCORE

+VCCP
+1.05VS
3500 mA
+VCCP_GMCH
JP900 SHORT_PIN
JP901 SHORT_PIN

+1.5VS
VCCD_LVDS 20 mA
Pin A28 B28 C28
C909 0.1UF/10V
C910 10UF/10V

+1.5VS
VCCD_TVDAC
Pin D21
C912 0.022UF/25V
C913 0.1UF/10V
24 mA

+1.5VS
VCCD_QTVDAC
H19 C28
C918 0.022UF/25V
C919 0.1UF/10V

Layout Note:
These Caps should be within 250 mils of edge of GMCH

Layout Note:
These 0.1uF caps should be placed within 200 mils of edge

+2.5VS
VCC_SYNC
Pin H22
C931 0.1UF/10V

VCCA_LVDS
Pin A38 10 mA
C900 0.01UF/25V
C932 0.1UF/10V

VCCA_3GBG
Pin G41 2 mA
C933 0.1UF/10V

VCCTX_LVDS 60 mA
Pin A30 B30 C30
C934 0.1UF/10V
C935 4.7UF/10V

R904 10Ohm
+VCCP_GMCH_R
D901 BAT54C
+VCCP_GMCH

70 mA
VCCA_CRTDAC
Pin E21 F21
L908 120Ohm/100Mhz
C944 0.022UF/25V
C945 0.1UF/10V
+2.5VS_CRTDAC

Layout Note:
These Caps should be within 250 mils of edge of GMCH

+3VS
VCC_HV 40 mA
Pin A23 B23 B25
C942 10UF/10V
C943 0.1UF/10V

U600H

H22	VCCSYNC	
C30	VCC_TXLVDS0	
B30	VCC_TXLVDS1	
A30	VCC_TXLVDS2	
AJ41	VCC3G0	
AB41	VCC3G1	
Y41	VCC3G2	
V41	VCC3G3	
R41	VCC3G4	
N41	VCC3G5	
L41	VCC3G6	
AC33	VCCA_3GPLL	
G41	VCCA_3GBG	
H41	VSSA_3GBG	
F21	VCCA_CRTDAC0	
E21	VCCA_CRTDAC1	
G21	VSSA_CRTDAC	
B26	VCCA_DPLLA	
C39	VCCA_DPLLB	
AF1	VCCA_HPLL	
A38	VCCA_LVDS	
B39	VSSA_LVDS	
AF2	VCCA_MPLL	
H20	VCCA_TVBG	
G20	VSSA_TVBG	
E19	VCCA_TVDACA0	
F19	VCCA_TVDACA1	
C20	VCCA_TVDACB0	
D20	VCCA_TVDACB1	
E20	VCCA_TVDACC0	
F20	VCCA_TVDACC1	
AH1	VCCD_HMPLL0	
AH2	VCCD_HMPLL1	
A28	VCCD_LVDS0	
B28	VCCD_LVDS1	
C28	VCCD_LVDS2	
D21	VCCD_TVDAC	
A23	VCC_HV0	
B23	VCC_HV1	
B25	VCC_HV2	
H19	VCCD_QTVDAC	
AK31	VCCAUX0	
AF31	VCCAUX1	
AE31	VCCAUX2	
AC31	VCCAUX3	
AL30	VCCAUX4	
AK30	VCCAUX5	
AJ30	VCCAUX6	
AH30	VCCAUX7	
AG30	VCCAUX8	
AF30	VCCAUX9	
AE30	VCCAUX10	
AD30	VCCAUX11	
AC30	VCCAUX12	
AG29	VCCAUX13	
AF29	VCCAUX14	
AE29	VCCAUX15	
AD29	VCCAUX16	
AC29	VCCAUX17	
AG28	VCCAUX18	
AF28	VCCAUX19	
AE28	VCCAUX20	
AH22	VCCAUX21	
AJ21	VCCAUX22	
AH21	VCCAUX23	
AJ20	VCCAUX24	
AH20	VCCAUX25	
AH19	VCCAUX26	
P19	VCCAUX27	
P16	VCCAUX28	
AH15	VCCAUX29	
P15	VCCAUX30	
AH14	VCCAUX31	
AG14	VCCAUX32	
AF14	VCCAUX33	
AE14	VCCAUX34	
Y14	VCCAUX35	
AE13	VCCAUX36	
AF13	VCCAUX37	
AE12	VCCAUX38	
AF12	VCCAUX39	
AD12	VCCAUX40	

CALISTOGA_Q137

POWER

VTT_0	AC14
VTT_1	AB14
VTT_2	W14
VTT_3	V14
VTT_4	T14
VTT_5	R14
VTT_6	P14
VTT_7	N14
VTT_8	M14
VTT_9	L14
VTT_10	AD13
VTT_11	AC13
VTT_12	AB13
VTT_13	AA13
VTT_14	Y13
VTT_15	W13
VTT_16	V13
VTT_17	U13
VTT_18	T13
VTT_19	R13
VTT_20	N13
VTT_21	M13
VTT_22	L13
VTT_23	AB12
VTT_24	AA12
VTT_25	Y12
VTT_26	W12
VTT_27	V12
VTT_28	U12
VTT_29	T12
VTT_30	R12
VTT_31	P12
VTT_32	N12
VTT_33	M12
VTT_34	L12
VTT_35	R11
VTT_36	P11
VTT_37	N11
VTT_38	M11
VTT_39	R10
VTT_40	P10
VTT_41	N10
VTT_42	M10
VTT_43	P9
VTT_44	N9
VTT_45	M9
VTT_46	R8
VTT_47	P8
VTT_48	N8
VTT_49	M8
VTT_50	P7
VTT_51	N7
VTT_52	M7
VTT_53	R6
VTT_54	P6
VTT_55	M6
VTT_56	A6
VTT_57	R5
VTT_58	P5
VTT_59	N5
VTT_60	M5
VTT_61	P4
VTT_62	N4
VTT_63	M4
VTT_64	R3
VTT_65	P3
VTT_66	N3
VTT_67	M3
VTT_68	R2
VTT_69	P2
VTT_70	M2
VTT_71	D2
VTT_72	AB1
VTT_73	R1
VTT_74	P1
VTT_75	N1
VTT_76	M1

VTTLF_CAP3
C928 0.47UF/16V

VTTLF_CAP2
VTTLF_CAP1
C936 0.47UF/16V
C937 0.22UF/6.3V

NOTE:0.1UF CAPS USED IN +1.5VS, +3.3VS
+2.5VS should be placed within 200 mils of edge.

+VCCP_AGTL+ +VCCP_AGTL+ 2,3,5,6
+VCCP_GMCH +VCCP_GMCH 10,42
+1.5VS_PCIE +1.5VS_PCIE 7
+3VS +3VS 4,5,7,11,12,13,14,15,19,20,21,22,25,26,27,28,30,36,38,39,42,50,52,60,61
+2.5VS +2.5VS 13,36,54
+1.5VS +1.5VS 10,20,26,36,42,52

+VCCP_AGTL+
800 mA
C905 4.7UF/10V
C906 2.2UF/6.3V
C907 0.22UF/6.3V
CE901 330UF/2V 11G08D233722

Layout Note:
Place on the edge

Layout Note:
Place in cavity

+3VS +3VS_DAC
R900 0Ohm
R901 10Ohm
+1.5VS_DAC
D900 BAT54C
+1.5VS
L904 180Ohm/100Mhz
C914 10UF/10V

Total Power Consumption 120 mA

+3VS_TVBG
C915 0.022UF/25V
C916 0.1UF/10V
VCCA_TVBG
Pin H20

+3VS_TVDACA
C920 0.022UF/25V
C921 0.1UF/10V
VCCA_TVDACA
Pin E19 F19

+3VS_TVDACB
C924 0.022UF/25V
C925 0.1UF/10V
VCCA_TVDACB
Pin C20 D20

+3VS_TVDACC
C929 0.022UF/25V
C930 0.1UF/10V
VCCA_TVDACC
Pin E20 F20

Layout Note:
These Caps used in +3VS_TVDACx should be within 250 mils of edge of GMCH

+3VS
+5V
12/1
U900 SI9183DT
VIN VOUT GND FB SD#
R902 10KOhm
3VS_DAC_EN
3VS_DAC_ADJ
R903 35.7KOhm
+3VS_DAC
C938 0.1UF/50V
C939 4.7UF/16V
C940 0.1UF/50V
20KOhm R905
C941 4.7UF/16V

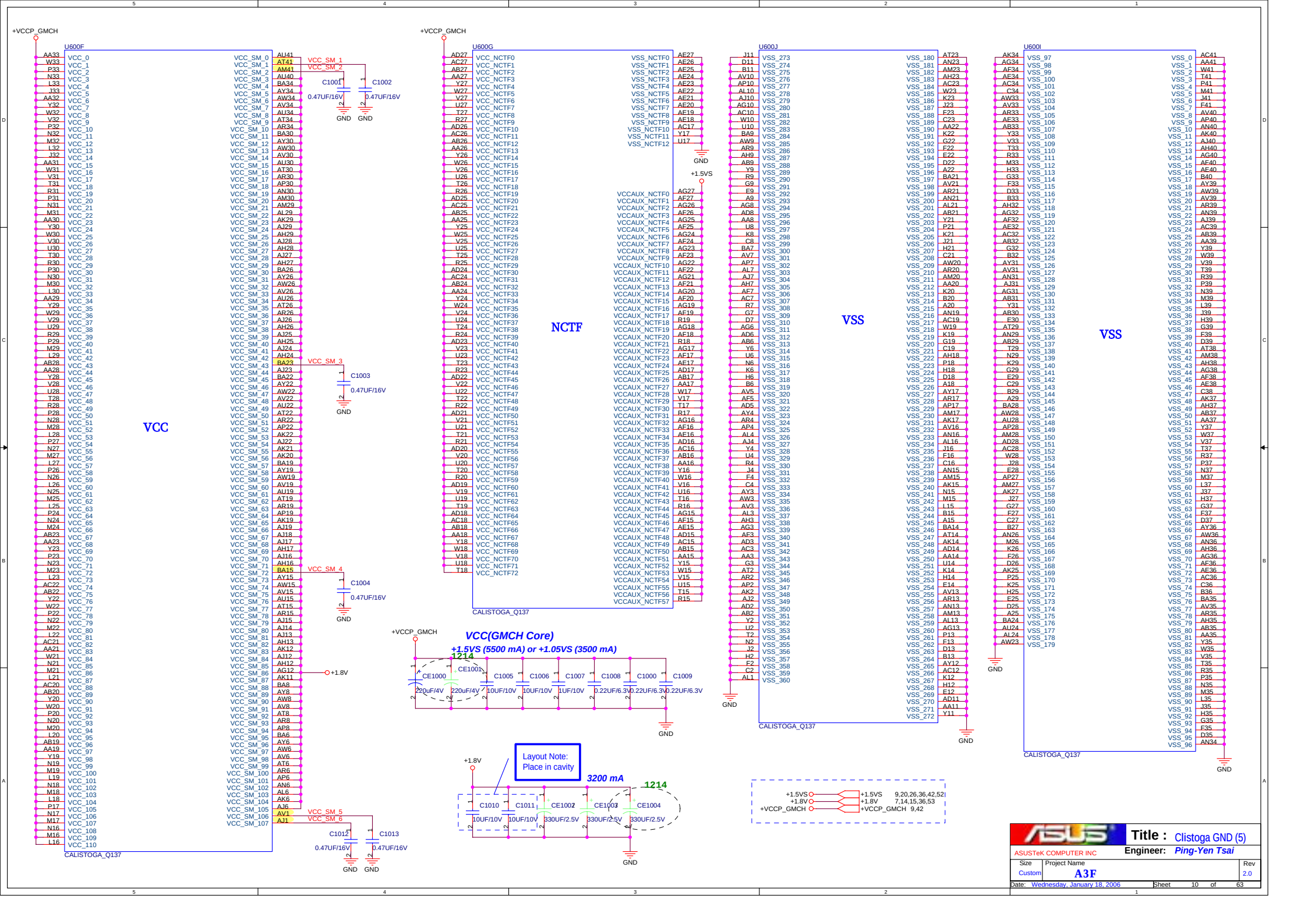
ASUSTeK COMPUTER INC

Title : Calistoga Power (4)

Engineer: *Ping-Yen Tsai*

Size	Project Name	Rev
A3	A3F	2.0

Date: Wednesday, January 18, 2006 Sheet 9 of 63


+VCCP_GMCH
U600F
VCC_0
VCC_1
VCC_2
VCC_3
VCC_4
VCC_5
VCC_6
VCC_7
VCC_8
VCC_9
VCC_10
VCC_11
VCC_12
VCC_13
VCC_14
VCC_15
VCC_16
VCC_17
VCC_18
VCC_19
VCC_20
VCC_21
VCC_22
VCC_23
VCC_24
VCC_25
VCC_26
VCC_27
VCC_28
VCC_29
VCC_30
VCC_31
VCC_32
VCC_33
VCC_34
VCC_35
VCC_36
VCC_37
VCC_38
VCC_39
VCC_40
VCC_41
VCC_42
VCC_43
VCC_44
VCC_45
VCC_46
VCC_47
VCC_48
VCC_49
VCC_50
VCC_51
VCC_52
VCC_53
VCC_54
VCC_55
VCC_56
VCC_57
VCC_58
VCC_59
VCC_60
VCC_61
VCC_62
VCC_63
VCC_64
VCC_65
VCC_66
VCC_67
VCC_68
VCC_69
VCC_70
VCC_71
VCC_72
VCC_73
VCC_74
VCC_75
VCC_76
VCC_77
VCC_78
VCC_79
VCC_80
VCC_81
VCC_82
VCC_83
VCC_84
VCC_85
VCC_86
VCC_87
VCC_88
VCC_89
VCC_90
VCC_91
VCC_92
VCC_93
VCC_94
VCC_95
VCC_96
VCC_97
VCC_98
VCC_99
VCC_100
VCC_101
VCC_102
VCC_103
VCC_104
VCC_105
VCC_106
VCC_108
VCC_109
VCC_110
VCC
CALISTOGA_Q137
VCC_SM_0
VCC_SM_1
VCC_SM_2
VCC_SM_3
VCC_SM_4
VCC_SM_5
VCC_SM_6
VCC_SM_7
VCC_SM_8
VCC_SM_9
VCC_SM_10
VCC_SM_11
VCC_SM_12
VCC_SM_13
VCC_SM_14
VCC_SM_15
VCC_SM_16
VCC_SM_17
VCC_SM_18
VCC_SM_19
VCC_SM_20
VCC_SM_21
VCC_SM_22
VCC_SM_23
VCC_SM_24
VCC_SM_25
VCC_SM_26
VCC_SM_27
VCC_SM_28
VCC_SM_29
VCC_SM_30
VCC_SM_31
VCC_SM_32
VCC_SM_33
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VCC_SM_35
VCC_SM_36
VCC_SM_37
VCC_SM_38
VCC_SM_39
VCC_SM_40
VCC_SM_41
VCC_SM_42
VCC_SM_43
VCC_SM_44
VCC_SM_45
VCC_SM_46
VCC_SM_47
VCC_SM_48
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VCC_SM_50
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VCC_SM_61
VCC_SM_62
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VCC_SM_64
VCC_SM_65
VCC_SM_66
VCC_SM_67
VCC_SM_68
VCC_SM_69
VCC_SM_70
VCC_SM_71
VCC_SM_72
VCC_SM_73
VCC_SM_74
VCC_SM_75
VCC_SM_76
VCC_SM_77
VCC_SM_78
VCC_SM_79
VCC_SM_80
VCC_SM_81
VCC_SM_82
VCC_SM_83
VCC_SM_84
VCC_SM_85
VCC_SM_86
VCC_SM_87
VCC_SM_88
VCC_SM_89
VCC_SM_90
VCC_SM_91
VCC_SM_92
VCC_SM_93
VCC_SM_94
VCC_SM_95
VCC_SM_96
VCC_SM_97
VCC_SM_98
VCC_SM_99
VCC_SM_100
VCC_SM_101
VCC_SM_102
VCC_SM_103
VCC_SM_104
VCC_SM_105
VCC_SM_106
VCC_SM_107
C1001
C1002
C1003
C1004
C1012
C1013
0.47UF/16V
GND
+1.8V
+VCCP_GMCH
U600G
VCC_NCTF0
VCC_NCTF1
VCC_NCTF2
VCC_NCTF3
VCC_NCTF4
VCC_NCTF5
VCC_NCTF6
VCC_NCTF7
VCC_NCTF8
VCC_NCTF9
VCC_NCTF10
VCC_NCTF11
VCC_NCTF12
VCC_NCTF13
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VCC_NCTF56
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VCC_NCTF69
VCC_NCTF70
VCC_NCTF71
VCC_NCTF72
VSS_NCTF0
VSS_NCTF1
VSS_NCTF2
VSS_NCTF3
VSS_NCTF4
VSS_NCTF5
VSS_NCTF6
VSS_NCTF7
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VSS_NCTF9
VSS_NCTF10
VSS_NCTF11
VSS_NCTF12
VCCAUX_NCTF0
VCCAUX_NCTF1
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VCCAUX_NCTF6
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VCCAUX_NCTF9
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VCCAUX_NCTF50
VCCAUX_NCTF51
VCCAUX_NCTF52
VCCAUX_NCTF53
VCCAUX_NCTF54
VCCAUX_NCTF55
VCCAUX_NCTF56
VCCAUX_NCTF57
NCTF
CALISTOGA_Q137
+1.5VS
VCC(GMCH Core)
+1.5VS (5500 mA) or +1.05VS (3500 mA)
1214
CE1000
CE1001
C1005
C1006
C1007
C1008
C1000
C1009
220uF/4V
220uF/4V
10UF/10V
10UF/10V
1UF/10V
0.22UF/6.3V
0.22UF/6.3V
0.22UF/6.3V
Layout Note:
Place in cavity
3200 mA
C1010
C1011
CE1002
CE1003
CE1004
10UF/10V
10UF/10V
330UF/2.5V
330UF/2.5V
330UF/2.5V
U600J
VSS_273
VSS_274
VSS_275
VSS_276
VSS_277
VSS_278
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CALISTOGA_Q137
U600I
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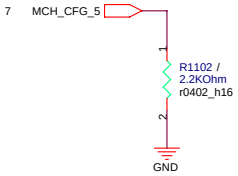
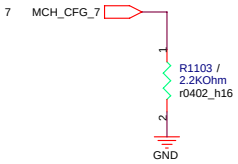
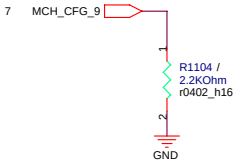
VSS_172
VSS_173
VSS_174
VSS_175
VSS_176
VSS_177
VSS_178
VSS_179
VSS
CALISTOGA_Q137
+1.5VS 9,20,26,36,42,52
+1.8V 7,14,15,36,53
+VCCP_GMCH 9,42
ASUSTeK COMPUTER INC
Title : Clistoga GND (5)
Engineer: Ping-Yen Tsai
Size Custom
Project Name A3F
Rev 2.0
Date: Wednesday, January 18, 2006
Sheet 10 of 63



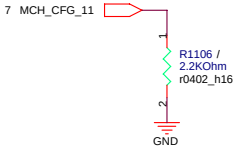
CFG5 : DMI X2 Select
LOW = DMI X 2
HIGH = DMI X 4 (Default)



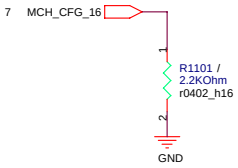
CFG7 : CPU STRAP
LOW = Reserved
HIGH = Mobility CPU (Default)



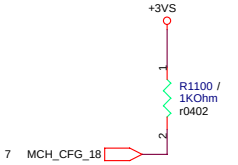
CFG9 : PCIE GRAPHIC LANE
LOW = REVERSE LANES
HIGH = NORMAL OPERATION (Default)



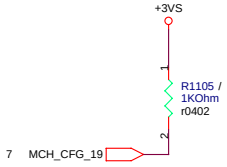
CFG11 : Reserved but need to be pull low



CFG16 : FSB DYNAMIC ODT
LOW = Dynamic ODT Disabled
HIGH = Dynamic ODT Enabled (Default)



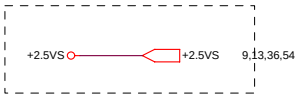
CFG18 : GMCH Core Voltage Level
LOW = 1.05V
HIGH = 1.5V (default)



CFG19 : DMI LANE REVERSAL
LOW = NORMAL
HIGH = LANES REVERSED

CFG[17..3] have internal pullup resistors.
CFG[19..18] have internal pulldown resistors.
SDVOCRTL_DATA has internal pulldown resistors.

CFG	All are sampled with respect to the leading edge of the GMCH PWROK	
2:0	FSB Freq select	001 = FSB533 011 = FSB667
4:3		
5	DMI X 2 Select	0 = DMI X 2 1 = DMI X 4 (Default)
6		
7	CPU Strap	0 = Reserved 1 = Mobile CPU (Default)
8		
9	PCIE Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal (Default)
11:10		
13:12	XOR/ALLZ	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal operation (Default)
15:14		
16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
17		
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card Present (Default) 1 = SDVO Card Present
18	VCC select	0 = 1.05V (Default) 1 = 1.5V
19	DMI Lane Reversal	0 = Normal (Default) 1 = Reverse Lanes
20	SDVO/PCIE concurrent	0 = Only SDVO or PCIE x1 is operational(Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port

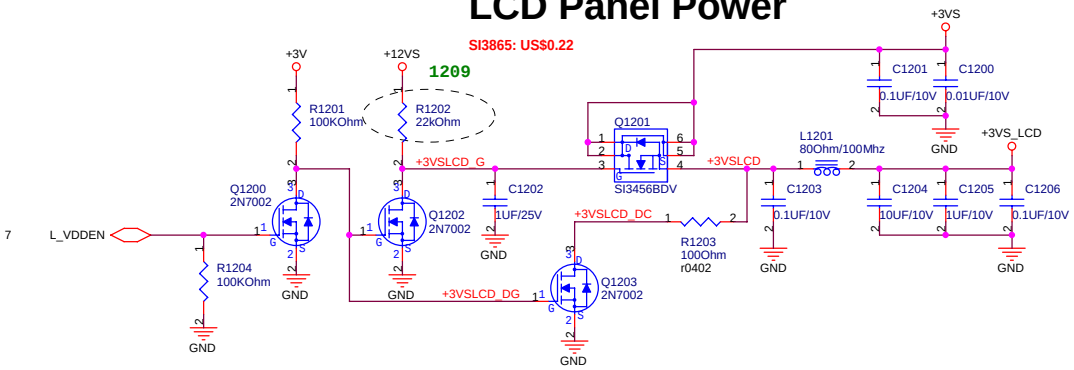


ASUSTeK COMPUTER INC
Title : Calistoga Strapping
Engineer: *Ping-Yen Tsai*
Size: Custom | Project Name: A3F | Rev: 2.0
Date: Wednesday, January 18, 2006 | Sheet 11 of 63

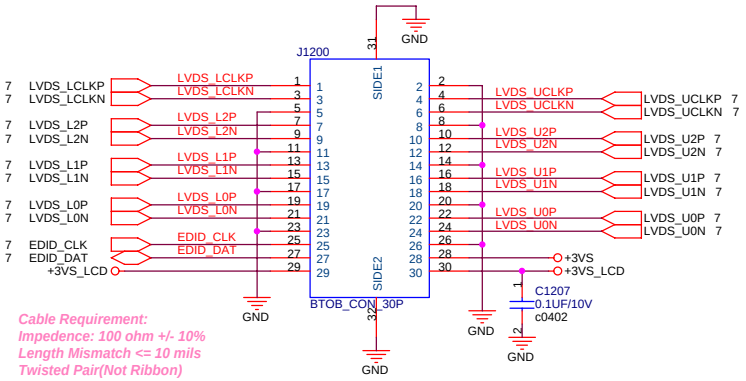
LCD Panel Power

3~3.6V
Full Active: 410 mA(Max. 500 mA)
3~3.6V
S0-S1 M: 410 mA(Max. 500 mA)

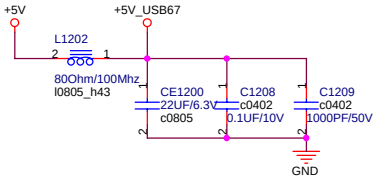
SI3865: US$0.22



LCD LVDS Interface



Cable Requirement:
Impedence: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"



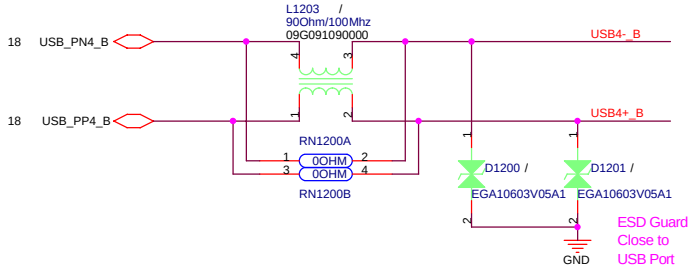
LCD Backlight Control

BIOS
LCD_BACKOFF#
When user push "Fn+F7" button
BIOS active this pin to turn On/Off backlight

EC
INVTER_DA:
EC output D/A signal (adjust voltage level) to adjust backlight

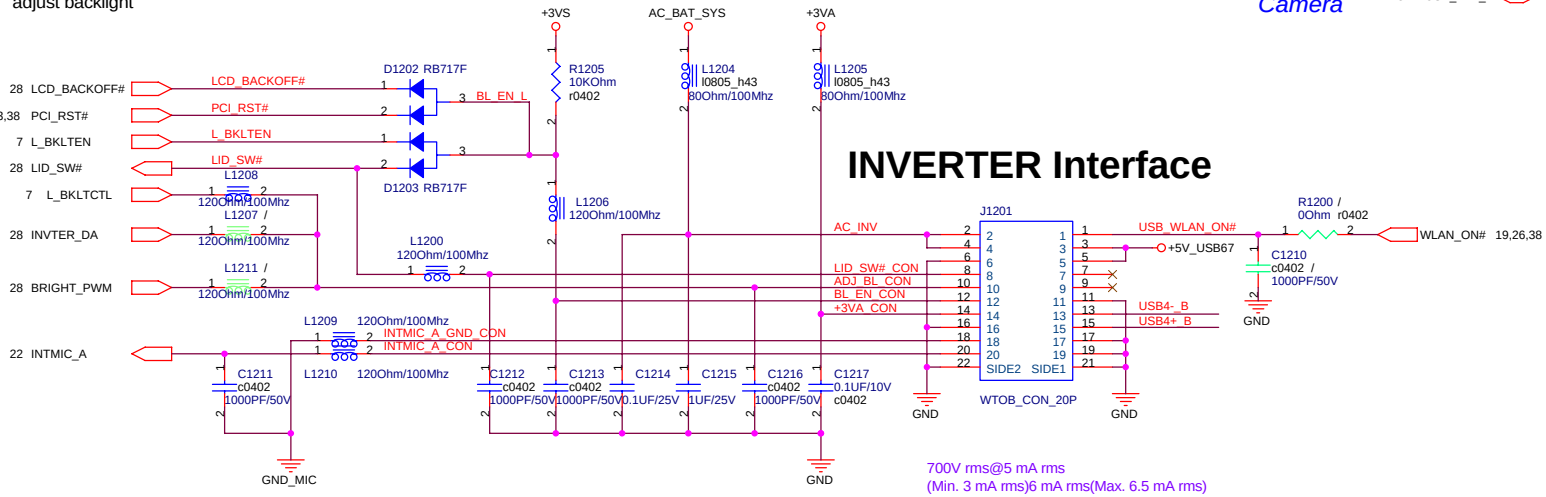
Inverter Board built in 14.1W LCD Panel

USB4 For CMOS Camera



ESD Guard Close to USB Port

INVERTER Interface



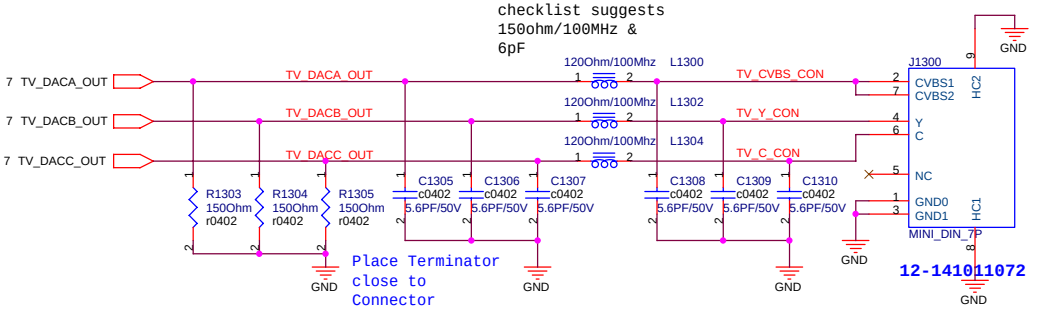
700V rms@5 mA rms
(Min. 3 mA rms)6 mA rms(Max. 6.5 mA rms)

ASUSTeK COMPUTER INC	Title : LVDS & INVERTER	
	Engineer: *Ping-Yen Tsai*	
Size: A3	Project Name: **A3F**	Rev: 2.0
Date: Wednesday, January 18, 2006	Sheet 12 of 63	

TV OUT

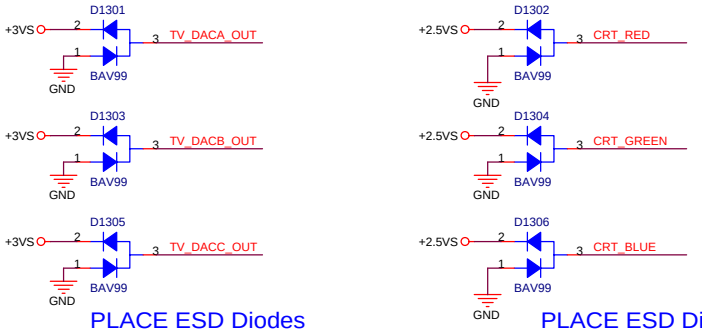
12G14101107D

checklist suggests
150ohm/100MHz &
6pF



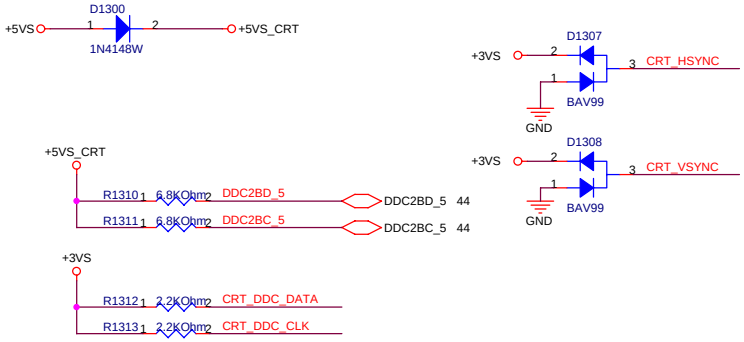
Place Terminator close to Connector

12-141011072



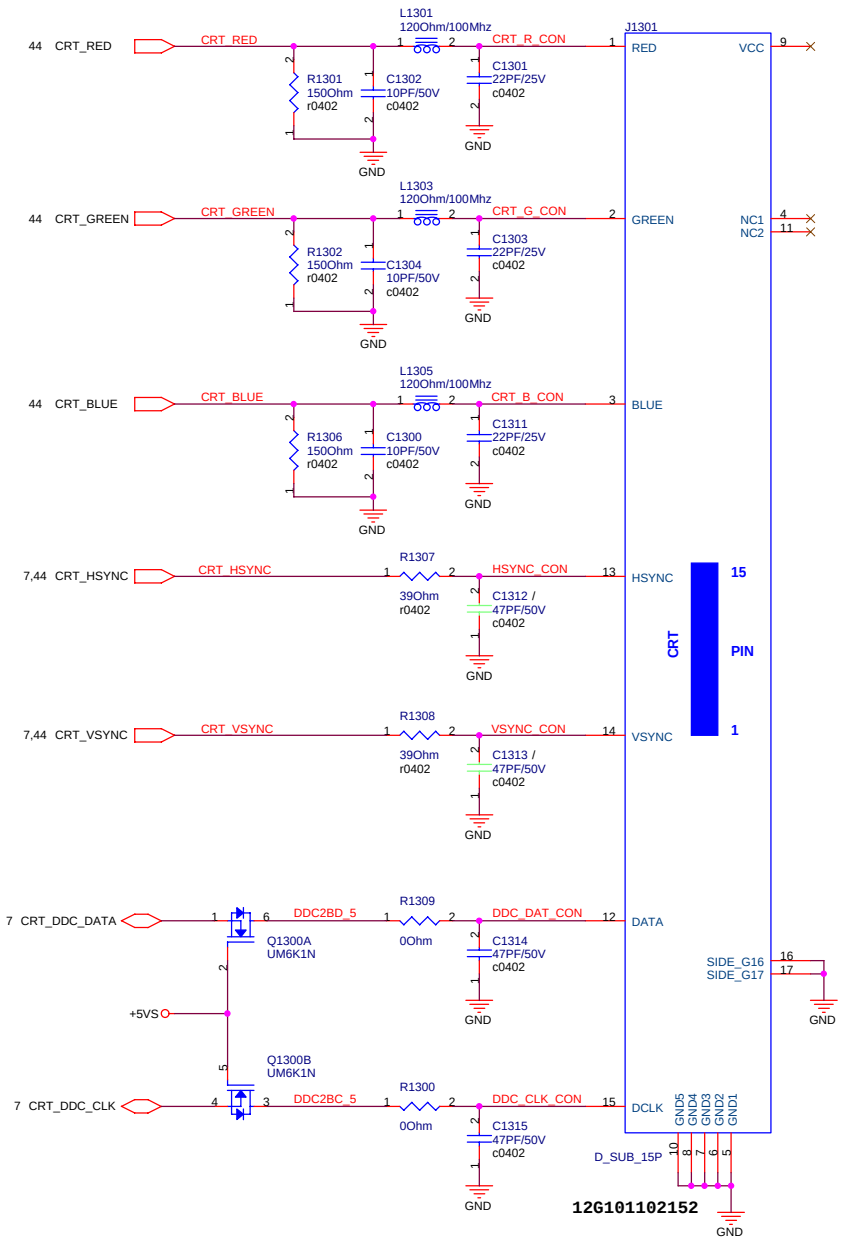
PLACE ESD Diodes near TV port

PLACE ESD Diodes near VGA port



CRT OUT

checklist suggests 47ohm/100MHz



12G101102152

ASUSTeK COMPUTER INC	Title : CRT & TV OUT	
	Engineer: *Ping-Yen Tsai*	
Size: A3	Project Name: **A3F**	Rev: 2.0
Date: Wednesday, January 18, 2006	Sheet 13 of 63	

8 M_B_DQ[0..63]

8,16 M_B_A[0..13]

U1400A

M_B_A0 102 A0
M_B_A1 101 A1
M_B_A2 100 A2
M_B_A3 99 A3
M_B_A4 98 A4
M_B_A5 97 A5
M_B_A6 94 A6
M_B_A7 92 A7
M_B_A8 93 A8
M_B_A9 91 A9
M_B_A10 105 A10/AP
M_B_A11 90 A11
M_B_A12 89 A12
M_B_A13 116 A13
86 A14
84 A15
M_B_BS#2 85 A16_BA2

8,16 M_B_BS#2

M_B_BS#0 107 BA0
M_B_BS#1 106 BA1
M_CS#2 110 S0#
M_CS#3 115 S1#
M_CLK_DDR3 30 CK0
M_CLK_DDR#3 32 CK0#
M_CLK_DDR2 164 CK1
M_CLK_DDR#2 166 CK1#
M_CKE2 79 CKE0
M_CKE3 80 CKE1
M_CAS# 113 CAS#
M_RAS# 108 RAS#
M_WE# 109 WE#
198 SA0
200 SA1
SMB_CLK_S 197 SCL
SMB_DAT_S 195 SDA

8,16 M_B_BS#0
8,16 M_B_BS#1
7,16 M_CS#2
7,16 M_CS#3
7 M_CLK_DDR3
7 M_CLK_DDR#3
7 M_CLK_DDR2
7 M_CLK_DDR#2
7,16 M_CKE2
7,16 M_CKE3
8,16 M_CAS#
8,16 M_B_RAS#
8,16 M_B_WE#

11/14

+3VS — 1 R1401 2 — r0402 10KOhm

GND

5,15,19,26 SMB_CLK_S
5,15,19,26 SMB_DAT_S

7,16 M_ODT2
7,16 M_ODT3

M_ODT2 114 ODT0
M_ODT3 119 ODT1

For Data Swap

M_B_DM0 10 DM0
M_B_DM1 26 DM1
M_B_DM2 52 DM2
M_B_DM3 67 DM3
M_B_DM4 130 DM4
M_B_DM5 147 DM5
M_B_DM6 170 DM6
M_B_DM7 185 DM7

M_B_DQS0 13 DQS0
M_B_DQS1 31 DQS1
M_B_DQS2 51 DQS2
M_B_DQS3 70 DQS3
M_B_DQS4 131 DQS4
M_B_DQS5 148 DQS5
M_B_DQS6 169 DQS6
M_B_DQS7 188 DQS7
M_B_DQS#0 11 DQS#0
M_B_DQS#1 29 DQS#1
M_B_DQS#2 49 DQS#2
M_B_DQS#3 68 DQS#3
M_B_DQS#4 129 DQS#4
M_B_DQS#5 146 DQS#5
M_B_DQS#6 167 DQS#6
M_B_DQS#7 186 DQS#7

DQ0 5 M_B_DQ1
DQ1 7 M_B_DQ5
DQ2 17 M_B_DQ2
DQ3 19 M_B_DQ3
DQ4 4 M_B_DQ4
DQ5 6 M_B_DQ0
DQ6 14 M_B_DQ6
DQ7 16 M_B_DQ7
DQ8 23 M_B_DQ8
DQ9 25 M_B_DQ12
DQ10 35 M_B_DQ9
DQ11 37 M_B_DQ11
DQ12 20 M_B_DQ13
DQ13 22 M_B_DQ10
DQ14 36 M_B_DQ14
DQ15 38 M_B_DQ15
DQ16 43 M_B_DQ20
DQ17 45 M_B_DQ17
DQ18 55 M_B_DQ23
DQ19 57 M_B_DQ22
DQ20 44 M_B_DQ21
DQ21 46 M_B_DQ16
DQ22 56 M_B_DQ19
DQ23 58 M_B_DQ18
DQ24 61 M_B_DQ29
DQ25 63 M_B_DQ28
DQ26 73 M_B_DQ27
DQ27 75 M_B_DQ30
DQ28 62 M_B_DQ24
DQ29 64 M_B_DQ25
DQ30 74 M_B_DQ26
DQ31 76 M_B_DQ31
DQ32 123 M_B_DQ32
DQ33 125 M_B_DQ36
DQ34 135 M_B_DQ38
DQ35 137 M_B_DQ35
DQ36 124 M_B_DQ33
DQ37 126 M_B_DQ37
DQ38 134 M_B_DQ39
DQ39 136 M_B_DQ34
DQ40 141 M_B_DQ40
DQ41 143 M_B_DQ41
DQ42 151 M_B_DQ47
DQ43 153 M_B_DQ42
DQ44 140 M_B_DQ44
DQ45 142 M_B_DQ45
DQ46 152 M_B_DQ43
DQ47 154 M_B_DQ46
DQ48 157 M_B_DQ53
DQ49 159 M_B_DQ48
DQ50 173 M_B_DQ50
DQ51 175 M_B_DQ51
DQ52 158 M_B_DQ52
DQ53 160 M_B_DQ49
DQ54 174 M_B_DQ55
DQ55 176 M_B_DQ54
DQ56 179 M_B_DQ56
DQ57 181 M_B_DQ60
DQ58 189 M_B_DQ58
DQ59 191 M_B_DQ59
DQ60 180 M_B_DQ57
DQ61 182 M_B_DQ61
DQ62 192 M_B_DQ62
DQ63 194 M_B_DQ63

DDR_DIMM_200P_A
12G025122007

Group0 Group1 Group2 Group3 Group4 Group5 Group6 Group7

8 M_B_DM[0..7]
8 M_B_DQS[0..7]
8 M_B_DQS#[0..7]

M_VREF_DIMM1 — M_VREF_DIMM1 7,15,16
+1.8V — +1.8V 7,10,15,36,53
+3VS — +3VS 4,5,7,9,11,12,13,15,19,20,21,22,25,26,27,28,30,36,38,39,42,50,52,60,61

+1.8V
C1401 C1402 C1403 C1400
0.1UF/10V 0.1UF/10V 0.1UF/10V 0.1UF/10V
GND

Layout Note:
Place these resistors
near the GMCH

+3VS
C1404 2.2UF/6.3V
C1405 0.1UF/10V
GND GND

M_VREF_DIMM1
VREF -> 10/10 mils
C1406 2.2UF/6.3V
C1407 0.1UF/10V
GND GND

+1.8V
Layout Note:
Place these Caps near SO DIMM 1
C1408 C1411 C1409 C1410
0.1UF/10V 0.1UF/10V 0.1UF/10V 0.1UF/10V
GND

+1.8V
Layout Note:
Place these Caps near SO DIMM 1
C1412 C1413 C1414 C1415 C1416
2.2UF/6.3V 2.2UF/6.3V 2.2UF/6.3V 2.2UF/6.3V 2.2UF/6.3V
GND

+1.8V

U1400B

112	VDD1	VSS16	18
111	VDD2	VSS17	24
117	VDD3	VSS18	41
96	VDD4	VSS19	53
95	VDD5	VSS20	42
118	VDD6	VSS21	54
81	VDD7	VSS22	59
82	VDD8	VSS23	65
87	VDD9	VSS24	60
103	VDD10	VSS25	66
88	VDD11	VSS26	127
104	VDD12	VSS27	139
		VSS28	128
199	VDDSPD	VSS29	145
		VSS30	165
83	NC1	VSS31	171
120	NC2	VSS32	172
50	NC3	VSS33	177
69	NC4	VSS34	187
163	NCTEST	VSS35	178
		VSS36	190
1	VREF	VSS37	9
		VSS38	21
201	GND0	VSS39	33
202	GND1	VSS40	155
		VSS41	34
203	NP_NC1	VSS42	132
204	NP_NC2	VSS43	144
		VSS44	156
47	VSS1	VSS45	168
133	VSS2	VSS46	2
183	VSS3	VSS47	3
77	VSS4	VSS48	15
12	VSS5	VSS49	27
48	VSS6	VSS50	39
184	VSS7	VSS51	149
78	VSS8	VSS52	161
71	VSS9	VSS53	28
72	VSS10	VSS54	40
121	VSS11	VSS55	138
122	VSS12	VSS56	150
196	VSS13	VSS57	162
193	VSS14		
8	VSS15		

GND GND

DDR_DIMM_200P_A
12G025122007

ASUSTeK COMPUTER INC	Title : DDR2_SO-DIMM(1)		
	Engineer: Ping-Yen Tsai		
Size: A4	Project Name: A3F		Rev: 2.0
Date: Wednesday, January 18, 2006	Sheet 14 of 63		

Green Part Number:12G025122006
Green Part Number:12-025122006

8 M_A_DQ[0..63]
8,16 M_A_A[0..13]

J1500A

M_A_A0	102	A0		DQ0	5	M_A_DQ5	
M_A_A1	101	A1		DQ1	7	M_A_DQ4	
M_A_A2	100	A2		DQ2	17	M_A_DQ2	
M_A_A3	99	A3		DQ3	19	M_A_DQ3	
M_A_A4	98	A4		DQ4	4	M_A_DQ1	
M_A_A5	97	A5		DQ5	6	M_A_DQ0	
M_A_A6	94	A6		DQ6	14	M_A_DQ6	
M_A_A7	92	A7		DQ7	16	M_A_DQ7	
M_A_A8	93	A8		DQ8	23	M_A_DQ13	
M_A_A9	91	A9		DQ9	25	M_A_DQ8	
M_A_A10	105	A10/AP		DQ10	35	M_A_DQ10	
M_A_A11	90	A11	Group1	DQ11	37	M_A_DQ11	
M_A_A12	89	A12		DQ12	20	M_A_DQ12	
M_A_A13	116	A13		DQ13	22	M_A_DQ14	
	86	A14		DQ14	36	M_A_DQ15	
	84	A15		DQ15	38	M_A_DQ9	
M_A_BS#2	85	A16_BA2		DQ16	43	M_A_DQ16	
				DQ17	45	M_A_DQ21	
M_A_BS#0	107	BA0		DQ18	55	M_A_DQ23	
M_A_BS#1	106	BA1		DQ19	57	M_A_DQ19	
M_CS#0	110	S0#	Group2	DQ20	44	M_A_DQ20	
M_CS#1	115	S1#		DQ21	46	M_A_DQ17	
M_CLK_DDR0	30	CK0		DQ22	56	M_A_DQ18	
M_CLK_DDR#0	32	CK0#		DQ23	58	M_A_DQ22	
M_CLK_DDR1	164	CK1		DQ24	61	M_A_DQ24	
M_CLK_DDR#1	166	CK1#		DQ25	63	M_A_DQ25	
M_CKE0	79	CKE0		DQ26	73	M_A_DQ26	
M_CKE1	80	CKE1		DQ27	75	M_A_DQ27	
M_A_CAS#	113	CAS#	Group3	DQ28	62	M_A_DQ28	
M_A_RAS#	108	RAS#		DQ29	64	M_A_DQ29	
M_A_WE#	109	WE#		DQ30	74	M_A_DQ30	
	198	SA0		DQ31	76	M_A_DQ31	
	200	SA1		DQ32	123	M_A_DQ36	
SMB_CLK_S	197	SCL		DQ33	125	M_A_DQ37	
SMB_DAT_S	195	SDA		DQ34	135	M_A_DQ35	
				DQ35	137	M_A_DQ34	
M_ODT0	114	ODT0		DQ36	124	M_A_DQ32	
M_ODT1	119	ODT1	Group4	DQ37	126	M_A_DQ33	
				DQ38	134	M_A_DQ39	
M_A_DM0	10	DM0		DQ39	136	M_A_DQ38	
M_A_DM1	26	DM1		DQ40	141	M_A_DQ45	
M_A_DM2	52	DM2		DQ41	143	M_A_DQ41	
M_A_DM3	67	DM3		DQ42	151	M_A_DQ47	
M_A_DM4	130	DM4		DQ43	153	M_A_DQ46	
M_A_DM5	147	DM5	Group5	DQ44	140	M_A_DQ44	
M_A_DM6	170	DM6		DQ45	142	M_A_DQ40	
M_A_DM7	185	DM7		DQ46	152	M_A_DQ43	
				DQ47	154	M_A_DQ42	
M_A_DQS0	13	DQS0		DQ48	157	M_A_DQ48	
M_A_DQS1	31	DQS1		DQ49	159	M_A_DQ49	
M_A_DQS2	51	DQS2		DQ50	173	M_A_DQ50	
M_A_DQS3	70	DQS3		DQ51	175	M_A_DQ51	
M_A_DQS4	131	DQS4		DQ52	158	M_A_DQ53	
M_A_DQS5	148	DQS5	Group6	DQ53	160	M_A_DQ52	
M_A_DQS6	169	DQS6		DQ54	174	M_A_DQ54	
M_A_DQS7	188	DQS7		DQ55	176	M_A_DQ55	
M_A_DQS#0	11	DQS#0		DQ56	179	M_A_DQ60	
M_A_DQS#1	29	DQS#1		DQ57	181	M_A_DQ56	
M_A_DQS#2	49	DQS#2		DQ58	189	M_A_DQ63	
M_A_DQS#3	68	DQS#3		DQ59	191	M_A_DQ59	
M_A_DQS#4	129	DQS#4	Group7	DQ60	180	M_A_DQ61	
M_A_DQS#5	146	DQS#5		DQ61	182	M_A_DQ57	
M_A_DQS#6	167	DQS#6		DQ62	192	M_A_DQ58	
M_A_DQS#7	186	DQS#7		DQ63	194	M_A_DQ62	

DDR2_DIMM_200P_REV

GND

For Data Swap

7,16 M_ODT0
7,16 M_ODT1

5,14,19,26 SMB_CLK_S
5,14,19,26 SMB_DAT_S

8,16 M_A_BS#2

8,16 M_A_BS#0
8,16 M_A_BS#1
7,16 M_CS#0
7,16 M_CS#1
7 M_CLK_DDR0
7 M_CLK_DDR#0
7 M_CLK_DDR1
7 M_CLK_DDR#1
7,16 M_CKE0
7,16 M_CKE1
8,16 M_A_CAS#
8,16 M_A_RAS#
8,16 M_A_WE#

8 M_A_DM[0..7]
8 M_A_DQS[0..7]
8 M_A_DQS#[0..7]

GMCH=====>SODIMM1=>SODIMM0

+1.8V → +1.8V 7,10,14,36,53
+3VS → +3VS 4,5,7,9,11,12,13,14,19,20,21,22,25,26,27,28,30,36,38,39,42,50,52,60,61
M_VREF_DIMM0 → M_VREF_DIMM0 7,14,16

J1500B

112	VDD1	VSS16	18
111	VDD2	VSS17	24
117	VDD3	VSS18	41
96	VDD4	VSS19	53
95	VDD5	VSS20	42
118	VDD6	VSS21	54
81	VDD7	VSS22	59
82	VDD8	VSS23	65
87	VDD9	VSS24	60
103	VDD10	VSS25	66
88	VDD11	VSS26	127
104	VDD12	VSS27	139
		VSS28	128
199	VDDSPD	VSS29	145
		VSS30	165
83	NC1	VSS31	171
120	NC2	VSS32	172
50	NC3	VSS33	177
69	NC4	VSS34	187
163	NCTEST	VSS35	178
		VSS36	190
1	VREF	VSS37	9
		VSS38	21
201	GND0	VSS39	33
202	GND1	VSS40	155
		VSS41	34
203	NP_NC1	VSS42	132
204	NP_NC2	VSS43	144
		VSS44	156
47	VSS1	VSS45	168
133	VSS2	VSS46	2
183	VSS3	VSS47	3
77	VSS4	VSS48	15
12	VSS5	VSS49	27
48	VSS6	VSS50	39
184	VSS7	VSS51	149
78	VSS8	VSS52	161
71	VSS9	VSS53	28
72	VSS10	VSS54	40
121	VSS11	VSS55	138
122	VSS12	VSS56	150
196	VSS13	VSS57	162
193	VSS14		
8	VSS15		

DDR2_DIMM_200P_REV

+1.8V
+3VS
C1501 2.2UF/6.3V
C1502 0.1UF/10V
GND

M_VREF_DIMM0
VREF -> 10/10 mils
C1503 2.2UF/6.3V
C1504 0.1UF/10V
GND

+1.8V
Layout Note:
Place these Caps near SO DIMM 0
C1500 0.1UF/10V
C1505 0.1UF/10V
C1506 0.1UF/10V
C1507 0.1UF/10V
GND

+1.8V
Layout Note:
Place these Caps near SO DIMM 0
C1508 2.2UF/6.3V
C1509 2.2UF/6.3V
C1510 2.2UF/6.3V
C1511 2.2UF/6.3V
C1512 2.2UF/6.3V
GND

ASUSTeK COMPUTER INC

Title : DDR2 SO-DIMM(0)

Engineer: Ping-Yen Tsai

Size	Project Name	Rev
A4	A3F	2.0

Date: Wednesday, January 18, 2006 Sheet 15 of 63

+0.9VS

NEED TO SWAP

1	56Ohm	16	RN1601A	M_CKE2
2	56Ohm	15	RN1601B	M_B_BS#2
3	56Ohm	14	RN1601C	M_B_A12
4	56Ohm	13	RN1601D	M_B_A9
5	56Ohm	12	RN1601E	M_CKE3
6	56Ohm	11	RN1601F	M_B_A8
7	56Ohm	10	RN1601G	M_B_A7
8	56Ohm	9	RN1601H	M_B_A11
1	56Ohm	16	RN1602A	M_B_A5
2	56Ohm	15	RN1602B	M_B_A3
3	56Ohm	14	RN1602C	M_B_A6
4	56Ohm	13	RN1602D	M_B_A4
5	56Ohm	12	RN1602E	M_B_A1
6	56Ohm	11	RN1602F	M_B_A2
7	56Ohm	10	RN1602G	M_B_A0
8	56Ohm	9	RN1602H	M_B_BS#1
1	56Ohm	16	RN1603A	M_B_RAS#
2	56Ohm	15	RN1603B	M_B_A10
3	56Ohm	14	RN1603C	M_ODT2
4	56Ohm	13	RN1603D	M_B_A13
5	56Ohm	12	RN1603E	M_CS#2
6	56Ohm	11	RN1603F	M_B_CAS#
7	56Ohm	10	RN1603G	M_B_BS#0
8	56Ohm	9	RN1603H	M_B_WE#
1	56Ohm	2	RN1604A	
3	56Ohm	4	RN1604B	
5	56Ohm	6	RN1604C	M_CS#3
7	56Ohm	8	RN1604D	M_ODT3
1	56Ohm	16	RN1605A	M_A_A4
2	56Ohm	15	RN1605B	M_A_A11
3	56Ohm	14	RN1605C	M_A_A7
4	56Ohm	13	RN1605D	M_A_A9
5	56Ohm	12	RN1605E	M_A_A12
6	56Ohm	11	RN1605F	M_A_BS#2
7	56Ohm	10	RN1605G	M_CKE1
8	56Ohm	9	RN1605H	M_CKE0
1	56Ohm	16	RN1606A	
2	56Ohm	15	RN1606B	
3	56Ohm	14	RN1606C	M_A_BS#0
4	56Ohm	13	RN1606D	M_A_A10
5	56Ohm	12	RN1606E	M_A_A0
6	56Ohm	11	RN1606F	M_A_A6
7	56Ohm	10	RN1606G	M_A_A5
8	56Ohm	9	RN1606H	M_A_A8
1	56Ohm	16	RN1607A	M_A_A13
2	56Ohm	15	RN1607B	M_A_RAS#
3	56Ohm	14	RN1607C	M_A_BS#1
4	56Ohm	13	RN1607D	M_A_A2
5	56Ohm	12	RN1607E	M_A_CAS#
6	56Ohm	11	RN1607F	M_A_WE#
7	56Ohm	10	RN1607G	M_A_A3
8	56Ohm	9	RN1607H	M_A_A1
1	56Ohm	2	RN1608A	M_ODT0
3	56Ohm	4	RN1608B	M_CS#0
5	56Ohm	6	RN1608C	M_CS#1
7	56Ohm	8	RN1608D	M_ODT1

M_A_A[0..13] 8,15
M_A_BS#[0..2] 8,15
M_A_CAS# 8,15
M_A_RAS# 8,15
M_A_WE# 8,15

M_B_A[0..13] 8,14
M_B_BS#[0..2] 8,14
M_B_CAS# 8,14
M_B_RAS# 8,14
M_B_WE# 8,14

M_CS#[0..3] 7,14,15
M_ODT[0..3] 7,14,15
M_CKE[0..3] 7,14,15

M_VREF_DIMM0 → M_VREF_DIMM0 7,14,15
M_VREF_DIMM1 → M_VREF_DIMM1 7,14,15
M_VREF_MCH → M_VREF_MCH 7,14,15
+0.9VS → +0.9VS 36,53

+0.9VS
L1600 (1, 2) 120Ohm/100Mhz
→ M_VREF_DIMM1
→ M_VREF_MCH
→ M_VREF_DIMM0

+0.9VS

C1601	C1602	C1603	C1604	C1605	C1606	C1607	C1608	C1609	C1610	C1600	C1611	C1612
c0402	c0402	c0402	c0402	c0402	c0402	c0402	c0402	c0402	c0402	c0402	c0402	c0402
0.1UF/10V	0.1UF/10V	0.1UF/10V	0.1UF/10V	0.1UF/10V	0.1UF/10V	0.1UF/10V	0.1UF/10V	0.1UF/10V	0.1UF/10V	0.1UF/10V	0.1UF/10V	0.1UF/10V

GND

Layout note:
Place one cap close to every 2 pull-up resistors terminated to +0.9VS

+0.9VS

C1613	C1614	C1615	C1616	C1617	C1618	C1619	C1620	C1621	C1622	C1623	C1624	C1625
c0402	c0402	c0402	c0402	c0402	c0402	c0402	c0402	c0402	c0402	c0402	c0402	c0402
0.1UF/10V	0.1UF/10V	0.1UF/10V	0.1UF/10V	0.1UF/10V	0.1UF/10V	0.1UF/10V	0.1UF/10V	0.1UF/10V	0.1UF/10V	0.1UF/10V	0.1UF/10V	0.1UF/10V

GND

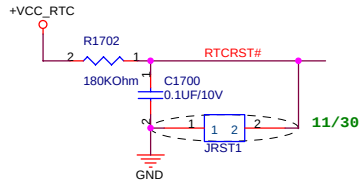
ASUSTeK COMPUTER INC

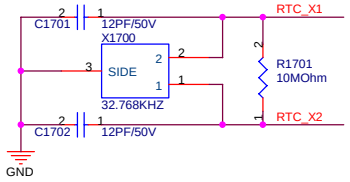
Title : DDR2 TERM

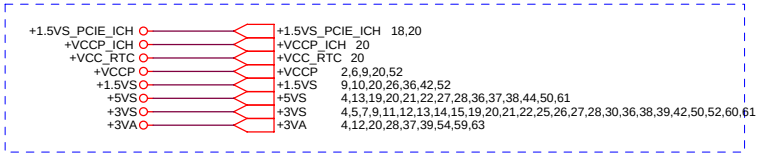
Engineer: *Ping-Yen Tsai*

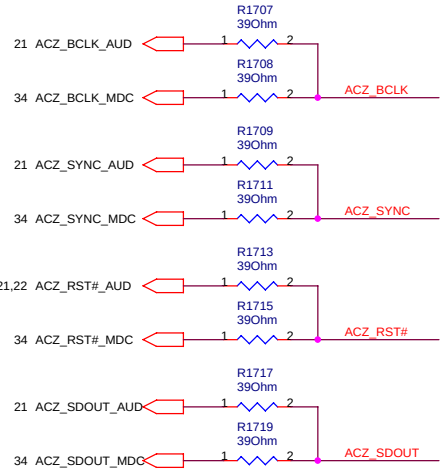
Size	Project Name	Rev
A4	A3F	2.0

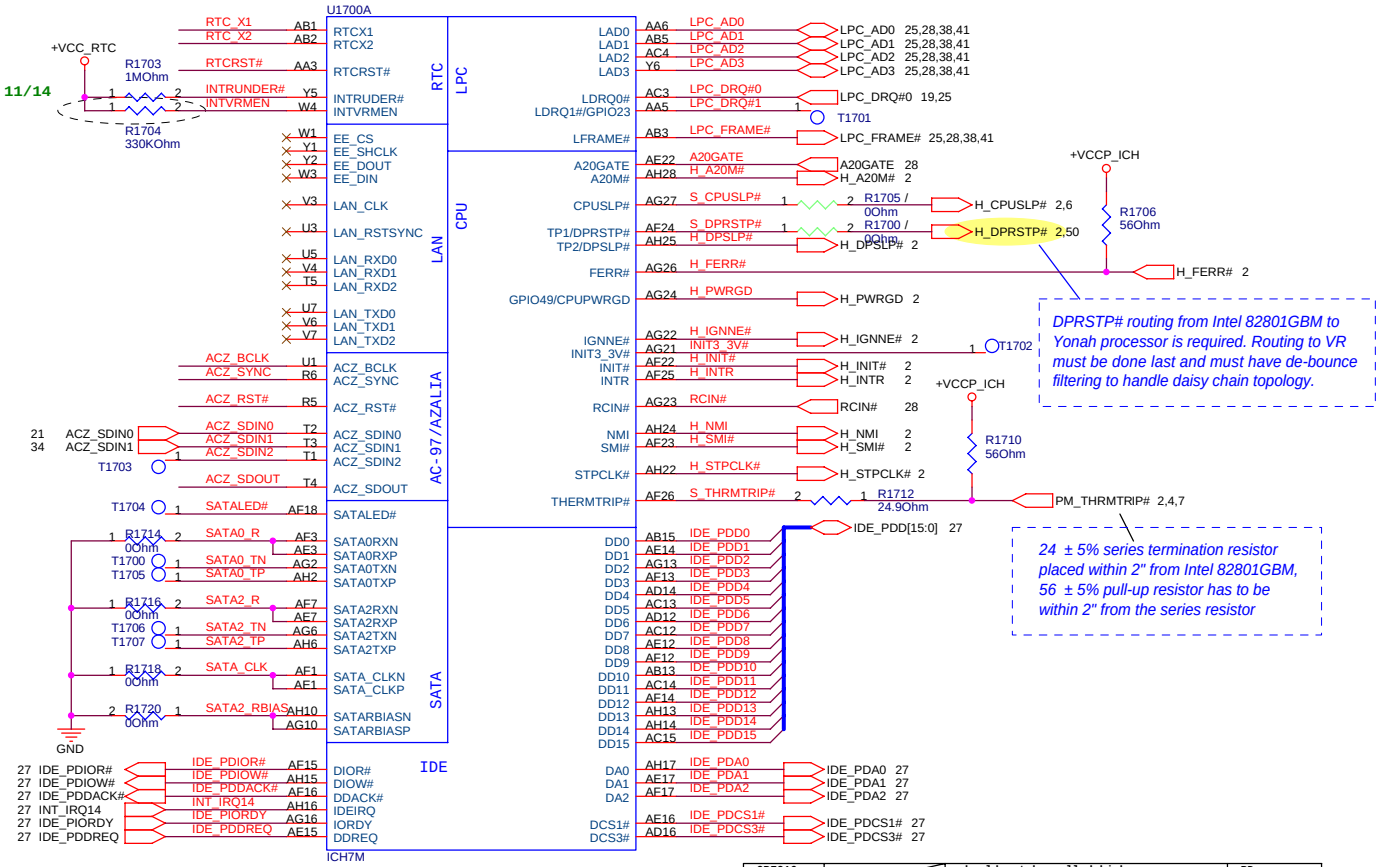
Date: Wednesday, January 18, 2006 Sheet 16 of 63











DPRSTP# routing from Intel 82801GBM to Yonah processor is required. Routing to VR must be done last and must have de-bounce filtering to handle daisy chain topology.

24 ± 5% series termination resistor placed within 2" from Intel 82801GBM, 56 ± 5% pull-up resistor has to be within 2" from the series resistor

ACZ_SDOUT	PWROK rising	TP3 pull low: allow entrance to XOR Chain testing TP3 not pull low: sets bit 1 of RPC.PC	PD
ACZ_SYNC	PWROK rising	sets bit 0 of RPC.PC	PD
EE_CS		should not be pulled high	PD
EE_DOUT		should not be pulled low	PU
GNT2#		should not be pulled low	PU
GNT3#	PWROK rising	low: "top-block swap" mode	PU
GNT5#/GPIO17# GNT4#/GPIO48	PWROK rising	GNT5# GNT4# 0 1 SPI 1 0 PCI 1 1 LPC	PU

GPIO16 /DPRSLPVR		should not be pulled high	PD
GPIO25	RSMRST# rising	should not be pulled low	PU
INTVRMEN	ALWAYS	high: Enable integrated VccSus1_05 VRM	
LINKALERT#		REQUIRE an extenal pull-up R	Need PU
REQ[4:1]#	PWROK rising		
SATALED#		should not be pulled low	Conditional PU
SPKR	PWROK rising	high: "No reboot" mode	PD
TP3	PWROK rising	should not be pulled low unless using XOR Chain testing	PU

Title : ICH7-M (1/4)

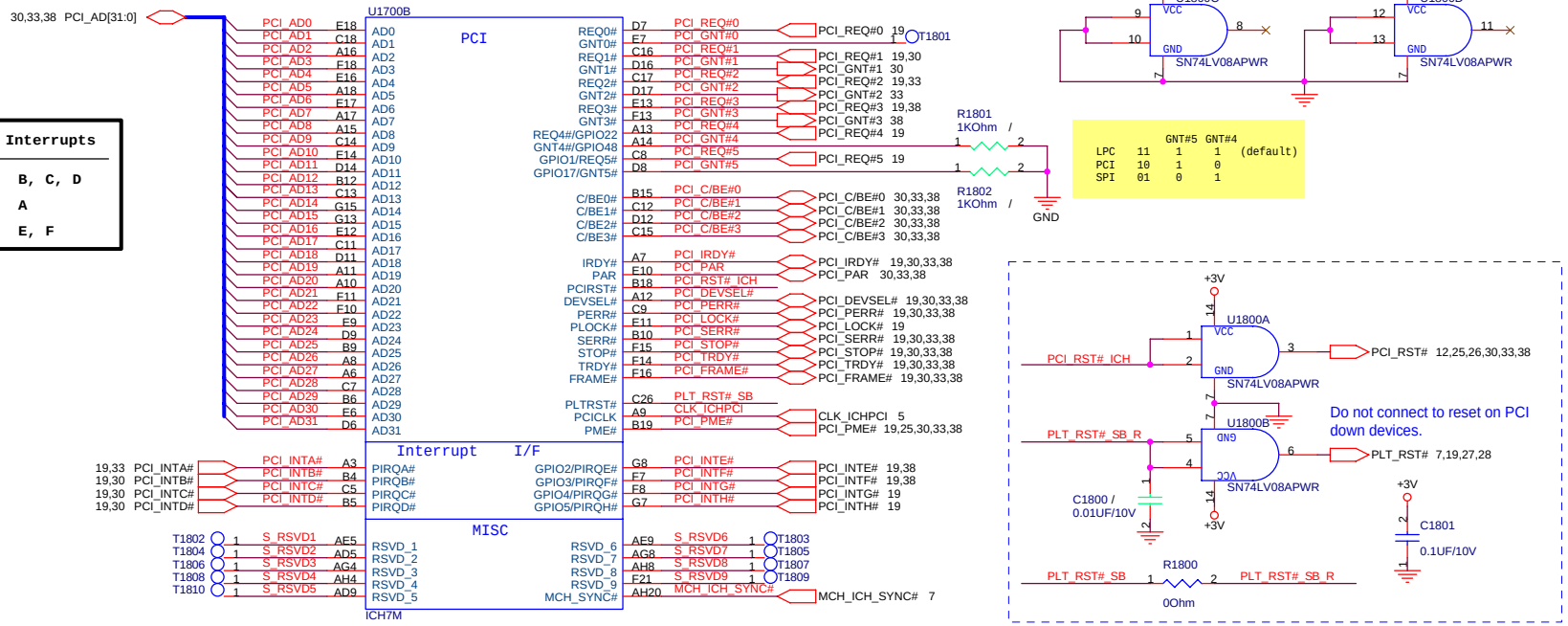
ASUSTeK COMPUTER INC Engineer: Ping-Yen Tsai

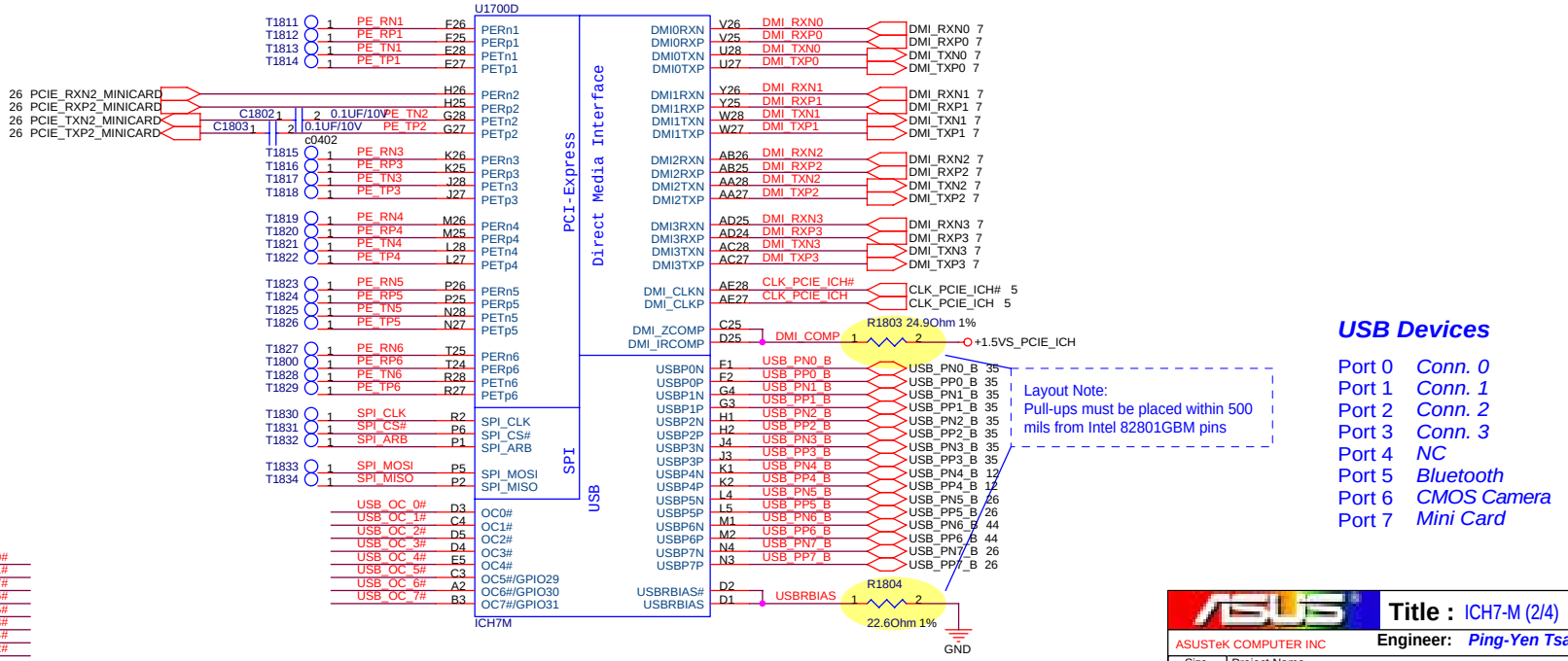
Size	Project Name	Rev
Custom	A3F	2.0

Date: Wednesday, January 18, 2006 Sheet 17 of 63

PCI Device

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus	AD17	REQ1#/GNT1#	B, C, D
LAN	AD23	REQ2#/GNT2#	A
Mini-PCI	AD19	REQ3#/GNT3#	E, F



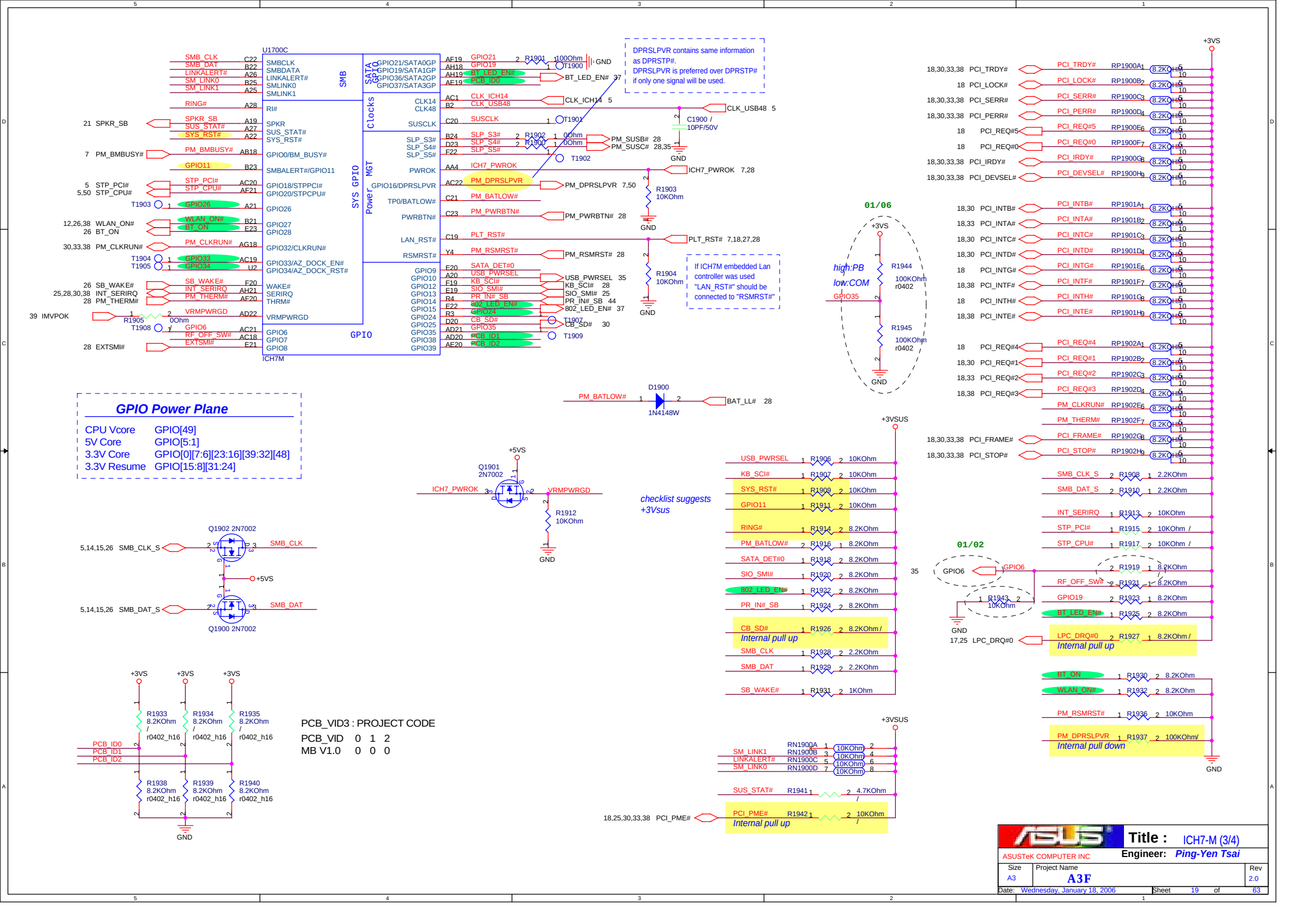


Layout Note:
Pull-ups must be placed within 500 mils from Intel 82801GBM pins

USB Devices

Port 0	Conn. 0
Port 1	Conn. 1
Port 2	Conn. 2
Port 3	Conn. 3
Port 4	NC
Port 5	Bluetooth
Port 6	CMOS Camera
Port 7	Mini Card

ASUSTeK COMPUTER INC	Title : ICH7-M (2/4)	
	Engineer: Ping-Yen Tsai	
Size: Custom	Project Name: A3F	Rev: 2.0
Date: Wednesday, January 18, 2006	Sheet 18 of 63	


U1700C
SMB
SATA
CLOCKS
SYS GPIO
MGT
Power
GPIO
ICH7M
SMB_CLK
SMB_DAT
LINKALERT#
SM_LINK0
SM_LINK1
SMBCLK
SMBDATA
LINKALERT#
SMLINK0
SMLINK1
RING#
SPKR_SB
SUS_STAT#
SYS_RST#
PM_BMBUSY#
GPIO11
STP_PCI#
STP_CPU#
GPIO26
WLAN_ON#
BT_ON
PM_CLKRUN#
GPIO33
GPIO34
SB_WAKE#
INT_SERIRQ
PM_THERM#
VRMPWRGD
GPIO6
RF_OFF_SW#
EXTSMI#
RI#
SPKR
SUS_STAT#
SYS_RST#
GPIO0/BM_BUSY#
SMBALERT#/GPIO11
GPIO18/STPPCI#
GPIO20/STPCPU#
GPIO26
GPIO27
GPIO28
GPIO32/CLKRUN#
GPIO33/AZ_DOCK_EN#
GPIO34/AZ_DOCK_RST#
WAKE#
SERIRQ
THRM#
VRMPWRGD
GPIO6
GPIO7
GPIO8
GPIO21/SATA0GP
GPIO19/SATA1GP
GPIO36/SATA2GP
GPIO37/SATA3GP
CLK14
CLK48
SUSCLK
SLP_S3#
SLP_S4#
SLP_S5#
PWROK
GPIO16/DPRSLPVR
TP0/BATLOW#
PWRBTN#
LAN_RST#
RSMRST#
GPIO9
GPIO10
GPIO12
GPIO13
GPIO14
GPIO15
GPIO24
GPIO25
GPIO35
GPIO38
GPIO39
GPIO21
GPIO19
BT_LED_EN#
PCB_ID0
CLK_ICH14
CLK_USB48
SUSCLK
SLP_S3#
SLP_S4#
SLP_S5#
ICH7_PWROK
PM_DPRSLPVR
PM_BATLOW#
PM_PWRBTN#
PLT_RST#
PM_RSMRST#
SATA_DET#0
USB_PWRSEL
KB_SCI#
SIO_SMI#
PR_IN#_SB
802_LED_EN#
GPIO24
CB_SD#
GPIO35
PCB_ID1
PCB_ID2
R1901 100Ohm
R1902 0Ohm
R1900 0Ohm
PM_SUSB# 28
PM_SUSC# 28,35
C1900 / 10PF/50V
R1903 10KOhm
R1904 10KOhm
T1900
T1901
T1902
T1907
T1909
BT_LED_EN# 37
CLK_ICH14 5
CLK_USB48 5
ICH7_PWROK 7,28
PM_DPRSLPVR 7,50
PM_PWRBTN# 28
PLT_RST# 7,18,27,28
PM_RSMRST# 28
USB_PWRSEL 35
KB_SCI# 28
SIO_SMI# 25
PR_IN# SB 44
802_LED_EN# 37
CB_SD# 30
GND
DPRSLPVR contains same information as DPRSTP#.
DPRSLPVR is preferred over DPRSTP# if only one signal will be used.
If ICH7M embedded Lan controller was used "LAN_RST#" should be connected to "RSMRST#"
GPIO Power Plane
CPU Vcore GPIO[49]
5V Core GPIO[5:1]
3.3V Core GPIO[0][7:6][23:16][39:32][48]
3.3V Resume GPIO[15:8][31:24]
D1900
1N4148W
PM_BATLOW#
BAT_LL# 28
Q1901 2N7002
ICH7_PWROK
VRMPWRGD
R1912 10KOhm
Q1902 2N7002
Q1900 2N7002
5,14,15,26 SMB_CLK_S
5,14,15,26 SMB_DAT_S
SMB_CLK
SMB_DAT
+5VS
+3VS
R1933 8.2KOhm / r0402_h16
R1934 8.2KOhm / r0402_h16
R1935 8.2KOhm / r0402_h16
R1938 8.2KOhm r0402_h16
R1939 8.2KOhm r0402_h16
R1940 8.2KOhm r0402_h16
PCB_ID0
PCB_ID1
PCB_ID2
PCB_VID3 : PROJECT CODE
PCB_VID 0 1 2
MB V1.0 0 0 0
+3VSUS
checklist suggests +3Vsus
USB_PWRSEL R1906 10KOhm
KB_SCI# R1907 10KOhm
SYS_RST# R1909 10KOhm
GPIO11 R1911 10KOhm
RING# R1914 8.2KOhm
PM_BATLOW# R1916 8.2KOhm
SATA_DET#0 R1918 8.2KOhm
SIO_SMI# R1920 8.2KOhm
802_LED_EN# R1922 8.2KOhm
PR_IN#_SB R1924 8.2KOhm
CB_SD# R1926 8.2KOhm / Internal pull up
SMB_CLK R1928 2.2KOhm
SMB_DAT R1929 2.2KOhm
SB_WAKE# R1931 1KOhm
SM_LINK1 RN1900A 10KOhm
LINKALERT# RN1900B 10KOhm
SM_LINK0 RN1900C 10KOhm
RN1900D 10KOhm
SUS_STAT# R1941 4.7KOhm /
PCI_PME# R1942 10KOhm / Internal pull up
18,25,30,33,38 PCI_PME#
01/06
high:PB
low:COM
GPIO35
R1944 100KOhm r0402
R1945 100KOhm r0402
01/02
GPIO6
R1943 10KOhm
LPC_DRQ#0 R1927 8.2KOhm / Internal pull up
PCI_TRDY# RP1900A1
PCI_LOCK# RP1900B2
PCI_SERR# RP1900C3
PCI_PERR# RP1900D4
PCI_REQ#5 RP1900E6
PCI_REQ#0 RP1900F7
PCI_IRDY# RP1900G8
PCI_DEVSEL# RP1900H9
PCI_INTB# RP1901A1
PCI_INTA# RP1901B2
PCI_INTC# RP1901C3
PCI_INTD# RP1901D4
PCI_INTG# RP1901E6
PCI_INTF# RP1901F7
PCI_INTH# RP1901G8
PCI_INTE# RP1901H9
PCI_REQ#4 RP1902A1
PCI_REQ#1 RP1902B2
PCI_REQ#2 RP1902C3
PCI_REQ#3 RP1902D4
PM_CLKRUN# RP1902E6
PM_THERM# RP1902F7
PCI_FRAME# RP1902G8
PCI_STOP# RP1902H9
SMB_CLK_S R1908 2.2KOhm
SMB_DAT_S R1910 2.2KOhm
INT_SERIRQ R1913 10KOhm
STP_PCI# R1915 10KOhm /
STP_CPU# R1917 10KOhm /
R1919 8.2KOhm
RF_OFF_SW# R1921 8.2KOhm
GPIO19 R1923 8.2KOhm
BT_LED_EN# R1925 8.2KOhm
BT_ON R1930 8.2KOhm
WLAN_ON# R1932 8.2KOhm
PM_RSMRST# R1936 10KOhm
PM_DPRSLPVR R1937 100KOhm/ Internal pull down
Title : ICH7-M (3/4)
ASUSTeK COMPUTER INC
Engineer: Ping-Yen Tsai
Size A3
Project Name A3F
Rev 2.0
Date: Wednesday, January 18, 2006
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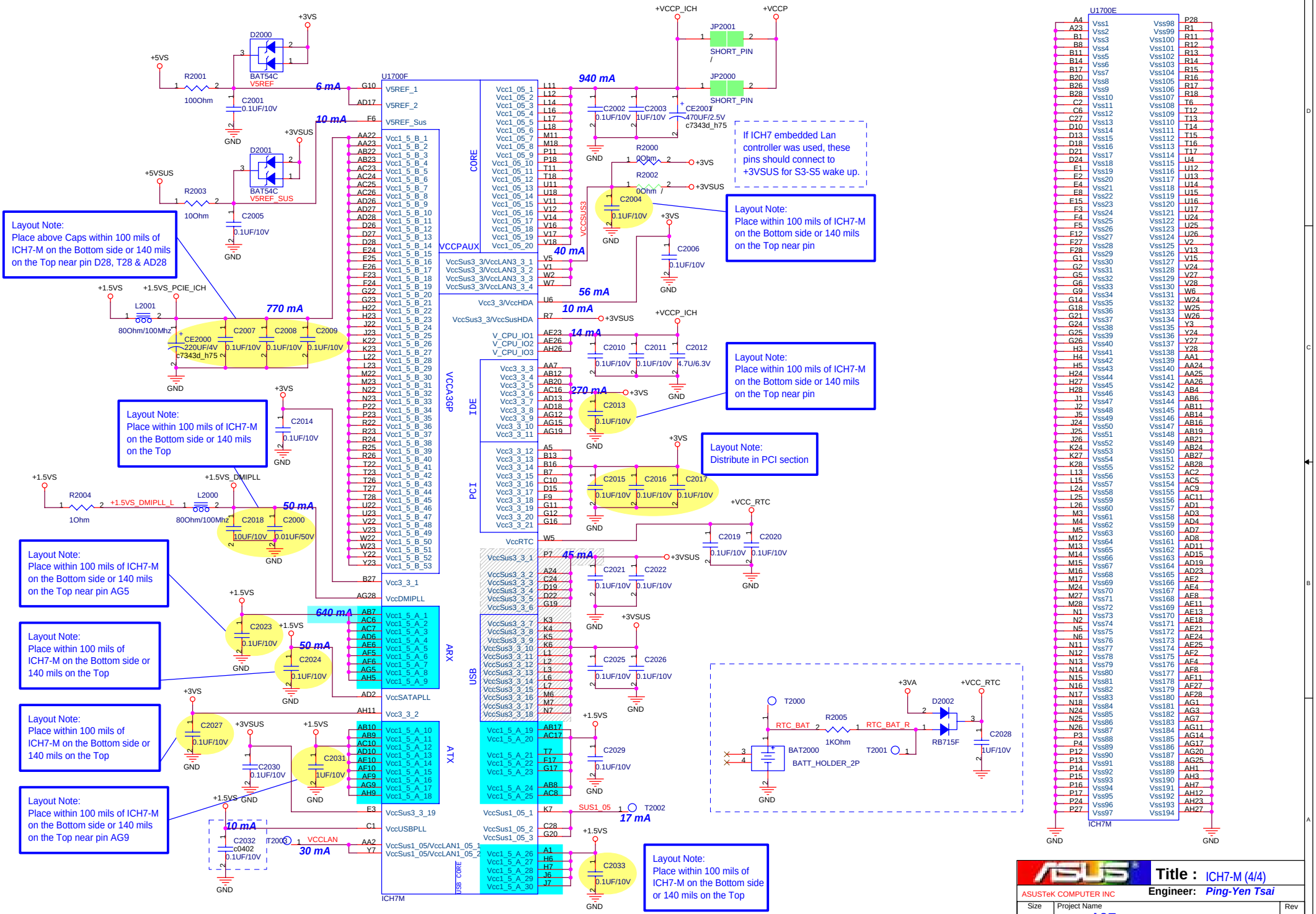
U1700F
ICH7M
U1700E
CORE
VCCPAUX
VCCA96P
IDE
PCI
USB
ARX
ATX
Layout Note:
Place above Caps within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top near pin D28, T28 & AD28
Layout Note:
Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top
Layout Note:
Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top near pin AG5
Layout Note:
Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top
Layout Note:
Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top
Layout Note:
Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top near pin AG9
If ICH7 embedded Lan controller was used, these pins should connect to +3VSUS for S3-S5 wake up.
Layout Note:
Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top near pin
Layout Note:
Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top near pin
Layout Note:
Distribute in PCI section
Layout Note:
Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top
940 mA
40 mA
56 mA
10 mA
14 mA
270 mA
45 mA
17 mA
6 mA
10 mA
770 mA
50 mA
640 mA
50 mA
10 mA
30 mA
Title : ICH7-M (4/4)
ASUSTeK COMPUTER INC
Engineer: Ping-Yen Tsai
Size A3
Project Name A3F
Rev 2.0
Date: Wednesday, January 18, 2006
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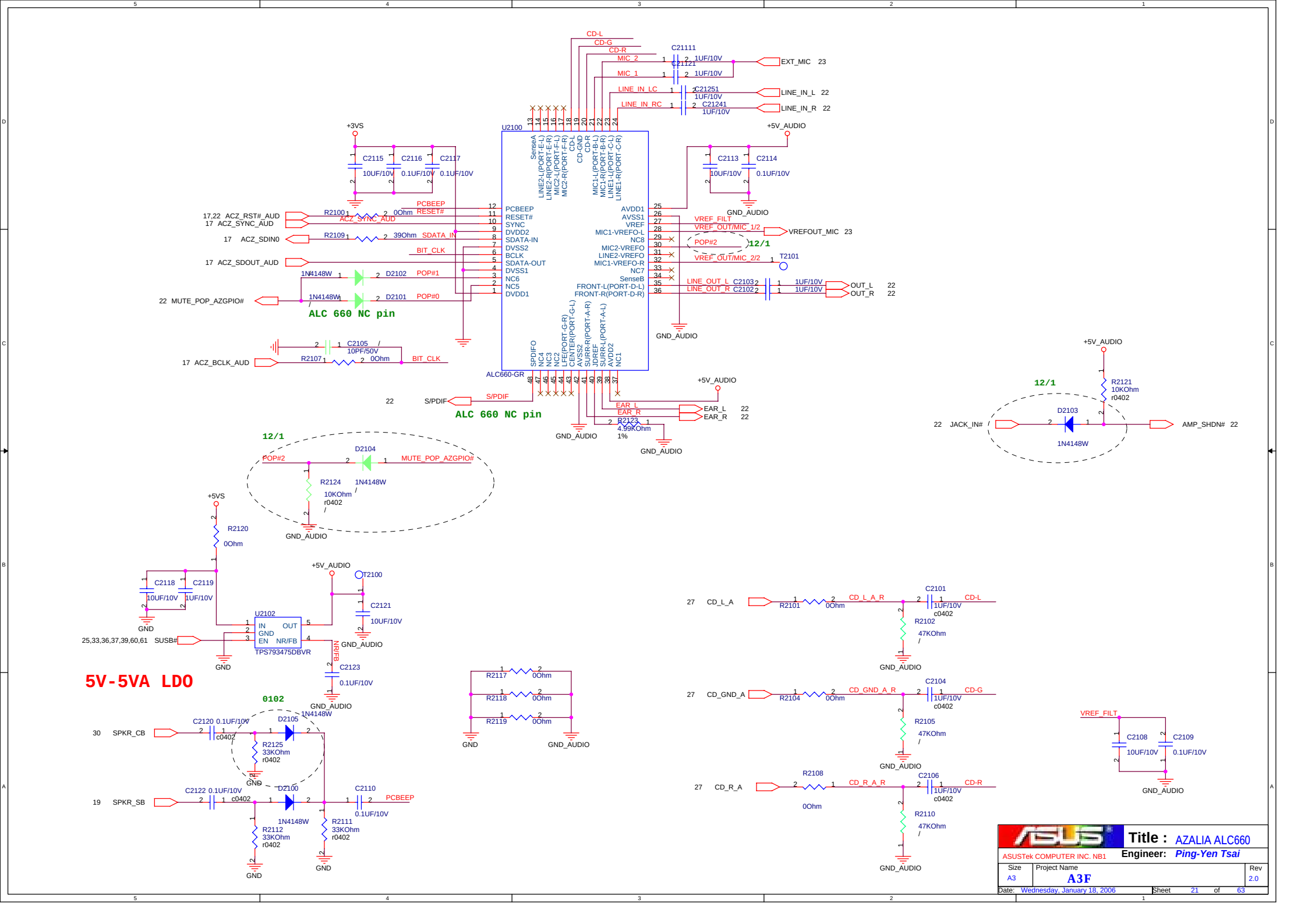
U2100
ALC660-GR
CD-L
CD-G
CD-R
MIC_2
MIC_1
LINE_IN_LC
LINE_IN_RC
C21111
C21121
C21251
C21241
EXT_MIC 23
LINE_IN_L 22
LINE_IN_R 22
+3VS
+5V_AUDIO
C2115 10UF/10V
C2116 0.1UF/10V
C2117 0.1UF/10V
C2113 10UF/10V
C2114 0.1UF/10V
GND_AUDIO
PCBEEP
RESET#
SYNC
DVDD2
SDATA-IN
DVSS2
BCLK
SDATA-OUT
DVSS1
NC6
NC5
DVDD1
17,22 ACZ_RST#_AUD
17 ACZ_SYNC_AUD
17 ACZ_SDIN0
17 ACZ_SDOUT_AUD
17 ACZ_BCLK_AUD
R2100 0Ohm
R2109 39Ohm
R2107 0Ohm
C2105 10PF/50V
D2102 1N4148W
D2101 1N4148W
22 MUTE_POP_AZGPIO#
POP#1
POP#0
BIT_CLK
ALC 660 NC pin
AVDD1
AVSS1
VREF
MIC1-VREFO-L
NC8
MIC2-VREFO
LINE2-VREFO
MIC1-VREFO-R
NC7
SenseB
FRONT-L(PORT-D-L)
FRONT-R(PORT-D-R)
VREF_FILT
VREF_OUT/MIC_1/2
VREFOUT_MIC 23
POP#2
12/1
VREF_OUT/MIC_2/2
T2101
LINE_OUT_L C2103 1UF/10V
LINE_OUT_R C2102 1UF/10V
OUT_L 22
OUT_R 22
SPDIFO
NC4
NC3
NC2
LFE(PORT-G-R)
CENTER(PORT-G-L)
AVSS2
SURR-R(PORT-A-R)
SURR-L(PORT-A-L)
AVDD2
NC1
22 S/PDIF
S/PDIF
EAR_L
EAR_R
EAR_L 22
EAR_R 22
R2123 4.99KOhm 1%
ALC 660 NC pin
12/1
D2104 1N4148W
POP#2
MUTE_POP_AZGPIO#
R2124 10KOhm r0402
GND_AUDIO
+5V_AUDIO
R2121 10KOhm r0402
D2103 1N4148W
22 JACK_IN#
AMP_SHDN# 22
+5VS
R2120 0Ohm
C2118 10UF/10V
C2119 1UF/10V
GND
U2102
IN OUT
GND
EN NR/FB
TPS793475DBVR
25,33,36,37,39,60,61 SUSB#
T2100
C2121 10UF/10V
C2123 0.1UF/10V
NR/FB
5V-5VA LDO
0102
1N4148W
D2105
D2100
C2120 0.1UF/10V
C2122 0.1UF/10V
C2110 0.1UF/10V
PCBEEP
30 SPKR_CB
19 SPKR_SB
R2125 33KOhm r0402
R2112 33KOhm r0402
R2111 33KOhm r0402
R2117 0Ohm
R2118 0Ohm
R2119 0Ohm
27 CD_L_A
CD_L_A_R
R2101 0Ohm
C2101 1UF/10V c0402
R2102 47KOhm
27 CD_GND_A
CD_GND_A_R
R2104 0Ohm
C2104 1UF/10V c0402
R2105 47KOhm
27 CD_R_A
CD_R_A_R
R2108 0Ohm
C2106 1UF/10V c0402
R2110 47KOhm
C2108 10UF/10V
C2109 0.1UF/10V
VREF_FILT
Title : AZALIA ALC660
ASUSTek COMPUTER INC. NB1
Engineer: Ping-Yen Tsai
Size A3
Project Name A3F
Rev 2.0
Date: Wednesday, January 18, 2006
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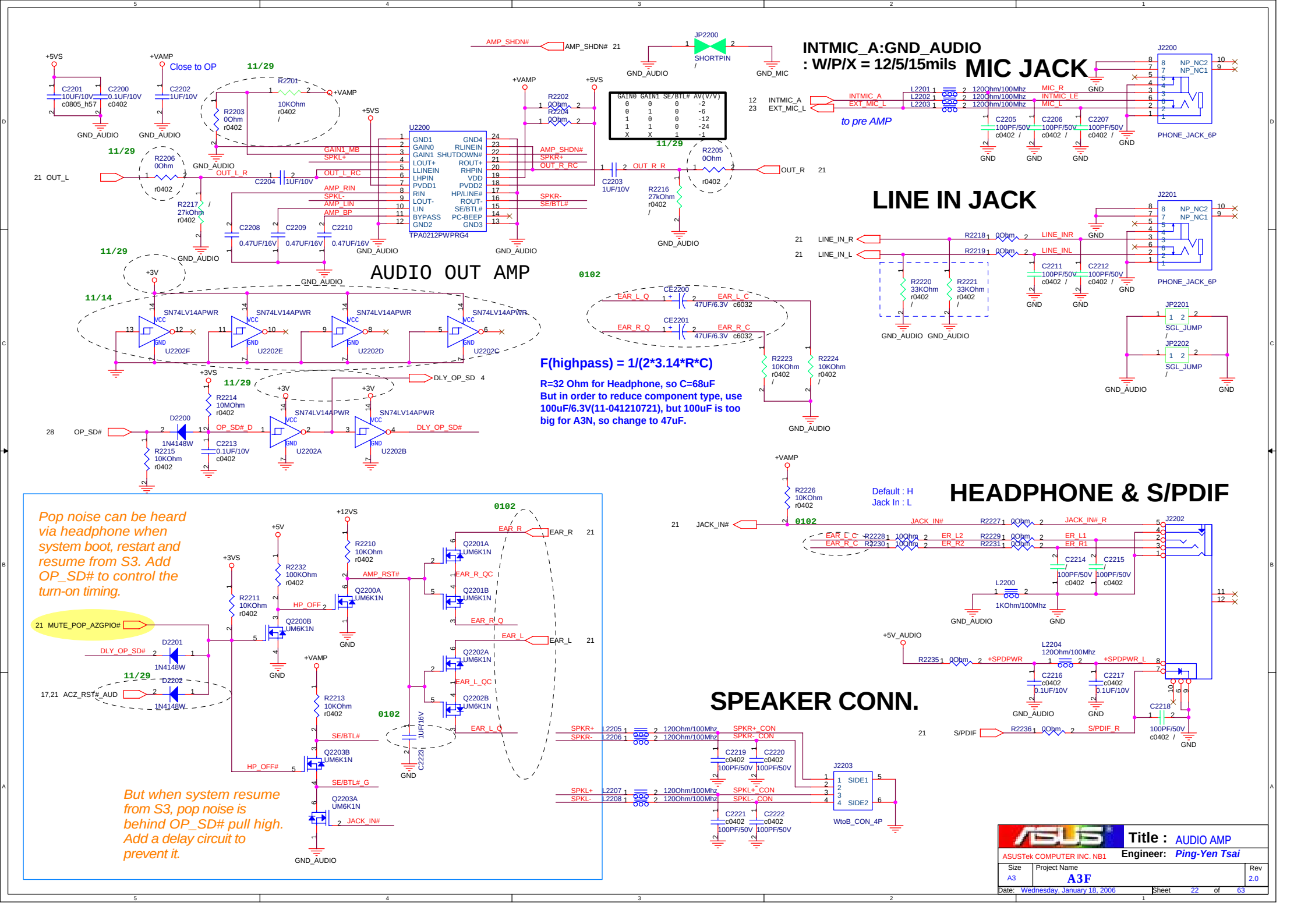
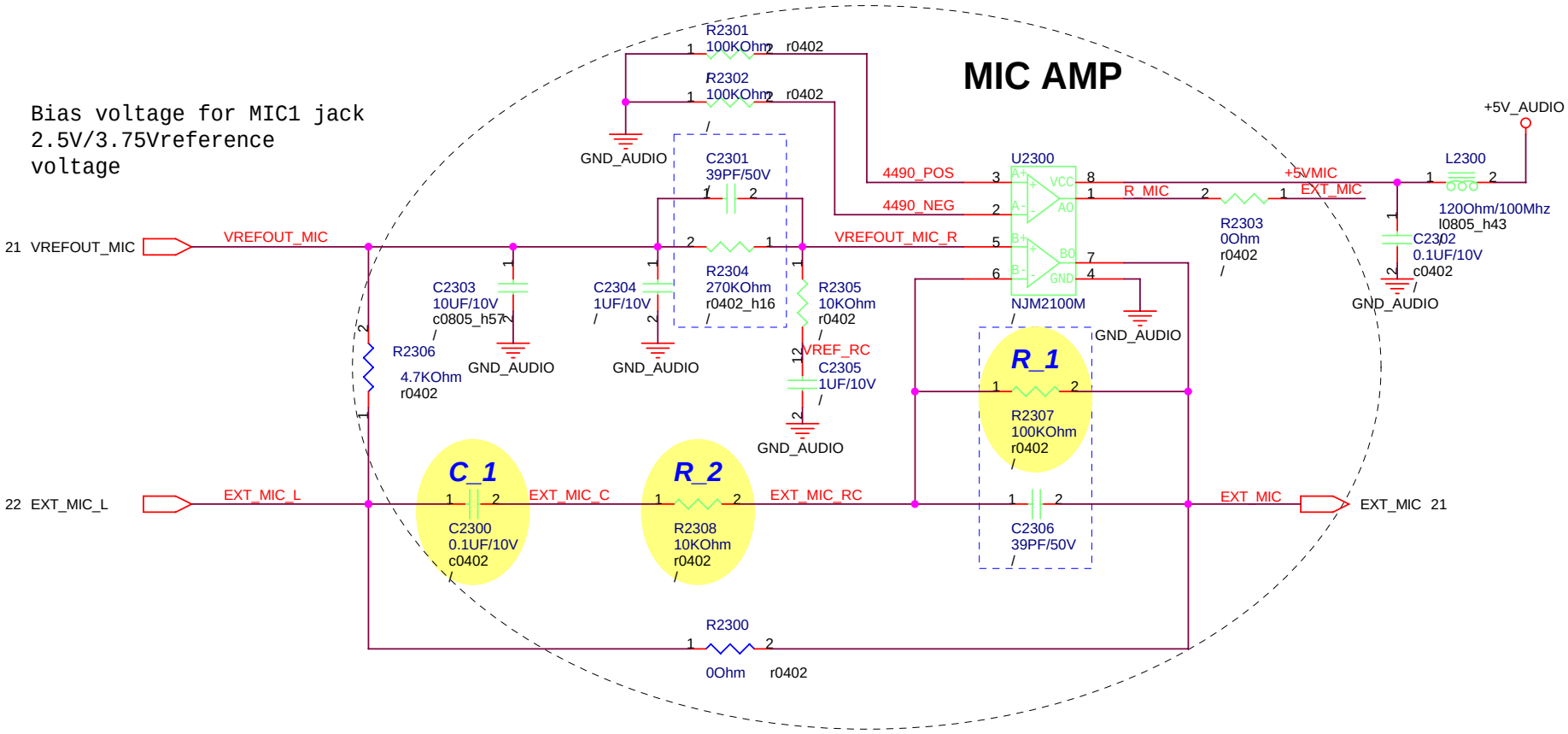

INTMIC_A:GND_AUDIO
: W/P/X = 12/5/15mils
MIC JACK
LINE IN JACK
AUDIO OUT AMP
HEADPHONE & S/PDIF
SPEAKER CONN.
F(highpass) = 1/(2*3.14*R*C)
R=32 Ohm for Headphone, so C=68uF
But in order to reduce component type, use 100uF/6.3V(11-041210721), but 100uF is too big for A3N, so change to 47uF.
Pop noise can be heard via headphone when system boot, restart and resume from S3. Add OP_SD# to control the turn-on timing.
But when system resume from S3, pop noise is behind OP_SD# pull high. Add a delay circuit to prevent it.
Close to OP
Default : H
Jack In : L
to pre AMP
Title : AUDIO AMP
ASUSTek COMPUTER INC. NB1
Engineer: Ping-Yen Tsai
Project Name A3F
Rev 2.0
Date: Wednesday, January 18, 2006
Sheet 22 of 63

1214

MIC AMP

Bias voltage for MIC1 jack
2.5V/3.75Vreference
voltage

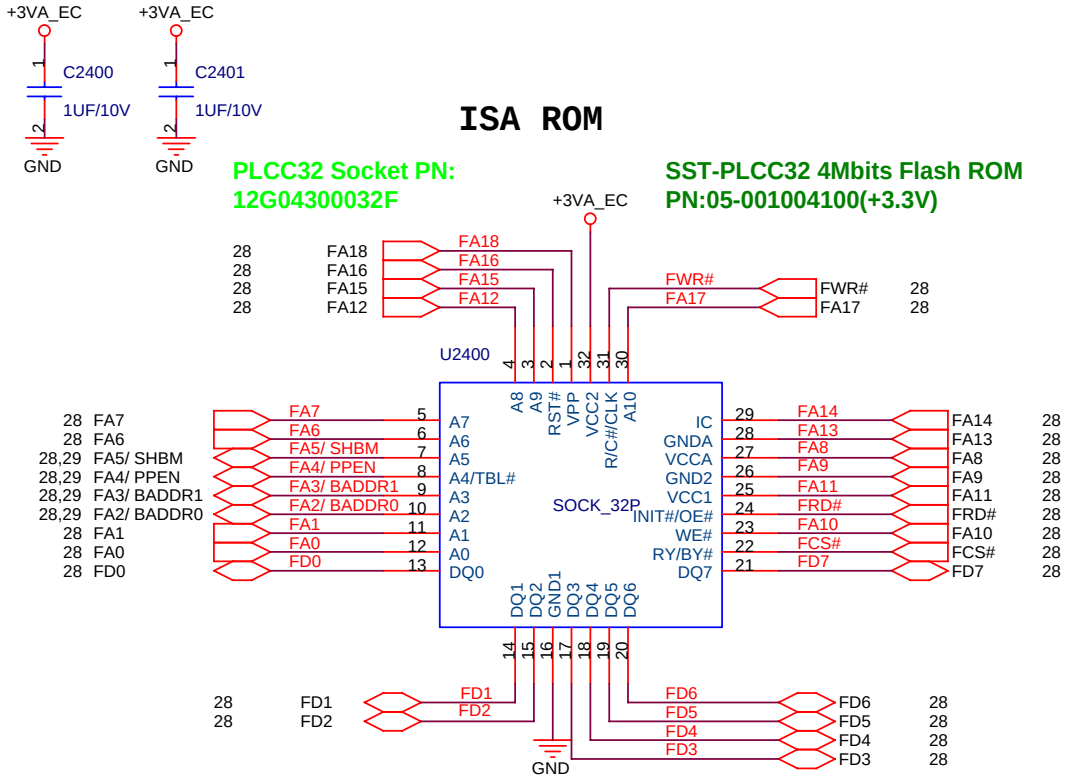


High-Pass Filter Cutoff Frequency
Fc = 1 / (2*3.14*C_1*R_2) = 159 Hz

Gain = - R_1 / R_2 = -10

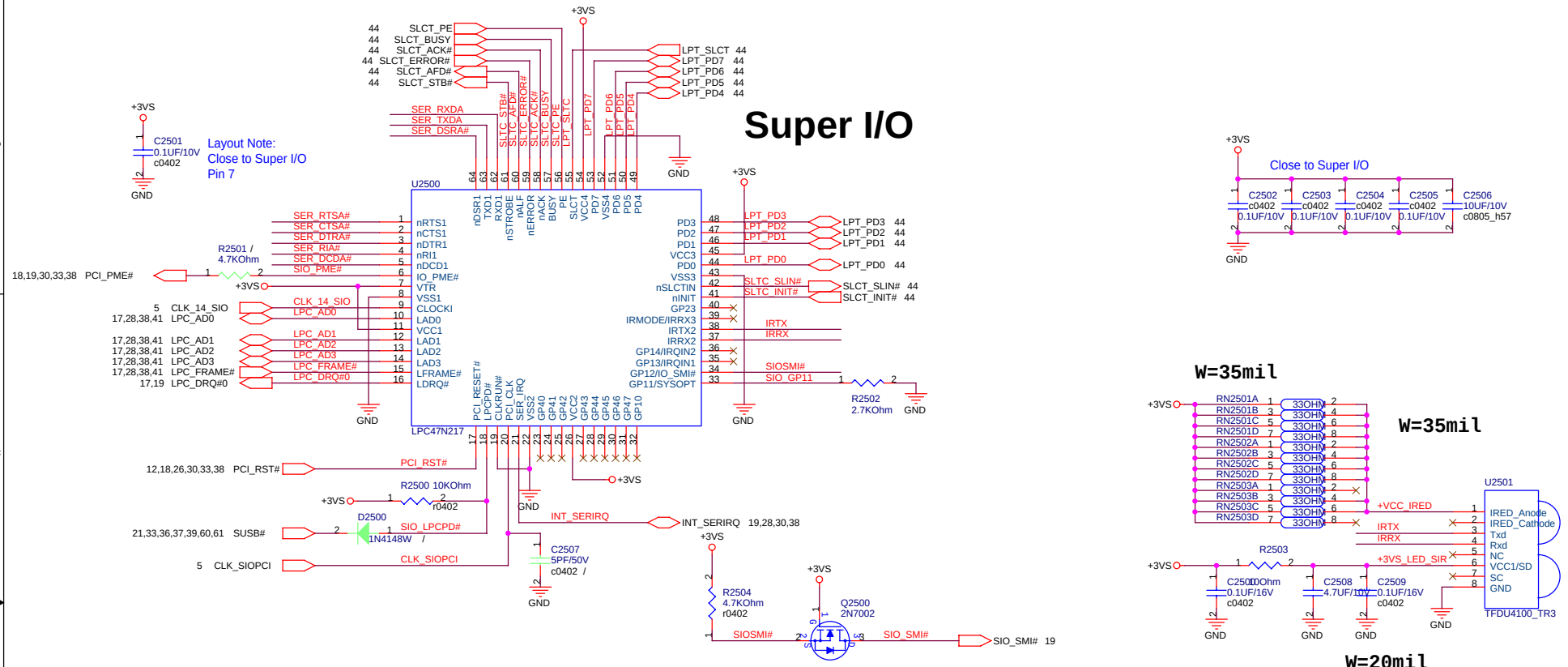
ASUSTek COMPUTER INC. NB1	Title : MIC Pre-AMP	
	Engineer: *Ping-Yen Tsai*	
Size: A4	Project Name: A3F	Rev: 2.0
Date: Wednesday, January 18, 2006	Sheet 23 of 63	

ISA ROM

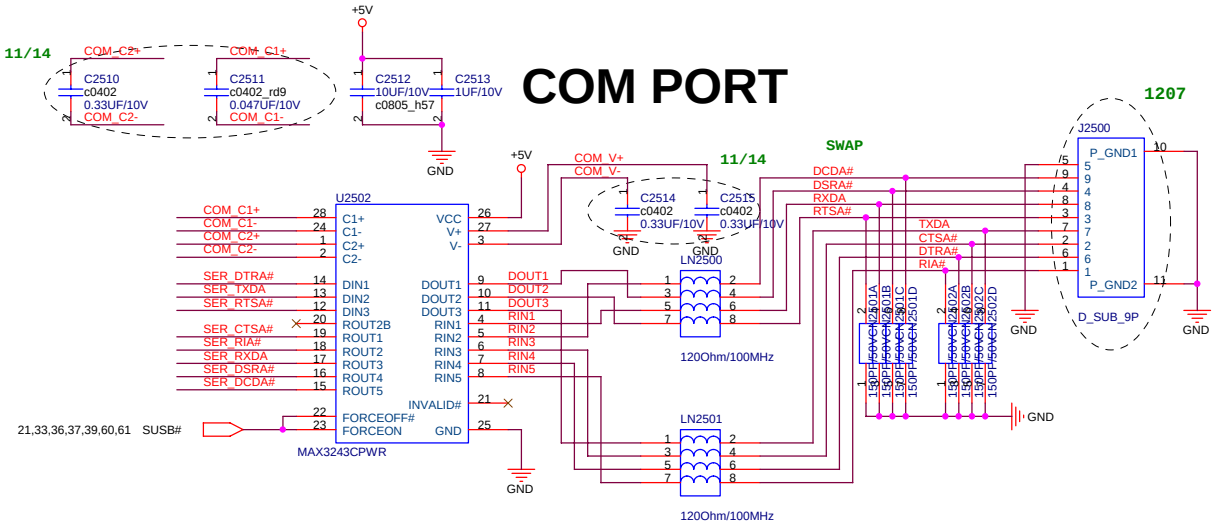


ASUSTeK COMPUTER INC	Title : ISA ROM	
	Engineer: *Ping-Yen Tsai*	
Size: A4	Project Name: **A3F**	Rev: 2.0
Date: Wednesday, January 18, 2006	Sheet 24 of 63	

Super I/O

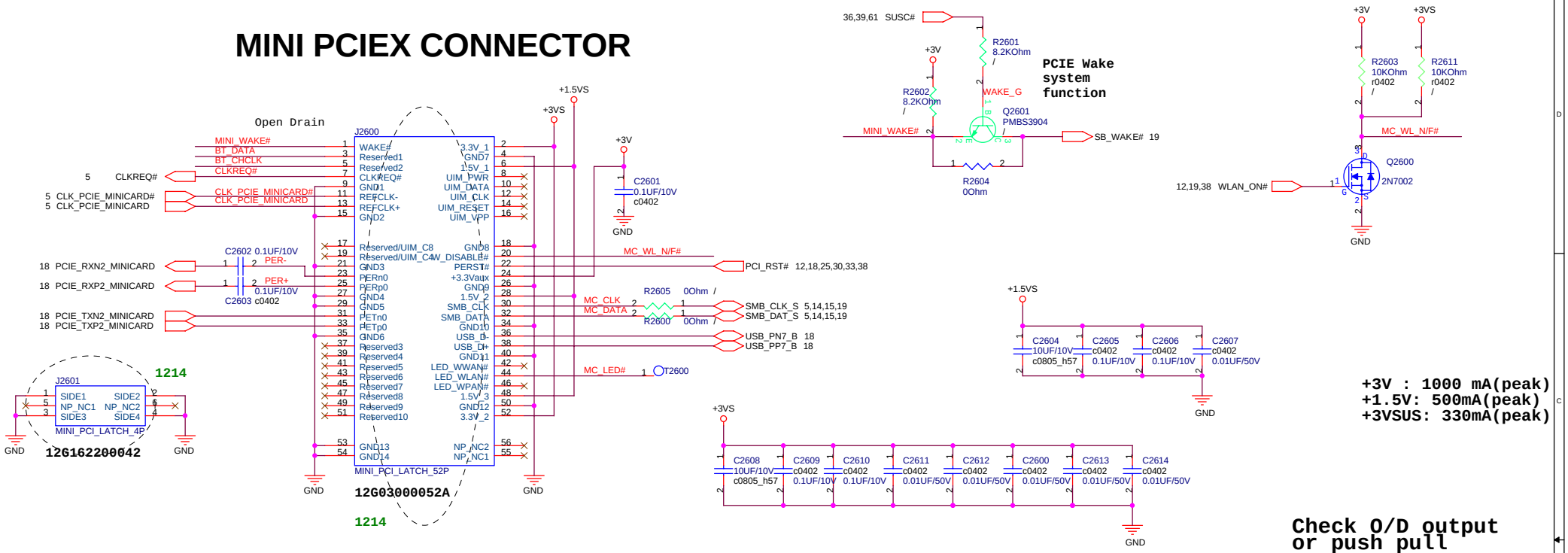


COM PORT



ASUSTeK COMPUTER INC	Title : SUPER I/O		
	Engineer: *Ping-Yen Tsai*		
Size: A3	Project Name: **A3F**		Rev: 2.0
Date: Wednesday, January 18, 2006	Sheet 25 of 63		

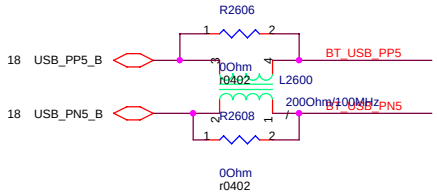
MINI PCIEX CONNECTOR

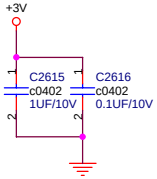


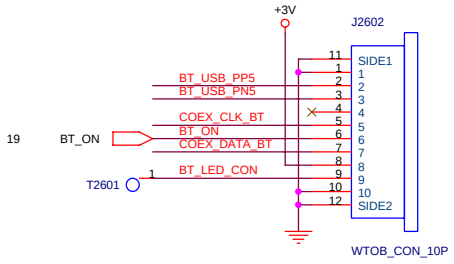
+3V : 1000 mA(peak)
+1.5V: 500mA(peak)
+3VSUS: 330mA(peak)

Check O/D output or push pull

BLUETOOTH CONNECTOR



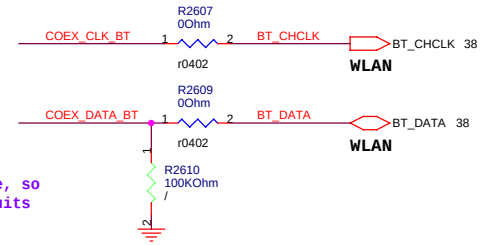




Signal direction-
CLK: BT -> WLAN;
DATA: WLAN -> BT

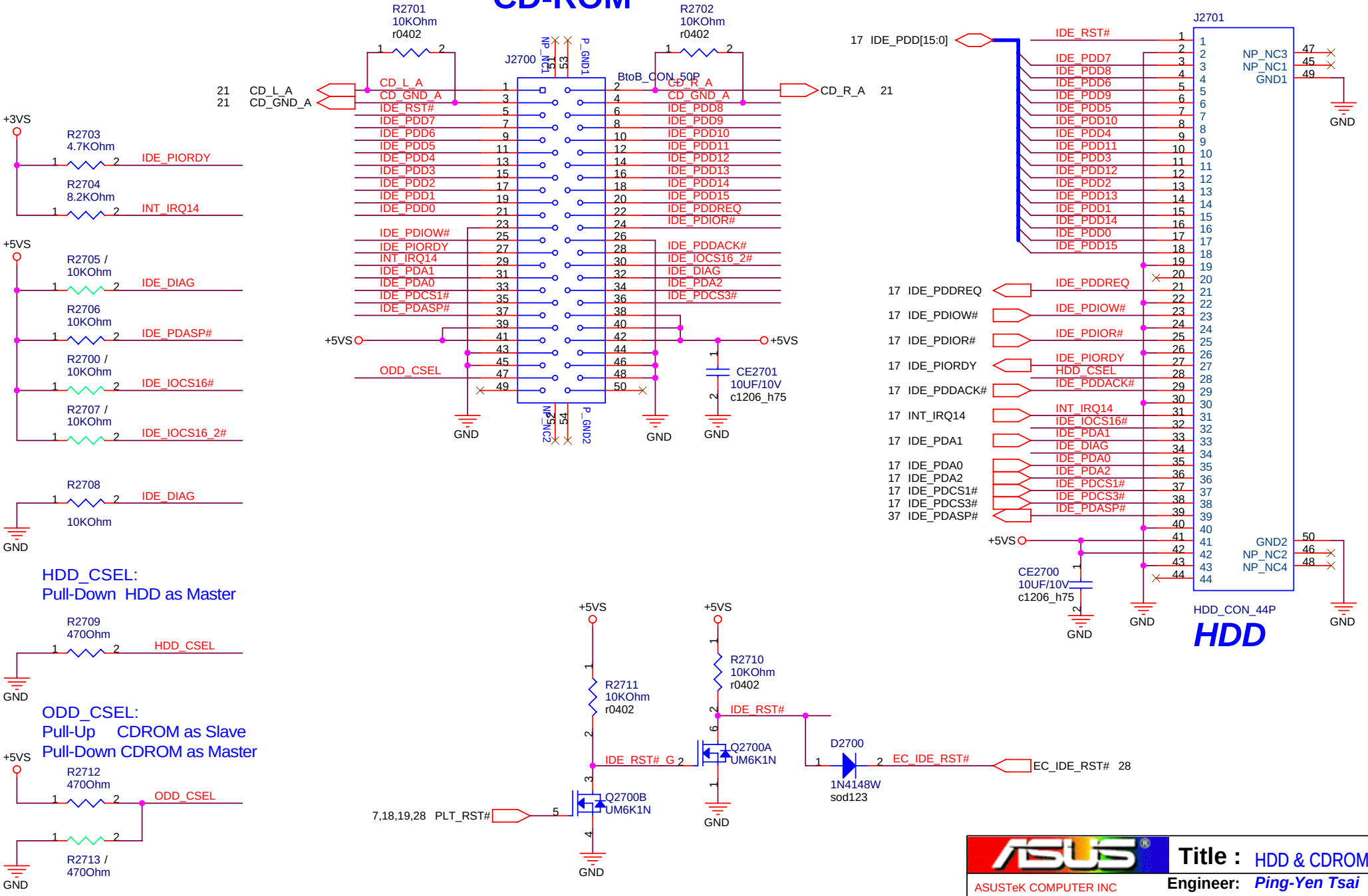
BT_ON 3.3V at GPIO38

BT Module has no leakage, so discard PMOS block circuits



ASUSTeK COMPUTER INC	Title : MINI PCIEX (TV) & BT Conn	
	Engineer: *Ping-Yen Tsai*	
Size: A3	Project Name: **A3F**	Rev: 2.0
Date: Wednesday, January 18, 2006	Sheet 26 of 63	

CD-ROM



ASUSTeK COMPUTER INC	Title : HDD & CDROM	
	Engineer: *Ping-Yen Tsai*	
Size: A4	Project Name: **A3F**	Rev: 2.0
Date: Wednesday, January 18, 2006	Sheet 27 of 63	

TYPE	JP	UK	US
KID0	H	H	L
KID1	L	H	L

Follow A4 Keyboard

U2800 — IT8510TE

LPC: LAD0 LAD1 LAD2 LAD3 LPCCLK LFRAME# LPCRST#/WUI4/GPD2 SERIRQ ECSMI# ECSCI#/GPD3 GA20/GPB5 KBRST#/GPB6 WRST# PWUREQ#

FLASH ROM: FRD# FWR# FCS# FD0 FD1 FD2 FD3 FD4 FD5 FD6 FD7 FA0 FA1 FA2/BADDR0 FA3/BADDR1 FA4/PPEN FA5/SHBM FA6 FA7 FA8 FA9 FA10 FA11 FA12 FA13 FA14 FA15 FA16/GPG0 FA17/GPG1 FA18/GPG2 FA19/GPG3

KBMX: KSI0/STB# KSI1/AFD# KSI2/INIT# KSI3/SLIN# KSI4 KSI5 KSI6 KSI7 KSO0/PD0 KSO1/PD1 KSO2/PD2 KSO3/PD3 KSO4/PD4 KSO5/PD5 KSO6/PD6 KSO7/PD7 KSO8/ACK# KSO9/BUSY KSO10/PE KSO11/ERR# KSO12/SLCT KSO13 KSO14 KSO15

PS/2: CK32K CK32KE PS2CLK0/GPF0 PS2DAT0/GPF1 PS2CLK1/GPF2 PS2DAT1/GPF3

SMBus: SMCLK0/GPB3 SMDAT0/GPB4 SMCLK1/GPC1 SMDAT1/GPC2

ADC: ADC0 ADC1 ADC2 ADC3 ADC8 ADC9

DAC: DAC0 DAC1 DAC2 DAC3

GPIO: PWM0/GPA0 PWM1/GPA1 PWM2/GPA2 PWM3/GPA3 PWM4/GPA4 PWM5/GPA5 PWM6/GPA6 PWM7/GPA7 RXD/GPB0 TXD/GPB1 GPB2 RING#/PWRFAIL#/LPCRST#/GPB7 CLKOUT/GPC0 GPC3 TMRI0/WUI2/GPC4 GPC5 TMRI1/WUI3/GPC6 CK32KOUT/GPC7 RI1#/WUI0/GPD0 RI2#/WUI1/GPD1 GPD4 GINT/GPD5 TACH0/GPD6 TACH1/GPD7 ADC4/GPE0 ADC5/GPE1 ADC6/GPE2 ADC7/GPE3 PWRSW/GPE4 WUI5/GPE5 LPCPD#/WUI6/GPE6 CLKRUN#/WUI7/GPE7 PS2CLK2/GPF4 PS2DAT2/GPF5 PS2CLK3/GPF6 PS2DAT3/GPF7 FA20/GPG4 FA21/GPG5 LPC80HL/GPG6 LPC80LL/GPG7 GPH0 GPH1 GPH2 GPH3 GPH4 GPH5 GPH6 GPH7 GPI0 GPI1 GPI2 GPI3 GPI4 GPI5 GPI6

VSTBY1 VSTBY2 VSTBY3 VSTBY4 VSTBY_PLL VSTBY5 VCC VBAT AVCC VSS1 VSS2 VSS3 VSS4 VSS5 VSS6 VSS7 AVSS

NC1 NC2 NC3 NC4 NC5 NC6 NC7 NC8 NC9 NC10 NC11 NC12 NC13 NC14 NC15

to Battery

to Thermal

no define

watchdog

close to EC

Cload=12.5PF

Layout Note: Close to Switch

Change threshold = 2.9V

tD = 0.69*10^6*CD ps = 6.9 ms

Title :	EC IT8510TE
ASUSTek COMPUTER INC	Engineer: Ping-Yen Tsai
Size: A3	Project Name: A3F
Rev: 2.0	
Date: Wednesday, January 18, 2006	Sheet 28 of 63

EC Hardware Strap

Strap value sampled after VSTBY power up reset

+3VA_EC

PNPCFG base address set by SWCBAHR/SWCBALR

R2901 / 10KOhm r0402

FA2/ BADDR0 → FA2/ BADDR0 24,28

R2905 10KOhm r0402

GND

+3VA_EC

R2902 10KOhm r0402

FA3/ BADDR1 → FA3/ BADDR1 24,28

R2906 / 10KOhm r0402

GND

BADDR[1:0]

No pull up:	*The register pair to access PNPCFG is 002Eh and 002Fh.*
Ext 10K up on BADDR0:	*The register pair to access PNPCFG is 004Eh and 004Fh.*
Ext 10K up on BADDR1:	*The register pair to access PNPCFG is determined by EC domain registers SWCBALR and SWCBAHR.*

Share Memory

+3VA_EC

R2909 10KOhm r0402

FA5/ SHBM → FA5/ SHBM 24,28

R2912 / 10KOhm r0402

GND

SHBM

No pull up:	*Disable shared memory with host BIOS*
Ext 10K up:	*Enable shared memory with host BIOS*

+3VA_EC

R2900 / 10KOhm r0402

FA4/ PPEN → FA4/ PPEN 24,28

R2913 10KOhm r0402

GND

PPEN

No pull up:	*Normal*
Ext 10K up:	*KBS interface pins are switched to parallel port interface for in-system programming.*

EC ADC

Battery

BAT **16.8V**

R2903 / 18KOhm r0402_h16

BAT0_R_AD

R2904 / 1KOhm

R2907 / 3.92KOhm

D2901 / 1N4148W

D2902 / 1N4148W

+3VACC

BAT0_AD 28

C2900 / 0.1UF/10V c0402

GND

Adaptor

A/D_DOCK_IN **19V**

3V

R2908 / 20KOhm

AC_R_AD

R2910 / 1KOhm

R2911 / 3.74KOhm

D2903 / 1N4148W

D2900 / 1N4148W

+3VACC

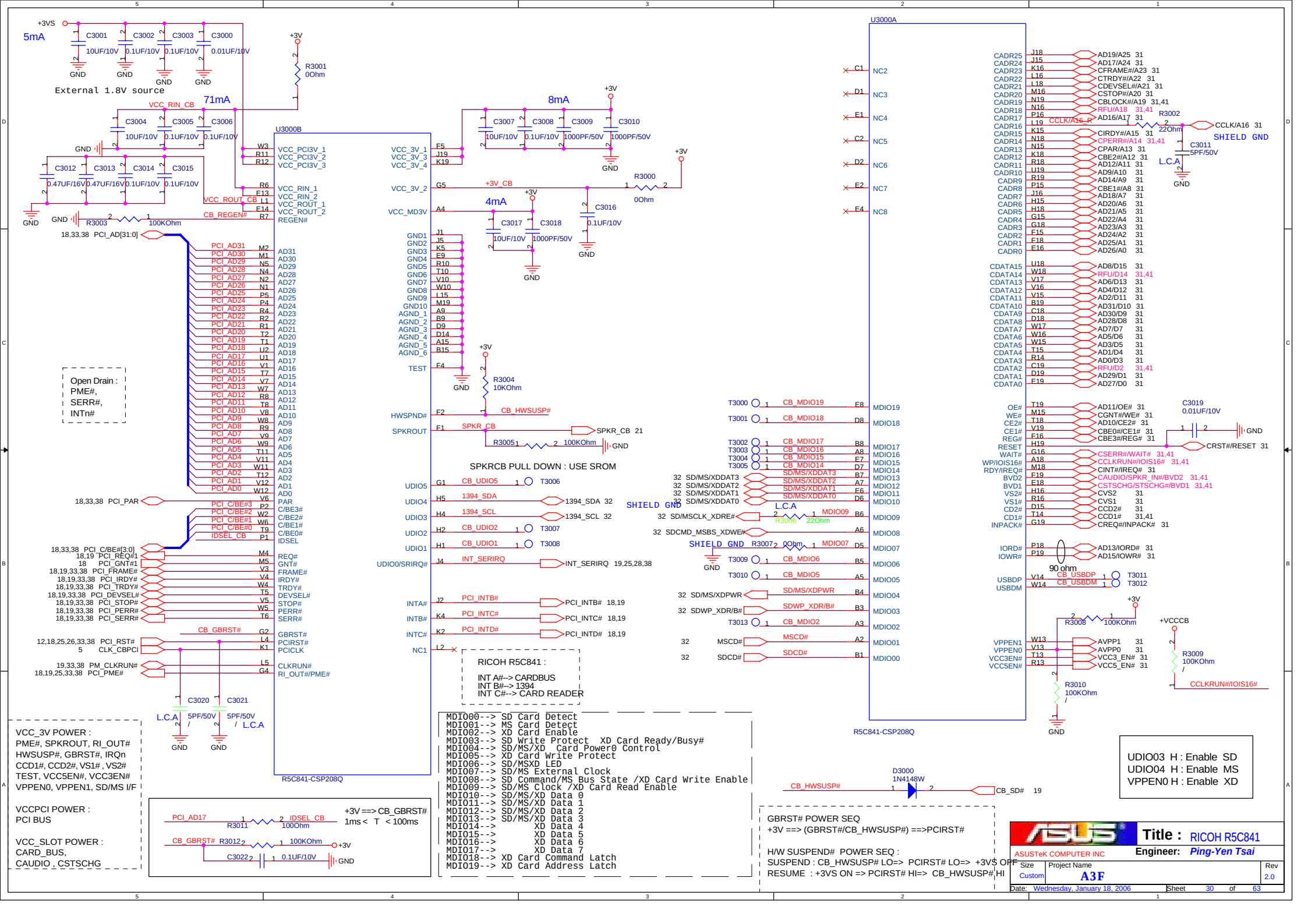
AC_AD 28

2.99V

C2901 / 0.1UF/10V c0402

GND

ASUSTek COMPUTER INC	Title : EC IT8510TE(2/2)	
	Engineer: *Ping-Yen Tsai*	
Size: A4	Project Name: A3F	Rev: 2.0
Date: Wednesday, January 18, 2006	Sheet 29 of 63	


+3VS
5mA
C3001 10UF/10V
C3002 0.1UF/10V
C3003 0.1UF/10V
C3000 0.01UF/10V
GND
External 1.8V source
+3V
R3001 0Ohm
71mA
VCC_RIN_CB
C3004 10UF/10V
C3005 0.1UF/10V
C3006 0.1UF/10V
C3012 0.47UF/16V
C3013 0.47UF/16V
C3014 0.1UF/10V
C3015 0.1UF/10V
VCC_ROUT_CB
CB_REGEN#
R3003 100KOhm
18,33,38 PCI_AD[31:0]
PCI_AD31 PCI_AD30 PCI_AD29 PCI_AD28 PCI_AD27 PCI_AD26 PCI_AD25 PCI_AD24 PCI_AD23 PCI_AD22 PCI_AD21 PCI_AD20 PCI_AD19 PCI_AD18 PCI_AD17 PCI_AD16 PCI_AD15 PCI_AD14 PCI_AD13 PCI_AD12 PCI_AD11 PCI_AD10 PCI_AD9 PCI_AD8 PCI_AD7 PCI_AD6 PCI_AD5 PCI_AD4 PCI_AD3 PCI_AD2 PCI_AD1 PCI_AD0
AD31 AD30 AD29 AD28 AD27 AD26 AD25 AD24 AD23 AD22 AD21 AD20 AD19 AD18 AD17 AD16 AD15 AD14 AD13 AD12 AD11 AD10 AD9 AD8 AD7 AD6 AD5 AD4 AD3 AD2 AD1 AD0
Open Drain : PME#, SERR#, INTn#
18,33,38 PCI_PAR
PAR
PCI_C/BE#3 PCI_C/BE#2 PCI_C/BE#1 PCI_C/BE#0
C/BE3# C/BE2# C/BE1# C/BE0#
IDSEL_CB
IDSEL
18,33,38 PCI_C/BE#[3:0]
18,19 PCI_REQ#1
18 PCI_GNT#1
18,19,33,38 PCI_FRAME#
18,19,33,38 PCI_IRDY#
18,19,33,38 PCI_TRDY#
18,19,33,38 PCI_DEVSEL#
18,19,33,38 PCI_STOP#
18,19,33,38 PCI_PERR#
18,19,33,38 PCI_SERR#
REQ# GNT# FRAME# IRDY# TRDY# DEVSEL# STOP# PERR# SERR#
CB_GBRST#
12,18,25,26,33,38 PCI_RST#
5 CLK_CBPCI
GBRST# PCIRST# PCICLK
19,33,38 PM_CLKRUN#
18,19,25,33,38 PCI_PME#
CLKRUN# RI_OUT#/PME#
C3020 5PF/50V
C3021 5PF/50V
L.C.A
U3000B
R5C841-CSP208Q
VCC_3V POWER :
PME#, SPKROUT, RI_OUT#
HWSUSP#, GBRST#, IRQn
CCD1#, CCD2#, VS1# , VS2#
TEST, VCC5EN#, VCC3EN#
VPPEN0, VPPEN1, SD/MS I/F
VCCPCI POWER :
PCI BUS
VCC_SLOT POWER :
CARD_BUS,
CAUDIO , CSTSCHG
PCI_AD17
R3011 100Ohm
IDSEL_CB
+3V ==> CB_GBRST#
1ms < T < 100ms
CB_GBRST#
R3012 100KOhm
C3022 0.1UF/10V
8mA
C3007 10UF/10V
C3008 0.1UF/10V
C3009 1000PF/50V
C3010 1000PF/50V
VCC_3V_1 VCC_3V_3 VCC_3V_4
VCC_3V_2
+3V_CB
R3000 0Ohm
4mA
C3017 10UF/10V
C3018 1000PF/50V
C3016 0.1UF/10V
VCC_MD3V
GND1 GND2 GND3 GND4 GND5 GND6 GND7 GND8 GND9 GND10
AGND_1 AGND_2 AGND_3 AGND_4 AGND_5 AGND_6
TEST
R3004 10KOhm
HWSPND#
CB_HWSUSP#
SPKROUT
SPKR_CB
R3005 100KOhm
SPKR_CB 21
SPKRCB PULL DOWN : USE SROM
UDIO5 CB_UDIO5 T3006
UDIO4 1394_SDA 1394_SDA 32
UDIO3 1394_SCL 1394_SCL 32
UDIO2 CB_UDIO2 T3007
UDIO1 CB_UDIO1 T3008
UDIO0/SRIRQ# INT_SERIRQ INT_SERIRQ 19,25,28,38
INTA# PCI_INTB# PCI_INTB# 18,19
INTB# PCI_INTC# PCI_INTC# 18,19
INTC# PCI_INTD# PCI_INTD# 18,19
NC1
RICOH R5C841 :
INT A#--> CARDBUS
INT B#--> 1394
INT C#--> CARD READER
MDIO00--> SD Card Detect
MDIO01--> MS Card Detect
MDIO02--> XD Card Enable
MDIO03--> SD Write Protect XD Card Ready/Busy#
MDIO04--> SD/MS/XD Card Power0 Control
MDIO05--> XD Card Write Protect
MDIO06--> SD/MSXD LED
MDIO07--> SD/MS External Clock
MDIO08--> SD Command/MS Bus State /XD Card Write Enable
MDIO09--> SD/MS Clock /XD Card Read Enable
MDIO10--> SD/MS/XD Data 0
MDIO11--> SD/MS/XD Data 1
MDIO12--> SD/MS/XD Data 2
MDIO13--> SD/MS/XD Data 3
MDIO14--> XD Data 4
MDIO15--> XD Data 5
MDIO16--> XD Data 6
MDIO17--> XD Data 7
MDIO18--> XD Card Command Latch
MDIO19--> XD Card Address Latch
U3000A
NC1 NC2 NC3 NC4 NC5 NC6 NC7 NC8
T3000 CB_MDIO19 MDIO19
T3001 CB_MDIO18 MDIO18
T3002 CB_MDIO17 MDIO17
T3003 CB_MDIO16 MDIO16
T3004 CB_MDIO15 MDIO15
T3005 CB_MDIO14 MDIO14
32 SD/MS/XDDAT3 MDIO13
32 SD/MS/XDDAT2 MDIO12
32 SD/MS/XDDAT1 MDIO11
32 SD/MS/XDDAT0 MDIO10
SHIELD GND
L.C.A
32 SD/MSCLK_XDRE# MDIO09
R3006 22Ohm
32 SDCMD_MSBS_XDWE# MDIO08
SHIELD GND R3007 0Ohm MDIO07
T3009 CB_MDIO6 MDIO06
T3010 CB_MDIO5 MDIO05
32 SD/MS/XDPWR MDIO04
32 SDWP_XDR/B# MDIO03
T3013 CB_MDIO2 MDIO02
32 MSCD# MDIO01
32 SDCD# MDIO00
R5C841-CSP208Q
CADR25 CADR24 CADR23 CADR22 CADR21 CADR20 CADR19 CADR18 CADR17 CADR16 CADR15 CADR14 CADR13 CADR12 CADR11 CADR10 CADR9 CADR8 CADR7 CADR6 CADR5 CADR4 CADR3 CADR2 CADR1 CADR0
AD19/A25 AD17/A24 CFRAME#/A23 CTRDY#/A22 CDEVSEL#/A21 CSTOP#/A20 CBLOCK#/A19 RFU/A18 AD16/A17
CCLK/A16_R
R3002 22Ohm
CCLK/A16 31
SHIELD GND
C3011 5PF/50V
L.C.A
CIRDY#/A15 CPERR#/A14 CPAR/A13 CBE2#/A12 AD12/A11 AD9/A10 AD14/A9 CBE1#/A8 AD18/A7 AD20/A6 AD21/A5 AD22/A4 AD23/A3 AD24/A2 AD25/A1 AD26/A0
CDATA15 CDATA14 CDATA13 CDATA12 CDATA11 CDATA10 CDATA9 CDATA8 CDATA7 CDATA6 CDATA5 CDATA4 CDATA3 CDATA2 CDATA1 CDATA0
AD8/D15 RFU/D14 AD6/D13 AD4/D12 AD2/D11 AD31/D10 AD30/D9 AD28/D8 AD7/D7 AD5/D6 AD3/D5 AD1/D4 AD0/D3 RFU/D2 AD29/D1 AD27/D0
OE# WE# CE2# CE1# REG# RESET WAIT# WP/IOIS16# RDY/IREQ# BVD2 BVD1 VS2# VS1# CD2# CD1# INPACK#
AD11/OE# CGNT#/WE# AD10/CE2# CBE0#/CE1# CBE3#/REG# CSERR#/WAIT# CCLKRUN#/IOIS16# CINT#/IREQ# CAUDIO/SPKR_IN#/BVD2 CSTSCHG/STSCHG#/BVD1 CVS2 CVS1 CCD2# CCD1# CREQ#/INPACK#
C3019 0.01UF/10V
GND
CRST#/RESET 31
IORD# IOWR#
AD13/IORD# AD15/IOWR#
90 ohm
USBDP USBDM
CB_USBDP T3011
CB_USBDM T3012
R3008 100KOhm
+VCCCB
VPPEN1 VPPEN0 VCC3EN# VCC5EN#
AVPP1 AVPP0 VCC3_EN# VCC5_EN#
R3009 100KOhm
CCLKRUN#/IOIS16#
R3010 100KOhm
UDIO03 H : Enable SD
UDIO04 H : Enable MS
VPPEN0 H : Enable XD
CB_HWSUSP#
D3000 1N4148W
CB_SD# 19
GBRST# POWER SEQ
+3V ==> (GBRST#/CB_HWSUSP#) ==>PCIRST#
H/W SUSPEND# POWER SEQ :
SUSPEND : CB_HWSUSP# LO=> PCIRST# LO=> +3VS OFF
RESUME : +3VS ON => PCIRST# HI=> CB_HWSUSP# HI
Title : RICOH R5C841
ASUSTeK COMPUTER INC
Engineer: Ping-Yen Tsai
Size Custom
Project Name A3F
Rev 2.0
Date: Wednesday, January 18, 2006
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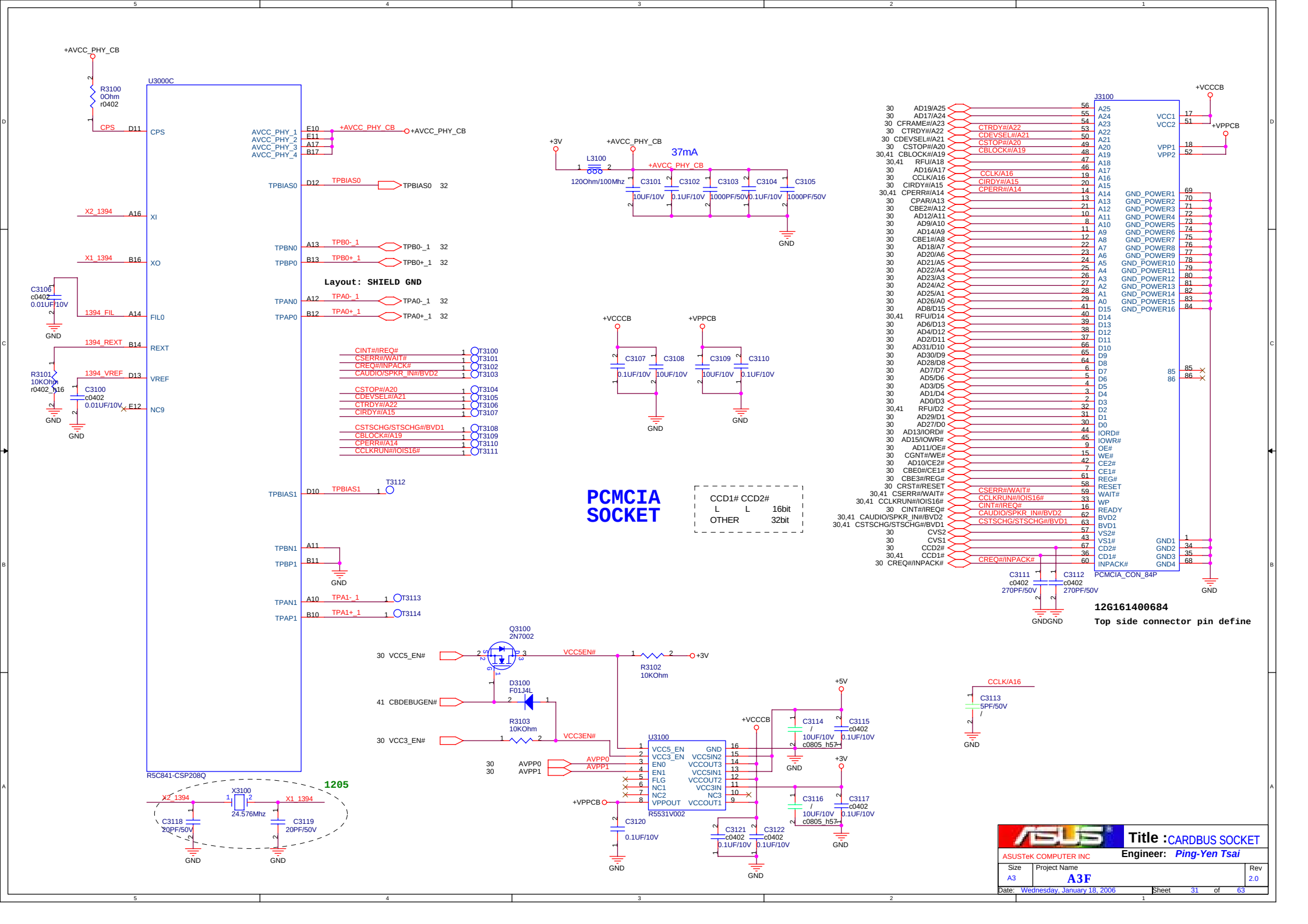
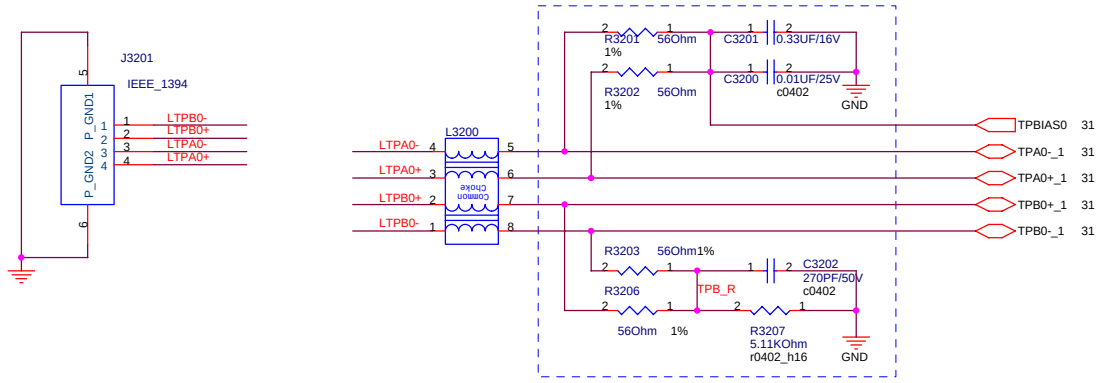
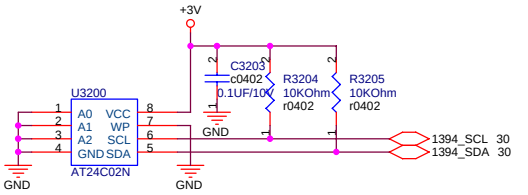
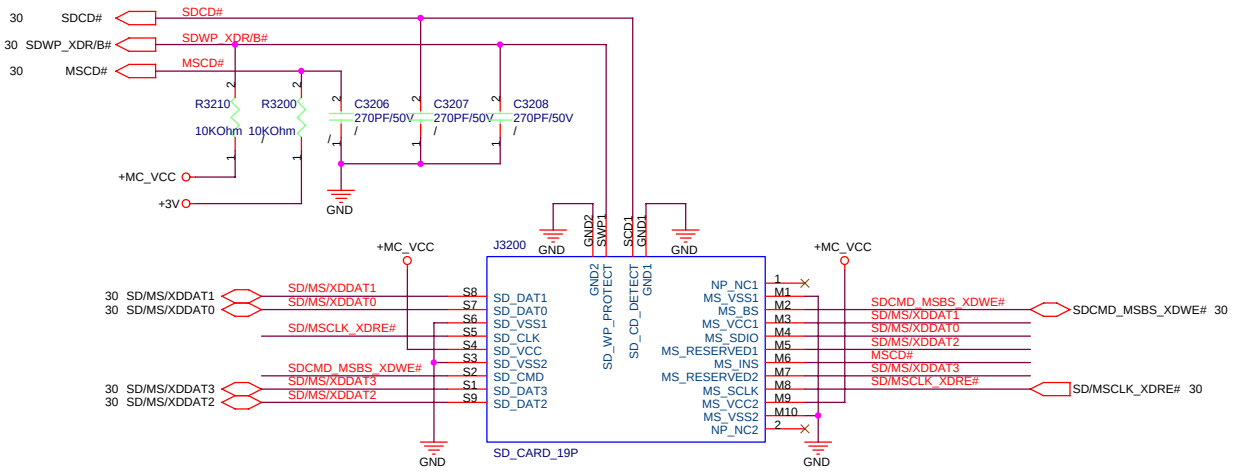

+AVCC_PHY_CB
R3100
0Ohm
r0402
U3000C
CPS
D11
CPS
AVCC_PHY_1
AVCC_PHY_2
AVCC_PHY_3
AVCC_PHY_4
E10
E11
A17
B17
+AVCC_PHY_CB
+AVCC_PHY_CB
TPBIAS0
D12
TPBIAS0
TPBIAS0 32
X2_1394
A16
XI
TPBN0
A13
TPB0-_1
TPB0-_1 32
X1_1394
B16
XO
TPBP0
B13
TPB0+_1
TPB0+_1 32
Layout: SHIELD GND
C3106
c0402
0.01UF/10V
1394_FIL
A14
FIL0
TPAN0
A12
TPA0-_1
TPA0-_1 32
TPAP0
B12
TPA0+_1
TPA0+_1 32
GND
1394_REXT
B14
REXT
CINT#/IREQ#
CSERR#/WAIT#
CREQ#/INPACK#
CAUDIO/SPKR_IN#/BVD2
T3100
T3101
T3102
T3103
R3101
10KOhm
r0402_h16
1394_VREF
D13
VREF
CSTOP#/A20
CDEVSEL#/A21
CTRDY#/A22
CIRDY#/A15
T3104
T3105
T3106
T3107
C3100
c0402
0.01UF/10V
E12
NC9
CSTSCHG/STSCHG#/BVD1
CBLOCK#/A19
CPERR#/A14
CCLKRUN#/IOIS16#
T3108
T3109
T3110
T3111
GND
GND
TPBIAS1
D10
TPBIAS1
T3112
TPBN1
A11
TPBP1
B11
GND
TPAN1
A10
TPA1-_1
T3113
TPAP1
B10
TPA1+_1
T3114
R5C841-CSP208Q
1205
X3100
X2_1394
X1_1394
24.576Mhz
C3118
20PF/50V
C3119
20PF/50V
GND
GND
+3V
+AVCC_PHY_CB
37mA
L3100
120Ohm/100Mhz
C3101
10UF/10V
C3102
0.1UF/10V
C3103
1000PF/50V
C3104
0.1UF/10V
C3105
1000PF/50V
GND
+VCCCB
+VPPCB
C3107
0.1UF/10V
C3108
10UF/10V
C3109
10UF/10V
C3110
0.1UF/10V
GND
GND
PCMCIA
SOCKET
CCD1# CCD2#
L L 16bit
OTHER 32bit
J3100
AD19/A25
AD17/A24
CFRAME#/A23
CTRDY#/A22
CDEVSEL#/A21
CSTOP#/A20
CBLOCK#/A19
CBLOCK#/A19
RFU/A18
AD16/A17
CCLK/A16
CIRDY#/A15
CPERR#/A14
CPAR/A13
CBE2#/A12
AD12/A11
AD9/A10
AD14/A9
CBE1#/A8
AD18/A7
AD20/A6
AD21/A5
AD22/A4
AD23/A3
AD24/A2
AD25/A1
AD26/A0
AD8/D15
RFU/D14
AD6/D13
AD4/D12
AD2/D11
AD31/D10
AD30/D9
AD28/D8
AD7/D7
AD5/D6
AD3/D5
AD1/D4
AD0/D3
RFU/D2
AD29/D1
AD27/D0
AD13/IORD#
AD15/IOWR#
AD11/OE#
CGNT#/WE#
AD10/CE2#
CBE0#/CE1#
CBE3#/REG#
CRST#/RESET
CSERR#/WAIT#
CCLKRUN#/IOIS16#
CINT#/IREQ#
CAUDIO/SPKR_IN#/BVD2
CSTSCHG/STSCHG#/BVD1
CVS2
CVS1
CCD2#
CCD1#
CREQ#/INPACK#
A25
A24
A23
A22
A21
A20
A19
A18
A17
A16
A15
A14
A13
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
D15
D14
D13
D12
D11
D10
D9
D8
D7
D6
D5
D4
D3
D2
D1
D0
IORD#
IOWR#
OE#
WE#
CE2#
CE1#
REG#
RESET
WAIT#
WP
READY
BVD2
BVD1
VS2#
VS1#
CD2#
CD1#
INPACK#
VCC1
VCC2
VPP1
VPP2
GND_POWER1
GND_POWER2
GND_POWER3
GND_POWER4
GND_POWER5
GND_POWER6
GND_POWER7
GND_POWER8
GND_POWER9
GND_POWER10
GND_POWER11
GND_POWER12
GND_POWER13
GND_POWER14
GND_POWER15
GND_POWER16
GND1
GND2
GND3
GND4
+VCCCB
+VPPCB
C3111
c0402
270PF/50V
C3112
c0402
270PF/50V
PCMCIA_CON_84P
GNDGND
GND
12G161400684
Top side connector pin define
Q3100
2N7002
30 VCC5_EN#
VCC5EN#
+3V
R3102
10KOhm
D3100
F01J4L
41 CBDEBUGEN#
R3103
10KOhm
30 VCC3_EN#
VCC3EN#
30 AVPP0
30 AVPP1
AVPP0
AVPP1
U3100
VCC5_EN
VCC3_EN
EN0
EN1
FLG
NC1
NC2
VPPOUT
GND
VCC5IN2
VCCOUT3
VCC5IN1
VCCOUT2
VCC3IN
NC3
VCCOUT1
R5531V002
+VPPCB
C3120
0.1UF/10V
+VCCCB
+5V
C3114
/
10UF/10V
C3115
c0402
0.1UF/10V
c0805_h57
+3V
C3116
/
10UF/10V
C3117
c0402
0.1UF/10V
c0805_h57
C3121
c0402
0.1UF/10V
C3122
c0402
0.1UF/10V
GND
GND
GND
GND
CCLK/A16
C3113
5PF/50V
GND
ASUSTeK COMPUTER INC
Title : CARDBUS SOCKET
Engineer: Ping-Yen Tsai
Size
A3
Project Name
A3F
Rev
2.0
Date: Wednesday, January 18, 2006
Sheet 31 of 63

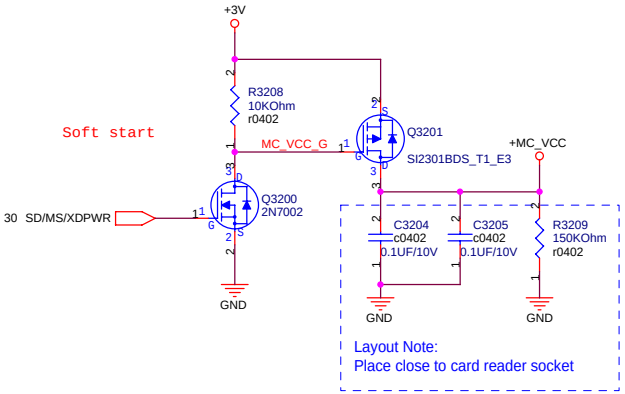


1. Close to R5C841
2. The area is as compact as possible,length < 10 mm
3. TPA Pair and TPB pair mismatch < 2.5mm
4. No via recommend , maxmium is one.
5. Total length < 50 mm
6. Differential impedance is 110+/- 6 ohm
7. TPA Pair trace or TPB pair trace mismatch < 1.25mm

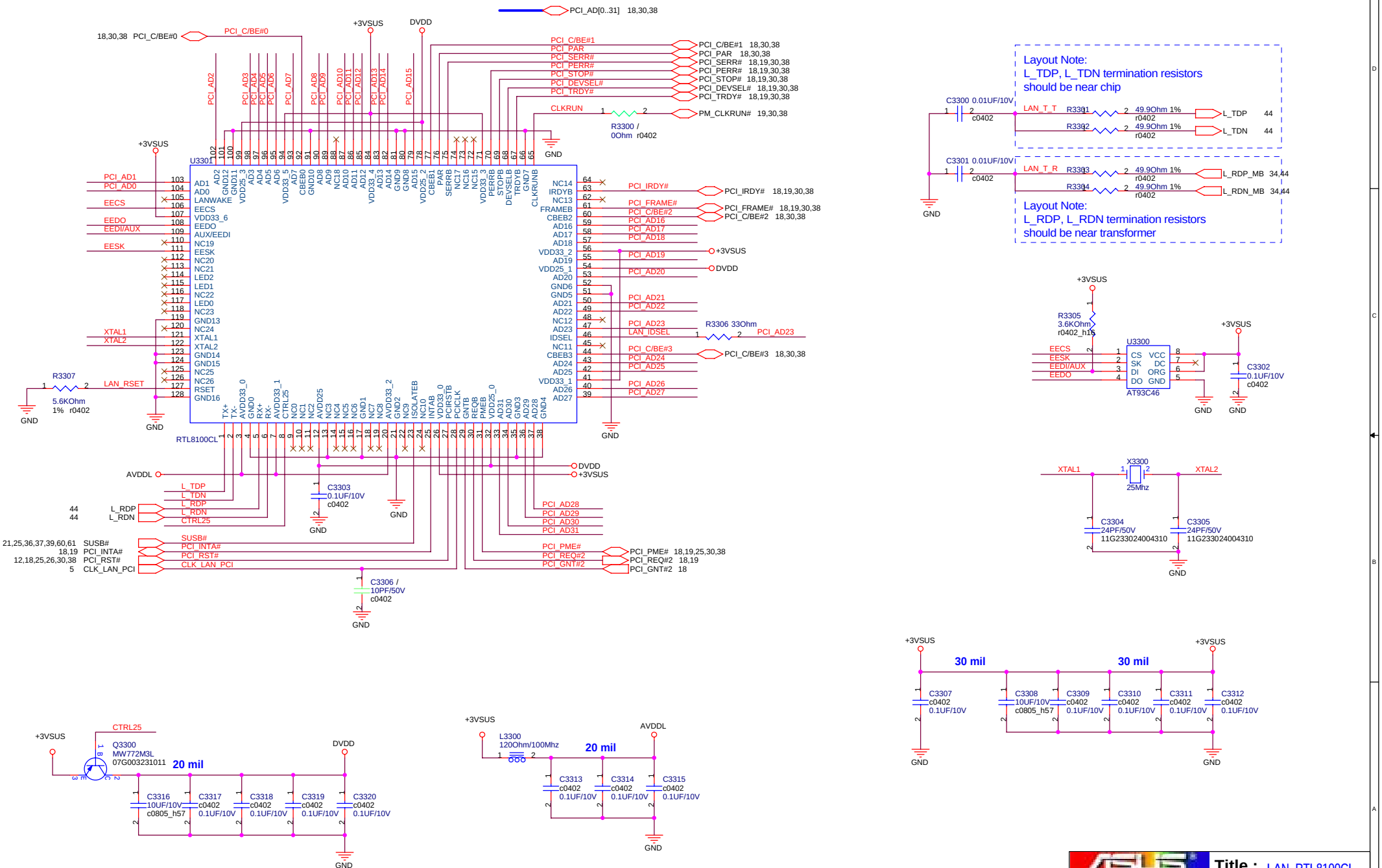




Layout: SHIELD GND

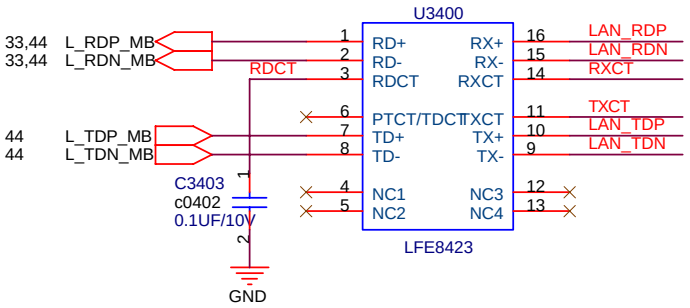


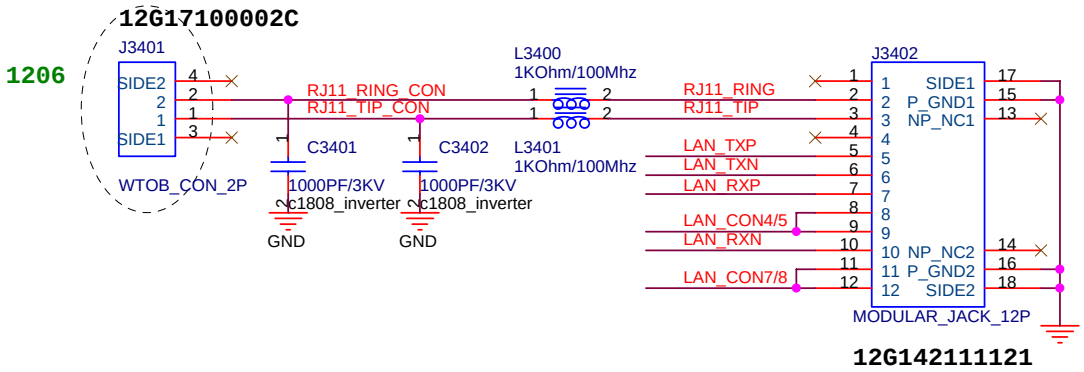
ASUSTeK COMPUTER INC	Title : 1394 & 3 IN 1 CON		
	Engineer: Ping-Yen Tsai		
Size: A3	Project Name: A3F		Rev: 2.0
Date: Wednesday, January 18, 2006	Sheet 32 of 63		

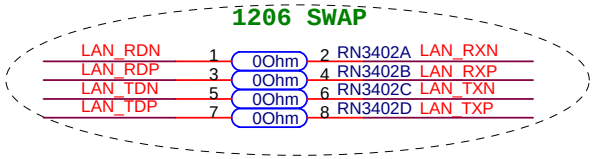


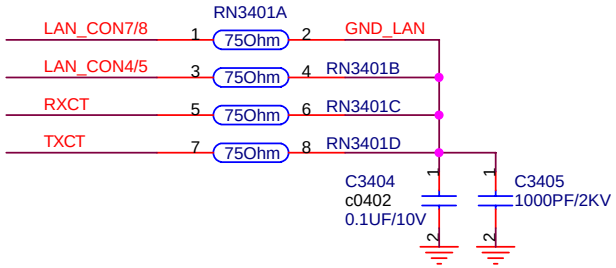
Title : LAN_RTL8100CL		
ASUSTek COMPUTER INC. NB6	Engineer: *Ping-Yen Tsai*	
Size: A3	Project Name: **A3F**	Rev: 2.0
Date: Wednesday, January 18, 2006	Sheet 33 of 63	

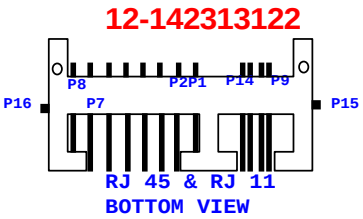
LAN PORT



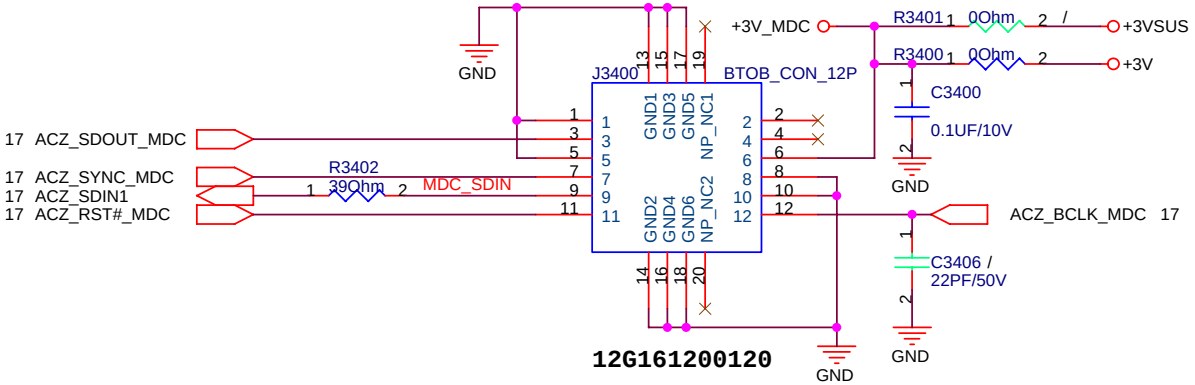




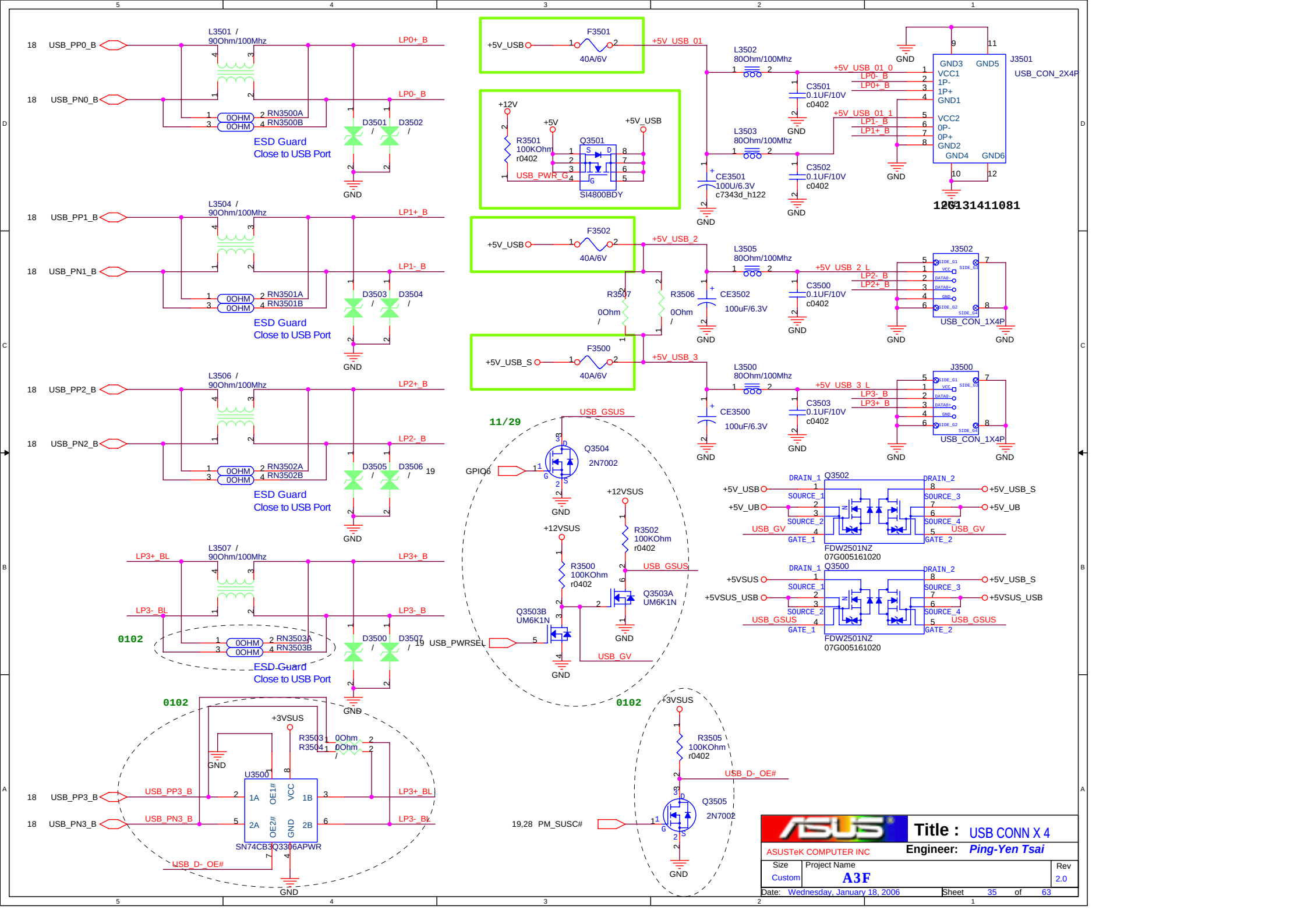




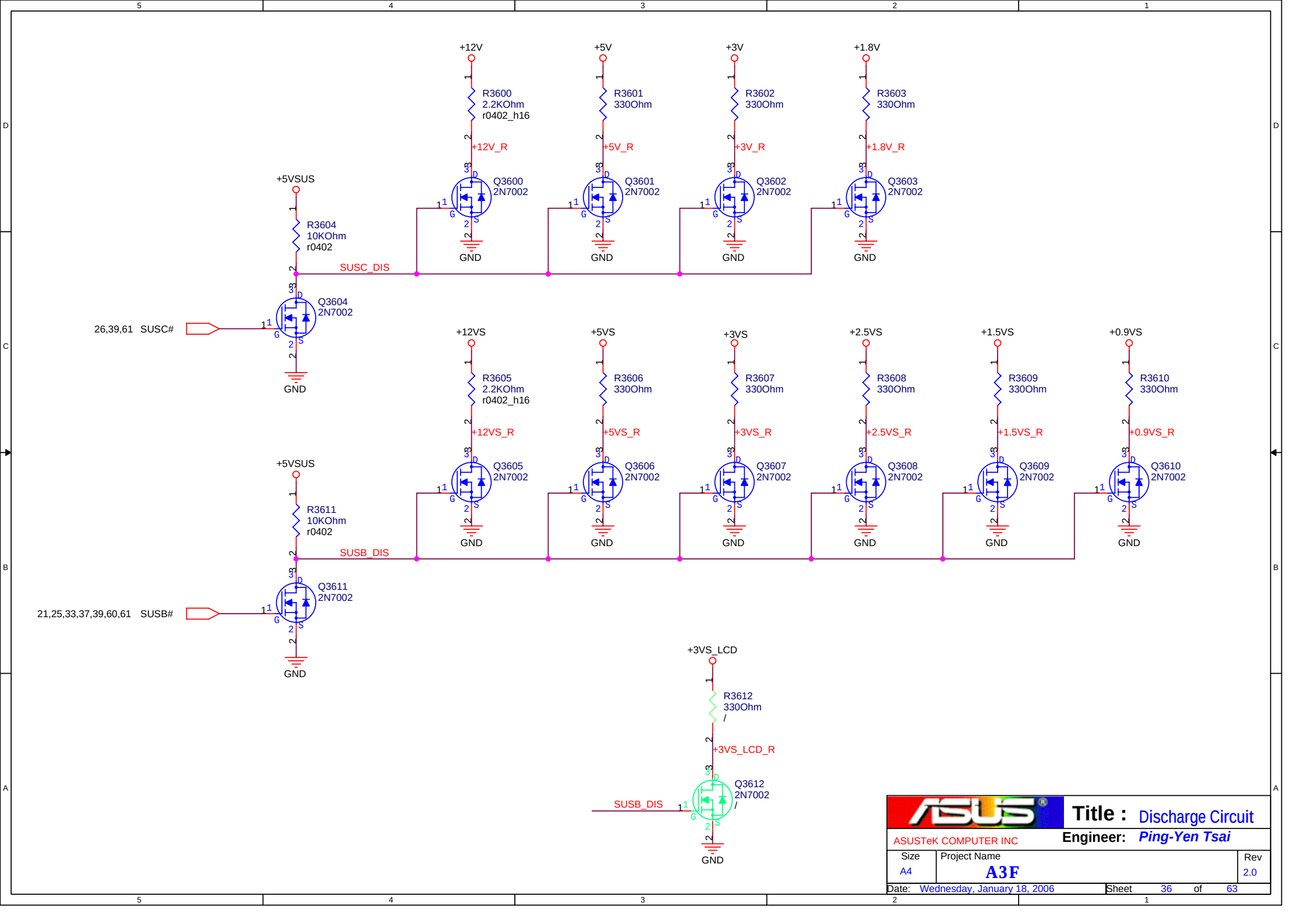
MDC Conn



ASUSTeK COMPUTER INC	Title : RJ11/45 & MDC	
	Engineer: *Ping-Yen Tsai*	
Size: A4	Project Name: **A3F**	Rev: 2.0
Date: Wednesday, January 18, 2006	Sheet 34 of 63	



ASUSTeK COMPUTER INC	Title : USB CONN X 4		
	Engineer: Ping-Yen Tsai		
Size: Custom	Project Name: A3F		Rev: 2.0
Date: Wednesday, January 18, 2006		Sheet 35 of 63	



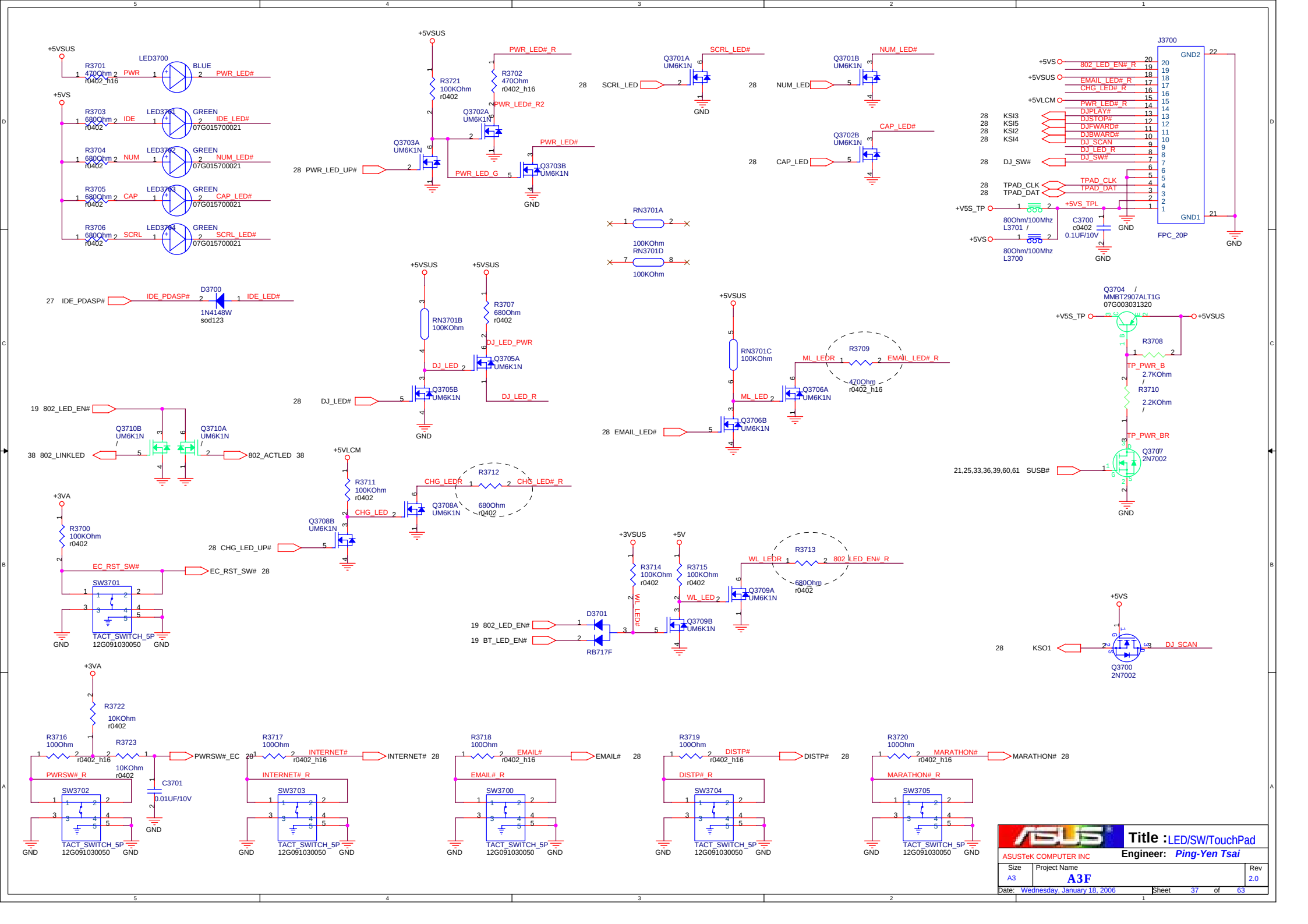
ASUSTeK COMPUTER INC

Title : Discharge Circuit

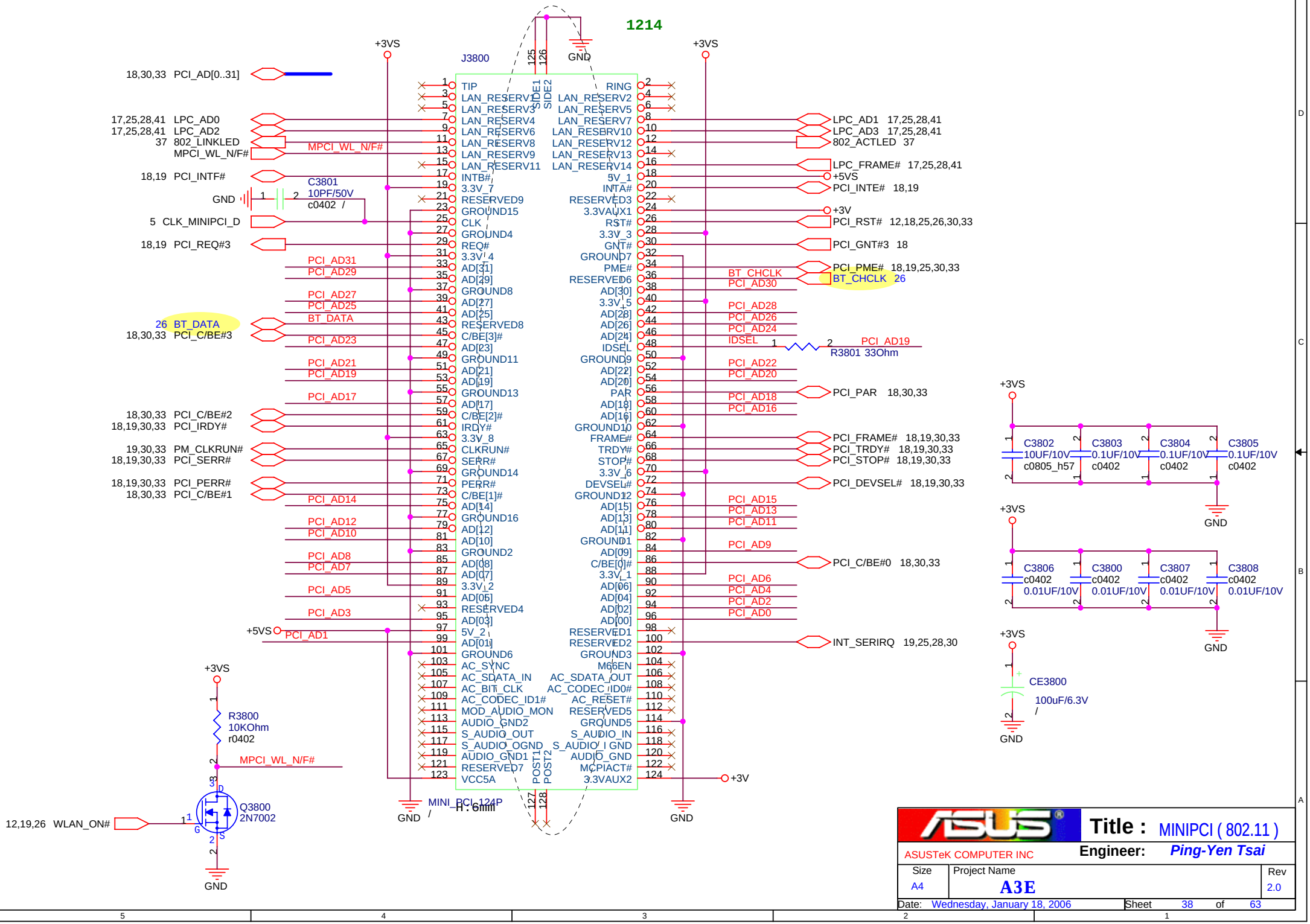
Engineer: *Ping-Yen Tsai*

Size	Project Name	Rev
A4	A3F	2.0

Date: Wednesday, January 18, 2006 Sheet 36 of 63



ASUSTeK COMPUTER INC	Title : LED/SW/TouchPad		
	Engineer: *Ping-Yen Tsai*		
Size: A3	Project Name: **A3F**		Rev: 2.0
Date: Wednesday, January 18, 2006	Sheet 37 of 63		


1214
J3800
18,30,33 PCI_AD[0..31]
17,25,28,41 LPC_AD0
17,25,28,41 LPC_AD2
37 802_LINKLED
MPCI_WL_N/F#
18,19 PCI_INTF#
GND
C3801
10PF/50V
c0402 /
5 CLK_MINIPCI_D
18,19 PCI_REQ#3
26 BT_DATA
18,30,33 PCI_C/BE#3
18,30,33 PCI_C/BE#2
18,19,30,33 PCI_IRDY#
19,30,33 PM_CLKRUN#
18,19,30,33 PCI_SERR#
18,19,30,33 PCI_PERR#
18,30,33 PCI_C/BE#1
+5VS
12,19,26 WLAN_ON#
R3800
10KOhm
r0402
Q3800
2N7002
MINI_PCI_124P
H: 6mm
LPC_AD1 17,25,28,41
LPC_AD3 17,25,28,41
802_ACTLED 37
LPC_FRAME# 17,25,28,41
PCI_INTE# 18,19
PCI_RST# 12,18,25,26,30,33
PCI_GNT#3 18
PCI_PME# 18,19,25,30,33
BT_CHCLK 26
R3801 33Ohm
PCI_PAR 18,30,33
PCI_FRAME# 18,19,30,33
PCI_TRDY# 18,19,30,33
PCI_STOP# 18,19,30,33
PCI_DEVSEL# 18,19,30,33
PCI_C/BE#0 18,30,33
INT_SERIRQ 19,25,28,30
C3802 10UF/10V c0805_h57
C3803 0.1UF/10V c0402
C3804 0.1UF/10V c0402
C3805 0.1UF/10V c0402
C3806 c0402 0.01UF/10V
C3800 c0402 0.01UF/10V
C3807 c0402 0.01UF/10V
C3808 c0402 0.01UF/10V
CE3800
100uF/6.3V
/
Title : MINIPCI (802.11)
ASUSTeK COMPUTER INC
Engineer: Ping-Yen Tsai
Size A4
Project Name A3E
Rev 2.0
Date: Wednesday, January 18, 2006
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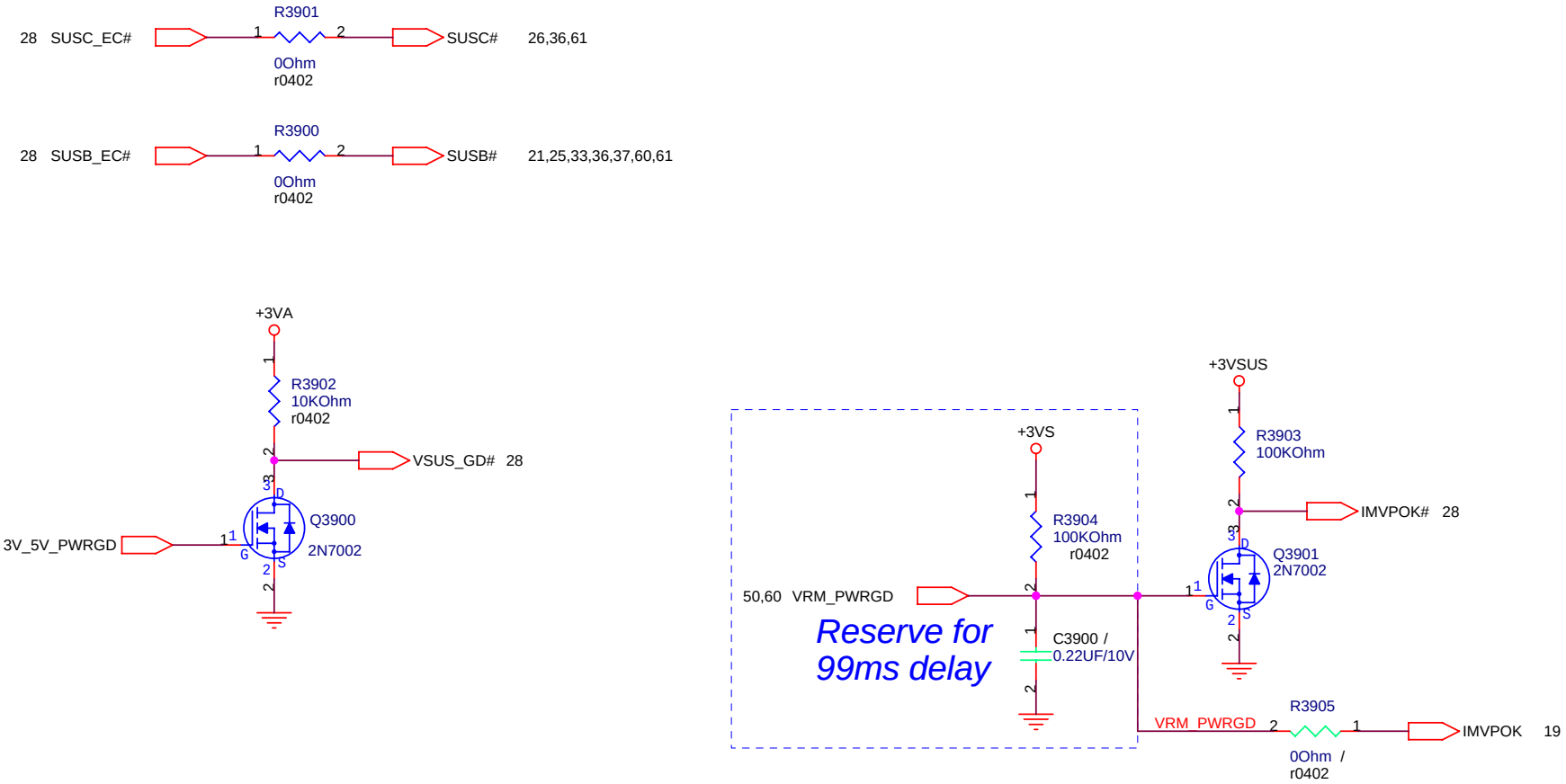
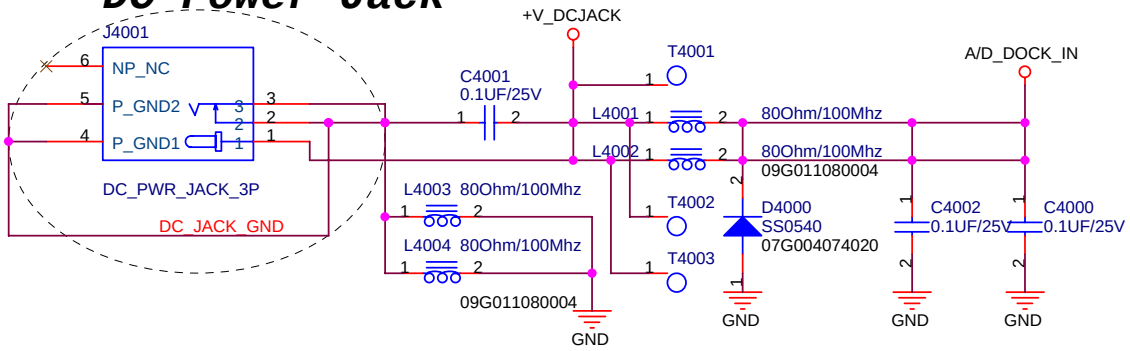
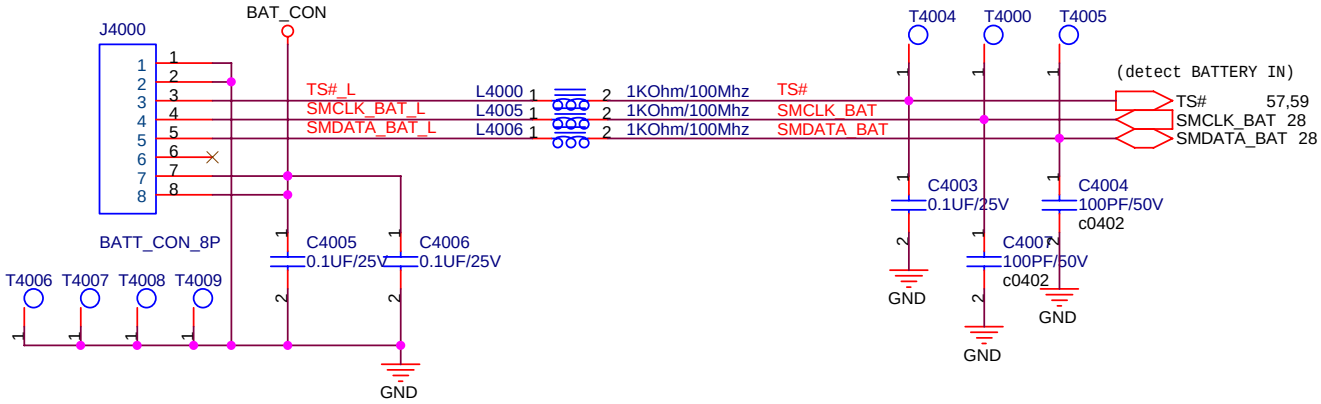


ASUSTeK COMPUTER INC	Title : POWER-ON SEQ.	
	Engineer: *Ping-Yen Tsai*	
Size: A4	Project Name: A3F	Rev: 2.0
Date: Wednesday, January 18, 2006	Sheet 39 of 63	

DC Power Jack

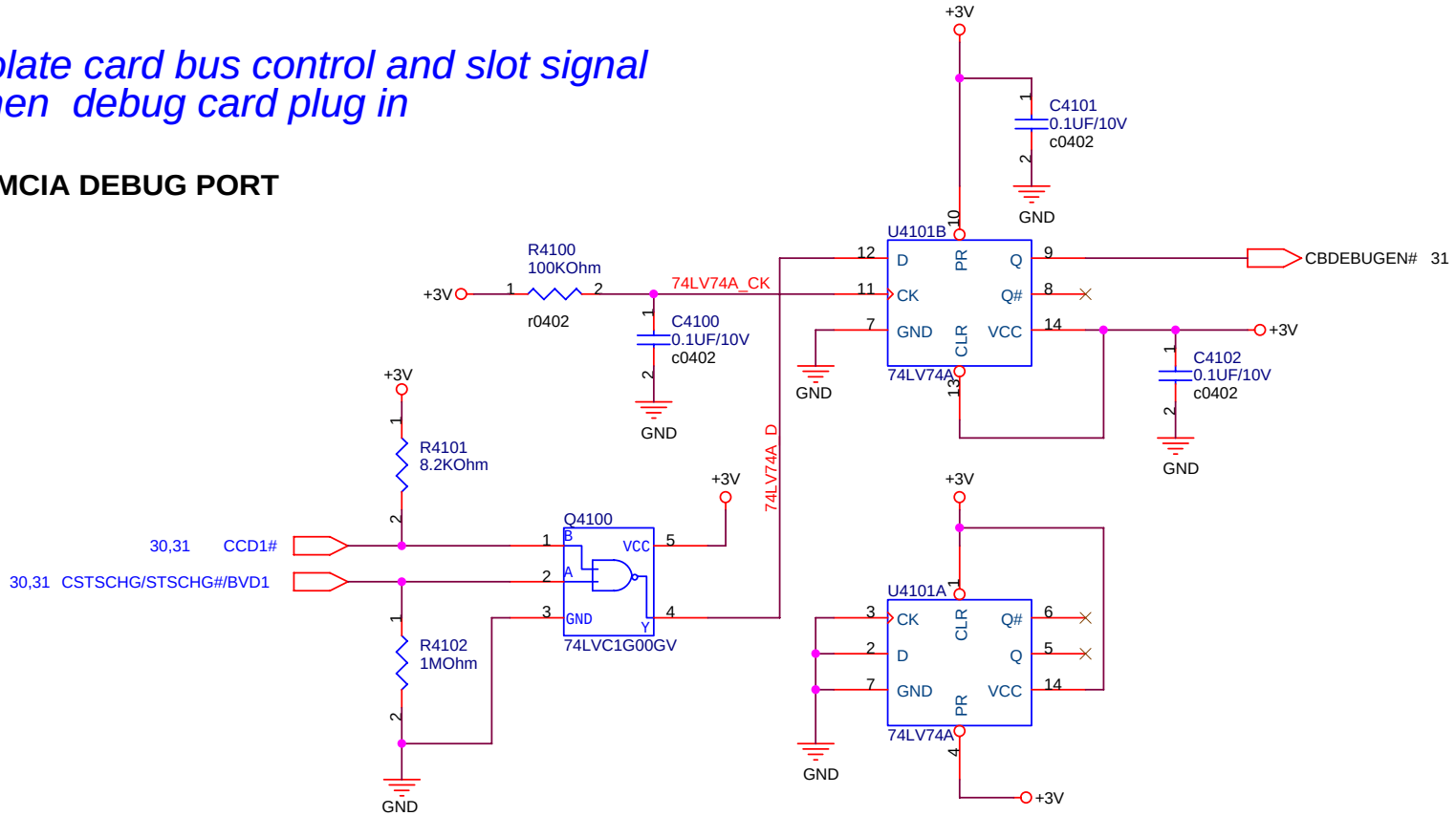


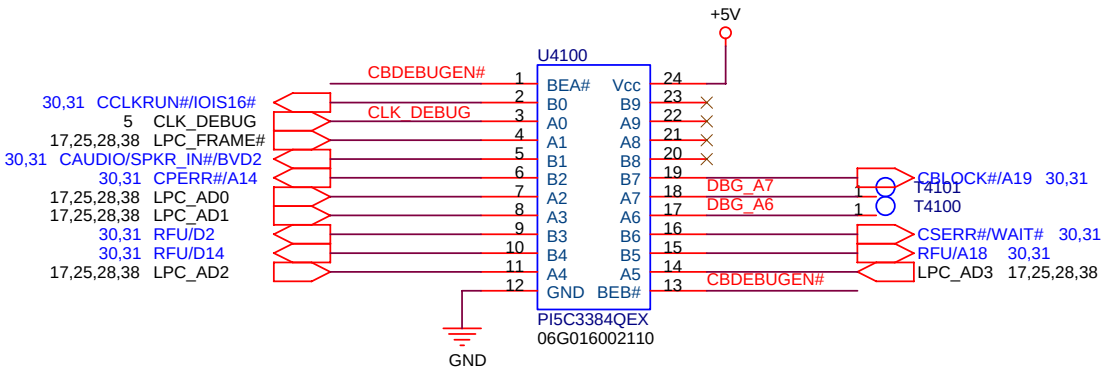


ASUSTeK COMPUTER INC	Title : DC/ BATT IN	
	Engineer: Ping-Yen Tsai	
Size: A4	Project Name: A3F	Rev: 2.0
Date: Wednesday, January 18, 2006	Sheet 40 of 63	

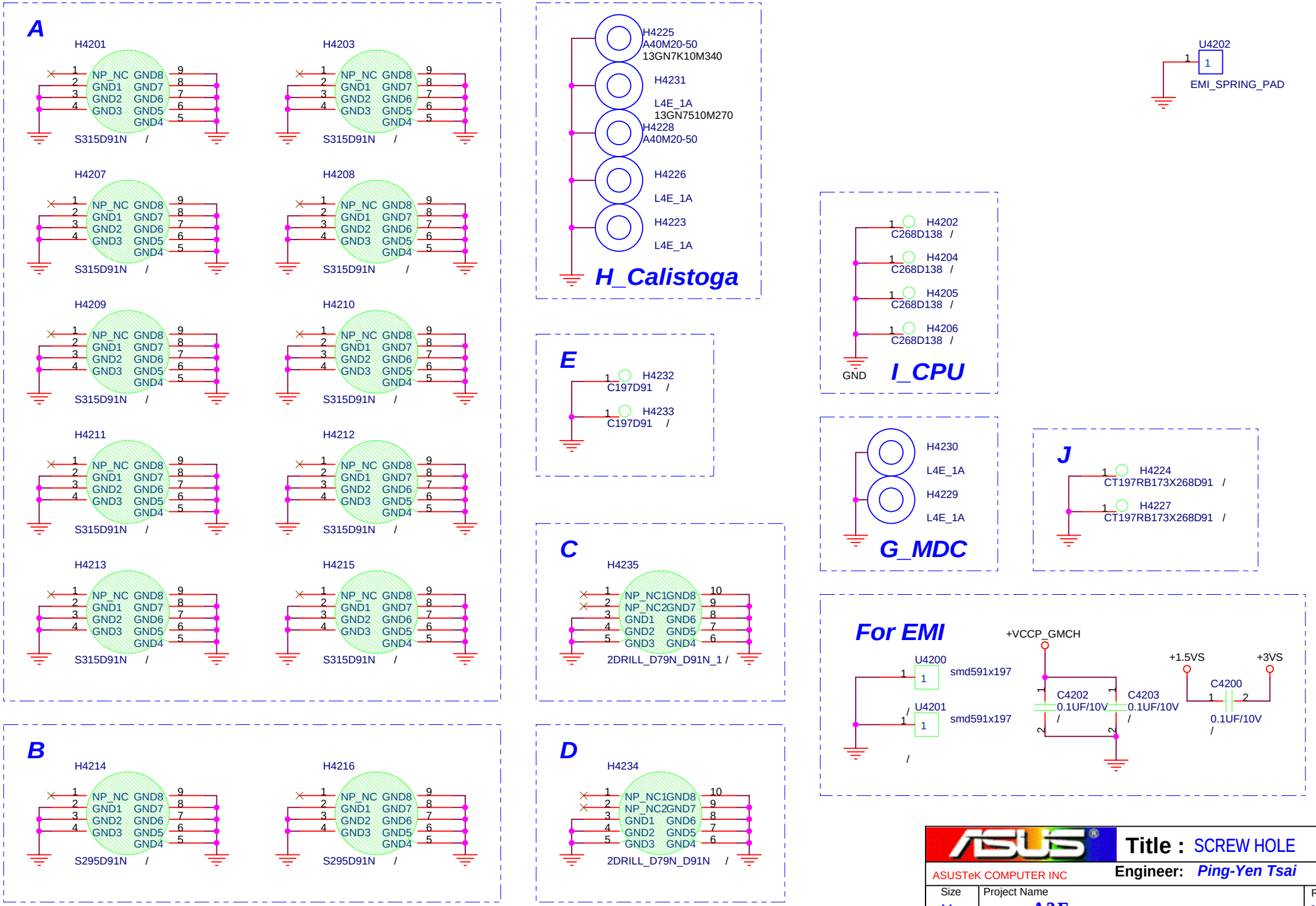
Isolate card bus control and slot signal when debug card plug in

PCMCIA DEBUG PORT





ASUSTeK COMPUTER INC	Title : PCMCIA Debug	
	Engineer: *Ping-Yen Tsai*	
Size: A4	Project Name: **A3F**	Rev: 2.0
Date: Wednesday, January 18, 2006	Sheet 41 of 63	



ASUSTeK COMPUTER INC	Title : SCREW HOLE	
	Engineer: *Ping-Yen Tsai*	
Size: A4	Project Name: **A3F**	Rev: 2.0
Date: Wednesday, January 18, 2006	Sheet 42 of 63	

R1.1

11/14 1. Change resistor number from R1 to R1401
2. Change R1704 value from 10K to 330K
3. Add U2202 C D E F
4. Change C2511 value from 0.1uF to 0.047uF(11G232147316360)
5. Change C2510, C2514 and C2515 value from 0.1uF to 0.33uF(11G232333436030)

11/29 1. Remove R409
2. USB port (J3500) power control on shutdown of AC mode
3. Change U2202 power source form "+3VS" to "+3V" to solve pop noise
4. Add D2202 1N 4148W P/N 07G001001612 to solve pop noise when power off
5. Remove R2201 and mount R2203 to change Gain Setting

12/1 1. Change component D2103 DAP202K to 1N4148W P/N 07G001001612
2. Add Components 10K Ohm & 1N4148W P/N 07G001001612 and connect U2100 pin 30
3. Change J1500,U900,U2502,U3400,H4225,H4226,H4228,H4229,H4230 ,H4223,H4231,Q4400 to green part

12/2 1. Change Thermal Sensor to SO-8 MAX6657
2. USB4-->Camera, USB6-->PB

12/5 1.Change material CE1200, F3500, F3501, F3502
2. Add EC new function-->THRO_CPU
3. Change X3100, C3118, C3119 J3401 part number

12/7 1.Change J2500 footprint

12/9 1.Change R1202 value

R2.0

1/2 1. BOM Add R1943, Remove R1919
2. BOM Add D2105, R2125
3. BOM Add C2223
4. BOM Add R3505, Q3505, U3500
5. Schematics Add R3503, R3504 but don't mount
6. Schematics Add R4418~R4424 but don't mount

1/4 1. change R3709, R3712 & R3713 value

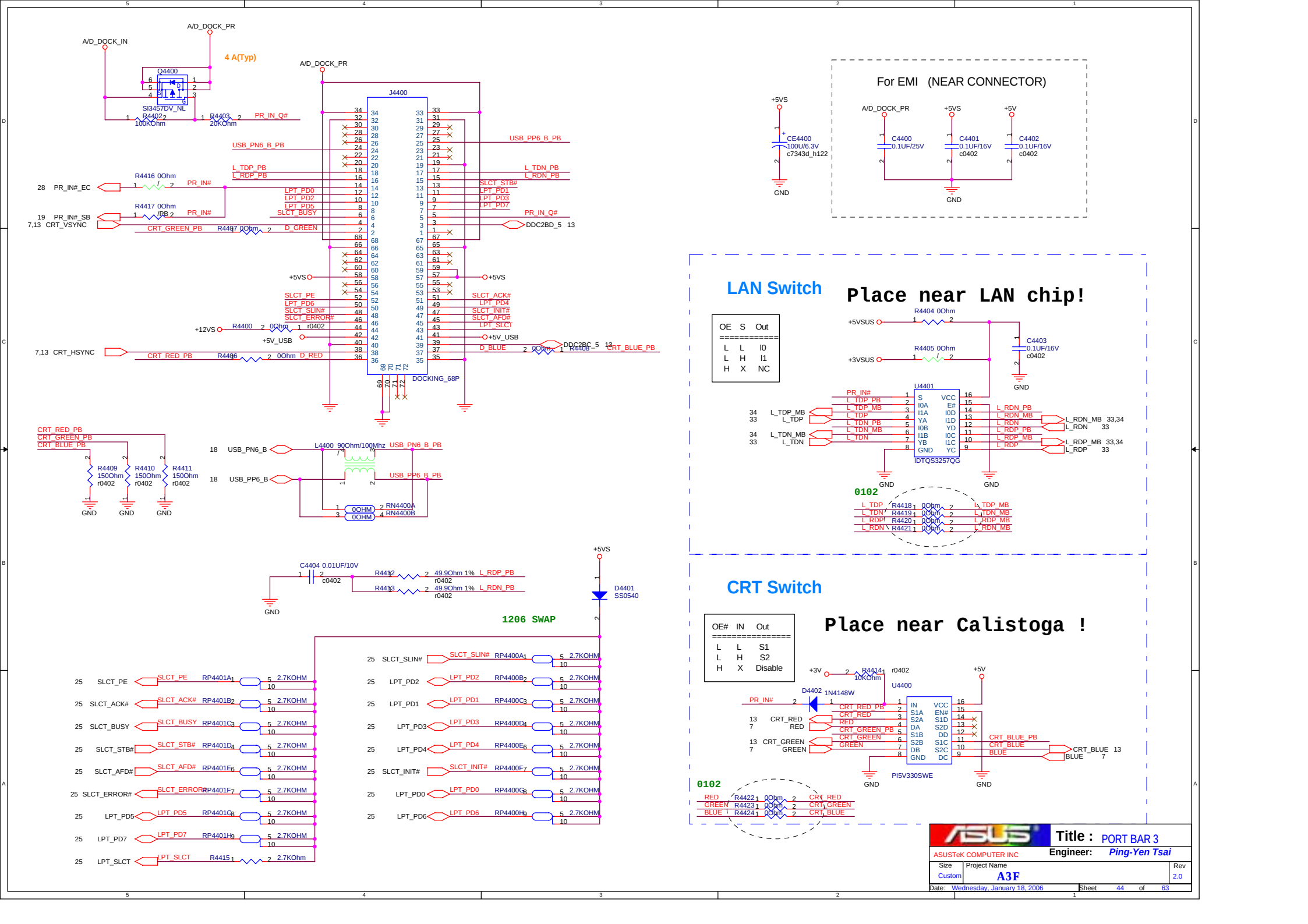
1/6 1. Add Power schematics & GPIO35 (Add R1944,R1945)

1/9 1. Remove JP3500, Add R3506, R3507

1/10 1. Add R415, BOM remove R408 Q403

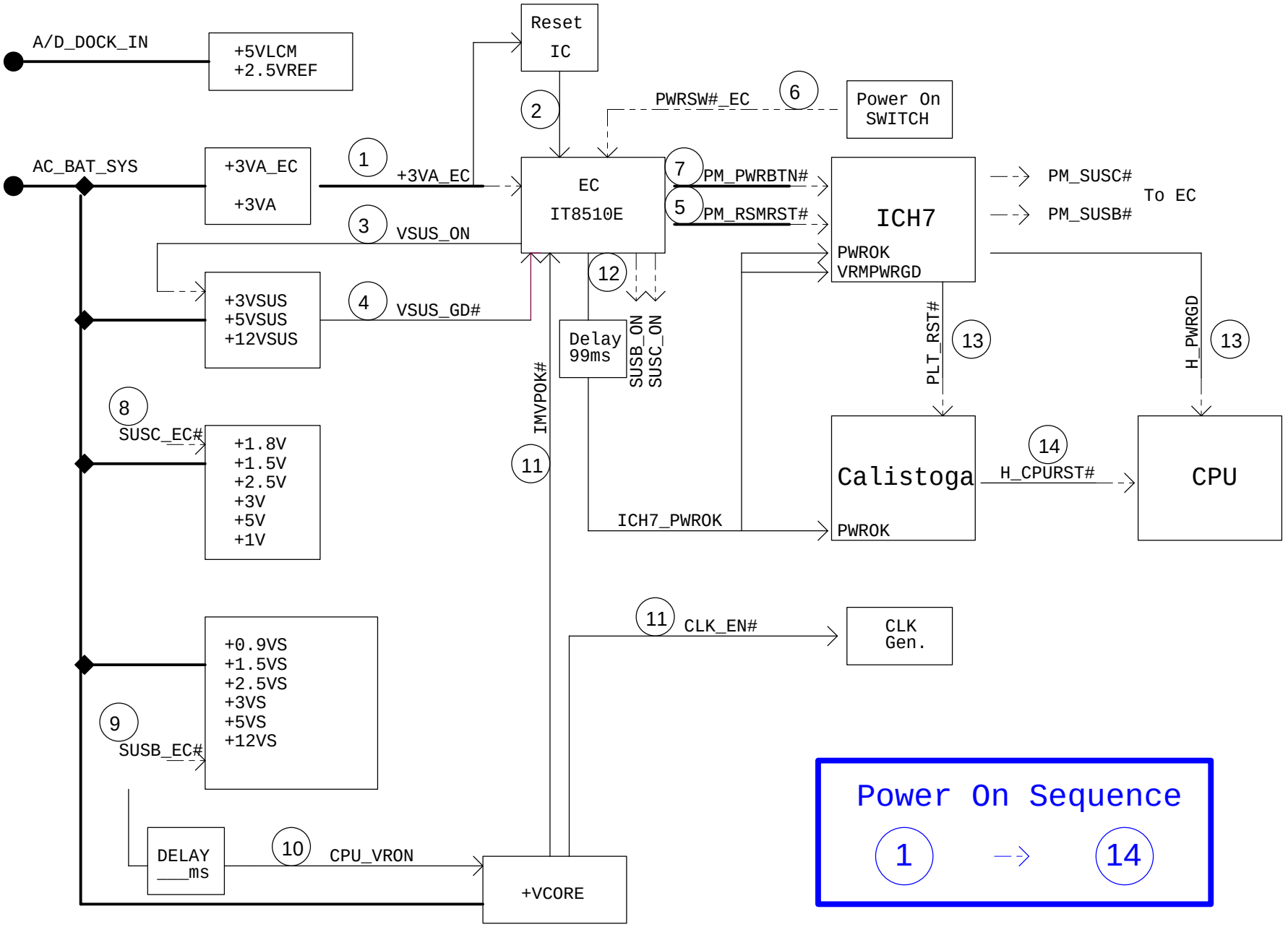
1/11 1. Change C404 to 0.47uF
2. Change DJ JACK part number

ASUSTeK COMPUTER INC	Title : HISTORY	
	Engineer: *Ping-Yen Tsai*	
Size: Custom	Project Name: A3F	Rev: 2.0
Date: Wednesday, January 18, 2006	Sheet 43 of 63	



ASUSTeK COMPUTER INC	Title : PORT BAR 3	
	Engineer: Ping-Yen Tsai	
Size: Custom	Project Name: A3F	Rev: 2.0
Date: Wednesday, January 18, 2006	Sheet 44 of 63	

Title	<Title>
Size A	Document Number A3F
Rev	2.0
Date:	Wednesday, January 18, 2006
Sheet	45 of 63



ASUSTeK COMPUTER INC	Title : FLOWCHART	
	Engineer: Ping-Yen Tsai	
Size: Custom	Project Name: A3F	Rev: 2.0
Date: Wednesday, January 18, 2006	Sheet 46 of 63	

PCI Device	IDSEL#	REQ/GNT#	Interrupts
10/100 RTL8100CL	AD23	2	A
CARD READER	AD17	1	D
CARDBUS	AD17	1	B
1394	AD17	1	C
MINIPCI (802.11a/b/g)	AD19	3	E,F

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	1001100x (98)

ICH7-M GPIO	A3F	Note	Volt
GPIO08	EXTSMI#		+3VSUS
GPIO09	SATA_DET#0		+3VSUS
GPIO12	KBCSCI#		+3VSUS
GPIO13	SIO_SMI#		+3VSUS
GPIO14	PWRLED_1Hz		+3VSUS
GPIO15	802_LED_EN#		+3VSUS
GPIO25	CB_SD#		+3VSUS
GPIO27	WLAN_ON#		+3VSUS
GPIO28	BT_ON		+3VSUS
GPIO36	BT_LED_EN#		+3VS
GPIO37	PCB_ID0		+3VS
GPIO38	PCB_ID1		+3VS
GPIO39	PCB_ID2		+3VS

Title : SYSTEM RESOURCE

ASUSTeK COMPUTER INC

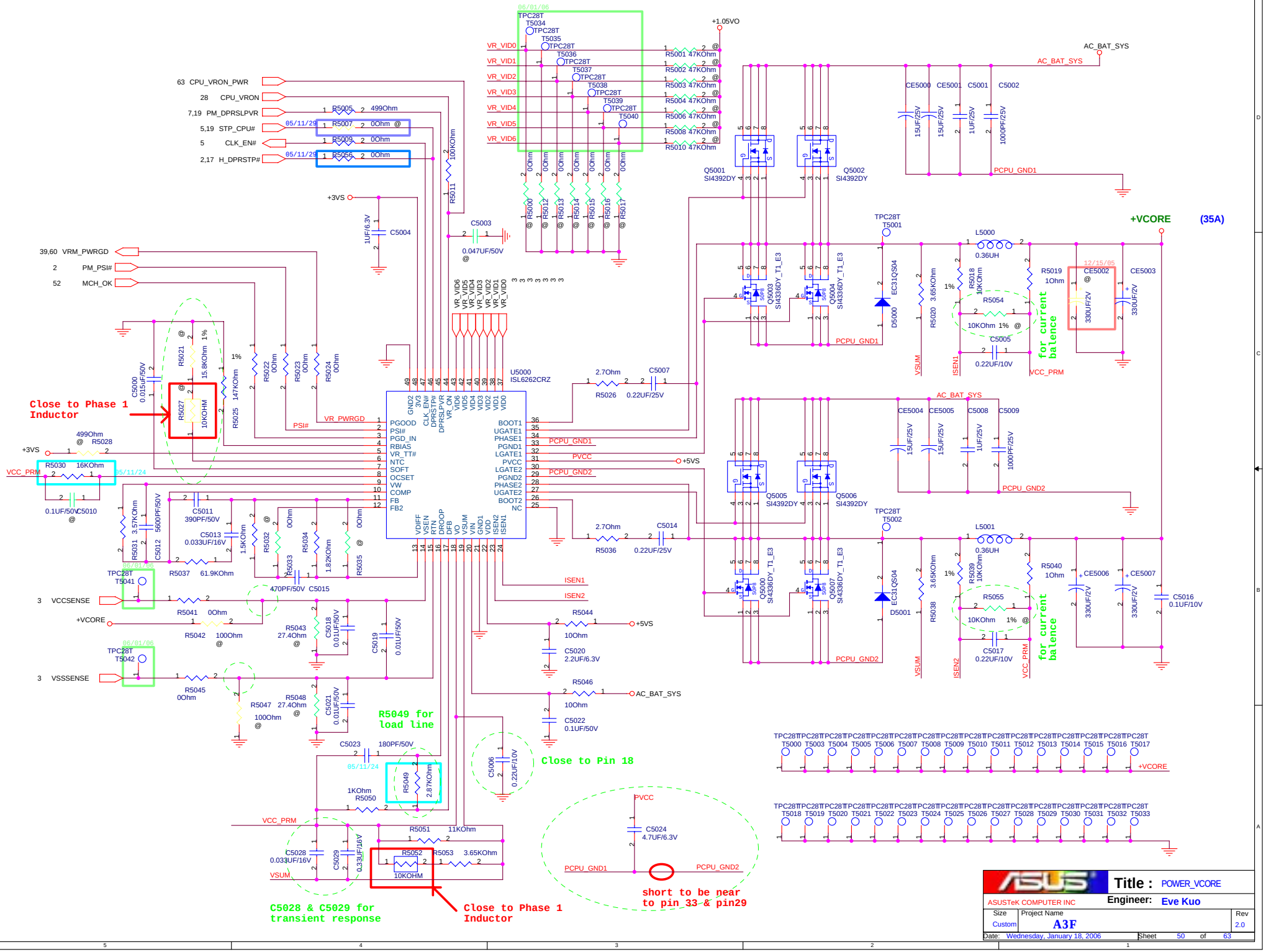
Engineer: *Ping-Yen Tsai*

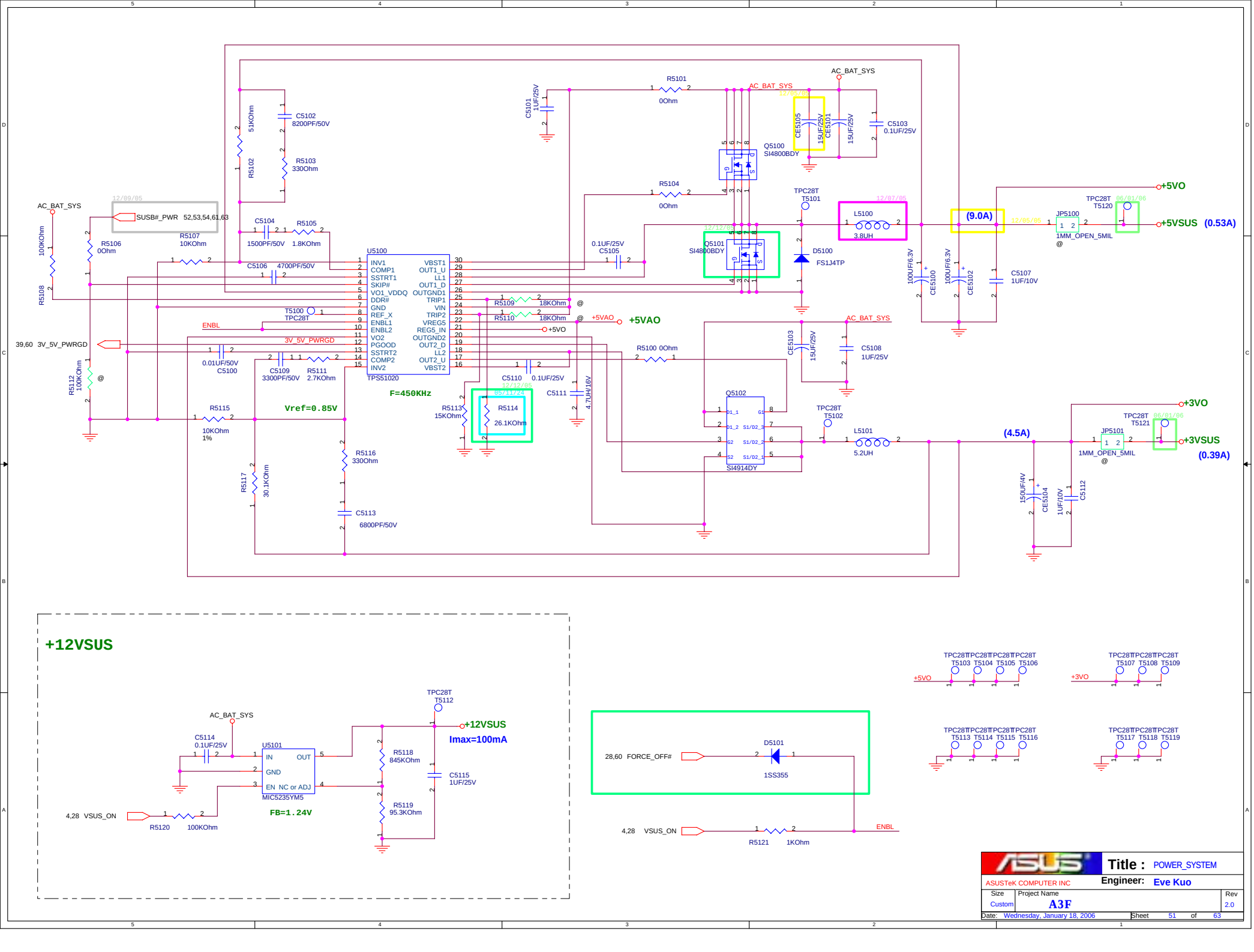
Size	Project Name	Rev
Custom	A3F	2.0

Date: Wednesday, January 18, 2006 Sheet 47 of 63

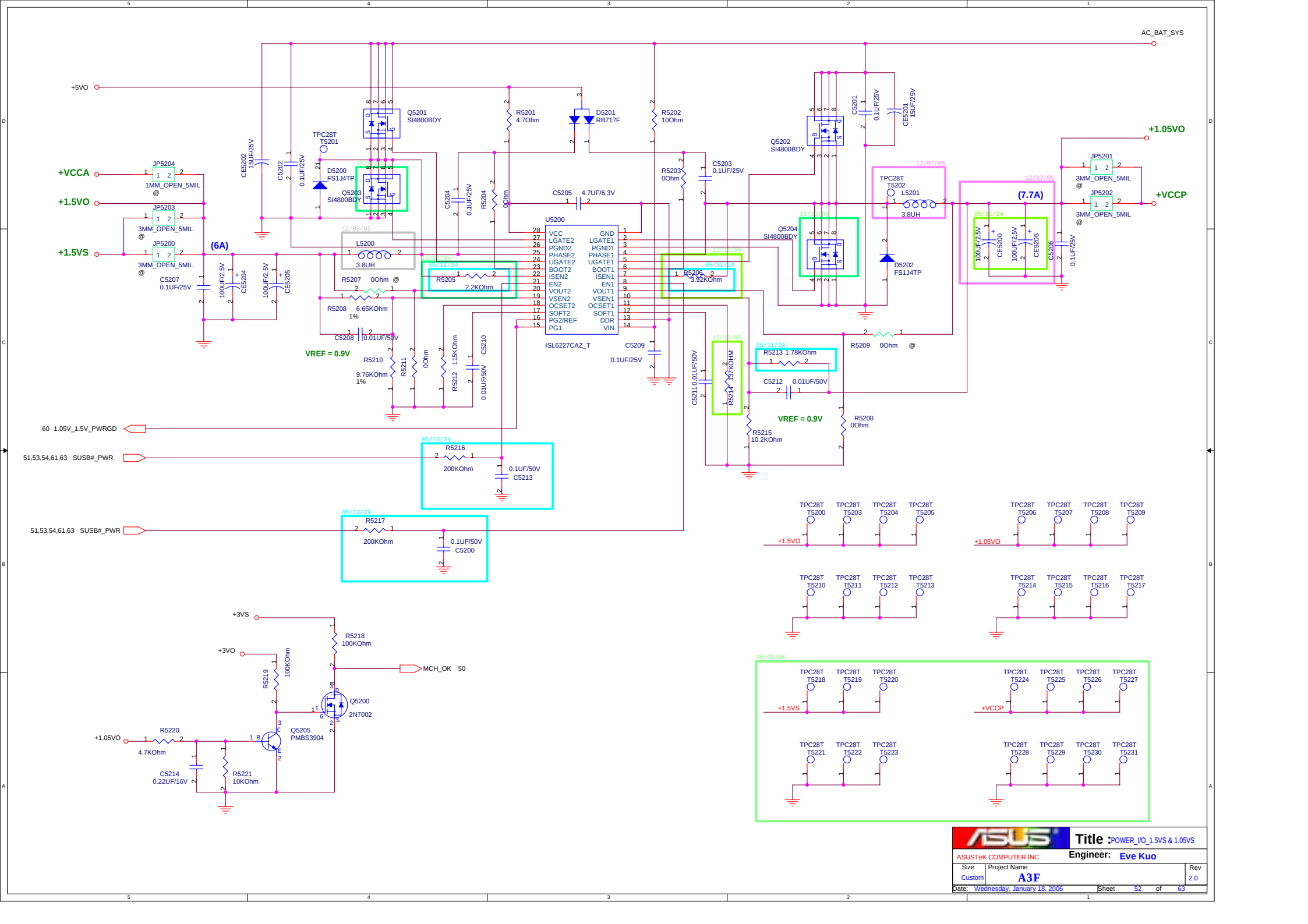
Title	<Title>
Size: CustomA3F	Document Number:	Rev: 2.0
Date: Wednesday, January 18, 2006	Sheet 48 of 63	

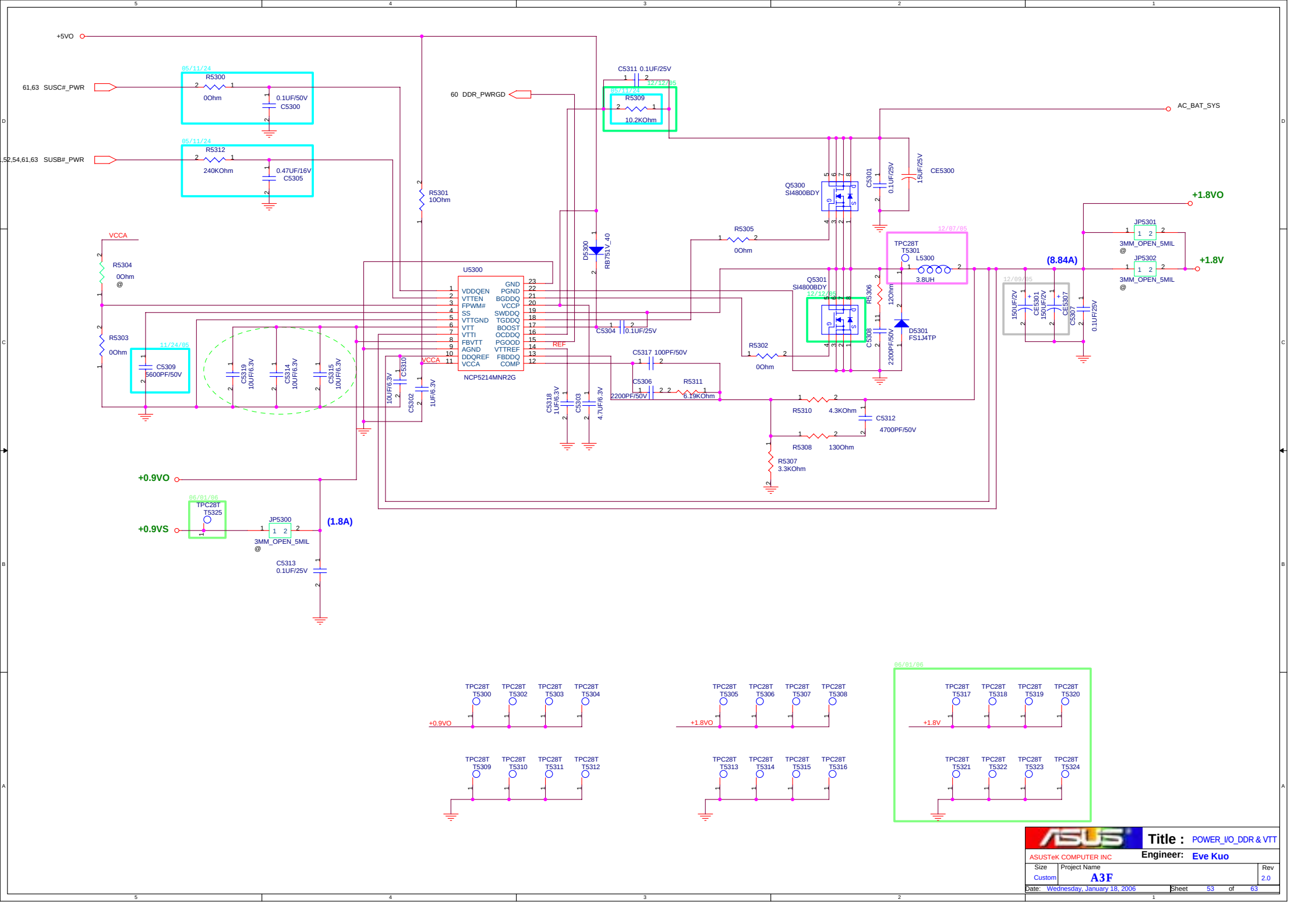
Title	<Title>
Size A	Document Number A3F
Rev	2.0
Date:	Wednesday, January 18, 2006
Sheet	49 of 63


+VCORE (35A)
U5000 ISL6262CRZ
Close to Phase 1 Inductor
R5049 for load line
Close to Pin 18
C5028 & C5029 for transient response
Close to Phase 1 Inductor
short to be near to pin 33 & pin29
for current balence
for current balence
Title : POWER_VCORE
ASUSTeK COMPUTER INC
Engineer: Eve Kuo
Size Custom
Project Name A3F
Rev 2.0
Date: Wednesday, January 18, 2006
Sheet 50 of 63



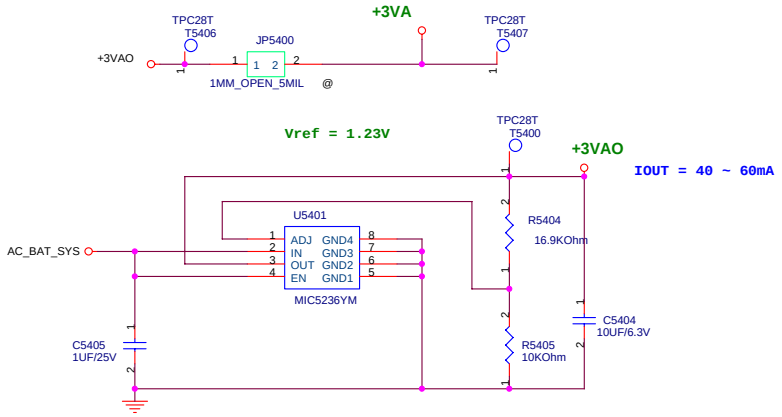
ASUSTeK COMPUTER INC	Title : POWER_SYSTEM	
	Engineer: Eve Kuo	
Size: Custom	Project Name: A3F	Rev: 2.0
Date: Wednesday, January 18, 2006	Sheet 51 of 63	


AC_BAT_SYS
+5VO
+VCCA
+1.5VO
+1.5VS
(6A)
JP5204
1MM_OPEN_5MIL
JP5203
3MM_OPEN_5MIL
JP5200
3MM_OPEN_5MIL
C5207 0.1UF/25V
CE5204 100UF/2.5V
CE5205 100UF/2.5V
CE5202 15UF/25V
C5202 0.1UF/25V
TPC28T T5201
D5200 FS1J4TP
Q5201 SI4800BDY
Q5203 SI4800BDY
R5201 4.7Ohm
D5201 RB717F
R5202 10Ohm
R5203 0Ohm
C5203 0.1UF/25V
C5204 0.1UF/25V
R5204 0Ohm
C5205 4.7UF/6.3V
L5200 3.8UH
R5205 2.2KOhm
R5206 3.92KOhm
R5207 0Ohm @
R5208 6.65KOhm 1%
C5208 0.01UF/50V
VREF = 0.9V
R5210 9.76KOhm 1%
R5211 0Ohm
R5212 115KOhm
C5210 0.01UF/50V
U5200
VCC LGATE2 PGND2 PHASE2 UGATE2 BOOT2 ISEN2 EN2 VOUT2 VSEN2 OCSET2 SOFT2 PG2/REF PG1
GND LGATE1 PGND1 PHASE1 UGATE1 BOOT1 ISEN1 EN1 VOUT1 VSEN1 OCSET1 SOFT1 DDR VIN
ISL6227CAZ_T
C5209 0.1UF/25V
Q5202 SI4800BDY
Q5204 SI4800BDY
C5201 0.1UF/25V
CE5201 15UF/25V
TPC28T T5202
L5201 3.8UH
D5202 FS1J4TP
(7.7A)
CE5200 100UF/2.5V
CE5206 100UF/2.5V
C5206 0.1UF/25V
+1.05VO
+VCCP
JP5201
3MM_OPEN_5MIL
JP5202
3MM_OPEN_5MIL
R5213 1.78KOhm
C5212 0.01UF/50V
R5209 0Ohm @
C5211 0.01UF/50V
R5214 127KOHM
R5215 10.2KOhm
R5200 0Ohm
60 1.05V_1.5V_PWRGD
51,53,54,61,63 SUSB#_PWR
R5216 200KOhm
C5213 0.1UF/50V
R5217 200KOhm
C5200 0.1UF/50V
+3VS
+3VO
R5218 100KOhm
R5219 100KOhm
MCH_OK 50
Q5200 2N7002
Q5205 PMBS3904
R5220 4.7KOhm
C5214 0.22UF/16V
R5221 10KOhm
TPC28T T5200 T5203 T5204 T5205
TPC28T T5206 T5207 T5208 T5209
TPC28T T5210 T5211 T5212 T5213
TPC28T T5214 T5215 T5216 T5217
TPC28T T5218 T5219 T5220
TPC28T T5221 T5222 T5223
TPC28T T5224 T5225 T5226 T5227
TPC28T T5228 T5229 T5230 T5231
Title : POWER_I/O_1.5VS & 1.05VS
ASUSTeK COMPUTER INC
Engineer: Eve Kuo
Size Custom
Project Name A3F
Rev 2.0
Date: Wednesday, January 18, 2006
Sheet 52 of 63

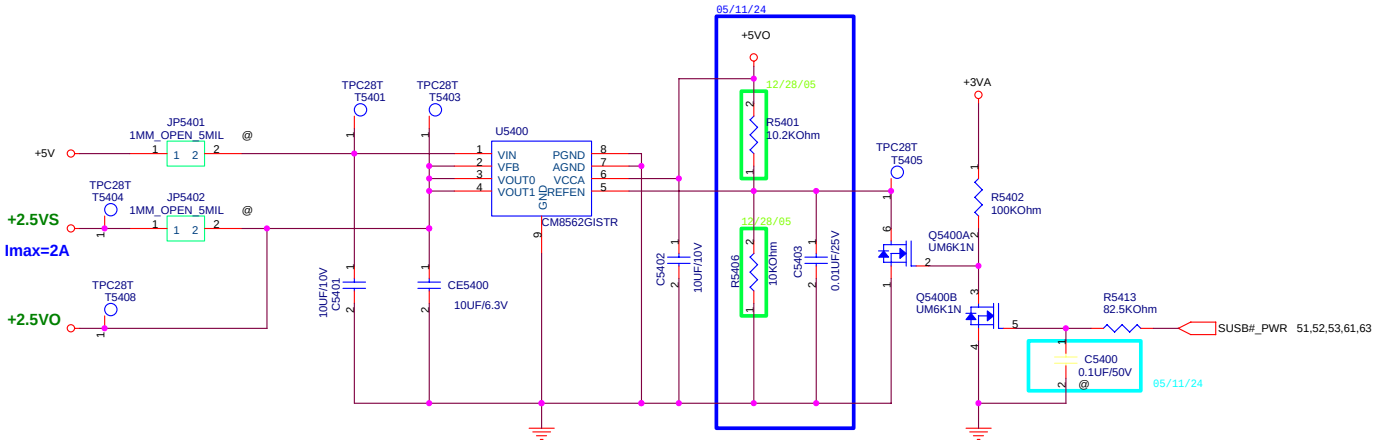


ASUSTeK COMPUTER INC	Title : POWER_I/O_DDR & VTT	
	Engineer: Eve Kuo	
Size: Custom	Project Name: A3F	Rev: 2.0
Date: Wednesday, January 18, 2006	Sheet 53 of 63	

+3VA0



+2.5VS



ASUSTeK COMPUTER INC	Title : POWER_I/O_+3VA & +2.5VS	
	Engineer: Eve Kuo	
Size: Custom	Project Name: A3F	Rev: 2.0
Date: Wednesday, January 18, 2006	Sheet 54 of 63	

R1.0

Item	Before	After	Reason	Owner	Date

R1.1

Item	Before	After	Reason	Owner	Date

R2.0

Item	Before	After	Reason	Owner	Date

ASUSTeK COMPUTER INC

Title : POWER_HISTORY

Engineer: Eve Kuo

Size	Project Name	Rev
C	A3F	2.0

Date: Wednesday, January 18, 2006 Sheet 55 of 63

Title : N/A

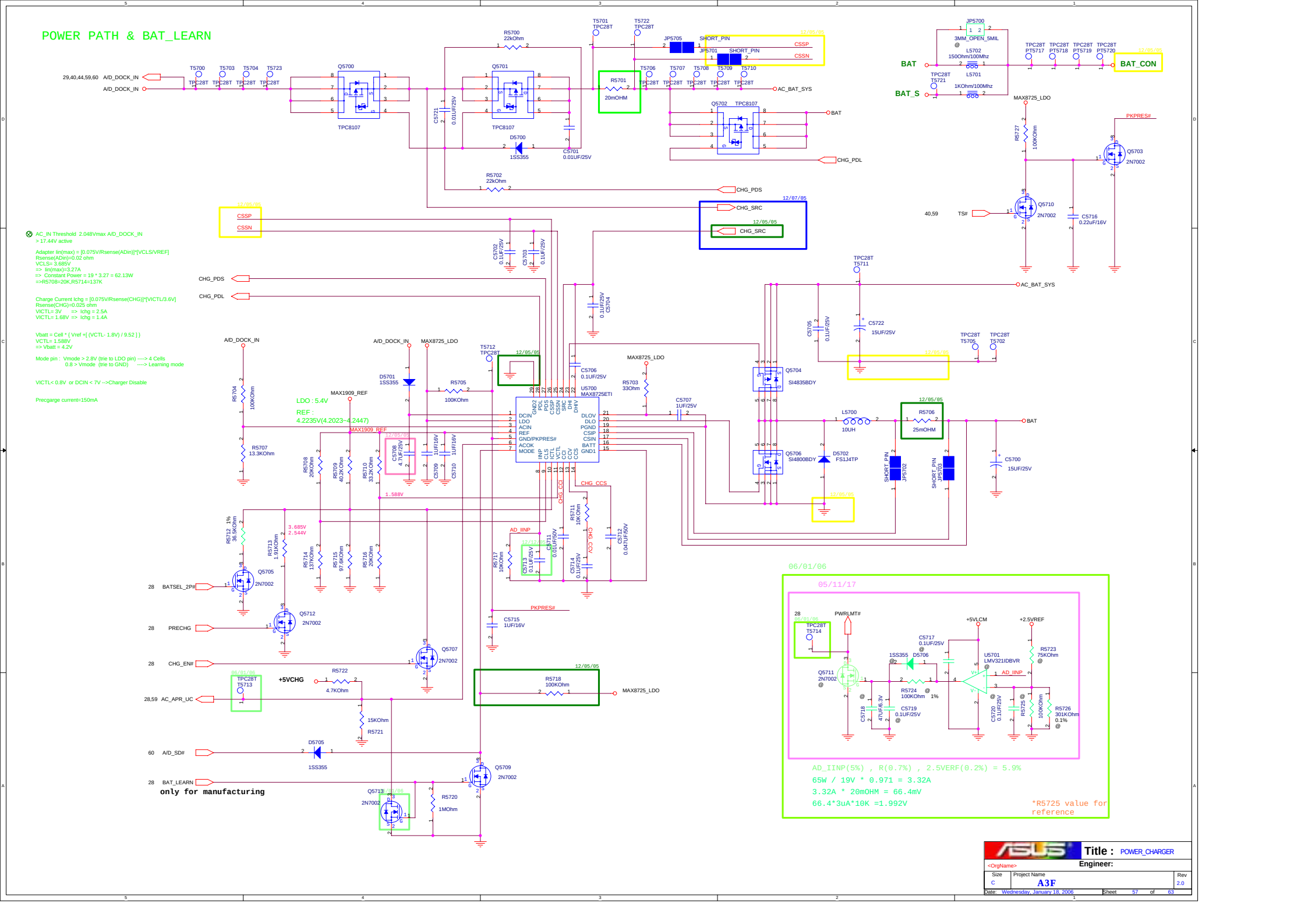
Engineer: *Eve Kuo*

ASUSTeK COMPUTER INC

Size	Project Name	Rev
C	A3F	2.0

Date: Wednesday, January 18, 2006 Sheet 56 of 63

POWER PATH & BAT_LEARN



Title : N/A

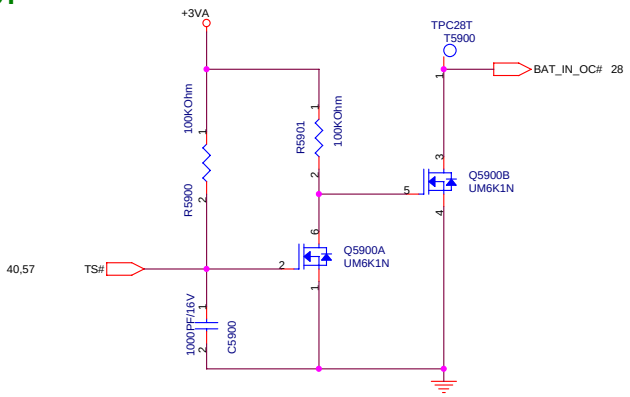
Engineer: Eve Kuo

ASUSTeK COMPUTER INC

Size	Project Name	Rev
C	A3F	2.0

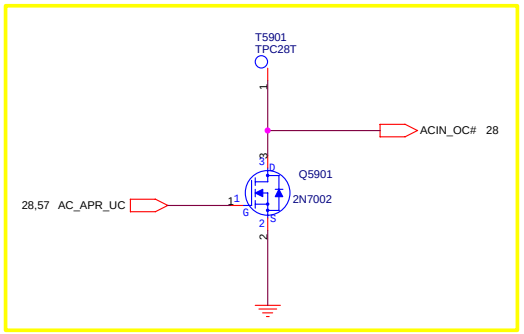
Date: Wednesday, January 18, 2006 Sheet 58 of 63

BATTERY IN DETECT

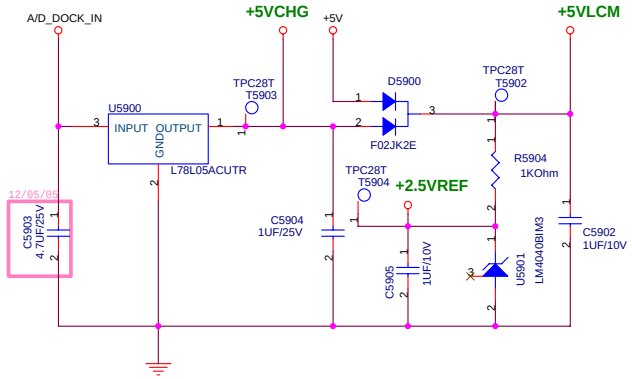


ADAPTER IN DETECT

05/11/07

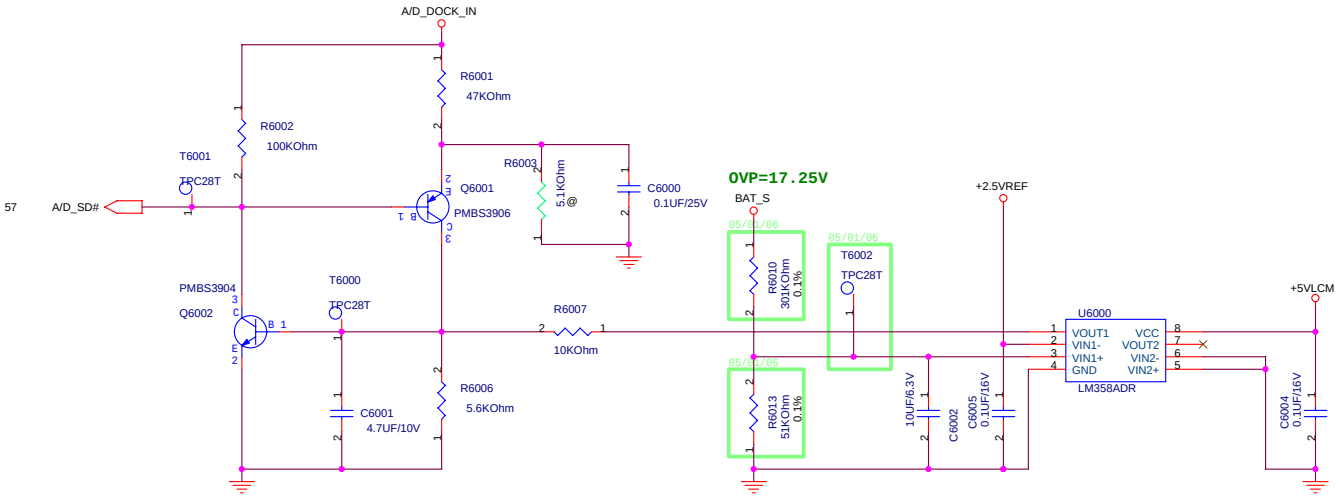


+5VLCM, +5VCHG & +2.5VREF

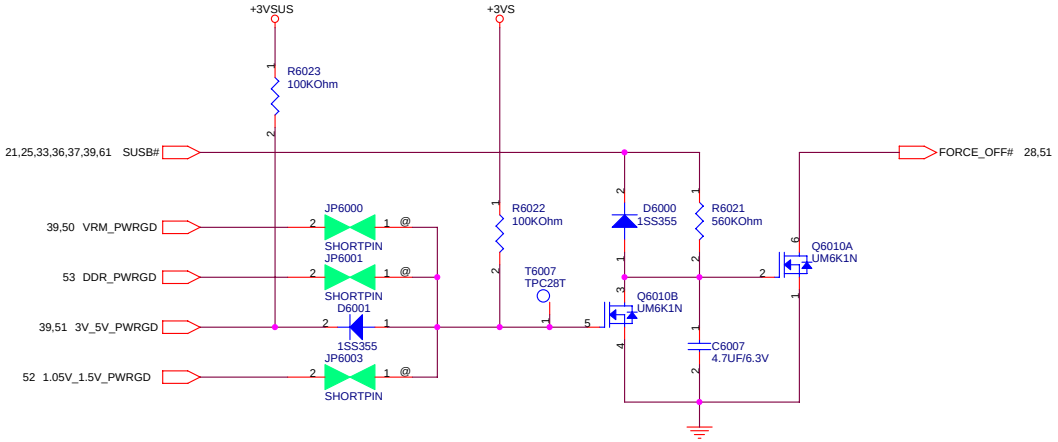


ASUSTeK COMPUTER INC	Title : POWER_DETECT	
	Engineer: Eve Kuo	
Size: Custom	Project Name: A3F	Rev: 2.0
Date: Wednesday, January 18, 2006	Sheet 59 of 63	

BATTERY A/D_SD# (OVP)



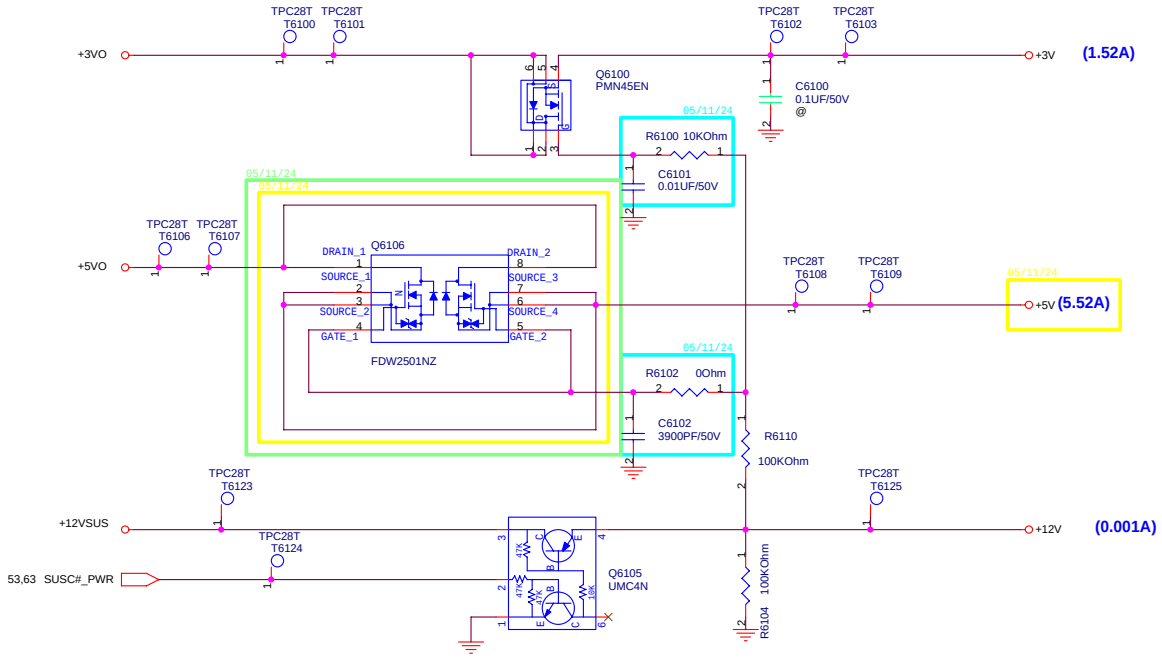
POWER GOOD DETECTER

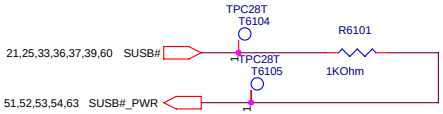


TPC28T T6003 1 VRM_PWRGD
TPC28T T6004 1 DDR_PWRGD
TPC28T T6005 1 3V_5V_PWRGD
TPC28T T6006 1 1.05V_1.5V_PWRGD

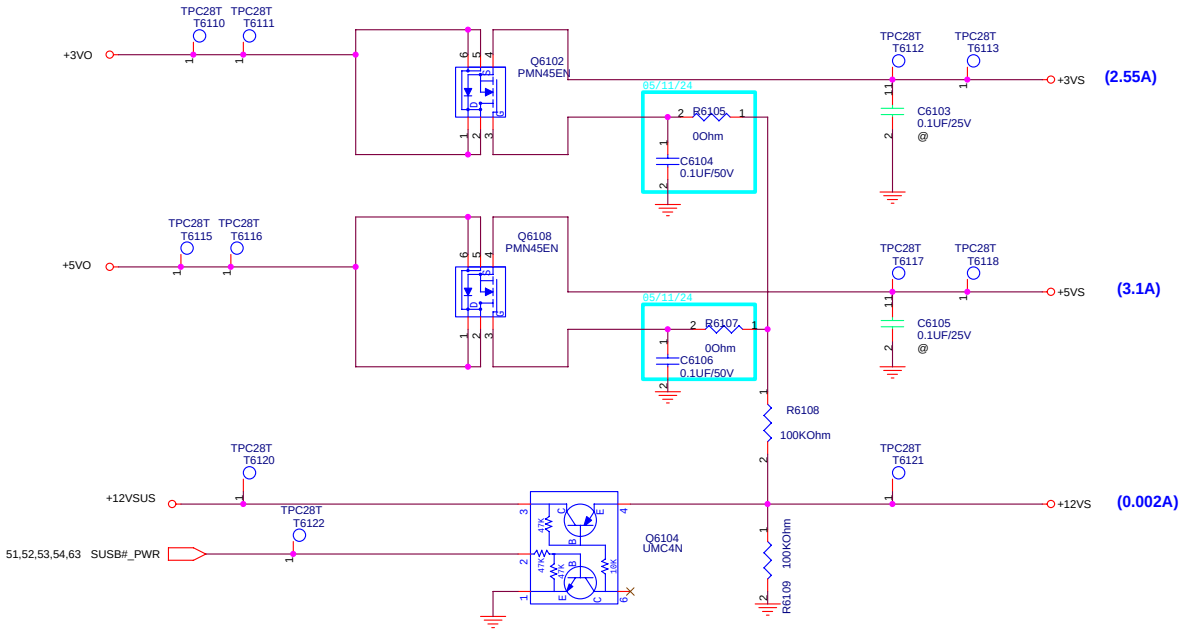
ASUSTeK COMPUTER INC	Title : POWER_PROTECT	
	Engineer: Eve Kuo	
Size: Custom	Project Name: A3F	Rev: 2.0
Date: Wednesday, January 18, 2006	Sheet 60 of 63	

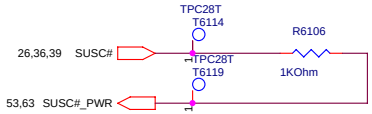
SUSC#_PWR POWER



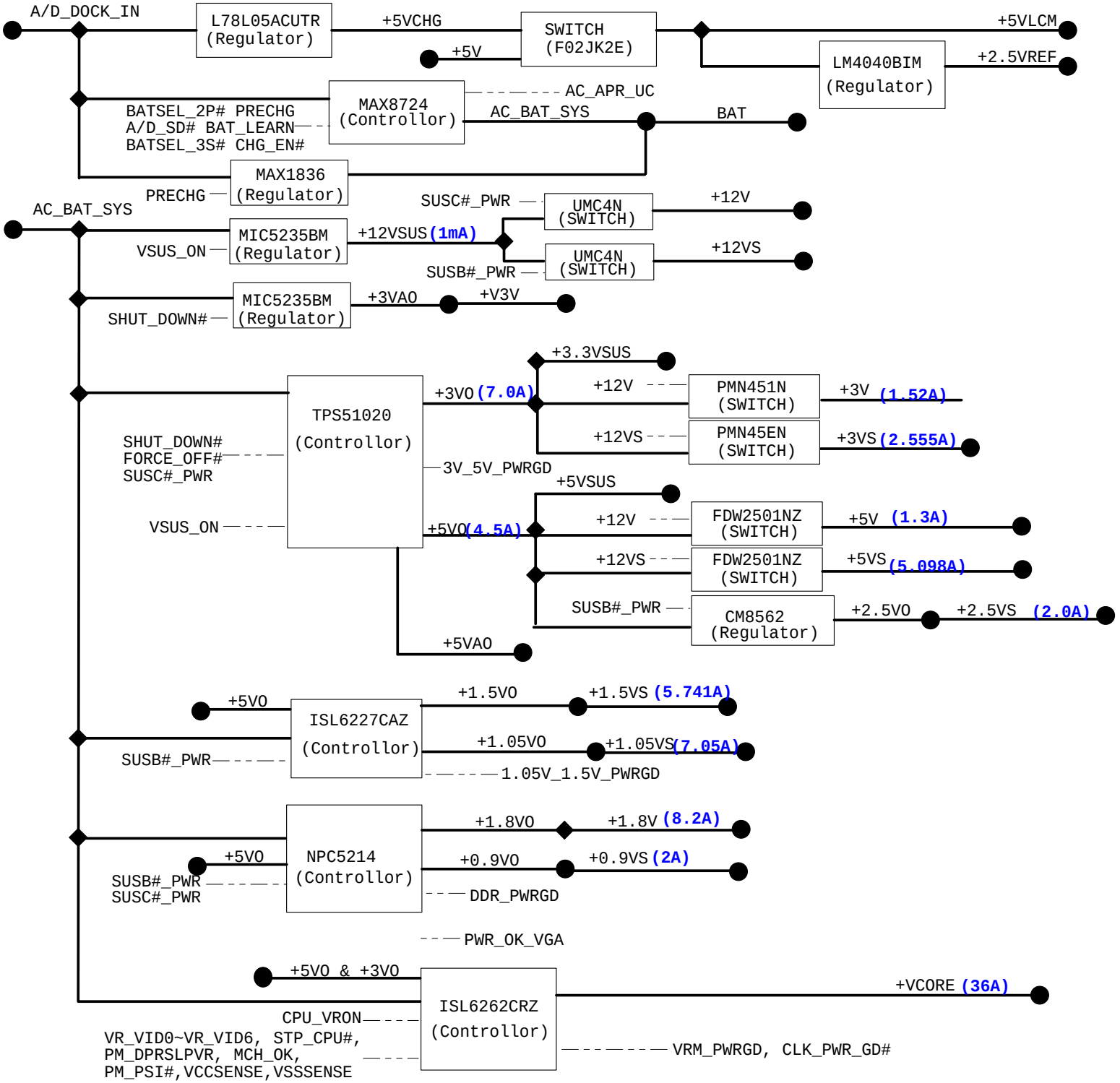


SUSB#_PWR POWER





Title :	POWER_LOAD SWITCH	
ASUSTeK COMPUTER INC	Engineer:	Eve Kuo
Size: Custom	Project Name: A3F	Rev: 2.0
Date: Wednesday, January 18, 2006	Sheet 61 of 63	



ASUSTeK COMPUTER INC	Title : POWER_FLOWCHART	
	Engineer: Eve Kuo	
Size: Custom	Project Name: A3F	Rev: 2.0
Date: Wednesday, January 18, 2006	Sheet 62 of 63	

AC_BAT_SYS → AC_BAT_SYS 12,50,51,52,53,54,57

+3VA → +3VA 4,12,20,28,37,39,54,59

+5VO → +5VO 51,52,53,54,61

+3VO → +3VO 51,52,61

+3VSUS → +3VSUS 18,19,20,28,33,34,35,37,39,44,51,60

+5VSUS → +5VSUS 20,35,36,37,44,51

+3V → +3V 12,18,22,26,30,31,32,34,36,38,41,44,61

+3VS → +3VS 4,5,7,9,11,12,13,14,15,19,20,21,22,25,26,27,28,30,36,38,39,42,50,52,60,61

+12VSUS → +12VSUS 35,51,61

+12V → +12V 4,35,36,61

+12VS → +12VS 12,22,36,44,61

+5V → +5V 9,12,22,25,31,35,36,37,41,44,54,59,61

+5VS → +5VS 4,13,19,20,21,22,27,28,36,37,38,44,50,61

+2.5VO → +2.5VO 54

+2.5VS → +2.5VS 9,13,36,54

+1.8VO → +1.8VO 53

+1.8V → +1.8V 7,10,14,15,36,53

+0.9VS → +0.9VS 16,36,53

BAT → BAT 29,57

+5VCHG → +5VCHG 57,59

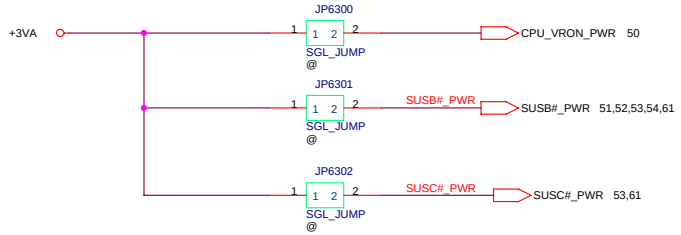
+5VLCM → +5VLCM 37,57,59,60

+2.5VREF → +2.5VREF 57,59,60

+VCORE → +VCORE 3,50

BAT_CON → BAT_CON 40,57

FOR POWER TEST



ASUSTeK COMPUTER INC	Title : POWER_SIGNAL	
	Engineer: Eve Kuo	
Size: Custom	Project Name: A3F	Rev: 2.0
Date: Wednesday, January 18, 2006	Sheet 63 of 63	