


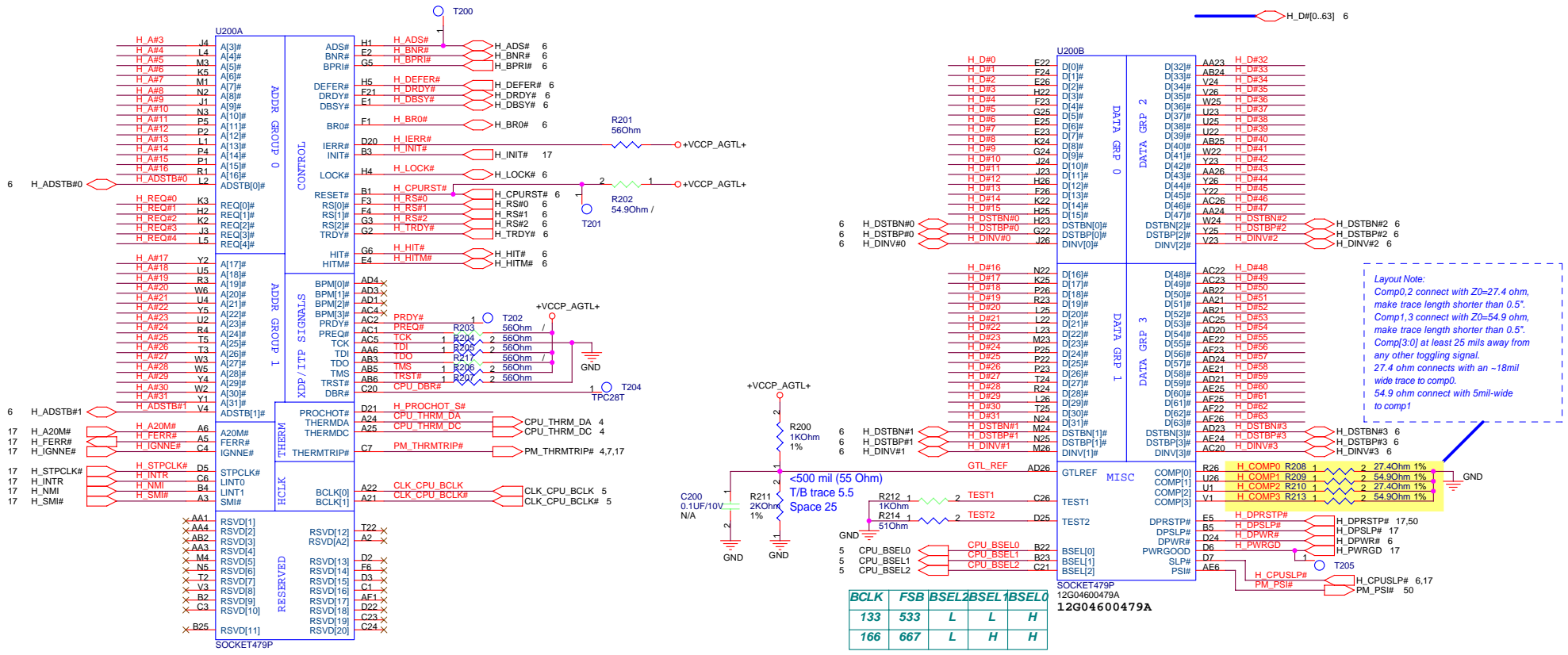


6 H_A#16..3] 
 6 H_REQ#4..0] 
 6 H_A#31..17] 

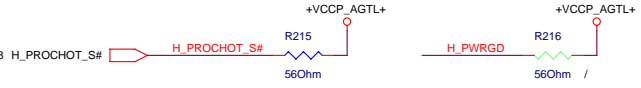
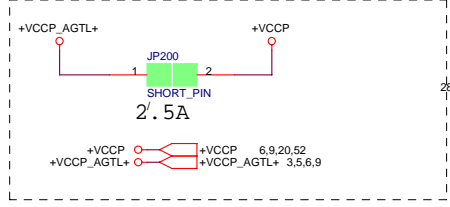
H_D#0..63] 6 



Layout Note:
 Comp0,2 connect with Z0=27.4 ohm, make trace length shorter than 0.5".
 Comp1,3 connect with Z0=54.9 ohm, make trace length shorter than 0.5".
 Comp(3,0) at least 25 mils away from any other toggling signal.
 27.4 ohm connects with an ~18mil wide trace to comp0.
 54.9 ohm connect with 5mil-wide to comp1

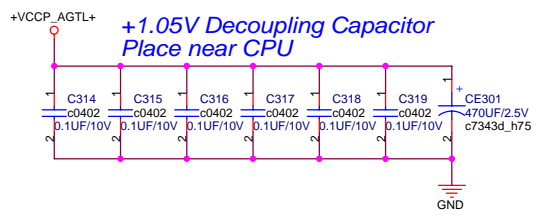
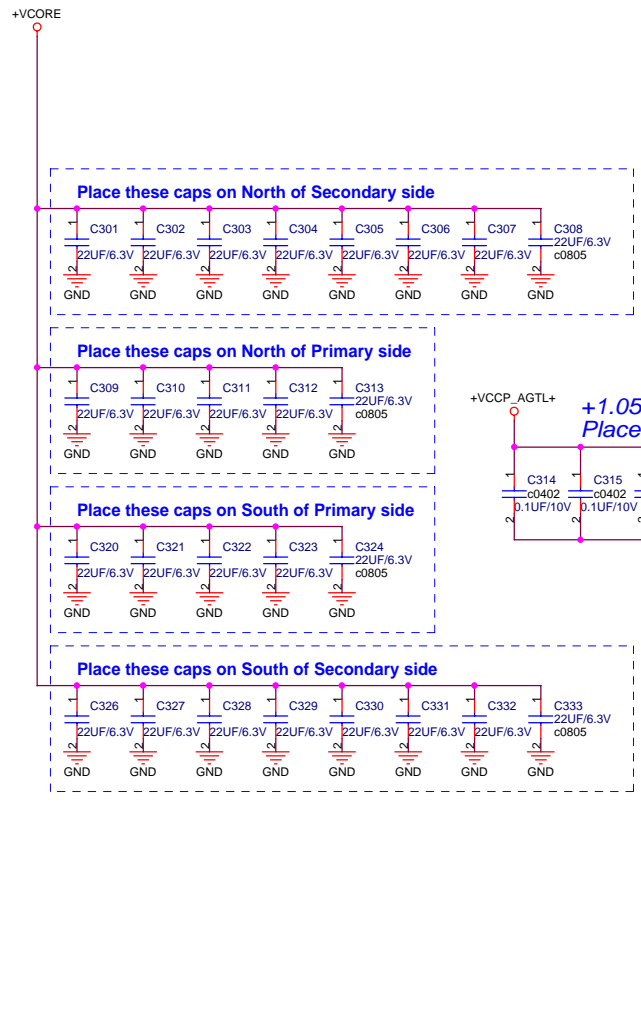
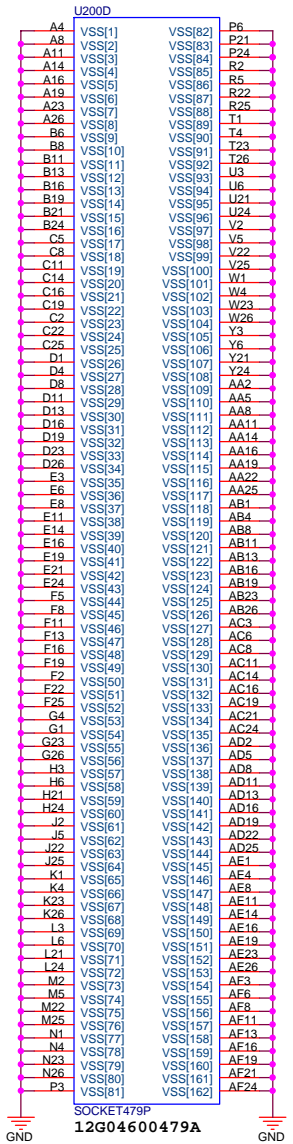
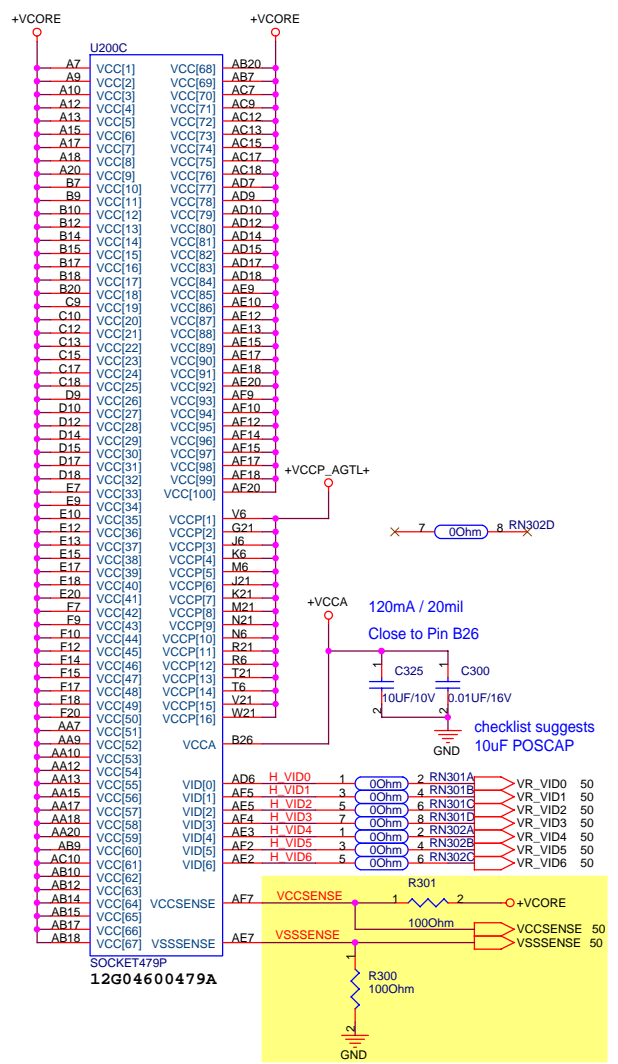
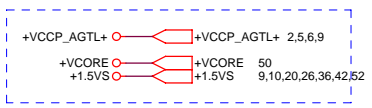
12G04600479A

68 ± 5% pull-up to Vcc1_05
 If PROCHOT# is not used, then it must be terminated with a 56 pull-up resistor to VCCP.
 If PROCHOT# is routed between CPU, IMVP and MCH, pull-up resistor has to be 75 Ohm ± 5%



YUNAH FSB667			
LFM	TYP	HFM	
VCC	1.14V	1.2V	1.356V
C4	C3	C0	
ICC	0.9A	7.59A	27A

YUNAH FSB667			
Min	Typ	Max	
VCCP	0.997V	1.05V	1.102V
Min	Typ	Max	
ICCP			2.5A



Layout Note:
 VCCSENSE/VSSSENSE lines between the CPU and the VR should have a trace width of 18 mils on 7 mils spacing, with trace impedance of $Z_0 \approx 27.4 \text{ Ohm}$.
 The VCCSENSE/VSSSENSE should be length matched to within 25 mils.
 These resistors should be placed within 2 inch of the CPU.

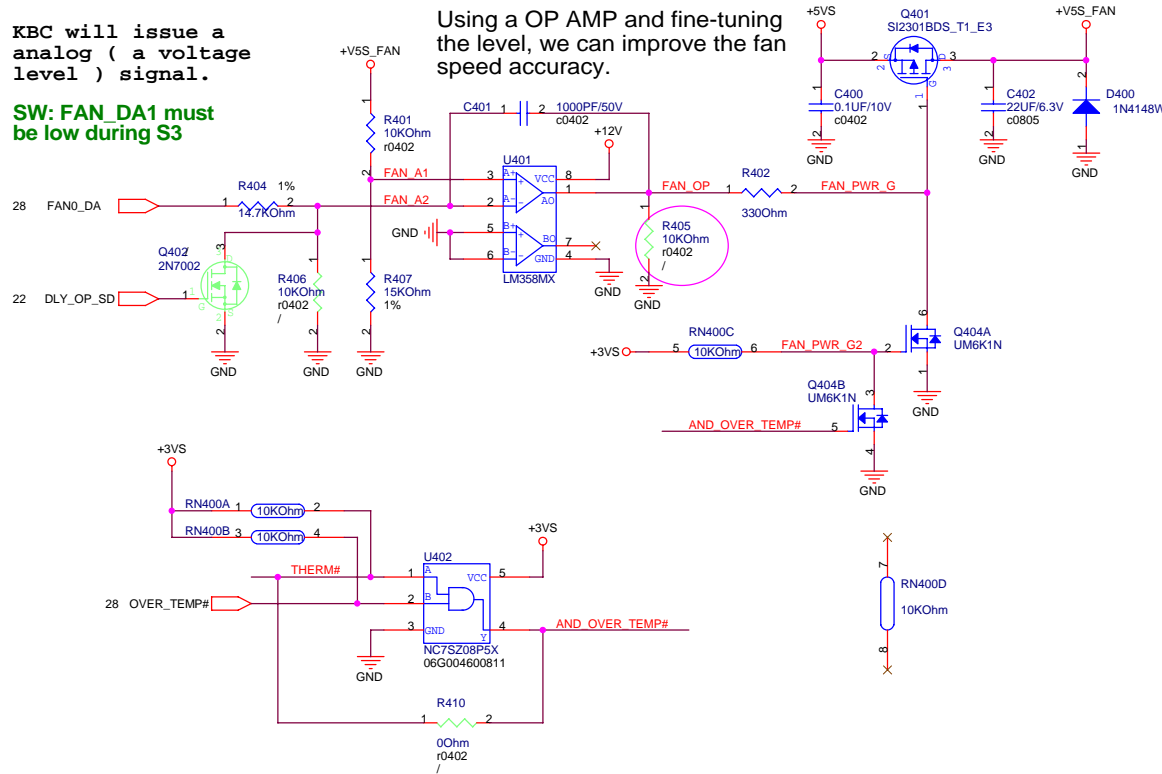
Fan Speed Control

+12V	32,36,61
+5VS	13,19,20,21,22,27,28,36,37,38,44,50,61
+3VS	5,7,9,11,12,13,14,15,19,20,21,22,25,26,27,28,30,36,38,39,42,50,52,60,61
+3VA	12,20,28,37,39,54,59,63

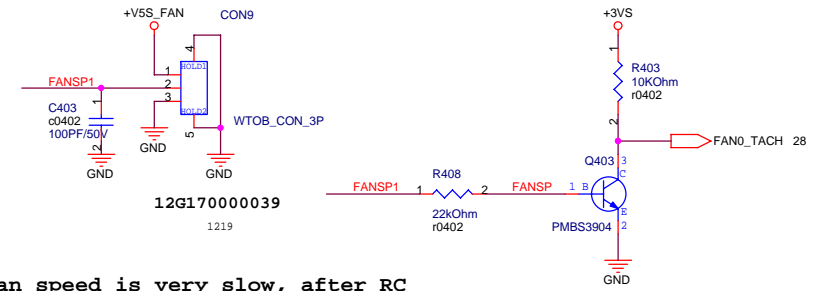
KBC will issue a analog (a voltage level) signal.

SW: FAN_DA1 must be low during S3

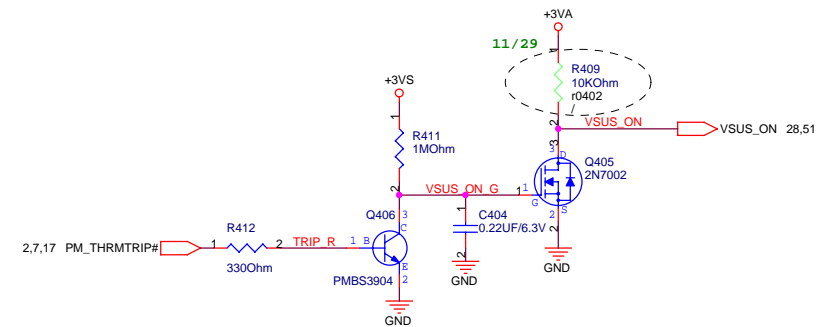
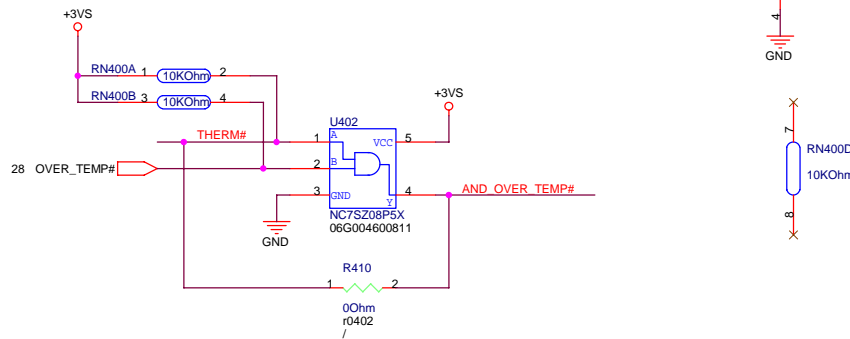
Using a OP AMP and fine-tuning the level, we can improve the fan speed accuracy.



CPU FAN



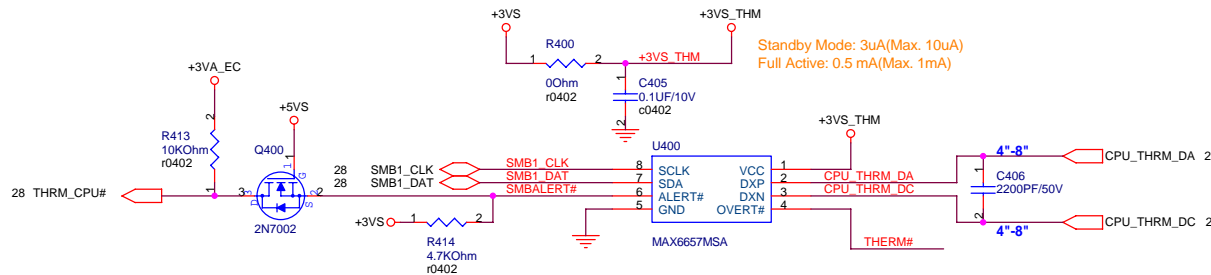
When fan speed is very slow, after RC integrator the level of FANSP1 will be very low that may make south bridge do the wrong detection.



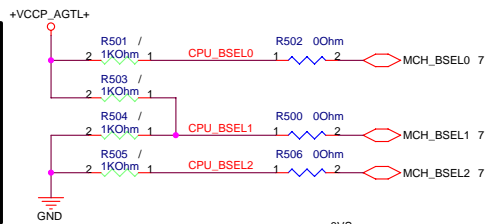
Route H_THERMDA and H_THERMDC on the same layer

- OTHER SIGNALS
- 12 mils
- =====GND
- 10 mils
- =====H_THERMDA(10 mils)
- 10 mils
- =====H_THERMDC(10 mils)
- 10 mils
- =====GND
- 12 mils
- OTHER SIGNALS

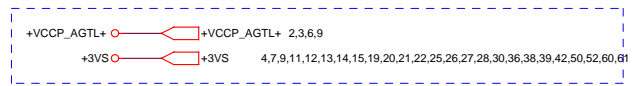
Avoid BPSB,Power



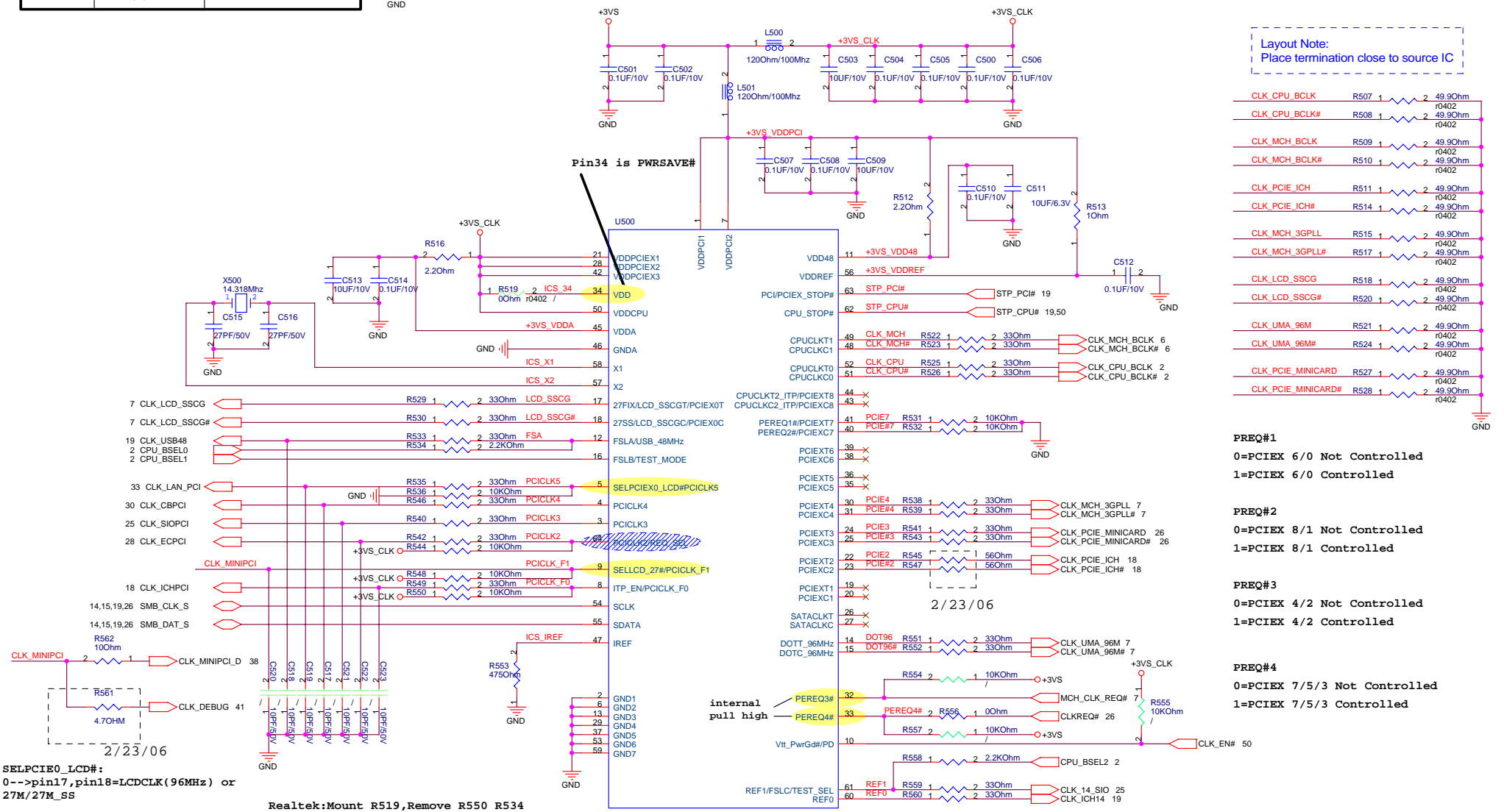
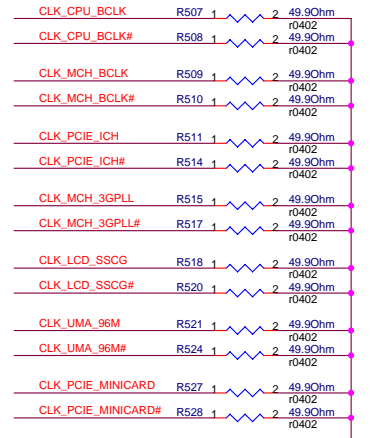
Request	Control net	Net name
PCIE_REQ1#	PCIE0(#), PCIE6(#)	None
PCIE_REQ2#	PCIE1(#), PCIE8(#)	None
PCIE_REQ3#	PCIE2(#), PCIE4(#)	CLK_PCIE_MINICARD(#)
PCIE_REQ4#	PCIE3(#), PCIE5(#), PCIE7(#)	CLK_MCH_3GPLL(#)



Bclk	FSB	FSLC	FSLB	FSLA
133	533	L	L	H
166	667	L	H	H



Layout Note:
Place termination close to source IC



- PREQ#1
0=PCIEX 6/0 Not Controlled
1=PCIEX 6/0 Controlled
- PREQ#2
0=PCIEX 8/1 Not Controlled
1=PCIEX 8/1 Controlled
- PREQ#3
0=PCIEX 4/2 Not Controlled
1=PCIEX 4/2 Controlled
- PREQ#4
0=PCIEX 7/5/3 Not Controlled
1=PCIEX 7/5/3 Controlled

SELPCIE0_LCD#: 0-->pin17, pin18=LCDCLK(96MHz) or 27M/27M_SS

Realtek: Mount R519, Remove R550 R534

SELLCD_27#/PCICLK_F1: 1-->pin17, pin18=LCDCLK(96MHz)

PCICLK2/REQ_SEL: 1-->pin40, pin41=PREQ1#, PREQ2#

ITP_EN/PCICLK_F0: 1-->CPU_ITP pair



2 H_D#[0..63]

H_A#[31..3] 2

U600A

H_D#0	F1	H_D#_0
H_D#1	J1	H_D#_1
H_D#2	H1	H_D#_2
H_D#3	J6	H_D#_3
H_D#4	H3	H_D#_4
H_D#5	K2	H_D#_5
H_D#6	G1	H_D#_6
H_D#7	G2	H_D#_7
H_D#8	K9	H_D#_8
H_D#9	K1	H_D#_9
H_D#10	K7	H_D#_10
H_D#11	J8	H_D#_11
H_D#12	H4	H_D#_12
H_D#13	J3	H_D#_13
H_D#14	K11	H_D#_14
H_D#15	G4	H_D#_15
H_D#16	T10	H_D#_16
H_D#17	W11	H_D#_17
H_D#18	T3	H_D#_18
H_D#19	U7	H_D#_19
H_D#20	U9	H_D#_20
H_D#21	U11	H_D#_21
H_D#22	T11	H_D#_22
H_D#23	W9	H_D#_23
H_D#24	T1	H_D#_24
H_D#25	T8	H_D#_25
H_D#26	T4	H_D#_26
H_D#27	W7	H_D#_27
H_D#28	U5	H_D#_28
H_D#29	T9	H_D#_29
H_D#30	W6	H_D#_30
H_D#31	T5	H_D#_31
H_D#32	AB7	H_D#_32
H_D#33	AA9	H_D#_33
H_D#34	W4	H_D#_34
H_D#35	W3	H_D#_35
H_D#36	Y3	H_D#_36
H_D#37	Y7	H_D#_37
H_D#38	W5	H_D#_38
H_D#39	Y10	H_D#_39
H_D#40	AB8	H_D#_40
H_D#41	W2	H_D#_41
H_D#42	AA4	H_D#_42
H_D#43	AA7	H_D#_43
H_D#44	AA2	H_D#_44
H_D#45	AA6	H_D#_45
H_D#46	AA10	H_D#_46
H_D#47	Y8	H_D#_47
H_D#48	AA1	H_D#_48
H_D#49	AB4	H_D#_49
H_D#50	AC9	H_D#_50
H_D#51	AB11	H_D#_51
H_D#52	AC11	H_D#_52
H_D#53	AB3	H_D#_53
H_D#54	AC2	H_D#_54
H_D#55	AD1	H_D#_55
H_D#56	AD9	H_D#_56
H_D#57	AC1	H_D#_57
H_D#58	AD7	H_D#_58
H_D#59	AC6	H_D#_59
H_D#60	AB5	H_D#_60
H_D#61	AD10	H_D#_61
H_D#62	AD4	H_D#_62
H_D#63	AC8	H_D#_63

HOST

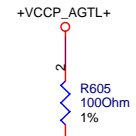
H_A#_3	H9	H_A#3
H_A#_4	C9	H_A#4
H_A#_5	E11	H_A#5
H_A#_6	G11	H_A#6
H_A#_7	F11	H_A#7
H_A#_8	G12	H_A#8
H_A#_9	F9	H_A#9
H_A#_10	H11	H_A#10
H_A#_11	J12	H_A#11
H_A#_12	G14	H_A#12
H_A#_13	D9	H_A#13
H_A#_14	J14	H_A#14
H_A#_15	H13	H_A#15
H_A#_16	I15	H_A#16
H_A#_17	F14	H_A#17
H_A#_18	D12	H_A#18
H_A#_19	A11	H_A#19
H_A#_20	C11	H_A#20
H_A#_21	A12	H_A#21
H_A#_22	A13	H_A#22
H_A#_23	E13	H_A#23
H_A#_24	G13	H_A#24
H_A#_25	F12	H_A#25
H_A#_26	B12	H_A#26
H_A#_27	C14	H_A#27
H_A#_28	A14	H_A#28
H_A#_29	C14	H_A#29
H_A#_30	D14	H_A#30
H_A#_31	C14	H_A#31

H_REQ#_0	D8	H_REQ#0
H_REQ#_1	G8	H_REQ#1
H_REQ#_2	B8	H_REQ#2
H_REQ#_3	F8	H_REQ#3
H_REQ#_4	A8	H_REQ#4
H_RS#_0	B4	H_RS#0
H_RS#_1	E6	H_RS#1
H_RS#_2	D6	H_RS#2
H_CPUSLP#	E3	H_CPUSLP# 2,17
H_TRDY#	E7	H_TRDY# 2

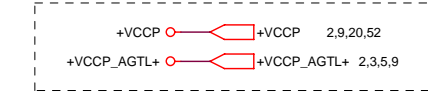
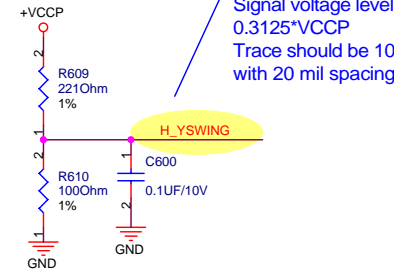
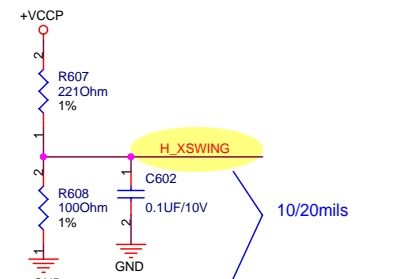
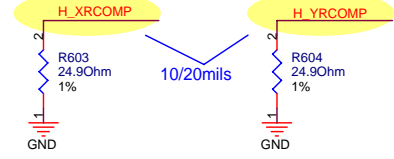
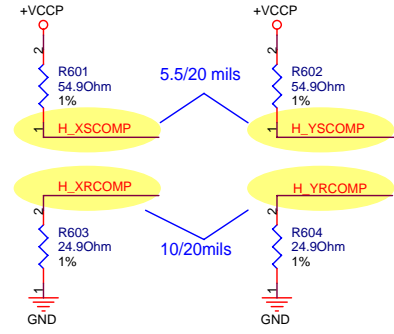
5 CLK_MCH_BCLK
5 CLK_MCH_BCLK#

H_XRCOMP	E1	H_XRCOMP
H_XSCOMP	E2	H_XSCOMP
H_XSWING	E4	H_XSWING
H_YRCOMP	Y1	H_YRCOMP
H_YSCOMP	U1	H_YSCOMP
H_YSWING	W1	H_YSWING
CLK_MCH_BCLK	AG2	H_CLKIN
CLK_MCH_BCLK#	AG1	H_CLKIN#

CALISTOGA_Q137

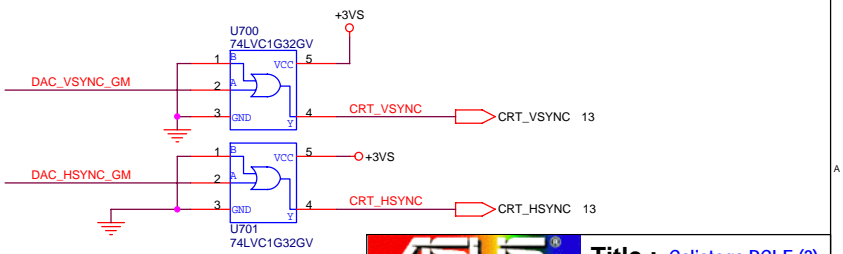
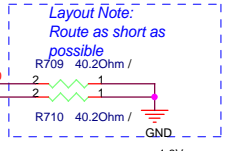
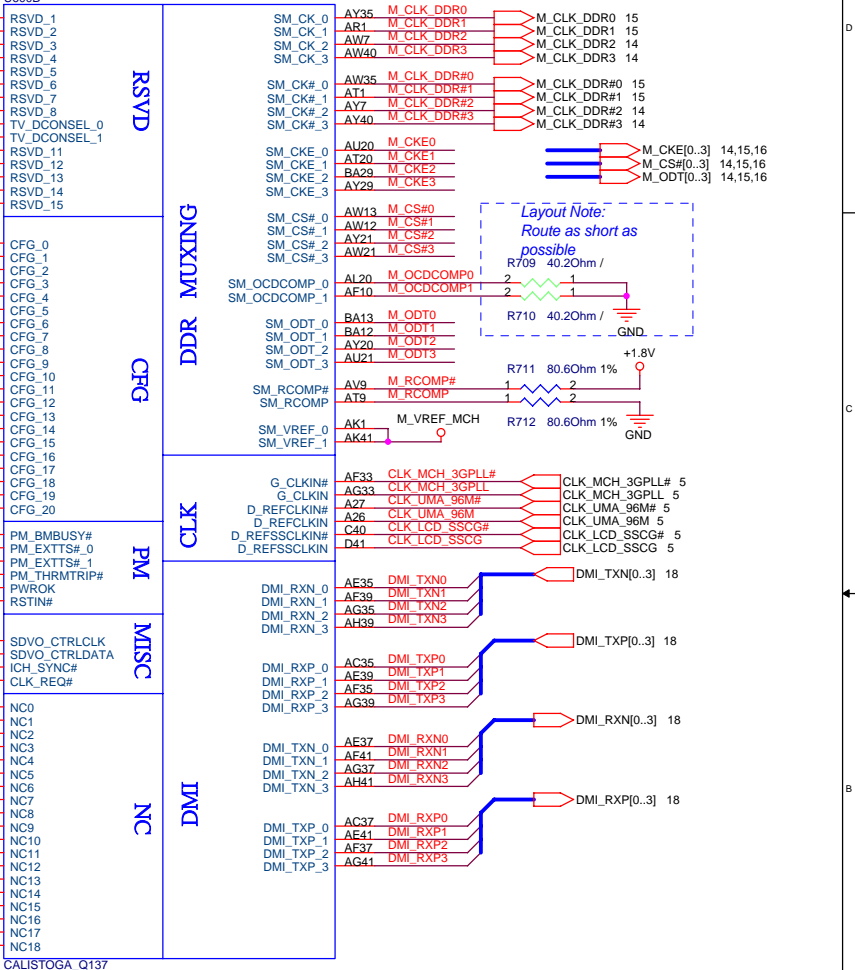
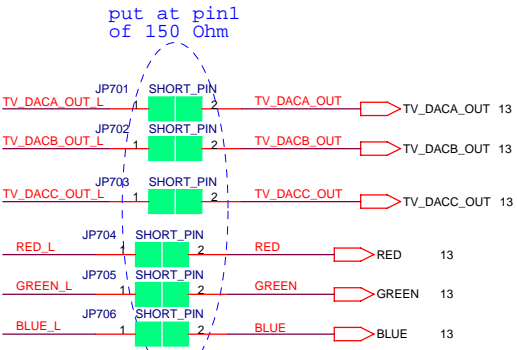
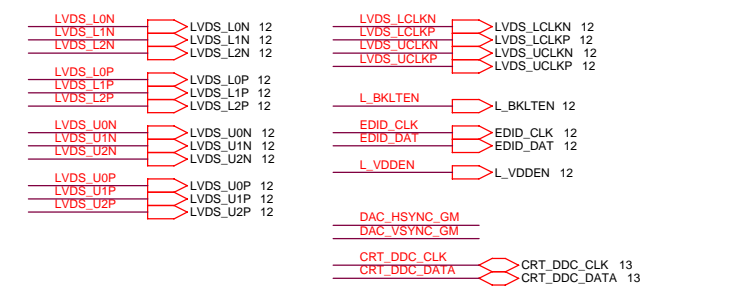
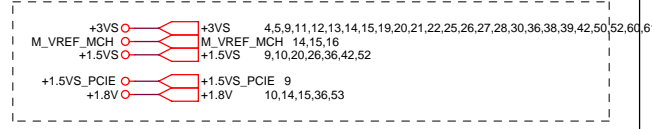
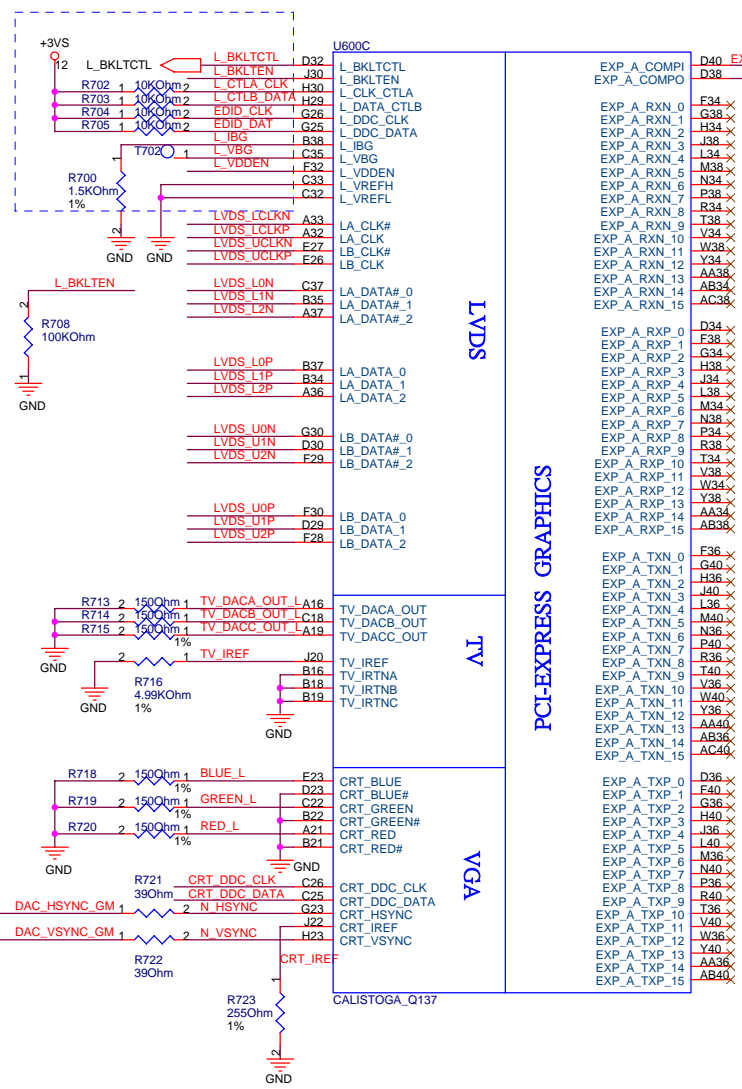


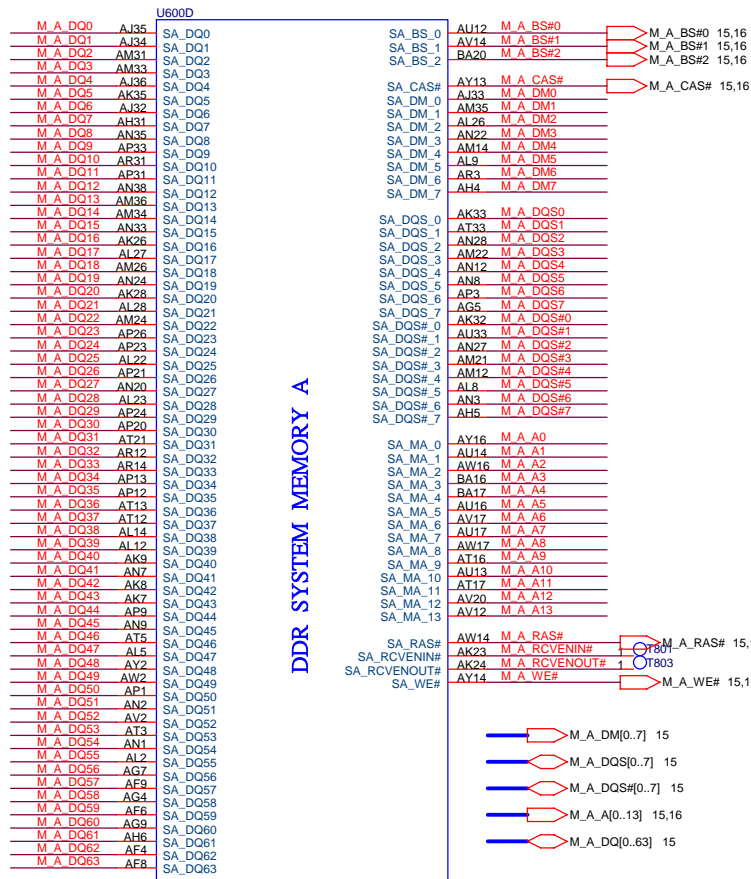
Layout Note:
0.1uF should be placed 100mils or less from GMCH pin.



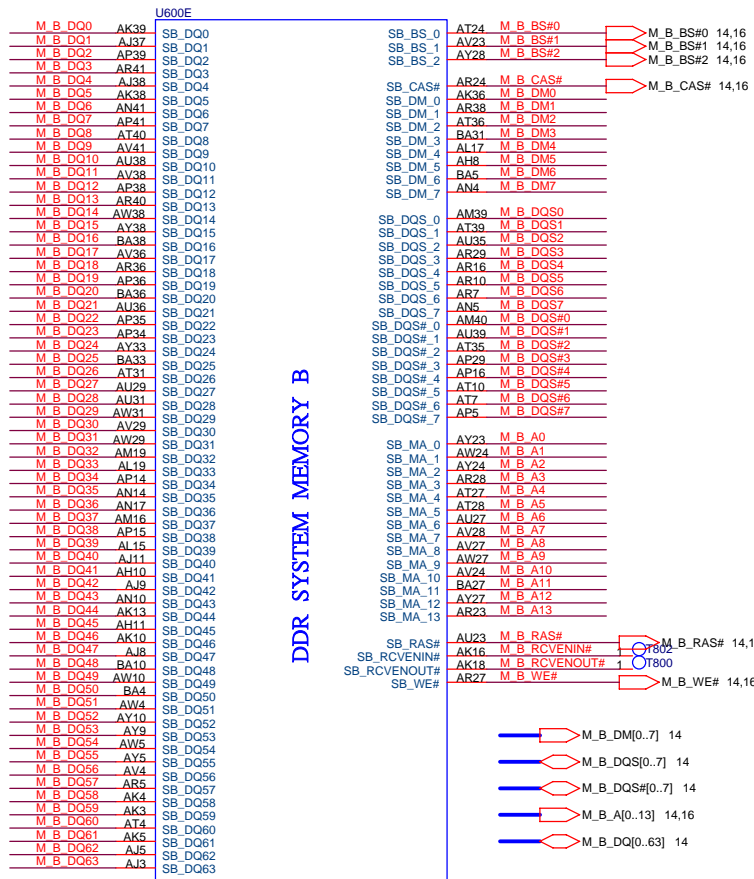
ASUS Title : Calistoga MCH (1)
 ASUSTeK COMPUTER INC Engineer: Jack Wang

Size	Project Name	Rev
B	A6F	1.0
Date: Monday, March 06, 2006	Sheet 6 of 63	



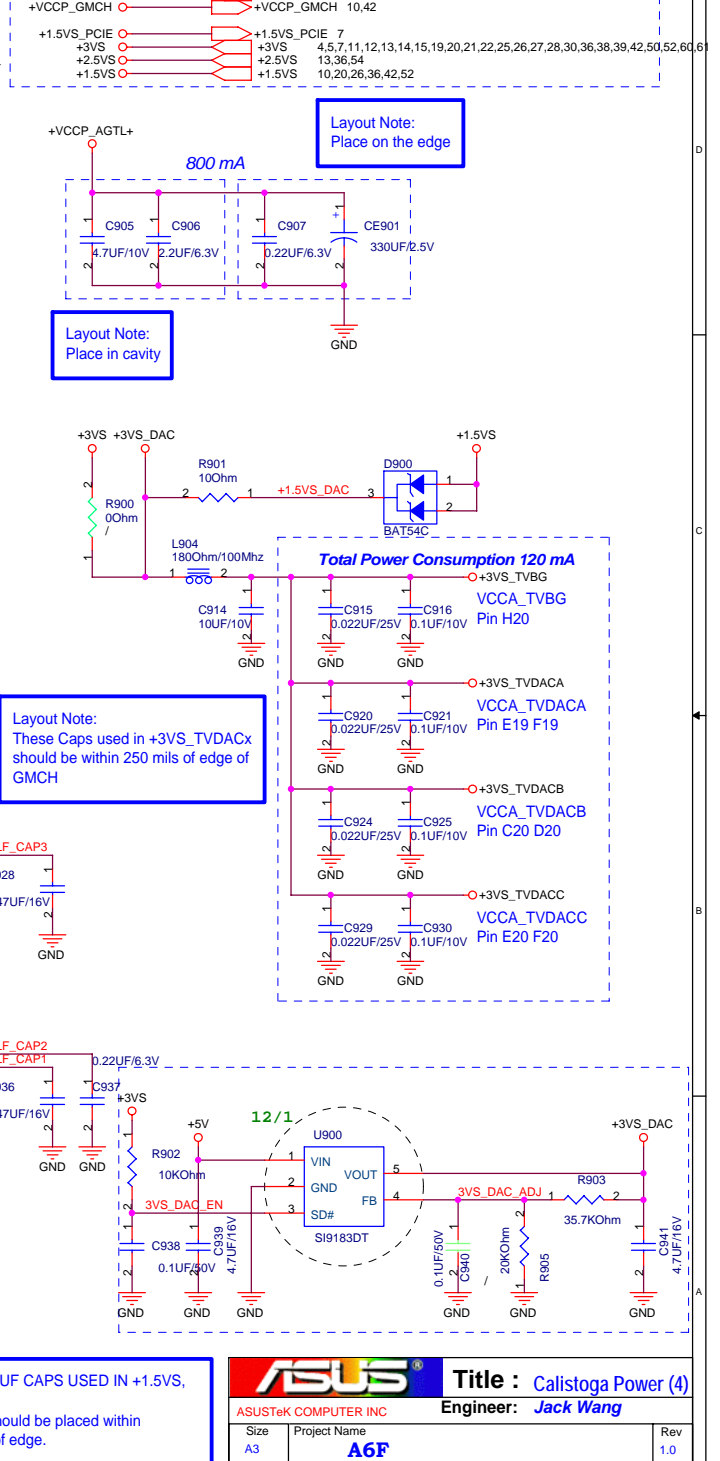
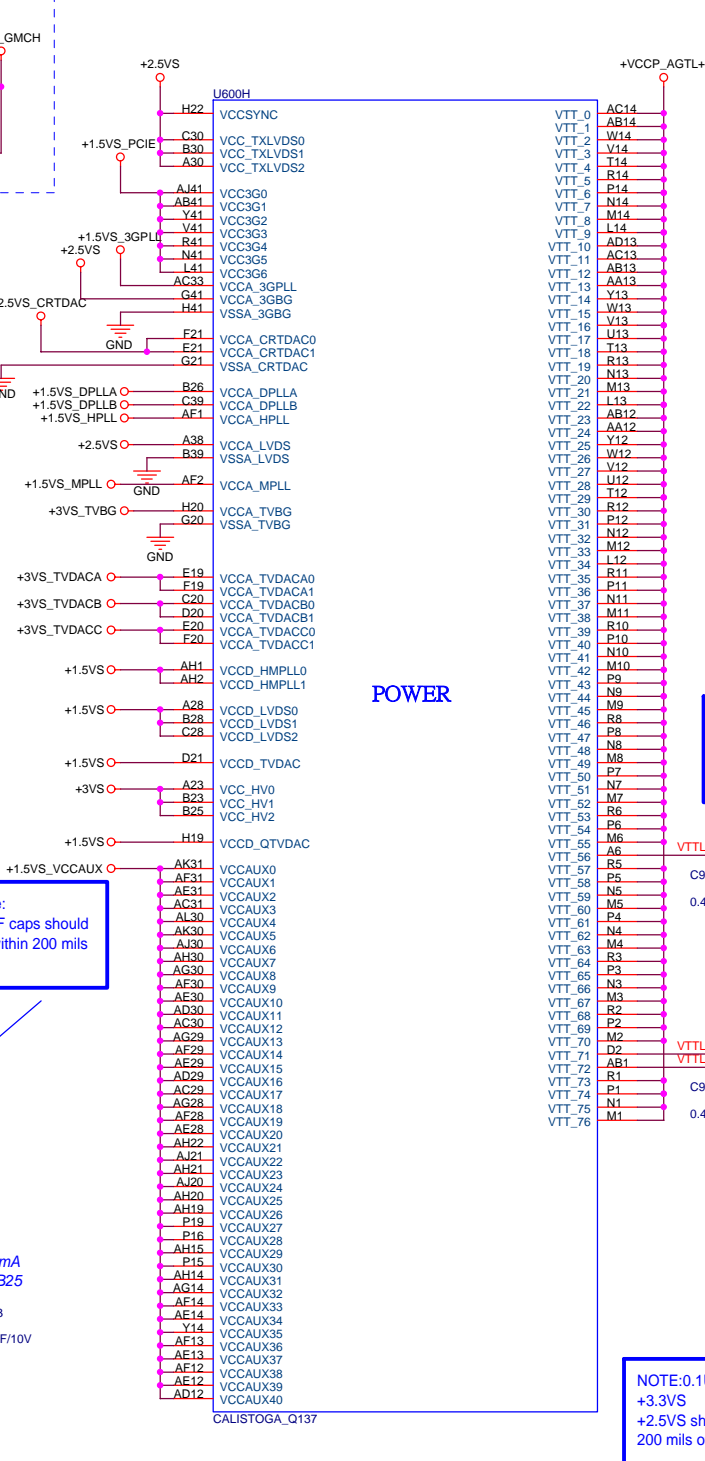
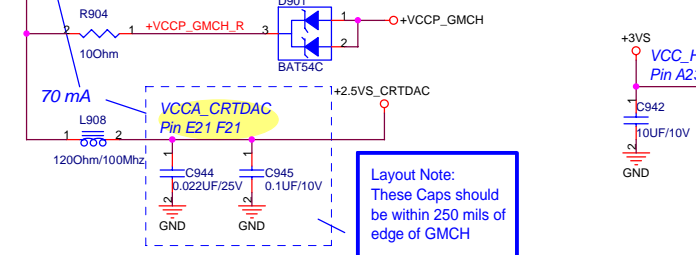
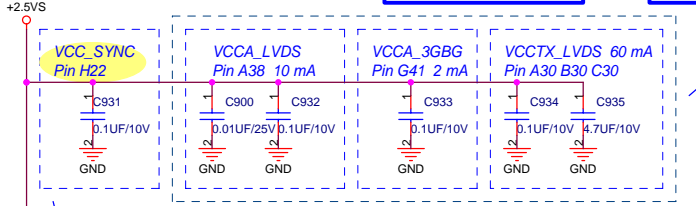
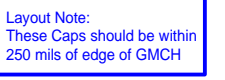
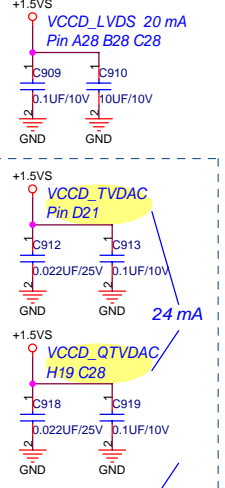
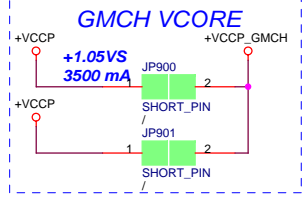
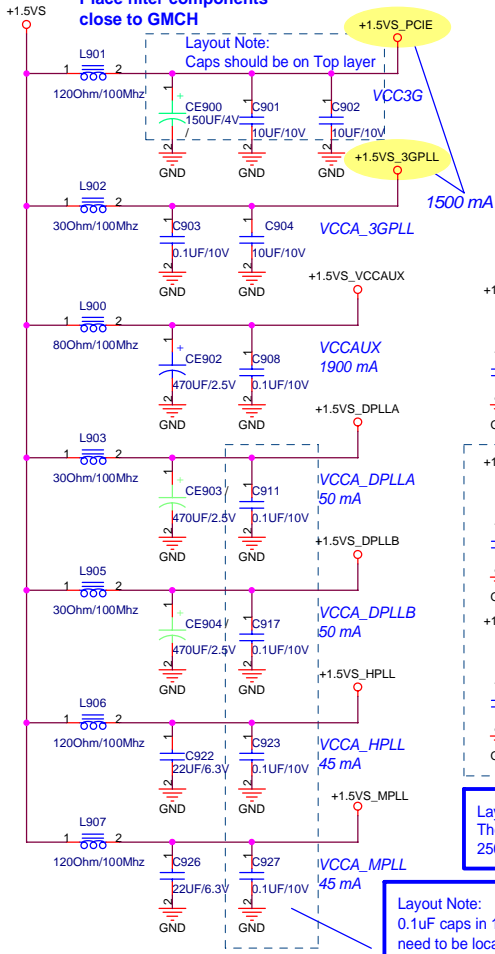


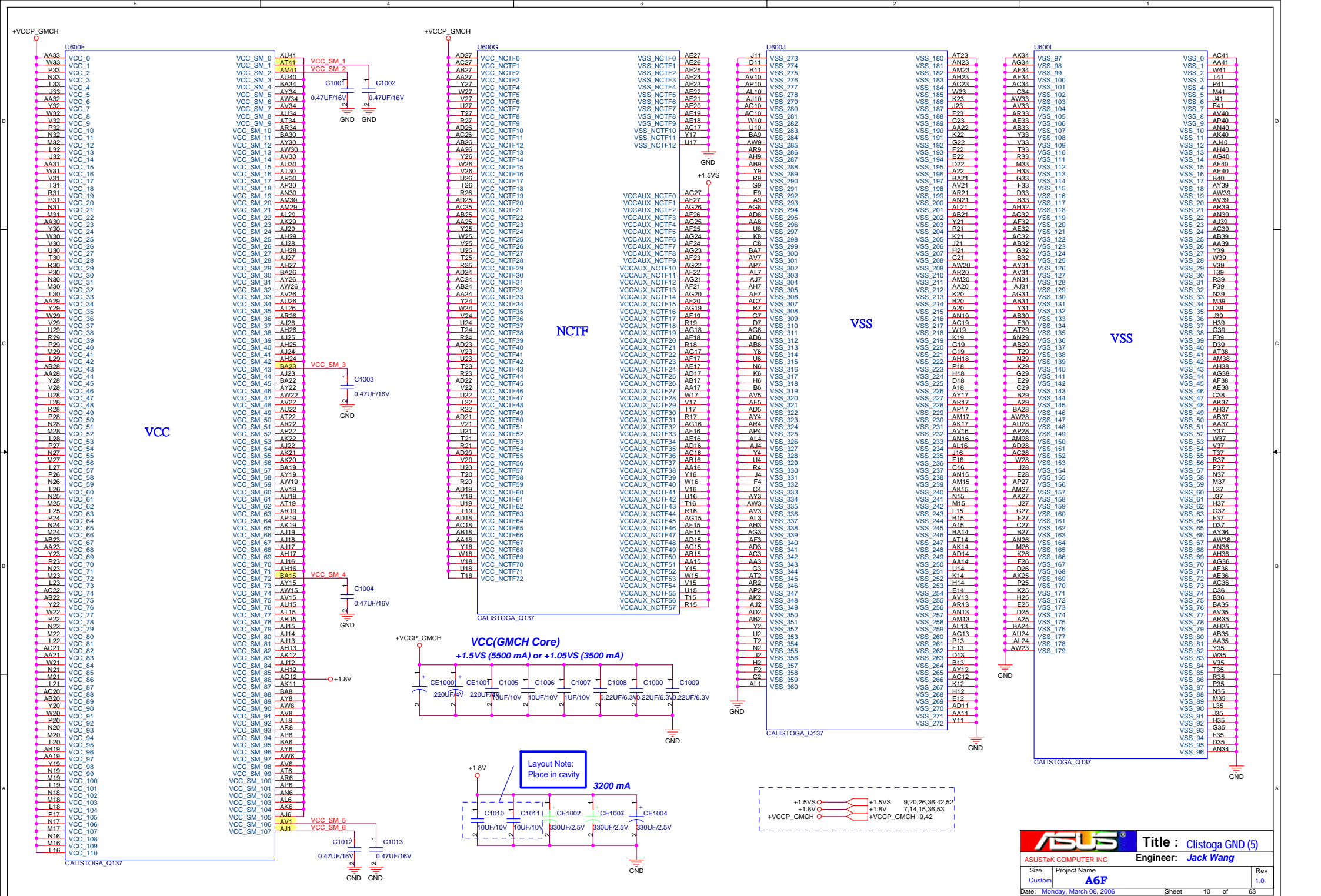
DDR SYSTEM MEMORY A



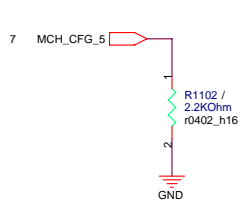
DDR SYSTEM MEMORY B

Layout Note:
Place filter components
close to GMCH

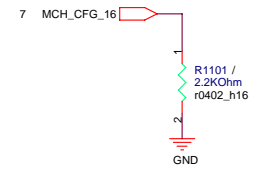




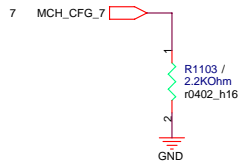
ASUS Title : **Clistoga GND (5)**
 ASUSTek COMPUTER INC Engineer: **Jack Wang**
A6F
 Date: Monday, March 06, 2006 Sheet 10 of 63
 Size Custom Project Name Rev 1.0



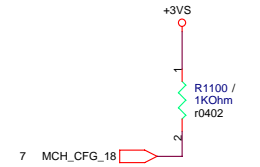
CFG5 : DMI X2 Select
 LOW = DMI X 2
HIGH = DMI X 4 (Default)



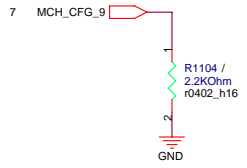
CFG16 : FSB DYNAMIC ODT
 LOW = Dynamic ODT Disabled
HIGH = Dynamic ODT Enabled (Default)



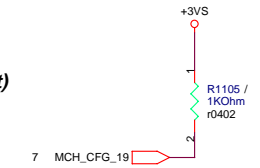
CFG7 : CPU STRAP
 LOW = Reserved
HIGH = Mobility CPU (Default)



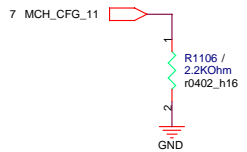
CFG18 : GMCH Core Voltage Level
 LOW = 1.05V
HIGH = 1.5V (default)



CFG9 : PCIE GRAPHIC LANE
 LOW = REVERSE LANES
HIGH = NORMAL OPERATION (Default)



CFG19 : DMI LANE REVERSAL
 LOW = NORMAL
 HIGH = LANES REVERSED

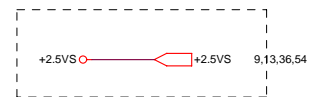


CFG11 : Reserved but need to be pull low

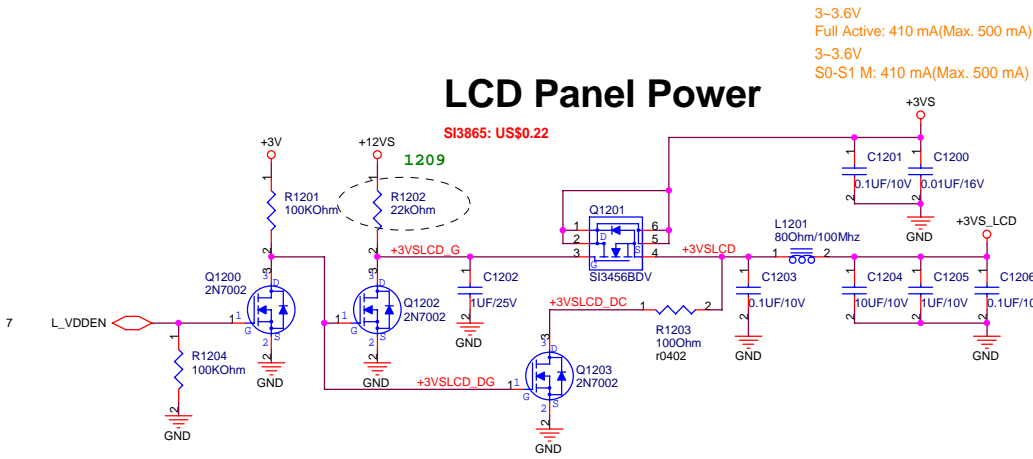
CFG[17..3] have internal pullup resistors.
 CFG[19..18] have internal pulldown resistors.
 SDVOCRTL_DATA has internal pulldown resistors.

CFG All are sampled with respect to the leading edge of the GMCH PWR0K

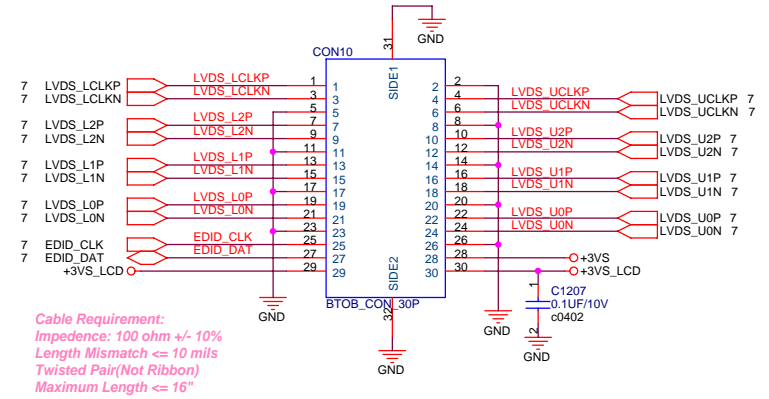
2:0	FSB Freq select	001 = FSB533 011 = FSB667
4:3		
5	DMI X 2 Select	0 = DMI X 2 1 = DMI X 4 (Default)
6		
7	CPU Strap	0 = Reserved 1 = Mobile CPU (Default)
8		
9	PCIE Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal (Default)
11:10		
13:12	XOR/ALLZ	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal operation (Default)
15:14		
16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
17		
SDVO_C TRLDATA	SDVO Present	0 = No SDVO Card Present (Default) 1 = SDVO Card Present
18	VCC select	0 = 1.05V (Default) 1 = 1.5V
19	DMI Lane Reversal	0 = Normal (Default) 1 = Reverse Lanes
20	SDVO/PCIE concurrent	0 = Only SDVO or PCIE x1 is operational(Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port



LCD Panel Power



LCD LVDS Interface

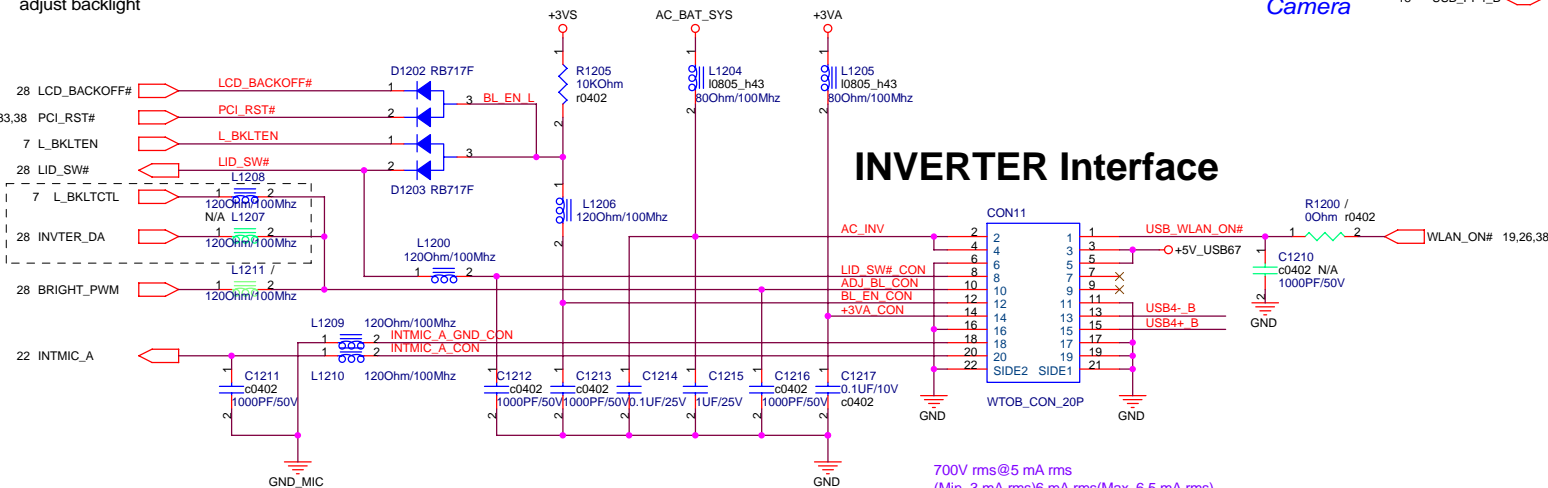


LCD Backlight Control

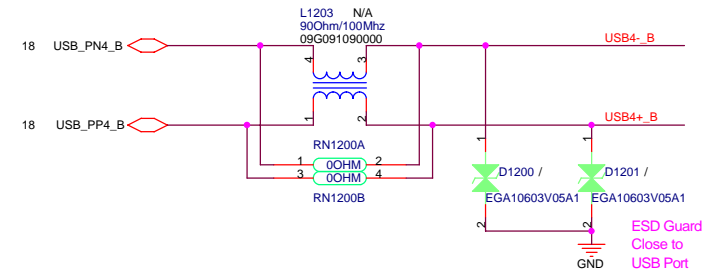
BIOS
LCD_BACKOFF#
When user push "Fn+F7" button
BIOS active this pin to turn On/Off backlight

EC
INVTER_DA:
EC output D/A signal (adjust voltage level) to
adjust backlight

*Inverter Board
built in 14.1W
LCD Panel*



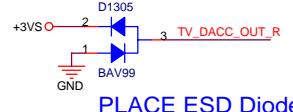
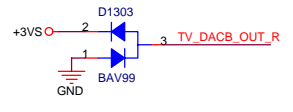
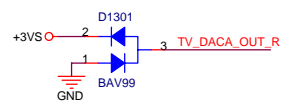
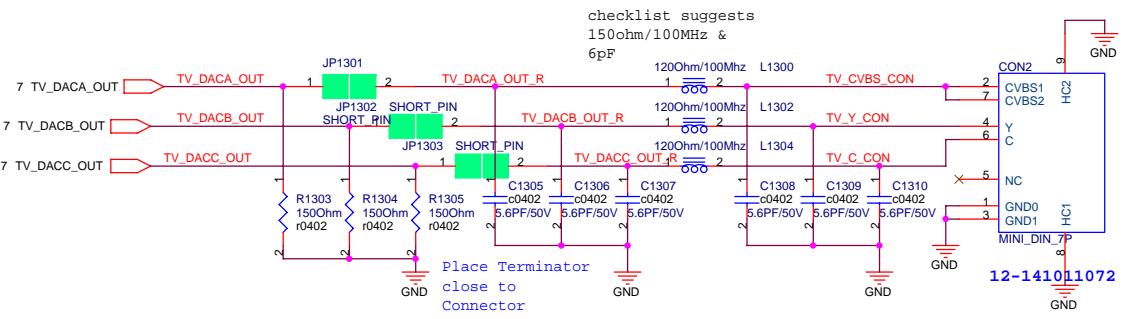
*USB4
For
CMOS
Camera*



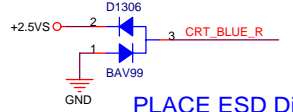
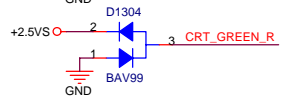
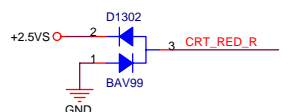
INVERTER Interface

TV OUT

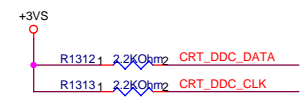
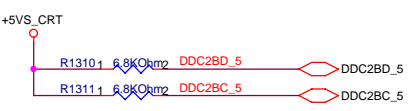
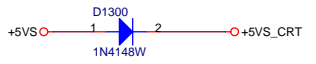
12G14101107D



PLACE ESD Diodes
near TV port

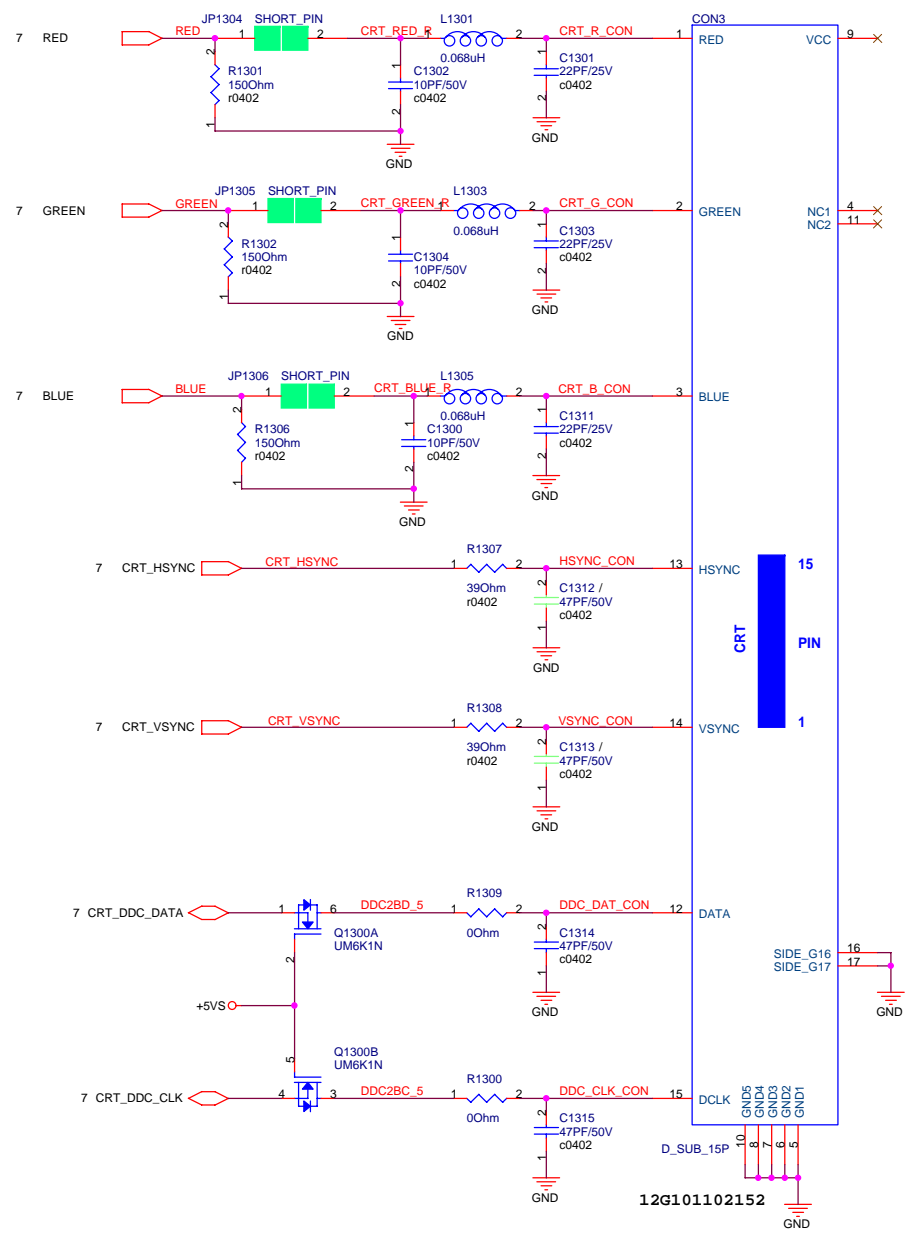


PLACE ESD Diodes
near VGA port

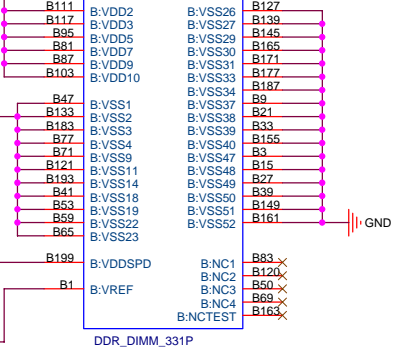
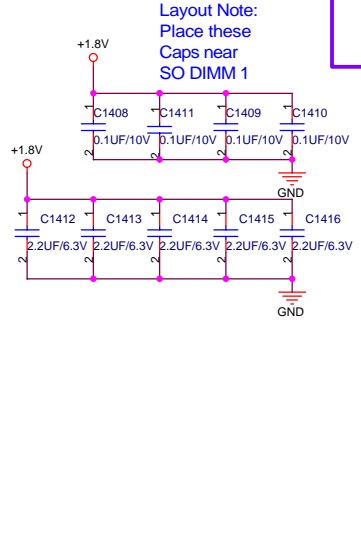
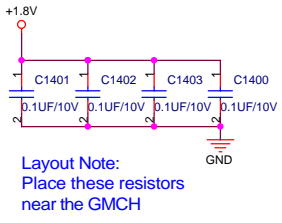
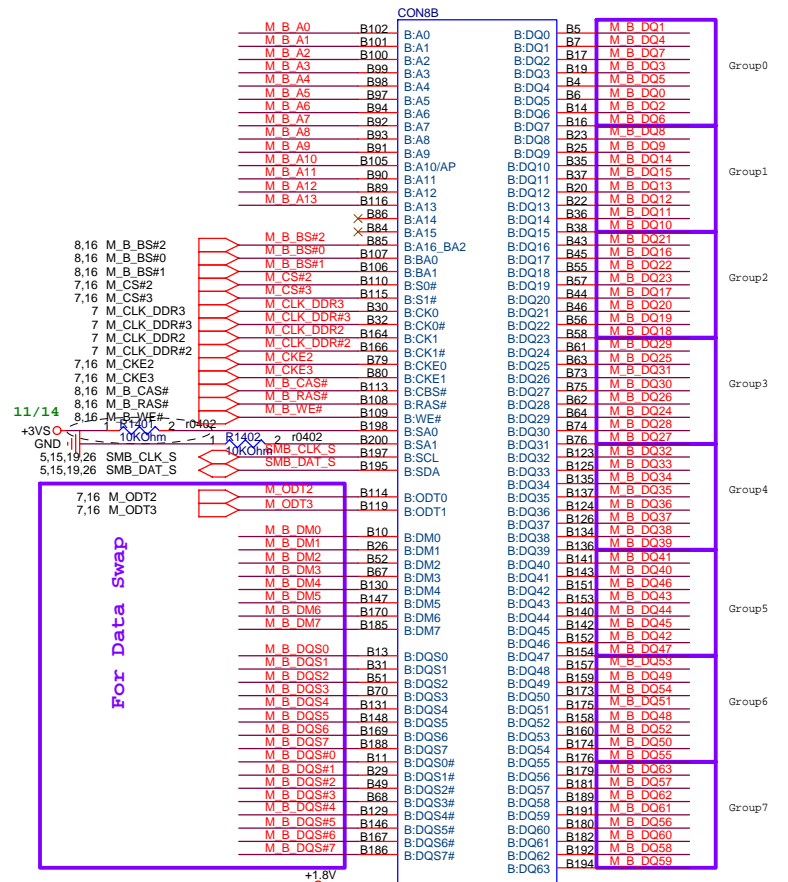
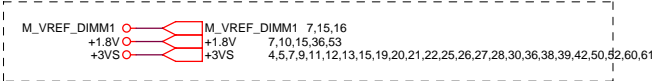
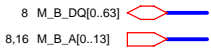


CRT OUT

checklist suggests 47ohm/100MHz

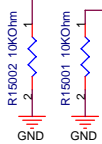
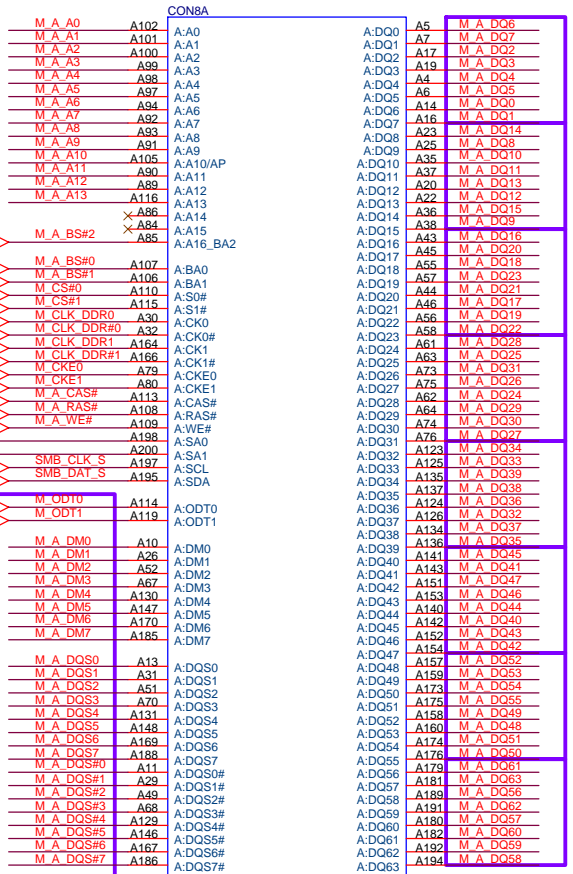
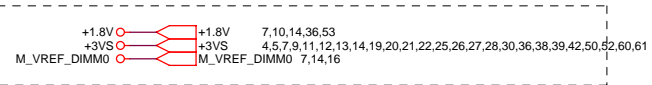


		Title : CRT & TV OUT	
ASUSTek COMPUTER INC		Engineer: Jack Wang	
Size A3	Project Name A6F	Date: Monday, March 06, 2006	Rev 1.0
Date: Monday, March 06, 2006		Sheet 13	of 63



8 M_A_DQ[0..63]
8,16 M_A_A[0..13]

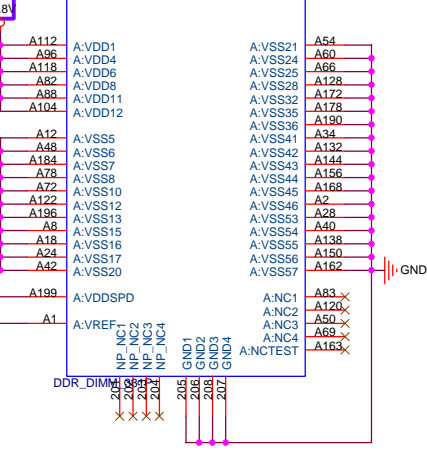
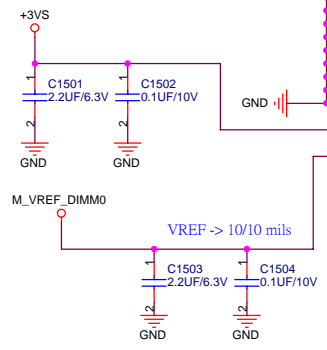
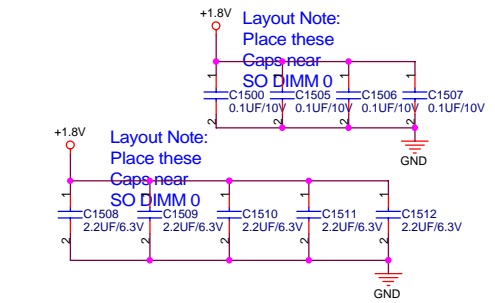
Green Part Number:12G025122006



For Data Swap

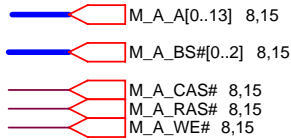
8 M_A_DM[0..7]
8 M_A_DQS[0..7]
8 M_A_DQS#[0..7]

GMCH=====>SODIMM1=>SODIMM0

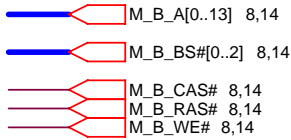


NEED TO SWAP

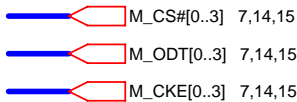
1	56Ohm	16	RN1601A	M_A_A2
2	56Ohm	15	RN1601B	M_A_A0
3	56Ohm	14	RN1601C	M_A_BS#1
4	56Ohm	13	RN1601D	M_A_RAS#
5	56Ohm	12	RN1601E	M_ODT0
6	56Ohm	11	RN1601F	M_CS#0
7	56Ohm	10	RN1601G	M_CS#2
8	56Ohm	9	RN1601H	M_ODT2



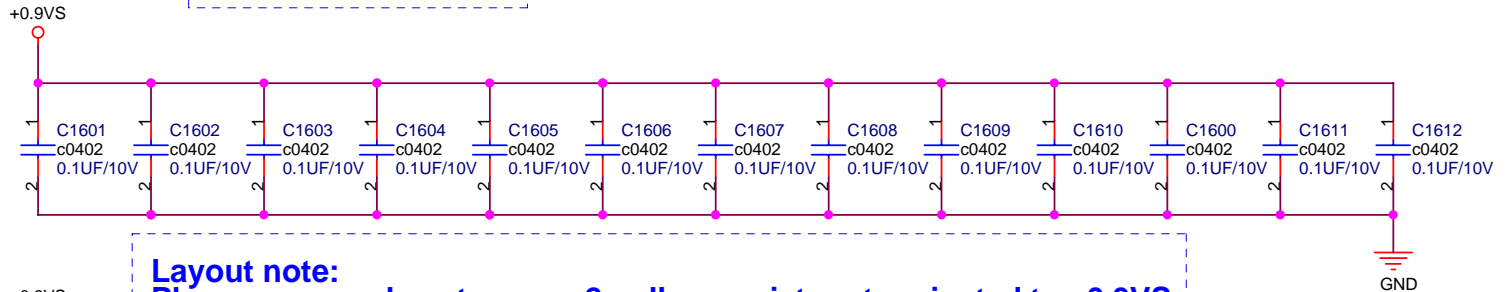
1	56Ohm	16	RN1602A	M_B_A11
2	56Ohm	15	RN1602B	M_B_A6
3	56Ohm	14	RN1602C	M_B_A7
4	56Ohm	13	RN1602D	M_B_A4
5	56Ohm	12	RN1602E	M_B_A2
6	56Ohm	11	RN1602F	M_B_A0
7	56Ohm	10	RN1602G	M_B_BS#1
8	56Ohm	9	RN1602H	M_B_RAS#



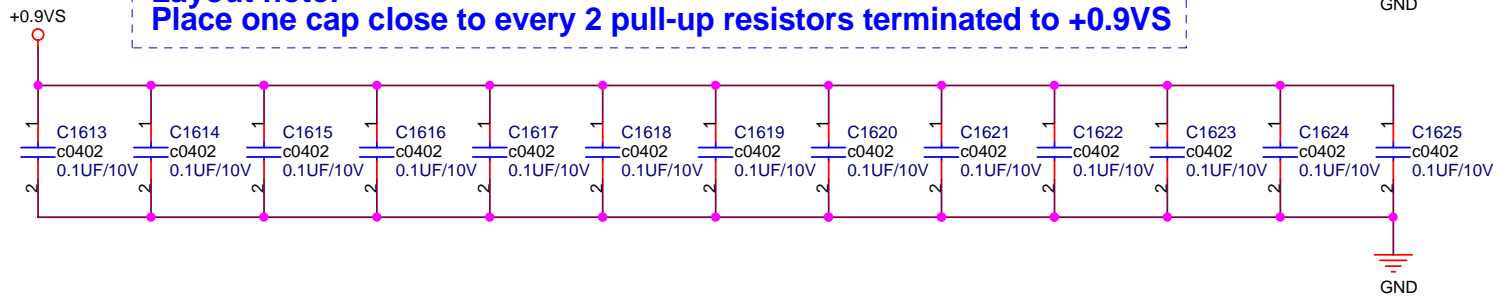
1	56Ohm	16	RN1603A	M_B_BS#0
2	56Ohm	15	RN1603B	M_B_A10
3	56Ohm	14	RN1603C	M_B_WE#
4	56Ohm	13	RN1603D	M_B_CAS#
5	56Ohm	12	RN1603E	M_CS#3
6	56Ohm	11	RN1603F	M_ODT3
7	56Ohm	10	RN1603G	M_ODT1
8	56Ohm	9	RN1603H	M_CS#1



1	56Ohm	16	RN1605A	M_B_A12
2	56Ohm	15	RN1605B	M_B_BS#2
3	56Ohm	14	RN1605C	M_A_A12
4	56Ohm	13	RN1605D	M_A_BS#0
5	56Ohm	12	RN1605E	M_A_BS#2
6	56Ohm	11	RN1605F	M_CKE2
7	56Ohm	10	RN1605G	M_CKE0
8	56Ohm	9	RN1605H	M_CKE3

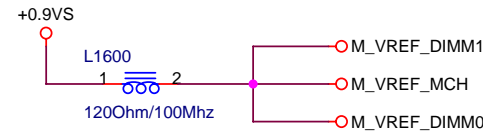
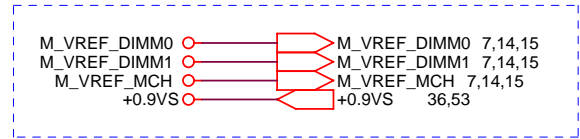


1	56Ohm	16	RN1606A	M_B_A13
2	56Ohm	15	RN1606B	M_CKE1
3	56Ohm	14	RN1606C	M_A_A13
4	56Ohm	13	RN1606D	M_A_A4
5	56Ohm	12	RN1606E	M_A_A6
6	56Ohm	11	RN1606F	M_A_A7
7	56Ohm	10	RN1606G	M_A_A11
8	56Ohm	9	RN1606H	M_A_A9



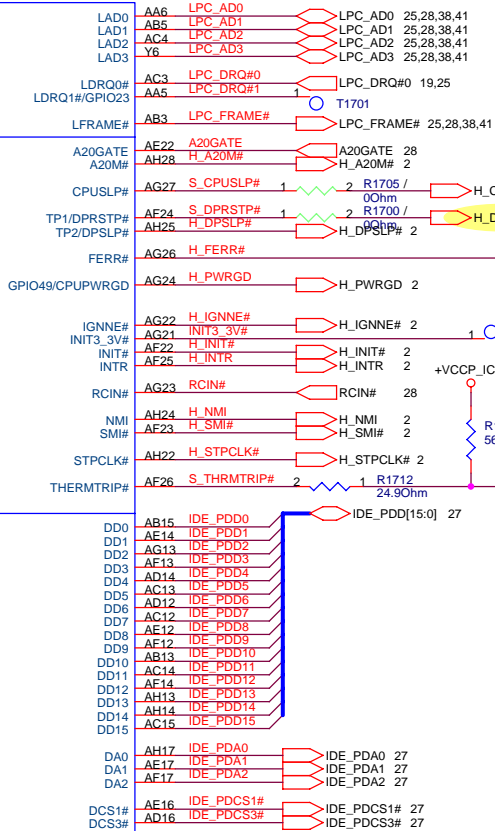
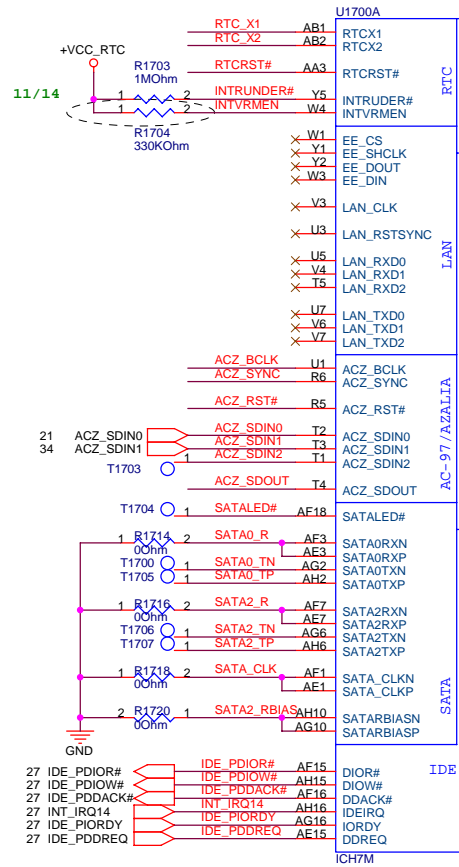
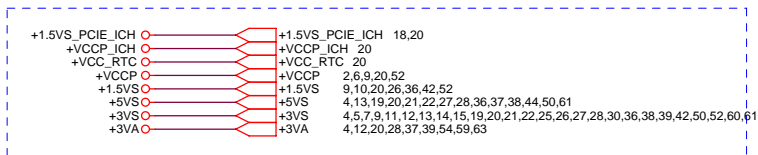
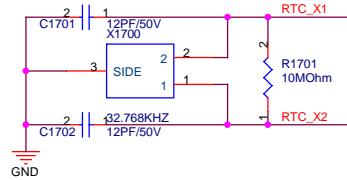
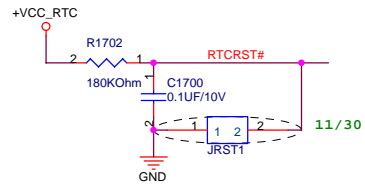
1	56Ohm	16	RN1607A	M_A_A5
2	56Ohm	15	RN1607B	M_B_A1
3	56Ohm	14	RN1607C	M_B_A3
4	56Ohm	13	RN1607D	M_B_A5
5	56Ohm	12	RN1607E	M_B_A8
6	56Ohm	11	RN1607F	M_A_A3
7	56Ohm	10	RN1607G	M_A_A8
8	56Ohm	9	RN1607H	M_B_A9

1	56Ohm	2	RN1608A	M_A_CAS#
3	56Ohm	4	RN1608B	M_A_WE#
5	56Ohm	6	RN1608C	M_A_A10
7	56Ohm	8	RN1608D	M_A_A1



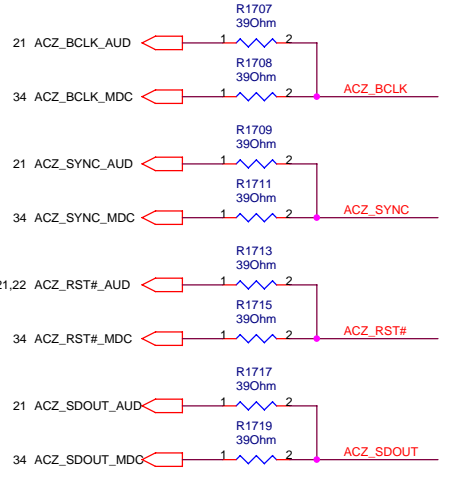
Layout note:
Place one cap close to every 2 pull-up resistors terminated to +0.9VS

		Title : DDR2 TERM	
ASUSTeK COMPUTER INC		Engineer: Jack Wang	
Size A4	Project Name A6F	Date: Monday, March 06, 2006	Rev 1.0
Date: Monday, March 06, 2006		Sheet 16 of 63	



DPRSTP# routing from Intel 82801GBM to Yonah processor is required. Routing to VR must be done last and must have de-bounce filtering to handle daisy chain topology.

24 ± 5% series termination resistor placed within 2" from Intel 82801GBM, 56 ± 5% pull-up resistor has to be within 2" from the series resistor



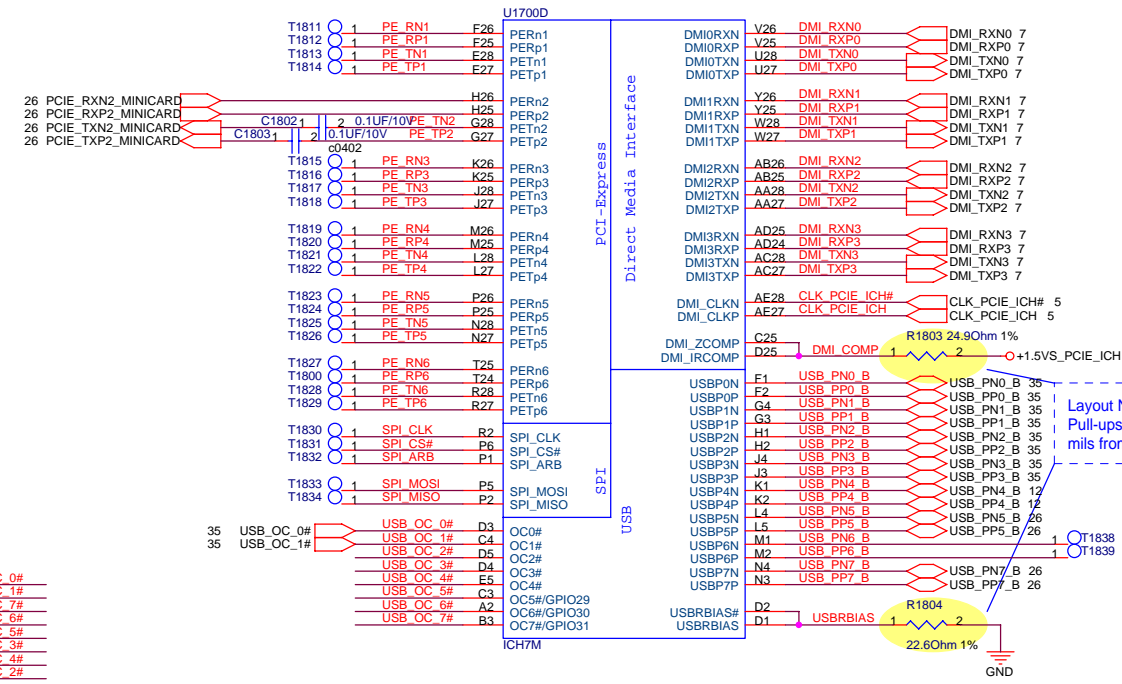
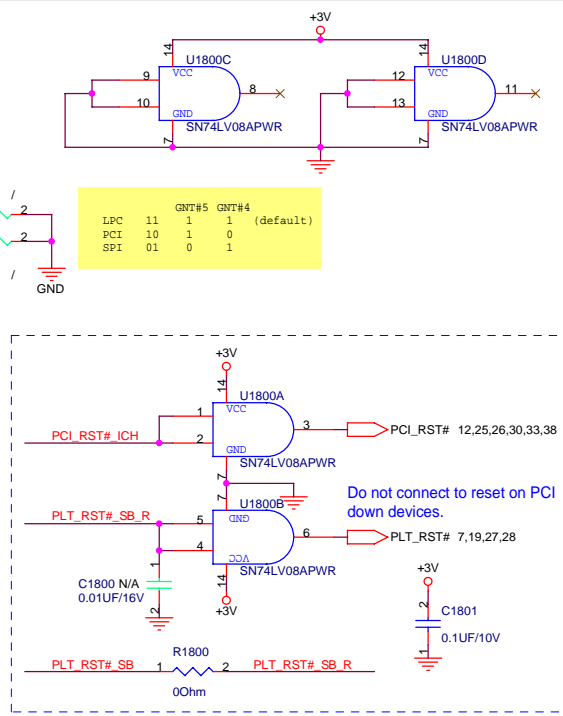
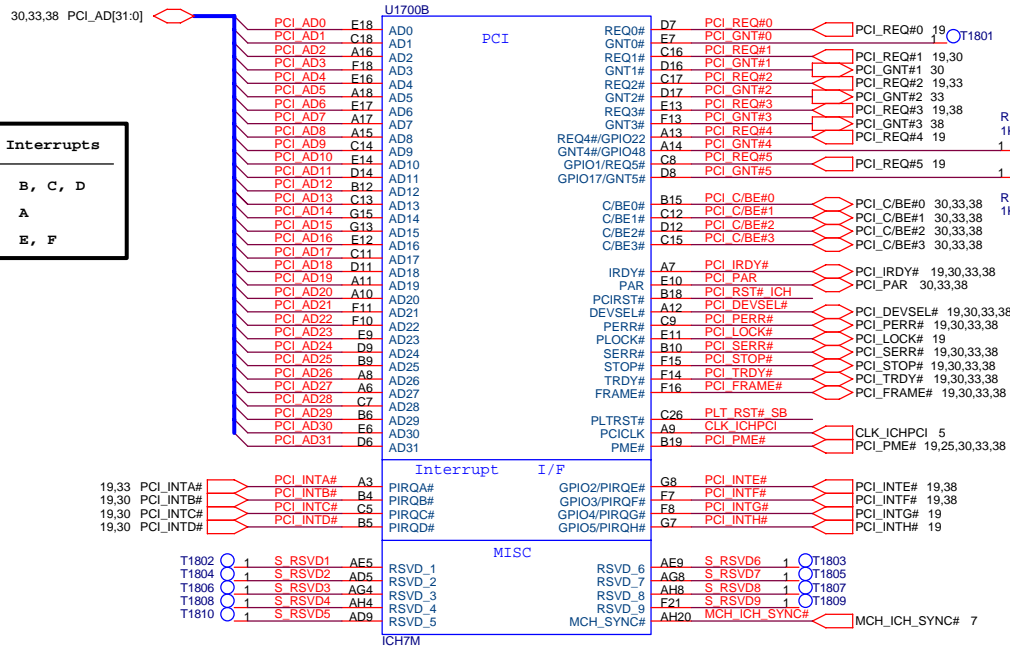
ACZ_SDOUT	PWROK rising	TP3 pull low: allow entrance to XOR Chain testing TP3 not pull low: sets bit 1 of RPC.PC	PD
ACZ_SYNC	PWROK rising	sets bit 0 of RPC.PC	PD
EE_CS		should not be pulled high	PD
EE_DOUT		should not be pulled low	PU
GNT2#		should not be pulled low	PU
GNT3#	PWROK rising	low: "top-block swap" mode	PU
GNT5#/GPIO17#		GNT5# GNT4#	
GNT4#/GPIO48	PWROK rising	0 1 SPI 1 0 PCI 1 1 LPC	PU

GPIO16		should not be pulled high	PD
DPRSTP#		should not be pulled low	PU
GPIO25	RSMRST# rising	should not be pulled low	PU
INTVRMEN	ALWAYS	high: Enable integrated VccSus1.05 VRM	
LINKALERT#		REQUIRE an external pull-up R	Need
REQ[4:1]#	PWROK rising		PU
SATALED#		should not be pulled low	Conditional PU
SPKR	PWROK rising	high: "No reboot" mode	PD
TP3	PWROK rising	should not be pulled low unless using XOR Chain testing	PU

ASUS Title: ICH7-M (1/4)
 ASUSTek COMPUTER INC Engineer: Jack Wang
 Size Project Name
 Custom **A6F** Rev 1.0
 Date: Monday, March 06, 2006 Sheet 17 of 63

PCI Device

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus	AD17	REQ1#/GNT1#	B, C, D
LAN	AD23	REQ2#/GNT2#	A
Mini-PCI	AD19	REQ3#/GNT3#	E, F

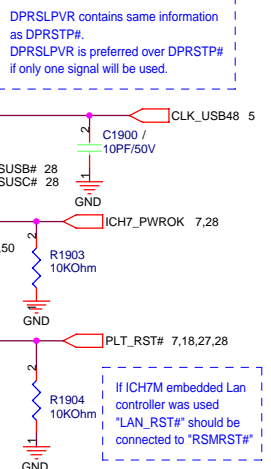
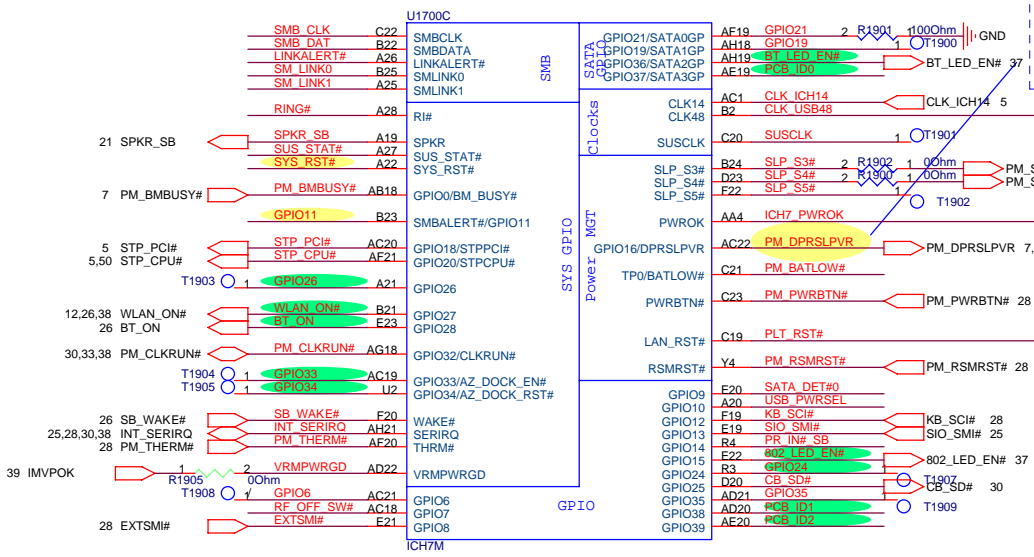


USB Devices

- Port 0 Conn. 0
- Port 1 Conn. 1
- Port 2 Conn. 2
- Port 3 Conn. 3
- Port 4 CMOS Camera
- Port 5 Bluetooth
- Port 6 NC
- Port 7 Mini Card

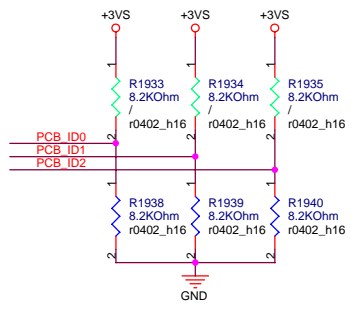
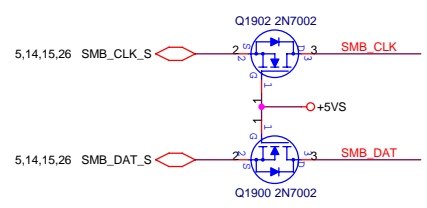
Layout Note:
Pull-ups must be placed within 500 mils from Intel 82801GMB pins

ASUS		Title : ICH7-M (2/4)	
ASUSTek COMPUTER INC		Engineer: Jack Wang	
Size	Project Name	Rev	
Custom	A6F	1.0	
Date: Monday, March 06, 2006	Sheet 18 of 63		

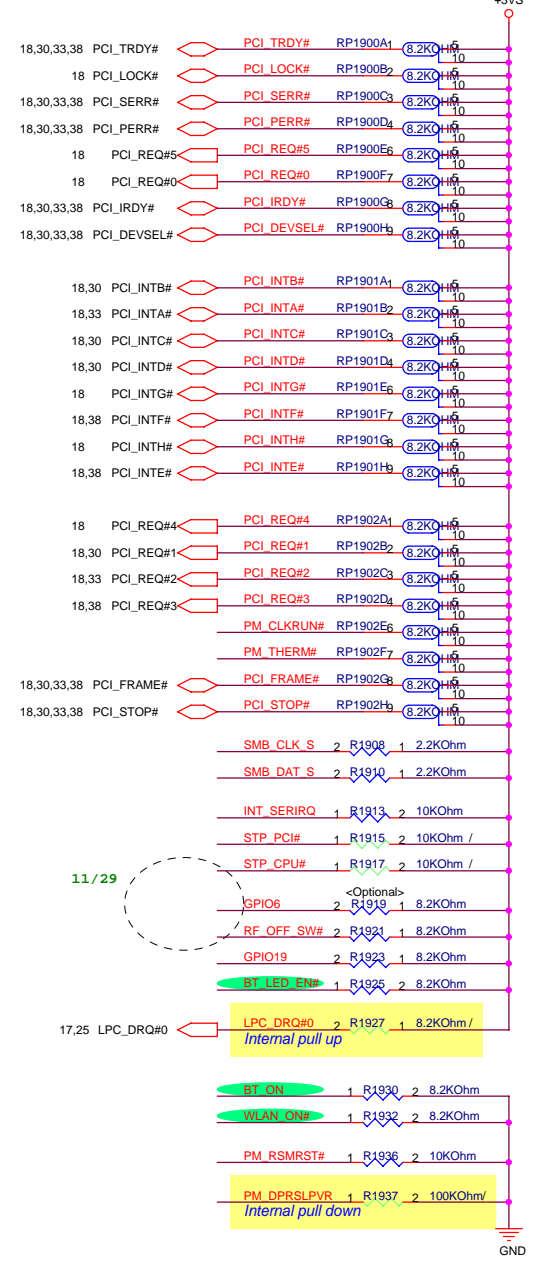
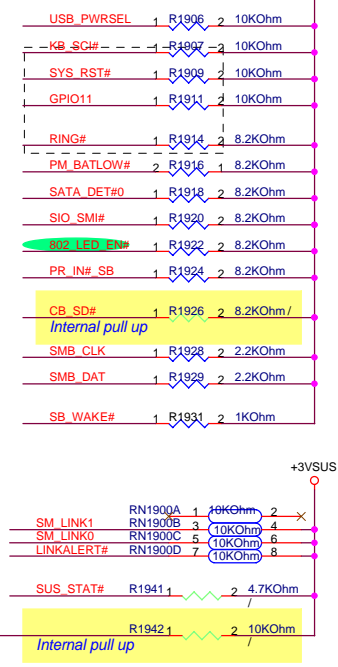
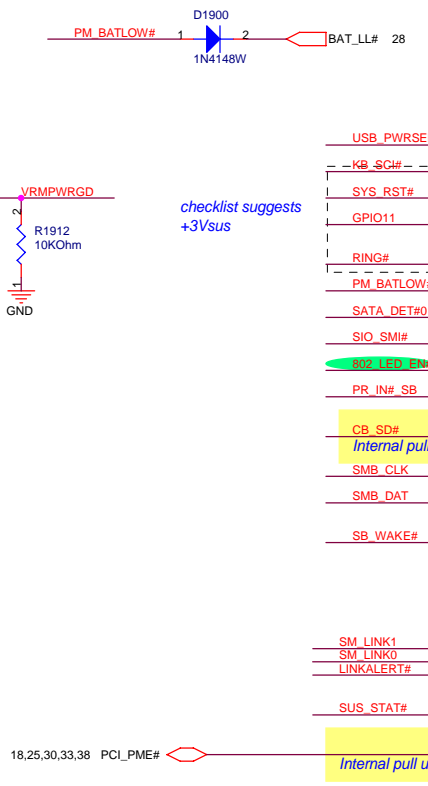


GPIO Power Plane

CPU Vcore GPIO[49]
 5V Core GPIO[5:1]
 3.3V Core GPIO[0][7:6][23:16][39:32][48]
 3.3V Resume GPIO[15:8][31:24]



PCB_VID3 : PROJECT CODE
 PCB_VID 0 1 2
 MB V1.0 0 0 0



Layout Note:
Place above Caps within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top near pin D28, T28 & AD28

Layout Note:
Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top

Layout Note:
Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top near pin AG5

Layout Note:
Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top

Layout Note:
Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top

Layout Note:
Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top near pin AG9

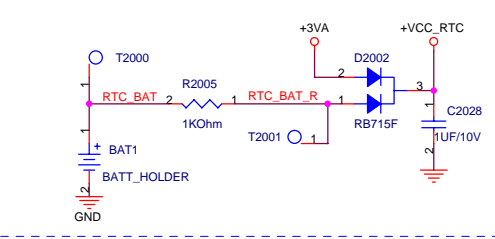
Layout Note:
Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top

If ICH7 embedded Lan controller was used, these pins should connect to +3VSUS for S3-S5 wake up.

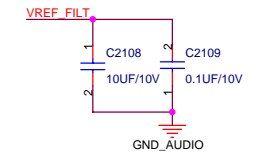
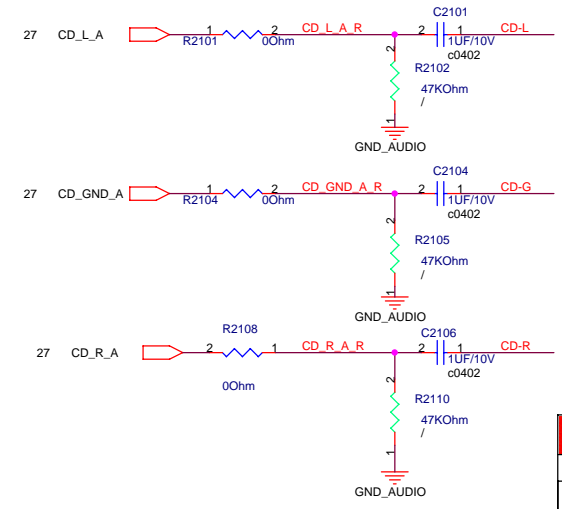
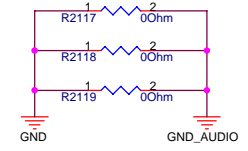
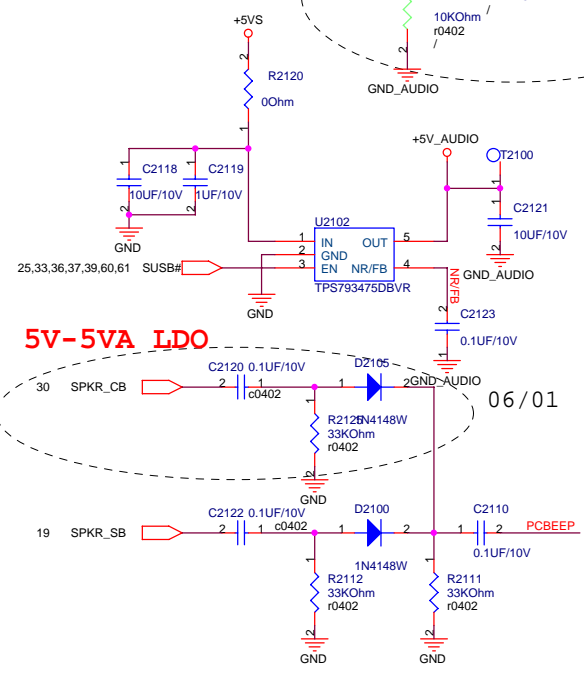
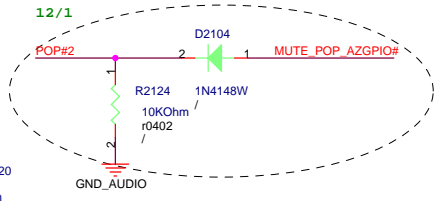
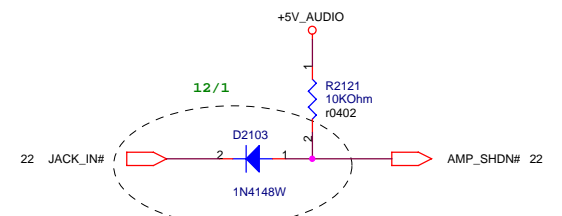
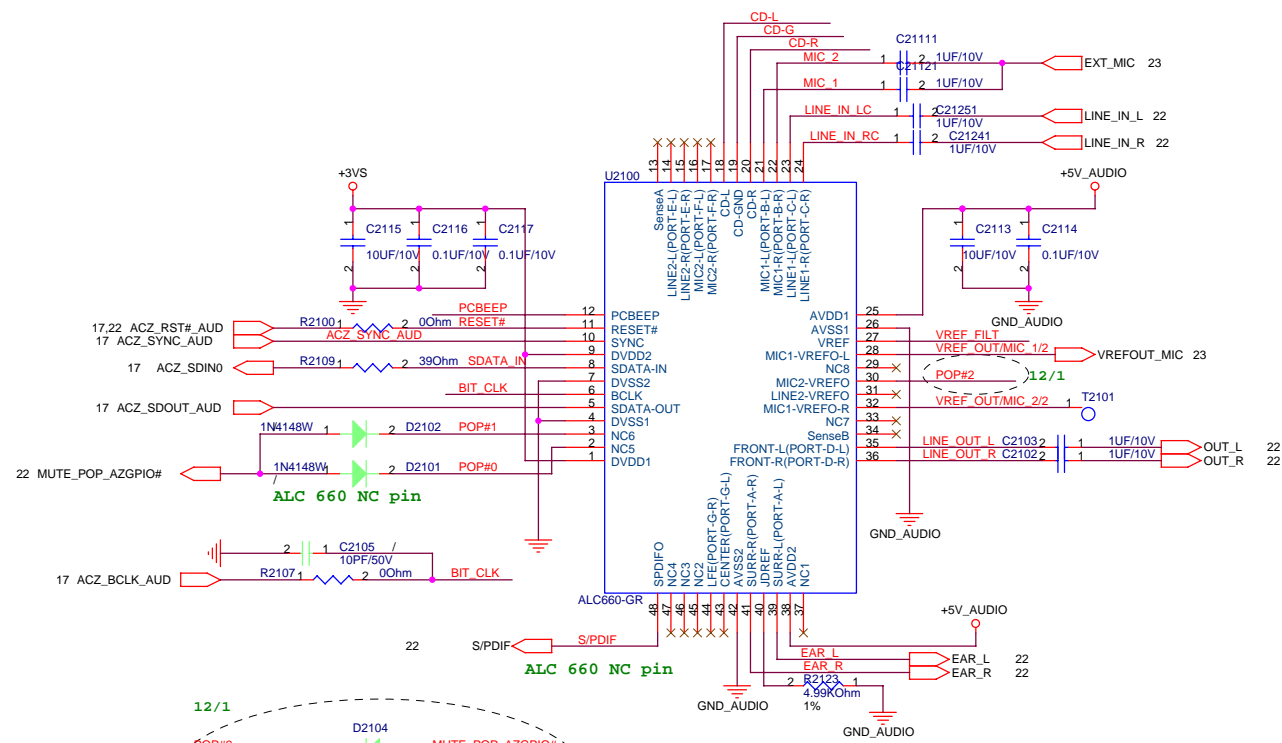
Layout Note:
Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top near pin

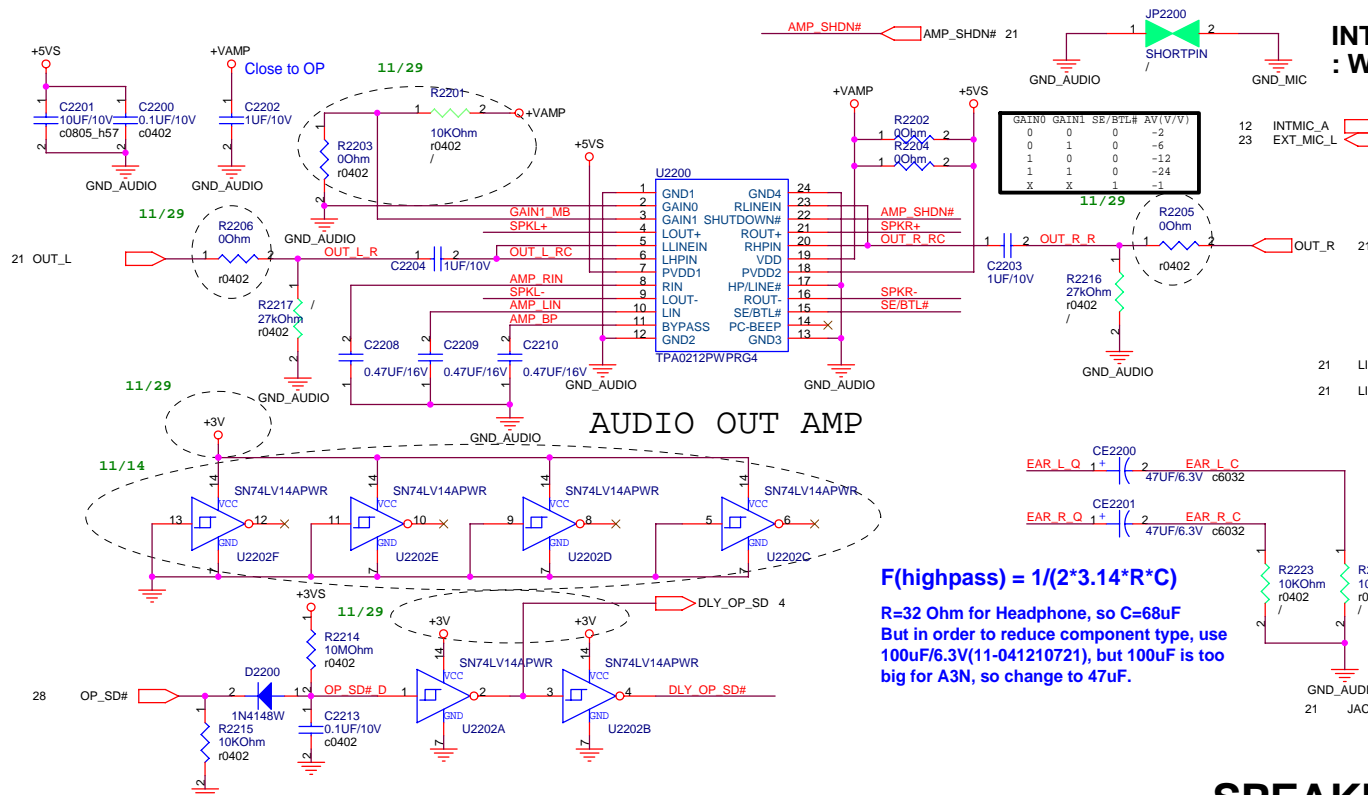
Layout Note:
Place within 100 mils of ICH7-M on the Bottom side or 140 mils on the Top near pin

Layout Note:
Distribute in PCI section

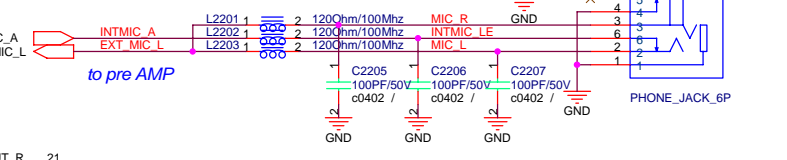


A4	Vss1	Vss98	P28
A23	Vss2	Vss99	R11
B1	Vss3	Vss100	R11
B8	Vss4	Vss101	R12
B11	Vss5	Vss102	R13
B17	Vss6	Vss103	R15
B20	Vss7	Vss104	R16
B26	Vss8	Vss105	R17
B28	Vss9	Vss106	R18
C2	Vss10	Vss107	R19
C6	Vss11	Vss108	T6
C7	Vss12	Vss109	T13
D10	Vss13	Vss110	T14
D13	Vss14	Vss111	T15
D18	Vss15	Vss112	T16
D21	Vss16	Vss113	T17
E1	Vss17	Vss114	U4
E2	Vss18	Vss115	U12
E4	Vss19	Vss116	U13
E8	Vss20	Vss117	U14
F4	Vss21	Vss118	U15
F7	Vss22	Vss119	U16
F28	Vss23	Vss120	U16
G1	Vss24	Vss121	U17
G2	Vss25	Vss122	U17
G5	Vss26	Vss123	U25
G6	Vss27	Vss124	U26
G9	Vss28	Vss125	V2
G29	Vss29	Vss126	V3
G30	Vss30	Vss127	V4
G2	Vss31	Vss128	V7
G1	Vss32	Vss129	V8
G2	Vss33	Vss130	V9
G6	Vss34	Vss131	W6
G14	Vss35	Vss132	W24
G18	Vss36	Vss133	W25
G21	Vss37	Vss134	W26
G24	Vss38	Vss135	Y3
G25	Vss39	Vss136	Y24
G26	Vss40	Vss137	Y27
H3	Vss41	Vss138	Y28
H4	Vss42	Vss139	AA1
H5	Vss43	Vss140	AA24
H2	Vss44	Vss141	AA26
H28	Vss45	Vss142	AB4
J1	Vss46	Vss143	AB6
J2	Vss47	Vss144	AB6
J5	Vss48	Vss145	AB14
J24	Vss49	Vss146	AB16
J25	Vss50	Vss147	AB19
J26	Vss51	Vss148	AB21
K24	Vss52	Vss149	AB24
K27	Vss53	Vss150	AB27
K28	Vss54	Vss151	AC2
L13	Vss55	Vss152	AC2
L15	Vss56	Vss153	AC5
L24	Vss57	Vss154	AC9
L25	Vss58	Vss155	AC9
L26	Vss59	Vss156	AC11
M3	Vss60	Vss157	AD1
M4	Vss61	Vss158	AD4
M5	Vss62	Vss159	AD7
M12	Vss63	Vss160	AD8
M13	Vss64	Vss161	AD11
M14	Vss65	Vss162	AD15
M15	Vss66	Vss163	AD19
M16	Vss67	Vss164	AD23
M17	Vss68	Vss165	AE2
M24	Vss69	Vss166	AE4
M27	Vss70	Vss167	AE8
M28	Vss71	Vss168	AE11
N11	Vss72	Vss169	AE13
N2	Vss73	Vss170	AE18
N5	Vss74	Vss171	AE21
N6	Vss75	Vss172	AE24
N11	Vss76	Vss173	AE25
N12	Vss77	Vss174	AE28
N13	Vss78	Vss175	AE4
N14	Vss79	Vss176	AE8
N15	Vss80	Vss177	AE11
N16	Vss81	Vss178	AE14
N17	Vss82	Vss179	AE27
N18	Vss83	Vss180	AE28
N18	Vss84	Vss181	AG7
N25	Vss85	Vss182	AG7
N26	Vss86	Vss183	AG11
P3	Vss87	Vss184	AG14
P4	Vss88	Vss185	AG17
P12	Vss89	Vss186	AG20
P13	Vss90	Vss187	AG25
P14	Vss91	Vss188	AG25
P15	Vss92	Vss189	AH3
P16	Vss93	Vss190	AH7
P17	Vss94	Vss191	AH12
P24	Vss95	Vss192	AH23
P27	Vss96	Vss193	AH27
P27	Vss97	Vss194	AH27

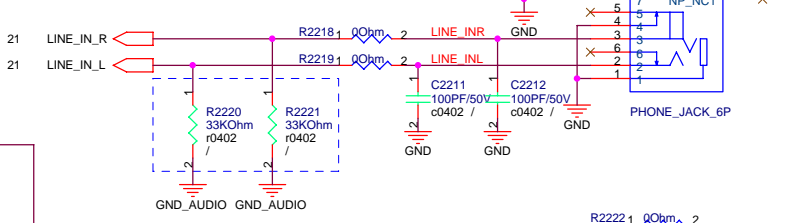




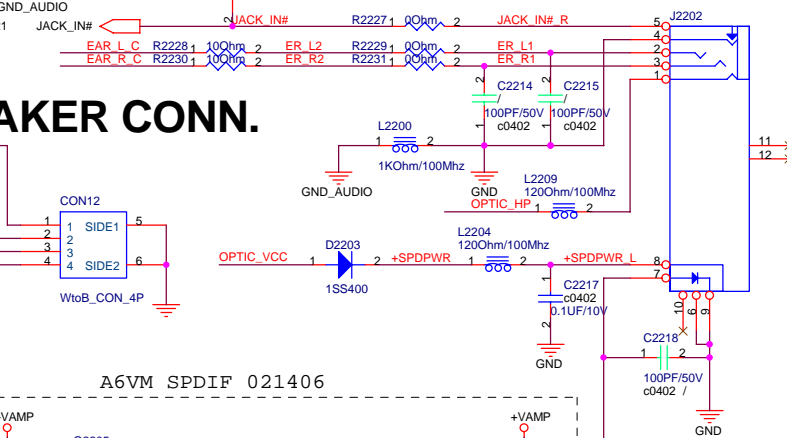
INTMIC_A:GND_AUDIO : W/P/X = 12/5/15mils



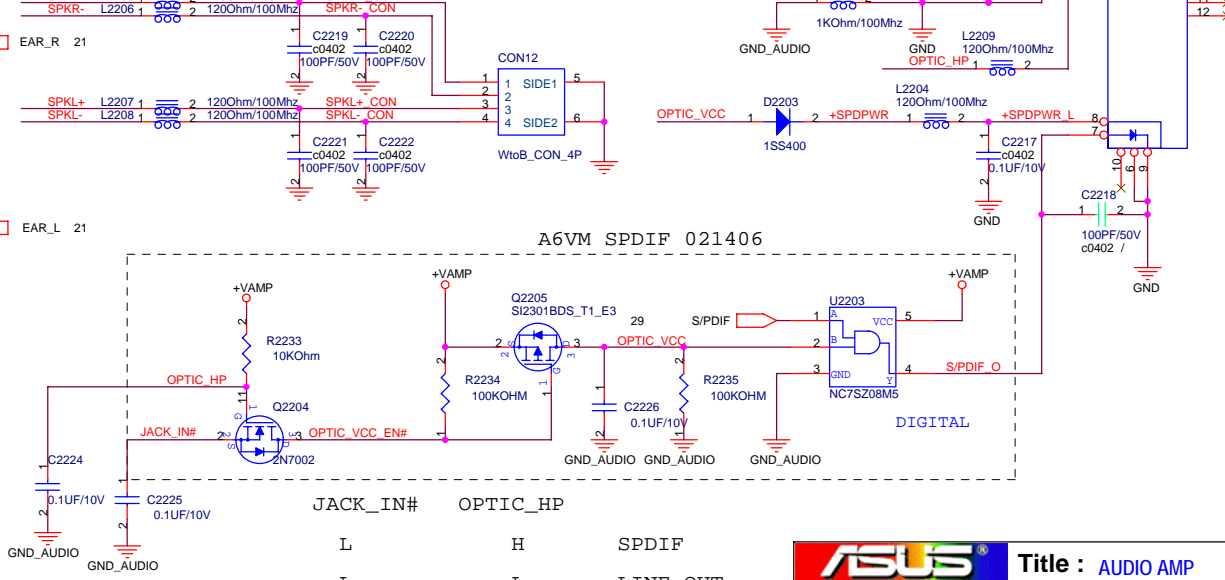
LINE IN JACK



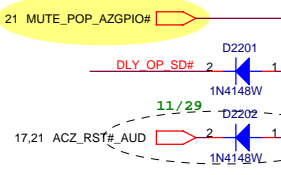
HEADPHONE & S/PDIF



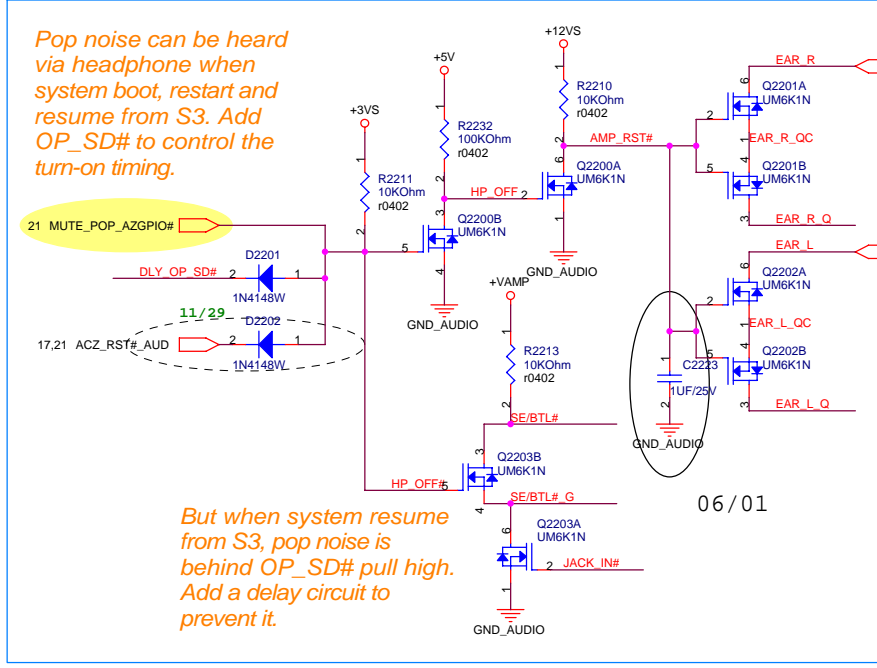
SPEAKER CONN.

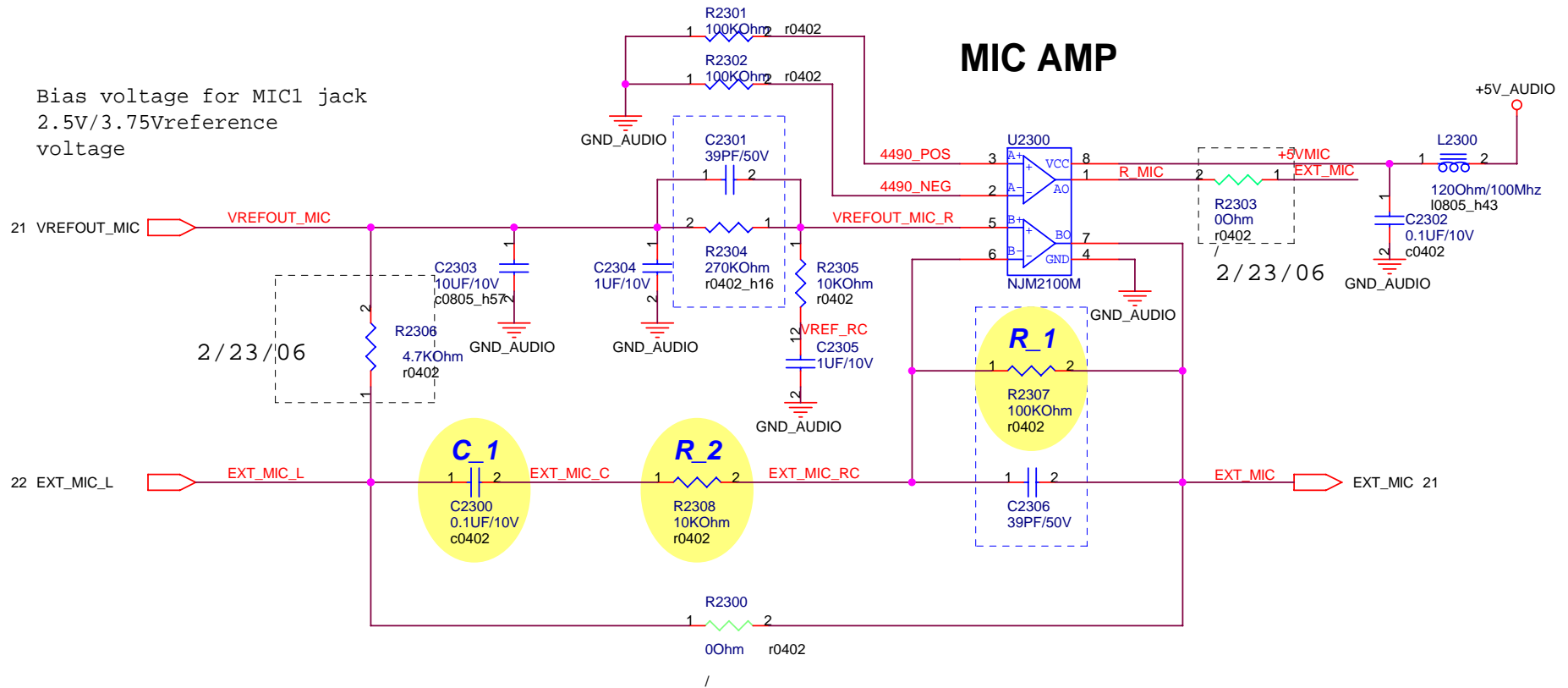


Pop noise can be heard via headphone when system boot, restart and resume from S3. Add OP_SD# to control the turn-on timing.



But when system resume from S3, pop noise is behind OP_SD# pull high. Add a delay circuit to prevent it.





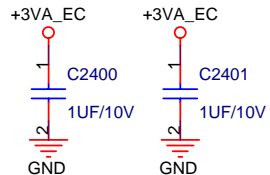
Bias voltage for MIC1 jack
2.5V/3.75Vreference
voltage

MIC AMP

High-Pass Filter Cutoff Frequency
 $F_c = 1 / (2 * 3.14 * C_1 * R_2) = 159 \text{ Hz}$

Gain = - R_1 / R_2 = -10

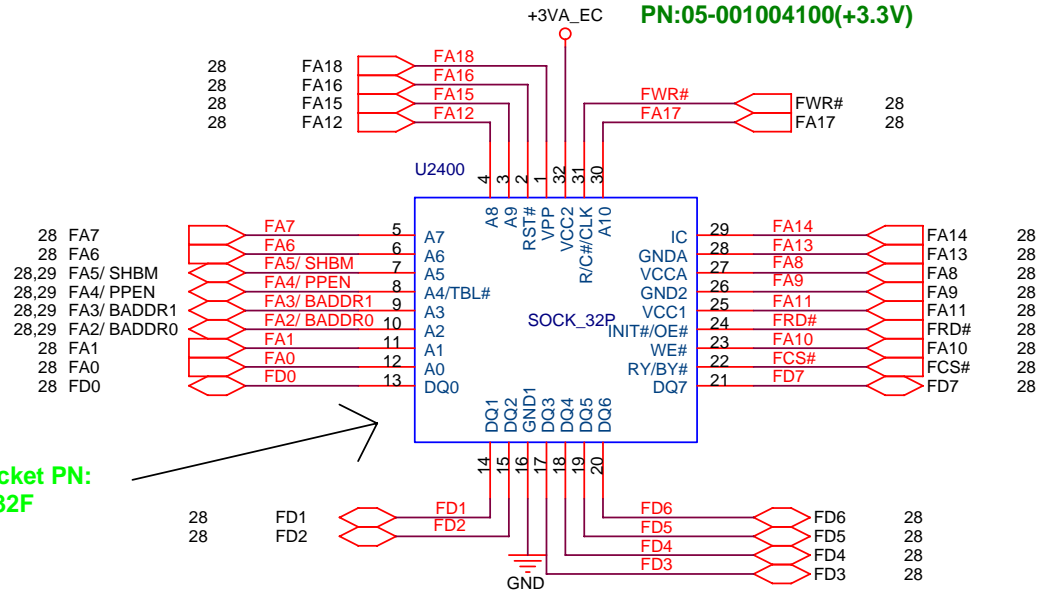
ASUS		Title : MIC Pre-AMP	
ASUSTek COMPUTER INC. NB1		Engineer: Jack Wang	
Size A4	Project Name A6F	Rev 1.1	
Date: Monday, March 06, 2006		Sheet 23 of 63	

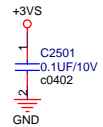


ISA ROM

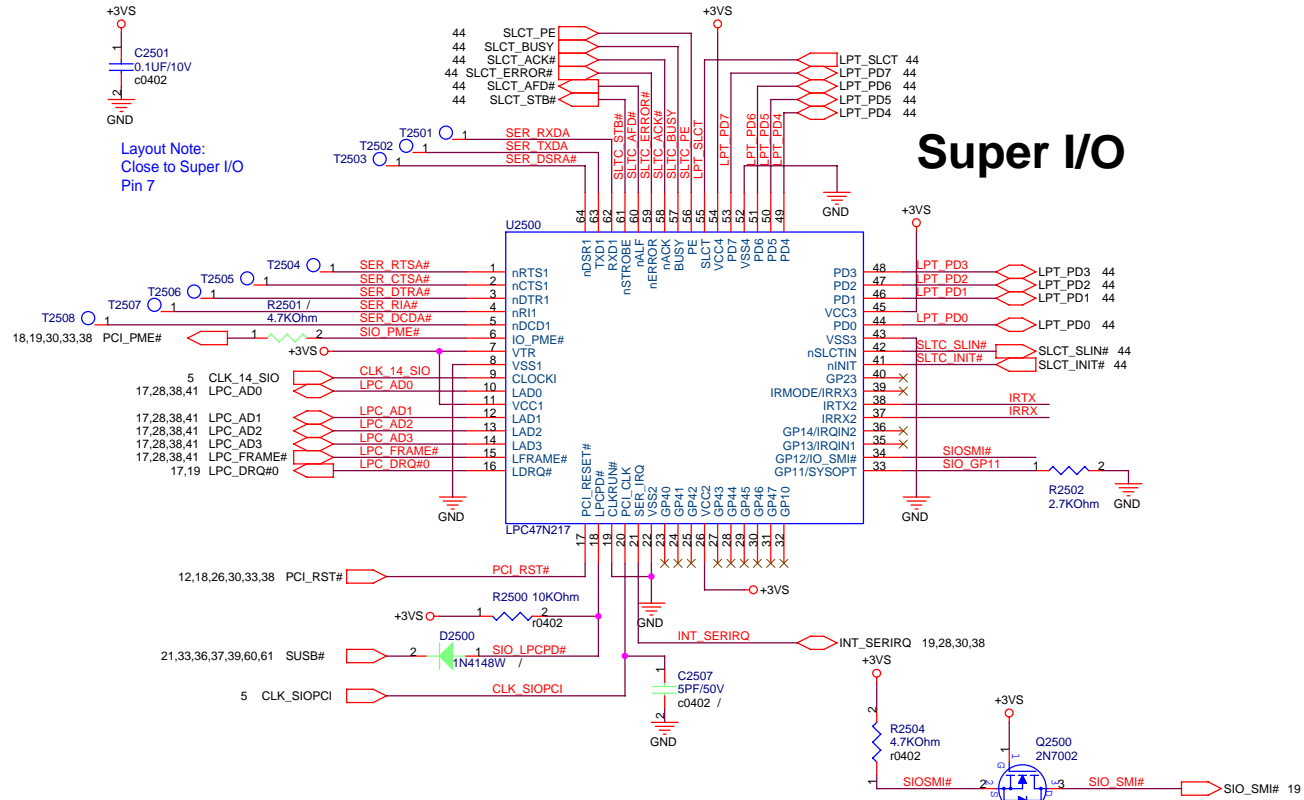
**SST-PLCC32 4Mbits Flash ROM
PN:05-001004100(+3.3V)**

**PLCC32 Socket PN:
12G04300032F**

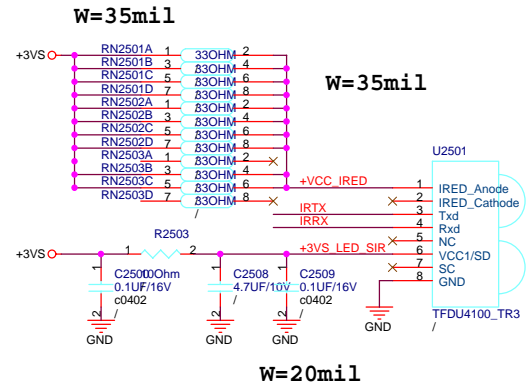
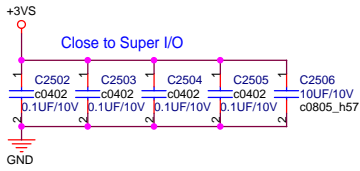




Layout Note:
Close to Super I/O
Pin 7

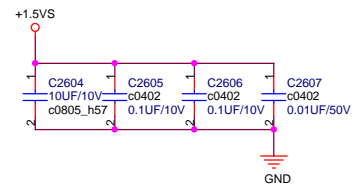
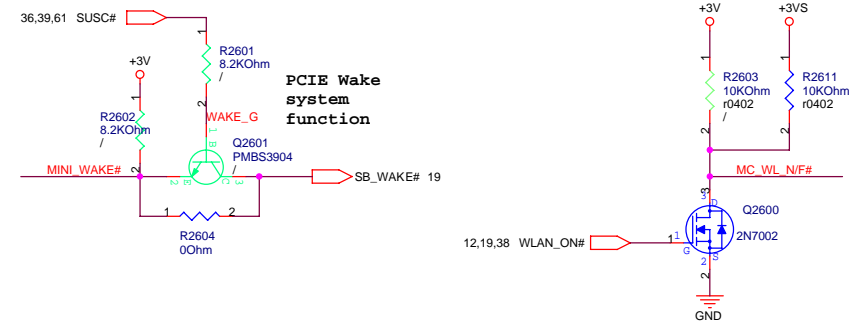
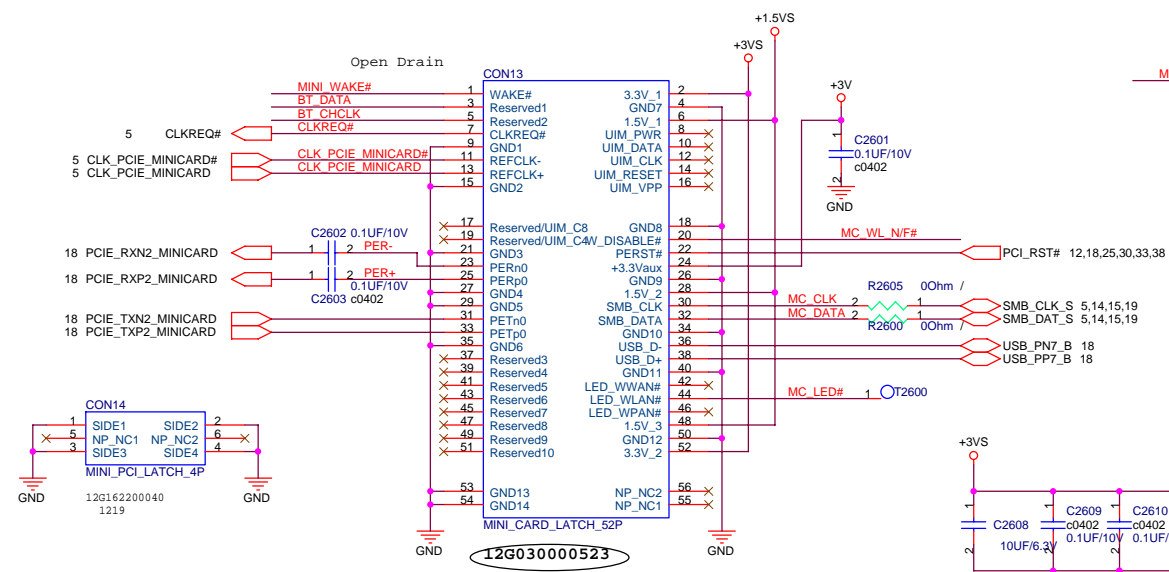


Super I/O



W=20mil

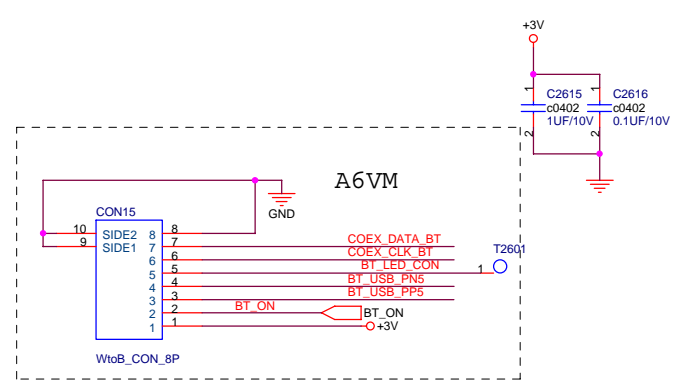
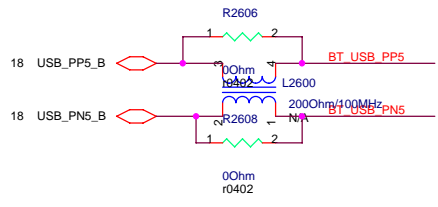
MINI PCIEX CONNECTOR



+3V : 1000 mA (peak)
 +1.5V: 500mA (peak)
 +3VSUS: 330mA (peak)

Check O/D output or push pull

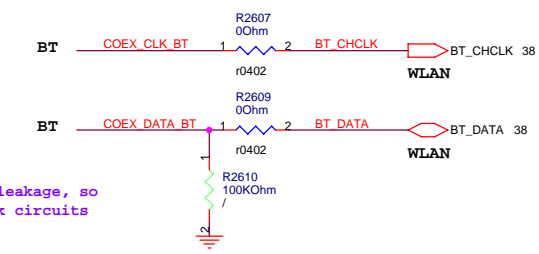
BLUETOOTH CONNECTOR



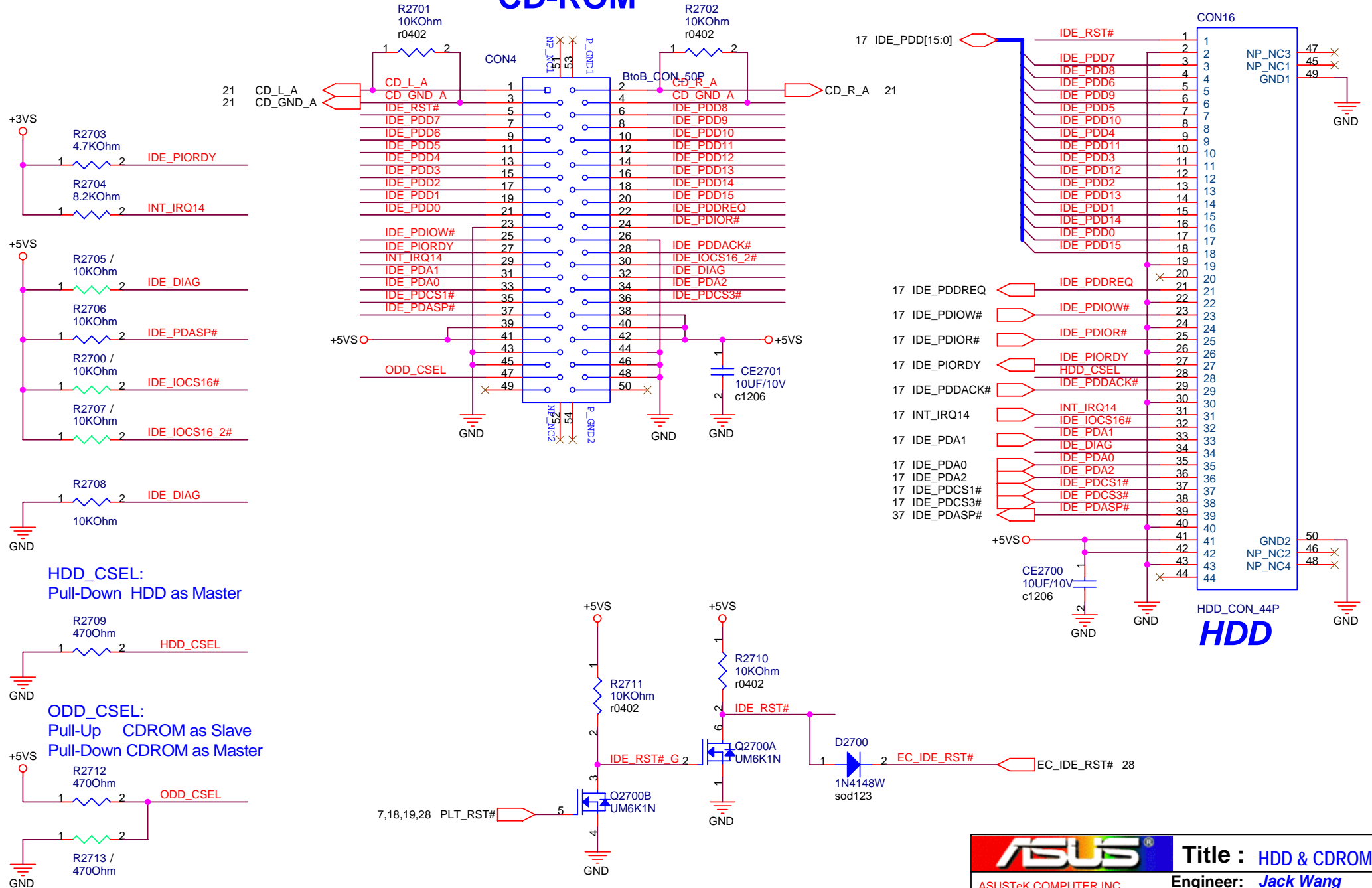
Signal direction-
 CLK: BT -> WLAN;
 DATA: WLAN -> BT

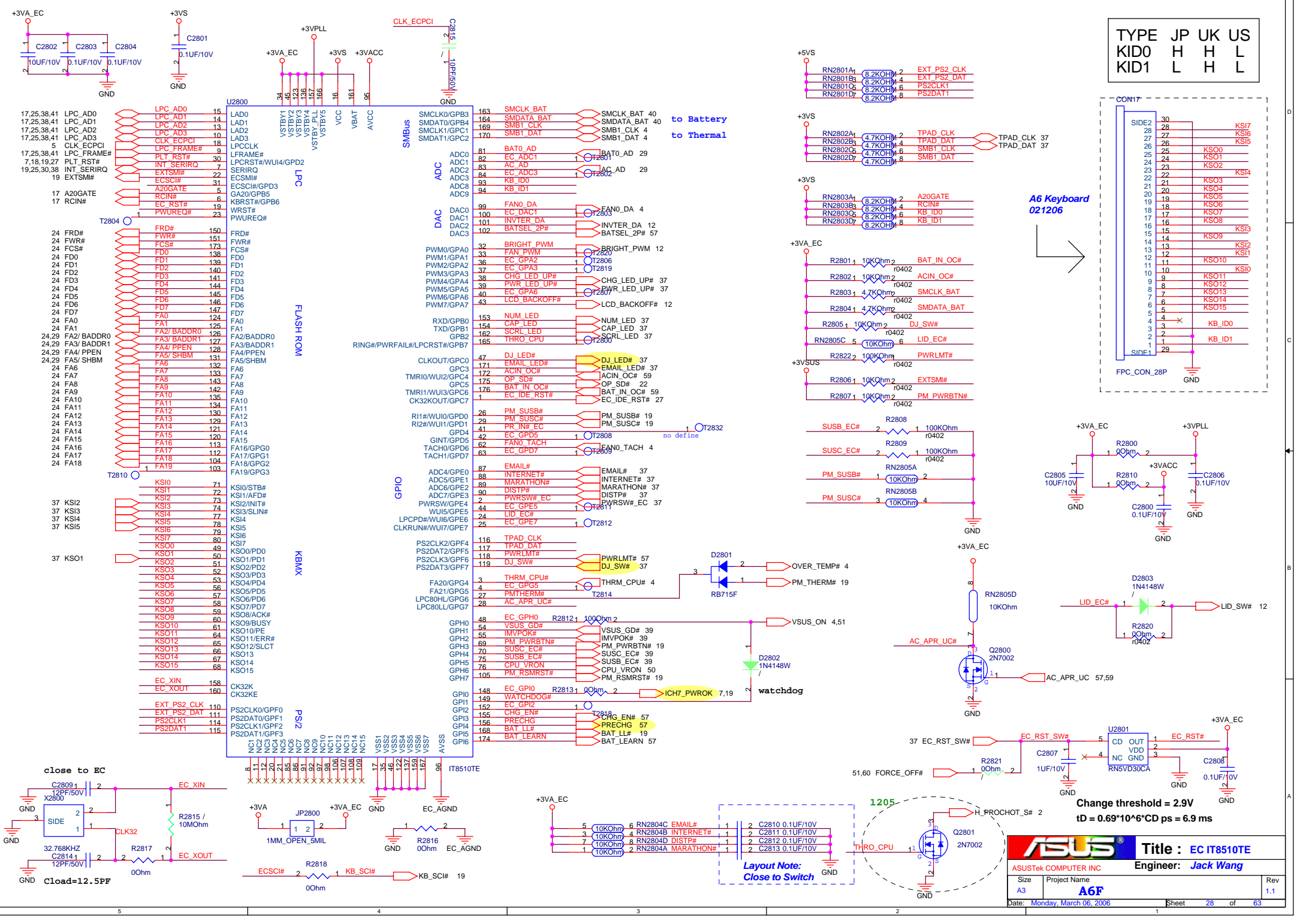
BT_ON 3.3V at GPIO38

BT Module has no leakage, so discard PMOS block circuits

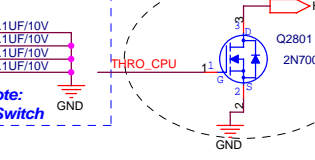
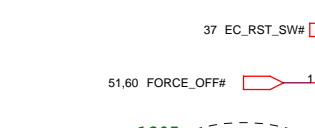
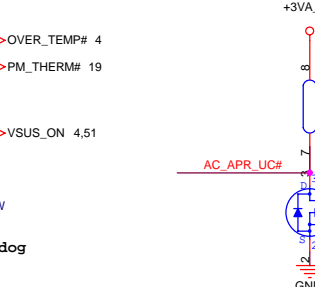
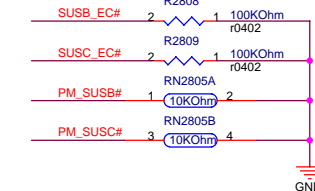
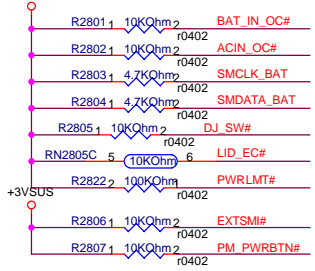
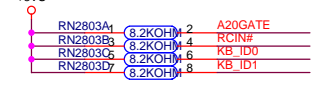
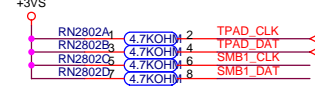
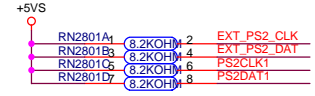
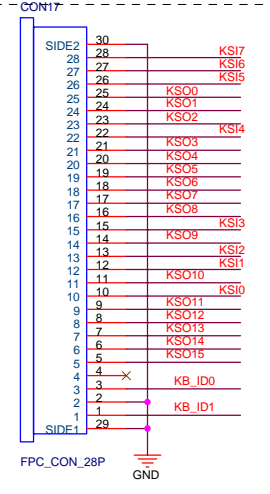


CD-ROM

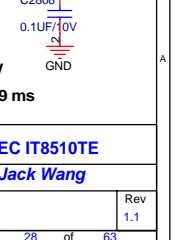
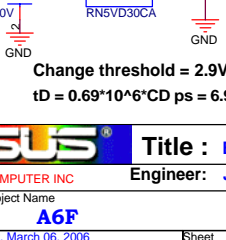
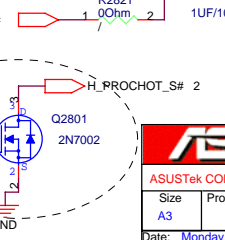
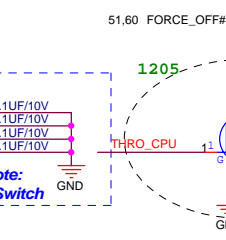
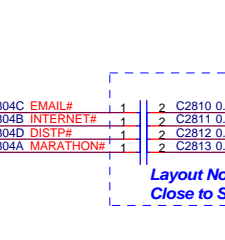
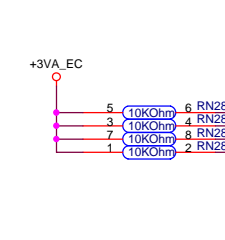
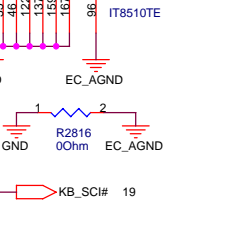
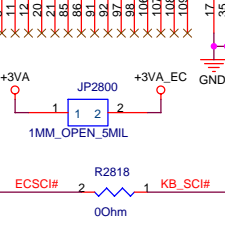
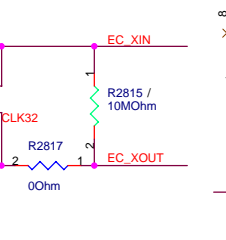
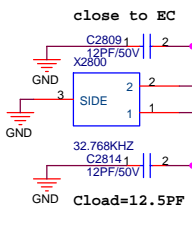
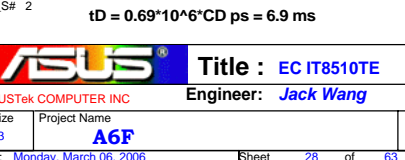
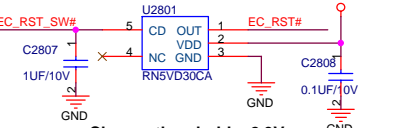
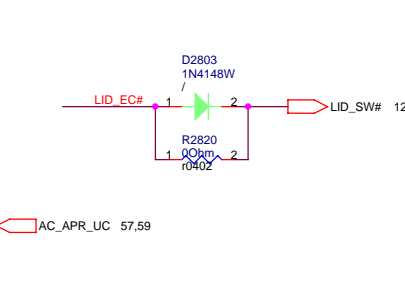
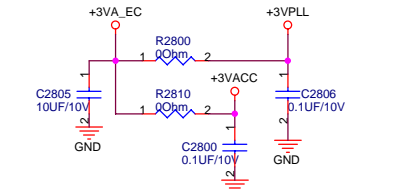




TYPE	JP	UK	US
KID0	H	H	L
KID1	L	H	L



A6 Keyboard
021206

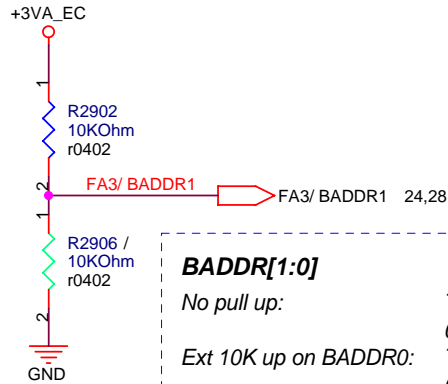
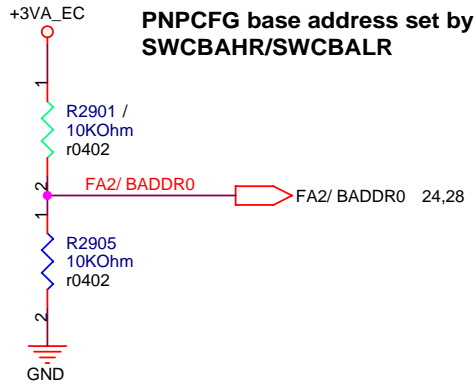


Layout Note:
Close to Switch

Change threshold = 2.9V
tD = 0.69*10^6 CD ps = 6.9 ms

EC Hardware Strap

Strap value sampled after VSTBY power up reset



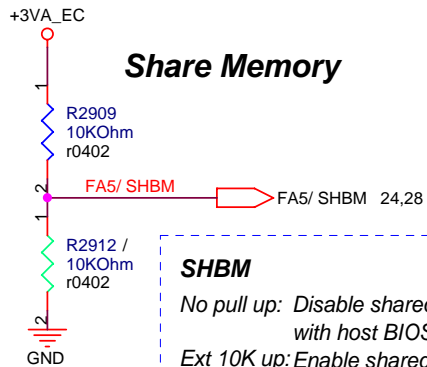
BADDR[1:0]

No pull up:

Ext 10K up on BADDR0:

Ext 10K up on BADDR1:

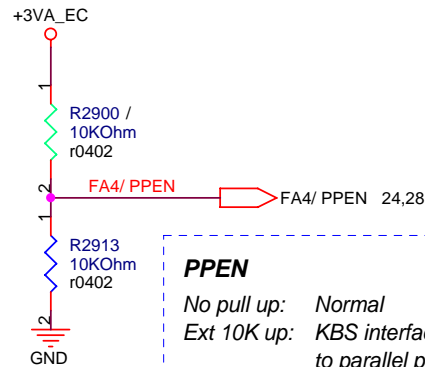
The register pair to access PNPCFG is 002Eh and 002Fh.
 The register pair to access PNPCFG is 004Eh and 004Fh.
 The register pair to access PNPCFG is determined by EC domain registers SWCBALR and SWCBAHR.



Share Memory

SHBM

No pull up: Disable shared memory with host BIOS
 Ext 10K up: Enable shared memory with host BIOS

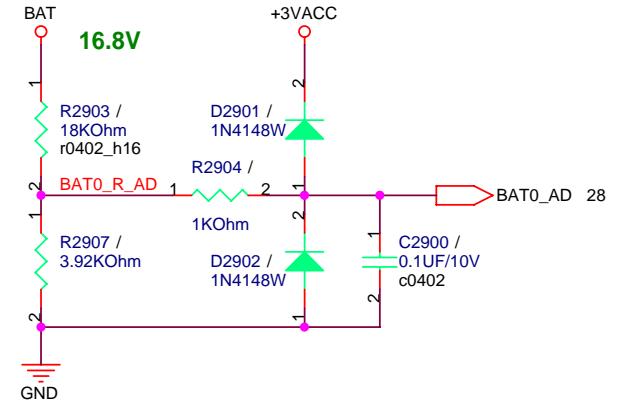


PPEN

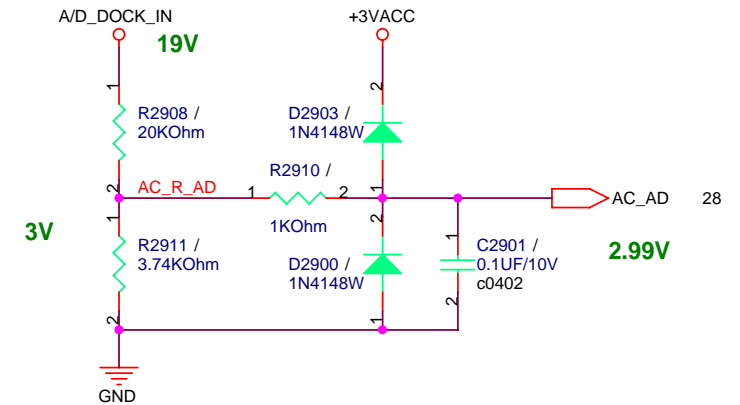
No pull up: Normal
 Ext 10K up: KBS interface pins are switched to parallel port interface for in-system programming.

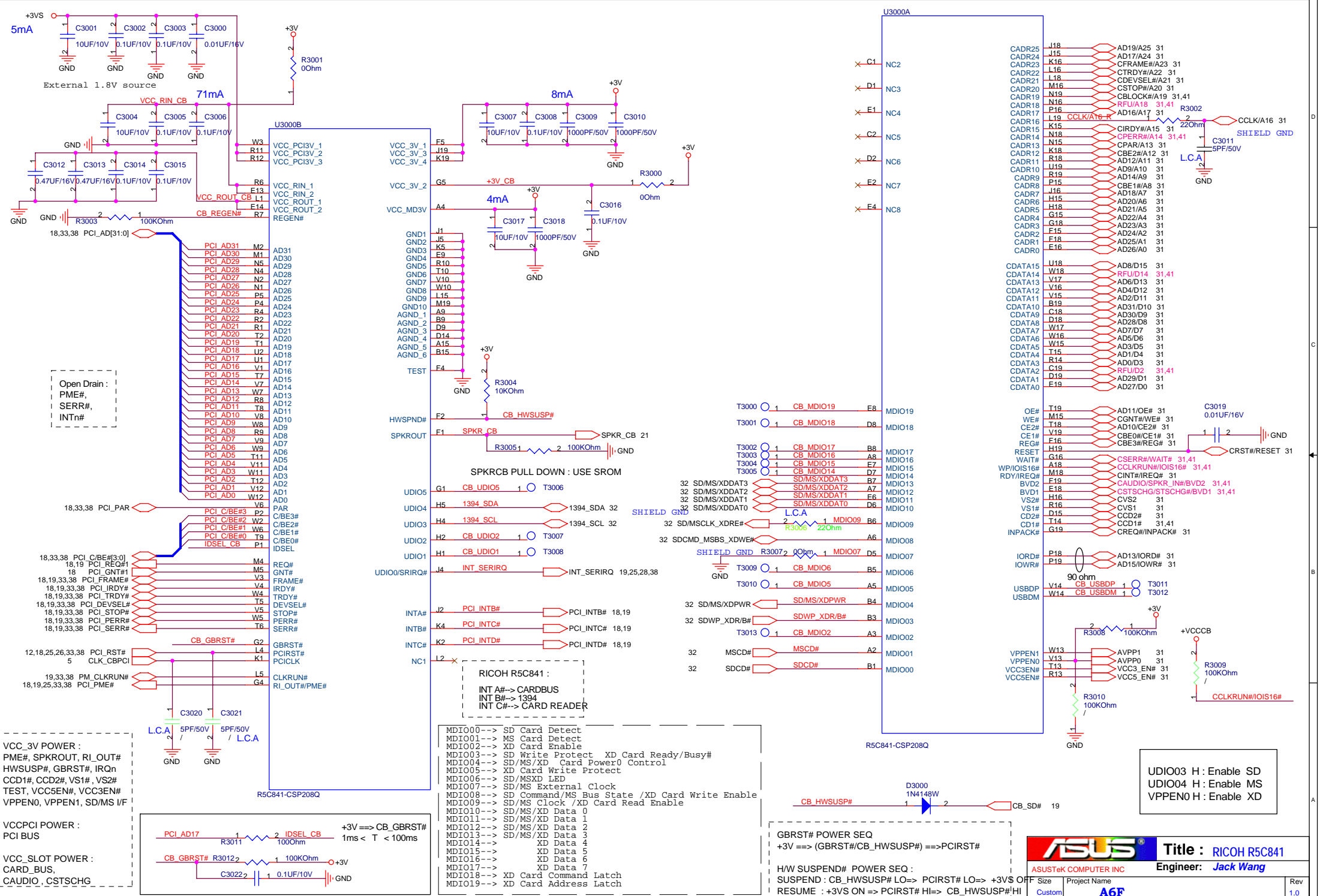
EC ADC

Battery



Adaptor

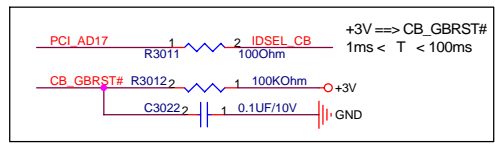




VCC_3V POWER :
 PME#, SPKROUT, RI_OUT#
 HWSUSP#, GBRST#, IRQn
 CCD1#, CCD2#, VS1#, VS2#
 TEST, VCC5EN#, VCC3EN#
 VPPEN0, VPPEN1, SD/MS I/F

VCCPCI POWER :
 PCI BUS

VCC_SLOT POWER :
 CARD_BUS,
 CAUDIO, CSTSCHG



RICOH R5C841 :

INT A#-> CARDBUS
 INT B#-> 1394
 INT C#-> CARD READER

MDIO00->	SD Card Detect
MDIO01->	MS Card Detect
MDIO02->	XD Card Enable
MDIO03->	SD Write Protect / XD Card Ready/Busy#
MDIO04->	SD/MS/XD Card Power0 Control
MDIO05->	XD Card Write Protect
MDIO06->	SD/MSXD LED
MDIO07->	SD/MS External Clock
MDIO08->	SD Command/MS Bus State / XD Card Write Enable
MDIO09->	SD/MS Clock / XD Card Read Enable
MDIO10->	SD/MS/XD Data 0
MDIO11->	SD/MS/XD Data 1
MDIO12->	SD/MS/XD Data 2
MDIO13->	SD/MS/XD Data 3
MDIO14->	XD Data 4
MDIO15->	XD Data 5
MDIO16->	XD Data 6
MDIO17->	XD Data 7
MDIO18->	XD Card Command Latch
MDIO19->	XD Card Address Latch

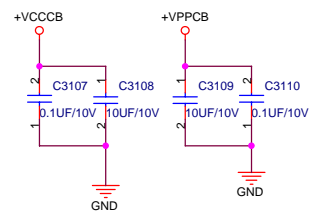
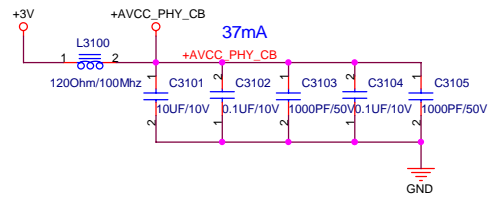
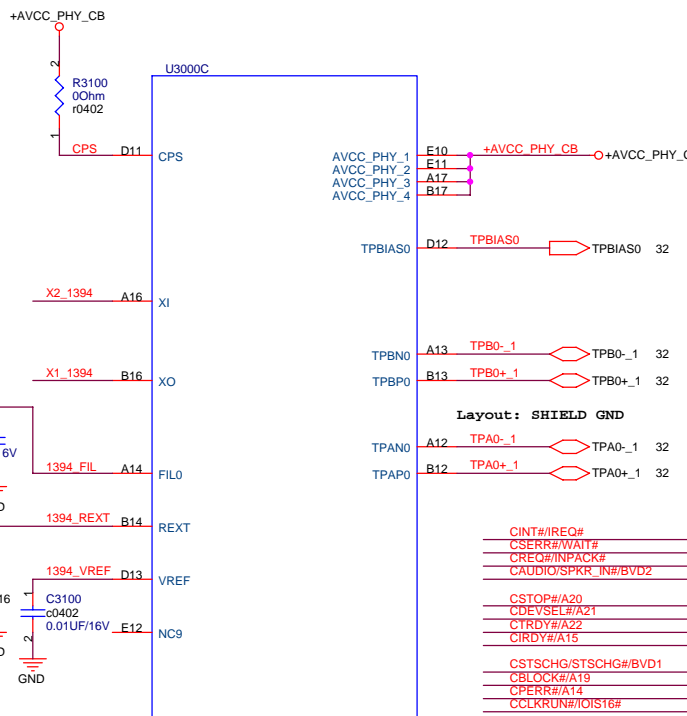
GBRST# POWER SEQ
 +3V ==> (GBRST#/CB_HWSUSP#) ==>PCIRST#

H/W SUSPEND# POWER SEQ :
 SUSPEND : CB_HWSUSP# LO=> PCIRST# LO=> +3V\$ OF
 RESUME : +3VS ON => PCIRST# HI=> CB_HWSUSP# HI

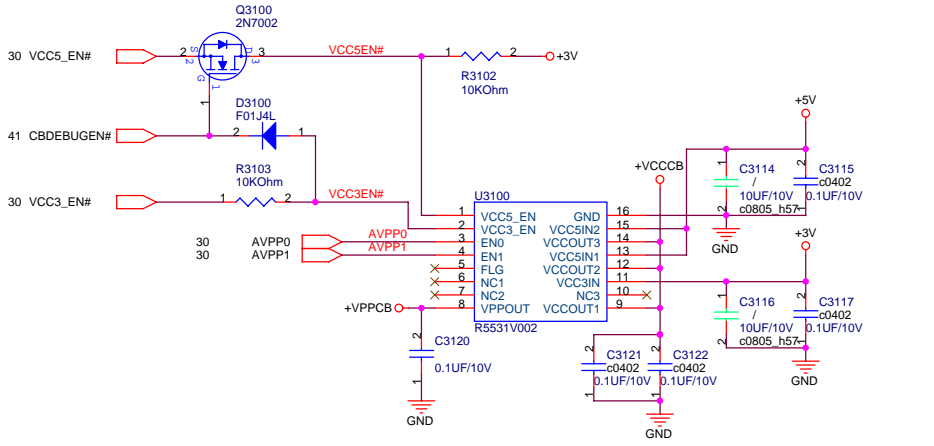
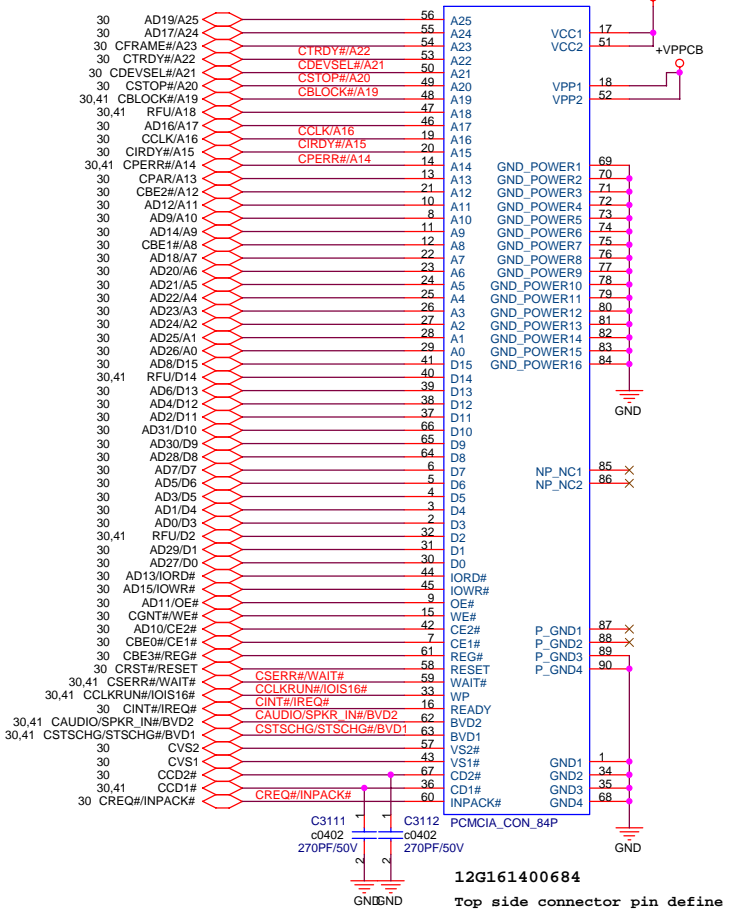
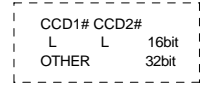
ASUS Title : **RICOH R5C841**
 ASUSTek COMPUTER INC Engineer: **Jack Wang**

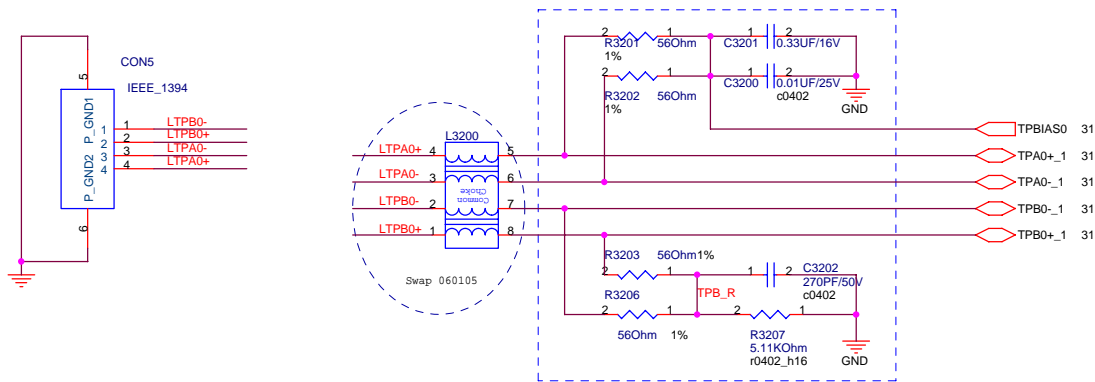
Project Name
 Date: Monday, March 06, 2006 Sheet 30 of 63

UDIO03 H : Enable SD
 UDIO04 H : Enable MS
 VPPEN0 H : Enable XD

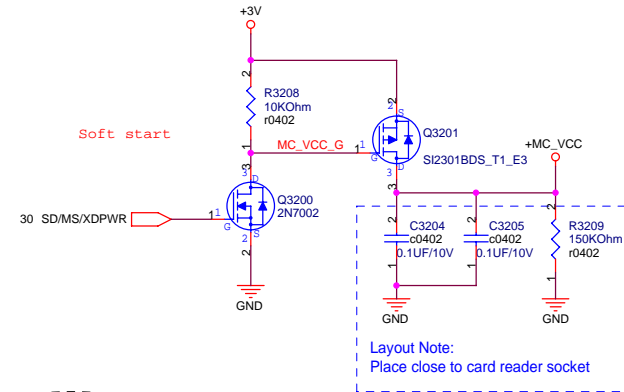
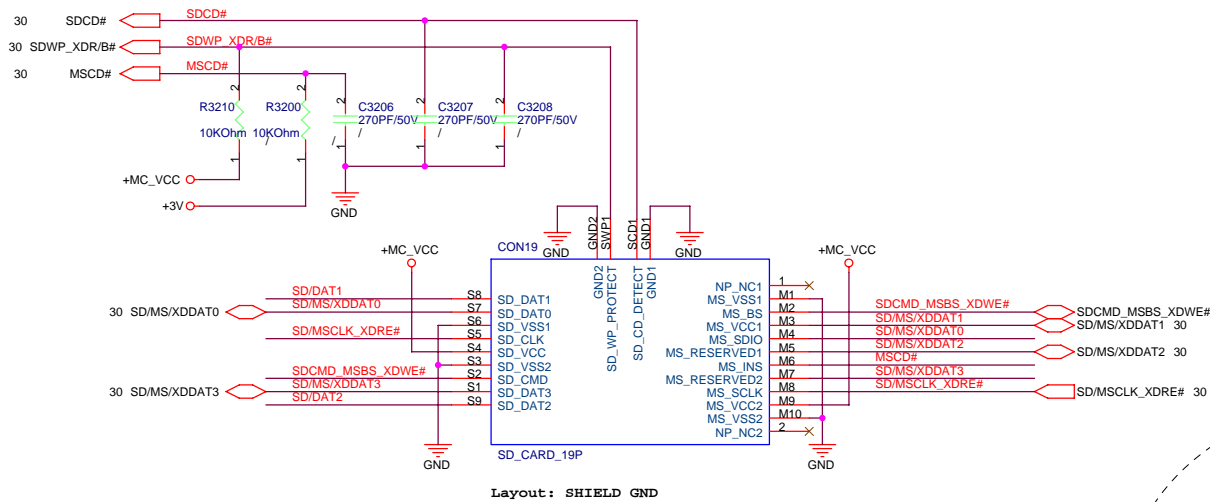
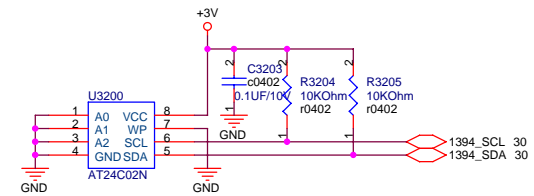


PCMCIA SOCKET

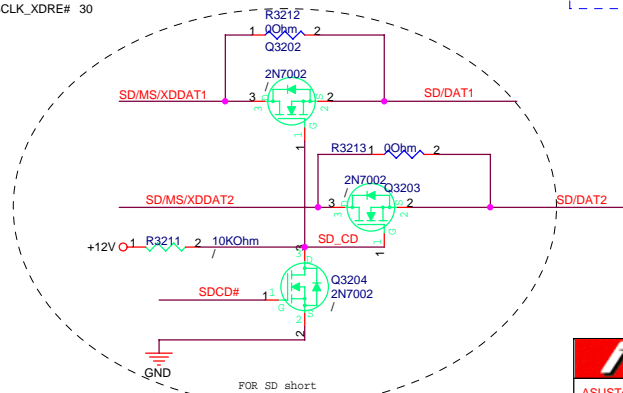


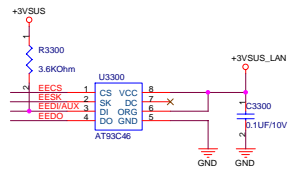


1. Close to R5C841
2. The area is as compact as possible, length < 10 mm
3. TPA Pair and TPB pair mismatch < 2.5mm
4. No via recommend, maximum is one.
5. Total length < 50 mm
6. Differential impedance is 110+/- 6 ohm
7. TPA Pair trace or TPB pair trace mismatch < 1.25mm

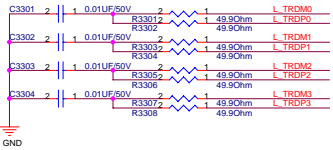


Layout Note:
Place close to card reader socket

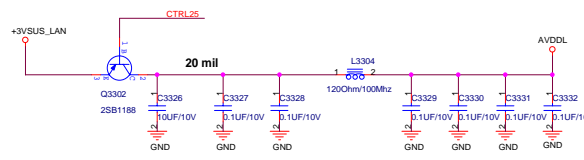
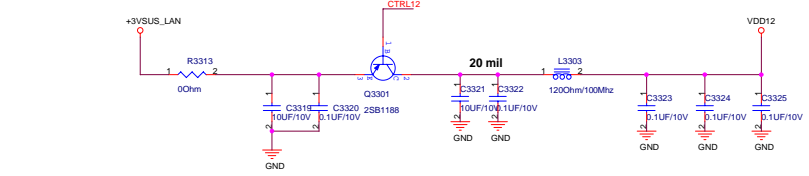
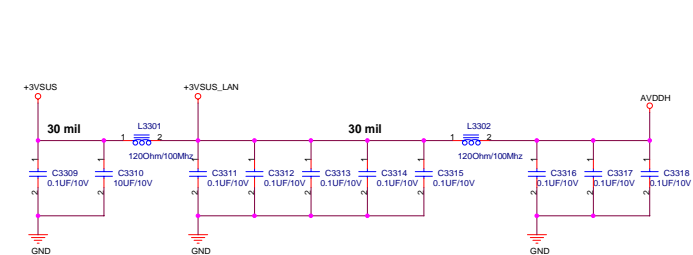
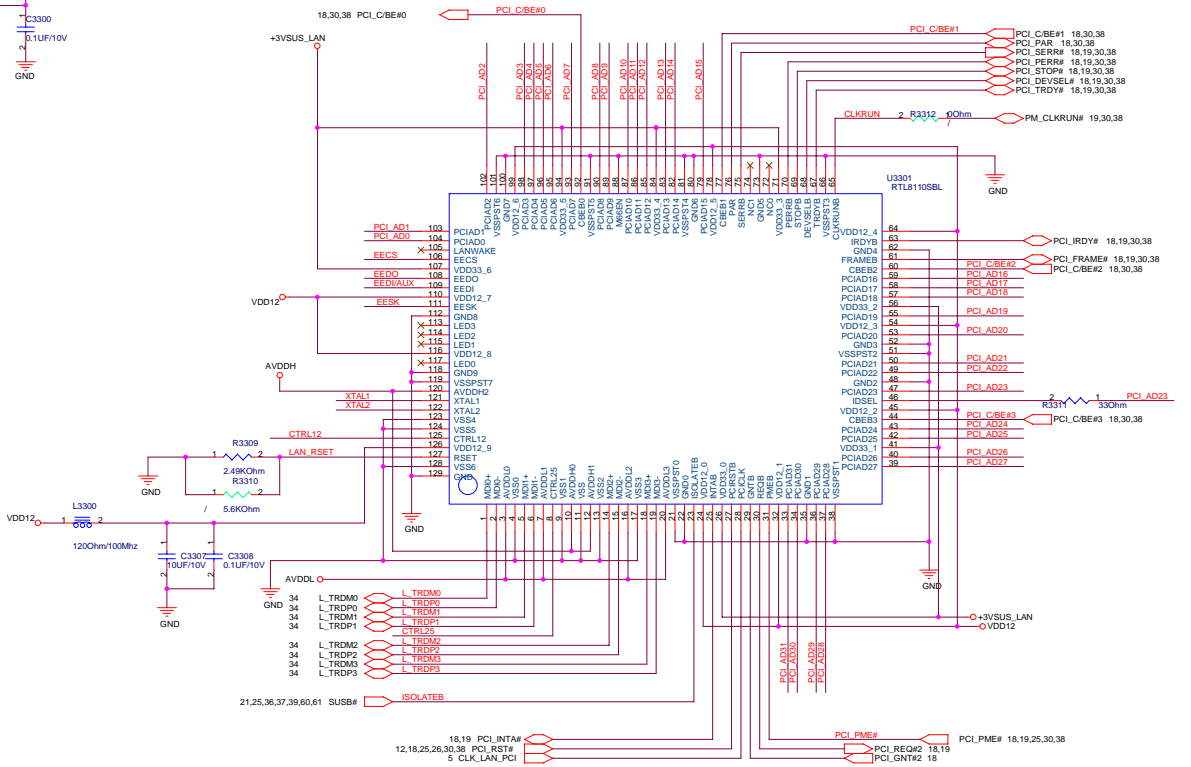
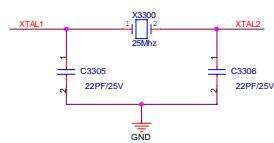


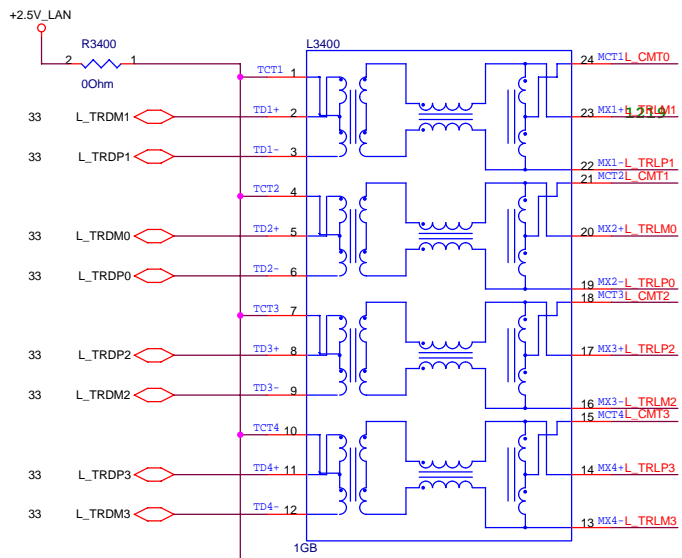


*All termination resistors should be near chip

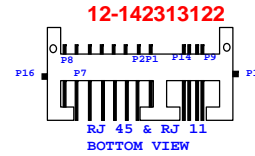
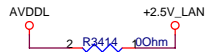
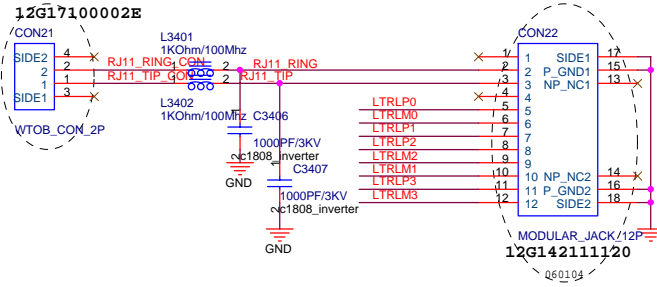


The Crystal should be placed far away from I/O ports, important or high frequency signal traces (Tx, Rx, power), magnetics or board edges.

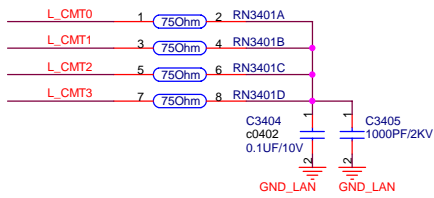
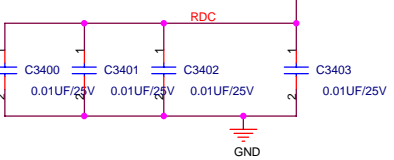




LAN PORT

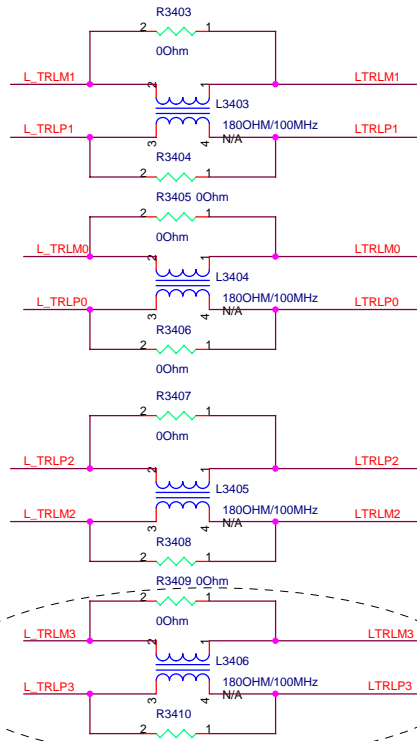
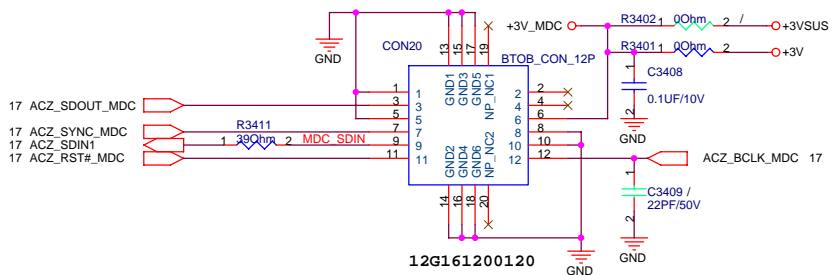


LAN PORT

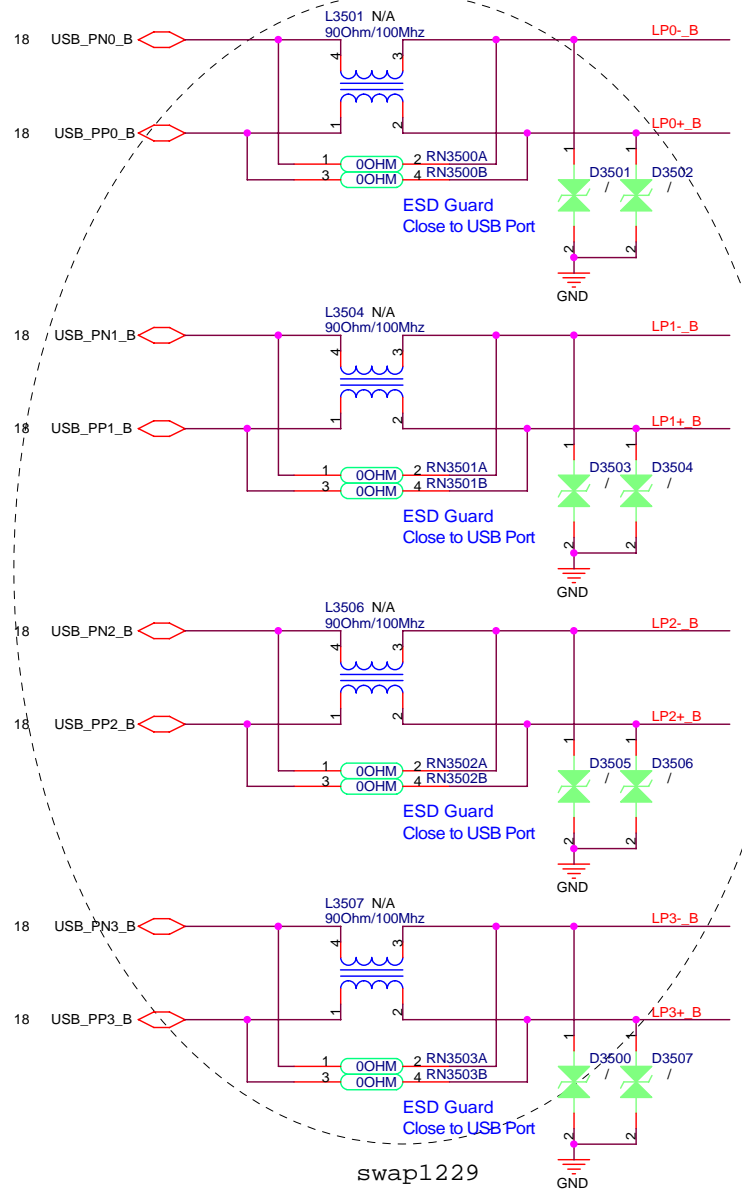


Change 1228

MDC Conn

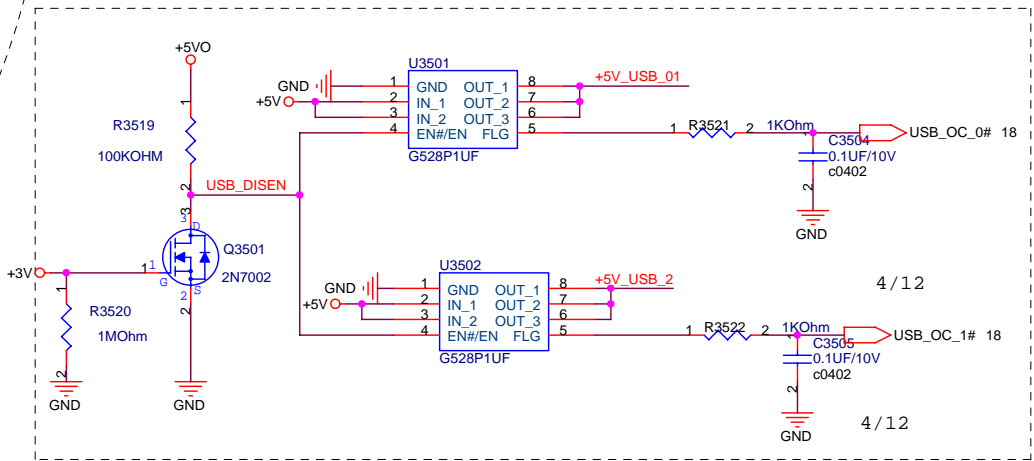
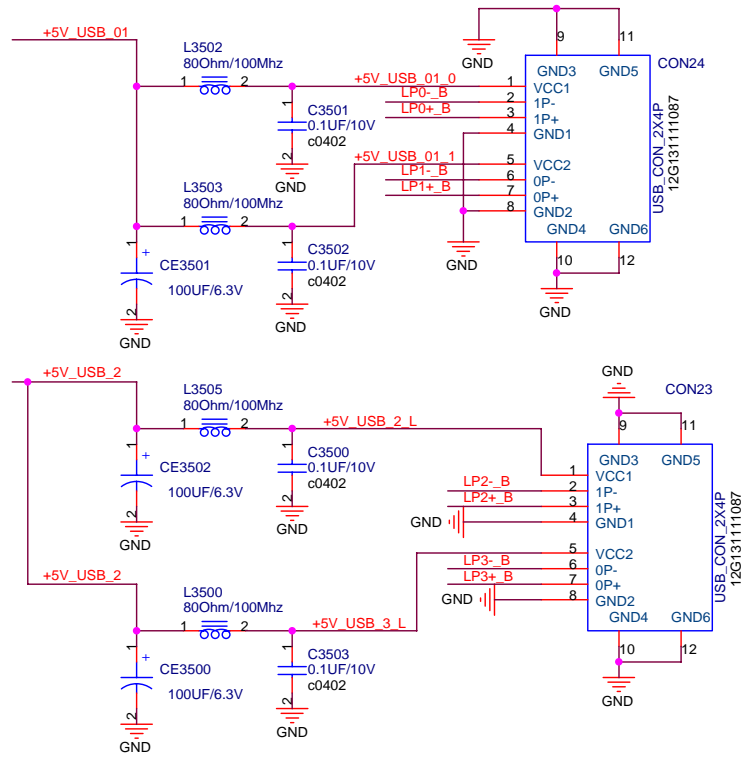


12.26 swap1229

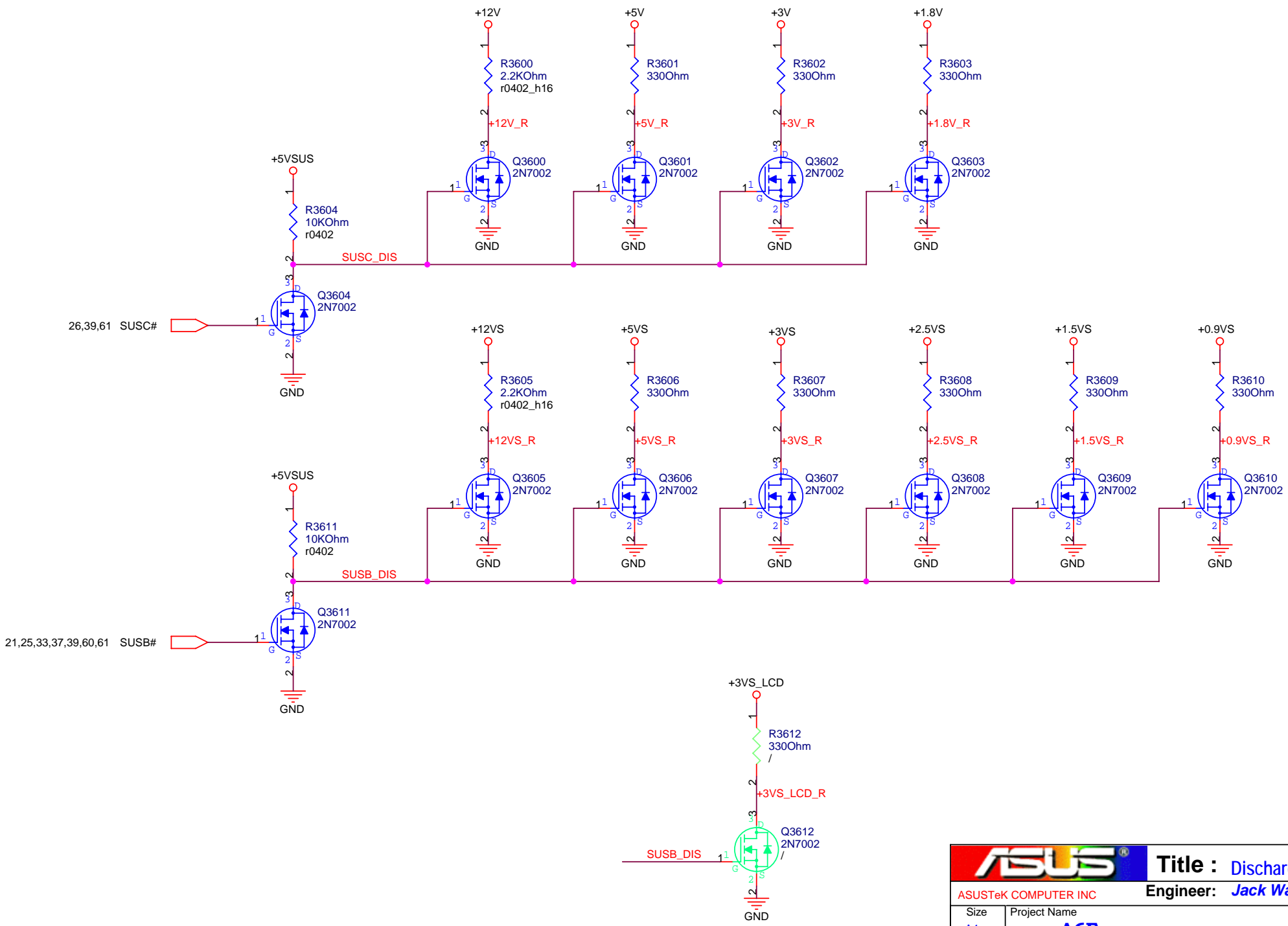


swap1229

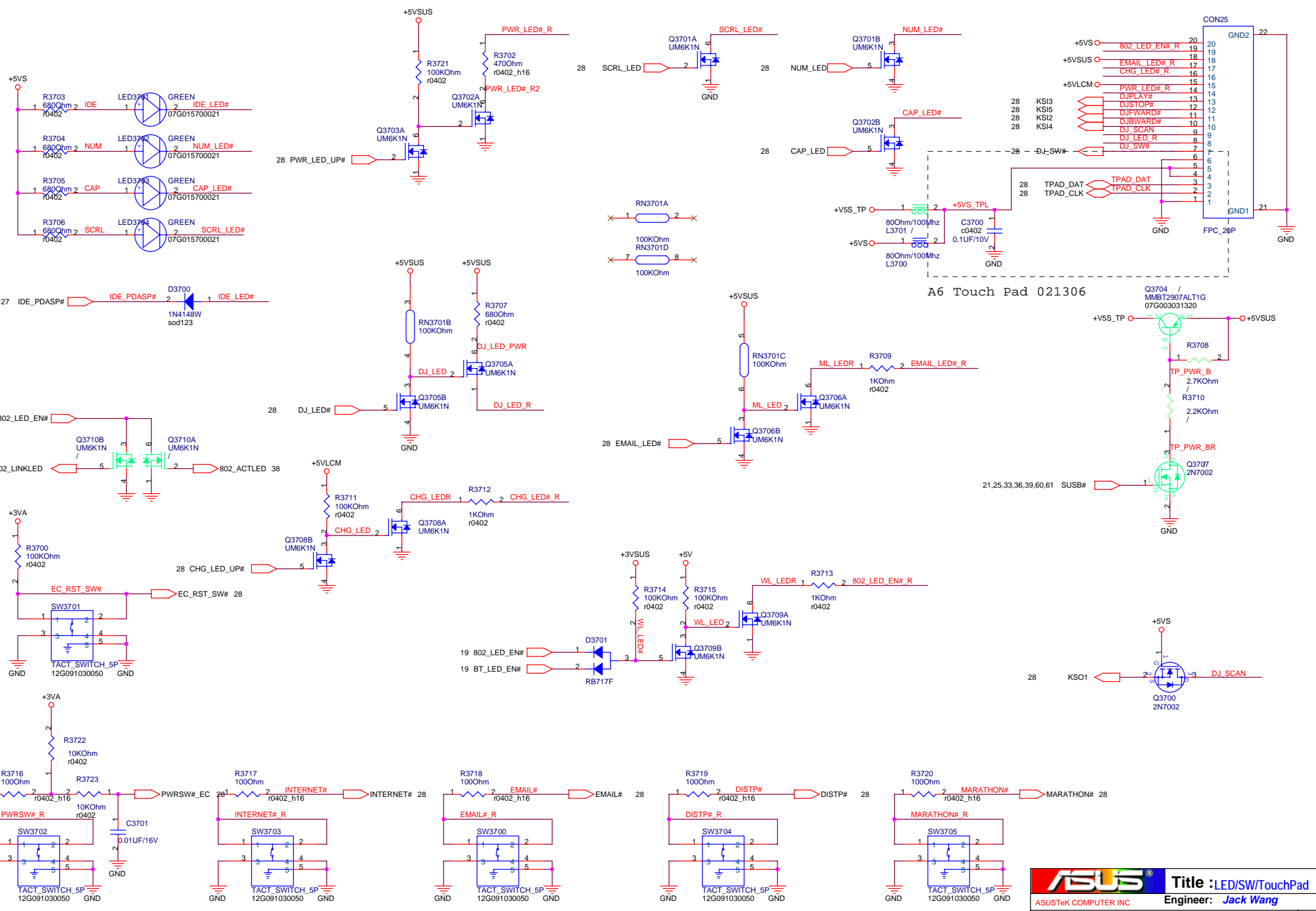
11 / 29

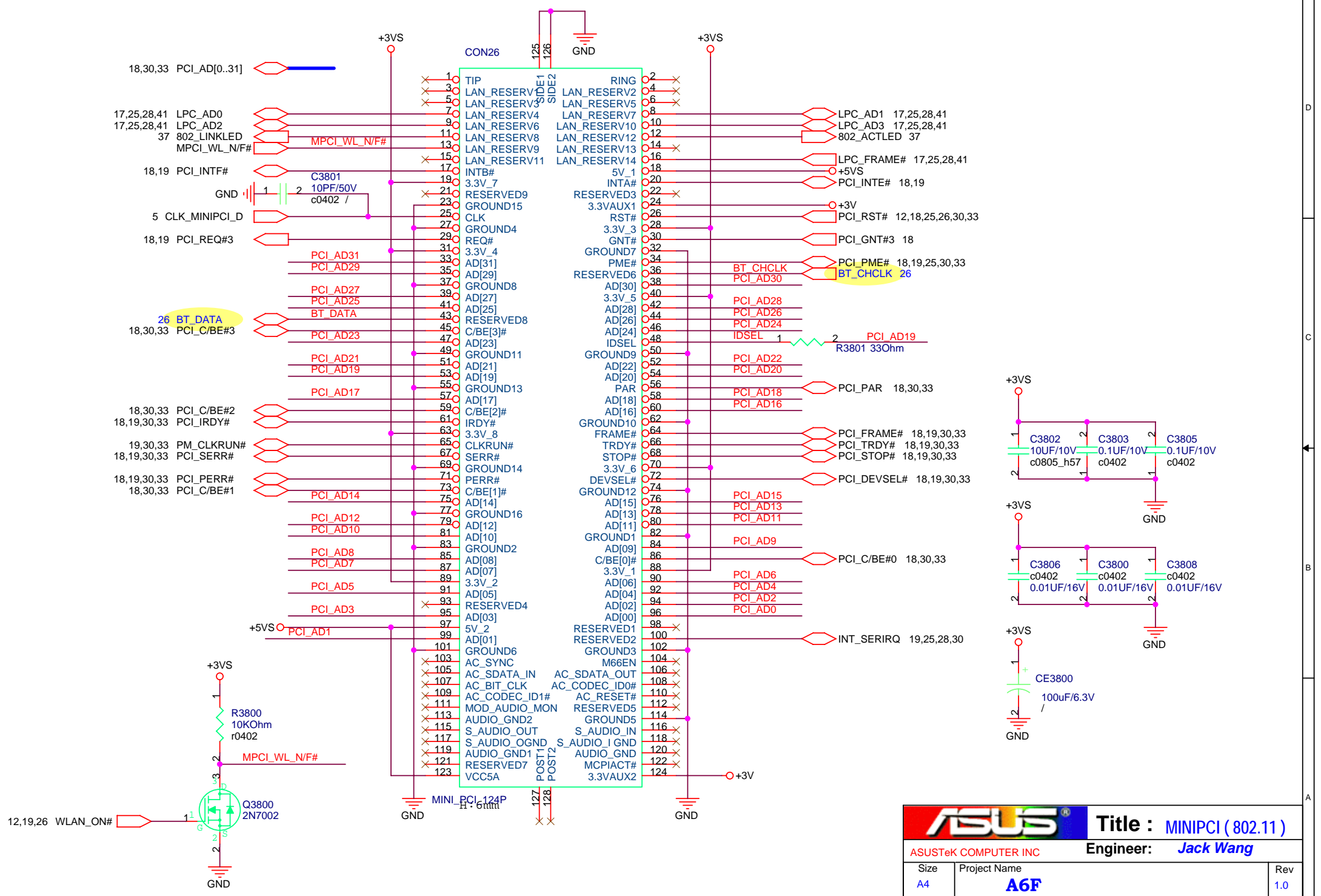


Jack 12/12



		Title : Discharge Circuit	
ASUSTeK COMPUTER INC		Engineer: Jack Wang	
Size A4	Project Name A6F	Rev 1.0	
Date: Monday, March 06, 2006		Sheet	36 of 63

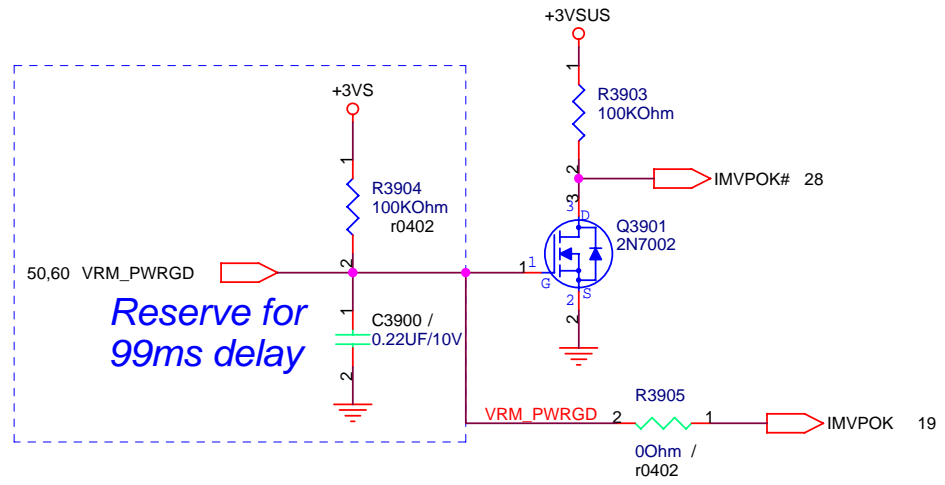
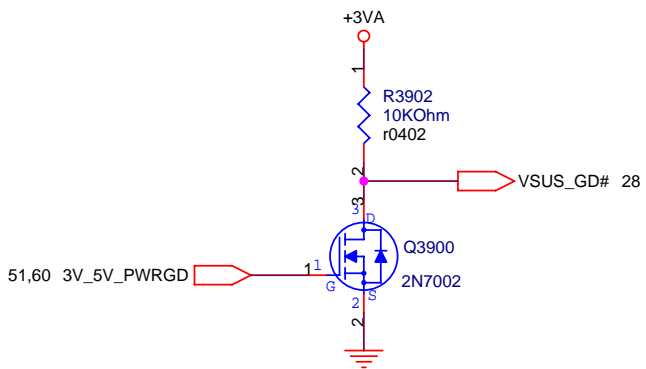
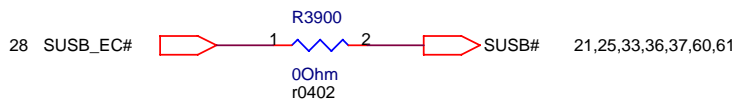
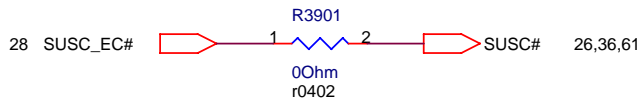




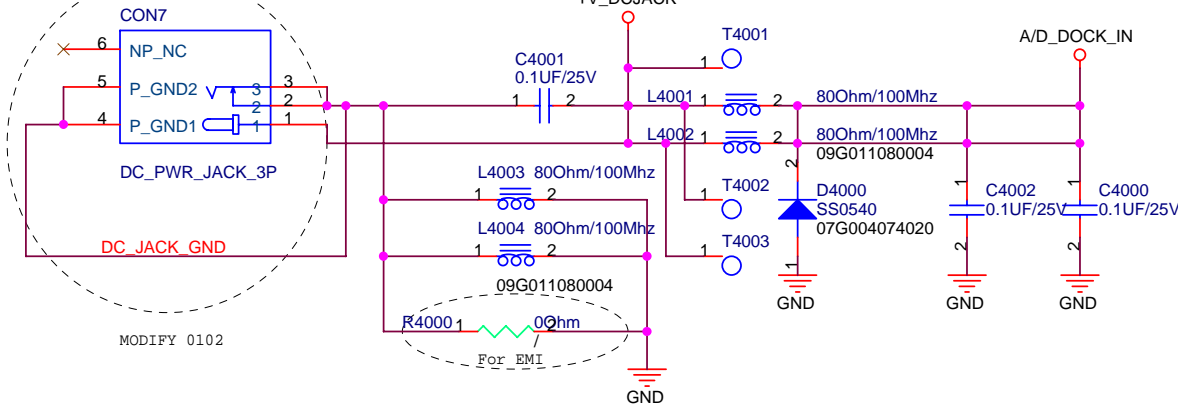
ASUS Title : **MINIPCI (802.11)**
 ASUSTeK COMPUTER INC Engineer: **Jack Wang**

Size	Project Name	Rev
A4	A6F	1.0

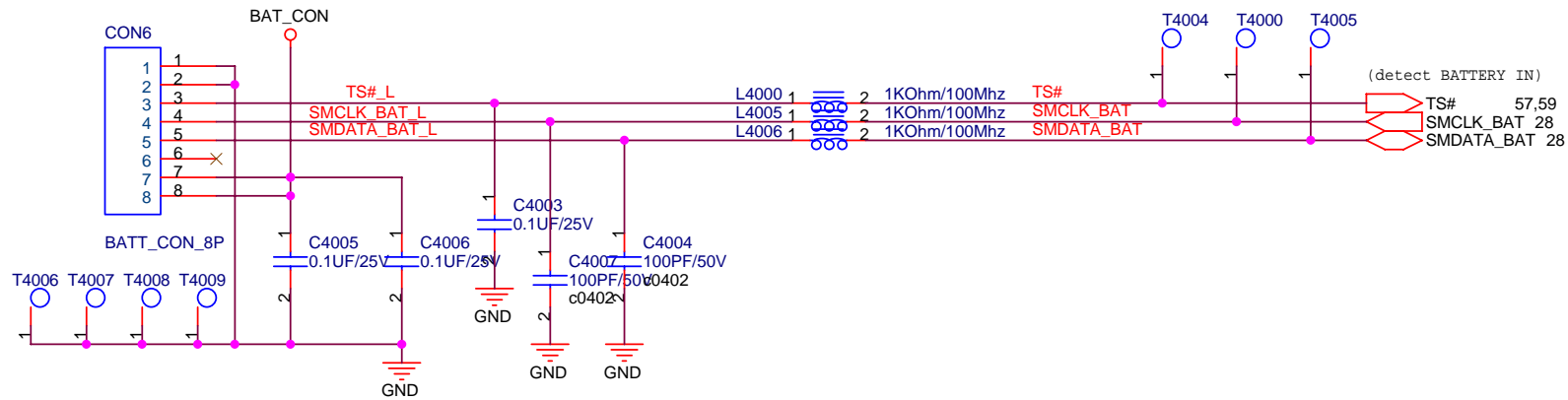
Date: **Monday, March 06, 2006** Sheet **38** of **63**



DC Power Jack



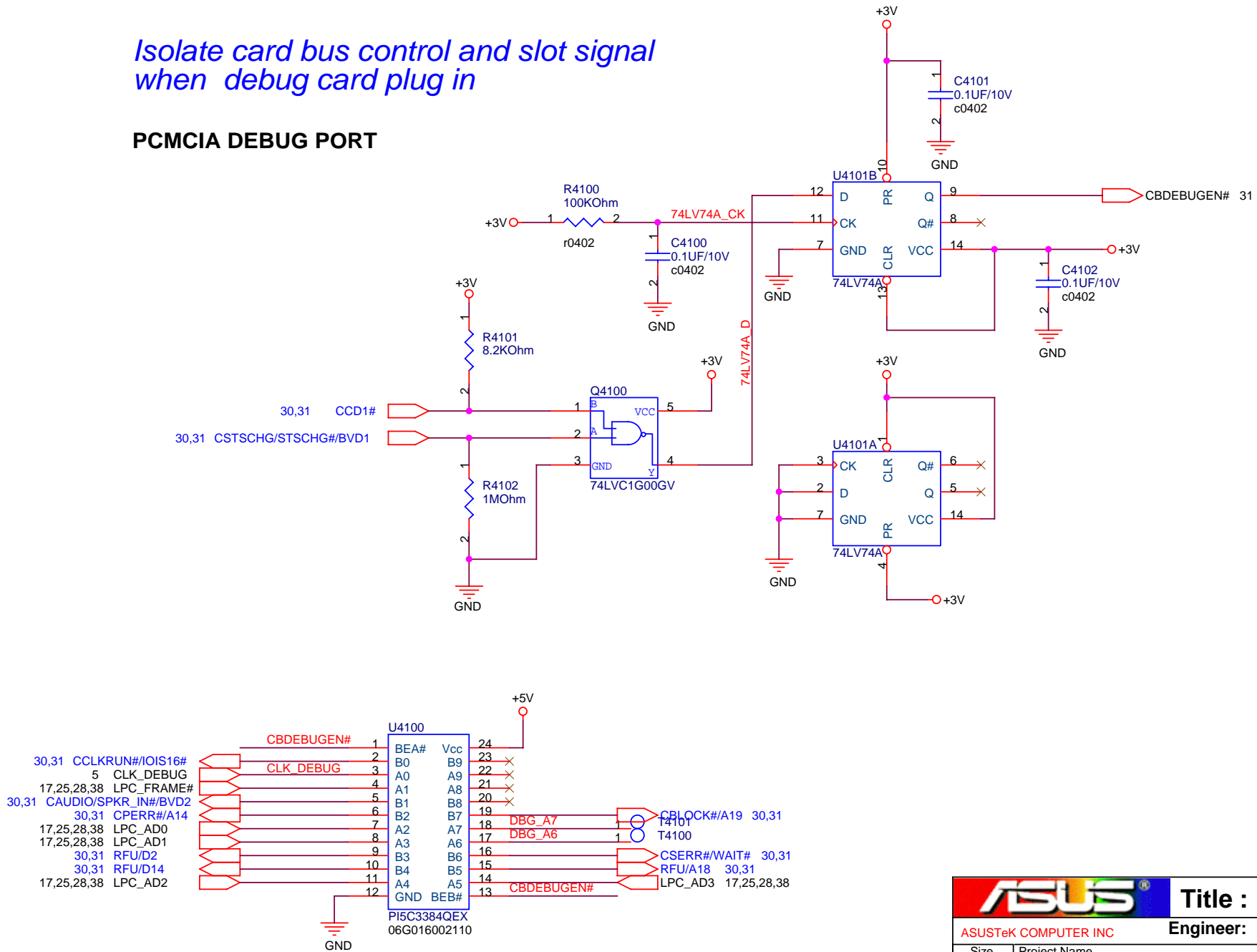
MODIFY 0102



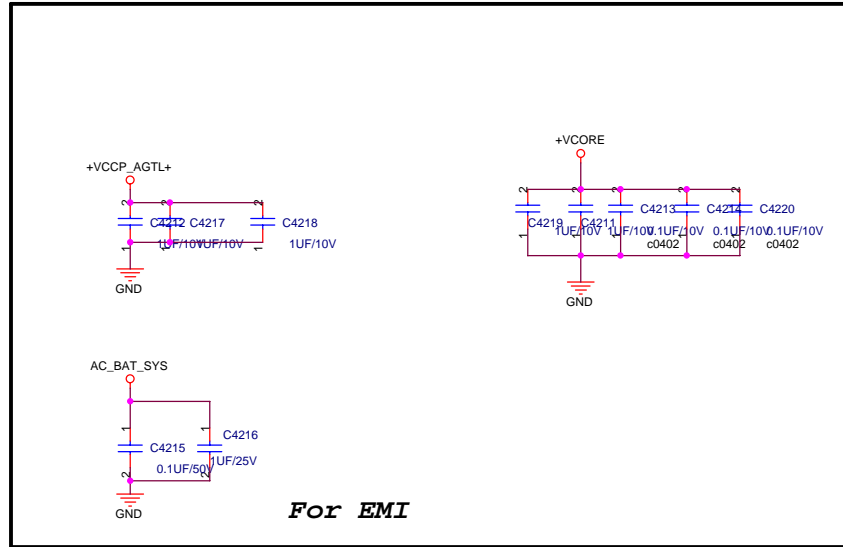
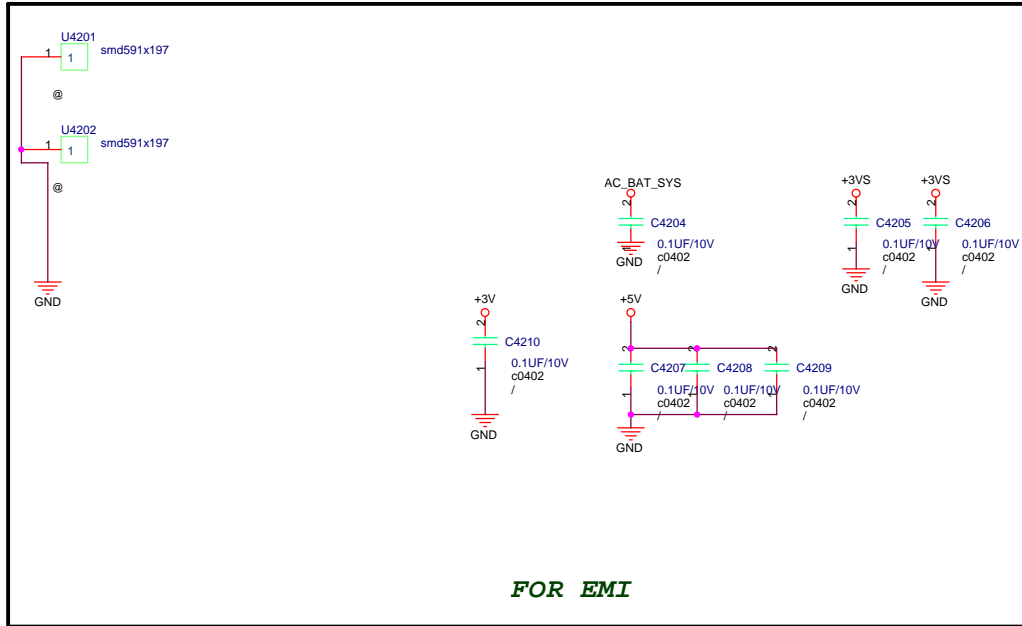
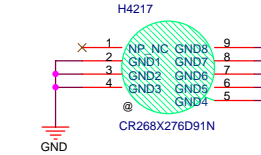
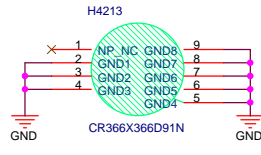
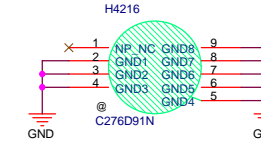
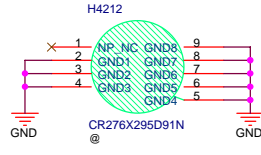
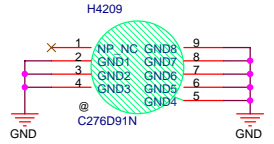
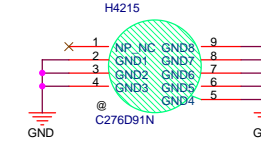
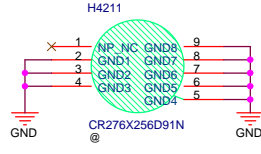
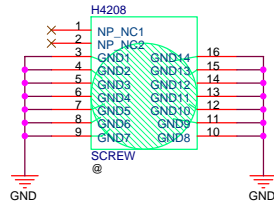
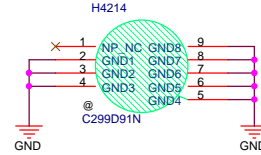
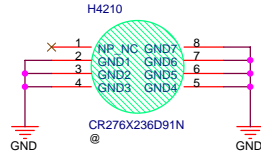
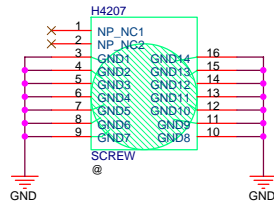
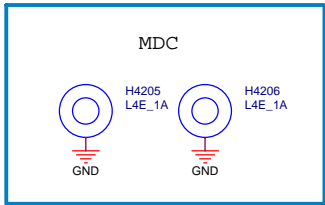
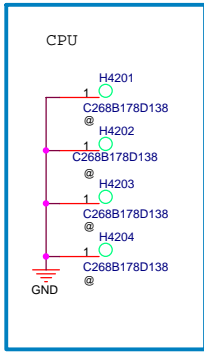
		Title : DC/ BATT IN	
ASUSTeK COMPUTER INC		Engineer: Jack Wang	
Size A4	Project Name A6F	Rev 1.0	
Date: Monday, March 06, 2006		Sheet 40 of 63	

Isolate card bus control and slot signal when debug card plug in

PCMCIA DEBUG PORT



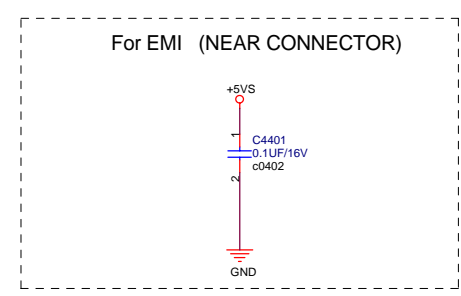
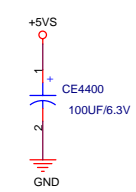
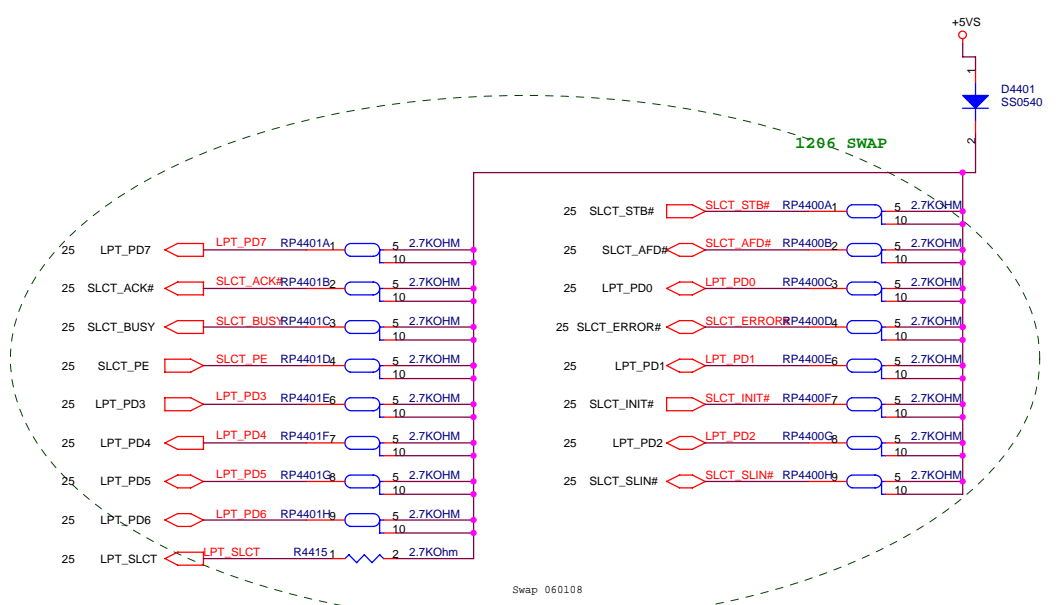
ASUS		Title : PCMCIA Debug	
ASUSTeK COMPUTER INC		Engineer: Jack Wang	
Size	Project Name		Rev
A4	A6F		1.0
Date: Monday, March 06, 2006		Sheet	41 of 63



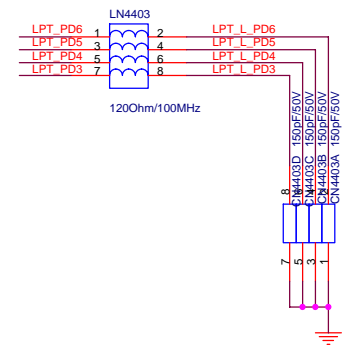
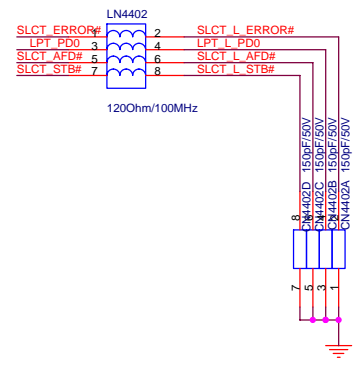
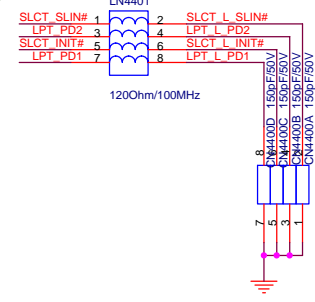
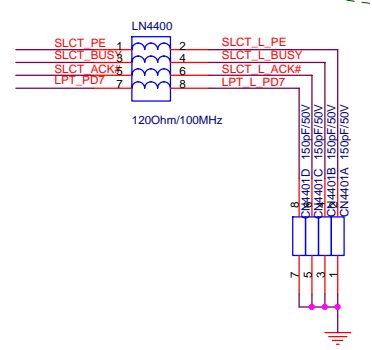
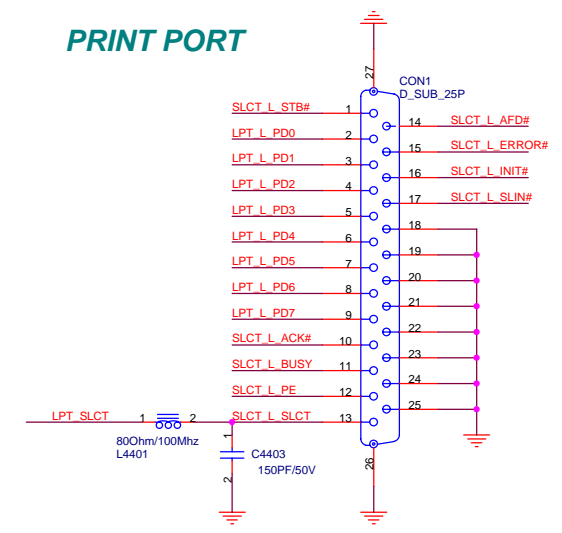
R1.1

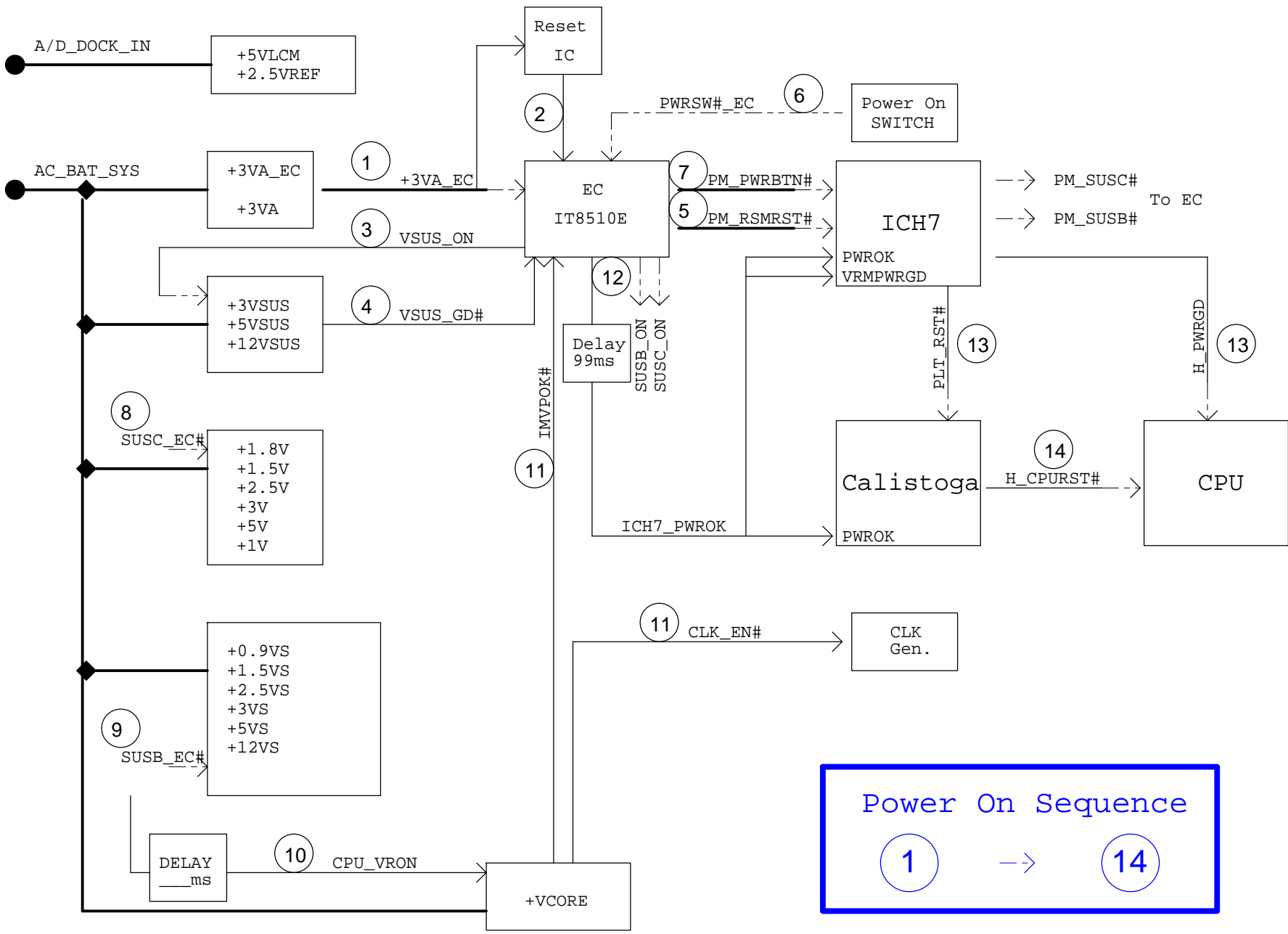
- 11/14
1. Change resistor number from R1 to R1401
 2. Change R1704 value from 10K to 330K
 3. Add U2202 C D E F
 4. Change C2511 value from 0.1uF to 0.047uF(11G232147316360)
 5. Change C2510, C2514 and C2515 value from 0.1uF to 0.33uF(11G232333436030)
- 11/29
1. Remove R409
 2. USB port (J3500) power control on shutdown of AC mode
 3. Change U2202 power source form "+3VS" to "+3V" to solve pop noise
 4. Add D2202 1N 4148W P/N 07G001001612 to solve pop noise when power off
 5. Remove R2201 and mount R2203 to change Gain Setting
- 12/1
1. Change component D2103 DAP202K to 1N4148W P/N 07G001001612
 2. Add Components 10K Ohm & 1N4148W P/N 07G001001612 and connect U2100 pin 30
 3. Change J1500,U900,U2502,U3400,H4225,H4226,H4228,H4229,H4230 ,H4223,H4231,Q4400 to green part
- 12/2
1. Change Thermal Sensor to SO-8 MAX6657
 2. USB4-->Camera, USB6-->PB
- 12/5
- 1.Change material CE1200, F3500, F3501, F3502
 2. Add EC new function-->THRO_CPU
 3. Change X3100, C3118, C3119 J3401 part number
- 12/7
- 1.Change J2500 footprint
- 12/9
- 1.Change R1202 value

		Title : HISTORY	
ASUSTeK COMPUTER INC		Engineer: <i>Jack Wang</i>	
Size	Project Name	Rev	
Custom	A6F	1.0	
Date: <i>Monday, March 06, 2006</i>		Sheet	43 of 63



PRINT PORT





Power On Sequence


① → ⑭

PCI Device	IDSEL#	REQ/GNT#	Interrupts
10/100 RTL8100CL	AD23	2	A
CARD READER	AD17	1	D
CARDBUS	AD17	1	B
1394	AD17	1	C
MINIPCI (802.11a/b/g)	AD19	3	E,F

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	1001100x (98)

ICH7-M GPIO	A3F	Note	Volt
GPIO08	EXTSMI#		+3VSUS
GPIO09	SATA_DET#0		+3VSUS
GPIO12	KBCSCI#		+3VSUS
GPIO13	SIO_SM1#		+3VSUS
GPIO14	PWRLED_1Hz		+3VSUS
GPIO15	802_LED_EN#		+3VSUS
GPIO25	CB_SD#		+3VSUS
GPIO27	WLAN_ON#		+3VSUS
GPIO28	BT_ON		+3VSUS
GPIO36	BT_LED_EN#		+3VS
GPIO37	PCB_ID0		+3VS
GPIO38	PCB_ID1		+3VS
GPIO39	PCB_ID2		+3VS

	5	4	3	2	1
D					
C					
B					
A					
	5	4	3	2	1

		Title : N/A	
ASUSTeK COMPUTER INC		Engineer: Jack Wang	
Size	Project Name	Rev	
Custom	A6F	1.0	
Date: Monday, March 06, 2006		Sheet 1 of 63	

5

4

3

2

1

D

D

C


C

B

B

A

A

		Title : N/A	
ASUSTeK COMPUTER INC		Engineer: Jack Wang	
Size	Project Name	Rev	
C	A6F	1.0	
Date: Monday, March 06, 2006		Sheet 49 of 63	

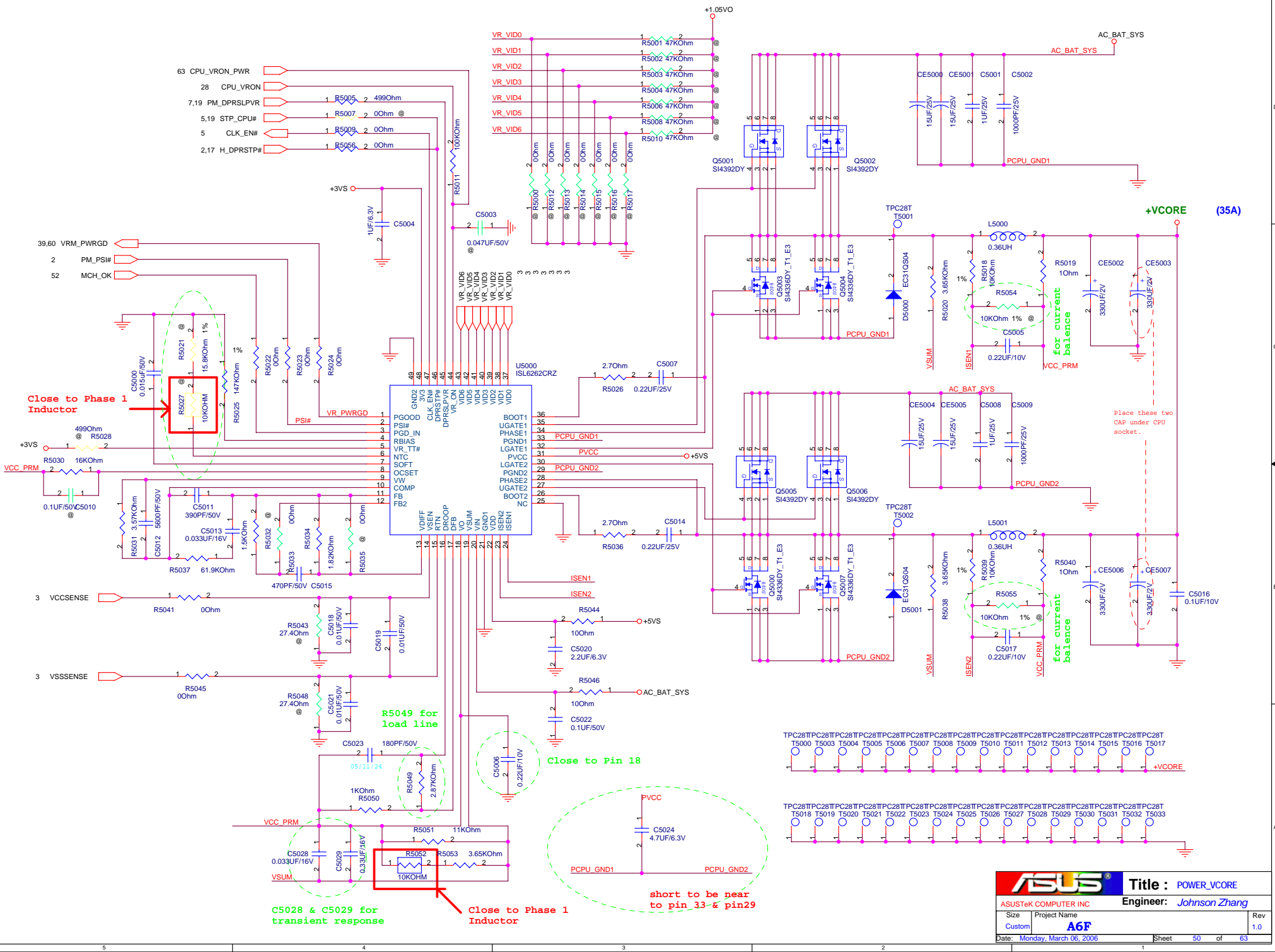
5

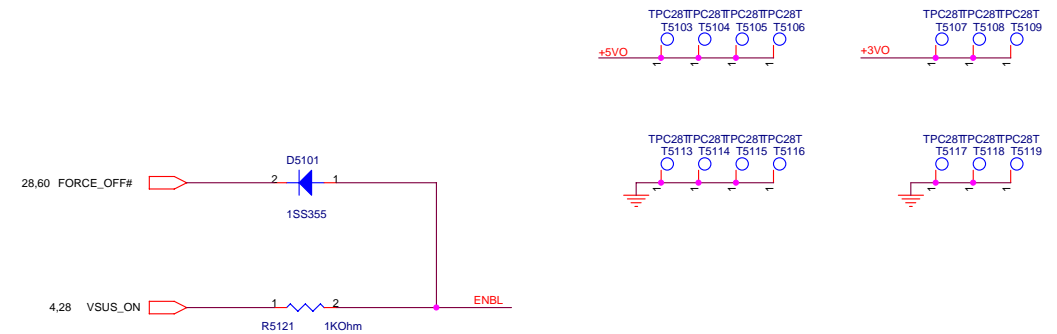
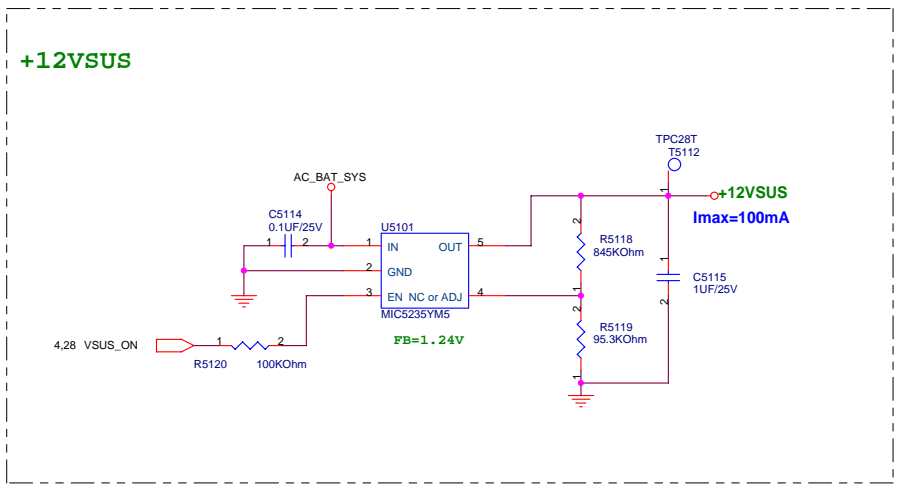
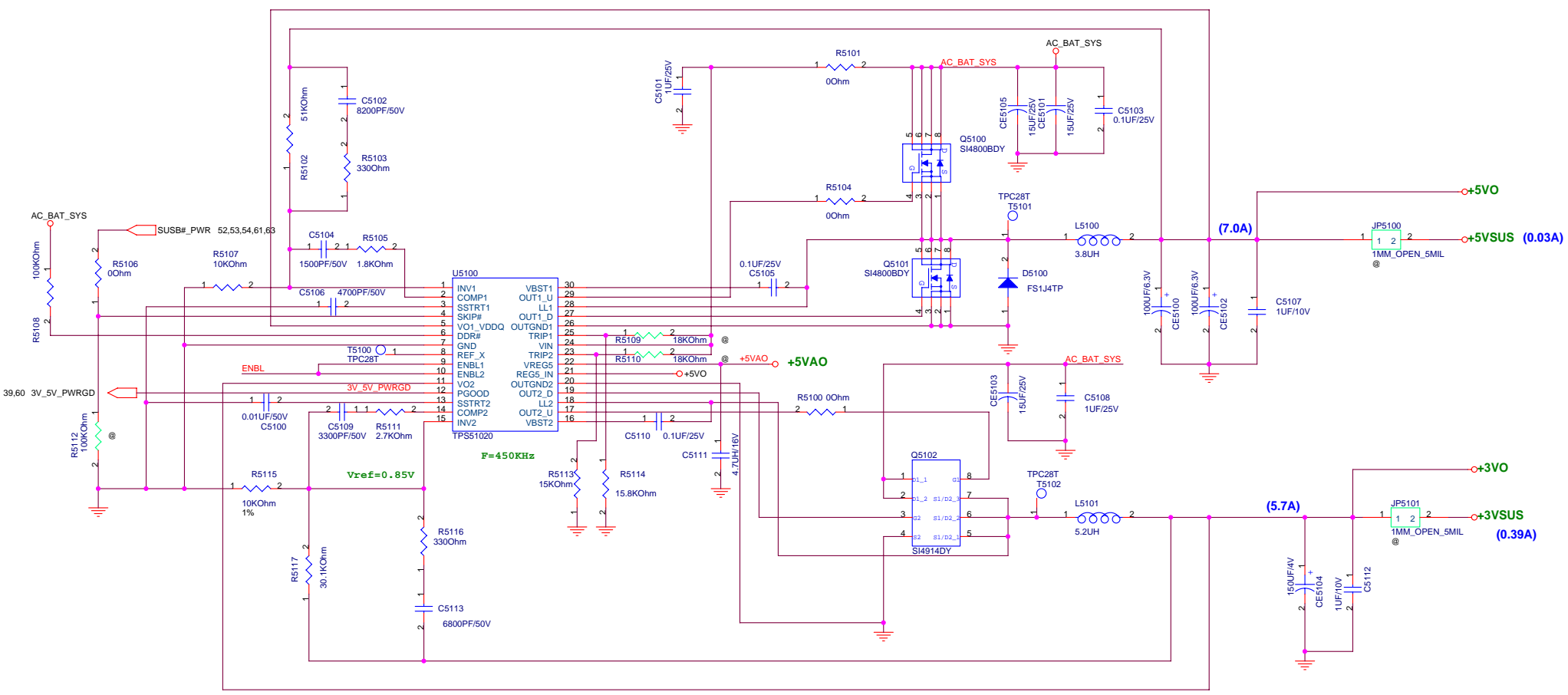
4

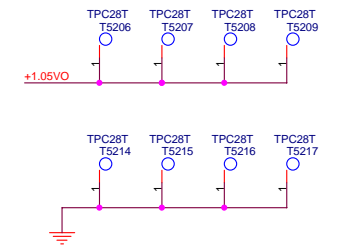
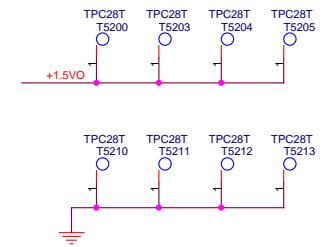
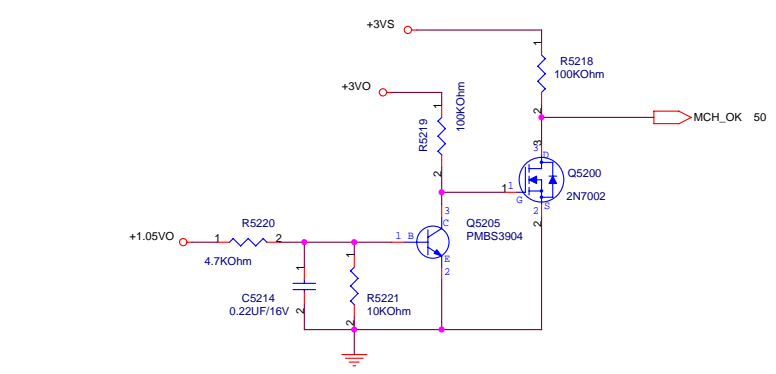
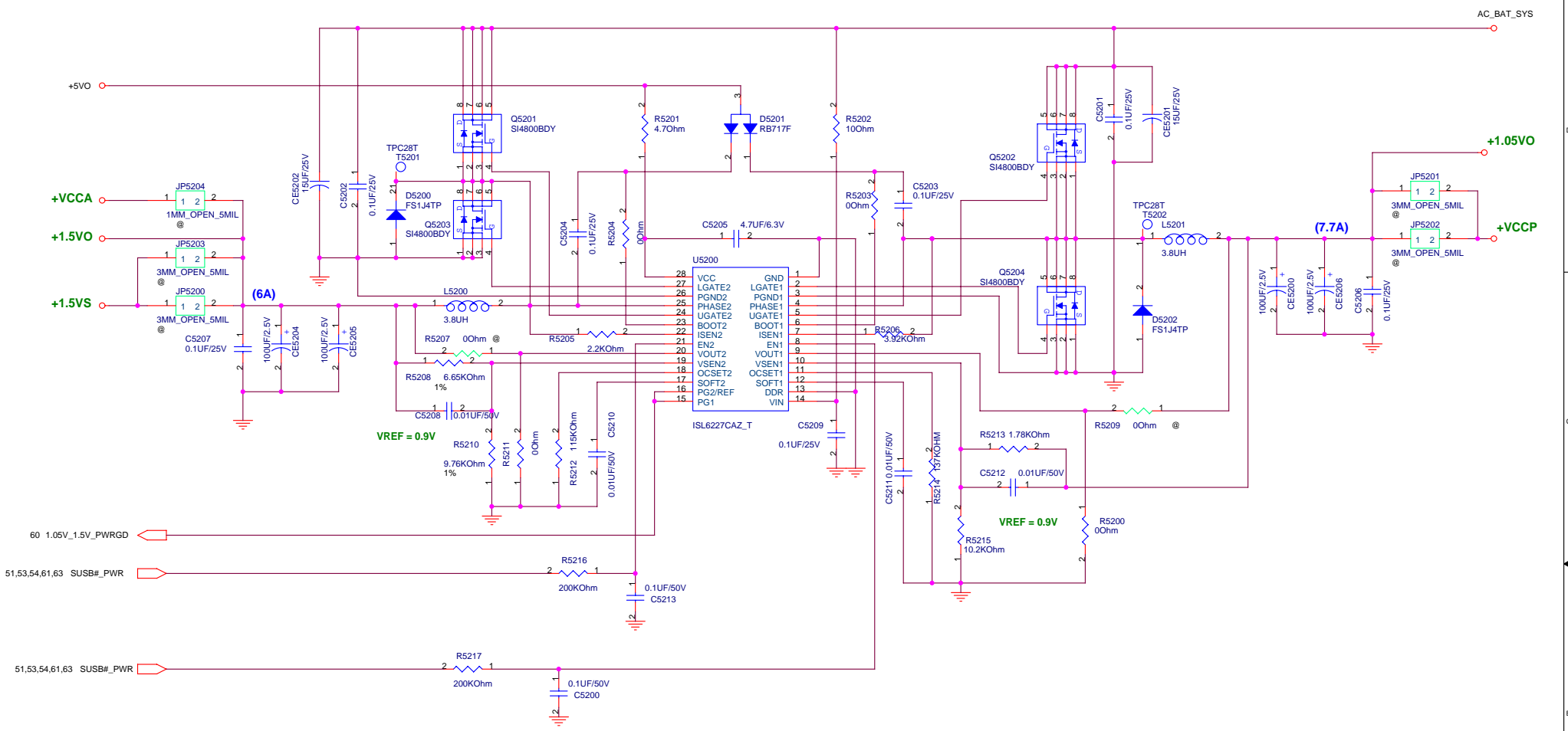
3

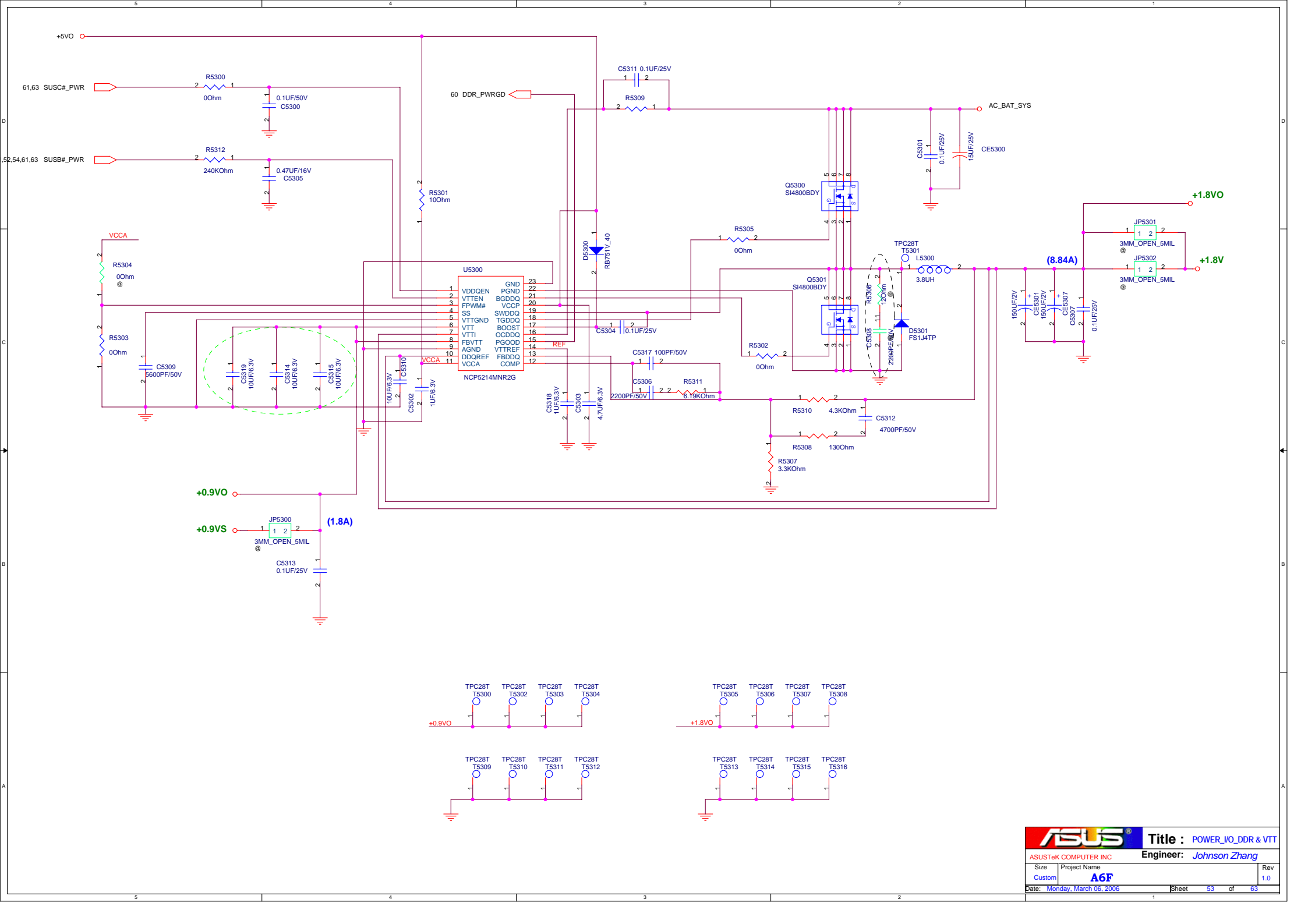
2

1

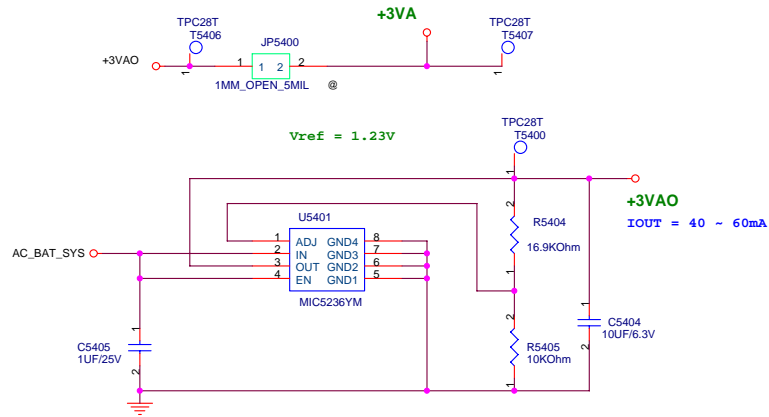




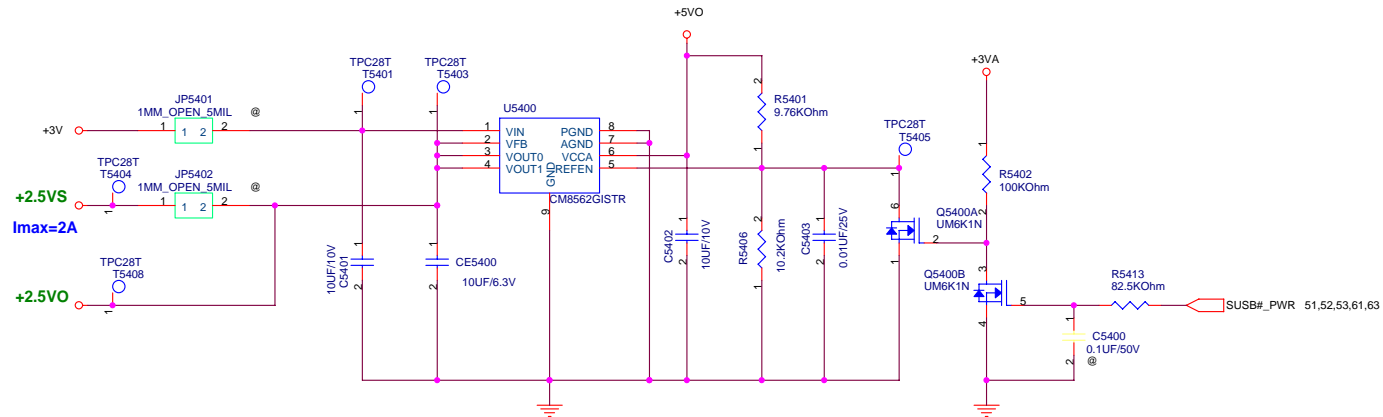




+3VAO



+2.5VS



5

4

3

2

1

D

D

C

C

B

B

A

A

		Title : Dummy	
ASUSTek COMPUTER INC		Engineer: Johnson Zhang	
Size	Project Name		Rev
C	A6F		1.0
Date: Monday, March 06, 2006		Sheet	55 of 63

5

4

3

2

1

5

4

3

2

1

D

D

C


C

B

B

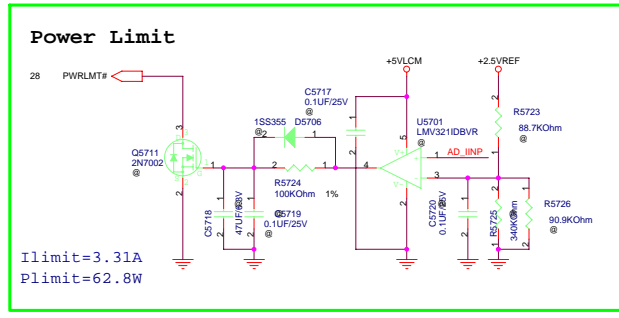
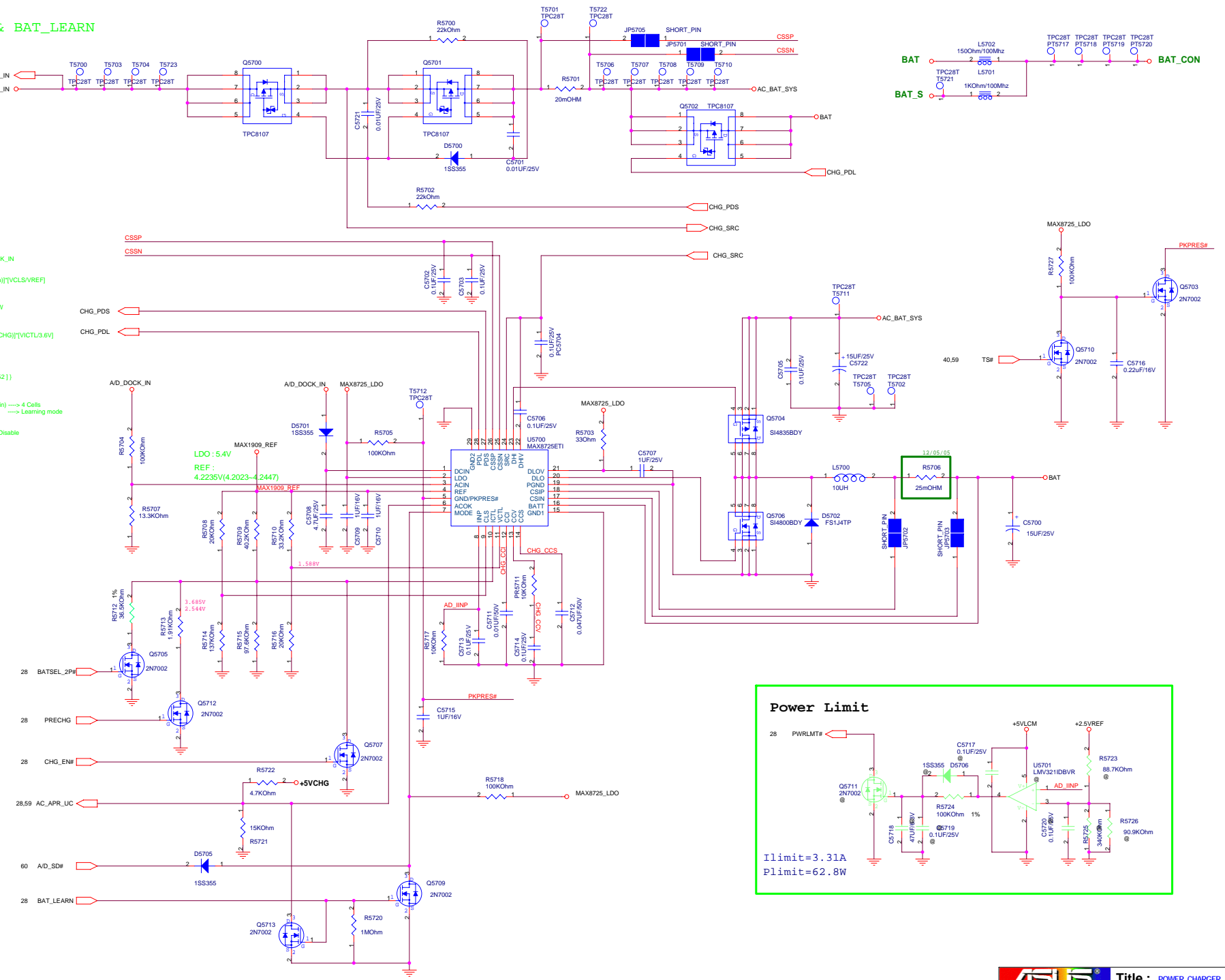
A

A

		Title : Dummy	
ASUSTeK COMPUTER INC		Engineer: Johnson Zhang	
Size	Project Name		Rev
C	A6F		1.0
Date: Monday, March 06, 2006		Sheet	56 of 63

POWER PATH & BAT_LEARN

\otimes AC_IN Threshold $2.048V_{max} A/D_DOCK_IN > 17.44V$ active
 Adapter $I_{in(max)} = [0.075V/R_{sense(Adin)}] \cdot [V_{CLS}/V_{REF}]$
 $R_{sense(Adin)} = 0.02 \text{ ohm}$
 $V_{CLS} = 3.685V$
 $\Rightarrow I_{in(max)} = 3.27A$
 $\Rightarrow \text{Constant Power} = 19 \cdot 3.27 = 62.13W$
 $\Rightarrow R_{5708-20K}, R_{5714} = 137K$
 Charge Current $I_{chg} = [0.075V/R_{sense(CHG)}] \cdot [V_{ICTL3.6V}]$
 $R_{sense(CHG)} = 0.025 \text{ ohm}$
 $V_{ICTL} = 3V \Rightarrow I_{chg} = 2.5A$
 $V_{ICTL} = 1.68V \Rightarrow I_{chg} = 1.4A$
 $V_{batt} = \text{Cell} \cdot (V_{ref} + (V_{CTL} - 1.8V) / 9.52)$
 $V_{CTL} = 1.588V \Rightarrow V_{batt} = 4.2V$
 Mode pin : $V_{mode} > 2.8V$ (tie to LDO pin) \rightarrow 4 Cells
 $0.8 > V_{mode}$ (tie to GND) \rightarrow Learning mode
 $V_{ICTL} < 0.8V$ or $DCIN < 7V \rightarrow$ Charger Disable
 Precharge current = 150mA



5

4

3

2

1

D

D

C

C

B

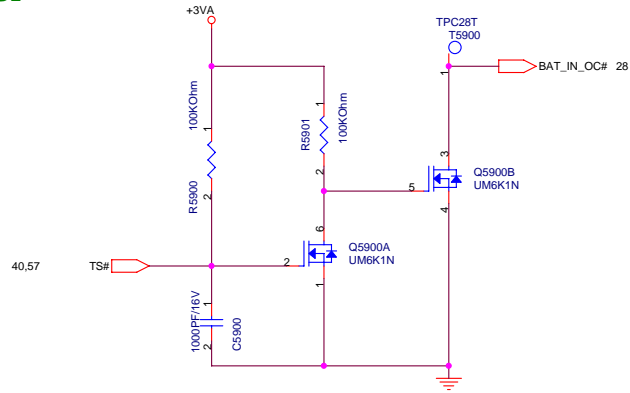
B

A

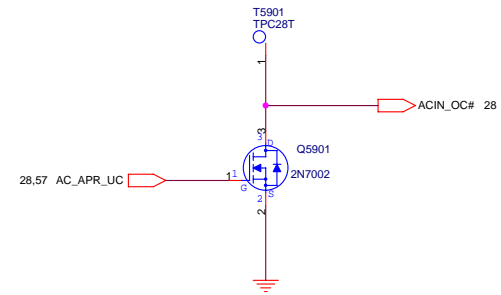
A

		Title : Dummy	
ASUSTek COMPUTER INC		Engineer: Johnson Zhang	
Size	Project Name		Rev
C	A6F		1.0
Date: Monday, March 06, 2006		Sheet	58 of 63

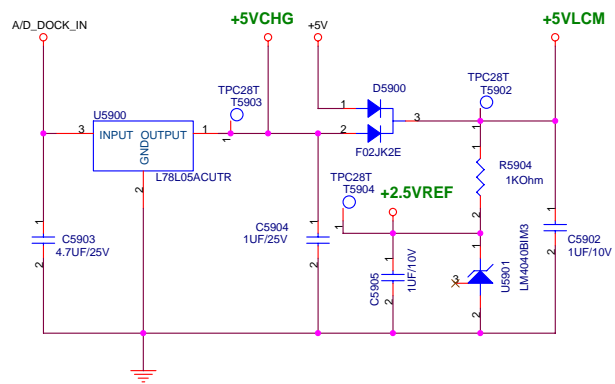
BATTERY IN DETECT



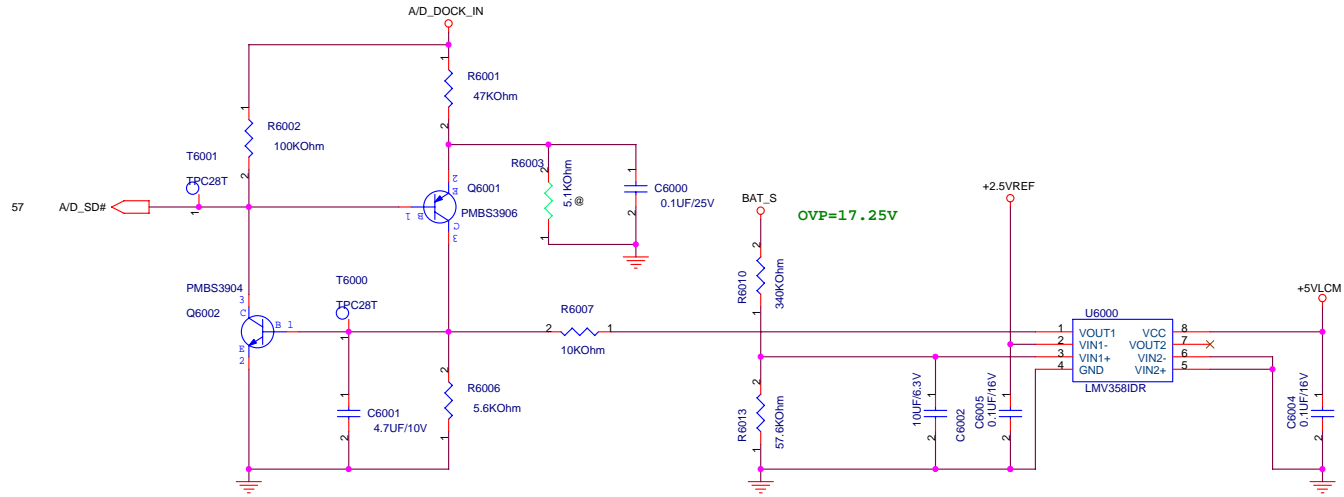
ADAPTER IN DETECT



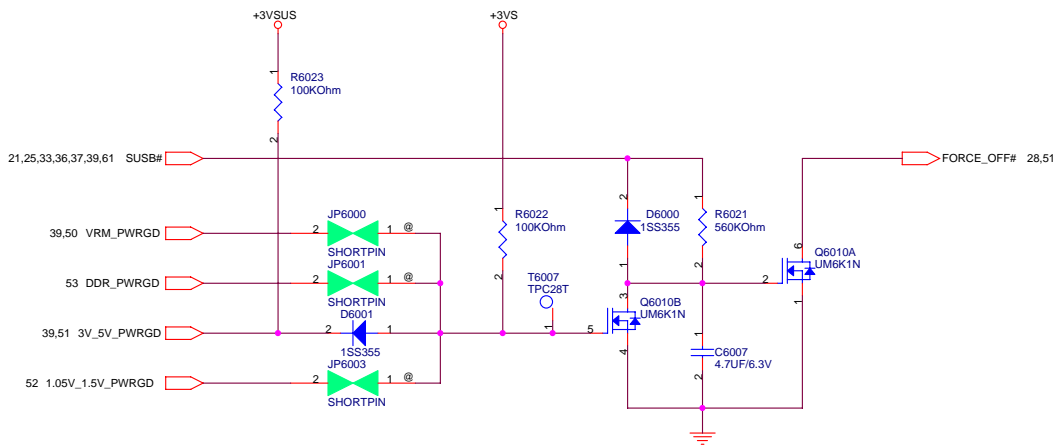
+5VLCM, +5VCHG & +2.5VREF



BATTERY A/D_SD# (OVP)

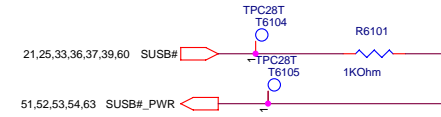
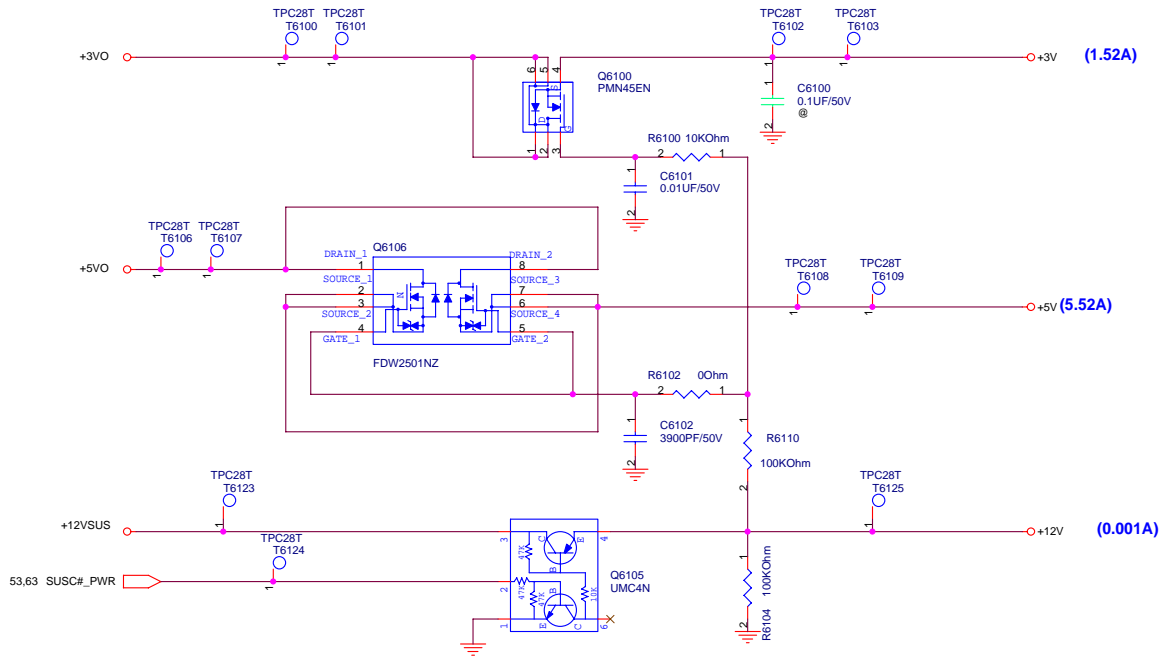


POWER GOOD DETECTOR

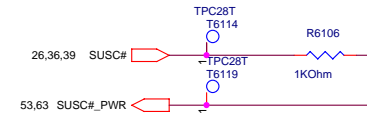
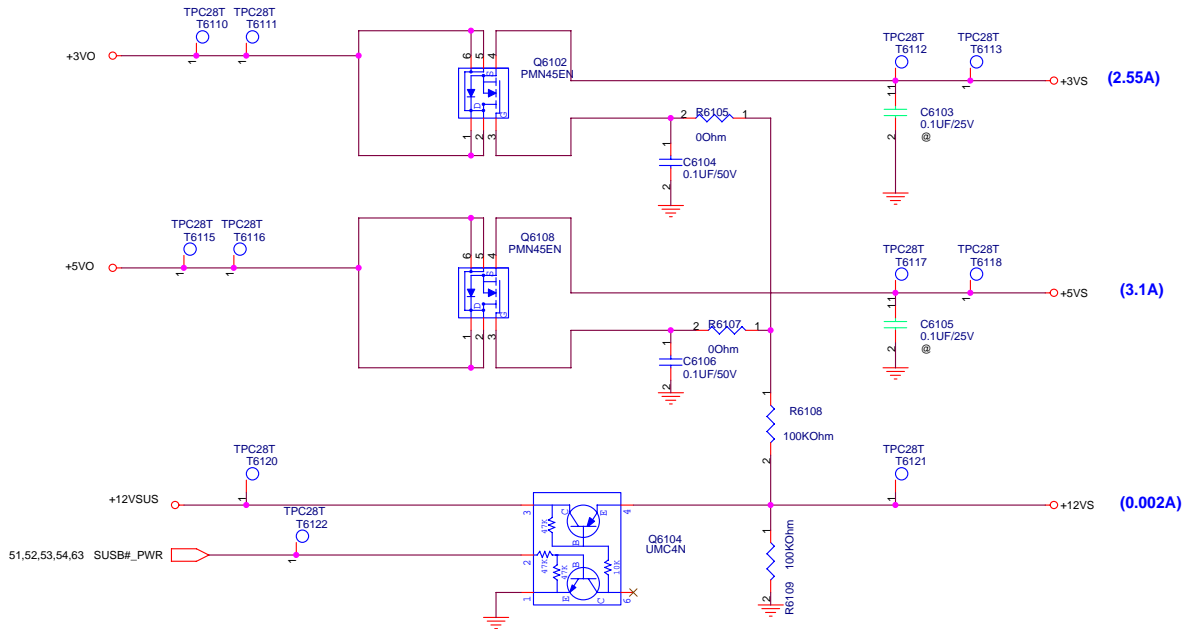


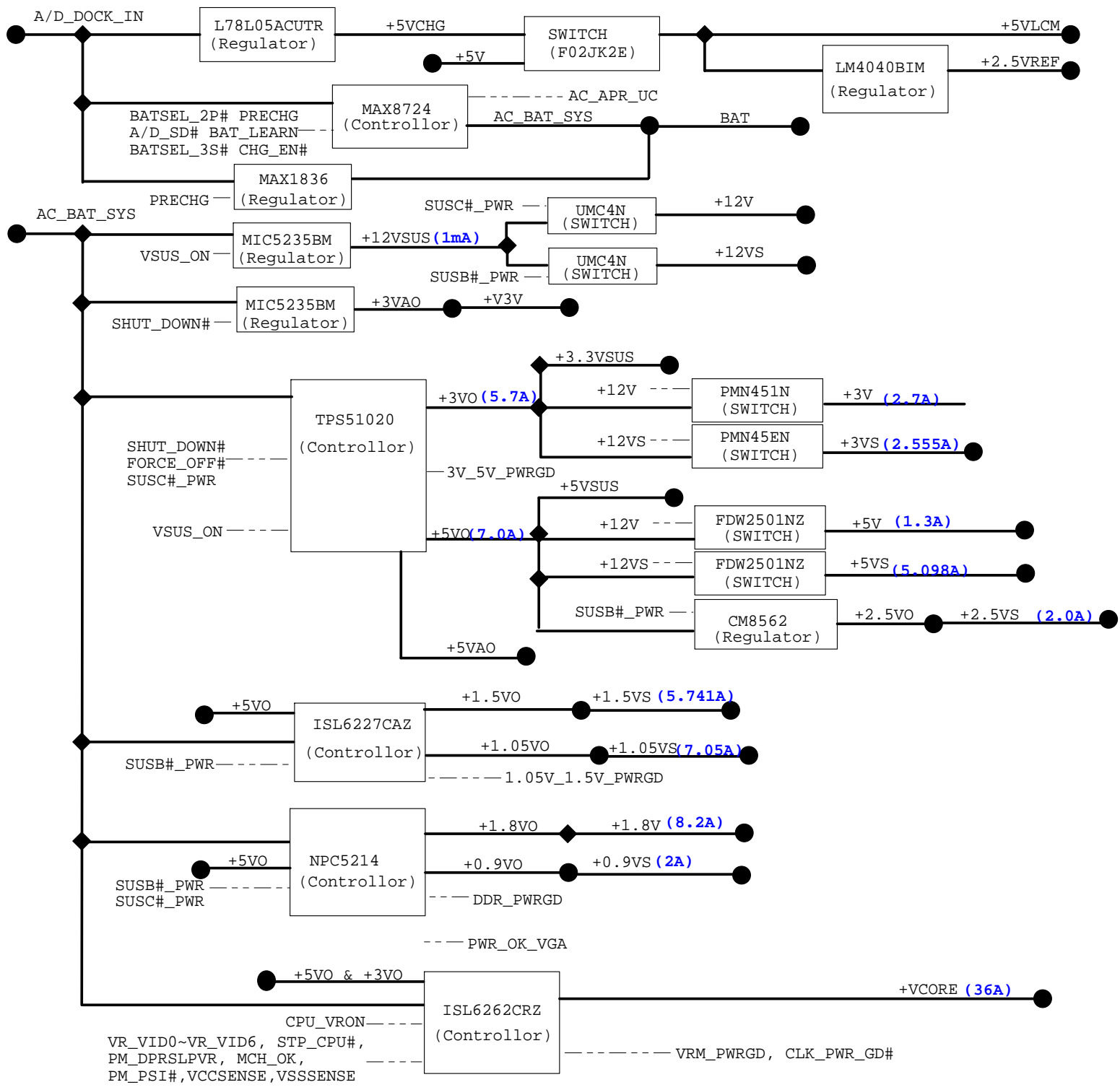
TPC28T	T6003	VRM_PWRGD
TPC28T	T6004	DDR_PWRGD
TPC28T	T6005	3V_5V_PWRGD
TPC28T	T6006	1.05V_1.5V_PWRGD

SUSC#_PWR POWER



SUSB#_PWR POWER







FOR POWER TEST

