F9S SCHEMATIC Revision 1.3

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9	NB_-965PM--DDR2/PEG (2)
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31	EMPTY
32	EMPTY
33	NEWCARD
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38	Instant Key & Touch Pad
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41	NB8M-SE--FB (2)
42	NB8M-SE--VRAM (3)
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	91_POWER_LOAD SWITCH
	92_POWER_PROTECT
	93_POWER_SIGNAL
	94_POWER_FLOWCHART

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<Variant Name>

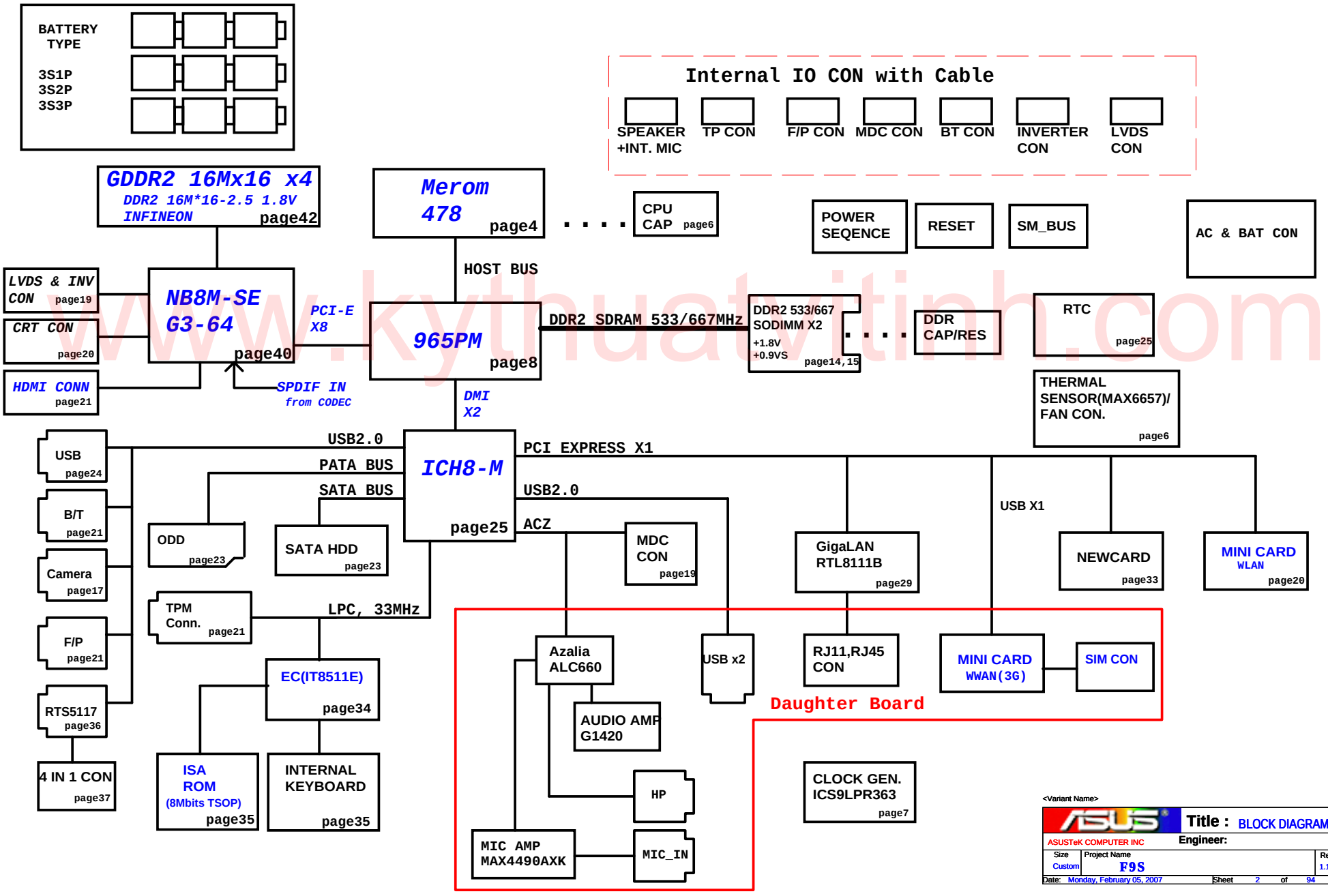
Title : PAGE REF.

ASUSTeK COMPUTER INC Engineer:

Size	Project Name	Rev
Custom	F9S	1.1

Date: Thursday, February 15, 2007 Sheet 1 of 94

F9S BLOCK DIAGRAM



<Variant Name>

ASUSTeK COMPUTER INC

Title : BLOCK DIAGRAM

Engineer:

Size	Project Name	Rev
Custom	F9S	1.1

Date: Monday, February 05, 2007 Sheet 2 of 94

EC-IT8511 GPIO SETTING

Pin	Pin Name	Signal Name	Type
32	PWM0/GPA0	LCD_BL_PWM	
33	PWM1/GPA1	FAN_PWM	
36	PWM2/GPA2	BAT1_CNT1#	I
37	PWM3/GPA3	BAT2_CNT1#	
38	PWM4/GPA4	CHG_LED_UP#	O
39	PWM5/GPA5	PWR_LED_UP#	O
40	PWM6/GPA6	BATSEL_3S#	O
43	PWM7/GPA7	LCD_BACKOFF#	O
153	RXD/GPB0	NUM_LED	O
154	TXD/GPB1	CAP_LED	O
162	GPB2	SCRL_LED	O
163	SMCLK0/GPB3	SMB0_CLK	O
164	SMDAT0GPB4	SMB0_DAT	I/0
5	GA20/GPB5	A20GATE	O
6	KBRST#/GPB6	RCIN#	O
165	GPB7	THRO_CPU	O
47	CLKOUT/GPC0	N/A	
169	SMCLK1/GPC1	SMB1_CLK	O
170	SMDAT1/GPC2	SMB1_DAT	I/0
171	GPC3	PWRLIMIT#	O
172	TMRI0/WUI2/GPC4	ACIN_OC#	I
175	GPC5	OP_SD#	O
176	TMRI1/WUI3/GPC6	BAT_IN_OC#	I
1	CK32KOUT/GPC7	EC_IDE_RST#	O
26	RI1#/WUI0/GPD0	SUSB#	I
29	RI2#/WUI1/GPD1	SUSC#	I
30	LPCRST#/WUI4//GPD2	BUF_PLT_RST#	I
31	ECSCI#/GPD3	EXT_SCI#	O
41	GPD4	RF_ON_SW#	O
42	GINT/GPD5	PM_SLP_M#	O
62	TACH0/GPD6	FAN0_TACH	
63	TACH1/GPD7	COLOREN#	I
87	ADC4/GPE0	BLUETOOTH#	I
88	ADC5/GPE1	INTERNET#	I
89	ADC6/GPE2	MARATHON#	I
90	ADC7/GPE3	DISTP#	I
2	PWRSW/GPE4	PWR_SW#	I
44	WUI5/GPE5	BAT2_IN_OC#	I
24	LPCPD#/WUI6/GPE6	WLAN_SW#	I
25	CLKRUN#/WUI7/GPE7	ME_ALERT#	
110	PS2CLK0/GPF0	NC/PS2CLK0	O
111	PS2DAT0/GPF1	NC/PS2DAT0	I/0
114	PS2CLK1/GPF2	DVD/CD_ON#	I
115	PS2DAT1/GPF3	TV_ON#	I
116	PS2CLK2/GPF4	TP_CLK	O
117	PS2DAT2/GPF5	TP_DAT	I/0
118	PS2CLK3/GPF6	SLOT_ON# ??	I
119	PS2DAT3/GPF7	INSTANT_ON#	I
113	FA16/GPG0	FA16_SWAP	O
112	FA17/GPG1	FA17	O
104	FA18/GPG2	FA18	O
103	FA19/GPG3	FA19 BAT2_IN_OC#	O
3	FA20/GPG4	LID_EC#	I
4	FA21/GPG5	BAT2_IN_OC#	I
27	LPC80HL/GPG6	PMTHERM#	O
28	LPC80LL/GPG7	AC_APR_UC#	I

Pin	Pin Name	Signal Name	Type
48	GPH0	VSUS_ON	O
54	GPH1	VSUS_GD	I
55	GPH2	CPUPWR_GD	I
69	GPH3	PM_PWRBTN#	O
70	GPH4	SUSC_EC#	O
75	GPH5	SUSB_EC0#	O
76	GPH6	CPU_VRON	O
105	GPH7	PM_RSMRST#	O
148	GPI0	ICH8_PWROK	O
149	GPI1	ALL_SYS_PWRGD	I
152	GPI2	BAT1_CNT2#	O
155	GPI3	CHG_EN#	O
156	GPI4	PRECHG	O
168	GPI5	EC_CLK_EN	O
174	GPI6	BAT_LEARN	O

SM_BUS ADDRESS :

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor(MAX6657)	1001100x (98)
VGA Thermal IC(G781-1)	1001101x (9A)

ICH8M_GPIO

Pin.	Default	RST#	Use As	Signal Name	Power	Mux
GPIO 00	i		GPI	PM_BMBUSY#	+3VS	BM_BUSY#
GPIO 01	i	0	GPI	BT_DET#	+3VS	TACH1
GPIO [5:2]	i	H-Z	GPI	PCI_INT[H:E]#	+3VS	PIRQ[H:E]#
GPIO 06	i	0	GPO	BIOS_REC_?_(TP)	+3VS	TACH2
GPIO 07	i	0	GPO	802_LED_EN	+3VS	TACH3
GPIO 08	i		GPI	EXTSMI#	+3VSUS	N/A
GPIO 09	i	H-Z	GPO	LAN_WOL_EN_?_(TP)	+3VSUS	WOL_EN
GPIO 10	i	H-Z	GPO	RST#_NEWCARD	+3VSUS	ALERT#
GPIO 11	Nat.	H-Z	Native	SMB_ALERT#	+3VSUS	SMBALERT#
GPIO 12	i		GPI	KBC_SCI#	+3VSUS	GLAN_DOCK#
GPIO 13	Nat.		GPI	N/A	+3VSUS	ENERGY_DETECT
GPIO 14	i	H-Z	GPI	N/A	+3VSUS	NETDETECT
GPIO 15	Nat.	1	Native	STP_PCI#	+3VSUS	STP_PCI# , No-GPIO, in Mobile
GPIO 16	Nat.	0	Native	PM_DPRSLPVR	+3VS	DPRSLPVR
GPIO 17	i	1	GPO	WLAN_ON#	+3VS	TACH0
GPIO 18	O	freq 1K	GPO	N/A	+3VS	N/A
GPIO 19	i		GPO	CPU_SELECT	+3VS	SATA1GP
GPIO 20	O	1	GPO	BT_LED_EN	+3VS	N/A
GPIO 21	i		GPI	CPPE#_DET	+3VS	SATA0GP
GPIO 22	i		GPI	N/A	+3VS	SCLOCK
GPIO 23	Nat.		Native	N/A	+3VS	LDRQ1#
GPIO 24	O	H-Z	GPO	MSK_PCIRST	+3VSUS	CLGPIO0(MEM_LED), Not Cleared by CF9h RST event.
GPIO 25	Nat.	1	Native	STP_CPU#	+3VS	STP_CPU# , No-GPIO, in Mobile
GPIO 26	Nat.		GPO	CPPE_EN	+3VSUS	S4_STATE#
GPIO 27	O	0	GPO	BT_ON#	+3VSUS	QRT_STATE0
GPIO 28	O	0	GPO	CB_SD#_?_(TP)	+3VSUS	QRT_STATE1
GPIO 29	Nat.		Native	USB_OC#5	+3VSUS	OC5#
GPIO 30	Nat.		Native	USB_OC#6	+3VSUS	OC6#
GPIO 31	Nat.		Native	USB_OC#7	+3VSUS	OC7#
GPIO 32	O	0	Native	PM_CLKRUN#	+3VS	CLKRUN# , No-GPIO, in Mobile
GPIO 33	O	1	GPO	N/A	+3VS	HDA_DOCK_EN#
GPIO 34	O	0	GPO	N/A	+3VS	HDA_DOCK_RST#
GPIO 35	O	0	GPO	SATACLKREQ#_?_(TP)	+3VS	SATACLKREQ#
GPIO 36	i		GPO	EMAIL_LED#_?_(TP)	+3VS	SATA2GP
GPIO 37	i	0	GPI	PCB_ID0	+3VS	SATA3GP
GPIO 38	i		GPI	PCB_ID1	+3VS	SLOAD

Pin	Default	RST#	Use As	Signal Name	Power	Mux
GPIO 39	i		GPI	PCB_ID2	+3VS	SDATAOUT0
GPIO [40:43]	Nat.		Native	USB_OC[4:1]#	+3VSUS	OC[4:1]#
GPIO [47:44]	n/a		N/A	N/A	N/A	No implement
GPIO 48	i	1	Native		+3VS	SDATAOUT1
GPIO 49	Nat.		Native	H_PWRGD	+VCORE	CPUPWRGD
GPIO 50	Nat.		Native	PCI_REQ1#	+5VS	REQ1#
GPIO 51	Nat.	1	Native	PCI_GNT1#	+3VS	GNT1#
GPIO 52	Nat.		Native	PCI_REQ2#	+5VS	REQ2#
GPIO 53	Nat.	1	Native	PCI_GNT2#	+3VS	GNT2#
GPIO 54	Nat.		Native	PCI_REQ3#	+5VS	REQ3#
GPIO 55	Nat.	1	Native	PCI_GNT3#	+3VS	GNT3#

<Variant Name>

Title : Schematic Info.

ASUSTeK COMPUTER INC Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom	F9S	1.1

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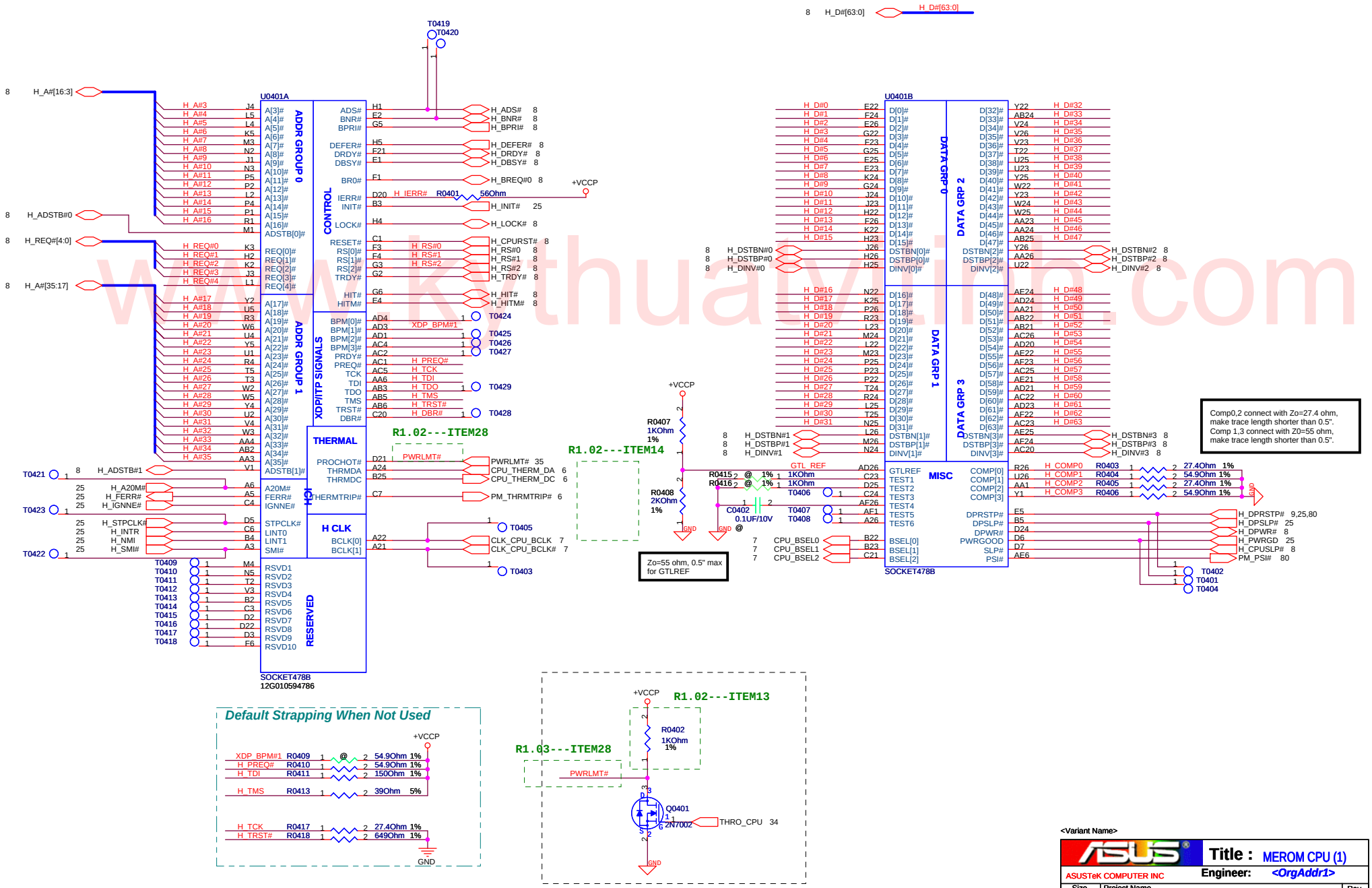
U0401A
ADDR GROUP 0
ADDR GROUP 1
CONTROL
XDP/ITP SIGNALS
THERMAL
H CLK
RESERVED
SOCKET478B
12G010594786
U0401B
DATA GRP 0
DATA GRP 1
DATA GRP 2
DATA GRP 3
MISC
SOCKET478B
R1.02---ITEM28
R1.02---ITEM14
R1.02---ITEM13
R1.03---ITEM28
Zo=55 ohm, 0.5" max for GTLREF
Comp0,2 connect with Zo=27.4 ohm, make trace length shorter than 0.5". Comp 1,3 connect with Z0=55 ohm, make trace length shorter than 0.5".
Default Strapping When Not Used
+VCCP
GND
H_A#[16:3]
H_A#[35:17]
H_ADSTB#0
H_ADSTB#1
H_REQ#[4:0]
H_D#[63:0]
H_DSTBN#0
H_DSTBP#0
H_DINV#0
H_DSTBN#1
H_DSTBP#1
H_DINV#1
H_DSTBN#2
H_DSTBP#2
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PWRLMT#
THRO_CPU
Q0401
2N7002
<Variant Name>
Title : MEROM CPU (1)
ASUSTeK COMPUTER INC
Engineer: <OrgAddr1>
Size: Custom
Project Name: F9S
Rev: 1.1
Date: Tuesday, February 27, 2007
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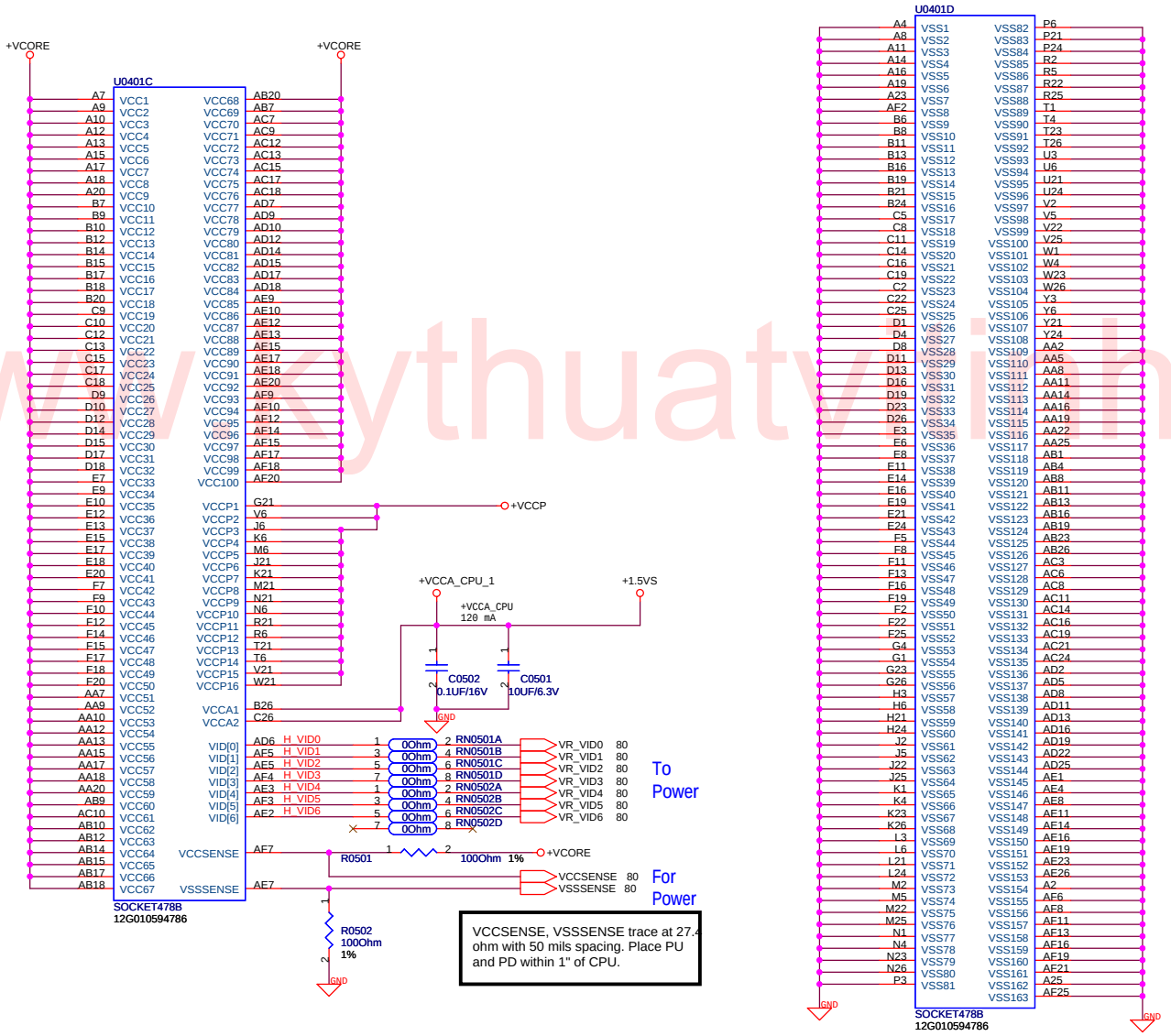


<Variant Name>

ASUSTeK COMPUTER INC

Title : MEROM CPU (2)

Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom	F9S	1.1

Date: Tuesday, February 27, 2007 Sheet 5 of 94

+VCCP 4,5,7,8,9,11,12,28,37,85
+VCORE 5,37,80
+3VS 7,9,12,13,14,15,17,18,19,20,21,22,23,25,27,28,29,33,34,37,39,40,43,44,45,80,91,92
+5VA 81

Place on L1/L8, upper/lower side of inside socket. according intel layout suggestion.

44A for Merom

+VCORE

C0614 10UF/6.3V, C0632 10UF/6.3V, C0621 10UF/6.3V, C0603 10UF/6.3V, C0625 10UF/6.3V, C0609 10UF/6.3V, C0631 10UF/6.3V, C0604 10UF/6.3V, C0622 10UF/6.3V, C0629 10UF/6.3V

C0627 10UF/6.3V, C0620 10UF/6.3V, C0626 10UF/6.3V, C0607 10UF/6.3V, C0624 10UF/6.3V, C0605 10UF/6.3V, C0623 10UF/6.3V, C0601 10UF/6.3V, C0615 10UF/6.3V, C0602 10UF/6.3V

C0616 10UF/6.3V, C0639 10UF/6.3V, C0619 10UF/6.3V, C0610 10UF/6.3V, C0613 10UF/6.3V, C0608 10UF/6.3V, C0612 10UF/6.3V, C0617 10UF/6.3V, C0628 10UF/6.3V, C0630 10UF/6.3V

C0611 10UF/6.3V, C0633 10UF/6.3V

GND

+VCCP Decoupling Capacitor (Place near CPU)

+VCCP

CE0601 150UF/4V, C0618 0.1UF/16V X7R, C0606 0.1UF/16V X7R, C0636 0.1UF/16V X7R, C0635 0.1UF/16V X7R, C0638 0.1UF/16V X7R, C0637 0.1UF/16V X7R

GND

Decoupling guide from INTEL

VCORE	22uF/10V	* 32pcs
	330uF/2V	* 6pcs
VCCP	0.1uF	* 6pcs for CPU
	150uF	* 1pcs for CPU

Optimize it !_0907

Sub-SYS=CPU CAP

R0651 0Ohm ICH_THRMTRIP# 25

+VCCP, +3VS

R0652 330, C0650 0.1U, R0654 10KOhm

Enable: Turn OFF system

To EC(Internal Pull Hi)

4 PM_THRMTRIP#

9 GMCH_THRMTRIP# R0655 0Ohm

9,23,26,40 PLT_RST#

Q0650 PMBS3904, Q0651 H2N7002

THRMTRIP# 34

To EC

Thermal Sensor

+3VS_THM

R0656 200 +3VS

C0652 0.1U

Max: 1mA

U0650 MAX6657MSA

VCC, DXP, DXN, OVERT#, SCLK, SDA, ALERT#, GND

SMB1_CLK R0658 2 4.7KOhm

SMB1_DAT R0657 2 4.7KOhm

THRM_ALERT#_CPU R0650 2 10KOhm

SMB1_CLK 34,40,45

SMB1_DAT 34,44,45

T0601

4 CPU_THERM_DA

4 CPU_THERM_DC

CPU_THERM_DA C0651 1000P CPU_THERM_DC

OS#_OC OS#_OC 34,43,45

Close to Pin A24 & A25 of CPU

Enable: Turn OFF system

Slave address: 98h

Max6657: 0.26(USD)

ADT7401ARMZ: 0.28(USD)

PWM FAN Control

+3VS

R0659 4.7KOhm

34 FAN0_TACH R0661 1.2KOhm

34 FAN_PWM R0671 @ 150Ohm FAN_PWM_CON FANSP

+5VS

CE0602 47UF/6.3V

D0601 1N4148W

P/N:12G17000004B

CON601 SIDE2, SIDE1

WtoB_CON_4P_1

C0653 100PF/50V

C0654 100PF/50V @

GND

R1.02---ITEM12

H/W Thermal Protect

+5VA

(94~98'C protect)

R0670 22.1K 1%

RT0671 100K

C0670 0.1U

U0670 NC, SUB, GND, VCC, VOUT

PST9013NR

R0662 4.7KOhm @

FORCE_OFF# 34,81,92

Enable: Turn OFF system

OPEN Collector

+3VS

R0673 10KOhm

FAN_PWM

U0671 NC7SZ32M5X_NL

C0655 0.1UF/16V c0402

FAN_PWM_CON

34,43,45 OS#_OC R0672 0Ohm Q0631 H2N7002

<Variant Name>

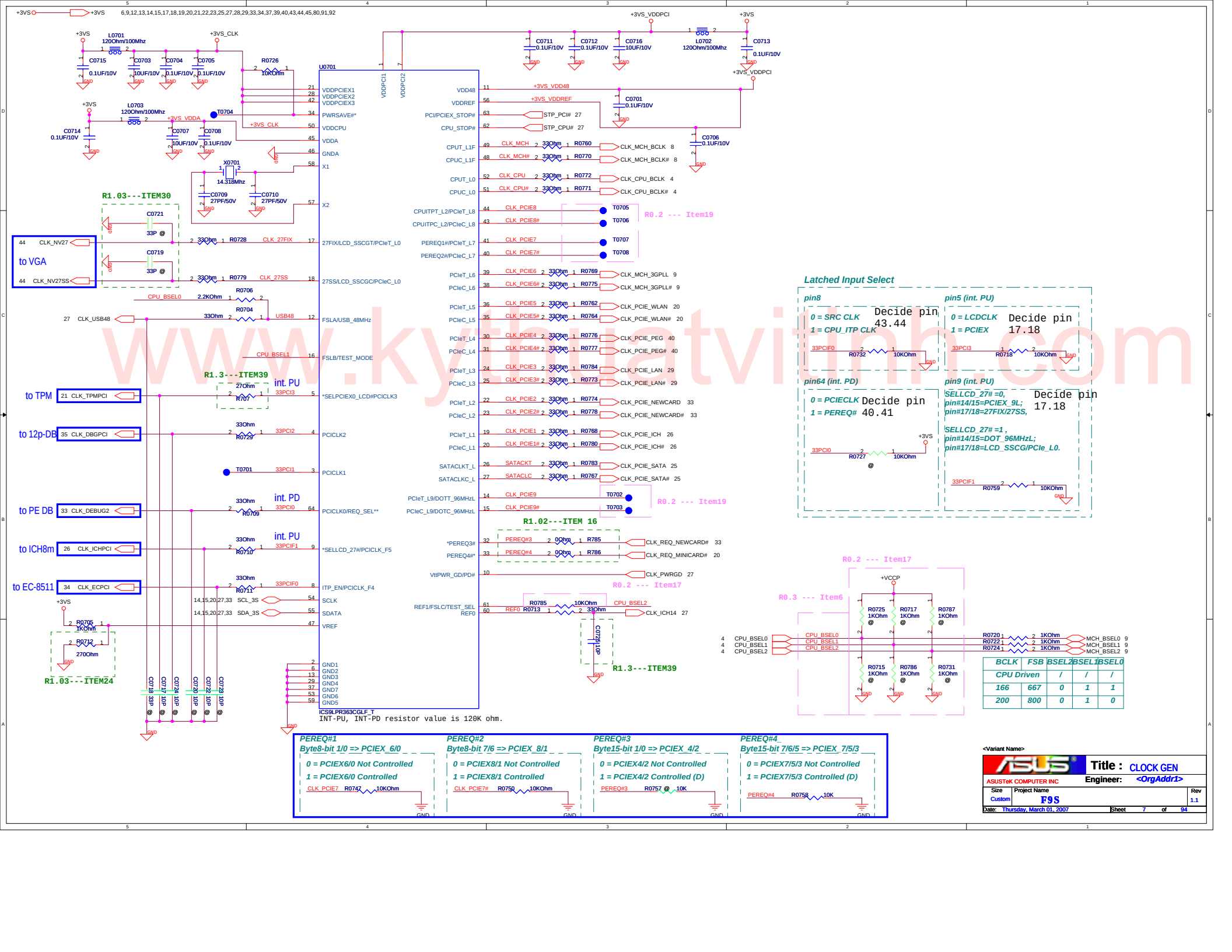
ASUSTeK COMPUTER INC

Title : CPU CAP, Thermal,FAN_CTRL

Engineer:

Size	Project Name	Rev
Custom	F9S	1.1

Date: Tuesday, February 27, 2007 Sheet 6 of 94



RCOMP

For Calibrating the FSB I/O Buffer

R0801 24.9Ohm 1% — H_RCOMP — GND

SCOMP

For Slew Rate Compenssation on the FSB

+VCCP

R0802 54.9Ohm 1% — H_SCOMP

R0803 54.9Ohm 1% — H_SCOMP#

Voltage Swing

For Providing a Reference Voltage to The FSB RCOMP circuits

+VCCP — R0804 221Ohm — H_SWING — R0805 100Ohm 1% — GND; C0802 0.1UF/16V — GND

4 H_D#[63:0] — H_D#[63:0]

4 H_A#[35:3] — H_A#[35:3]

U0801A — HOST — CRESTLINE_965PM

H_D#0	E2	H_D#_0	
H_D#1	G2	H_D#_1	
H_D#2	G7	H_D#_2	
H_D#3	M6	H_D#_3	
H_D#4	H7	H_D#_4	
H_D#5	H3	H_D#_5	
H_D#6	G4	H_D#_6	
H_D#7	F3	H_D#_7	
H_D#8	N8	H_D#_8	
H_D#9	H2	H_D#_9	
H_D#10	M10	H_D#_10	
H_D#11	N12	H_D#_11	
H_D#12	N9	H_D#_12	
H_D#13	H5	H_D#_13	
H_D#14	P13	H_D#_14	
H_D#15	K9	H_D#_15	
H_D#16	M2	H_D#_16	
H_D#17	W10	H_D#_17	
H_D#18	Y8	H_D#_18	
H_D#19	V4	H_D#_19	
H_D#20	M3	H_D#_20	
H_D#21	J1	H_D#_21	
H_D#22	N5	H_D#_22	
H_D#23	N3	H_D#_23	
H_D#24	W6	H_D#_24	
H_D#25	W9	H_D#_25	
H_D#26	N2	H_D#_26	
H_D#27	Y7	H_D#_27	
H_D#28	Y9	H_D#_28	
H_D#29	P4	H_D#_29	
H_D#30	W3	H_D#_30	
H_D#31	N1	H_D#_31	
H_D#32	AD12	H_D#_32	
H_D#33	AE3	H_D#_33	
H_D#34	AD9	H_D#_34	
H_D#35	AC9	H_D#_35	
H_D#36	AC7	H_D#_36	
H_D#37	AC14	H_D#_37	
H_D#38	AD11	H_D#_38	
H_D#39	AC11	H_D#_39	
H_D#40	AB2	H_D#_40	
H_D#41	AD7	H_D#_41	
H_D#42	AB1	H_D#_42	
H_D#43	Y3	H_D#_43	
H_D#44	AC6	H_D#_44	
H_D#45	AE2	H_D#_45	
H_D#46	AC5	H_D#_46	
H_D#47	AG3	H_D#_47	
H_D#48	AJ9	H_D#_48	
H_D#49	AH8	H_D#_49	
H_D#50	AJ14	H_D#_50	
H_D#51	AE9	H_D#_51	
H_D#52	AE11	H_D#_52	
H_D#53	AH12	H_D#_53	
H_D#54	AJ5	H_D#_54	
H_D#55	AH5	H_D#_55	
H_D#56	AJ6	H_D#_56	
H_D#57	AE7	H_D#_57	
H_D#58	AJ7	H_D#_58	
H_D#59	AJ2	H_D#_59	
H_D#60	AE5	H_D#_60	
H_D#61	AJ3	H_D#_61	
H_D#62	AH2	H_D#_62	
H_D#63	AH13	H_D#_63	
H_SWING	B3	H_SWING	
H_RCOMP	C2	H_RCOMP	
H_SCOMP	W1	H_SCOMP	
H_SCOMP#	W2	H_SCOMP#	
	B6	H_CPURST#	
	E5	H_CPUSLP#	
	B9	H_AVREF	
	A9	H_DVREF	

H_A#_3	J13	H_A#3	
H_A#_4	B11	H_A#4	
H_A#_5	C11	H_A#5	
H_A#_6	M11	H_A#6	
H_A#_7	C15	H_A#7	
H_A#_8	F16	H_A#8	
H_A#_9	L13	H_A#9	
H_A#_10	G17	H_A#10	
H_A#_11	C14	H_A#11	
H_A#_12	K16	H_A#12	
H_A#_13	B13	H_A#13	
H_A#_14	L16	H_A#14	
H_A#_15	J17	H_A#15	
H_A#_16	B14	H_A#16	
H_A#_17	K19	H_A#17	
H_A#_18	P15	H_A#18	
H_A#_19	R17	H_A#19	
H_A#_20	B16	H_A#20	
H_A#_21	H20	H_A#21	
H_A#_22	L19	H_A#22	
H_A#_23	D17	H_A#23	
H_A#_24	M17	H_A#24	
H_A#_25	N16	H_A#25	
H_A#_26	J19	H_A#26	
H_A#_27	B18	H_A#27	
H_A#_28	E19	H_A#28	
H_A#_29	B17	H_A#29	
H_A#_30	B15	H_A#30	
H_A#_31	E17	H_A#31	
H_A#_32	C18	H_A#32	
H_A#_33	A19	H_A#33	
H_A#_34	B19	H_A#34	
H_A#_35	N19	H_A#35	
H_ADS#	G12	H_ADS#	H_ADS# 4
H_ADSTB#_0	H17	H_ADSTB#0	H_ADSTB#0 4
H_ADSTB#_1	G20	H_ADSTB#1	H_ADSTB#1 4
H_BNR#	C8	H_BNR#	H_BNR# 4
H_BPRI#	E8	H_BPRI#	H_BPRI# 4
H_BREQ#	F12	H_BREQ#0	H_BREQ#0 4
H_DEFER#	D6	H_DEFER#	H_DEFER# 4
H_DBSY#	C10	H_DBSY#	H_DBSY# 4
HPLL_CLK	AM5		CLK_MCH_BCLK 7
HPLL_CLK#	AM7		CLK_MCH_BCLK# 7
H_DPWR#	H8	H_DPWR#	H_DPWR# 4
H_DRDY#	K7	H_DRDY#	H_DRDY# 4
H_HIT#	E4		H_HIT# 4
H_HITM#	C6		H_HITM# 4
H_LOCK#	G10		H_LOCK# 4
H_TRDY#	B7		H_TRDY# 4
H_DINV#_0	K5		H_DINV#0 4
H_DINV#_1	L2		H_DINV#1 4
H_DINV#_2	AD13		H_DINV#2 4
H_DINV#_3	AE13		H_DINV#3 4
H_DSTBN#_0	M7		H_DSTBN#0 4
H_DSTBN#_1	K3		H_DSTBN#1 4
H_DSTBN#_2	AD2		H_DSTBN#2 4
H_DSTBN#_3	AH11		H_DSTBN#3 4
H_DSTBP#_0	L7		H_DSTBP#0 4
H_DSTBP#_1	K2		H_DSTBP#1 4
H_DSTBP#_2	AC2		H_DSTBP#2 4
H_DSTBP#_3	AJ10		H_DSTBP#3 4
H_REQ#_0	M14	H_REQ#0	
H_REQ#_1	E13	H_REQ#1	
H_REQ#_2	A11	H_REQ#2	
H_REQ#_3	H13	H_REQ#3	
H_REQ#_4	B12	H_REQ#4	
H_RS#_0	E12	H_RS#0	H_RS#0 4
H_RS#_1	D7	H_RS#1	H_RS#1 4
H_RS#_2	D8	H_RS#2	H_RS#2 4

4 H_REQ#[4:0] — H_REQ#[4:0]

T0801

4 H_CPURST#
4 H_CPUSLP#
R0807 0Ohm

+VCCP — R0809 1KOhm 1% — H_VREF — R0806 0Ohm — H_AVREF

H_VREF — C0801 0.1UF/10V — GND; R0808 2KOhm 1% — GND

<Variant Name>

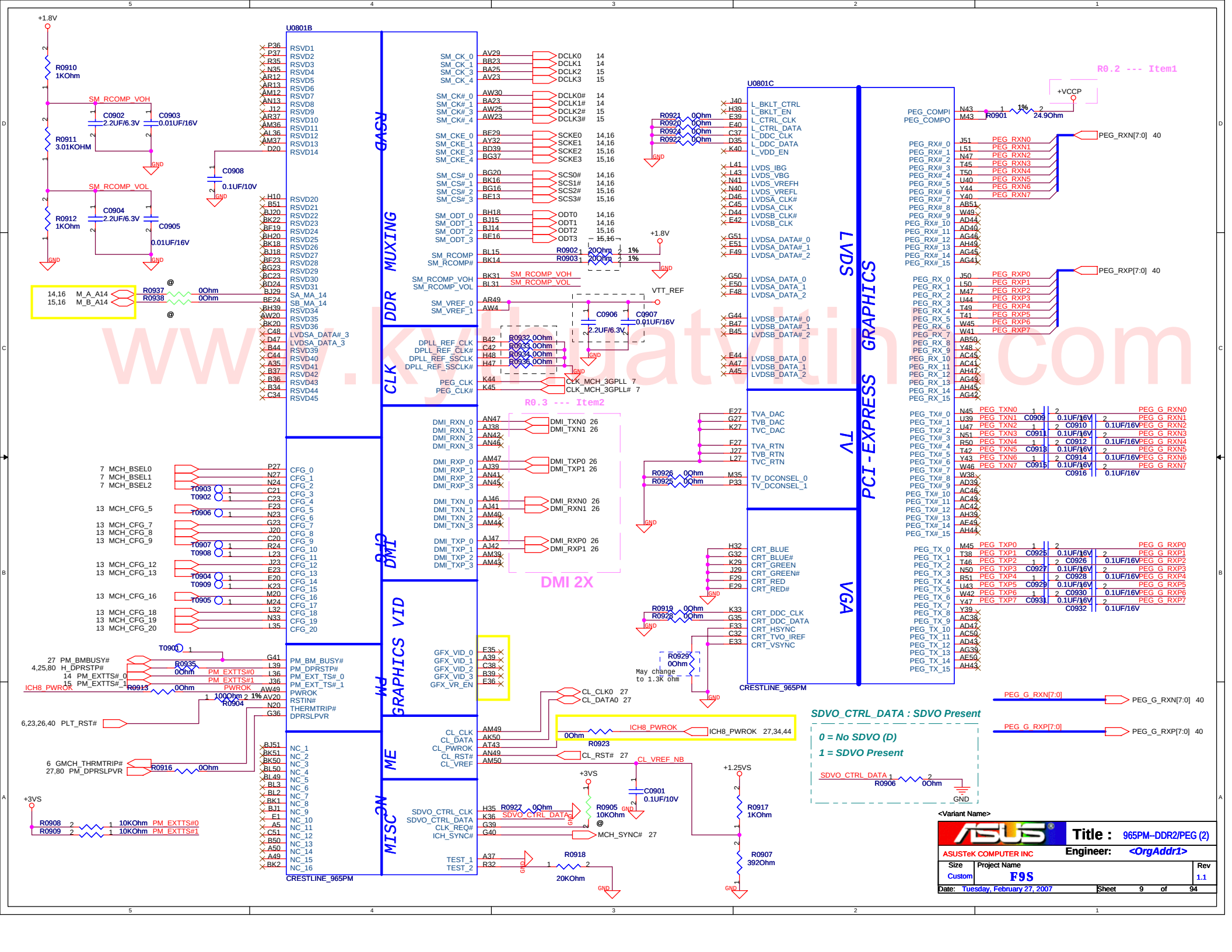
ASUSTeK COMPUTER INC

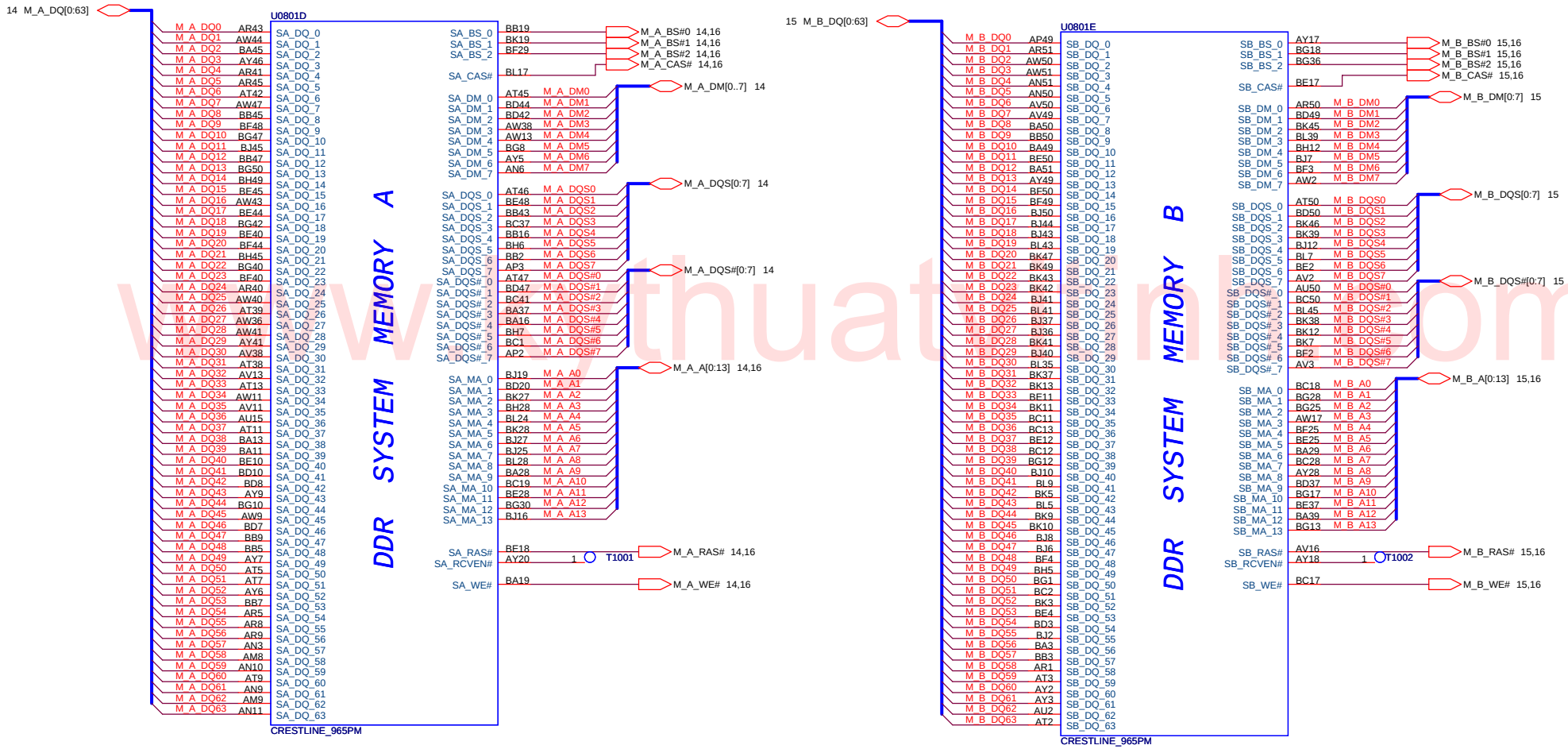
Title : 965PM -- CPU (1)

Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom	F9S	1.1

Date: Tuesday, February 27, 2007 Sheet 8 of 94


U0801B
U0801C
CRESTLINE_965PM
DDR MUXING
CLK
DMI
GRAPHICS VID
PM
ME
MISC
SDVO
LVDS
TV
VGA
PCI-EXPRESS GRAPHICS
DMI 2X
R0.2 --- Item1
R0.3 --- Item2
SDVO_CTRL_DATA : SDVO Present
0 = No SDVO (D)
1 = SDVO Present
Title : 965PM--DDR2/PEG (2)
ASUSTeK COMPUTER INC
Engineer: <OrgAddr1>
Project Name F9S
Date: Tuesday, February 27, 2007
Sheet 9 of 94



<Variant Name>

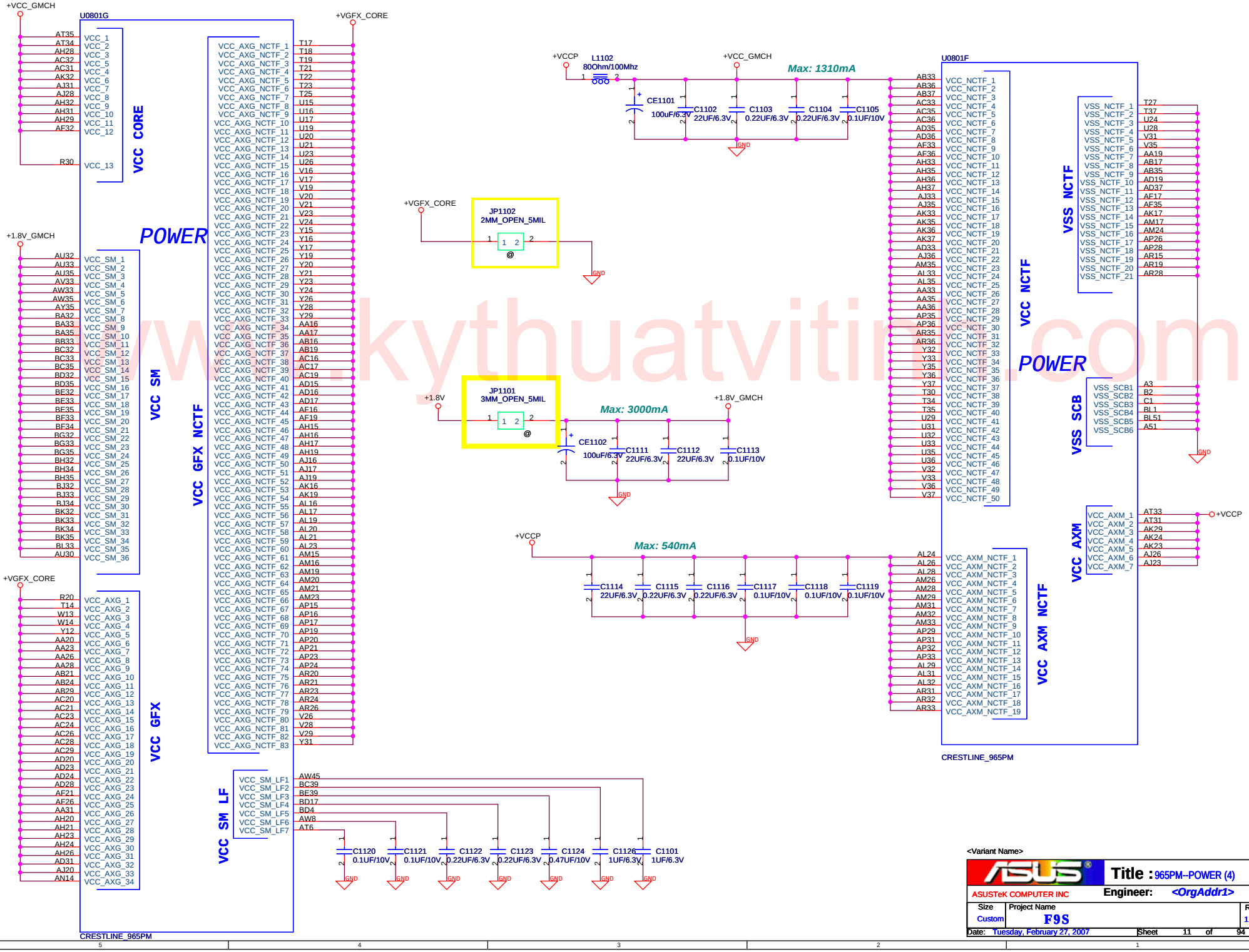
ASUSTeK COMPUTER INC

Title : 965PM--DDR2 bus (3)

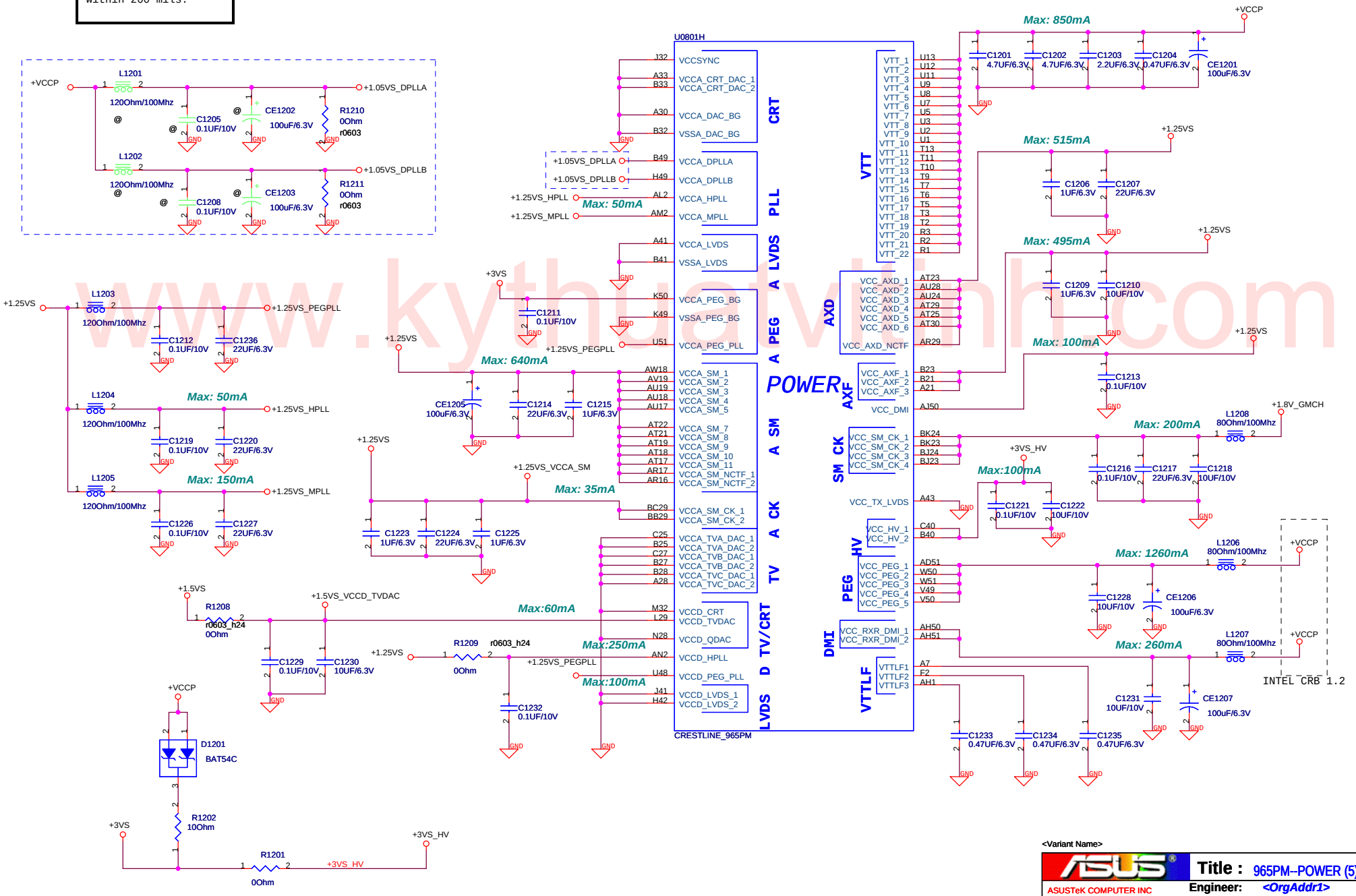
Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom	F9S	1.1

Date: Tuesday, February 27, 2007 Sheet 10 of 94



NOTE:0.1uF caps in 1.5VS_XPLL need to be located as edge caps within 200 mils.



<Variant Name>

ASUSTeK COMPUTER INC

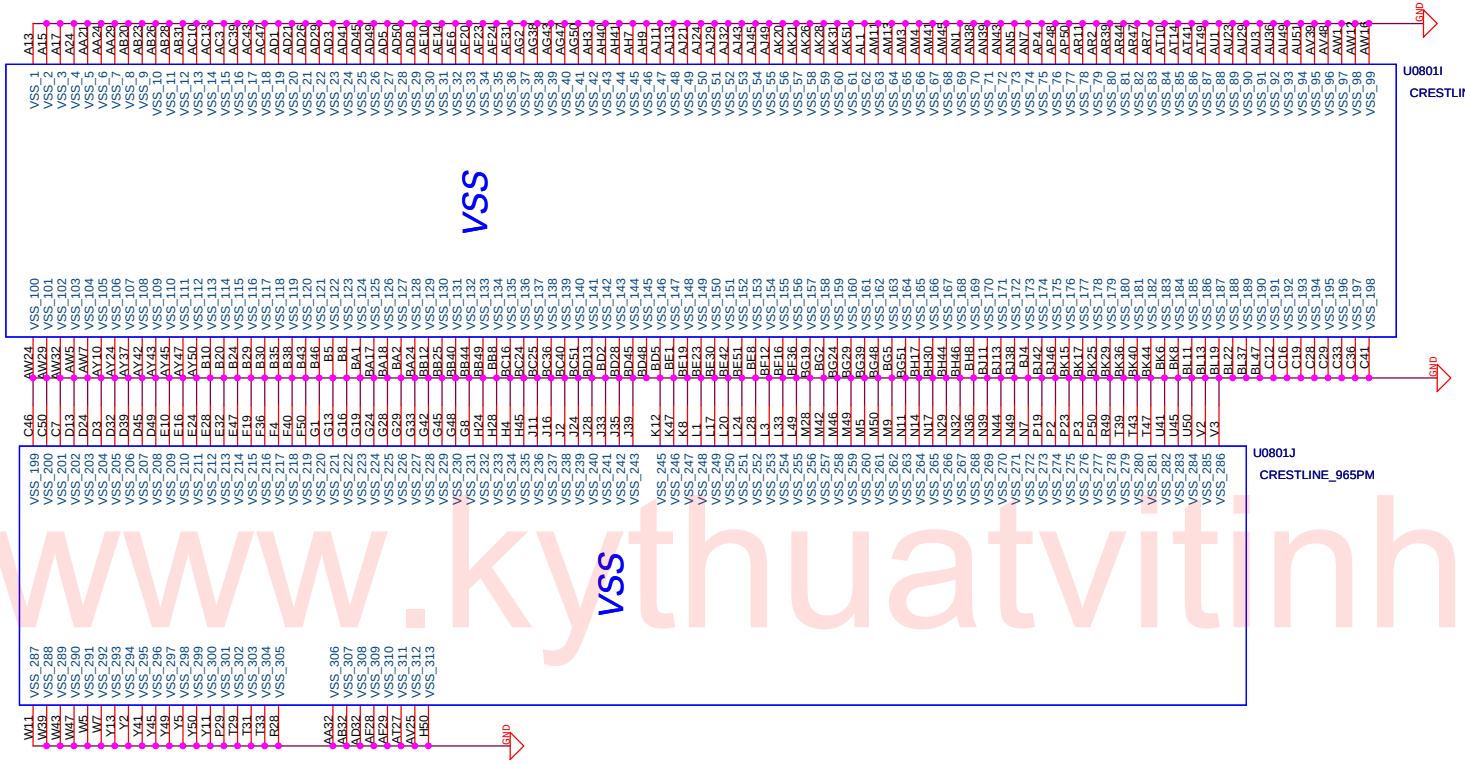
Title : 965PM--POWER (5)

Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom	F9S	1.1

Date: Monday, February 05, 2007 Sheet 12 of 94

HIGH = LANES REVERSED



9 MCH_CFG_5
R0.2 --- Item2
R1301
4.02KOHM

CFG5 : DMI STRAP
HIGH = DMI X 4 (Default)
LOW = DMI X 2

9 MCH_CFG_7
R1304
4.02KOHM
@

CFG7 : CPU STRAP
HIGH = Mobile CPU (Default)
LOW = Reserved

9 MCH_CFG_8
R1306
4.02KOHM
@

CFG8 : Low Power PCI-E
0 = Normal mode
1 = Low Power Mode (Default)

9 MCH_CFG_9
R1302
4.02KOHM
@

CFG9 : PCIE GRAPHIC LANE
LOW = REVERSE LANE
HIGH = Normal Operation (Default)

9 MCH_CFG_16
R1305
4.02KOHM
@

CFG16 : Dynamic ODT STRAP
Low = Dynamic ODT Disabled
HIGH = Dyanamic ODT Enabled (default)

+3VS
R1310
4.02KOHM
@
9 MCH_CFG_18

CFG18 : VCC Select
LOW = 1.05V (default)
HIGH = 1.5V

+3VS
R1303
4.02KOHM
@
9 MCH_CFG_19

CFG19 : DMI LANE REVERSAL
LOW = NORMAL (default)
HIGH = LANES REVERSED

+3VS
R1307
4.02KOHM
@
9 MCH_CFG_20

CFG20 : SDVO/PCIE CONCURRENT MODE
LOW = ONLY SDVO or PCIE is Operational (default)
HIGH = SDVO and PCIE are operating simultaneously via the PEG port

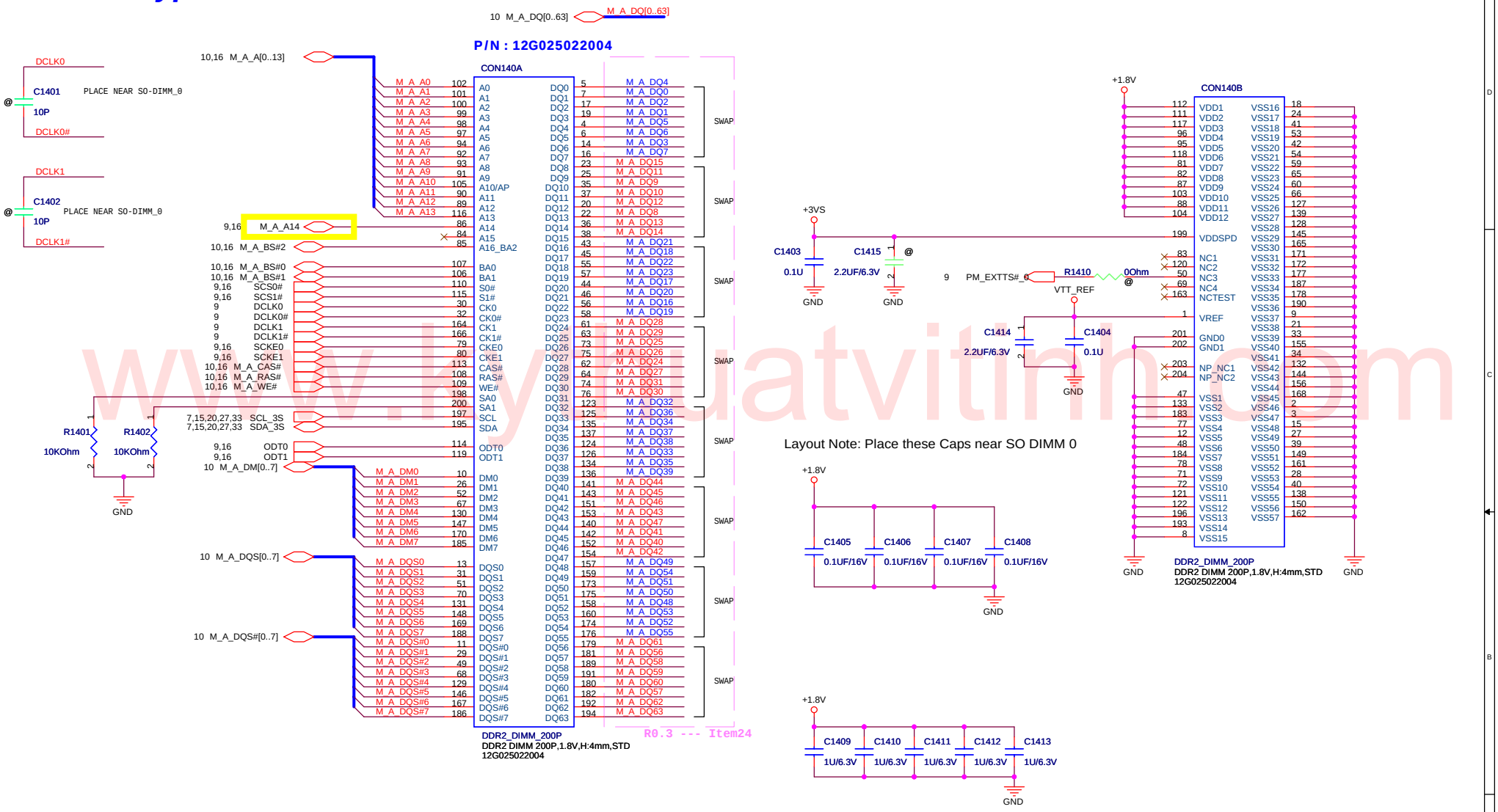
9 MCH_CFG_13
R1308
4.02KOHM
@

9 MCH_CFG_12
R1309
4.02KOHM
@

CFG [13:12] : XOR/ALL-Z
00 = Reserved
01= XOR Mode Enabled
10= All-Z Mode Enabled
11= Normal Operation (Default)

ASUSTeK COMPUTER INC	Title : GND/Strapping (6)	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: F9S	Rev: 1.1
Date: Tuesday, February 27, 2007	Sheet 13 of 94	

Standard Type



<Variant Name>

ASUSTeK COMPUTER INC

Title : DDR SO-DIMM 0

Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom	F9S	1.1

Date: Tuesday, February 27, 2007 Sheet 14 of 94

Standard Type

10 M_B_DQ[0..63] — M_B_DQ[0..63]

10,16 M_B_A[0..13]

P/N : 12G025C22004

CON150A

DDR2_DIMM_200P

DDR2 DIMM 200P,1.8V,H:9.2mm,ST

12G025C22004

R0.3 --- Item24

DCLK2 — C1501 PLACE NEAR SO-DIMM_1 — @ 10P — DCLK2#

DCLK3 — C1502 PLACE NEAR SO-DIMM_1 — @ 10P — DCLK3#

+3VS — R1501 10KOhm — R1502 10KOhm — GND

Pin	Signal	Pin	Signal
102	M_B_A0	5	M_B_DQ4
101	M_B_A1	7	M_B_DQ1
100	M_B_A2	17	M_B_DQ3
99	M_B_A3	19	M_B_DQ2
98	M_B_A4	4	M_B_DQ5
97	M_B_A5	6	M_B_DQ0
94	M_B_A6	14	M_B_DQ6
92	M_B_A7	16	M_B_DQ7
93	M_B_A8	23	M_B_DQ9
91	M_B_A9	25	M_B_DQ8
105	M_B_A10	35	M_B_DQ12
90	M_B_A11	37	M_B_DQ11
89	M_B_A12	20	M_B_DQ10
116	M_B_A13	22	M_B_DQ13
86	9,16 M_B_A14	36	M_B_DQ15
84	A15	38	M_B_DQ14
85	10,16 M_B_BS#2	43	M_B_DQ21
	A16_BA2	45	M_B_DQ16
107		55	M_B_DQ18
106	10,16 M_B_BS#0 — BA0	57	M_B_DQ22
110	10,16 M_B_BS#1 — BA1	44	M_B_DQ20
115	9,16 SCS2# — S0#	46	M_B_DQ17
30	9,16 SCS3# — S1#	56	M_B_DQ23
32	9 DCLK2 — CK0	58	M_B_DQ19
164	9 DCLK2# — CK0#	61	M_B_DQ25
166	9 DCLK3 — CK1	63	M_B_DQ28
79	9 DCLK3# — CK1#	73	M_B_DQ26
80	9,16 SCKE2 — CKE0	75	M_B_DQ31
113	9,16 SCKE3 — CKE1	62	M_B_DQ29
108	10,16 M_B_CAS# — CAS#	64	M_B_DQ24
109	10,16 M_B_RAS# — RAS#	74	M_B_DQ27
198	10,16 M_B_WE# — WE#	76	M_B_DQ30
200	SA0	123	M_B_DQ36
197	7,14,20,27,33 SCL_3S — SA1 / SCL	125	M_B_DQ37
195	7,14,20,27,33 SDA_3S — SDA	135	M_B_DQ38
114	9,16 ODT2 — ODT0	137	M_B_DQ35
119	9,16 ODT3 — ODT1	124	M_B_DQ32
	10 M_B_DM[0..7]	126	M_B_DQ34
		134	M_B_DQ39
		136	M_B_DQ33
10	M_B_DM0 — DM0	141	M_B_DQ44
26	M_B_DM1 — DM1	143	M_B_DQ41
52	M_B_DM2 — DM2	151	M_B_DQ43
67	M_B_DM3 — DM3	153	M_B_DQ42
130	M_B_DM4 — DM4	140	M_B_DQ40
147	M_B_DM5 — DM5	142	M_B_DQ45
170	M_B_DM6 — DM6	152	M_B_DQ46
185	M_B_DM7 — DM7	154	M_B_DQ47
	10 M_B_DQS[0..7]	157	M_B_DQ50
13	M_B_DQS0 — DQS0	159	M_B_DQ55
31	M_B_DQS1 — DQS1	173	M_B_DQ54
51	M_B_DQS2 — DQS2	175	M_B_DQ53
70	M_B_DQS3 — DQS3	158	M_B_DQ52
131	M_B_DQS4 — DQS4	160	M_B_DQ49
148	M_B_DQS5 — DQS5	174	M_B_DQ51
169	M_B_DQS6 — DQS6	176	M_B_DQ48
188	M_B_DQS7 — DQS7	179	M_B_DQ60
	10 M_B_DQS#[0..7]	181	M_B_DQ61
11	M_B_DQS#0 — DQS#0	189	M_B_DQ58
29	M_B_DQS#1 — DQS#1	191	M_B_DQ63
49	M_B_DQS#2 — DQS#2	180	M_B_DQ56
68	M_B_DQS#3 — DQS#3	182	M_B_DQ57
129	M_B_DQS#4 — DQS#4	192	M_B_DQ62
146	M_B_DQS#5 — DQS#5	194	M_B_DQ59
167	M_B_DQS#6 — DQS#6		
186	M_B_DQS#7 — DQS#7		

SWAP

+1.8V — +1.8V — 9,11,14,16,37,83

+3VS — +3VS — 6,7,9,12,13,14,17,18,19,20,21,22,23,25,27,28,29,33,34,37,39,40,43,44,45,80,91,92

VTT_REF — VTT_REF — 9,14,16

+3VS — C1503 0.1U — GND; C1506 @ 2.2UF/6.3V — GND

9 PM_EXTTS#_1 — R1510 0Ohm @ — VTT_REF

C1504 2.2UF/6.3V — C1505 0.1U — VTT_REF — GND

CON150B

DDR2_DIMM_200P

DDR2 DIMM 200P,1.8V,H:9.2mm,ST

12G025C22004

Pin	Signal	Pin	Signal
112	VDD1	18	VSS16
111	VDD2	24	VSS17
117	VDD3	41	VSS18
96	VDD4	53	VSS19
95	VDD5	42	VSS20
118	VDD6	54	VSS21
81	VDD7	59	VSS22
82	VDD8	65	VSS23
87	VDD9	60	VSS24
103	VDD10	66	VSS25
88	VDD11	127	VSS26
104	VDD12	139	VSS27
		128	VSS28
199	VDDSPD	145	VSS29
		165	VSS30
83	NC1	171	VSS31
120	NC2	172	VSS32
50	NC3	177	VSS33
69	NC4	187	VSS34
163	NCTEST	178	VSS35
		190	VSS36
1	VREF	9	VSS37
		21	VSS38
201	GND0	33	VSS39
202	GND1	155	VSS40
		34	VSS41
203	NP_NC1	132	VSS42
204	NP_NC2	144	VSS43
		156	VSS44
47	VSS1	168	VSS45
133	VSS2	2	VSS46
183	VSS3	3	VSS47
77	VSS4	15	VSS48
12	VSS5	27	VSS49
48	VSS6	39	VSS50
184	VSS7	149	VSS51
78	VSS8	161	VSS52
71	VSS9	28	VSS53
72	VSS10	40	VSS54
121	VSS11	138	VSS55
122	VSS12	150	VSS56
196	VSS13	162	VSS57
193	VSS14		
8	VSS15		

R0.3 --- Item1

Layout Note: Place these Caps near SO DIMM 1

+1.8V — C1517 0.1UF/16V — C1518 0.1UF/16V — C1515 0.1UF/16V — C1516 0.1UF/16V — GND

+1.8V — C1510 1U/6.3V — C1511 1U/6.3V — C1512 1U/6.3V — C1513 1U/6.3V — C1514 1U/6.3V — GND

<Variant Name>

Title : DDR SO-DIMM_1

ASUSTeK COMPUTER INC

Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom	F9S	1.1

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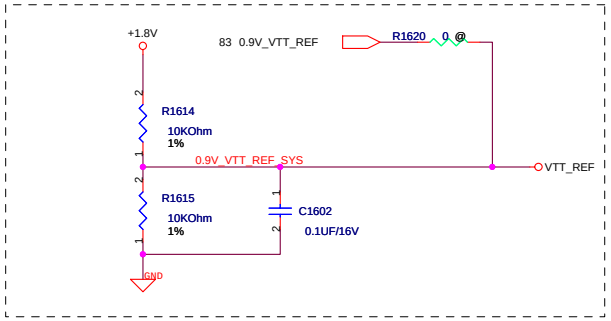
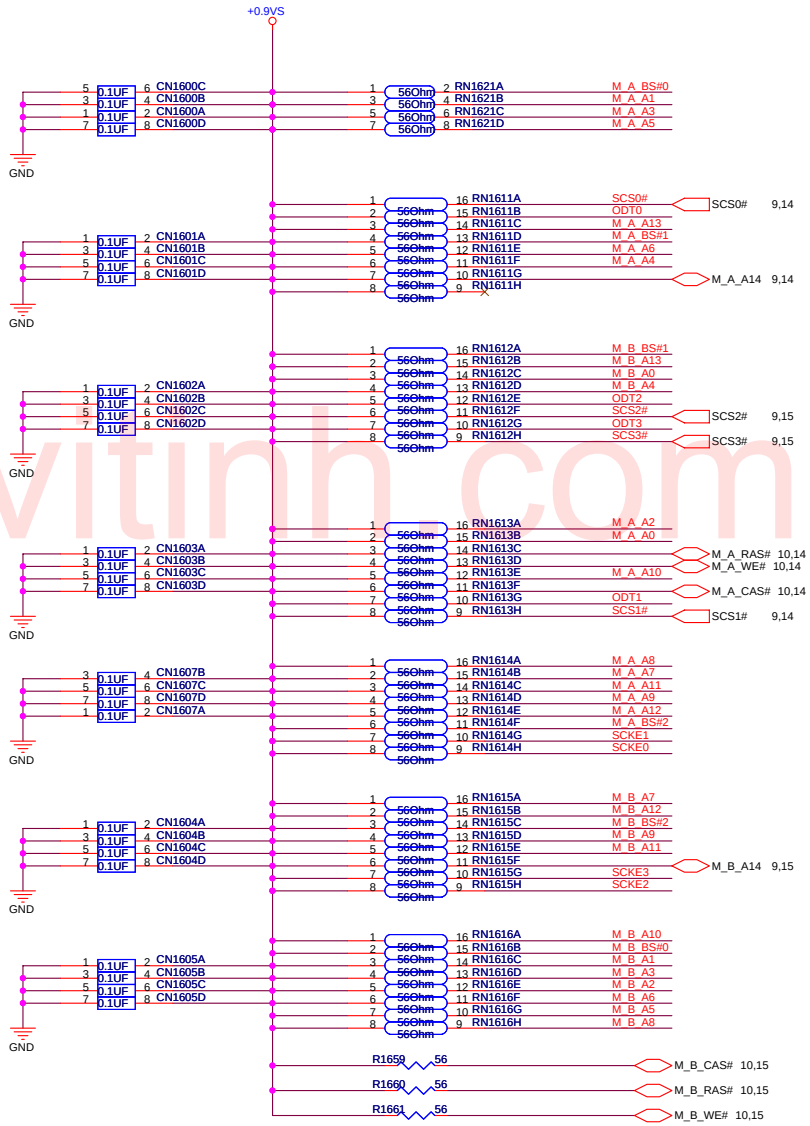


M_A_A[0..13] 10,14
M_A_BS#[0..2] 10,14
M_B_A[0..13] 10,15
M_B_BS#[0..2] 10,15
SCKE[0:3] 9,14,15
ODT[0:3] 9,14,15

SWAPPED

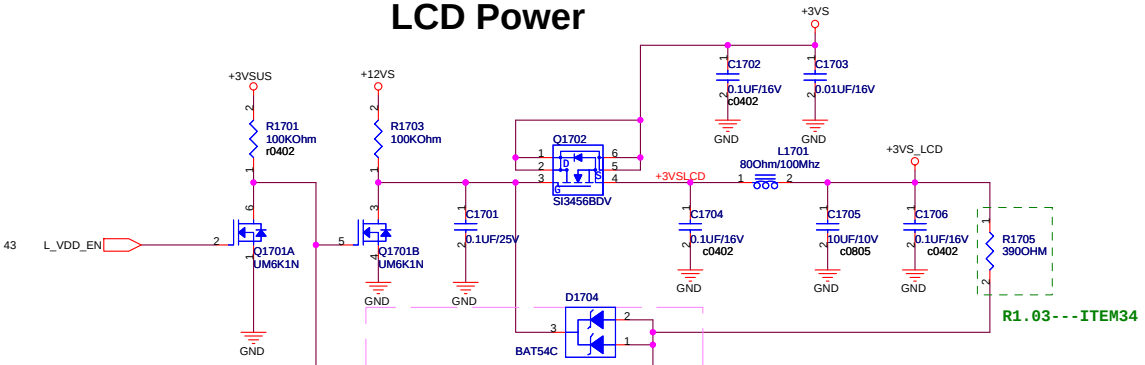


Layout note: Place array cap close to each pullup resistors terminated to +0.9VS

<Variant Name>

ASUSTeK COMPUTER INC	Title : DDR2 ADDR TERM	
	Engineer: <OrgAddr1>	
Size: Custom	Project Name: F9S	Rev: 1.1
Date: Tuesday, February 27, 2007	Sheet 16 of 94	

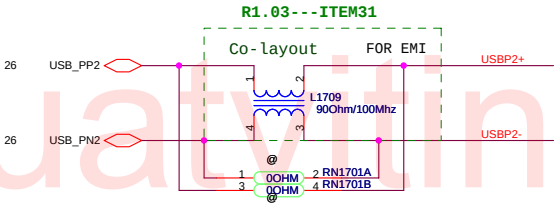
LCD Power



R1.03---ITEM34

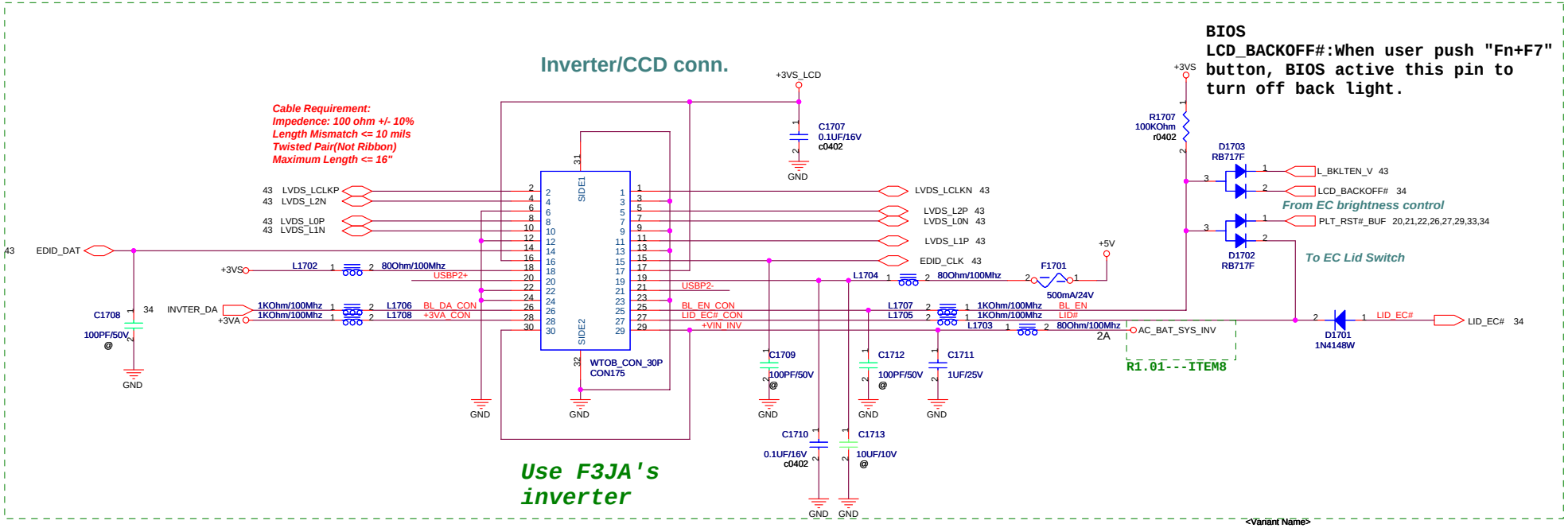
R0.3 --- Item5

R1.03---ITEM31



R1.2---ITEM36

Inverter/CCD conn.



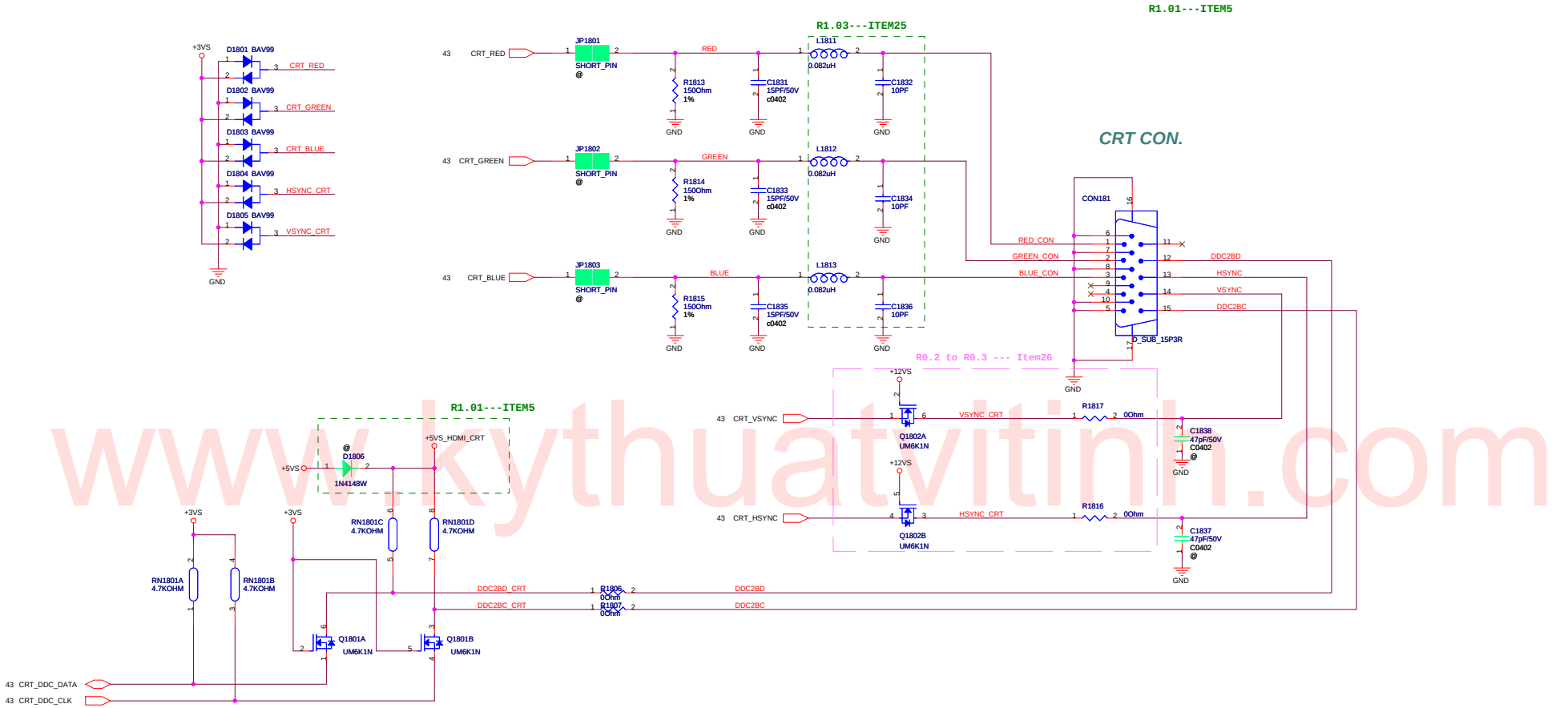
BIOS
LCD_BACKOFF#:When user push "Fn+F7" button, BIOS active this pin to turn off back light.

R1.01---ITEM8

Use F3JA's inverter

<Variant Name>

ASUSTeK COMPUTER INC	Title : LVDS & INVERTER	
	Engineer:	
Size: Custom	Project Name: F9S	Rev: 1.1
Date: Tuesday, February 27, 2007	Sheet 17 of 94	



<Variant Name>

ASUSTeK COMPUTER INC

Title : CRT

Engineer:

Size	Project Name	Rev
C	F9S	1.1

Date: Tuesday, February 27, 2007 Sheet 18 of 94

R0.2 --- Item5

Place near to GPU(NB8M-SE)

IFPC_IOVDD

R1912 49.9Ohm
R1913 49.9Ohm
R1914 49.9Ohm
R1915 49.9Ohm
R1916 49.9Ohm
R1917 49.9Ohm
R1918 49.9Ohm
R1919 49.9Ohm

44 TMDS_TX2P — R1905 0Ohm — L1904 200Ohm — R1904 0Ohm — HDMI_TX2P
44 TMDS_TX2N — HDMI_TX2N
44 TMDS_TX1P — R1907 0Ohm — L1905 200Ohm — R1906 0Ohm — HDMI_TX1P
44 TMDS_TX1N — HDMI_TX1N
44 TMDS_TX0P — R1909 0Ohm — L1906 200Ohm — R1908 0Ohm — HDMI_TX0P
44 TMDS_TX0N — HDMI_TX0N
44 TMDS_TXCP — R1911 0Ohm — L1907 200Ohm — R1910 0Ohm — HDMI_TXCP
44 TMDS_TXCN — HDMI_TXCN

MDC CON.

For MDC
H1900 L4E_1A — GND
H1901 L4E_1A — GND

CON1901 (BTOB_CON_12P)
25 ACZ_SDOUT_MDC
25 ACZ_SYNC_MDC
25 ACZ_SDIN1_MDC
25 ACZ_RST#_MDC
R1901 r0402 33Ohm
+3V
R1902 0Ohm
ACZ_BCLK_MDC 25
C1901 22PF/50V @
C1902 0.1UF/16V c0402 @
P/N:12G161200120

R1.01---ITEM4
+12VS
+5VS
+5VS_HDMI_CRT
Q1902 SI2302ADS
F1901 0.2A/30V
+5VS_HDMI
L1901 120Ohm/100Mhz
C1903 0.1U
C1904 0.1U
C1905 4700PF
+5VSHDMI

HDMI CON.

R0.4 --- Item9
+3VS
R1928 4.7KOhm
R1929 4.7KOhm
43 HDMI_DDC_CLK — Q1901A UM6K1N
43 HDMI_DDC_DATA — Q1901B UM6K1N

R1.01---ITEM4
R1926 1.8KOHM
R1927 1.8KOHM
DDC_CLK_HDMI — L1902 600Ohm/100Mhz — DDC Clock
DDC_DATA_HDMI — L1903 600Ohm/100Mhz — DDC Data
C1906 10PF
C1907 10PF

HDMI_CON_19P
HDMI_TX2P
HDMI_TX2N
HDMI_TX1P
HDMI_TX1N
HDMI_TX0P
HDMI_TX0N
HDMI_TXCP
HDMI_TXCN
DDC Clock
DDC Data
+5VSHDMI
P_GND2 P_GND4 P_GND3 P_GND1
CON1902
R1924 1KOhm
43 HDMI_HP
D1905 MMSZ4681T1G
R1925 10KOhm
D1904 BAV99
+5VS

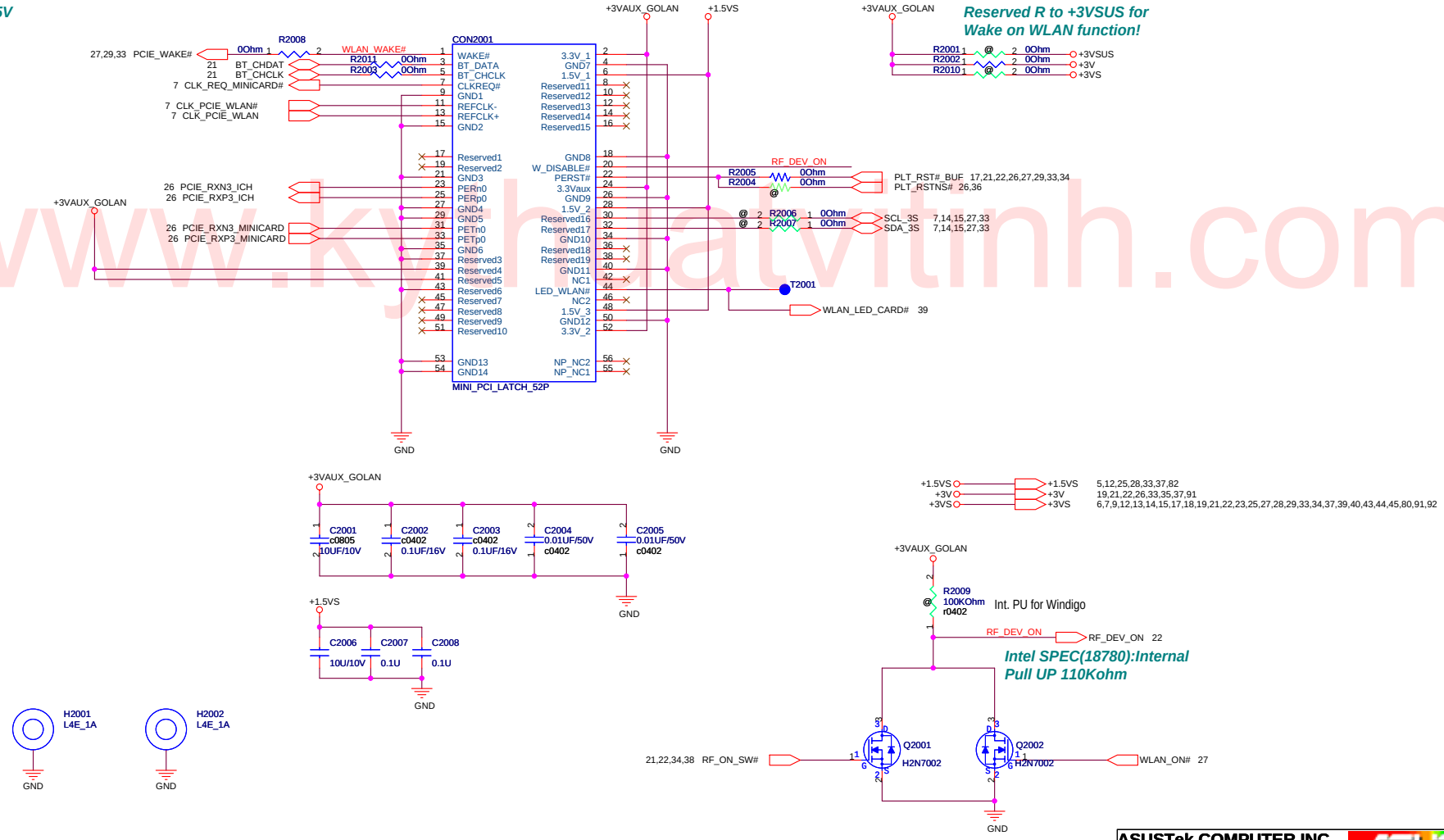
Note: 1. L1901,L1902,L1903: For EMI.(defult=0 ohm)
2. HDMI_DDC_CLK,HDMI_DDC_DATA: +5V tolerant

ASUSTek COMPUTER INC.
<OrgAddr1> Li-Te Rd.,Peitou, Taipei,Taiwan, ROC
Title: MDC,HDMI CON
Size: Custom | Document Number: F9S | Rev: 1.1
Date: Tuesday, February 27, 2007 | Sheet 19 of 94

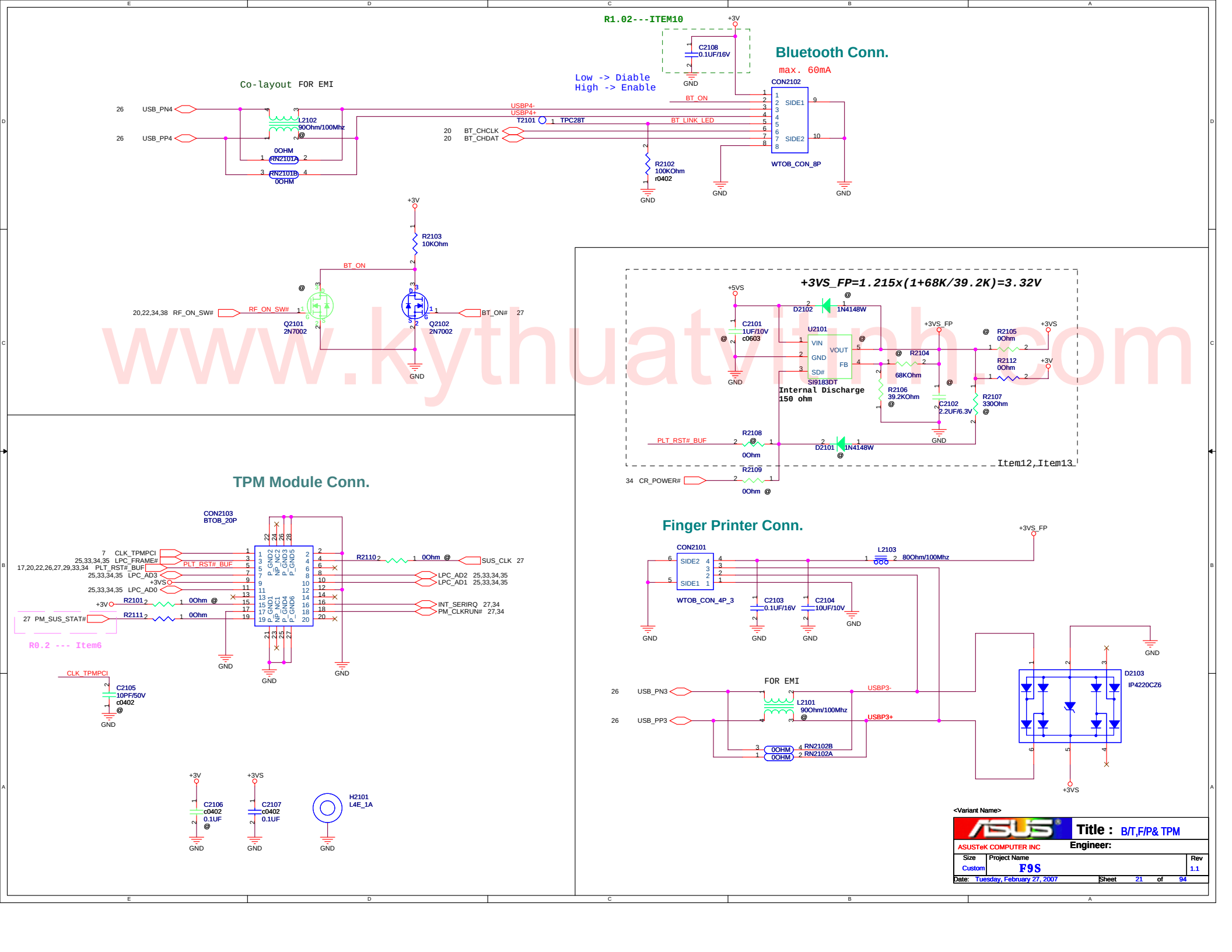
+3VAUX_GOLAN:+3.003V~+3.597V
Max= 1100 mA
+1.5VS:+1.425V~+1.575V
Max= 375 mA

P/N : 12G030100525_2006/1024

WLAN



ASUSTek COMPUTER INC.		
<OrgAddr1> Li-Te Rd.,Peitou, Taipei,Taiwan, ROC		
Title: MINI CARD--(1)		
Size: Custom	Document Number: F9S	Rev: 1.1
Date: Tuesday, February 27, 2007	Sheet 20 of 94	



<Variant Name>

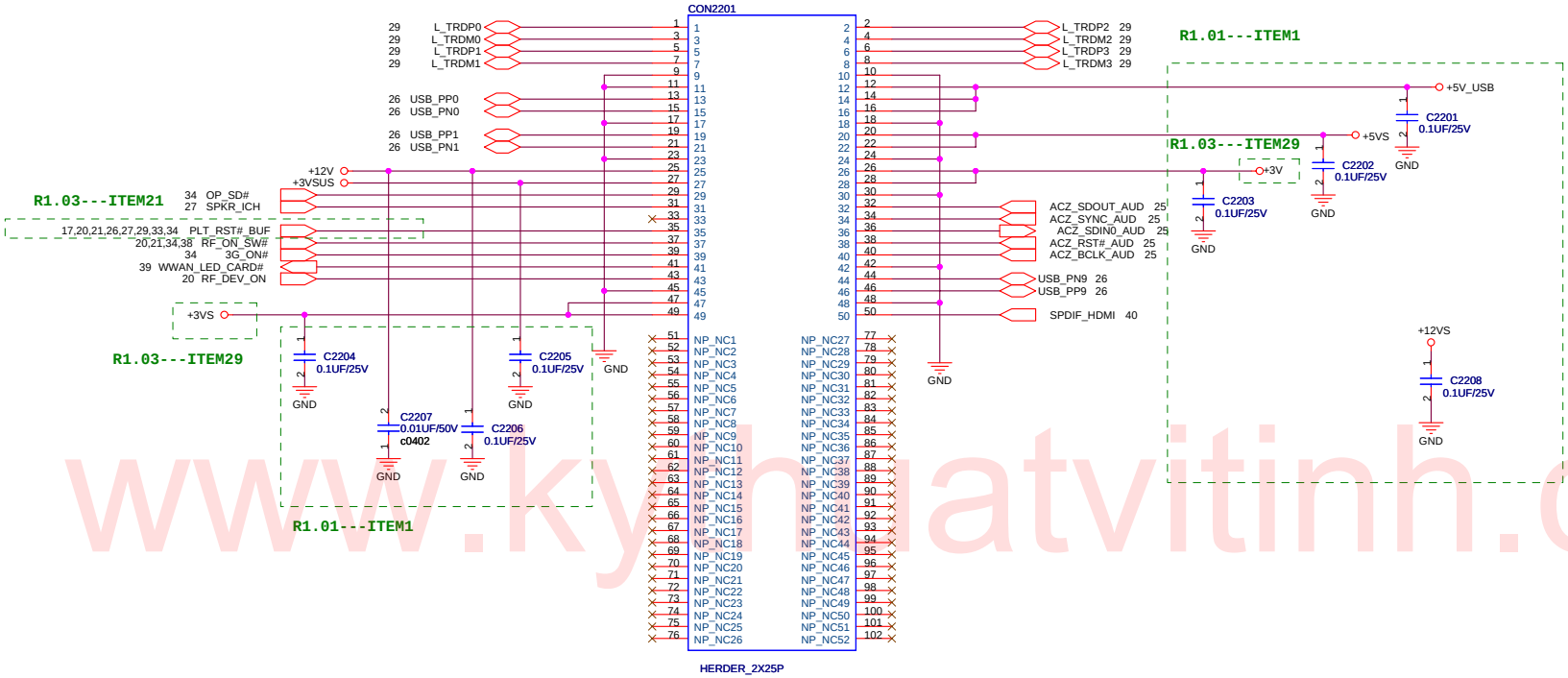
Title : B/T,F/P& TPM

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	F9S	1.1

Date: Tuesday, February 27, 2007 Sheet 21 of 94



<Variant Name>

ASUSTeK COMPUTER INC

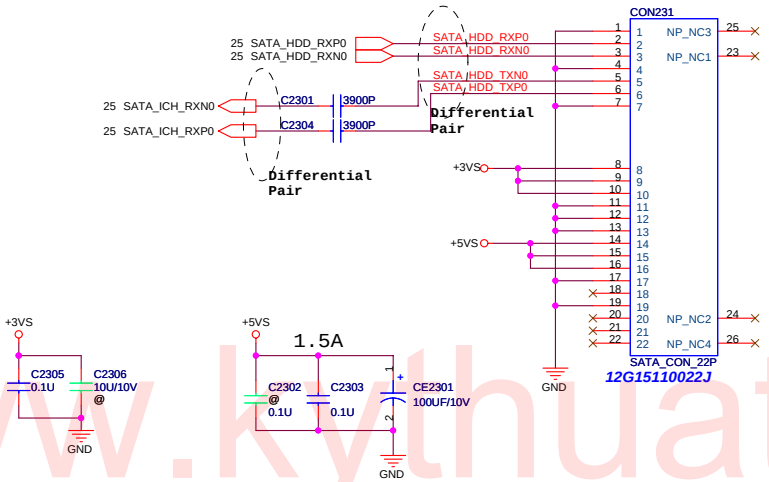
Title : B TO B CONN(M)

Engineer:

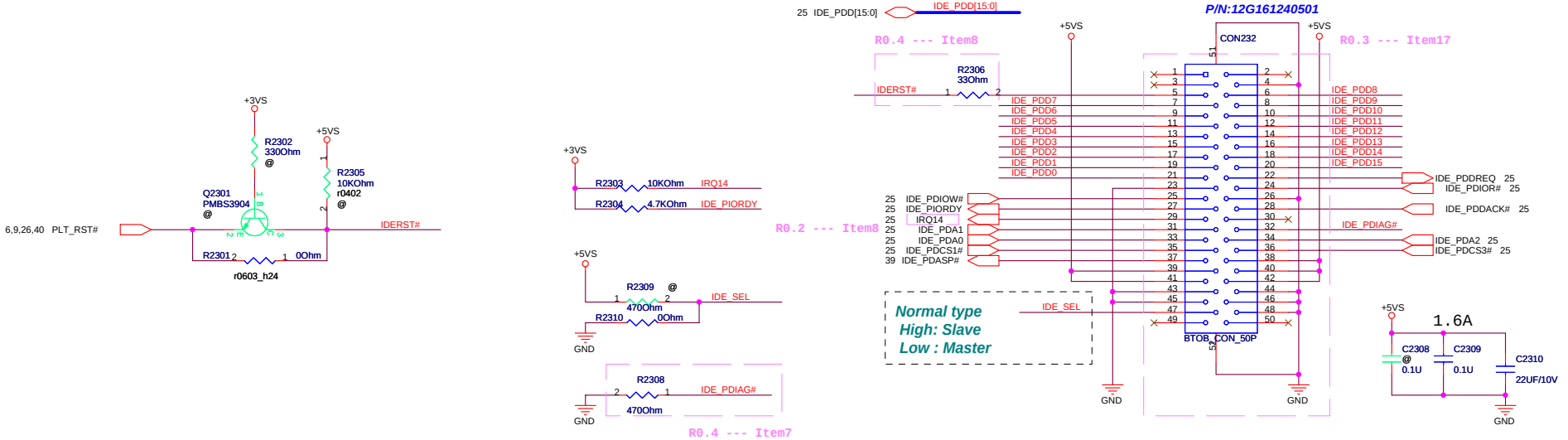
Size	Project Name	Rev
Custom	F9S	1.1

Date: Tuesday, February 27, 2007 Sheet 22 of 94

SATA HDD CON

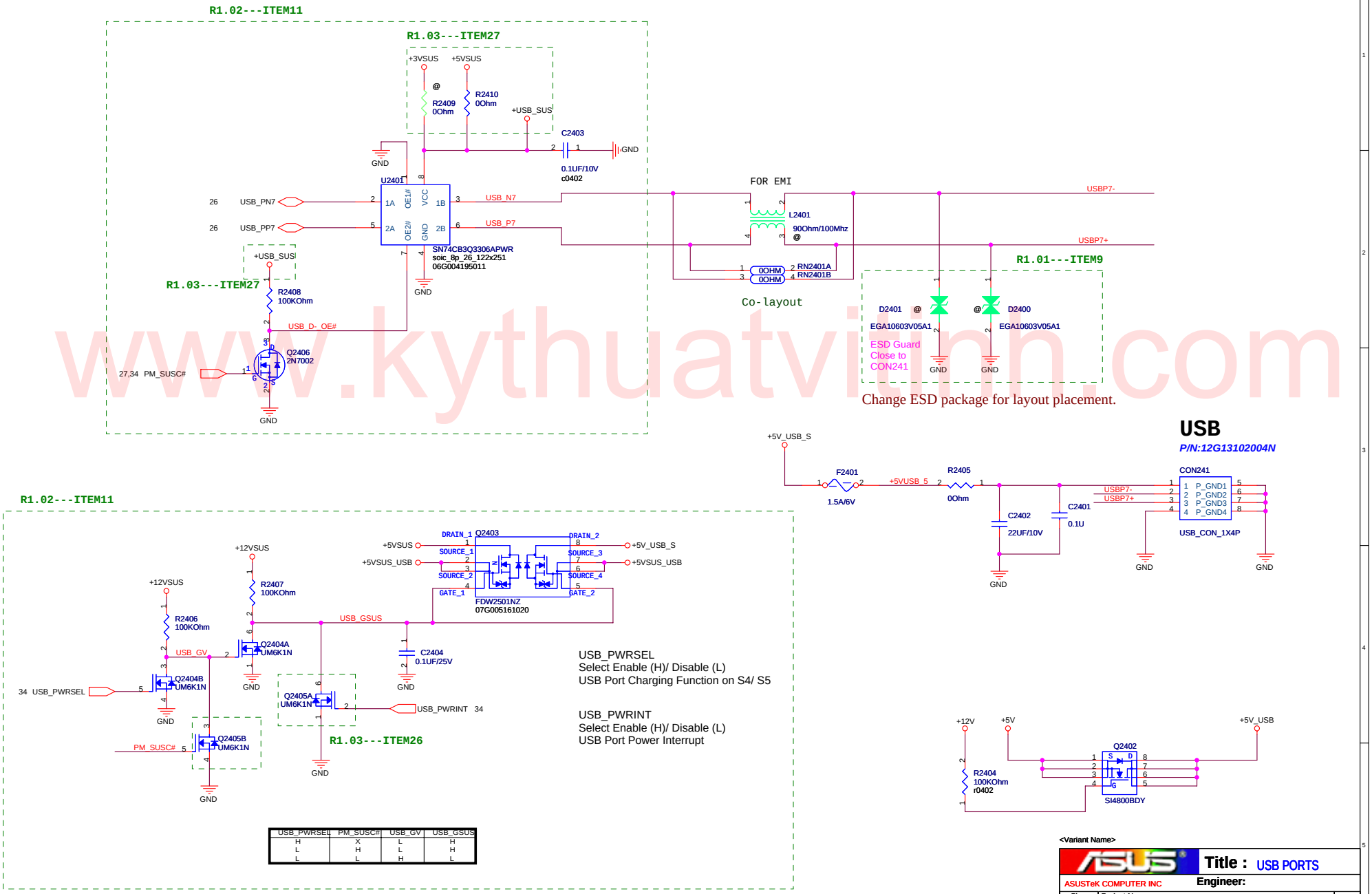


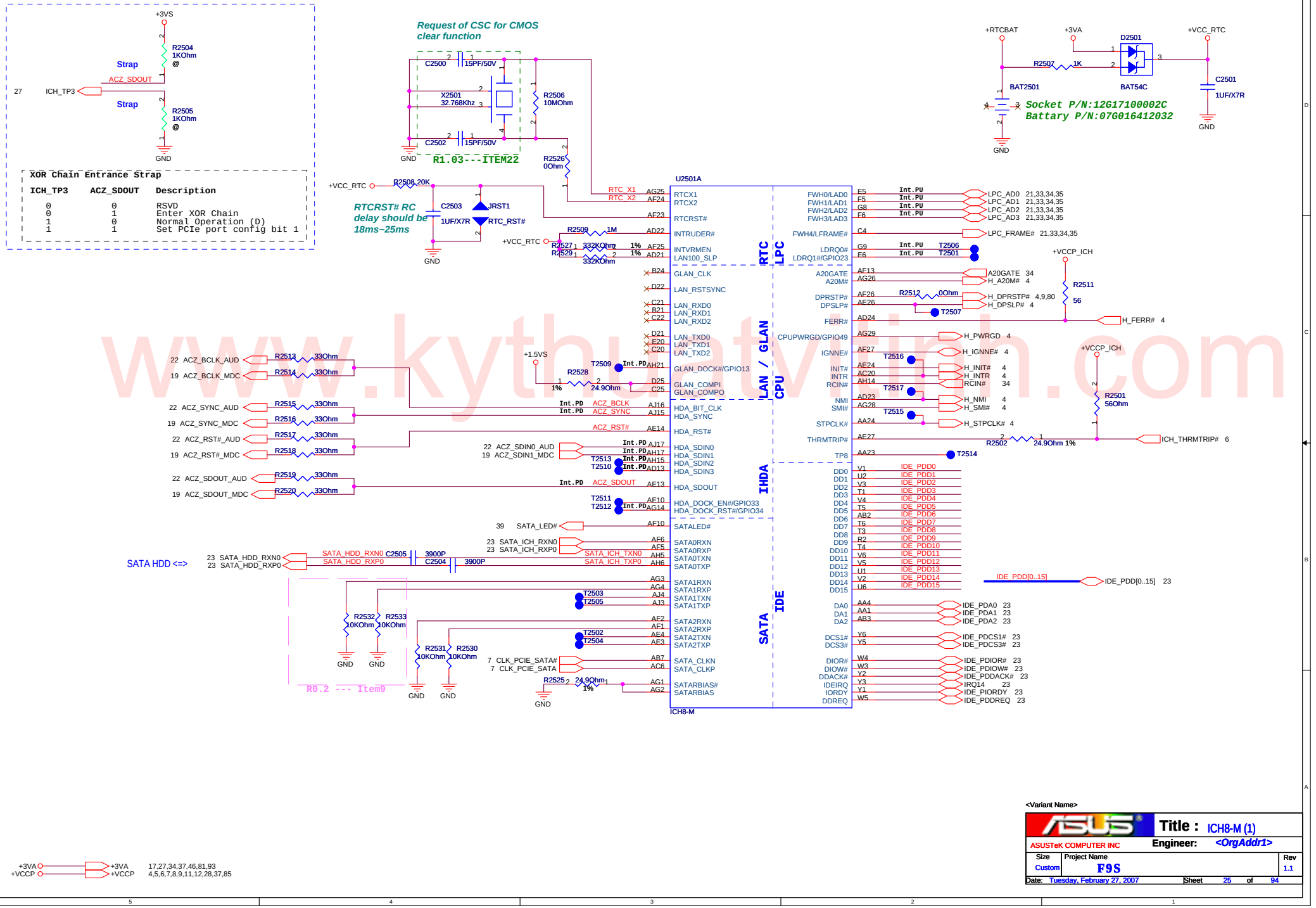
PATA CD-ROM CON

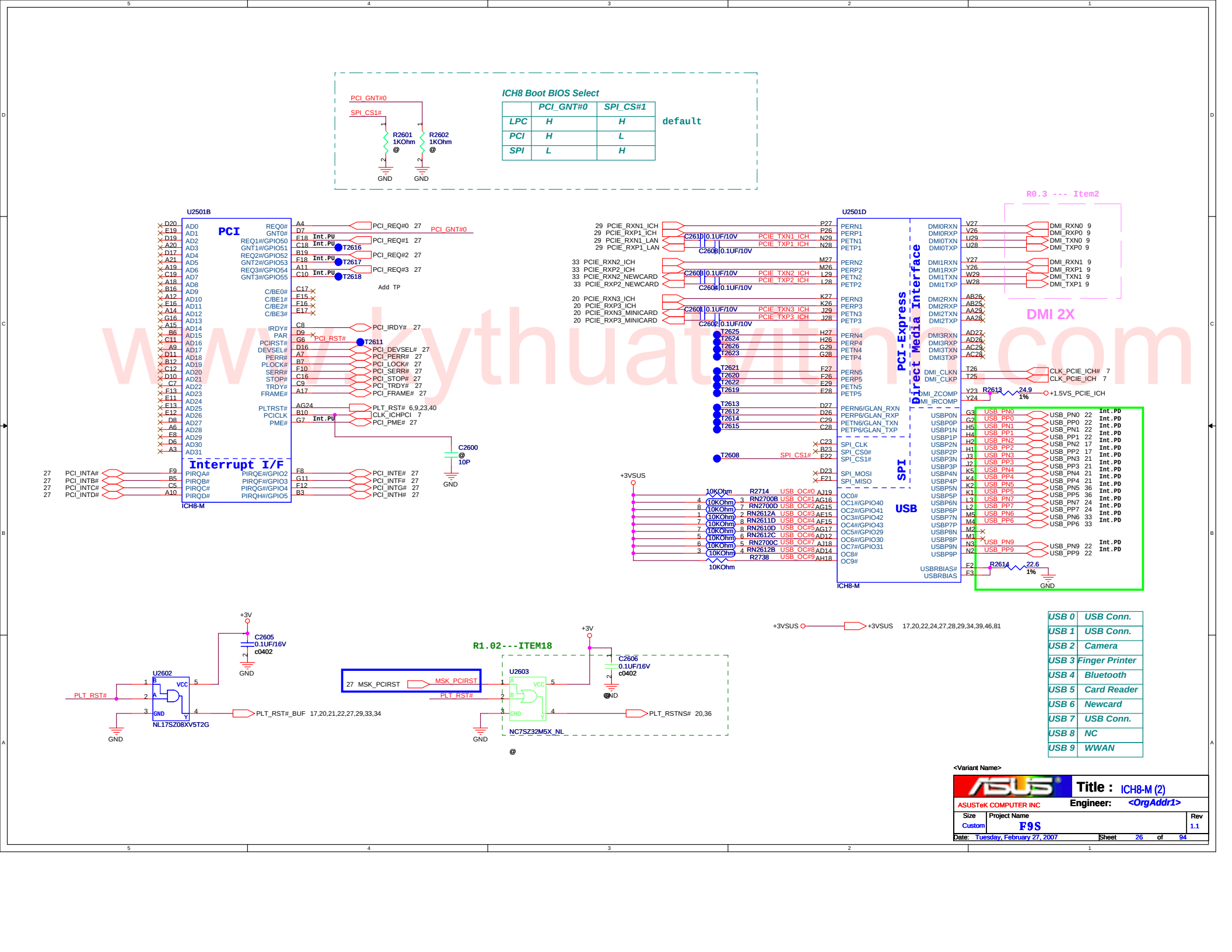


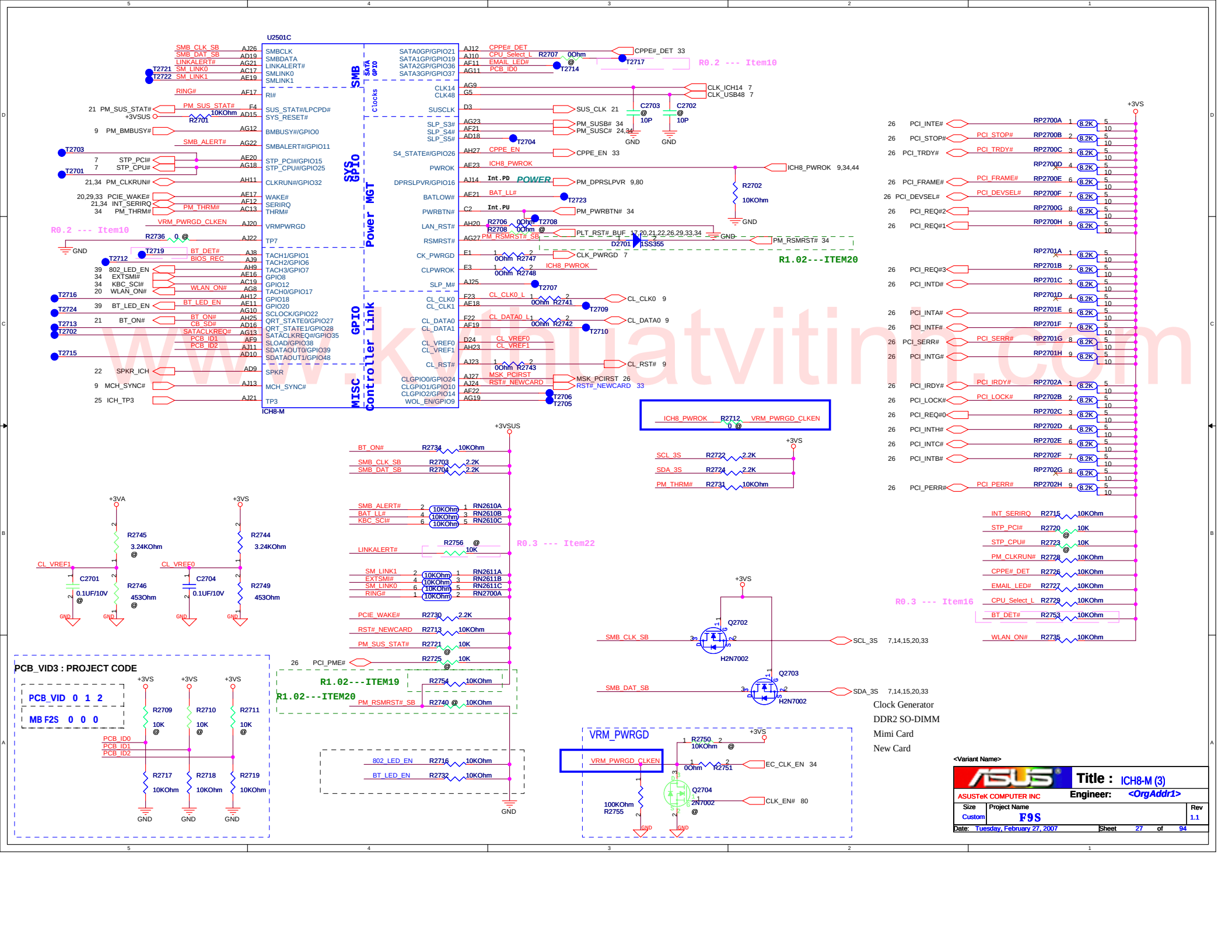
<Variant Name>

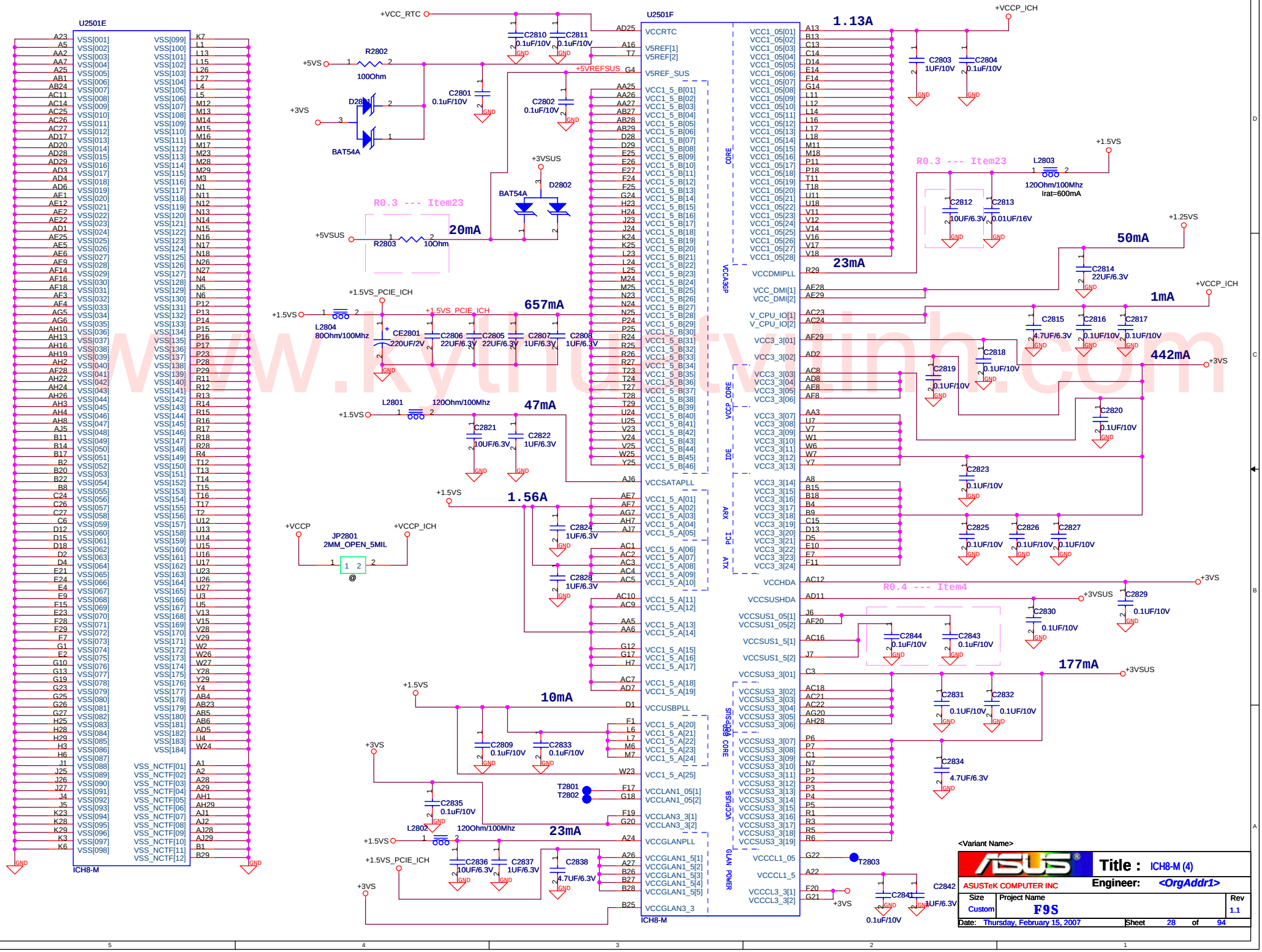
ASUSTeK COMPUTER INC	Title : HDD & CDROM	
	Engineer:	
Size: Custom	Project Name: F9S	Rev: 1.1
Date: Tuesday, February 27, 2007	Sheet 23 of 94	

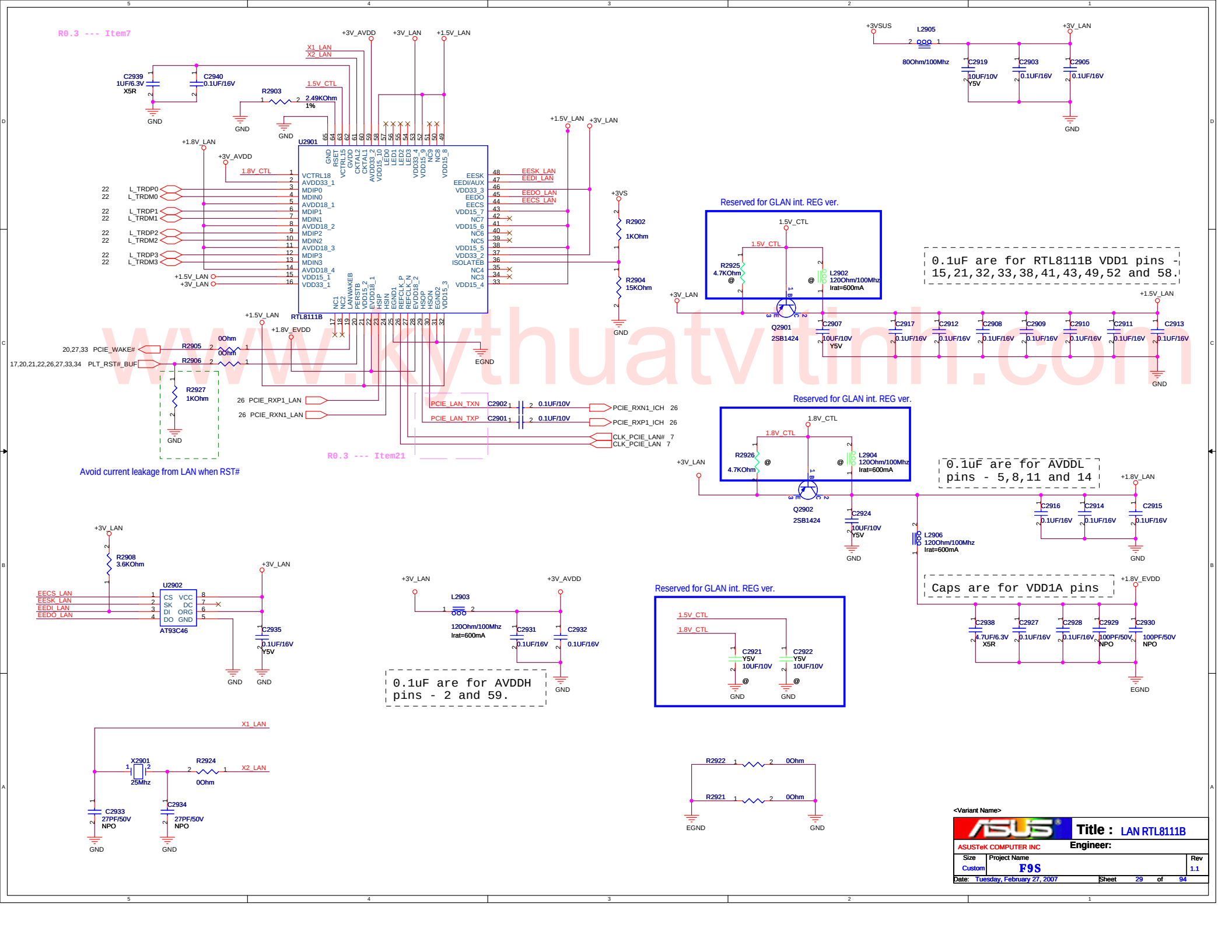



Strap
ACZ_SDOUT
ICH_TP3
R2504 1KOhm @
R2505 1KOhm @
XOR Chain Entrance Strap
ICH_TP3 ACZ_SDOUT Description
0 0 RSVD
0 1 Enter XOR Chain
1 0 Normal Operation (D)
1 1 Set PCIe port config bit 1
Request of CSC for CMOS clear function
C2500 15PF/50V
X2501 32.768Khz
C2502 15PF/50V
R2506 10MOhm
R2526 0Ohm
R1.03---ITEM22
RTCRST# RC delay should be 18ms~25ms
R2508 20K
C2503 1UF/X7R
JRST1
RTC_RST#
R2509 1M
R2527 332KOhm
R2529 332KOhm
U2501A
RTCX1
RTCX2
RTCRST#
INTRUDER#
INTVRMEN
LAN100_SLP
GLAN_CLK
LAN_RSTSYNC
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
GLAN_DOCK#/GPIO13
GLAN_COMPI
GLAN_COMPO
HDA_BIT_CLK
HDA_SYNC
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDOUT
HDA_DOCK_EN#/GPIO33
HDA_DOCK_RST#/GPIO34
SATALED#
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP
SATA_CLKN
SATA_CLKP
SATARBIAS#
SATARBIAS
RTC
LPC
LAN / GLAN
CPU
IHDA
SATA
IDE
FWH0/LAD0
FWH1/LAD1
FWH2/LAD2
FWH3/LAD3
FWH4/LFRAME#
LDRQ0#
LDRQ1#/GPIO23
A20GATE
A20M#
DPRSTP#
DPSLP#
FERR#
CPUPWRGD/GPIO49
IGNNE#
INIT#
INTR
RCIN#
NMI
SMI#
STPCLK#
THRMTRIP#
TP8
DD0
DD1
DD2
DD3
DD4
DD5
DD6
DD7
DD8
DD9
DD10
DD11
DD12
DD13
DD14
DD15
DA0
DA1
DA2
DCS1#
DCS3#
DIOR#
DIOW#
DDACK#
IDEIRQ
IORDY
DDREQ
ICH8-M
+RTCBAT
+3VA
+VCC_RTC
D2501
R2507 1K
BAT2501
BAT54C
C2501 1UF/X7R
Socket P/N:12G17100002C
Battary P/N:076016412032
R2511 56
R2512 0Ohm
R2501 56Ohm
R2502 24.9Ohm 1%
T2506
T2501
T2507
T2516
T2517
T2515
T2514
R2513 33Ohm
R2514 33Ohm
R2515 33Ohm
R2516 33Ohm
R2517 33Ohm
R2518 33Ohm
R2519 33Ohm
R2520 33Ohm
R2528 24.9Ohm
T2509
T2513
T2510
T2511
T2512
SATA HDD <=>
C2505 3900P
C2504 3900P
R2532 10KOhm
R2533 10KOhm
R2531 10KOhm
R2530 10KOhm
T2503
T2505
T2502
T2504
R2525 24.9Ohm
R0.2 --- Item9
LPC_AD0 21,33,34,35
LPC_AD1 21,33,34,35
LPC_AD2 21,33,34,35
LPC_AD3 21,33,34,35
LPC_FRAME# 21,33,34,35
A20GATE 34
H_A20M# 4
H_DPRSTP# 4,9,80
H_DPSLP# 4
H_FERR# 4
H_PWRGD 4
H_IGNNE# 4
H_INIT# 4
H_INTR 4
RCIN# 34
H_NMI 4
H_SMI# 4
H_STPCLK# 4
ICH_THRMTRIP# 6
IDE_PDD0
IDE_PDD1
IDE_PDD2
IDE_PDD3
IDE_PDD4
IDE_PDD5
IDE_PDD6
IDE_PDD7
IDE_PDD8
IDE_PDD9
IDE_PDD10
IDE_PDD11
IDE_PDD12
IDE_PDD13
IDE_PDD14
IDE_PDD15
IDE_PDD[0..15]
IDE_PDA0 23
IDE_PDA1 23
IDE_PDA2 23
IDE_PDCS1# 23
IDE_PDCS3# 23
IDE_PDIOR# 23
IDE_PDIOW# 23
IDE_PDDACK# 23
IRQ14 23
IDE_PIORDY 23
IDE_PDDREQ 23
+3VA +VCCP 17,27,34,37,46,81,93 4,5,6,7,8,9,11,12,28,37,85
<Variant Name>
Title : ICH8-M (1)
ASUSTeK COMPUTER INC
Engineer: <OrgAddr1>
Size Custom
Project Name F9S
Rev 1.1
Date: Tuesday, February 27, 2007
Sheet 25 of 94




U2501C
ICH8-M
SMB
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
SMBCLK
SMBDATA
LINKALERT#
SMLINK0
SMLINK1
RI#
SUS_STAT#/LPCPD#
SYS_RESET#
BMBUSY#/GPIO0
SMBALERT#/GPIO11
STP_PCI#/GPIO15
STP_CPU#/GPIO25
CLKRUN#/GPIO32
WAKE#
SERIRQ
THRM#
VRMPWRGD
TP7
TACH1/GPIO1
TACH2/GPIO6
TACH3/GPIO7
GPIO8
GPIO12
TACH0/GPIO17
GPIO18
GPIO20
SCLOCK/GPIO22
QRT_STATE0/GPIO27
QRT_STATE1/GPIO28
SATACLKREQ#/GPIO35
SLOAD/GPIO38
SDATAOUT0/GPIO39
SDATAOUT1/GPIO48
SPKR
MCH_SYNC#
TP3
SATA0GP/GPIO21
SATA1GP/GPIO19
SATA2GP/GPIO36
SATA3GP/GPIO37
CLK14
CLK48
SUSCLK
SLP_S3#
SLP_S4#
SLP_S5#
S4_STATE#/GPIO26
PWROK
DPRSLPVR/GPIO16
BATLOW#
PWRBTN#
LAN_RST#
RSMRST#
CK_PWRGD
CLPWROK
SLP_M#
CL_CLK0
CL_CLK1
CL_DATA0
CL_DATA1
CL_VREF0
CL_VREF1
CL_RST#
CLGPIO0/GPIO24
CLGPIO1/GPIO10
CLGPIO2/GPIO14
WOL_EN/GPIO9
SMB_CLK_SB
SMB_DAT_SB
LINKALERT#
SMLINK0
SMLINK1
T2721
T2722
SM_LINK0
SM_LINK1
RING#
PM_SUS_STAT#
PM_BMBUSY#
SMB_ALERT#
STP_PCI#
STP_CPU#
PM_CLKRUN#
PCIE_WAKE#
INT_SERIRQ
PM_THRM#
VRM_PWRGD_CLKEN
BT_DET#
BIOS_REC
802_LED_EN
EXTSMI#
KBC_SCI#
WLAN_ON#
BT_LED_EN
BT_ON#
CB_SD#
SATACLKREQ#
PCB_ID1
PCB_ID2
SPKR_ICH
MCH_SYNC#
ICH_TP3
CPPE# DET
CPU_Select_L
EMAIL_LED#
PCB_ID0
CLK_ICH14
CLK_USB48
SUS_CLK
PM_SUSB#
PM_SUSC#
CPPE_EN
ICH8_PWROK
Int.PD
POWER
PM_DPRSLPVR
BAT_LL#
Int.PU
PM_PWRBTN#
PLT_RST#_BUF
PM_RSMRST#_SB
PM_RSMRST#
CLK_PWRGD
MSK_PCIRST
RST#_NEWCARD
R0.2 --- Item10
R1.02---ITEM20
R0.3 --- Item22
R0.3 --- Item16
R1.02---ITEM19
PCB_VID3 : PROJECT CODE
PCB_VID 0 1 2
MB F2S 0 0 0
VRM_PWRGD
Q2702
Q2703
Q2704
H2N7002
2N7002
Clock Generator
DDR2 SO-DIMM
Mimi Card
New Card
<Variant Name>
Title : ICH8-M (3)
ASUSTeK COMPUTER INC
Engineer: <OrgAddr1>
Size Custom
Project Name F9S
Rev 1.1
Date: Tuesday, February 27, 2007
Sheet 27 of 94


U2501E
ICH8-M
U2501F
ICH8-M
R2802
100Ohm
D2801
BAT54A
D2802
BAT54A
R2803
10Ohm
R0.3 --- Item23
20mA
L2804
80Ohm/100Mhz
CE2801
220UF/2V
L2801
120Ohm/100Mhz
L2802
120Ohm/100Mhz
JP2801
2MM_OPEN_5MIL
L2803
120Ohm/100Mhz
Irat=600mA
R0.4 --- Item4
1.13A
23mA
50mA
1mA
442mA
657mA
47mA
1.56A
10mA
23mA
177mA
Title : ICH8-M (4)
ASUSTeK COMPUTER INC
Engineer: <OrgAddr1>
Project Name F9S
Size Custom
Rev 1.1
Date: Thursday, February 15, 2007
Sheet 28 of 94



<Variant Name>

Title :	LAN RTL8111B
ASUSTeK COMPUTER INC	Engineer:
Size: Custom	Project Name: F9S
Rev: 1.1	
Date: Tuesday, February 27, 2007	Sheet 29 of 94

ASUSTek COMPUTER INC	Title :		
	Engineer:		
Size: Custom	Project Name: F9S		Rev: 1.1
Date: Thursday, February 08, 2007	Sheet 30 of 94		

ASUSTek COMPUTER INC	Title : EMPTY		
	Engineer:		
Size: Custom	Project Name: F9S		Rev: 1.1
Date: Monday, February 05, 2007	Sheet 31 of 94		

<Variant Name>

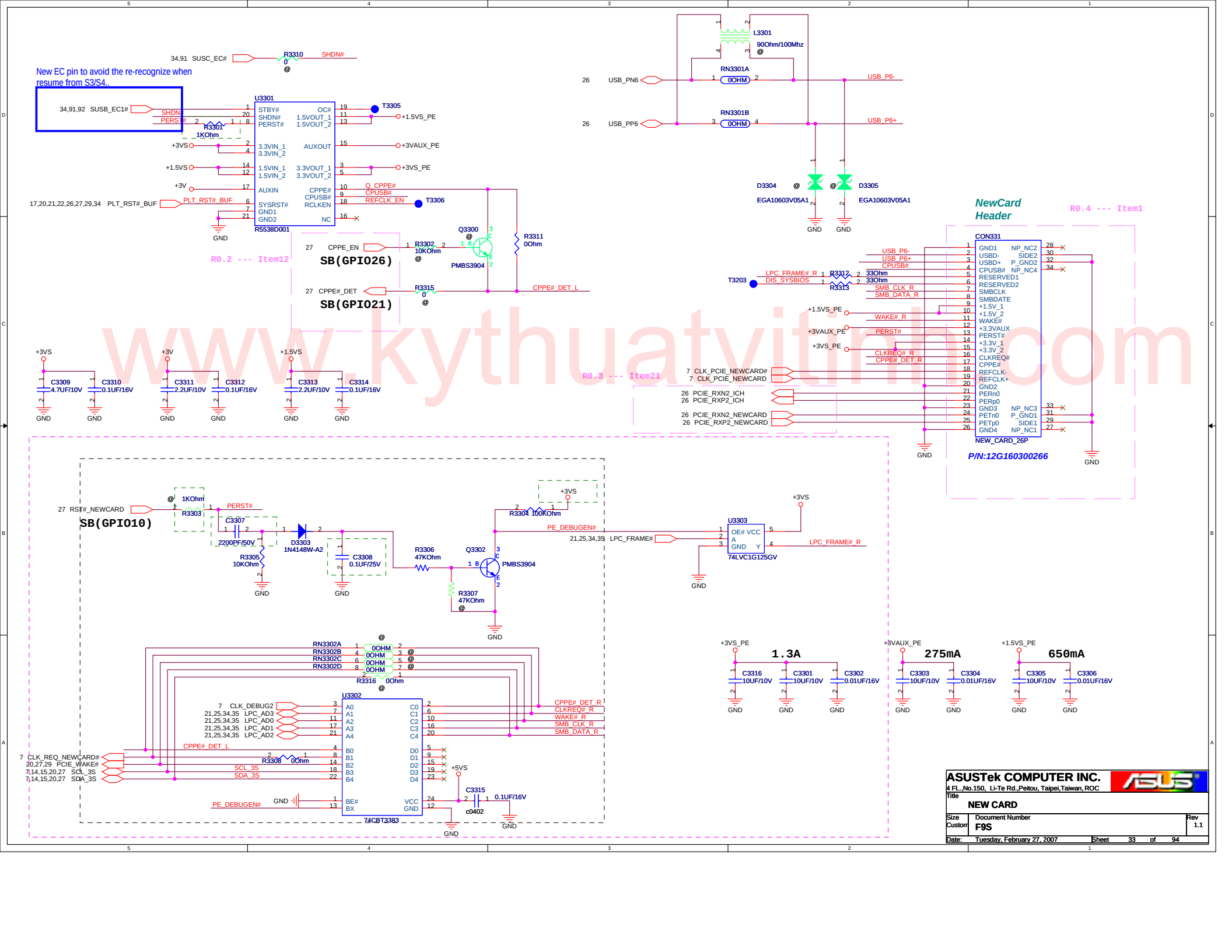
Title : EMPTY

ASUSTeK COMPUTER INC

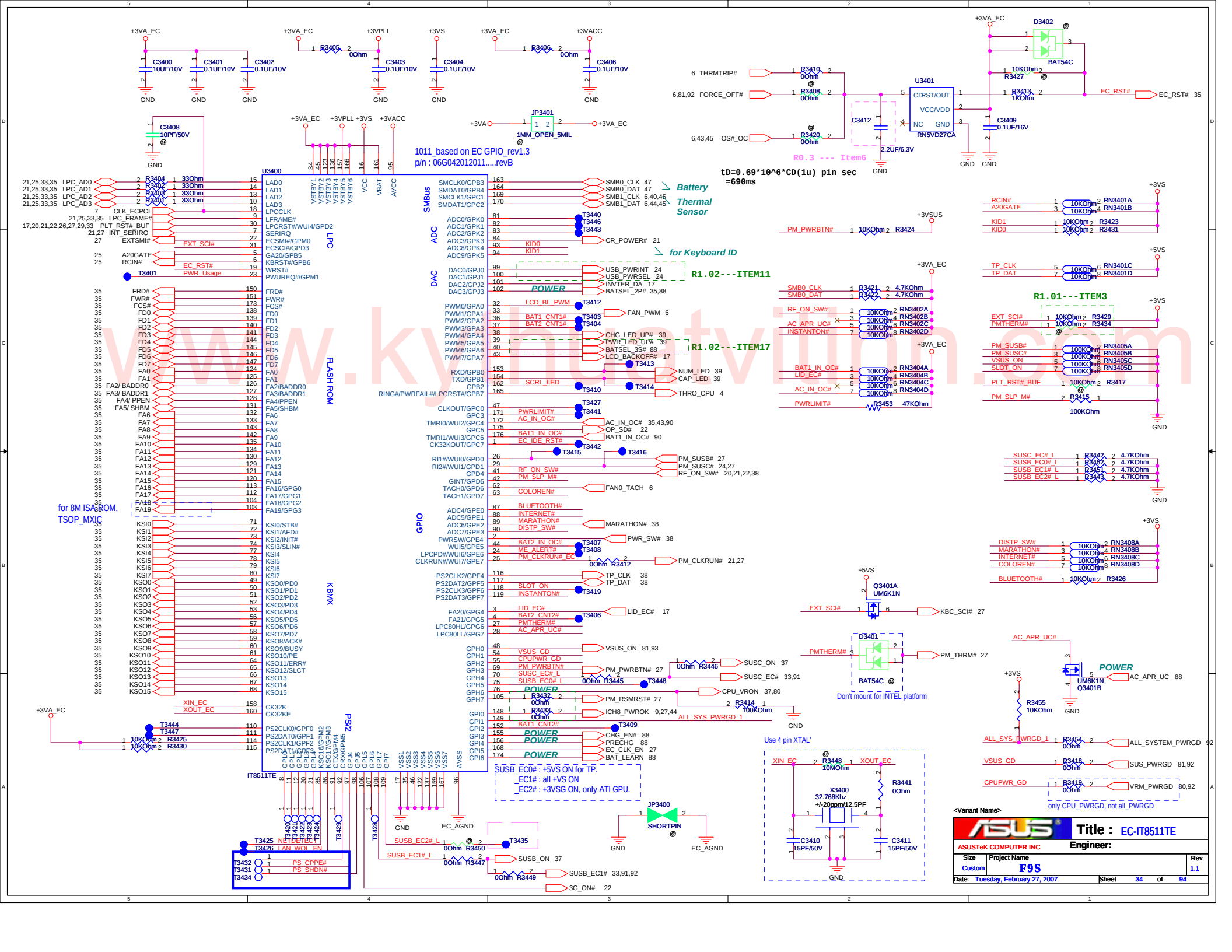
Engineer:

Size	Project Name	Rev
Custom	F9S	1.1

Date: Monday, February 05, 2007 Sheet 32 of 94



ASUSTek COMPUTER INC.		
4 FL.,No.150, Li-Te Rd.,Peitou, Taipei,Taiwan, ROC		
Title: NEW CARD		
Size: Custom	Document Number: F9S	Rev: 1.1
Date: Tuesday, February 27, 2007	Sheet 33 of 94	


1011_based on EC GPIO_rev1.3
p/n : 06G042012011.....revB
U3400
IT8511TE
LPC
FLASH ROM
KBMX
PS2
SMBus
ADC
DAC
GPIO
Battery
Thermal Sensor
for Keyboard ID
POWER
R1.02---ITEM11
R1.02---ITEM17
R1.01---ITEM3
R0.3 --- Item6
tD=0.69*10^6*CD(1u) pin sec
=690ms
U3401
RN5VD27CA
BAT54C
Q3401A
UM6K1N
Q3401B
D3401
JP3401
1MM_OPEN_5MIL
JP3400
SHORTPIN
X3400
32.768Khz
+/-20ppm/12.5PF
for 8M ISA ROM,
TSOP_MXIC
Don't mount for INTEL platform
Use 4 pin XTAL'
SUSB_EC0# : +5VS ON for TP.
_EC1# : all +VS ON
_EC2# : +3VSG ON, only ATI GPU.
only CPU_PWRGD, not all_PWRGD
<Variant Name>
Title : EC-IT8511TE
ASUSTeK COMPUTER INC
Engineer:
Size Custom
Project Name F9S
Rev 1.1
Date: Tuesday, February 27, 2007
Sheet 34 of 94

ISA ROM_TSOP

EC Hardware Strapping

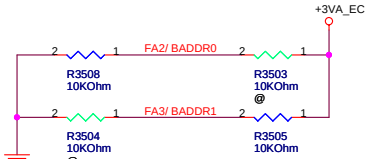
FA2/ BADDR0 & FA3/ BADDR1

00: PNPCNG Access Register Pair Are 002Eh and 002Fh

10: PNPCNG Access Register Pair Are 004Eh and 004Fh

01: PNPCNG Access Register Pair Are Determined by EC Domain Registers SWCBALR and SWCBAHR.

11: Reserved

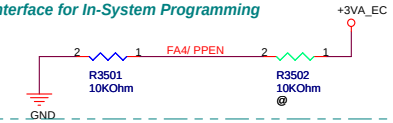


Note: Sampled at VSTBY Power Up Reset

FA4/ PPEN

0: Normal

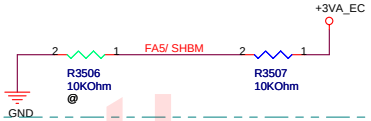
1: KBS Interface Pins Are Switched to Parallel Port Interface for In-System Programming



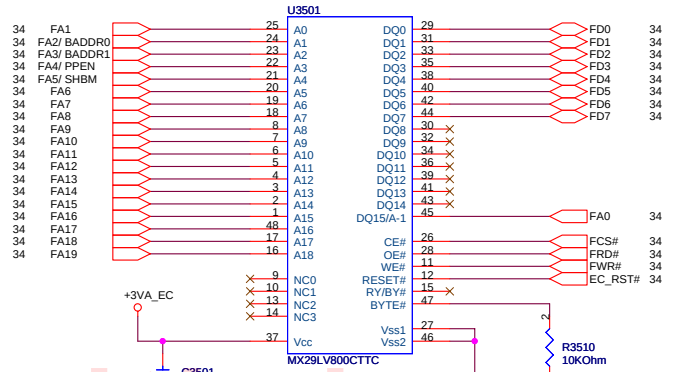
FA5/ SHBM

0: Disable Shared Memory with Host BIOS

1: Enable Shared Memory with Host BIOS



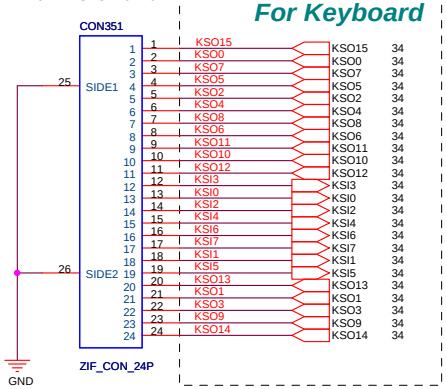
8M TSOP _ MXIC



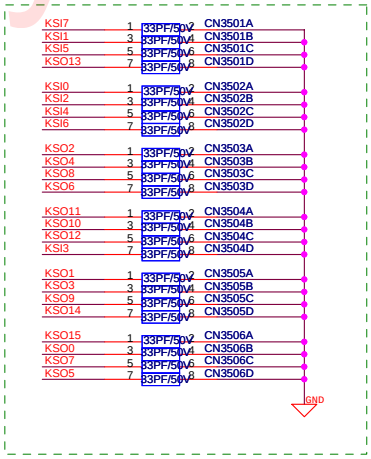
ISA ROM
P/N:05G001204043

For Keyboard

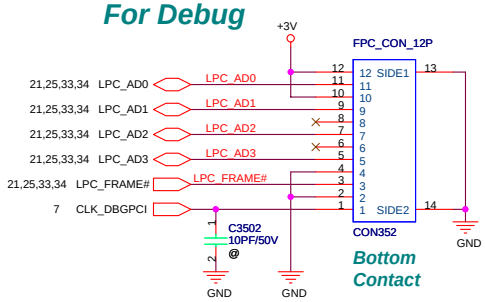
P/N:12G182402404



R1.3---ITEM38



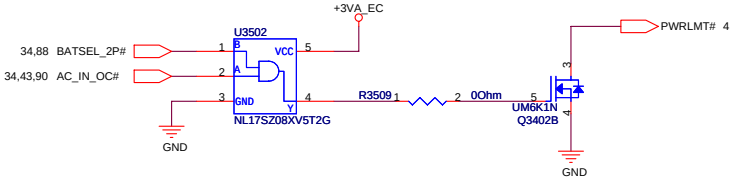
For Debug



Bottom Contact

R1.03---ITEM28

PWRLMT Circuit: For Battery 1P



<Variant Name>

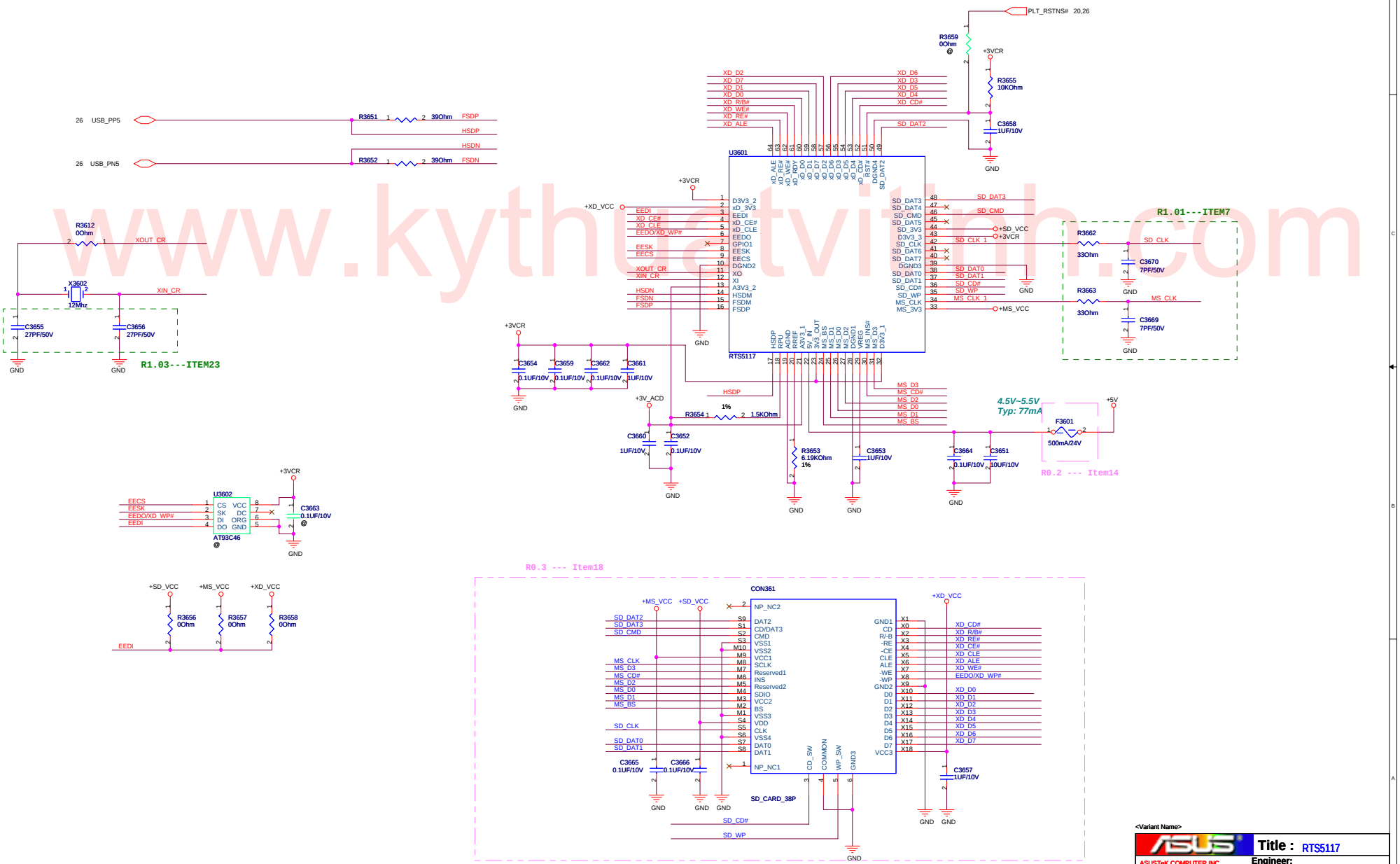
ASUSTeK COMPUTER INC

Title : ISA_ROM&KB conn

Engineer:

Size	Project Name	Rev
Custom	F9S	1.1

Date: Tuesday, February 27, 2007 Sheet 35 of 94



<Variant Name>

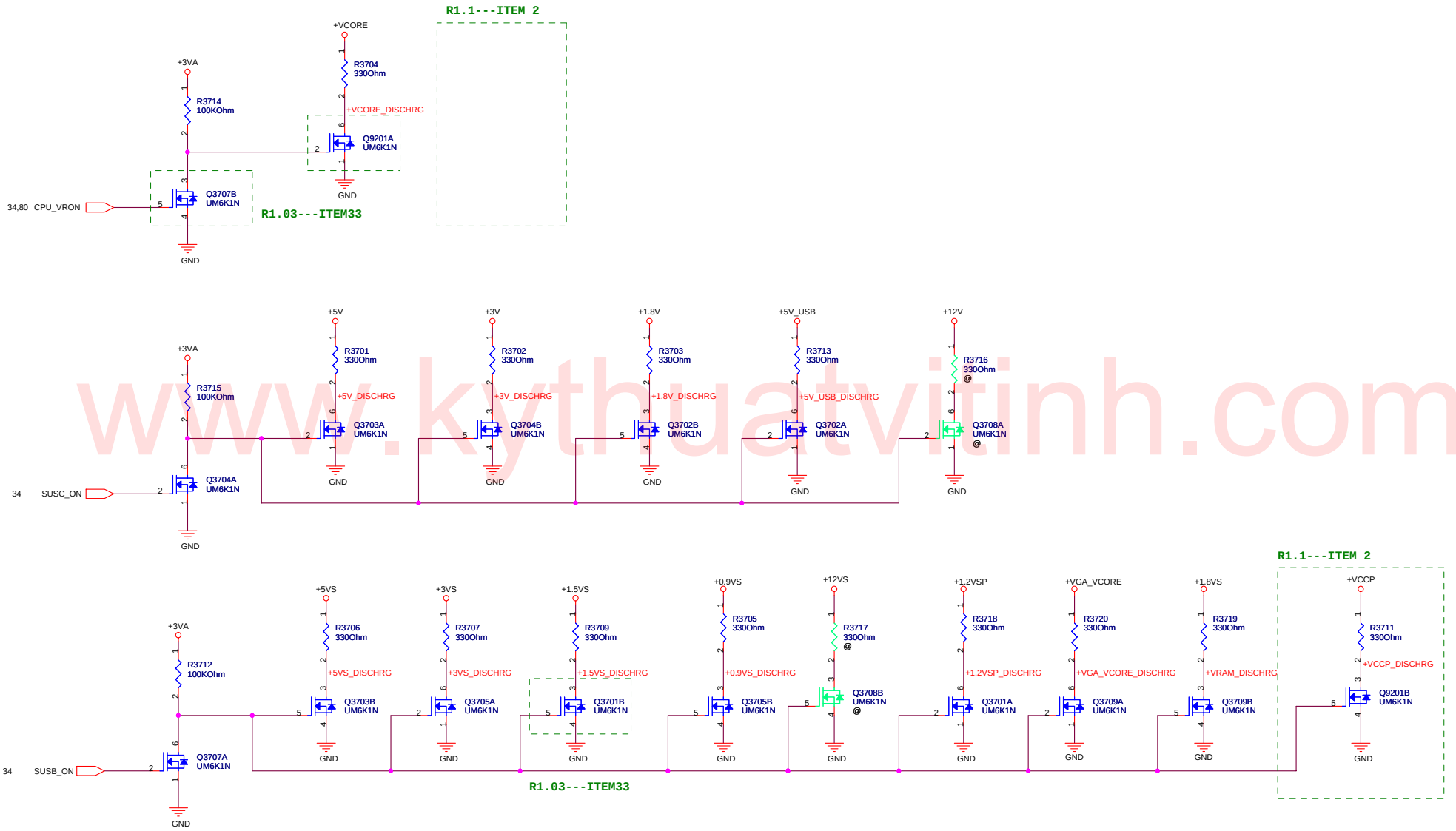
Title : RTS5117

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
C	F9S	1.1

Date: Tuesday, March 06, 2007 Sheet 36 of 94



<Variant Name>

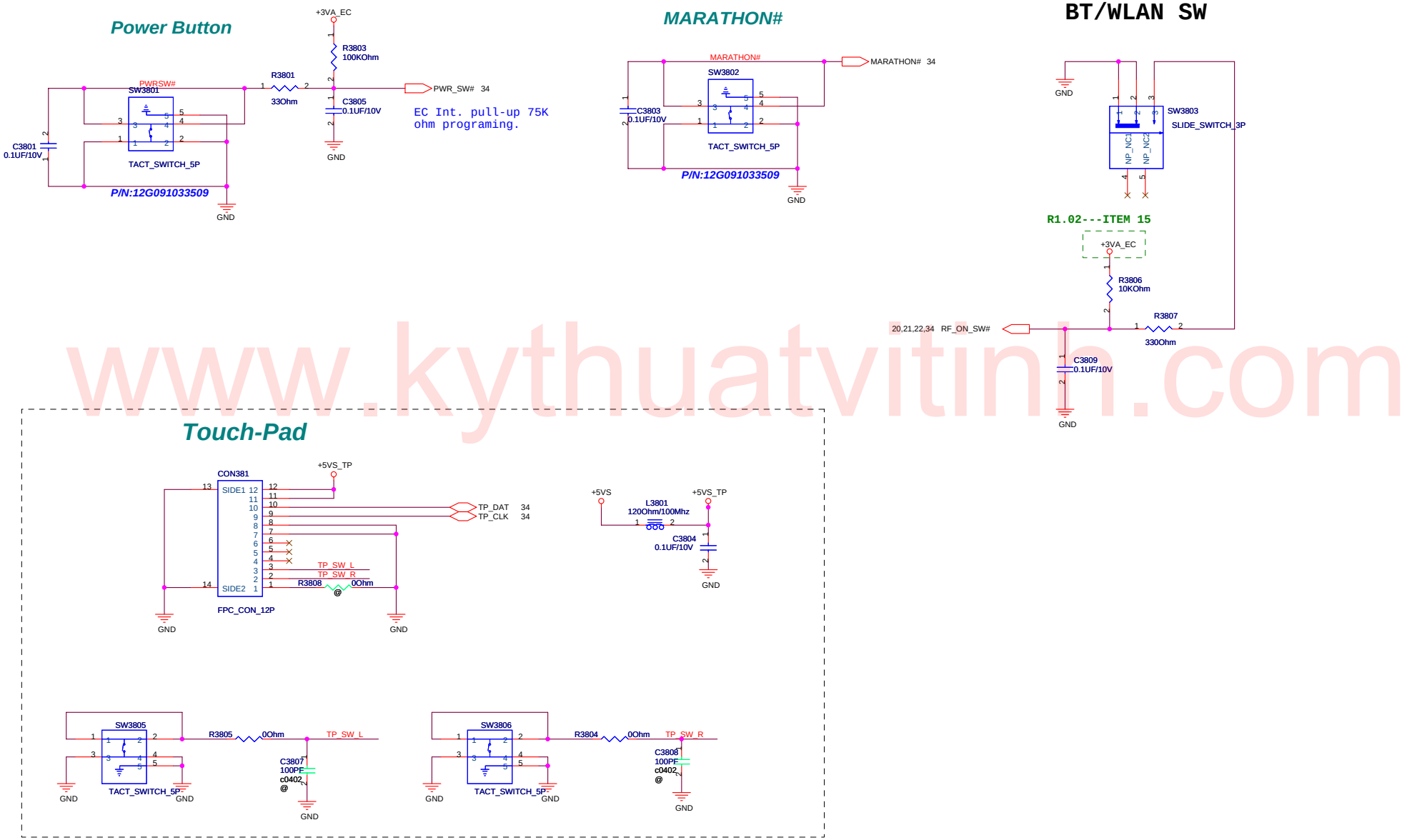
ASUSTeK COMPUTER INC

Title : DISCHARGE

Engineer:

Size	Project Name	Rev
Custom	F9S	1.1

Date: Tuesday, February 27, 2007 Sheet 37 of 94



<Variant Name>

ASUSTeK COMPUTER INC

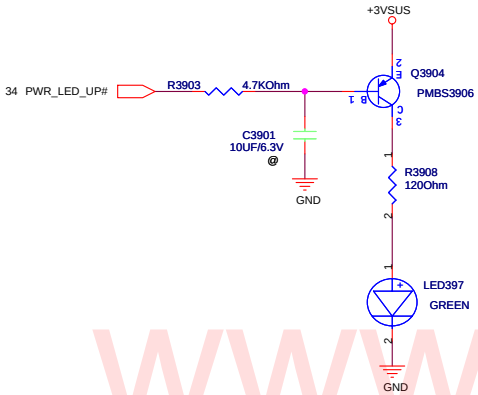
Title : KEY & LED

Engineer:

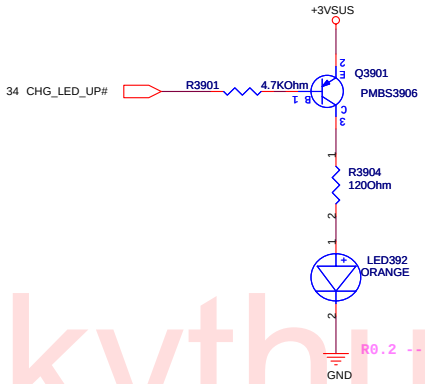
Size	Project Name	Rev
Custom	F9S	1.1

Date: Tuesday, February 27, 2007 Sheet 38 of 94

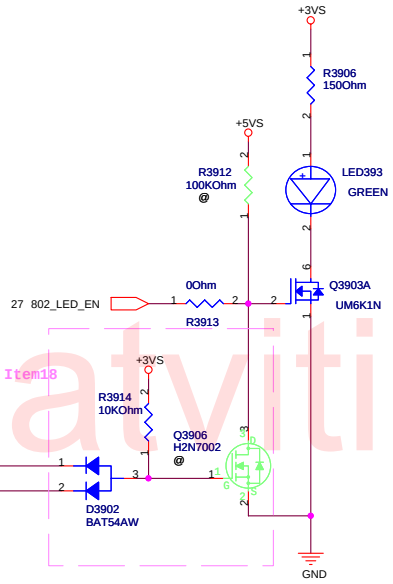
PWR LED



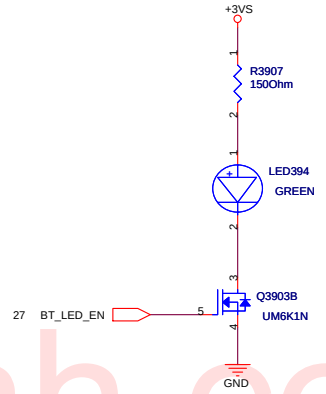
BATTERY LED



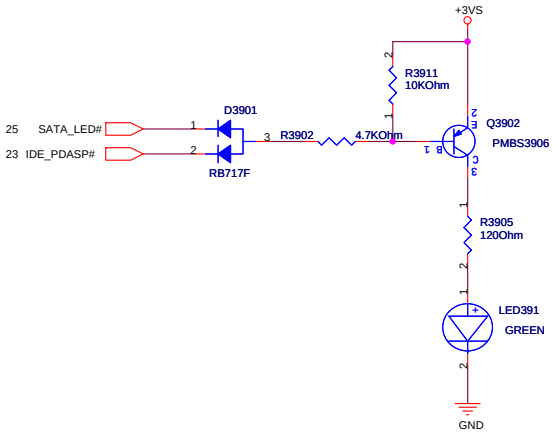
WireLess LED



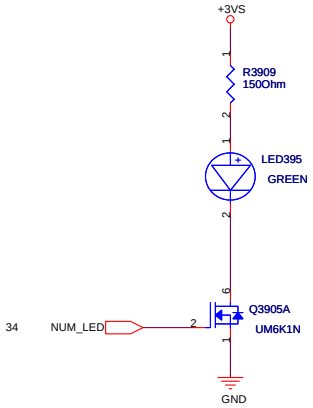
BT LED



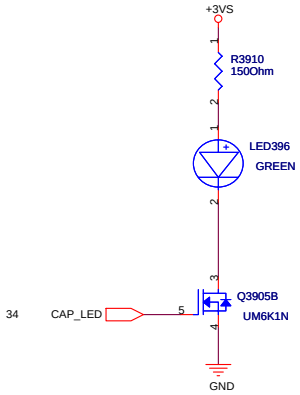
SATA/IDE LED



Num Lock



Cap. Lock



<Variant Name>

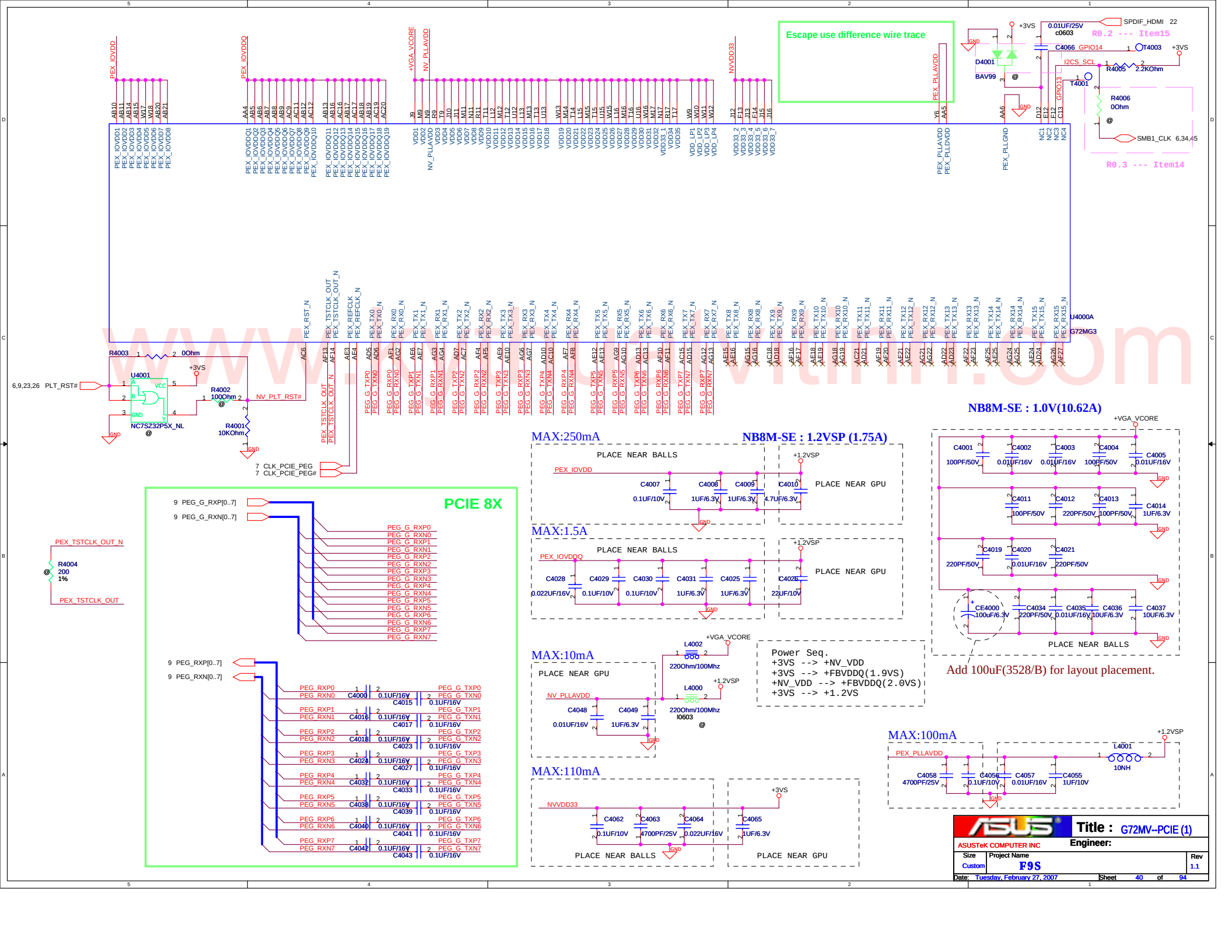
ASUSTeK COMPUTER INC

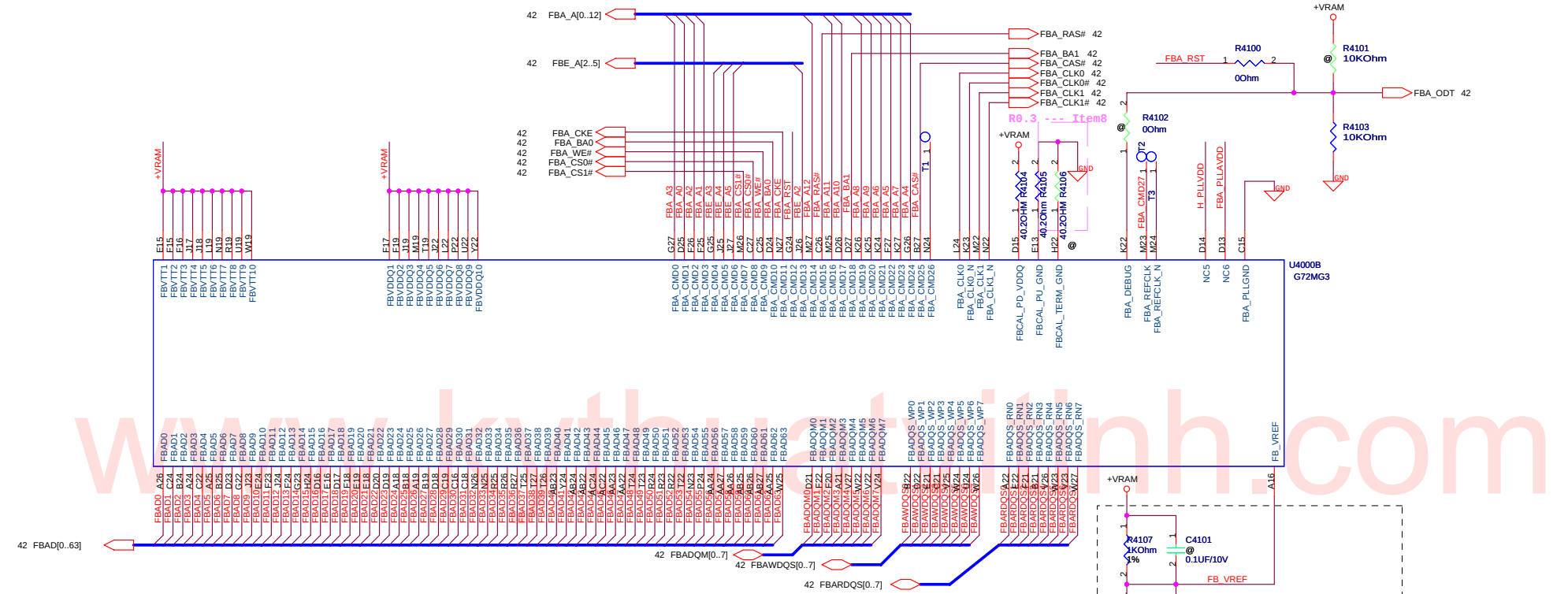
Title : LEDs

Engineer:

Size	Project Name	Rev
Custom	F9S	1.1

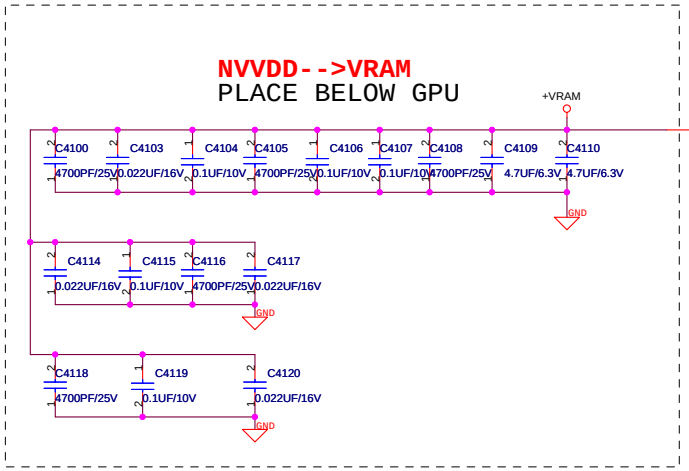
Date: Tuesday, February 27, 2007 Sheet 39 of 94

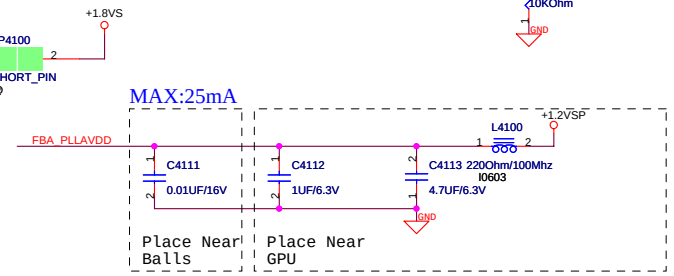

Escape use difference wire trace
PCIE 8X
NB8M-SE : 1.0V(10.62A)
NB8M-SE : 1.2VSP (1.75A)
MAX:250mA
MAX:1.5A
MAX:10mA
MAX:110mA
MAX:100mA
Power Seq.
+3VS --> +NV_VDD
+3VS --> +FBVDDQ(1.9VS)
+NV_VDD --> +FBVDDQ(2.0VS)
+3VS --> +1.2VS
Add 100uF(3528/B) for layout placement.
PLACE NEAR BALLS
PLACE NEAR GPU
R0.2 --- Item15
R0.3 --- Item14
Title : G72MV--PCIE (1)
ASUSTeK COMPUTER INC
Engineer:
Project Name F9S
Rev 1.1
Date: Tuesday, February 27, 2007
Sheet 40 of 94

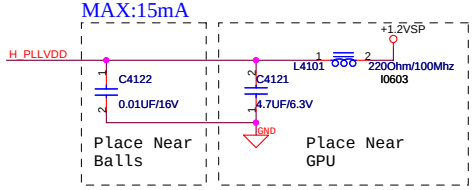


NB8M:MAX:2.47A
G72M:MAX:2.075A
G72M-V:MAX:1A

GDDR2 16x16 FBVDDQ 1.8V 84PIN

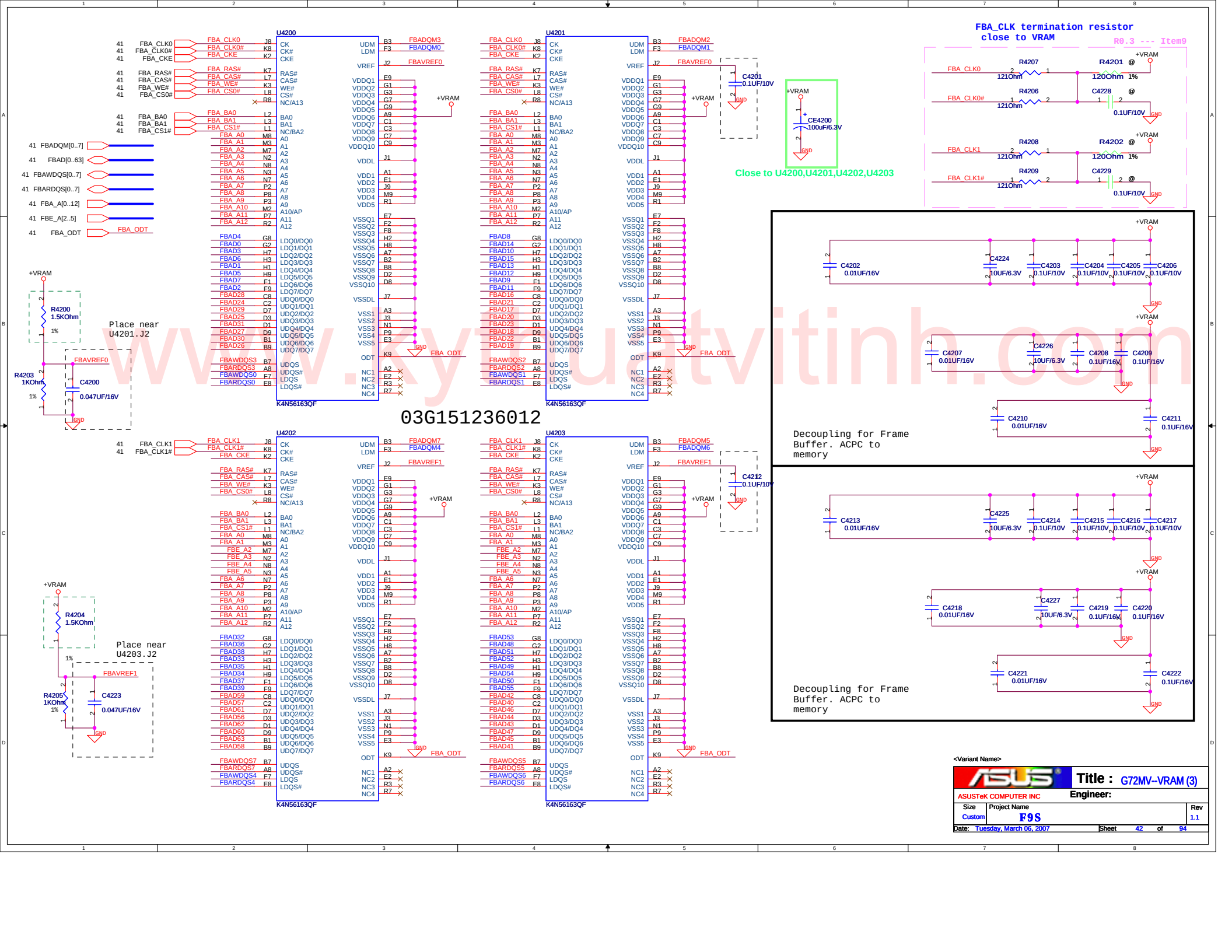


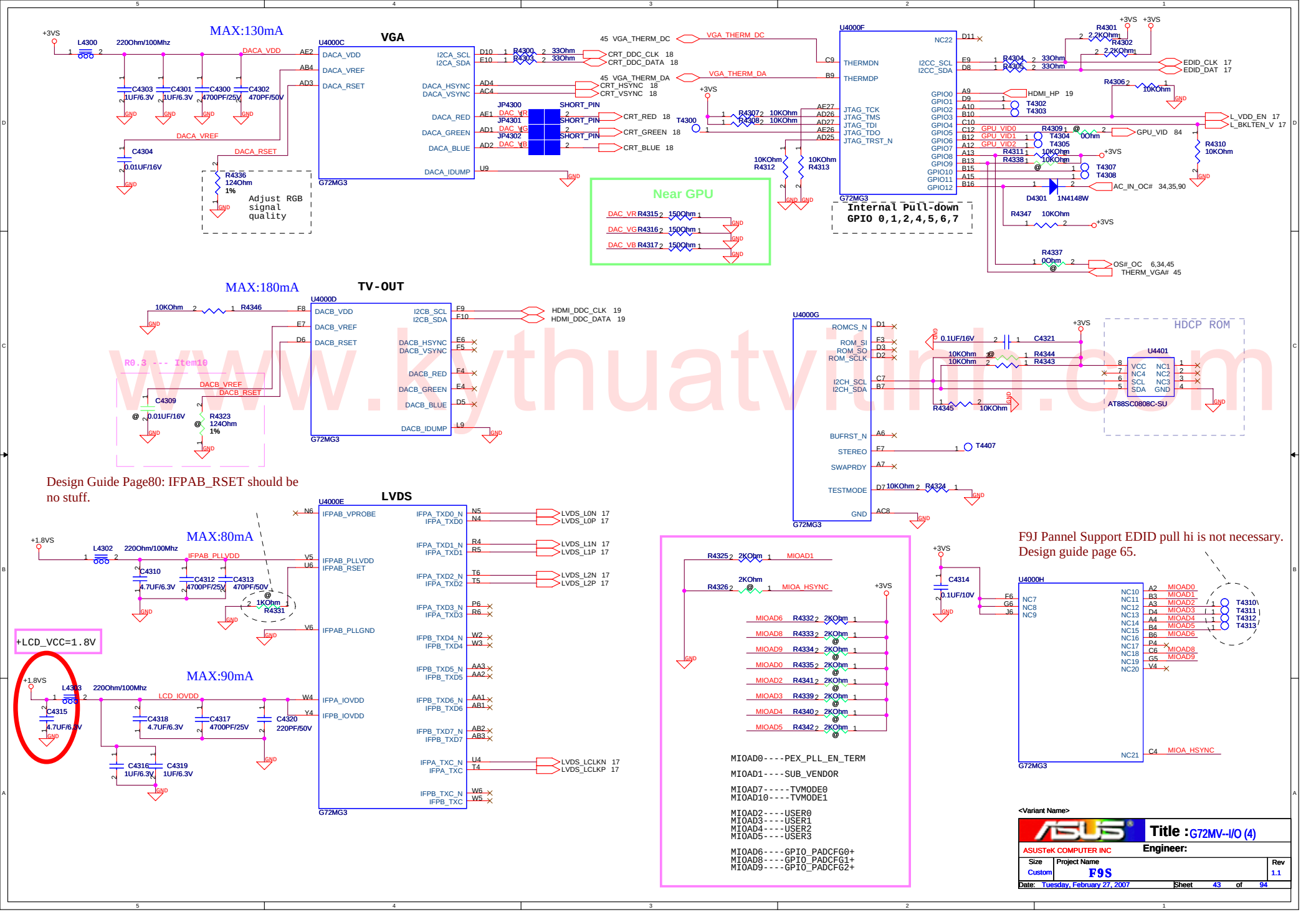


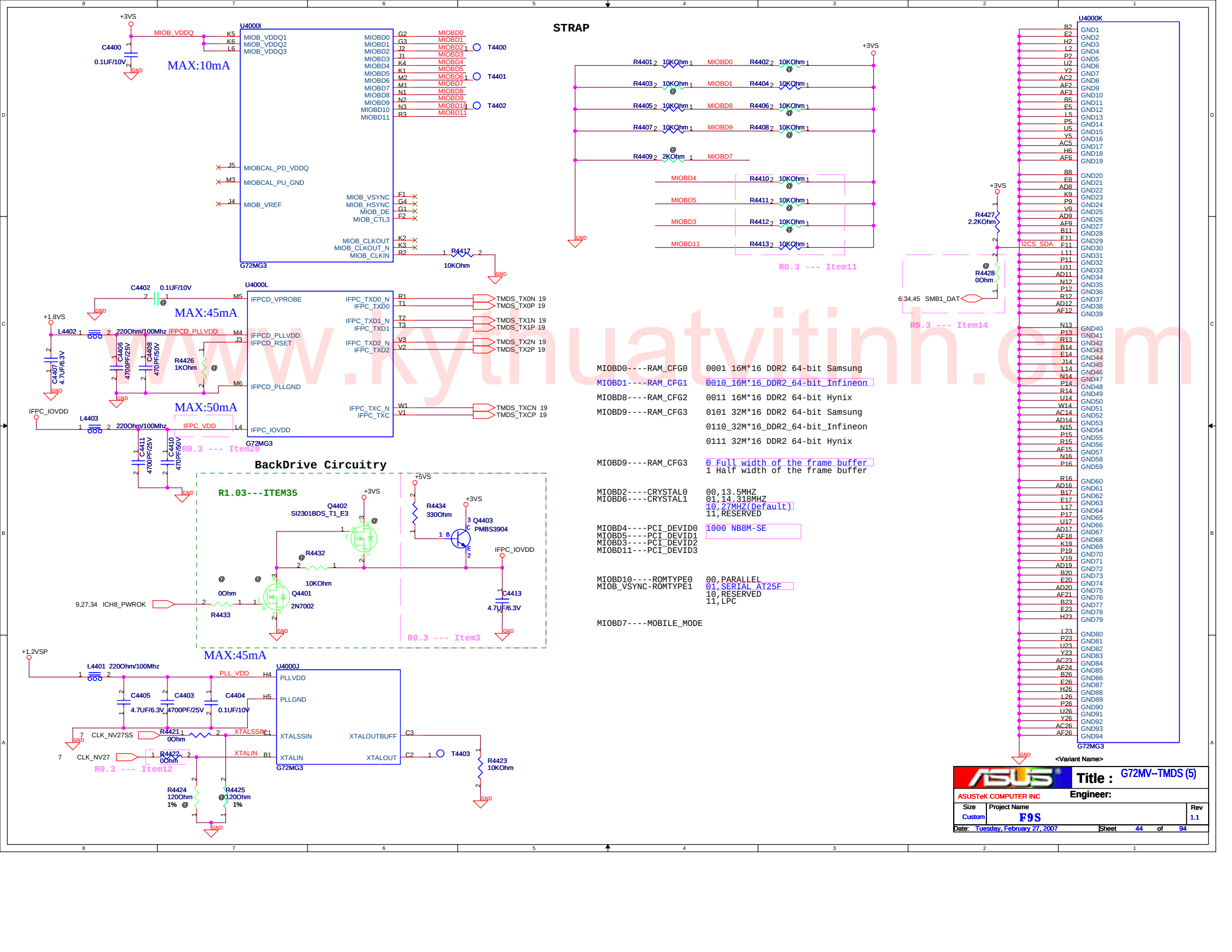


<Variant Name>

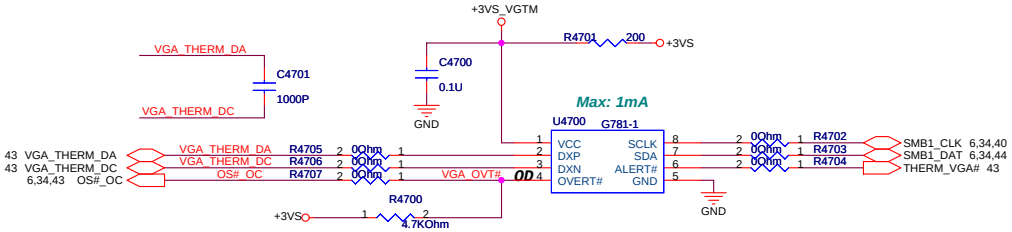
ASUSTeK COMPUTER INC	Title : G72MV-FB (2)	
	Engineer:	
Size: Custom	Project Name: F9S	Rev: 1.1
Date: Tuesday, February 27, 2007	Sheet 41 of 94	


FBA_CLK termination resistor close to VRAM
R0.3 --- Item9
Close to U4200,U4201,U4202,U4203
Place near U4201.J2
Place near U4203.J2
Decoupling for Frame Buffer. ACPC to memory
Decoupling for Frame Buffer. ACPC to memory
03G151236012
www.kythuatvitinh.com
U4200
U4201
U4202
U4203
K4N56163QF
+VRAM
GND
FBA_ODT
FBAVREF0
FBAVREF1
<Variant Name>
ASUSTeK COMPUTER INC
Engineer:
Title : G72MV--VRAM (3)
Size Custom
Project Name F9S
Rev 1.1
Date: Tuesday, March 06, 2007
Sheet 42 of 94





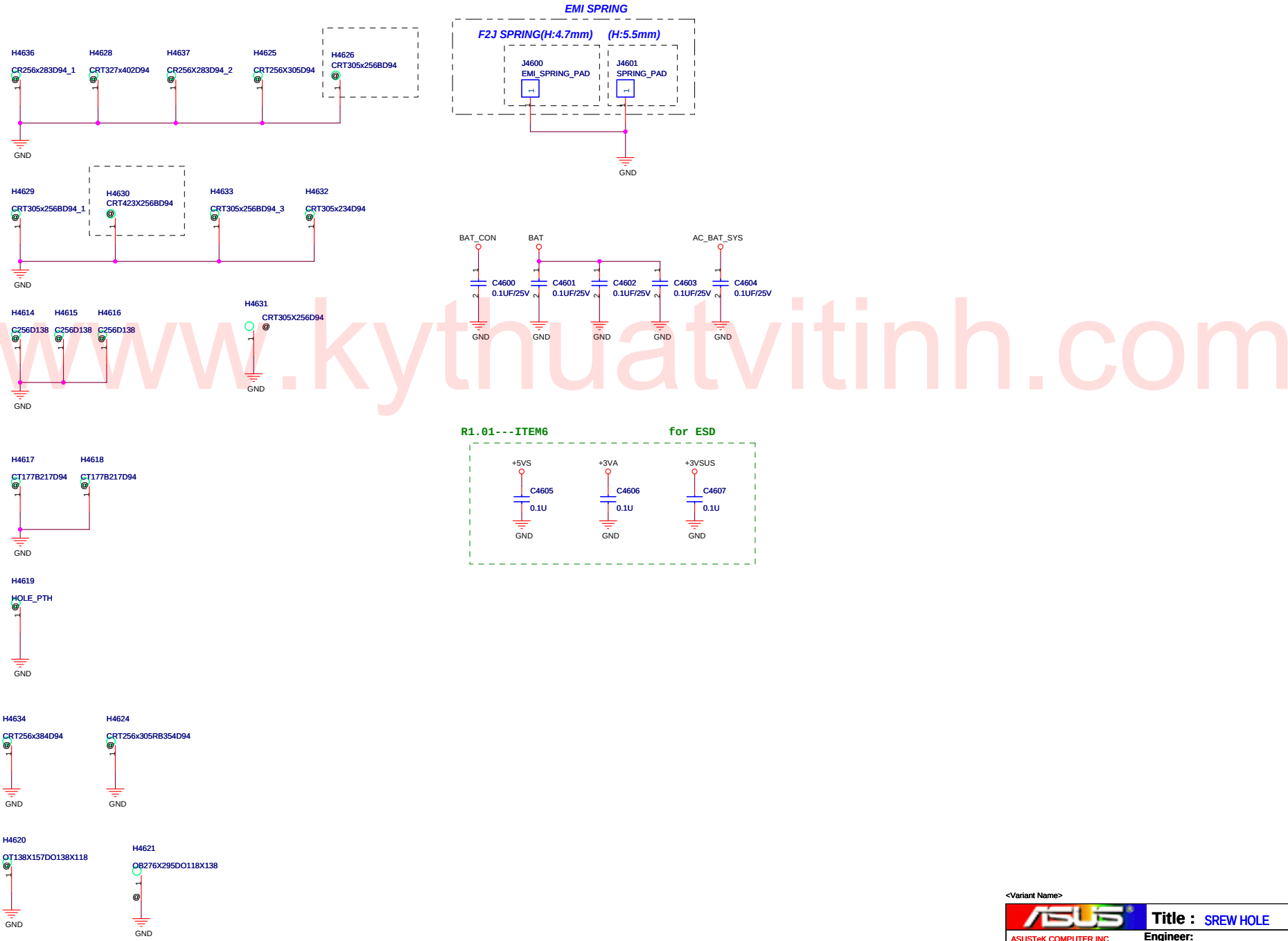
Slave Address:9A



For frame buffer address/command lines those external pull up resistor can be removed for easy layout from Nvidia FAE

<Variant Name>

ASUSTeK COMPUTER INC	Title G72MV--VRAM_TERM	
	Engineer:	
Size: Custom	Project Name: F9S	Rev: 1.1
Date: Tuesday, February 27, 2007	Sheet 45 of 94	



<Variant Name>

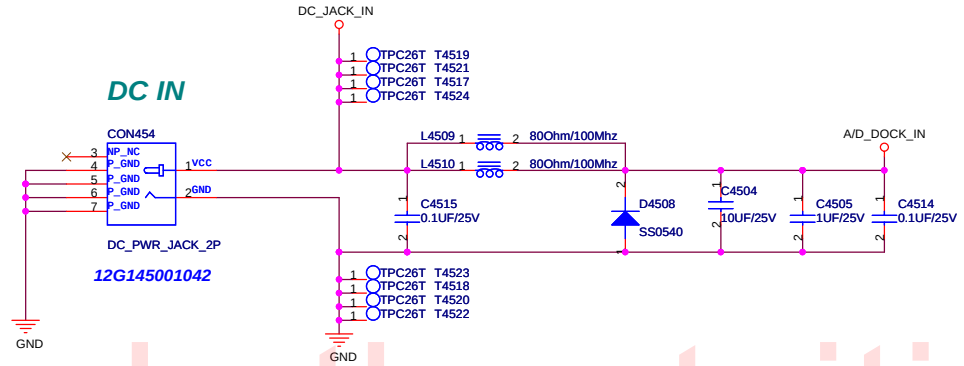
Title : SREW HOLE

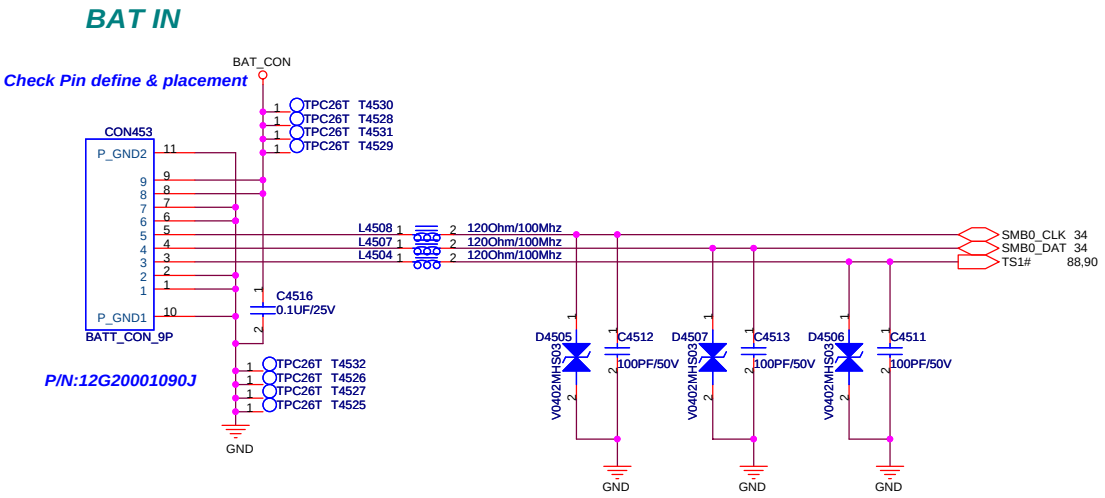
ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	F9S	1.1

Date: Monday, February 05, 2007 Sheet 46 of 94





<Variant Name>

ASUSTeK COMPUTER INC

Title : G72M-Terminator

Engineer:

Size	Project Name	Rev
Custom	F9S	1.1

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F9S SR_1128(R0.1---->R0.2)

(1)Delete R0930,R0931 to follow Intel spec.---page9
(2)Mount R1301 for DMI x2 ---page13
(3)Modify netname USBP1 to USBP2 ---page17
(4)Modify U1803,U1804 to N/A and R1817,R1818 connect to CRT_VSYNC,CRT_HSYNC ---page18
(5)change TMDS pull high from +3VS to IFPC_IOVDD ---page19
(6)Modify netname SUS_STAT# to PM_SUS_STAT# ---page21
(7)Add signal for 1G LAN, ---page22
Delete R2201,R2202,Q2201,Q2202 and Modify netname ----- page22
(8)Modify netname to IRQ14 ---page23
(9)Delete E-SATA signal and add R2532,R2533 ---page25
(10)Add test point T2717,T2719 ---page27
(11)change 10/100 LAN to 10/100/1000 LAN(RTL811B) ---page29
(12)Modify debug circuit ---page33
(13)Modify single netname ---page34
(14)Modify F3601 to 0.5A ---page36
(15)Add C4066 ,D4001 for SPDIF_HDMI ---page40
(16)Add R4434 to N/A ---page44
(17)Add R0785,R0786,R0787 to follow Intel for CPU_BSEL ---page7
(18)Add D3902,R3914,Q3906,R3912 for WLAN,WWAN LED(reserve) ---page39
(19)Delete R0765,R0766,R0781,R0782,R0761,R0763 ---page7
(20)Change CON2201 pin9 from +1.8V_LAN to GND---page22

F9S SR_1130(R0.2---->R0.3)

(1)Delete CN1500 and add C1515~C1518---page15
(2)DMI change to 2X---page9,26
(3)Modify backdrive circuitry ---page44
(4)Modify F1701 from 0.2A to 0.5A ---page17
(5)Add R1702,C1714,Q1703 to reserve it for LCD power---page17
(6)Delete R0719,R0721,R0723---page7
(7)Modify L2902,L2903,L2904 size and add L2905,L2906 ---page29
(8)R4105 change to 40ohm instead of 30ohm,and R4106 to N/A ---page41
(9)Reserve FBA_CLKx clock terminator for NB8M-SE memory tuning---page42
(10)Due to without TV function,C4309 and R4323 to N/A---page43
(11)PCI_DEVICEID please set to "1000" for NB8M-SE--page44
(12)For NB8M-SE ext. 27Mhz can connect directly without level shift, R4422 use 0 ohm is ok--page44
(13)For frame buffer address/command lines those external pull up resistor can be removed for easy layout.-page45
(14)I2CS_SCL and I2C_SDA to EC to access NB8M-SE internal thermal sensor---page40,44
(15)Delete power limit circuit due to EC change to IT8511TE--page35
(16)BT_DET# connect 3Vs to avoid the leakage-----Page27
(17)Change the ODD CON(CON232) from 12G16121050P to 12G161240501 for ME request. (Board lock hole:1.8mm; 3.0H)---Page23
(18)CON361 change from 12G340003800 to 12G340003810 to improve the yield rate.--Page36
(19)Add R1210,R1211 connect to GND for intel recommendation Rev1.5----page12
(20)To modify duplicated netname from IFPC_IOVDD to IFPC_VDD ---page44
(21)To modify duplicated netname of PCIE signal ---page29,33
(22)Change RN2700 to 0402 size and no mount R2756 for Intel recommendation---page27
(23)Change C2812,R2803 size from 0805 to 0603 for layout request.---page28
(24)DDR SWAP for layout request---page14,15
(25)Delete R3708,Q3710 due to +2.5VS power no use---page37
(26)Add Q1802 to avoid current leakage from CRT device---page18

F9S SR_1130(R0.3---->R0.4 same as R1.0)

(1)Change Newcard header H=3.2 and card ejector for F9S/E---page33
(2)C3658/C3655 change from 15pF to 18pF for card reader crystal adjustment.---page36
(3)No Mount R3806,to avoid +3VA_EC leakage to +3Vs--page38
(4)Add C2843,C2844 connect to GND for intel recommendation--page28
(5)Change C06XX from 10U to 22U for intel recommendation---page06
(6)Change C3412 from 1U to 2.2U and delay EC_RST#---page34
(7)R2308 reserve high change to pull low for intel recommendation. ---page23
(8)Add R2306 33ohm for checklist ---page24
(9)Add Q1901,R1928,R1929 to avoid leakage for HDMI DDC clk, and Data---page19
(10)Add R3660,R3661,C3667,C3668(SD and MS CLK) for EMI request ---page36

F9S ER_0122(R1.0---->R1.01)

(1)Add C2201 ~ C2208 for EMI request ---page22
(2)Change +VCCP discharge by SUSB_ON for the correspondence with power enable ----page37
(3)Change RES. 4R8P RN3403 to single RES R3429, R3434 for uncertain PMTHERM# leakag ---page34
(4)Delete D1901 and add Q1902 and R1926,R1927 change to 1.8K ohm for HDMI spec. ---page19
(5)+5VS_CRT change to +5VS_HDMI_CRT and D1806 to DNI ---page18
(6)Add C4605,C4606,C4607 0.1uf cap. for ESD ---page46
(7)R3660,R3661 mount 33 0hm and C3667,C3668 mount 10p for EMI issue---page36
(8)Power change to AC_BAT_SYS_INV for layout improve---page17
(9)Change D2401 ,D2400 part from RSB6.8S to EGA10603V05A1---page24

F9S ER_0125(R1.01---->R1.02)

(10)Add C2108 0.1uf cap. for ESD---page21
(11)Add USB Port Charging Function on S4/ S5---page24
(12))Add OS#_OC to FAN---page6
(13)Change R0402 from 68 ohm to 1k ohm 1% because it can fixes the PROCHOT# failure when driven by thermal sensor on the CRB.----page4
(14)Delete C0401 for intel recommend.---page4
(15)Change WLAN SW pull up to +3VA_EC for leakage prevention.--page38
(16)Del D0701,D0702 and add R785,R786 because there is no leakage at S3/S4 or card insertion.---page7
(17)Power add BATSEL_3S# connect to EC.---page34
(18)DNI useless U2603 and C2606.---page26
(19)Reserve a RES R2754 to pull up PM_RSMRST# to +3VSUS.---page27
(20)Change net name PM_RSMRST# to PM_RSMRST#_SB to pull up +3VSUS & add D2701 for leakage prevention.---page27

F9S ER_0126(R1.02---->R1.03 same as R1.1)

(21)Add PLT_RST#_BUF for Sierra card moderm reset signal MDL_RESET#.---page22
(22)Change C2500,C2502 from 22pF to 15pF to meet XTAL requirement---page25
(23)C3656/C3655 change from 18pF to 27pF to meet XTAL requirement---page36
(24)Change R0712 from 220 ohm to 270 ohm for clock signal quality improvement.--page07
(25)Change L1811,L1812,L1813 from BEAD 120ohm to 82nH and C1832,C1834,C1836 from 22p to 10p for CRT signal quality---page18
(26)Change Q2405,Q2407 2N7002 to UM6K1N ---page24
(27)Add R2409,R2410 to reserve +5VSUS for SN74CBTD3306 5V power. ---page24
(28)PWRLMT Circuit: For Battery 1P ---page35
(29)SWAP +3V and +3VS power for 3G requirement ---page22
(30)Add C0719,C0721 for 3G requirement ---page07
(31)Mount L1709 common mode choke for 3G requirement---page17
(32)Add C1715,C1716 for 3G requirement---page17
(33)To combine UM6K1N for cost down :delete Q3706,Q9202,Q9203---page37
(34)R1705 from 100 ohm change to 390 ohm for LCD power off sequence---page17
(35)Mount Q4403 and remove Q4402,Q4401,R4432,R4433 for cost down---page44

F9S ER_0207(R1.1---->R1.2)

(36)LVDS conn. pin modification for LVDS coxal cable---page17

F9S ER_0215(R1.2---->R1.3)

(37)Power team modify +1.5VS power rating to 3.5A ---page82
(38)Add CN3501~CN3506 for 3G requirement---page35
(39)Change CLK_TPMPCI R0707 from 33 ohm to 27 ohm and mount C0725(10p) to meet edge rate spec---page36

ASUSTeK COMPUTER INC	Title : History(1)	
	Engineer:	
Size: Custom	Project Name: F9S	Rev: 1.1
Date: Thursday, March 01, 2007	Sheet 48 of 94	

F9S ER_0122(R1.0---->R1.01 same as R1.1)---------POWER

change list:

1. Delete R8046.
2. Change C8004(DNI) to U8000 pin8.
3. Change C8032 to U8000 pin18.
4. Add test point T8037~T8042.
5. For power sequency, change R8400 from 0 to 20K ohm.
6. For OCP adjust, change R8407 from 200K to 30K ohm.
7. For output voltage adjust, change R8406 from 20K to 4.22K, change R8409 from 100K to 20K ohm.
8. To Increase the saturation crrent of L8400, change L8400 from 09G02X103022 to 09G02X103U00.
9. DNI Q8404 and R8408.
10. Delete Q8505 and Q8501.
11. Change L8500 from 0.56uH to 1uH.
12. For OCP adjust, change R8508 from 100K to 51K.
13. For PWM oscillation issue, change output capacitor to 150uF/2V(ESR=18m ohm) *2.
14. For power sequency, change R8504 from 0 to 120K, change C8504 from DNI to 0.1uF, change C8515 from 0.033uF to 0.1uF.
15. Add JP8805 for layout improve.
16. Add 3S/4S selector circuit(DNI).
17. Add U9001 colay to U9000.
18. For power sequency, change R9108 and R9107 to 47K, change R9109 and R9110 to 22K, Delete R9106 and R9112.
19. Change Schematic_Part at Q8000,Q8001,Q8002,Q8003,Q8004 Q8005,Q8006,Q8007,Q8300,Q8301,Q8401,Q8403.
20. Change L8101 from 3.3uH/CYNTEC to 3.8uH/SUMIDA.
21. Change R8120 from 21K to 20K for OCP adjust.
22. For spec. change.Chagne Q8004 from SI4392 to SI4800, Change Q8006 from SI4336to SI4800, Change R8524 from 30K to 174K, Change L8500 from 1uH/18A to 1.8uH/9A. DNI CE8506, CE8504.

F9S ER_0215(R1.1 --> R1.3)-----------------POWER

23. Power team modify +1.5VS power rating to 3.5A ---page82

<Variant Name>

Title : History(2)

ASUSTeK COMPUTER INC Engineer:

Size	Project Name	Rev
Custom	F9S	1.1

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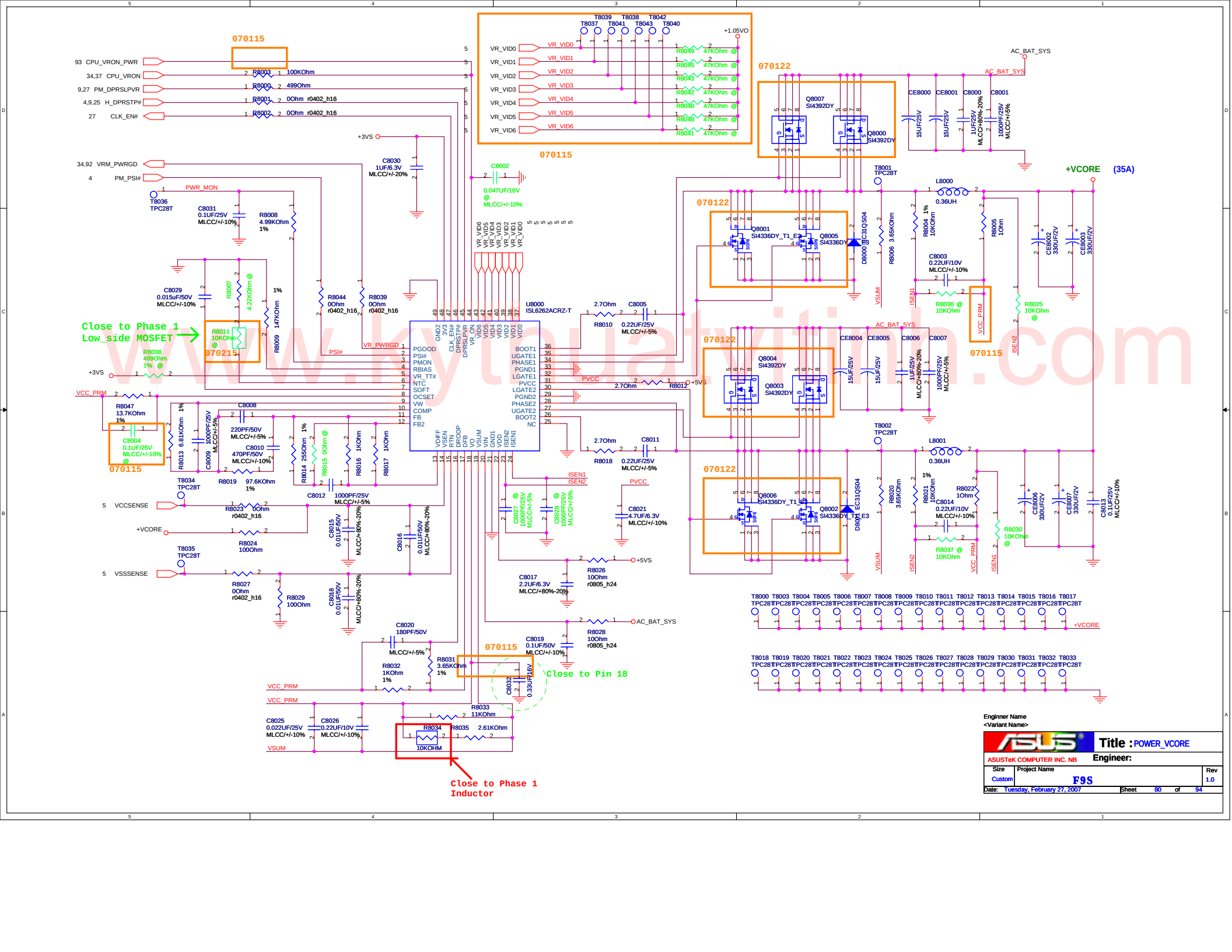

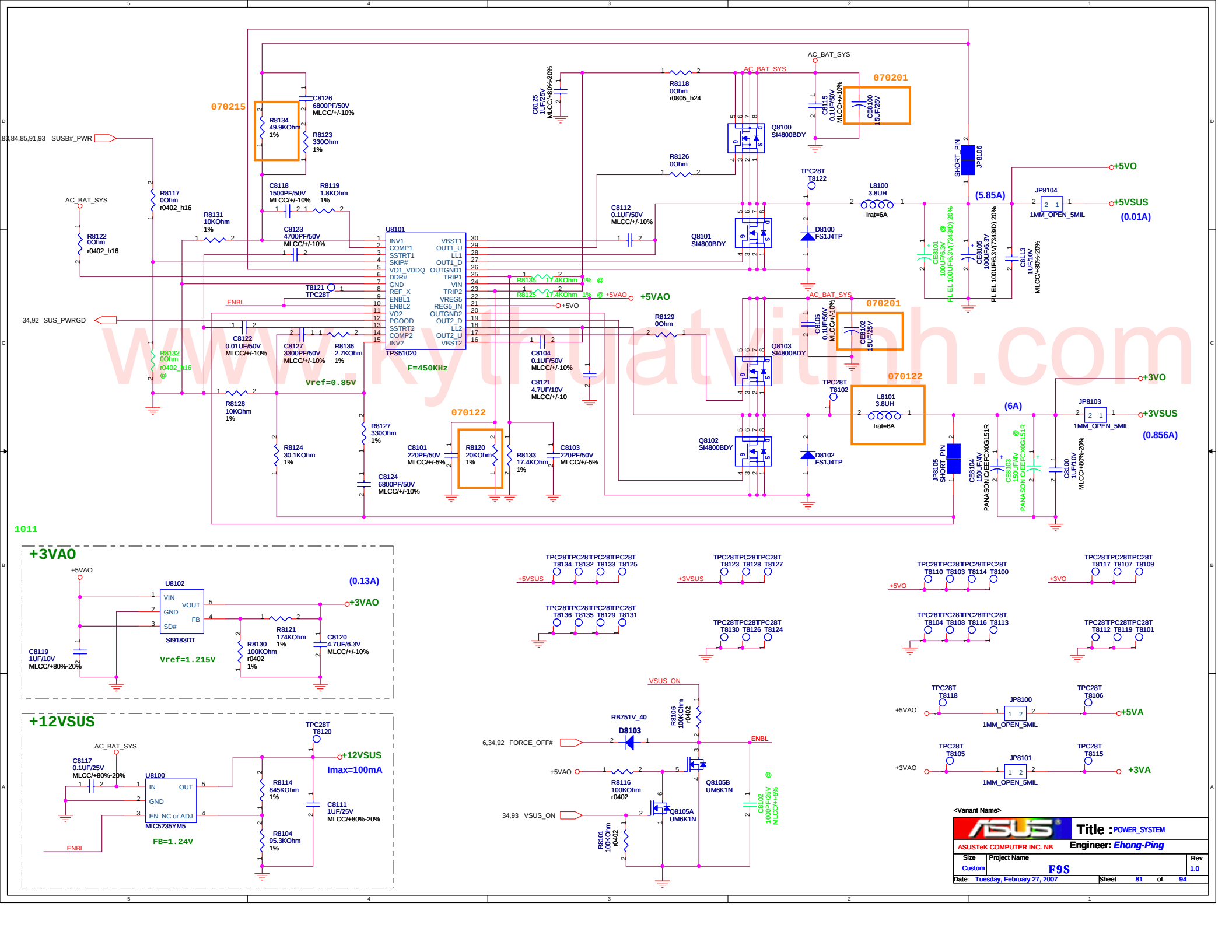

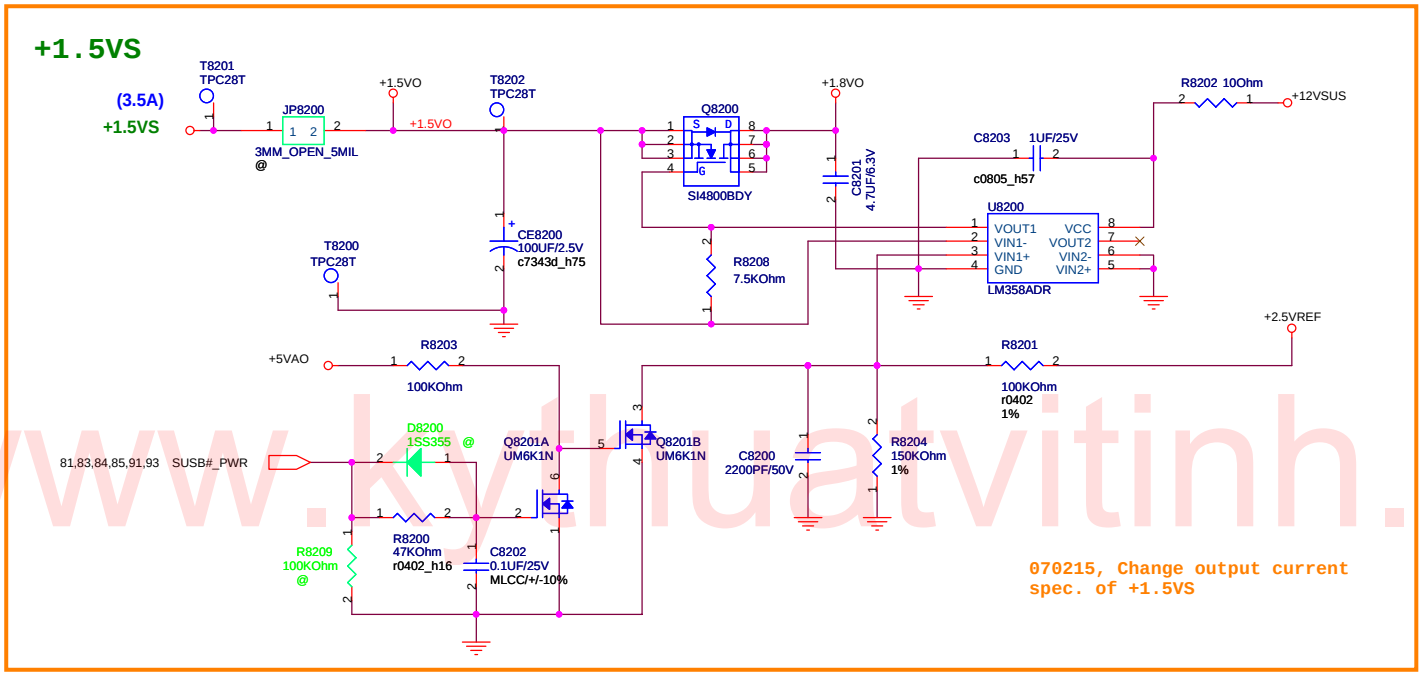

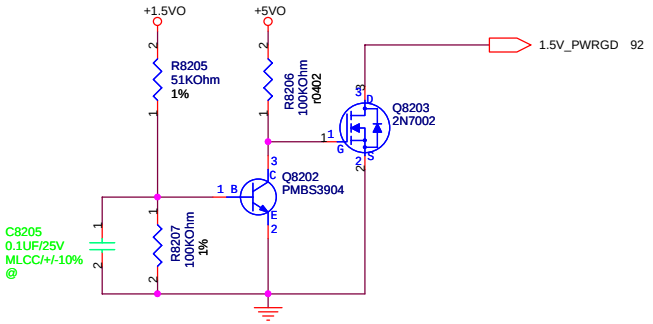

<Variant Name>

Title : POWER_I/O_1.5VS & 1.05VS

ASUSTeK COMPUTER INC. NB

Engineer: Ehong-Ping

Size	Project Name	Rev
B	F9S	1.0

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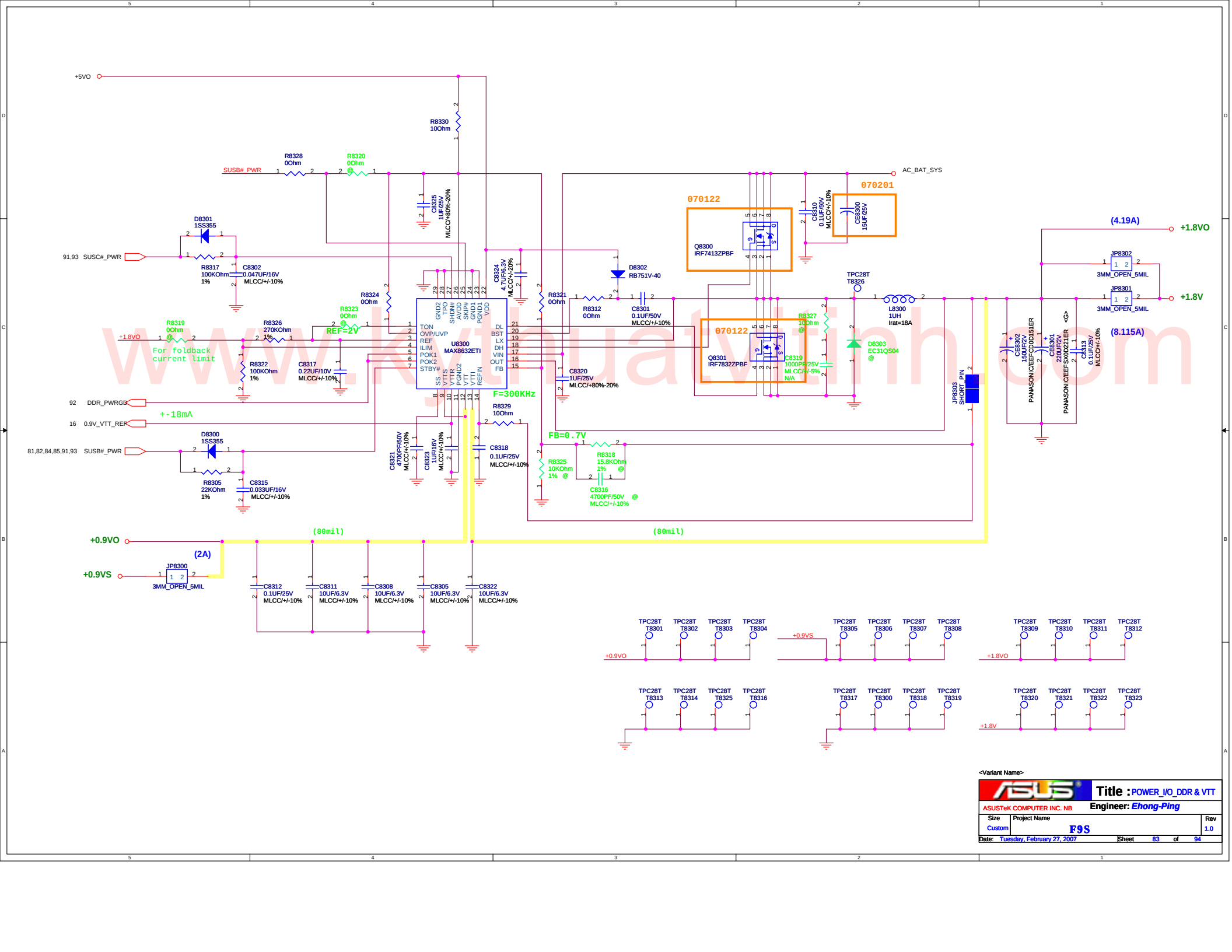


<Variant Name>

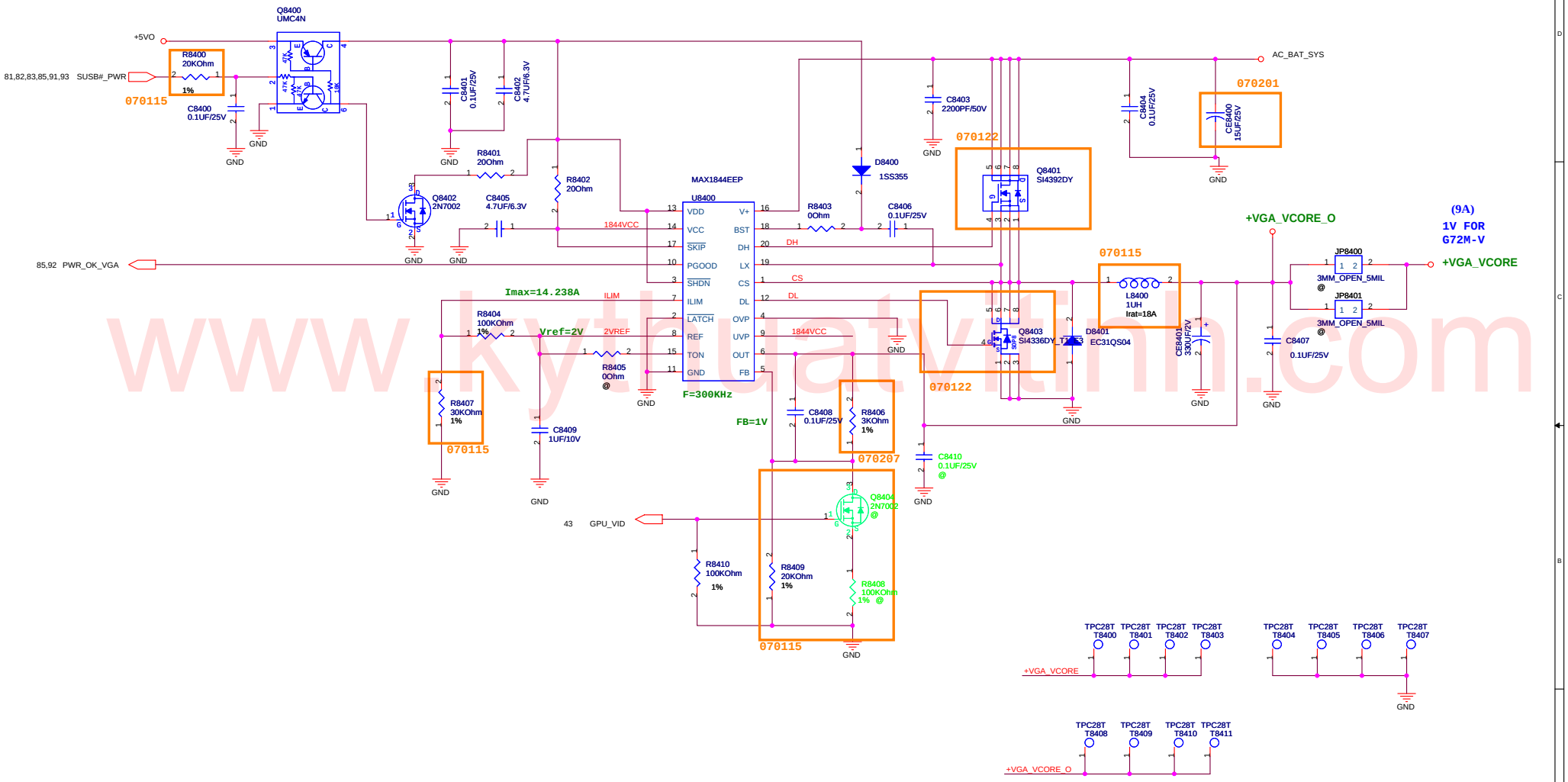
ASUSTeK COMPUTER INC. NB

Title : POWER_I/O_DDR & VTT

Engineer: Ehong-Ping

Size	Project Name	Rev
Custom	F9S	1.0

Date: Tuesday, February 27, 2007 Sheet 83 of 94



<Variant Name>

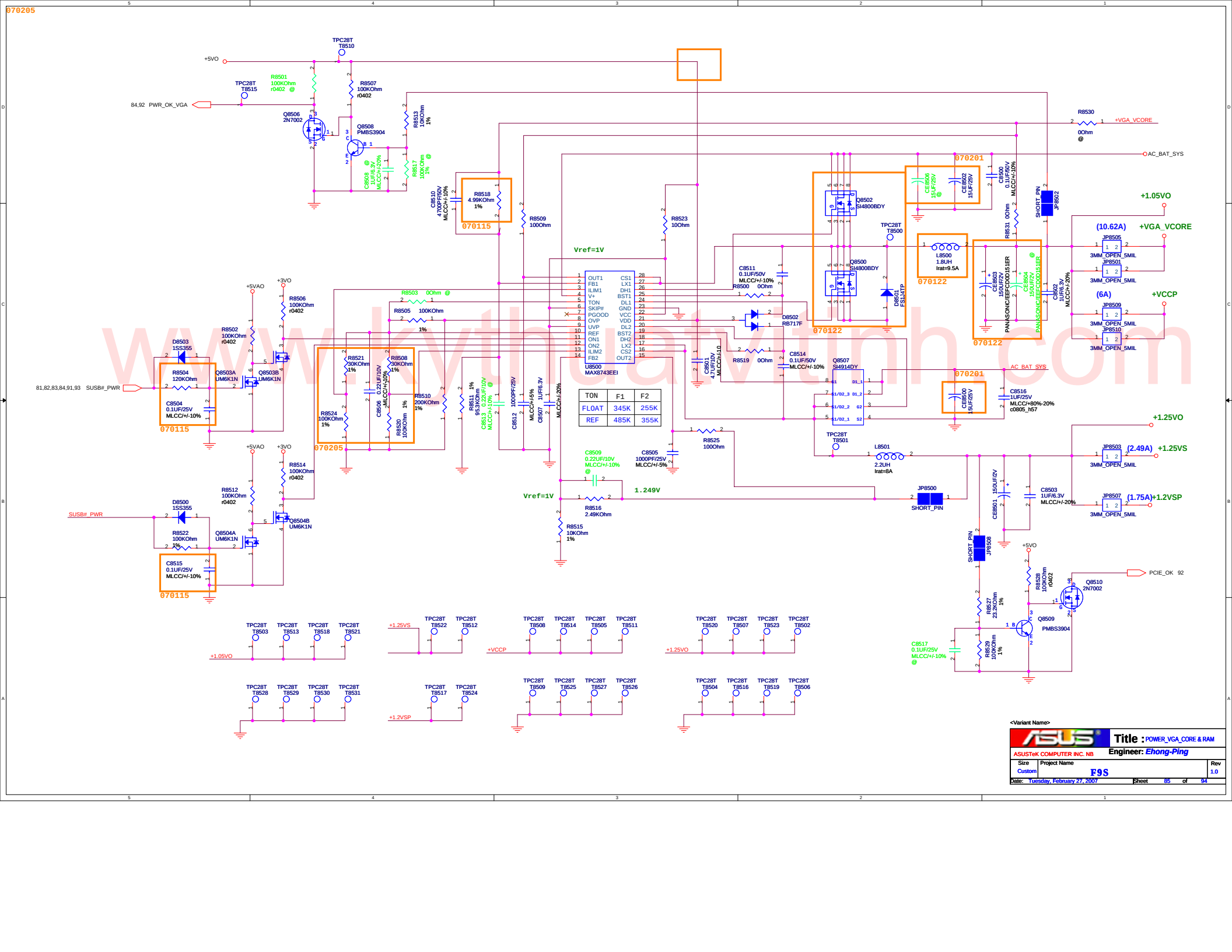
ASUSTeK COMPUTER INC. NB

Title : POWER_I/O_ +2.5VS

Engineer: Ehong-Ping

Size	Project Name	Rev
Custom	F9S	1.0

Date: Tuesday, February 27, 2007 Sheet 84 of 94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U8500
MAX8743EEI
Vref=1V
1.249V
TON F1 F2
FLOAT 345K 255K
REF 485K 355K
+5VO
+3VO
+5VAO
+1.05VO
+1.25VS
+1.25VO
+VCCP
+1.2VSP
+VGA_VCORE
+1.25VO
+VCCP
+1.25VS
+1.2VSP
AC_BAT_SYS
PWR_OK_VGA
SUSB#_PWR
PCIE_OK
Title : POWER_VGA_CORE & RAM
Engineer: Ehong-Ping
ASUSTeK COMPUTER INC. NB
Project Name F9S
Size Custom
Rev 1.0
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<Variant Name>

Title : N/A

ASUSTeK COMPUTER INC. NB

Engineer: Ehong-Ping

Size	Project Name	Rev
B	F9S	1.0

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<Variant Name>

Title : POWER_SHUTDOWN#

ASUSTeK COMPUTER INC. NB

Engineer: Ehong-Ping

Size	Project Name	Rev
Custom	F9S	1.0

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POWER PATH & BAT_LEARN

90 WATT

AC_IN Threshold 2.048Vmax A/D_DOCK_IN
> 17.44V active

Adapter Iin(max) = [0.075V/Rsense(ADin)]*[VCLS/VREF]
Rsense(ADin)=0.010ohm
VCLS=2.5341V
=> Iin(max)=4.5A
=> Constant Power = 19 * 4.5 = 85.5W
=> R5710=20K,R5715=30K

Charge Current Ichg = [0.075V/Rsense(CHG)]*[VICTL/3.6V]
Rsense(CHG)=0.025 ohm
VICTL= 3V => Ichg = 2.5A
VICTL= 1.68V => Ichg = 1.4A

Vbatt = Cell * { Vref +[(VCTL- 1.8V) / 9.52] }
VCTL= 1.588V
=> Vbatt = 4.2V

Mode pin : Vmode > 2.8V (trie to LDO pin) ----> 4 Cells
2.0 > Vmode > 1.6V (floating) ----> 3 Cells
0.8 > Vmode (trie to GND) ----> Learning mode

VICTL< 0.8V or DCIN < 7V -->Charger Disable

Precgarge current=150mA

LDO : 5.4V
REF : 4.2235V

90W->10m Ohm
65W->20m Ohm

90W->30K Ohm
65W->137K Ohm

070115

AC_BAT_SYS_INV to Inverter connect,
Power trace =60mil(min),
Put JP8805 close to Q8800

070115

4S: Mount R8808 only
3S: Unmount all components
3S/4S: Unmount R8808, and mount others

<Variant Name>

ASUSTeK COMPUTER INC. NB

Title : POWER_CHARGER

Engineer: Ehong-Ping

Size	Project Name	Rev
Custom	F9S	1.0

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<Variant Name>

Title : N/A

ASUSTeK COMPUTER INC. NB

Engineer: Ehong-Ping

Size	Project Name	Rev
Custom	F9S	1.0

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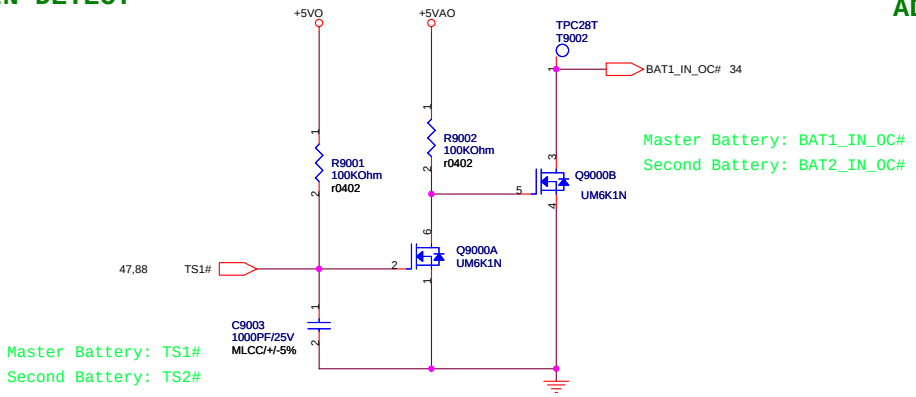
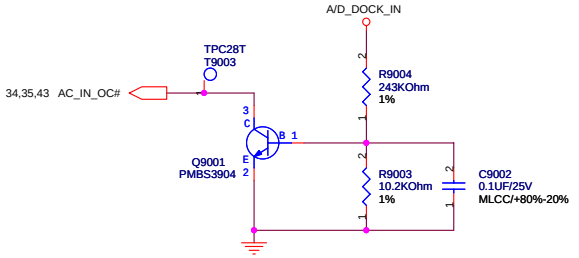
BATTERY IN DETECT



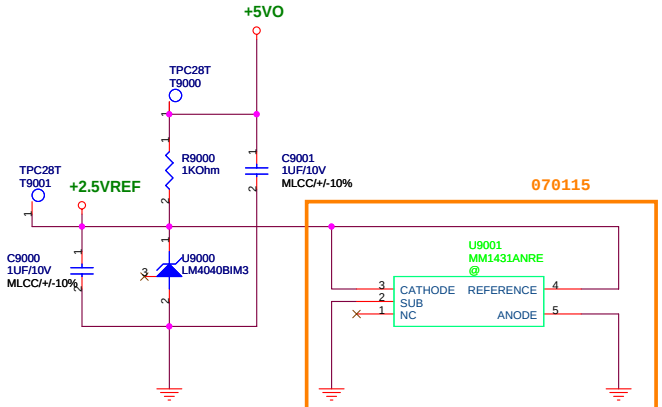
Master Battery: BAT1_IN_OC#
Second Battery: BAT2_IN_OC#

Master Battery: TS1#
Second Battery: TS2#

ADAPTER IN DETECT



+2.5VREF



U9000 & U9001 colay

<Variant Name>

Title : POWER_DETECT

ASUSTeK COMPUTER INC. NB

Engineer: Ehong-Ping

Size	Project Name	Rev
Custom	F9S	1.0

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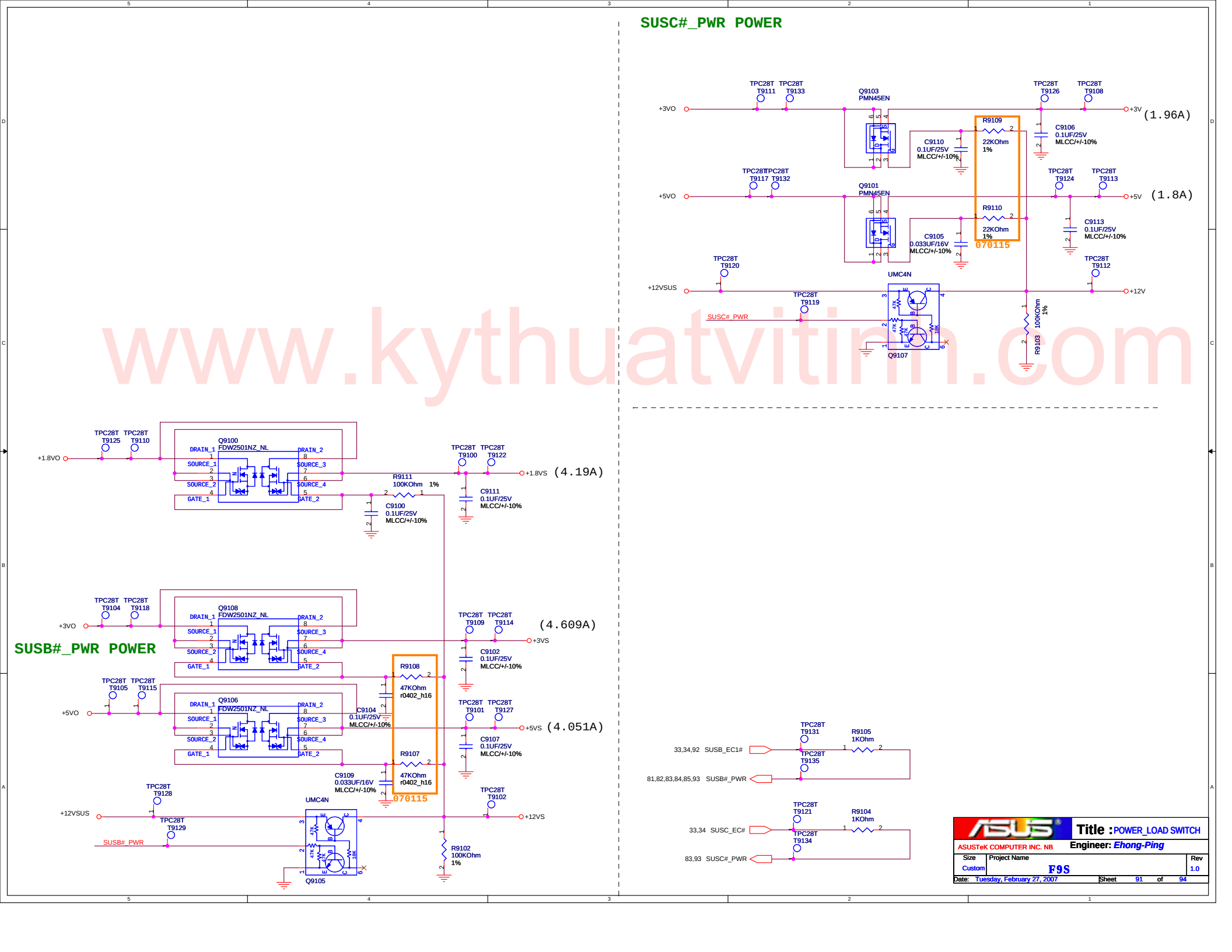
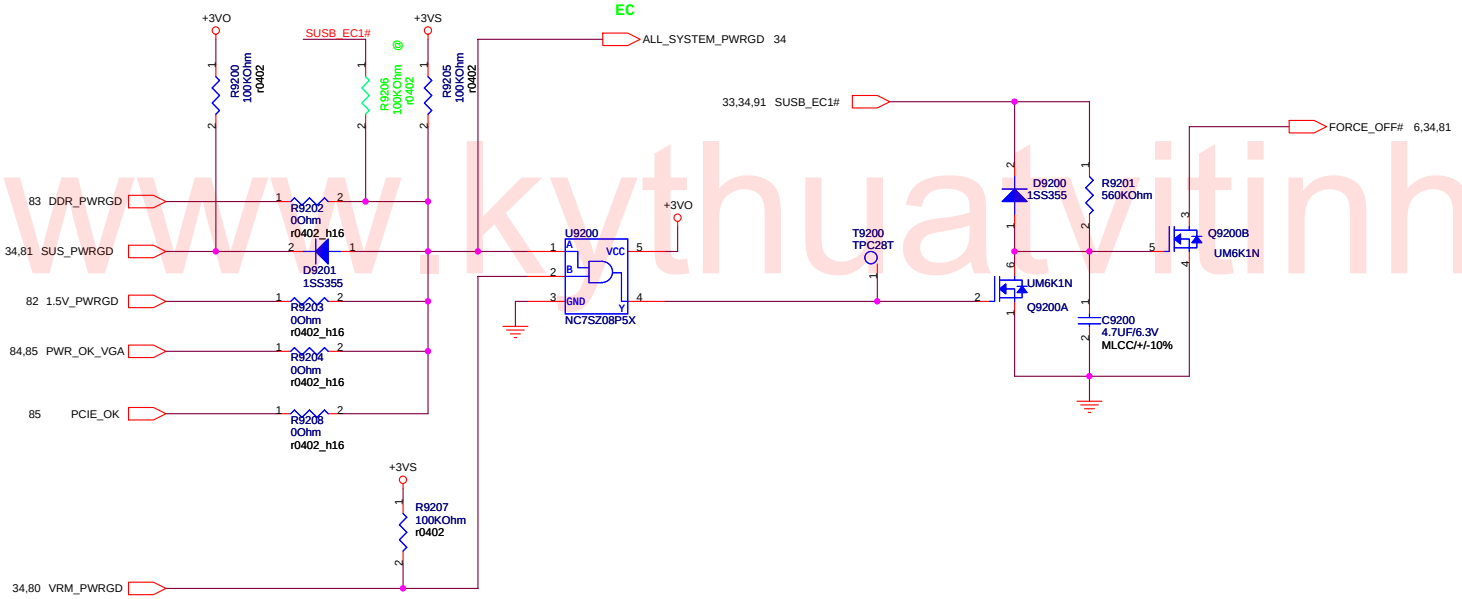


POWER GOOD DETECTER



<Variant Name>

Title : POWER_PROTECT

ASUSTeK COMPUTER INC. NB

Engineer: Ehong-Ping

Size	Project Name	Rev
Custom	F9S	1.0

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AC_BAT_SYS — AC_BAT_SYS 46,80,81,83,84,85,88

BAT — BAT 46,88

BAT_CON — BAT_CON 46,47,88

+2.5VREF — +2.5VREF 82,90

+3VA — +3VA 17,25,27,34,37,46,81

+5VAO — +5VAO 81,82,85,90

+5VO — +5VO 81,82,83,84,85,90,91

+5VSUS — +5VSUS 24,28,81

+5V — +5V 17,24,36,37,91

+5VS — +5VS 6,18,19,21,22,23,28,33,34,37,38,39,44,46,80,91

+3VO — +3VO 81,85,91,92

+3VSUS — +3VSUS 17,20,22,24,26,27,28,29,34,39,46,81

+3V — +3V 19,20,21,22,26,33,35,37,91

+3VS — +3VS 6,7,9,12,13,14,15,17,18,19,20,21,22,23,25,27,28,29,33,34,37,39,40,43,44,45,80,91,92

+12VSUS — +12VSUS 24,81,82,91

+12V — +12V 22,24,37,91

+12VS — +12VS 17,18,19,22,37,91

+1.8VO — +1.8VO 82,83,91

+1.8V — +1.8V 9,11,14,15,16,37,83

+0.9VS — +0.9VS 16,37,83

+0.9VO — +0.9VO 83

+1.05VO — +1.05VO 80,85

+VCCP — +VCCP 4,5,6,7,8,9,11,12,28,37,85

+1.5VO — +1.5VO 82

+1.5VS — +1.5VS 5,12,20,25,28,33,37,82

+VCORE — +VCORE 5,6,37,80

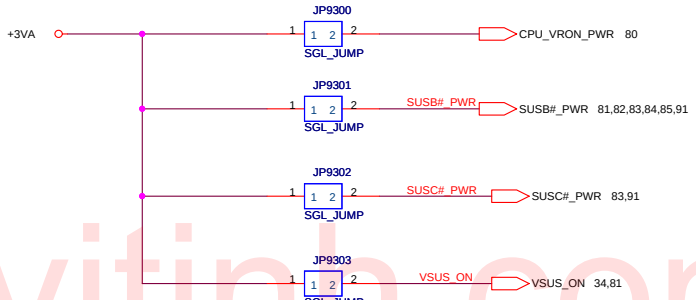
+VGA_VCORE — +VGA_VCORE 37,40,84,85

+1.8VS — +1.8VS 37,41,43,44,91

+1.2VSP — +1.2VSP 37,40,41,44,85

+1.25VS — +1.25VS 9,12,28,85

FOR POWER TEST



<Variant Name>

Title : POWER_SIGNAL

ASUSTeK COMPUTER INC. NB

Engineer: Ehong-Ping

Size	Project Name	Rev
Custom	F9S	1.0

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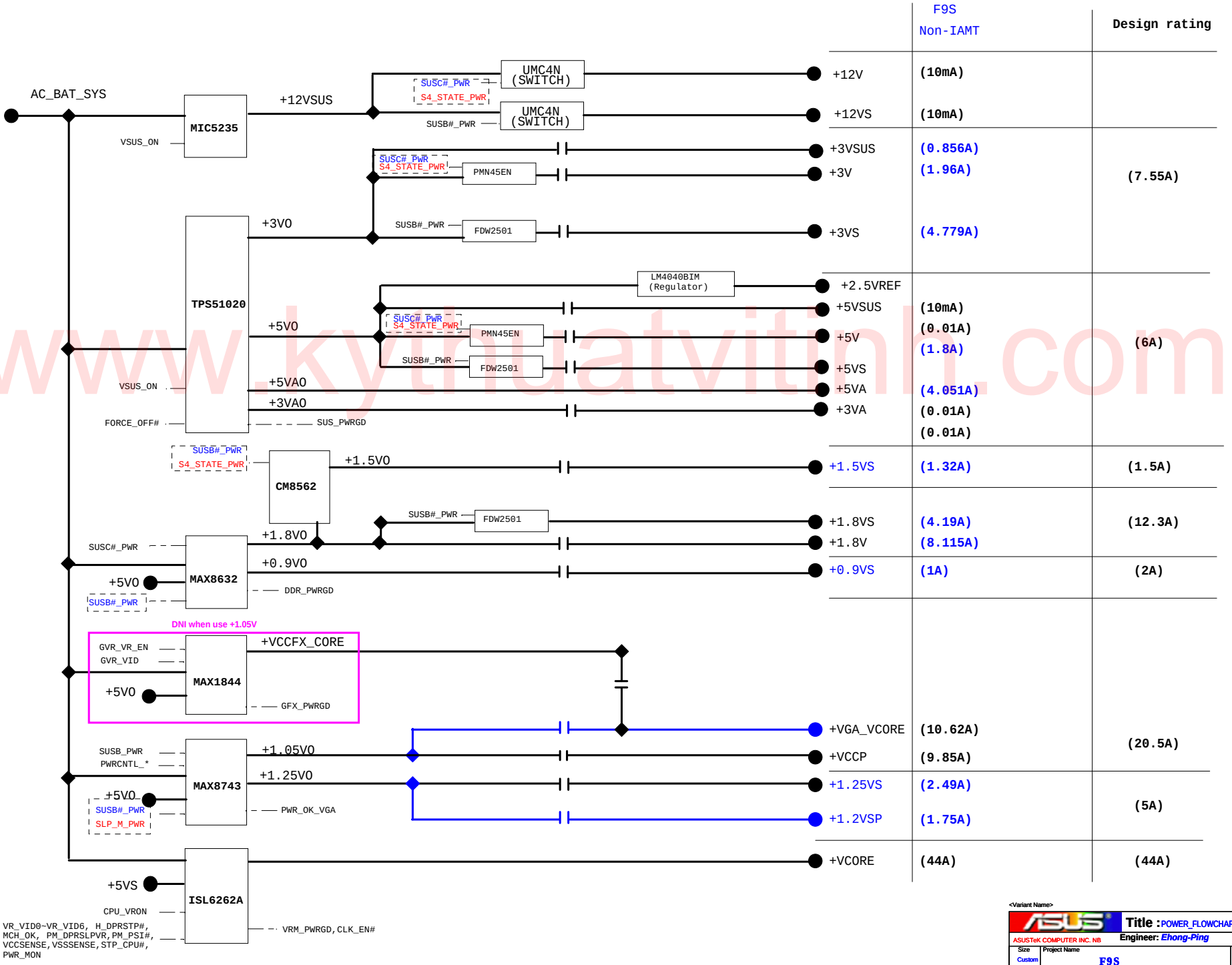

	F9S Non-IAMT	Design rating
+12V	(10mA)	
+12VS	(10mA)	
+3VSUS	(0.856A)	(7.55A)
+3V	(1.96A)	
+3VS	(4.779A)	
+2.5VREF		
+5VSUS	(10mA)	(6A)
+5V	(0.01A)	
+5VS	(1.8A)	
+5VA	(4.051A)	
+3VA	(0.01A)	
	(0.01A)	
+1.5VS	(1.32A)	(1.5A)
+1.8VS	(4.19A)	(12.3A)
+1.8V	(8.115A)	
+0.9VS	(1A)	(2A)
+VGA_VCORE	(10.62A)	(20.5A)
+VCCP	(9.85A)	
+1.25VS	(2.49A)	(5A)
+1.2VSP	(1.75A)	
+VCORE	(44A)	(44A)

<Variant Name>

Title : POWER_FLOWCHART

ASUSTeK COMPUTER INC. NB

Engineer: Ehong-Ping

Size	Project Name	Rev
Custom	F9S	1.0

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