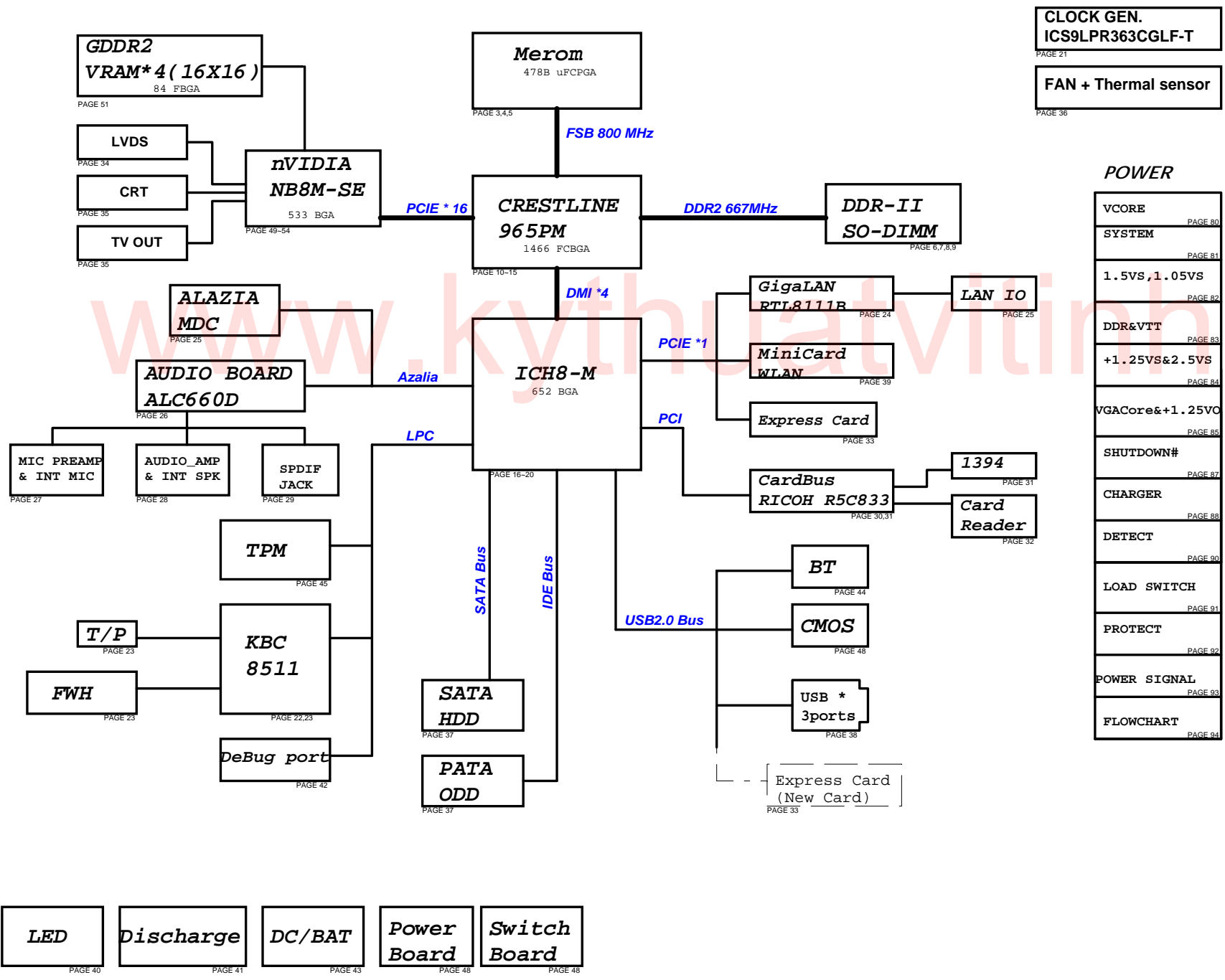


T76S: MEROM/965-PM/ICH8-M/NB8M-SE BLOCK DIAGRAM



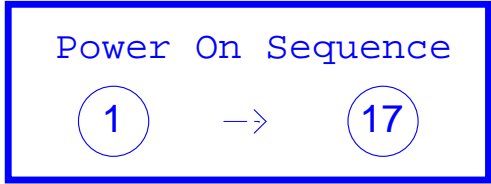
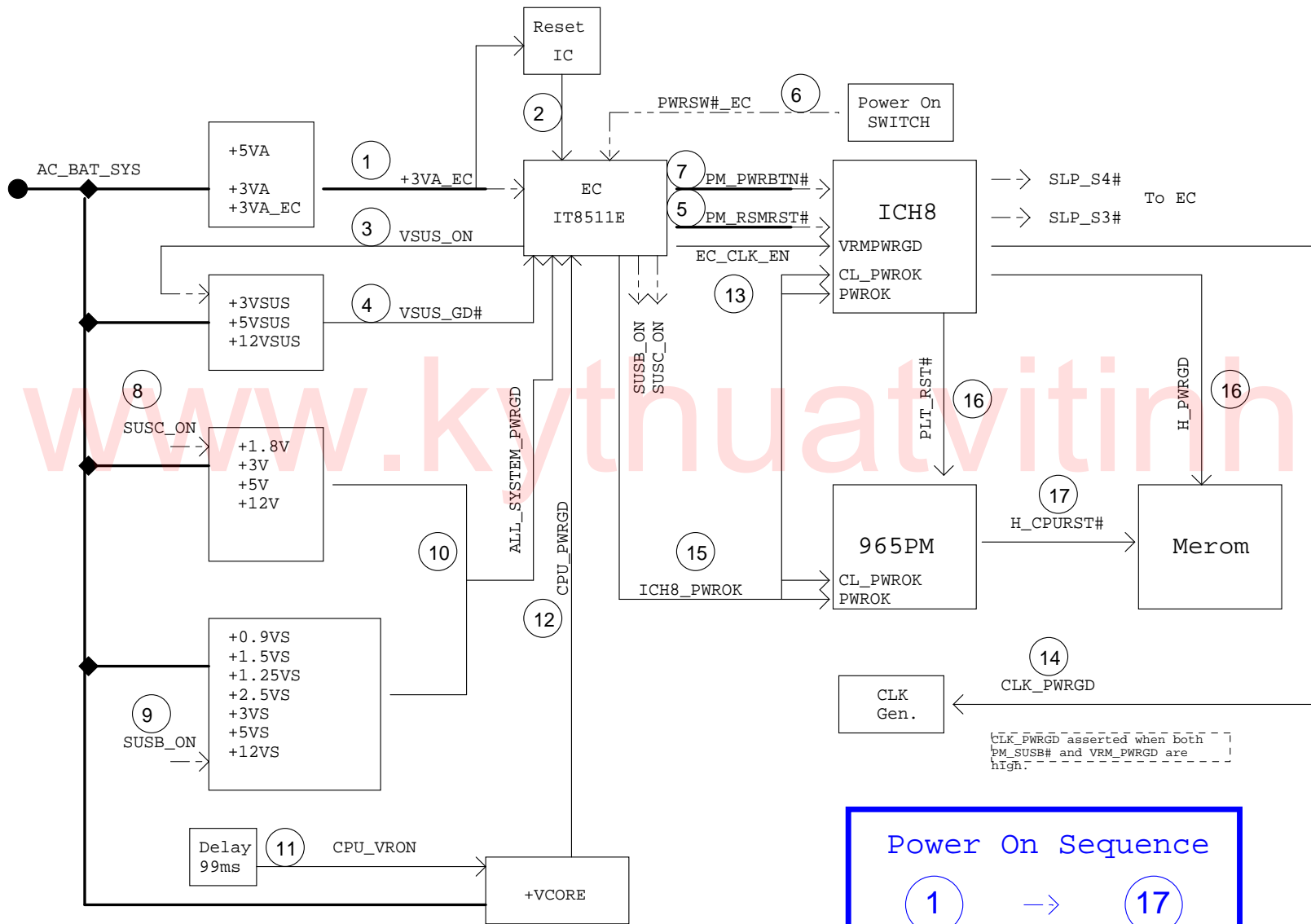
CLOCK GEN.
ICS9LPR363CGLF-T
PAGE 21

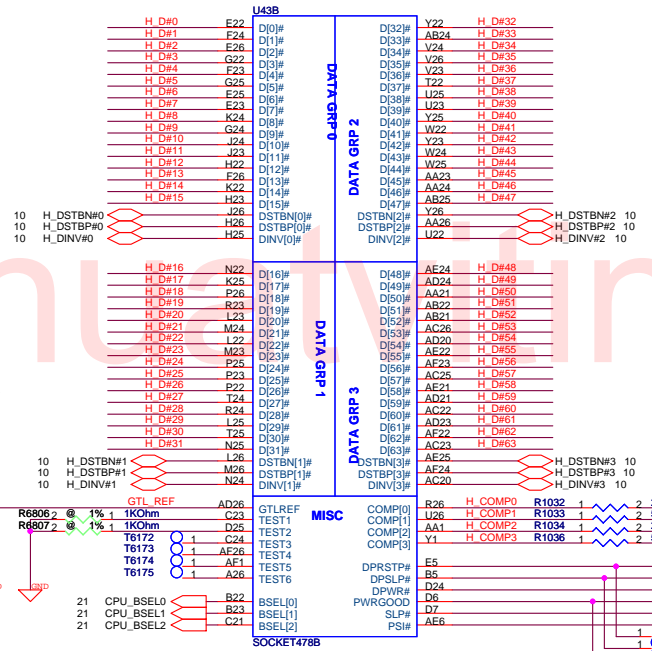
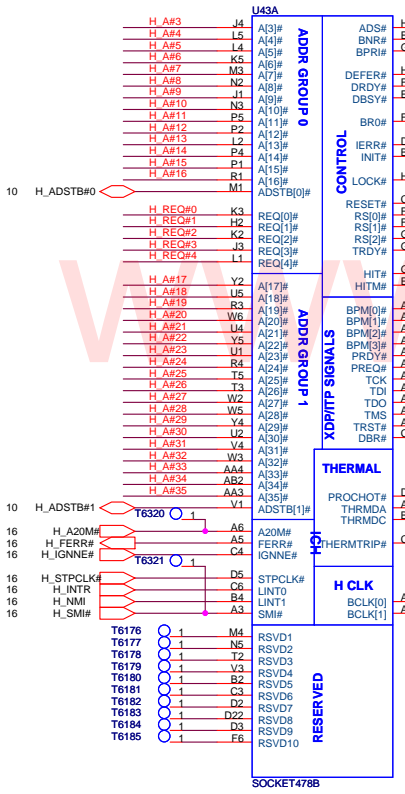
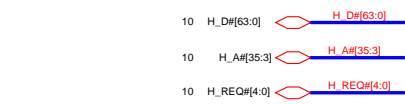
FAN + Thermal sensor
PAGE 36

POWER

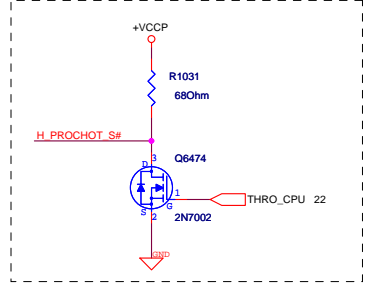
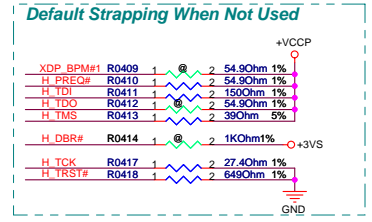
VCORE	PAGE 80
SYSTEM	PAGE 81
1.5VS, 1.05VS	PAGE 82
DDR&VTT	PAGE 83
+1.25VS&2.5VS	PAGE 84
VGACore&+1.25VO	PAGE 85
SHUTDOWN#	PAGE 87
CHARGER	PAGE 88
DETECT	PAGE 90
LOAD SWITCH	PAGE 91
PROTECT	PAGE 92
POWER SIGNAL	PAGE 93
FLOWCHART	PAGE 94

LED (PAGE 40) **Discharge** (PAGE 41) **DC/BAT** (PAGE 43) **Power Board** (PAGE 48) **Switch Board** (PAGE 48)



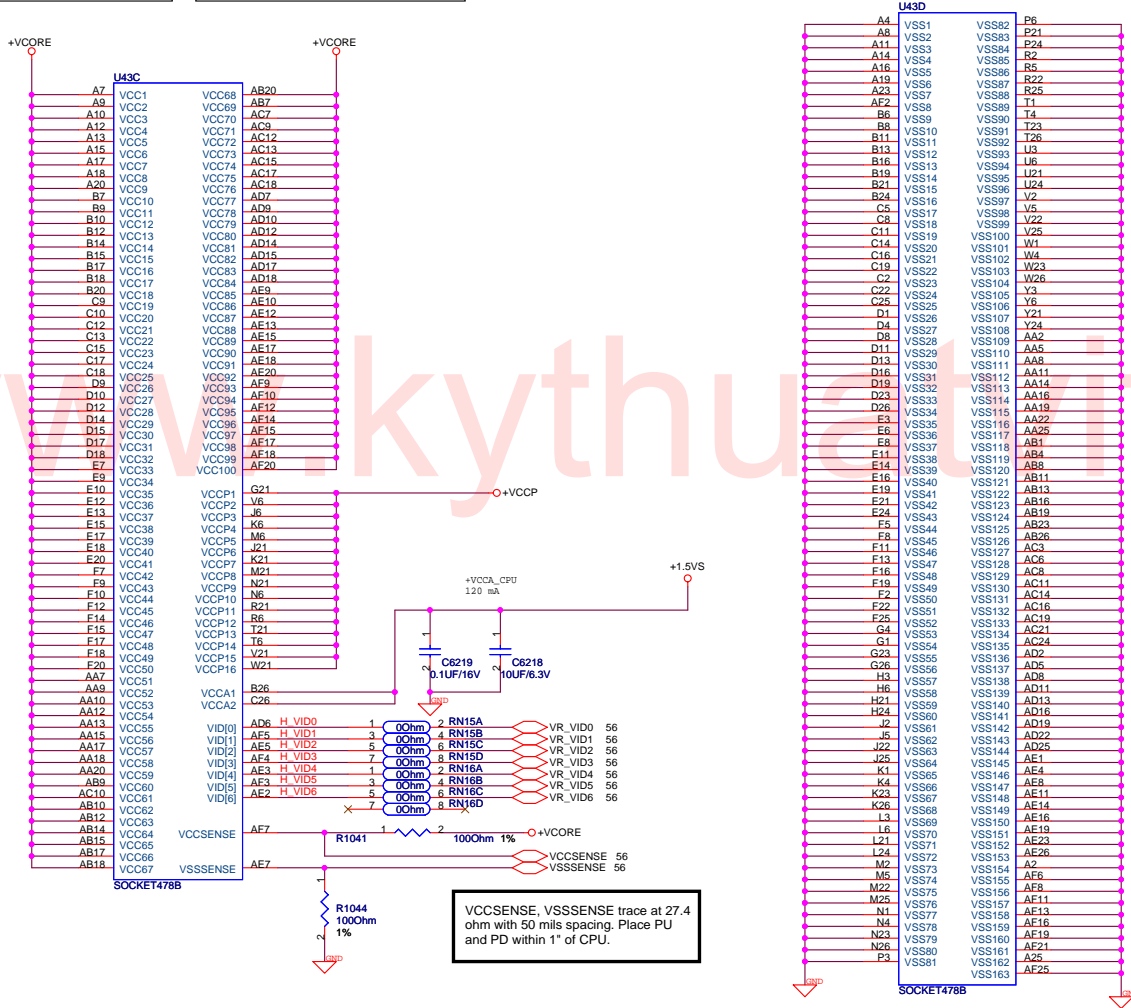


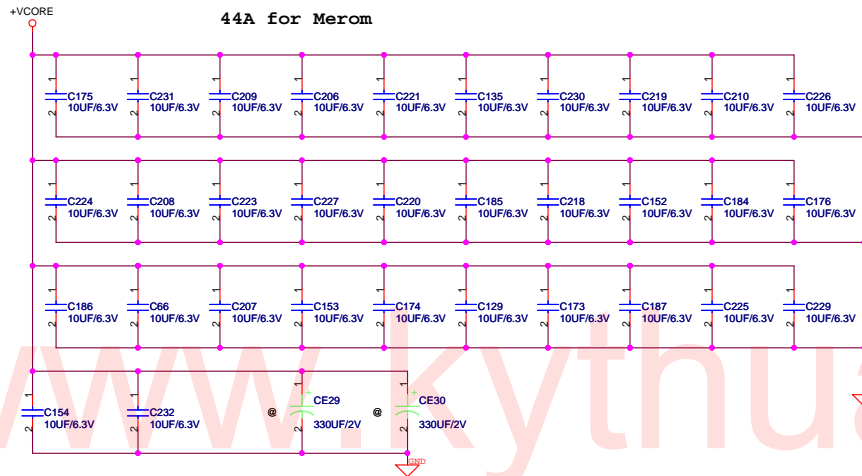
Comp0,2 connect with Z0=27.4 ohm, make trace length shorter than 0.5".
 Comp 1,3 connect with Z0=55 ohm, make trace length shorter than 0.5".



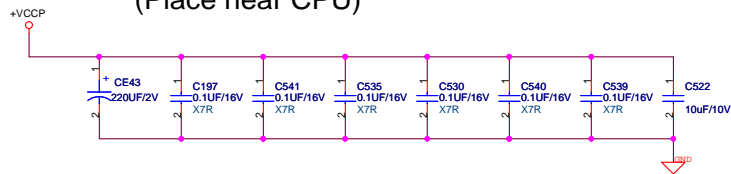
MEROM FSB800 Vcore			
VCC	LFM	TYP	HFM
0.75V		1.325V	
I _{CC}			
30.4A		41A	

MEROM FSB800 Vcore			
VCCP	Min	Typ	Max
1.0V		1.05V	1.1V
I _{CCP}	Min	Typ	Max
			2.5A





**+VCCP Decoupling Capacitor
(Place near CPU)**

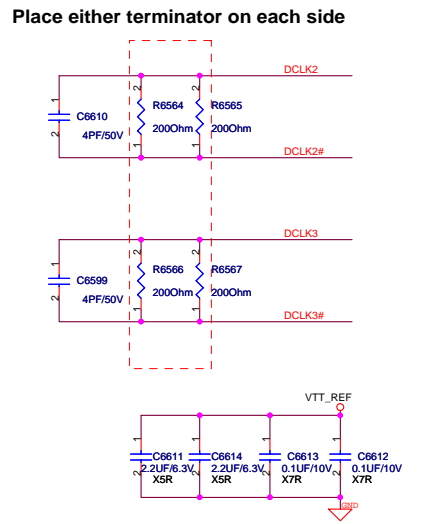
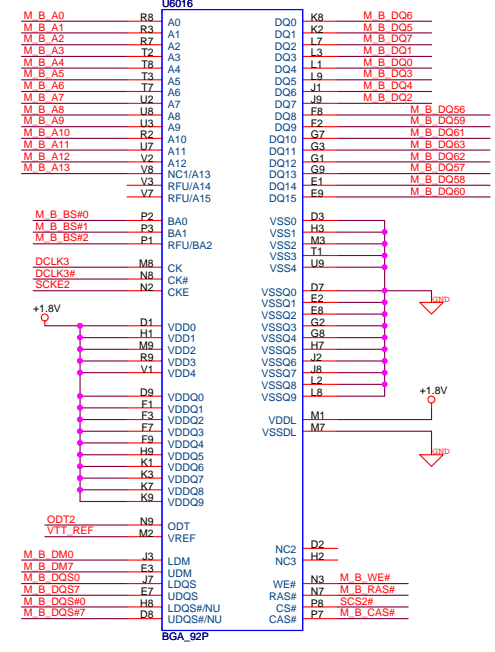
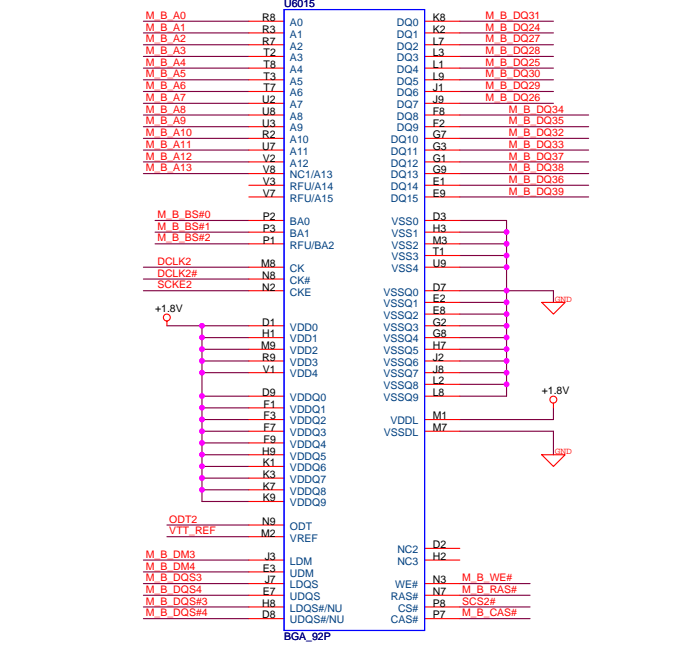
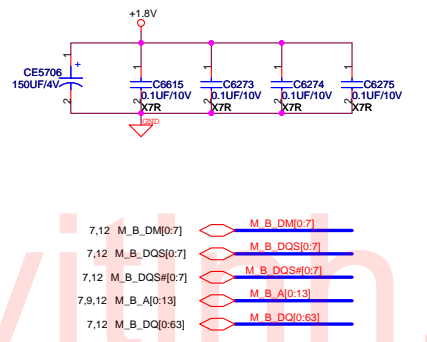
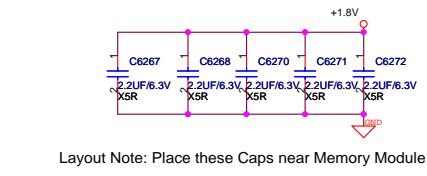
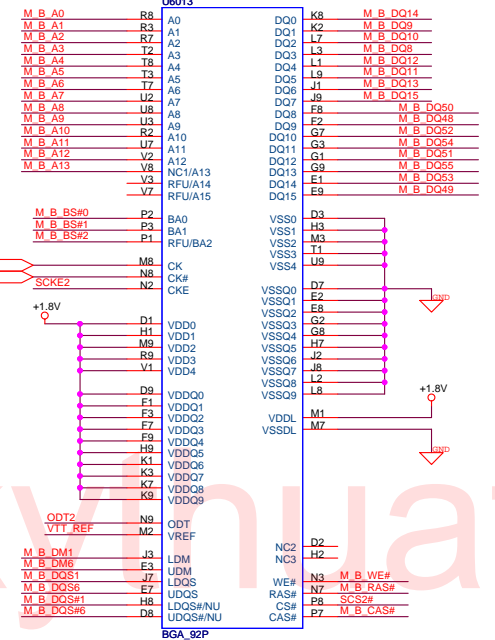
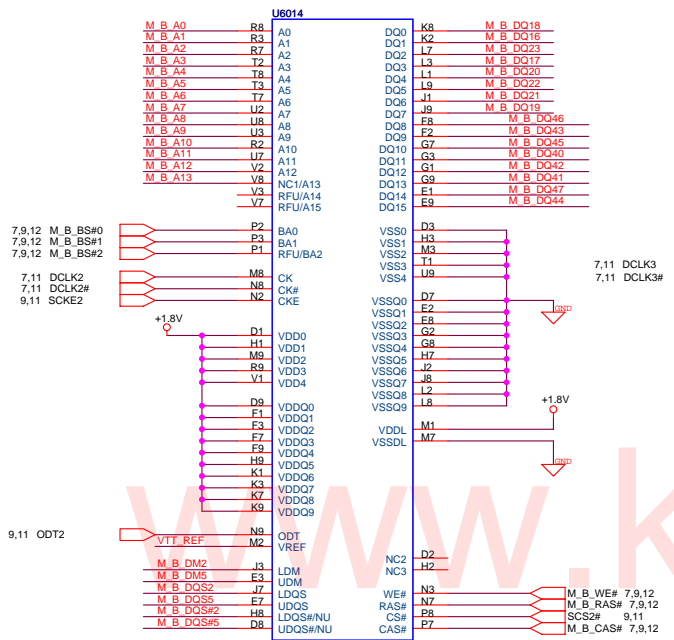


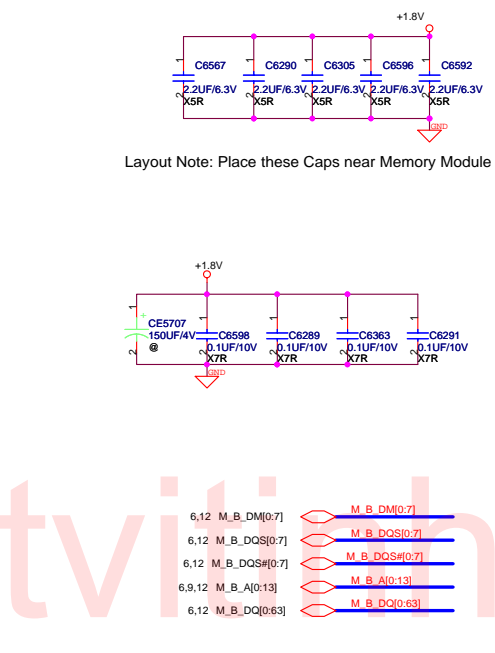
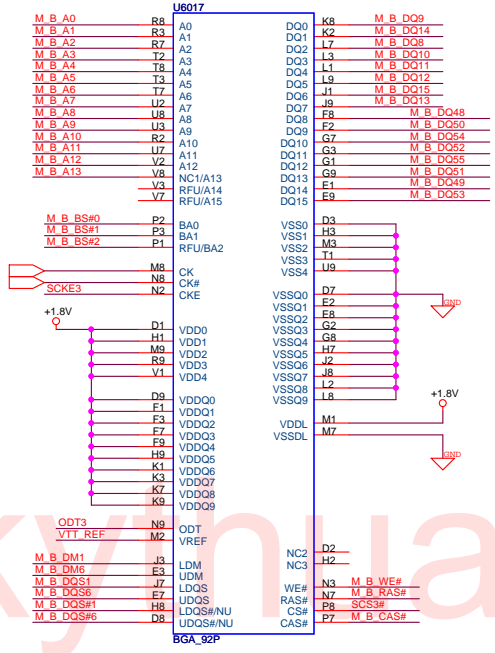
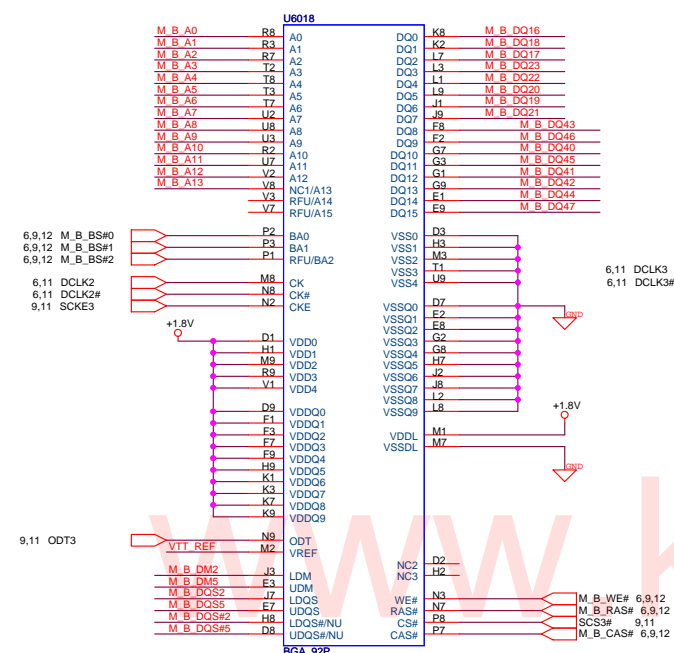
Decoupling guide from INTEL

VCORE	22uF/10V	* 32pcs
	330uF/2V	* 6pcs
VCCP	0.1uF	* 6pcs for CPU
	270uF	* 1pcs for CPU

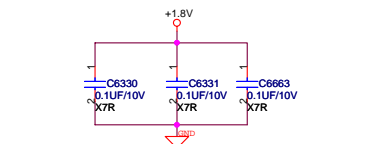
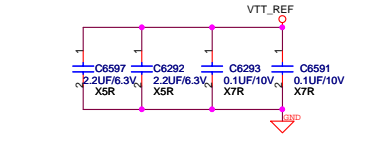
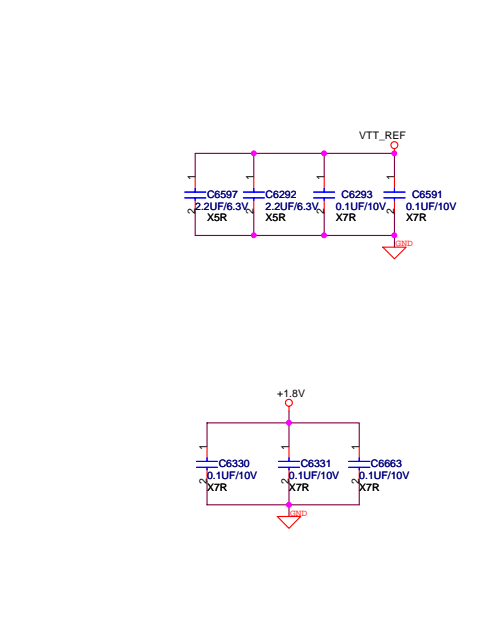
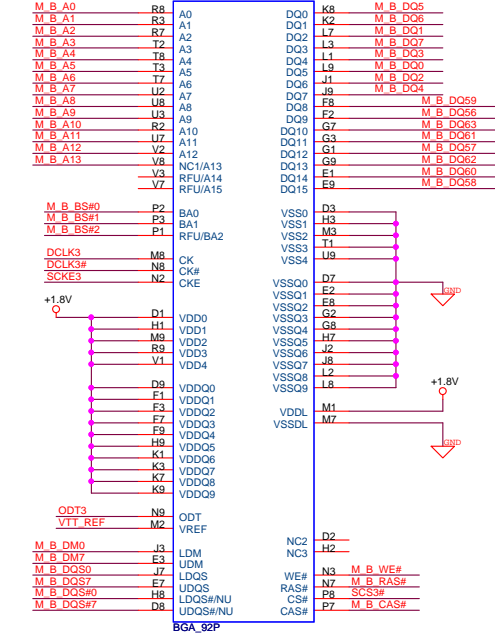
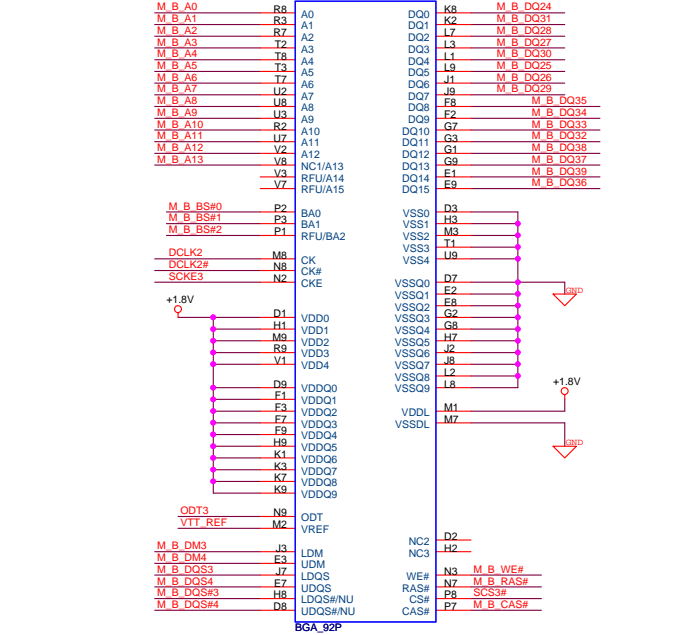
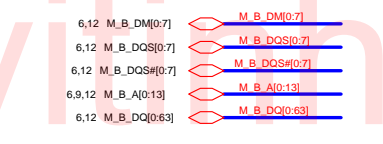
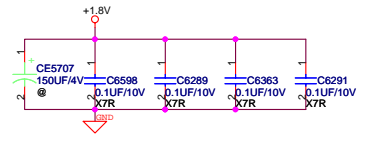
Decoupling for W7S

VCORE	10uF/6.3V	* 32pcs
	330uF/2V	* 2pcs
VCCP	0.1uF	* 6pcs for CPU
	150uF	* 1pcs for CPU



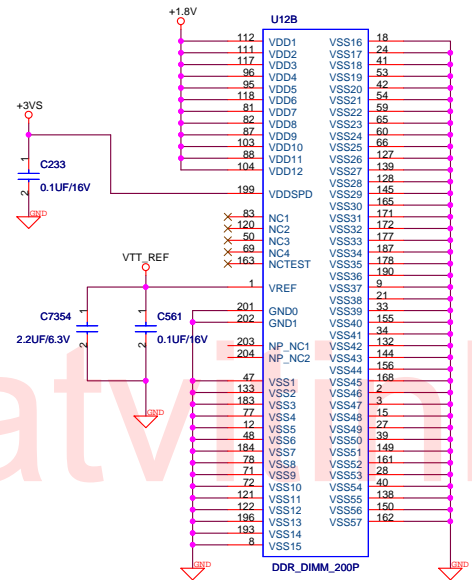
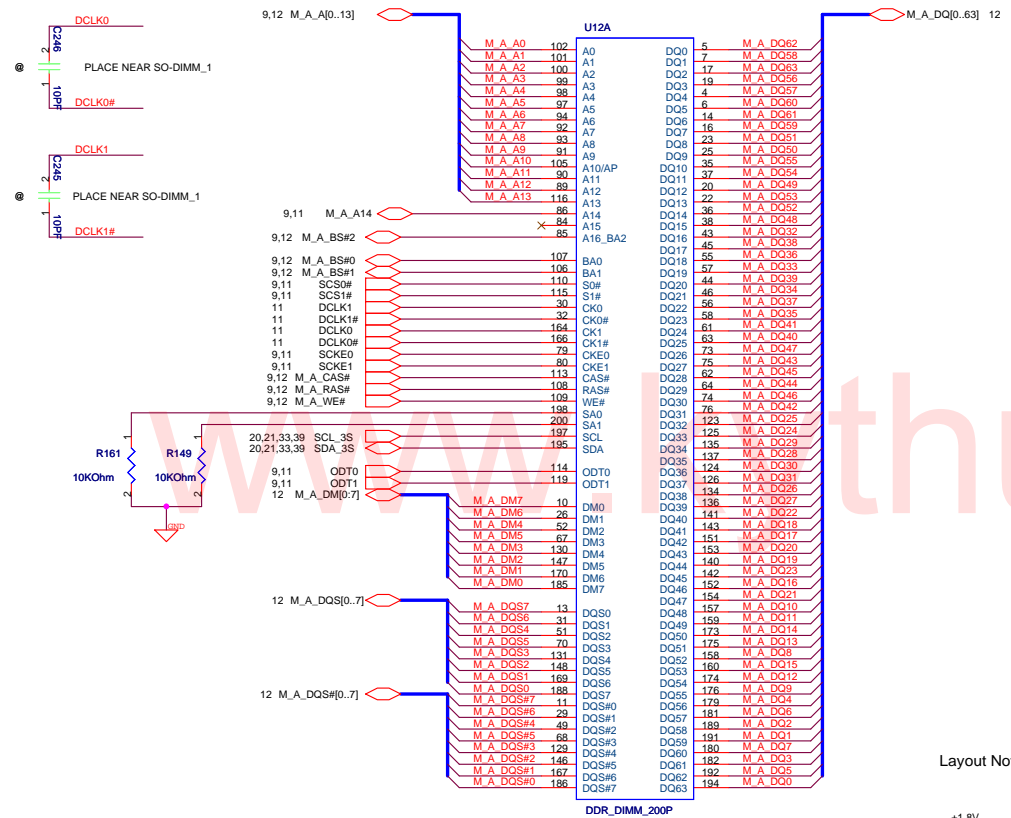


Layout Note: Place these Caps near Memory Module

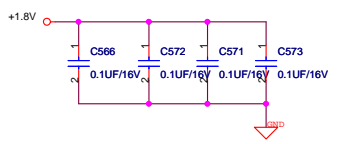


BOTTOM SIDE:
Channel B

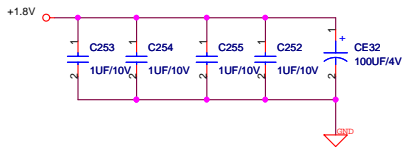
ASUS Title **DDR2 ON BOARD(BOT)**
 ASUSTek COMPUTER INC Engineer: **Lorentz Chang**
 Size Project Name
 Custom **T76S** Rev
 Date: Tuesday, August 21, 2007 Sheet 7 of 70



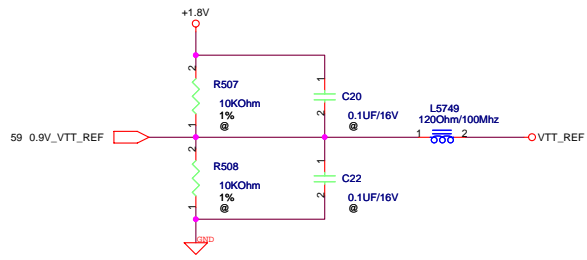
Layout Note: Place these Caps near SO DIMM 1



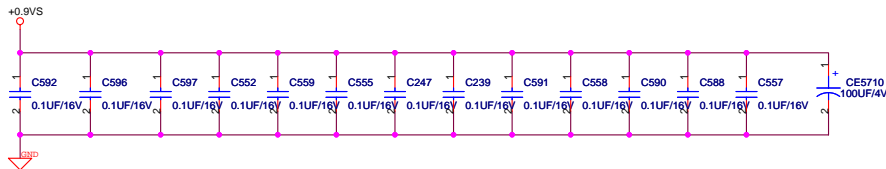
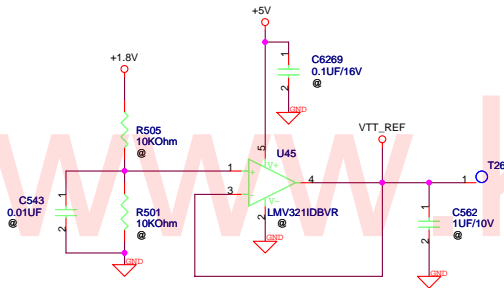
Layout Note: Place these Caps near SO DIMM 1



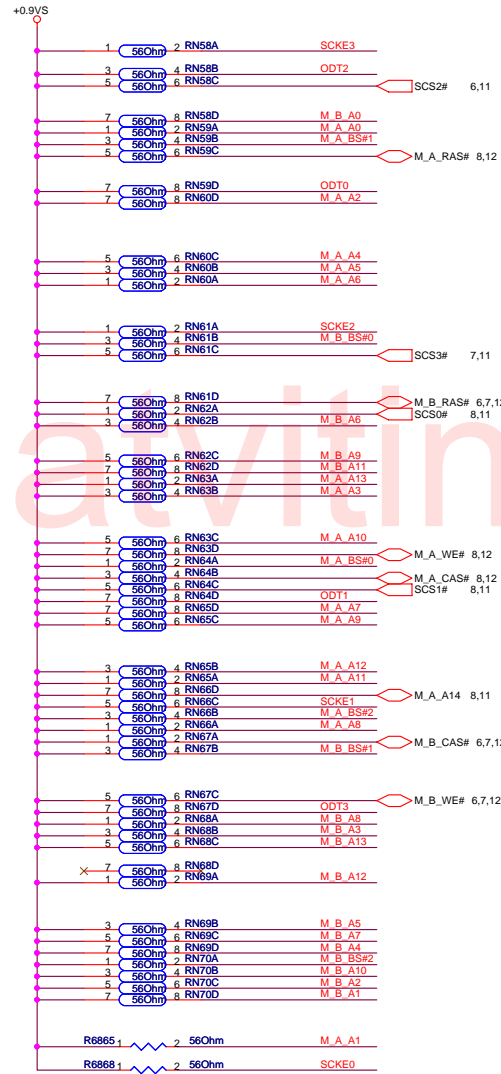
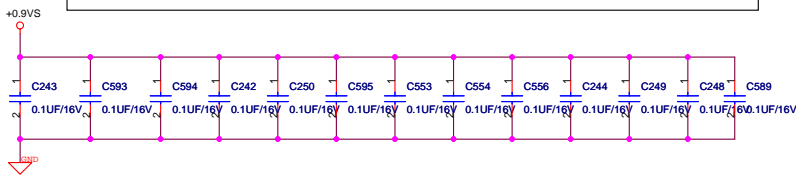
TOP SIDE:
Channel A

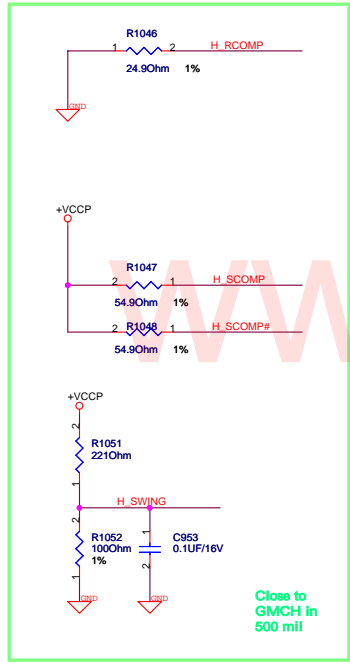


- M_A_A[0..13] 8,12
- M_A_BS#[0..2] 8,12
- M_B_A[0..13] 6,7,12
- M_B_BS#[0..2] 6,7,12
- SCKE[0..3] 6,7,8,11
- ODT[0..3] 6,7,8,11

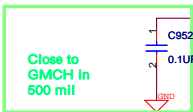


Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9VS

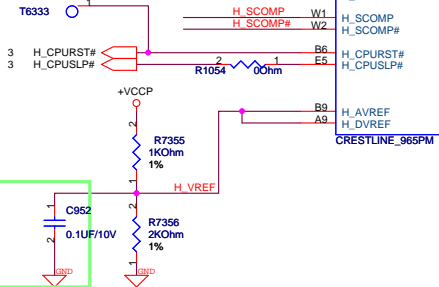




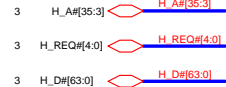
Close to GMCH in 500 mil



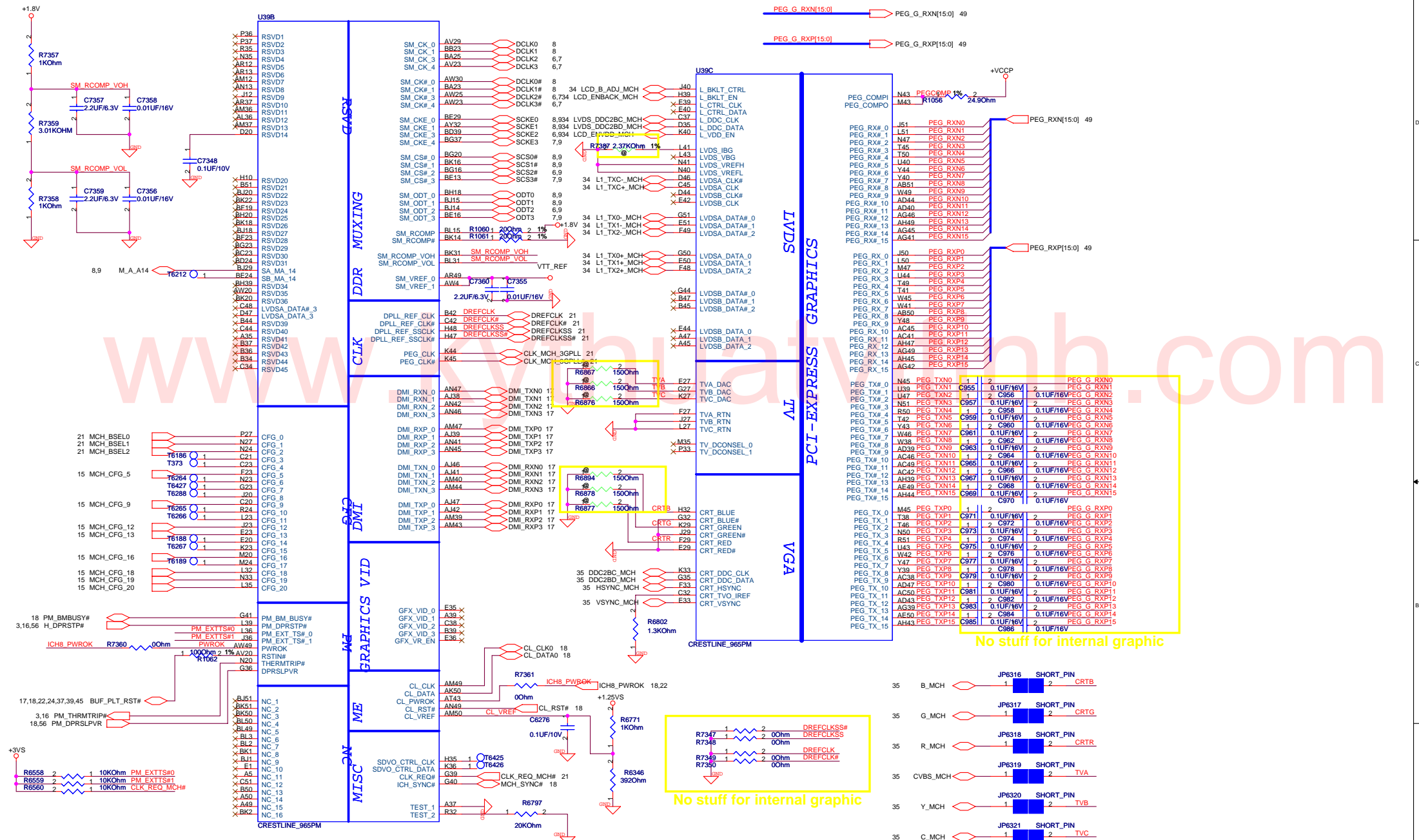
Close to GMCH in 500 mil

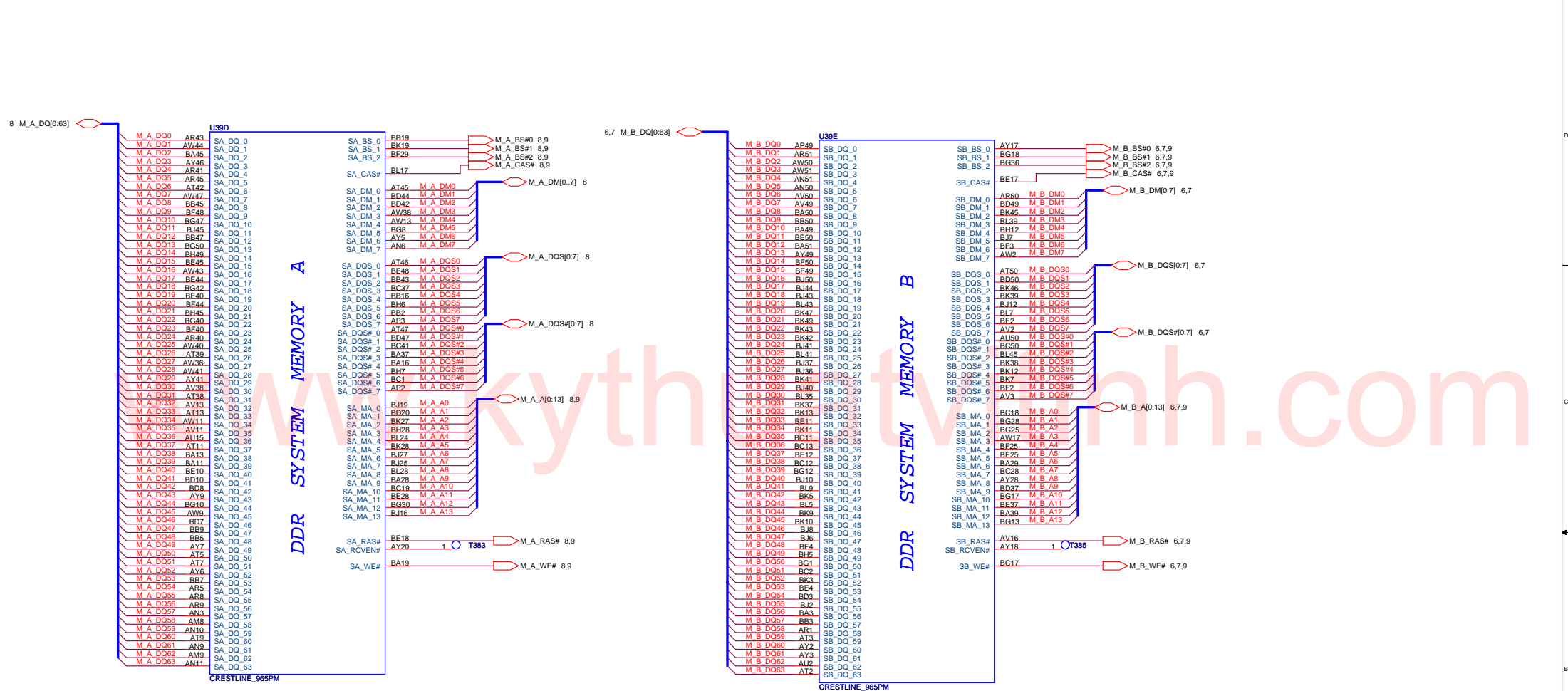


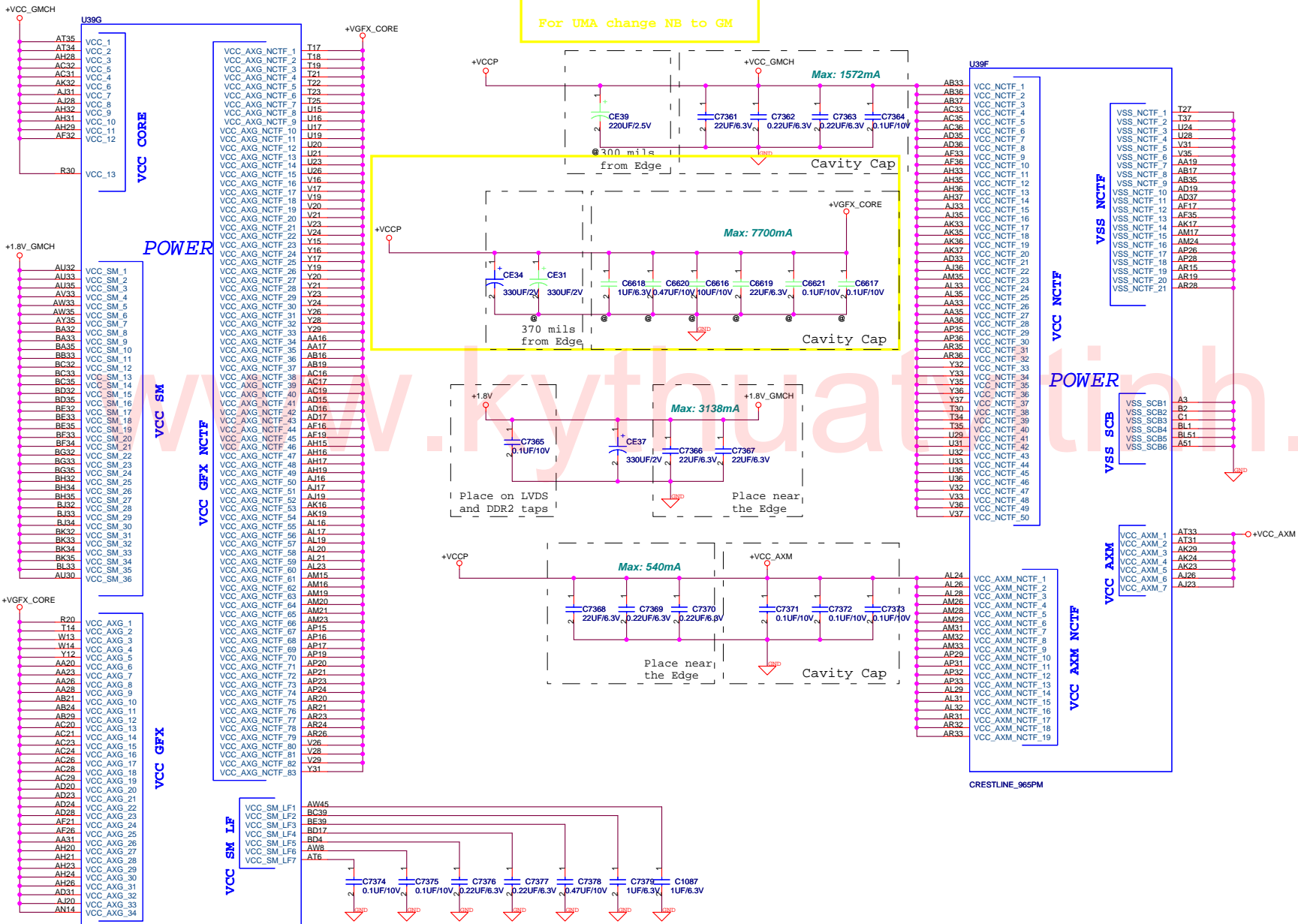
U39A		CRESTLINE_965PM	
H_D#0	E2	H_D#_0	
H_D#1	G2	H_D#_1	
H_D#2	G2	H_D#_2	
H_D#3	M6	H_D#_3	
H_D#4	H7	H_D#_4	
H_D#5	H3	H_D#_5	
H_D#6	G4	H_D#_6	
H_D#7	F3	H_D#_7	
H_D#8	N8	H_D#_8	
H_D#9	H2	H_D#_9	
H_D#10	M10	H_D#_10	
H_D#11	N12	H_D#_11	
H_D#12	H5	H_D#_12	
H_D#13	N9	H_D#_13	
H_D#14	H6	H_D#_14	
H_D#15	P13	H_D#_15	
H_D#16	K9	H_D#_16	
H_D#17	M2	H_D#_17	
H_D#18	W10	H_D#_18	
H_D#19	Y8	H_D#_19	
H_D#20	V4	H_D#_20	
H_D#21	M3	H_D#_21	
H_D#22	N5	H_D#_22	
H_D#23	N3	H_D#_23	
H_D#24	V6	H_D#_24	
H_D#25	V9	H_D#_25	
H_D#26	N2	H_D#_26	
H_D#27	Y7	H_D#_27	
H_D#28	Y9	H_D#_28	
H_D#29	P4	H_D#_29	
H_D#30	W3	H_D#_30	
H_D#31	N1	H_D#_31	
H_D#32	AD12	H_D#_32	
H_D#33	AE3	H_D#_33	
H_D#34	AD9	H_D#_34	
H_D#35	AC9	H_D#_35	
H_D#36	AC7	H_D#_36	
H_D#37	AC14	H_D#_37	
H_D#38	AD11	H_D#_38	
H_D#39	AC11	H_D#_39	
H_D#40	AD7	H_D#_40	
H_D#41	AD7	H_D#_41	
H_D#42	AB1	H_D#_42	
H_D#43	Y3	H_D#_43	
H_D#44	AC8	H_D#_44	
H_D#45	AE2	H_D#_45	
H_D#46	AC5	H_D#_46	
H_D#47	AB9	H_D#_47	
H_D#48	AC3	H_D#_48	
H_D#49	AH8	H_D#_49	
H_D#50	AJ14	H_D#_50	
H_D#51	AE9	H_D#_51	
H_D#52	AE11	H_D#_52	
H_D#53	AH12	H_D#_53	
H_D#54	AJ5	H_D#_54	
H_D#55	AI5	H_D#_55	
H_D#56	AJ6	H_D#_56	
H_D#57	AE7	H_D#_57	
H_D#58	AJZ	H_D#_58	
H_D#59	AJZ	H_D#_59	
H_D#60	AE5	H_D#_60	
H_D#61	AJ3	H_D#_61	
H_D#62	AH2	H_D#_62	
H_D#63	AH13	H_D#_63	
H_SWING	B3		
H_RCAMP	C2		
H_SCOMP	W1		
H_SCOMP#	W2		
H_CPURST#	B6		
H_CPUSLP#	E5		
H_AVREF	B9		
H_DIVREF	A9		
H_A#_3	J13	H_A#3	
H_A#_4	B11	H_A#4	
H_A#_5	C11	H_A#5	
H_A#_6	M11	H_A#6	
H_A#_7	C15	H_A#7	
H_A#_8	F16	H_A#8	
H_A#_9	L13	H_A#9	
H_A#_10	G17	H_A#10	
H_A#_11	C14	H_A#11	
H_A#_12	B13	H_A#12	
H_A#_13	L16	H_A#13	
H_A#_14	J17	H_A#14	
H_A#_15	K16	H_A#15	
H_A#_16	B14	H_A#16	
H_A#_17	K18	H_A#17	
H_A#_18	P15	H_A#18	
H_A#_19	R17	H_A#19	
H_A#_20	B16	H_A#20	
H_A#_21	H20	H_A#21	
H_A#_22	L19	H_A#22	
H_A#_23	D17	H_A#23	
H_A#_24	M17	H_A#24	
H_A#_25	N16	H_A#25	
H_A#_26	J19	H_A#26	
H_A#_27	B18	H_A#27	
H_A#_28	F19	H_A#28	
H_A#_29	B17	H_A#29	
H_A#_30	B15	H_A#30	
H_A#_31	E17	H_A#31	
H_A#_32	C18	H_A#32	
H_A#_33	A19	H_A#33	
H_A#_34	B19	H_A#34	
H_A#_35	N19	H_A#35	
H_ADS#	G12	H_ADS#	3
H_ADSTB#_0	H17	H_ADSTB#0	3
H_ADSTB#_1	G20	H_ADSTB#1	3
H_BNR#	C8	H_BNR#	3
H_BPRE#	E8	H_BPRE#	3
H_BREQ#	F12	H_BREQ#	3
H_DEFER#	D6	H_DEFER#	3
H_DBSY#	C10	H_DBSY#	3
HPLL_CLK#	AM5	CLK_MCH_BCLK#	21
HPLL_CLK#	AM7	CLK_MCH_BCLK#	21
H_DPWR#	H8	H_DPWR#	3
H_DRDY#	K7	H_DRDY#	3
H_HIT#	E4	H_HIT#	3
H_HITM#	C6	H_HITM#	3
H_LOCK#	G10	H_LOCK#	3
H_TRDY#	B7	H_TRDY#	3
H_DINV#_0	K5	H_DINV#0	3
H_DINV#_1	L2	H_DINV#1	3
H_DINV#_2	AD13	H_DINV#2	3
H_DINV#_3	AE13	H_DINV#3	3
H_DSTBN#_0	M7	H_DSTBN#0	3
H_DSTBN#_1	K3	H_DSTBN#1	3
H_DSTBN#_2	AD2	H_DSTBN#2	3
H_DSTBN#_3	AH11	H_DSTBN#3	3
H_DSTBP#_0	L7	H_DSTBP#0	3
H_DSTBP#_1	K2	H_DSTBP#1	3
H_DSTBP#_2	AC2	H_DSTBP#2	3
H_DSTBP#_3	AJ10	H_DSTBP#3	3
H_REQ#_0	M14	H_REQ#0	3
H_REQ#_1	E13	H_REQ#1	3
H_REQ#_2	A11	H_REQ#2	3
H_REQ#_3	H13	H_REQ#3	3
H_REQ#_4	B12	H_REQ#4	3
H_RS#_0	E12	H_RS#0	3
H_RS#_1	D7	H_RS#1	3
H_RS#_2	D8	H_RS#2	3

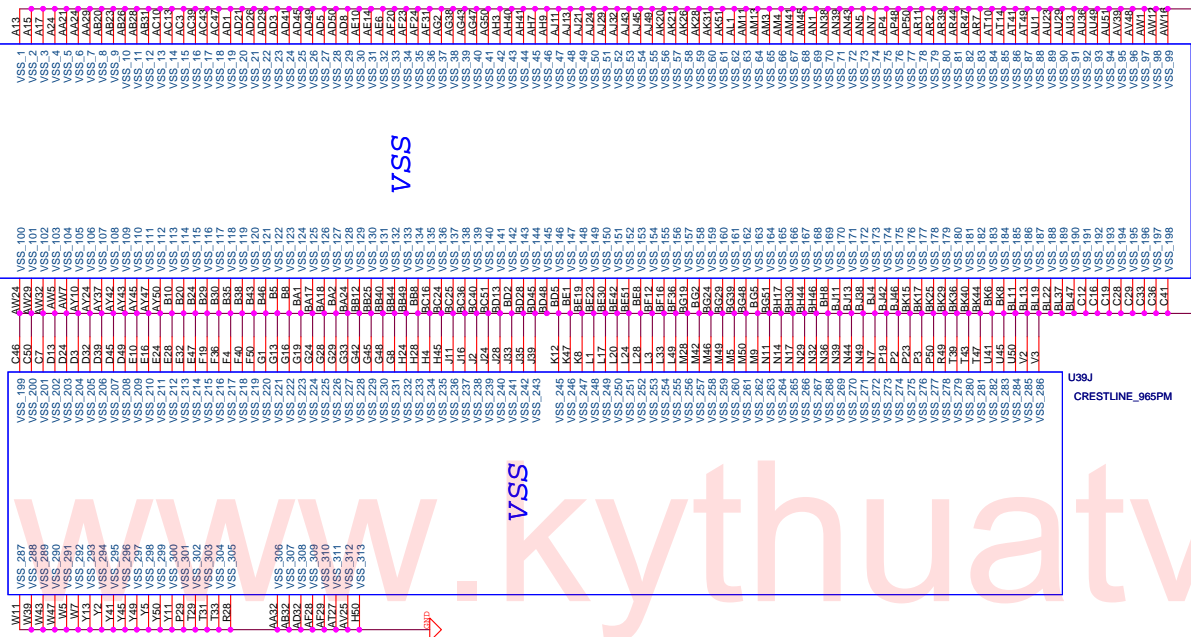


HOST

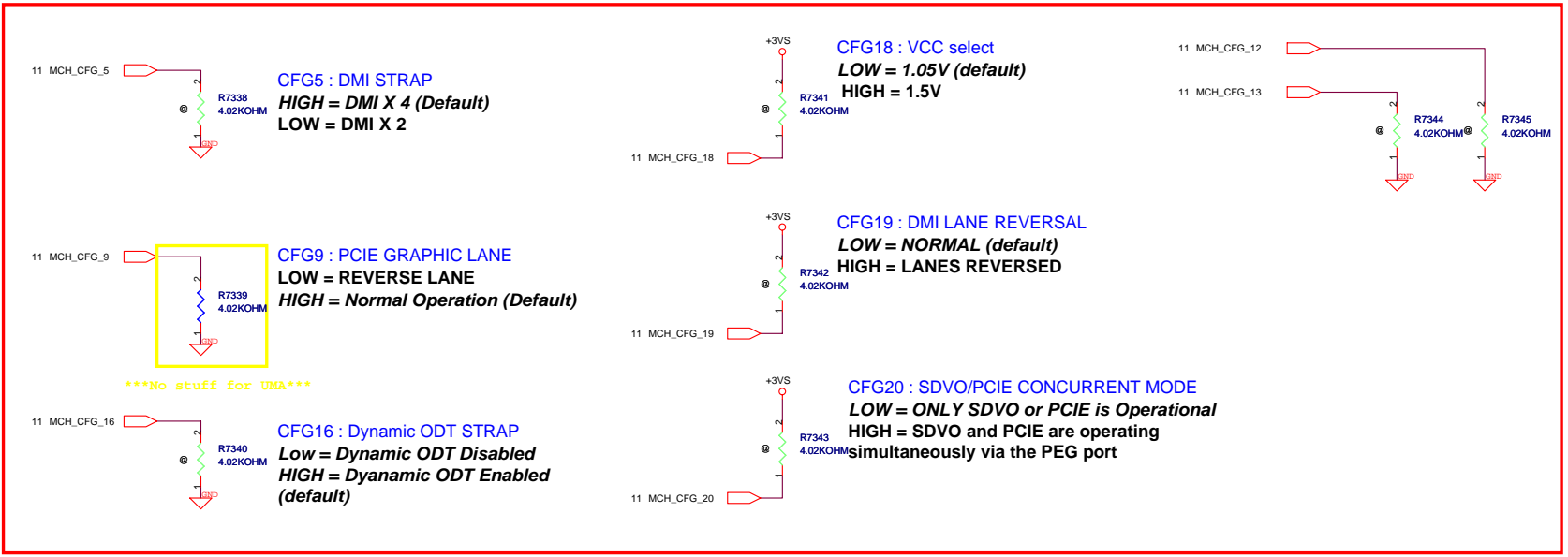


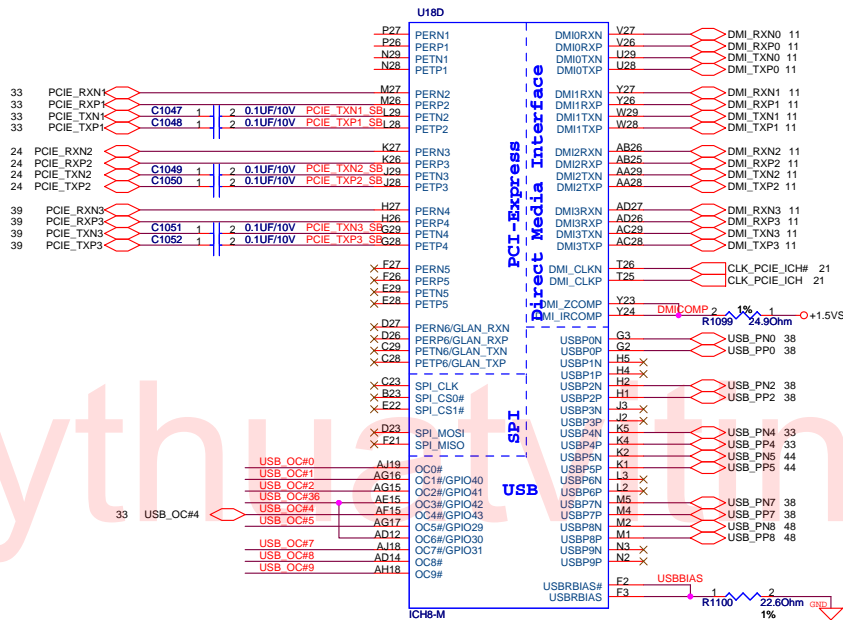
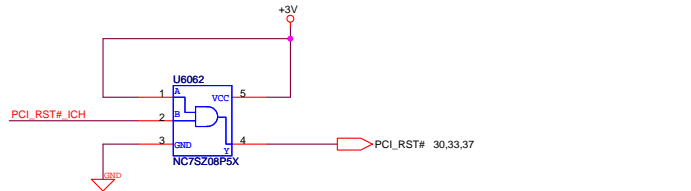
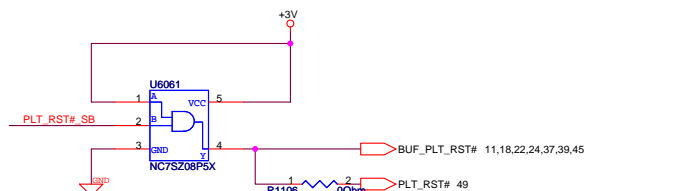
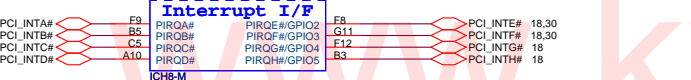
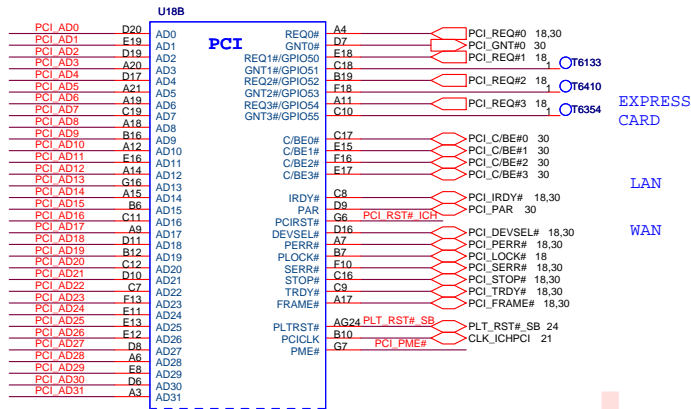






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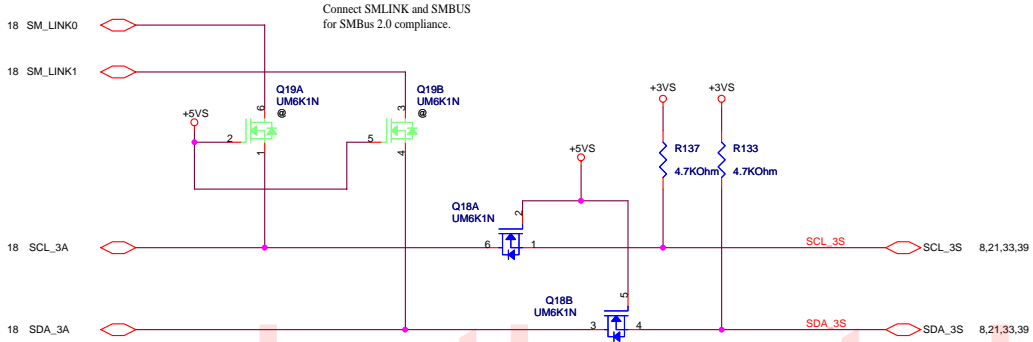


Place within 500 mils of ICH

0: I/O
 1:
 2: I/O
 3:
 4: NewCard
 5: BT
 6:
 7: I/O
 8: CMOS
 9: @

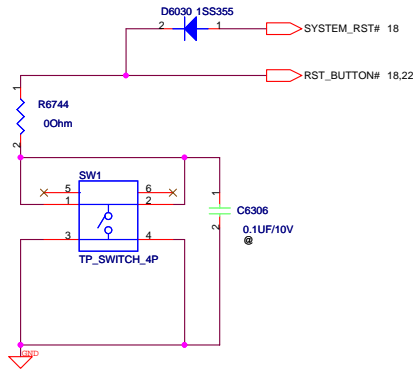
Place within 500 mils of ICH

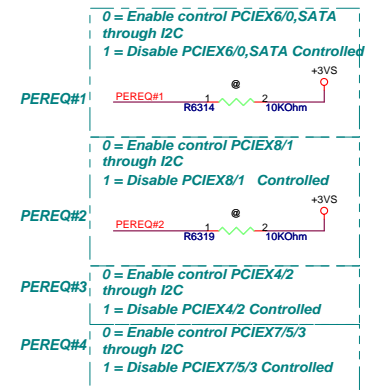
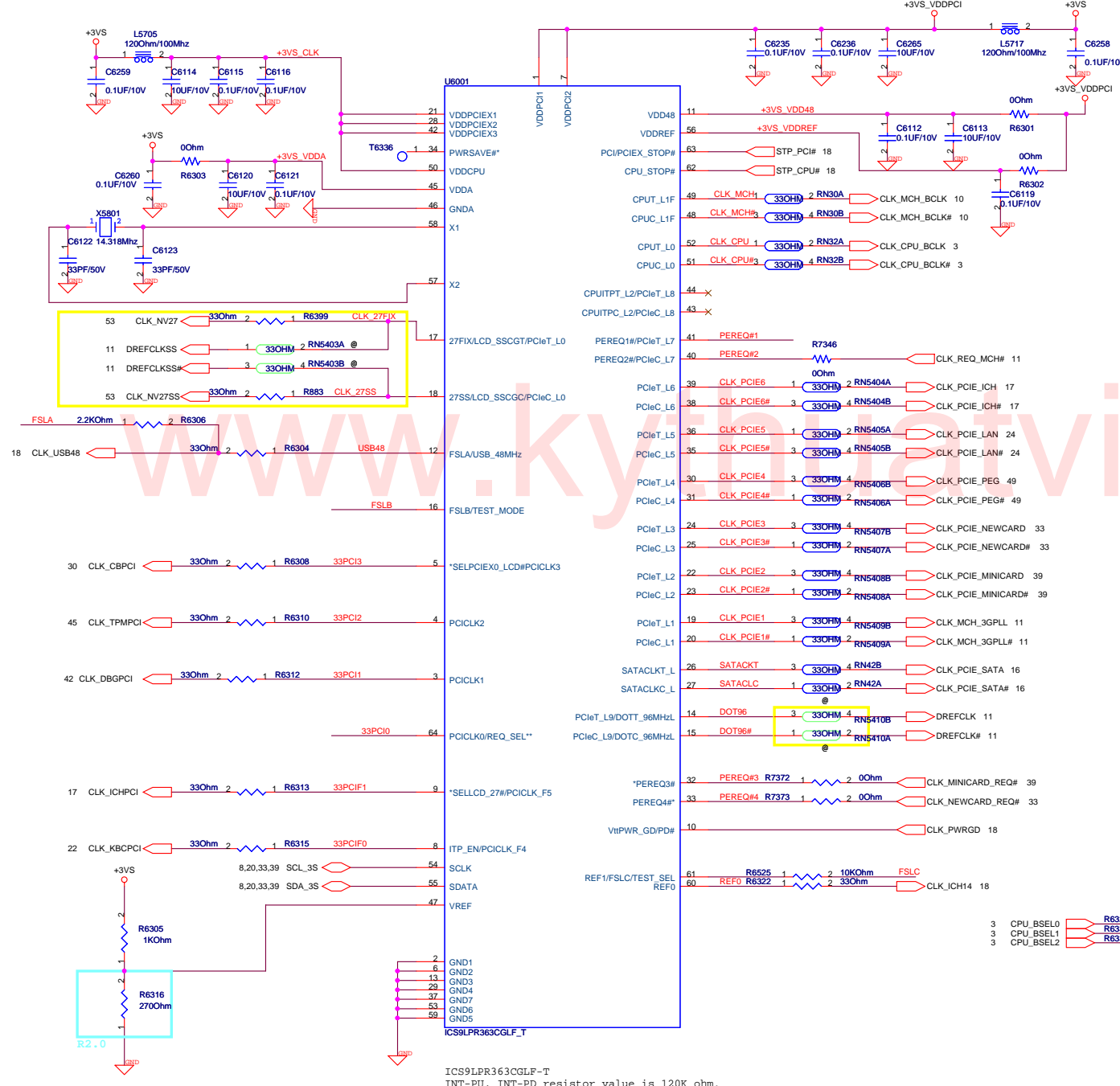
ICH8-M



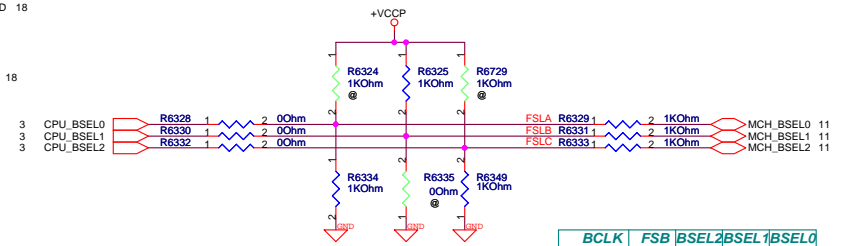
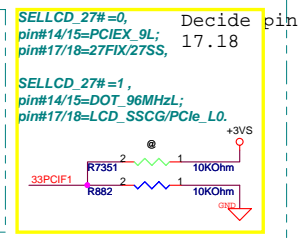
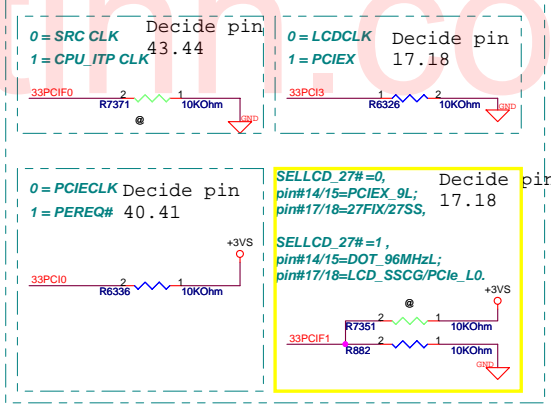
ICH8-M

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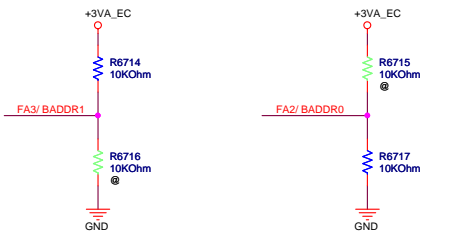
Latched Input Select



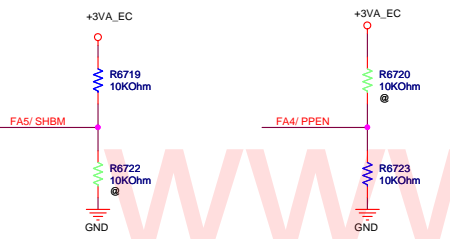
BCLK	FSB	BSEL2	BSEL1	BSEL0
CPU Driven	/	/	/	/
166	667	0	1	1
200	800	0	1	0

ICS9LPR363CGLF-T
INT-PU, INT-PD resistor value is 120K ohm.

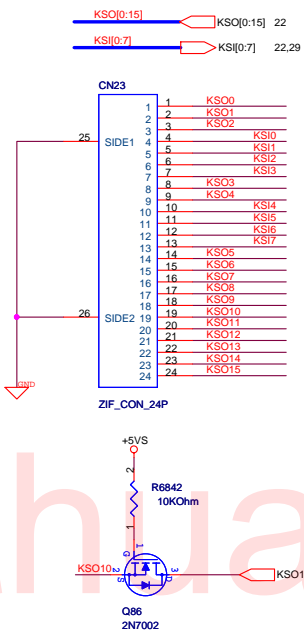
10:Determined by EC



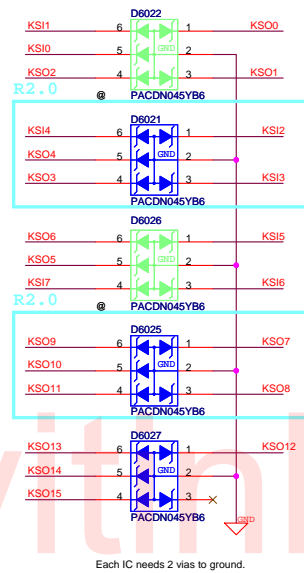
FA3/ BADDR1:sect LPC address: 4E/4F
FA2/ BADDR0 :sect LPC address:2E/2F



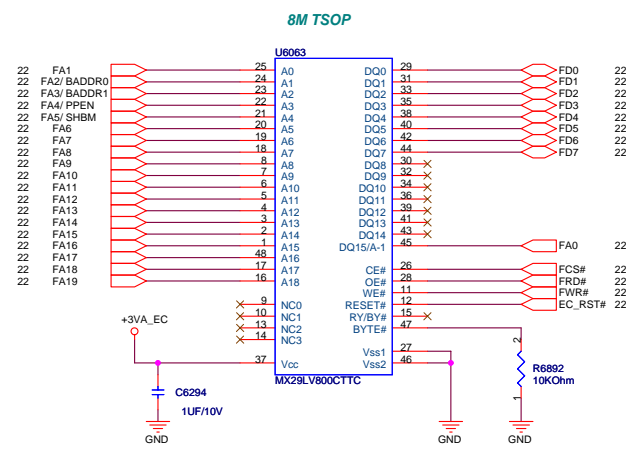
FA5/ SHBM:share BIOS mode enable.
FA4/ PPEN:enable in-system program via parallel port interface.(KBS down)



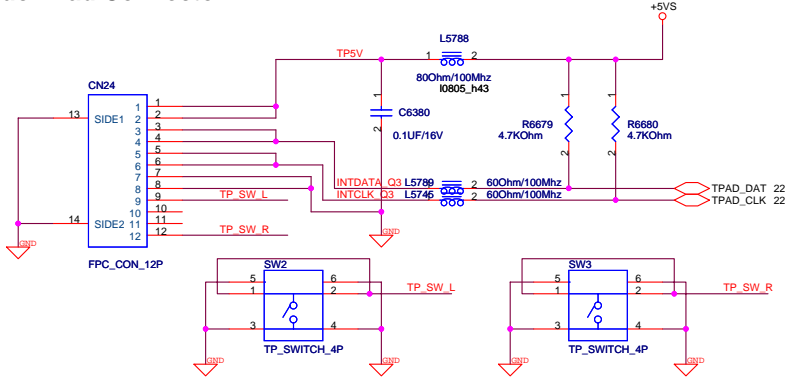
EMI recommendation: To protect KBC destroy by ESD. Need put between KB connector and KBC, and close to the connector as possible.



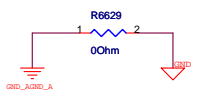
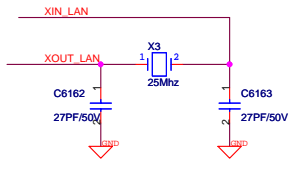
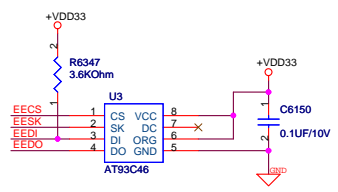
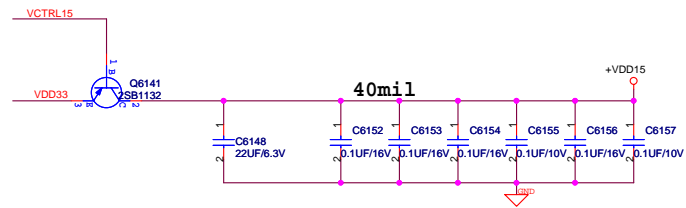
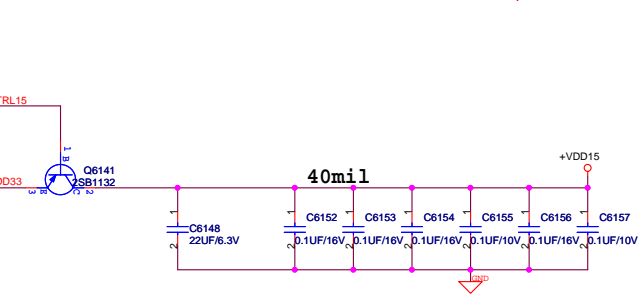
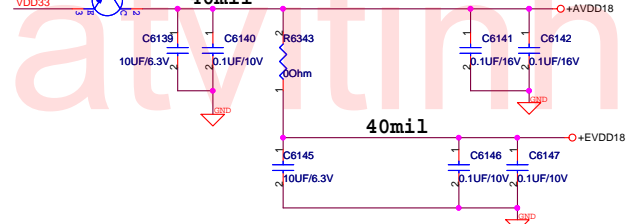
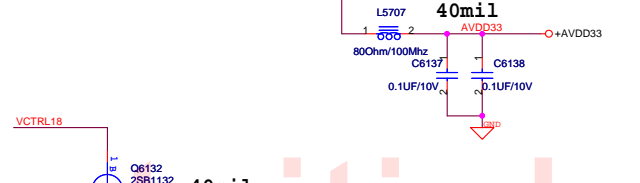
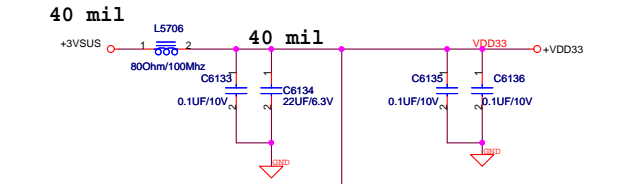
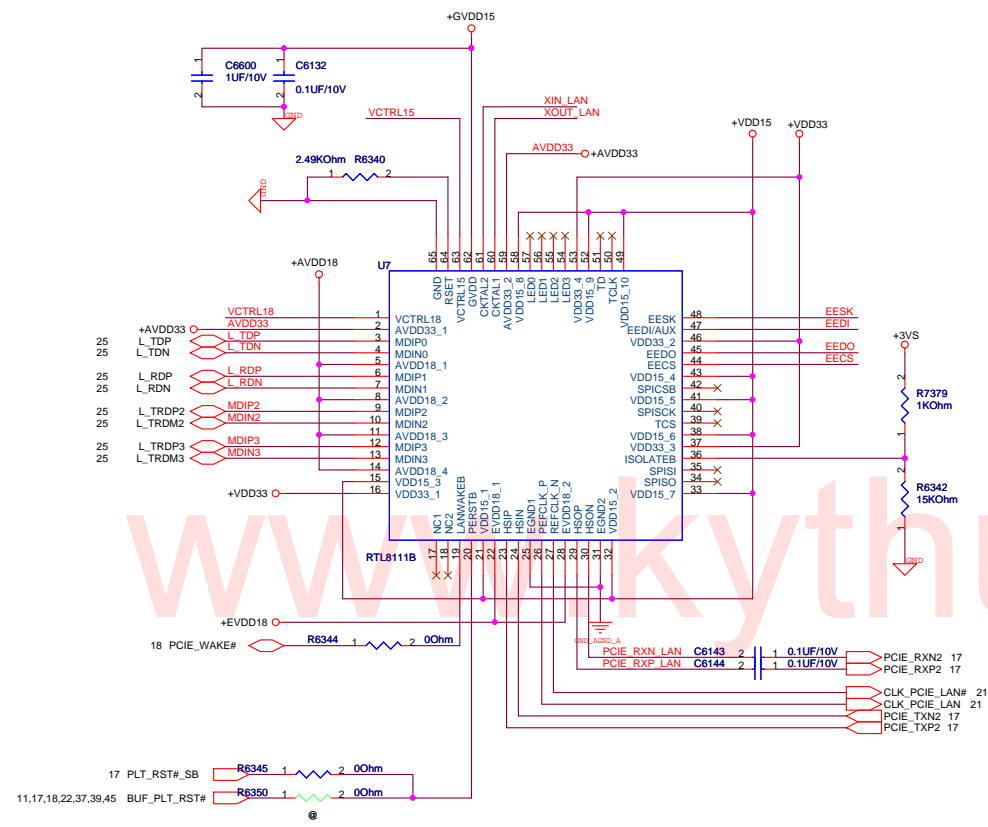
8M-ROM

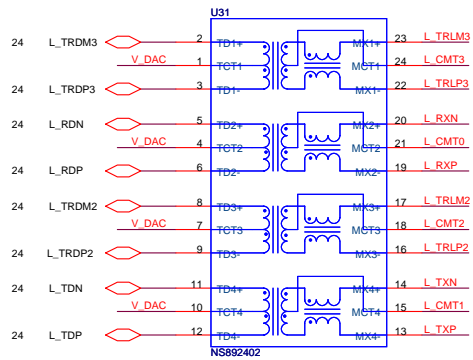


Touch Pad Connector

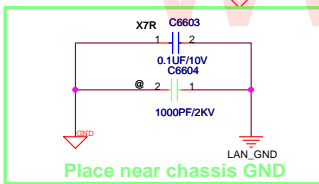
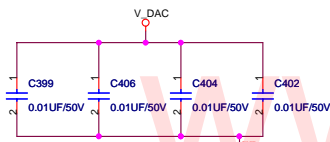


Average supply current
 VDD33 103mA
 AVDD18+E'VDD18 198mA
 VDD15 367mA

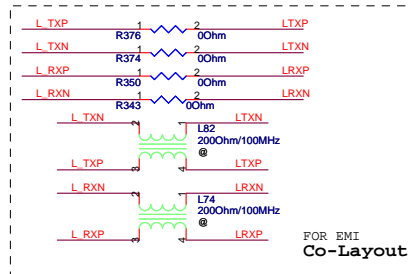
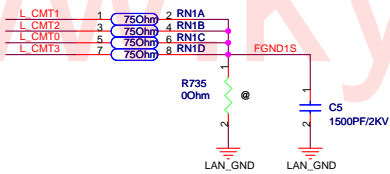




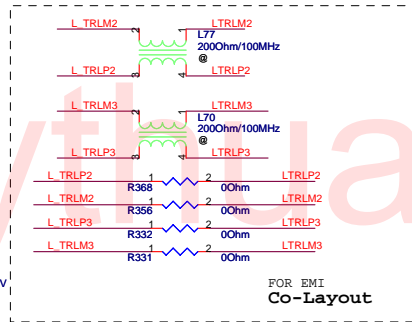
Transformer close CON7



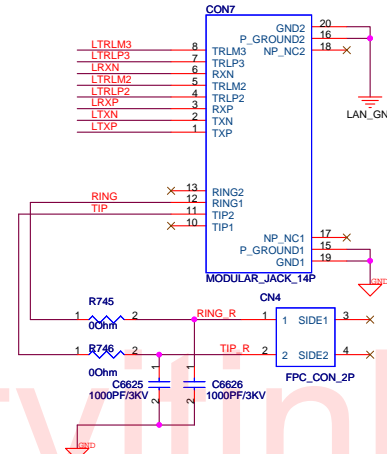
Place near chassis GND



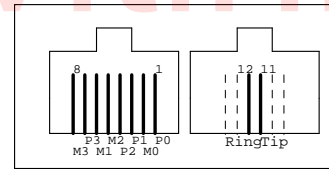
FOR EMI Co-Layout



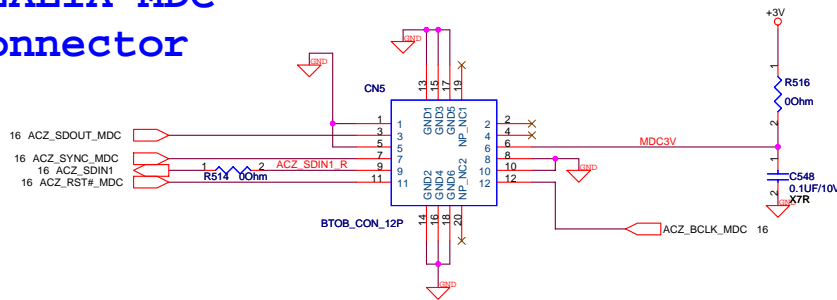
FOR EMI Co-Layout

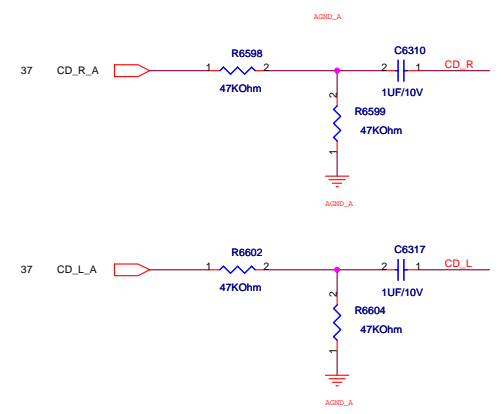
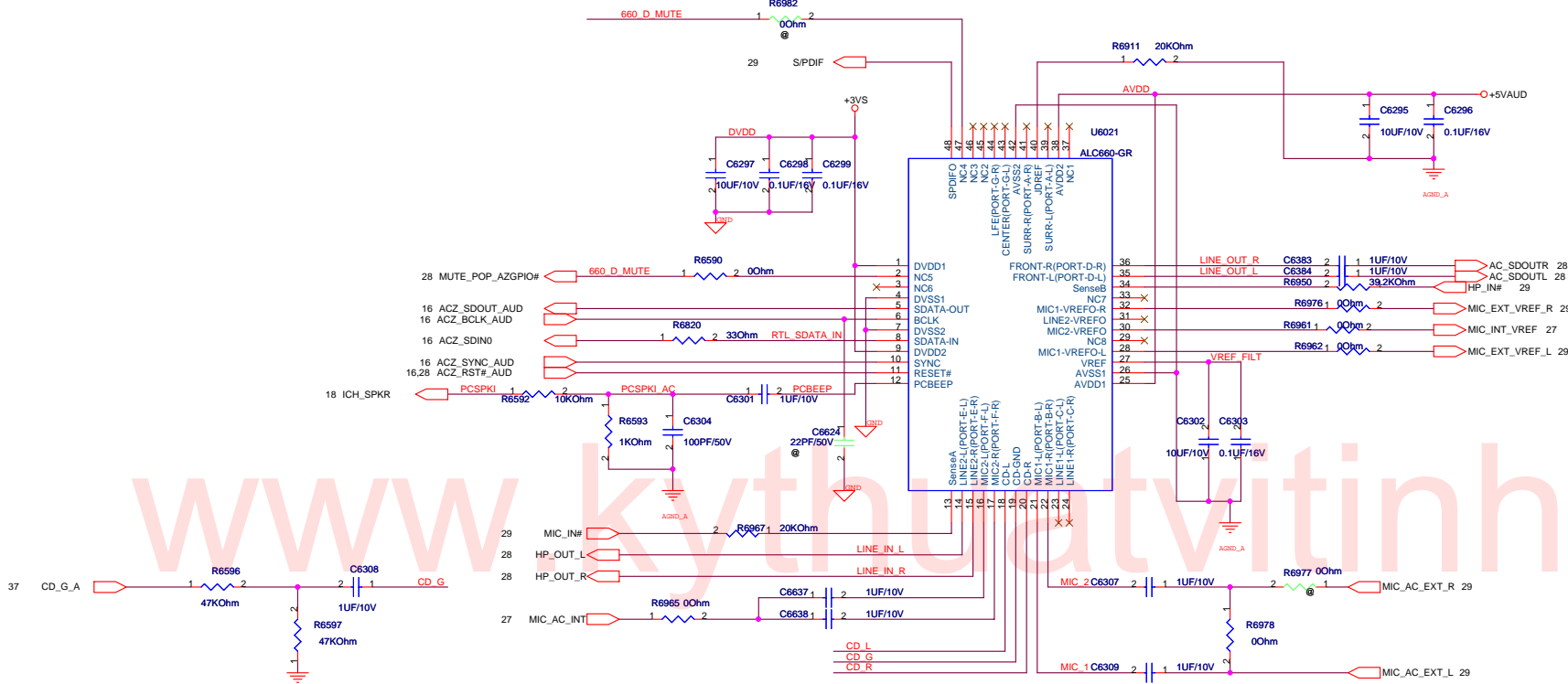


LAN Modem

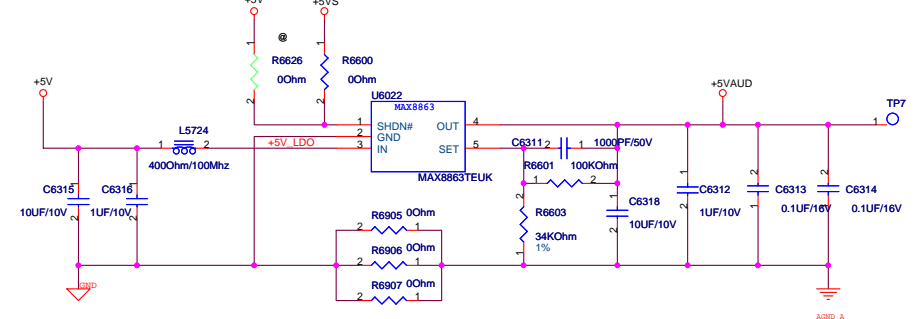


AZALIA MDC Connector

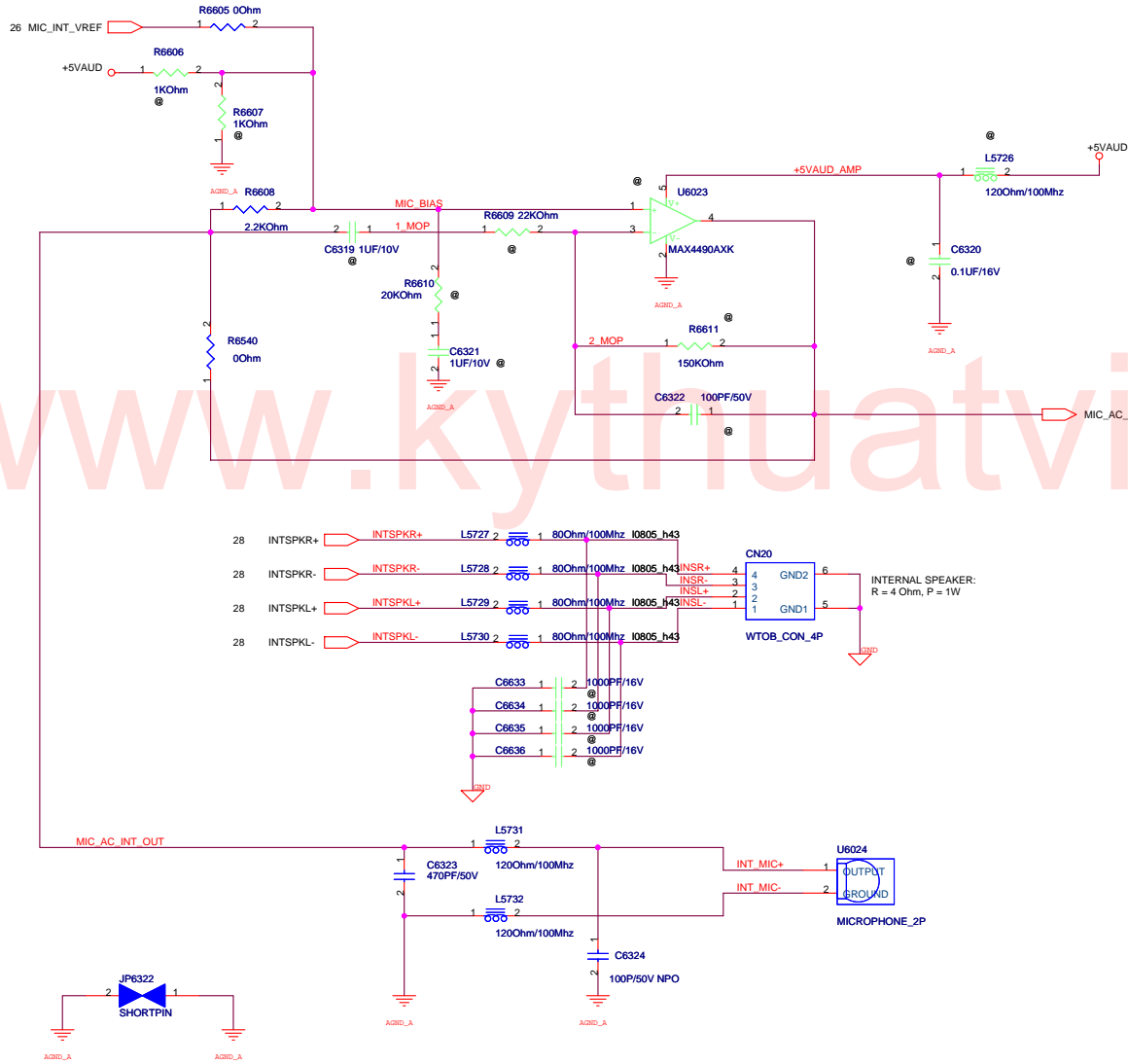




AUDIO_LDO



MIC PreAmp & Mic Jack

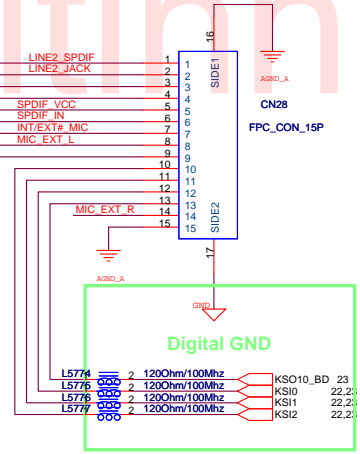
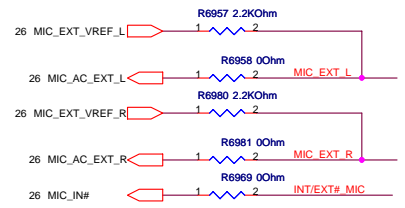
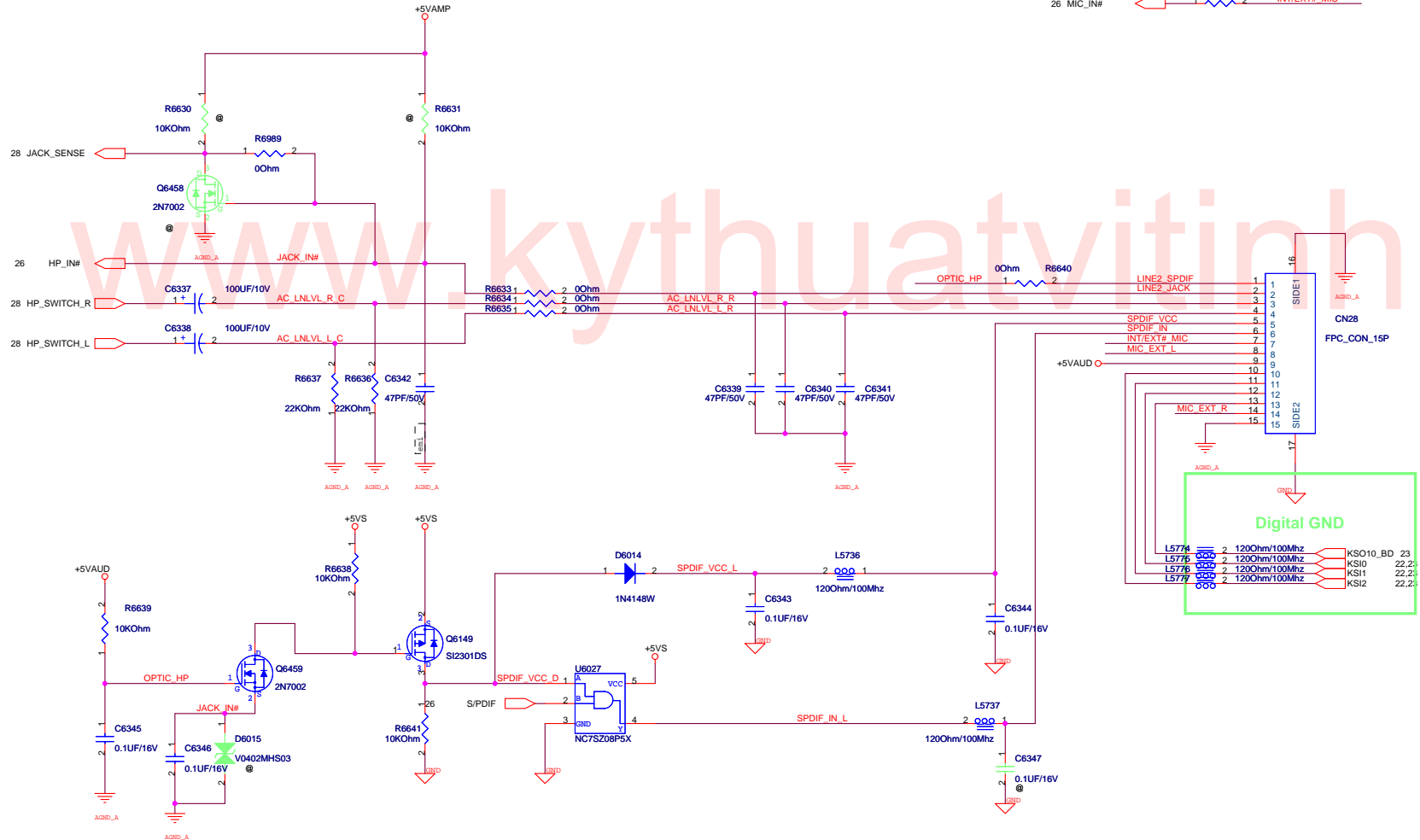


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<Variant Name>

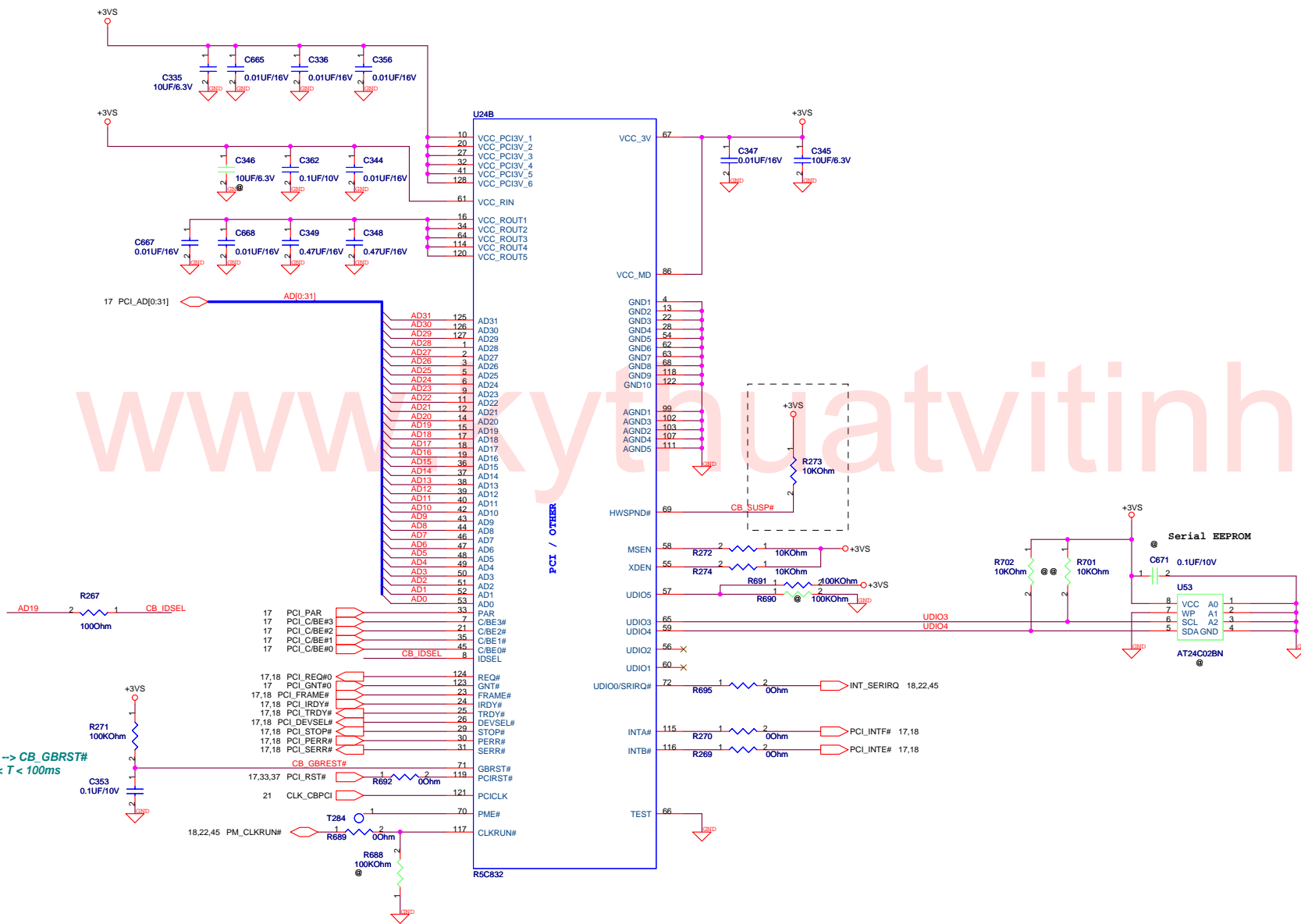
ASUS		Title : MIC PREAMP & INT MIC
ASUSTeK COMPUTER INC		Engineer:
Size	Project Name	Rev
Custom	T76S	2.0
Date: Tuesday, August 21, 2007		Sheet 27 of 70

JACK_IN#	OPTIC_HP	SPDIF
L	H	LINE OUT
L	L	NO CONNECT
H	H	NO CONNECT

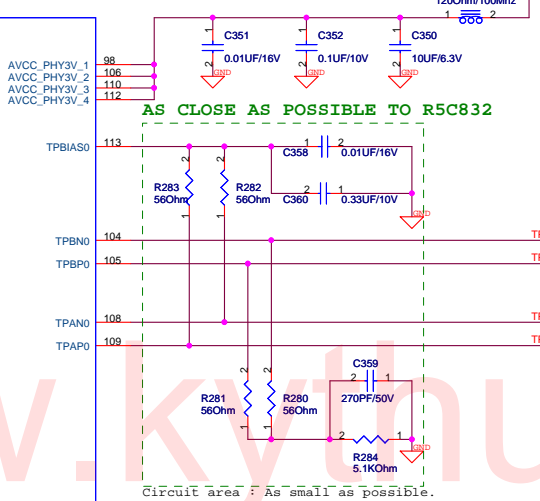
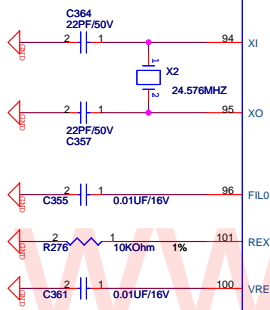


<Variant Name>

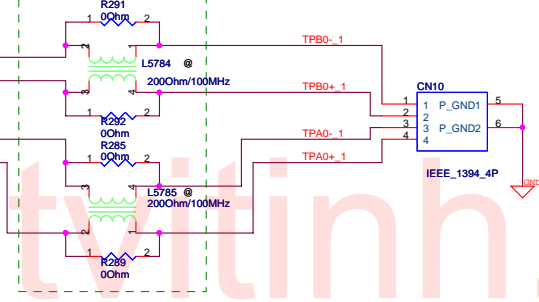
ASUS		Title : SPDIF JACK
ASUSTek COMPUTER INC		Engineer:
Size Custom	Project Name T76S	Rev 2.0
Date: Tuesday, August 21, 2007		Sheet 29 of 70



as close as possible to R5C832

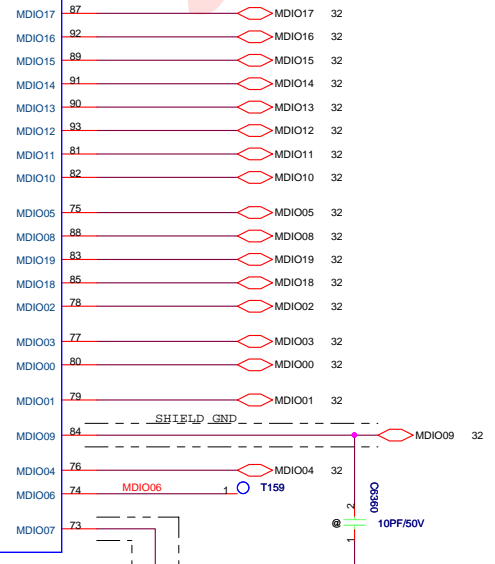


AS CLOSE AS POSSIBLE TO .1394-CONNECTOR



IEEE1394 / SD

Circuit area : As small as possible.

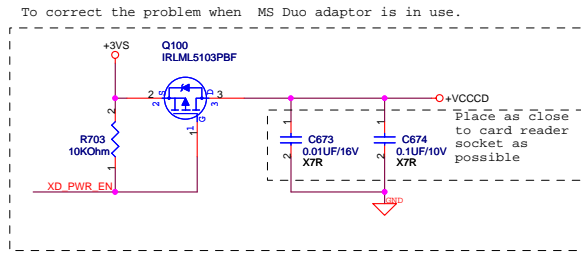
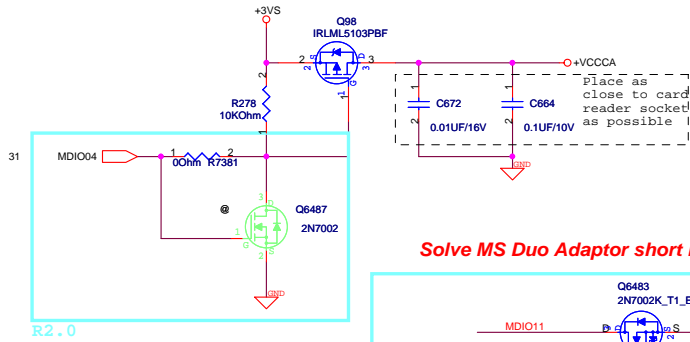


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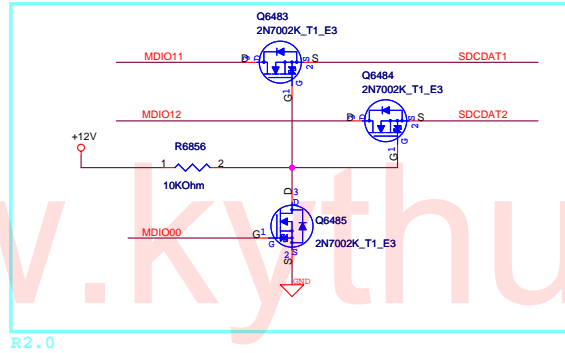
MDIO02--> xDCE#
MDIO05--> SD Power Control 1 / xDWP
MDIO06--> xD/MS/SD LED Control
MDIO14--> xD Data
MDIO15--> xD Data
MDIO16--> xD Data
MDIO17--> xD Data
MDIO18--> xD CLE
MDIO19--> xD ALE
    
```

```

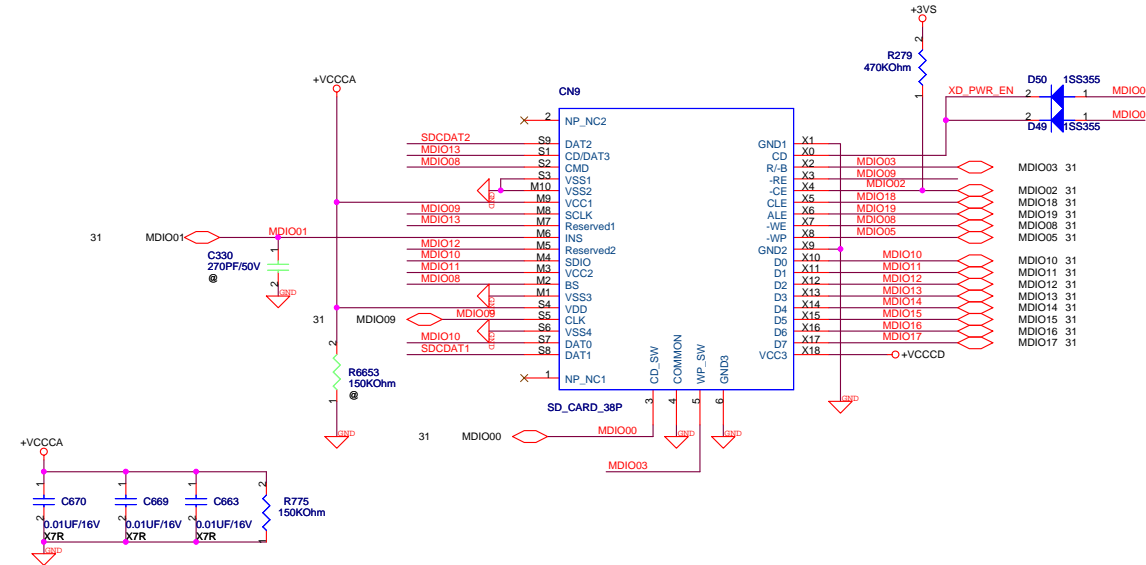
MDIO01--> MS Card Detect
MDIO03--> SD Write Protect
MDIO04--> SD Card Power0 Control/
MS Power Control
MDIO07--> SD External Clock/
MS External Clock
MDIO08--> SD Command/MS Bus State
MDIO09--> SD Clock/MS Clock
MDIO10--> SD Data 0/MS Data 0
MDIO11--> SD Data 1/MS Data 1
MDIO12--> SD Data 2/MS Data 2
MDIO13--> SD Data 3/MS Data 3
    
```



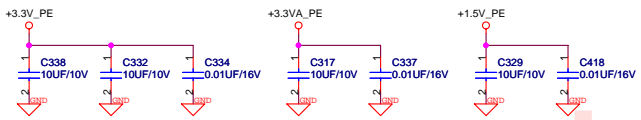
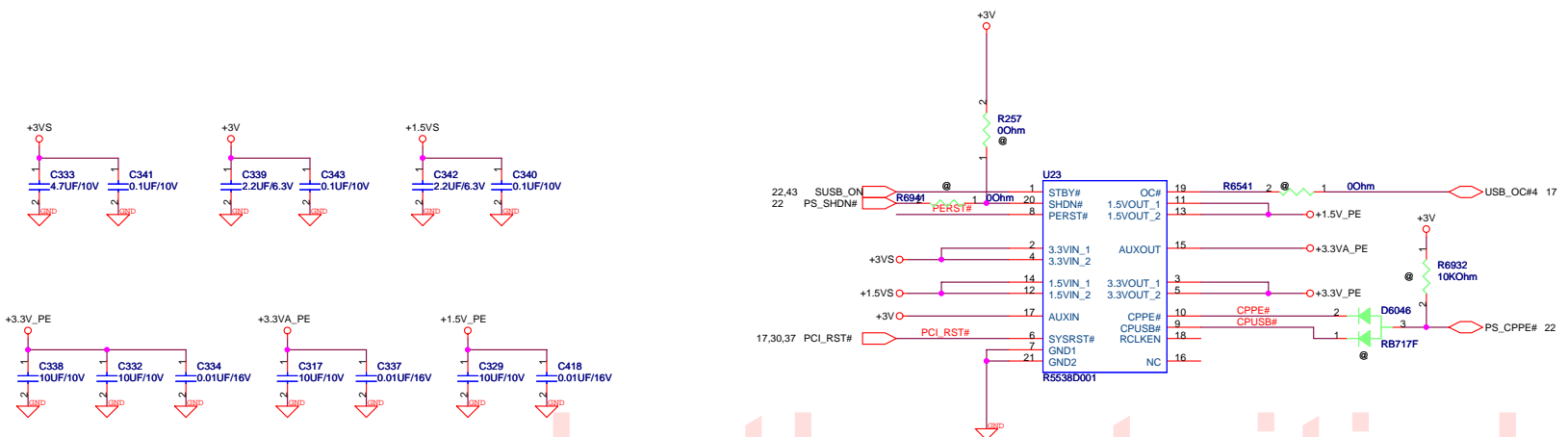
Solve MS Duo Adaptor short issue.



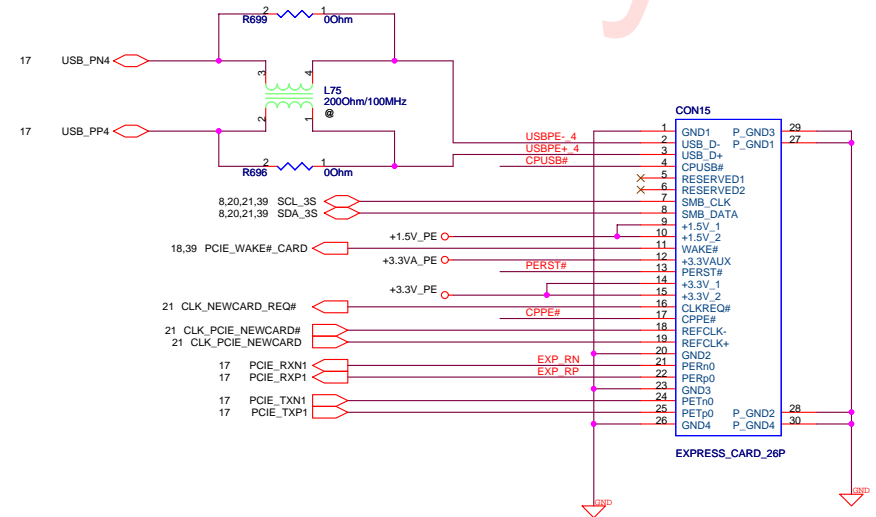
- MDIO00--> SD Card Detect
- MDIO01--> MS Card Detect
- MDIO03--> SD Write Protect
- MDIO04--> SD Card Power0 Control/
MS Power Control
- MDIO08--> SD Command/MS Bus State
- MDIO09--> SD Clock/MS Clock
- MDIO10--> SD Data 0/MS Data 0
- MDIO11--> SD Data 1/MS Data 1
- MDIO12--> SD Data 2/MS Data 2
- MDIO13--> SD Data 3/MS Data 3

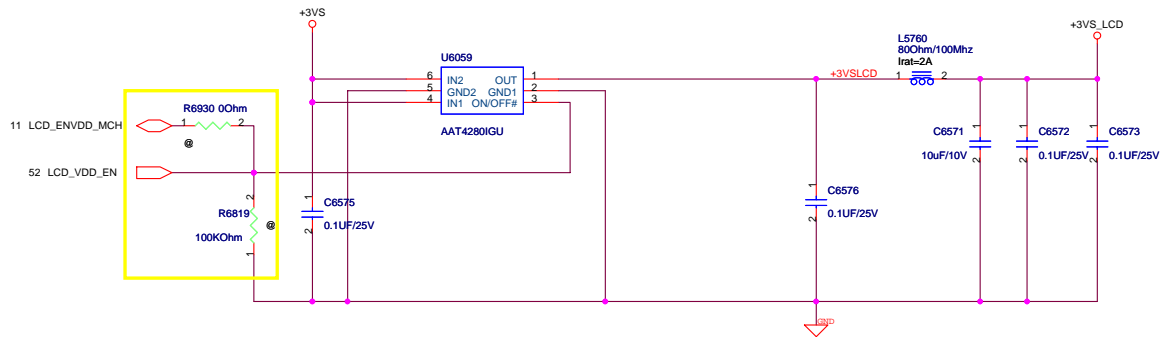


- MDIO02--> xDCE#
- MDIO05--> SD Power Control 1 / xDWP
- MDIO06--> xD/MS/SD LED Control
- MDIO14--> xD Data
- MDIO15--> xD Data
- MDIO16--> xD Data
- MDIO17--> xD Data
- MDIO18--> xD CLE
- MDIO19--> xD ALE



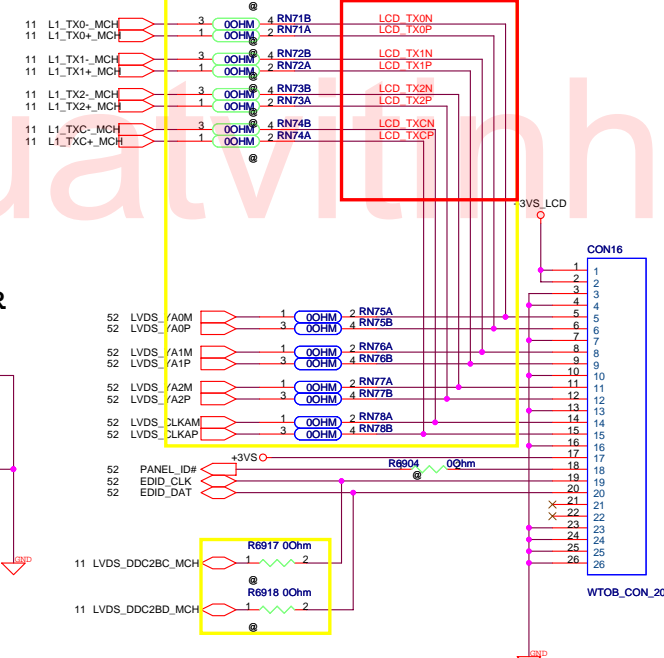
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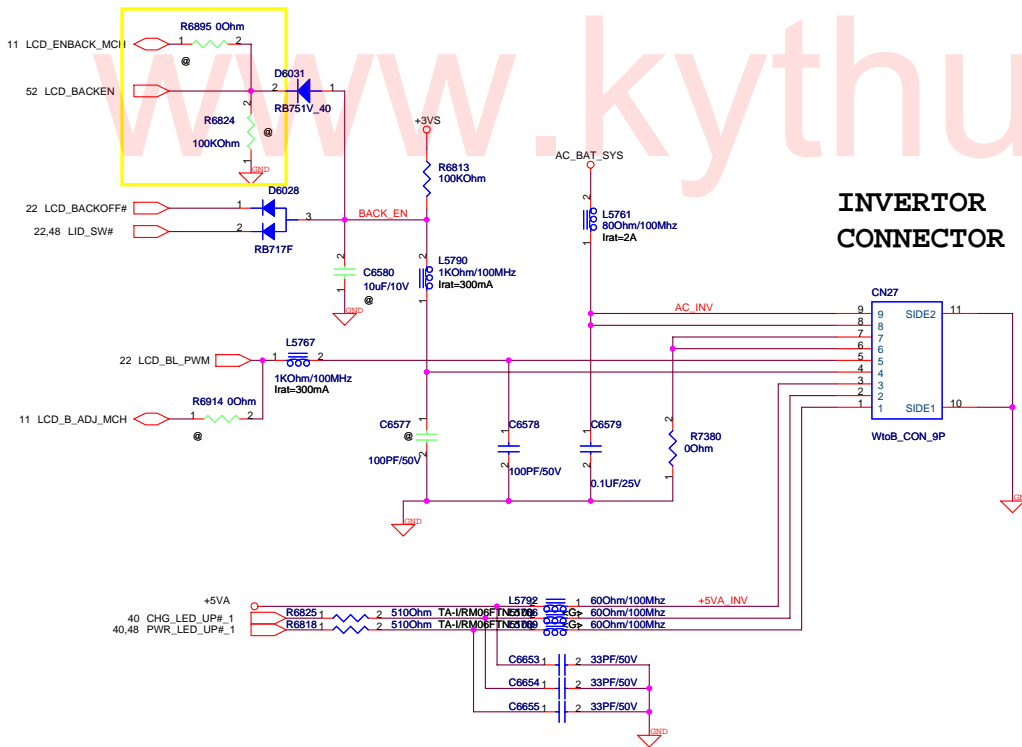


LCD CONNECTOR

Place close to CON16
As short as possible

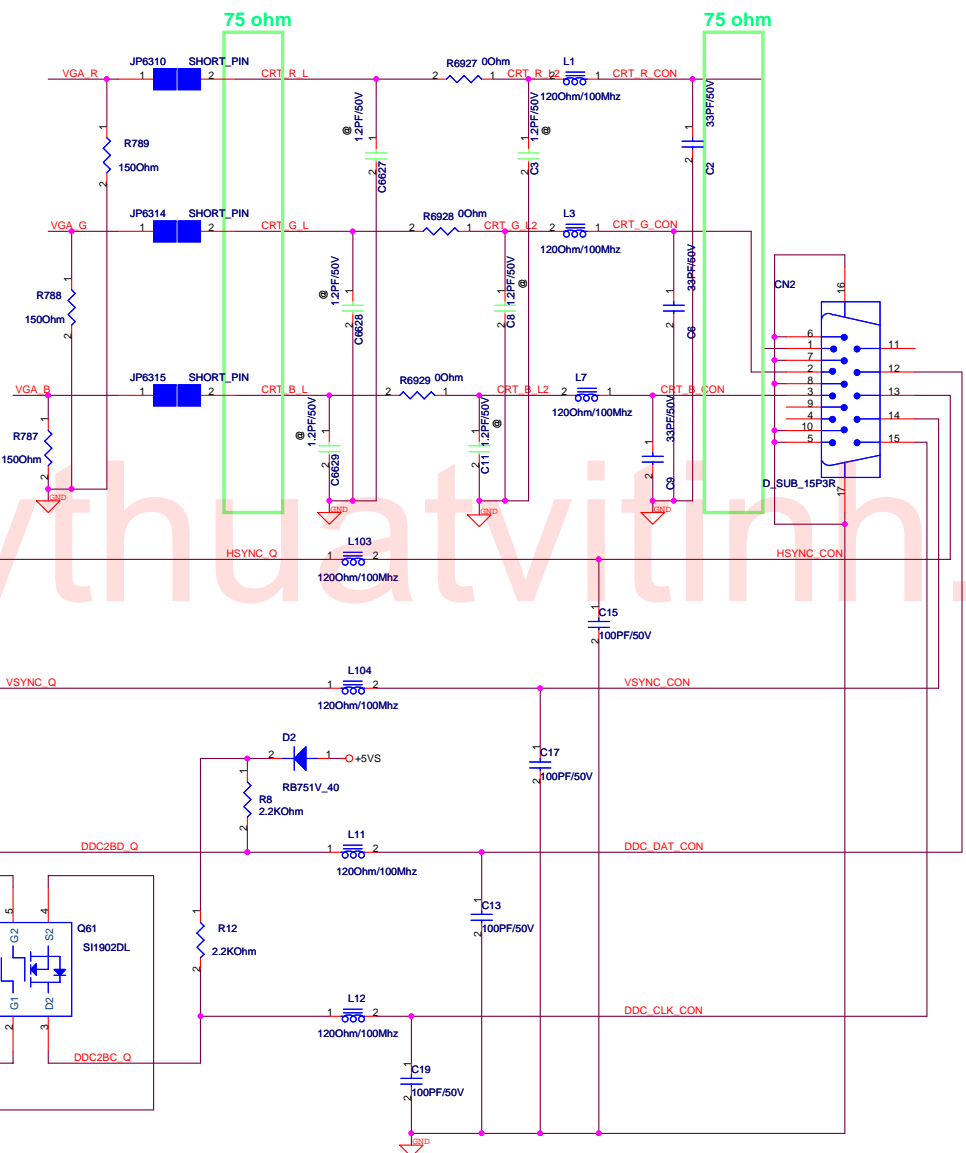
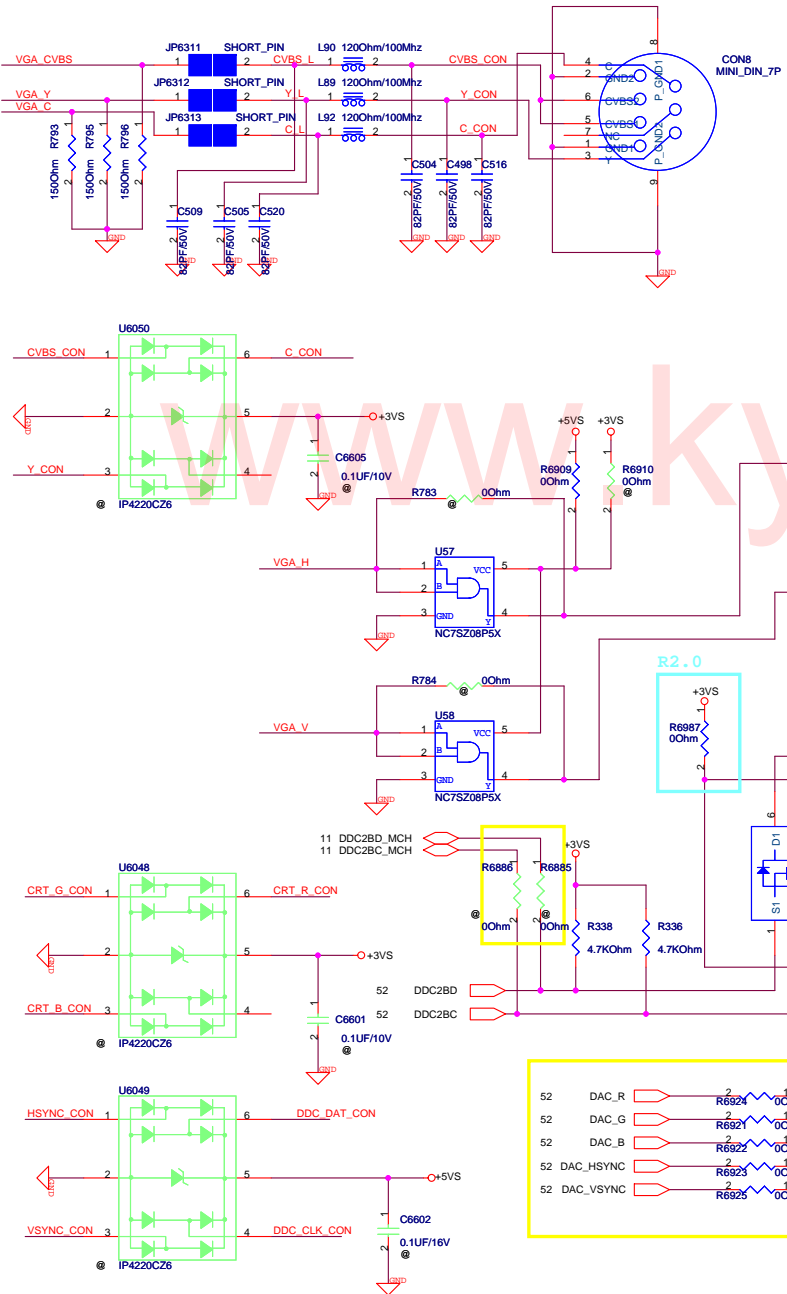


INVERTOR CONNECTOR



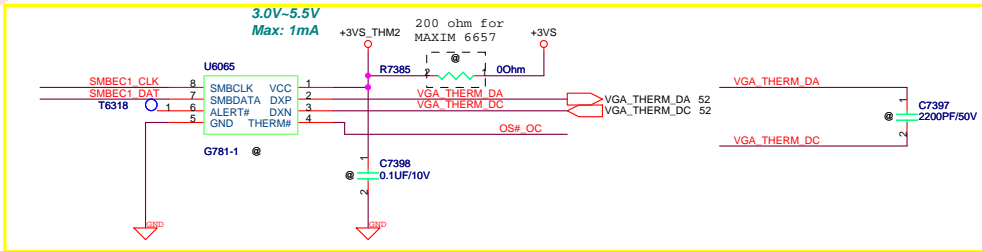
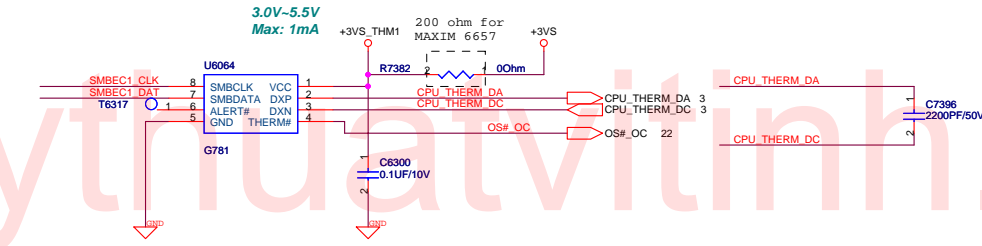
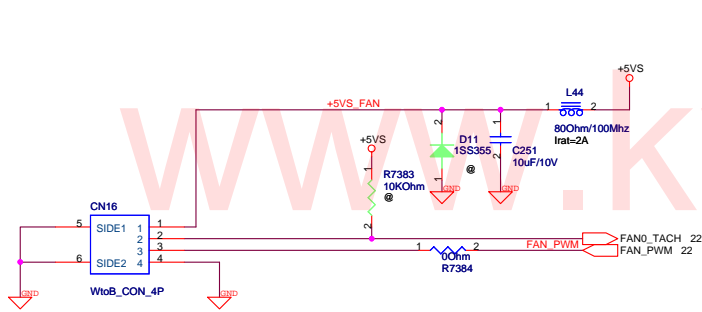
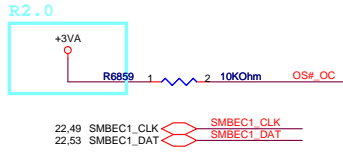
52 TV_COMP_B_PB	2	R6880	1	00hm	VGA CVBS	2	R6878	1	00hm	CVBS_MCH	11
52 TV_Y_G	1	R6884	1	00hm	VGA Y	2	R6886	1	00hm	Y_MCH	11
52 TV_C_R_PR	2	R6882	1	00hm	VGA C	2	R6883	1	00hm	C_MCH	11

TV OUT

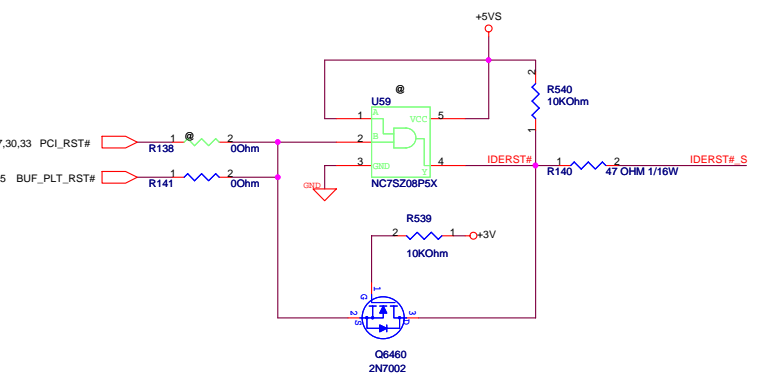
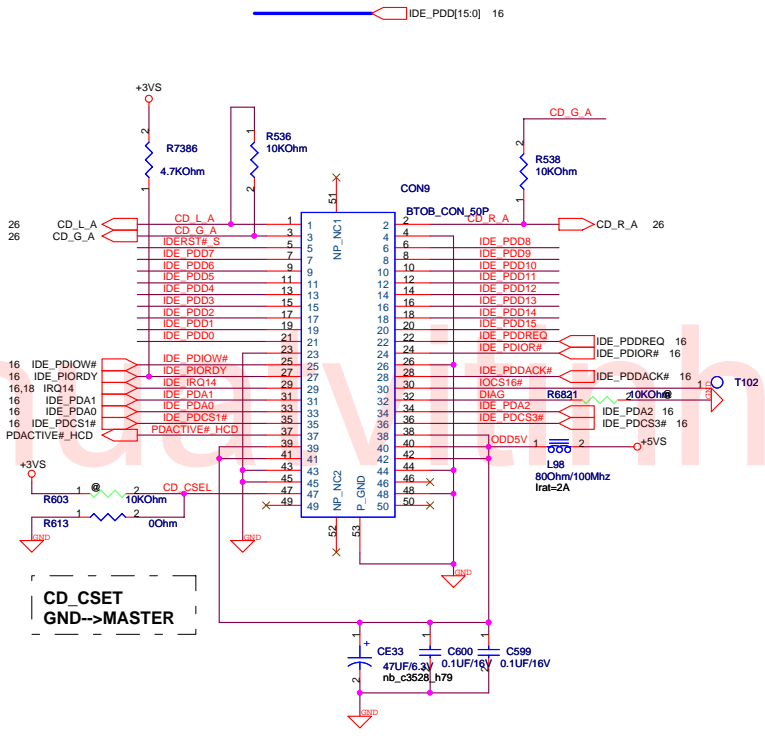
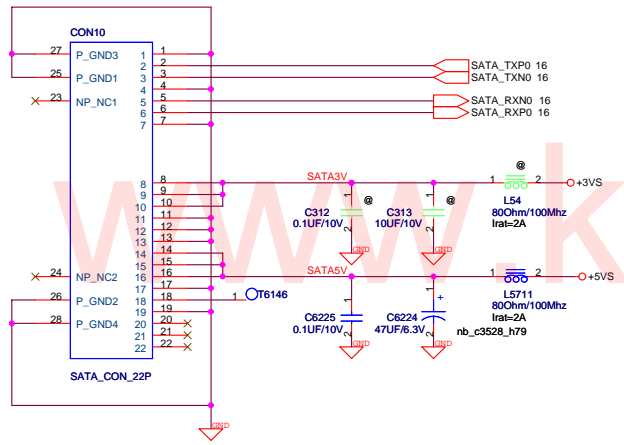


52 DAC_R	2	R6924	1	00hm	VGA R	2	R6898	1	00hm	R_MCH	11
52 DAC_G	2	R6921	1	00hm	VGA G	2	R6899	1	00hm	G_MCH	11
52 DAC_B	2	R6922	1	00hm	VGA B	2	R6920	1	00hm	B_MCH	11
52 DAC_HSYNC	2	R6923	1	00hm	VGA H	2	R6920	1	00hm	HSYNC_MCH	11
52 DAC_VSYNC	2	R6925	1	00hm	VGA V	2	R6919	1	00hm	VSYNC_MCH	11

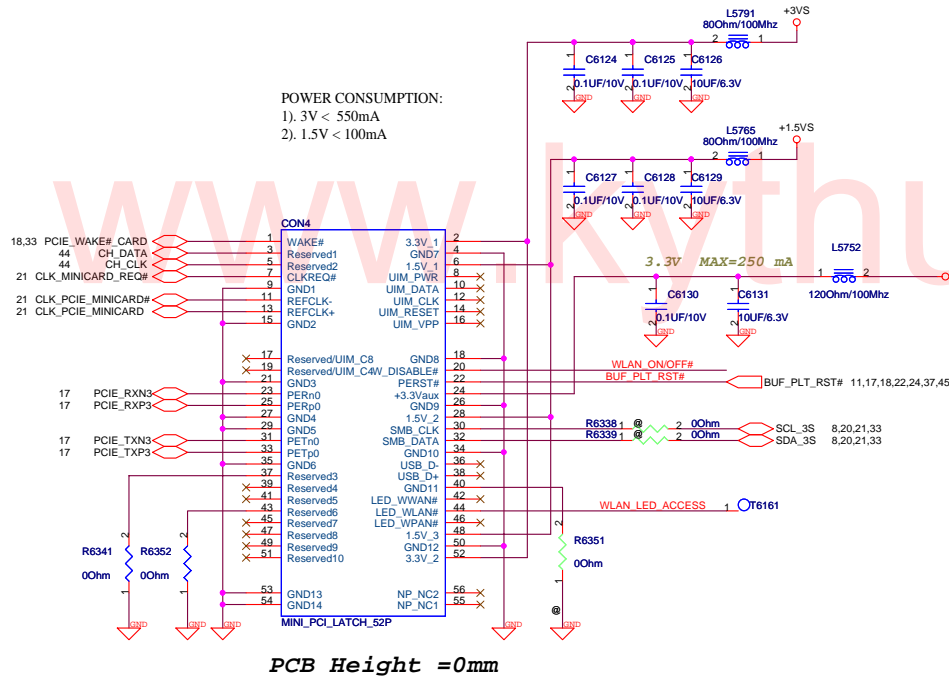
FAN & THERMAL CONTROLLER



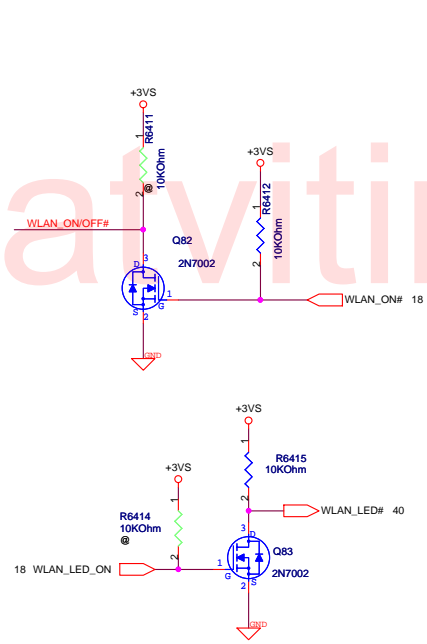
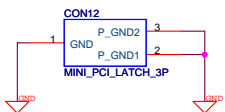
No stuff for UMA



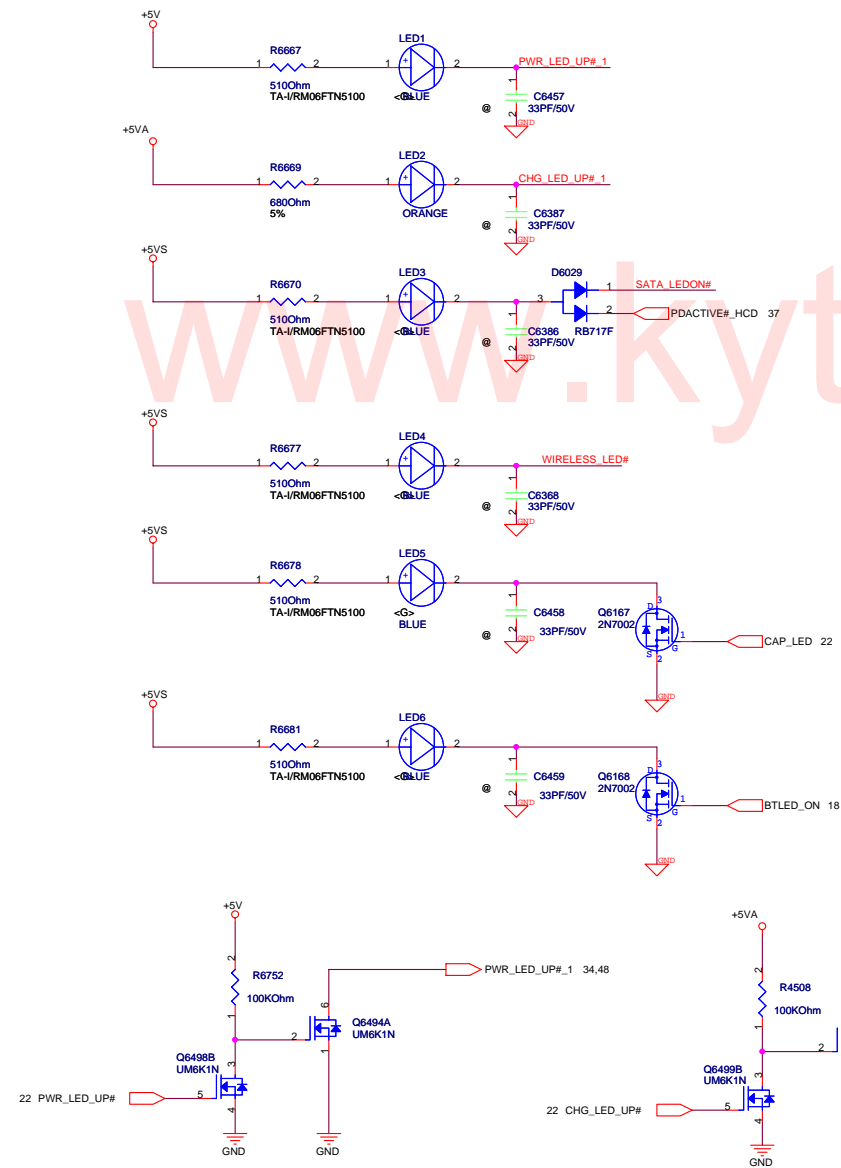
WLAN CON



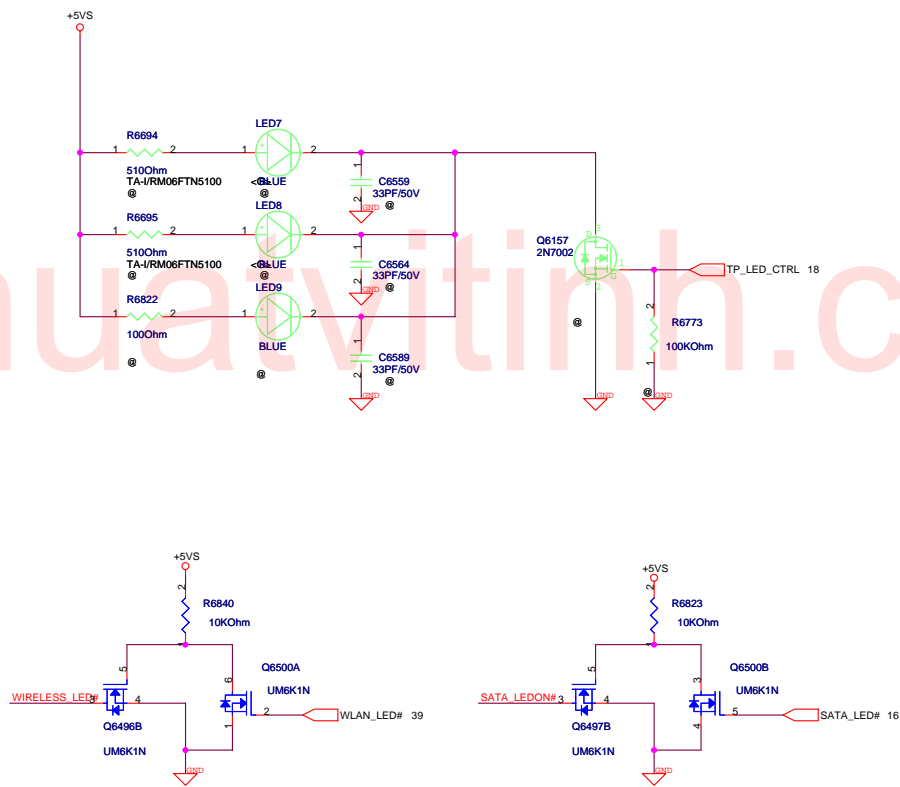
Mini Card Latch



MB/LEDs

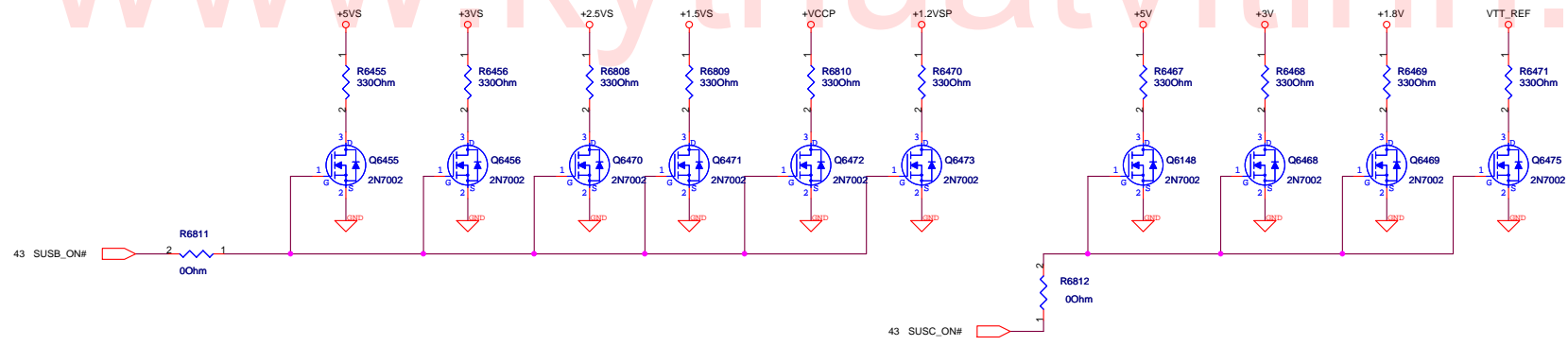


Touch Pad LED



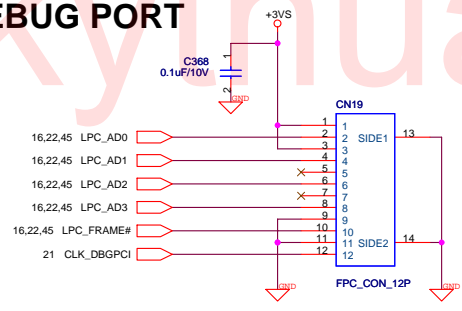
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Discharge Circuit

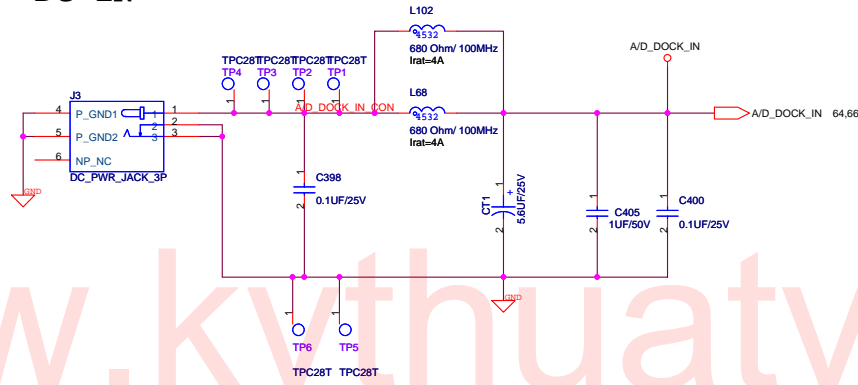


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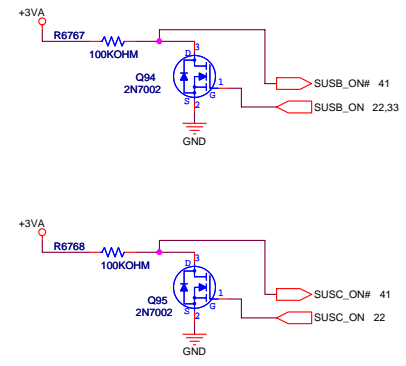
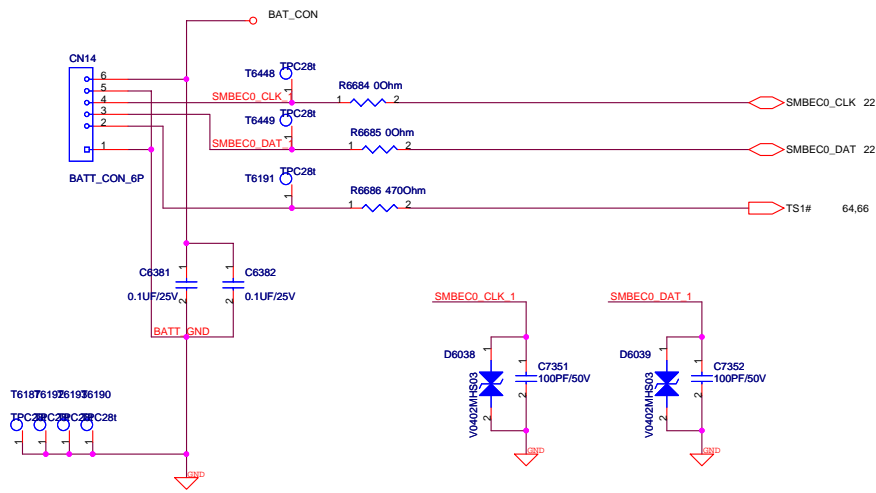
LPC DEBUG PORT



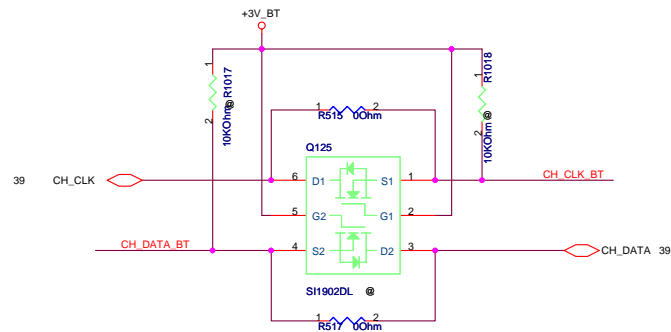
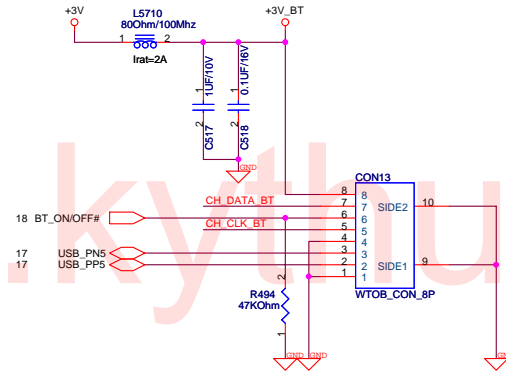
DC-IN



Battery Connector

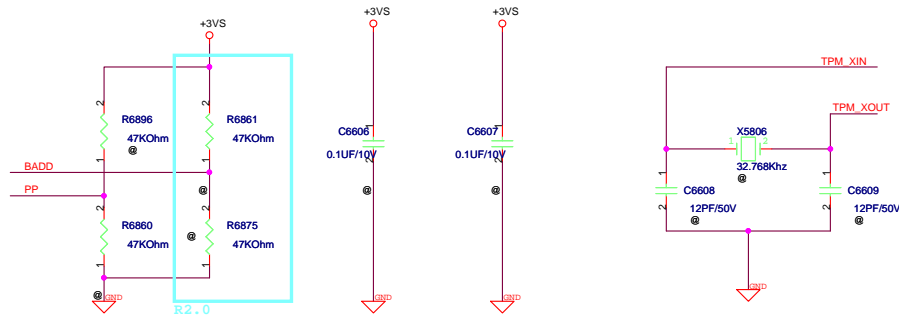
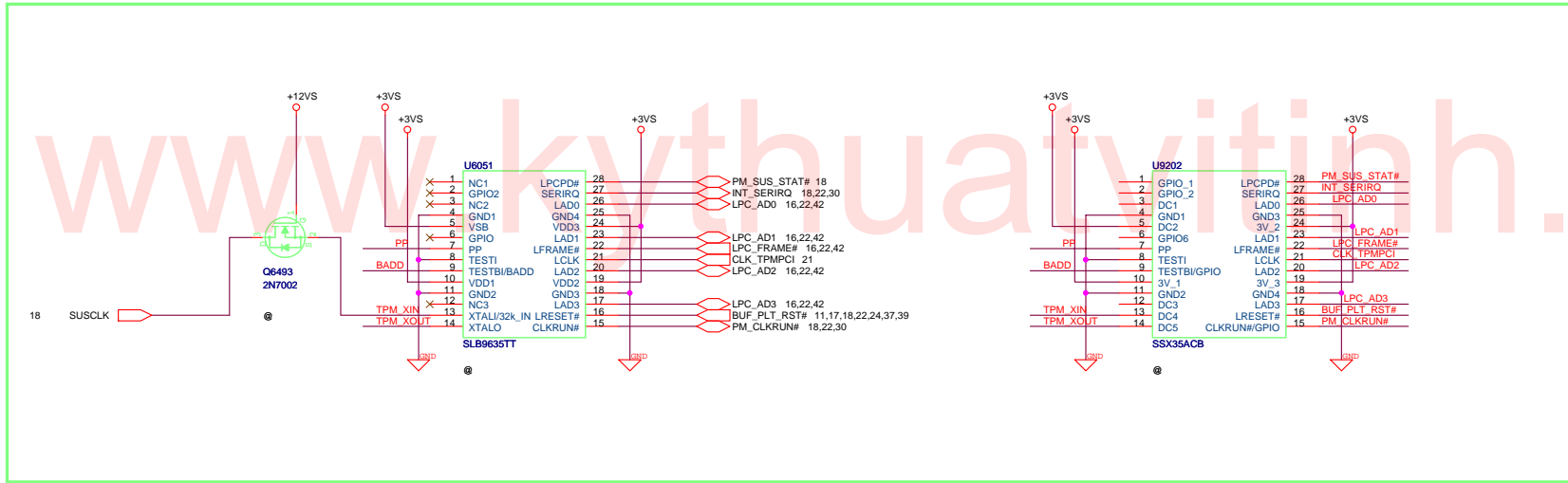


Bluetooth Module Connector



CO-LAYOUT

TESTBI/BADD PIN LPC ADDRESS SELETE High 48 h, LOW 2E h.
 TEST PIN For normal operation, connect TESTI to GND.
 PP PIN is connected to VDD, some special commands are enabled.



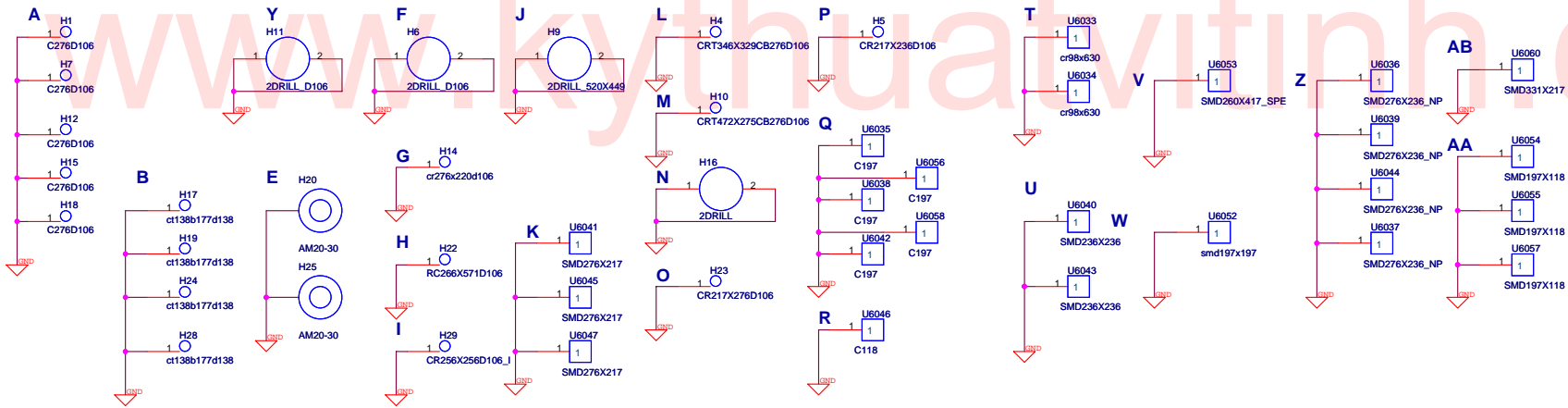
PCI Device	IDSEL#	REQ/GNT#	Interrupts
Chipset (Host to PCI)	AD30 (Internal)		
VGA	AD16		A
LAN	AD16	0	B
CARD READER	AD17	1	B
CARDBUS	AD19	1	C
1394	AD17	1	D
MINIPCI 2 (802.11)	AD17	3	D,C

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
Thermal Sensor (CPU)	1001100x (98)
Thermal Sensor (VGA)	1001101x (9A)

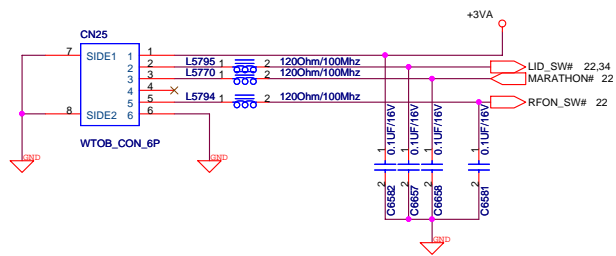
ICH8-M GPIO	W7S
GPIO 0	PM_BMBUSY#
GPIO 2	PCI_INTE#
GPIO 3	PCI_INTF#
GPIO 4	PCI_INTG#
GPIO 5	PCI_INTH#
GPIO 7	WLAN_LED_ON
GPIO 8	EXT_SMI#
GPIO 11	SMBALERT#
GPIO 12	EXT_SCI_SBY#
GPIO 15	STP_PCI#
GPIO 16	DPRSPLVR
GPIO 17	WLAN_ON#
GPIO 19	MEM_ID1
GPIO 20	BTLED_ON
GPIO 21	MEM_ID0
GPIO 22	MEMCLK_SET
GPIO 25	STP_CPU#
GPIO 27	BT_ON/OFF#
GPIO 29	USB_OC#5
GPIO 31	USB_OC#7
GPIO 32	CLKRUN#
GPIO 36	MEM_ID2
GPIO 37	PCB_ID0
GPIO 38	PCB_ID1
GPIO 39	PCB_ID2
GPIO 40	USB_OC#1
GPIO 41	USB_OC#2
GPIO 43	USB_OC#4
GPIO 49	CPUPWRGD
GPIO 50	PCI_REQ#1
GPIO 52	PCI_REQ#2
GPIO 54	PCI_REQ#3

ITE8511 GPIO	W7S
GPA0	LCD_BL_PWM
GPA1	FAN_PWN
GPA4	CHG_LED_UP#
GPA5	PWR_LED_UP#
GPA7	LCD_BACKOFF#
GPB1	CAP_LED
GPB2	TP_LED_CTRL
GPB3	SMBECO_CLK
GPB4	SMBECO_DAT
GPB5	A20GATE
GPB6	RC_IN#
GPB7	THRO_CPU
GPC1	SMBEC1_CLK
GPC2	SMBEC1_DAT
GPC4	ACIN_OC#
GPC5	MUTE_POP_GPIO#
GPC6	BAT_IN_OC#
GPDO	SLP_S3#_R
GPD1	SLP_S4#_R
GPD2	BUF_PLT_RST#
GPD3	EXT_SCI#
GPD4	RFON_SW#
GPD6	FANO_TACH
GPE2	MARATHON#
GPE4	PWR_ON#
GPE7	PM_CLKRUN#
GPF4	TPAD_CLK
GPF5	TPAD_DAT
GPG0	FA16
GPG1	FA17
GPG2	FA18
GPG3	FA19
GPG4	LID_SW#
GPG7	AC_APR_UC#
GPH0	VSUS_ON
GPH1	SUS_PWRGD
GPH2	CPU_PWRGD
GPH3	PM_PWRBTN#
GPH4	SUSC_ON
GPH5	SUSB_ON
GPH6	CPU_VRON
GPH7	PM_RSMRST#
GPIO	ICH8_PWROK
GP11	ALL_SYSTEM_PWRGD
GP13	CHG_EN#
GP14	PRECHG
GP15	EC_CLK_EN
GP16	BAT_LEARN
GPJ4	PS_CPPE#
GPJ5	PS_SHDN#
GPM0	EXT_SMI#

SCREW HOLE



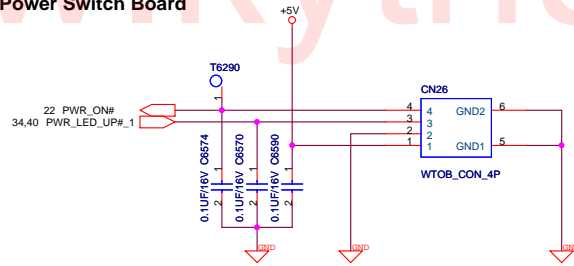
LID_SW_Board



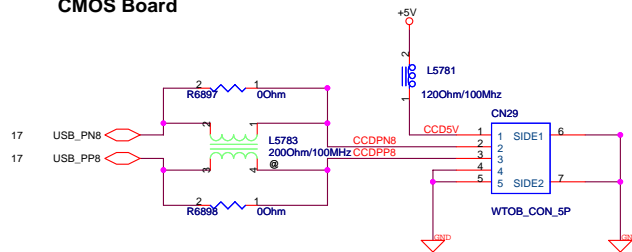
RFON_SW# (RF OFF)

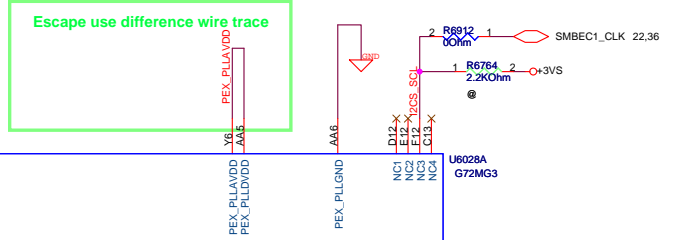
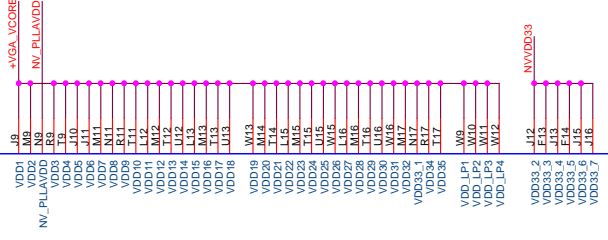
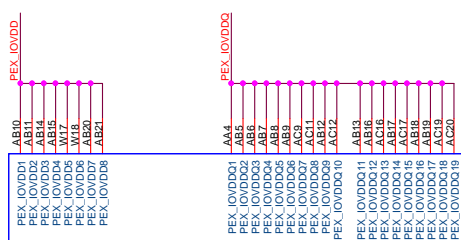
 right off ---> high
 left on ---> low

Power Switch Board

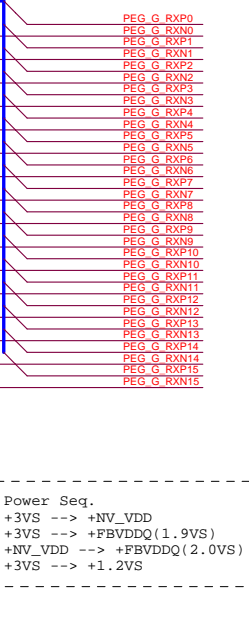
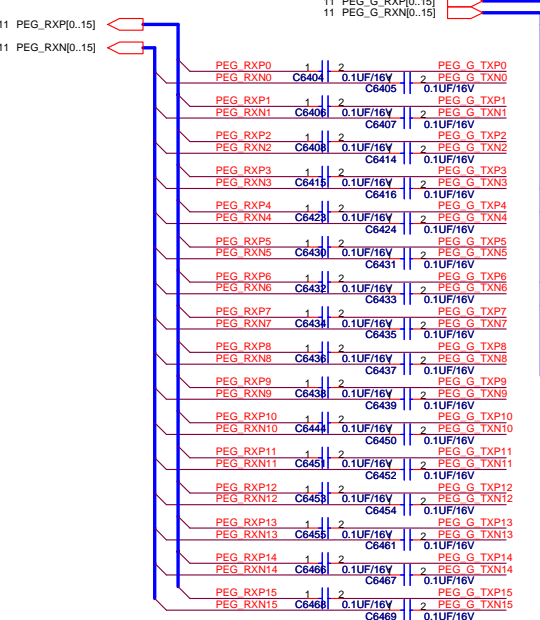
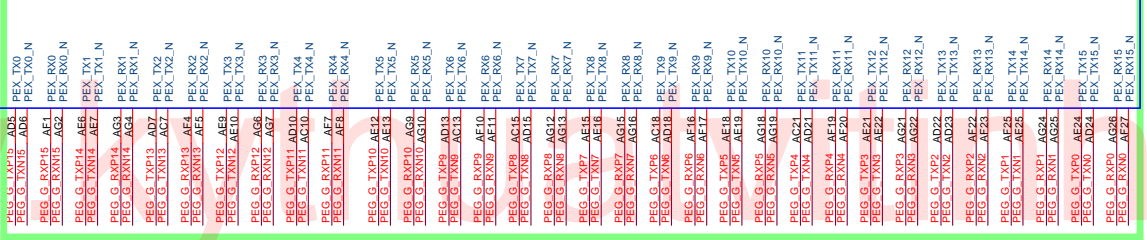


CMOS Board

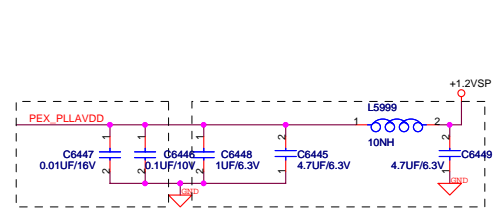
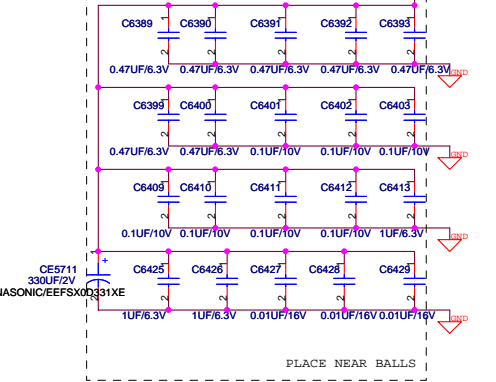
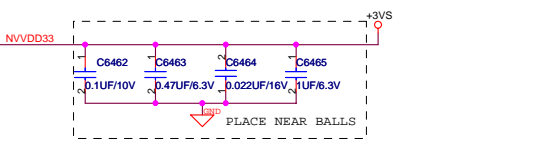
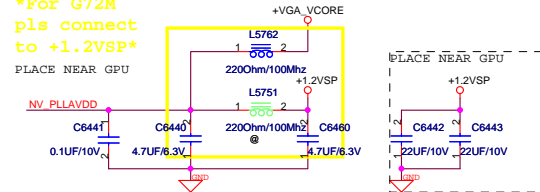
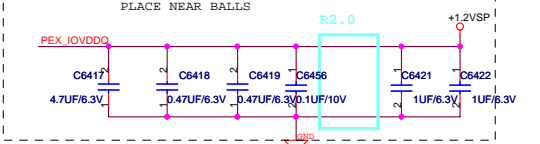
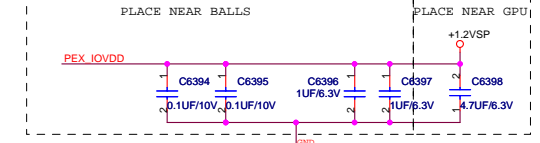




PCIE LAN REVERSE



Power Seq.
 +3VS --> +NV_VDD
 +3VS --> +FBVDDQ(1.9VS)
 +NV_VDD --> +FBVDDQ(2.0VS)
 +3VS --> +1.2VS

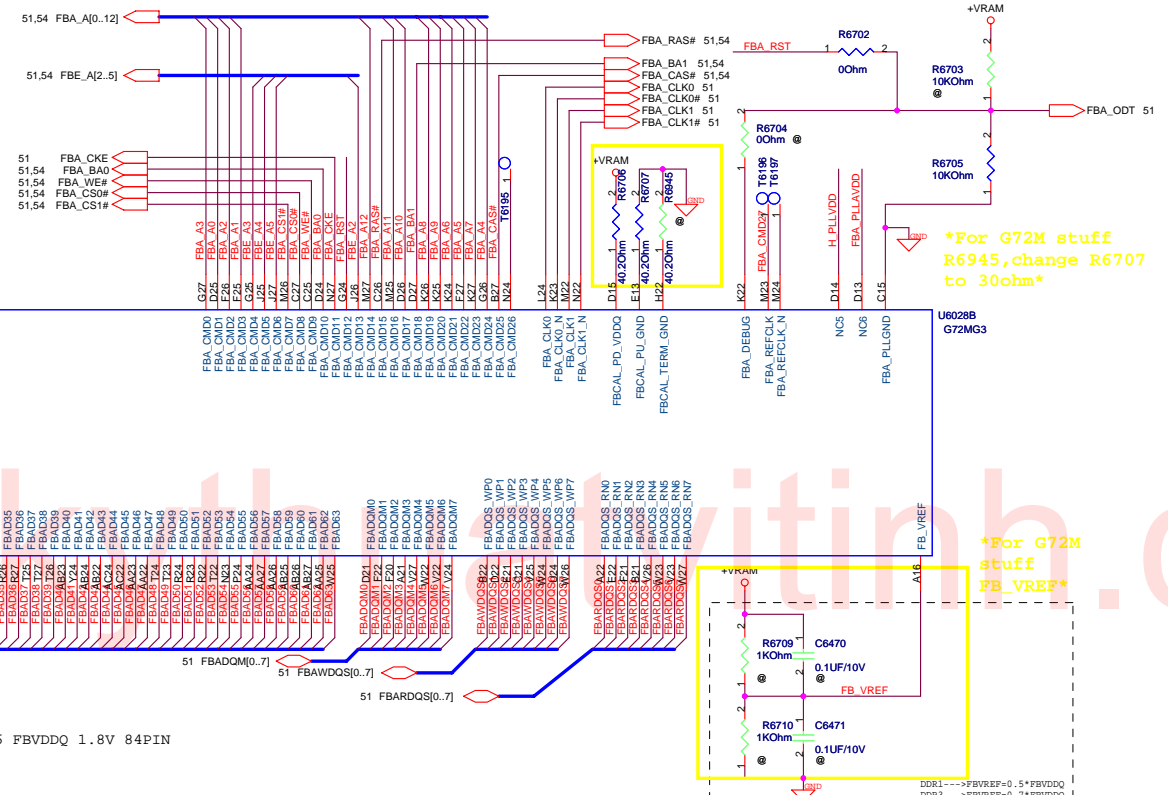


<Variant Name>

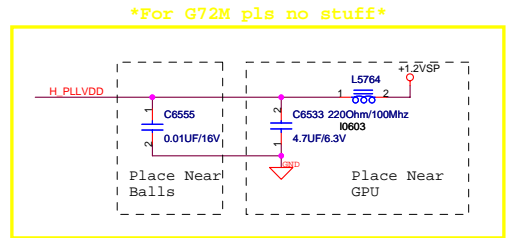
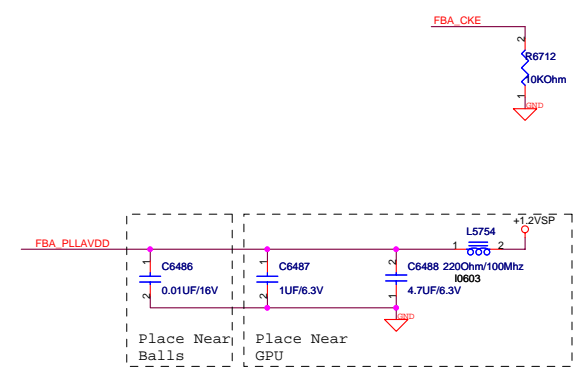
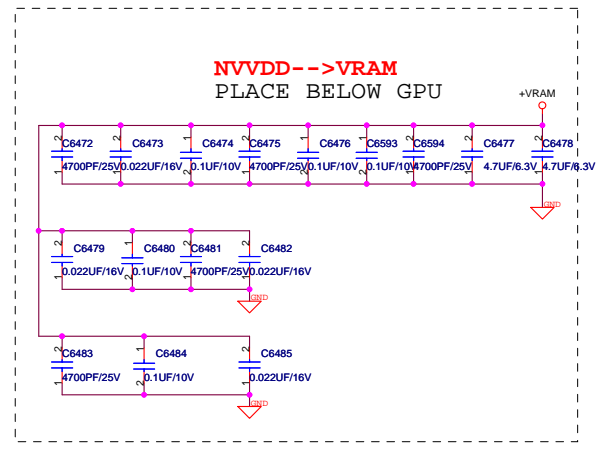


REVISION	DATE: Tuesday, August 21, 2007	DESCRIPTION:
2.0	SHEET 49 OF 70	T76S

SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
RELEASE DATE :		



GDDR2 16x16 FBVDDQ 1.8V 84PIN



<Variant Name>



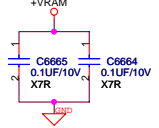
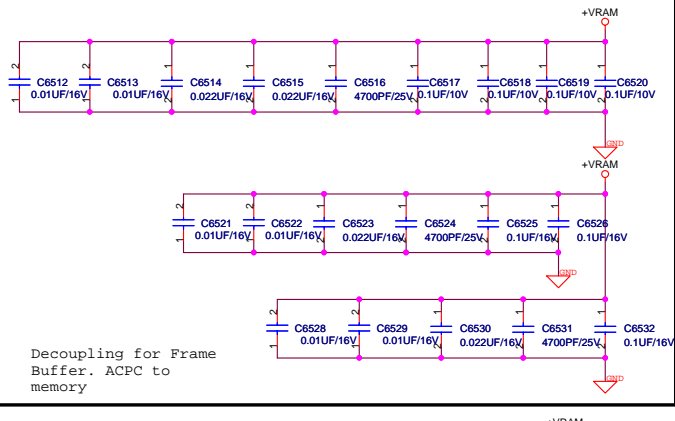
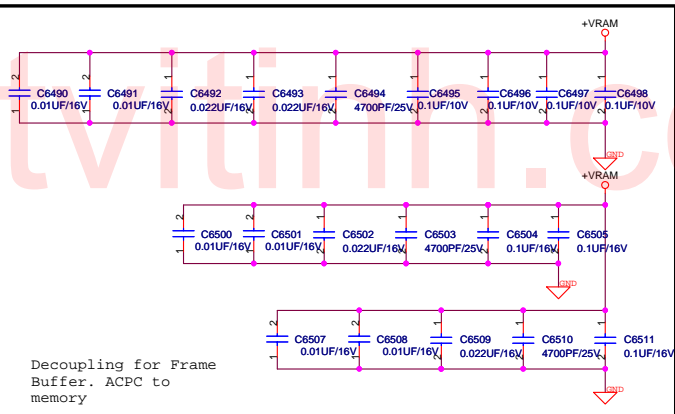
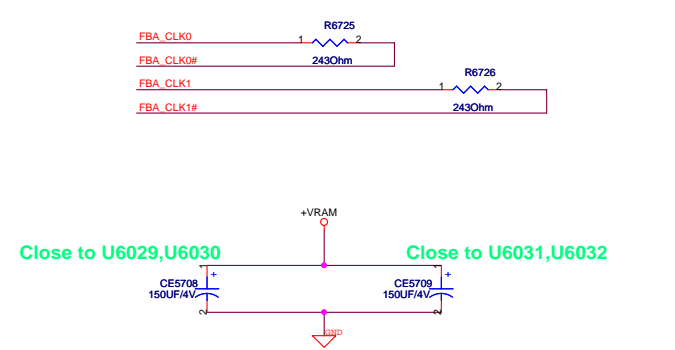
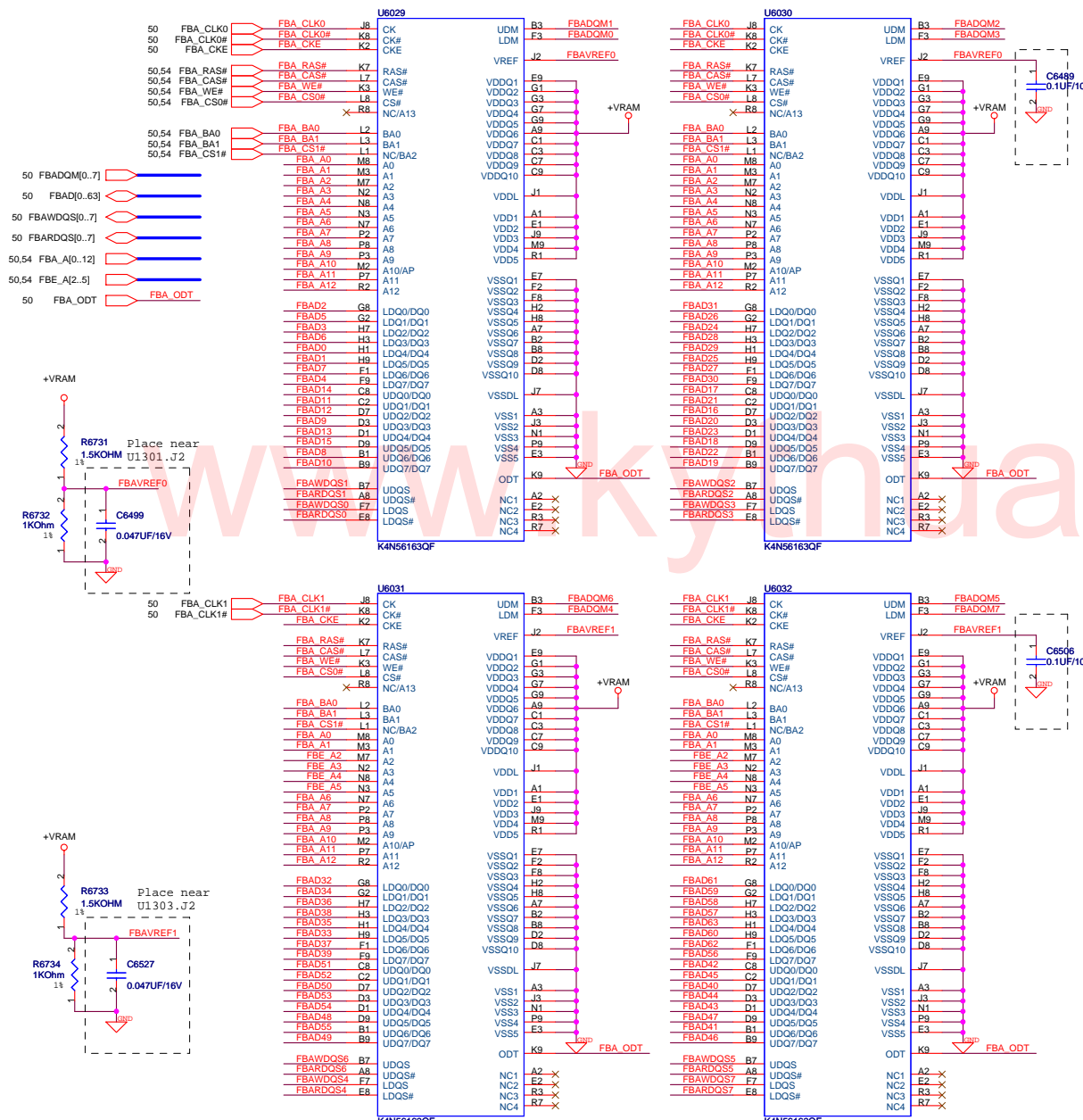
PROJECT: W7S

REVISION: 2.0
 DATE: Tuesday, August 21, 2007
 SHEET: 50 OF 70

DESCRIPTION: T76S

SCHEMATIC FILE NAME: <OrgName>
 RELEASE DATE:

DESIGN ENGINEER:



<Variant Name>



PROJECT: W7S

REVISION
2.0

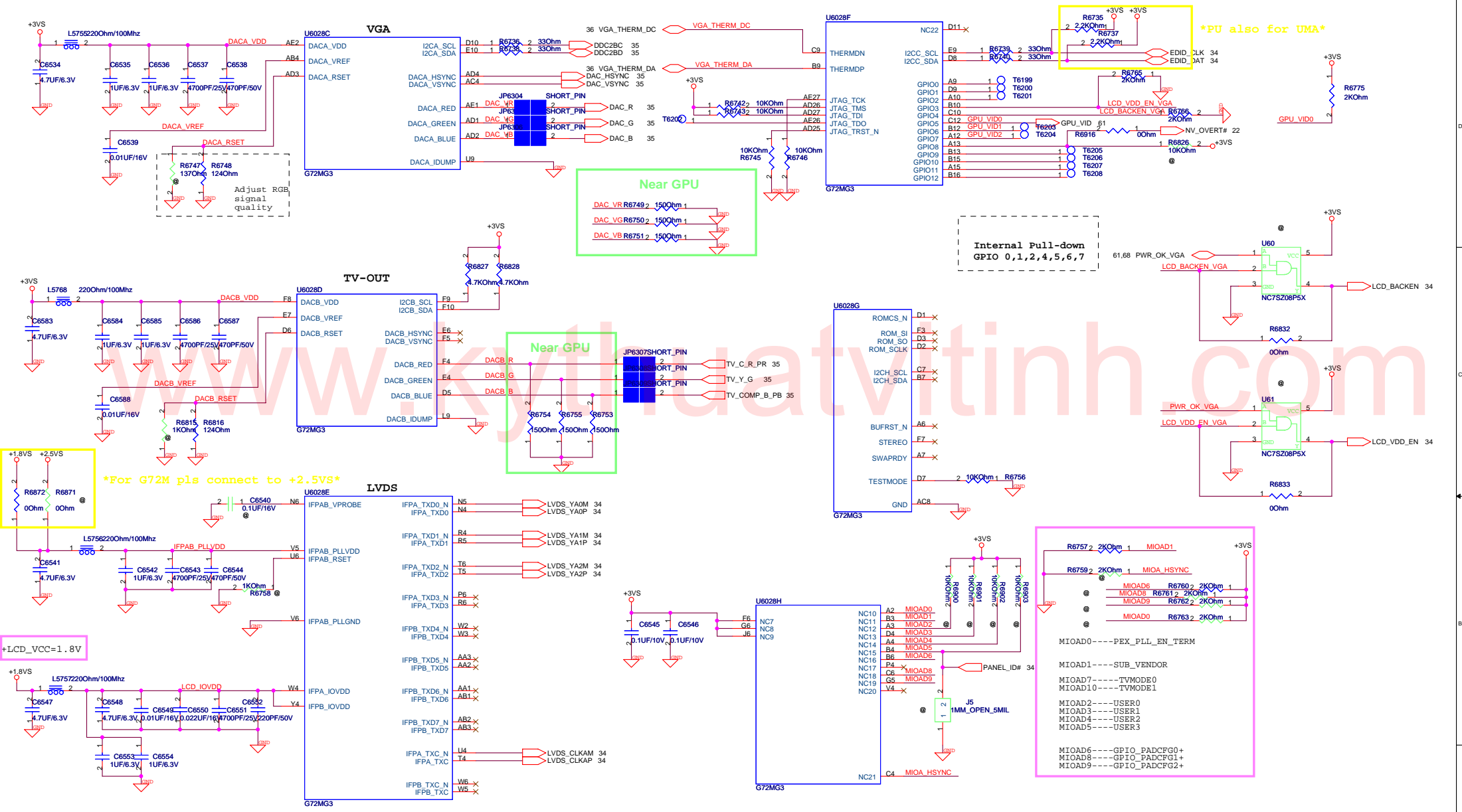
DATE: Tuesday, August 21, 2007
SHEET 51 OF 70

DESCRIPTION:
T76S

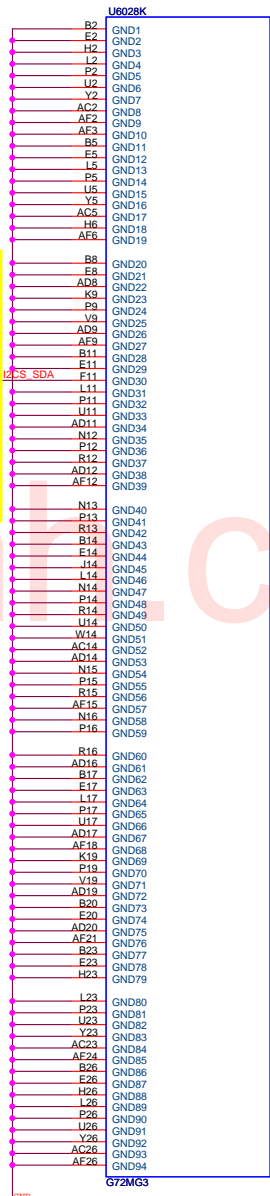
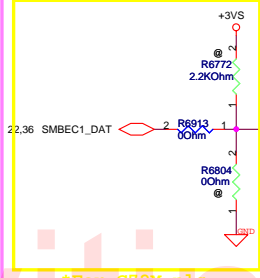
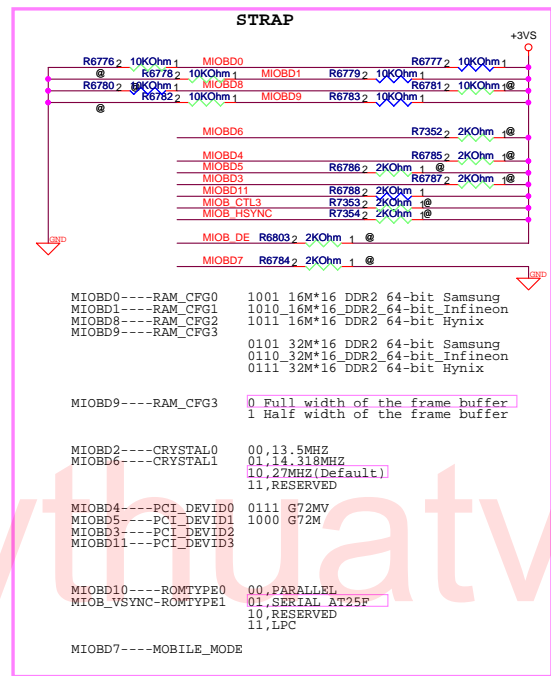
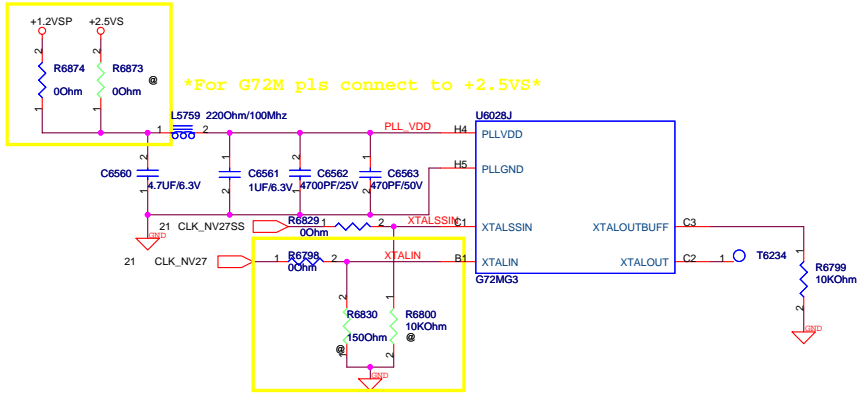
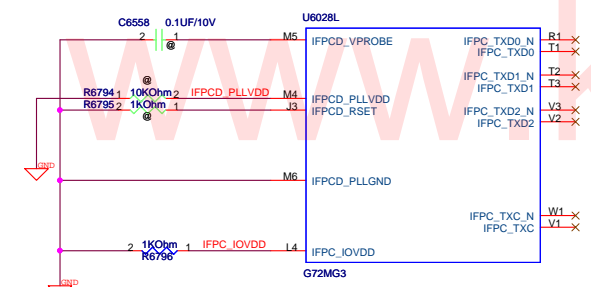
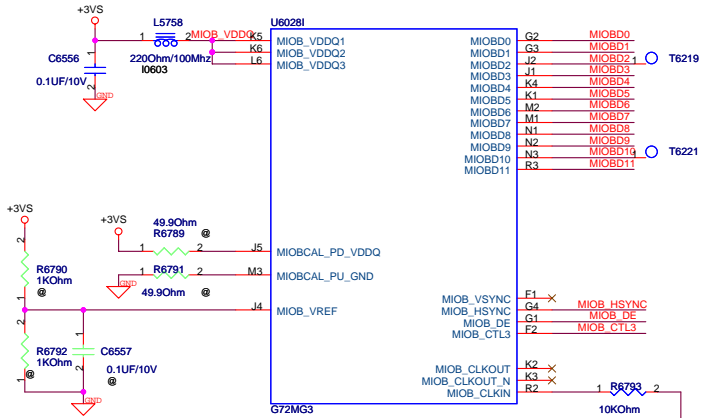
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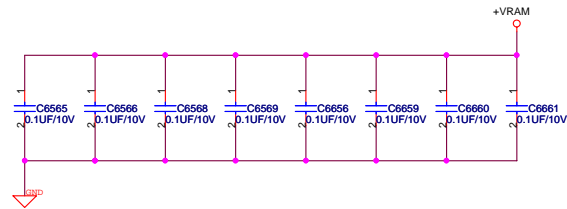
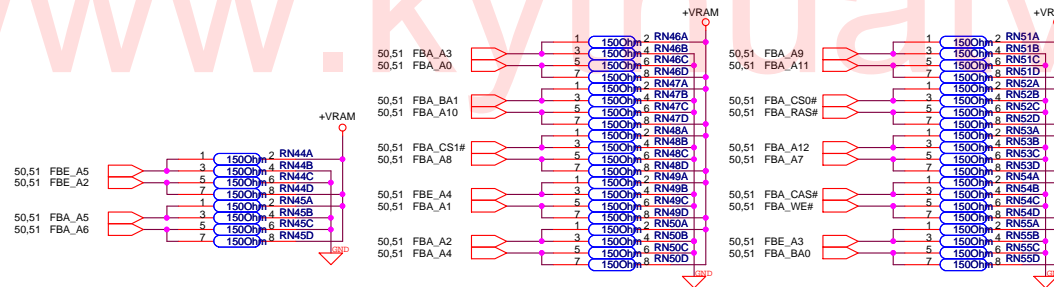
DESIGN ENGINEER :



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FBA CMD/ADDR Termination

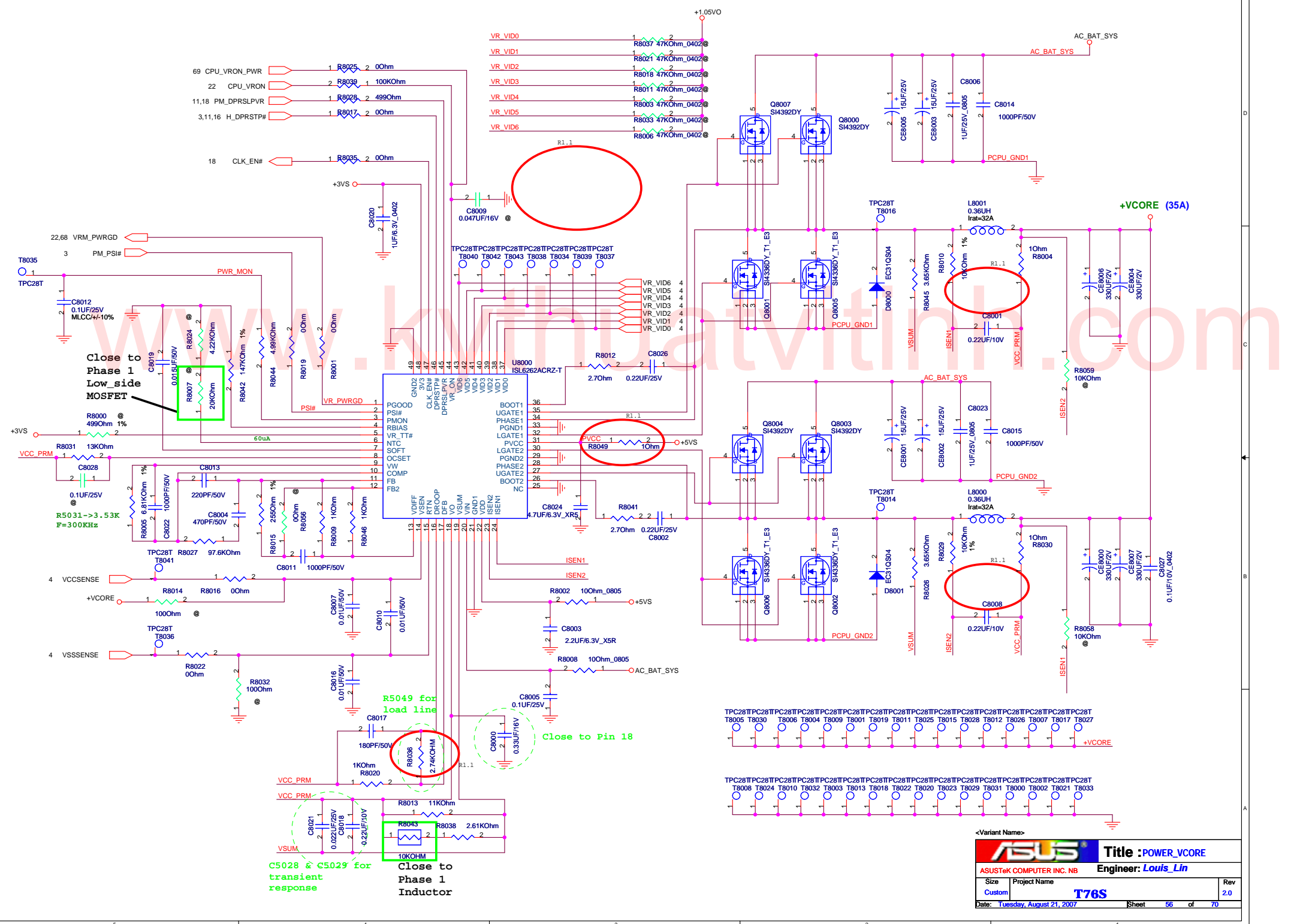


<Variant Name>

		Title VGA-Terminator
ASUSTeK COMPUTER INC		Engineer:
Size	Project Name	Rev
Custom	T76S	2.0
Date: Tuesday, August 21, 2007	Sheet	54 of 70

Rev	Date	Description
R1.0	2006/10/25	1. Initial release.
R1.1	2007/01/12	1. Change R6316 to 390 ohm page.21 2. Add R6662 and NET_NV_OVERT# page.22 3. Del R6026 Add D6044,D6045,R6988 and R6990 page.28 4. Add R6989 page.29 5. Add R691 page.30 6. Add R6415 page.39 7. Add R6471 and Q6475 page.41 8. Add R6912 page.49 9. Change R6731,R6733 to 1.5Kohm and R6725, R6726 to 243ohm page.51 10. Add R6916 page.52 11. Add R6913 page.53
R2.0	2007/03/14	1. Add R6805 page.18 2. Change R6316 to 270 ohm page.21 3. Add R6628 page.28 4. Add R7381,Q6487 page.32 5. Change Q6483,Q6484,Q6485 to ESD protect device page.32 6. Change R6987 to 0 ohm page.35 7. Change R6859 pull high to +3VA page.36 8. Del C6595 page.49

Rev	Date	Description



Close to Phase 1 Low_side MOSFET

R5049 for load line

Close to Pin 18

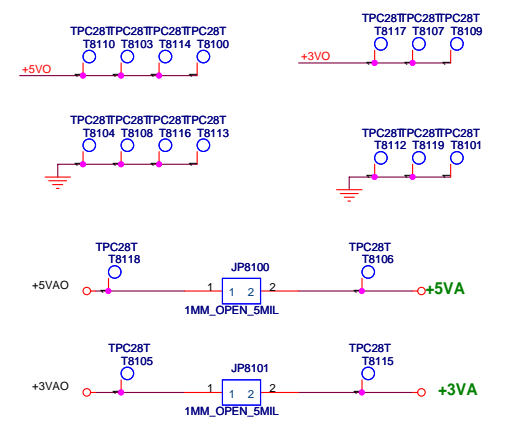
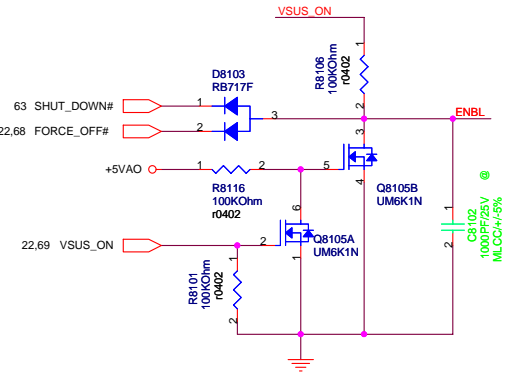
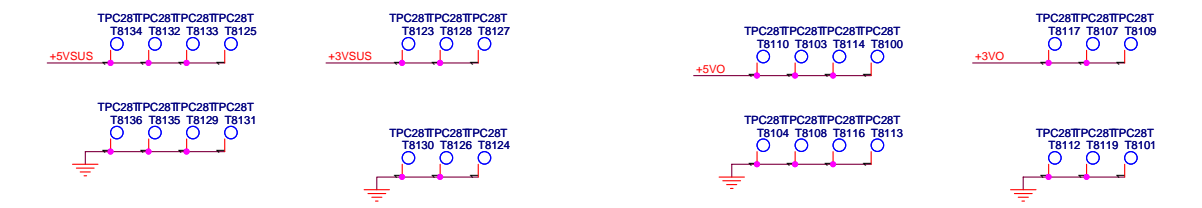
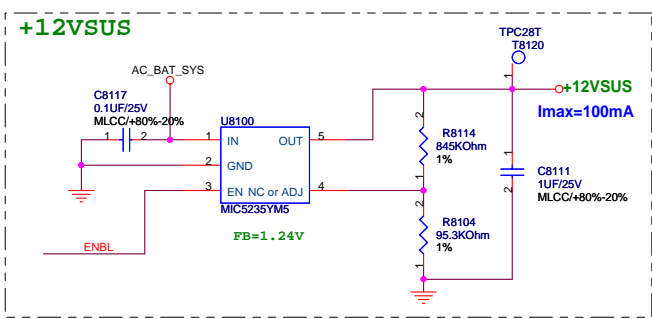
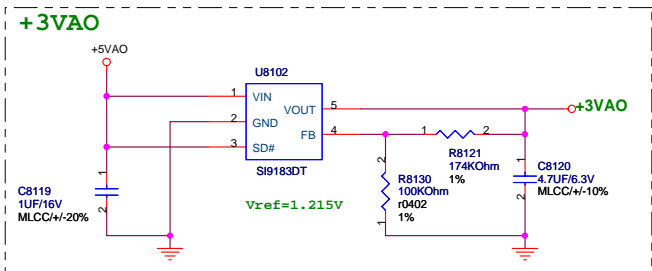
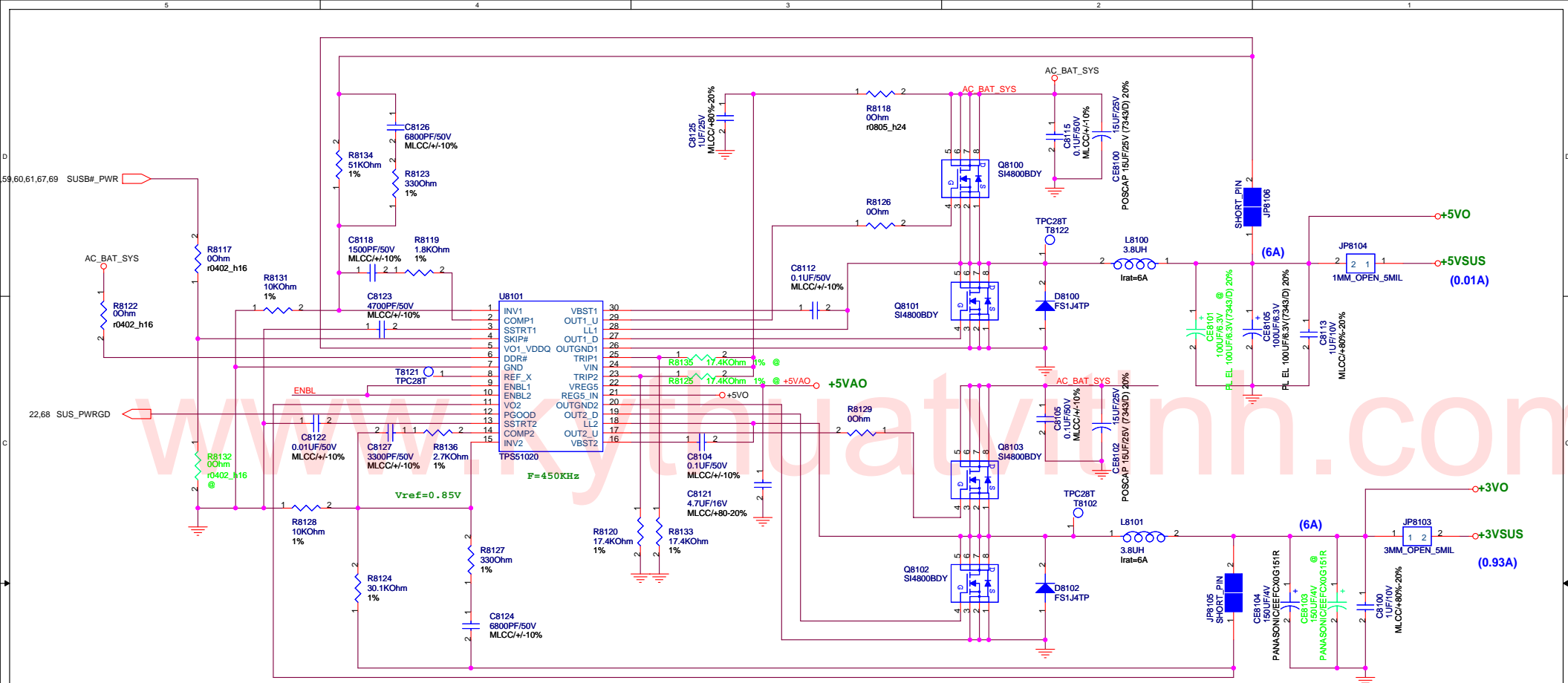
C5028 & C5029 for transient response

Close to Phase Inductor

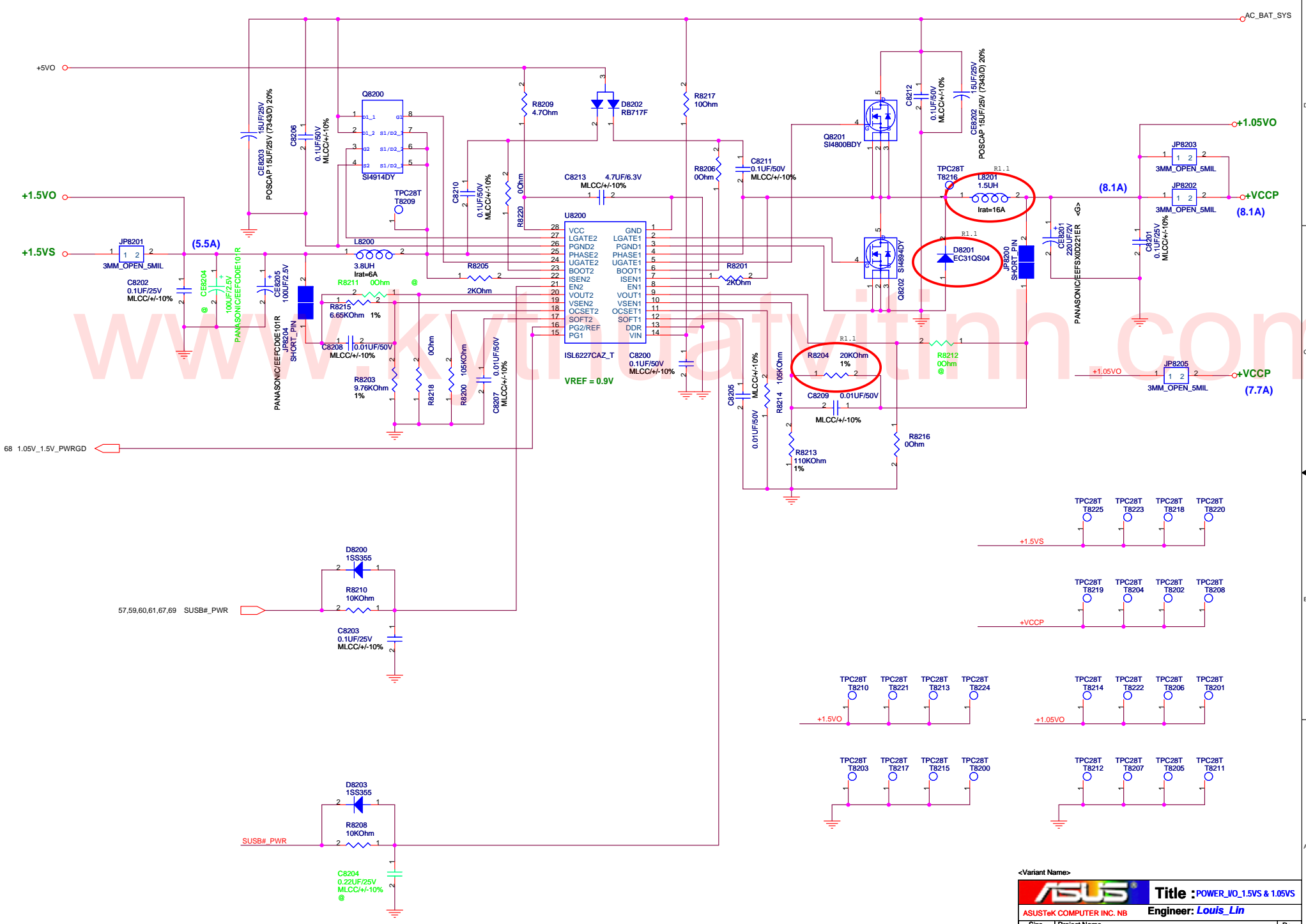
<Variant Name>

ASUS Title : POWER_VCORE
 ASUSTeK COMPUTER INC. NB Engineer: Louis_Lin

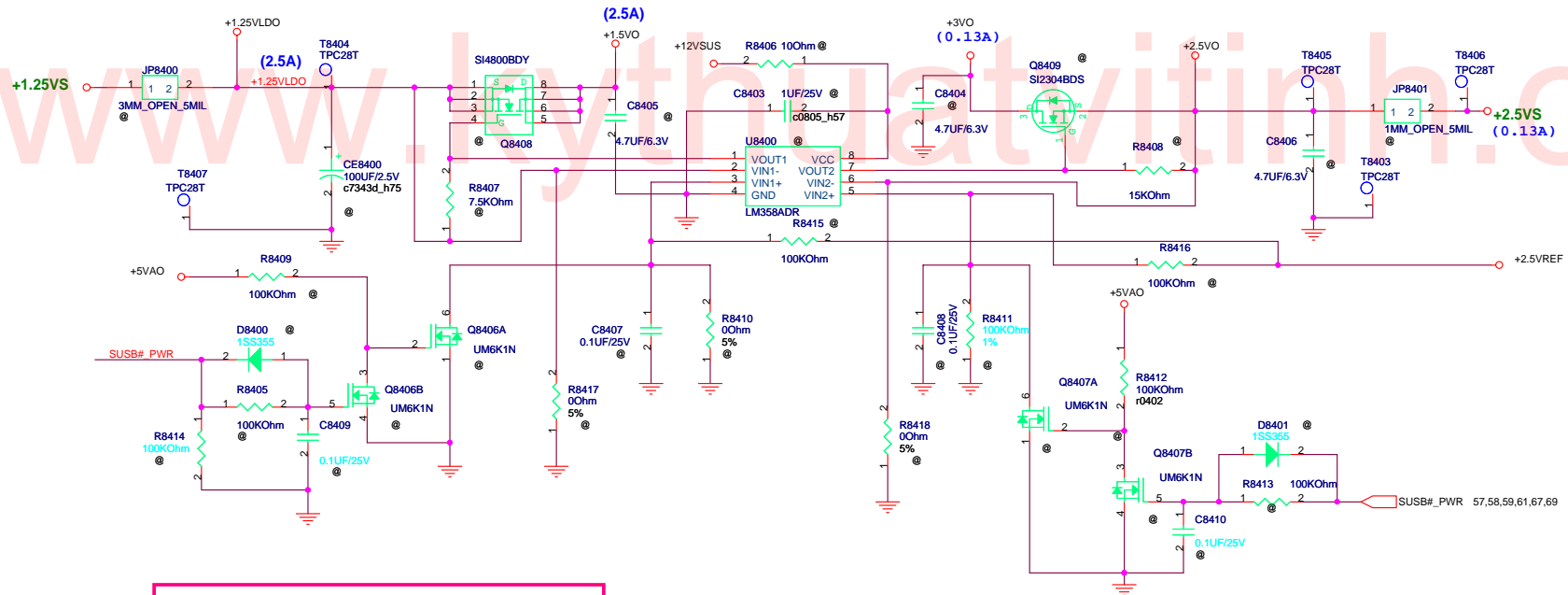
Size	Project Name	Rev
Custom	T76S	2.0
Date: Tuesday, August 21, 2007	Sheet	56 of 70



Title : POWER_SYSTEM	
ASUSTeK COMPUTER INC. NB Engineer: Louis_Lin	
Size	Project Name
Custom	T76S
Date: Tuesday, August 21, 2007	Sheet 57 of 70
Rev	2.0



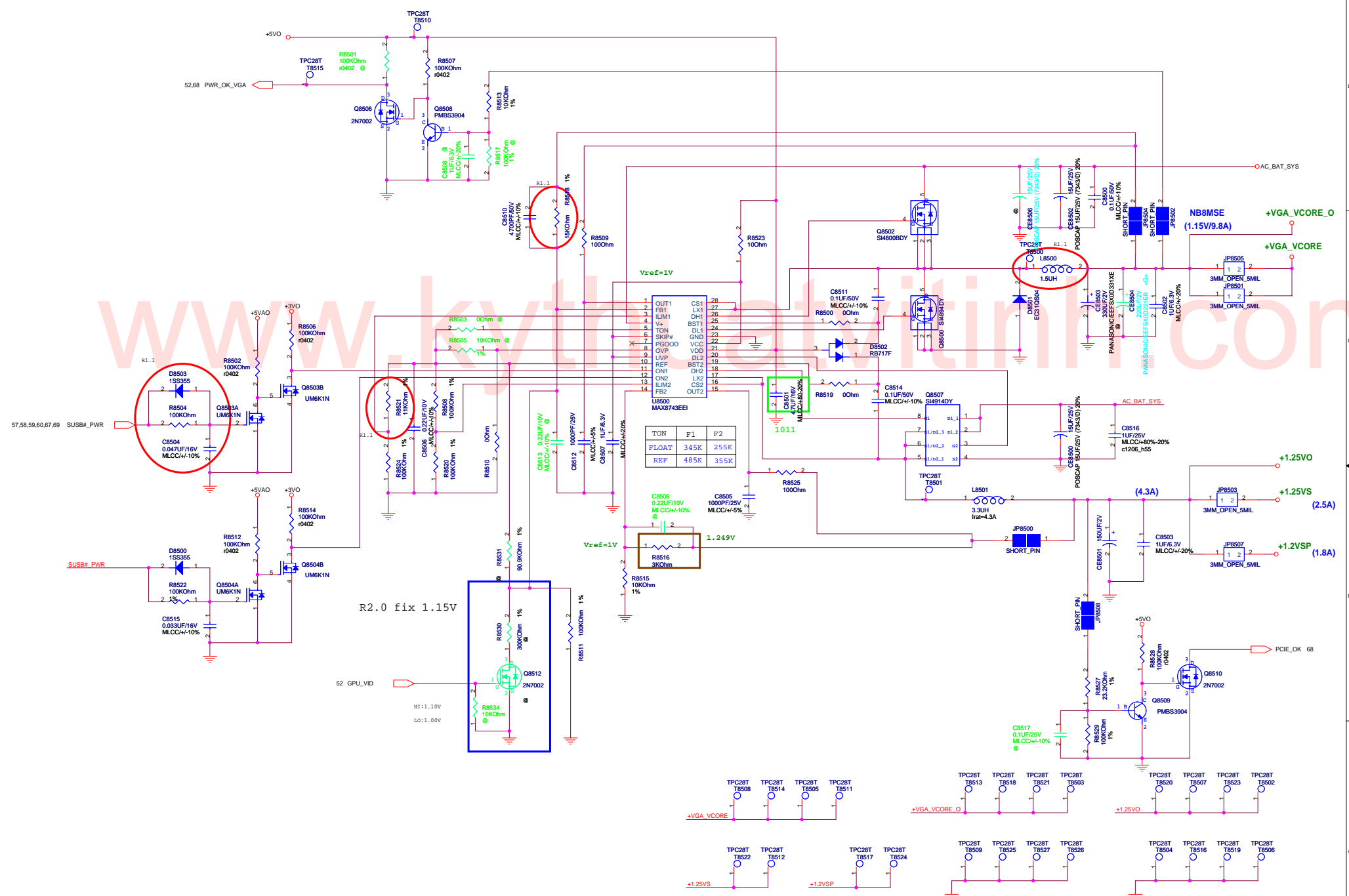
+1.25VS & +2.5VS



UMA Enable +1.25VS
R8417 UNMOUNT, R8410 100K 10G212100314010


Discrete VGA Disable +1.25VS
R8417 MOUNT, R8410 0 ohm 10G212000004030
And other UNMOUNT.

R8414,D8400,C8409 Always Keep UNMOUNT

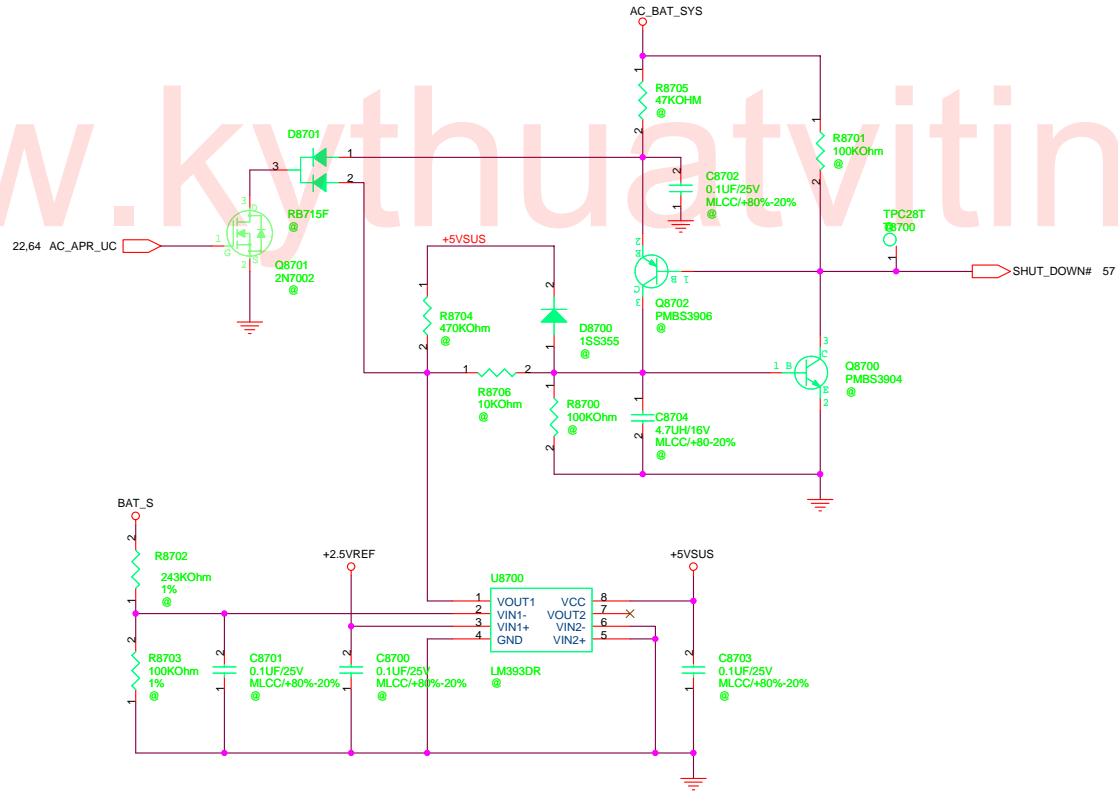


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<Variant Name>

		Title : N/A
ASUSTeK COMPUTER INC. NB		Engineer: Louis_Lin
Size B	Project Name T76S	Rev 2.0
Date: Tuesday, August 21, 2007		Sheet 62 of 70

PIC only



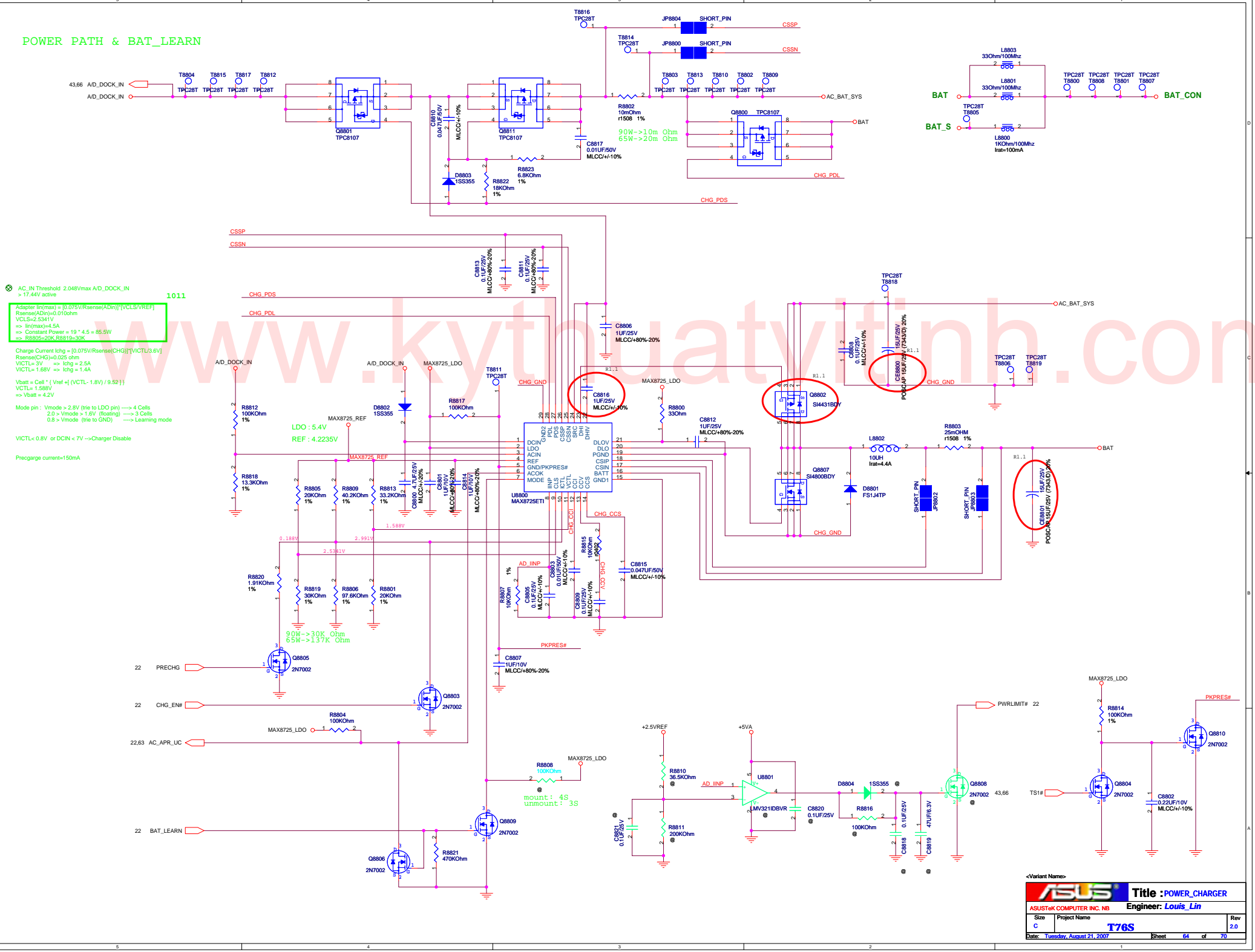
<Variant Name>

		Title :POWER_SHUTDOWN#	
ASUS TeK COMPUTER INC. NB		Engineer: Louis_Lin	
Size	Project Name	Rev	
Custom	T76S	2.0	
Date: Tuesday, August 21, 2007	Sheet	63	of 70

POWER PATH & BAT_LEARN

AC_IN_Threshold 2.048Vmax A/D_DOCK_IN > 17.44V active
 Adapter In(max) = [0.075V/Rsense(Adm)]/[VCLS/VREF]
 Rsense(Adm)=0.010ohm
 VCLS=2.5341V
 => In(max)=4.5A
 => Constant Power = 19 * 4.5 = 85.5W
 => R8805=20K, R8819=30K


Charge Current Ichg = [0.075V/Rsense(CHG)]/[VICTL/3.6V]
 Rsense(CHG)=0.025 ohm
 VICTL= 3V => Ichg = 2.5A
 VICTL= 1.58V => Ichg = 1.4A
 Vbatt = Cell * Vref + (VCTL - 1.8V) / 9.52
 VCTL= 1.58V
 => Vbatt = 4.2V
 Mode pin : Vmode > 2.8V (tie to LDO pin) -> 4 Cells
 2.0 > Vmode > 1.6V (floating) -> 3 Cells
 0.8 > Vmode (tie to GND) -> Learning mode
 VICTL < 0.8V or DCIN < 7V -> Charger Disable
 Precharge current=150mA



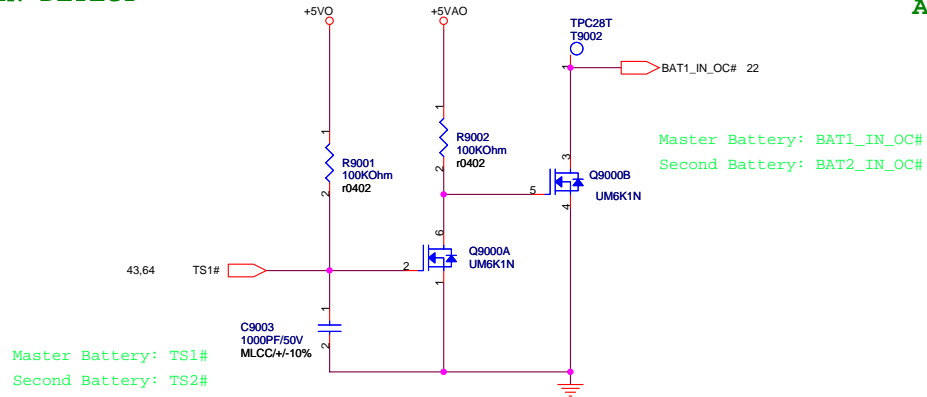
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ASUS Title : POWER_CHARGER
 ASUSTeK COMPUTER INC. NB Engineer: Louis Lin
 Size | Project Name
 C | T76S
 Date: Tuesday, August 21, 2007 Sheet 64 of 70

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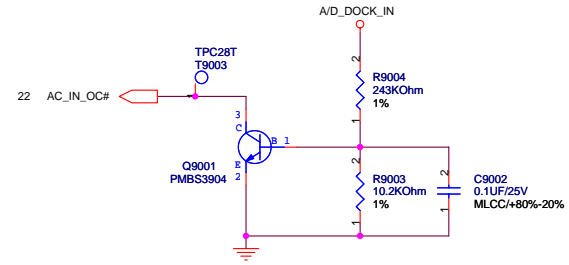
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ASUSTeK COMPUTER INC. NB		Engineer: <i>Louis_Lin</i>	
Size	Project Name	Rev	
Custom	T76S	2.0	
Date: <i>Tuesday, August 21, 2007</i>		Sheet	65 of 70

BATTERY IN DETECT

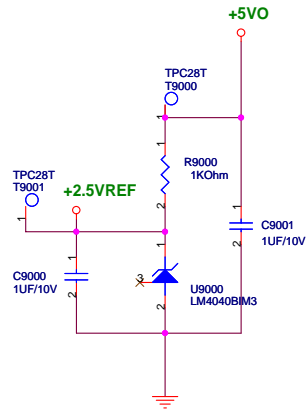


ADAPTER IN DETECT

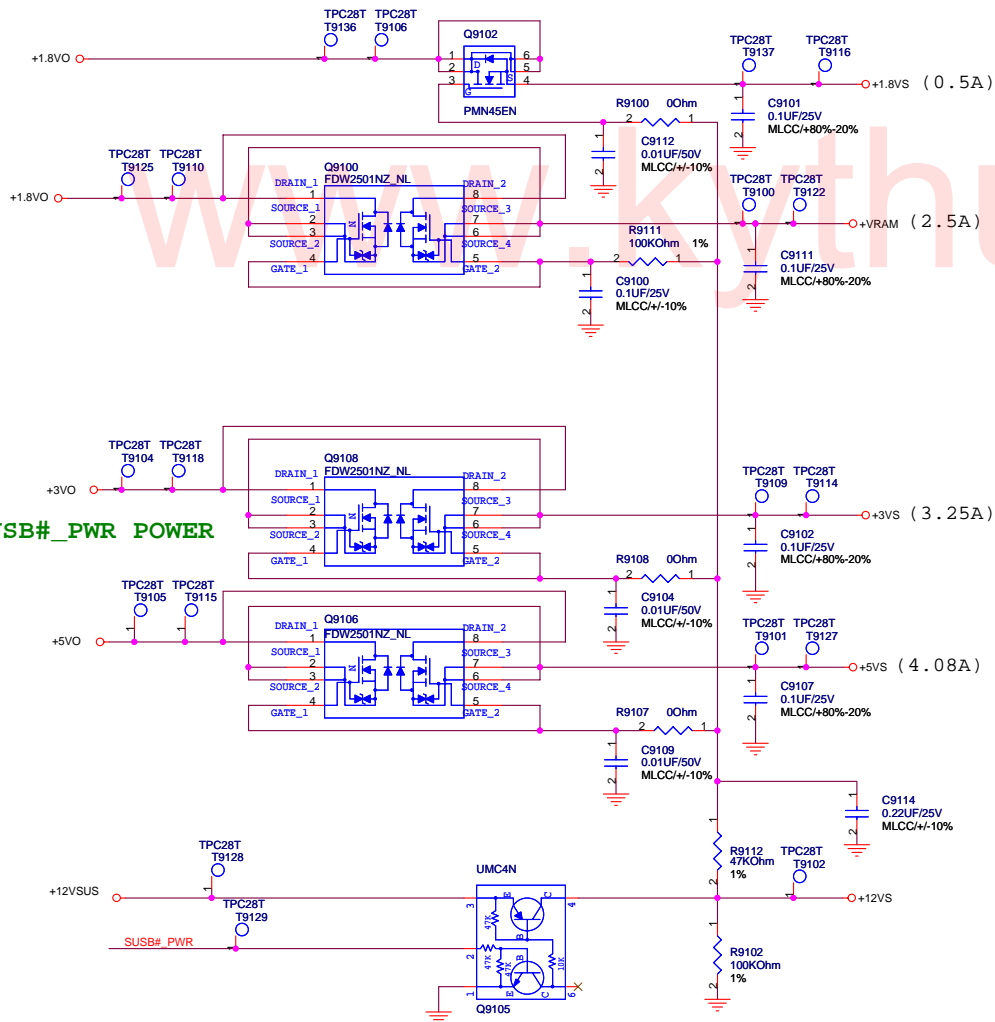


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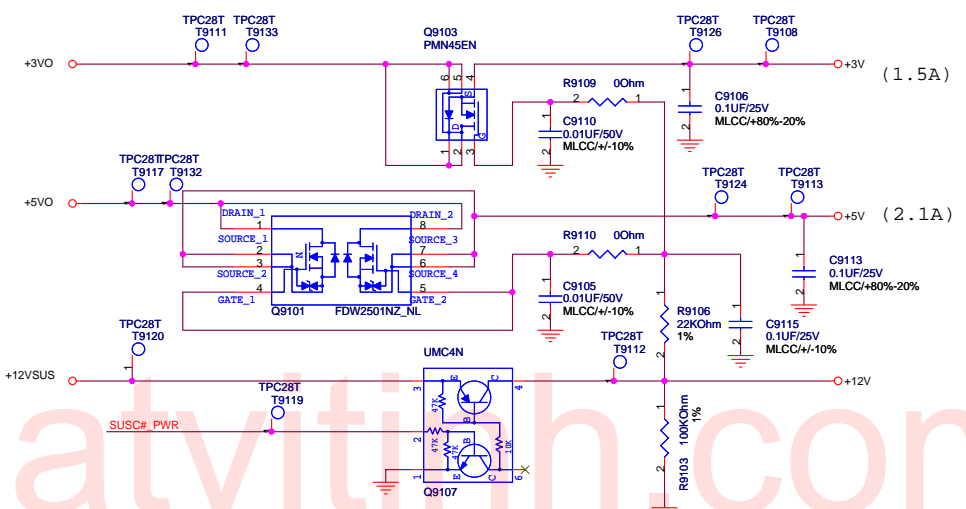
+2.5VREF



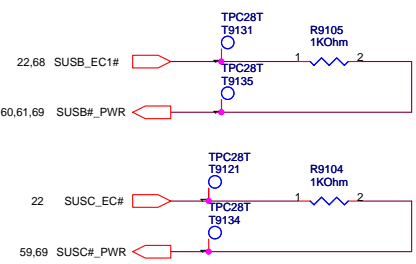
SUSC#_PWR POWER



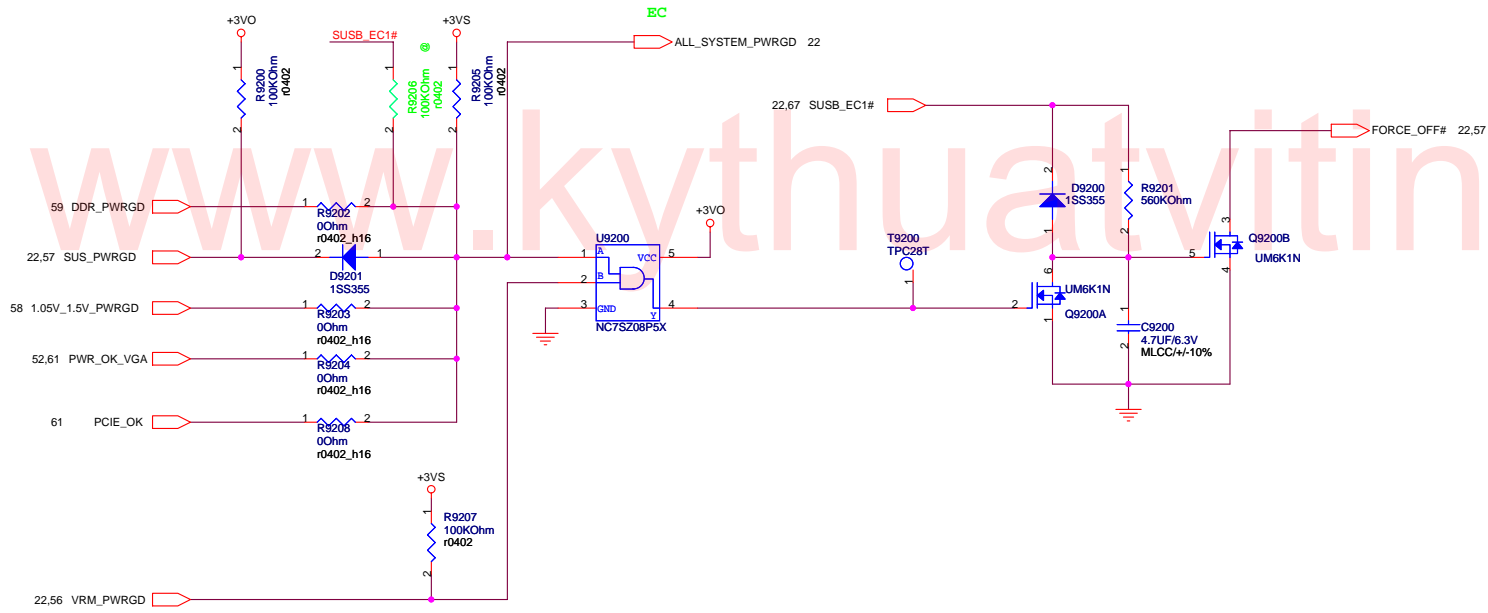
SUSB#_PWR POWER



SUSC#_PWR

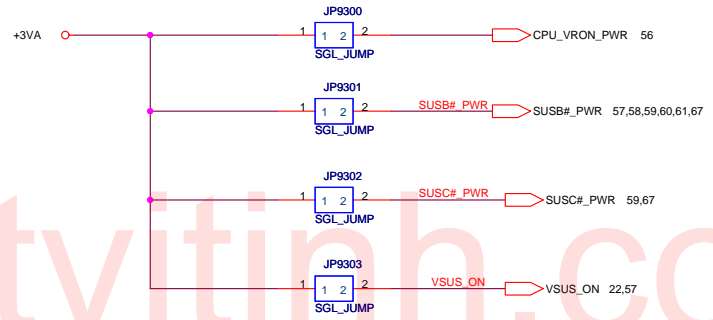


POWER GOOD DETECTOR

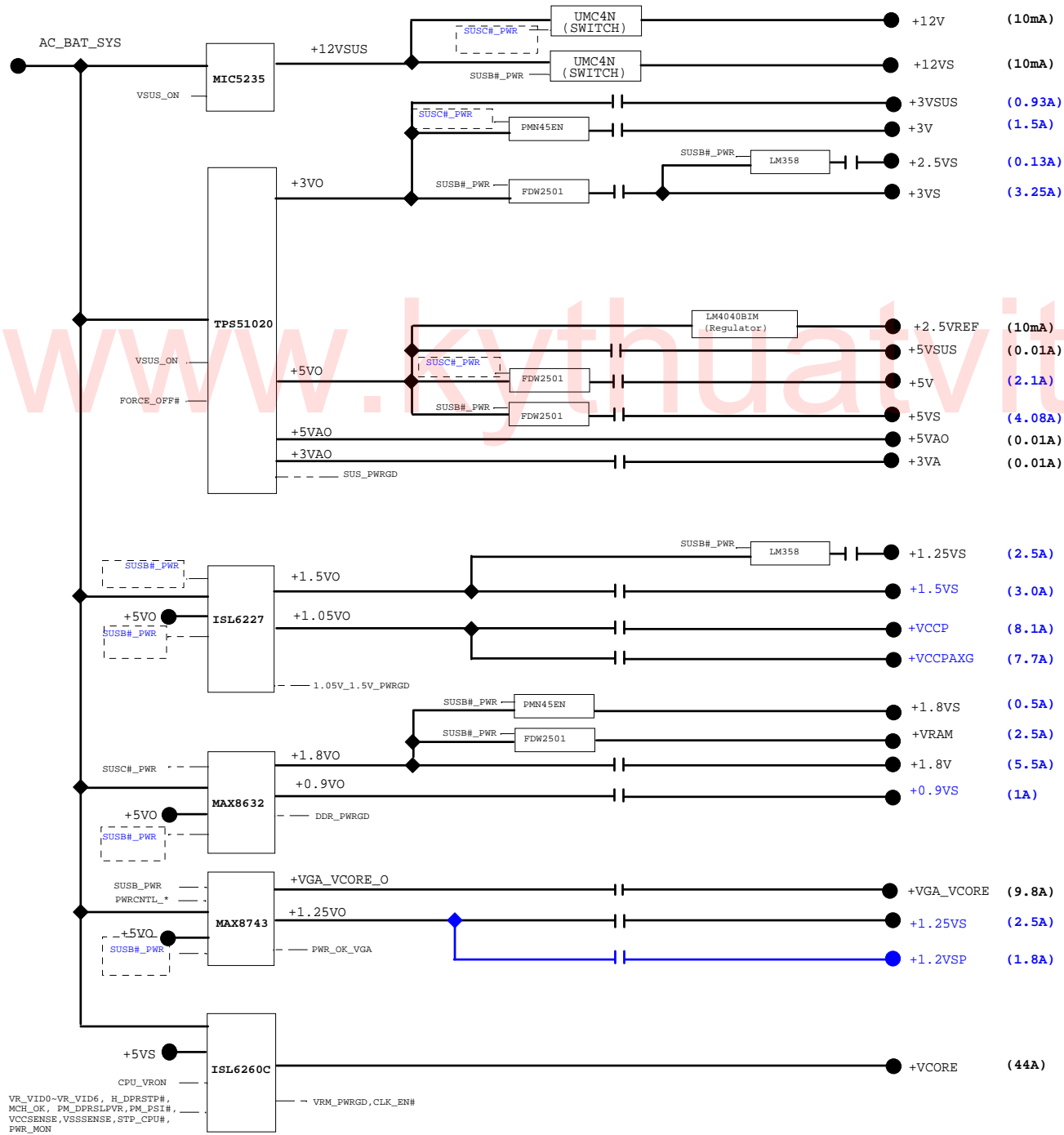


AC_BAT_SYS	AC_BAT_SYS	34,56,57,58,59,61,63,64
BAT	BAT	64
BAT_CON	BAT_CON	43,64
+2.5VREF	+2.5VREF	60,63,64,66
+3VA	+3VA	16,22,43,48,57
+5VAO	+5VAO	57,60,61,66
+5VO	+5VO	57,58,59,61,66,67
+5VSUS	+5VSUS	19,57,63
+5V	+5V	9,26,28,38,40,41,48,67
+5VS	+5VS	19,20,23,26,28,29,35,36,37,40,41,56,67
+3VO	+3VO	57,60,61,67,68
+3VSUS	+3VSUS	17,18,19,22,24,28,57
+3V	+3V	17,25,33,37,39,41,44,67
+3VS	+3VS	3,8,11,14,15,16,18,19,20,21,22,24,26,28,30,31,32,33,34,35,36,37,39,41,42,45,49,52,53,56,67,68
+12VSUS	+12VSUS	57,60,67
+12V	+12V	18,28,32,67
+12VS	+12VS	45,67
+1.8VO	+1.8VO	59,67
+1.8V	+1.8V	6,7,8,9,11,13,14,41,59
+1.8VS	+1.8VS	52,67
+0.9VS	+0.9VS	9,59
+0.9VO	+0.9VO	59
+1.05VO	+1.05VO	56,58
+VCCP	+VCCP	3,4,5,10,11,13,14,16,19,21,41,58
+1.5VO	+1.5VO	58,60
+1.5VS	+1.5VS	4,14,16,17,19,33,39,41,58
+2.5VO	+2.5VO	60
+2.5VS	+2.5VS	41,52,53,60
+VCORE	+VCORE	4,5,56
+VGA_VCORE	+VGA_VCORE	49,61
+VRAM	+VRAM	50,51,54,67
+1.2VSP0	+1.2VSP	41,49,50,53,61
+1.25VS	+1.25VS	11,14,19,60,61

FOR POWER TEST



Non-IAMT



VR_VID0~VR_VID6, H_DPRSTP#,
 MCH_OK, PM_DPRS1PWR, PM_PSI#,
 VCCSENSE, VSSSENSE, STP_CPU#,
 PWR_MON