

Alba Discrete ATI M92-LP gDDR2 Schematics

uFCPGA Mobile Penryn

Intel Cantiga-PM + ICH9M

2009-03-23

REV : SA

DY : Nopop Component

GM : Pop when Cantiga is GM

PM : Pop when Cantiga is PM

G/P : BOM control if Cantiga is PM

<Core Design>



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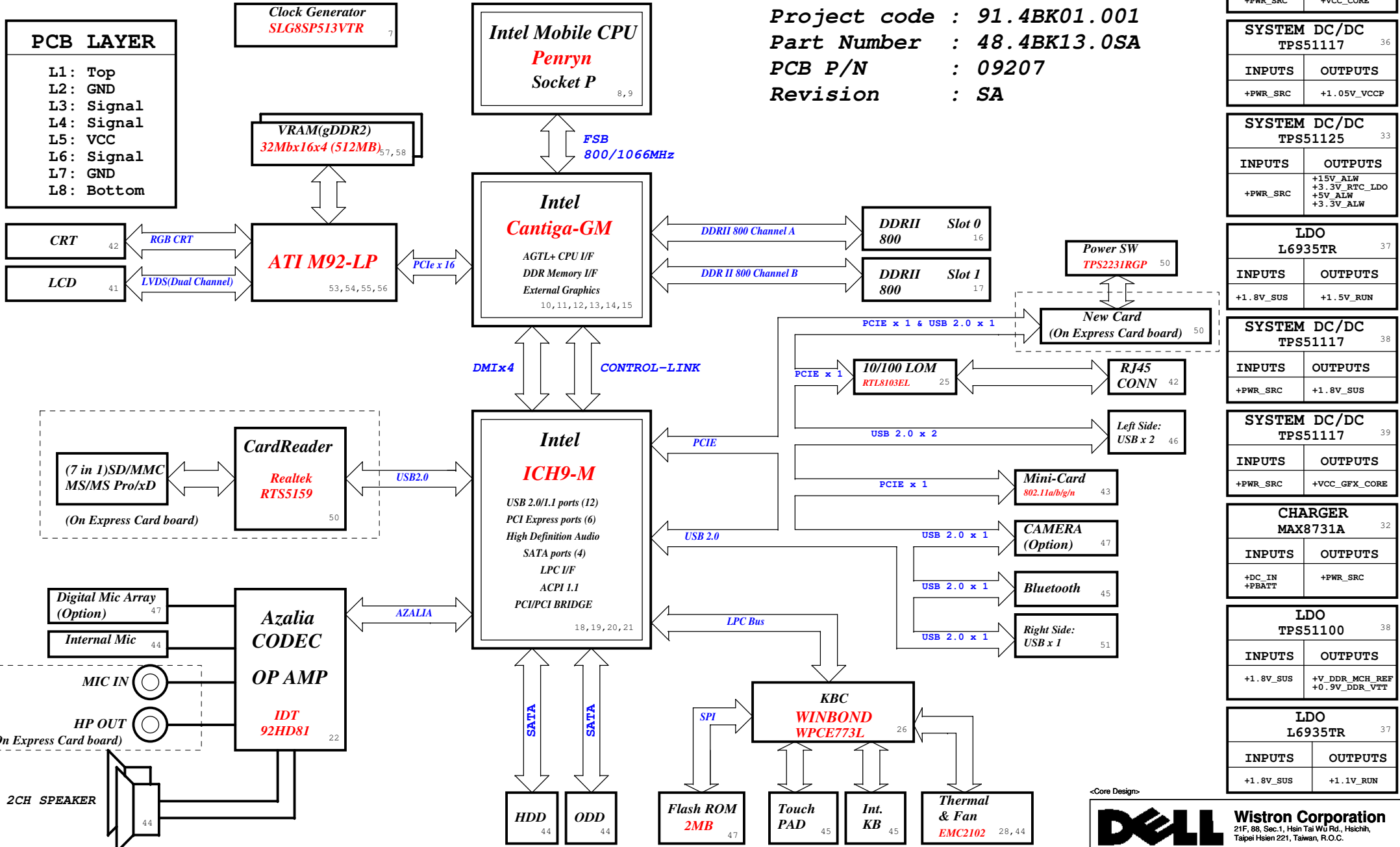
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| Title | | | |
| Cover Page | | | |
| Size Custom | Document Number | Rev | SB |
| Date: Monday, March 23, 2009 | | Sheet 1 | of 60 |

ALBA Discrete Block Diagram

Project code : 91.4BK01.001
 Part Number : 48.4BK13.0SA
 PCB P/N : 09207
 Revision : SA

PCB LAYER

- L1: Top
- L2: GND
- L3: Signal
- L4: Signal
- L5: VCC
- L6: Signal
- L7: GND
- L8: Bottom



CPU DC/DC ISL6266A 34,35

| INPUTS | OUTPUTS |
|----------|-----------|
| +PWR_SRC | +VCC_CORE |

SYSTEM DC/DC TPS51117 36

| INPUTS | OUTPUTS |
|----------|-------------|
| +PWR_SRC | +1.05V_VCCP |

SYSTEM DC/DC TPS51125 33

| INPUTS | OUTPUTS |
|----------|---|
| +PWR_SRC | +15V_ALW +3.3V_RTC_LDO +5V_ALW +3.3V_ALW |

LDO L6935TR 37

| INPUTS | OUTPUTS |
|-----------|-----------|
| +1.8V_SUS | +1.5V_RUN |

SYSTEM DC/DC TPS51117 38

| INPUTS | OUTPUTS |
|----------|-----------|
| +PWR_SRC | +1.8V_SUS |

SYSTEM DC/DC TPS51117 39

| INPUTS | OUTPUTS |
|----------|---------------|
| +PWR_SRC | +VCC GFX_CORE |

CHARGER MAX8731A 32

| INPUTS | OUTPUTS |
|------------------|----------|
| +DC_IN +PBATT | +PWR_SRC |

LDO TPS51100 38

| INPUTS | OUTPUTS |
|-----------|---------------------------------|
| +1.8V_SUS | +V_DDR_MCH_REF +0.9V_DDR_VTT |

LDO L6935TR 37

| INPUTS | OUTPUTS |
|-----------|-----------|
| +1.8V_SUS | +1.1V_RUN |

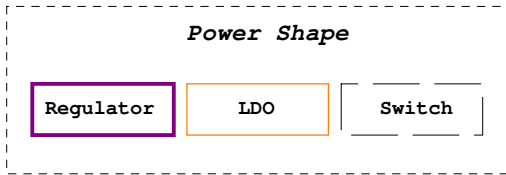
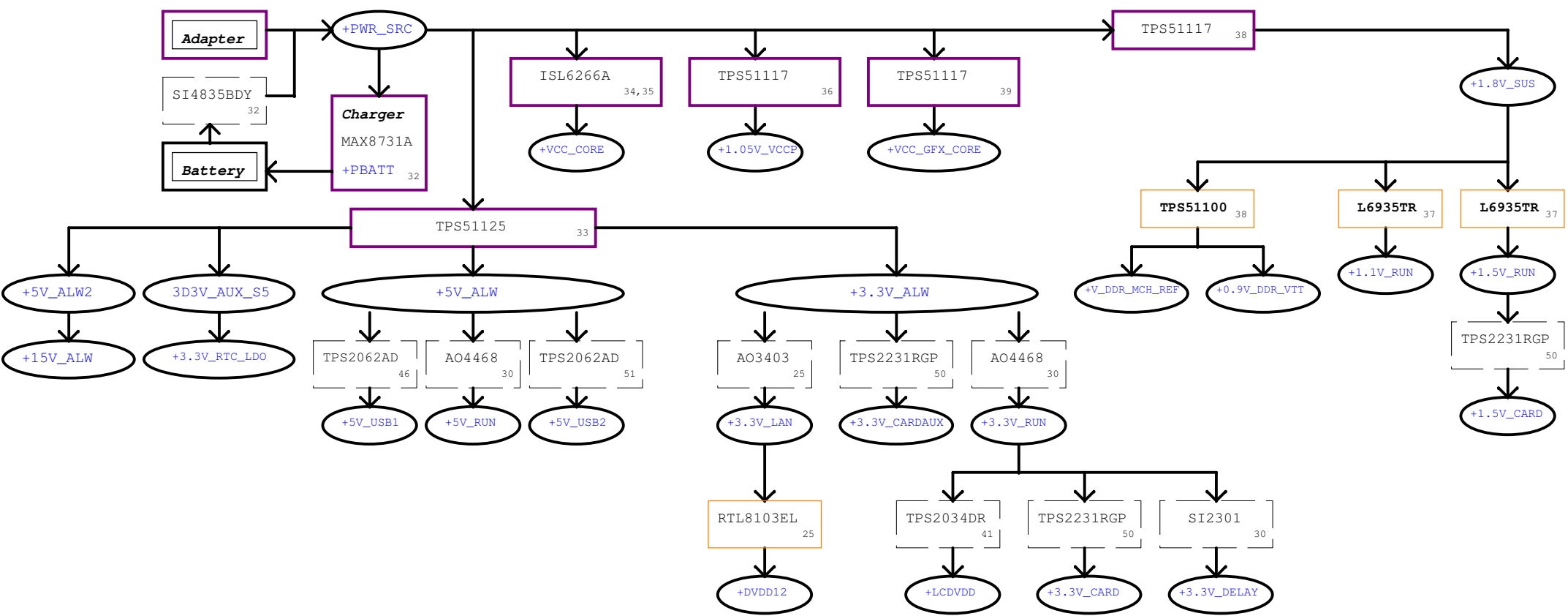
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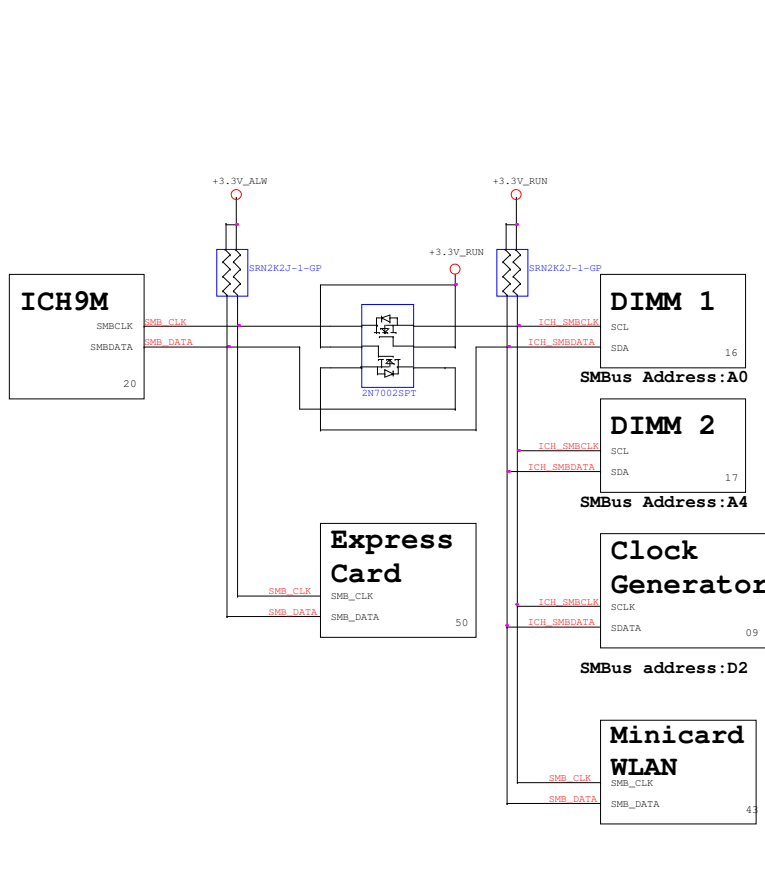
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Size: Custom Document Number: **Alba Discrete** Rev: **SB**

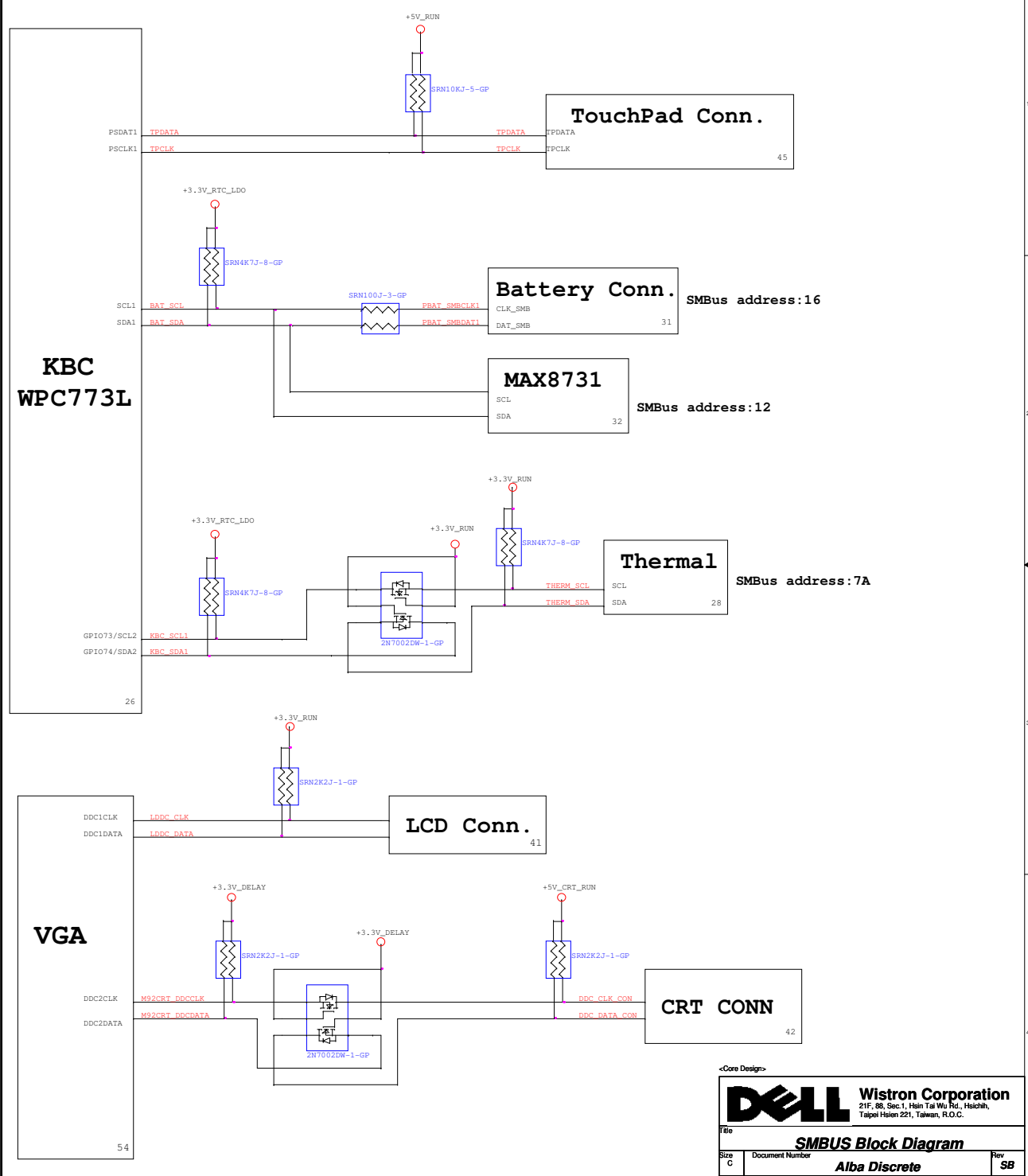
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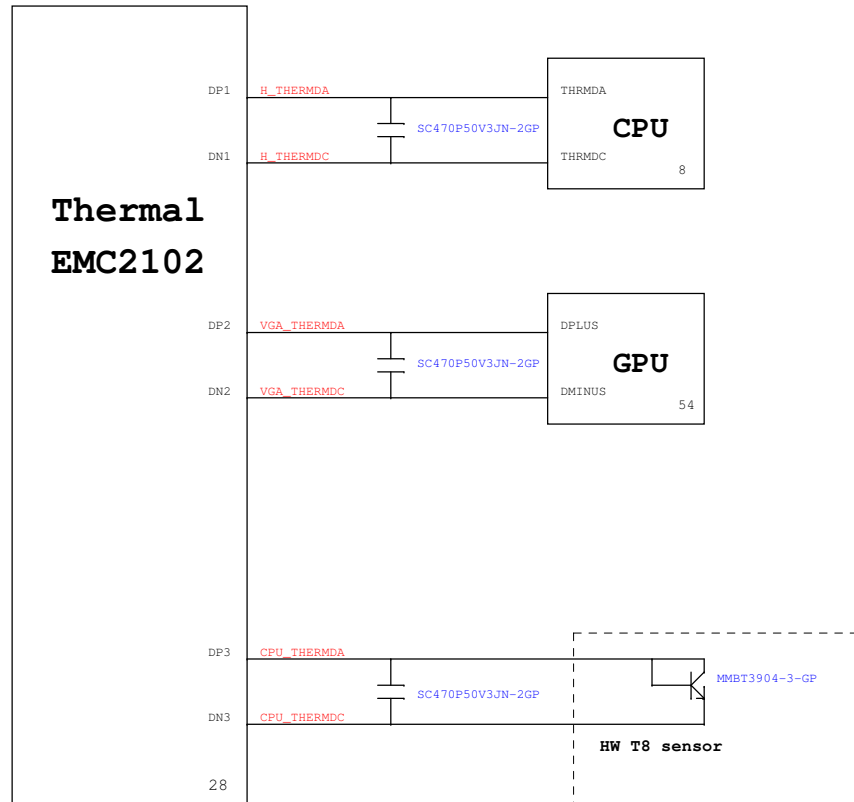
ICH9M SMBus Block Diagram



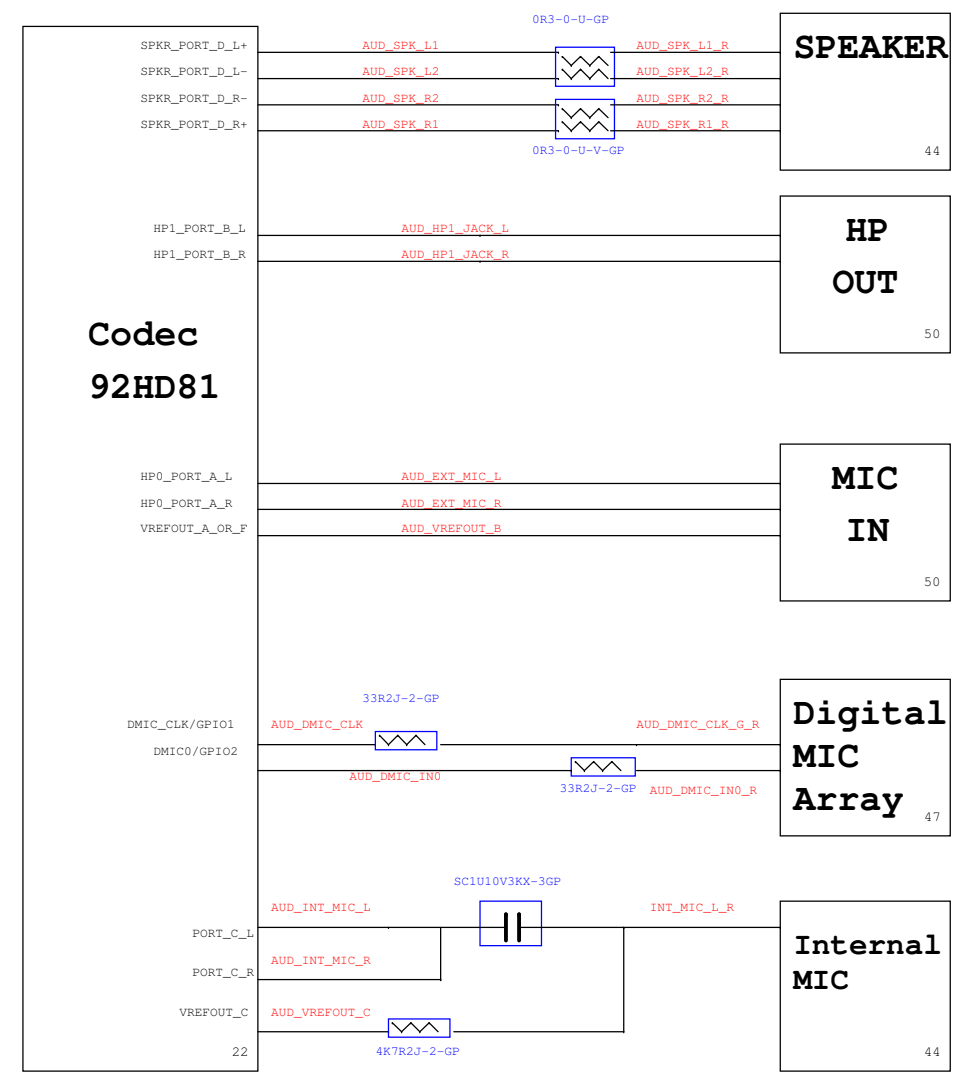
KBC SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram



ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5

ICH9 Integrated pull-up and pull-down Resistors

ICH9 EDS 642879 Rev.1.5

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 Rev.0.5

| Signal | Usage/When Sampled | Comment |
|------------------------|--|---|
| HDA_SDOUT | XOR Chain Entrance/PCIE Port Config1 bit1, Rising Edge of PWROK. | Allows entrance to XOR Chain testing when TP3 pulled low. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC (Config Registers: offset 224h). This signal has weak internal pull-down. |
| HDA_SYNC | PCIE config1 bit0, Rising Edge of PWROK. | This signal has a weak internal pull-down. Sets bit0 of PRC.PC (Config Registers: Offset 224h). |
| GNT2#/GPIO53 | PCIE config2 bit2, Rising Edge of PWROK. | This signal has a weak internal pull-up. Sets bit2 of PRC.PC2 (Config Registers: Offset 224h). |
| GPIO20 | Reserved. | This signal should not be pulled high. |
| GNT1#/GPIO51 | ESI Strap (Server Only) Rising Edge of PWROK. | ESI compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile. |
| GNT3#/GPIO55 | Top-Block Swap override. Rising Edge of PWROK. | Sampled low: Top-Block Swap mode (inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down. |
| GNT0#: SPI_CS1#/GPIO58 | Boot BIOS Destination Selection 0:1. Rising Edge of PWROK. | Controllable via Boot BIOS Destination bit (Config Registers: Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC |
| SPI_MOSI | Integrated TPM Enable, Rising Edge of CLPWROK | Sample low: the Integrated TPM will be disable. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable. |
| GPIO49 | DMI Termination Voltage. Rising Edge of CLPWROK. | The signal is required to be low for desktop applications and required to be high for mobile applications. |
| SATALED# | PCI Express Lane Reversal. Rising Edge of PWROK. | Signal has weak internal pull-up. Sets bit 27 of MPC.LR (Device 28: Function 0:Offset D8). |
| SPKR | No Reboot. Rising Edge of PWROK. | If sampled high, the system is strapped to the "No Reboot" mode (ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit. |
| TP3 | XOR Chain Entrance. Rising Edge of PWROK. | This signal should not be pull low unless using XOR Chain testing. |
| GPIO33/HDA_DOCK_EN# | Flash Descriptor Security Override Strap. Rising Edge of PWROK. | Sampled low: the Flash Descriptor Security will be overridden. If high, the security measures will be in effect. This should only be enabled in manufacturing environments using an external pull-up resistor. |

| SIGNAL | Resistor Type/Value |
|--------------------------|---|
| CL_CLK[1:0] | PULL-UP 20K |
| CL_DATA[1:0] | PULL-UP 20K |
| CL_RST0# | PULL-UP 20K |
| DPRSLEVR/GPIO16 | PULL-DOWN 20K |
| ENERGY_DETECT | PULL-UP 20K |
| HDA_BIT_CLK | PULL-DOWN 20K |
| HDA_DOCK_EN#/GPIO33 | PULL-UP 20K |
| HDA_RST# | PULL-DOWN 20K |
| HDA_SDIN[3:0] | PULL-DOWN 20K |
| HDA_SDOUT | PULL-DOWN 20K |
| HDA_SYNC | PULL-DOWN 20K |
| GLAN_DOCK# | The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller. |
| GNT[3:0]#/GPIO[55,53,51] | PULL-UP 20K |
| GPIO20 | PULL-DOWN 20K |
| GPIO49 | PULL-UP 20K |
| LDA[3:0]#/FWH[3:0]# | PULL-UP 20K |
| LAN_RXD[2:0] | PULL-UP 20K |
| LDRQ[0] | PULL-UP 20K |
| LDRQ[1]/GPIO23 | PULL-UP 20K |
| PME# | PULL-UP 20K |
| PWRBTN# | PULL-UP 20K |
| SATALED# | PULL-UP 15K |
| SPI_CS1#/GPIO58/CLGPIO6 | PULL-UP 20K |
| SPI_MOSI | PULL-DOWN 20K |
| SPI_MISO | PULL-UP 20K |
| SPKR | PULL-DOWN 20K |
| TACH_[3:0] | PULL-UP 20K |
| TP[3] | PULL-UP 20K |
| USB[11:0][P,N] | PULL-DOWN 15K |

| Pin Name | Strap Description | Configuration |
|--|---|--|
| CFG[2:0] | FSB Frequency Select | 000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved |
| CFG[4:3] CFG8 CFG[15:14] CFG[18:17] | Reserved | |
| CFG5 | DMI x2 Select | 0 = DMI x2 1 = DMI x4 (Default) |
| CFG6 | iTPM Host Interface | 0 = The iTPM Host Interface is enabled (Note 2) 1 = The iTPM Host Interface is disabled (default) |
| CFG7 | Intel Management engine crypto strap | 0 = Transport Layer Security (TLS) cipher suite with no confidentiality 1 = TLS cipher suite with confidentiality (Default) |
| CFG9 | PCIE Graphics Lane | 0 = Reserved Lanes, 15->0, 14->1 ect.. 1 = Normal operation (Default): Lane Numbered in Order |
| CFG10 | PCIE Loopback enable | 0 = Enable (Note 3) 1 = Disable (Default) |
| CFG[13:12] | XOR/ALL | 00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enable (Note 3) 11 = Disabled (Default) |
| CFG16 | FSB Dynamic ODT | 0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default) |
| CFG19 | DMI Lane Reversal | 0 = Normal operation (Default): Lane Numbered in Order 1 = Reverse Lanes DMI x4 mode [MCH->ICH]: (3->0, 2->1, 1->2 and 0->3) DMI x2 mode [MCH->ICH]: (3->0, 2->1) |
| CFG20 | Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE | 0 = Only Digital Display Port or PCIE is operational (Default) 1 = Digital display Port and PCIE are operating simultaneously via the PEG port |
| SDVO_CTRLDATA | SDVO Present | 0 = No SDVO Card Present (Default) 1 = SDVO Card Present |
| L_DDC_DATA | Local Flat Panel (LFP) Present | 0 = LFP Disabled (Default) 1 = LFP Card Present; PCIE disabled |

- NOTE:**
- All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
 - iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6. Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.


PCIE Routing

| LANE2 | MiniCard WLAN |
|-------|---------------|
| LANE3 | LAN |
| LANE5 | New Card |

USB Table

| USB | |
|------|-------------|
| Pair | Device |
| 0 | USB1 |
| 1 | USB2 |
| 2 | USB3 |
| 3 | RESERVED |
| 4 | MINI CARD |
| 5 | RESERVED |
| 6 | BLUETOOTH |
| 7 | NEW CARD |
| 8 | RESERVED |
| 9 | RESERVED |
| 10 | Card Reader |
| 11 | CAMERA |

-Core Design-

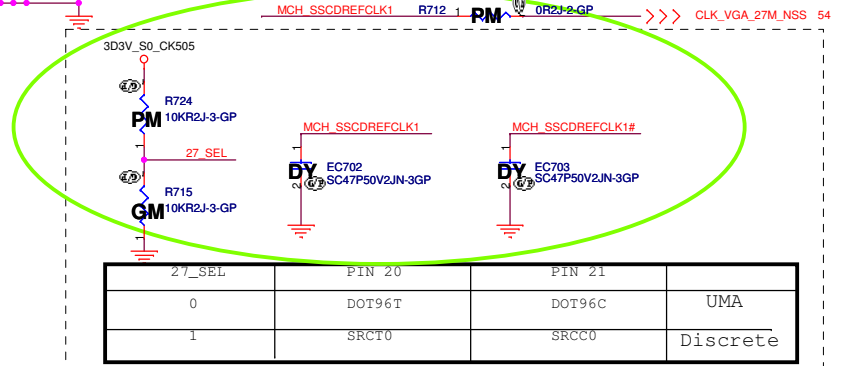
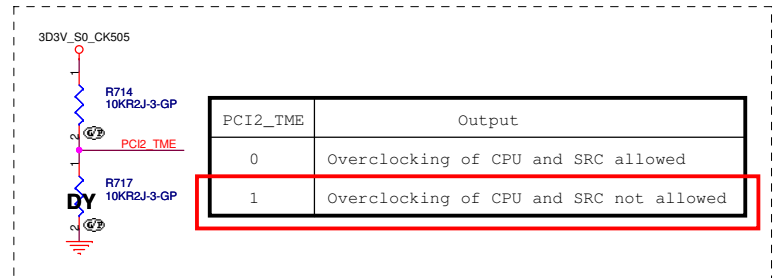
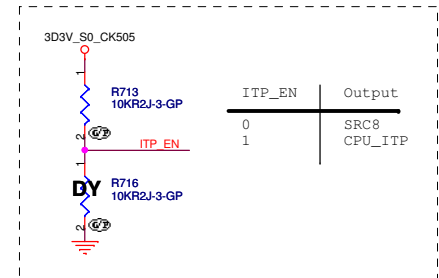
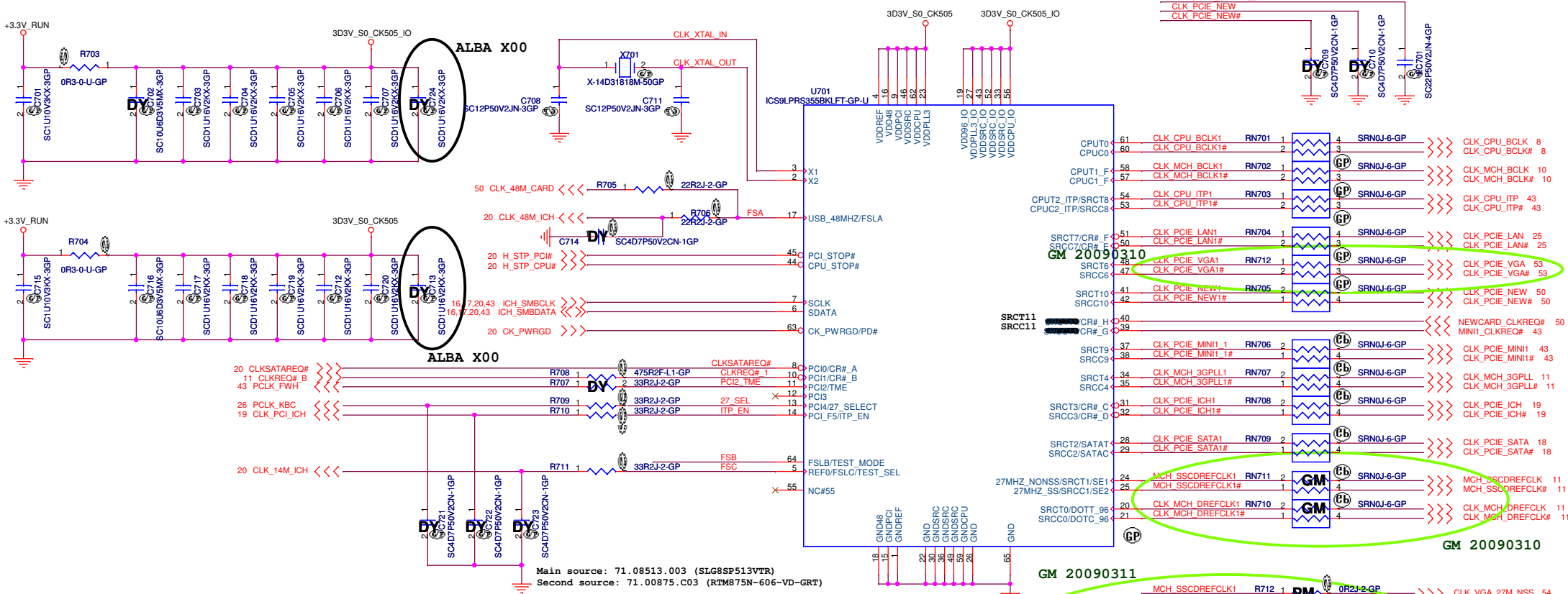


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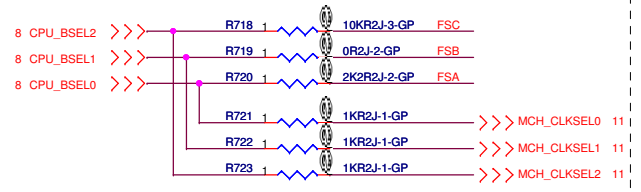
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SSID = CLOCK



| SEL2 | SEL1 | SEL0 | CPU | FSB |
|------|------|------|------|-------|
| FSC | FSB | FSA | | |
| 1 | 0 | 1 | 100M | X |
| 0 | 0 | 1 | 133M | 533M |
| 0 | 1 | 1 | 166M | 667M |
| 0 | 1 | 0 | 200M | 800M |
| 0 | 0 | 0 | 266M | 1067M |



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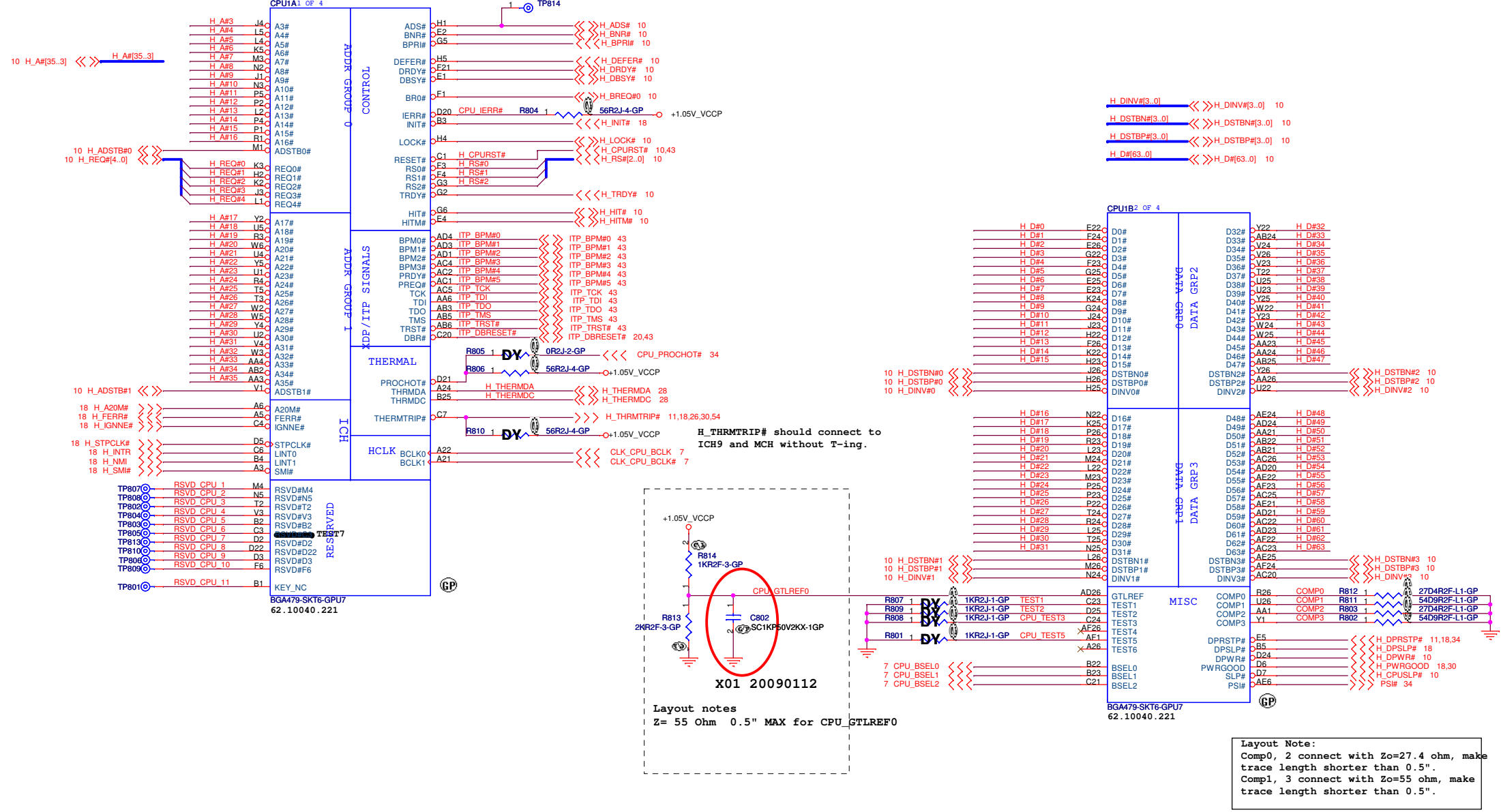
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Title: **Clock Generator SLG8SP513VTR**

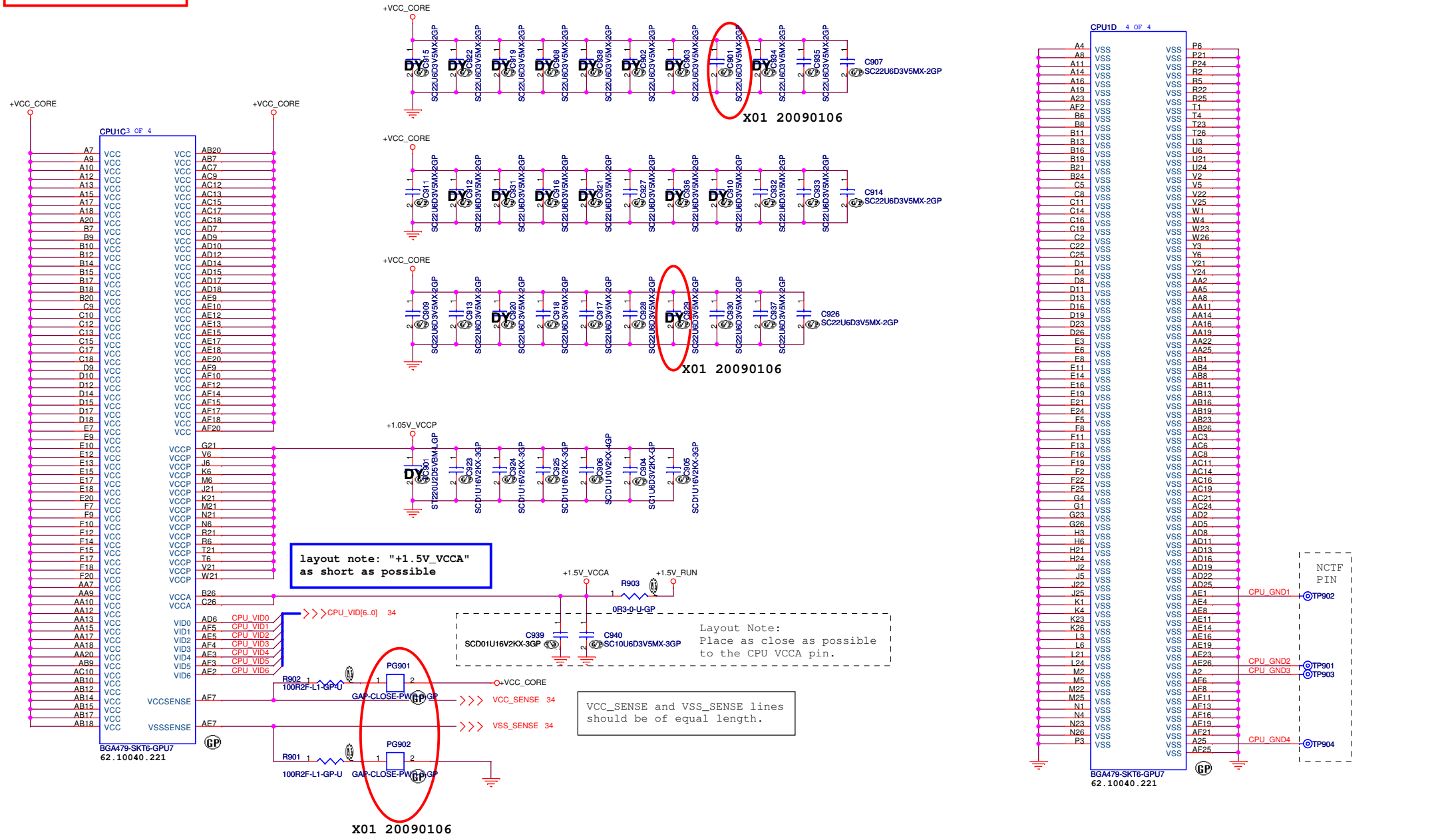
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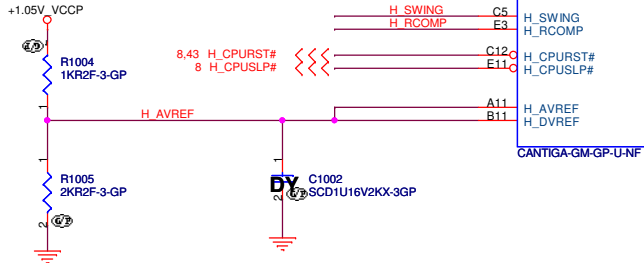
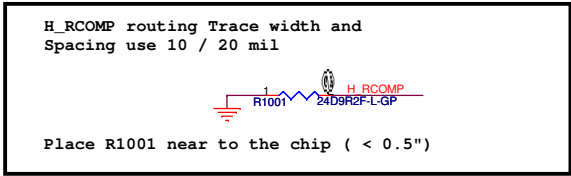
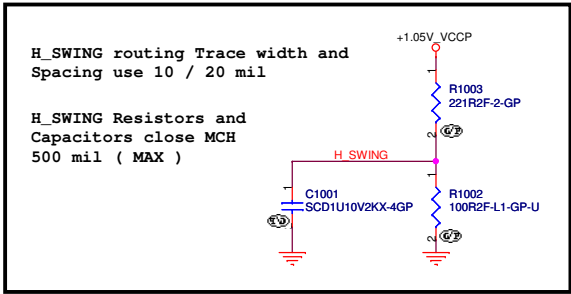
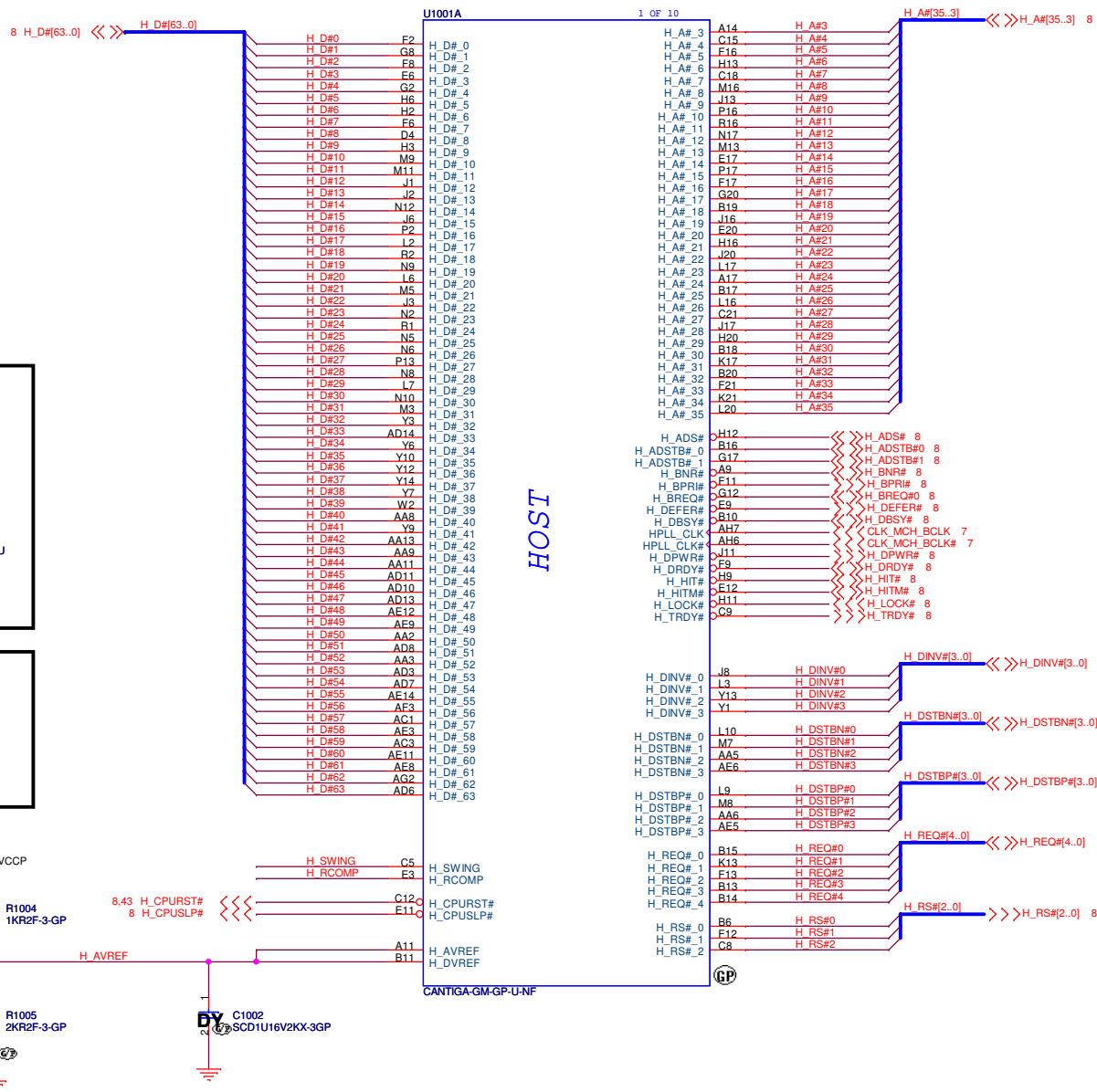
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D
C
B
A



SSID = CPU

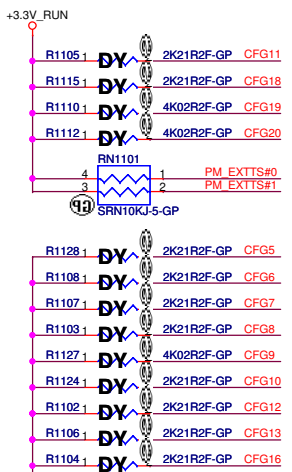




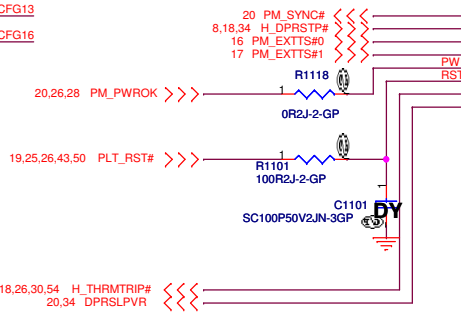
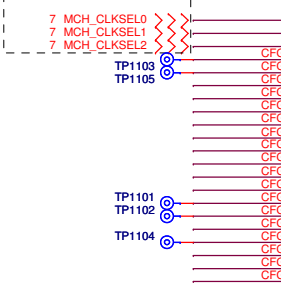
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* is current setting

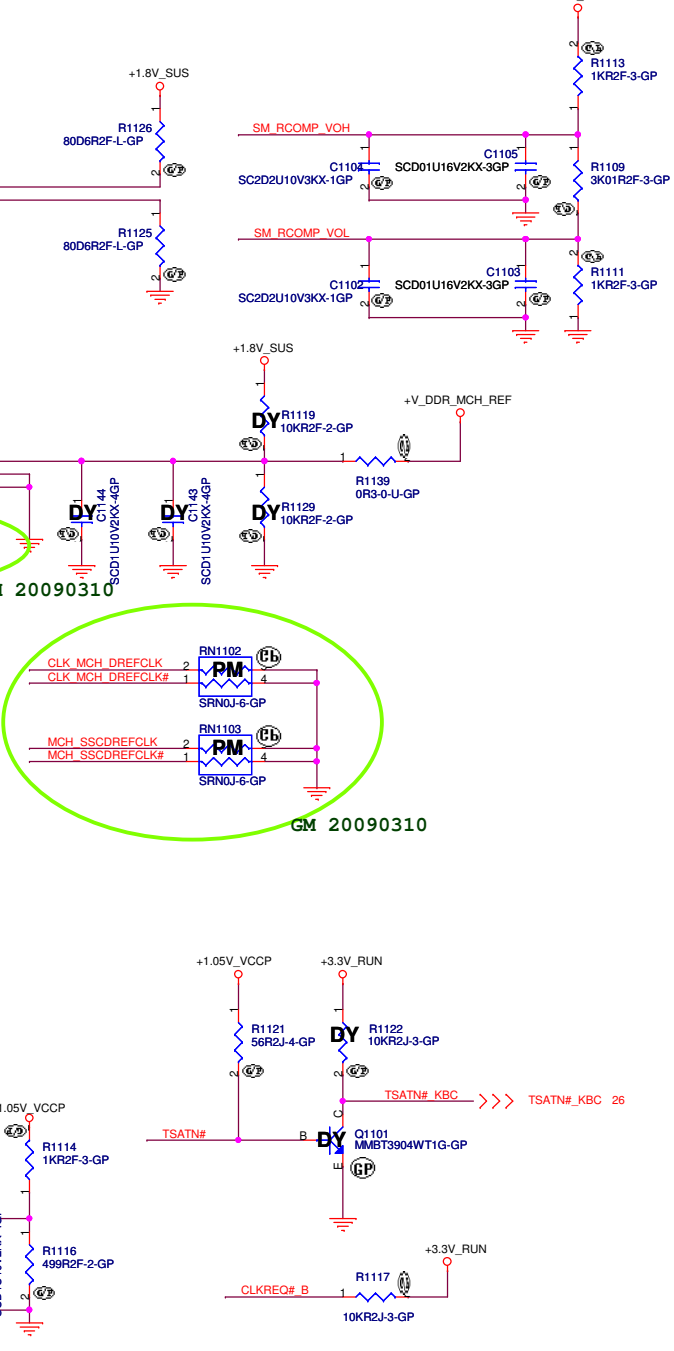
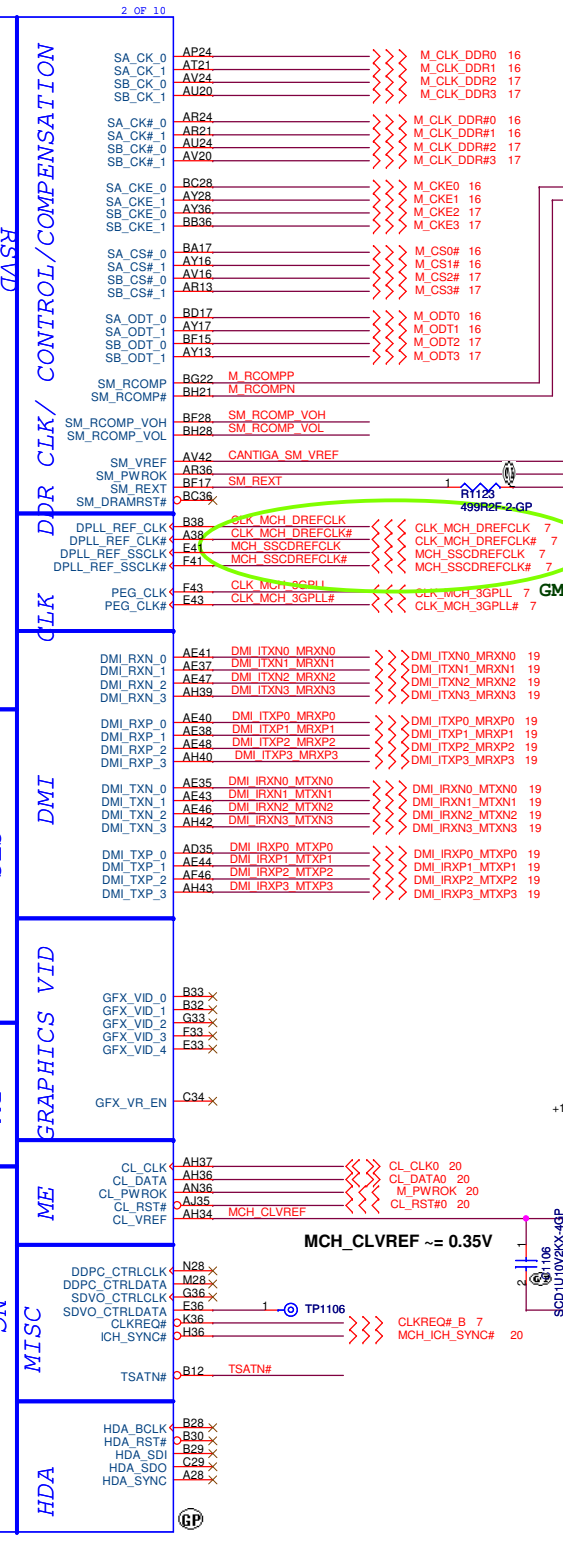
| CFG Strap | Low | High |
|---------------|--|---|
| CFG 5 | DMI X 2 | DMI X 4 * |
| CFG 6 | ITPM enable | ITPM disable * |
| CFG 7 | TLS cipher suite with no confidentiality | TLS cipher suite with confidentiality * |
| CFG 9 | PCIE GFX lane reversed | PCIE GFX lane numbered in order * |
| CFG 10 | PCIE loopback enable | PCIE loopback disable * |
| CFG 12 | ALLZ mode enable | ALLZ mode disable * |
| CFG 13 | XOR mode enable | XOR mode disable * |
| CFG 16 | FSB dynamic ODT disable | FSB Dynamic ODT enable * |
| CFG 19 | DMI Lane Reserved | Reverse DMI lanes * |
| CFG 20 | SDVO concurrent with PCIE | PCIE and SDVO are operating simultaneously via the PEG port * |
| SDVO_CTRLDATA | SDVO interface disable * | SDVO interface enable |
| L_DDC_DATA | LFP disable * | LFP card present |
| DDPC_CTRLDATA | SDVO/iHDMI/DP interface disabled * | SDVO/iHDMI/DP interface enabled |



FSB setting



- U1001B 2 OF 10
- M36 RESERVED#M36
- N36 RESERVED#N36
- R33 RESERVED#R33
- T33 RESERVED#T33
- AH9 RESERVED#AH9
- AH10 RESERVED#AH10
- AH12 RESERVED#AH12
- AH13 RESERVED#AH13
- K12 RESERVED#K12
- AL34 RESERVED#AL34
- AK34 RESERVED#AK34
- AN35 RESERVED#AN35
- T24 RESERVED#T24
- B31 RESERVED#B31
- B1 RESERVED#B1
- M1 RESERVED#M1
- AY21 RESERVED#AY21
- BG23 RESERVED#BG23
- BF23 RESERVED#BF23
- BH18 RESERVED#BH18
- BF18 RESERVED#BF18
- CFG_0
- CFG_1
- CFG_2
- CFG_3
- CFG_4
- CFG_5
- CFG_6
- CFG_7
- CFG_8
- CFG_9
- CFG_10
- CFG_11
- CFG_12
- CFG_13
- CFG_14
- CFG_15
- CFG_16
- CFG_17
- CFG_18
- CFG_19
- CFG_20
- PM_SYNC#
- PM_DPRSTP#
- PM_EXT_TS#_0
- PM_EXT_TS#_1
- PWROK_R
- RSTIN#
- NC#BG48
- NC#BF48
- NC#BD48
- NC#BC48
- NC#BH47
- NC#BG47
- NC#BE47
- NC#BF46
- NC#BE46
- NC#BG45
- NC#BH44
- NC#BH43
- NC#BH6
- NC#BH5
- NC#BH4
- NC#BH3
- NC#BF3
- NC#BH2
- NC#BG2
- NC#BE2
- NC#BG1
- NC#BF1
- NC#BD1
- NC#BC1
- NC#F1
- NC#A47



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File: **Cantiga-DMI/CFG(2/6)**

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Alba Discrete Rev SB

16 M_A_DQ[63..0] <<< M_A_DQ[63..0]

| U1001D | | |
|----------|------|----------|
| M_A_DQ0 | AJ38 | SA_DQ_0 |
| M_A_DQ1 | AJ41 | SA_DQ_1 |
| M_A_DQ2 | AN38 | SA_DQ_2 |
| M_A_DQ3 | AM38 | SA_DQ_3 |
| M_A_DQ4 | AJ36 | SA_DQ_4 |
| M_A_DQ5 | AJ49 | SA_DQ_5 |
| M_A_DQ6 | AM44 | SA_DQ_6 |
| M_A_DQ7 | AM42 | SA_DQ_7 |
| M_A_DQ8 | AN43 | SA_DQ_8 |
| M_A_DQ9 | AN44 | SA_DQ_9 |
| M_A_DQ10 | AJ49 | SA_DQ_10 |
| M_A_DQ11 | AI38 | SA_DQ_11 |
| M_A_DQ12 | AN41 | SA_DQ_12 |
| M_A_DQ13 | AN39 | SA_DQ_13 |
| M_A_DQ14 | AU44 | SA_DQ_14 |
| M_A_DQ15 | AU42 | SA_DQ_15 |
| M_A_DQ16 | AV39 | SA_DQ_16 |
| M_A_DQ17 | AY44 | SA_DQ_17 |
| M_A_DQ18 | BA40 | SA_DQ_18 |
| M_A_DQ19 | BD43 | SA_DQ_19 |
| M_A_DQ20 | AV41 | SA_DQ_20 |
| M_A_DQ21 | AV43 | SA_DQ_21 |
| M_A_DQ22 | BD43 | SA_DQ_22 |
| M_A_DQ23 | BC40 | SA_DQ_23 |
| M_A_DQ24 | AY37 | SA_DQ_24 |
| M_A_DQ25 | BD38 | SA_DQ_25 |
| M_A_DQ26 | AV37 | SA_DQ_26 |
| M_A_DQ27 | AI36 | SA_DQ_27 |
| M_A_DQ28 | AY38 | SA_DQ_28 |
| M_A_DQ29 | BB38 | SA_DQ_29 |
| M_A_DQ30 | AV36 | SA_DQ_30 |
| M_A_DQ31 | AW36 | SA_DQ_31 |
| M_A_DQ32 | BD13 | SA_DQ_32 |
| M_A_DQ33 | AU11 | SA_DQ_33 |
| M_A_DQ34 | BC11 | SA_DQ_34 |
| M_A_DQ35 | BA12 | SA_DQ_35 |
| M_A_DQ36 | AU13 | SA_DQ_36 |
| M_A_DQ37 | AV13 | SA_DQ_37 |
| M_A_DQ38 | BD12 | SA_DQ_38 |
| M_A_DQ39 | BC12 | SA_DQ_39 |
| M_A_DQ40 | BB9 | SA_DQ_40 |
| M_A_DQ41 | BA9 | SA_DQ_41 |
| M_A_DQ42 | AU10 | SA_DQ_42 |
| M_A_DQ43 | AV9 | SA_DQ_43 |
| M_A_DQ44 | BA11 | SA_DQ_44 |
| M_A_DQ45 | BD9 | SA_DQ_45 |
| M_A_DQ46 | AY8 | SA_DQ_46 |
| M_A_DQ47 | BA6 | SA_DQ_47 |
| M_A_DQ48 | AV5 | SA_DQ_48 |
| M_A_DQ49 | AV7 | SA_DQ_49 |
| M_A_DQ50 | AT9 | SA_DQ_50 |
| M_A_DQ51 | AN8 | SA_DQ_51 |
| M_A_DQ52 | AU5 | SA_DQ_52 |
| M_A_DQ53 | AU6 | SA_DQ_53 |
| M_A_DQ54 | AT5 | SA_DQ_54 |
| M_A_DQ55 | AN10 | SA_DQ_55 |
| M_A_DQ56 | AM11 | SA_DQ_56 |
| M_A_DQ57 | AM5 | SA_DQ_57 |
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| M_A_DQ59 | AJ8 | SA_DQ_59 |
| M_A_DQ60 | AN12 | SA_DQ_60 |
| M_A_DQ61 | AM13 | SA_DQ_61 |
| M_A_DQ62 | AJ11 | SA_DQ_62 |
| M_A_DQ63 | AJ12 | SA_DQ_63 |

DDR SYSTEM MEMORY A

| | | |
|-----------|------|-----------------|
| SA_BS_0 | BD21 | M_A_BS#0 16 |
| SA_BS_1 | BG18 | M_A_BS#1 16 |
| SA_BS_2 | AT25 | M_A_BS#2 16 |
| SA_RAS# | BB20 | M_A_RAS# 16 |
| SA_CAS# | BB20 | M_A_CAS# 16 |
| SA_WE# | AY20 | M_A_WE# 16 |
| SA_DM_0 | AM37 | M_A_DM[7..0] 16 |
| SA_DM_1 | AT41 | M_A_DM1 |
| SA_DM_2 | AY41 | M_A_DM2 |
| SA_DM_3 | AU39 | M_A_DM3 |
| SA_DM_4 | BB12 | M_A_DM4 |
| SA_DM_5 | AV6 | M_A_DM5 |
| SA_DM_6 | AT7 | M_A_DM6 |
| SA_DM_7 | AJ5 | M_A_DM7 |
| SA_DQS_0 | AJ44 | M_A_DQS0 |
| SA_DQS_1 | AT44 | M_A_DQS1 |
| SA_DQS_2 | BA43 | M_A_DQS2 |
| SA_DQS_3 | BC37 | M_A_DQS3 |
| SA_DQS_4 | AW12 | M_A_DQS4 |
| SA_DQS_5 | BC8 | M_A_DQS5 |
| SA_DQS_6 | AU8 | M_A_DQS6 |
| SA_DQS_7 | AM7 | M_A_DQS7 |
| SA_DQS#_0 | AJ43 | M_A_DQS#0 |
| SA_DQS#_1 | AT43 | M_A_DQS#1 |
| SA_DQS#_2 | BA44 | M_A_DQS#2 |
| SA_DQS#_3 | BD37 | M_A_DQS#3 |
| SA_DQS#_4 | AY12 | M_A_DQS#4 |
| SA_DQS#_5 | BD8 | M_A_DQS#5 |
| SA_DQS#_6 | AU9 | M_A_DQS#6 |
| SA_DQS#_7 | AM8 | M_A_DQS#7 |
| SA_MA_0 | BA21 | M_A_A[14..0] 16 |
| SA_MA_1 | BC24 | M_A_A1 |
| SA_MA_2 | BG24 | M_A_A2 |
| SA_MA_3 | BH24 | M_A_A3 |
| SA_MA_4 | BG25 | M_A_A4 |
| SA_MA_5 | BA24 | M_A_A5 |
| SA_MA_6 | BD24 | M_A_A6 |
| SA_MA_7 | BG27 | M_A_A7 |
| SA_MA_8 | BF26 | M_A_A8 |
| SA_MA_9 | AW24 | M_A_A9 |
| SA_MA_10 | BC21 | M_A_A10 |
| SA_MA_11 | BG26 | M_A_A11 |
| SA_MA_12 | BH26 | M_A_A12 |
| SA_MA_13 | BH17 | M_A_A13 |
| SA_MA_14 | AY26 | M_A_A14 |

CANTIGA-GM-GP-U-NF



17 M_B_DQ[63..0] <<< M_B_DQ[63..0]

| U1001E | | |
|----------|------|----------|
| M_B_DQ0 | AK47 | SB_DQ_0 |
| M_B_DQ1 | AH46 | SB_DQ_1 |
| M_B_DQ2 | AP47 | SB_DQ_2 |
| M_B_DQ3 | AP46 | SB_DQ_3 |
| M_B_DQ4 | AJ46 | SB_DQ_4 |
| M_B_DQ5 | AJ48 | SB_DQ_5 |
| M_B_DQ6 | AM48 | SB_DQ_6 |
| M_B_DQ7 | AP48 | SB_DQ_7 |
| M_B_DQ8 | AU47 | SB_DQ_8 |
| M_B_DQ9 | AU46 | SB_DQ_9 |
| M_B_DQ10 | BA48 | SB_DQ_10 |
| M_B_DQ11 | AY48 | SB_DQ_11 |
| M_B_DQ12 | AT47 | SB_DQ_12 |
| M_B_DQ13 | AR47 | SB_DQ_13 |
| M_B_DQ14 | BA47 | SB_DQ_14 |
| M_B_DQ15 | BC47 | SB_DQ_15 |
| M_B_DQ16 | RC46 | SB_DQ_16 |
| M_B_DQ17 | BC44 | SB_DQ_17 |
| M_B_DQ18 | BG43 | SB_DQ_18 |
| M_B_DQ19 | BF43 | SB_DQ_19 |
| M_B_DQ20 | BE45 | SB_DQ_20 |
| M_B_DQ21 | BC41 | SB_DQ_21 |
| M_B_DQ22 | BF40 | SB_DQ_22 |
| M_B_DQ23 | BF41 | SB_DQ_23 |
| M_B_DQ24 | BG38 | SB_DQ_24 |
| M_B_DQ25 | BF38 | SB_DQ_25 |
| M_B_DQ26 | BH35 | SB_DQ_26 |
| M_B_DQ27 | BG35 | SB_DQ_27 |
| M_B_DQ28 | BH40 | SB_DQ_28 |
| M_B_DQ29 | BG39 | SB_DQ_29 |
| M_B_DQ30 | BG34 | SB_DQ_30 |
| M_B_DQ31 | BH34 | SB_DQ_31 |
| M_B_DQ32 | BH14 | SB_DQ_32 |
| M_B_DQ33 | BG12 | SB_DQ_33 |
| M_B_DQ34 | BH11 | SB_DQ_34 |
| M_B_DQ35 | BG8 | SB_DQ_35 |
| M_B_DQ36 | BH12 | SB_DQ_36 |
| M_B_DQ37 | BF11 | SB_DQ_37 |
| M_B_DQ38 | BF8 | SB_DQ_38 |
| M_B_DQ39 | BC7 | SB_DQ_39 |
| M_B_DQ40 | BC5 | SB_DQ_40 |
| M_B_DQ41 | BC6 | SB_DQ_41 |
| M_B_DQ42 | AY3 | SB_DQ_42 |
| M_B_DQ43 | AY1 | SB_DQ_43 |
| M_B_DQ44 | BF6 | SB_DQ_44 |
| M_B_DQ45 | BF5 | SB_DQ_45 |
| M_B_DQ46 | BA1 | SB_DQ_46 |
| M_B_DQ47 | BD3 | SB_DQ_47 |
| M_B_DQ48 | AV2 | SB_DQ_48 |
| M_B_DQ49 | AU3 | SB_DQ_49 |
| M_B_DQ50 | AR3 | SB_DQ_50 |
| M_B_DQ51 | AN2 | SB_DQ_51 |
| M_B_DQ52 | AY2 | SB_DQ_52 |
| M_B_DQ53 | AV1 | SB_DQ_53 |
| M_B_DQ54 | AP3 | SB_DQ_54 |
| M_B_DQ55 | AR1 | SB_DQ_55 |
| M_B_DQ56 | AI1 | SB_DQ_56 |
| M_B_DQ57 | AI2 | SB_DQ_57 |
| M_B_DQ58 | AJ1 | SB_DQ_58 |
| M_B_DQ59 | AH1 | SB_DQ_59 |
| M_B_DQ60 | AM2 | SB_DQ_60 |
| M_B_DQ61 | AM3 | SB_DQ_61 |
| M_B_DQ62 | AH3 | SB_DQ_62 |
| M_B_DQ63 | AJ3 | SB_DQ_63 |

DDR SYSTEM MEMORY B

| | | |
|-----------|------|-----------------|
| SB_BS_0 | BC16 | M_B_BS#0 17 |
| SB_BS_1 | BB17 | M_B_BS#1 17 |
| SB_BS_2 | BB33 | M_B_BS#2 17 |
| SB_RAS# | AU17 | M_B_RAS# 17 |
| SB_CAS# | BG16 | M_B_CAS# 17 |
| SB_WE# | BF14 | M_B_WE# 17 |
| SB_DM_0 | AM47 | M_B_DM[7..0] 17 |
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| SB_DM_2 | BD40 | M_B_DM2 |
| SB_DM_3 | BF35 | M_B_DM3 |
| SB_DM_4 | BG11 | M_B_DM4 |
| SB_DM_5 | BA3 | M_B_DM5 |
| SB_DM_6 | AP1 | M_B_DM6 |
| SB_DM_7 | AK2 | M_B_DM7 |
| SB_DQS_0 | AL47 | M_B_DQS0 |
| SB_DQS_1 | AV46 | M_B_DQS1 |
| SB_DQS_2 | BG41 | M_B_DQS2 |
| SB_DQS_3 | BG37 | M_B_DQS3 |
| SB_DQS_4 | BH9 | M_B_DQS4 |
| SB_DQS_5 | BB2 | M_B_DQS5 |
| SB_DQS_6 | AU1 | M_B_DQS6 |
| SB_DQS_7 | AN6 | M_B_DQS7 |
| SB_DQS#_0 | AL46 | M_B_DQS#0 |
| SB_DQS#_1 | AV47 | M_B_DQS#1 |
| SB_DQS#_2 | BH41 | M_B_DQS#2 |
| SB_DQS#_3 | BH37 | M_B_DQS#3 |
| SB_DQS#_4 | BG9 | M_B_DQS#4 |
| SB_DQS#_5 | BC2 | M_B_DQS#5 |
| SB_DQS#_6 | AT2 | M_B_DQS#6 |
| SB_DQS#_7 | AN5 | M_B_DQS#7 |
| SB_MA_0 | AV17 | M_B_A[14..0] 17 |
| SB_MA_1 | BA25 | M_B_A1 |
| SB_MA_2 | AU25 | M_B_A2 |
| SB_MA_3 | AW25 | M_B_A3 |
| SB_MA_4 | BB28 | M_B_A4 |
| SB_MA_5 | BB28 | M_B_A5 |
| SB_MA_6 | AW28 | M_B_A6 |
| SB_MA_7 | AT33 | M_B_A7 |
| SB_MA_8 | BD33 | M_B_A8 |
| SB_MA_9 | BB16 | M_B_A9 |
| SB_MA_10 | AW33 | M_B_A10 |
| SB_MA_11 | AY33 | M_B_A11 |
| SB_MA_12 | BH15 | M_B_A12 |
| SB_MA_13 | BH15 | M_B_A13 |
| SB_MA_14 | AU33 | M_B_A14 |

CANTIGA-GM-GP-U-NF

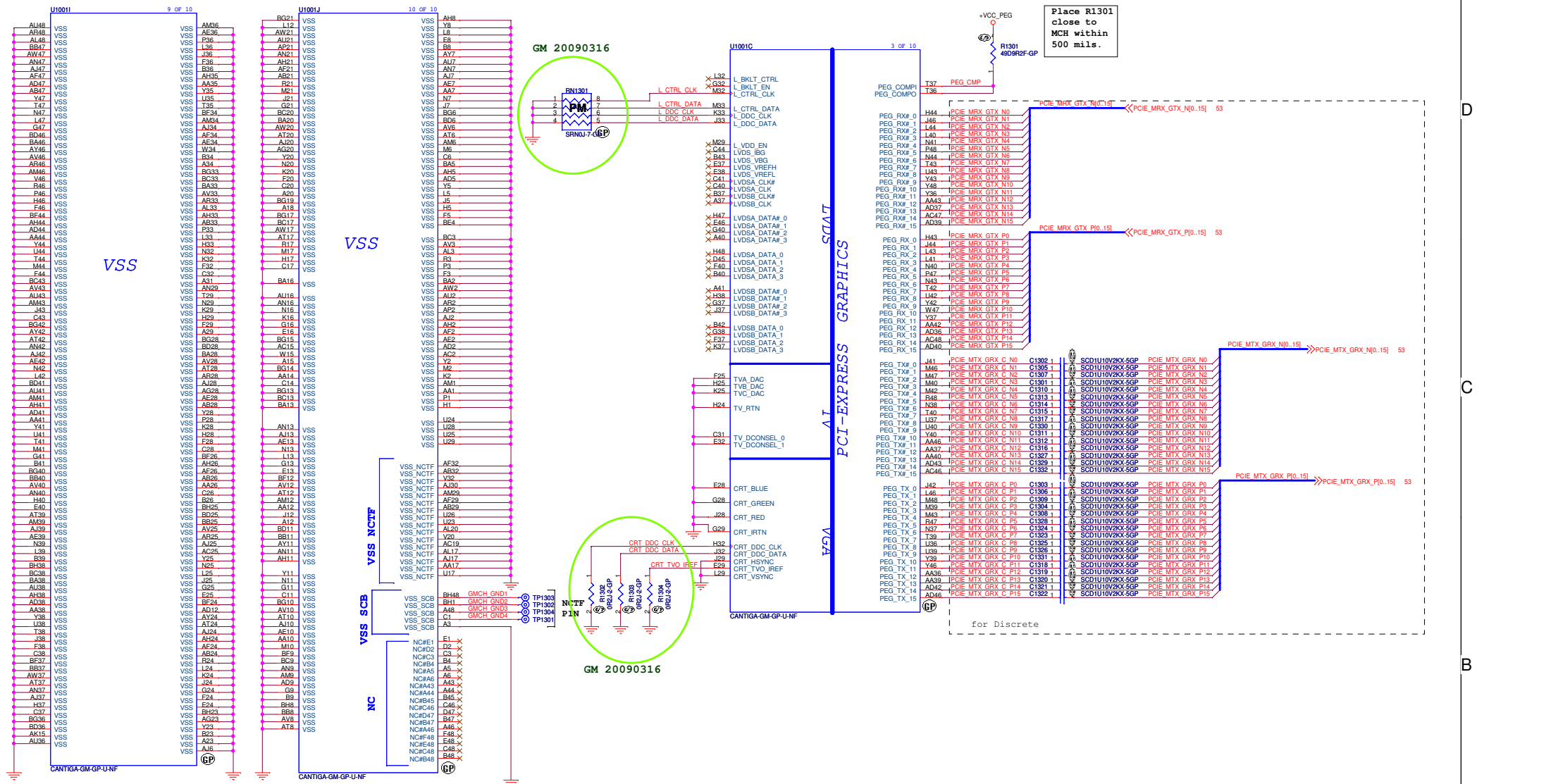


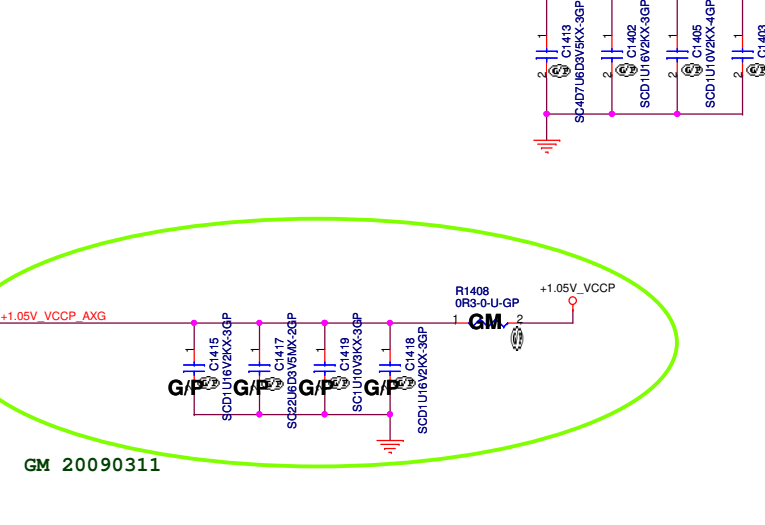
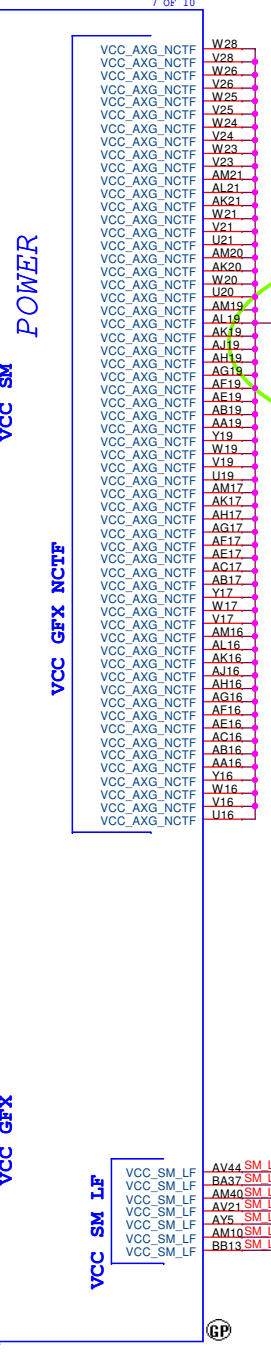
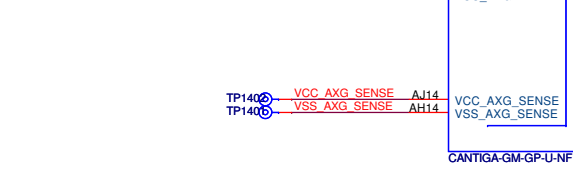
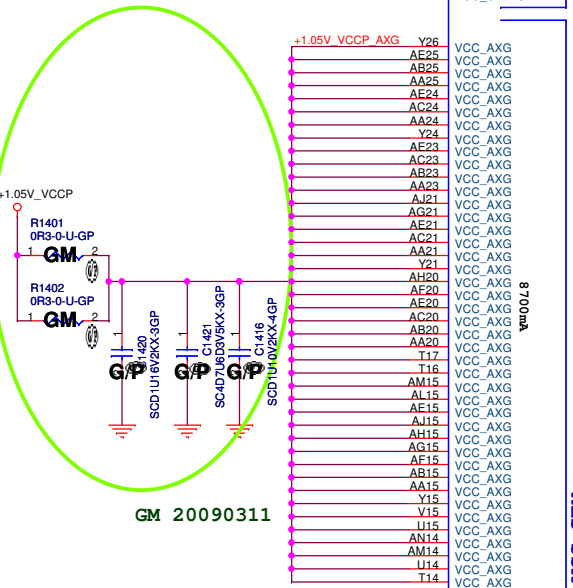
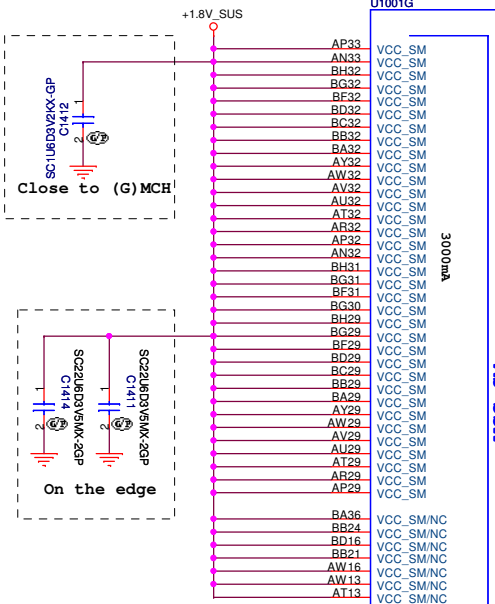
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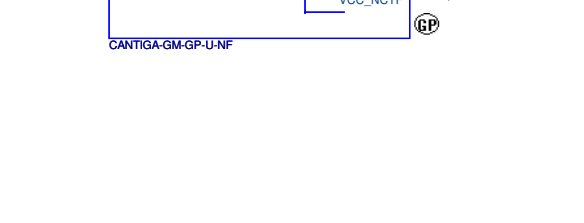
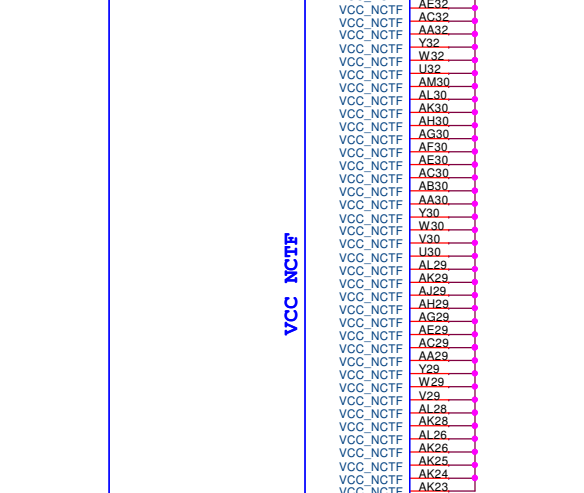
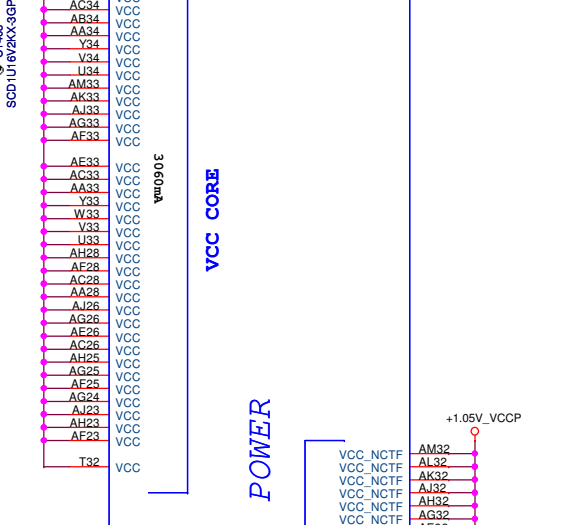
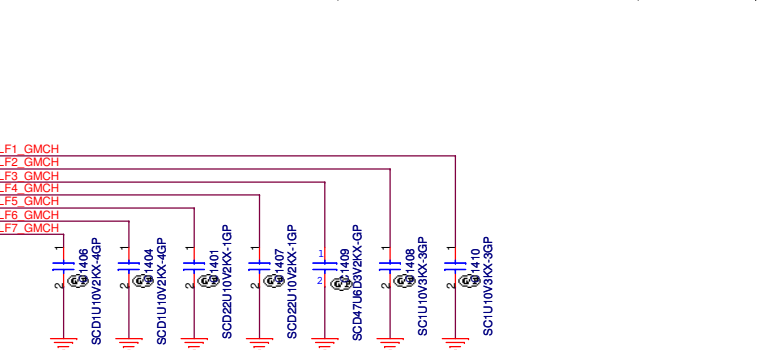
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| Title | | Cantiga-DDR(3/6) | |
| Size | Document Number | Rev | SB |
| Custom | Alba Discrete | | |
| Date: | Monday, March 23, 2009 | Sheet | 12 of 59 |

SSID = MCH





| Supply | Signal Group | I _{max} |
|-------------|--------------|------------------|
| +1.05V_VCCP | VCC | 3060mA |
| +1.05V_VCCP | VTT | 852mA |
| +1.05V_VCCP | VCC_PEG | 1782mA |
| +1.05V_VCCP | VCC_DMI | 456mA |
| +1.05V_VCCP | VCCA_SM | 720mA |
| +1.05V_VCCP | VCCA_SM_CK | 26mA |
| +1.05V_VCCP | VCCA_HPLL | 24mA |
| +1.05V_VCCP | VCCA_MPLL | 139.2mA |
| +1.05V_VCCP | VCCD_HPLL | 157.2mA |
| +1.05V_VCCP | VCCA_PEG_PLL | 50mA |
| +1.05V_VCCP | VCCD_PEG_PLL | 50mA |
| +1.05V_VCCP | VCC_AXF | 321.35mA |
| +1.5V_RUN | VCCD_TV DAC | 35mA |
| +1.8V_SUS | VCC_SM | 3000mA |
| +1.8V_SUS | VCC_SM_CK | 124mA |
| +1.5V_RUN | VCCA_PEG_BG | 414uA |
| +3.3V_RUN | VCC_HV | 105.3mA |

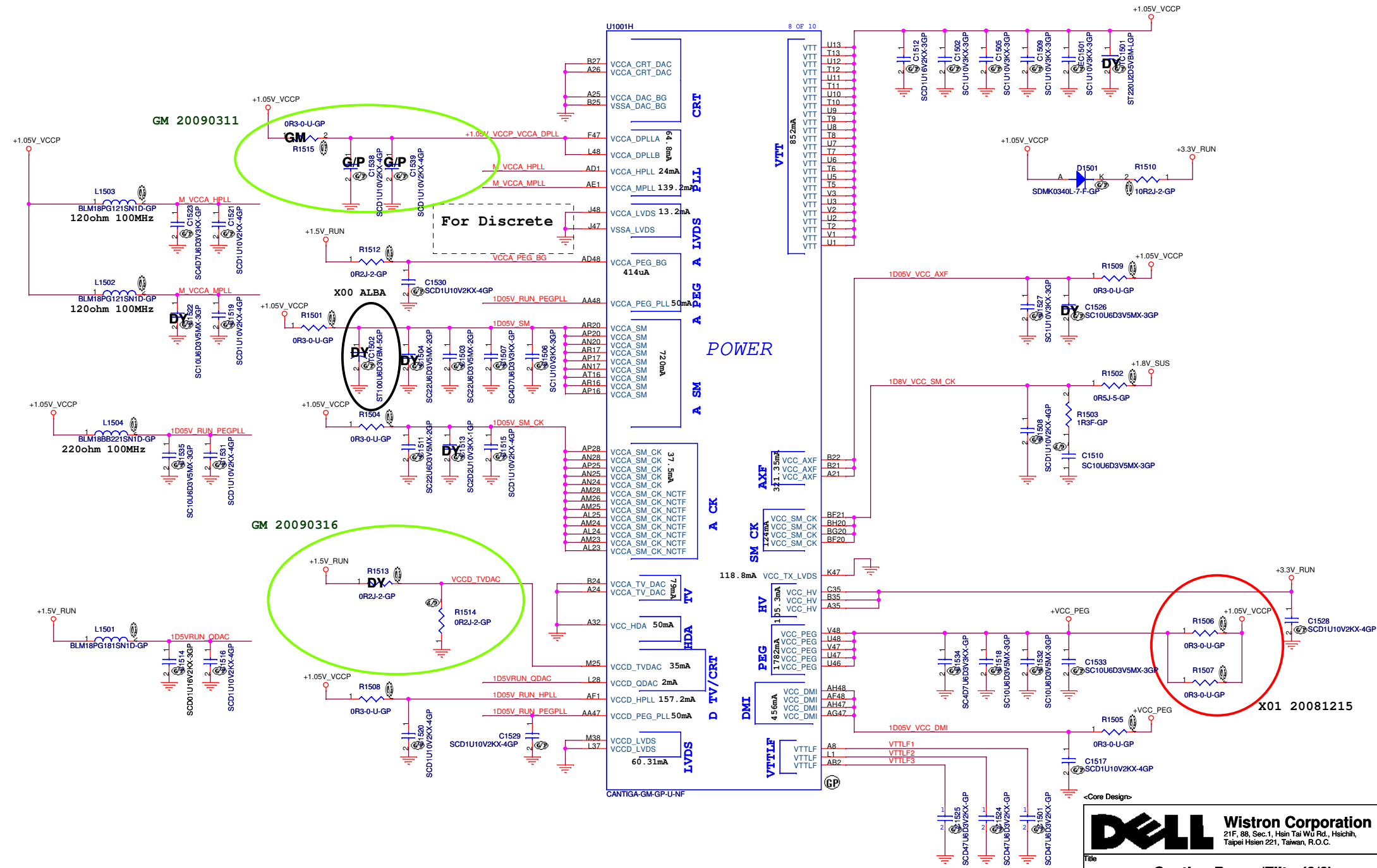


DELL Wistron Corporation
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 Taipei Hsien 221, Taiwan, R.O.C.

File: **Cantiga-Power(5/6)**

Size: Document Number
 Custom: **Alba Discrete** Rev: **SB**

Date: Monday, March 23, 2009 Sheet 14 of 59

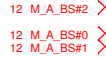
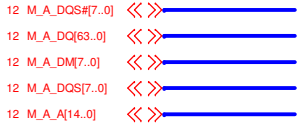


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Document Number: **Cantiga-Power/Filter(6/6)**
 Rev: **SB**

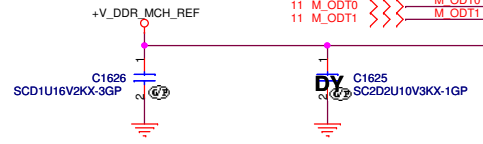
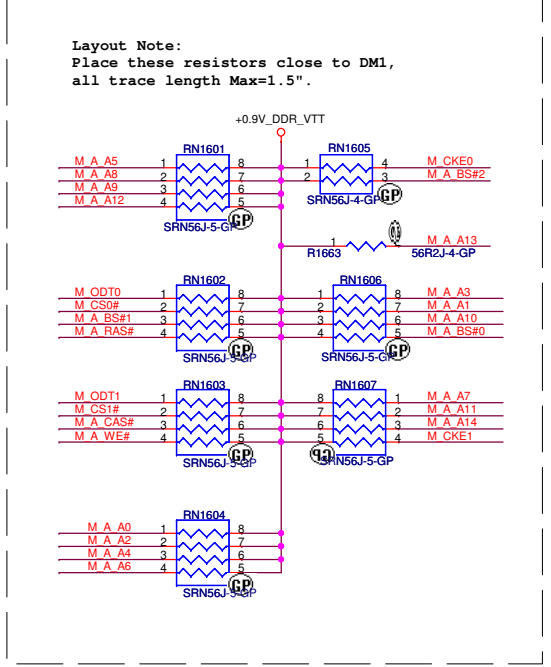
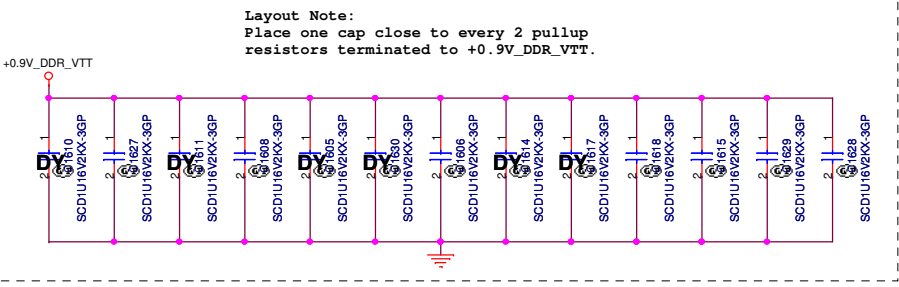
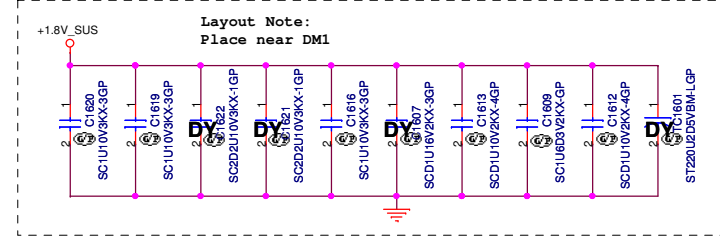
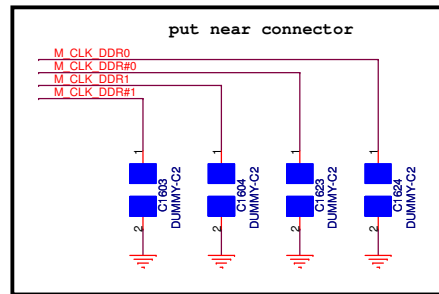
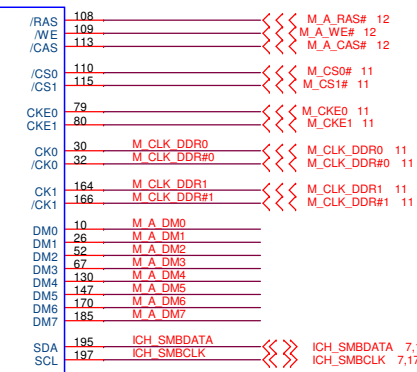
Date: Monday, March 23, 2009 Sheet 15 of 59

SSID = MEMORY



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| M A A2 | 100 | A1 |
| M A A3 | 99 | A2 |
| M A A4 | 98 | A3 |
| M A A5 | 97 | A4 |
| M A A6 | 94 | A5 |
| M A A7 | 92 | A6 |
| M A A8 | 93 | A7 |
| M A A9 | 91 | A8 |
| M A A10 | 105 | A9 |
| M A A11 | 89 | A10/AP |
| M A A12 | 89 | A11 |
| M A A13 | 116 | A12 |
| M A A14 | 86 | A13 |
| M A A15 | 84 | A14 |
| M A BS#2 | 85 | A15/BA2 |
| M A BS#0 | 107 | BA0 |
| M A BS#1 | 106 | BA1 |
| M A D00 | 5 | DO0 |
| M A D01 | 7 | DO1 |
| M A D02 | 17 | DO2 |
| M A D03 | 19 | DO3 |
| M A D04 | 4 | DO4 |
| M A D05 | 6 | DO5 |
| M A D06 | 14 | DO6 |
| M A D07 | 16 | DO7 |
| M A D08 | 23 | DO8 |
| M A D09 | 25 | DO9 |
| M A DQ10 | 35 | DO10 |
| M A DQ11 | 37 | DO11 |
| M A DQ12 | 20 | DO12 |
| M A DQ13 | 22 | DO13 |
| M A DQ14 | 36 | DO14 |
| M A DQ15 | 38 | DO15 |
| M A DQ16 | 43 | DO16 |
| M A DQ17 | 45 | DO17 |
| M A DQ18 | 57 | DO18 |
| M A DQ19 | 57 | DO19 |
| M A DQ20 | 46 | DO20 |
| M A DQ21 | 44 | DO21 |
| M A DQ22 | 56 | DO22 |
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| M A DQ25 | 63 | DO25 |
| M A DQ26 | 73 | DO26 |
| M A DQ27 | 75 | DO27 |
| M A DQ28 | 62 | DO28 |
| M A DQ29 | 64 | DO29 |
| M A DQ30 | 74 | DO30 |
| M A DQ31 | 76 | DO31 |
| M A DQ32 | 123 | DO32 |
| M A DQ33 | 125 | DO33 |
| M A DQ34 | 135 | DO34 |
| M A DQ35 | 137 | DO35 |
| M A DQ36 | 124 | DO36 |
| M A DQ37 | 126 | DO37 |
| M A DQ38 | 134 | DO38 |
| M A DQ39 | 136 | DO39 |
| M A DQ40 | 141 | DO40 |
| M A DQ41 | 143 | DO41 |
| M A DQ42 | 151 | DO42 |
| M A DQ43 | 153 | DO43 |
| M A DQ44 | 140 | DO44 |
| M A DQ45 | 142 | DO45 |
| M A DQ46 | 152 | DO46 |
| M A DQ47 | 154 | DO47 |
| M A DQ48 | 157 | DO48 |
| M A DQ49 | 159 | DO49 |
| M A DQ50 | 173 | DO50 |
| M A DQ51 | 175 | DO51 |
| M A DQ52 | 158 | DO52 |
| M A DQ53 | 160 | DO53 |
| M A DQ54 | 174 | DO54 |
| M A DQ55 | 176 | DO55 |
| M A DQ56 | 179 | DO56 |
| M A DQ57 | 181 | DO57 |
| M A DQ58 | 183 | DO58 |
| M A DQ59 | 191 | DO59 |
| M A DQ60 | 180 | DO60 |
| M A DQ61 | 182 | DO61 |
| M A DQ62 | 192 | DO62 |
| M A DQ63 | 194 | DO63 |
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| M A DOS#1 | 29 | /DOS1 |
| M A DOS#2 | 49 | /DOS2 |
| M A DOS#3 | 68 | /DOS3 |
| M A DOS#4 | 129 | /DOS4 |
| M A DOS#5 | 146 | /DOS5 |
| M A DOS#6 | 167 | /DOS6 |
| M A DOS#7 | 186 | /DOS7 |
| M A DOS0 | 13 | DOS0 |
| M A DOS1 | 31 | DOS1 |
| M A DOS2 | 51 | DOS2 |
| M A DOS3 | 70 | DOS3 |
| M A DOS4 | 131 | DOS4 |
| M A DOS5 | 148 | DOS5 |
| M A DOS6 | 169 | DOS6 |
| M A DOS7 | 188 | DOS7 |
| M ODT0 | 114 | ODT0 |
| M ODT1 | 119 | ODT1 |
| VREF | 1 | VREF |
| VSS | 2 | VSS |
| GND | 202 | GND |

Height 6.5mm



DDR2-200P-10-U1
62.10017.881

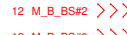
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **DDR2-SODIMM SLOT1**

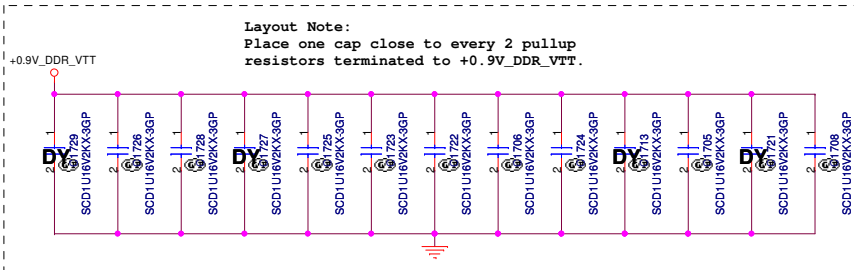
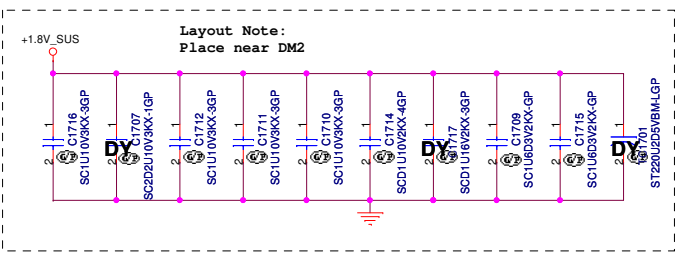
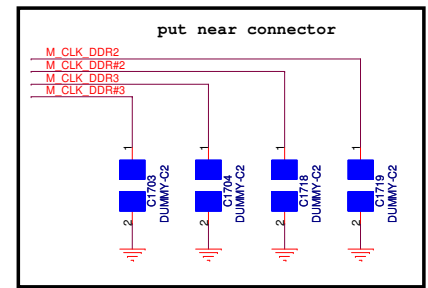
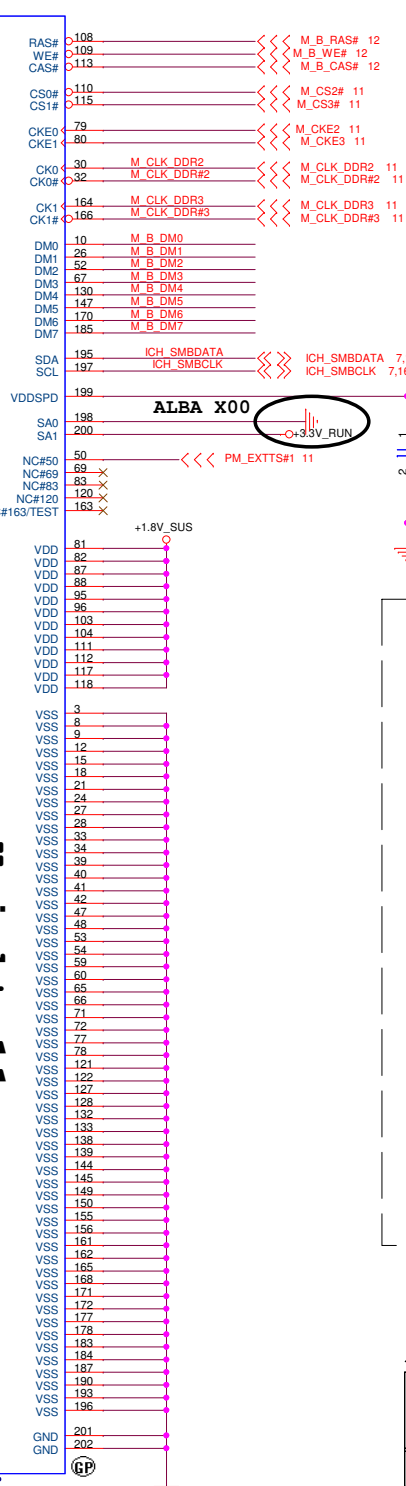
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| Size Custom | Document Number | Rev SB |
| Date: Monday, March 23, 2009 | Sheet 16 | of 59 |

SSID = MEMORY

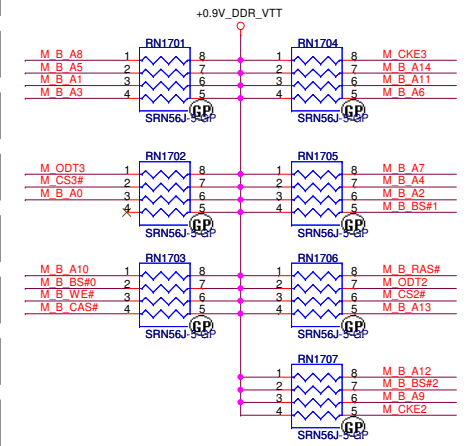


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| M B A6 | 94 | A6 |
| M B A7 | 92 | A7 |
| M B A8 | 93 | A8 |
| M B A9 | 91 | A9 |
| M B A10 | 105 | A10/AP |
| M B A11 | 90 | A11 |
| M B A12 | 89 | A12 |
| M B A13 | 116 | A13 |
| M B A14 | 88 | A14 |
| | 84 | A15 |
| | 85 | A16/BA2 |
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| M B BS#1 | 106 | BA1 |
| M B BS#2 | 107 | BA0 |
| M B BS#0 | 107 | BA0 |
| M B BS#1 | 106 | BA1 |
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| M B DQ1 | 7 | DQ1 |
| M B DQ2 | 17 | DQ2 |
| M B DQ3 | 19 | DQ3 |
| M B DQ4 | 4 | DQ4 |
| M B DQ5 | 6 | DQ5 |
| M B DQ6 | 14 | DQ6 |
| M B DQ7 | 16 | DQ7 |
| M B DQ8 | 23 | DQ8 |
| M B DQ9 | 25 | DQ9 |
| M B DQ10 | 35 | DQ10 |
| M B DQ11 | 37 | DQ11 |
| M B DQ12 | 20 | DQ12 |
| M B DQ13 | 22 | DQ13 |
| M B DQ14 | 36 | DQ14 |
| M B DQ15 | 38 | DQ15 |
| M B DQ16 | 43 | DQ16 |
| M B DQ17 | 45 | DQ17 |
| M B DQ18 | 55 | DQ18 |
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| M B DQ20 | 44 | DQ20 |
| M B DQ21 | 46 | DQ21 |
| M B DQ22 | 58 | DQ22 |
| M B DQ23 | 58 | DQ23 |
| M B DQ24 | 61 | DQ24 |
| M B DQ25 | 63 | DQ25 |
| M B DQ26 | 73 | DQ26 |
| M B DQ27 | 75 | DQ27 |
| M B DQ28 | 62 | DQ28 |
| M B DQ29 | 64 | DQ29 |
| M B DQ30 | 74 | DQ30 |
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| M B DQ32 | 123 | DQ32 |
| M B DQ33 | 125 | DQ33 |
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| M B DQ35 | 137 | DQ35 |
| M B DQ36 | 124 | DQ36 |
| M B DQ37 | 126 | DQ37 |
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| M B DQ39 | 136 | DQ39 |
| M B DQ40 | 141 | DQ40 |
| M B DQ41 | 143 | DQ41 |
| M B DQ42 | 151 | DQ42 |
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| M B DQ45 | 142 | DQ45 |
| M B DQ46 | 152 | DQ46 |
| M B DQ47 | 154 | DQ47 |
| M B DQ48 | 157 | DQ48 |
| M B DQ49 | 159 | DQ49 |
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| M B DQ51 | 175 | DQ51 |
| M B DQ52 | 158 | DQ52 |
| M B DQ53 | 160 | DQ53 |
| M B DQ54 | 174 | DQ54 |
| M B DQ55 | 176 | DQ55 |
| M B DQ56 | 179 | DQ56 |
| M B DQ57 | 181 | DQ57 |
| M B DQ58 | 189 | DQ58 |
| M B DQ59 | 191 | DQ59 |
| M B DQ60 | 180 | DQ60 |
| M B DQ61 | 182 | DQ61 |
| M B DQ62 | 192 | DQ62 |
| M B DQ63 | 194 | DQ63 |
| M B DQS#0 | 110 | DQS0# |
| M B DQS#1 | 290 | DQS1# |
| M B DQS#2 | 49 | DQS2# |
| M B DQS#3 | 68 | DQS3# |
| M B DQS#4 | 129 | DQS4# |
| M B DQS#5 | 146 | DQS5# |
| M B DQS#6 | 167 | DQS6# |
| M B DQS#7 | 186 | DQS7# |
| M B DQS0 | 13 | DQS0 |
| M B DQS1 | 31 | DQS1 |
| M B DQS2 | 51 | DQS2 |
| M B DQS3 | 70 | DQS3 |
| M B DQS4 | 131 | DQS4 |
| M B DQS5 | 148 | DQS5 |
| M B DQS6 | 169 | DQS6 |
| M B DQS7 | 188 | DQS7 |
| M ODT2 | 114 | ODT0 |
| M ODT3 | 119 | ODT1 |
| VREF | 2 | VREF |
| VSS | 1 | VSS |
| NP1 | NP1 | NP1 |
| NP2 | NP2 | NP2 |

DM2



Layout Note:
Place these resistors close to DM2,
all trace length Max=1.5".



Height 1mm

<Core Design>

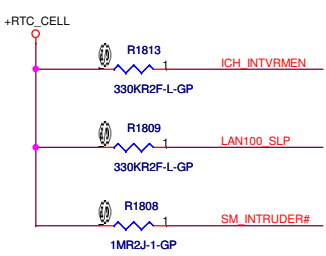
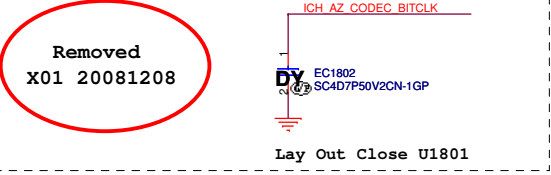
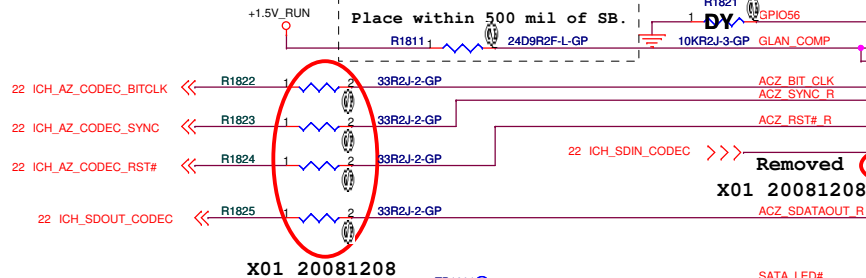
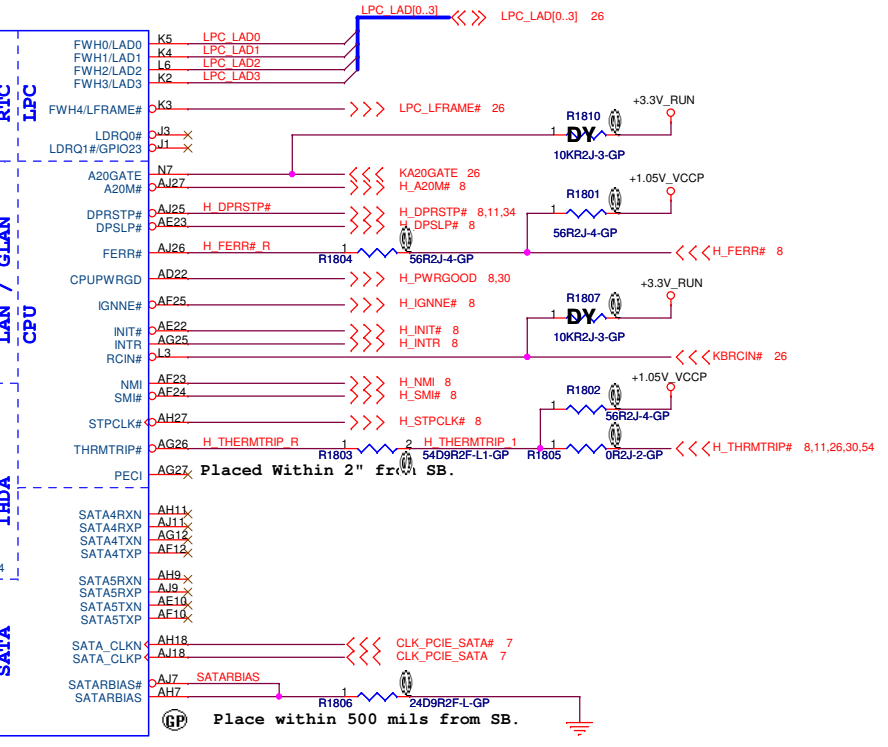
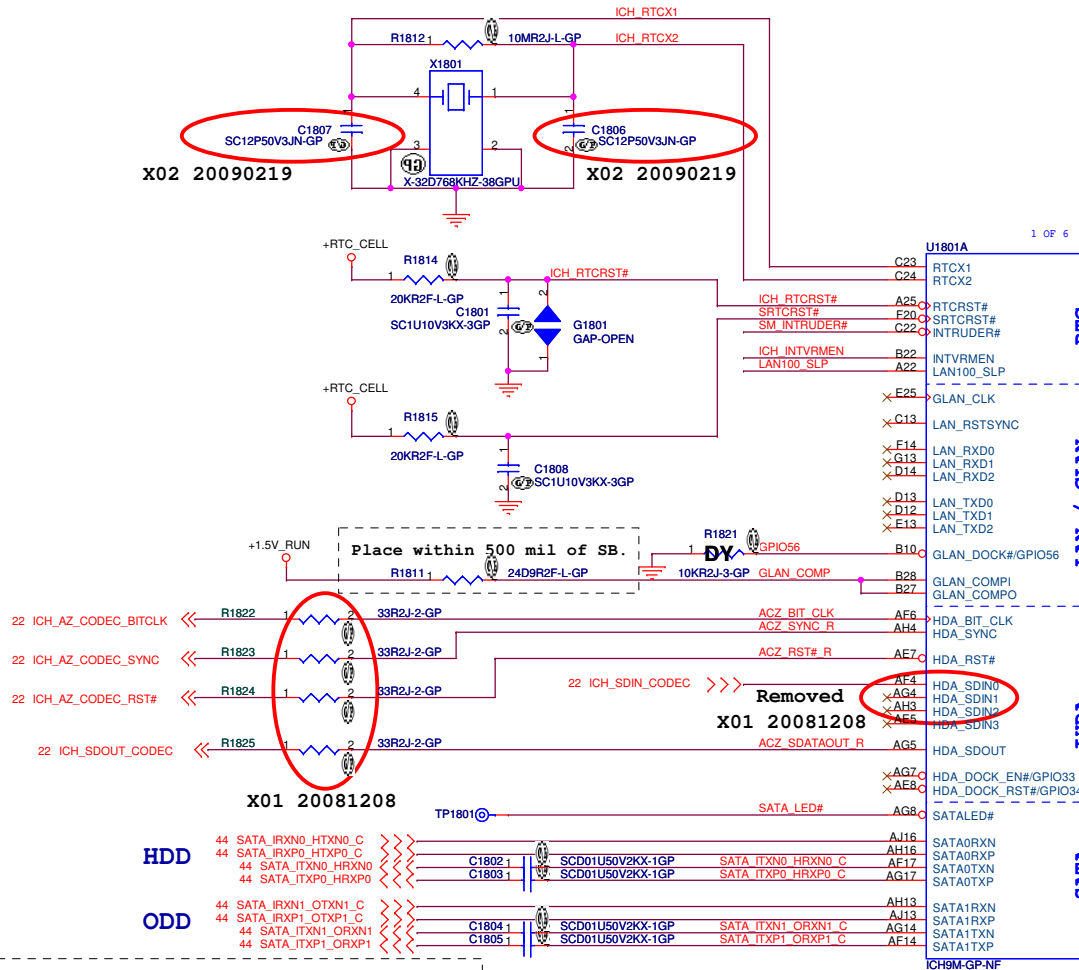
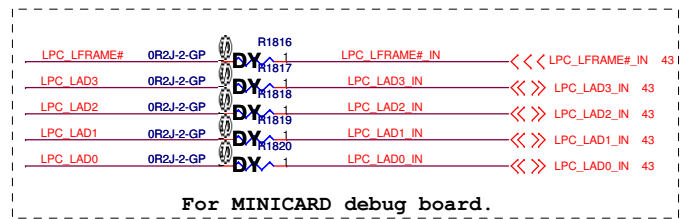
Wistron Corporation
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Title: **DDR2-SODIMM SLOT2**

Size: Custom Document Number: **Alba Discrete** Rev: **SB**

Date: Monday, March 23, 2009 Sheet 17 of 59

SSID = ICH



| | | |
|--|-------------|-------------|
| integrated VccSus1_05, VccSus1_5, VccCL1_5 | | |
| INTVRMEN | High=Enable | Low=Disable |
| integrated VccLan1_05VccCL1_05 | | |
| LAN100_SLP | High=Enable | Low=Disable |

<Core Design>

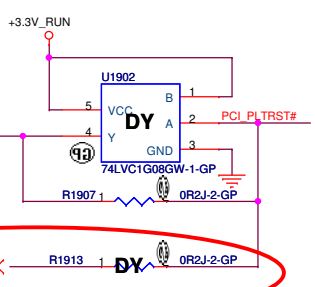
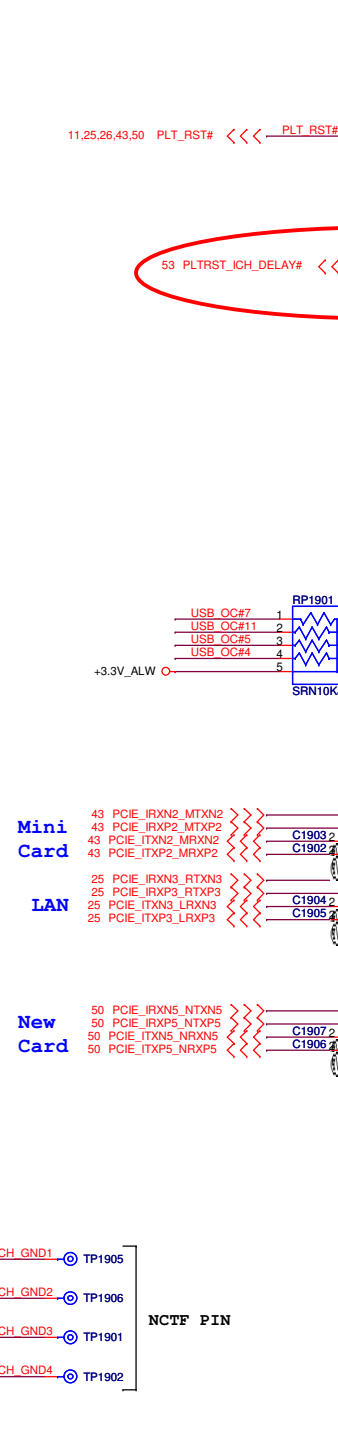
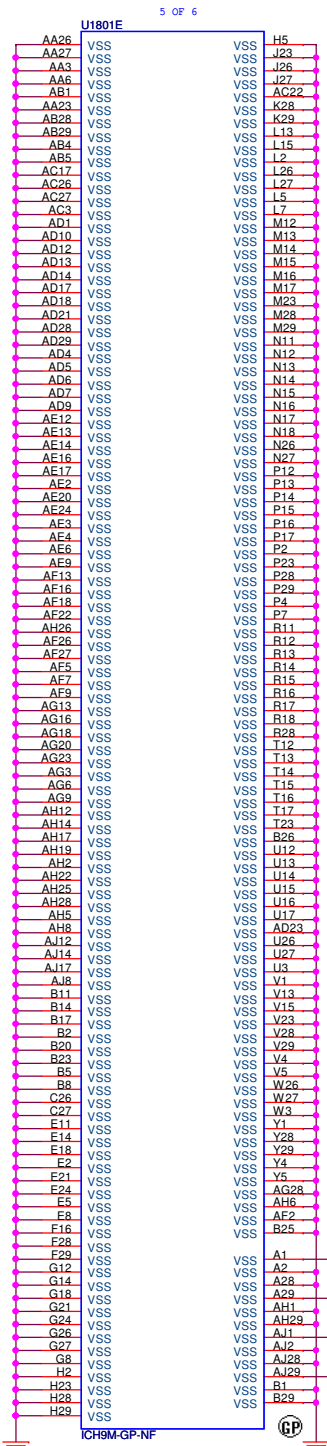
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **ICH9-LAN/HDA/SATA/LPC(1/4)**

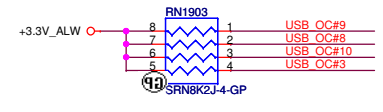
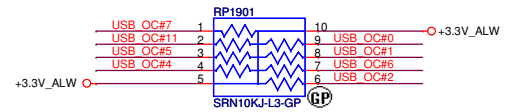
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|--------|----------------------|-----------|
| Size | Document Number | Rev |
| Custom | Alba Discrete | SB |

Date: Monday, March 23, 2009 Sheet 18 of 59

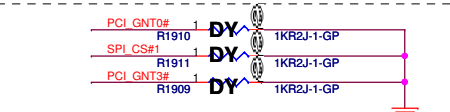
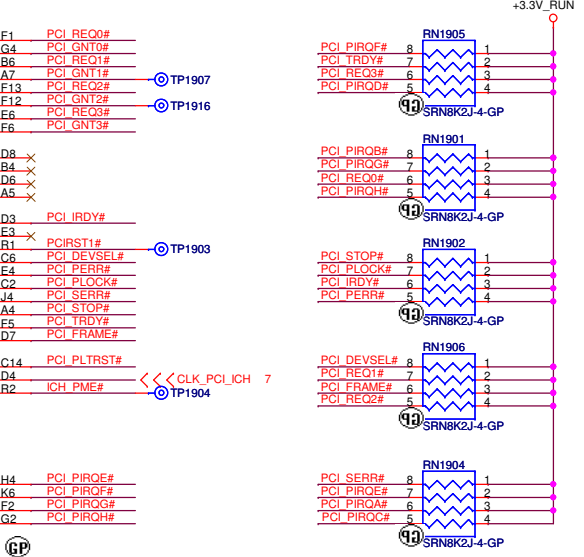
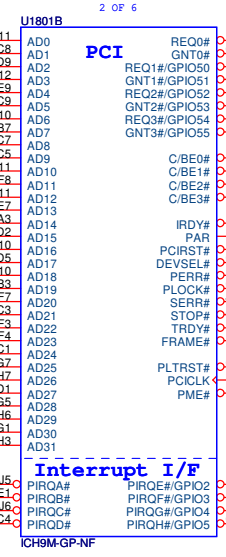
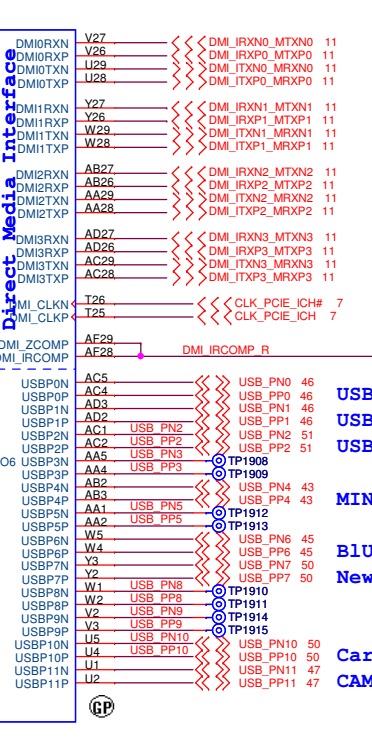
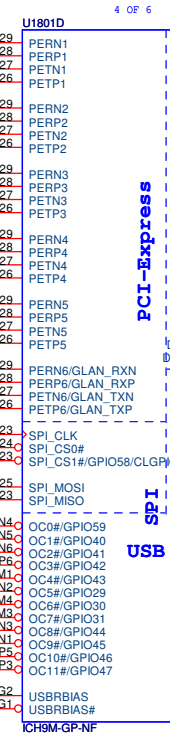
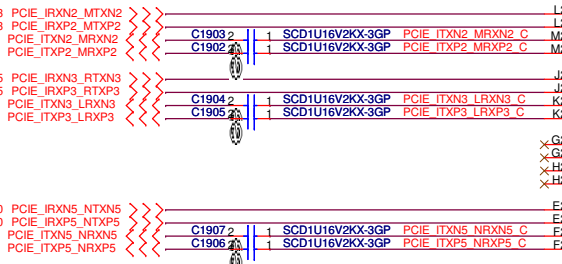
SSID = ICH



X01 20081208



Mini Card
LAN
New Card



| BOOT BIOS Strap | | |
|-----------------|----------|--------------------|
| PCI_GNT#0 | SPI_CS#1 | BOOT BIOS Location |
| 0 | 1 | SPI |
| 1 | 0 | PCI |
| 1 | 1 | LPC (Default) |

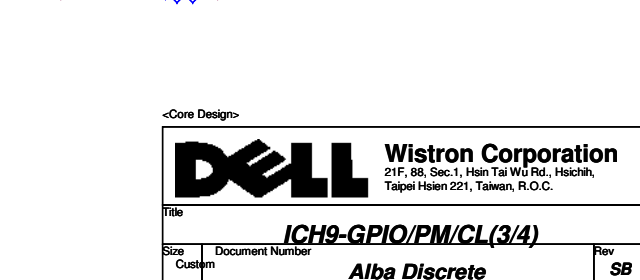
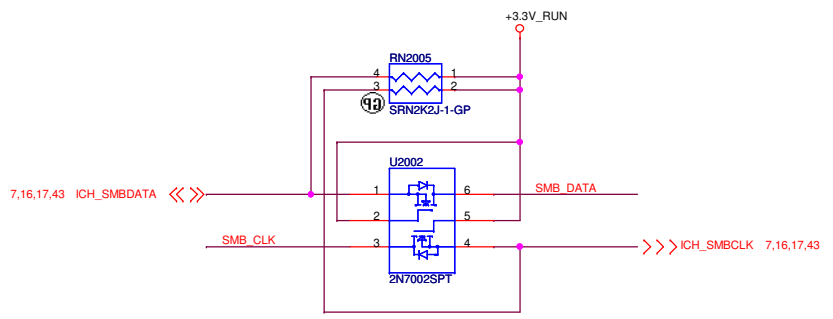
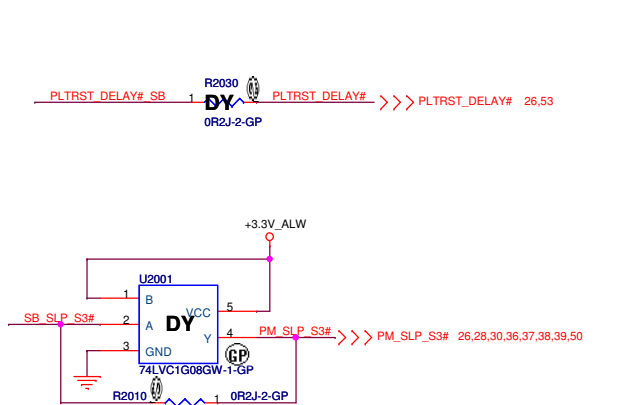
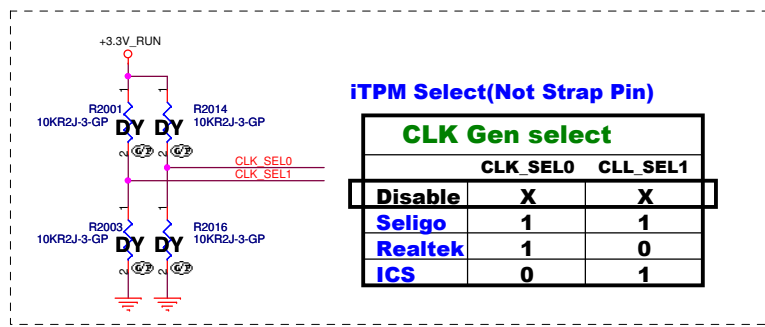
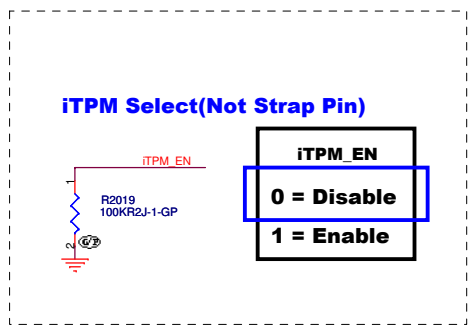
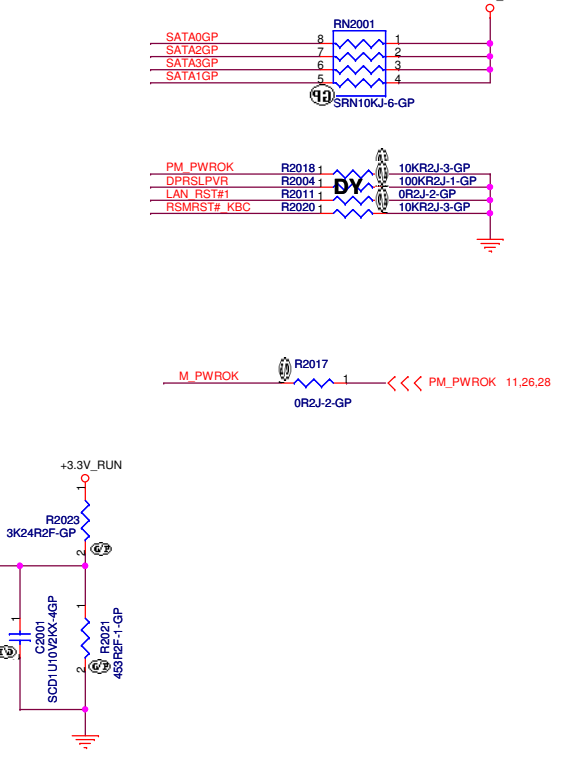
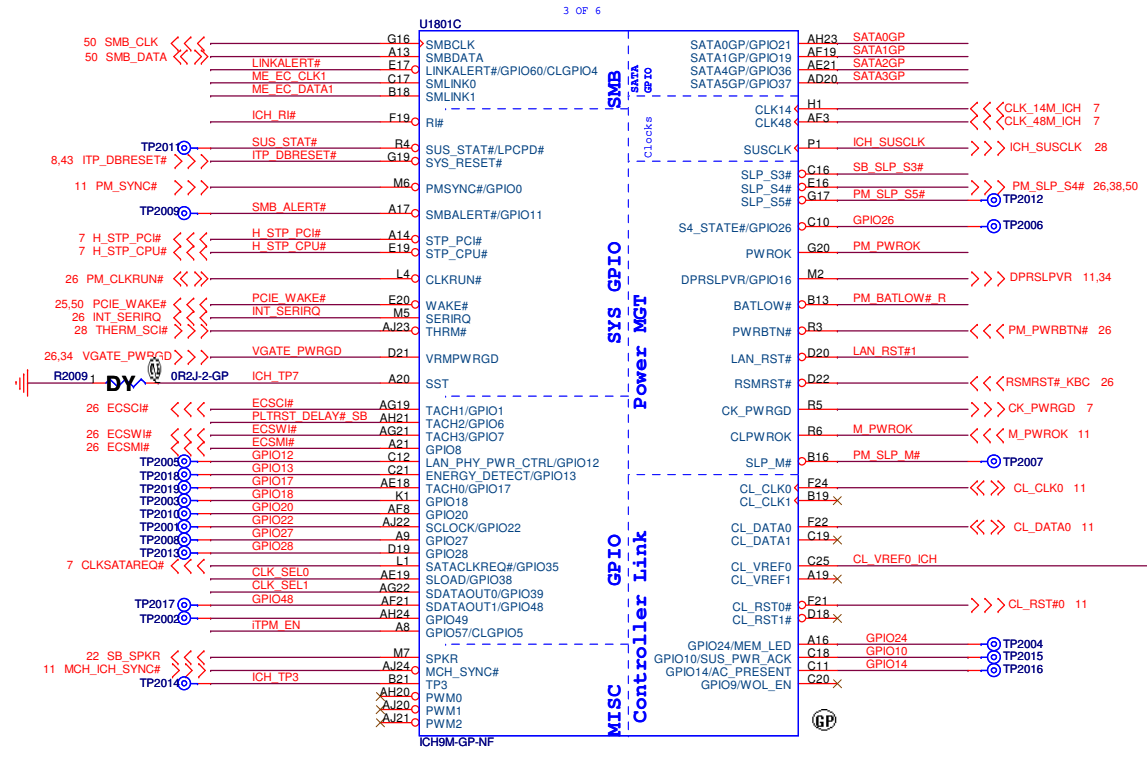
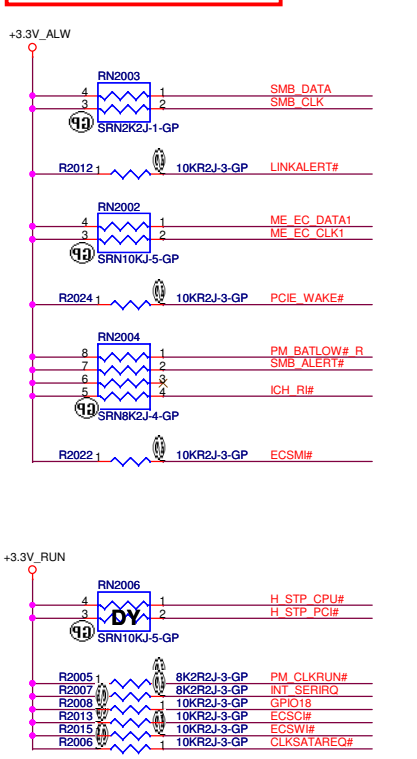
A16 swap override strap
low = A16 swap override enable
high = default

| USB Pair | Device |
|----------|-------------|
| 0 | USB1 |
| 1 | USB2 |
| 2 | USB3 |
| 3 | RESERVED |
| 4 | MINI CARD |
| 5 | RESERVED |
| 6 | BLUETOOTH |
| 7 | NEW CARD |
| 8 | RESERVED |
| 9 | RESERVED |
| 10 | Card Reader |
| 11 | CAMERA |

<Core Design>



SSID = ICH



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 Taipei Hsien 221, Taiwan, R.O.C.

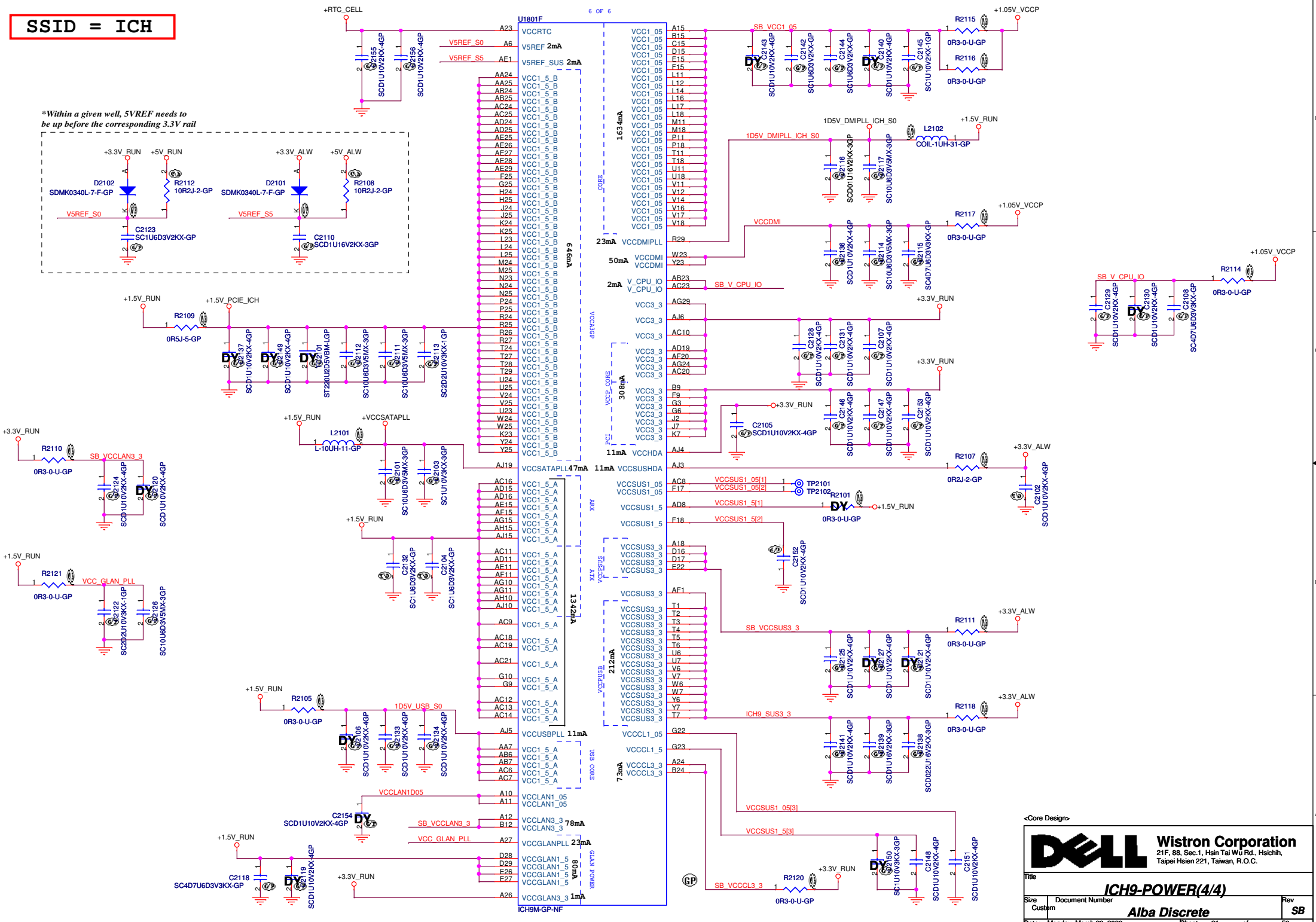
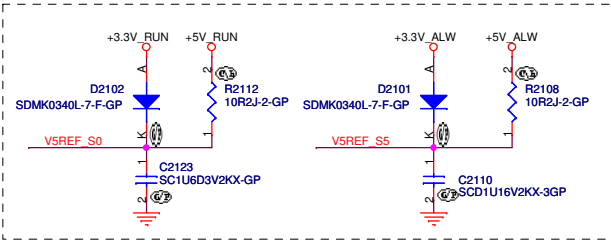
Title: **ICH9-GPIO/PM/CL(3/4)**

Size: Custom Document Number: **Alba Discrete** Rev: **SB**

Date: Monday, March 23, 2009 Sheet 20 of 59

SSID = ICH

*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail



<Core Design>

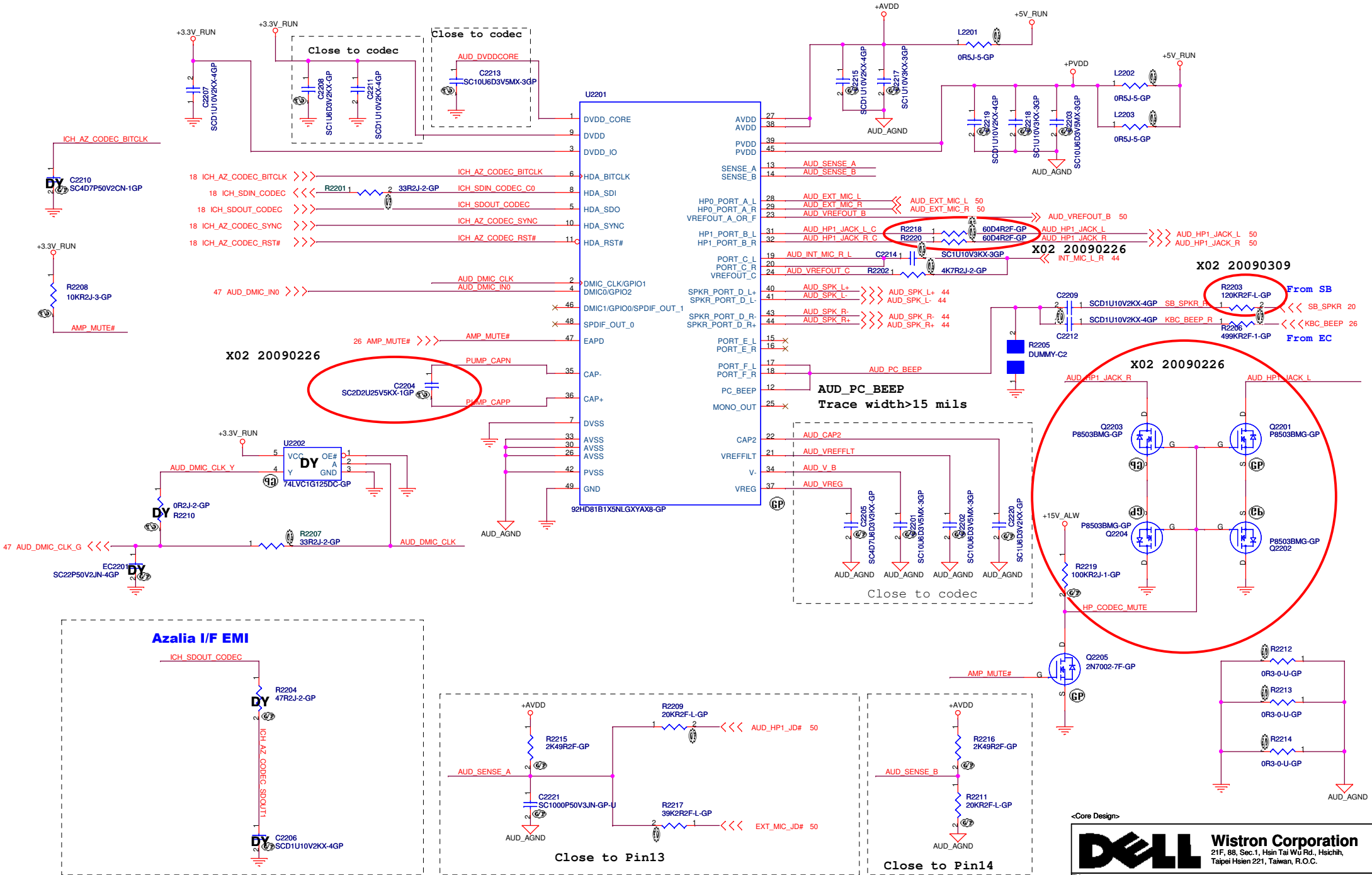
Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **ICH9-POWER(4/4)**

| | | |
|--------|----------------------|-----------|
| Size | Document Number | Rev |
| Custom | Alba Discrete | SB |

Date: Monday, March 23, 2009 Sheet 21 of 59

SSID = AUDIO



<Core Design>

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Title: **AUDIO CODEC 92HD81**

Size: Custom Document Number: **Alba Discrete** Rev: **SB**

Date: Monday, March 23, 2009 Sheet 22 of 59

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<Core Design>

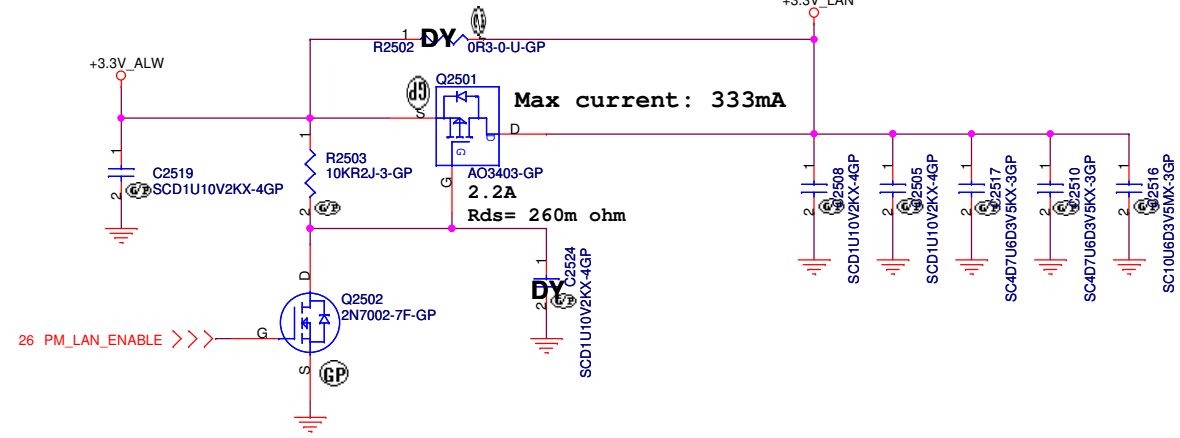
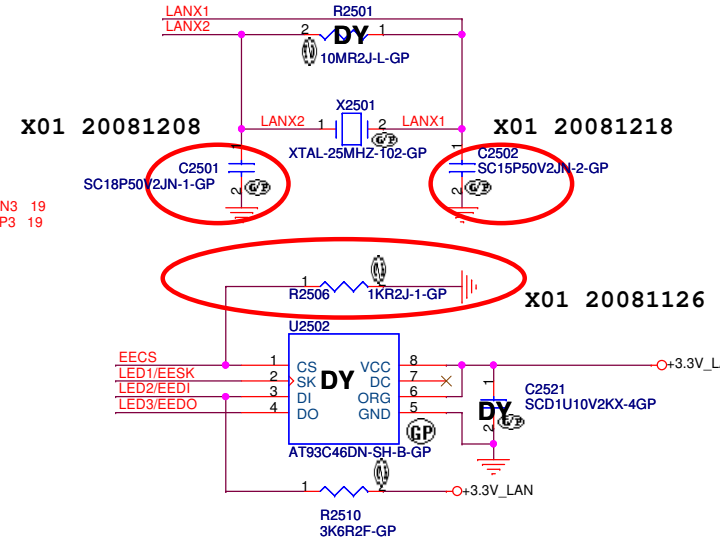
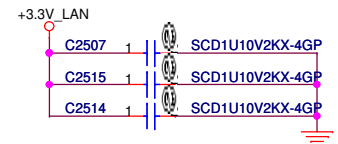
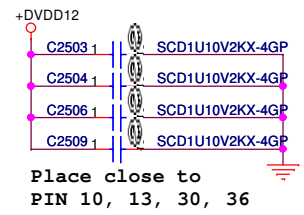
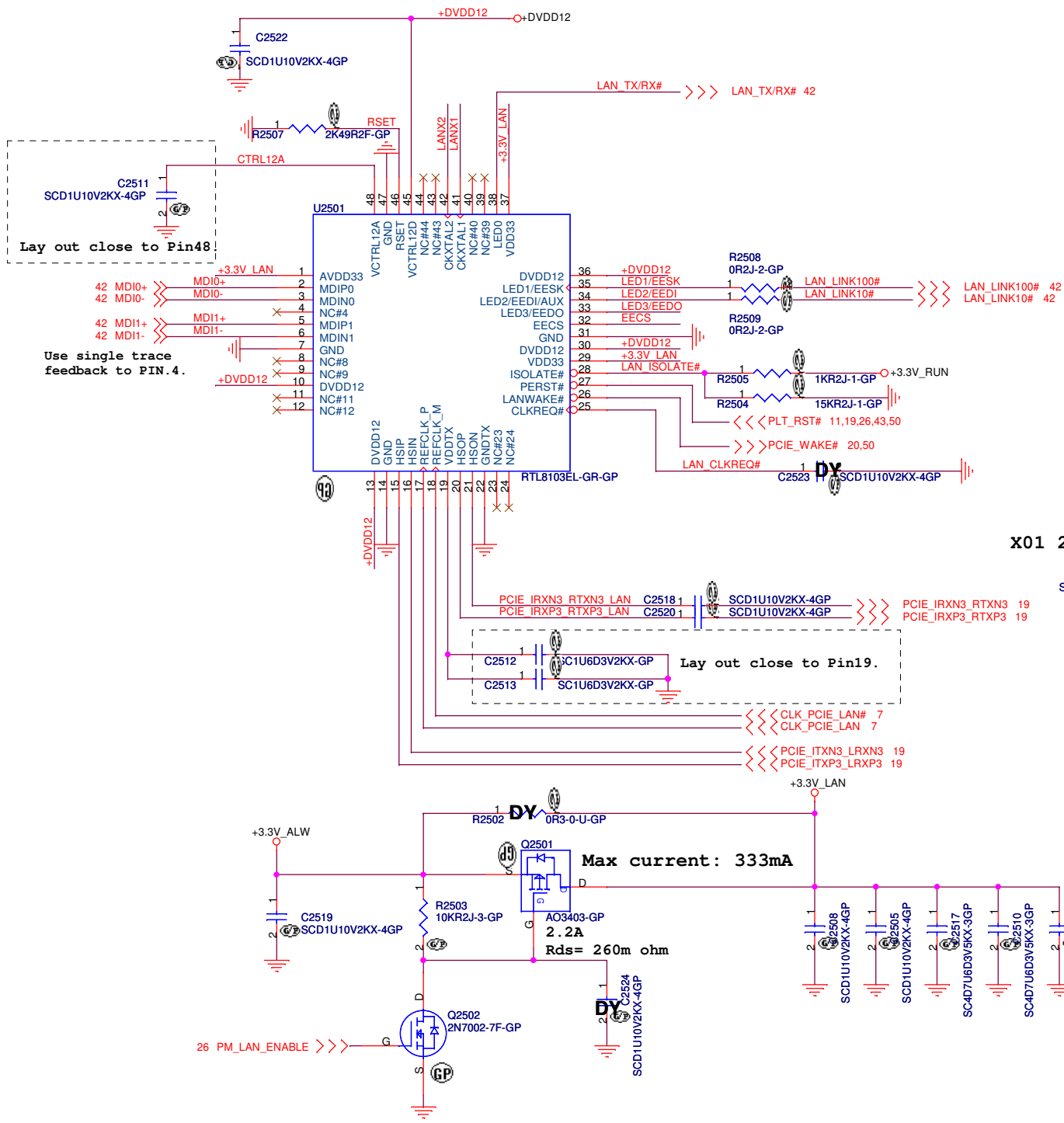
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|  | | Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | |
| Title | | | |
| (Reserve) | | | |
| Size | Document Number | Rev | |
| Custom | Alba Discrete | SB | |
| Date: Monday, March 23, 2009 | | Sheet 23 | of 59 |

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<Core Design>

| | | | |
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|  | | Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | |
| Title | | | |
| (Reserve) | | | |
| Size | Document Number | Rev | |
| Custom | Alba Discrete | SB | |
| Date: Monday, March 23, 2009 | | Sheet 24 | of 59 |

SSID = LOM

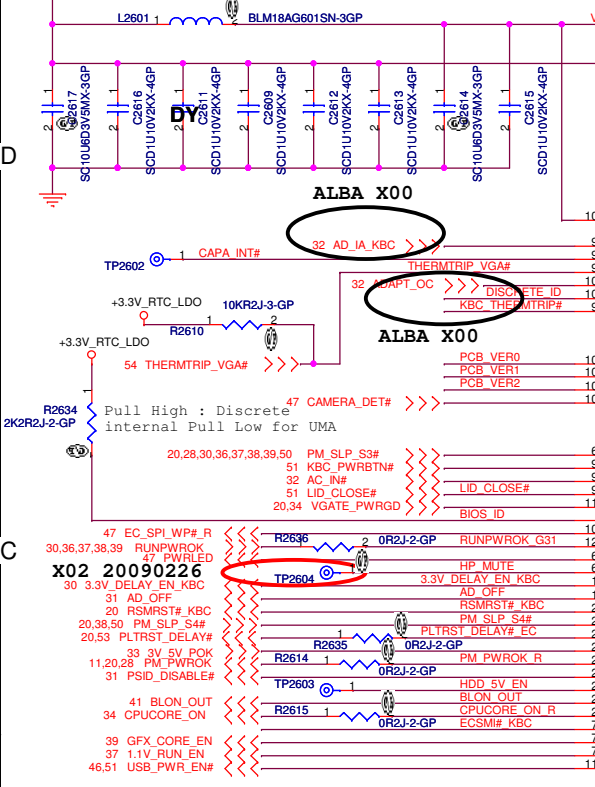


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Wistron Corporation
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| | | | |
|-------|------------------------|---------------|-------|
| Title | LAN Realtek-RTL8103EL | | Rev |
| Size | Document Number | Alba Discrete | SB |
| Date | Monday, March 23, 2009 | Sheet 25 | of 59 |

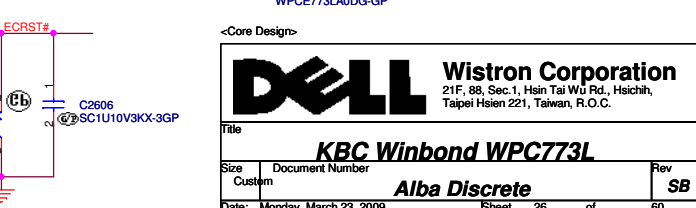
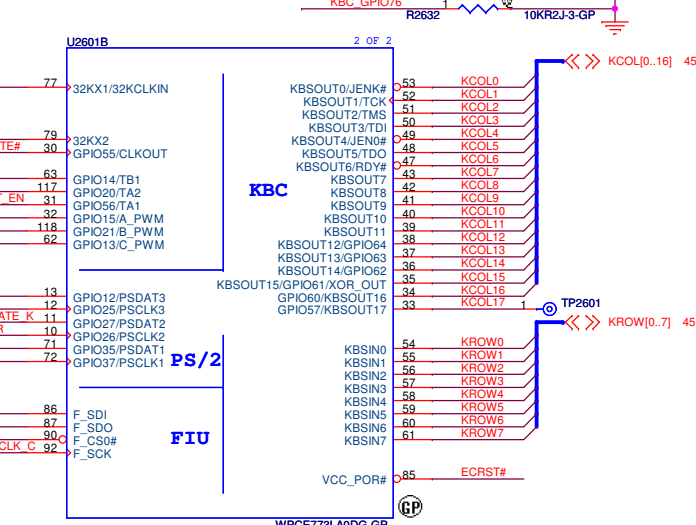
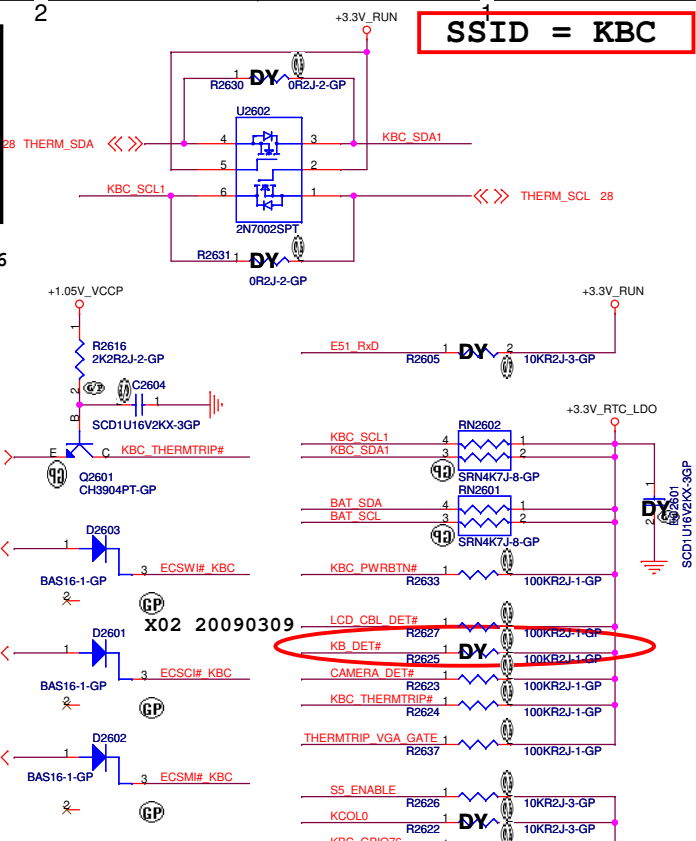
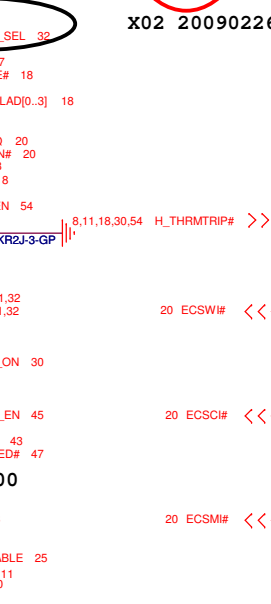
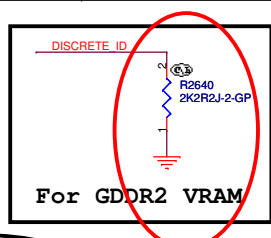
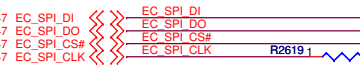
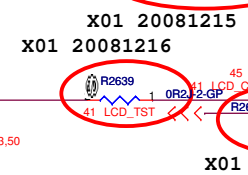
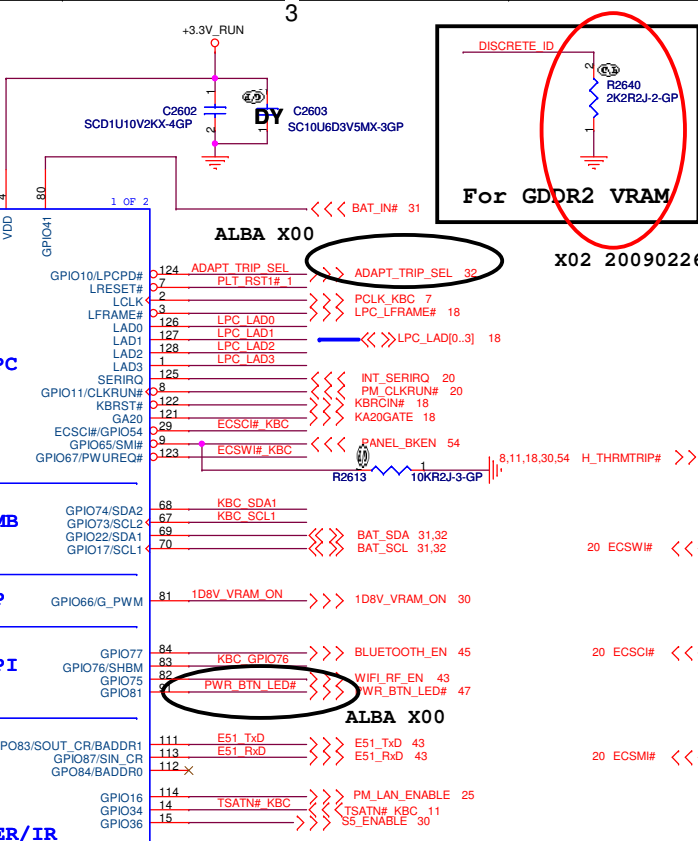
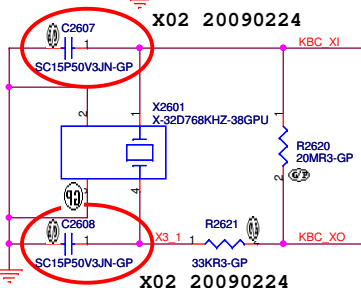
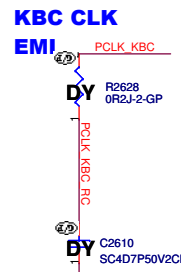
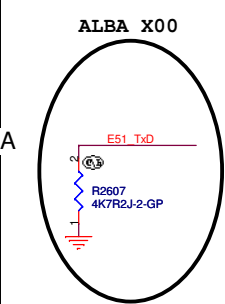
+3.3V_RTC_LDO Put 0.1uf close to VCC-GND pin pair.



X02 20090226

MB VERSION ID

| MB VERSION ID | VER2 | VER1 | VER0 |
|---------------|------|------|------|
| SA | 0 | 0 | 0 |
| SB | 0 | 0 | 1 |
| SC | 0 | 1 | 0 |
| -1 | 0 | 1 | 1 |



SSID = KBC

Wistron Corporation
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KBC Winbond WPC773L

Alba Discrete

Rev SB

Date: Monday, March 23, 2009 Sheet 26 of 60

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<Core Design>

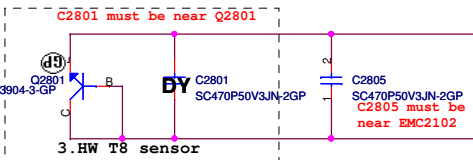
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|  | | Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | |
| Title | | | |
| (Reserve) | | | |
| Size | Document Number | Rev | |
| Custom | Alba Discrete | SB | |
| Date: Monday, March 23, 2009 | | Sheet 27 | of 59 |

SSID = Thermal

X01 20081215

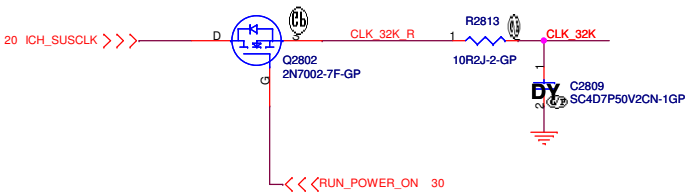
H_THERMDA, H_THERMDC routing together,
Trace width / Spacing = 10 / 10 mil

GPU Sensor
Layout notice :
Both VGA_THERMDA and THERMDC routing
10 mil trace width and 10 mil spacing.

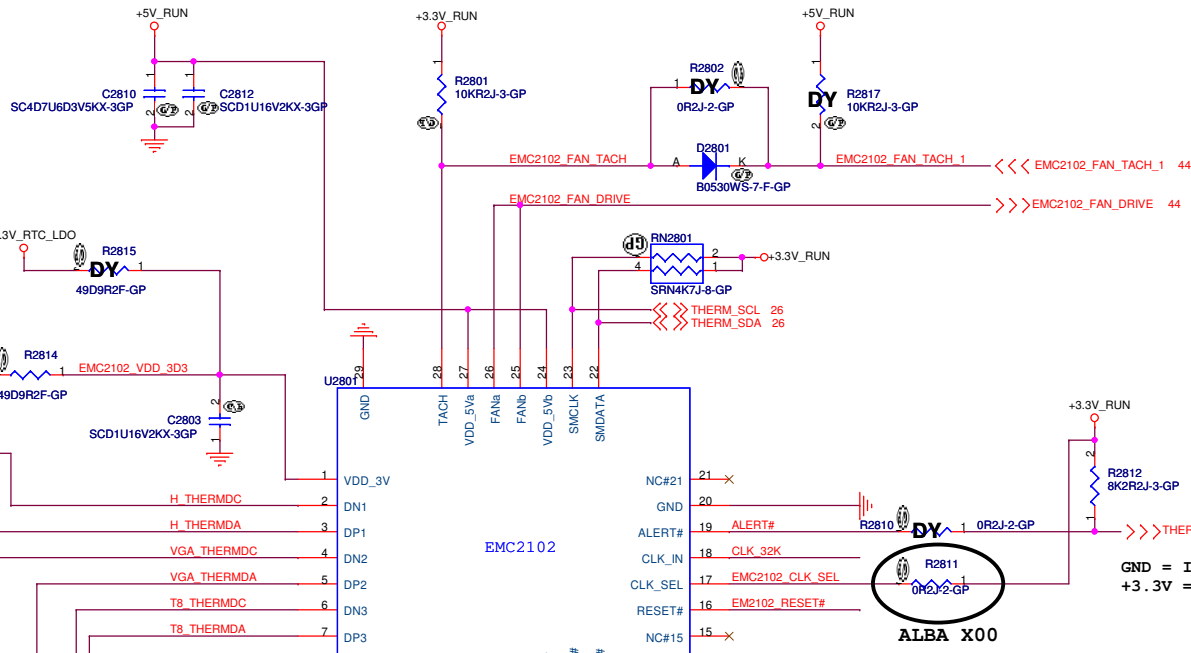
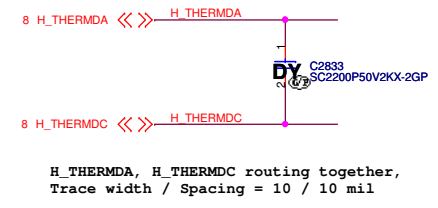


Layout notice :
Both DN3 and DP3 routing 10 mil
trace width and 10 mil spacing.

32K suspend clock output



Layout close to SKT2 (CPU socket)

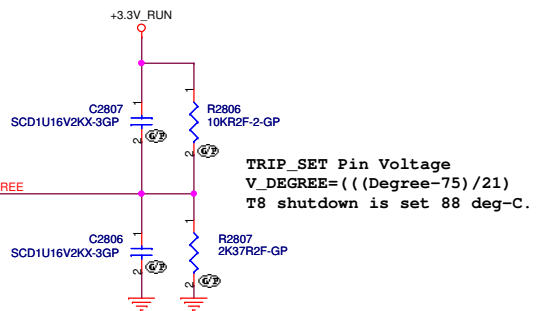
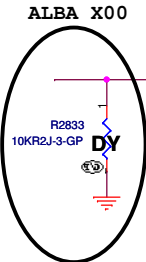


GND = Channel 1
OPEN = Channel 3
+3.3V = Disabled

GND = Fan is OFF
OPEN = Fan is at 60% full-scale
+3.3V = Fan is at 75% full-scale

GND = Internal Oscillator Selected
+3.3V = External 32.768kHz Clock Selected

TRIP_SET Pin Voltage
 $V_DEGREE = ((Degree - 75) / 21)$
T8 shutdown is set 88 deg-C.



<Core Design>

| | | | |
|---|------------------------|--|----------|
| DELL | | Wistron Corporation | |
| | | 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | |
| Title Thermal/Fan Controller EMC2102 | | | |
| Size | Document Number | Rev | |
| Custom | Alba Discrete | SB | |
| Date: | Monday, March 23, 2009 | Sheet | 28 of 59 |

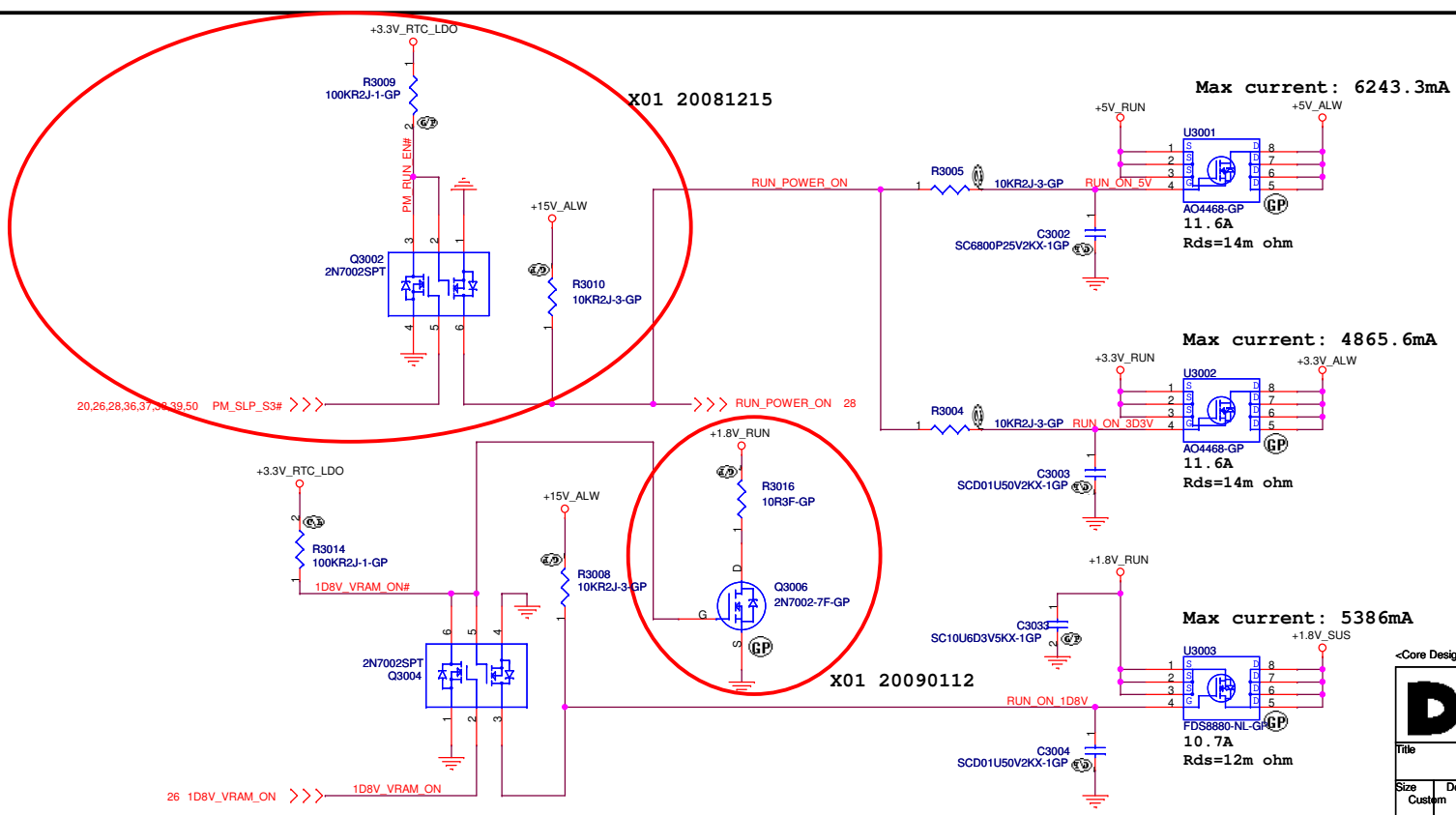
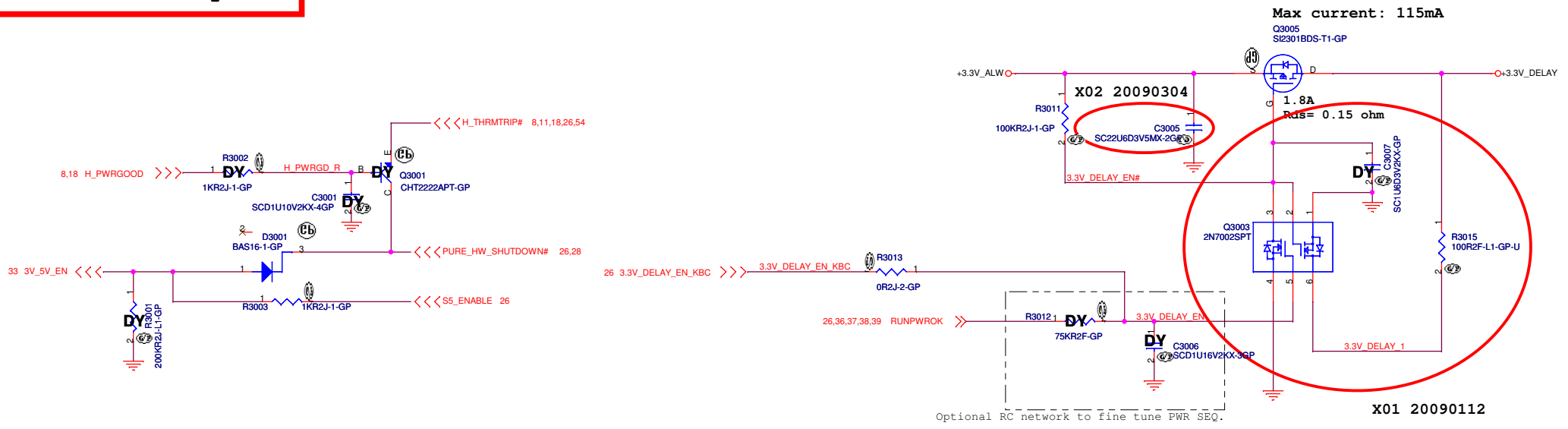
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| | |
|---|---|
|  | Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. |
|---|---|

| | | |
|------------------|------------------------|----------------|
| Title | | |
| (Reserve) | | |
| Size | Document Number | Rev |
| Custom | Alba Discrete | SB |
| Date: | Monday, March 23, 2009 | Sheet 29 of 59 |

SSID = Reset.Suspend



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

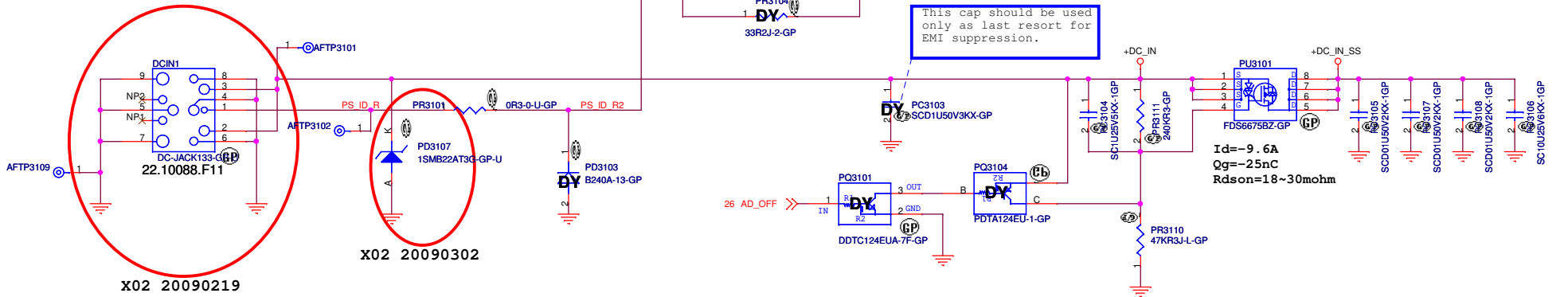
Title: **Power Plane Enable**

Size: Custom Document Number: **Alba Discrete** Rev: **SB**

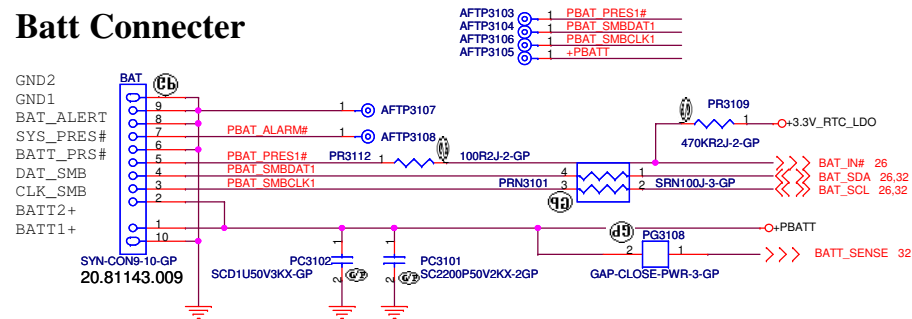
Date: Monday, March 23, 2009 Sheet 30 of 59

SSID = PWR.Support

DCin CONN



Batt Connector



<Core Design>

| | | | |
|------------------------------|-----------------|---|-----------|
| | | Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | |
| | | Title DC IN/BATT CONN/USB CONN | |
| Size | Document Number | Rev | |
| Custom | | Alba Discrete | SB |
| Date: Monday, March 23, 2009 | | Sheet 31 | of 59 |

SSID = Charger

Adaptor In Soft-Start Circuit

$I_d = -9.6A$
 $Q_g = -25nC$
 $R_{dson} = 18 \sim 30m\Omega$
Layout Trace 250mil

Layout Trace 300mil

$I_d = -9.6A$
 $Q_g = -25nC$
 $R_{dson} = 18 \sim 30m\Omega$
Layout Trace 300mil

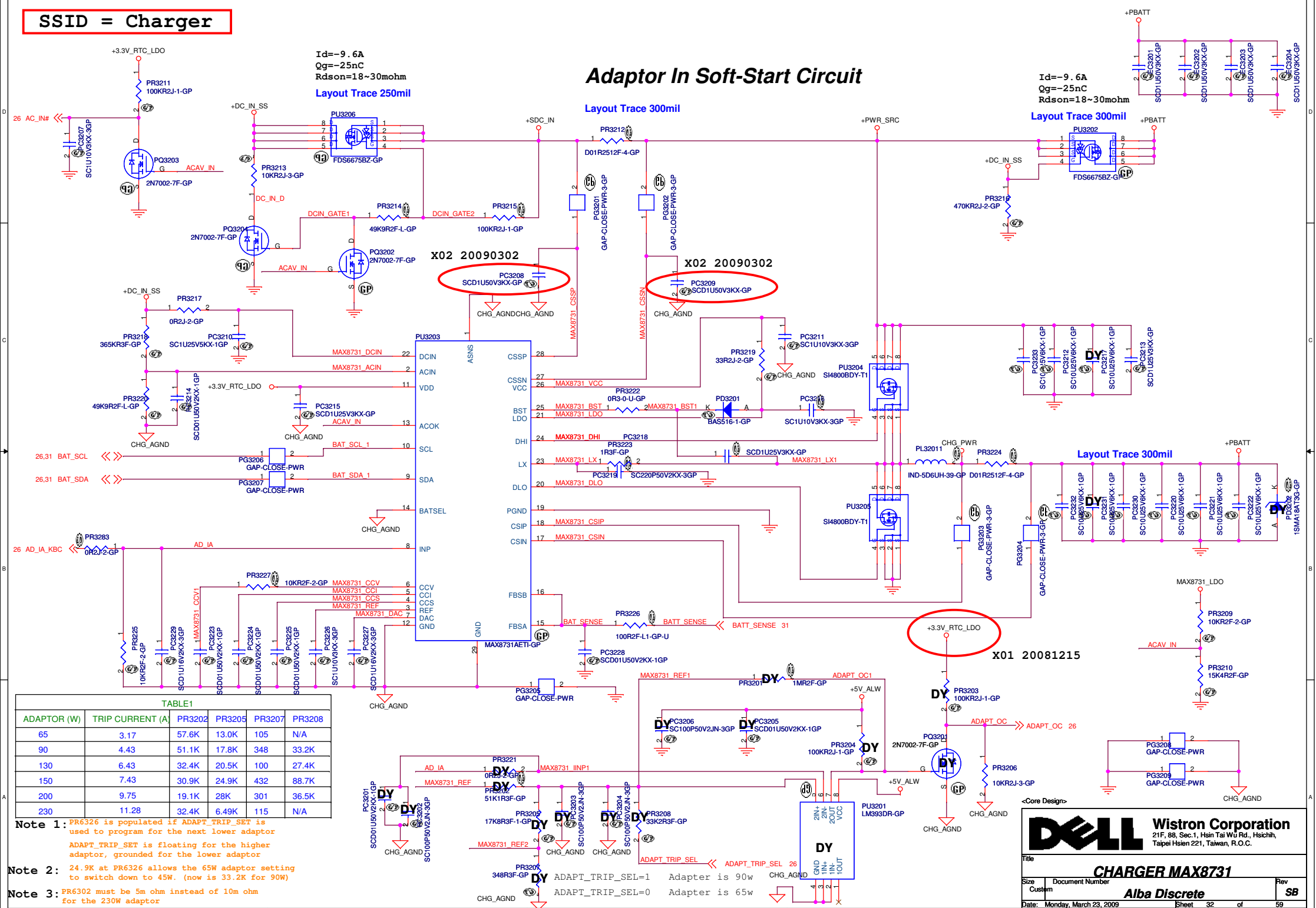


TABLE1

| ADAPTOR (W) | TRIP CURRENT (A) | PR3202 | PR3205 | PR3207 | PR3208 |
|-------------|------------------|--------|--------|--------|--------|
| 65 | 3.17 | 57.6K | 13.0K | 105 | N/A |
| 90 | 4.43 | 51.1K | 17.8K | 348 | 33.2K |
| 130 | 6.43 | 32.4K | 20.5K | 100 | 27.4K |
| 150 | 7.43 | 30.9K | 24.9K | 432 | 88.7K |
| 200 | 9.75 | 19.1K | 28K | 301 | 36.5K |
| 230 | 11.28 | 32.4K | 6.49K | 115 | N/A |

Note 1: PR6326 is populated if ADAPT_TRIP_SET is used to program for the next lower adaptor
 ADAPT_TRIP_SET is floating for the higher adaptor, grounded for the lower adaptor

Note 2: 24.9K at PR6326 allows the 65W adaptor setting to switch down to 45W. (now is 33.2K for 90W)

Note 3: PR6302 must be 5m ohm instead of 10m ohm for the 230W adaptor

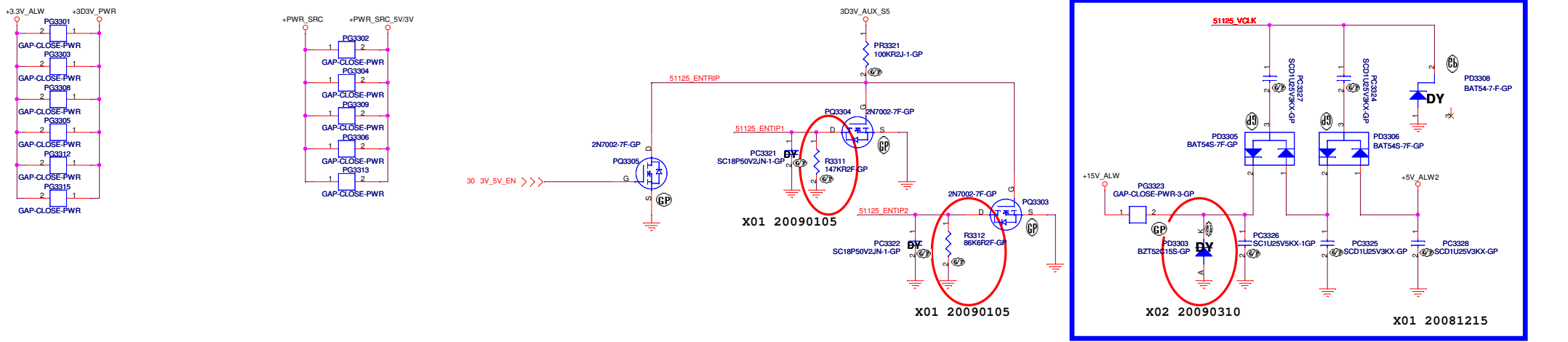
Core Design

DELL Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **CHARGER MAX8731**

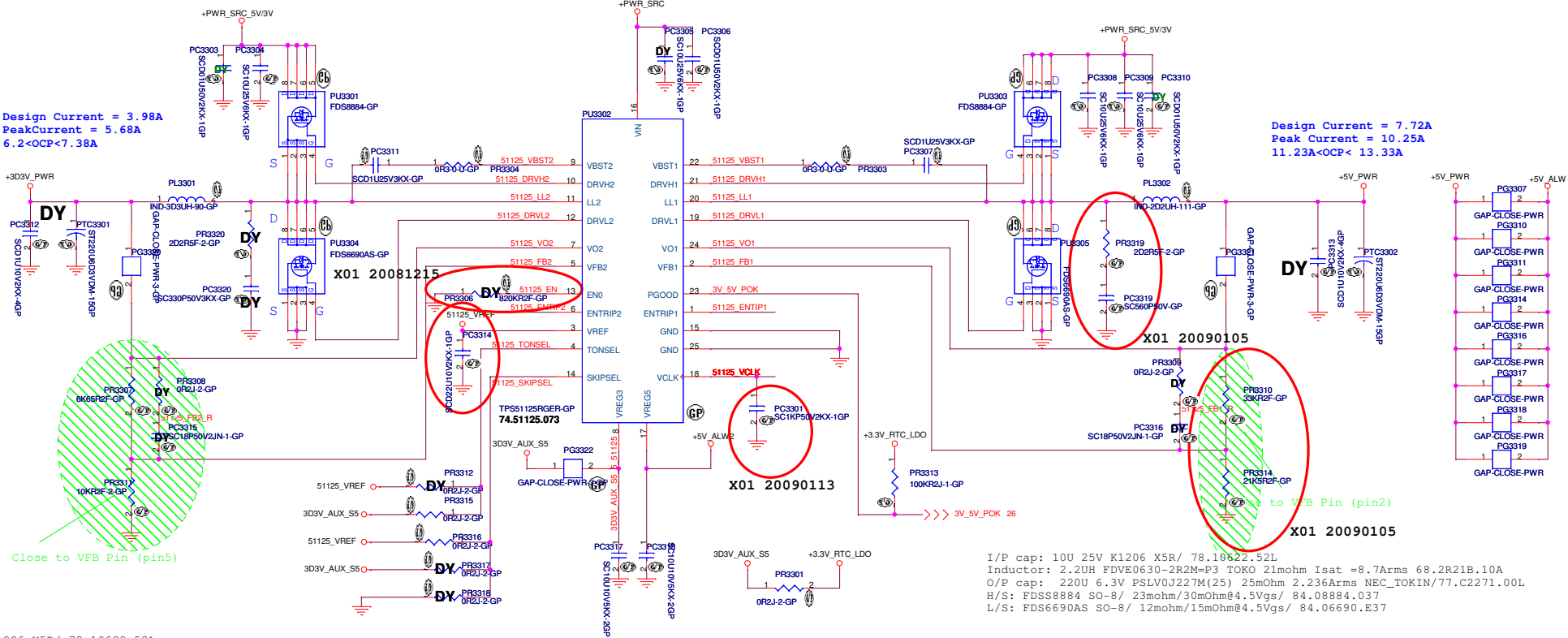
| | | |
|--------|-----------------|-----|
| Size | Document Number | Rev |
| Custom | | SB |

Date: Monday, March 23, 2009 Sheet 32 of 59



Design Current = 3.98A
 Peak Current = 5.68A
 6.2 < OCP < 7.38A

Design Current = 7.72A
 Peak Current = 10.25A
 11.23A < OCP < 13.33A



Close to VFB Pin (pin5)

Close to V&B Pin (pin2)

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
 Inductor: 3.3UH FDV0630-3R3M=P3 TOKO 31mohm Isat =6.9Arms 68.3R31A.10E
 O/P cap: 220U 6.3V PSLV0J227M(25) 25mOhm 2.236Arms NEC_TOKIN/77.C2271.
 H/S: FDS8884 SO-8/ 23mohm/30mOhm@4.5Vgs/ 84.08884.037
 L/S: FDS6690AS SO-8/ 12mohm/15mOhm@4.5Vgs/ 84.06690.E37

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
 Inductor: 2.2UH FDVE0630-2R2M=P3 TOKO 21mohm Isat =8.7Arms 68.2R21B.10A
 O/P cap: 220U 6.3V PSLV0J227M(25) 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
 H/S: FDS8884 SO-8/ 23mohm/30mOhm@4.5Vgs/ 84.08884.037
 L/S: FDS6690AS SO-8/ 12mohm/15mOhm@4.5Vgs/ 84.06690.E37

| EN0 | CH1 | CH2 | SKIPSEL | VREG3 or VREG5 | VREF (2V) | GND |
|----------------|--|---|---------------------|----------------|-----------|----------|
| Operating Mode | 200kHz | 265kHz | Operating Mode | OOA Auto Skip | Auto Skip | PWM only |
| | VREF | 245kHz | 305kHz | | | |
| | VREG3 | 300kHz | 375kHz | | | |
| | VREG5 | 365kHz | 460kHz | | | |
| Operating Mode | Open | 820kΩ to GND | GND | | | |
| | enable both LDOs, VCLK on and ready to turn on switcher channels | enable both LDOs, VCLK off and ready to turn on switcher channels | disable all circuit | | | |

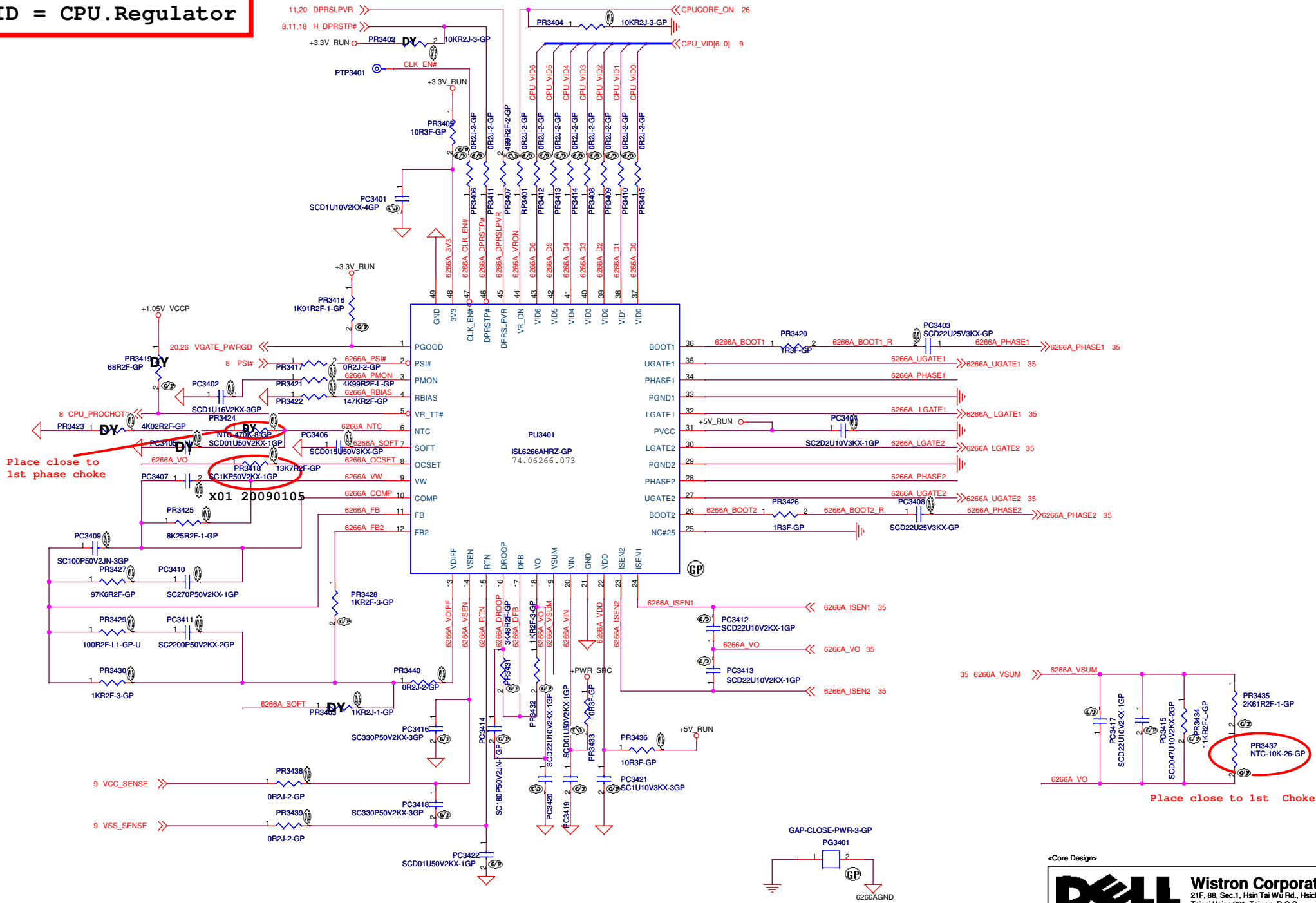
Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsein 221, Taiwan, R.O.C.

DCDC 5V/3D3V (TPS51125)

Alba Discrete

Date: Monday, March 23, 2009 Sheet 33 of 58

SSID = CPU.Regulator



<Core Design>

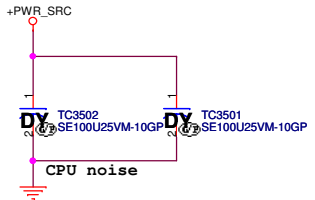
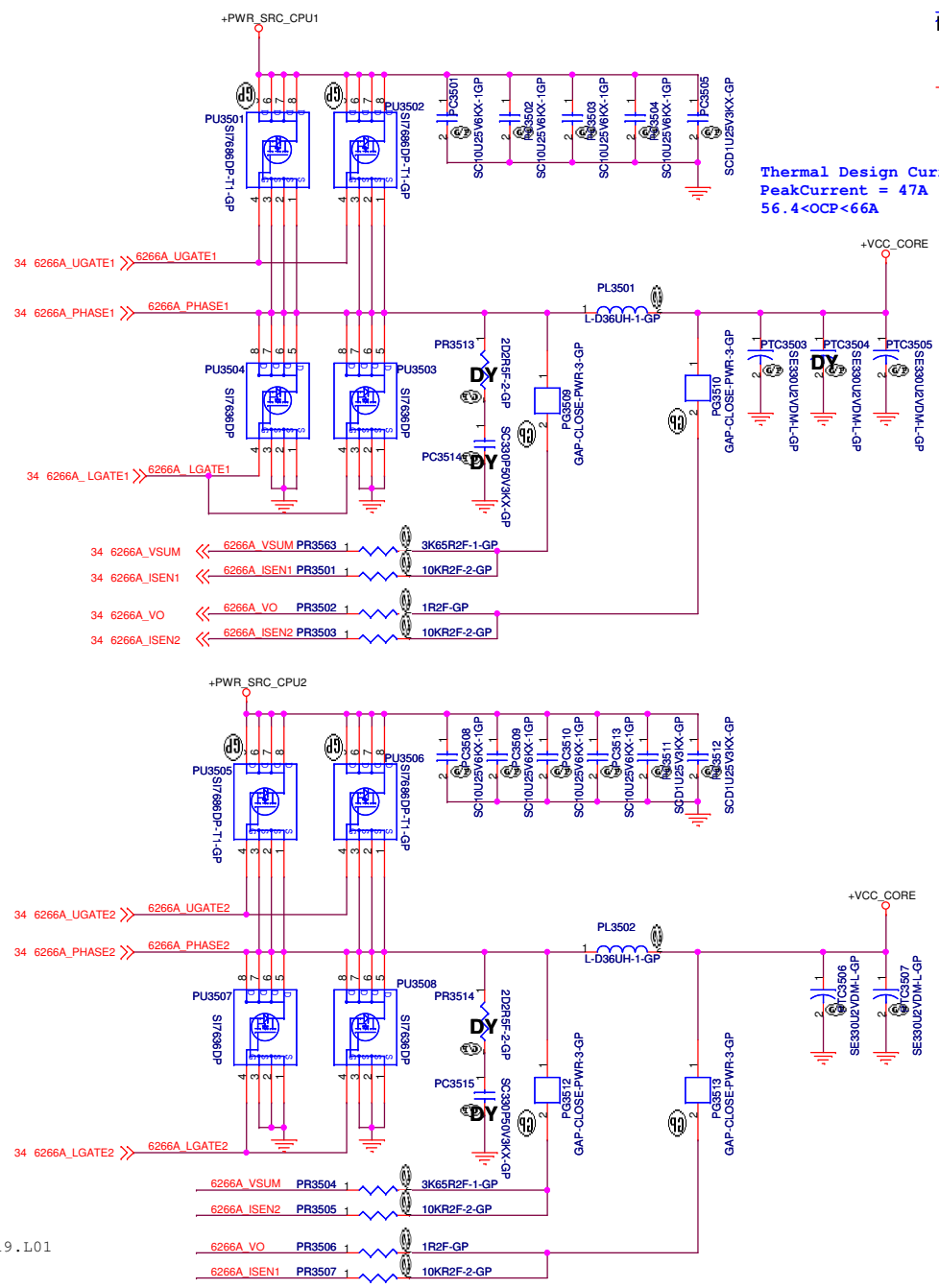
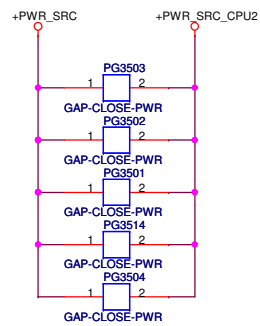
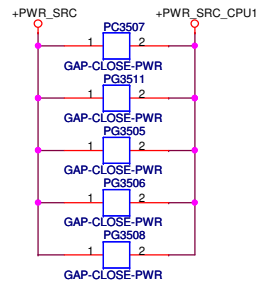
Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU VCORE POWER(1/2)**

| | | |
|--------|----------------------|-----------|
| Size | Document Number | Rev |
| Custom | Alba Discrete | SB |

Date: Monday, March 23, 2009 Sheet 34 of 59

SSID = CPU.Regulator



Thermal Design Current = 34A (IMVP6+ Rev:1.35)
 PeakCurrent = 47A
 56.4 < OCP < 66A

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
 Inductor: 0.36UH ETQP4LR36WFC PANASONIC 1.1mohm
 O/P cap: 330U 2V EEF5X0D331ER 9mOhm 3.0Arms Panasonic/79.33719.L01
 H/S: SI7686DP/ POWERPAK-8/ 14mOhm/ 4.5Vgs/ 84.07686.037
 L/S: SI7636ADP/ POWERPAK-8/ 4.8mOhm/ 4.5Vgs/ 84.07636.037

<Core Design>

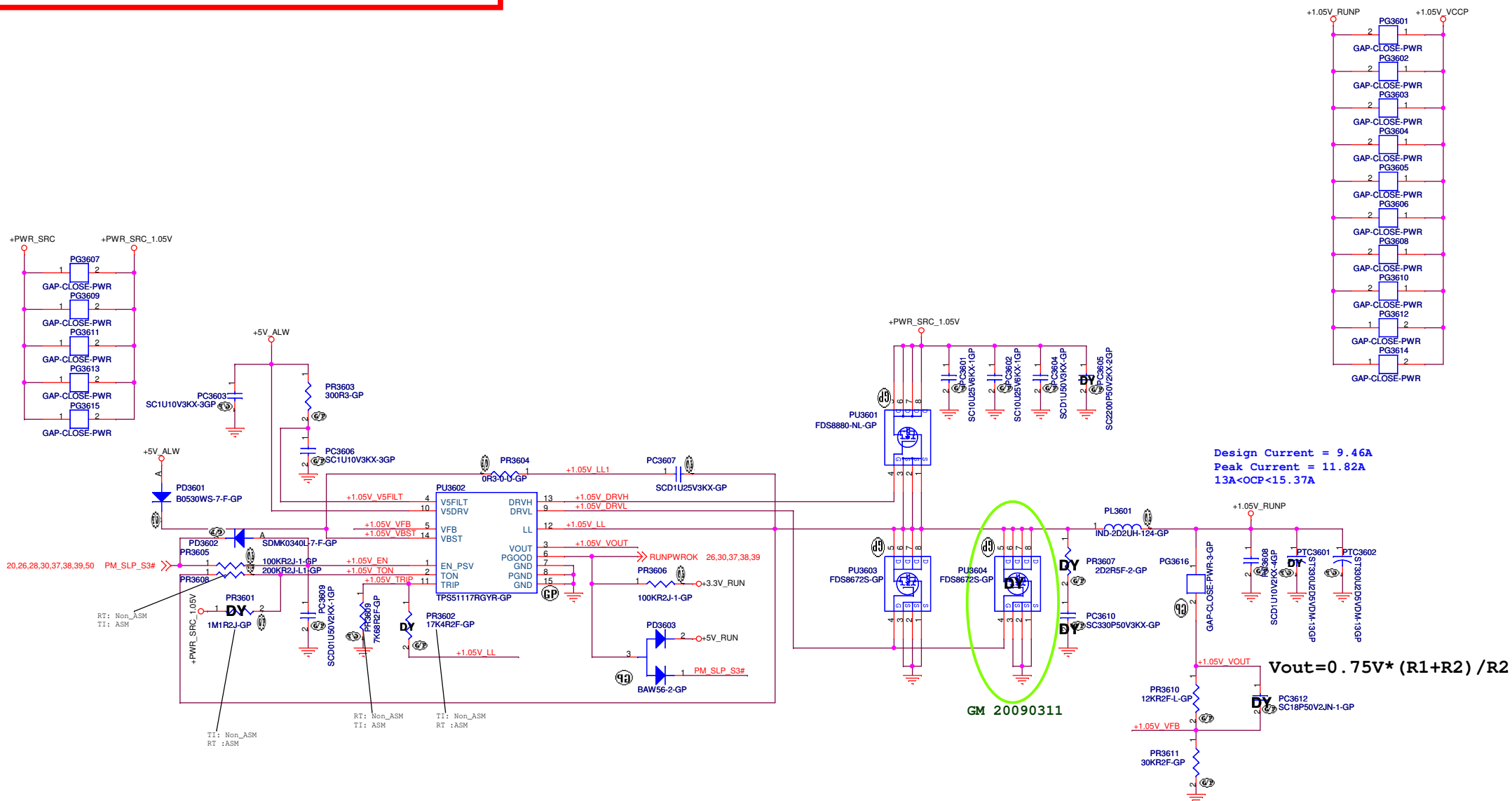
Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU VCORE POWER(2/2)**

| | | |
|--------|----------------------|-----------|
| Size | Document Number | Rev |
| Custom | Alba Discrete | SB |

Date: Monday, March 23, 2009 Sheet 35 of 59

SSID = PWR.Plane.Regulator_1p05v



Design Current = 9.46A
 Peak Current = 11.82A
 13A < OCP < 15.37A

$V_{out} = 0.75V * (R1 + R2) / R2$

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
 Inductor: 2.2UH FDVE1040-2R2M=P3 TOKO DCR:6.8mohm Isat =14.5Arms 68.2R21B.10M
 O/P cap: 330U 2.5V PSLV0E337M(15) 15mOhm 2.886Arms NEC_TOKIN/ 77.C3371.10L
 H/S: FDS8880 SO-8/ 9.6mOhm/12mOhm @4.5Vgs/ 84.08880.037
 L/S: FDS8672S SO-8/ 5.3mOhm/7.0mohm@4.5Vgs/ 84.08672.A37
 Switching freq-->350KHz

<Core Design>

Wistron Corporation
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 Taipei Hsien 221, Taiwan, R.O.C.

Title: **DC to DC 1.05V**

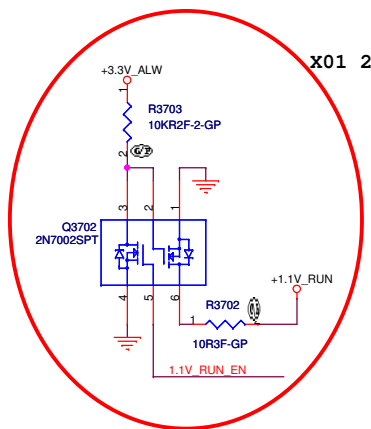
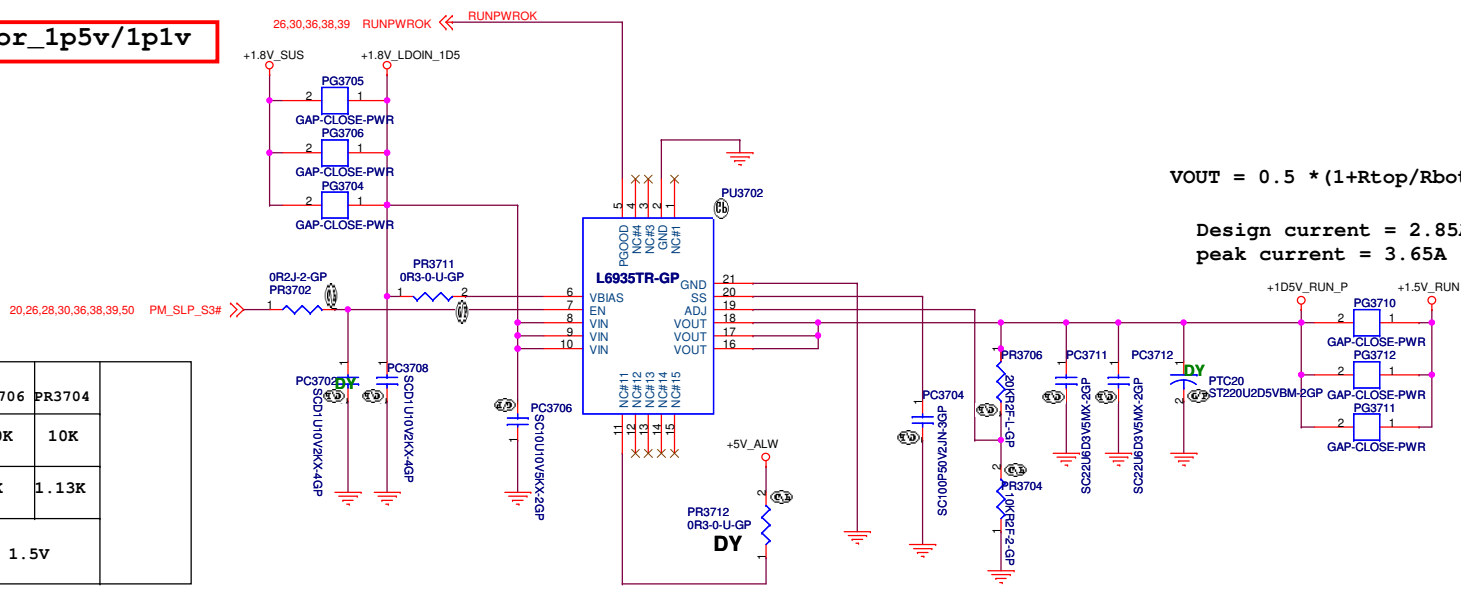
| | | |
|--------|----------------------|-----------|
| Size | Document Number | Rev |
| Custom | Alba Discrete | SB |

Date: Monday, March 23, 2009 Sheet 36 of 59

SSID = PWR.Plane.Regulator_lp5v/lp1v

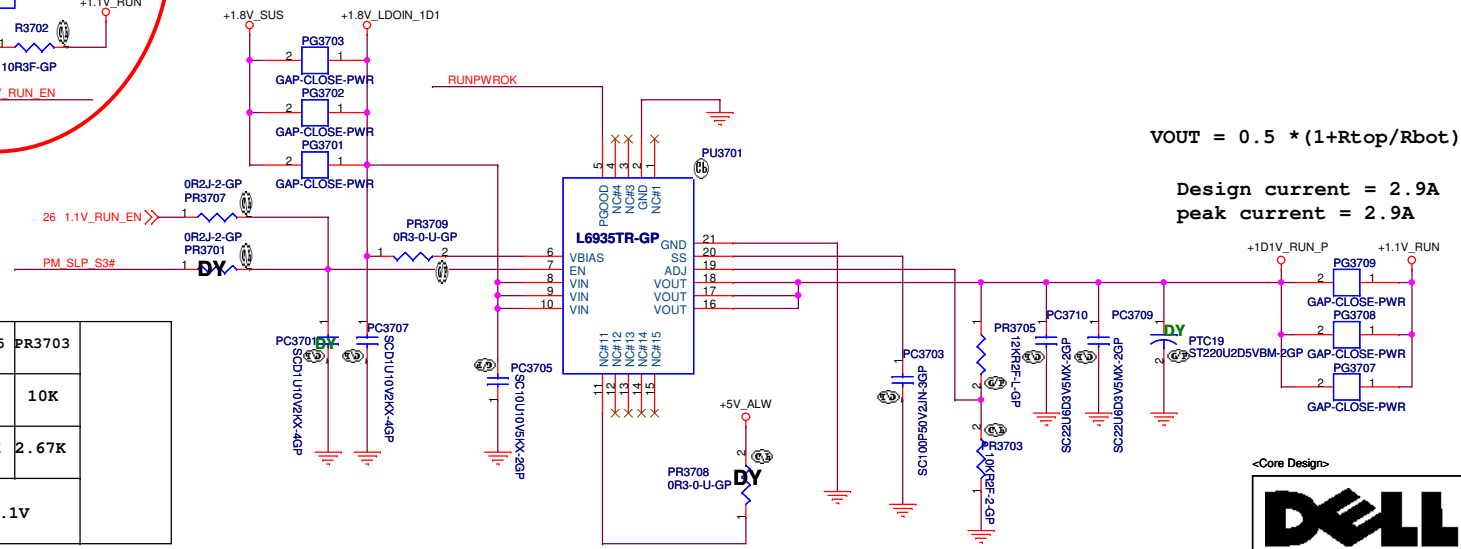
| Vendor | PIN6 | PIN11 | PIN20 |
|--------|-------|-------|-------|
| L6935 | VBIAS | N.C. | SS |
| RTXX35 | N.C. | VBIAS | N.C. |

| Vendor | PR3712 | PR3711 | PR3706 | PR3704 |
|--------|--------|--------|--------|--------|
| L6935 | DY | ASM | 20K | 10K |
| RTXX35 | ASM | DY | 1K | 1.13K |
| | | | 1.5V | |



| Vendor | PIN6 | PIN11 | PIN20 |
|--------|-------|-------|-------|
| L6935 | VBIAS | N.C. | SS |
| RTXX35 | N.C. | VBIAS | N.C. |

| Vendor | PR3708 | PR3709 | PR3705 | PR3703 |
|--------|--------|--------|--------|--------|
| L6935 | DY | ASM | 20K | 10K |
| RTXX35 | ASM | DY | 1.02K | 2.67K |
| | | | 1.1V | |



<Core Design>

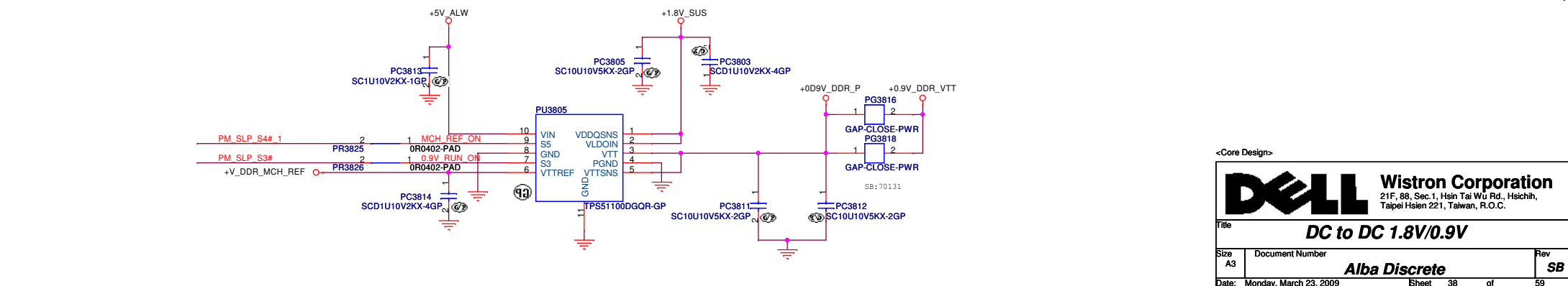
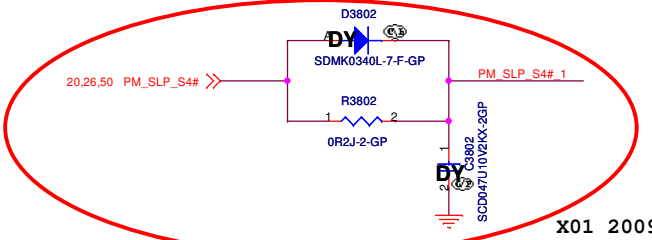
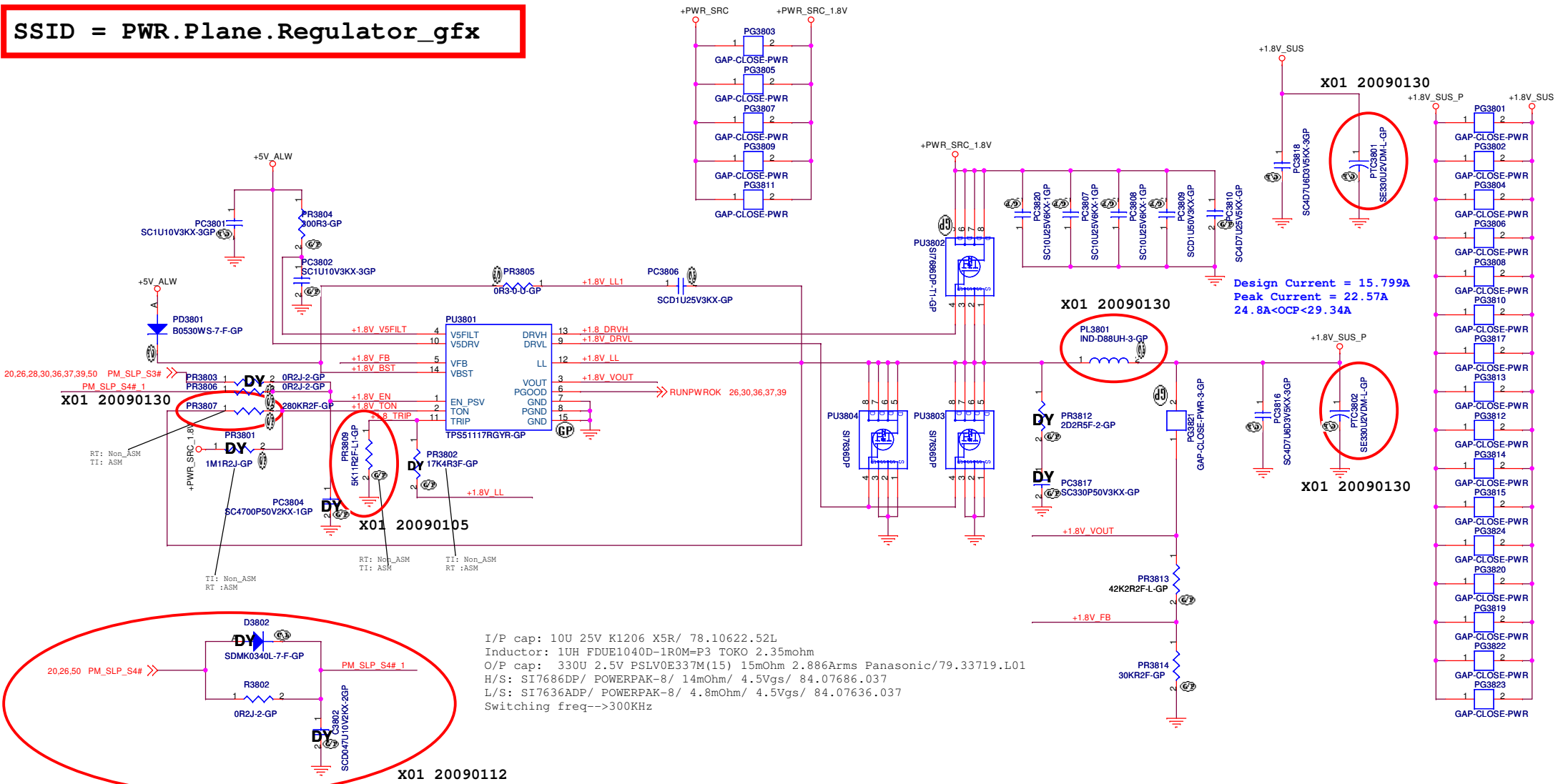
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **DC to DC L6935 1.5V / L6935 1.1V**

| | | |
|--------|----------------------|-----------|
| Size | Document Number | Rev |
| Custom | Alba Discrete | SB |

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SSID = PWR.Plane.Regulator_gfx



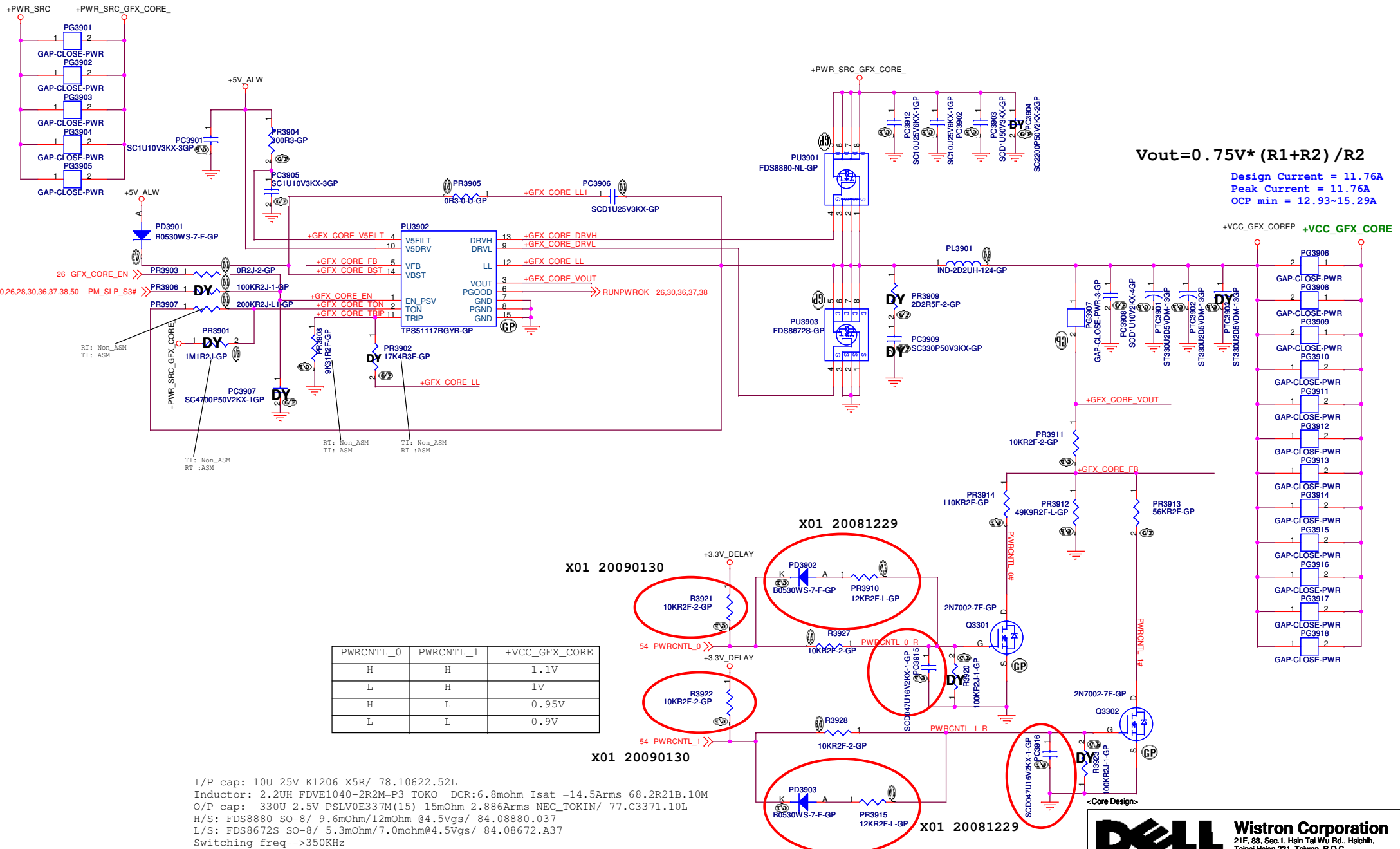
<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **DC to DC 1.8V/0.9V**

| | | |
|------------------------------|---|------------------|
| Size A3 | Document Number Alba Discrete | Rev SB |
| Date: Monday, March 23, 2009 | Sheet 38 of | 59 |

SSID = PWR.Plane.Regulator_gfx



$$V_{out} = 0.75V * (R1 + R2) / R2$$

Design Current = 11.76A
Peak Current = 11.76A
OCP min = 12.93~15.29A

| PWRCNTL_0 | PWRCNTL_1 | +VCC_GFX_CORE |
|-----------|-----------|---------------|
| H | H | 1.1V |
| L | H | 1V |
| H | L | 0.95V |
| L | L | 0.9V |

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
 Inductor: 2.2UH FDVE1040-2R2M=P3 TOKO DCR:6.8mohm Isat =14.5Arms 68.2R21B.10M
 O/P cap: 330U 2.5V PSLV0E337M(15) 15mOhm 2.886Arms NEC_TOKIN/ 77.C3371.10L
 H/S: FDS8880 SO-8/ 9.6mOhm/12mOhm @4.5Vgs/ 84.08880.037
 L/S: FDS8672S SO-8/ 5.3mOhm/7.0mOhm@4.5Vgs/ 84.08672.A37
 Switching freq-->350KHz

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Title: **VGA_CORE**

| | | |
|------------------------------|-----------------|--------|
| Size A3 | Document Number | Rev SB |
| Date: Monday, March 23, 2009 | Sheet 39 | of 59 |

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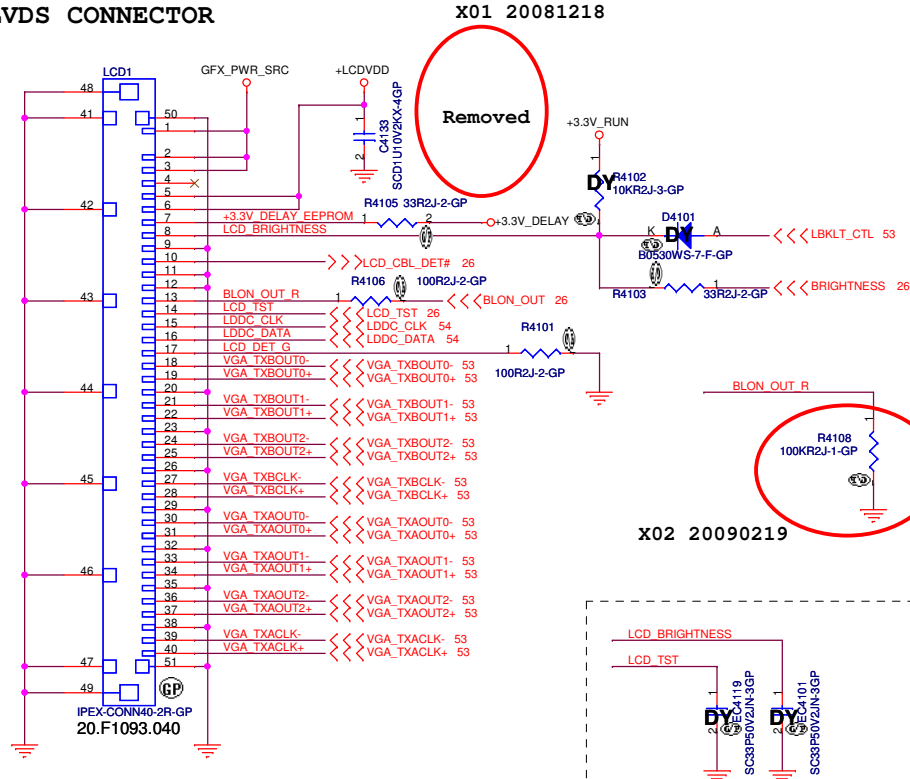
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| | | | |
|------------------|------------------------|-----------|----------|
| Title | | | |
| (Reserve) | | | |
| Size | Document Number | Rev | |
| Custom | Alba Discrete | SB | |
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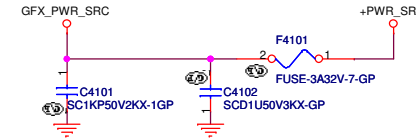
SSID = VIDEO

LVDS CONNECTOR

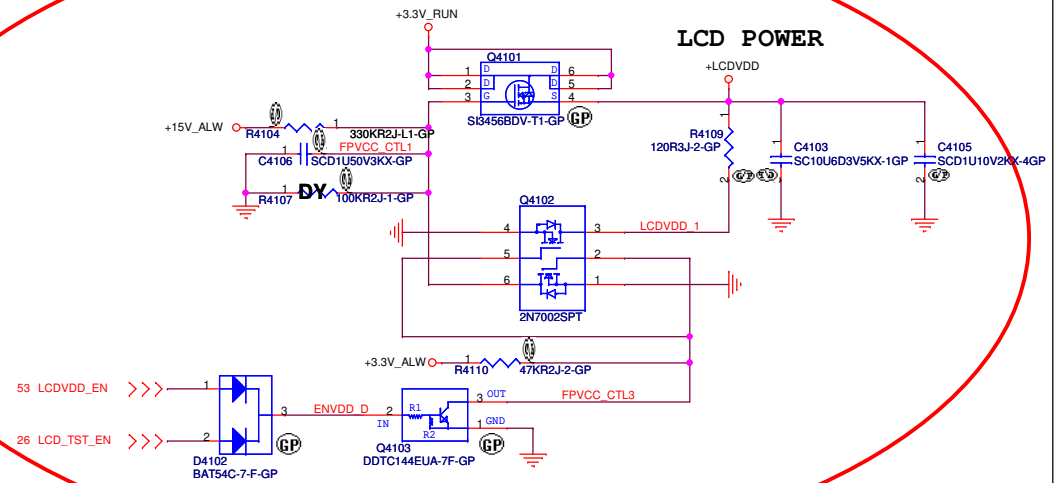


SSID = Inverter

INVERTER POWER



SSID = VIDEO

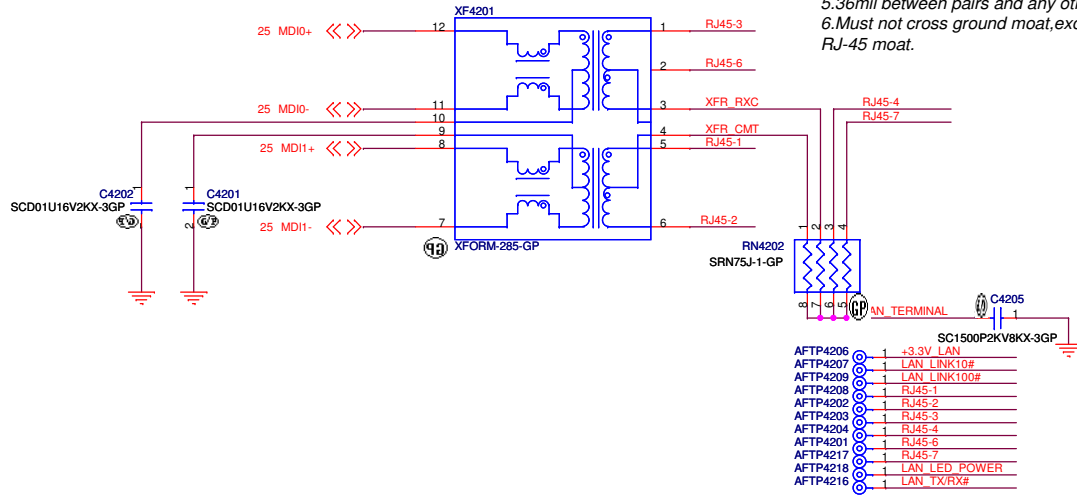


<Core Design>

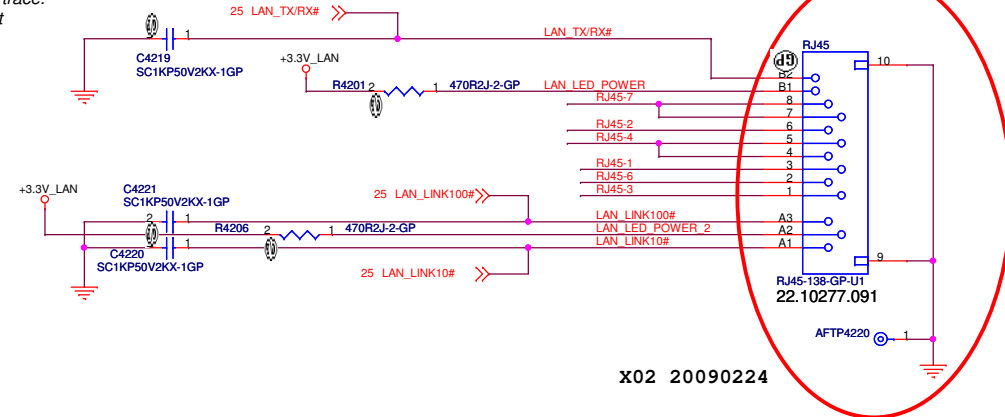
SSID = LOM

10/100M Lan Transformer

1. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
2. No vias, No 90 degree bends.
3. pairs must be equal lengths.
4. 6mil trace width, 12mil separation.
5. 36mil between pairs and any other trace.
6. Must not cross ground moat, except RJ-45 moat.



RJ45 Connector

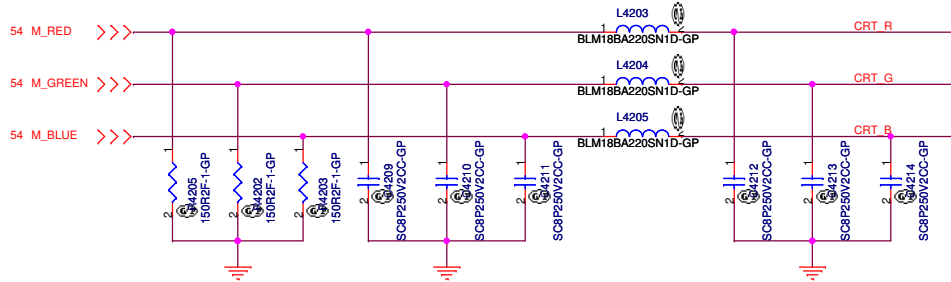


X02 20090224

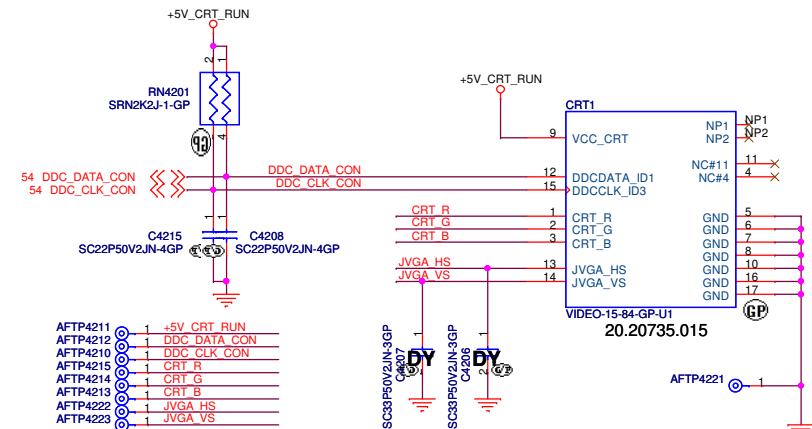
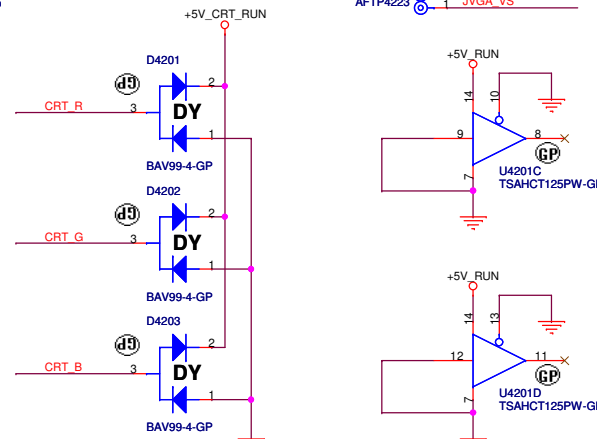
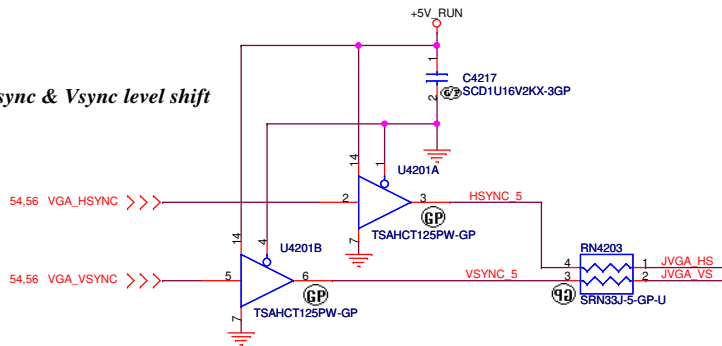
SSID = VIDEO

Layout Note:

- *Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.
- * RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.



Hsync & Vsync level shift



<Core Design>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

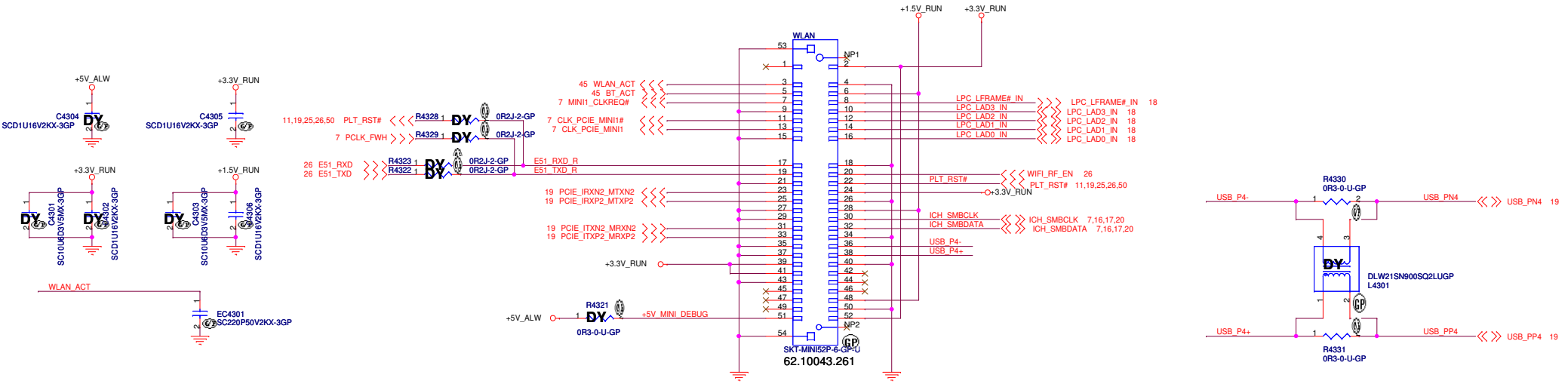
Title: **LAN/CRT Connector**

Size Custom Document Number **Alba Discrete** Rev **SB**

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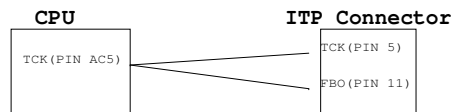
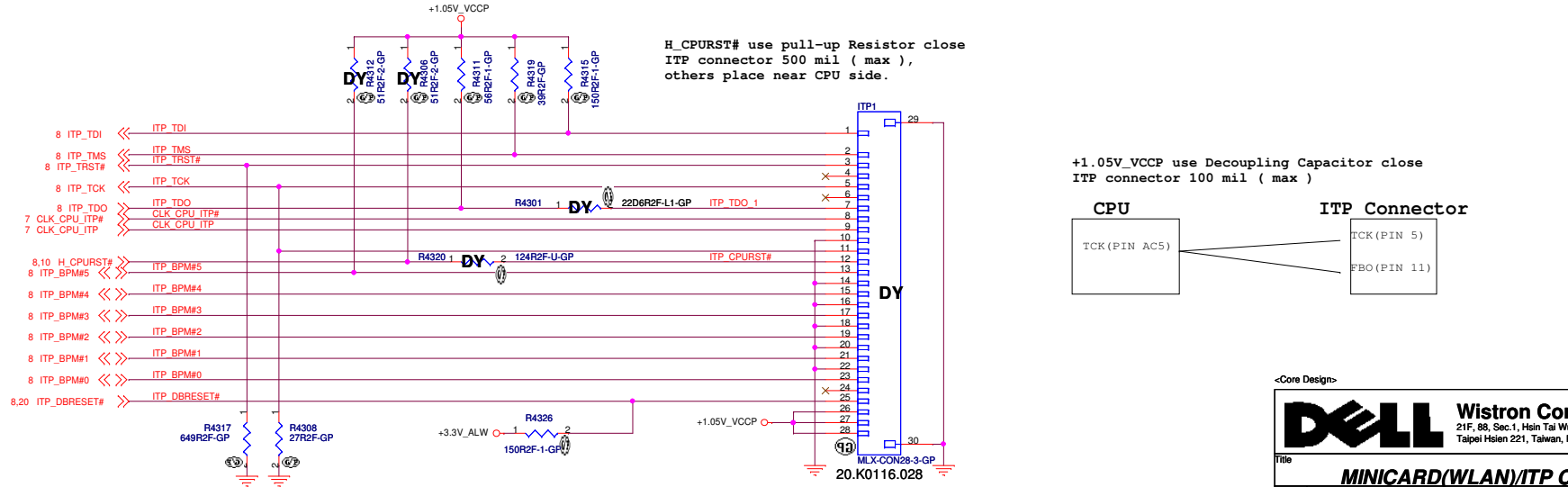
SSID = Wireless

Mini Card Connector(802.11a/b/g/n)



SSID = User.Interface

ITP Connector



<Core Design>

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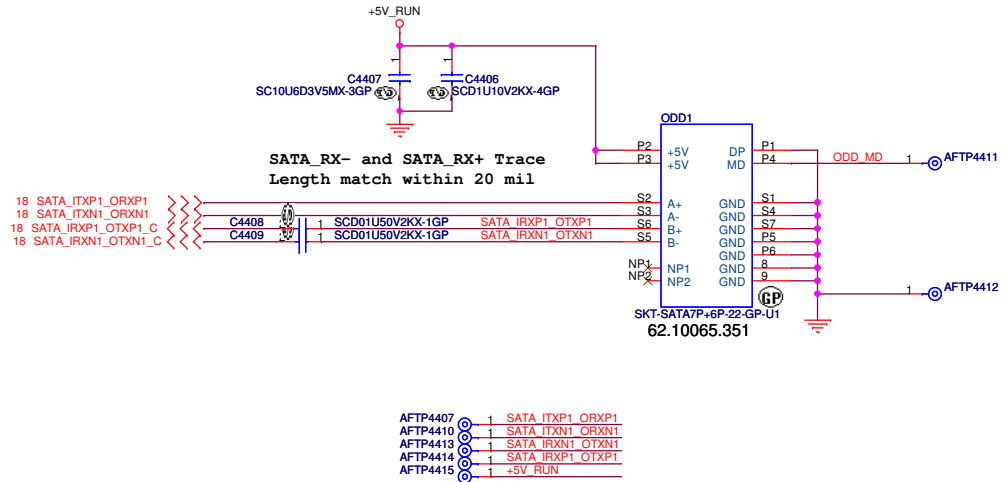
Title: **MINICARD(WLAN)/ITP CONN**

| | | |
|--------|----------------------|-----------|
| Size | Document Number | Rev |
| Custom | Alba Discrete | SB |

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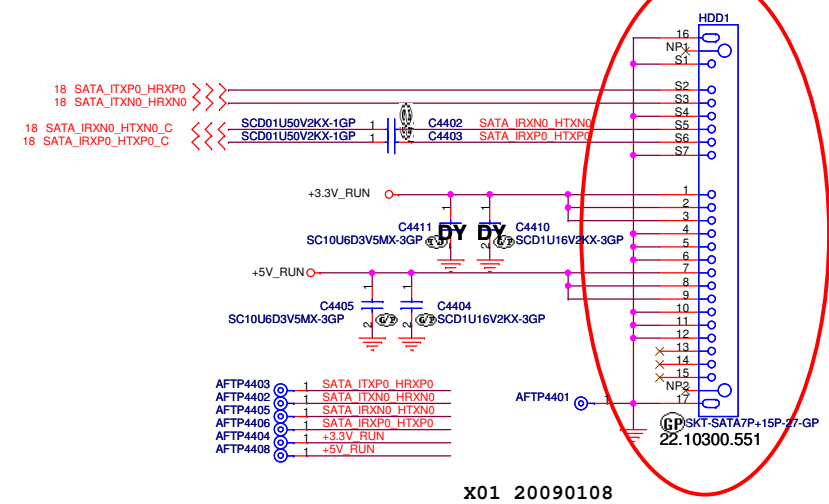
SSID = SATA

ODD Connector



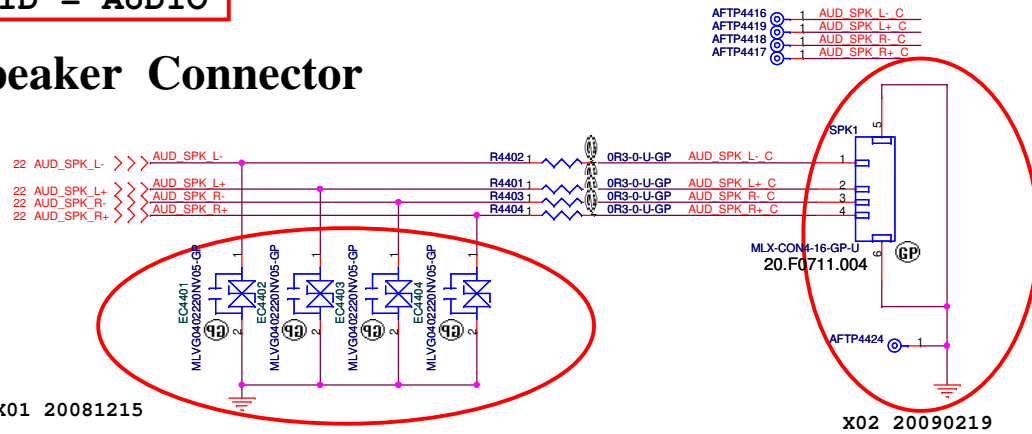
SSID = SATA

SATA HDD Connector



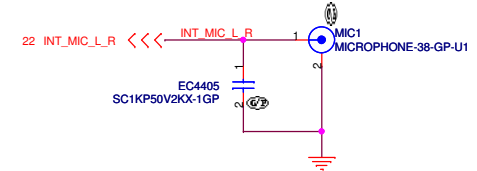
SSID = AUDIO

Speaker Connector



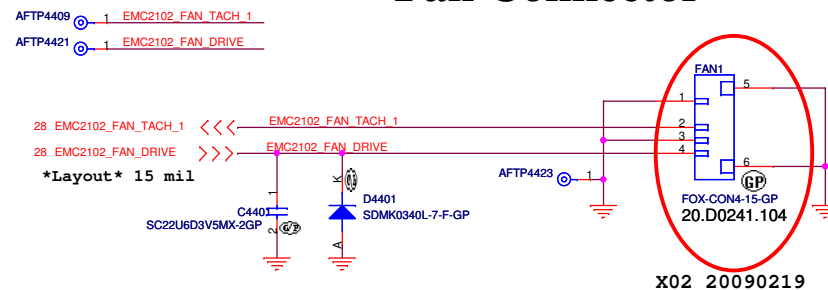
SSID = AUDIO

Internal MIC



SSID = Thermal

Fan Connector



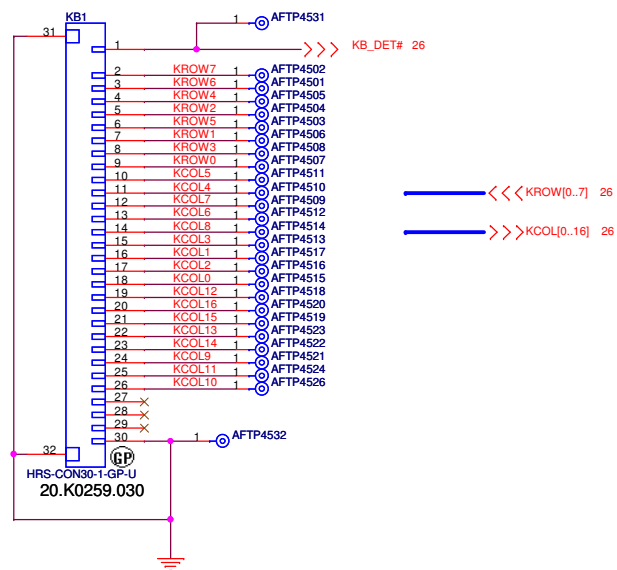
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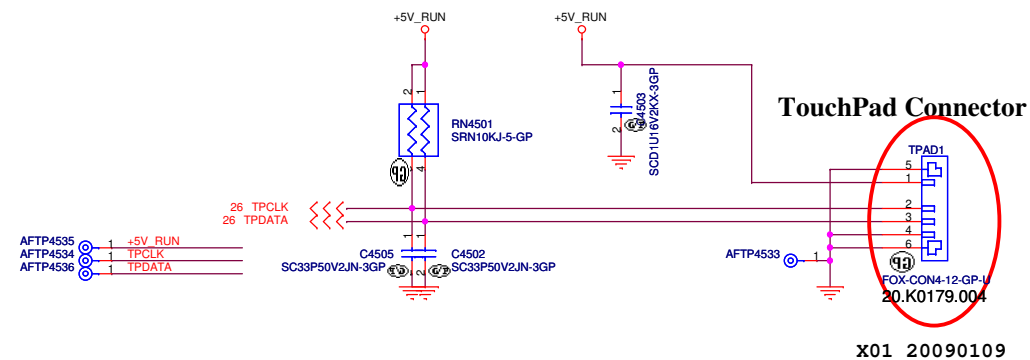
| | | | | | |
|--------|------------------------|-------|-------------------------|----|----|
| Title | | | HDD/ODD/FAN/SPEAKER/MIC | | |
| Size | Document Number | | Rev | | SB |
| Custom | Alba Discrete | | | | |
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SSID = KBC

Internal KeyBoard Connector

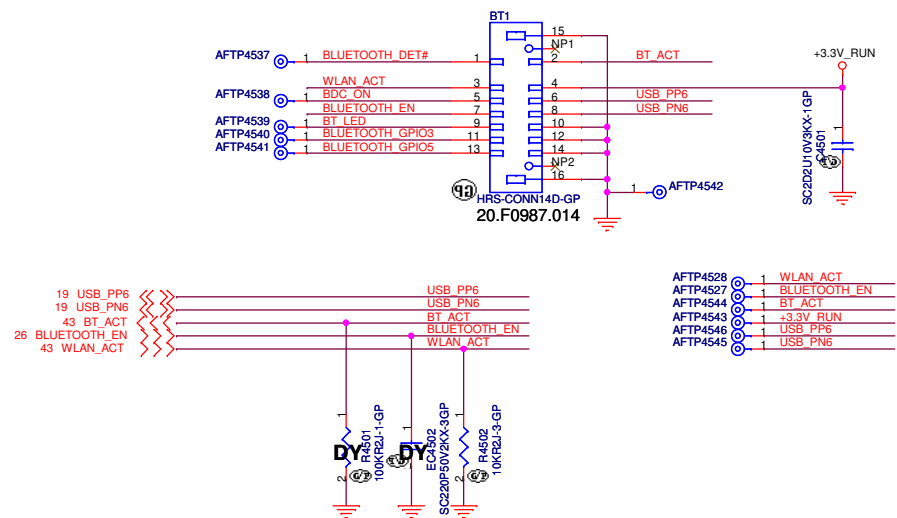


SSID = Touch.Pad



SSID = User.Interface

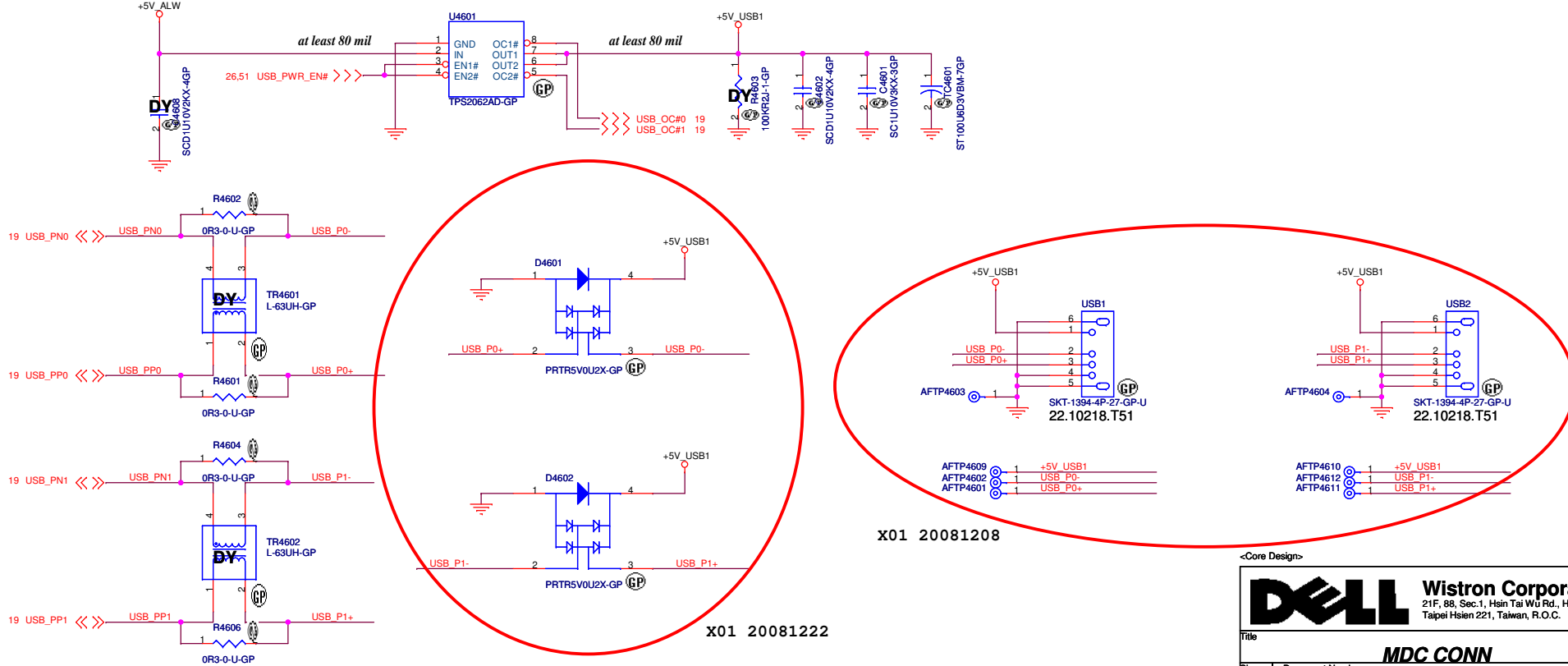
Bluetooth Module conn.



<Core Design>

Remove Modem
X01 20081208

USB Power



X01 20081208

X01 20081222

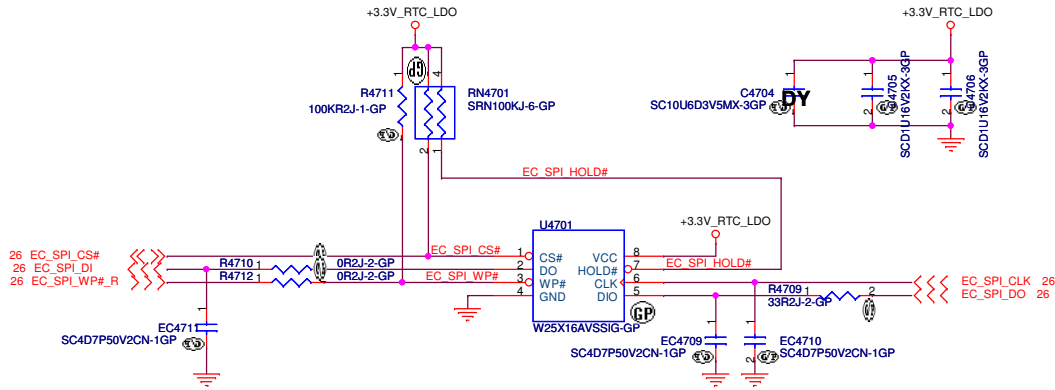
<Core Design>

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| | | |
|-----------------|------------------------|----------------|
| Title | | |
| MDC CONN | | |
| Size | Document Number | Rev |
| Custom | Alba Discrete | SB |
| Date: | Monday, March 23, 2009 | Sheet 46 of 59 |

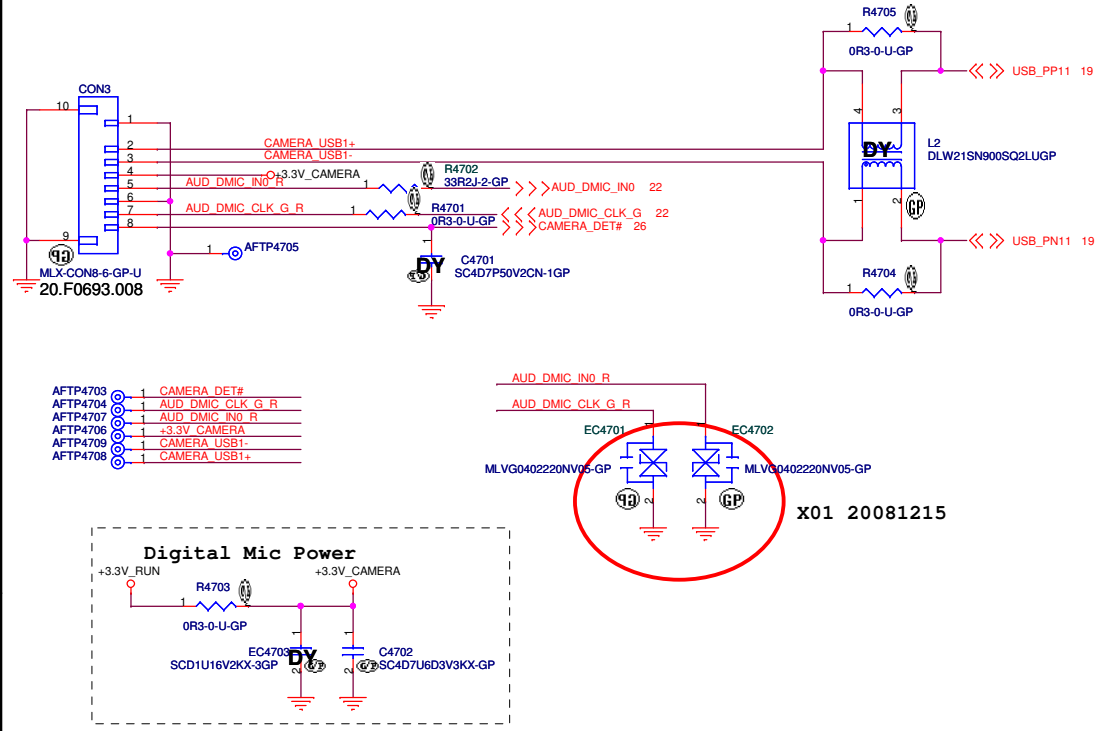
SSID = Flash.ROM

SPI FLASH ROM (16M bits)



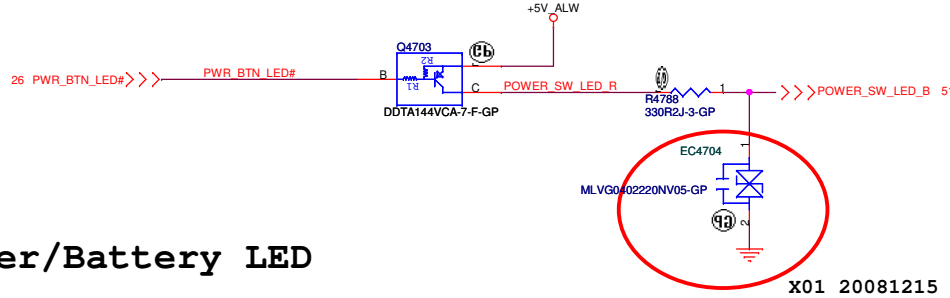
Camera Connector

SSID = User.Interface

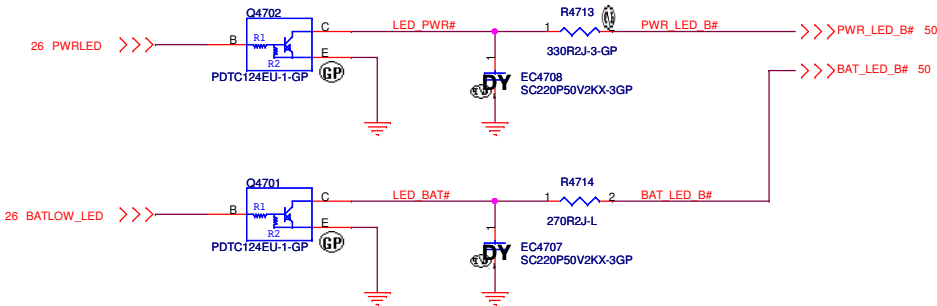


SSID = User.Interface

Power Button LED

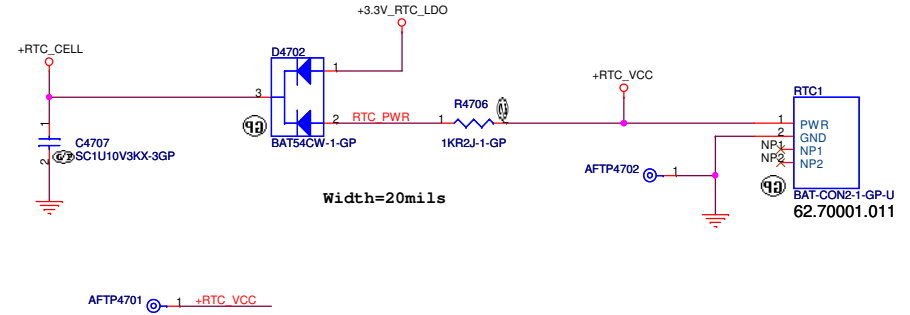


Power/Battery LED



SSID = RBATT

RTC Connector



<Core Design>

DELL Wistron Corporation
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 Taipei Hsien 221, Taiwan, R.O.C.

Title: **SPI Flash/LED/Camera/RTC**

Size: Custom Document Number: **Alba Discrete** Rev: **SB**

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<Core Design>

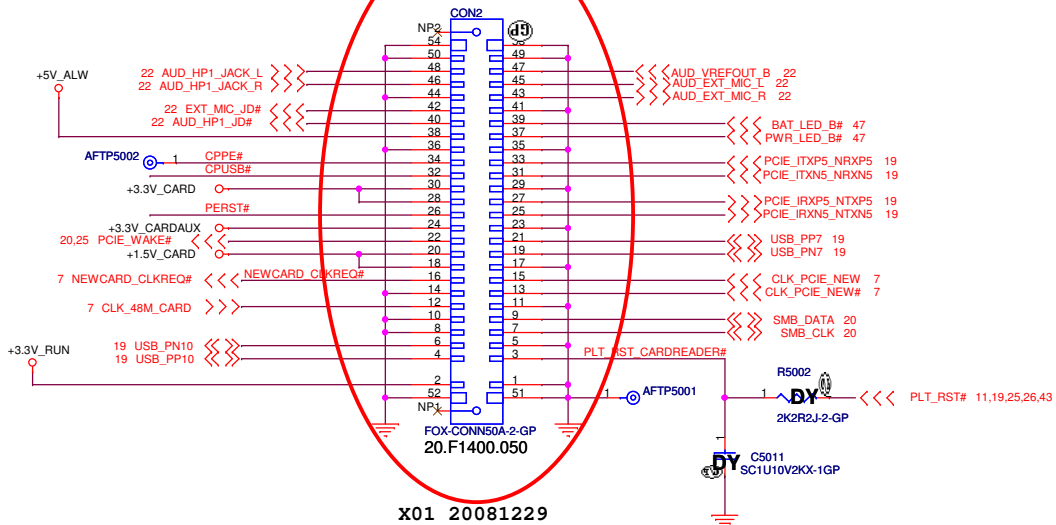
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|---|----------------------|---|-------|
|  | | Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | |
| Title | | | |
| (Reserve) | | | |
| Size | Document Number | Rev | |
| Custom | Alba Discrete | SB | |
| Date: Monday, March 23, 2009 | | Sheet 48 | of 59 |

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<Core Design>

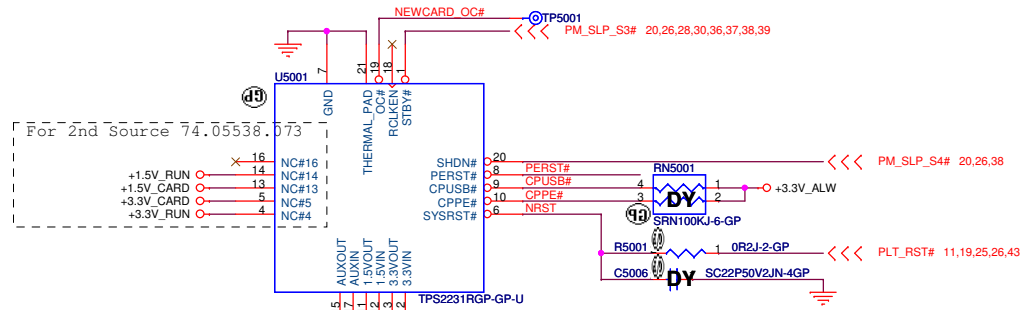
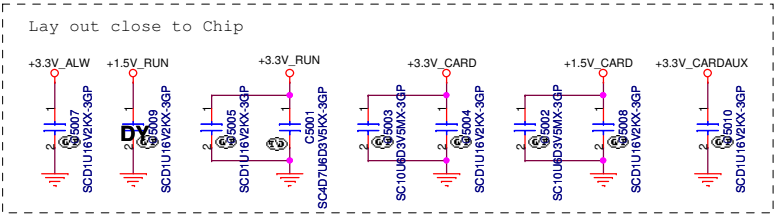
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|---|------------------------|--|---|----|-----------|
|  | | | Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | | |
| Title | | | | | |
| (Reserve) | | | | | |
| Size | Document Number | | | | Rev |
| Custom | Alba Discrete | | | | SB |
| Date: | Monday, March 23, 2009 | | Sheet | 49 | of 59 |

New Card Connector



X01 20081229

- AFTP5029 1 PWR_LED_B#
- AFTP5032 1 BAT_LED_B#
- AFTP5031 1 +5V_ALW
- AFTP5030 1 PLT_RST_CARDREADER#
- AFTP5028 1 PCIE_ITXP5_NRXPS
- AFTP5025 1 PCIE_ITXN5_NRXNS
- AFTP5023 1 PCIE_IRXP5_NTXPS
- AFTP5024 1 PCIE_IRXN5_NTXNS
- AFTP5026 1 AUD_VREFOUT_B
- AFTP5004 1 AUD_HP1_JACK_L
- AFTP5006 1 AUD_HP1_JACK_R
- AFTP5007 1 +3.3V_RUN
- AFTP5008 1 CPUSB#
- AFTP5005 1 USB_PP7
- AFTP5008 1 USB_PN7
- AFTP5011 1 AUD_EXT_MIC_L
- AFTP5010 1 AUD_EXT_MIC_R
- AFTP5011 1 EXT_MIC_ID#
- AFTP5013 1 AUD_HP1_ID#
- AFTP5014 1 CLK_48M_CARD
- AFTP5012 1 NEWCARD_CLKREQ#
- AFTP5015 1 +3.3V_CARD
- AFTP5022 1 PERST#
- AFTP5022 1 +3.3V_CARDAUX
- AFTP5021 1 PCIE_WAKE#
- AFTP5016 1 +1.5V_CARD
- AFTP5018 1 SMB_DATA
- AFTP5005 1 SMB_CLK
- AFTP5021 1 USB_PN10
- AFTP5028 1 USB_PP10

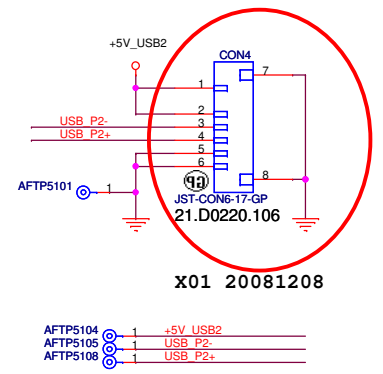
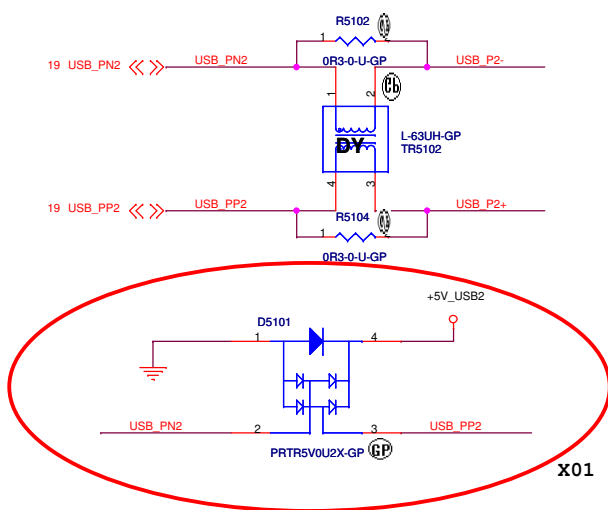
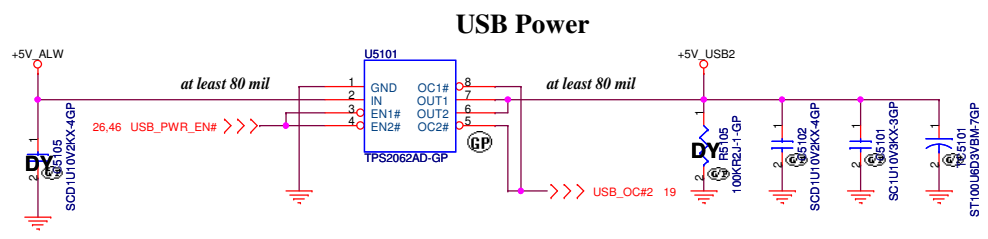


+1.5V_CARD Max. 650mA, Average 500mA.
 +3.3V_CARD Max. 1300mA, Average 1000mA
 +3.3V_CARDAUX Max. 275mA

<Core Design>

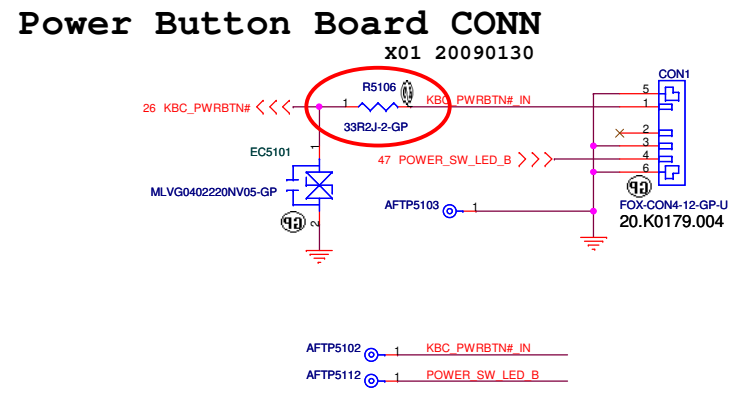
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| | | Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | |
| | | Title Express Card Board CONN | |
| Size | Document Number | Rev | |
| Custom | | Alba Discrete | SB |
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SSID = USB



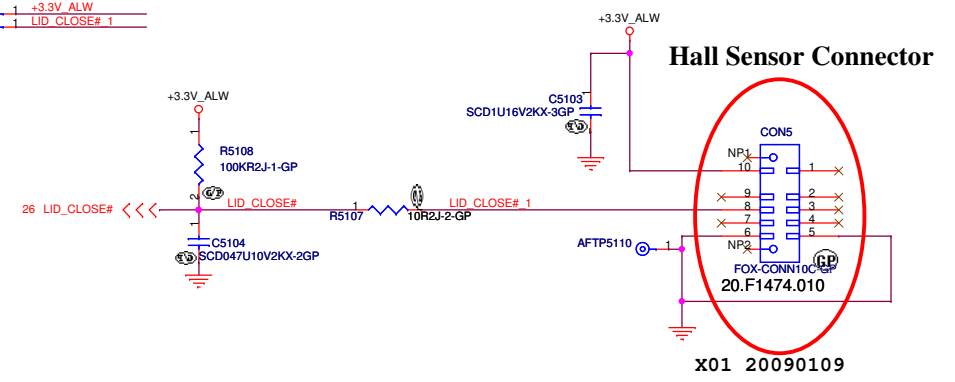
- X01 20081208
- AFTP5104 1 +5V_USB2
- AFTP5105 1 USB_P2
- AFTP5106 1 USB_P2+
- X01 20081222

SSID = User.Interface

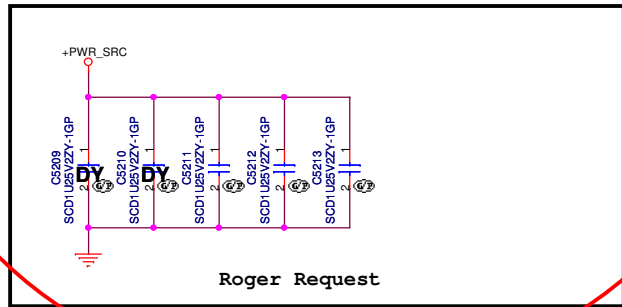
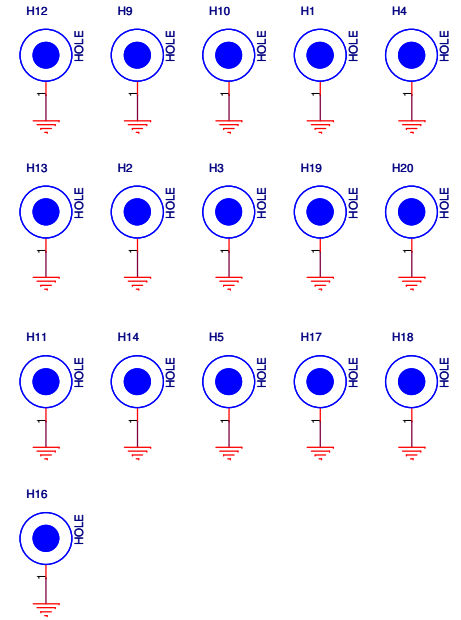
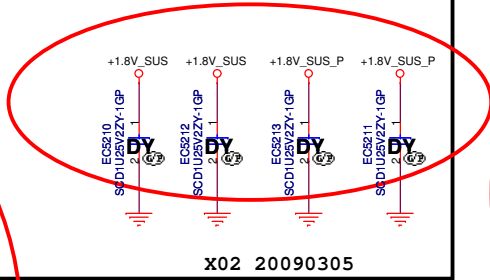
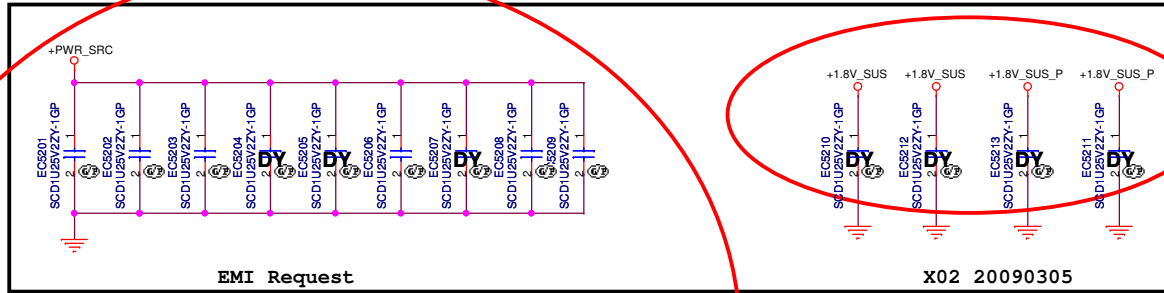


- AFTP5102 1 KBC_PWRBTN#_IN
- AFTP5112 1 POWER_SW_LED_B

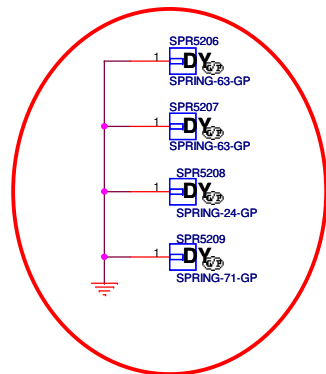
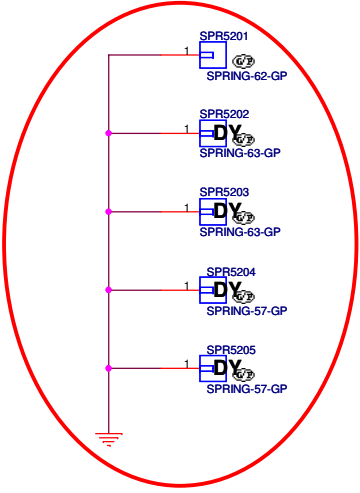
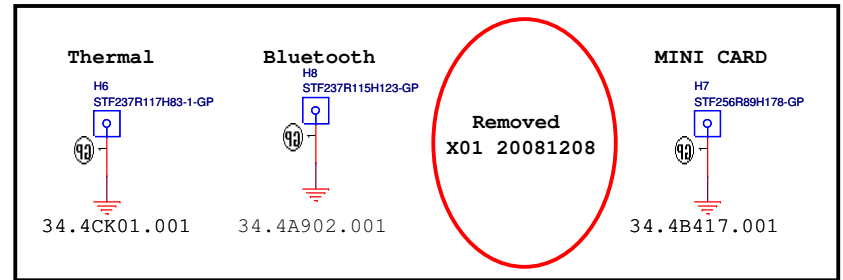
- AFTP5111 1 +3.3V_ALW
- AFTP5108 1 LID_CLOSE#_1



- X01 20090109



X01 20081215

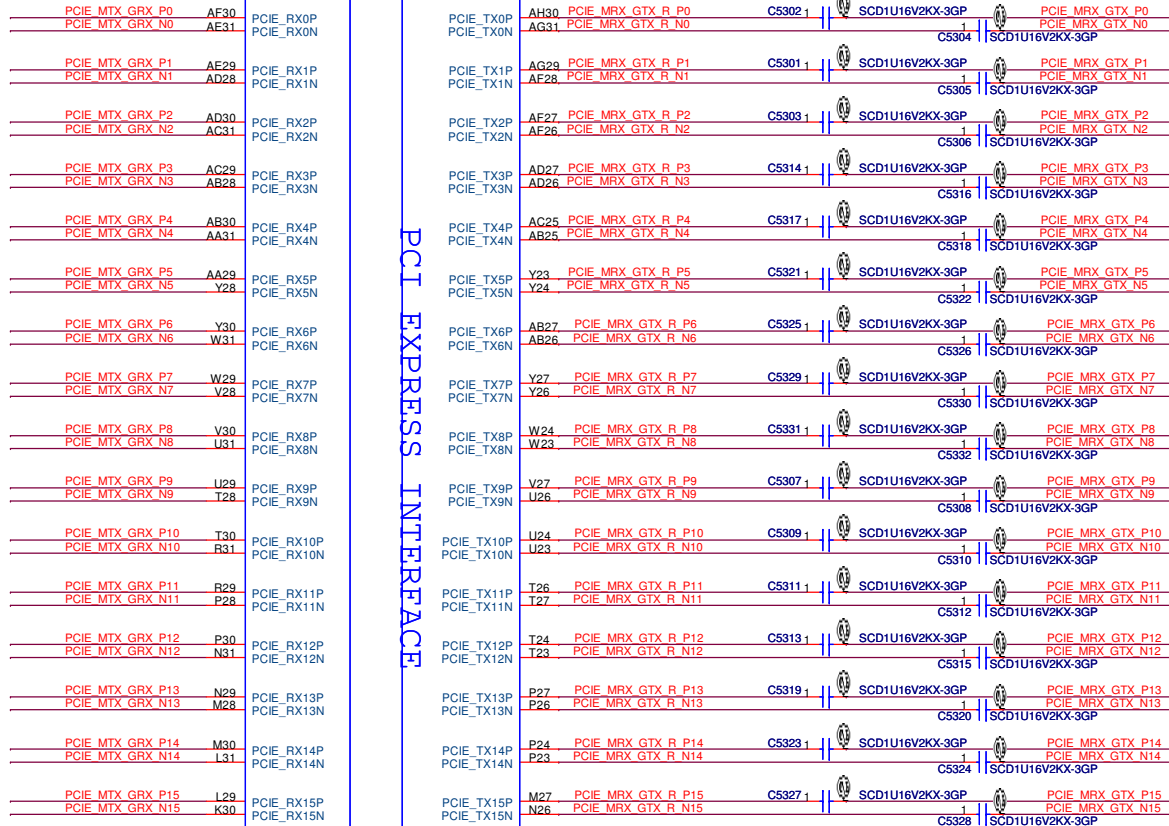


SSID = VIDEO

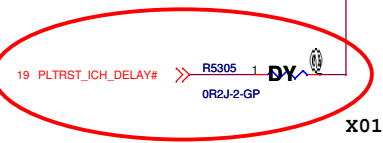
U5301A

1 OF 7

PCI EXPRESS INTERFACE



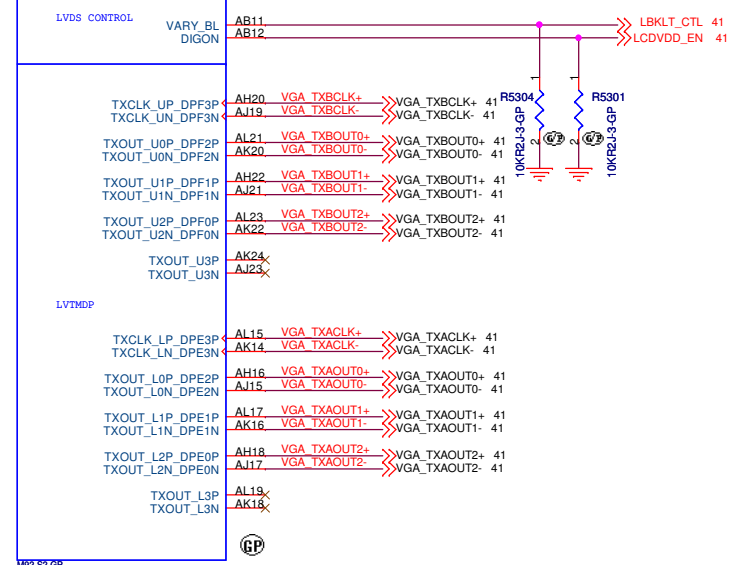
7 CLK_PCIE_VGA >>> CLK_PCIE_VGA# AK30
7 CLK_PCIE_VGA# >>> CLK_PCIE_VGA# AK32



X01 20081208

PCIE_MTX_GRX_P[0..15] <<< PCIE_MTX_GRX_P[0..15] 13
 PCIE_MTX_GRX_N[0..15] <<< PCIE_MTX_GRX_N[0..15] 13
 PCIE_MRX_GTX_P[0..15] >>> PCIE_MRX_GTX_P[0..15] 13
 PCIE_MRX_GTX_N[0..15] >>> PCIE_MRX_GTX_N[0..15] 13

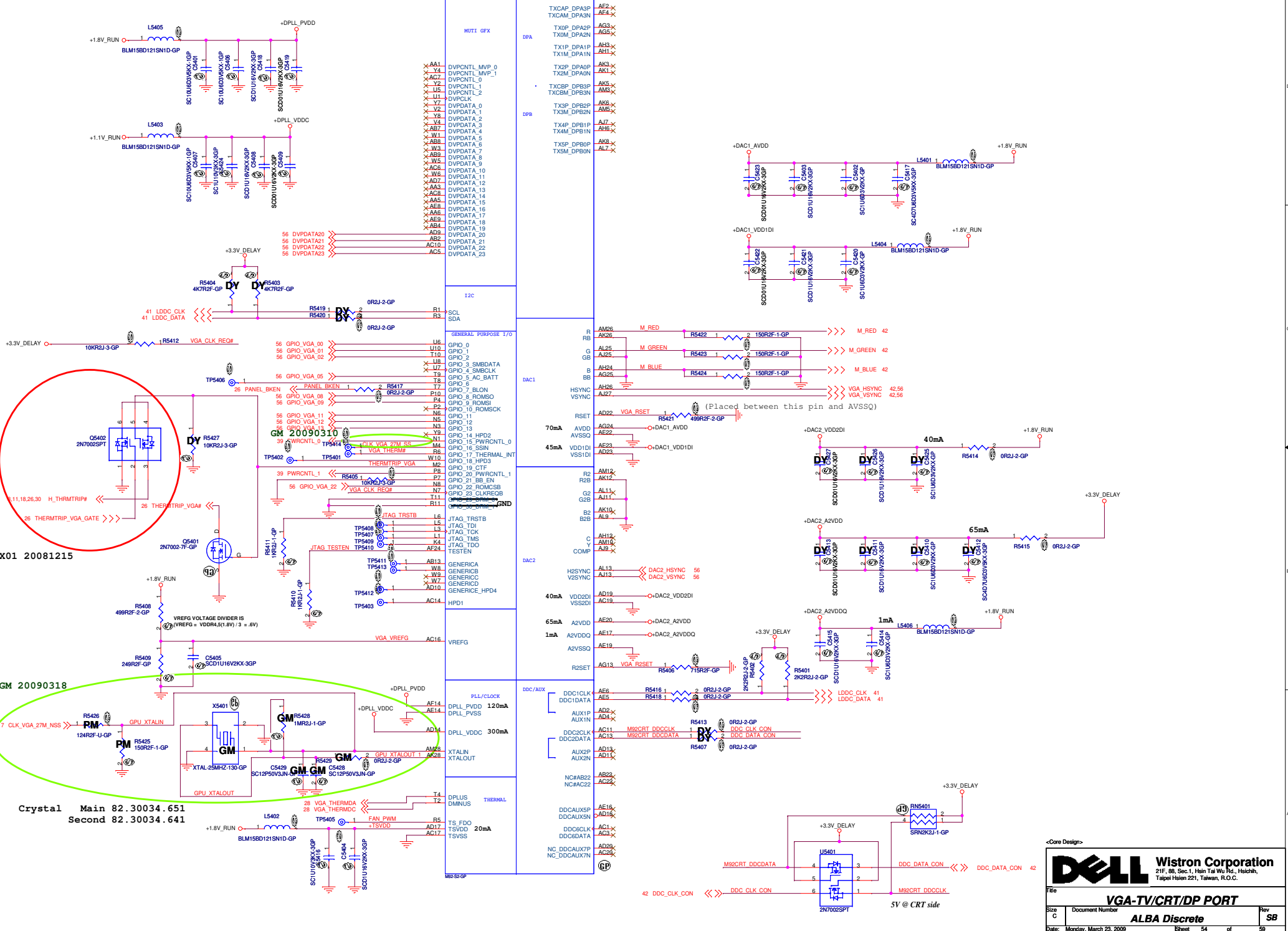
U5301F 6 OF 7



<Core Design>

| | | | |
|------------------------------|---------------------------------------|---|----|
| | | Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | |
| | | Title: VGA-PCIE/LVDS(1/4) | |
| Size: Custom | Document Number: ALBA Discrete | Rev: SB | |
| Date: Monday, March 23, 2009 | Sheet 53 | of | 59 |

SSID = VIDEO



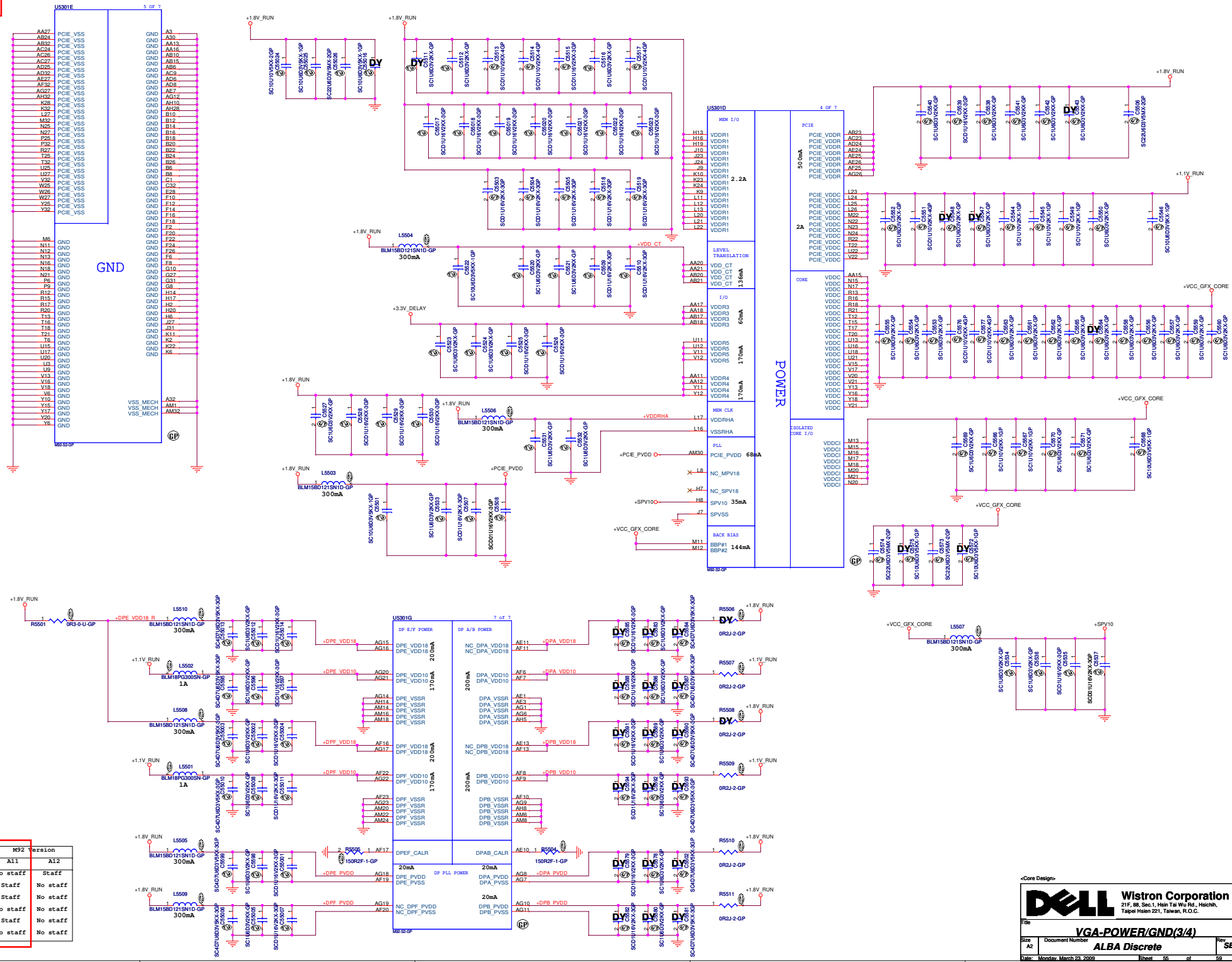
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File: **VGA-TV/CRT/DP PORT**

Size: Document Number **ALBA Discrete** Rev: **SB**

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| Part | M32 version | |
|-------|-------------|----------|
| | A11 | A12 |
| R5401 | No staff | Staff |
| Q5106 | Staff | No staff |
| R5402 | Staff | No staff |
| R5403 | No staff | No staff |
| Q5107 | Staff | No staff |
| C5384 | No staff | No staff |

-Core Design-

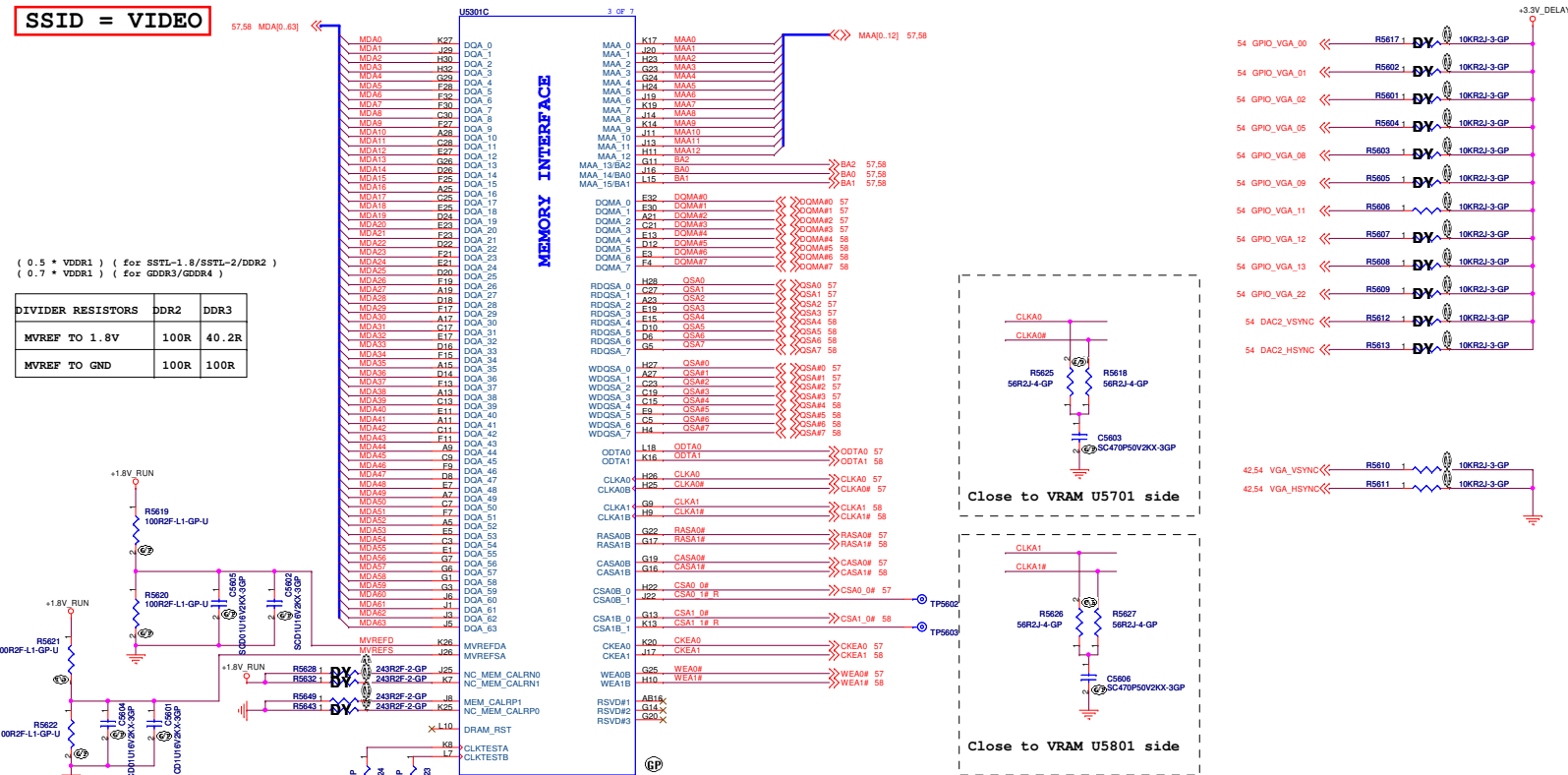
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File: **VGA-POWER/GND(3/4)**

Size: Document Number: **ALBA Discrete** Rev: **5B**

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SSID = VIDEO



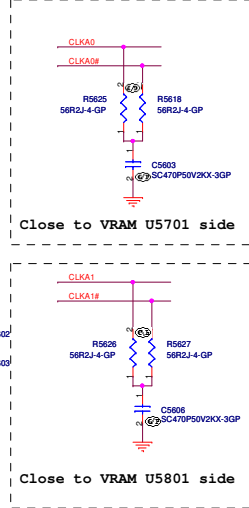
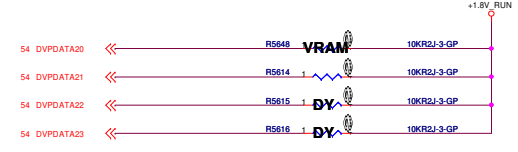
| DIVIDER RESISTORS | DDR2 | DDR3 |
|-------------------|------|-------|
| MVREF TO 1.8V | 100R | 40.2R |
| MVREF TO GND | 100R | 100R |

| | | | |
|---|--|--|--|
| ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESE | | | |
| GPIO3 , H2SYNC , V2SYNC | | | |
| PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESE | | | |

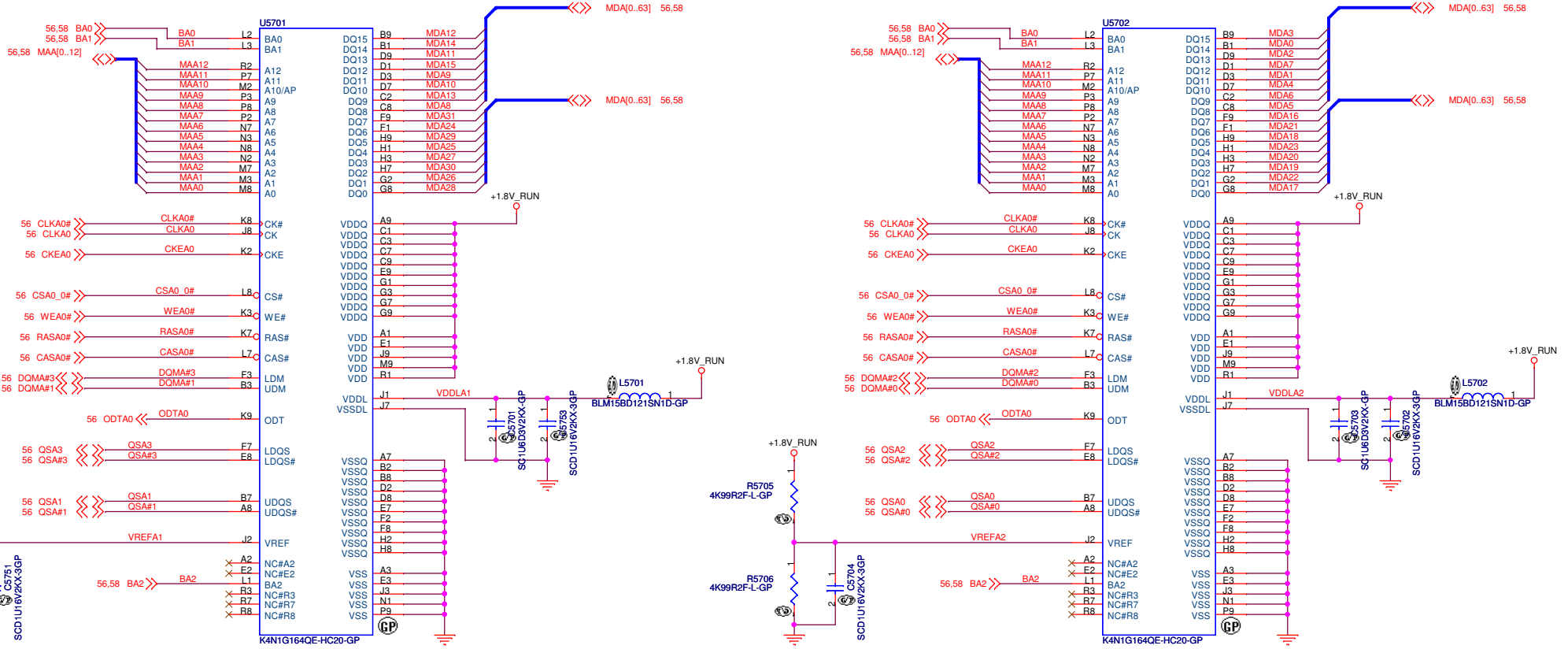
| If BIOS_ROM_EN (GPIO22) = 0 | | If BIOS_ROM_EN (GPIO22) = 1 | | |
|--------------------------------------|----------------|-----------------------------|-------------|----------------|
| Size of the primary memory apertures | GPIO(13,12,11) | Manufacturer | Part Number | GPIO(13,12,11) |
| 128MB | x000 | ST Microelectronics | M25P05A | 0100 |
| 256MB | x010 | | M25P10A | 0101 |
| 64MB | x010 | | M25P20 | 0101 |
| 32MB | x | | M25P40 | 0101 |
| 512MB | x | Chinglis (formerly PMC) | M25P80 | 0101 |
| 1GB | x | | Pm25LV512A | 0100 |
| 2GB | x | | | Pm25LV010A |
| 4GB | x | | | |

| STRAPS | PIN | DESCRIPTION |
|------------------|------------------------|---|
| TX_PWRS_ENB | GPIO0 | Transmitter Power Savings Enable 0 = 50% Tx output swing 1 = Full Tx output swing |
| TX_DEEMPH_EN | GPIO1 | Transmitter De-emphasis Enable 0 = Tx de-emphasis disabled 1 = Tx de-emphasis enabled |
| BIF_GEN2_EN_A | GPIO2 | 0 = Advertises the PCI-E device as 2.5GT/s 1 = Advertises the PCI-E device as 5GT/s |
| BIF_CLK_PM_EN | GPIO8 | 0 = Disable CLKREQ# power management capability 1 = Enable CLKREQ# power management capability |
| ROMIDCFG[3:0] | GPIO(13,12,11) | If BIOS_ROM_EN=1, then Config(3:0) defines the ROM type If BIOS_ROM_EN=0, then Config(3:0) defines the primary memory aperture size |
| BIOS_ROM_EN | GPIO_22_ROMCSB | Enable external BIOS ROM device 0 = Disable external BIOS ROM device 1 = Enable external BIOS ROM device |
| AUD[1] AUD[0] | VGA_HSYNC VGA_VSYNC | AUD[1:0] 00: No audio function 01: Audio for DisplayPort and HDMI (if adapter is detected) 10: Audio for DisplayPort only 11: Audio for both DisplayPort and HDMI |

| STRAPS | PIN | DESCRIPTION |
|----------|----------------|---|
| MEM_TYPE | DVPDATA(23:20) | MEMORY TYPE, MAKE AND SIZE INFO 0000 - gDDR2 ----- 0001 - gDDR2 64Mx16 HYNIX 0010 - gDDR2 64Mx16 SAMSUNG 0011 - gDDR2 32Mx16 HYNIX 0100 - gDDR2 32Mx16 SAMSUNG |

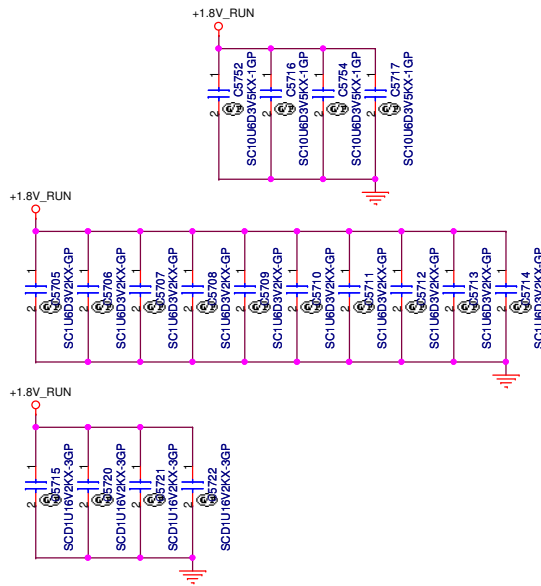


SSID = VIDEO



- 64X16 SAMSUNG 72.41164.G0U
- 64X16 HYNIX 72.51G63.A0U

- 32X16 SAMSUNG 72.45116.G0U
- 32X16 HYNIX 72.55162.B0U



<Core Design>

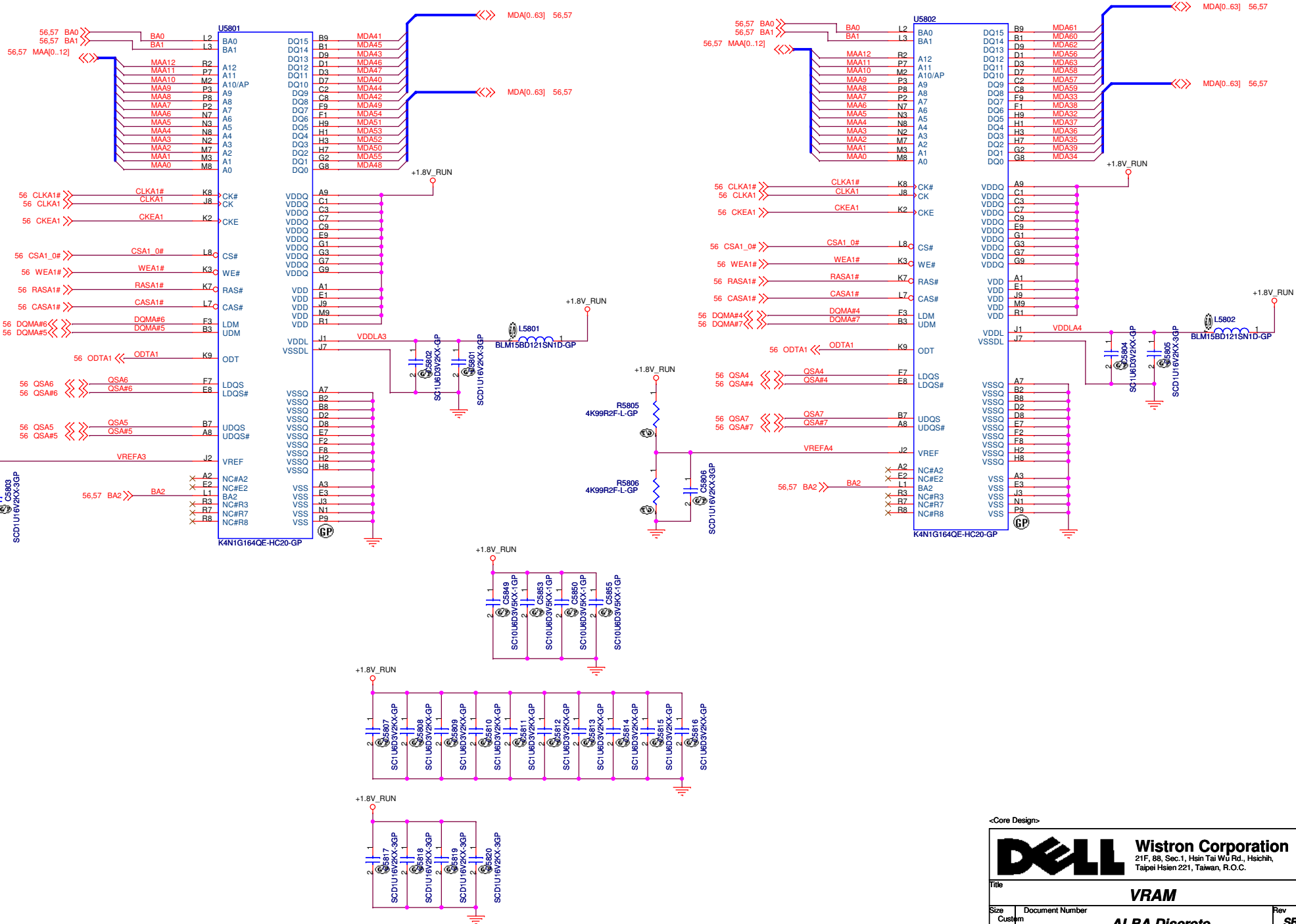
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 Taipei Hsien 221, Taiwan, R.O.C.

Title: **VRAM(1/2)**

| | | |
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Date: Monday, March 23, 2009 Sheet 57 of 60

SSID = VIDEO



<Core Design>

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Title: **VRAM**

| | | |
|--------------|---------------------------------------|----------------|
| Size: Custom | Document Number: ALBA Discrete | Rev: SB |
|--------------|---------------------------------------|----------------|

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| Item | Page# | Date | Request By | Issue description | Solution Description | Rev. |
|------|------------------|------------|------------|---|---|------|
| 1 | 18, 46 52, 42 | 2008/12/08 | DELL | Remove Modem function. | Remove MDC schematics, holding, stand off. | X01 |
| 2 | 19, 53 | 2008/12/08 | Wistron | Reserve PLT_RST# for GPU PCIE reset. | Add R1913 (DY), R5305 (DY). | X01 |
| 3 | 25 | 2008/11/26 | Realtek | Power down sequence issue, request by vendor. | Change R2506 to 1K ohm. | X01 |
| 4 | 25 | 2008/12/18 | KDS | Follow crystal vendor test report. | Change C2501 to 18pF. C2502 to 15pF. | X01 |
| 5 | 26 | 2008/12/08 | Wistron | MB version ID change. | Pop R2609, depop R2608. | X01 |
| 6 | 38 | 2008/12/08 | Wistron | AMD power regulator issue. | Change 1.8V, 0.9V power regulator. | X01 |
| 7 | 42 | 2008/12/08 | Wistron | Follow ME connector list for touch pad connector. | Change TPAD1. | X01 |
| 8 | 46, 51 | 2008/12/08 | Wistron | Follow ME connector list for USB connector. | Change USB1, USB2 and CON4. | X01 |
| 9 | 30, 33 | 2008/12/15 | Wistron | MOSFET can not fully trun on issue. | Add +15V_ALW power circuits. And modify 3.3V_RUN, 5V_RUN enable circuits. | X01 |
| 10 | 8, 28 | 2008/12/15 | Wistron | Thermal sensor order changed because DTS still have accuracy problem. | Change EMC2102 first channel to CPU internal diode. Change channel to GPU inernal diode. | X01 |
| 11 | 15 | 2008/12/15 | Wistron | Cantiga power rating issue. | Add R1507. | X01 |
| 12 | 26, 54 | 2008/12/15 | Wistron | AMD CTF glitch issue. | Reserve KBC GPIO27, Add R2639. | X01 |
| 13 | 40 | 2008/12/15 | Wistron | Add panel self test for factory. | Add D4002, Pop R2638. | X01 |
| 14 | 32 | 2008/12/15 | Wistron | Prevent leakage from KBC. | Change PR3203 pull high from +3.3V_ALW to +3.3V_RTC_LDO. | X01 |
| 15 | 44, 52 51, 47 | 2008/12/15 | Wistron | Modify based on EMI test result. | POP EC5203 C5212 EC5202 C5211 C5213 EC5206 EC5201 EC5208 and POP EC4701 EC4702 EC4401 EC4402 EC4403 EC4404 EC5101 with 22P-Varistor | X01 |
| 16 | 41 | 2008/12/18 | Wistron | LCD power sequence issue. | Change +LCD_VDD power produce solution. | X01 |
| 17 | 41 | 2008/12/19 | Wistron | CMO LCD white screen issue. | Add R4108 (DY). | X01 |
| 18 | 46, 51 | 2008/12/19 | Wistron | Add ESD diode for USB Port. | Add D4601, D4602, D5101. | X01 |
| 19 | 39 | 2008/12/29 | Wistron | GFX CORE glitch issue. | Add PD3902, PD3903, PR3910, PR3915. Change PC3915, PC3916 to 0.047uF. | X01 |
| 20 | 50 | 2008/12/29 | Wistron | Follow ME connector list for Express card board. | Change CON2 to 20.F1400.050. | X01 |

<Core Design>

| | | | |
|---|---|---|------------------|
|  | | Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | |
| Title Change List | | | |
| Size A3 | Document Number Alba Discrete | Date: Monday, March 23, 2009 | Rev SB |
| Date: Monday, March 23, 2009 | | Sheet 59 | of 60 |

| Item | Page# | Date | Request By | Issue description | Solution Description | Rev. |
|------|-----------------|------------|------------|---|---|------|
| 21 | 9 | 2009/01/06 | Wistron | Power team request for CPU core measurement. | Add PG901,PG902. Pop C901 and depot C902. | X01 |
| 22 | 26 | 2009/01/08 | Wistron | Keyboard detect issue. | Pop R2625. | X01 |
| 23 | 44,51 | 2009/01/08 | Wistron | Change new connector. | Change HDD1 and CON5. | X01 |
| 24 | 8 | 2009/01/12 | Wistron | For better GTL reference voltage. | Pop C802. | X01 |
| 25 | 30,36 37,38 | 2009/01/12 | Wistron | Add discharge circuit for GPU powers. | Add R3016,Q3006,R3015,Q3003,Q3702,R3702 R3703,D3802,R3802,C3802. | X01 |
| 26 | 22,26 | 2009/01/13 | IDT | For pop noise on YC version codec. | Add Q2201,Q2202,R2219. Add GPIO33 for HP_MUTE. | X01 |
| 27 | 33 | 2009/01/13 | Wistron | For +15V_ALW issue. Prevent higher than 20V. | Add PD3303,PC3301. | X01 |
| 28 | 51 | 2009/01/30 | Wistron | ESD protection concern. | Change R5106 to 33ohm. | X01 |
| 29 | 39 | 2009/01/30 | Wistron | For GFX_CORE overshoot and undershoot issue. | Pop R3921,R3922. Depop R3920,R3923. | X01 |
| 30 | 18,26 | 2009/02/19 | Wistron | Prevent 32768Hz crystal no oscillation from flux. | Change C1807,C1806,C2607,C2608 to 0603 size. | X02 |
| 31 | 22 | 2009/02/26 | IDT | For codec pop noise issue. | Change C2204 to 2.2uf. Add Q2201,Q2202,Q2203, Q2204,Q2205. Move R2218,R2220 to main board. | X02 |
| 32 | 26 | 2009/02/26 | Wistron | Change Board ID and add VRAM type select pin. | Change board ID to 010,Add GPIO5 for VRAM type | X02 |
| 33 | 30 | 2009/03/02 | Wistron | +3.3V_ALW drop issue. | Add C3005. | X02 |
| 34 | 31,42, 44,45 | 2009/02/19 | Wistron | Connector change request by ME. | Change RJ45,DCIN,FAN,SPEAKER connectors. | X02 |
| 35 | 41 | 2009/02/19 | Wistron | LCD white screen issue. | Pop R4108. | X02 |
| 36 | 31,32 | 2009/03/02 | Wistron | Power team request. | Change PD3107 to 1SMB22AT3G. Change PC3208, PC3209 to X7R. | X02 |
| 37 | 52 | 2009/03/05 | Wistron | Reserve capacitors and springs for EMI. | Add location for SPR5206~SPR5209 and EC5210~EC5213. | X02 |
| 38 | 26 | 2009/03/09 | Wistron | No need to support keyboard detect function. | Depop R2625. | X02 |
| 39 | 22 | 2009/03/09 | Wistron | For PC_BEEP sound volume issue. | Modify R2203 to 120Kohm. | X02 |
| 40 | 33 | 2009/03/10 | Wistron | +15V_ALW issue. | Depop PD3303. | X02 |

<Core Design>

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|---|---|--|--|
|  | | Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | |
| | | Change List | |
| Title _____ | Document Number Alba Discrete | Rev SB | |
| Date: Monday, March 23, 2009 | Sheet 60 of 60 | | |