ASUS CONFIDENTIAL

MODEL NAME : ***Elsa***

PCB NO : ***???***

ASUS P/N : ***???***

Lanai Discrete VGA nVidia NB8M Schematics Document

uFCPGA Mobile Merom
Intel Crestline-PM + ICH8M

2007-03-19

REV : 1.2(DELL: X02)

MB PCB

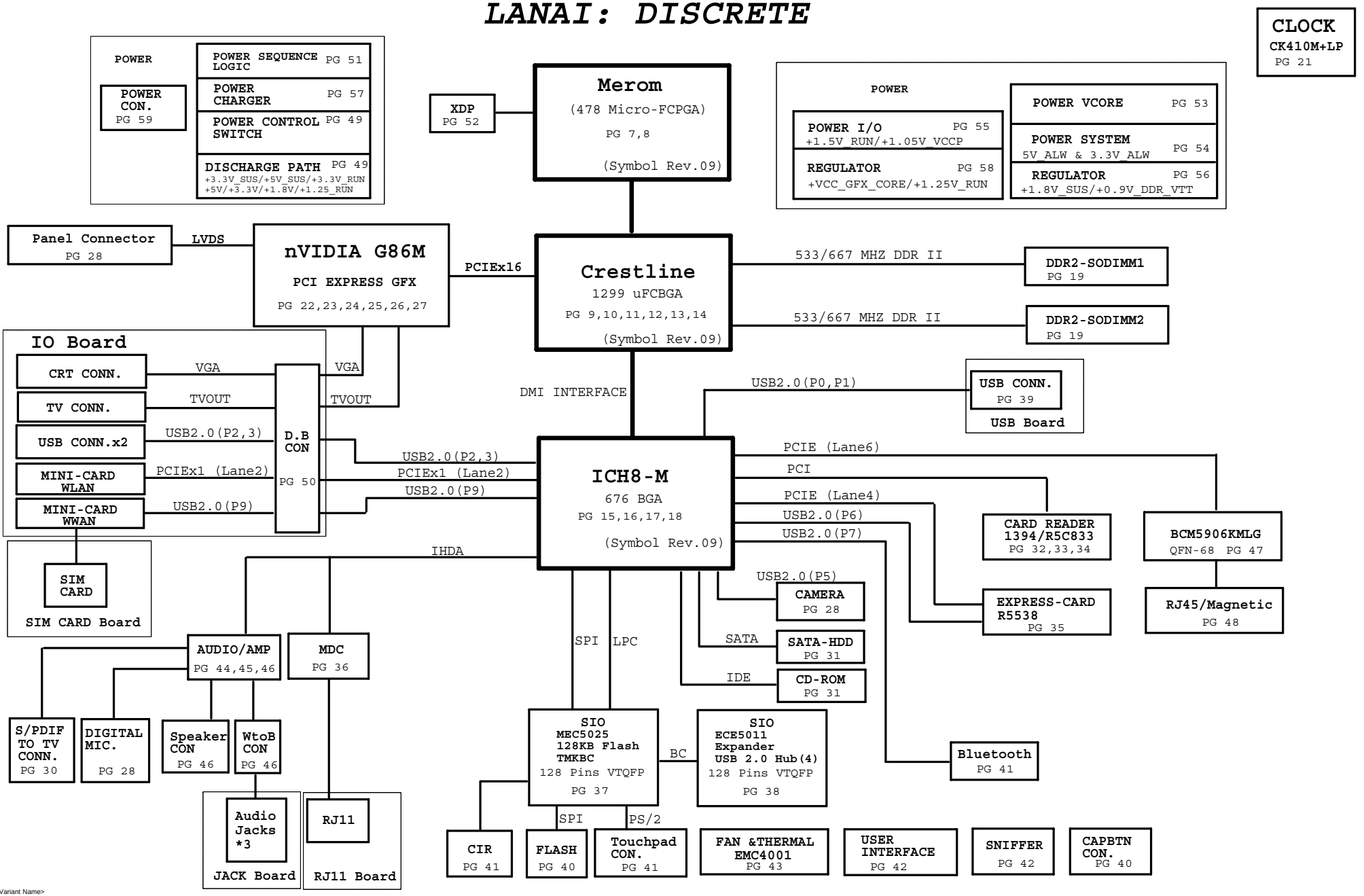
Part Number	Description
DA800004H0L	PCB 00B LA-3071P REV0 M/B

BOM NO. ???
PCB P/N: ???

<Variant Name>

PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007** SHEET **1** OF **69**	DESCRIPTION: ***Cover Page***	SCHEMATIC FILE NAME : RELEASE DATE :	DESIGN ENGINEER : ***Terry Lin***

LANAI: DISCRETE



<Variant Name>

PROJECT: **Lanai**	REVISION: **1.2**	DATE: Monday, March 19, 2007	DESCRIPTION: ***BLOCK DIAGRAM***	SCHEMATIC FILE NAME :
		SHEET 2 OF 69		RELEASE DATE :
				DESIGN ENGINEER : ***STANLY_HSU***

INDEX

Pg#	Description	DNI LIST
01	Cover Page	
02	Schematic Block Diagram	
03	INDEX	
04	Bus connection	
05	SMBUS BLOCK	
06	Power Rail	
07-08	CPU (Merom 、 Penryn)	
09-14	Crestline	
15-18	ICH8M	
19-20	DDRII SO-DIMM(533MHz 、 667MHz)	
21	Clock Generator (CK410M+LP)	
22-27	VGA (nVIADA - G86M & GDDR3)	
28	LVDS CON & Camera & DMIC	
29	RGB CON	
30	TV OUT CON	
31	SATA(HDD & CD_ROM)	
32-34	MEDIA CARD READER / 1394 (R5C833)	
35	PCI-Express Card	
36	MDC CONN	
37	EC (MEC5025)	
38	SIO (ECE5011)	
39	USB PORT x 2	
40	FLASH & RTC & CAPBTN CONN	
41	TOUCH PAD & BT & CIR & LID	
42	SWITCH & LED	
43	HARDWARE MONITOR (EMC4001)	
44-46	AUDIO CODEC & AMP	
47	LOM BCM5906	
48	Magnetics and RJ-45	
49	Power Control Switch	
50	BtoB CON	
51	Power Sequence Logic	
52	XDP	
53-59	Power Circuit	
60	SCREW PAD	
61	Change list (1)	
62	Change list (2)	
63	Change list (3)	

Pg#	Description	DNI LIST
64	Power circuit Change list	
R01	Modem board cover page	
R02	RJ-11 CONN	
R03	Modem board Change list	
U01	USB board cover page	
U02	USB PORT (SINGLE * 2)	

<Variant Name>

PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***INDEX***	SCHEMATIC FILE NAME :	DESIGN ENGINEER : ***Terry_Lin***
		SHEET **3** OF **69**		RELEASE DATE :	

Footprint Definition

Resistor	Footprint is 0402 if there is no description
Capacitor	Footprint is 0402 if there is no description
Ferrite Bead	Footprint is 0603 if there is no description

Layout Note

For all of ESD diode, they should be placed as close as possible to connectors and the signals from connectors should be routed to ESD diodes first. There is no branch or via before diodes

PCI TABLE

PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
R5C833	PCI_AD17	PCI_REQ1# PCI_GNT1#	PCI_PIRQC# PCI_PIRQD#

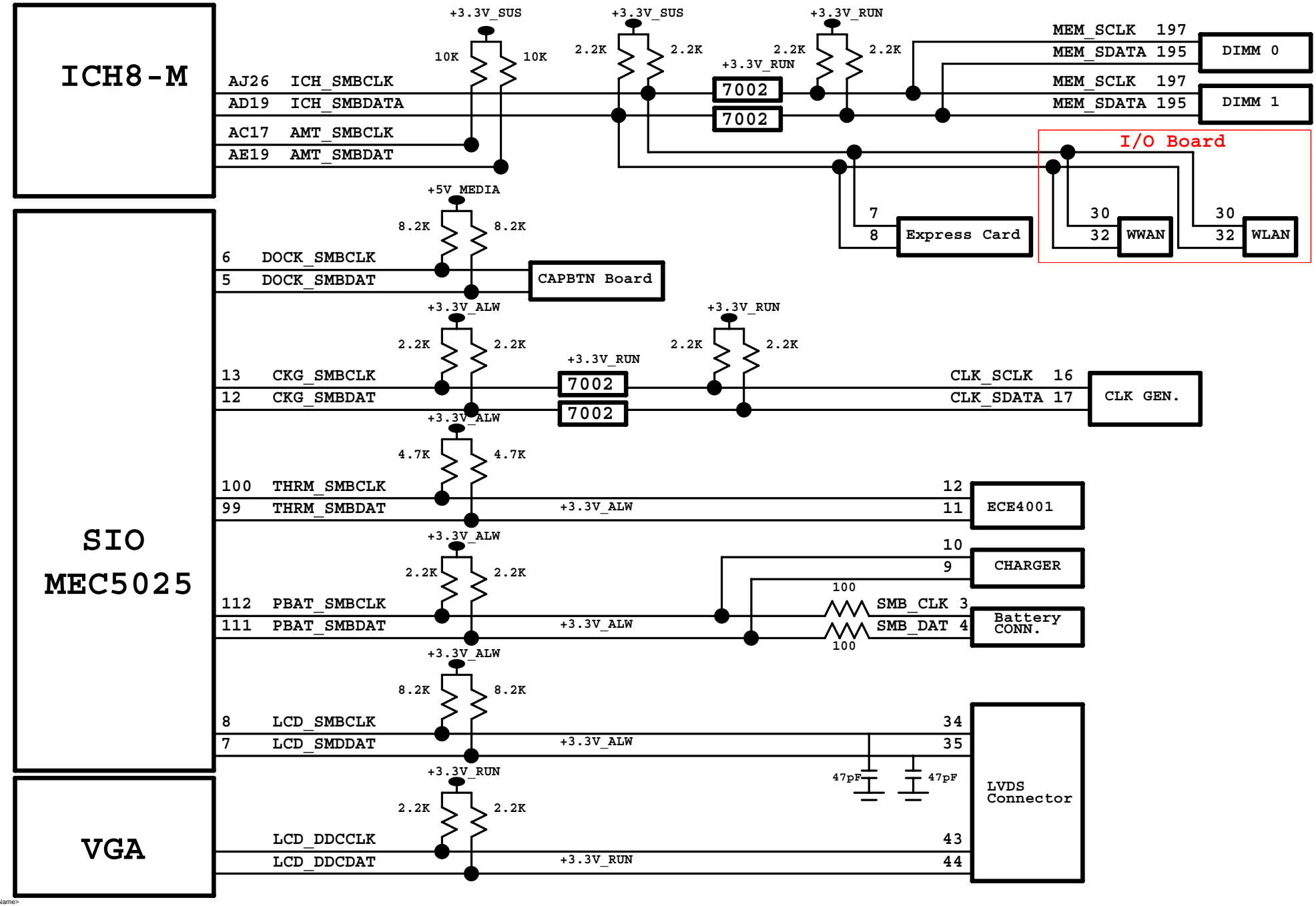
PCI Express TABLE

Lane 1	WWAN / Mini Card
Lane 2	WLAN / Mini Card
Lane 3	
Lane 4	ExpressCard
Lane 5	
Lane 6	LAN BCM5906KMLG

USB TABLE

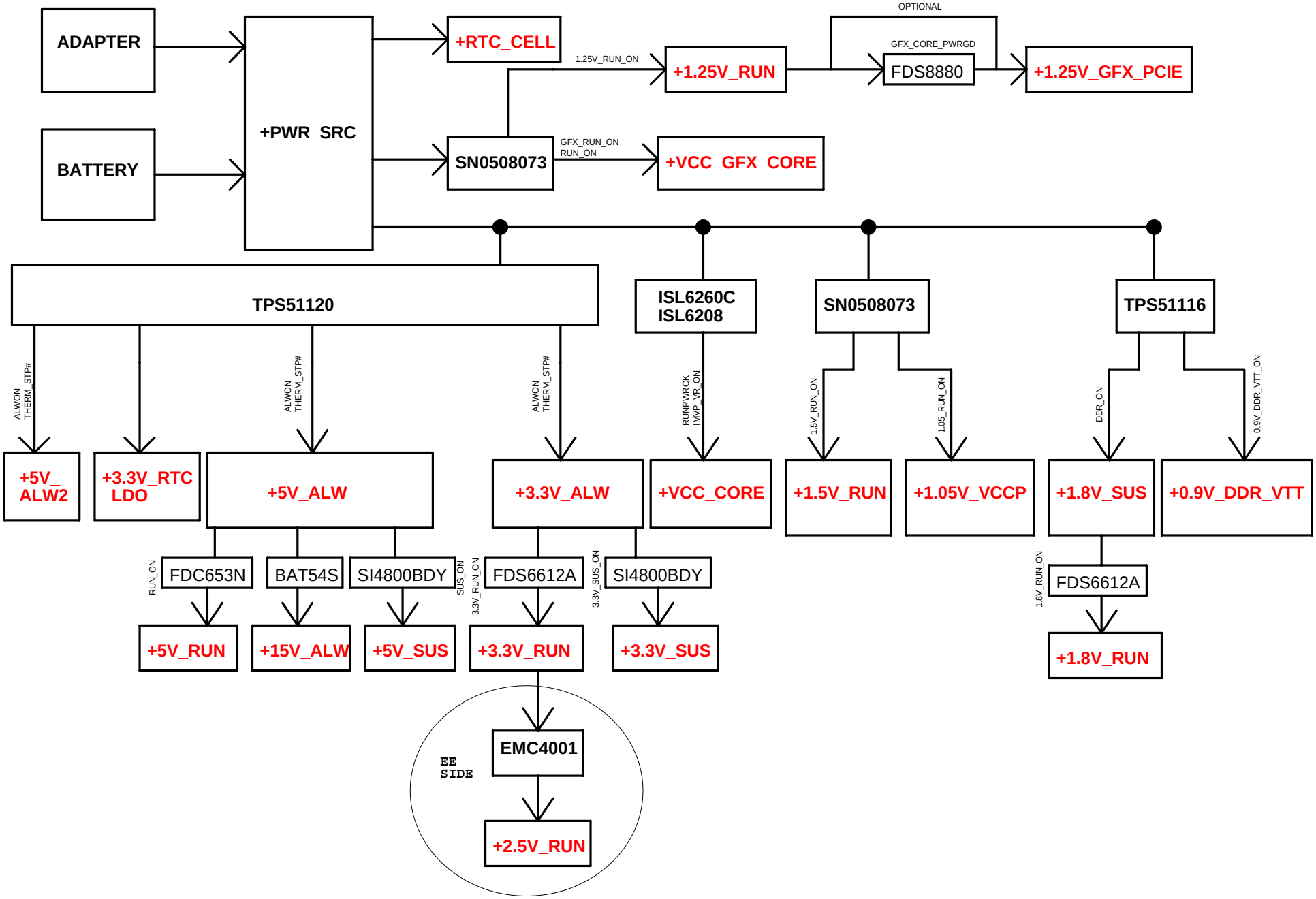
ICH8-0 (EHCI#1)	User1 (Single port , in USB BD)
ICH8-1 (EHCI#1)	User2 (Single port , in USB BD)
ICH8-2 (EHCI#1)	User3 (Dual port-bottom , in I/O BD)
ICH8-3 (EHCI#1)	User4 (Dual port-top , in I/O BD)
ICH8-4 (EHCI#1)	
ICH8-5 (EHCI#1)	Camera
ICH8-6 (EHCI#2)	ExpressCard
ICH8-7 (EHCI#2)	BT Module
ICH8-8 (EHCI#2)	
ICH8-9 (EHCI#2)	WWAN / Mini Card

Note : No USB for WLAN



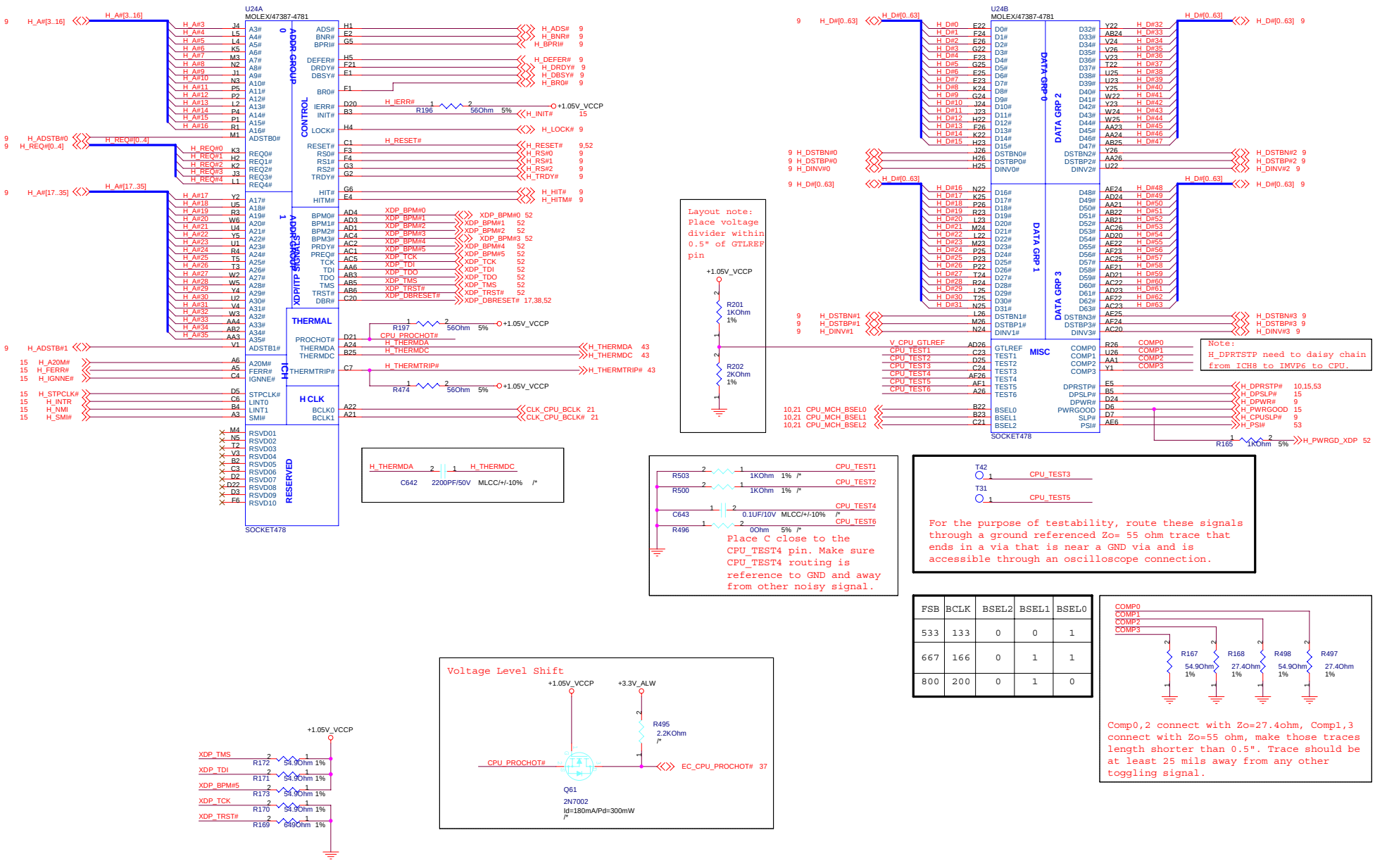
<Variant Name>

PROJECT: **Lanai**	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: *SMBUS BLOCK*	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER : *Terry_Lin*
		SHEET 5 OF 69		RELEASE DATE :	



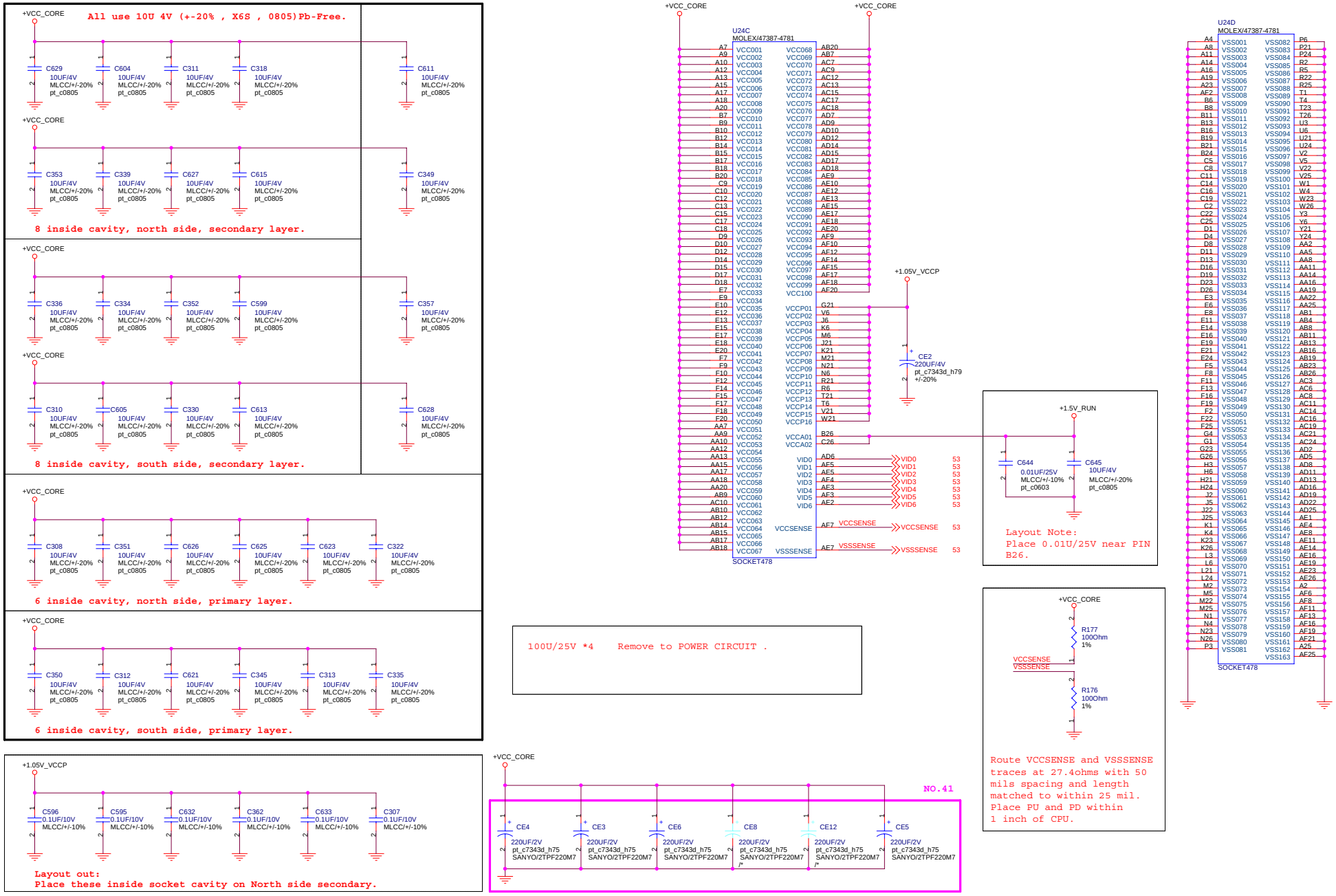
<Variant Name>

PROJECT: **Lanai**	REVISION: 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: *Power Rail*	SCHEMATIC FILE NAME :	DESIGN ENGINEER : *Eric_Ko*
		SHEET 6 OF 69		RELEASE DATE :	



<Variant Name>

PROJECT: **Lanai**	REVISION: **1.2**	DATE: Monday, March 19, 2007	SHEET 7 OF 69	DESCRIPTION: *MEROM CPU (1)*	SCHEMATIC FILE NAME: <OrgName>	DESIGN ENGINEER: *Terry_Lin*
					RELEASE DATE:	



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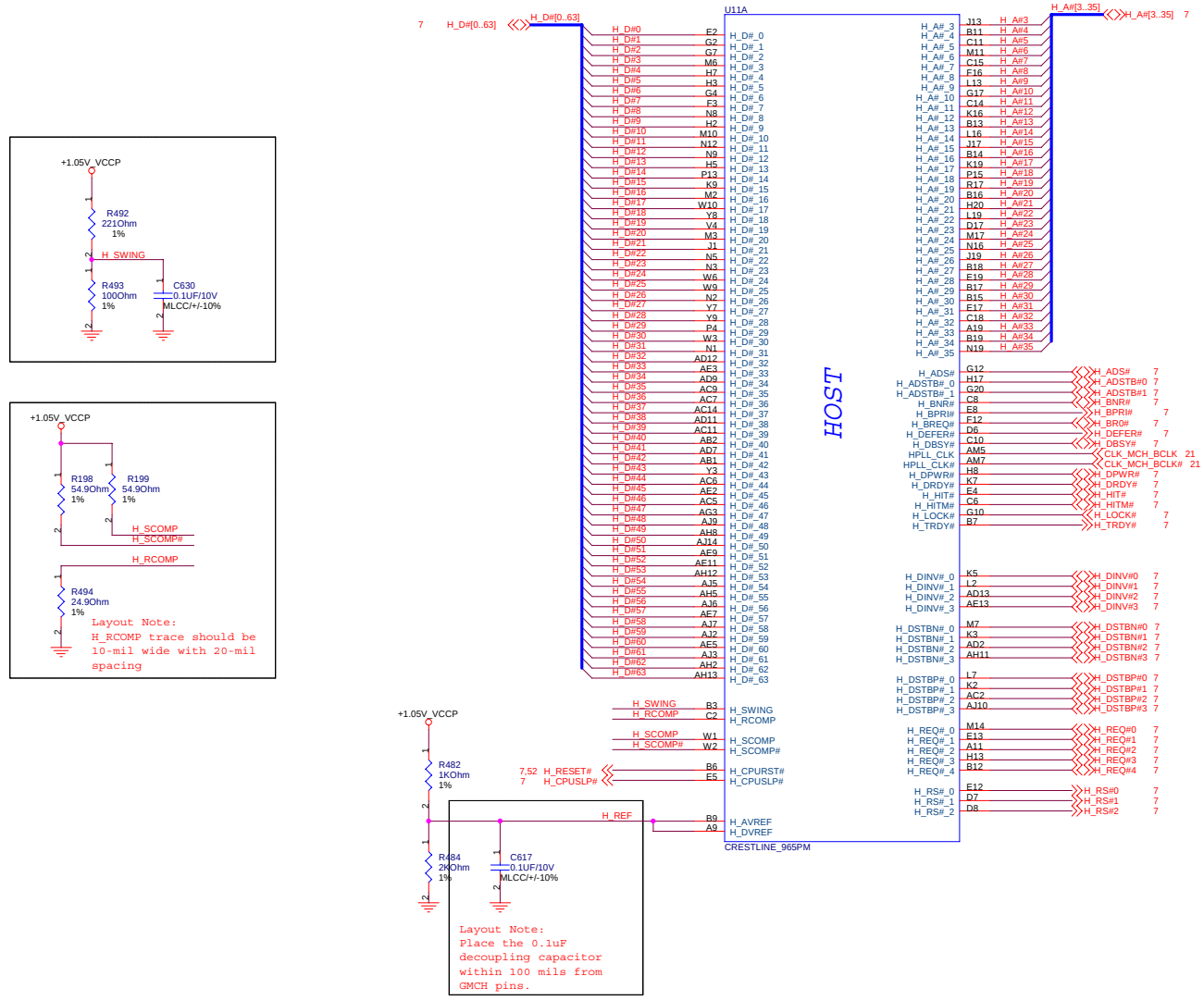
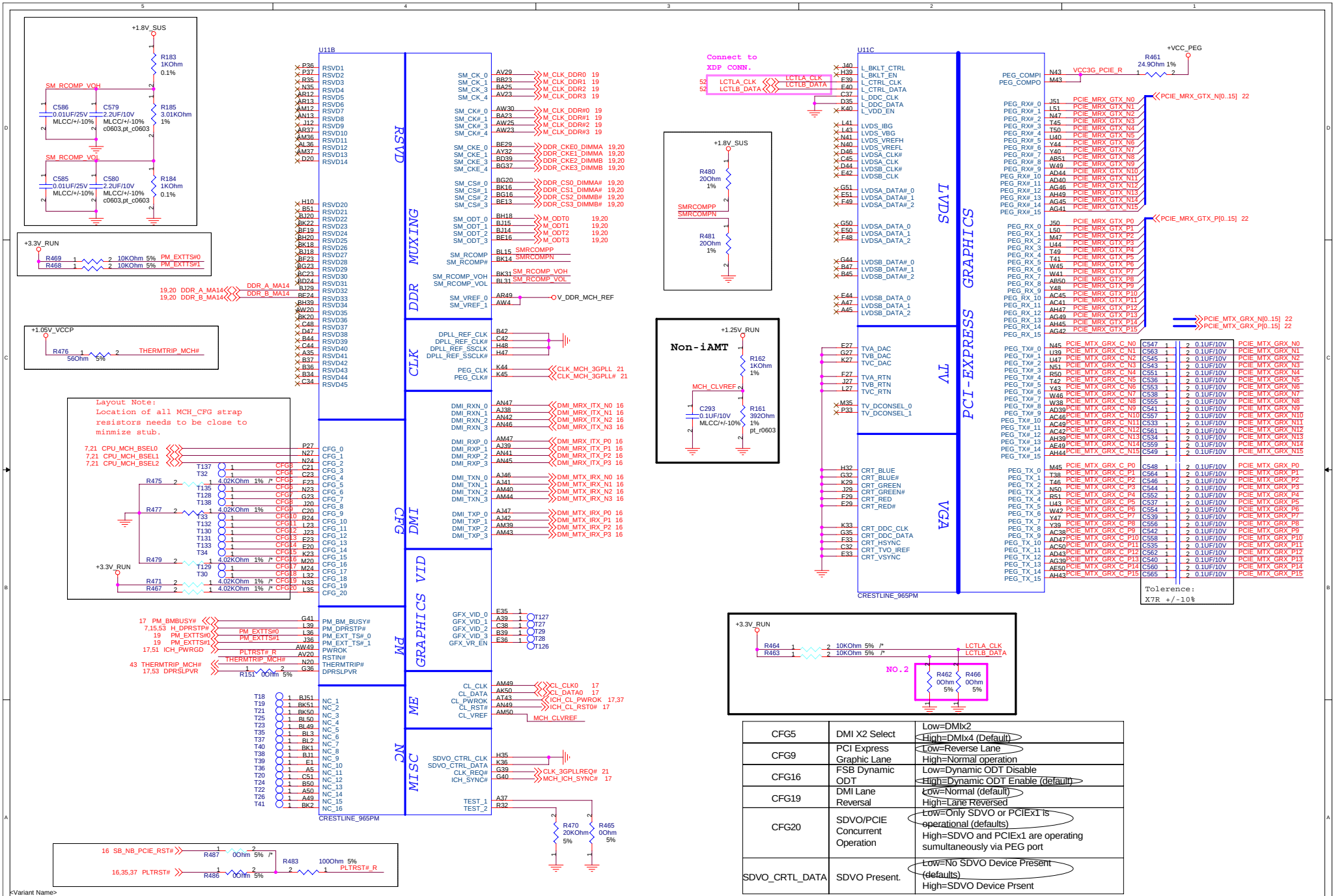
PROJECT: **Lanai**	REVISION: 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: *Merom CPU (2)*	SCHEMATIC FILE NAME: <OrgName>	DESIGN ENGINEER: *Terry_Lin*
		SHEET 8 OF 69		RELEASE DATE:	

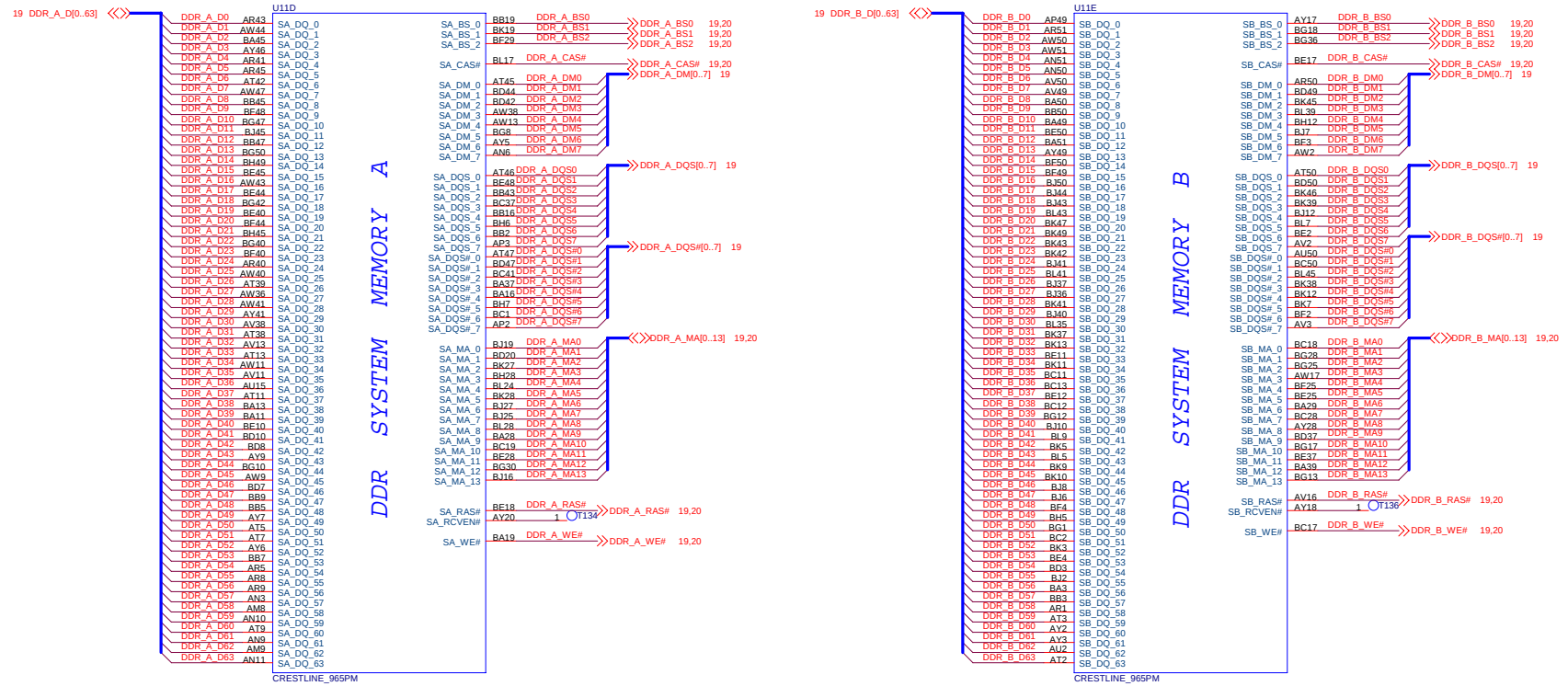


<Variant Name>

PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***Crestline(HOST)***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : ***Ivan_Chou***	
		SHEET **9** OF **69**		RELEASE DATE :		

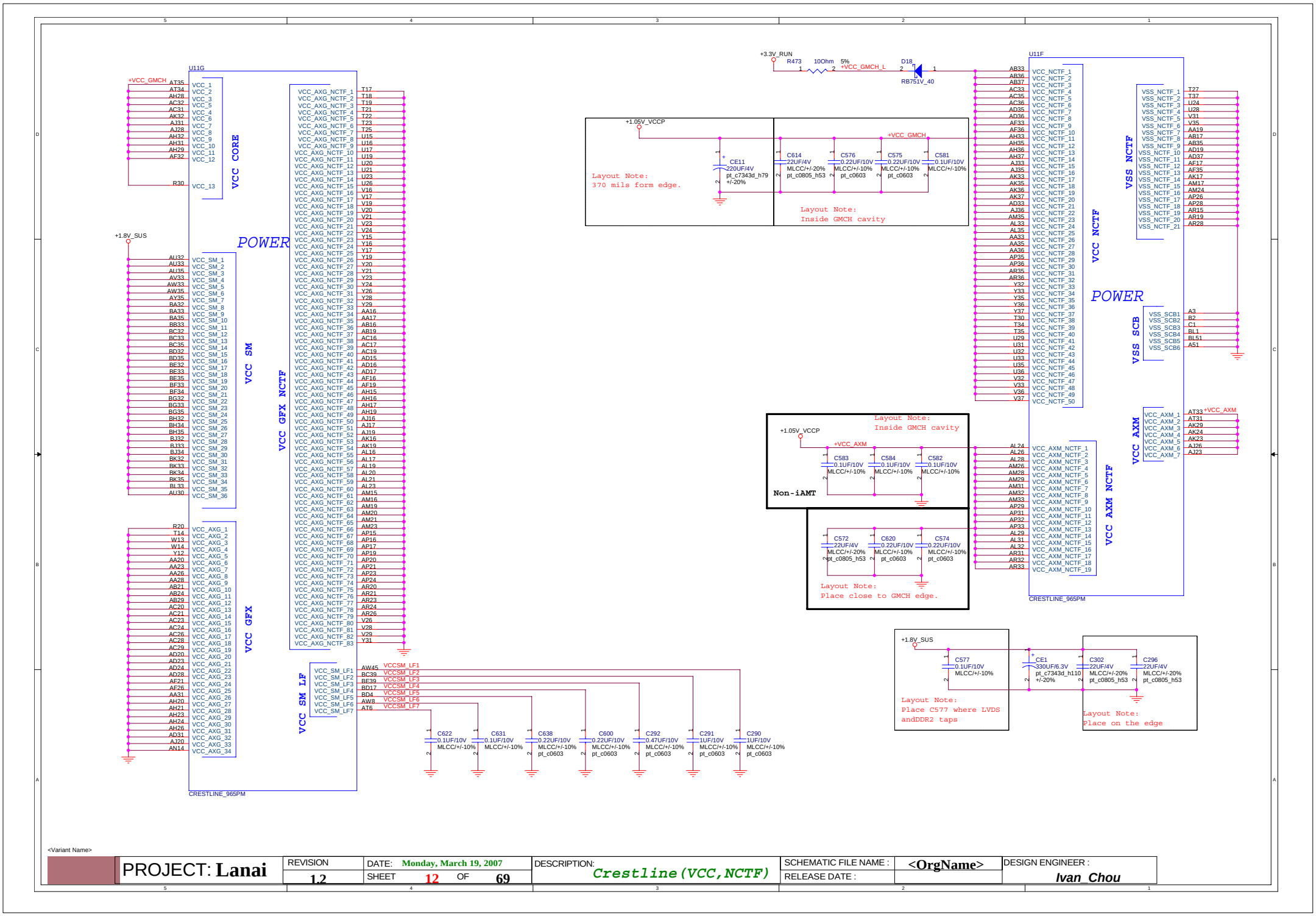


CFG5	DMI X2 Select	Low=DMIx2 High=DMIx4 (Default)
CFG9	PCI Express Graphic Lane	Low=Reverse Lane High=Normal operation
CFG16	FSB Dynamic ODT	Low=Dynamic ODT Disable High=Dynamic ODT Enable (default)
CFG19	DMI Lane Reversal	Low=Normal (default) High=Lane Reversed
CFG20	SDVO/PCIE Concurrent Operation	Low=Only SDVO or PCIEx1 is operational (defaults) High=SDVO and PCIEx1 are operating sumultaneously via PEG port
SDVO_CRTL_DATA	SDVO Present.	Low=No SDVO Device Present (defaults) High=SDVO Device Prsent



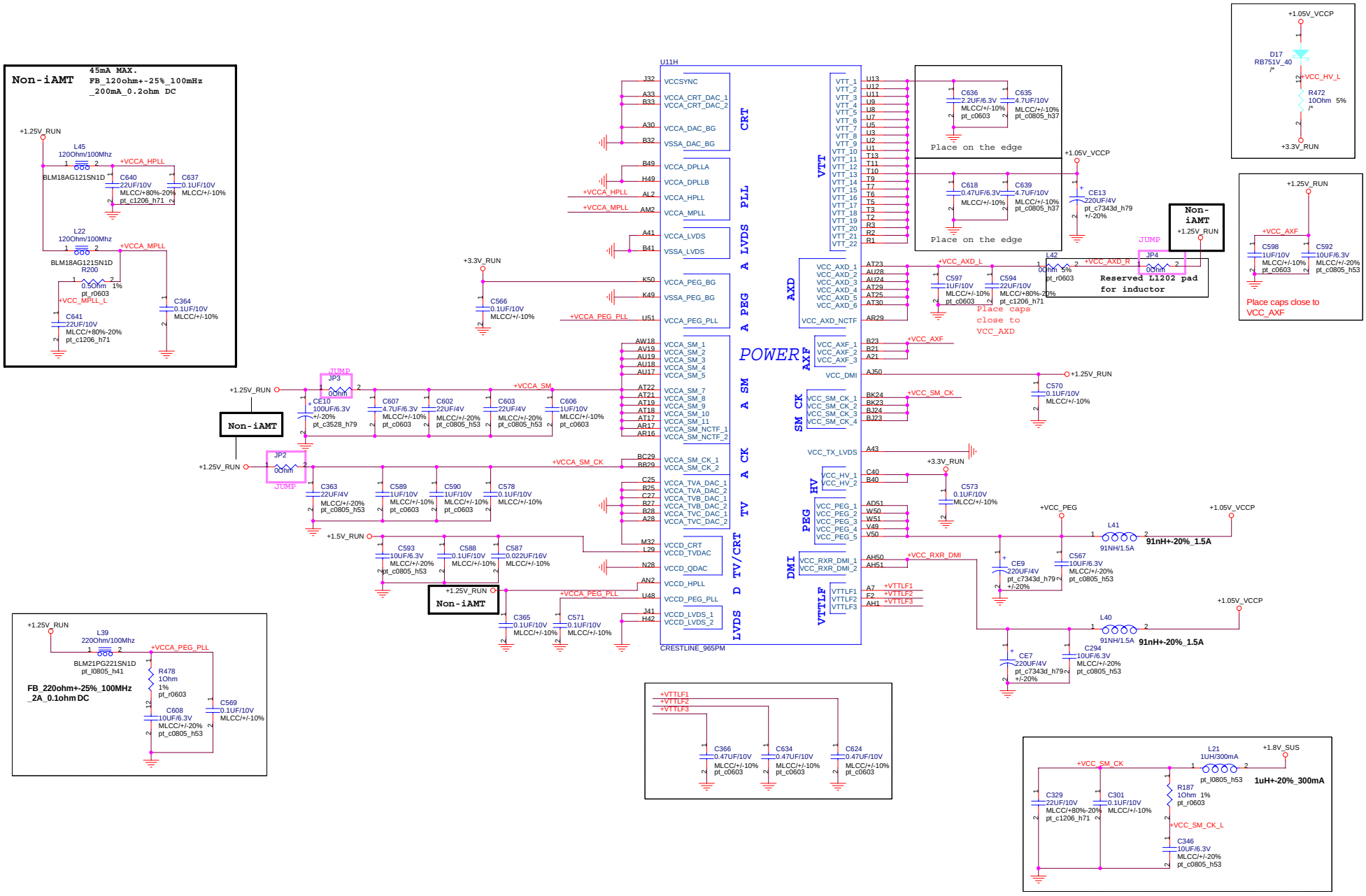
<Variant Name>

PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***Crestline(DDR2)***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : ***Ivan_Chou***
		SHEET **11** OF **69**		RELEASE DATE :	



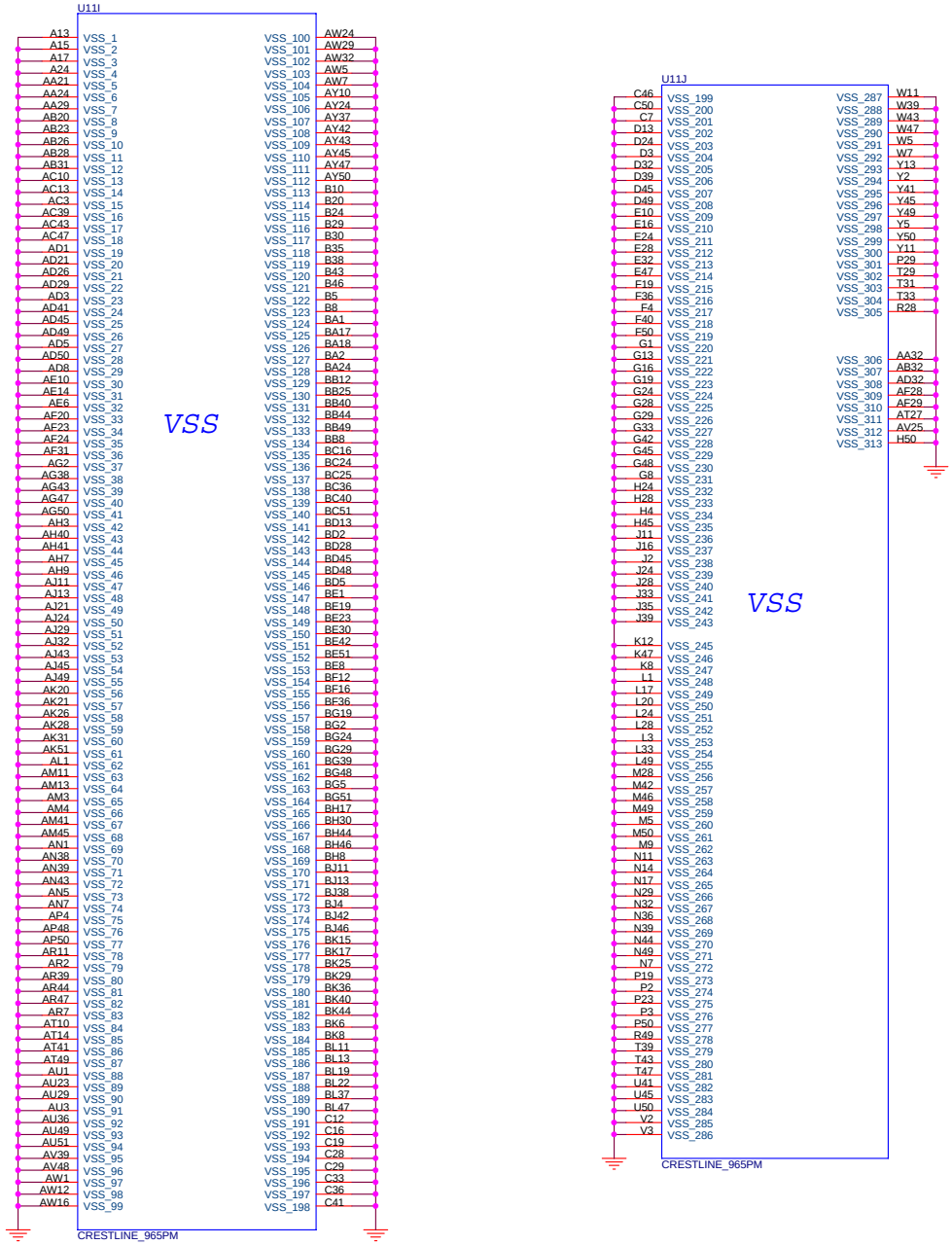
<Variant Name>

PROJECT: **Lanai**	REVISION: 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: *Crestline(VCC,NCTF)*	SCHEMATIC FILE NAME: <OrgName>	DESIGN ENGINEER: *Ivan_Chou*
		SHEET 12 OF 69		RELEASE DATE:	



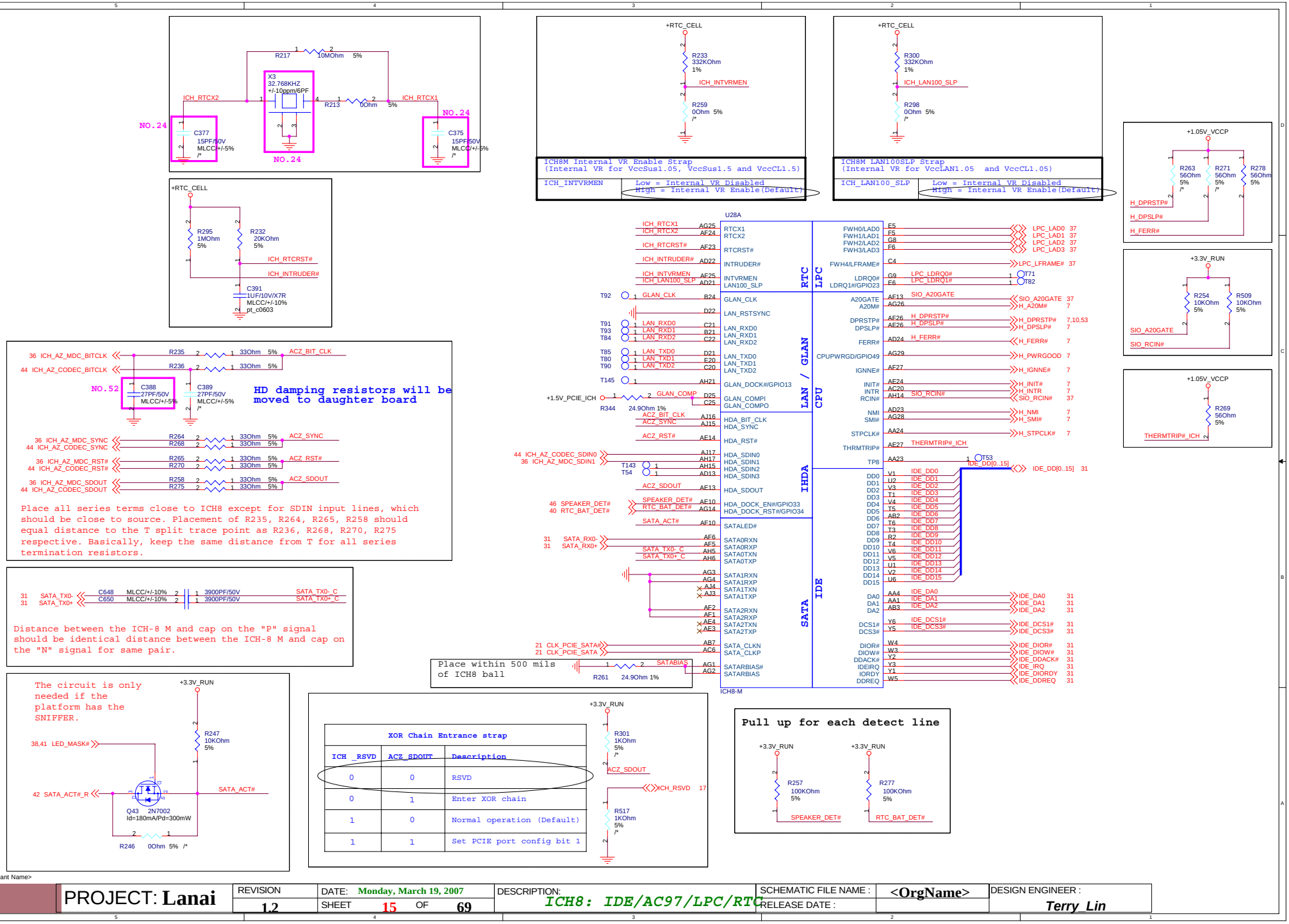
<Variant Name>

PROJECT: **Lanai**	REVISION: **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***Crestline(POWER)***	SCHEMATIC FILE NAME: **<OrgName>**	DESIGN ENGINEER: ***Ivan_Chou***
		SHEET **13** OF **69**		RELEASE DATE:	



<Variant Name>

PROJECT: **Lanai**	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: Crestline(VSS)	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER : Ivan_Chou
		SHEET 14 OF 69		RELEASE DATE :	



<Variant Name>

PROJECT: **Lanai**	REVISION: 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: *ICH8: IDE/AC97/LPC/RTC*	SCHEMATIC FILE NAME: <OrgName>	DESIGN ENGINEER: *Terry_Lin*
		SHEET 15 OF 69		RELEASE DATE:	

Place TX DC blocking caps close ICH8.

50 PCIE_TX1- C434 0.1UF/10V MLCC/+/-10% PCIE_TXN1_C
50 PCIE_TX1+ C436 0.1UF/10V MLCC/+/-10% PCIE_TXP1_C
50 PCIE_TX2- C443 0.1UF/10V MLCC/+/-10% PCIE_TXN2_C
50 PCIE_TX2+ C439 0.1UF/10V MLCC/+/-10% PCIE_TXP2_C
35 PCIE_TX4- C458 0.1UF/10V MLCC/+/-10% PCIE_TXN4_C
35 PCIE_TX4+ C461 0.1UF/10V MLCC/+/-10% PCIE_TXP4_C
47 PCIE_TX6-/GLAN_TX- C714 0.1UF/10V MLCC/+/-10% GLAN_TXN_C
47 PCIE_TX6+/GLAN_TX+ C713 0.1UF/10V MLCC/+/-10% GLAN_TXP_C

U28D

50 PCIE_RX1- P27 PERN1
50 PCIE_RX1+ P26 PERP1
MiniWWAN PCIE_TXN1_C N29 PETN1
PCIE_TXP1_C N28 PETP1
50 PCIE_RX2- M27 PERN2
50 PCIE_RX2+ M26 PERP2
MiniWLAN PCIE_TXN2_C L29 PETN2
PCIE_TXP2_C L28 PETP2
K27 PERN3
K26 PERP3
J29 PETN3
J28 PETP3
35 PCIE_RX4- H27 PERN4
35 PCIE_RX4+ H26 PERP4
ExpressCard PCIE_TXN4_C G29 PETN4
PCIE_TXP4_C G28 PETP4
F27 PERN5
F26 PERP5
E29 PETN5
E28 PETP5
47 PCIE_RX6-/GLAN_RX- D27 PERN6/GLAN_RXN
47 PCIE_RX6+/GLAN_RX+ D26 PERP6/GLAN_RXP
GLAN_TXN_C C29 PETN6/GLAN_TXN
GLAN_TXP_C C28 PETP6/GLAN_TXP

PCI-Express
Direct Media Interface

DMI0RXN V27 DMI_MTX_IRX_N0 10
DMI0RXP V26 DMI_MTX_IRX_P0 10
DMI0TXN U29 DMI_MRX_ITX_N0 10
DMI0TXP U28 DMI_MRX_ITX_P0 10
DMI1RXN Y27 DMI_MTX_IRX_N1 10
DMI1RXP Y26 DMI_MTX_IRX_P1 10
DMI1TXN W29 DMI_MRX_ITX_N1 10
DMI1TXP W28 DMI_MRX_ITX_P1 10
DMI2RXN AB26 DMI_MTX_IRX_N2 10
DMI2RXP AB25 DMI_MTX_IRX_P2 10
DMI2TXN AA29 DMI_MRX_ITX_N2 10
DMI2TXP AA28 DMI_MRX_ITX_P2 10
DMI3RXN AD27 DMI_MTX_IRX_N3 10
DMI3RXP AD26 DMI_MTX_IRX_P3 10
DMI3TXN AC29 DMI_MRX_ITX_N3 10
DMI3TXP AC28 DMI_MRX_ITX_P3 10
DMI_CLKN T26 CLK_PCIE_ICH# 21
DMI_CLKP T25 CLK_PCIE_ICH 21
DMI_ZCOMP Y23
DMI_IRCOMP Y24 DMI_COMP R286 24.9Ohm 1% +1.5V_PCIE_ICH

Place within 500 mils of ICH8

BIOS should not enable the internal GPIO pull up resistor

+3.3V_RUN
SB_NB_PCIE_RST# R338 10KOhm 5%
SB_WLAN_PCIE_RST# R147 10KOhm 5%
SB_NB_PCIE_RST# R491 100KOhm 5%
SB_WLAN_PCIE_RST# R334 100KOhm 5%
SB_LOM_PCIE_RST# R354 20KOhm 5%
SB_WWAN_PCIE_RST# R356 20KOhm 5%

Layout Note:
Place 15 ohm within
500 mils from ICH.

37 ICH_EC_SPI_CLK R353 15Ohm 5% ICH_EC_SPI_CLK_R C23 ICH_SPI_CS#
T78 B23 ICH_SPI_CS1#_R E22
37 ICH_EC_SPI_DO R343 15Ohm 5% ICH_EC_SPI_DO_R D23 SPI_MOSI
37 ICH_EC_SPI_DIN F21 SPI_MISO
SPI_CLK
SPI_CS0#
SPI_CS1#

SPI

USB

USBP0N G3 ICH_USBP0- 39 USER1 Left side pair top/left
USBP0P G2 ICH_USBP0+ 39
USBP1N H5 ICH_USBP1- 39 USER2 Left side pair bottom/right
USBP1P H4 ICH_USBP1+ 39
USBP2N H2 ICH_USBP2- 50 USER3 Right side pair top/left
USBP2P H1 ICH_USBP2+ 50
USBP3N J3 ICH_USBP3- 50 USER3 Right side pair bottom/right
USBP3P J2 ICH_USBP3+ 50
USBP4N K5 ICH_USBP4- T63
USBP4P K4 ICH_USBP4+ T68
USBP5N K2 ICH_USBP5- 28 CCD
USBP5P K1 ICH_USBP5+ 28
USBP6N L3 ICH_USBP6- 35 Express Card
USBP6P L2 ICH_USBP6+ 35
USBP7N M5 ICH_USBP7- 41 BlueTooth NO.5
USBP7P M4 ICH_USBP7+ 41
USBP8N M2 ICH_USBP8- T59
USBP8P M1 ICH_USBP8+ T62
USBP9N N3 ICH_USBP9- 50 WWAN
USBP9P N2 ICH_USBP9+ 50
USBRBIAS# F2
USBRBIAS F3 USBRBIAS

39 USB_OC0_1# USB_OC0_1# A19
50 USB_OC2_3# USB_OC2_3# AG16
AG15
AE15
OC4# AE15
OC5# AG17
OC6# AD12
OC7# AJ18
OC8# AD14
OC9# AH18
OC0#
OC1#/GPIO40
OC2#/GPIO41
OC3#/GPIO42
OC4#/GPIO43
OC5#/GPIO29
OC6#/GPIO30
OC7#/GPIO31
OC8#
OC9#

ICH8-M

Short F2 and F3 at the package and keep length to less than 500mils. Trace Impedance should be 60ohms +/- 15%.

R561 22.6Ohm 1% pt_r0603

PCI Pullups

PCI_STOP# R350 8.2KOhm 5% +3.3V_RUN
PCIE_MCARD2_DET# R613 100KOhm 5% +3.3V_RUN NO.13
PCI_DEVSEL# RP4E 8.2KOhm 5% +3.3V_RUN
PCI_FRAME# RP4F 8.2KOhm 5% RP4D PCI_REQ1#
ICH_GPIO2_PIRQE# RP4G 8.2KOhm 5% RP4C PCI_PIRQD#
PCI_SERR# RP4H 8.2KOhm 5% RP4B
RP4A PCI_TRDY#
PCI_REQ0# RP3E 8.2KOhm 5% +3.3V_RUN
PCI_PLOCK# RP3F 8.2KOhm 5% RP3D PCI_PIRQC#
PCI_PERR# RP3G 8.2KOhm 5% RP3C PCI_PIRQB#
RP3H 8.2KOhm 5% RP3B PCI_PIRQA#
RP3A PCI_IRDY#

+3.3V_ALW
U33
SPI_CS0# R595 15Ohm 5% /*
R596 15Ohm 5% ICH_SPI_CS# SIO_SPI_CS# 37
74AHC1G08GW /*
R594 0Ohm 5%

Non-iAMT

+3.3V_SUS
OC4# RP1E 10KOhm 5%
OC7# RP1F 10KOhm 5% RP1D USB_OC2_3#
OC6# RP1G 10KOhm 5% RP1C OC8#
OC9# RP1H 10KOhm 5% RP1B OC5#
RP1A USB_OC0_1#

ICH_SPI_CS1#_R
PCI_GNT0#
R347 1KOhm 5% /*
R337 1KOhm 5% /*

Boot BIOS Strap

		GNT0#	SPI_CS1#
LPC	11	No stuff	No stuff
PCI	10	No stuff	Stuff
SPI	01	Stuff	No stuff

PCI_GNT3#
R346 1KOhm 5% /*

A16 away override strap.

PCI_GNT3#	Low = A16 swap override enabled.
	High = Default.

Non-iAMT

Add Buffers as needed for Loading and fanout concerns.

+3.3V_SUS
C689 0.047UF/10V MLCC/+/-10%
U30 SN74AHC1G32DBVR
PCI_RST#_G PCI_RST# 32
C382 0.047UF/10V MLCC/+/-10%
U14 SN74AHC1G32DBVR
PCI_PLTRST# PLTRST# 10,35,37
NO.36
C747 0.047UF/10V MLCC/+/-10%
U37 SN74AHC1G32DBVR
PCI_PLTRST# PLTRST_LAN_MINICARD# 47,50
C758 47PF/50V MLCC/+/-5%
NO.51

32 PCI_AD[0..31]

U28B

PCI_AD0 D20 AD0
PCI_AD1 E19 AD1
PCI_AD2 D19 AD2
PCI_AD3 A20 AD3
PCI_AD4 D17 AD4
PCI_AD5 A21 AD5
PCI_AD6 A19 AD6
PCI_AD7 C19 AD7
PCI_AD8 A18 AD8
PCI_AD9 B16 AD9
PCI_AD10 A12 AD10
PCI_AD11 E16 AD11
PCI_AD12 A14 AD12
PCI_AD13 G16 AD13
PCI_AD14 A15 AD14
PCI_AD15 B6 AD15
PCI_AD16 C11 AD16
PCI_AD17 A9 AD17
PCI_AD18 D11 AD18
PCI_AD19 B12 AD19
PCI_AD20 C12 AD20
PCI_AD21 D10 AD21
PCI_AD22 C7 AD22
PCI_AD23 F13 AD23
PCI_AD24 E11 AD24
PCI_AD25 E13 AD25
PCI_AD26 E12 AD26
PCI_AD27 D8 AD27
PCI_AD28 A6 AD28
PCI_AD29 E8 AD29
PCI_AD30 D6 AD30
PCI_AD31 A3 AD31

PCI

REQ0# A4 PCI_REQ0#
GNT0# D7 PCI_GNT0#
REQ1#/GPIO50 E18 PCI_REQ1# PCI_REQ0#
GNT1#/GPIO51 C18 PCI_GNT1# PCI_GNT0#
REQ2#/GPIO52 B19 SB_WWAN_PCIE_RST# PCI_REQ1# 32
GNT2#/GPIO53 F18 PCI_GNT2# PCI_GNT1# 32
REQ3#/GPIO54 A11 SB_LOM_PCIE_RST# SB_WWAN_PCIE_RST# 50 T77
GNT3#/GPIO55 C10 PCI_GNT3# SB_LOM_PCIE_RST# 47 T89
C/BE0# C17 PCI_C_BE0# 32
C/BE1# E15 PCI_C_BE1# 32
C/BE2# F16 PCI_C_BE2# 32
C/BE3# E17 PCI_C_BE3# 32
IRDY# C8 PCI_IRDY# PCI_IRDY# 32
PAR D9 PCI_PAR 32
PCIRST# G6 PCI_RST#_G
DEVSEL# D16 PCI_DEVSEL# PCI_DEVSEL# 32
PERR# A7 PCI_PERR# PCI_PERR# 32
PLOCK# B7 PCI_PLOCK#
SERR# F10 PCI_SERR# PCI_SERR# 32
STOP# C16 PCI_STOP# PCI_STOP# 32
TRDY# C9 PCI_TRDY# PCI_TRDY# 32
FRAME# A17 PCI_FRAME# PCI_FRAME# 32
PLTRST# AG24 PCI_PLTRST#
PCICLK B10 CLK_PCI_ICH CLK_PCI_ICH 21
PME# G7 ICH_PME# 38

Interrupt I/F

T95 PCI_PIRQA# F9
PCI_PIRQB# PCI_PIRQB# B5
32 PCI_PIRQC# PCI_PIRQC# C5
32 PCI_PIRQD# PCI_PIRQD# A10
PIRQA# PIRQE#/GPIO2
PIRQB# PIRQF#/GPIO3
PIRQC# PIRQG#/GPIO4
PIRQD# PIRQH#/GPIO5
F8 ICH_GPIO2_PIRQE#
G11 SB_WLAN_PCIE_RST# SB_WLAN_PCIE_RST# 50
F12 SB_NB_PCIE_RST# SB_NB_PCIE_RST# 10
B3 PCIE_MCARD2_DET# 50
NO.13

ICH8-M

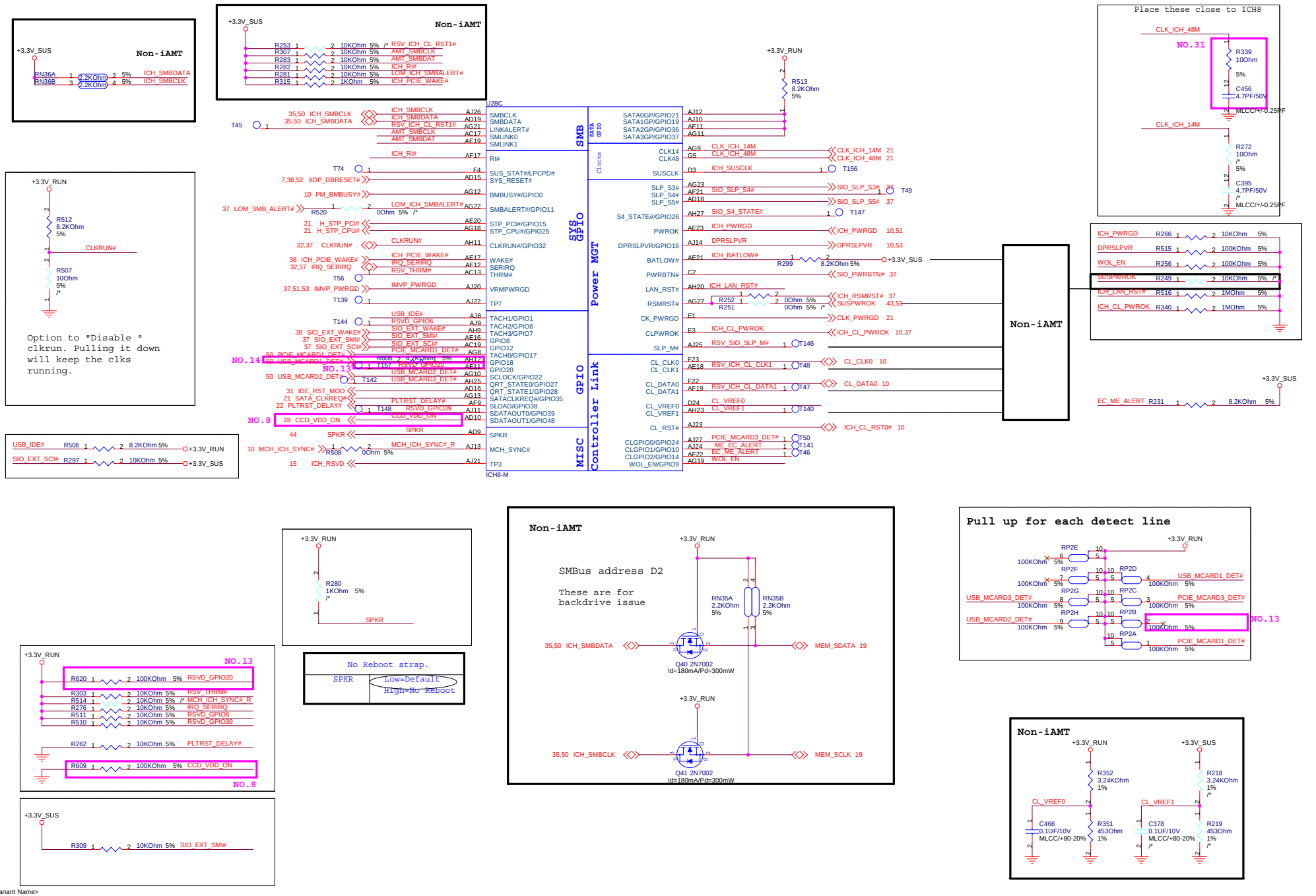
R5C833	REQ1 GNT1	PIRQC PIRQD

CLK_PCI_ICH
R355 10Ohm 5% /*
C475 8.2PF/50V MLCC/+/-0.25PF /*

Reserved for EMI.
Place resister and cap close to ICH.

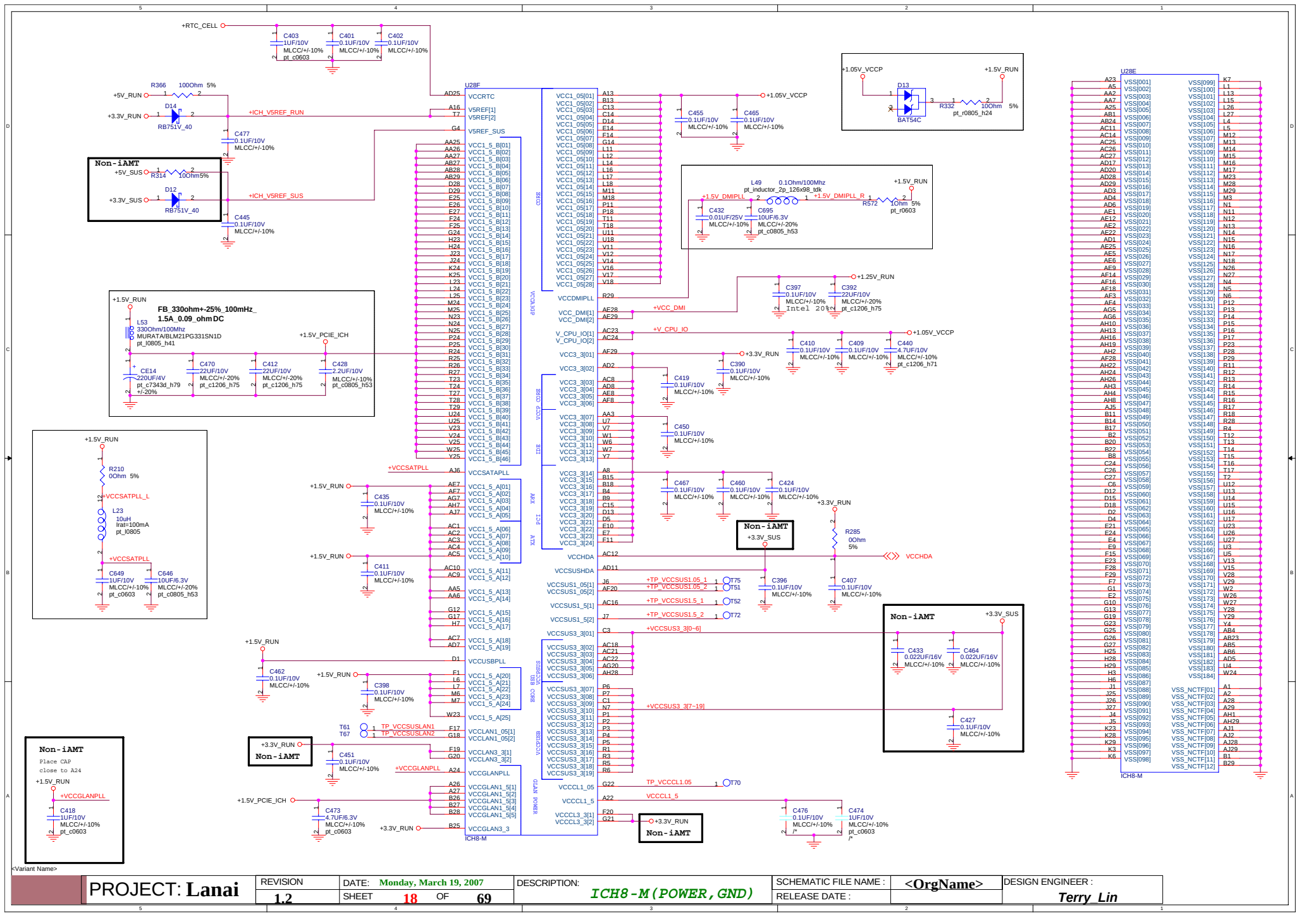
<Variant Name>

PROJECT: Lanai	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: ICH8: PCI/INT/DMI/USB	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER : Terry_Lin
		SHEET 16 OF 69		RELEASE DATE :	



<Variant Name>

PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***ICH8: SMB/PWR/CLK/GPIO***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : ***Terry_Lin***
		SHEET **17** OF **69**		RELEASE DATE :	


+RTC_CELL
C403 1UF/10V MLCC/+/-10% pt_c0603
C401 0.1UF/10V MLCC/+/-10%
C402 0.1UF/10V MLCC/+/-10%
R366 100Ohm 5%
+5V_RUN
+3.3V_RUN
D14 RB751V_40
+ICH_V5REF_RUN
C477 0.1UF/10V MLCC/+/-10%
Non-iAMT
+5V_SUS
R314 10Ohm5%
+3.3V_SUS
D12 RB751V_40
+ICH_V5REF_SUS
C445 0.1UF/10V MLCC/+/-10%
U28F
VCCRTC
V5REF[1]
V5REF[2]
V5REF_SUS
VCC1_5_B[01]
VCC1_5_B[02]
VCC1_5_B[03]
VCC1_5_B[04]
VCC1_5_B[05]
VCC1_5_B[06]
VCC1_5_B[07]
VCC1_5_B[08]
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VCC1_5_B[18]
VCC1_5_B[19]
VCC1_5_B[20]
VCC1_5_B[21]
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VCC1_5_B[43]
VCC1_5_B[44]
VCC1_5_B[45]
VCC1_5_B[46]
VCCSATAPLL
VCC1_5_A[01]
VCC1_5_A[02]
VCC1_5_A[03]
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VCC1_5_A[19]
VCCUSBPLL
VCC1_5_A[20]
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VCC1_5_A[24]
VCC1_5_A[25]
VCCLAN1_05[1]
VCCLAN1_05[2]
VCCLAN3_3[1]
VCCLAN3_3[2]
VCCGLANPLL
VCCGLAN1_5[1]
VCCGLAN1_5[2]
VCCGLAN1_5[3]
VCCGLAN1_5[4]
VCCGLAN1_5[5]
VCCGLAN3_3
ICH8-M
VCC1_05[01]
VCC1_05[02]
VCC1_05[03]
VCC1_05[04]
VCC1_05[05]
VCC1_05[06]
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VCC1_05[09]
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VCC1_05[11]
VCC1_05[12]
VCC1_05[13]
VCC1_05[14]
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VCC1_05[23]
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VCC1_05[25]
VCC1_05[26]
VCC1_05[27]
VCC1_05[28]
VCCDMIPLL
VCC_DMI[1]
VCC_DMI[2]
V_CPU_IO[1]
V_CPU_IO[2]
VCC3_3[01]
VCC3_3[02]
VCC3_3[03]
VCC3_3[04]
VCC3_3[05]
VCC3_3[06]
VCC3_3[07]
VCC3_3[08]
VCC3_3[09]
VCC3_3[10]
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VCC3_3[19]
VCC3_3[20]
VCC3_3[21]
VCC3_3[22]
VCC3_3[23]
VCC3_3[24]
VCCHDA
VCCSUSHDA
VCCSUS1_05[1]
VCCSUS1_05[2]
VCCSUS1_5[1]
VCCSUS1_5[2]
VCCSUS3_3[01]
VCCSUS3_3[02]
VCCSUS3_3[03]
VCCSUS3_3[04]
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VCCSUS3_3[06]
VCCSUS3_3[07]
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VCCSUS3_3[12]
VCCSUS3_3[13]
VCCSUS3_3[14]
VCCSUS3_3[15]
VCCSUS3_3[16]
VCCSUS3_3[17]
VCCSUS3_3[18]
VCCSUS3_3[19]
VCCCL1_05
VCCCL1_5
VCCCL3_3[1]
VCCCL3_3[2]
C455 0.1UF/10V MLCC/+/-10%
C465 0.1UF/10V MLCC/+/-10%
+1.05V_VCCP
+1.05V_RUN
D13 BAT54C
R332 10Ohm 5% pt_r0805_h24
L49 0.1Ohm/100Mhz pt_inductor_2p_126x98_tdk
+1.5V_DMIPLL
+1.5V_DMIPLL_R
R572 10Ohm 5% pt_r0603
C432 0.01UF/25V MLCC/+/-10%
C695 10UF/6.3V MLCC/+/-20% pt_c0805_h53
C397 0.1UF/10V MLCC/+/-10% Intel 20%
C392 22UF/10V MLCC/+/-20% pt_c1206_h75
+1.25V_RUN
+VCC_DMI
+V_CPU_IO
C410 0.1UF/10V MLCC/+/-10%
C409 0.1UF/10V MLCC/+/-10%
C440 4.7UF/10V MLCC/+/-10% pt_c1206_h71
+3.3V_RUN
C390 0.1UF/10V MLCC/+/-10%
C419 0.1UF/10V MLCC/+/-10%
C450 0.1UF/10V MLCC/+/-10%
C467 0.1UF/10V MLCC/+/-10%
C460 0.1UF/10V MLCC/+/-10%
C424 0.1UF/10V MLCC/+/-10%
Non-iAMT +3.3V_SUS
R285 0Ohm 5%
VCCHDA
C396 0.1UF/10V MLCC/+/-10%
C407 0.1UF/10V MLCC/+/-10%
+TP_VCCSUS1.05_1
+TP_VCCSUS1.05_2
+TP_VCCSUS1.5_1
+TP_VCCSUS1.5_2
+VCCSUS3_3[0~6]
+VCCSUS3_3[7~19]
C433 0.022UF/16V MLCC/+/-10%
C464 0.022UF/16V MLCC/+/-10%
C427 0.1UF/10V MLCC/+/-10%
TP_VCCCL1.05
VCCCL1_5
C476 0.1UF/10V MLCC/+/-10%
C474 1UF/10V MLCC/+/-10% pt_c0603
FB_330ohm+-25%_100mHz_ 1.5A_0.09_ohm DC
L53 330Ohm/100Mhz MURATA/BLM21PG331SN1D pt_l0805_h41
+1.5V_PCIE_ICH
CE14 220UF/4V pt_c7343d_h79 +/-20%
C470 22UF/10V MLCC/+/-20% pt_c1206_h75
C412 22UF/10V MLCC/+/-20% pt_c1206_h75
C428 2.2UF/10V MLCC/+/-10% pt_c0805_h53
R210 0Ohm 5%
+VCCSATPLL_L
L23 10uH Irat=100mA pt_l0805
+VCCSATPLL
C649 1UF/10V MLCC/+/-10% pt_c0603
C646 10UF/6.3V MLCC/+/-20% pt_c0805_h53
C435 0.1UF/10V MLCC/+/-10%
C411 0.1UF/10V MLCC/+/-10%
C462 0.1UF/10V MLCC/+/-10%
C398 0.1UF/10V MLCC/+/-10%
T61 TP_VCCSUSLAN1
T67 TP_VCCSUSLAN2
C451 0.1UF/10V MLCC/+/-10%
+VCCGLANPLL
C473 4.7UF/6.3V MLCC/+/-10% pt_c0603
Non-iAMT Place CAP close to A24
C418 1UF/10V MLCC/+/-10% pt_c0603
U28E
VSS[001]
VSS[002]
VSS[003]
VSS[004]
VSS[005]
VSS[006]
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VSS_NCTF[04]
VSS_NCTF[05]
VSS_NCTF[06]
VSS_NCTF[07]
VSS_NCTF[08]
VSS_NCTF[09]
VSS_NCTF[10]
VSS_NCTF[11]
VSS_NCTF[12]
ICH8-M
<Variant Name>
PROJECT: Lanai
REVISION 1.2
DATE: Monday, March 19, 2007
SHEET 18 OF 69
DESCRIPTION: ICH8-M(POWER,GND)
SCHEMATIC FILE NAME : <OrgName>
RELEASE DATE :
DESIGN ENGINEER : Terry_Lin

A is required to route to Top SODIMM for AMT to function Ch.A SODIMM needs to be populated for Intel AMT support.

TOP

+1.8V_SUS
V_DDR_MCH_REF

DDR_A_DM[0..7] 11
DDR_A_D[0..63] 11
DDR_A_DQS[0..7] 11
DDR_A_DQS#[0..7] 11
DDR_A_MA[0..14] 10,11,20

CON14

	1	VREF	VSS46	2	
DDR_A_D5	3	VSS47	DQ4	4	DDR_A_D4
DDR_A_D0	5	DQ0	DQ5	6	DDR_A_D6
	7	DQ1	VSS15	8	
DDR_A_DQS#0	9	VSS37	DM0	10	DDR_A_DM0
DDR_A_DQS0	11	DQS#0	VSS5	12	
	13	DQS0	DQ6	14	DDR_A_D2
DDR_A_D1	15	VSS48	DQ7	16	DDR_A_D7
DDR_A_D3	17	DQ2	VSS16	18	
	19	DQ3	DQ12	20	DDR_A_D8
DDR_A_D15	21	VSS38	DQ13	22	DDR_A_D12
DDR_A_D9	23	DQ8	VSS17	24	
	25	DQ9	DM1	26	DDR_A_DM1
DDR_A_DQS#1	27	VSS49	VSS53	28	
DDR_A_DQS1	29	DQS#1	CK0	30	M_CLK_DDR0 10
	31	DQS1	CK0#	32	M_CLK_DDR#0 10
DDR_A_D11	33	VSS39	VSS41	34	
DDR_A_D10	35	DQ10	DQ14	36	DDR_A_D14
	37	DQ11	DQ15	38	DDR_A_D13
	39	VSS50	VSS54	40	
	41	VSS18	VSS20	42	
DDR_A_D16	43	DQ16	DQ20	44	DDR_A_D17
DDR_A_D21	45	DQ17	DQ21	46	DDR_A_D20
	47	VSS1	VSS6	48	
DDR_A_DQS#2	49	DQS#2	NC3	50	PM_EXTTS#0 DDR_A_DM2 PM_EXTTS#0 10
DDR_A_DQS2	51	DQS2	DM2	52	
	53	VSS19	VSS21	54	
DDR_A_D19	55	DQ18	DQ22	56	DDR_A_D18
DDR_A_D22	57	DQ19	DQ23	58	DDR_A_D23
	59	VSS22	VSS24	60	
DDR_A_D25	61	DQ24	DQ28	62	DDR_A_D28
DDR_A_D27	63	DQ25	DQ29	64	DDR_A_D29
	65	VSS23	VSS25	66	
DDR_A_DM3	67	DM3	DQS#3	68	DDR_A_DQS#3
	69	NC4	DQS3	70	DDR_A_DQS3
	71	VSS9	VSS10	72	
DDR_A_D31	73	DQ26	DQ30	74	DDR_A_D30
DDR_A_D24	75	DQ27	DQ31	76	DDR_A_D26
	77	VSS4	VSS8	78	
10,20 DDR_CKE0_DIMMA	79	CKE0	CKE1	80	DDR_CKE1_DIMMA 10,20
	81	VDD7	VDD8	82	
	83	NC1	A15	84	DDR_A_MA14
11,20 DDR_A_BS2	85	A16_BA2	A14	86	
	87	VDD9	VDD11	88	DDR_A_MA11
DDR_A_MA12	89	A12	A11	90	DDR_A_MA7
DDR_A_MA9	91	A9	A7	92	DDR_A_MA6
DDR_A_MA8	93	A8	A6	94	
	95	VDD5	VDD4	96	DDR_A_MA4
DDR_A_MA5	97	A5	A4	98	DDR_A_MA2
DDR_A_MA3	99	A3	A2	100	DDR_A_MA0
DDR_A_MA1	101	A1	A0	102	
	103	VDD10	VDD12	104	
DDR_A_MA10	105	A10/AP	BA1	106	DDR_A_BS1 11,20
DDR_A_BS0 11,20	107	BA0	RAS#	108	DDR_A_RAS# 11,20
DDR_A_WE# 11,20	109	WE#	S0#	110	DDR_CS0_DIMMA# 10,20
	111	VDD2	VDD1	112	
DDR_A_CAS# 11,20	113	CAS#	ODT0	114	M_ODT0 DDR_A_MA13 M_ODT0 10,20
DDR_CS1_DIMMA# 10,20	115	S1#	A13	116	
	117	VDD3	VDD6	118	
M_ODT1 10,20	119	ODT1	NC2	120	
	121	VSS11	VSS12	122	
DDR_A_D36	123	DQ32	DQ36	124	DDR_A_D32
DDR_A_D33	125	DQ33	DQ37	126	DDR_A_D38
	127	VSS26	VSS28	128	
DDR_A_DQS#4	129	DQS#4	DM4	130	DDR_A_DM4
DDR_A_DQS4	131	DQS4	VSS42	132	
	133	VSS2	DQ38	134	DDR_A_D37
DDR_A_D39	135	DQ34	DQ39	136	DDR_A_D35
DDR_A_D34	137	DQ35	VSS55	138	
	139	VSS27	DQ44	140	DDR_A_D45
DDR_A_D40	141	DQ40	DQ45	142	DDR_A_D44
DDR_A_D47	143	DQ41	VSS43	144	
	145	VSS29	DQS#5	146	DDR_A_DQS#5
DDR_A_DM5	147	DM5	DQS5	148	DDR_A_DQS5
	149	VSS51	VSS56	150	
DDR_A_D42	151	DQ42	DQ46	152	DDR_A_D41
DDR_A_D43	153	DQ43	DQ47	154	DDR_A_D46
	155	VSS40	VSS44	156	
DDR_A_D48	157	DQ48	DQ52	158	DDR_A_D53
DDR_A_D49	159	DQ49	DQ53	160	DDR_A_D52
	161	VSS52	VSS57	162	
	163	NCTEST	CK1	164	M_CLK_DDR1 10
	165	VSS30	CK1#	166	M_CLK_DDR#1 10
DDR_A_DQS#6	167	DQS#6	VSS45	168	
DDR_A_DQS6	169	DQS6	DM6	170	DDR_A_DM6
	171	VSS31	VSS32	172	
DDR_A_D50	173	DQ50	DQ54	174	DDR_A_D51
DDR_A_D54	175	DQ51	DQ55	176	DDR_A_D55
	177	VSS33	VSS35	178	
DDR_A_D56	179	DQ56	DQ60	180	DDR_A_D58
DDR_A_D60	181	DQ57	DQ61	182	DDR_A_D57
	183	VSS3	VSS7	184	
DDR_A_DM7	185	DM7	DQS#7	186	DDR_A_DQS#7
	187	VSS34	DQS7	188	DDR_A_DQS7
DDR_A_D61	189	DQ58	VSS36	190	
DDR_A_D59	191	DQ59	DQ62	192	DDR_A_D63
	193	VSS14	DQ63	194	DDR_A_D62
MEM_SDATA 17	195	SDA	VSS13	196	
MEM_SCLK 17	197	SCL	SA0	198	
+3.3V_RUN	199	VDDSPD	SA1	200	
	201	GND0	GND1	202	
	203	NP_NC1NP_NC2		204	

STD FOXCONN/AS0A426-N2SN-7F

CLOCK 0 , 1
CKE 0 , 1

V_DDR_MCH_REF
C280 0.1UF/10V MLCC/+/-10%
C278 2.2UF/6.3V MLCC/+80-20%
pt_c0805_h53

+1.8V_SUS
R505 10KOhm 5%
R501 10KOhm 5%

+3.3V_RUN
Non-iAMT
C373 2.2UF/6.3V MLCC/+/-10%
C374 0.1UF/10V MLCC/+80-20%
pt_c0805_h53

MEM_SDATA
MEM_SCLK
+3.3V_RUN
Non-iAMT
SMbus address A0

BOT

+1.8V_SUS
V_DDR_MCH_REF

DDR_B_DM[0..7] 11
DDR_B_D[0..63] 11
DDR_B_DQS[0..7] 11
DDR_B_DQS#[0..7] 11
DDR_B_MA[0..14] 10,11,20

CON15

	1	VREF	VSS46	2	
DDR_B_D0	3	VSS47	DQ4	4	DDR_B_D5
DDR_B_D1	5	DQ0	DQ5	6	DDR_B_D4
	7	DQ1	VSS15	8	
DDR_B_DQS#0	9	VSS37	DM0	10	DDR_B_DM0
DDR_B_DQS0	11	DQS#0	VSS5	12	
	13	DQS0	DQ6	14	DDR_B_D6
DDR_B_D3	15	VSS48	DQ7	16	DDR_B_D7
DDR_B_D2	17	DQ2	VSS16	18	
	19	DQ3	DQ12	20	DDR_B_D8
DDR_B_D9	21	VSS38	DQ13	22	DDR_B_D12
DDR_B_D13	23	DQ8	VSS17	24	
	25	DQ9	DM1	26	DDR_B_DM1
DDR_B_DQS#1	27	VSS49	VSS53	28	
DDR_B_DQS1	29	DQS#1	CK0	30	M_CLK_DDR2 10
	31	DQS1	CK0#	32	M_CLK_DDR#2 10
DDR_B_D10	33	VSS39	VSS41	34	
DDR_B_D14	35	DQ10	DQ14	36	DDR_B_D11
	37	DQ11	DQ15	38	DDR_B_D15
	39	VSS50	VSS54	40	
	41	VSS18	VSS20	42	
DDR_B_D20	43	DQ16	DQ20	44	DDR_B_D21
DDR_B_D16	45	DQ17	DQ21	46	DDR_B_D23
	47	VSS1	VSS6	48	
DDR_B_DQS#2	49	DQS#2	NC3	50	PM_EXTTS#1 DDR_B_DM2 PM_EXTTS#1 10
DDR_B_DQS2	51	DQS2	DM2	52	
	53	VSS19	VSS21	54	
DDR_B_D18	55	DQ18	DQ22	56	DDR_B_D22
DDR_B_D19	57	DQ19	DQ23	58	DDR_B_D17
	59	VSS22	VSS24	60	
DDR_B_D25	61	DQ24	DQ28	62	DDR_B_D29
DDR_B_D28	63	DQ25	DQ29	64	DDR_B_D31
	65	VSS23	VSS25	66	
DDR_B_DM3	67	DM3	DQS#3	68	DDR_B_DQS#3
	69	NC4	DQS3	70	DDR_B_DQS3
	71	VSS9	VSS10	72	
DDR_B_D27	73	DQ26	DQ30	74	DDR_B_D24
DDR_B_D30	75	DQ27	DQ31	76	DDR_B_D26
	77	VSS4	VSS8	78	
10,20 DDR_CKE2_DIMMB	79	CKE0	CKE1	80	DDR_CKE3_DIMMB 10,20
	81	VDD7	VDD8	82	
	83	NC1	A15	84	DDR_B_MA14
11,20 DDR_B_BS2	85	A16_BA2	A14	86	
	87	VDD9	VDD11	88	DDR_B_MA11
DDR_B_MA12	89	A12	A11	90	DDR_B_MA7
DDR_B_MA9	91	A9	A7	92	DDR_B_MA6
DDR_B_MA8	93	A8	A6	94	
	95	VDD5	VDD4	96	DDR_B_MA4
DDR_B_MA5	97	A5	A4	98	DDR_B_MA2
DDR_B_MA3	99	A3	A2	100	DDR_B_MA0
DDR_B_MA1	101	A1	A0	102	
	103	VDD10	VDD12	104	
DDR_B_MA10	105	A10/AP	BA1	106	DDR_B_BS1 11,20
DDR_B_BS0 11,20	107	BA0	RAS#	108	DDR_B_RAS# 11,20
DDR_B_WE# 11,20	109	WE#	S0#	110	DDR_CS2_DIMMB# 10,20
	111	VDD2	VDD1	112	
DDR_B_CAS# 11,20	113	CAS#	ODT0	114	M_ODT2 DDR_B_MA13 M_ODT2 10,20
DDR_CS3_DIMMB# 10,20	115	S1#	A13	116	
	117	VDD3	VDD6	118	
M_ODT3 10,20	119	ODT1	NC2	120	
	121	VSS11	VSS12	122	
DDR_B_D38	123	DQ32	DQ36	124	DDR_B_D35
DDR_B_D36	125	DQ33	DQ37	126	DDR_B_D32
	127	VSS26	VSS28	128	
DDR_B_DQS#4	129	DQS#4	DM4	130	DDR_B_DM4
DDR_B_DQS4	131	DQS4	VSS42	132	
	133	VSS2	DQ38	134	DDR_B_D39
DDR_B_D34	135	DQ34	DQ39	136	DDR_B_D37
DDR_B_D33	137	DQ35	VSS55	138	
	139	VSS27	DQ44	140	DDR_B_D40
DDR_B_D45	141	DQ40	DQ45	142	DDR_B_D41
DDR_B_D46	143	DQ41	VSS43	144	
	145	VSS29	DQS#5	146	DDR_B_DQS#5
DDR_B_DM5	147	DM5	DQS5	148	DDR_B_DQS5
	149	VSS51	VSS56	150	
DDR_B_D44	151	DQ42	DQ46	152	DDR_B_D47
DDR_B_D42	153	DQ43	DQ47	154	DDR_B_D43
	155	VSS40	VSS44	156	
DDR_B_D53	157	DQ48	DQ52	158	DDR_B_D52
DDR_B_D48	159	DQ49	DQ53	160	DDR_B_D49
	161	VSS52	VSS57	162	
	163	NCTEST	CK1	164	M_CLK_DDR3 10
	165	VSS30	CK1#	166	M_CLK_DDR#3 10
DDR_B_DQS#6	167	DQS#6	VSS45	168	
DDR_B_DQS6	169	DQS6	DM6	170	DDR_B_DM6
DDR_B_D51	171	VSS31	VSS32	172	
DDR_B_D54	173	DQ50	DQ54	174	DDR_B_D55
	175	DQ51	DQ55	176	DDR_B_D50
DDR_B_D56	177	VSS33	VSS35	178	
DDR_B_D62	179	DQ56	DQ60	180	DDR_B_D57
	181	DQ57	DQ61	182	DDR_B_D61
DDR_B_DM7	183	VSS3	VSS7	184	
	185	DM7	DQS#7	186	DDR_B_DQS#7
DDR_B_D63	187	VSS34	DQS7	188	DDR_B_DQS7
DDR_B_D60	189	DQ58	VSS36	190	
MEM_SDATA	191	DQ59	DQ62	192	DDR_B_D58
MEM_SCLK	193	VSS14	DQ63	194	DDR_B_D59
	195	SDA	VSS13	196	
	197	SCL	SA0	198	
	199	VDDSPD	SA1	200	
	201	GND0	GND1	202	
	203	NP_NC1NP_NC2		204	

STD FOXCONN/AS0A426-NASN-7F

CLOCK 2 , 3
CKE 2 , 3

Non-iAMT
+3.3V_RUN
SMbus address A4

V_DDR_MCH_REF
C281 0.1UF/10V MLCC/+/-10%
C275 2.2UF/6.3V MLCC/+80-20%
pt_c0805_h53

+1.8V_SUS
R212 10KOhm 5%
R211 10KOhm 5%

+3.3V_RUN
Non-iAMT
C651 2.2UF/6.3V MLCC/+/-10%
C647 0.1UF/10V MLCC/+80-20%
pt_c0805_h53

+1.8V_SUS
Please these Caps near So-Dimm1
C327 C300 C333 C341 C342
2.2UF/6.3V MLCC/+/-10% pt_c0603

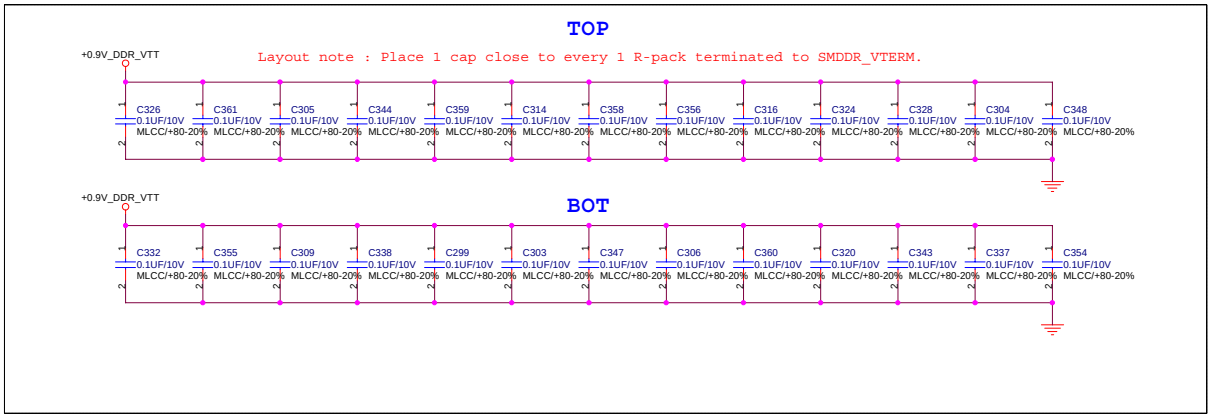
+1.8V_SUS
Please these Caps near So-Dimm2
C321 C619 C591 C331 C317
2.2UF/6.3V MLCC/+/-10% pt_c0603

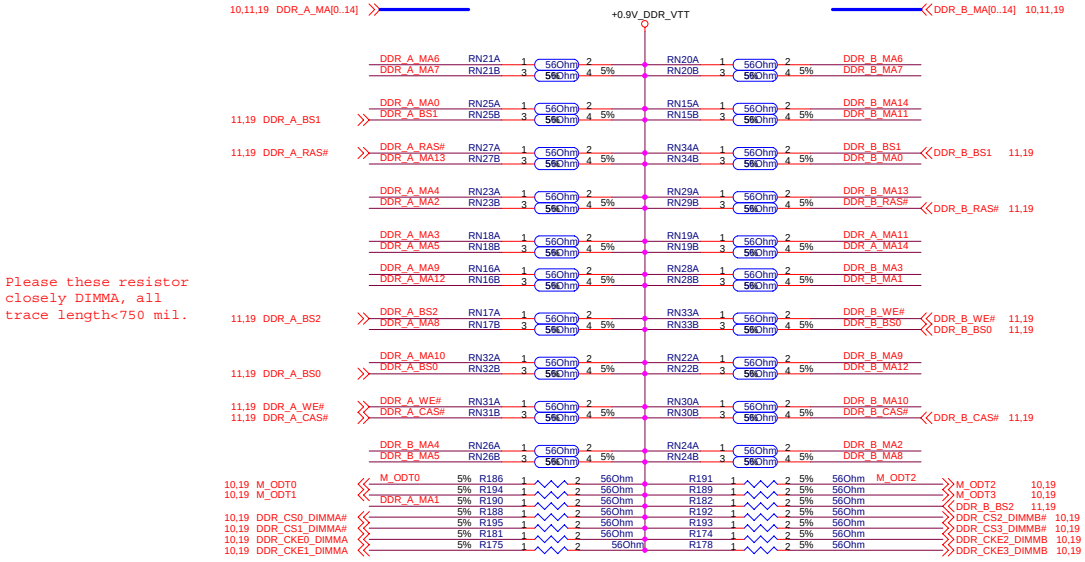
+1.8V_SUS
Please these Caps near So-Dimm1
C315 C325 C319 C323
0.1UF/10V MLCC/+80-20%

+1.8V_SUS
Please these Caps near So-Dimm2
C340 C601 C609 C616
0.1UF/10V MLCC/+80-20%

<Variant Name>

PROJECT: **Lanai**	REVISION: **1.2**	DATE: Monday, March 19, 2007	DESCRIPTION: *DDR2 SO-DIMM (0)*	SCHEMATIC FILE NAME: <OrgName>	DESIGN ENGINEER: *STANLY_HSU*
		SHEET 19 OF 69		RELEASE DATE:	



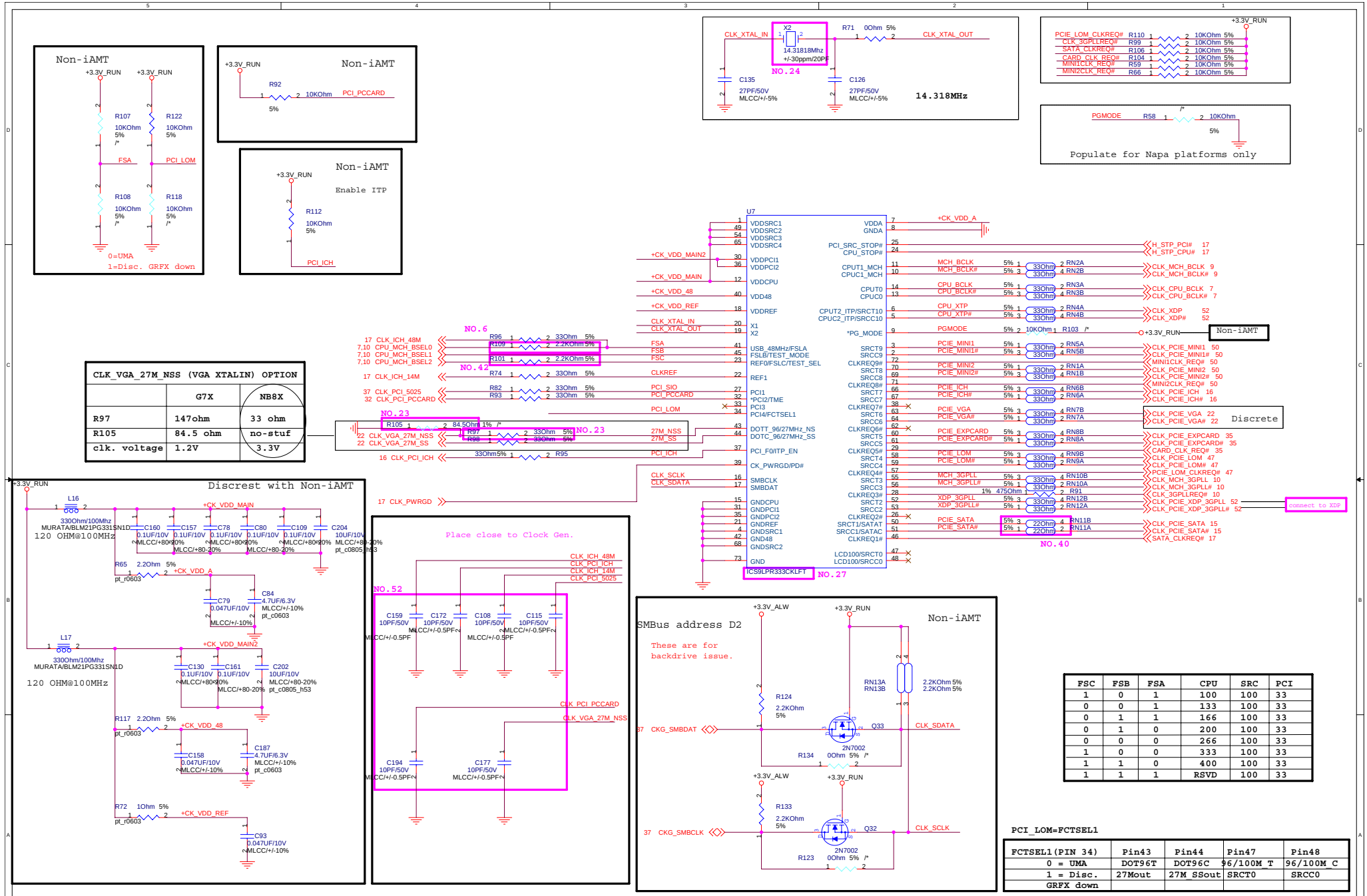


Please these resistor closely DIMMA, all trace length<750 mil.

Please these resistor closely DIMMB, all trace length<750 mil.

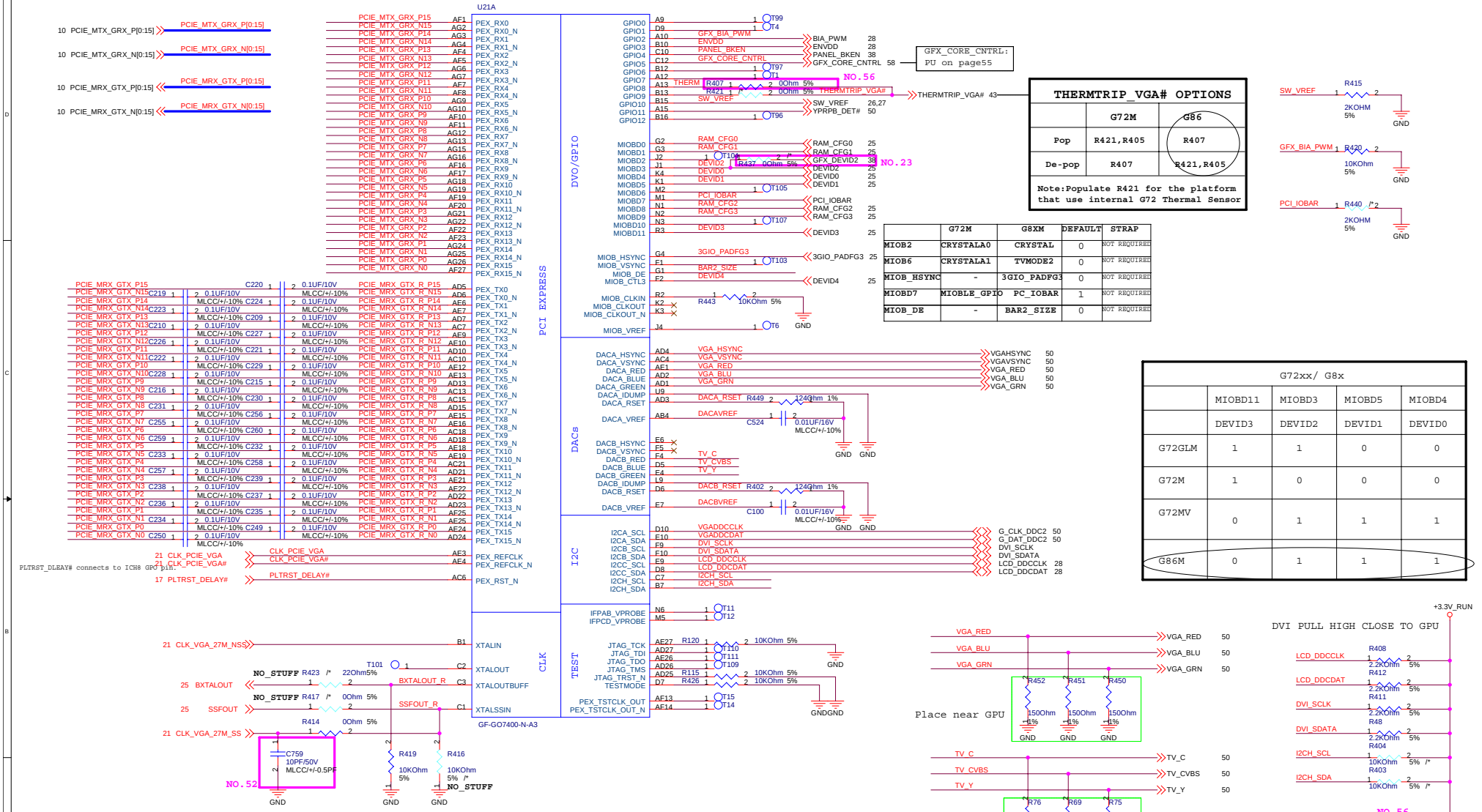
<Variant Name>

PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***DDR2 SO-DIMM (1)***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : ***STANLY_HSU***
		SHEET **20** OF **69**		RELEASE DATE :	



<Variant Name>

PROJECT: **Lanai**	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: *CLK GEN. CY28547*	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER : *STANLY_HSU*
		SHEET 21 OF 69		RELEASE DATE :	



THERMTRIP_VGA# OPTIONS		
	G72M	G86
Pop	R421,R405	R407
De-pop	R407	R421,R405

Note:Populate R421 for the platform that use internal G72 Thermal Sensor

	G72M	G8XM	DEFAULT	STRAP
MIOB2	CRYSTALA0	CRYSTAL	0	NOT REQUIRED
MIOB6	CRYSTALA1	TVMODE2	0	NOT REQUIRED
MIOB_HSYNC	-	3GIO_PADFG3	0	NOT REQUIRED
MIOBD7	MIOBLE_GPIO	PC_IOBAR	1	NOT REQUIRED
MIOB_DE	-	BAR2_SIZE	0	NOT REQUIRED

G72xx/ G8x				
	MIOBD11	MIOBD3	MIOBD5	MIOBD4
	DEVID3	DEVID2	DEVID1	DEVID0
G72GLM	1	1	0	0
G72M	1	0	0	0
G72MV	0	1	1	1
G86M	0	1	1	1

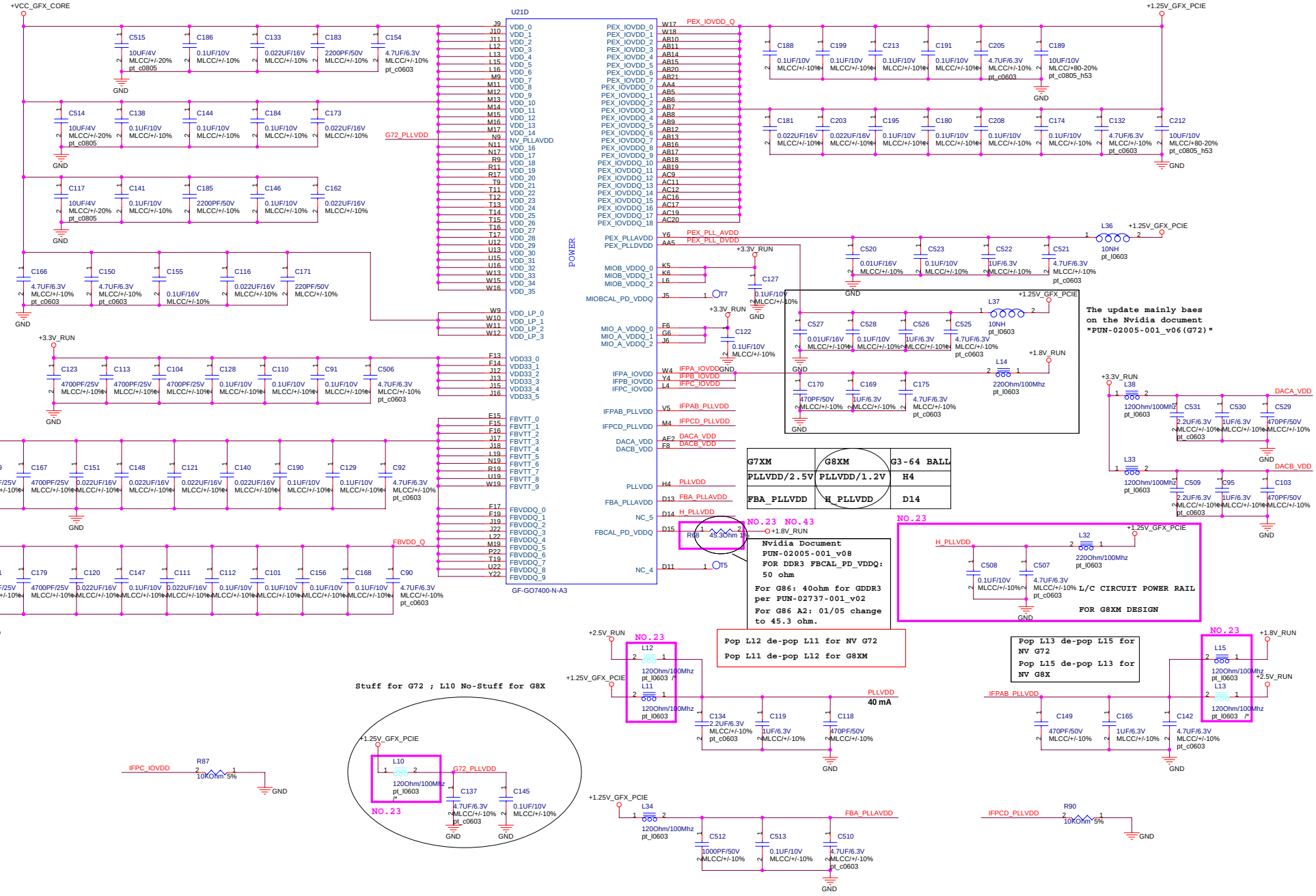
POPULATION OPTIONS			
	CY28547+SS	CY28547+U5	CY28547 wo/SS
Pop	R414,R419, R98	R423,R417, U5	R416,R419
De-pop	U5,R423, R417,R416	R414,R416, R419,R98	U5,R98, R414,R417, R423

'U5'indicate all ckt.related to U5 in Page.25

Layout comments: Place R423,R419 as close as possible to C3. . Place R414,R416and R417 as close as posisble to pin C1.

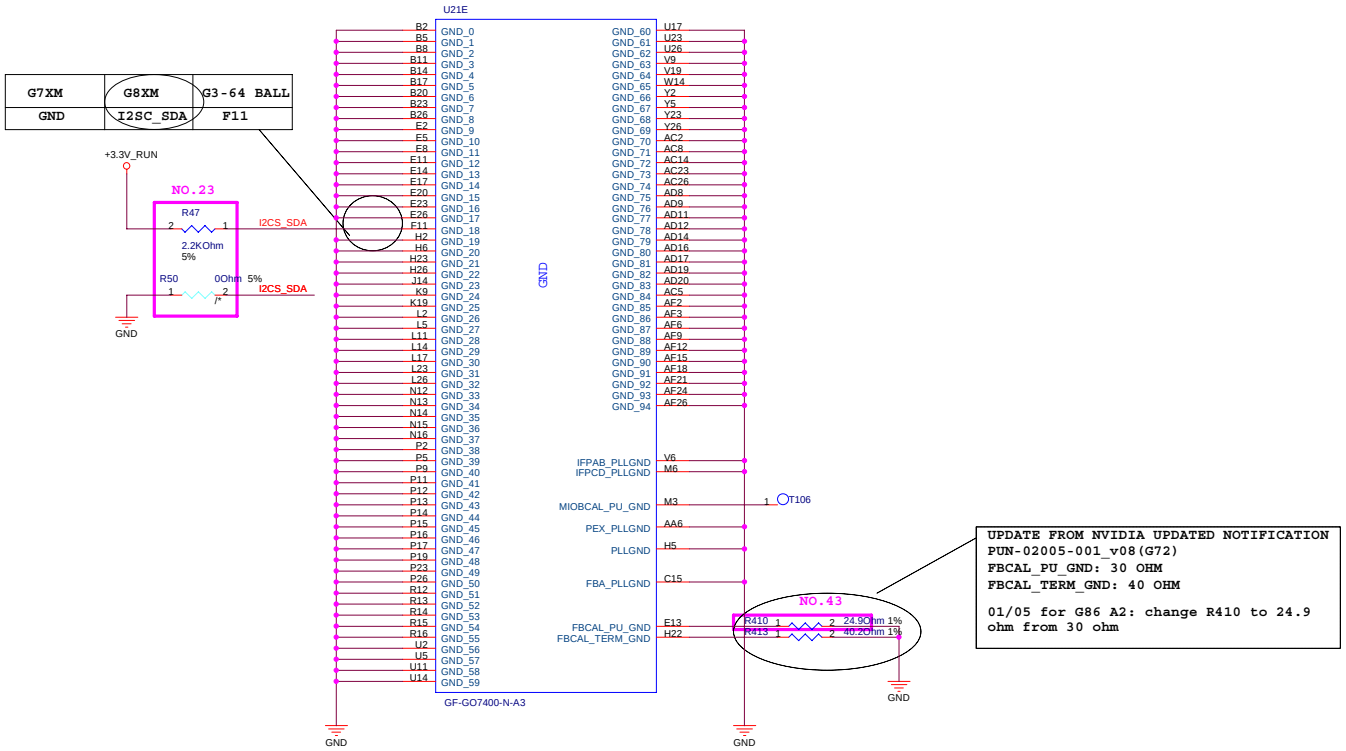
<Variant Name>

PROJECT: Lanai	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: G72M/G8X CORE PCIE	SCHEMATIC FILE NAME :	DESIGN ENGINEER : Sean Kuo
		SHEET 22 OF 69		RELEASE DATE :	



<Variant Name>

PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***G72M/G8X POWER***	SCHEMATIC FILE NAME :	DESIGN ENGINEER : ***Sean Kuo***
		SHEET **23** OF **69**		RELEASE DATE :	

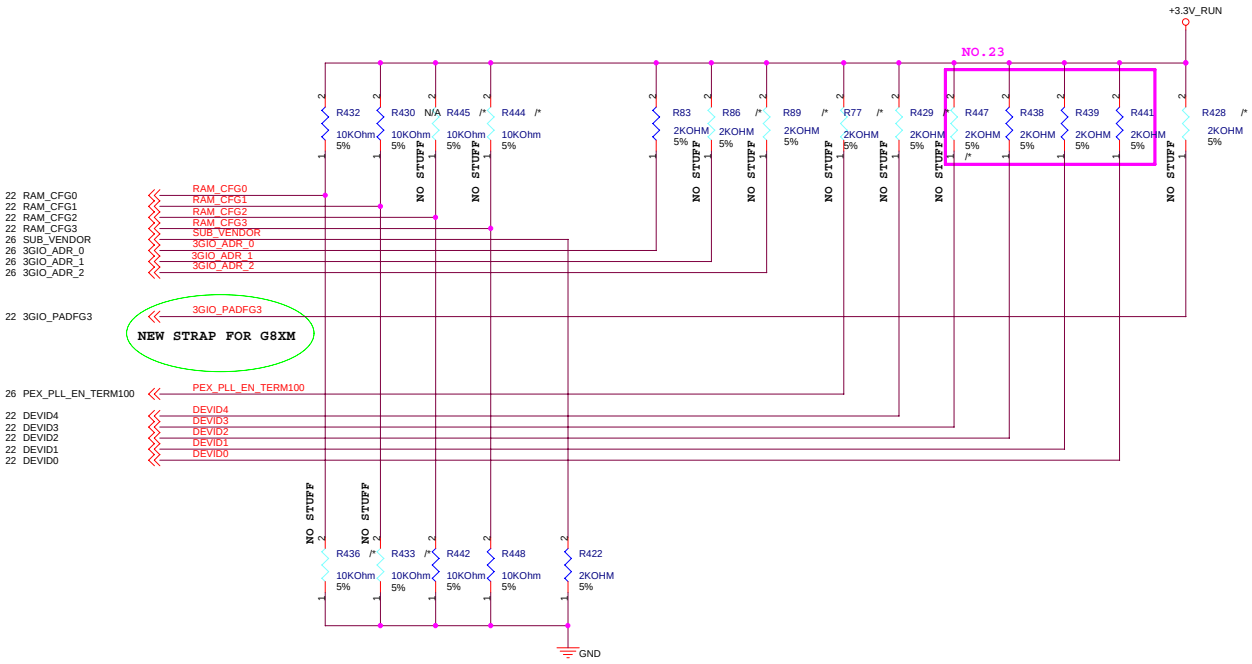


<Variant Name>

PROJECT: **Lanai**	REVISION: 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: *G7XM/G8X CORE GND*	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER : *Sean Kuo*
		SHEET 24 OF 69		RELEASE DATE :	

NV44M

STRAPS	PIN	DESCRIPTION		Value
ROM_TYPE[1:0]	MIOBD10 MIOB_VSYNC	Parallel=00, SERIAL AT25F=01 DEFAULT,Serial SST45VF=10, LPC=11		01
SUB_VENDOR	MIOAD1			0
PEX_PLL_TERM	MIOAD0			0
RAM_CFG[3:0]	MIOBD0 MIOBD1 MIOBD8 MIOBD9	FOR GDDR1	8Mx32 DDR monolithic (32bit) 300MHz,1.8V	1001
			4Mx32 DDR generic (64bit) 1.8V I/O	0100
			4Mx32 DDR generic (32bit) 1.8V I/O	1100
		FOR GDDR3	Infineon 8Mx32 500MHz, 1.8V	0101
			Hynix 8Mx32 500MHz, 1.8V	0111
			Samsung 8Mx32 500MHz, 1.8V	0110
			Infineon 16Mx32 GDDR3 ,1.8V	0001
			Hynix 16Mx32 GDDR3 1.8V	0010
			Samsung 16Mx32 GDDR3 1.8V	0011



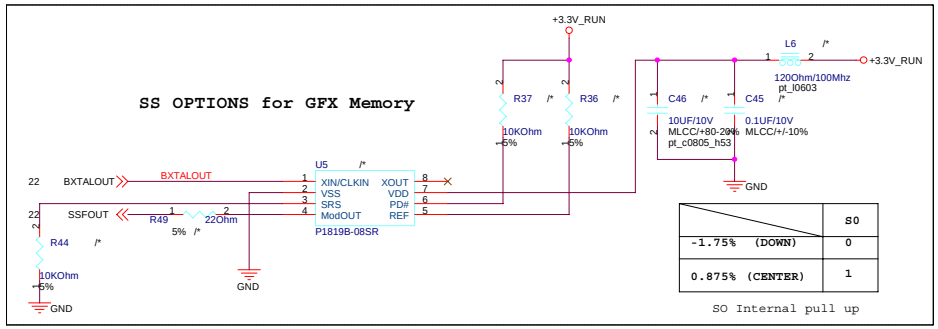
Internal Pull-down
MIOAD0, MIOAD6,
MIOAD8, MIOAD9

```
MIOAD1----SUB_VENDOR          0, SYSTEM BIOS

MIOAD0----PEX_PLL_EN_TERM

MIOAD6----3GIO_ADR_0          [2:0] 001 for NV43/NV44
MIOAD8----3GIO_ADR_1                010 for G7x, NV42
MIOAD9----3GIO_ADR_2
```

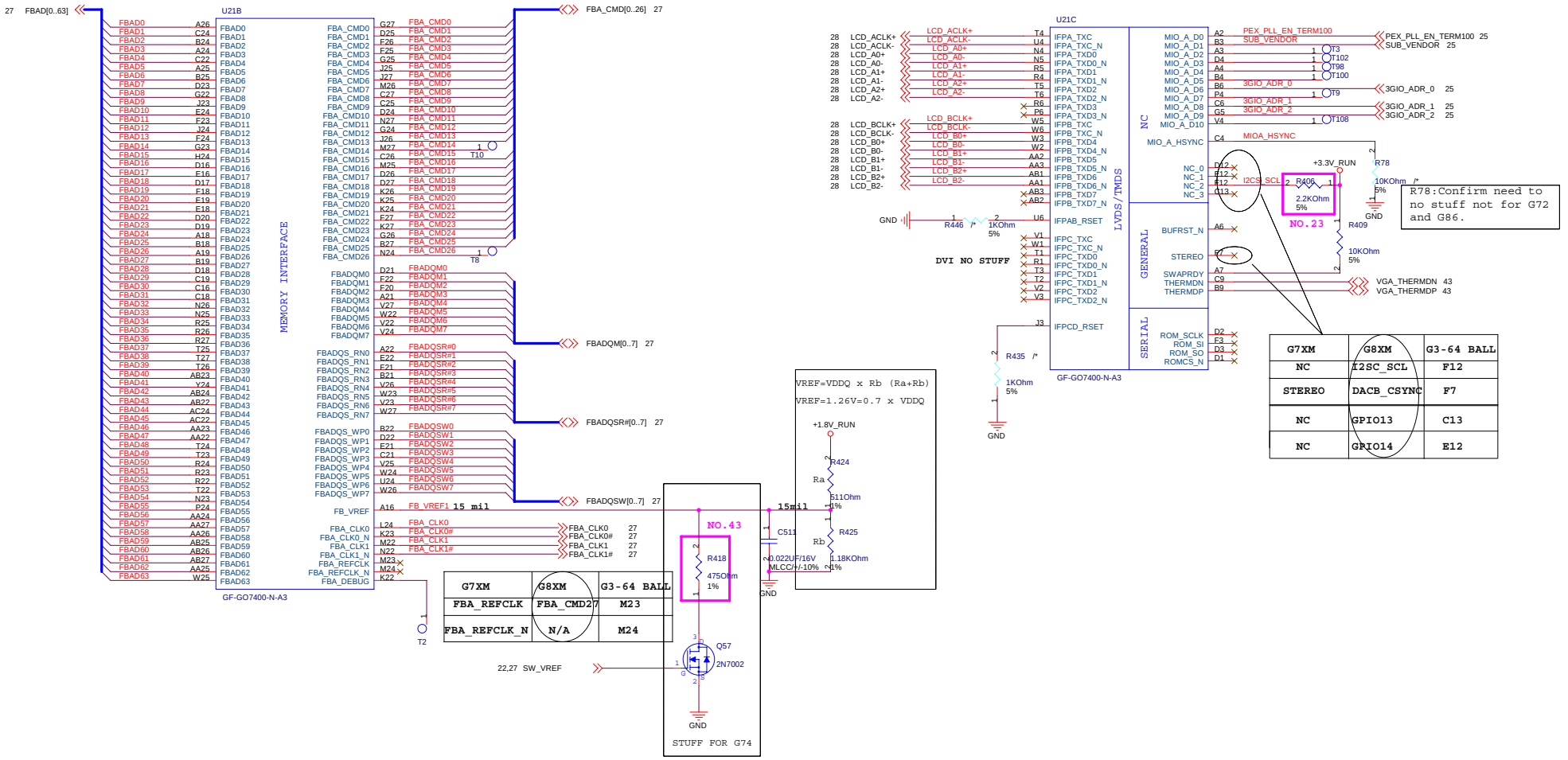
```
MIOBD4----PCI_DEVID0    1000,G72M
MIOBD5----PCI_DEVID1    0111,G72MV
MIOBD3----PCI_DEVID2
MIOBD11---PCI_DEVID3
```



M08 HAS REMOVED THIS PORTION
INSTALL OR NOT?

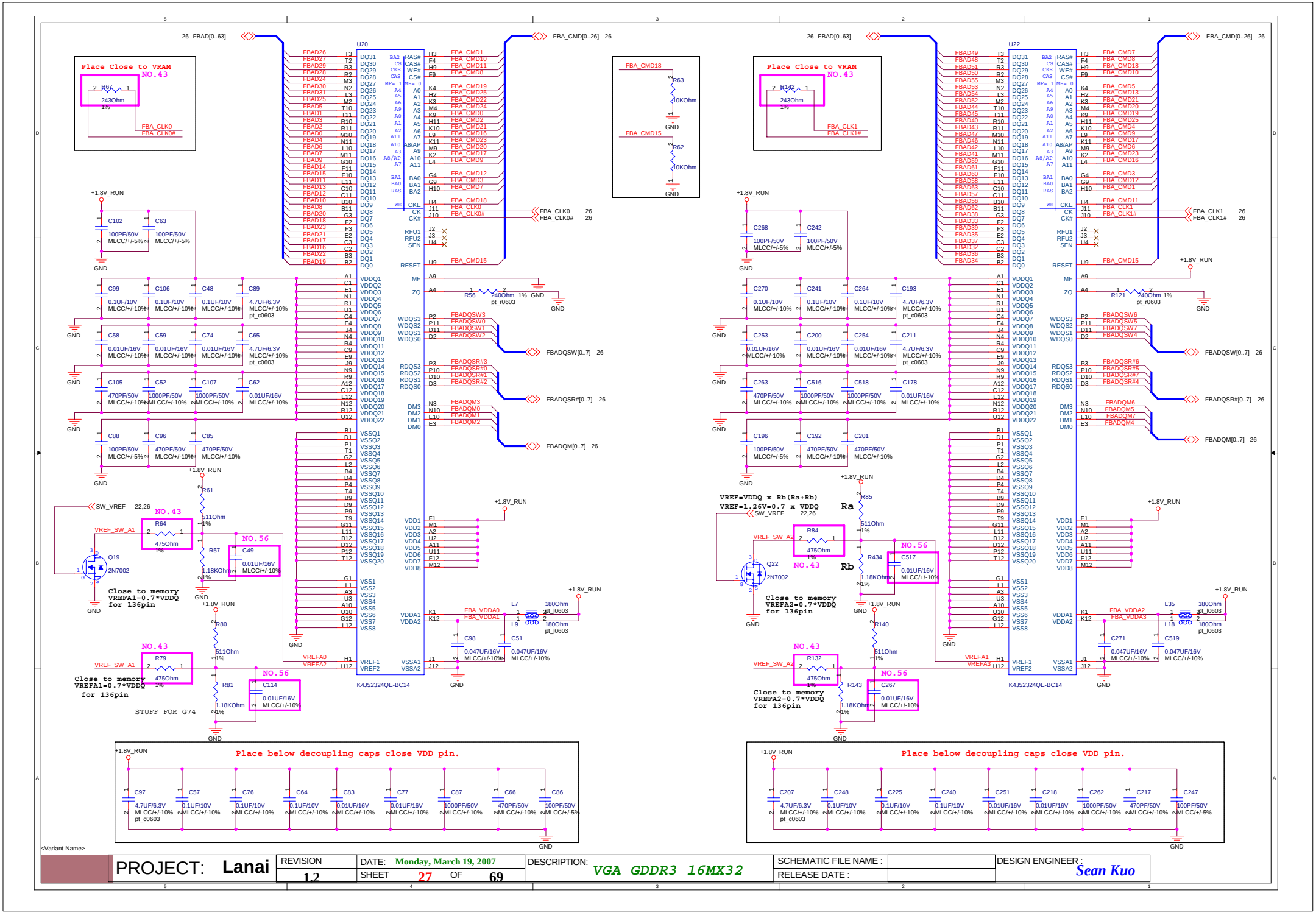
<Variant Name>

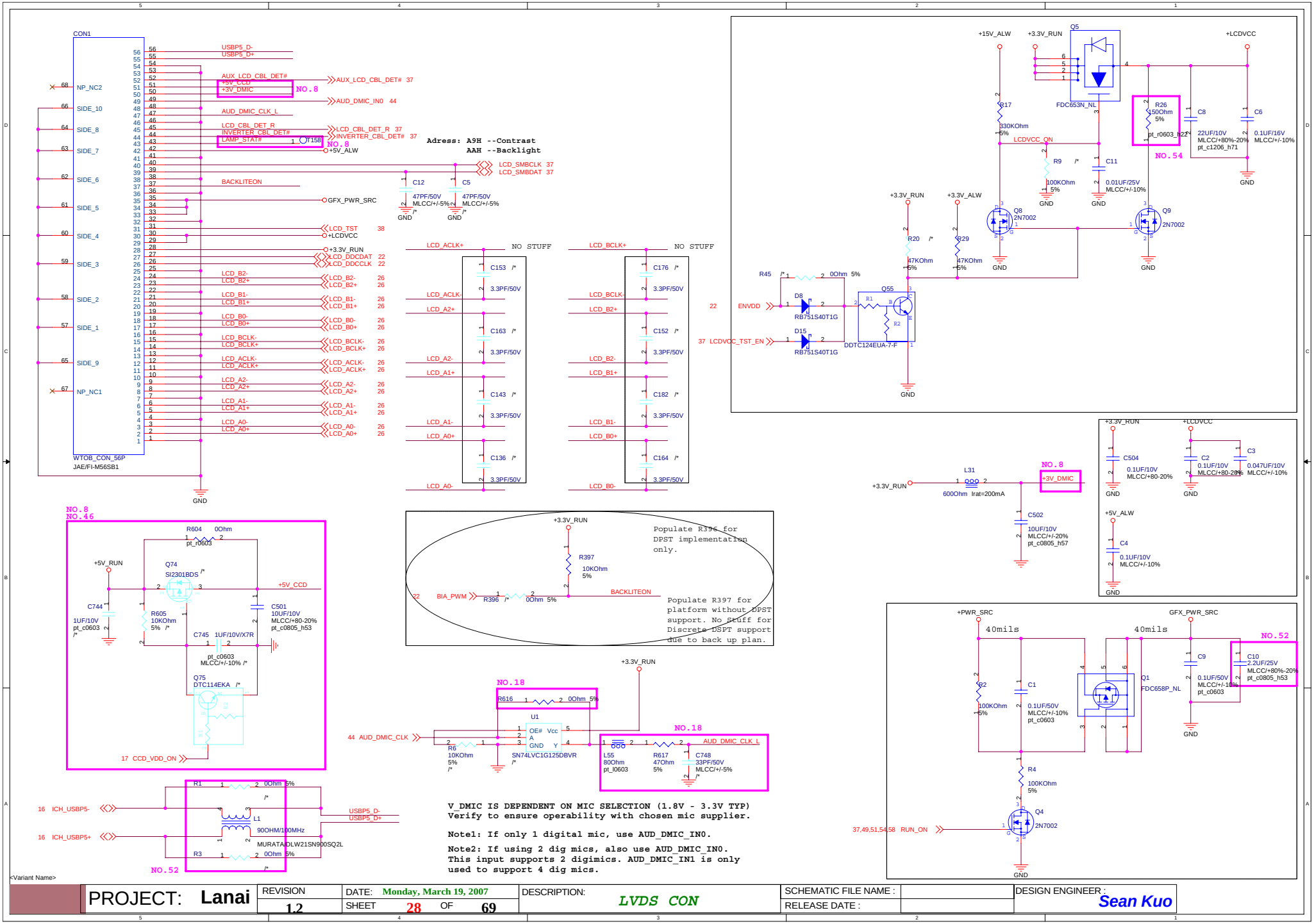
PROJECT: Lanai	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
	1.2	SHEET 25 OF 69	G72M/G8X STRAPPING PAGE	RELEASE DATE :	Sean Kuo



<Variant Name>

PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***G72M/G8X FBA/LVDS***	SCHEMATIC FILE NAME :	DESIGN ENGINEER : ***Sean Kuo***
		SHEET **26** OF **69**		RELEASE DATE :	


Place Close to VRAM
NO.43
R67
243Ohm
1%
FBA_CLK0
FBA_CLK0#
U20
K4J52324QE-BC14
FBA_CMD[0..26]
FBAD[0..63]
FBA_CMD18
FBA_CMD15
R63
10KOhm
R62
10KOhm
GND
+1.8V_RUN
C102
C63
100PF/50V
MLCC/+/-5%
C99
C106
C48
C89
0.1UF/10V
MLCC/+/-10%
4.7UF/6.3V
MLCC/+/-10%
pt_c0603
C58
C59
C74
C65
0.01UF/16V
C105
C52
C107
C62
470PF/50V
1000PF/50V
C88
C96
C85
R56
240Ohm 1%
pt_r0603
FBADQSW[0..7]
FBADQSR#[0..7]
FBADQM[0..7]
SW_VREF
22,26
R61
511Ohm
1%
R64
475Ohm
VREF_SW_A1
Q19
2N7002
R57
1.18KOhm
C49
0.01UF/16V
NO.56
Close to memory
VREFA1=0.7*VDDQ
for 136pin
R80
R79
R81
C114
STUFF FOR G74
VREFA0
VREFA2
FBA_VDDA0
FBA_VDDA1
L7
180Ohm
pt_l0603
C98
C51
0.047UF/16V
MLCC/+/-10%
VREF1
VREF2
VSSA1
VSSA2
Place below decoupling caps close VDD pin.
C97
C57
C76
C64
C83
C77
C87
C66
C86
1000PF/50V
470PF/50V
U22
R121
R268
C242
C270
C241
C264
C193
C253
C200
C254
C211
C263
C516
C518
C178
C196
C192
C201
VREF=VDDQ x Rb(Ra+Rb)
VREF=1.26V=0.7 x VDDQ
Ra
Rb
R85
R84
R434
Q22
R140
R132
R143
C517
C267
C271
C519
C207
C248
C225
C240
C251
C218
C262
C217
C247
<Variant Name>
PROJECT: Lanai
REVISION 1.2
DATE: Monday, March 19, 2007
SHEET 27 OF 69
DESCRIPTION: VGA GDDR3 16MX32
SCHEMATIC FILE NAME :
RELEASE DATE :
DESIGN ENGINEER : Sean Kuo



<Variant Name>

PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***LVDS CON***	SCHEMATIC FILE NAME :	DESIGN ENGINEER : **Sean Kuo**
		SHEET **28** OF **69**		RELEASE DATE :	

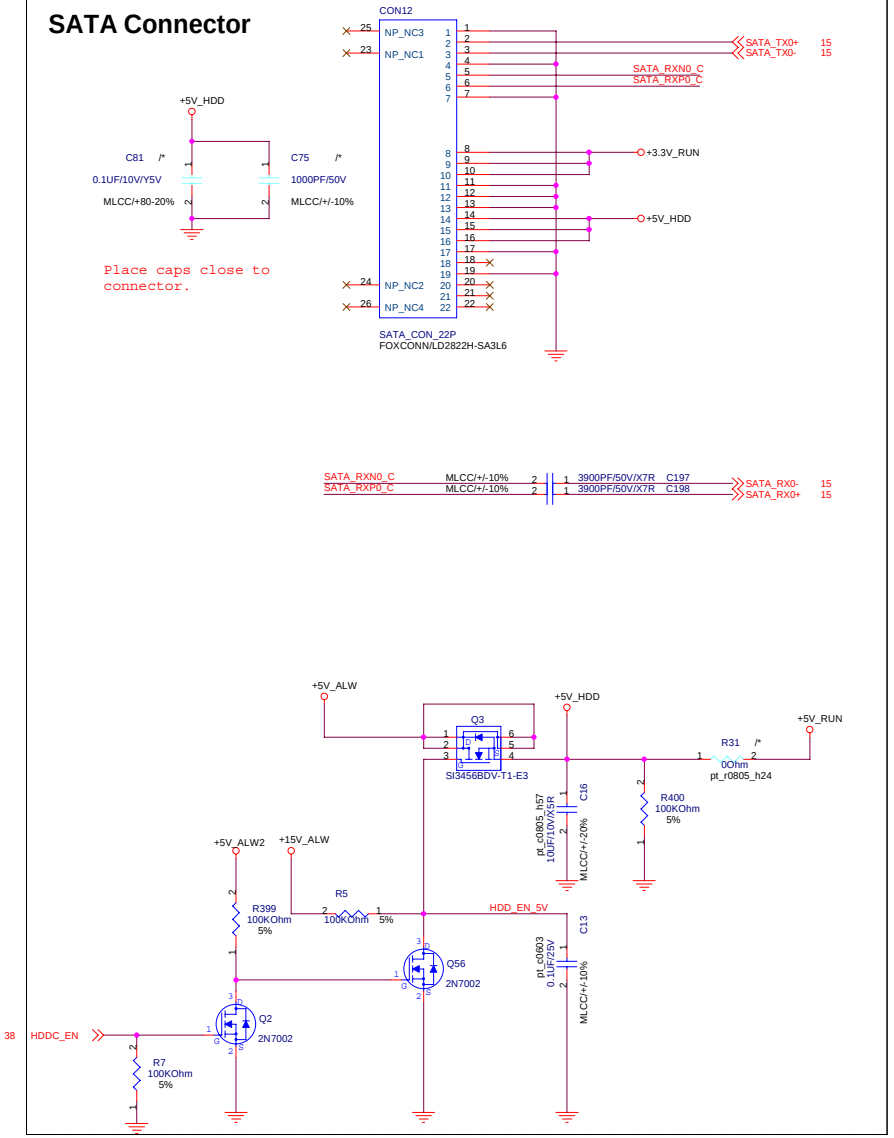
<Variant Name>

PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***VGA CRT CON***	SCHEMATIC FILE NAME :	DESIGN ENGINEER : ***Sean Kuo***
		SHEET **29** OF **69**		RELEASE DATE :	

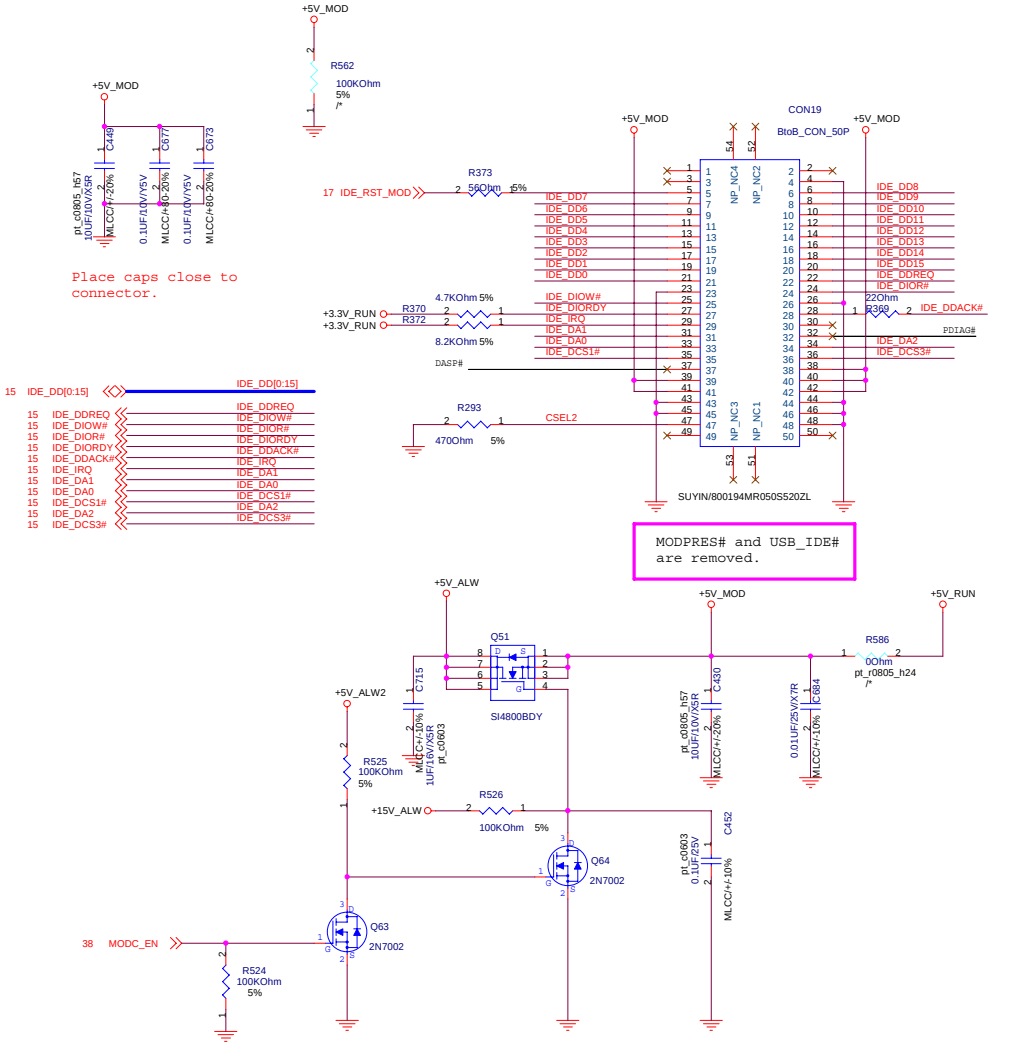
<Variant Name>

PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***TV OUT CON***	SCHEMATIC FILE NAME :		DESIGN ENGINEER : ***Sean Kuo***
		SHEET **30** OF **69**		RELEASE DATE :		

SATA Connector

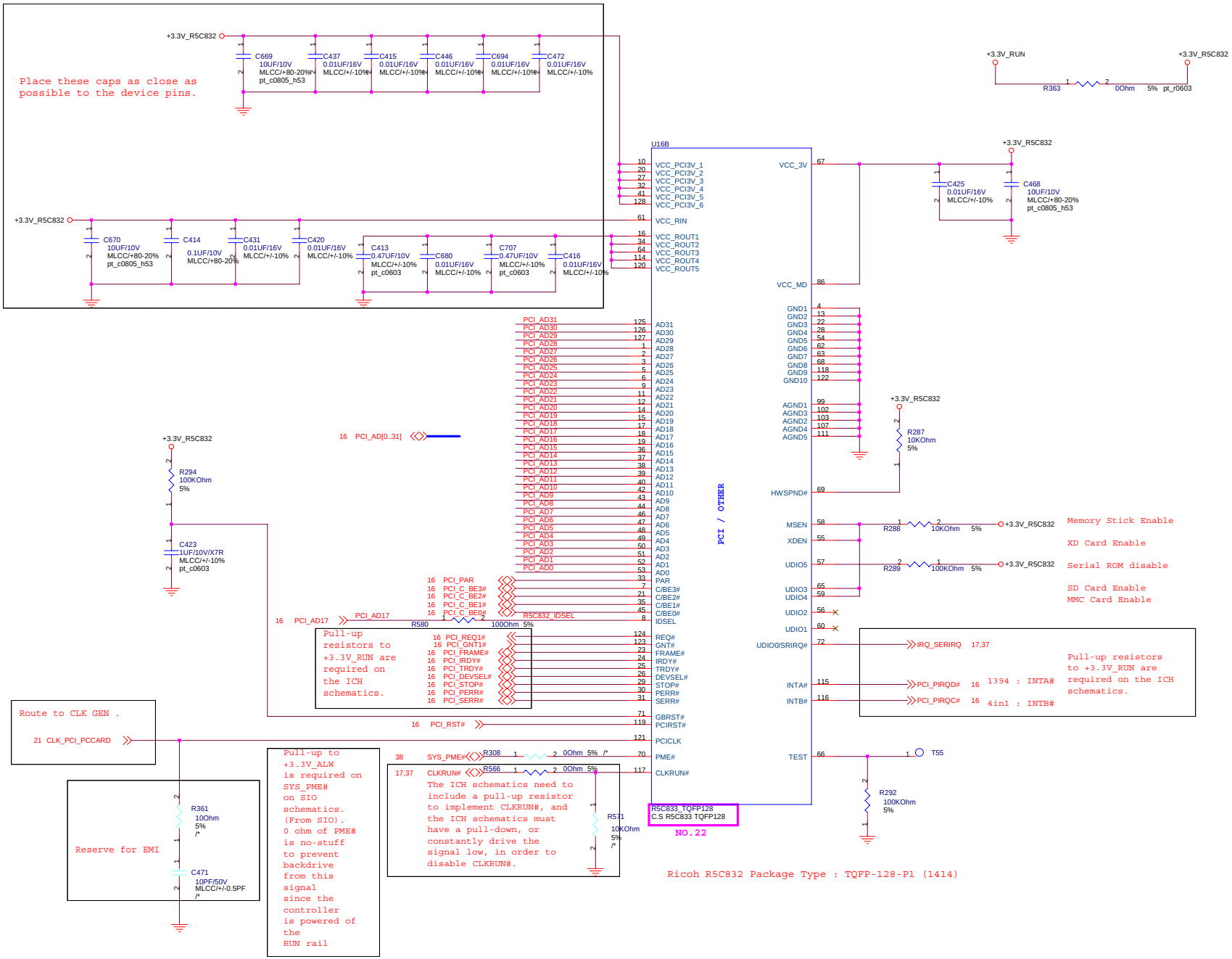


ODD Connector



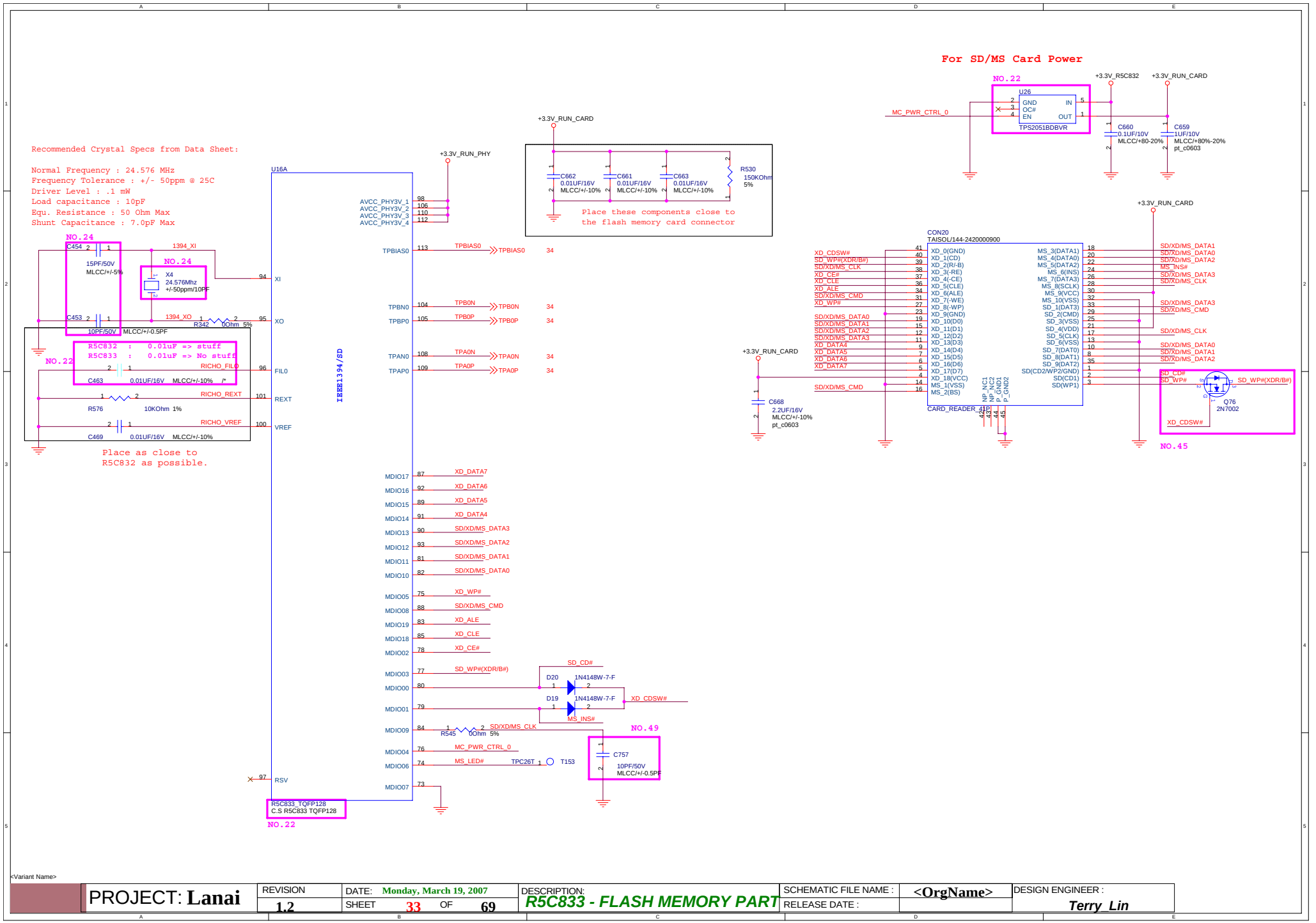
<Variant Name>

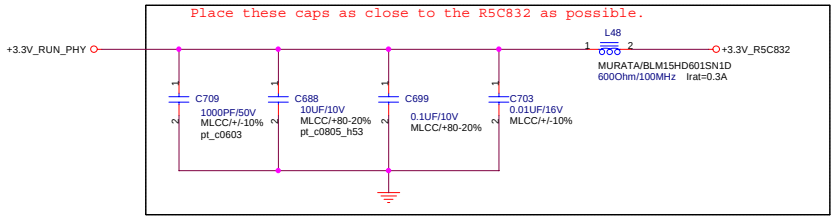
PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***SATA (HDD & CD_ROM)***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : ***Yihao Yeh***
		SHEET **31** OF **69**		RELEASE DATE :	

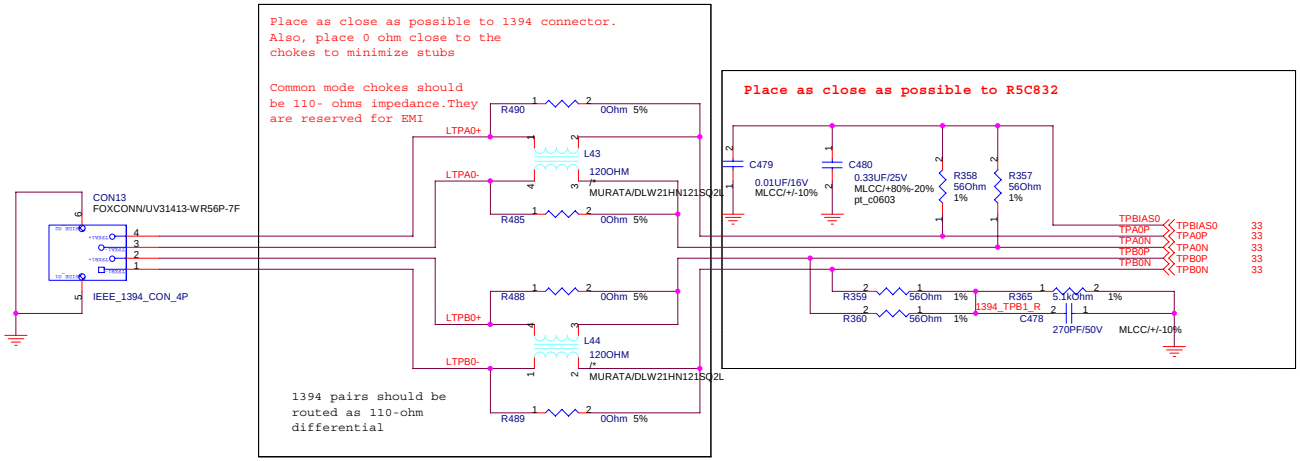


<Variant Name>

PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007** SHEET **32** OF **69**	DESCRIPTION: ***R5C833 - PCI INTERFACE***	SCHEMATIC FILE NAME : **<OrgName>** RELEASE DATE :	DESIGN ENGINEER : ***Terry_Lin***


For SD/MS Card Power
Recommended Crystal Specs from Data Sheet:
Normal Frequency : 24.576 MHz
Frequency Tolerance : +/- 50ppm @ 25C
Driver Level : .1 mW
Load capacitance : 10pF
Equ. Resistance : 50 Ohm Max
Shunt Capacitance : 7.0pF Max
R5C832 : 0.01uF => stuff
R5C833 : 0.01uF => No stuff
Place as close to R5C832 as possible.
Place these components close to the flash memory card connector
U16A
IEEE1394/SD
R5C833_TQFP128
C:\ R5C833 TQFP128
CON20
TAISOL/144-2420000900
CARD_READER_4IN1
TPS2051BDBVR
Q76
2N7002
T153
D20
D19
1N4148W-7-F
NO.22
NO.24
NO.45
NO.49
+3.3V_RUN_CARD
+3.3V_RUN_PHY
+3.3V_R5C832
<Variant Name>
PROJECT: Lanai
REVISION 1.2
DATE: Monday, March 19, 2007
SHEET 33 OF 69
DESCRIPTION: R5C833 - FLASH MEMORY PART
SCHEMATIC FILE NAME : <OrgName>
RELEASE DATE :
DESIGN ENGINEER : Terry_Lin

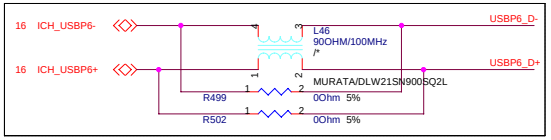


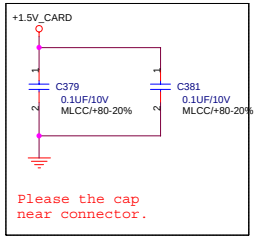


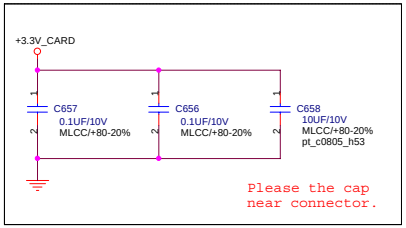
<Variant Name>

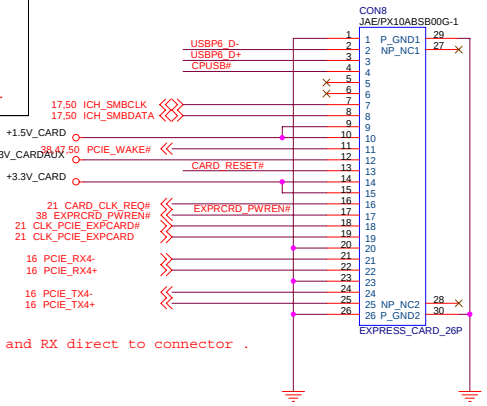
PROJECT: **Lanai**	REVISION **1.2**	DATE: Monday, March 19, 2007	DESCRIPTION: *R5C833 - IEEE1394 PART*	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : *Terry_Lin*
		SHEET **34** OF **69**		RELEASE DATE :	

Express Card



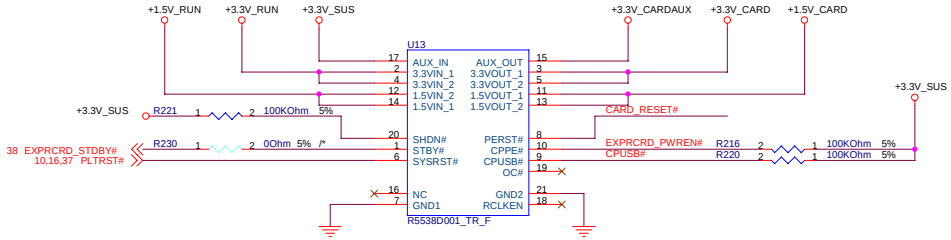


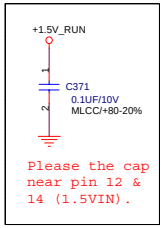


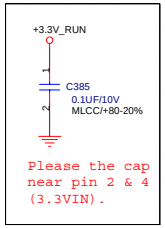


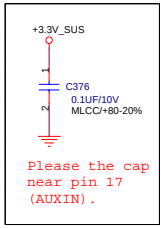
PCI-Express TX and RX direct to connector .

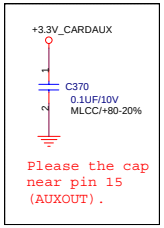
+1.5V_CARD Max. 650mA, Average 500mA.
+3V_CARD Max. 1300mA, Average 1000mA.

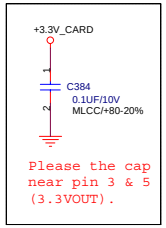


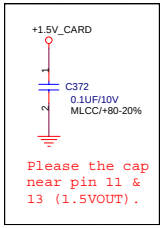






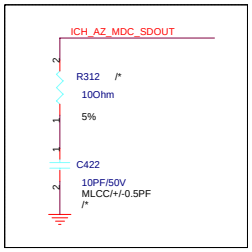


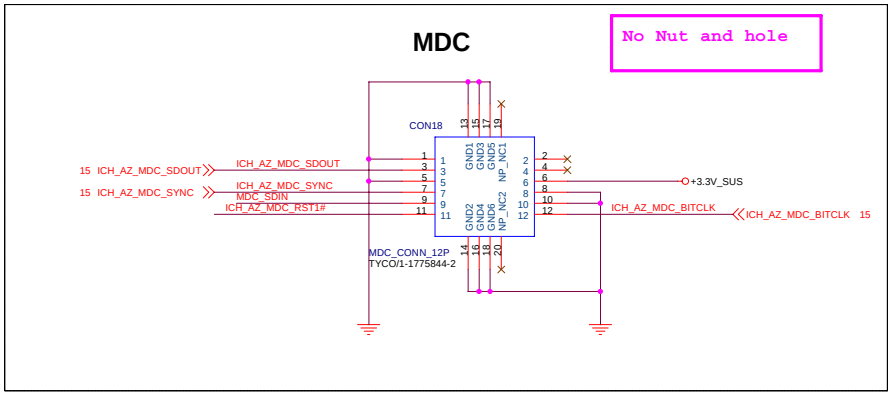


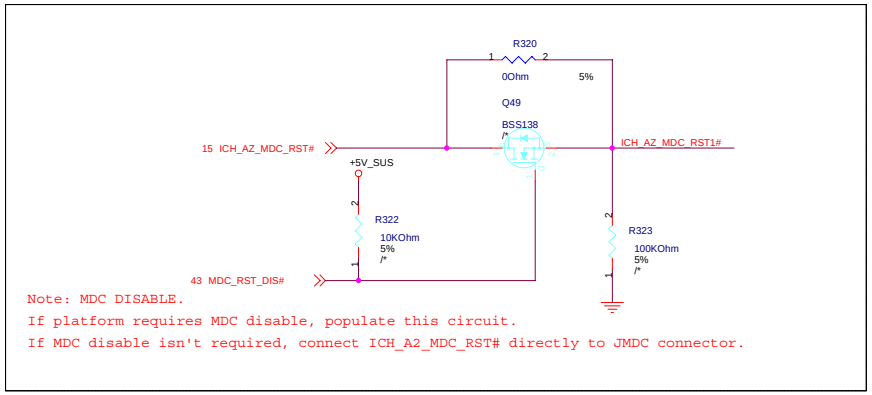


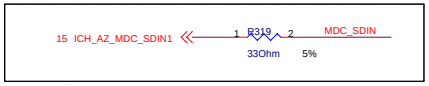
<Variant Name>

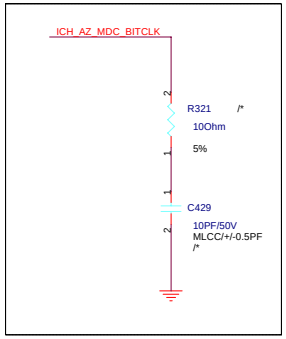
PROJECT: **Lanai**	REVISION **1.2**	DATE: Monday, March 19, 2007	DESCRIPTION: *PCI-Express Card*	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : *Terry_Lin*
		SHEET **35** OF **69**		RELEASE DATE :	

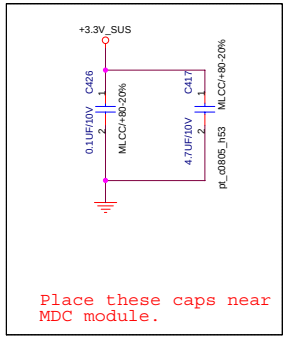






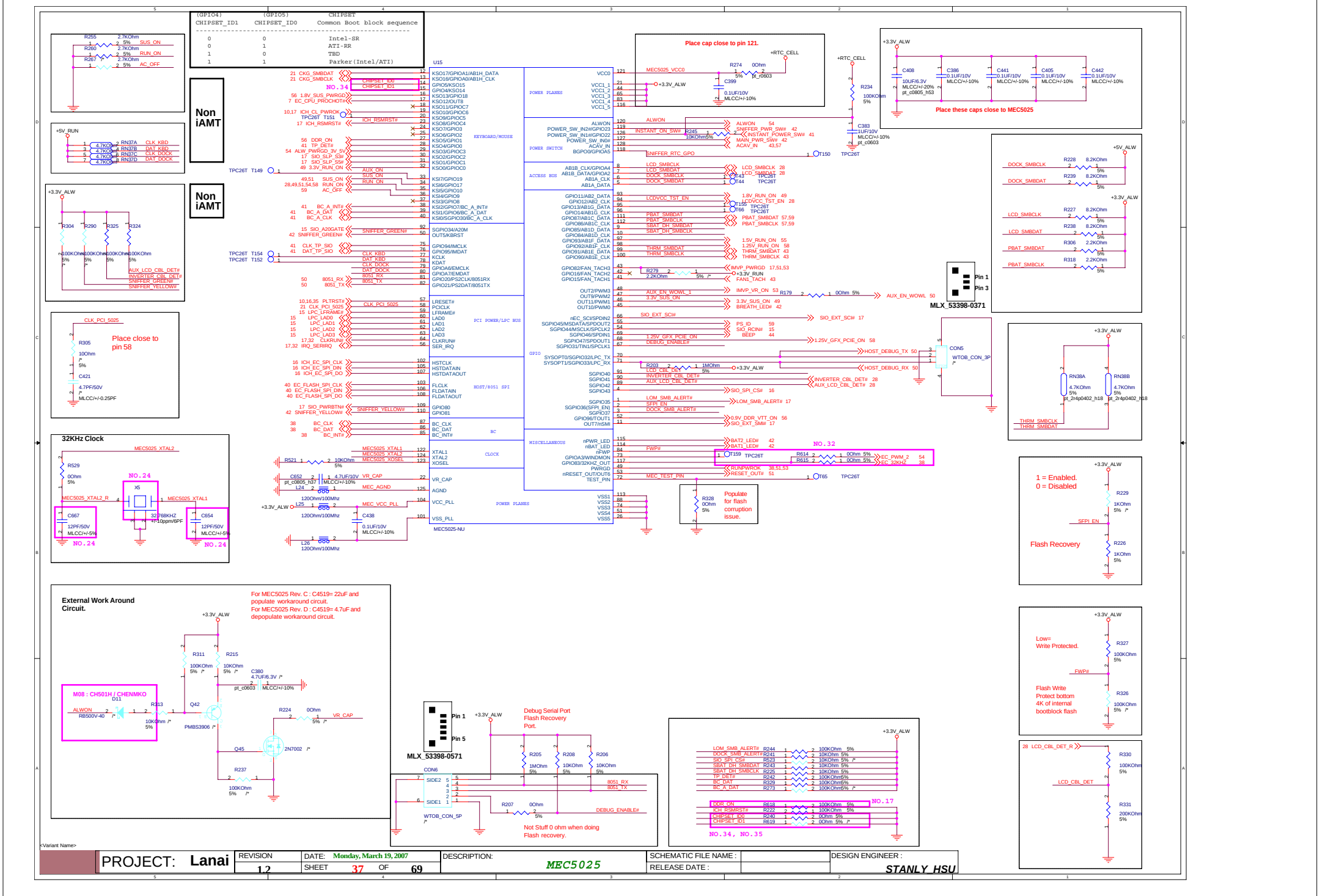


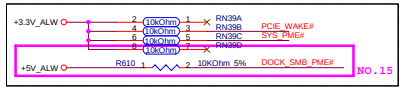


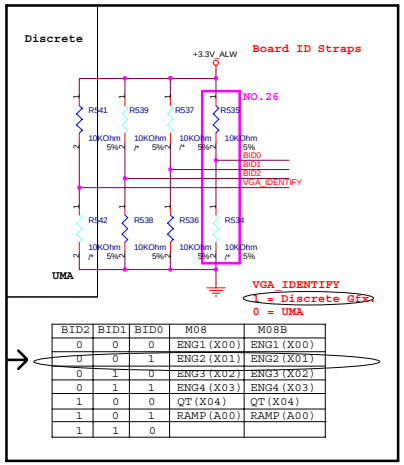


<Variant Name>

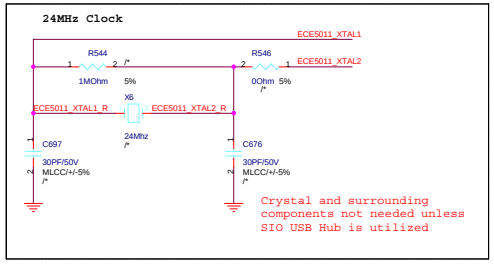
PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***MDC CONN***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : ***Yihao_Yeh***
		SHEET **36** OF **69**		RELEASE DATE :	

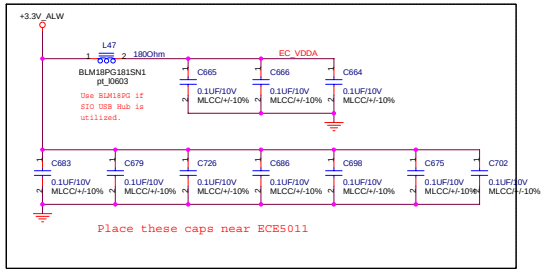

(GPIO4) (GPIO5) CHIPSET
CHIPSET_ID1 CHIPSET_ID0 Common Boot block sequence
0 0 Intel-SR
0 1 ATI-RR
1 0 TBD
1 1 Parker(Intel/ATI)
Non iAMT
Non iAMT
NO.34
Place cap close to pin 121.
Place these caps close to MEC5025
Place close to pin 58
32KHz Clock
NO.24
NO.32
NO.17
NO.34, NO.35
Pin 1
Pin 3
MLX_53398-0371
Pin 1
Pin 5
MLX_53398-0371
Populate for flash corruption issue.
1 = Enabled.
0 = Disabled
Flash Recovery
Low= Write Protected.
Flash Write Protect bottom 4K of internal bootblock flash
External Work Around Circuit.
For MEC5025 Rev. C : C4519= 22uF and populate workaround circuit.
For MEC5025 Rev. D : C4519= 4.7uF and depopulate workaround circuit.
Debug Serial Port Flash Recovery Port.
Not Stuff 0 ohm when doing Flash recovery.
MEC5025-NU
U15
PROJECT: Lanai
REVISION 1.2
DATE: Monday, March 19, 2007
SHEET 37 OF 69
DESCRIPTION: MEC5025
SCHEMATIC FILE NAME :
RELEASE DATE :
DESIGN ENGINEER : STANLY_HSU

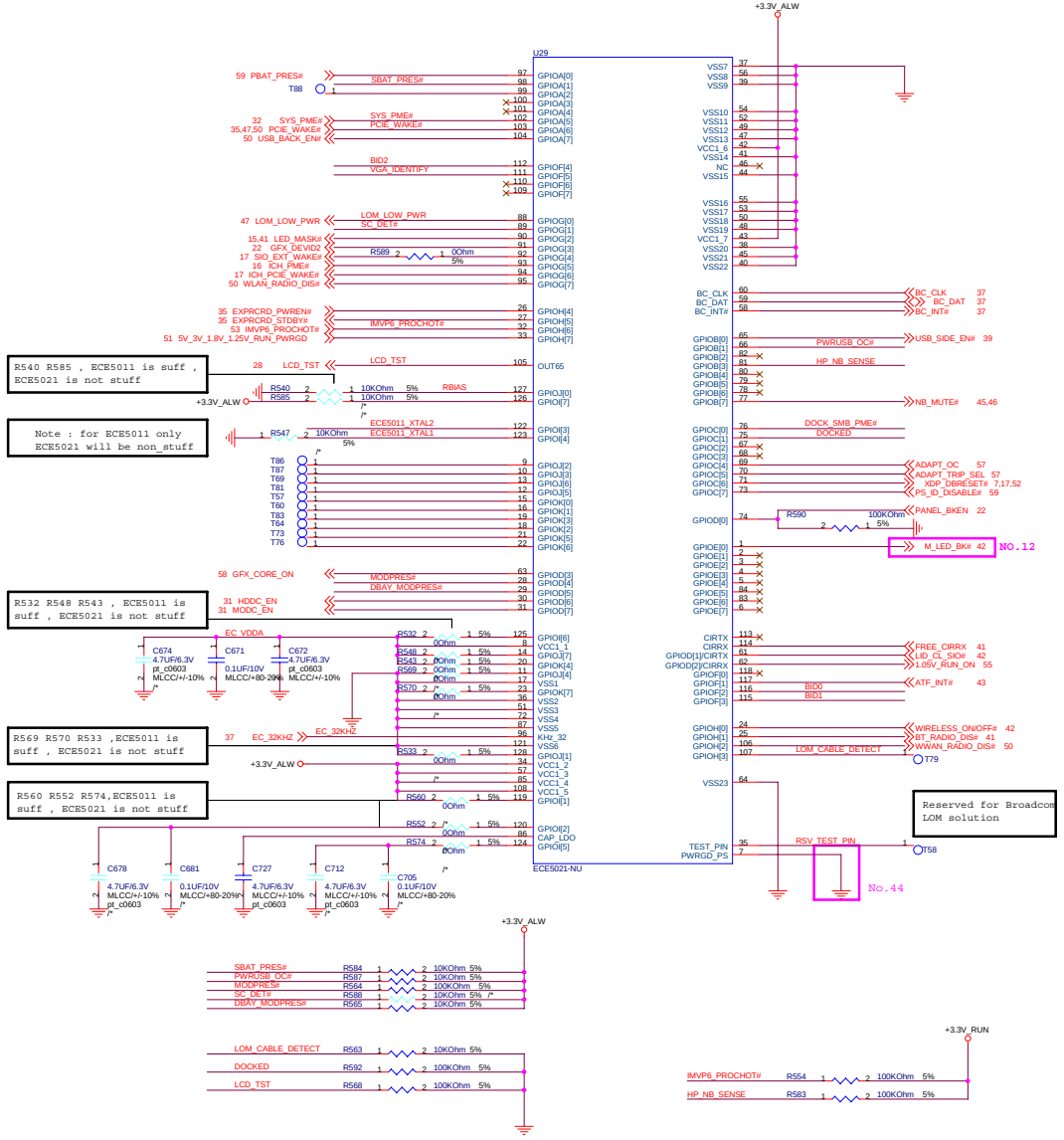




BID2	BID1	BID0	M08	M08B
0	0	0	ENG1(X00)	ENG1(X00)
0	0	1	ENG2(X01)	ENG2(X01)
0	1	0	ENG3(X02)	ENG3(X02)
0	1	1	ENG4(X03)	ENG4(X03)
1	0	0	QT(X04)	QT(X04)
1	0	1	RAMP(A00)	RAMP(A00)
1	1	0		

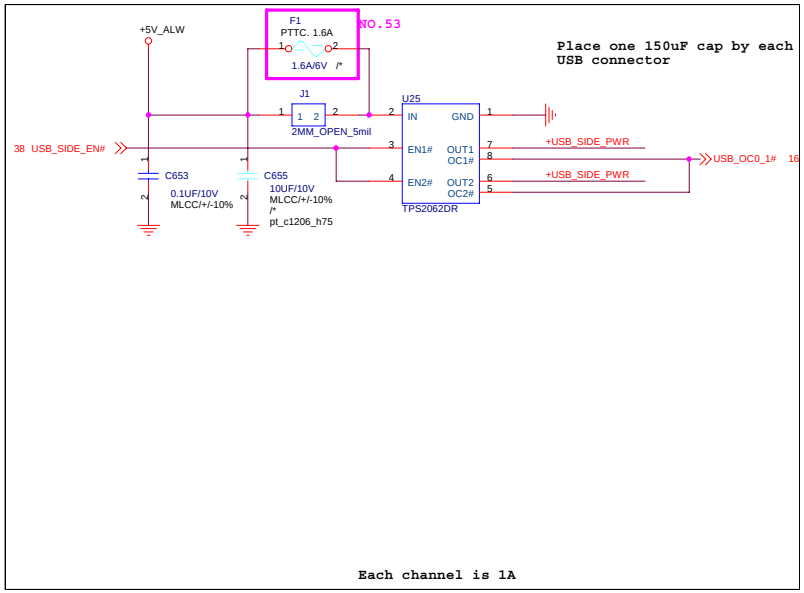


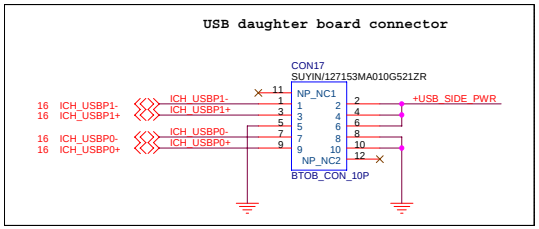




<Variant Name>

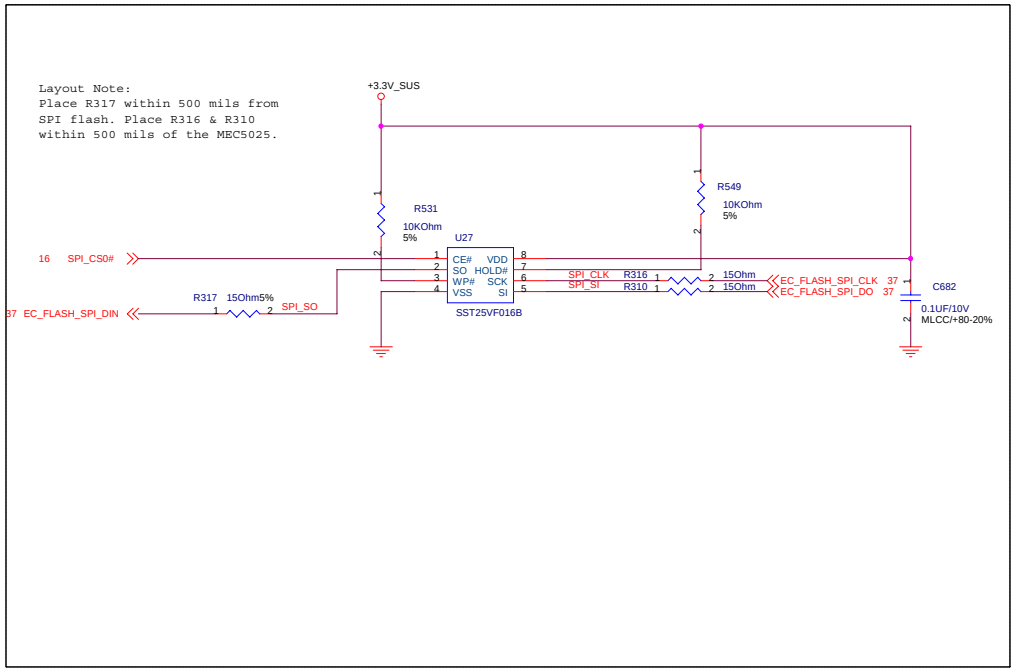
PROJECT: Lanai	REVISION 1.2	DATE: Monday, March 19, 2007	SHEET 38 OF 69	DESCRIPTION: ECE5021	SCHEMATIC FILE NAME :	RELEASE DATE :	DESIGN ENGINEER : STANLY_HSU

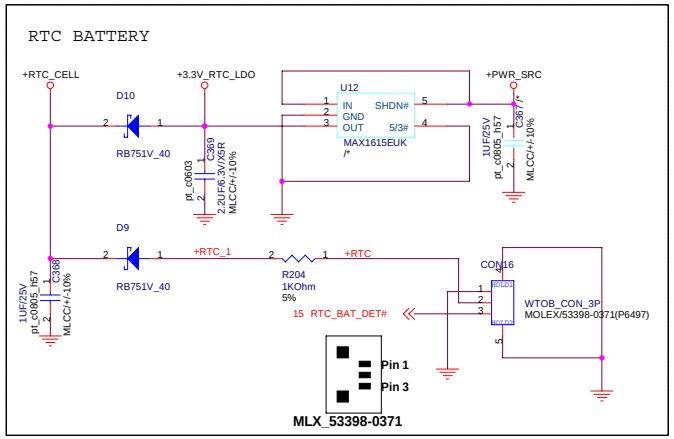




<Variant Name>

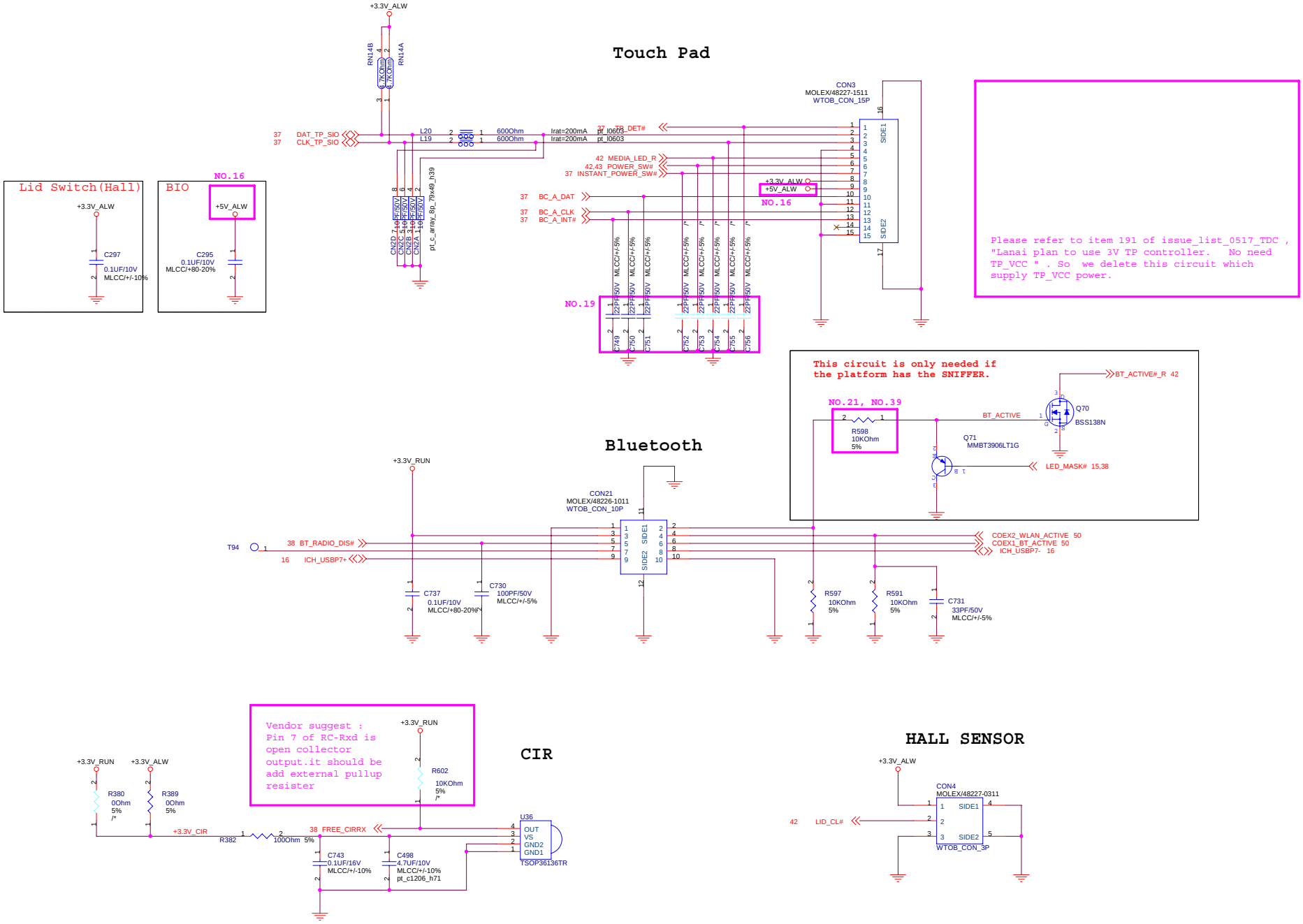
PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***USB PORT x 2***	SCHEMATIC FILE NAME :	**<OrgName>**	DESIGN ENGINEER : ***Terry_Lin***
		SHEET **39** OF **69**		RELEASE DATE :		





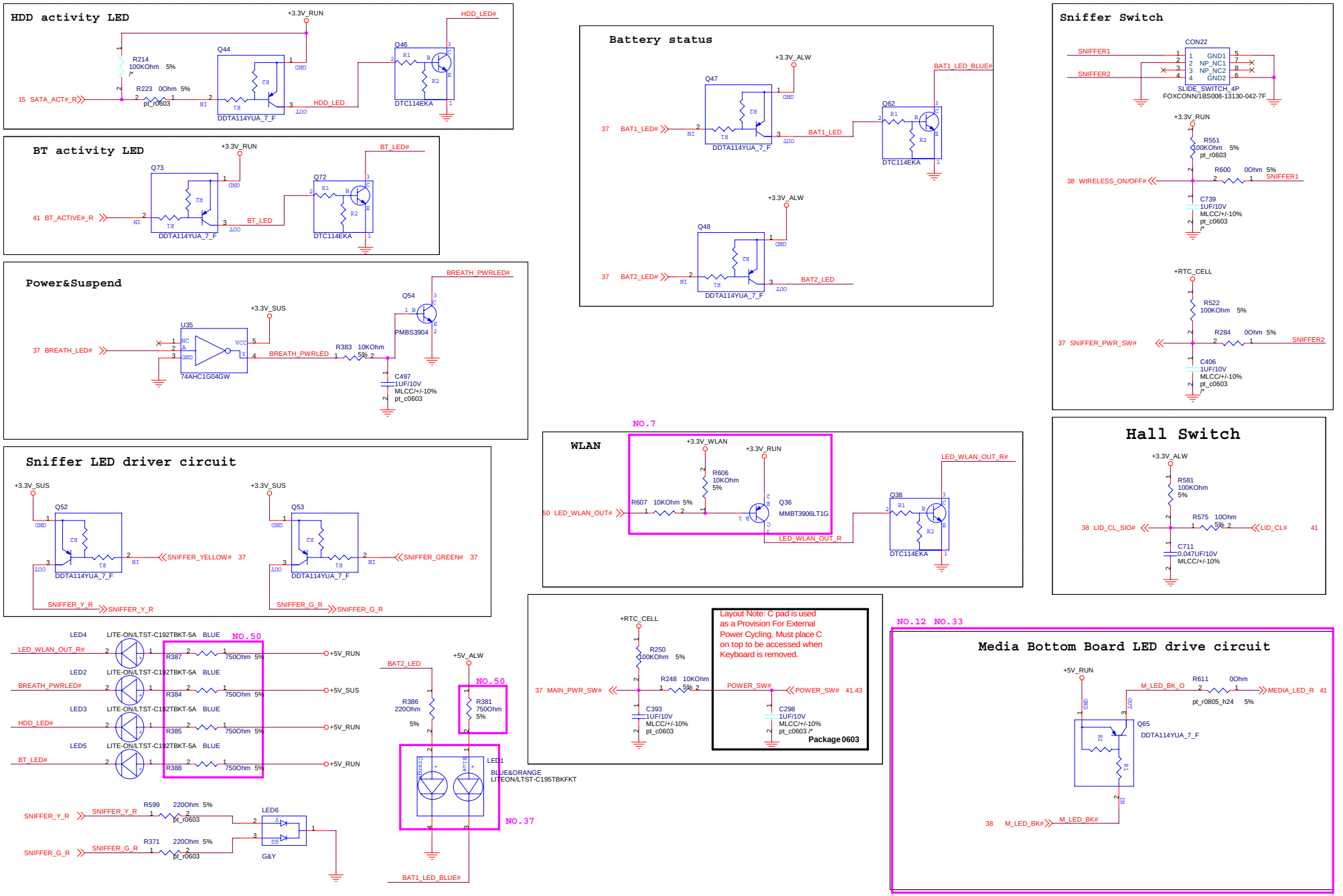
<Variant Name>

PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***FLASH & RTC***	SCHEMATIC FILE NAME :	**<OrgName>**	DESIGN ENGINEER : ***C.L. Ho***
		SHEET **40** OF **69**		RELEASE DATE :		



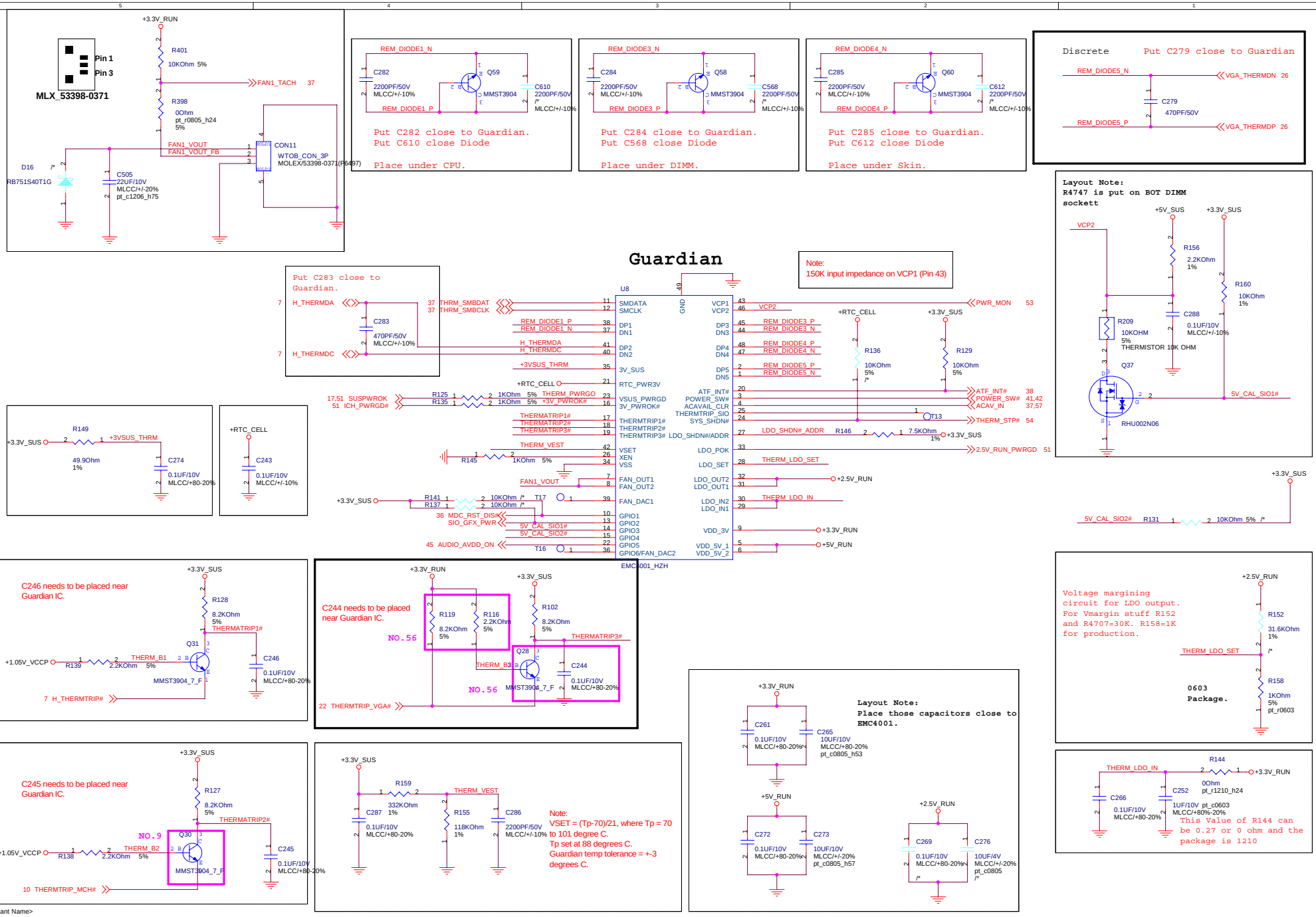
<Variant Name>

PROJECT: Lanai	REVISION	DATE: Monday, March 19, 2007	DESCRIPTION: TOUCH PAD & BT & CIR & HALL	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER : Terry_Lin
	1.2	SHEET 41 OF 69		RELEASE DATE :	



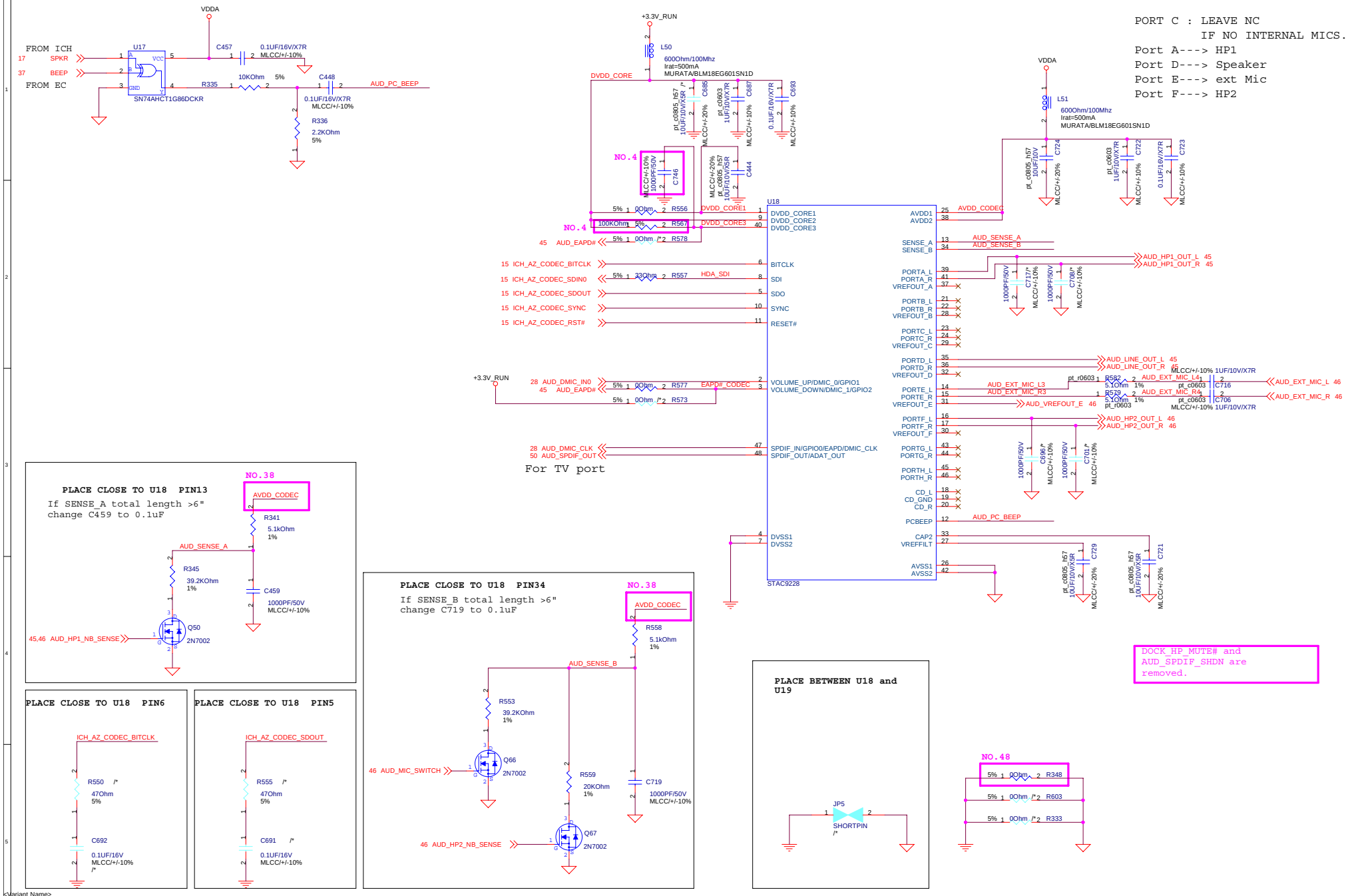
<Variant Name>

PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***SWITCH & LED***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : ***Ivan_Chou***
		SHEET **42** OF **69**		RELEASE DATE :	

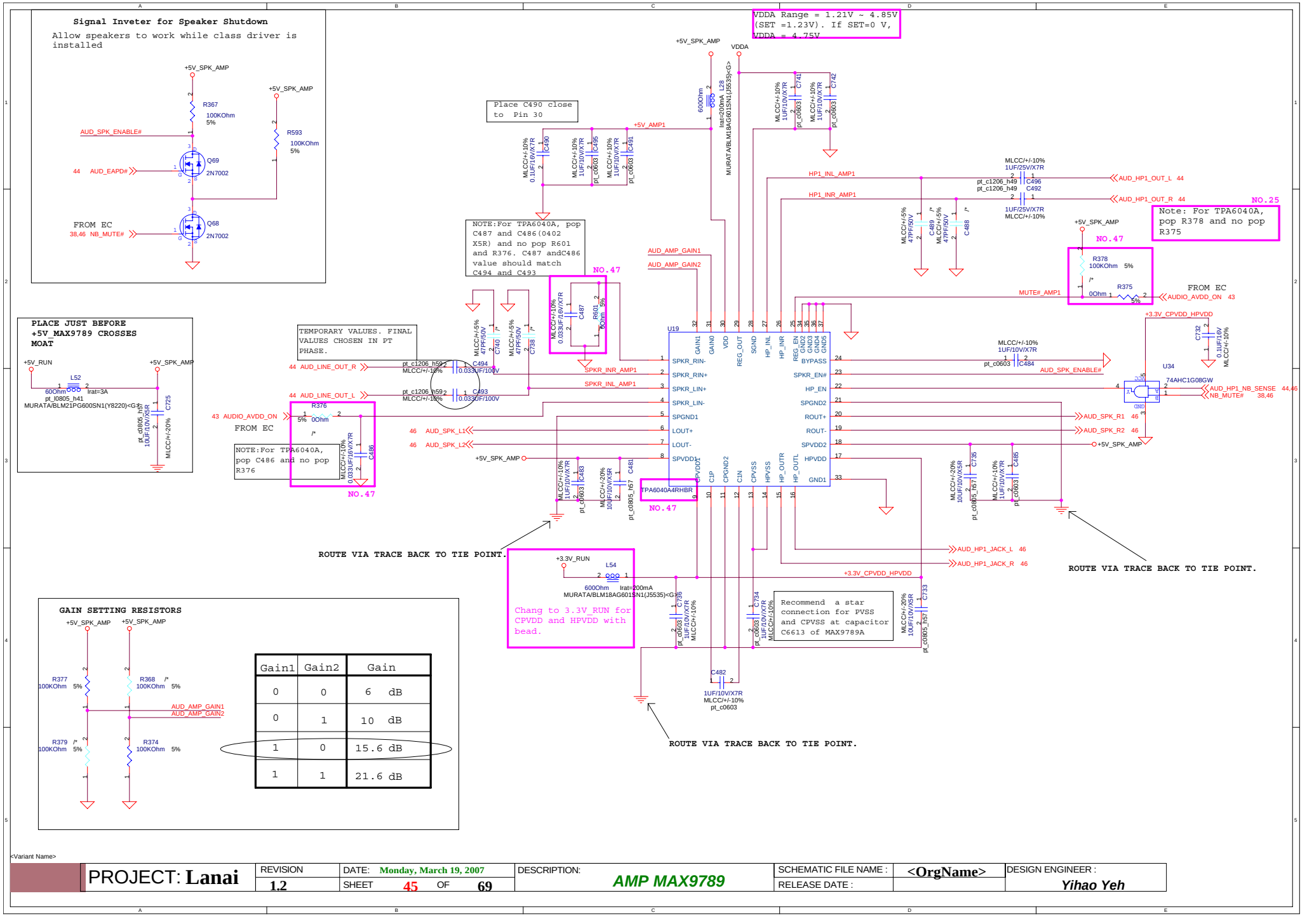


<Variant Name>

PROJECT: Lanai	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: EMC4001	SCHEMATIC FILE NAME :	DESIGN ENGINEER : STANLY_HSU
		SHEET 43 OF 69		RELEASE DATE :	

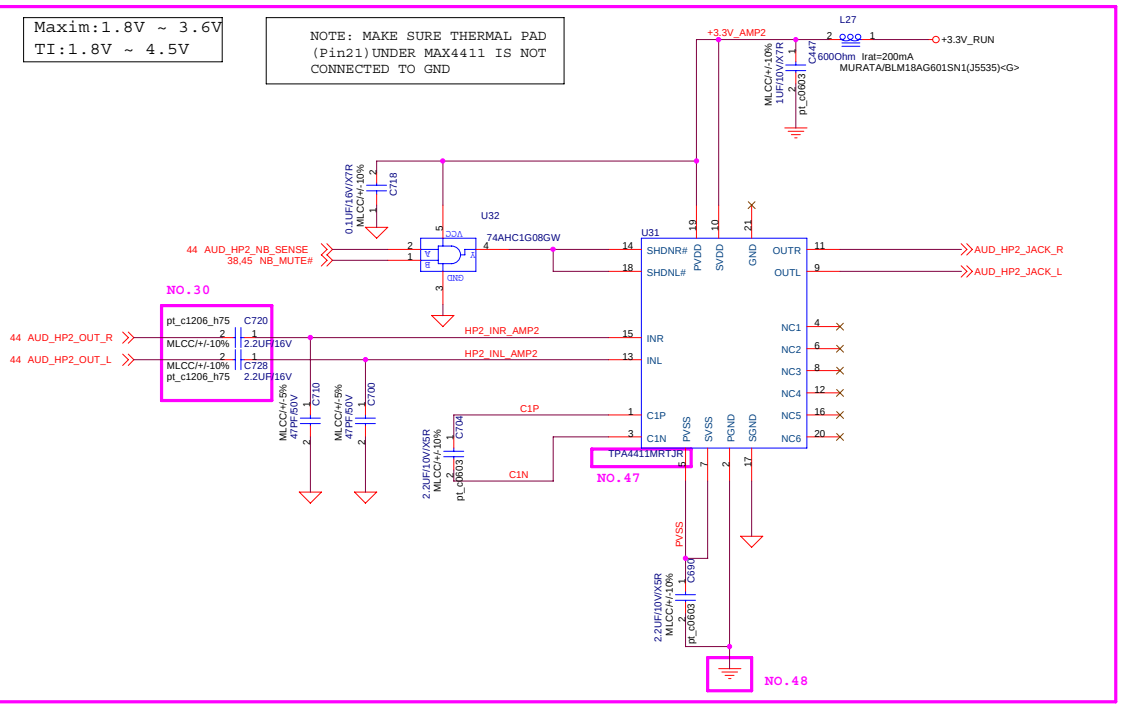


<Variant Name>					
PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***STAC9228***	SCHEMATIC FILE NAME :	DESIGN ENGINEER : ***Yihao Yeh***
		SHEET **44** OF **69**		RELEASE DATE :	

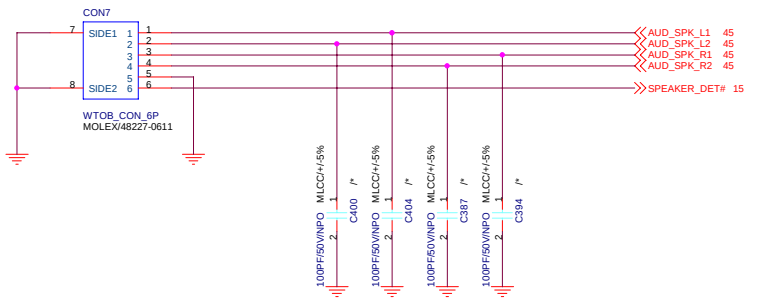

Signal Inveter for Speaker Shutdown
Allow speakers to work while class driver is installed
+5V_SPK_AMP
R367
100KOhm
5%
AUD_SPK_ENABLE#
Q69
2N7002
44 AUD_EAPD#
R593
100KOhm
5%
FROM EC
38,46 NB_MUTE#
Q68
2N7002
VDDA Range = 1.21V ~ 4.85V
(SET =1.23V). If SET=0 V,
VDDA = 4.75V
Place C490 close to Pin 30
NOTE:For TPA6040A, pop C487 and C486(0402 X5R) and no pop R601 and R376. C487 andC486 value should match C494 and C493
NO.47
TEMPORARY VALUES. FINAL VALUES CHOSEN IN PT PHASE.
PLACE JUST BEFORE +5V_MAX9789 CROSSES MOAT
NOTE:For TPA6040A, pop C486 and no pop R376
NO.25
Note: For TPA6040A, pop R378 and no pop R375
ROUTE VIA TRACE BACK TO TIE POINT.
Chang to 3.3V_RUN for CPVDD and HPVDD with bead.
Recommend a star connection for PVSS and CPVSS at capacitor C6613 of MAX9789A
GAIN SETTING RESISTORS
Gain1 Gain2 Gain
0 0 6 dB
0 1 10 dB
1 0 15.6 dB
1 1 21.6 dB
<Variant Name>
PROJECT: Lanai
REVISION 1.2
DATE: Monday, March 19, 2007
SHEET 45 OF 69
DESCRIPTION: AMP MAX9789
SCHEMATIC FILE NAME : <OrgName>
RELEASE DATE :
DESIGN ENGINEER : Yihao Yeh

Maxim:1.8V ~ 3.6V
TI:1.8V ~ 4.5V

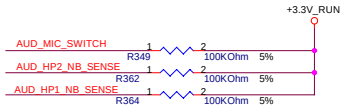
NOTE: MAKE SURE THERMAL PAD (Pin21)UNDER MAX4411 IS NOT CONNECTED TO GND

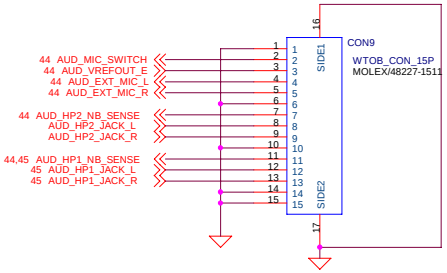


Speaker CON



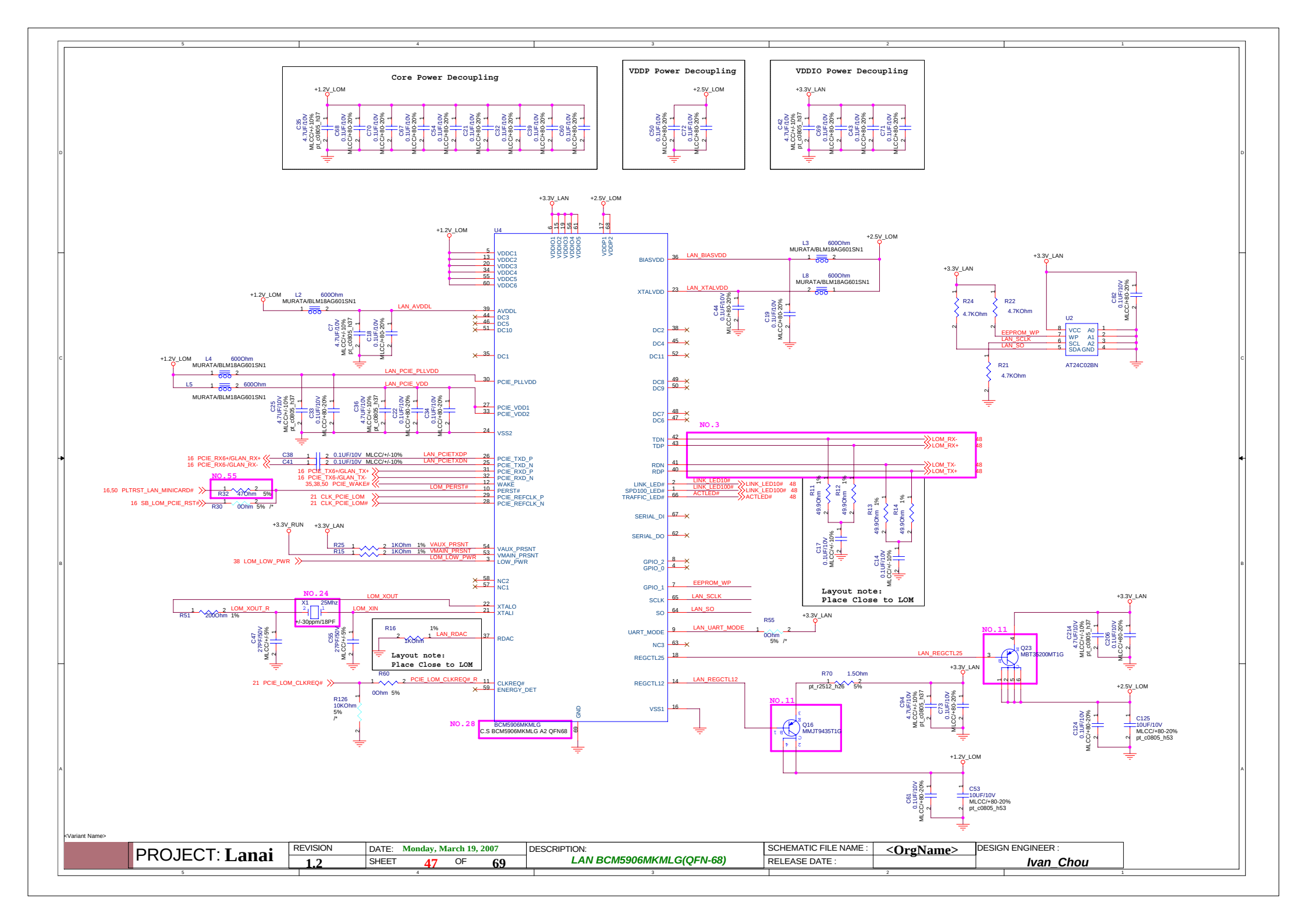
Need to adjust EMI cap values as necessary.





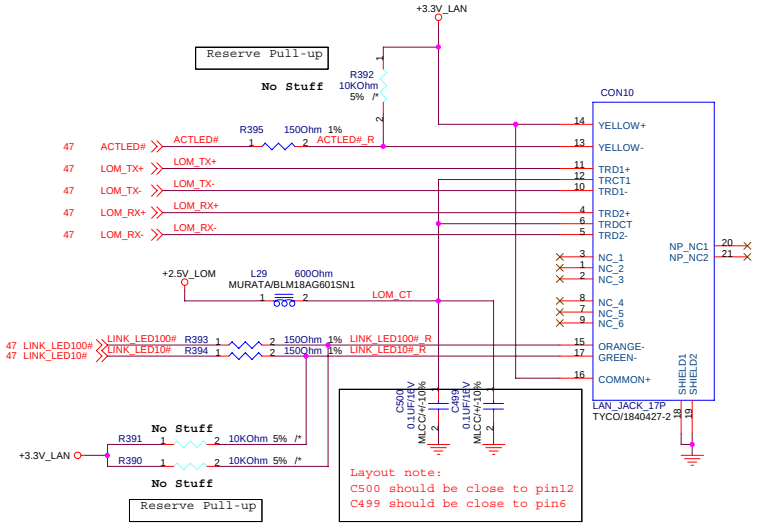
<Variant Name>

PROJECT: Lanai	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: AMP MAX4411 & AUDIO JACK	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER : Yihao Yeh
		SHEET 46 OF 69		RELEASE DATE :	



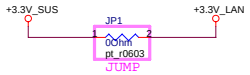
<Variant Name>

PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***LAN BCM5906MKMLG(QFN-68)***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : ***Ivan_Chou***
		SHEET **47** OF **69**		RELEASE DATE :	



+3.3V_LAN Source Guideline:

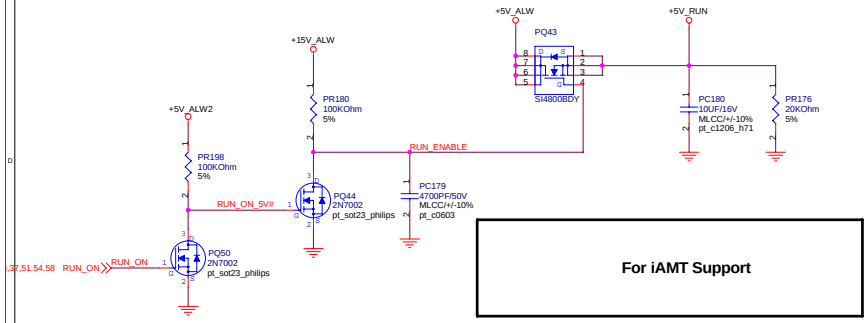
1. Use +3.3V_SUS if Wake-on-LAN is NOT required out of S4, S5
2. Use +3.3V_SRC if Wake-on-LAN is required out of S4, S5



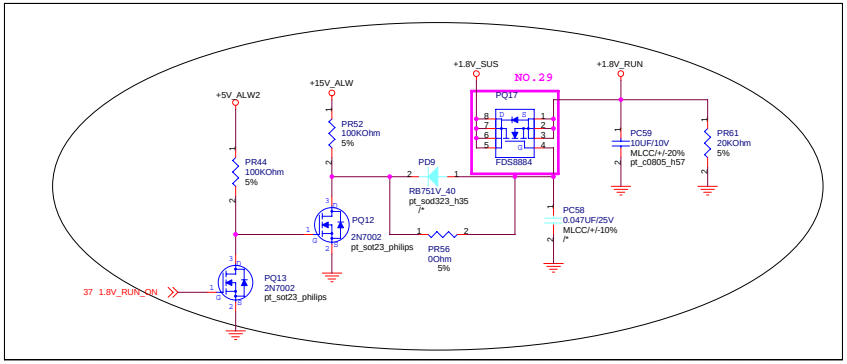
Per EE schematic checklist item.87: Only support wake up from S3

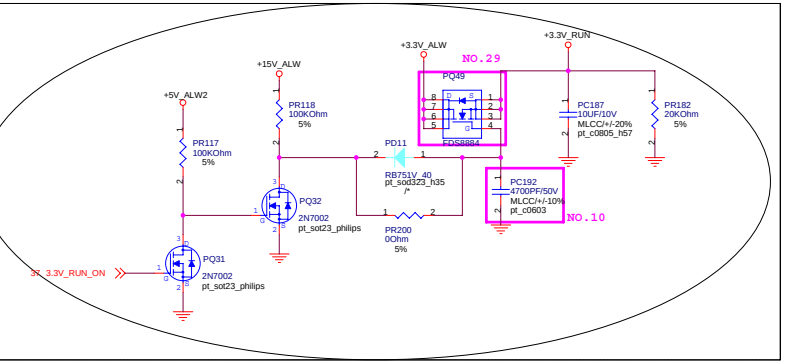
<Variant Name>

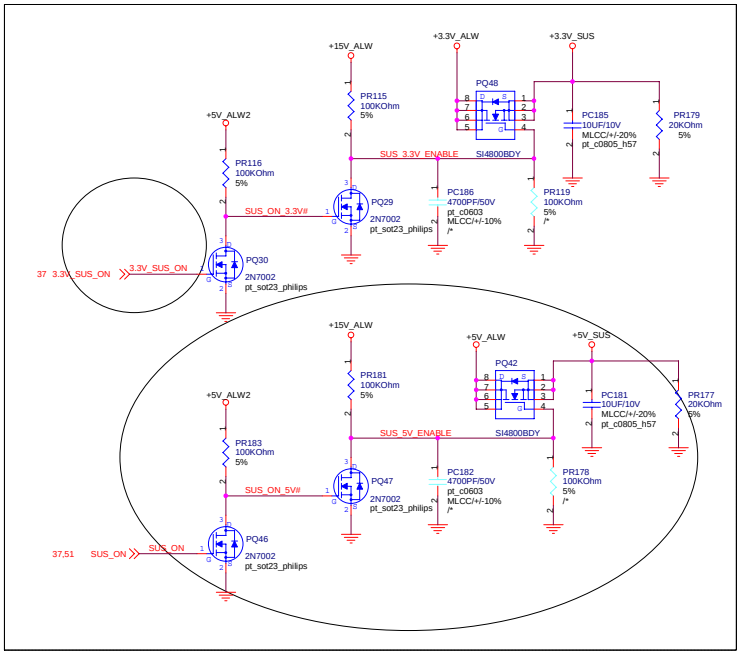
PROJECT: **Lanai**	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: ***Magnetics and RJ-45***	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
		SHEET 48 OF 69		RELEASE DATE :		*Ivan_Chou*

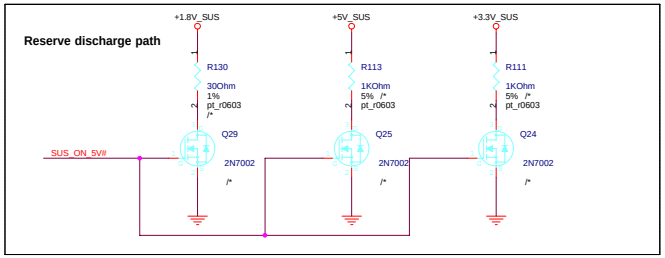


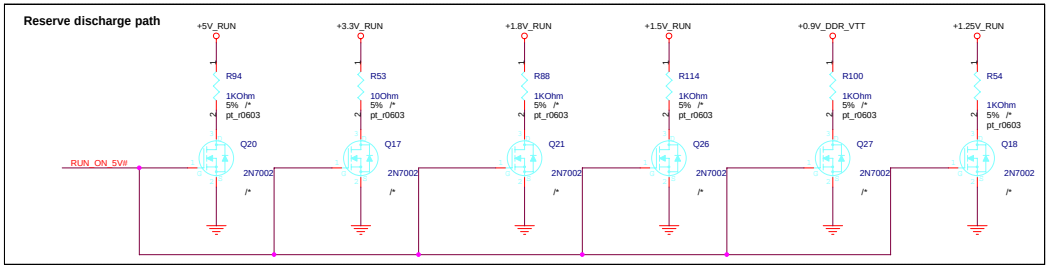
For iAMT Support









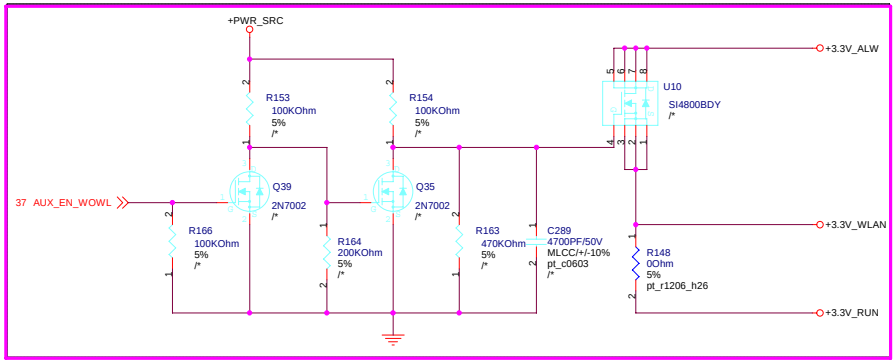


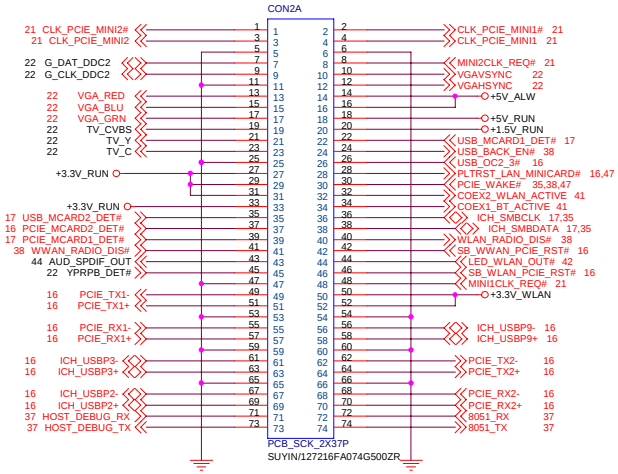
For iAMT Support

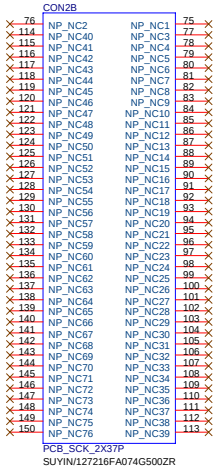
<Variant Name>

PROJECT: **Lanai**	REVISION: 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: *Power Control Switch*	SCHEMATIC FILE NAME :	DESIGN ENGINEER : **Eric Ko**
		SHEET 49 OF 69		RELEASE DATE :	

NO.20

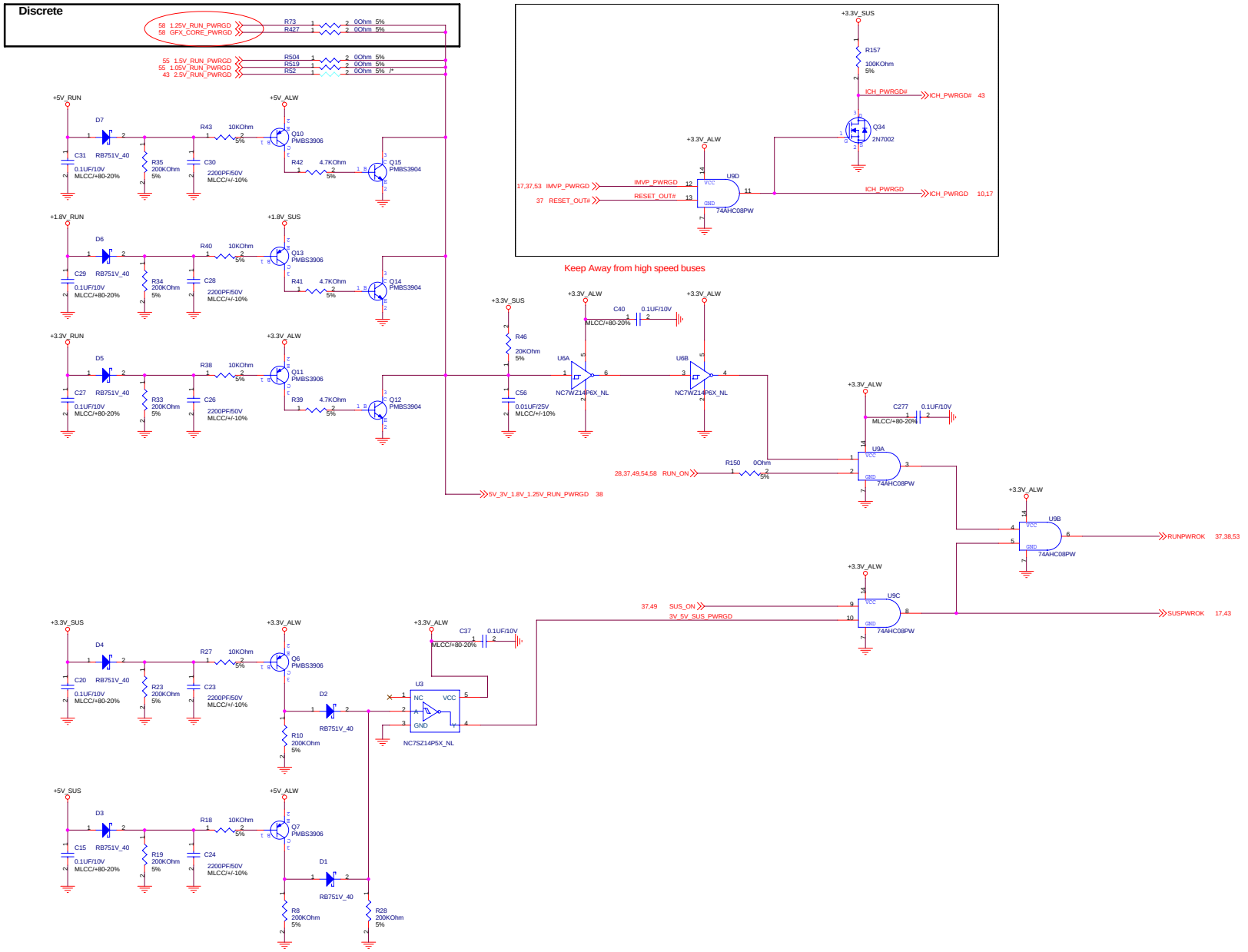






<Variant Name>

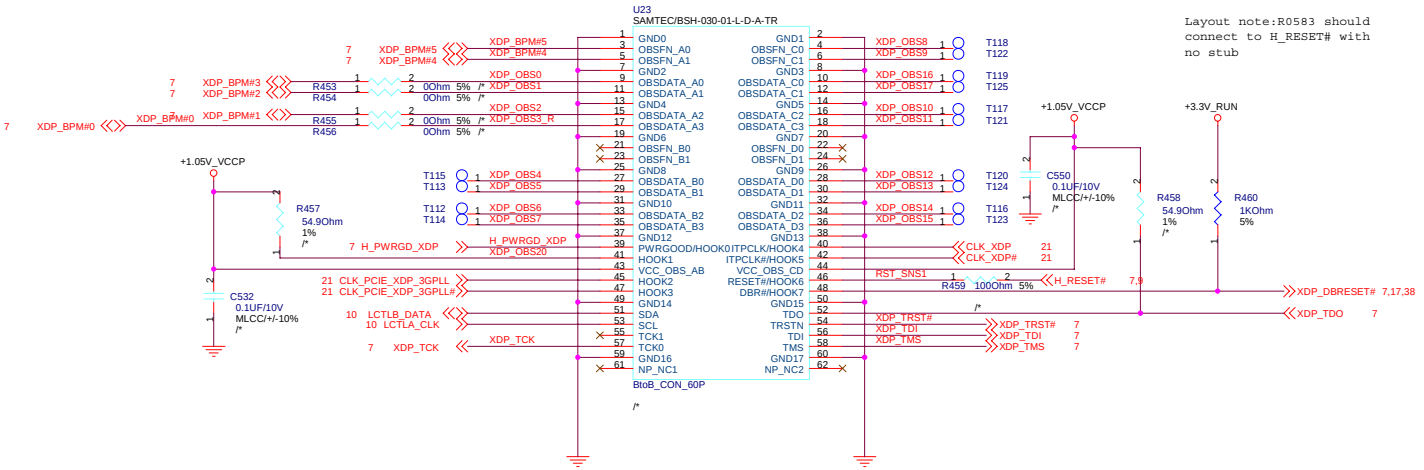
PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007** SHEET **50** OF **69**	DESCRIPTION: ***BtoB CON***	SCHEMATIC FILE NAME : **<OrgName>** RELEASE DATE :	DESIGN ENGINEER : ***STANLY_HSU***



<Variant Name>

PROJECT: Lanai	REVISION 1.2	DATE: Monday, March 19, 2007	SHEET 51 OF 69	DESCRIPTION: Power Sequence Logic	SCHEMATIC FILE NAME :	RELEASE DATE :	DESIGN ENGINEER : C.L. Ho

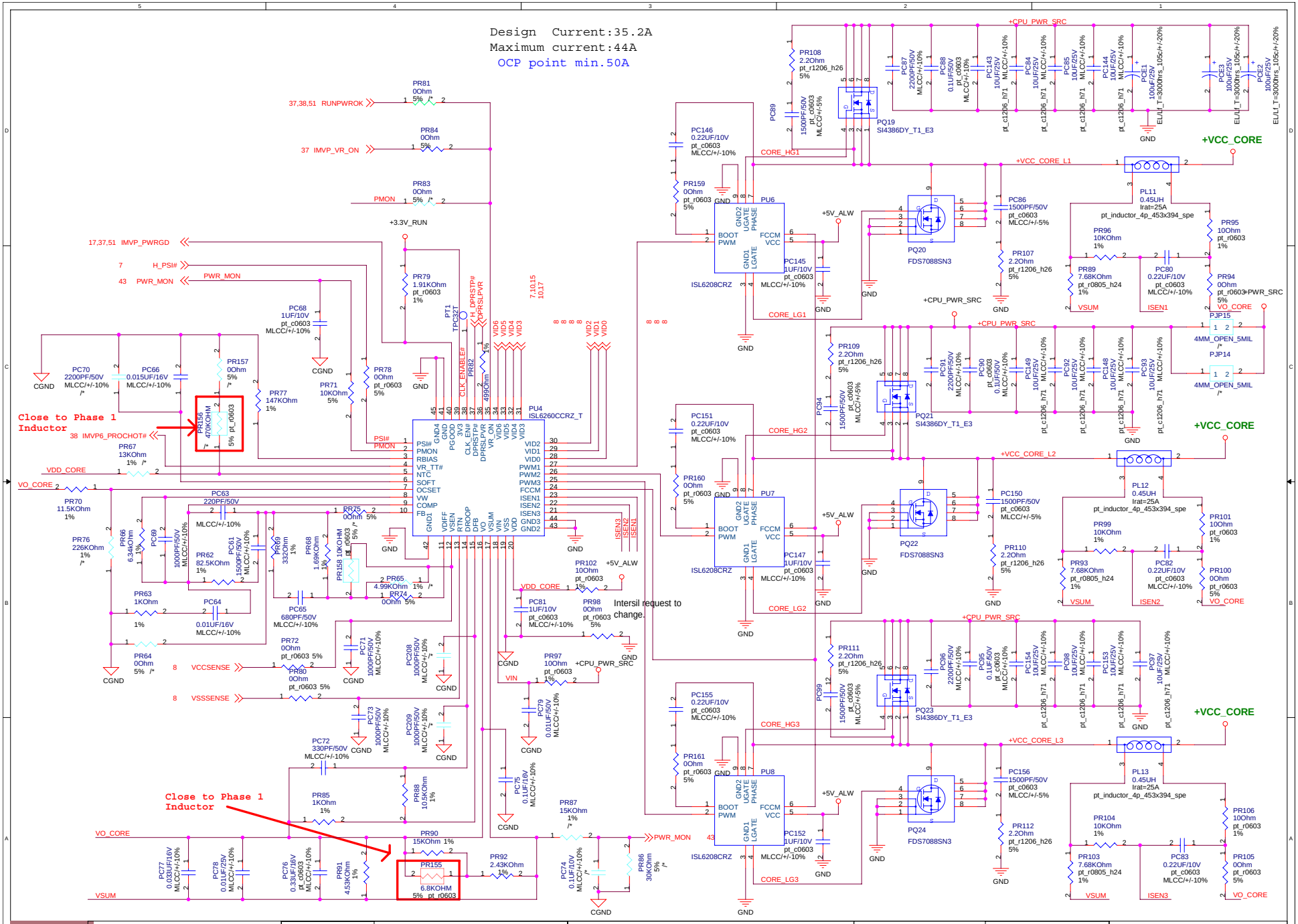
XDP



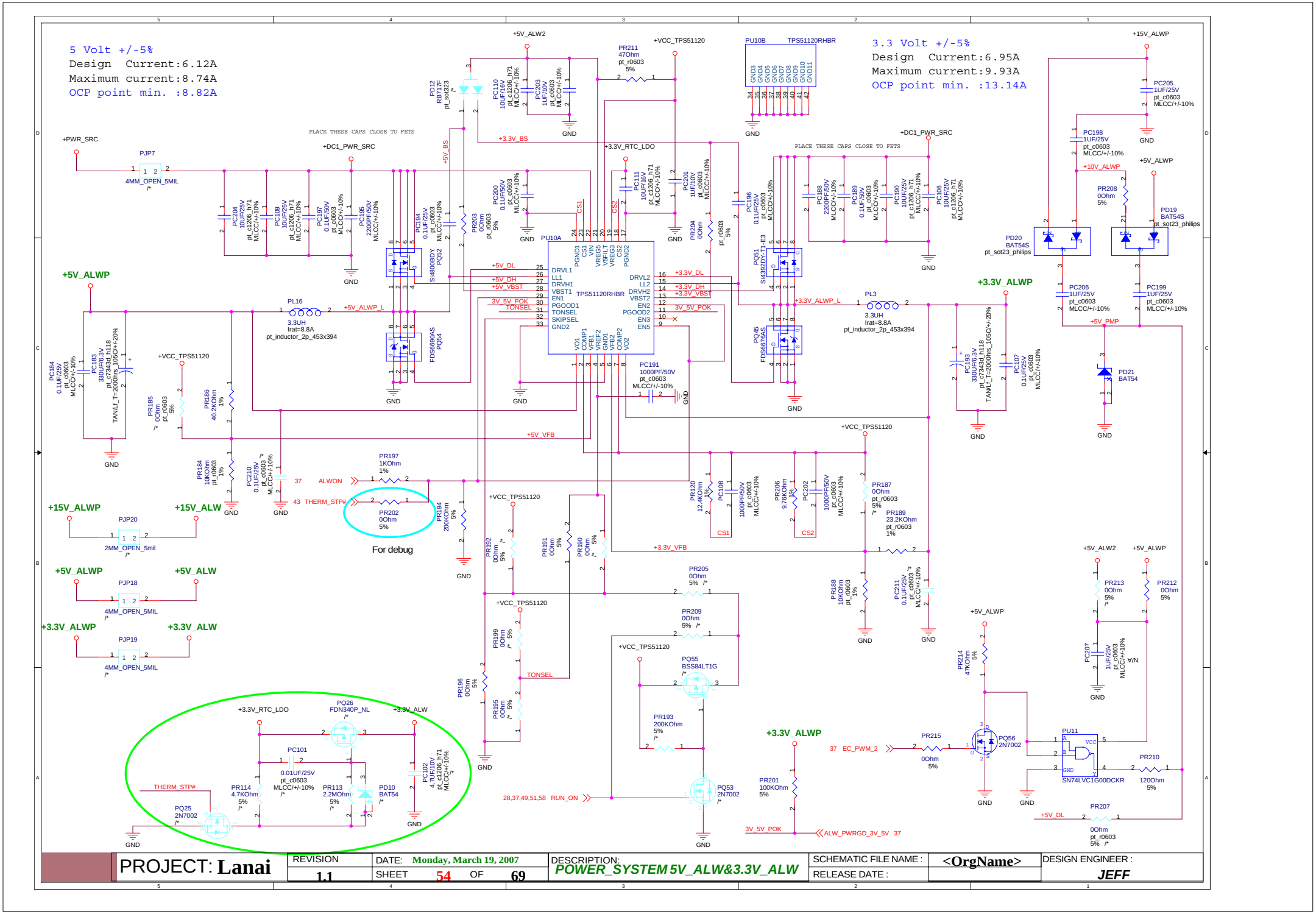
CAD NOTE:
Place the XDP connector on the primary side of the CRB and place all components near the connector.

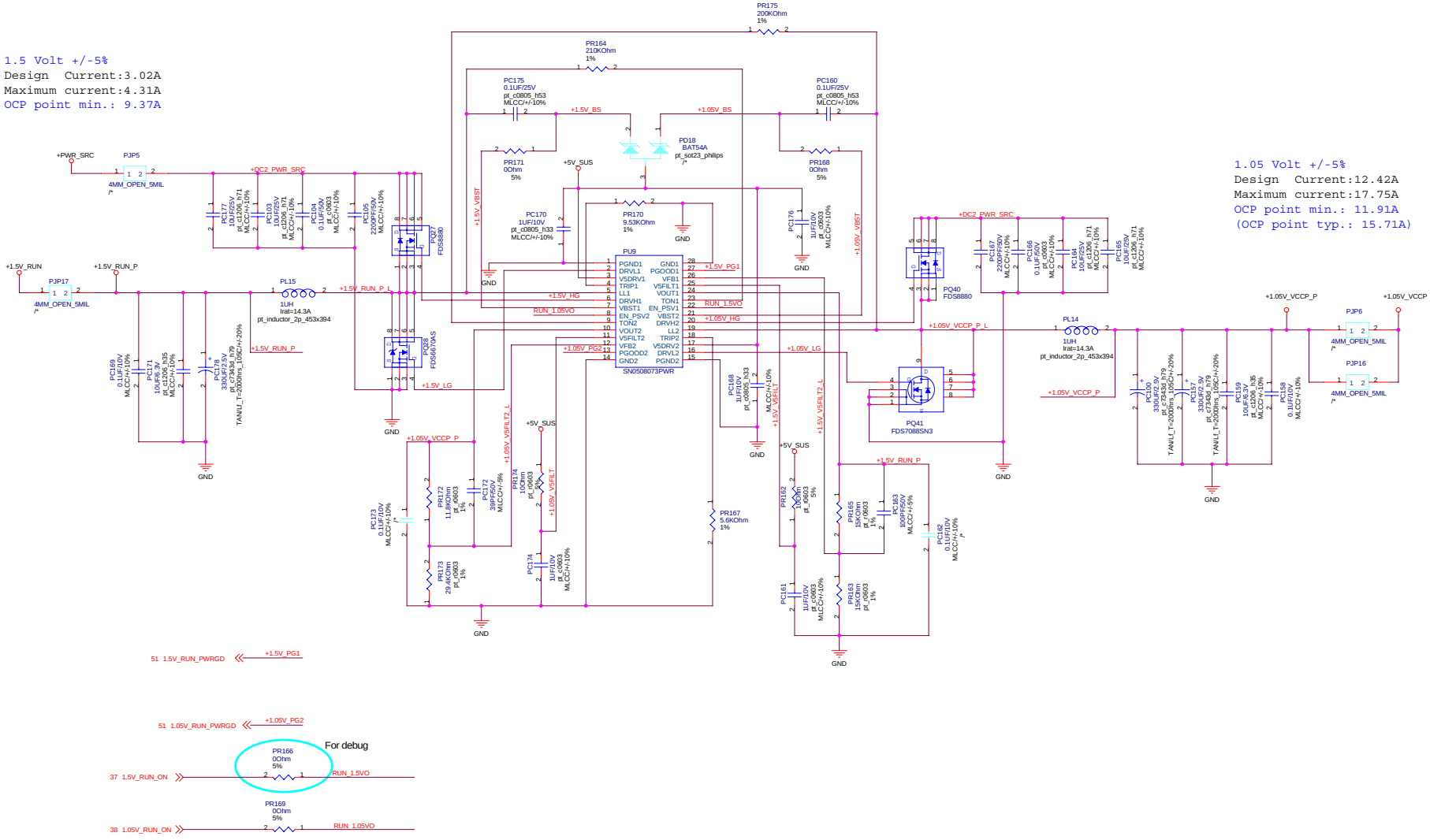
<Variant Name>

PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***XDP***	SCHEMATIC FILE NAME : **<OrgName>**	DESIGN ENGINEER : ***Terry_Lin***
		SHEET **52** OF **69**		RELEASE DATE :	

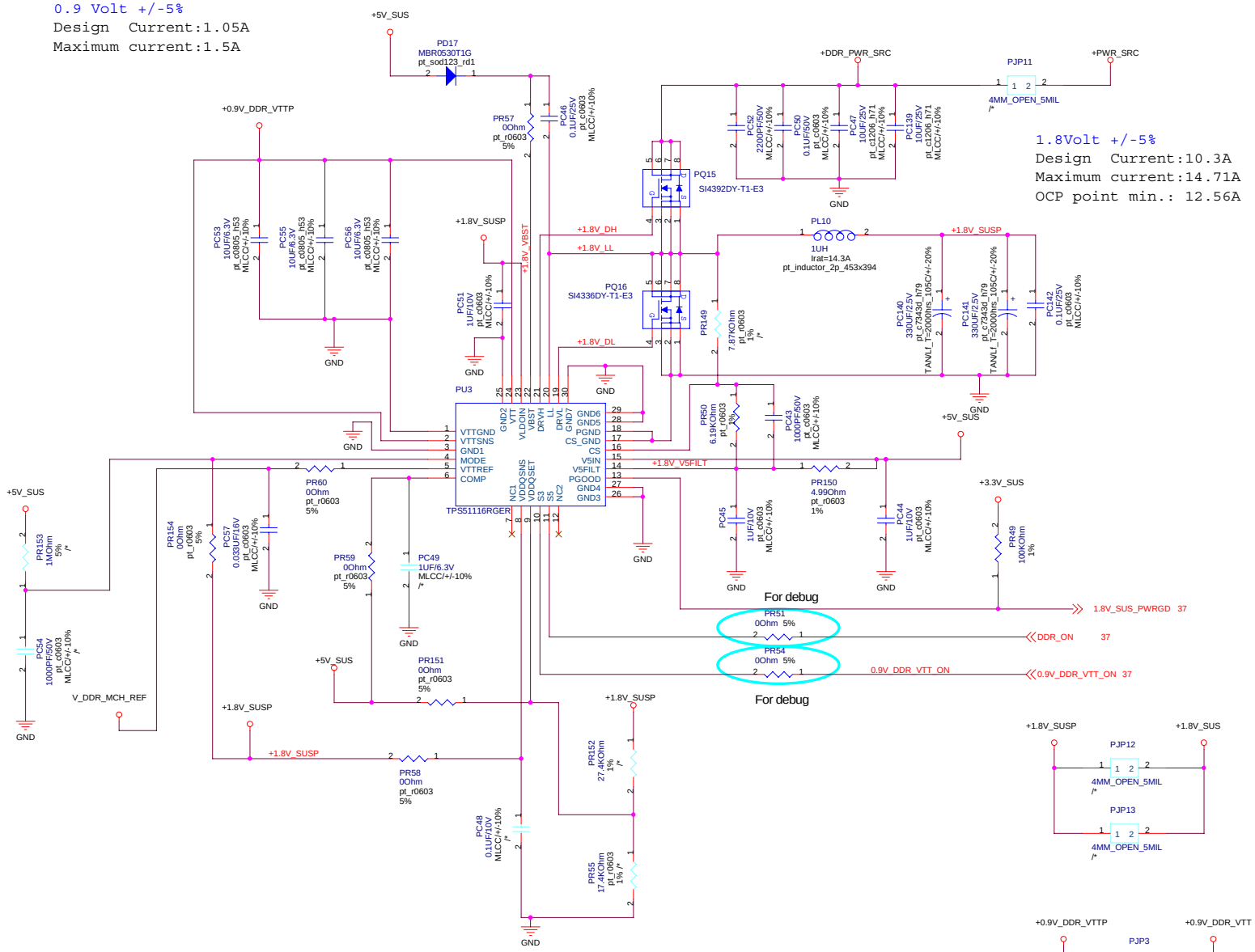


PROJECT: **Lanai**	REVISION: 1.1	DATE: Monday, March 19, 2007	DESCRIPTION: ***POWER_VCORE***	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER : ***JEFF***
		SHEET 53 OF 69		RELEASE DATE :	


5 Volt +/-5%
Design Current:6.12A
Maximum current:8.74A
OCP point min. :8.82A
3.3 Volt +/-5%
Design Current:6.95A
Maximum current:9.93A
OCP point min. :13.14A
PLACE THESE CAPS CLOSE TO FETS
TPS51120RHBR
For debug
PROJECT: Lanai
REVISION 1.1
DATE: Monday, March 19, 2007
SHEET 54 OF 69
DESCRIPTION: POWER_SYSTEM 5V_ALW&3.3V_ALW
SCHEMATIC FILE NAME : <OrgName>
RELEASE DATE :
DESIGN ENGINEER : JEFF

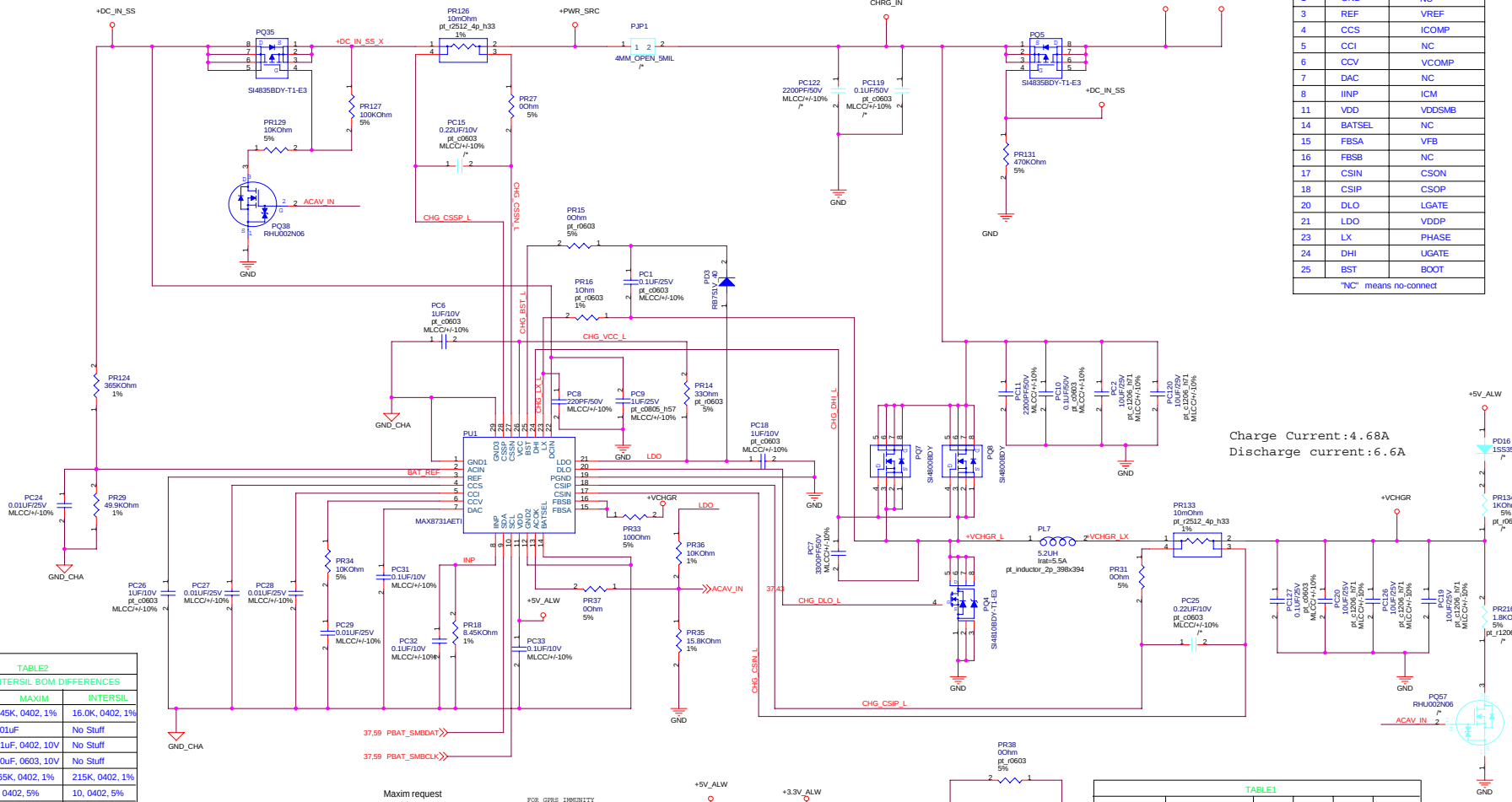


PROJECT: **Lanai**	REVISION: 1.1	DATE: Monday, March 19, 2007	DESCRIPTION:	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
		SHEET 55 OF 69	POWER I/O 1.5VS & 1.05VS	RELEASE DATE :		JEFF



PROJECT: **Lanai**	REVISION **1.1**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***POWER_I/O_DDR & VTT***	SCHEMATIC FILE NAME : RELEASE DATE :	**<OrgName>**
		SHEET **56** OF **69**			DESIGN ENGINEER : ***JEFF***

TOTAL POWER=90W
-->4.62A



Charge Current:4.68A
Discharge current:6.6A

TABLE3
PIN NAME DIFFERENCES

PIN	MAXIM	INTERSIL
1	GND	NC
3	REF	VREF
4	CCS	ICOMP
5	CCI	NC
6	CCV	VCOMP
7	DAC	NC
8	IINP	ICM
11	VDD	VDDSMB
14	BATSEL	NC
15	FBSA	VFB
16	FBSB	NC
17	CSIN	CSON
18	CSIP	CSOP
20	DLO	LGATE
21	LDO	VDDP
23	LX	PHASE
24	DHI	UGATE
25	BST	BOOT

"NC" means no-connect

TABLE2
MAXIM & INTERSIL BOM DIFFERENCES

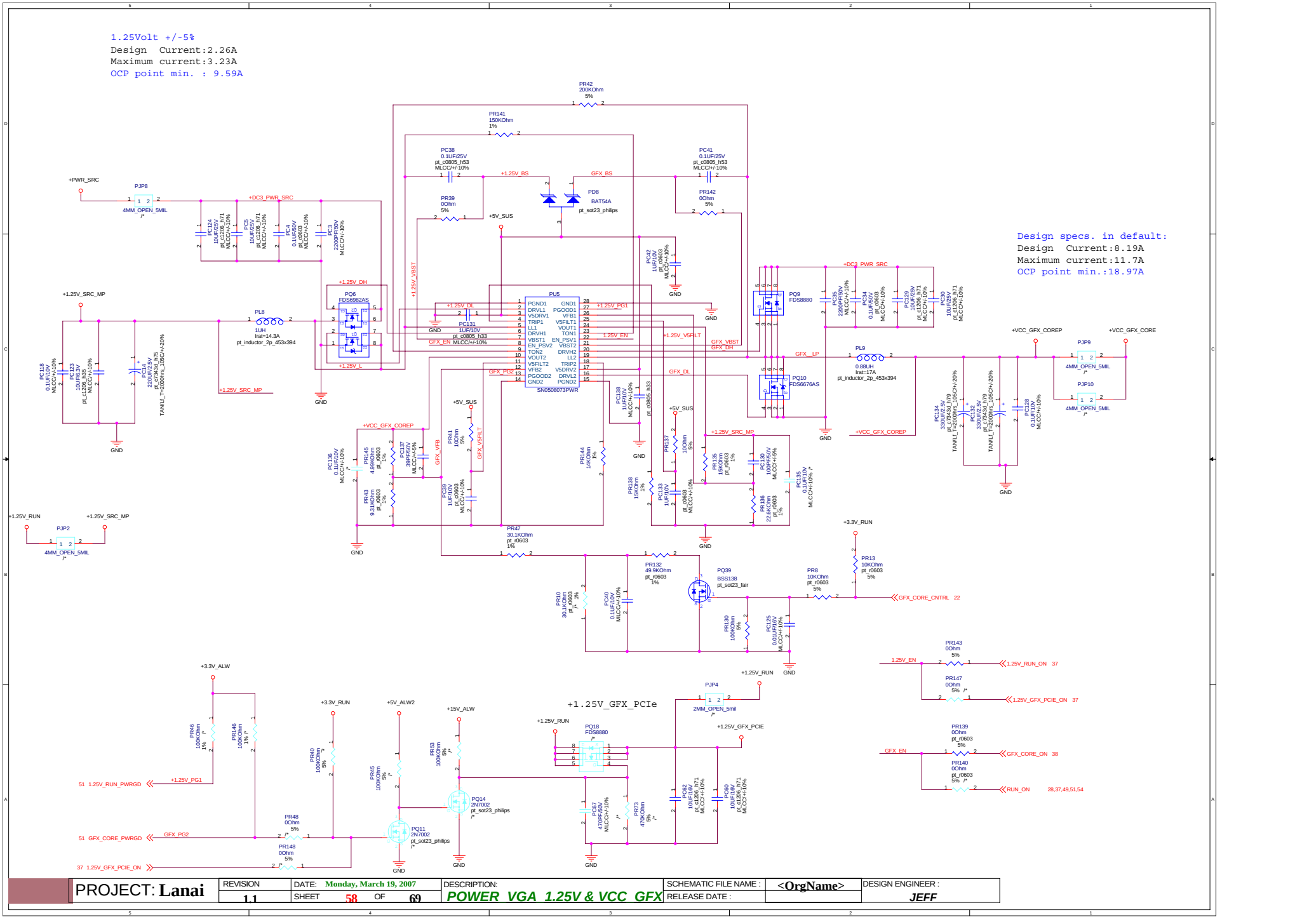
REF DES	MAXIM	INTERSIL
PR18	8.45K, 0402, 1%	16.0K, 0402, 1%
PC22	0.01uF	No Stuff
PC32	0.1uF, 0402, 10V	No Stuff
PC26	1.0uF, 0603, 10V	No Stuff
PR124	365K, 0402, 1%	215K, 0402, 1%
PR31	0, 0402, 5%	10, 0402, 5%
PR27	0, 0402, 5%	10, 0402, 5%
PC25	No Stuff	0.22uF
PC15	No Stuff	0.22uF
PC28	0.01uF	No Stuff
PC31	0.1uF, 0402, 10V	No Stuff
PC8	220pF, 0402, 50V	No Stuff
PD3	RB751V-40	No Stuff
PC7	3.3nF	No Stuff
PR16	1, 0603, 1%	0, 0603, 5%
PR33	100, 0402, 5%	0, 0402, 5%
PR34	4.7K, 0402, 5%	4.7K, 0402, 5%
PC29	0.01uF	0.01uF
PC27	0.01uF	0.01uF
PD16	1SS355	No stuff
PR134	1K, 0603, 5%	No stuff

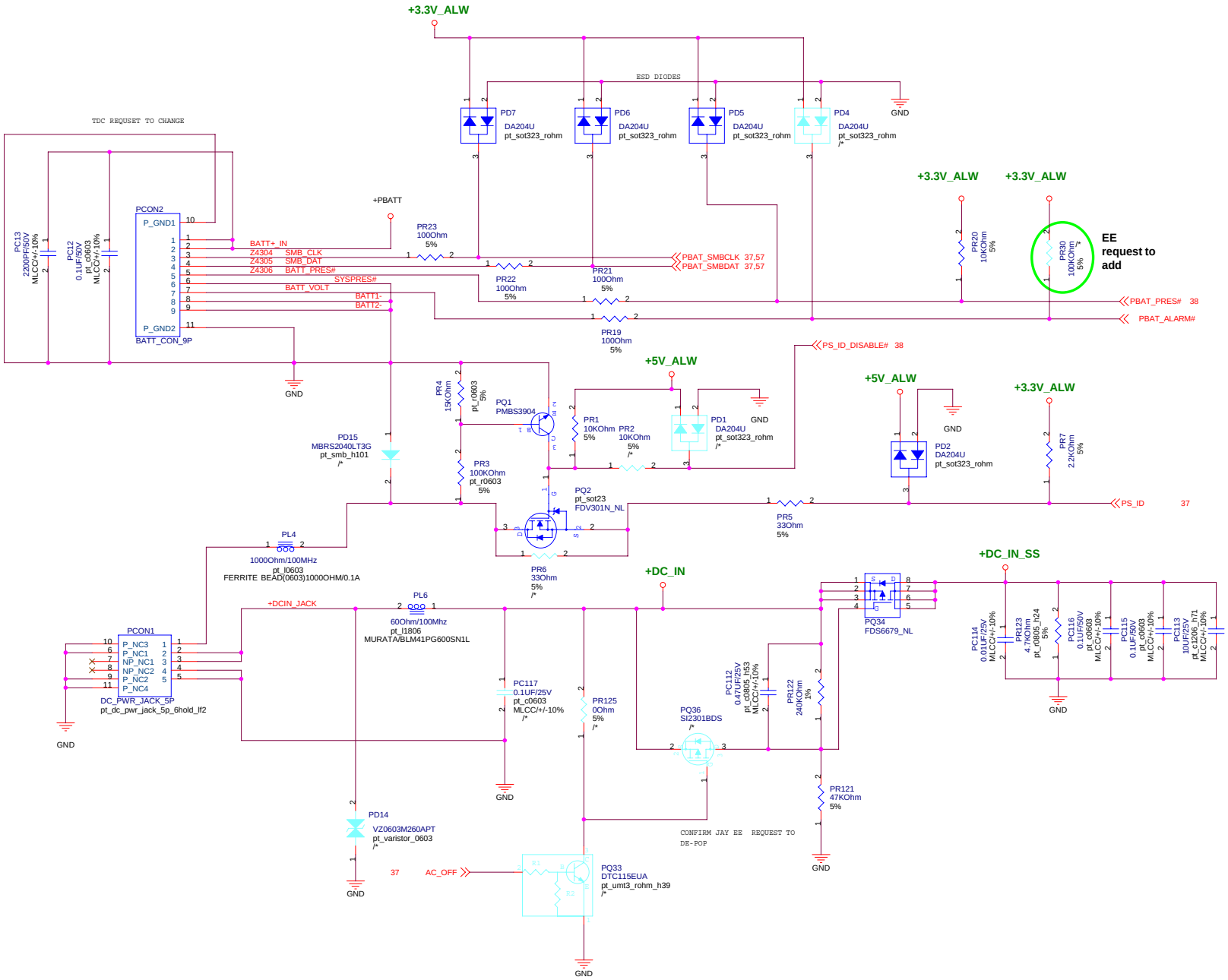
TABLE1

ADAPTOR (W)	TRIP CURRENT (A)	PR32	PR17	PR12	PR24
65	3.17	57.6K	13.0K	105	N/A
90	4.43	51.1K	17.8K	348	33.2K
130	6.43	32.4K	20.5K	100	27.4K
150	7.43	30.9K	24.9K	432	88.7K
200	9.75	19.1K	28K	301	36.5K
230	11.28	32.4K	6.49K	115	N/A

Note 1: PR24 is populated if ADAPT_TRIP_SET is used to program for the next lower adaptor
ADAPT_TRIP_SET is floating for the higher adaptor, grounded for the lower adaptor
Note 2: 24.9K at PR24 allows the 65W adaptor setting to switch down to 45W. (now is 33.2K for 90W)
Note 3: PR126 must be 5m ohm instead of 10m ohm for the 230W adaptor

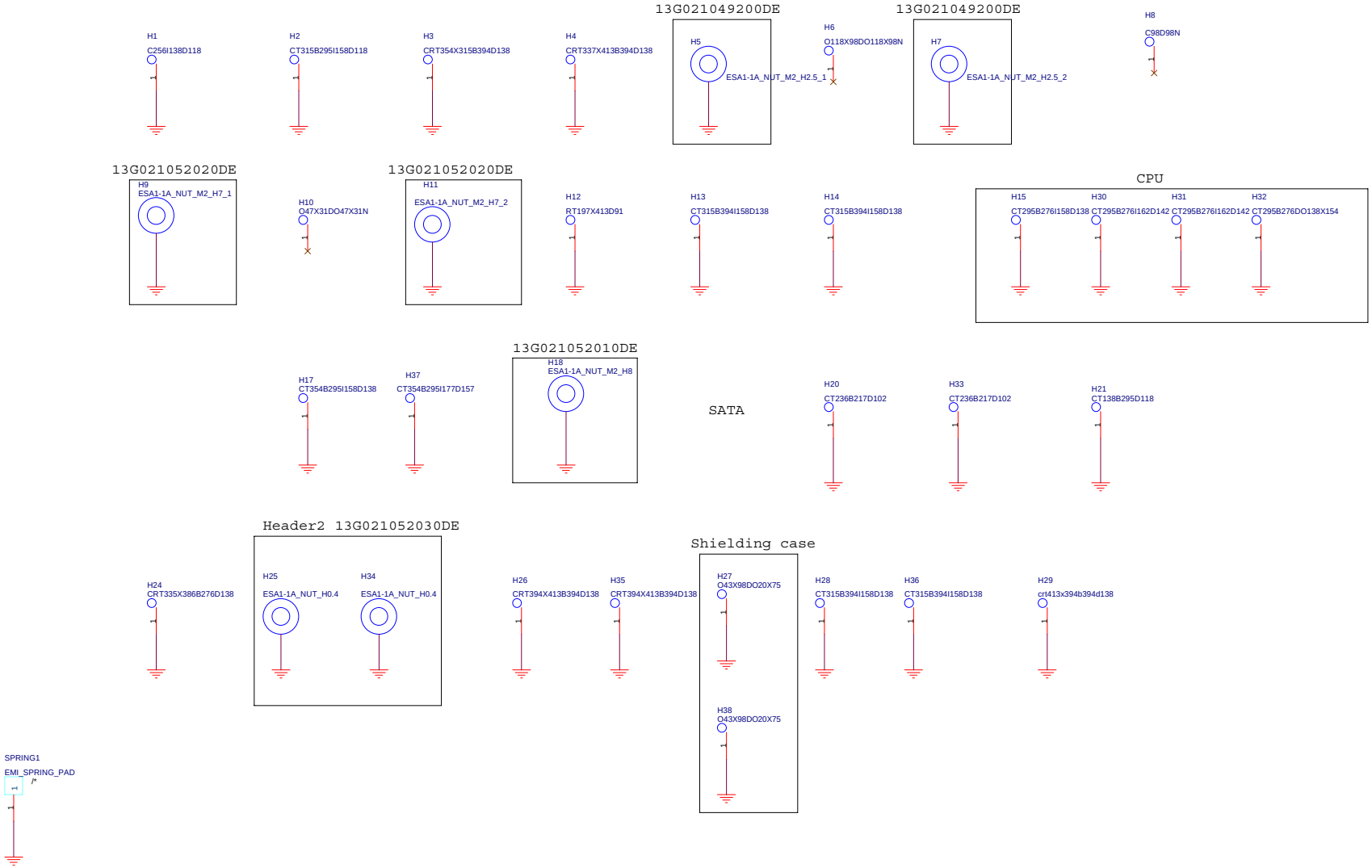
PROJECT: **Lanai**	REVISION 1.1	DATE: Monday, March 19, 2007	DESCRIPTION: **POWER_CHARGER**	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER : JEFF
		SHEET 57 OF 69		RELEASE DATE :	


1.25Volt +/-5%
Design Current:2.26A
Maximum current:3.23A
OCP point min. : 9.59A
Design specs. in default:
Design Current:8.19A
Maximum current:11.7A
OCP point min.:18.97A
+1.25V_GFX_PCIe
PROJECT: Lanai
REVISION 1.1
DATE: Monday, March 19, 2007
SHEET 58 OF 69
DESCRIPTION: POWER VGA 1.25V & VCC GFX
SCHEMATIC FILE NAME : <OrgName>
RELEASE DATE :
DESIGN ENGINEER : JEFF



PROJECT: **Lanai**	REVISION **1.1**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***POWER_CONNECTOR***	SCHEMATIC FILE NAME :	**<OrgName>**	DESIGN ENGINEER : ***JEFF***
		SHEET **59** OF **69**		RELEASE DATE :		

PM screw pad



PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***SCREW PAD***	SCHEMATIC FILE NAME :	DESIGN ENGINEER : **Sean Kuo**
		SHEET **60** OF **69**		RELEASE DATE :	

ASUS CONFIDENTIAL

MODEL NAME : ***Elsa***

PCB NO : ***???***

ASUS P/N : ***???***

Lanai USB Board

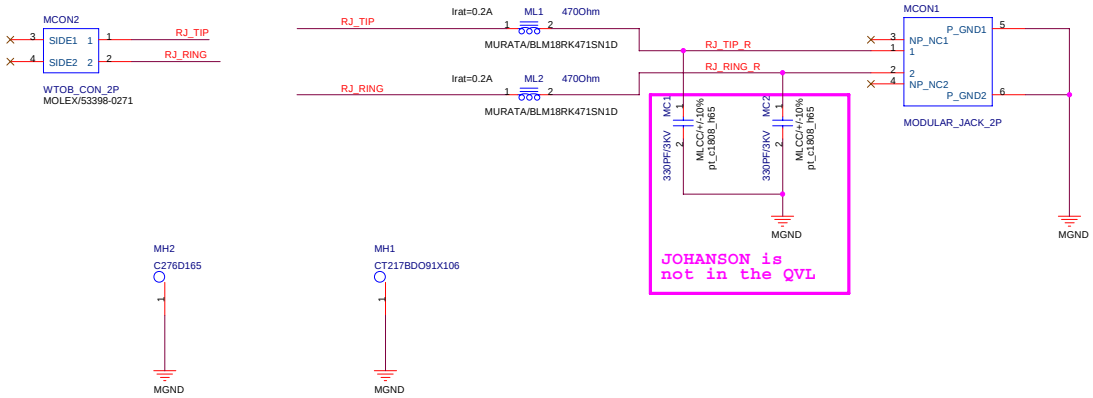
REV :1.1(DELL: X01)

MB PCB

Part Number	Description
DA800004H0L	PCB 00B LA-3071P REV0 M/B

BOM NO. ???
PCB P/N: ???

PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007** SHEET **65** OF **69**	DESCRIPTION: ***Cover Page***	SCHEMATIC FILE NAME : RELEASE DATE :	DESIGN ENGINEER : ***Terry Lin***



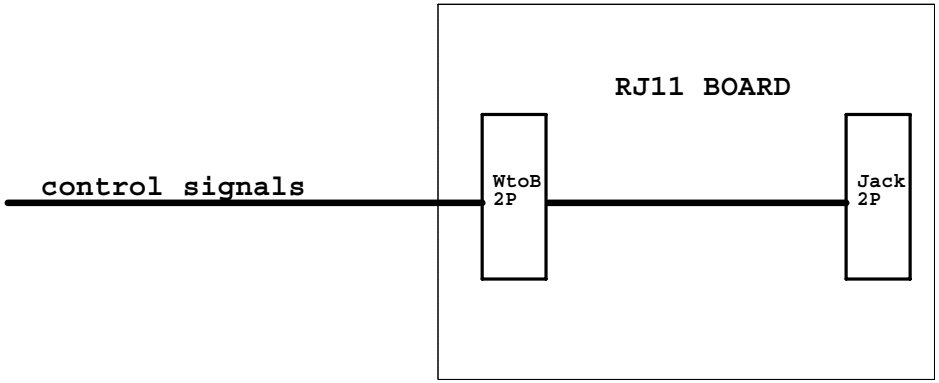
PROJECT: **Lanai**	REVISION **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION: ***RJ-11 CONN***	SCHEMATIC FILE NAME :	**<OrgName>**	DESIGN ENGINEER : ***Stanly_Hsu***
		SHEET **66** OF **69**		RELEASE DATE :		

ASUS CONFIDENTIAL

MODEL NAME : *Elsa*

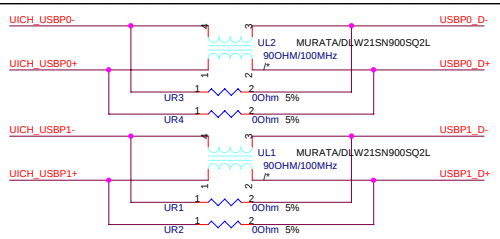
Lanai Modem Board

REV :1.1(DELL: X01)

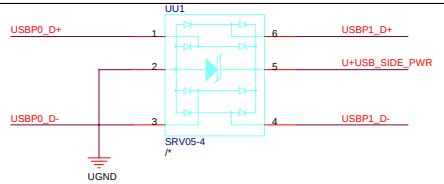


PROJECT: **Lanai**	REVISION: **1.2**	DATE: **Monday, March 19, 2007**	DESCRIPTION:	SCHEMATIC FILE NAME :	DESIGN ENGINEER :
		SHEET **68** OF **69**	***BLOCK DIAGRAM***	RELEASE DATE :	***Stanly Hsu***

External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently .

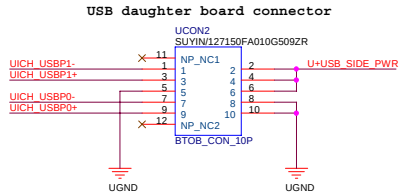


Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

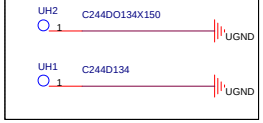


Place ESD diodes as close as USB connector. Semtech SRV05-4 can also be used but the Philips IP42220CZ6 have a lower input C (1pf vs 3pf).

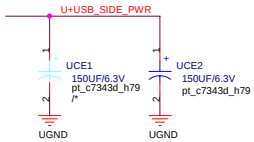
USB daughter board connector



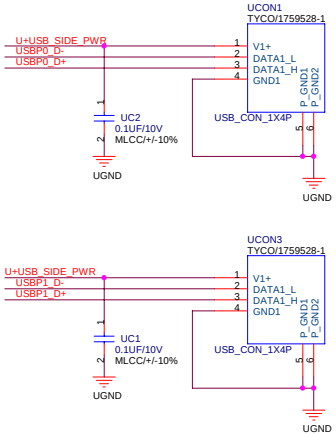
Screw hole



Place one 150uF cap by each USB connector



Each channel is 1A



Consult you ESD Engineer if you think you may need to add ESD Supression Components to your USB lines.
Add PADS ONLY until proven diodes are really needed.

PROJECT: **Lanai**	REVISION 1.2	DATE: Monday, March 19, 2007	DESCRIPTION: **USB PORT (SINGLE *2)**	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER : Terry_Lin
		SHEET 69 OF 69		RELEASE DATE :	