Wistron Confidential

PV

2007/03/30 REV :PV-04

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

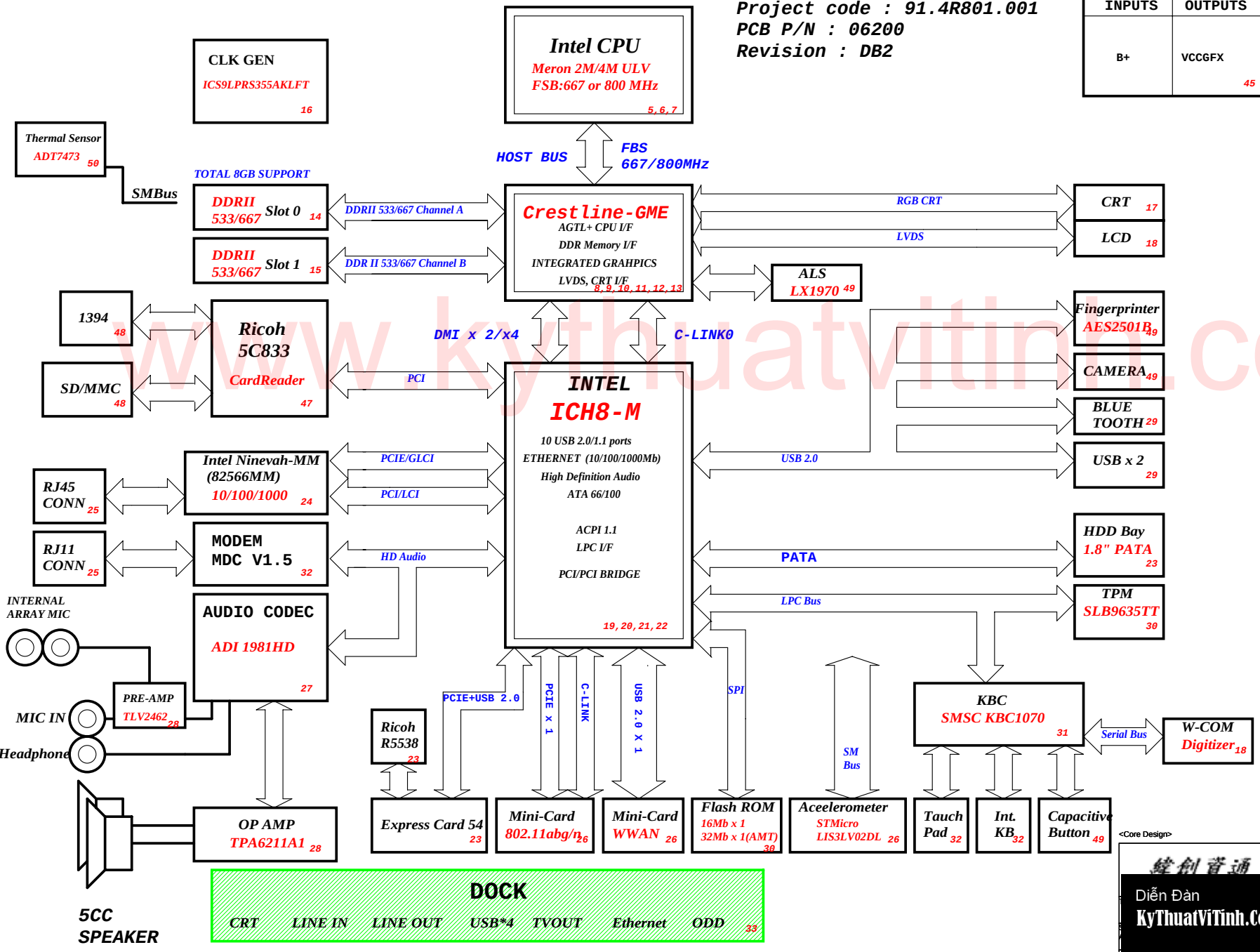
Title: NORN

Size	Document Number	Rev
A3	NORN	PV

Date: Friday, March 30, 2007 Sheet 1 of 51

NORN Block Diagram

Project code : 91.4R801.001
PCB P/N : 06200
Revision : DB2



VGA	
MAX8776	
INPUTS	OUTPUTS
B+	VCCGFX 45

SYSTEM DC/DC	
TPS51120	
INPUTS	OUTPUTS
B+	+5VALW 5A +3VALW 4A 40

SYSTEM DC/DC	
TPS51124	
INPUTS	OUTPUTS
B+	+1.5VS 4A +VCCP 6A 41

CHARGER	
BQ24703	
INPUTS	OUTPUTS
BATT_A BATT_B	BATT 18V 3.0A 5V 100mA 38

CPU DC/DC	
ISL6260	
INPUTS	OUTPUTS
B+	+VCC_CORE 0.844~1.3V 44A 43

PCB LAYER

L1: Signal 1
L2: Signal 2
L3: GND
L4: Signal 3
L5: VCC
L6: GND
L7: Signal 4
L8: GND
L9: Signal 5
L10: Signal 6

<Core Design>
Wistron Corporation
Rev PV
Date: 2009.12.04 19:46:56 +07'00'

鋒創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***Change Notes List***
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Voltage Rails

o MEANS ON x MEANS OFF

State \ power plane	+BB LDO3 LDO5	+5VALW +5VALW	+1.8V +0.9V	+5VS +3VS +1.8VS +1.5VS +1.25VS +VGA_CORE +CPU_CORE +VCCP	+3VM +1.05VM +1.25VM	CLOCK
S0	O	O	O	O	O	O
S3/M1	O	O	O	X	O	O
S3	O	O	O	X	O	O
S5 S4/AC	O	O	X	X	O	O
S5 S4/Battery only	O	X	X	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X	X	X

PCI Devices

EETERNAL	IDSEL#	REQ/GNT#	PIRQ
Cardreader & 1394	AD22	2	G,E

DMA Channel	Device
DMA0	Modem/LAN
DMA1	ECP
DMA2	~~Floppy Disk~~
DMA3	Audio
DMA4	(Cascade)
DMA5	Unused
DMA6	Unused
DMA7	Unused

USB PORT#	Destination
0	FREE
1	Fingerprint
2	EXPRESS SLOT
3	Camera
4	Walk-up1 (Right Side)
5	Walk-up2 (Left Side)
6	Bluetooth
7	Dock 1
8	WWAN
9	Dock 2

Symbols	Description
DY/DUMMY	No install
1KR2J	Resistor 1K ohm ,Size 0402 ,5%
1KR3F	Resistor 1K ohm ,Size 0603 ,1%
GP	ROHS parts
NC	Pin no connect to anything

IRQ	Device
0	System Timer
1	Keyboard
2	N/A
3	Serial port (COM2) ,LAN/Modem
4	Serial port (COM1)
5	Audio/VGA
6	~~Floppy~~
7	Parallel port
8	System CMOS/Real-time clock
9	Microsoft ACPI
10	N/A,Modem,LAN
11	Mass storage control/PCI simple communication control
12	synactic PS2 port GlidePAD
13	Numeric Data Process
14	Primary IDE interface ,HDD
15	Secondary IDE interface ,CD-ROM
16	Mobile Intel Crestline Express Chipset Family Microsoft UAA Bus Drive for High Definition Audio Intel 82801H (ICH8 Family) PCI Express Root Port -27D0 Broadcom NetXtreme Gigabit Ethernet
17	Intel 82801H (ICH8 Family) PCI Express Root Port -27D2 Broadcom 802.11b/g WLAN Intel 82801H (ICH8 Family) USB Universal Host Control
18	Intel 82801H (ICH8 Family) USB Universal Host Control Richo R5C853 Integrates FlashMedia Control Richo R5C853 Gemcore based SmartCard Control
19	Intel 82801H (ICH8 Family) PCI Express Root Port -27D6 Intel 82801H (ICH8 Family) USB Universal Host Control
20	Intel 82801H (ICH8 Family) USB Universal Host Control Intel 82801H (ICH8 Family) USB2 Enhanced Host Control
21	Intel 82801H (ICH8 Family) USB Universal Host Control
22	SDA Standard Compliant SD Host Control
23	HP Mobile Data Protection Sensor

<Variant Name>

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Title: **Notes List**

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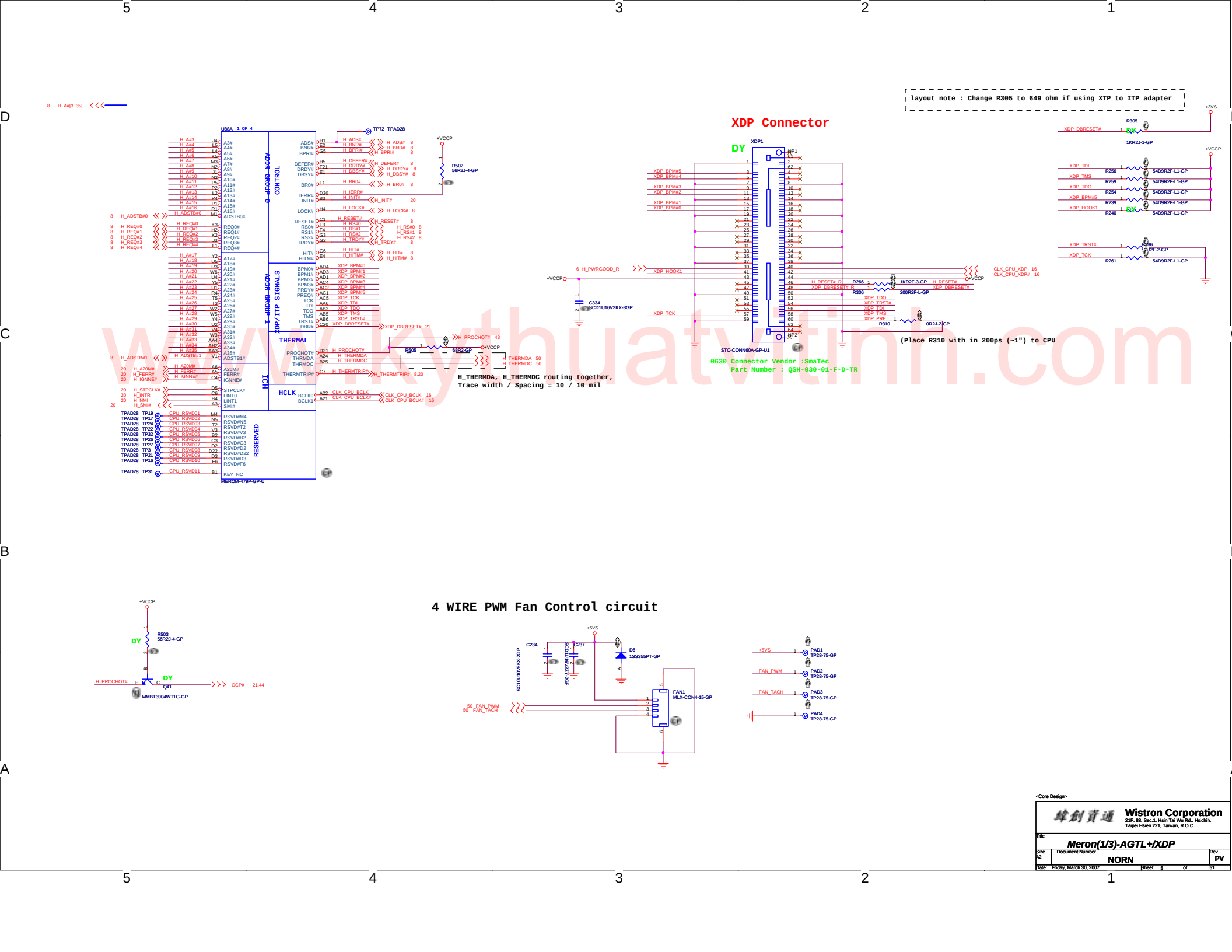
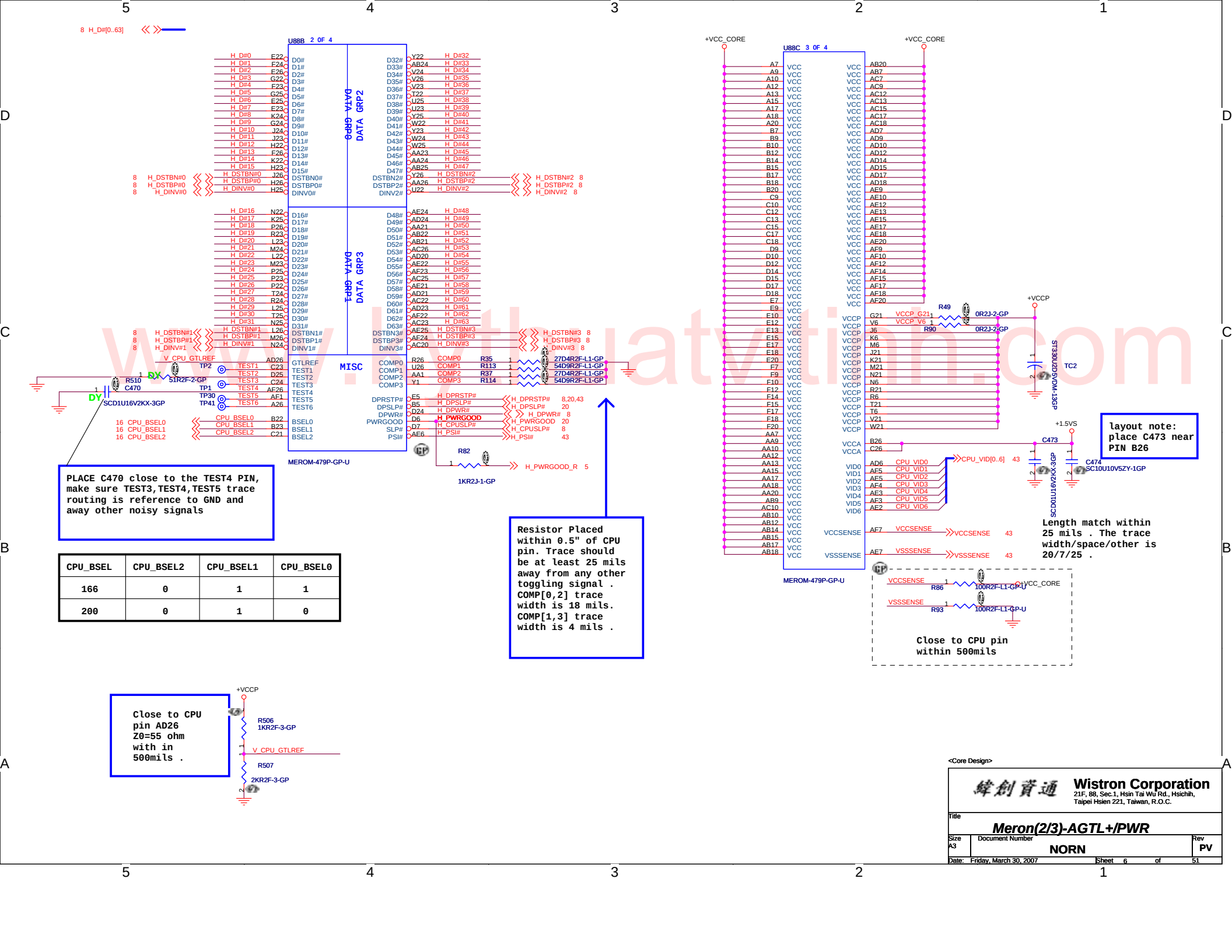

XDP Connector
layout note : Change R305 to 649 ohm if using XTP to ITP adapter
(Place R310 with in 200ps (~1") to CPU
H_THERMDA, H_THERMDC routing together,
Trace width / Spacing = 10 / 10 mil
4 WIRE PWM Fan Control circuit
0630 Connector Vendor :SmaTec
Part Number : QSH-030-01-F-D-TR
STC-CONN60A-GP-U1
MEROM-479P-GP-U
MMBT3904WT1G-GP
Wistron Corporation
Meron(1/3)-AGTL+/XDP
NORN



<Core Design>

Wistron Corporation
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Title: Meron(2/3)-AGTL+/PWR

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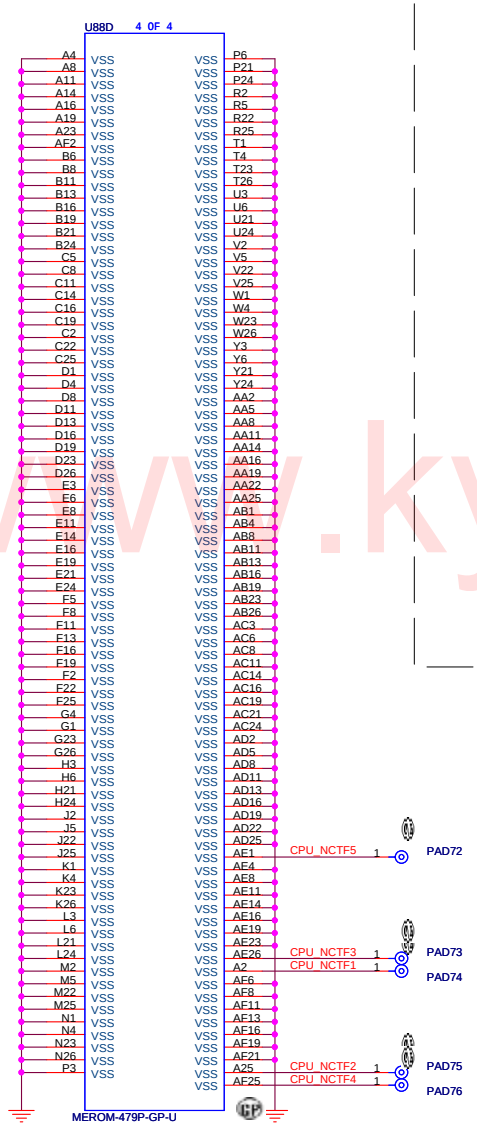

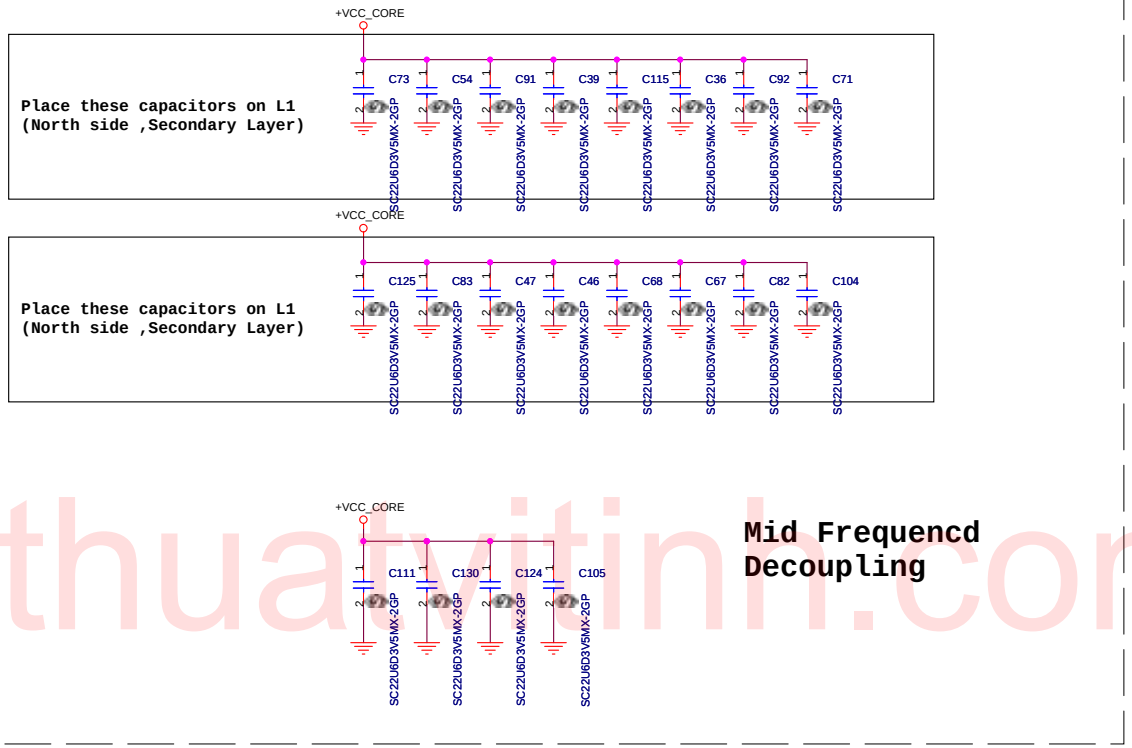

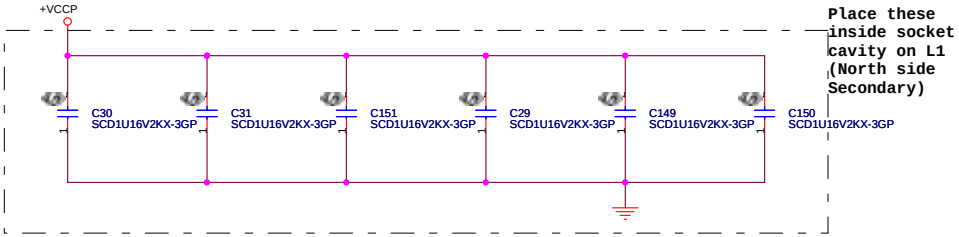

<Core Design>

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Title: Meron(3/3)-GND&Bypass

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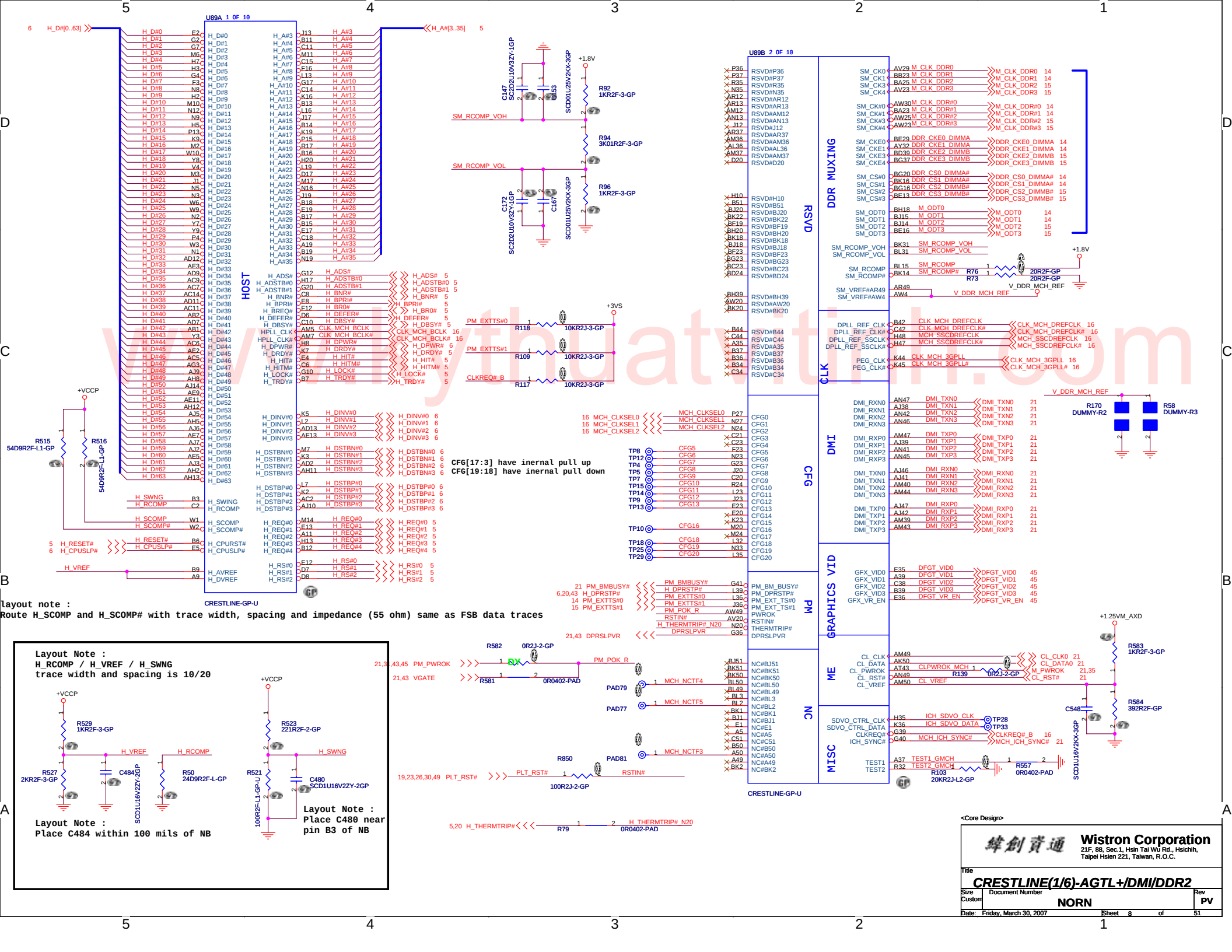
U89A 1 OF 10
HOST
U89B 2 OF 10
RSVD
DDR MUXING
CLK
DMI
CFG
GRAPHICS VID
PM
ME
NC
MISC
CRESTLINE-GP-U
CRESTLINE-GP-U
layout note :
Route H_SCOMP and H_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces
CFG[17:3] have inernal pull up
CFG[19:18] have inernal pull down
Layout Note :
H_RCOMP / H_VREF / H_SWNG
trace width and spacing is 10/20
Layout Note :
Place C484 within 100 mils of NB
Layout Note :
Place C480 near
pin B3 of NB
<Core Design>
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title
CRESTLINE(1/6)-AGTL+/DMI/DDR2
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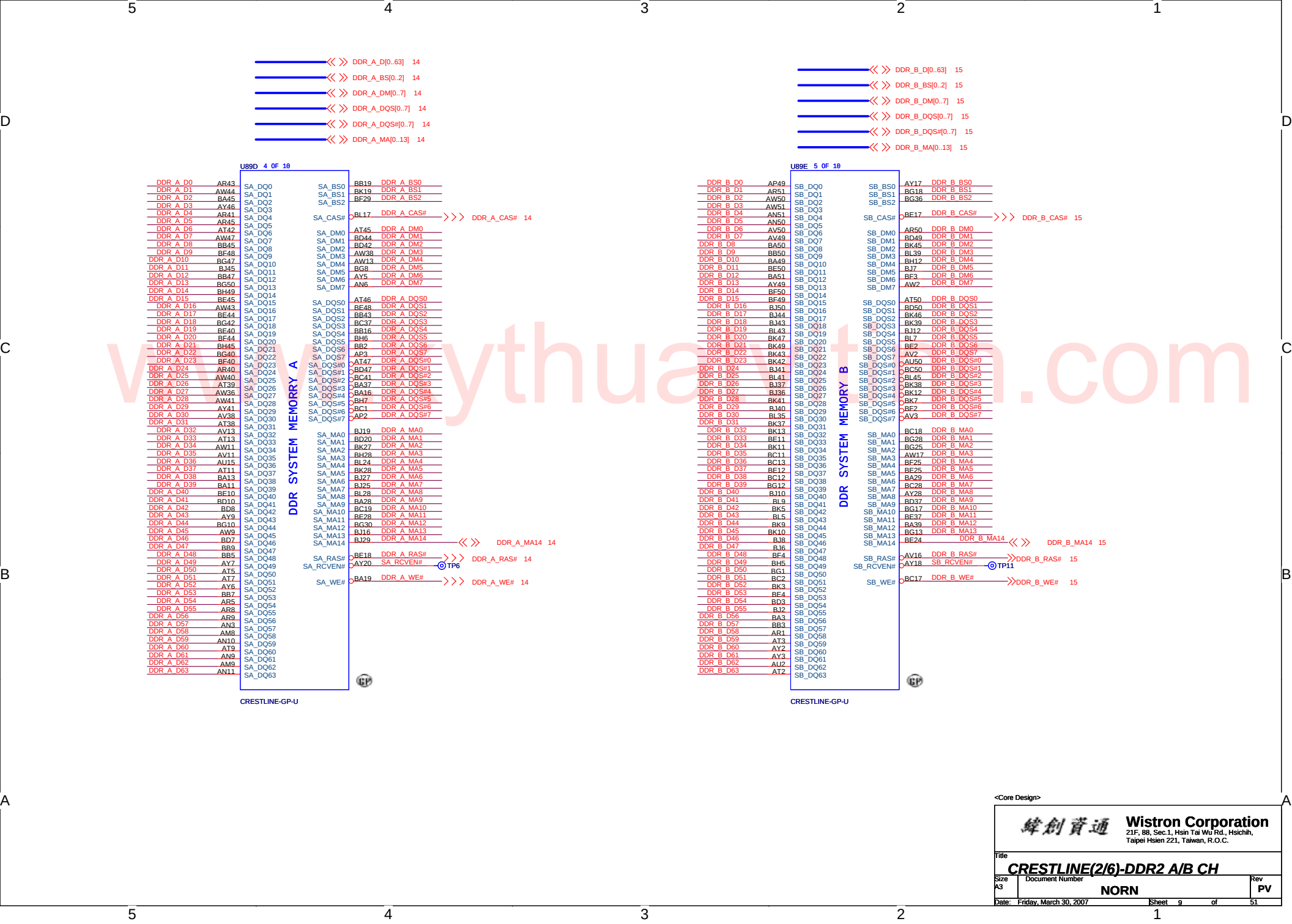

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Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	CRESTLINE(2/6)-DDR2 A/B CH
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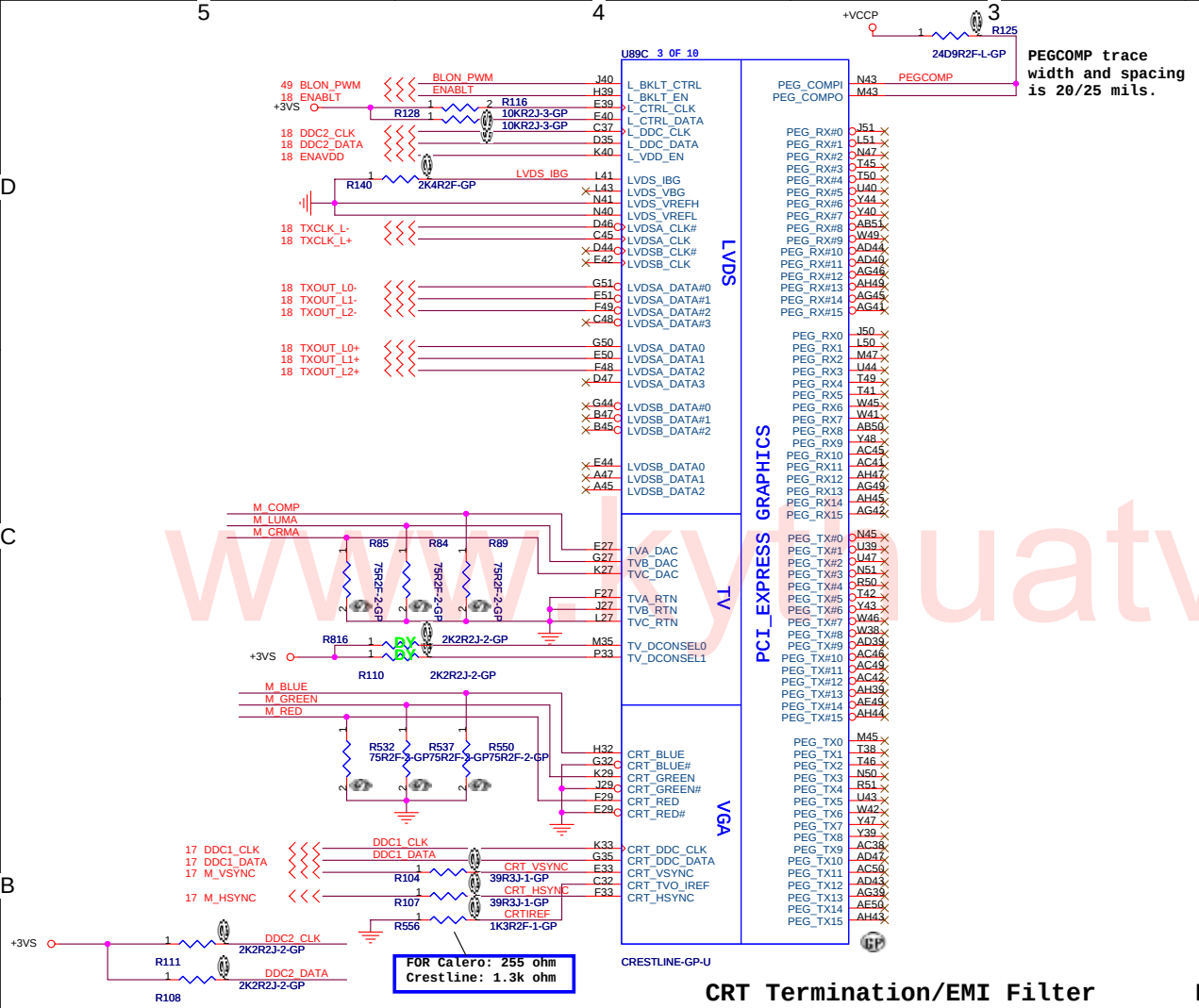
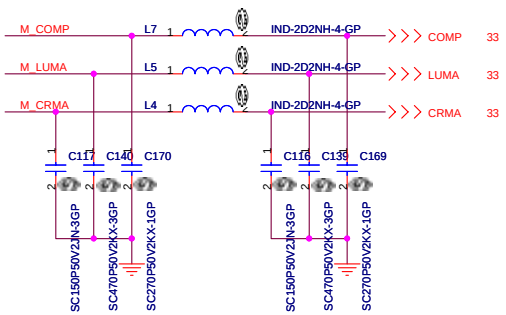


Strap Pin Table

CFG[2:0] FSB Freq select	010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	Reserved
CFG7 (CPU Strap)	0 = Reserved 1 = Mobile CPU *
CFG8 (Low power PCIE)	0 = Normal mode 1 = Low Power mode *
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane 1 = Normal Operation *
CFG[11:10]	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default)*
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disable 1 = Enable *
CFG[18:17]	Reversed
SDVO_CTRLDATA	0 = No SDVO Device Present * 1 = SDVO Device Present
CFG19(DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse lane
CFG20(PCIE/SDVO consurrent)	0 = Only PCIE or SDVO is operational * 1 = PCIE/SDVO are operating simu.

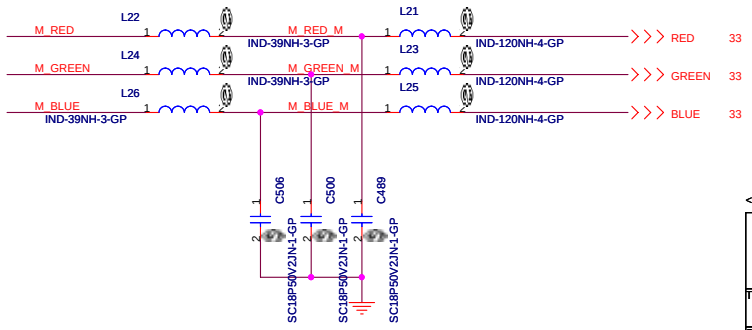
TV-Out Termination/EMI Filter

Place Close N/B



CRT Termination/EMI Filter

Place Close Connector



<Core Design>
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Title: CRESTLINE(3/6)-VGA/LVDS/TV

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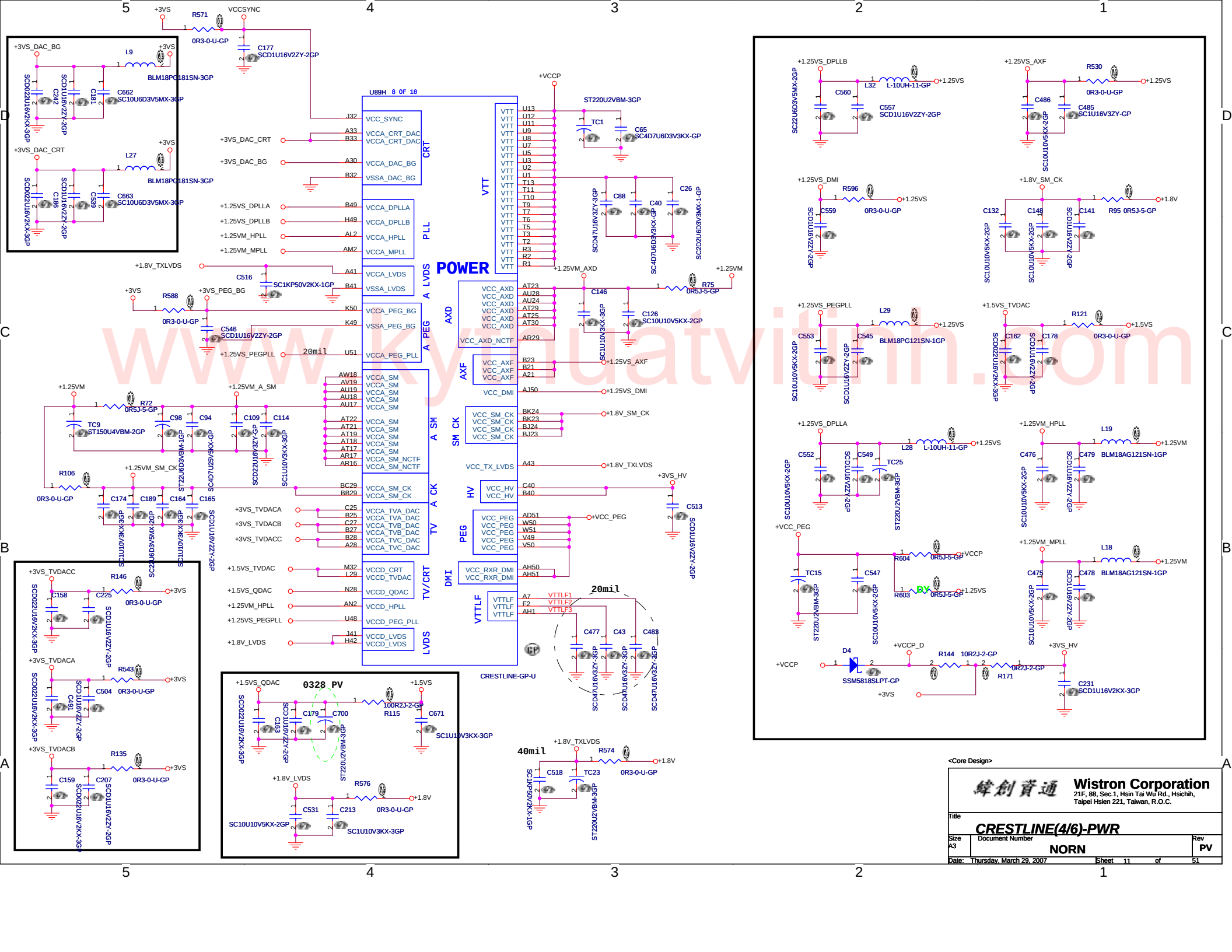

<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: CRESTLINE(4/6)-PWR

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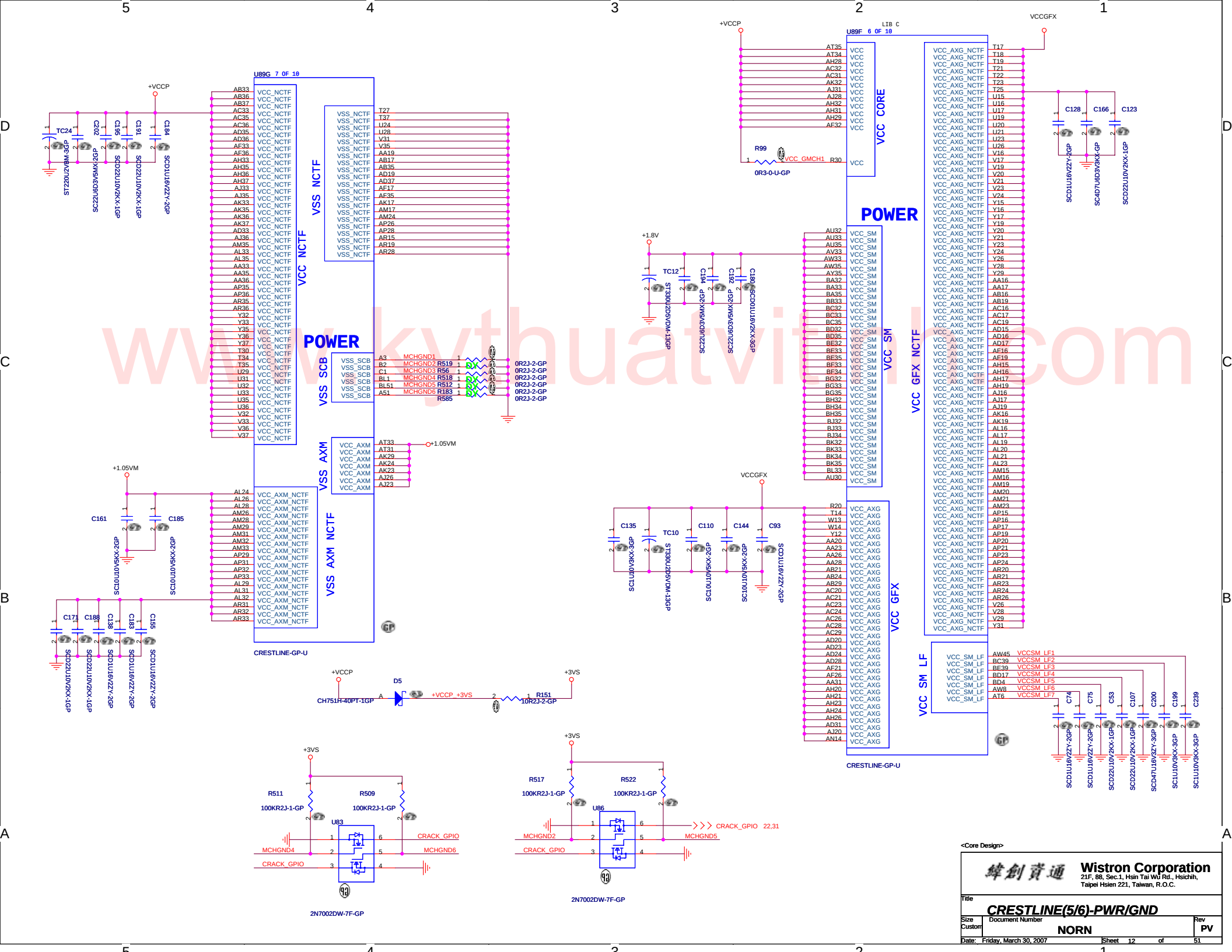
U89G 7 0F 10
VCC_NCTF
VSS_NCTF
VSS_SCB
VCC_AXM
VCC_AXM_NCTF
VSS_AXM
POWER
CRESTLINE-GP-U
U89F 6 0F 10
VCC_CORE
VCC_SM
VCC_GFX_NCTF
VCC_GFX
VCC_SM_LF
VCCGFX
+VCCP
+1.8V
+1.05VM
+3VS
R99
0R3-0-U-GP
D5
CH751H-40PT-1GP
R151
10R2J-2-GP
R511
R509
R517
R522
100KR2J-1-GP
U83
U86
2N7002DW-7F-GP
MCHGND1
MCHGND2
MCHGND3
MCHGND4
MCHGND5
MCHGND6
CRACK_GPIO
0R2J-2-GP
R519
R56
R518
R512
R183
R585
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CRESTLINE(5/6)-PWR/GND
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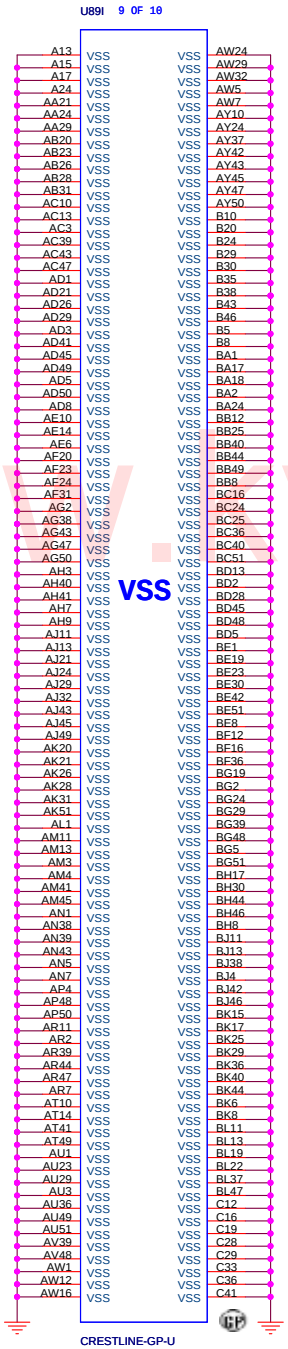

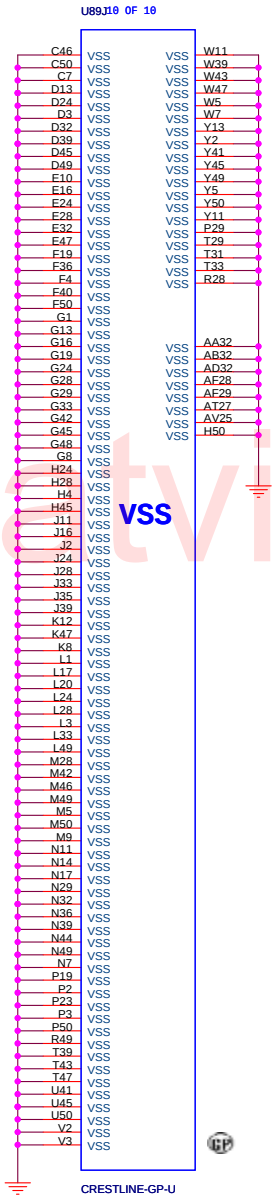

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Title: CRESTLINE(6/6)-PWR/GND

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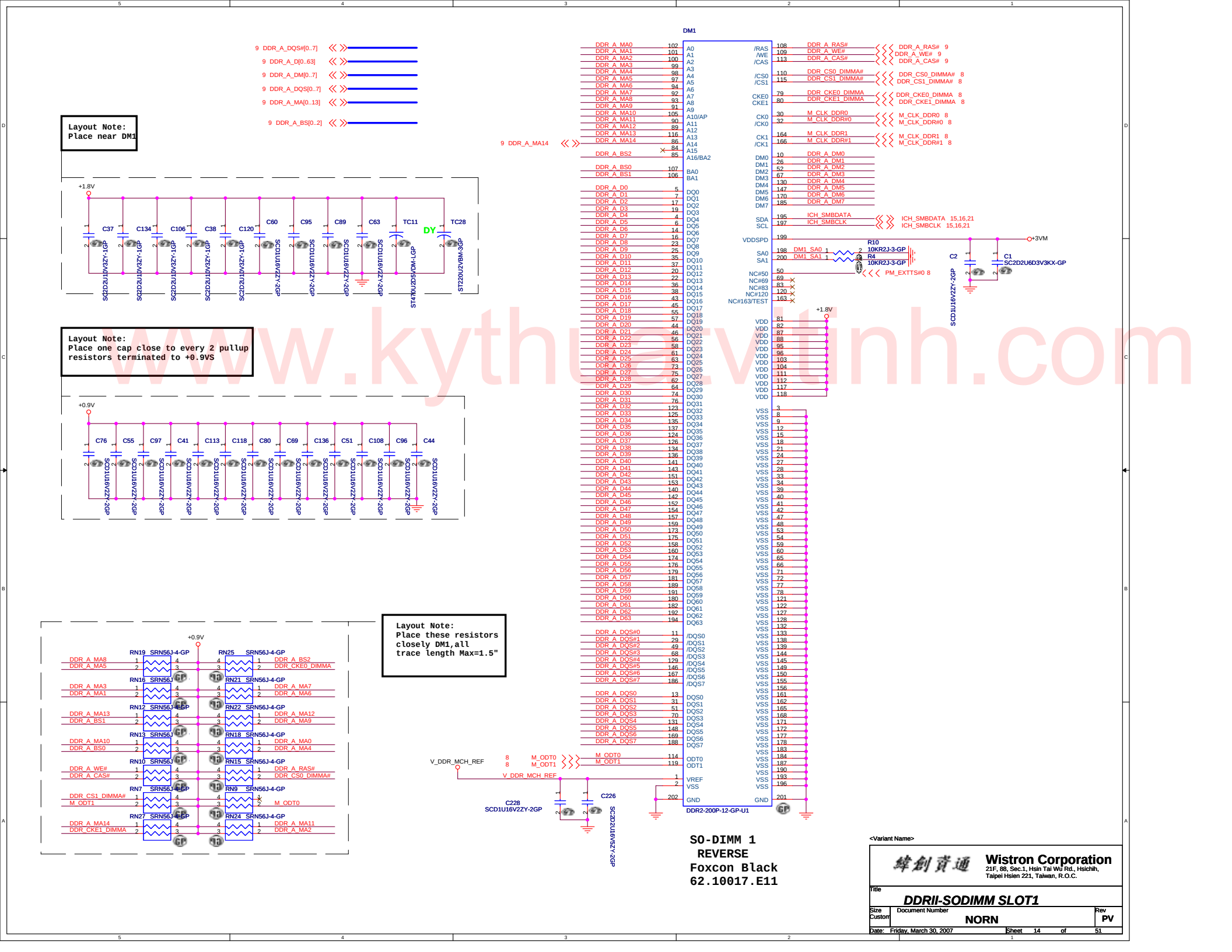

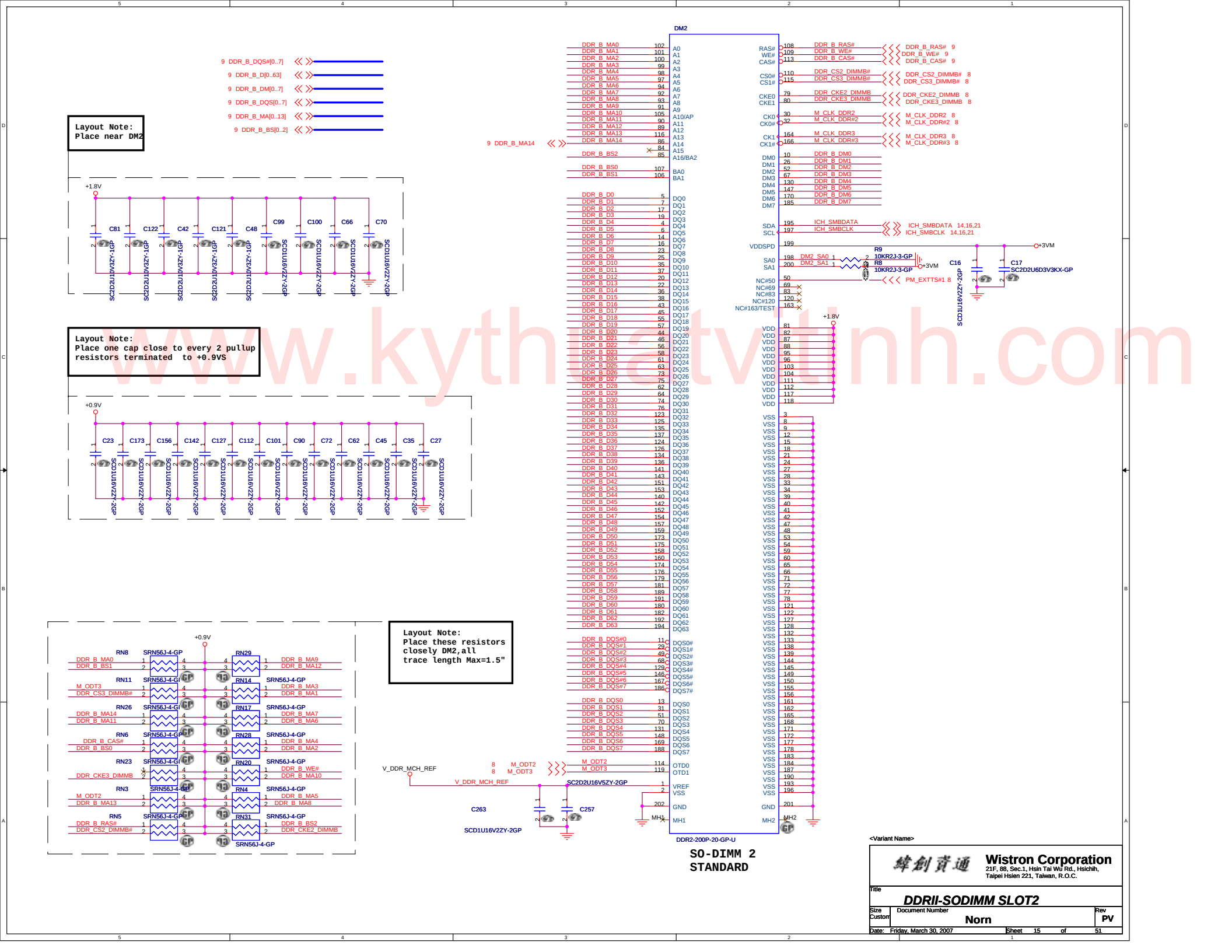

<Variant Name>

Wistron Corporation
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Title: DDRII-SODIMM SLOT2

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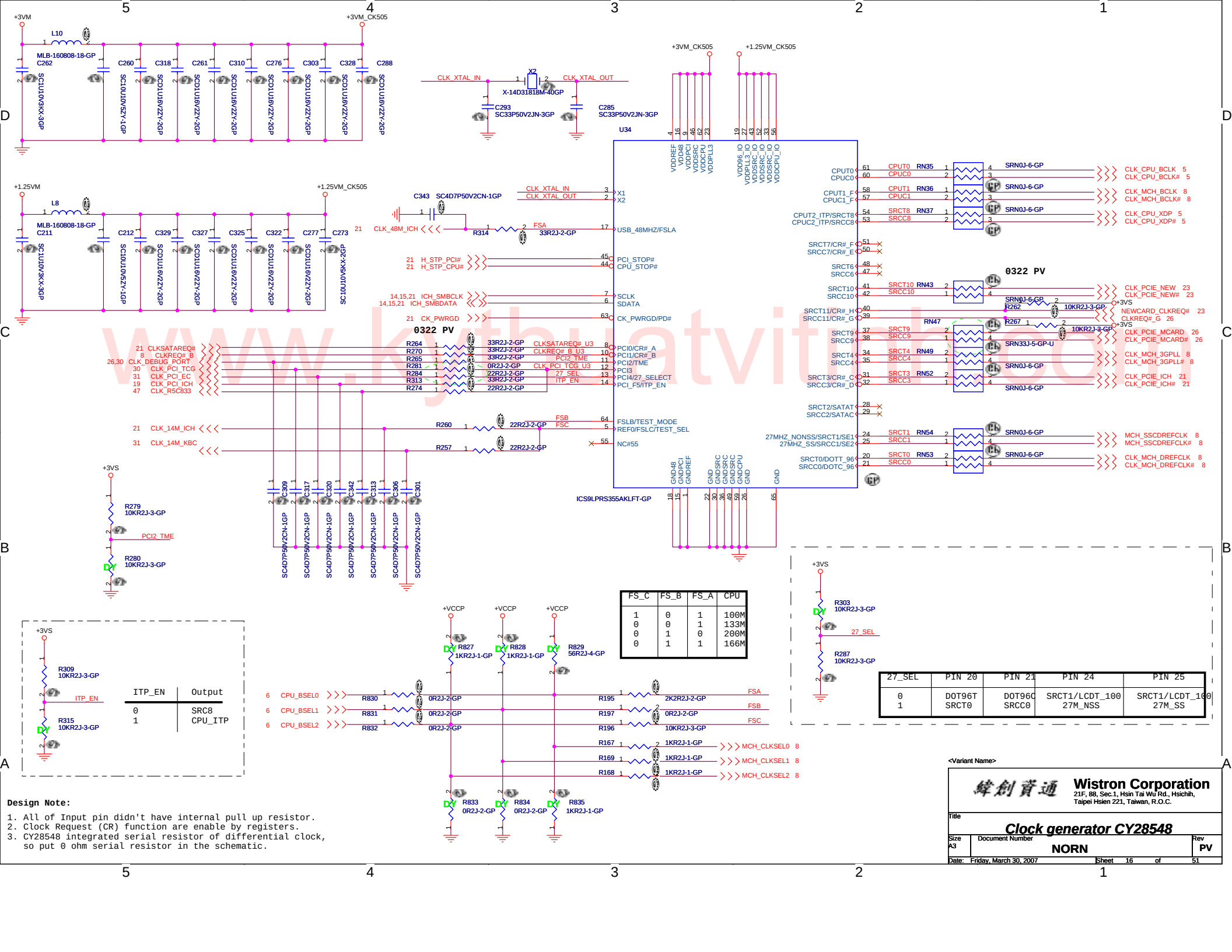
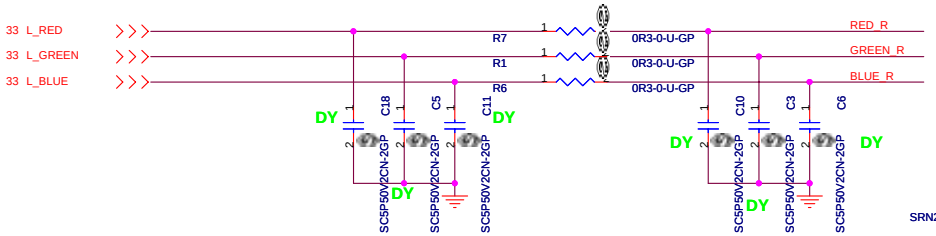
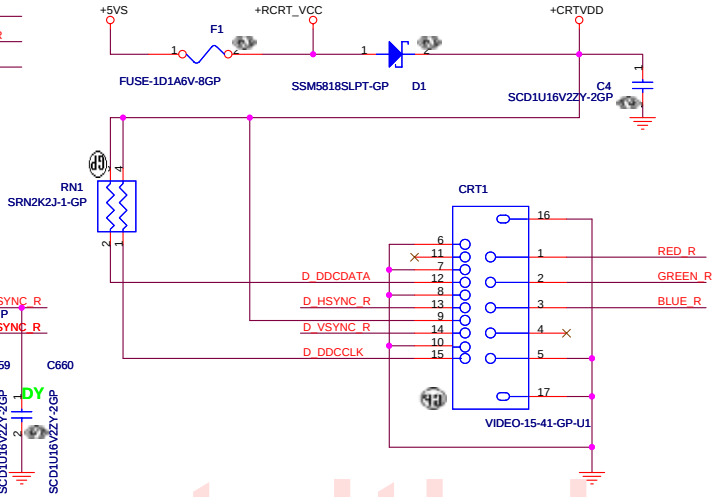
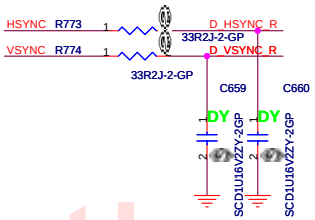


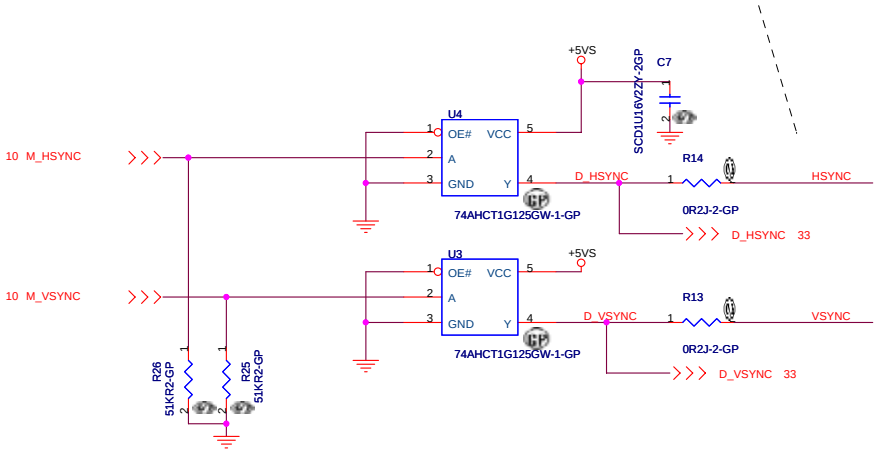


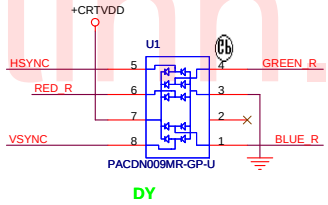


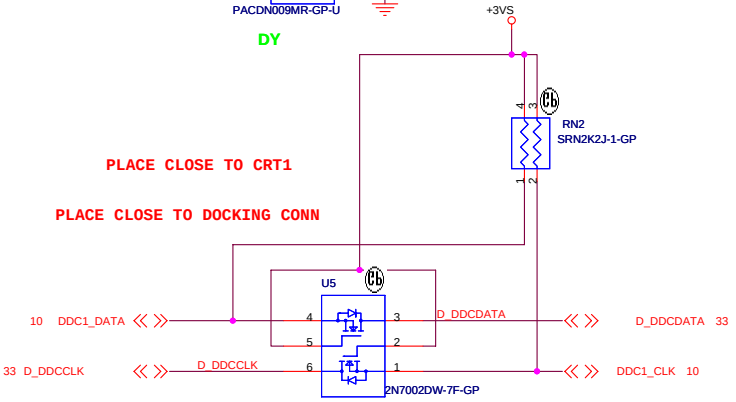


CRT

Layout Note : HSYNC & VSYNC SHOULD BE ROUTED TO DOCK CRT CONN. ,THEN TO SYSTEM CRT CONN.







<Core Design>

蜂創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: **CRT/TV CONNECTOR**

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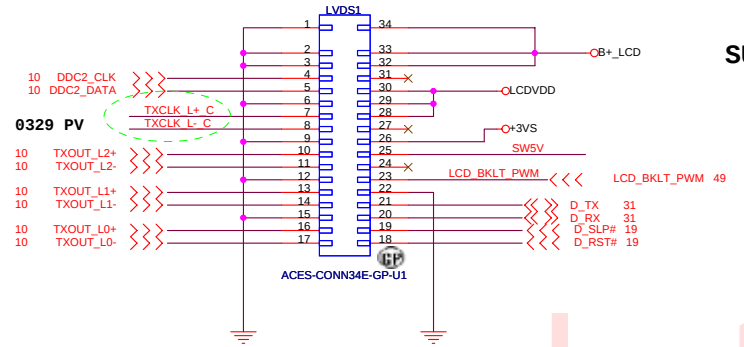
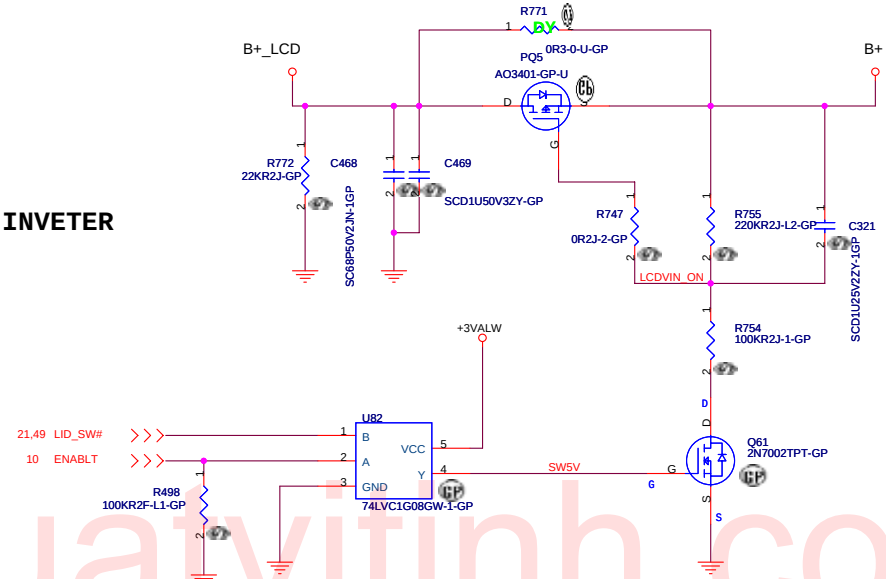
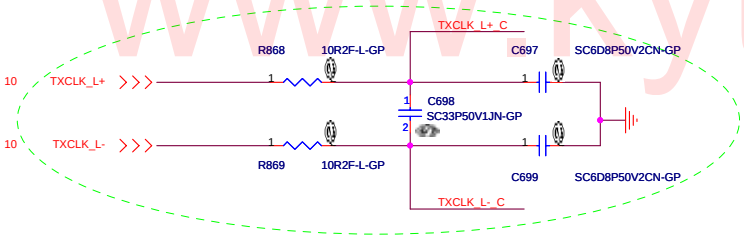
LVDS CONN



SUPPORT LED INVETER

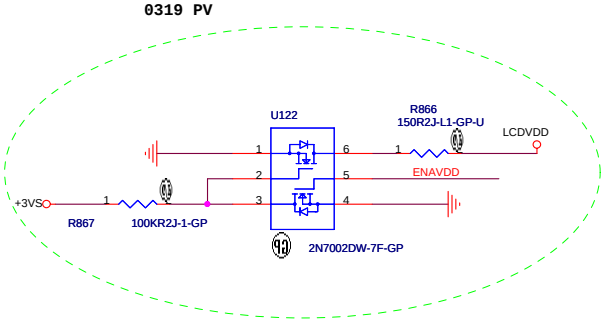


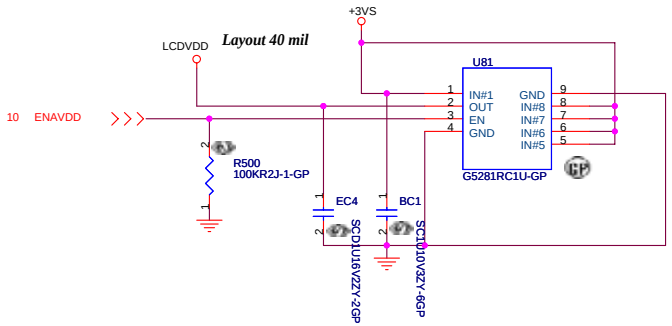
0329 PV Near the LVDS1 connector



LCD POWER CIRCUIT

0319 PV





<Core Design>

蜂創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***LCD CONN.***

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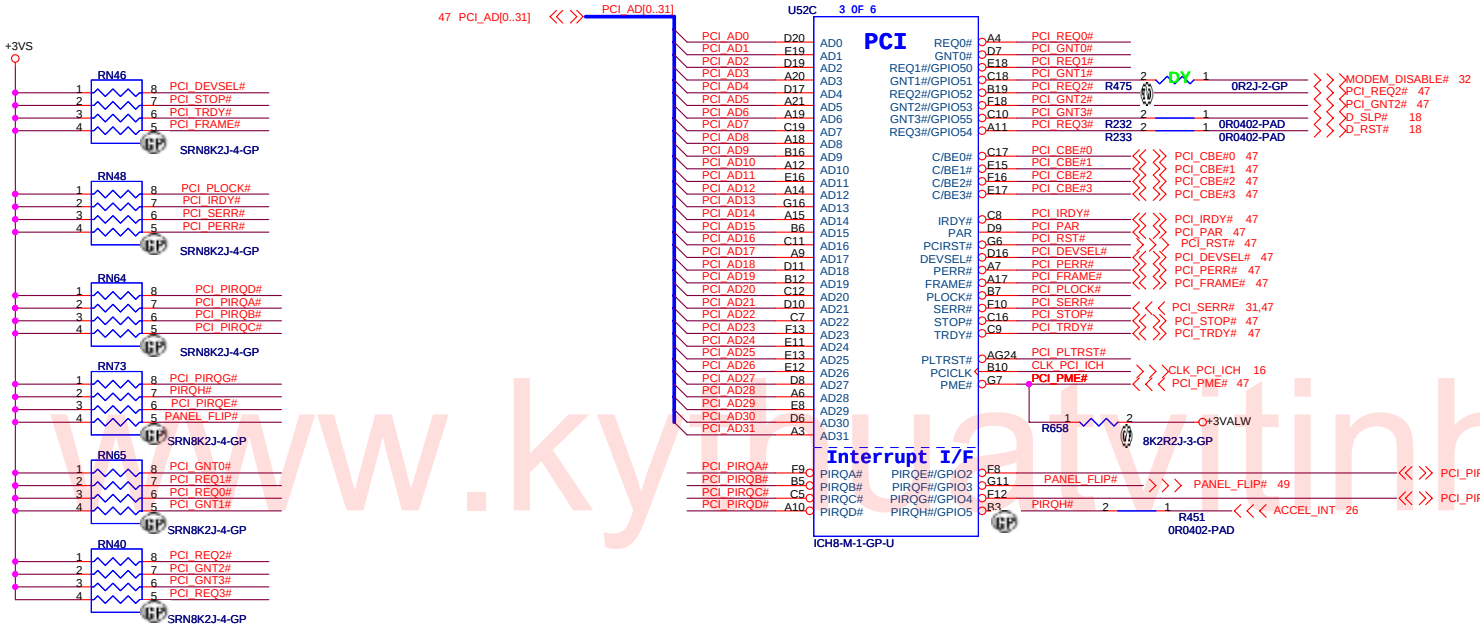
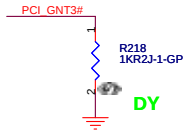
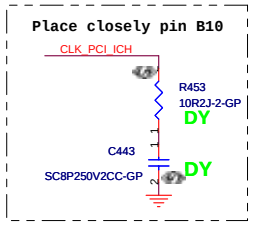
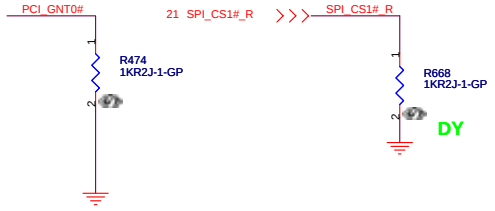


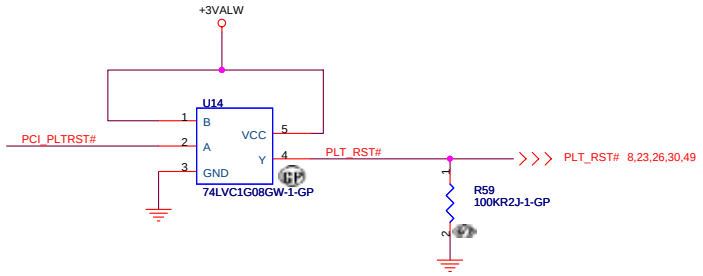


Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI *
1	0	PCI
1	1	LPC

A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enable High= Default *







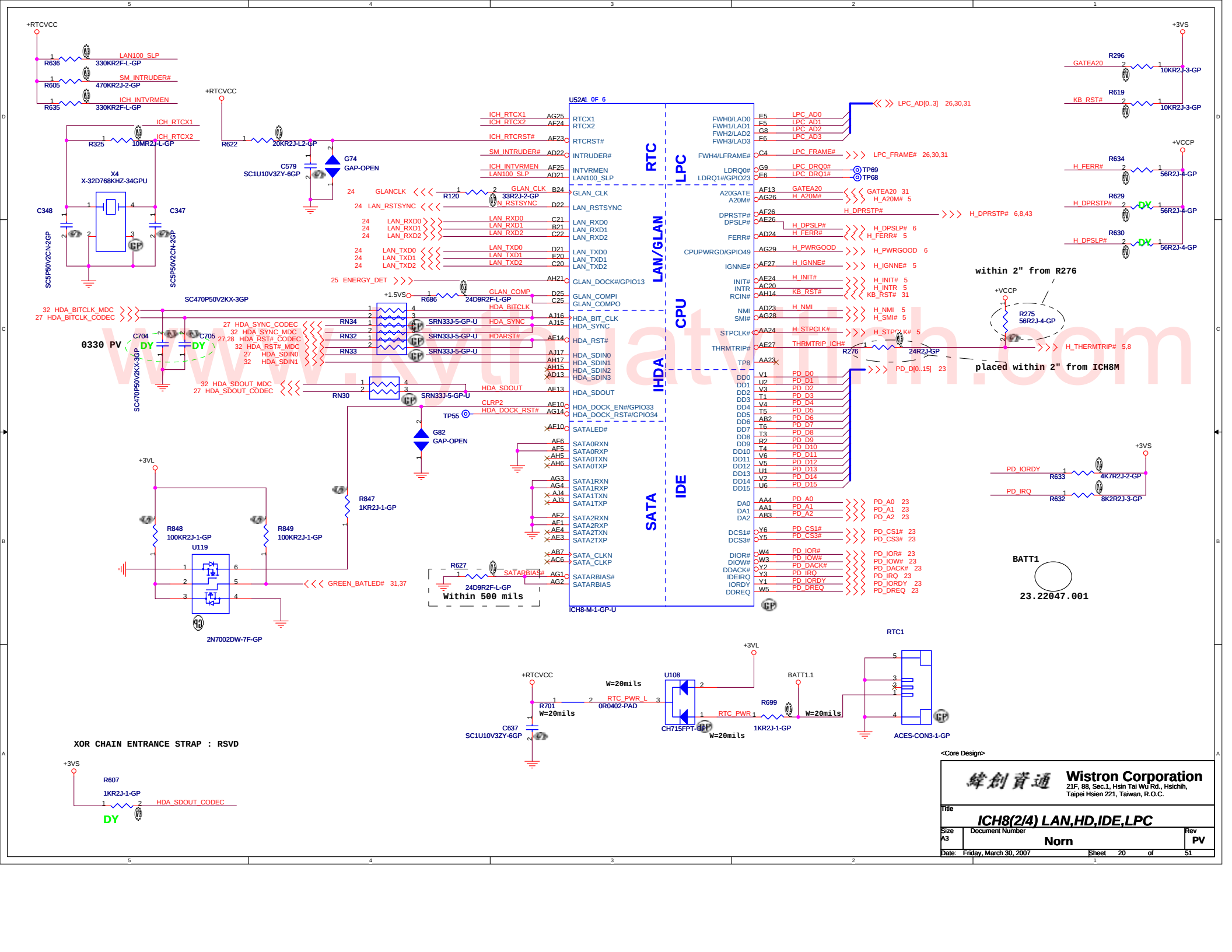
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH8(1/4)-PCI/INT

Size: A3 | Document Number: Norn | Rev: PV

Date: Friday, March 30, 2007 | Sheet 19 of 51



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蜂創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH8(2/4) LAN,HD,IDE,LPC

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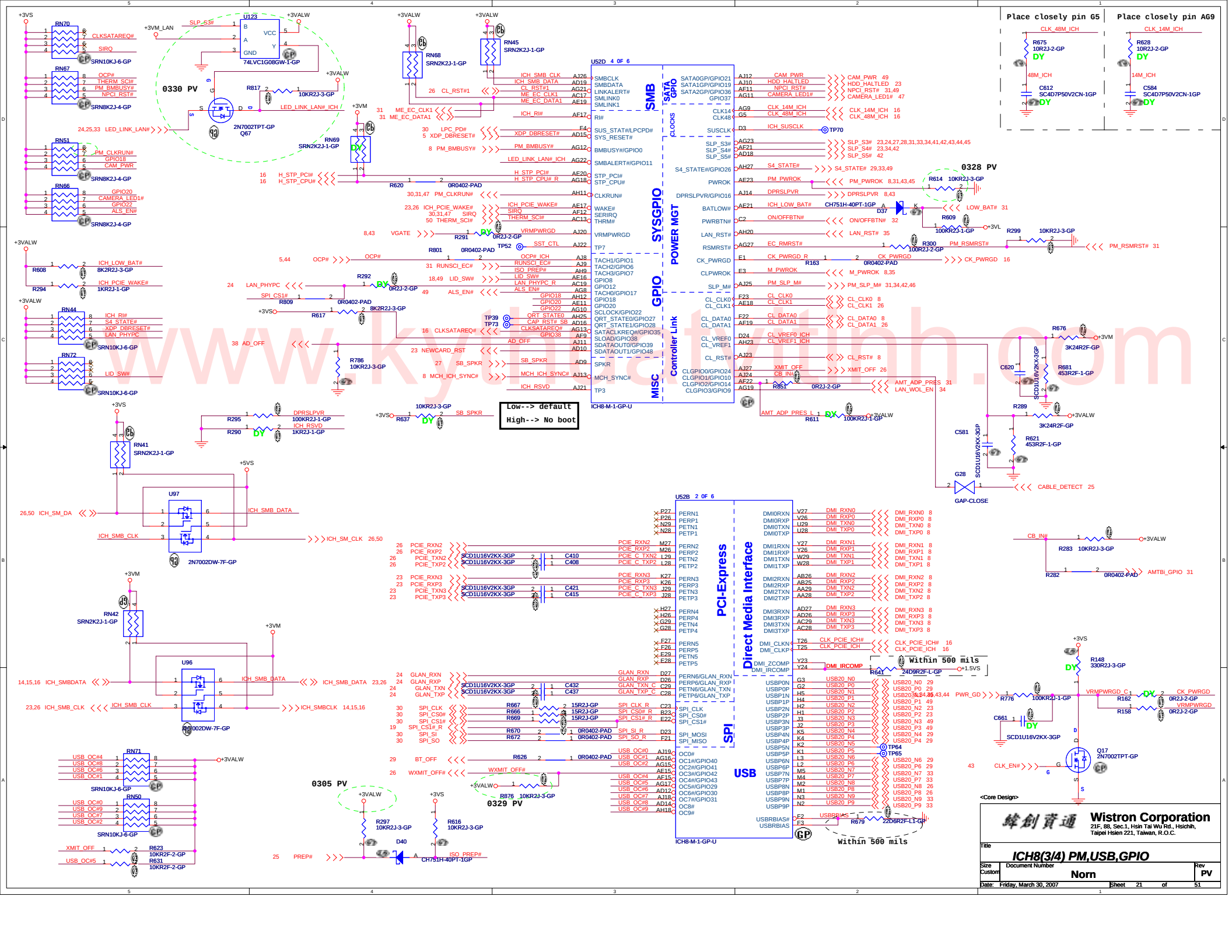

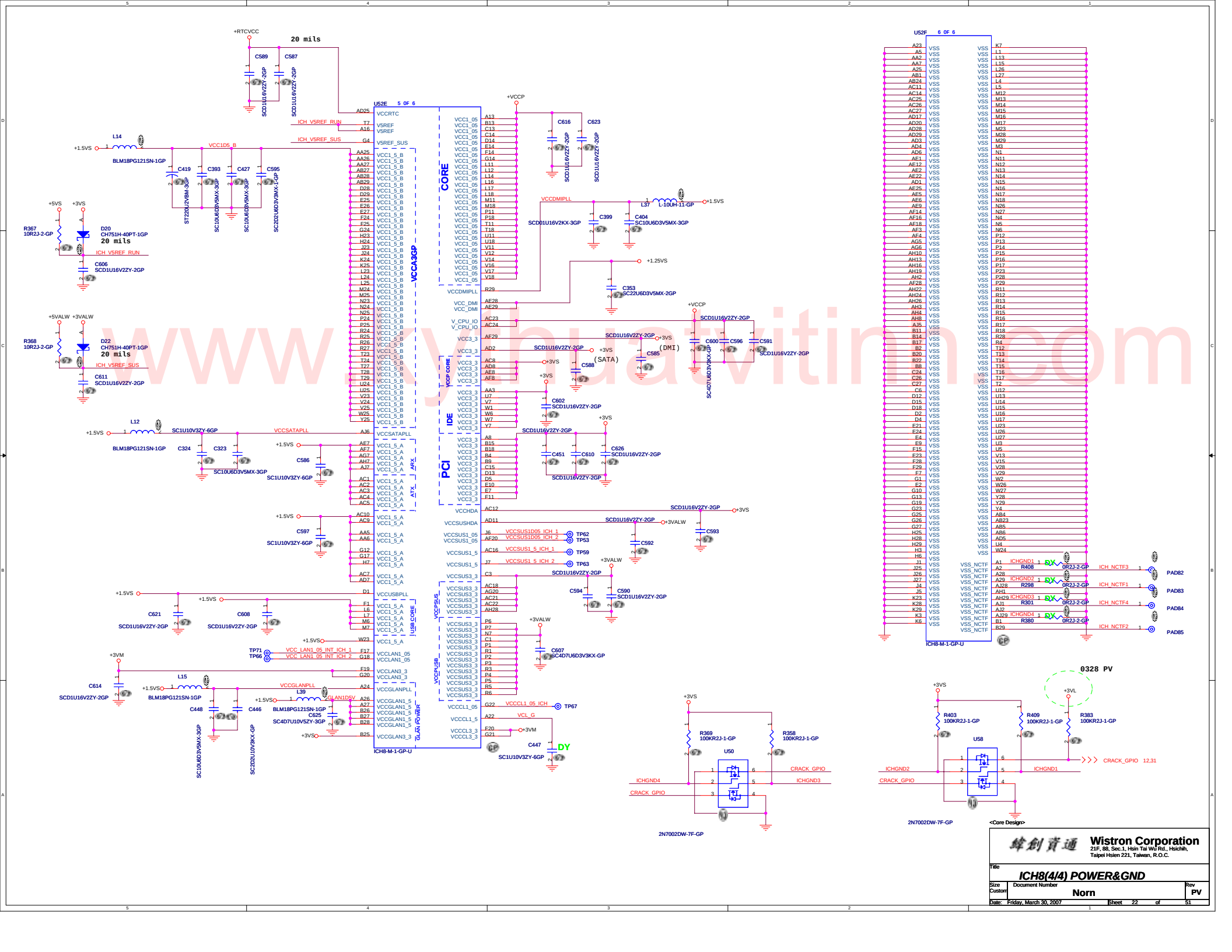
U52E 5 OF 6
U52F 6 OF 6
ICH8-M-1-GP-U
CORE
PCI
IDE
VCCA3GP
VCCP CORE
VCCP SUS
VCCP USB
GLAN POWER
U58
U50
2N7002DW-7F-GP
SC1U10V3ZY-6GP
SCD1U16V2ZY-2GP
SC10U6D3V5MX-3GP
SC4D7U10V5ZY-3GP
SC2D2U10V3KX-GP
SC4D7U6D3V3KX-GP
SC2D2U6D3V3MX-1GP
SCD01U16V2KX-3GP
SC22U6D3V5MX-2GP
SC10U6D3V5MX-3GP
BLM18PG121SN-1GP
L-10UH-11-GP
ST220U2V6M-3GP
R367 10R2J-2-GP
R368 10R2J-2-GP
D20 CH751H-40PT-1GP
D22 CH751H-40PT-1GP
20 mils
R369 100KR2J-1-GP
R358 100KR2J-1-GP
R403 100KR2J-1-GP
R409 100KR2J-1-GP
R383 100KR2J-1-GP
0328 PV
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ICH8(4/4) POWER&GND
Norn
PV
Friday, March 30, 2007
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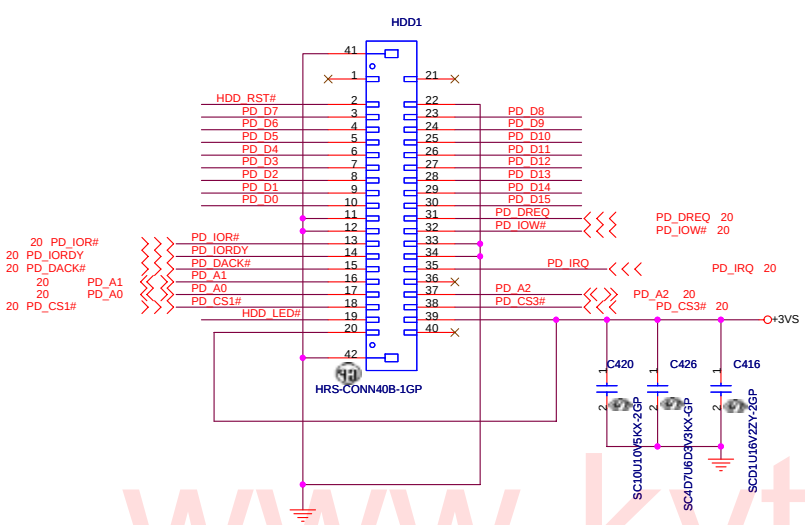
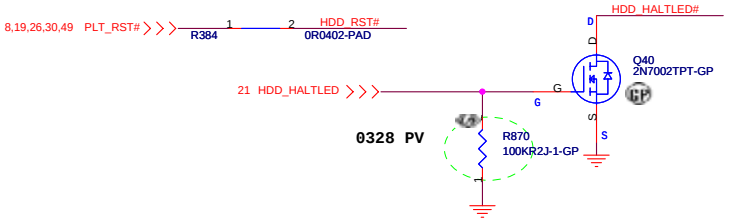
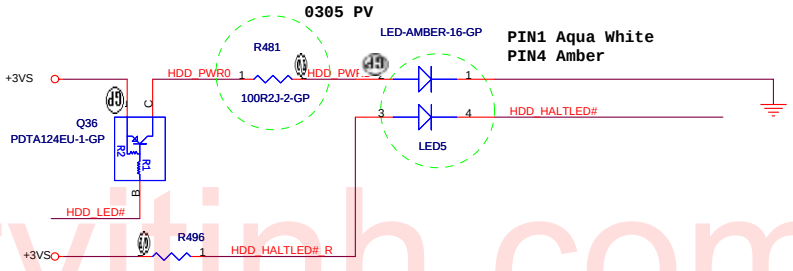
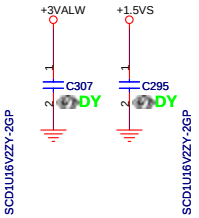
BTB PATA HDD



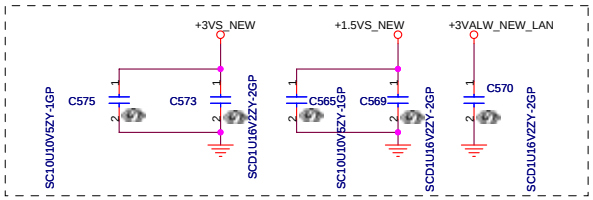


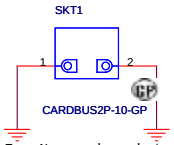


Place them Near to Chip

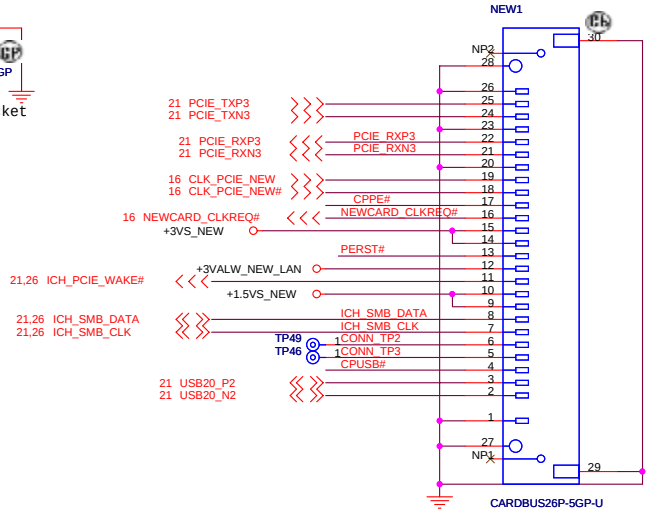


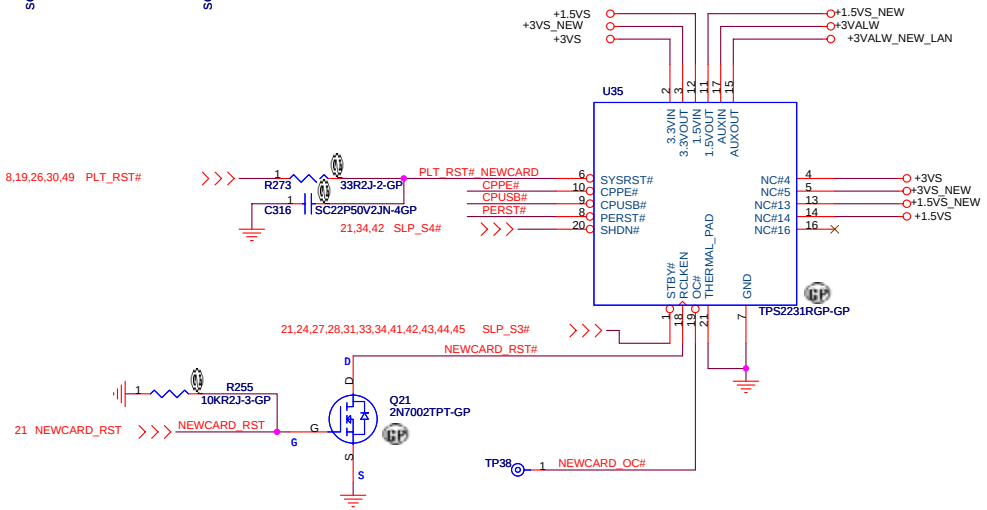
Place them Near to Connector





NEWCARD Connector





<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **HDD /NEW CARD CONN.**

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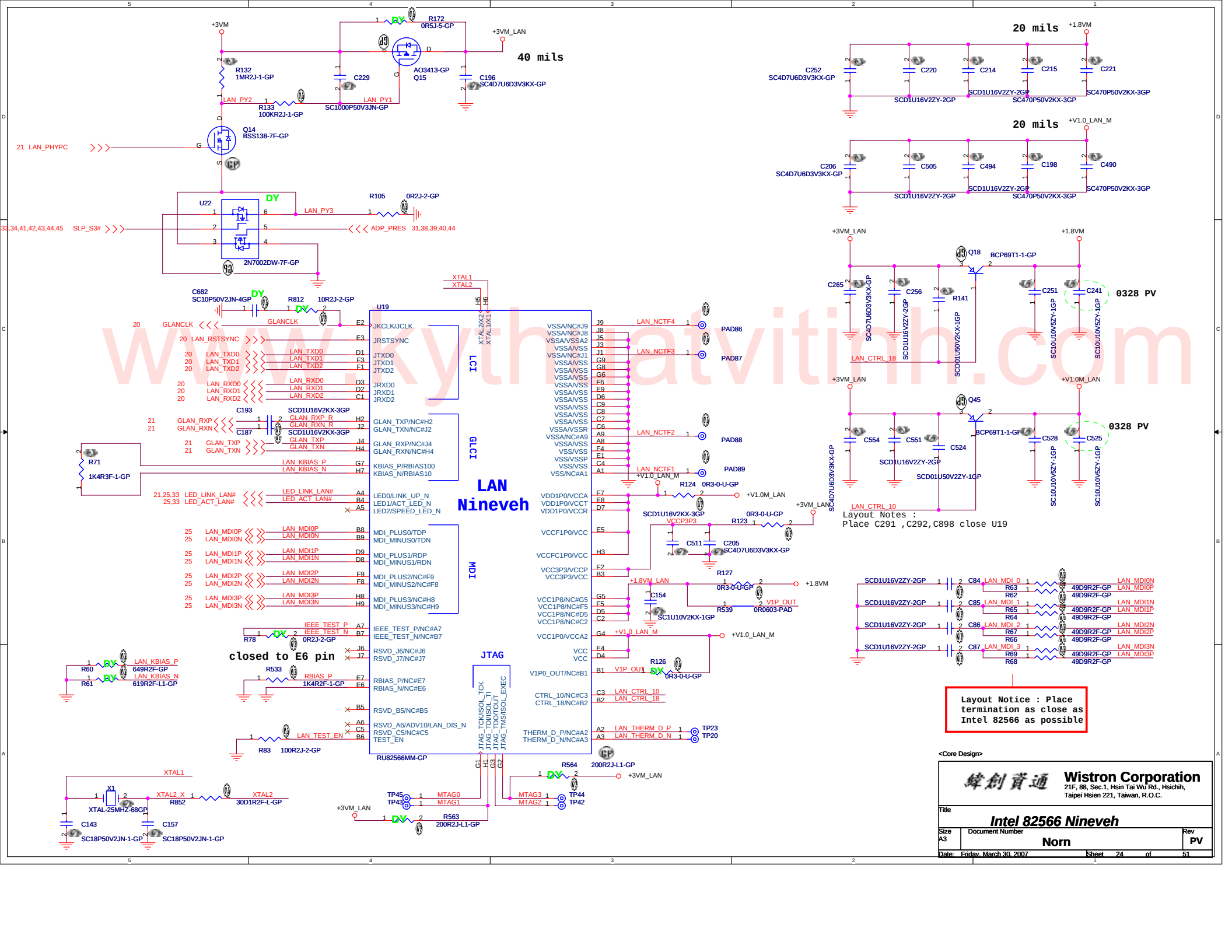
A3	NORN	PV

Date: Friday, March 30, 2007 Sheet 23 of 51


LAN Nineveh
RU82566MM-GP
JTAG
GLCI
MDI
LCI
40 mils
20 mils
20 mils
0328 PV
0328 PV
Layout Notes :
Place C291 ,C292,C898 close U19
closed to E6 pin
Layout Notice : Place termination as close as Intel 82566 as possible
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Intel 82566 Nineveh
Norn
PV
Friday, March 30, 2007
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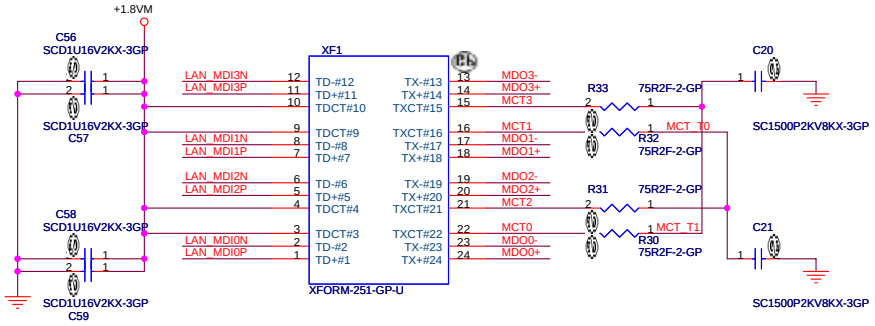
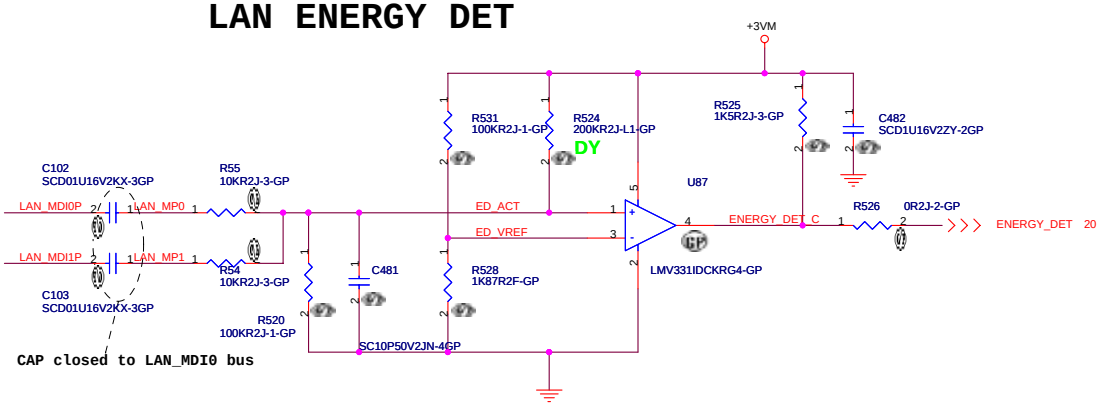
RJ-45 CONN.



LAN ENERGY DET

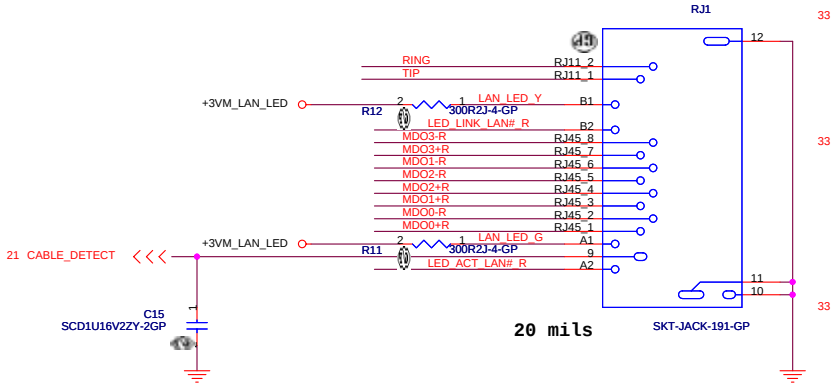


CAP closed to LAN_MDI0 bus

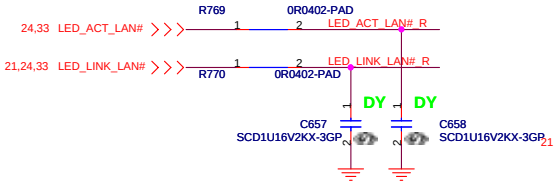
LAN_MDI0N 24
LAN_MDI0P 24
LAN_MDI1N 24
LAN_MDI1P 24
LAN_MDI2N 24
LAN_MDI2P 24
LAN_MDI3N 24
LAN_MDI3P 24

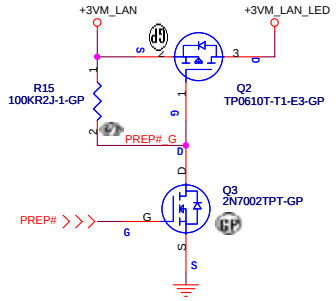
33 MDO3- → MDO3- R761 0R2J-2-GP MDO3-R
33 MDO2+ → MDO2+ R762 0R2J-2-GP MDO2+R

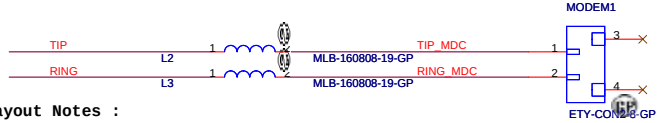
Note : MDO[3..0]+- signals should route to RJ45 first then to DOCK CONN .



33 MDO3+ → MDO3+ R764 0R2J-2-GP MDO3+R
33 MDO2- → MDO2- R763 0R2J-2-GP MDO2-R
33 MDO1- → MDO1- R765 0R2J-2-GP MDO1-R
33 MDO0- → MDO0- R766 0R2J-2-GP MDO0-R
33 MDO1+ → MDO1+ R767 0R2J-2-GP MDO1+R
33 MDO0+ → MDO0+ R768 0R2J-2-GP MDO0+R







Layout Notes :
Place MODEM1 & BEAD near RJ11 connector

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: Magnetic & RJ45/RJ11

Size	Document Number	Rev
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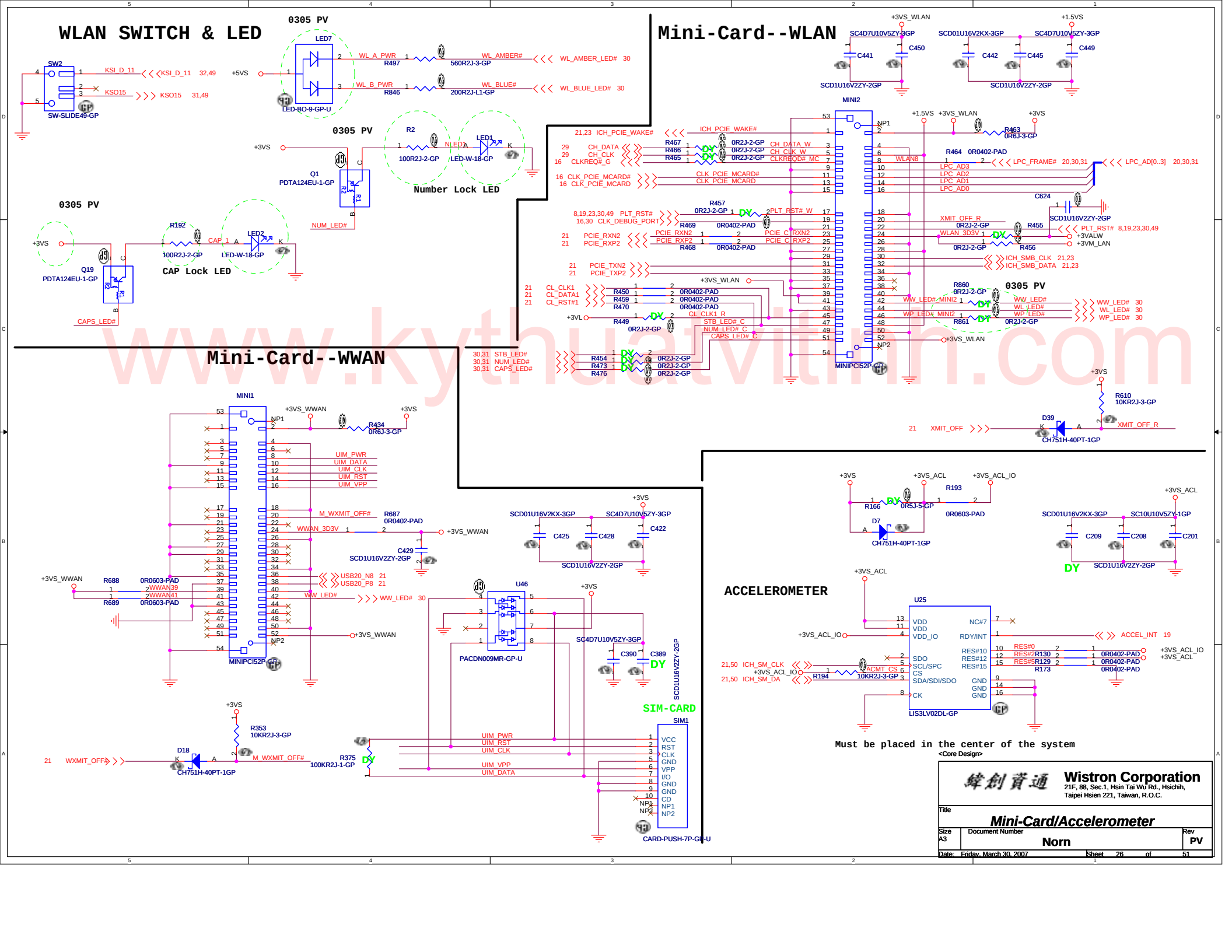
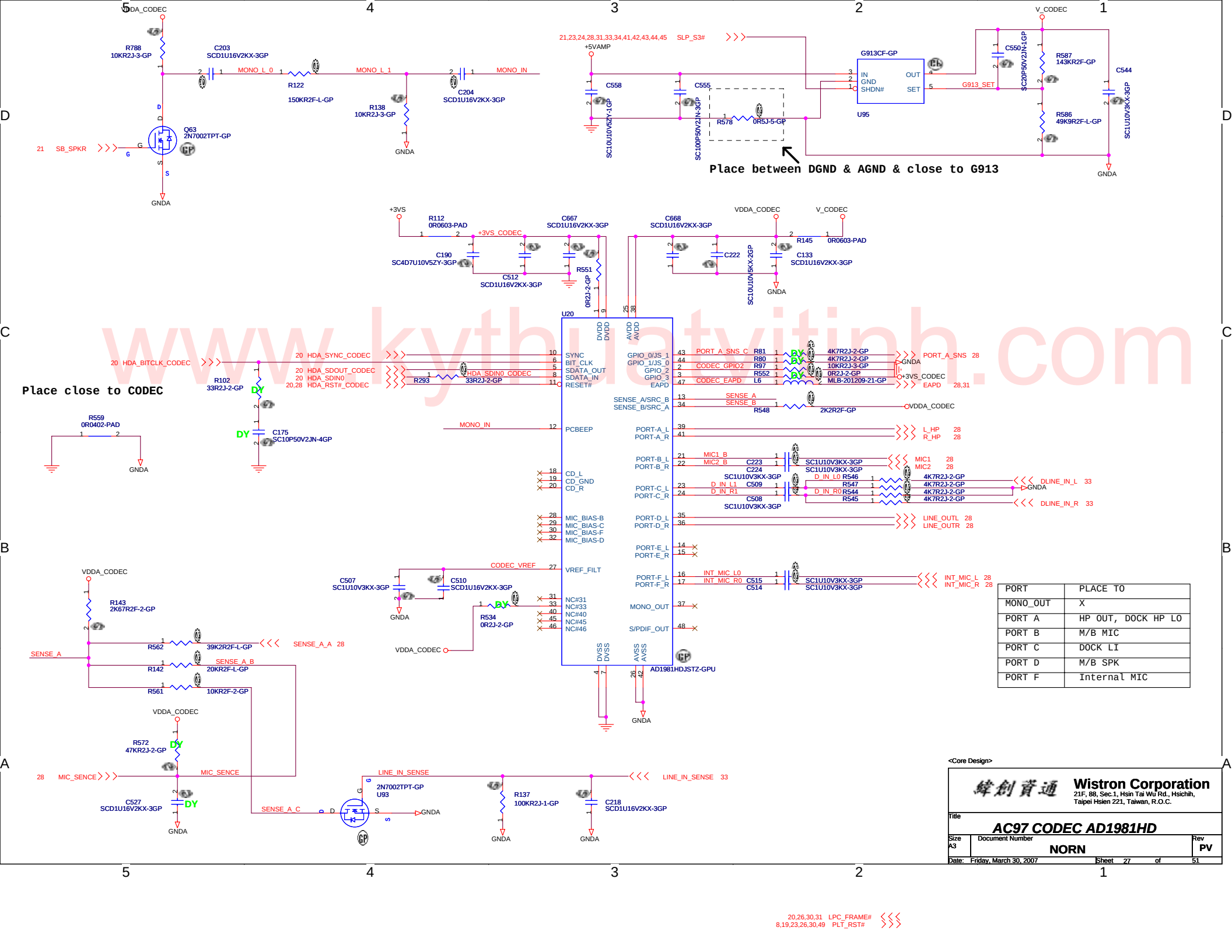
Date: Friday, March 30, 2007 Sheet 25 of 51





PORT	PLACE TO
MONO_OUT	X
PORT A	HP OUT, DOCK HP LO
PORT B	M/B MIC
PORT C	DOCK LI
PORT D	M/B SPK
PORT F	Internal MIC

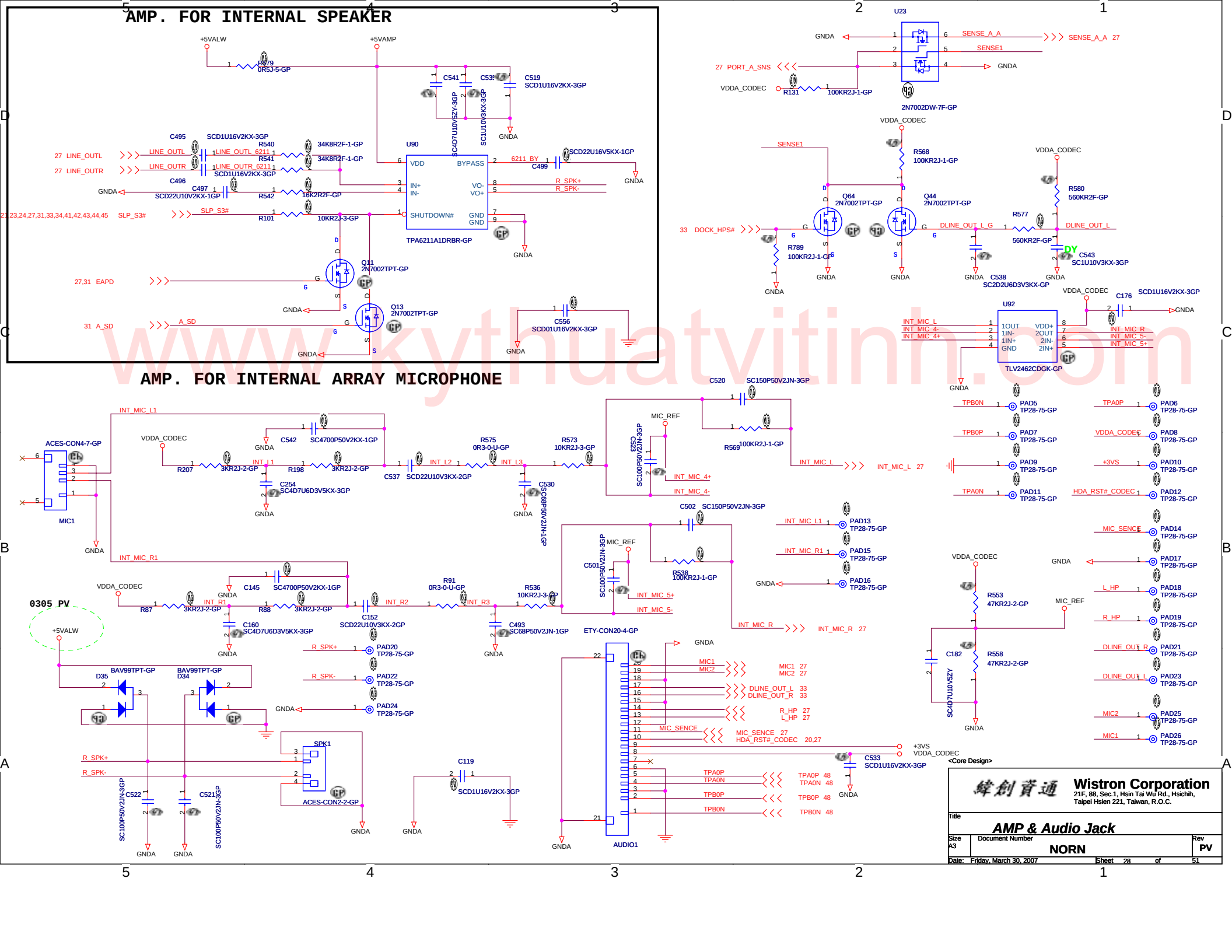
<Core Design>

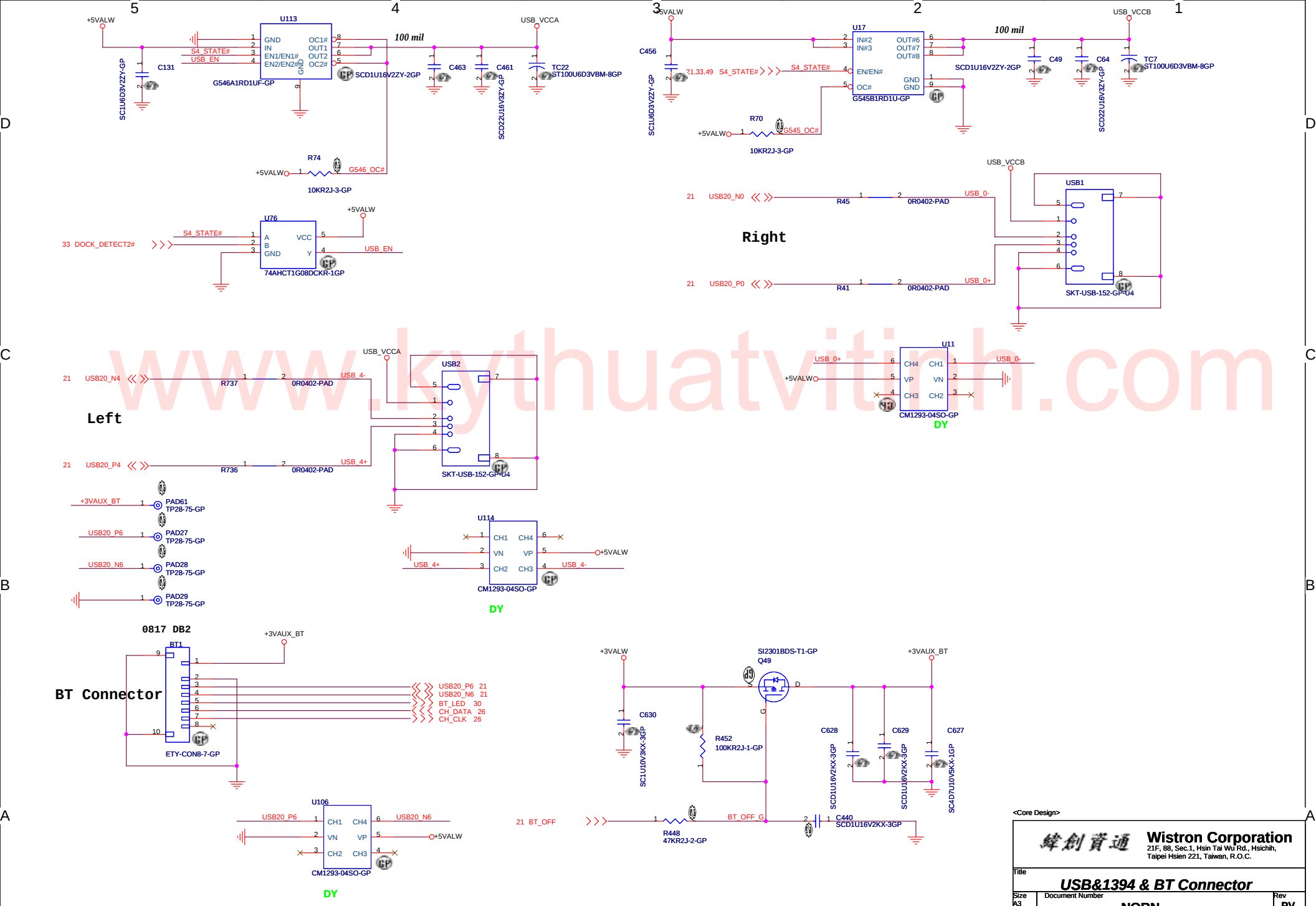
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AC97 CODEC AD1981HD

Size: A3 | Document Number: NORN | Rev: PV

Date: Friday, March 30, 2007 | Sheet 27 of 51

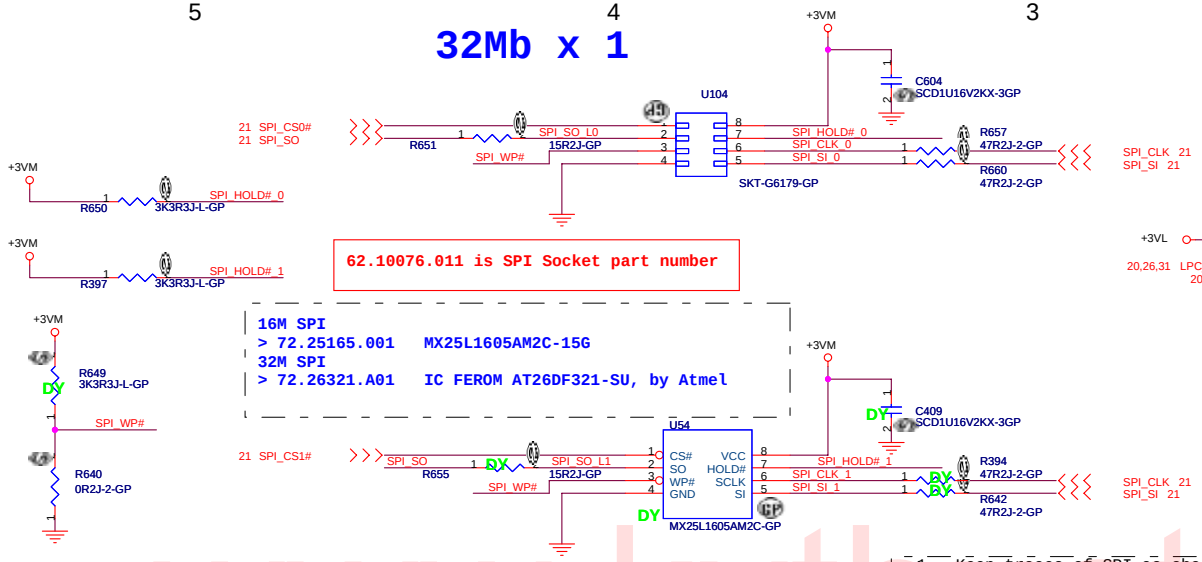




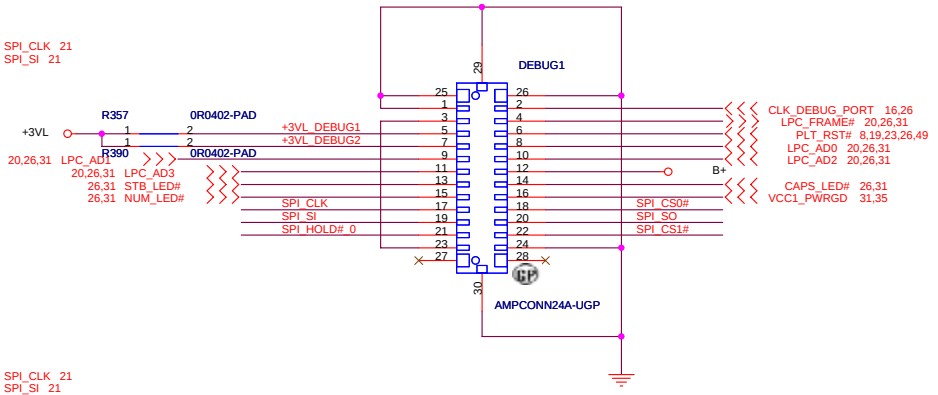
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

<Core Design>
Title: USB&1394 & BT Connector
Size: A3
Document Number: NORN
Rev: PV
Date: Friday, March 30, 2007
Sheet 29 of 51

32Mb x 1



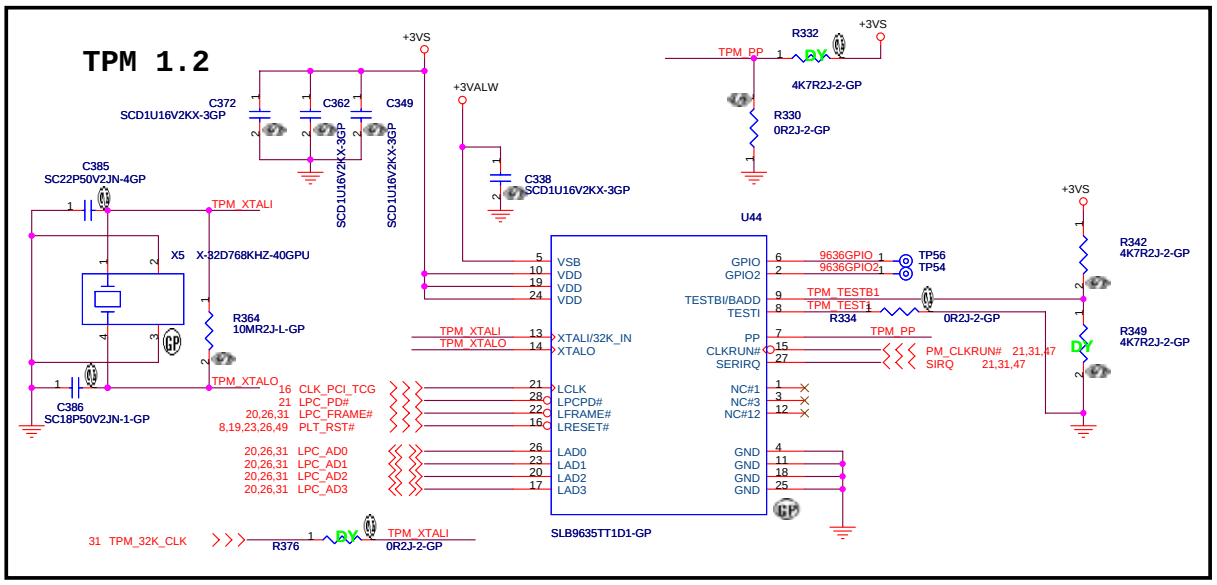
Debug port



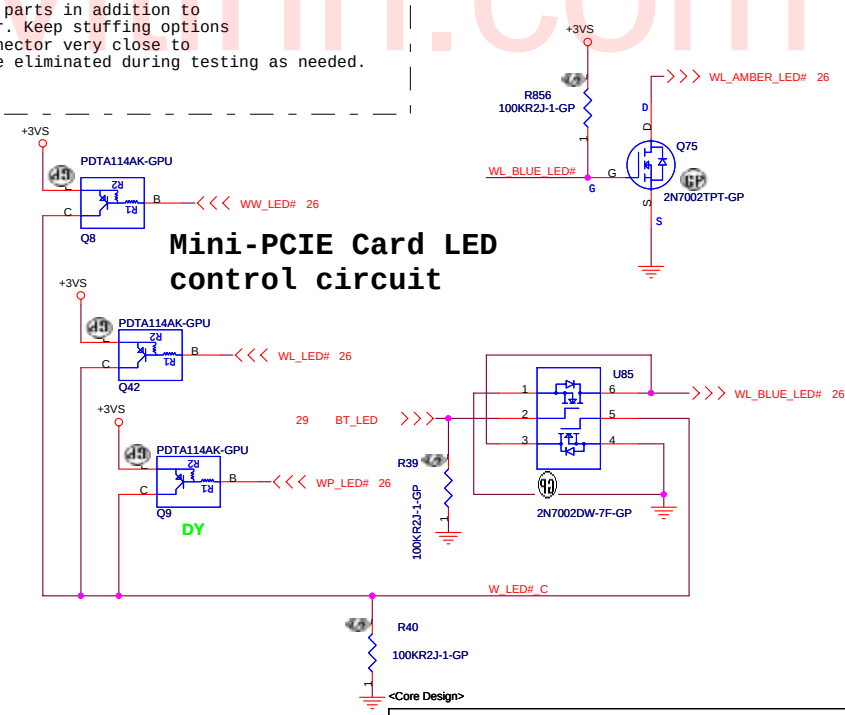
1. Keep traces of SPI as short as possible and keep trace spacing close to 7mils to any other signal (basically follow specs).

2. AMT designs need 2x2MB SPI parts in addition to connecting to a debug connector. Keep stuffing options from 2nd SPI part to debug connector very close to 2nd part so stub effect can be eliminated during testing as needed.

TPM 1.2



Mini-PCIE Card LED control circuit



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Title: TPM/BIOS/24 DEBUG PORT

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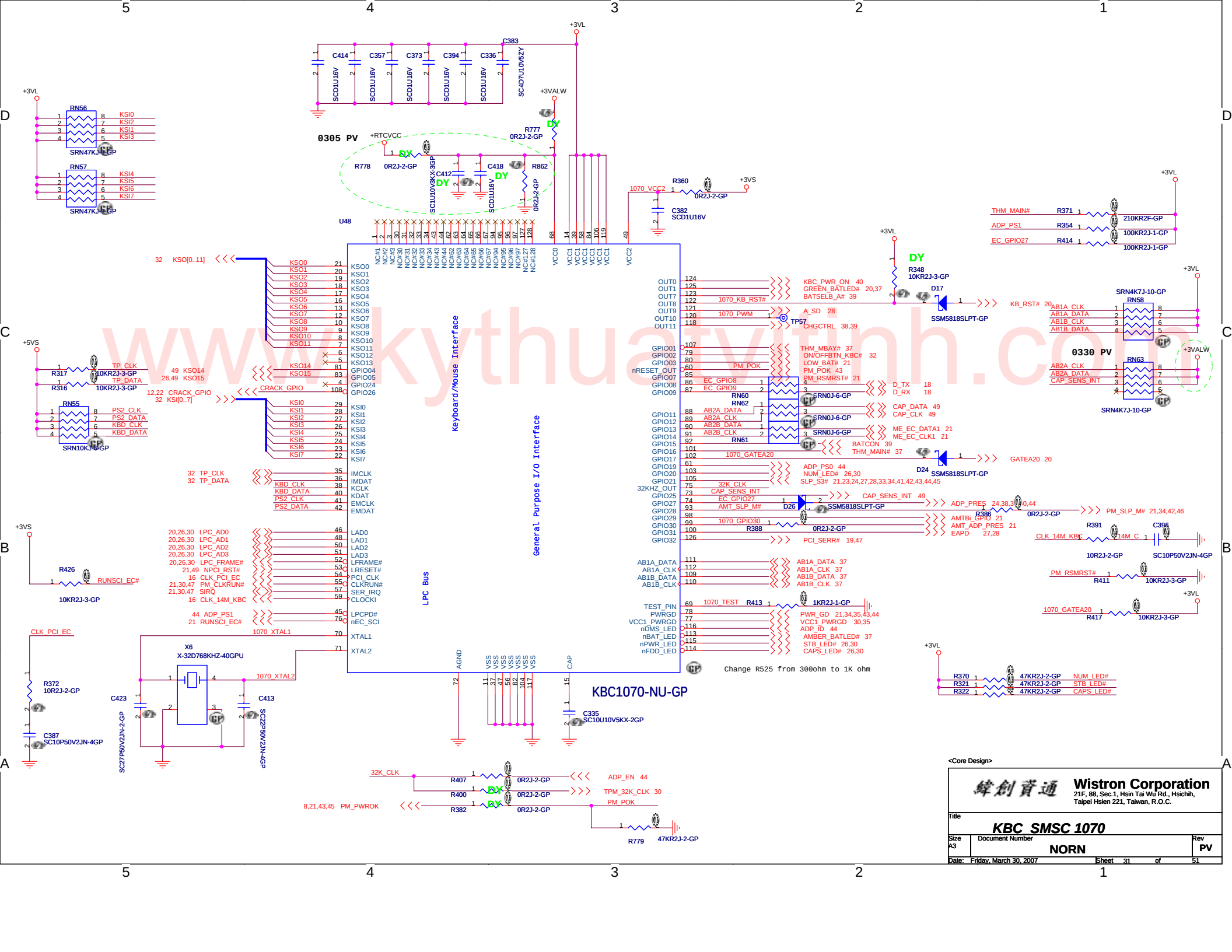
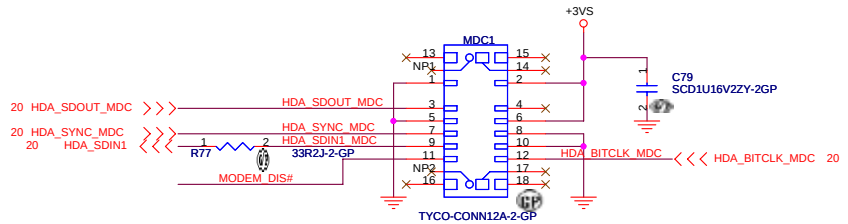
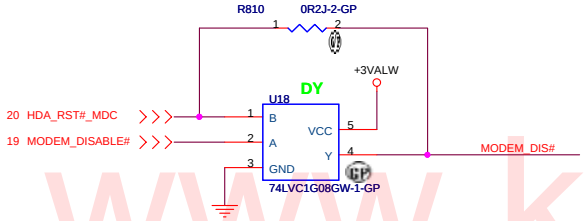


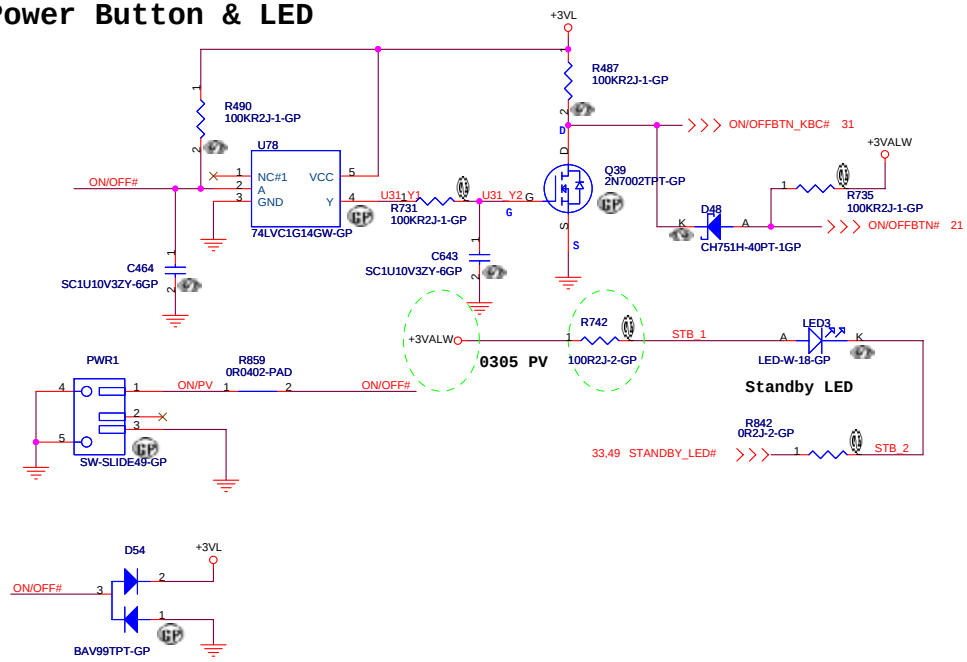
MDC 1.5 Conn.



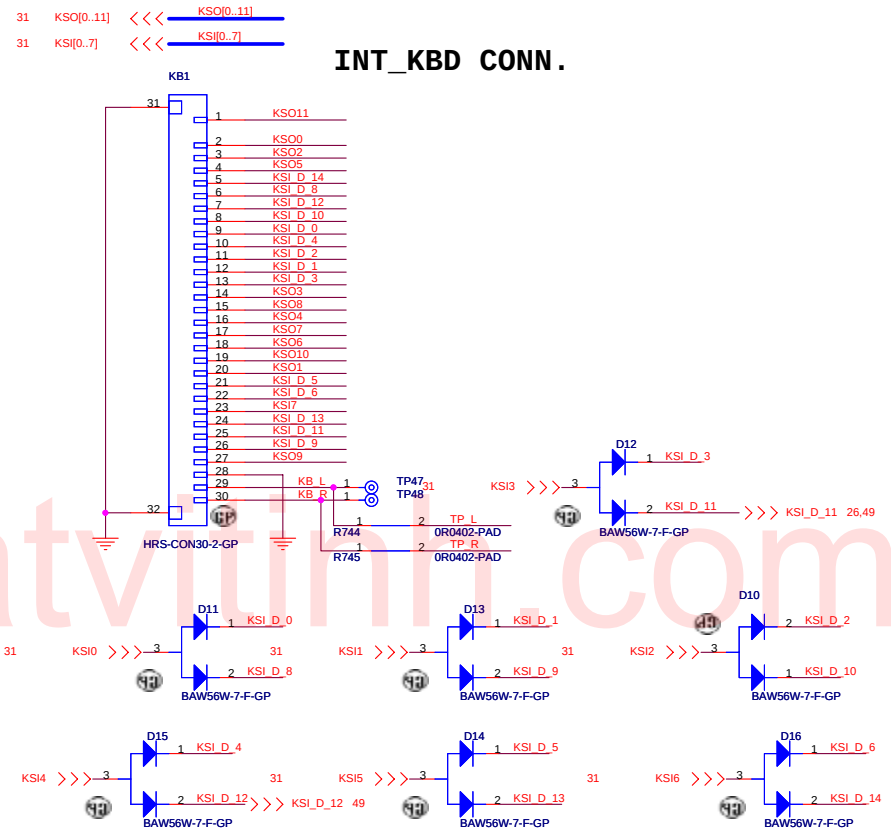
Connector for MDC Rev1.5



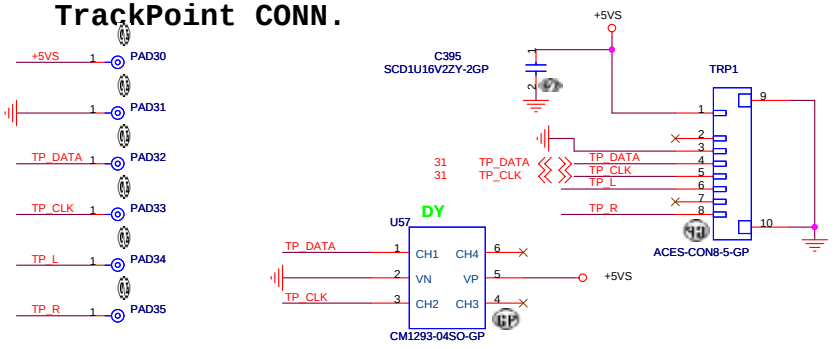
Power Button & LED



INT_KBD CONN.

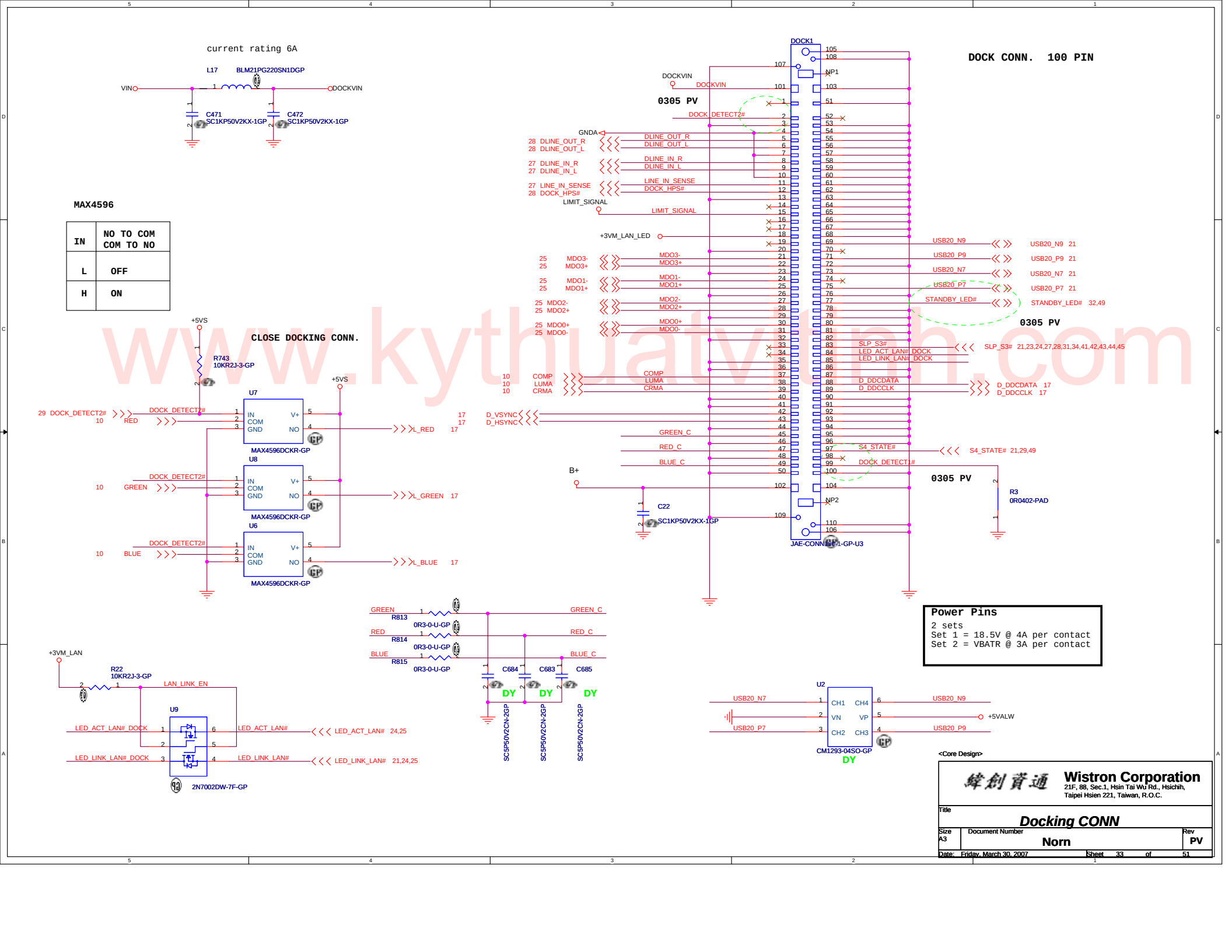


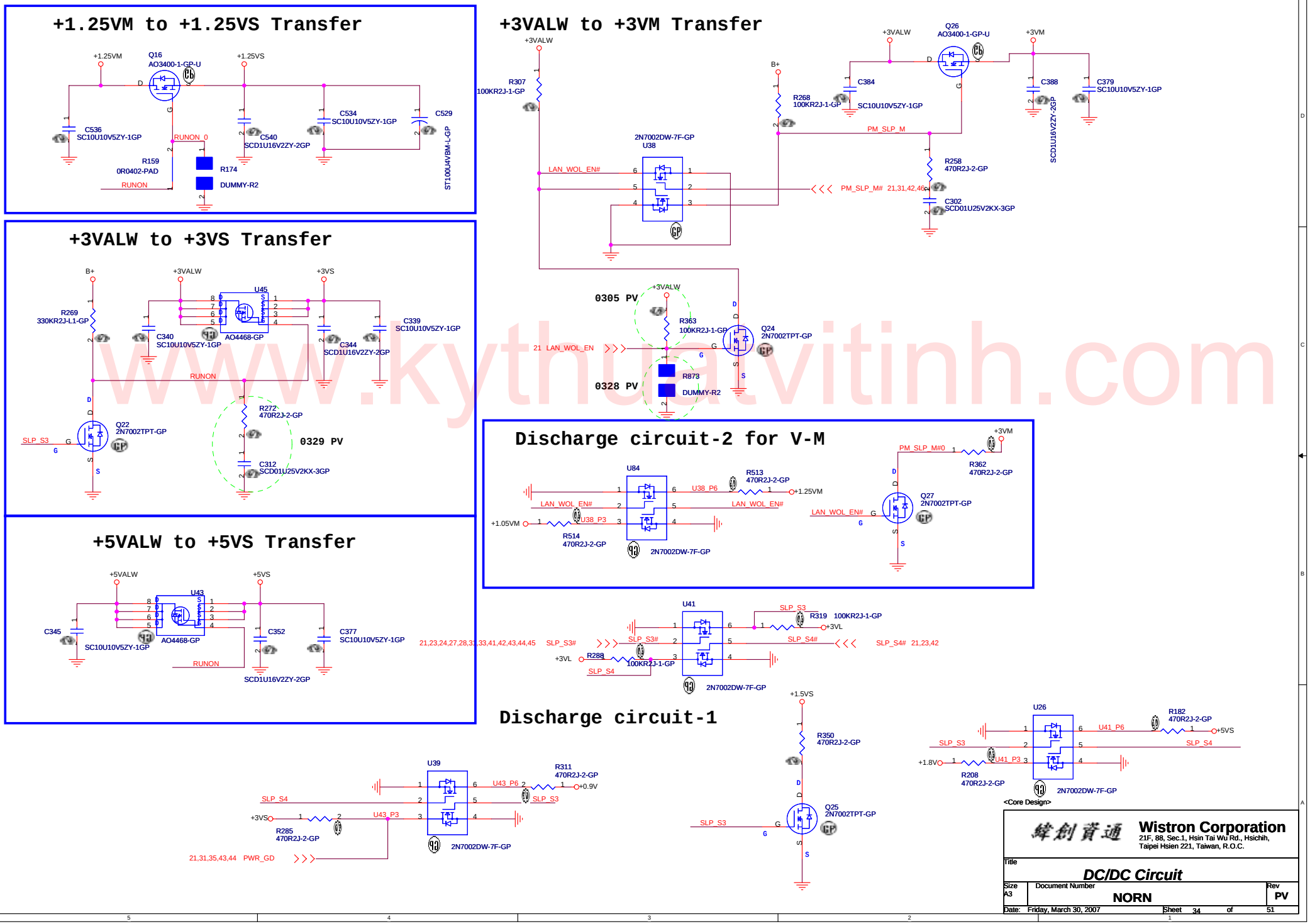
TrackPoint CONN.

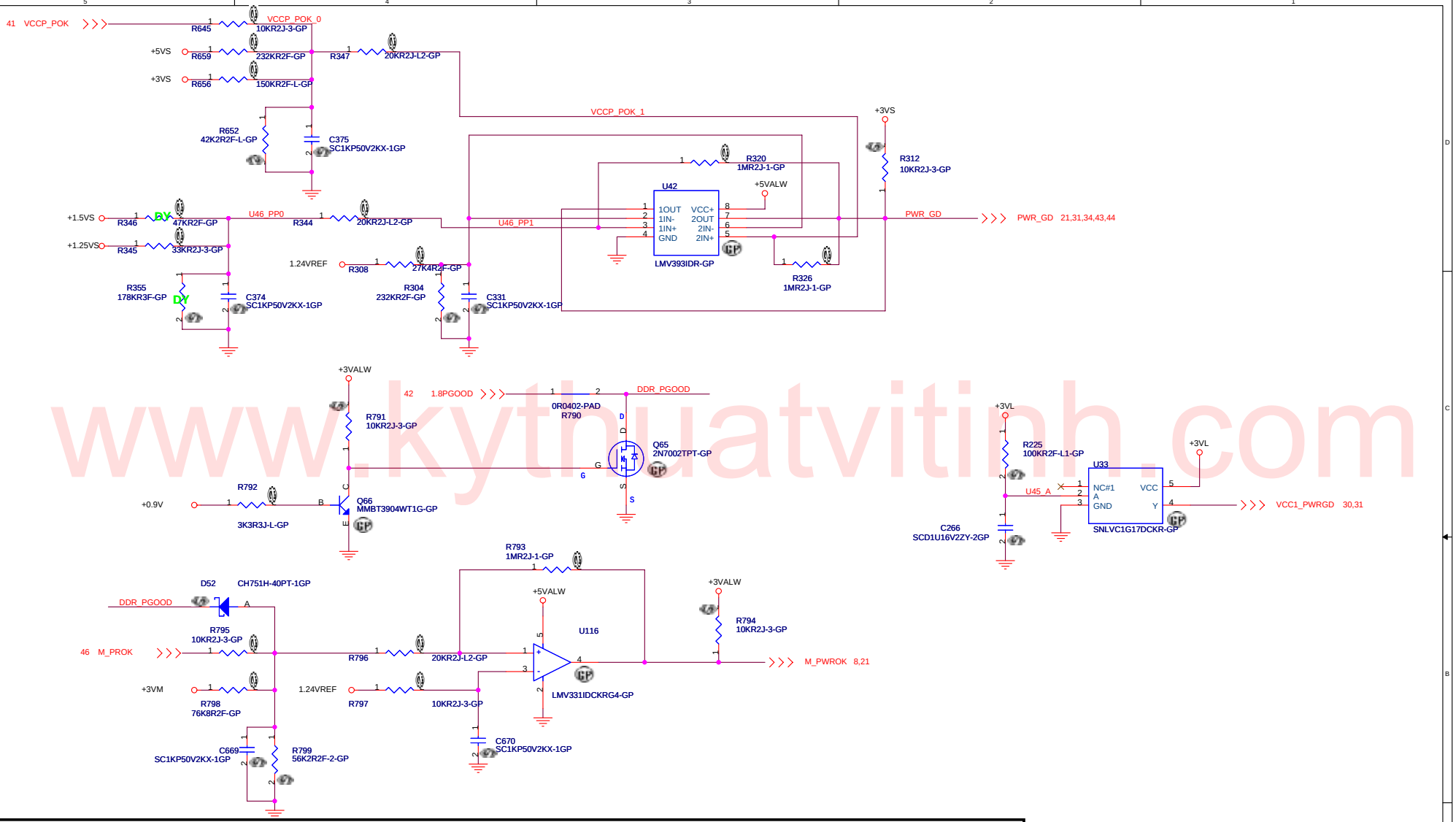


<Core Design>

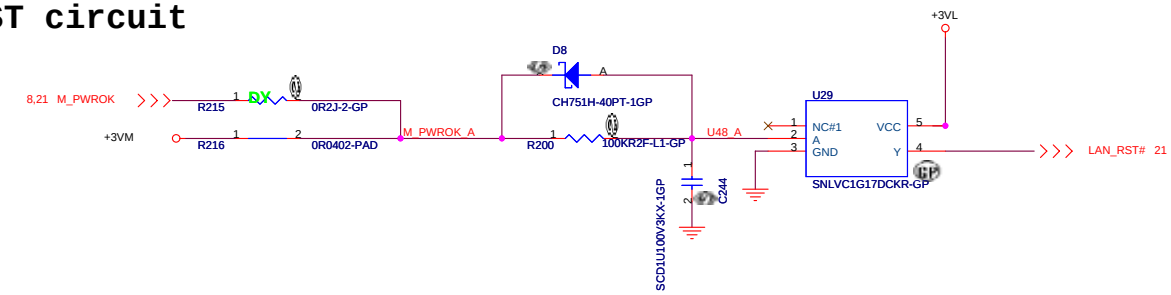
鋒創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***MDC/KBD/ON OFF/T.P.***
Size A3 / Document Number	Norn / Rev PV
Date: Friday, March 30, 2007	Sheet 32 of 51







LAN_RST circuit



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: POK CKT

Size: A3 | Document Number: NORN | Rev: PV

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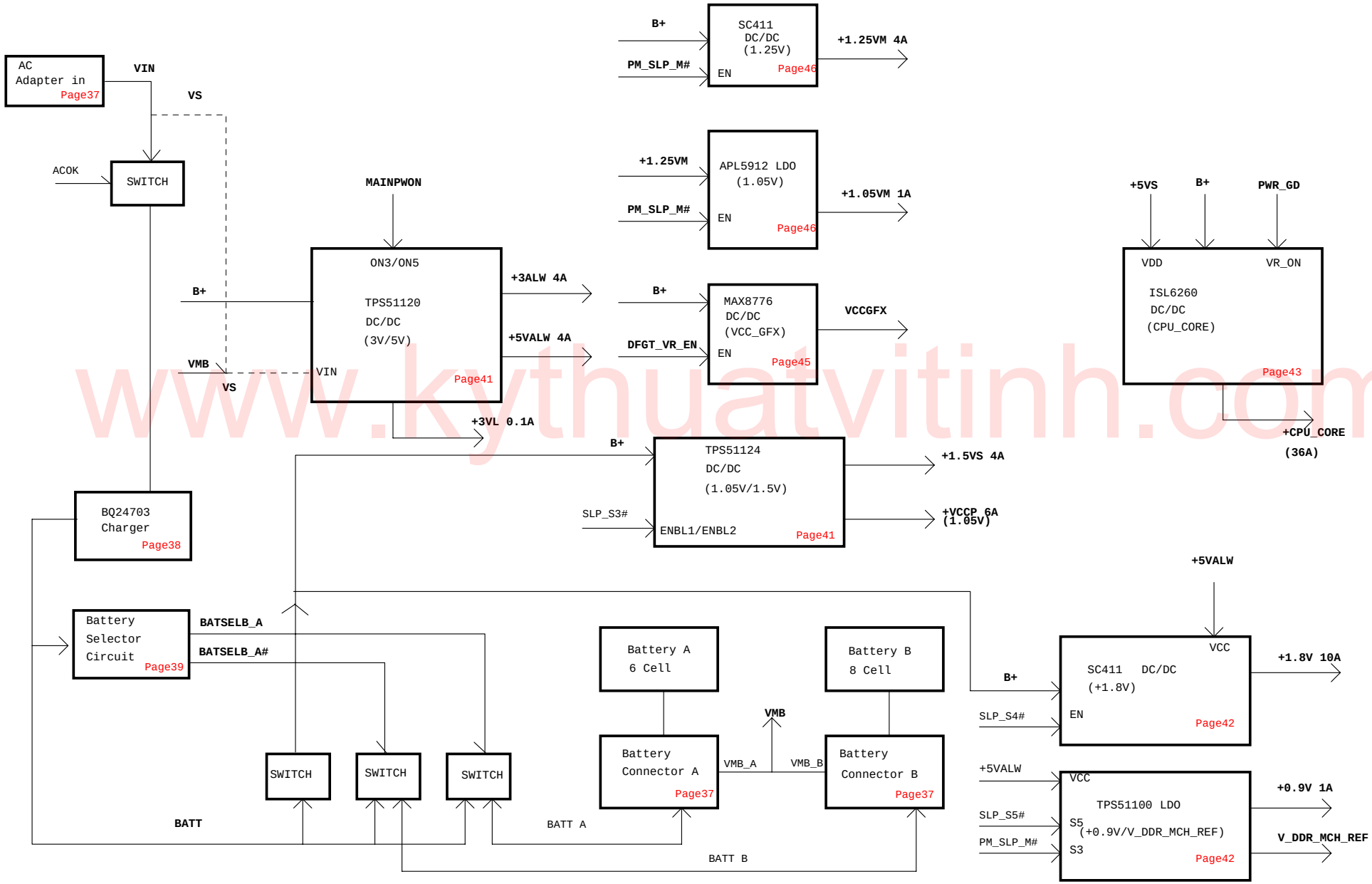

<Variant Name>

蜂創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Block Diagram**

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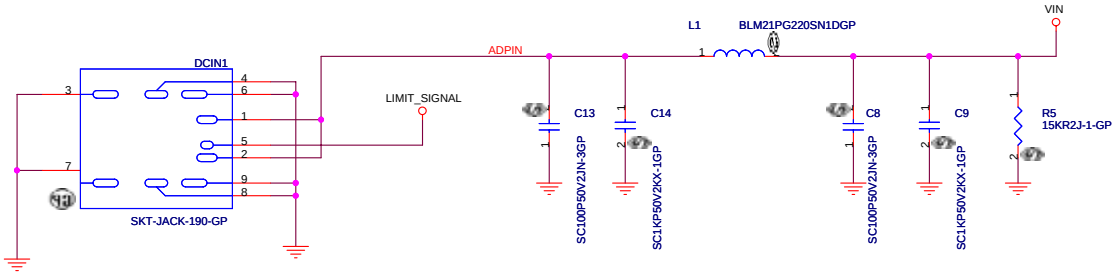
Adaptor in to generate DCBATOUT

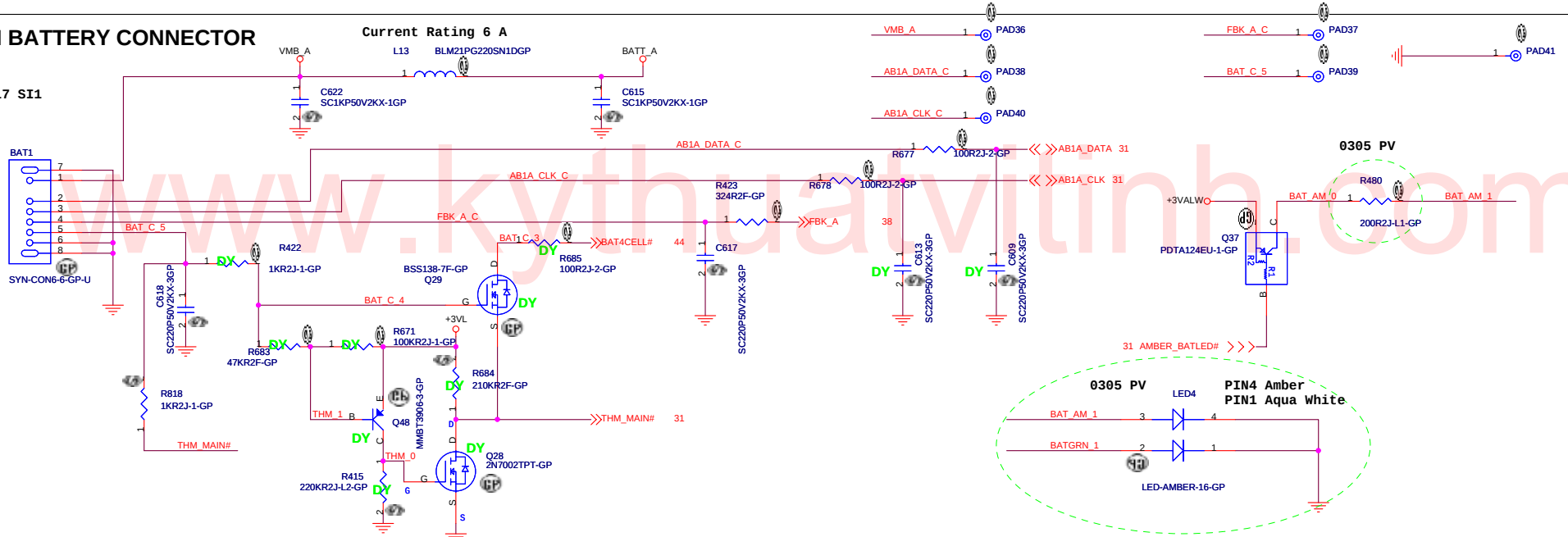
Current Rating 6 A



MAIN BATTERY CONNECTOR

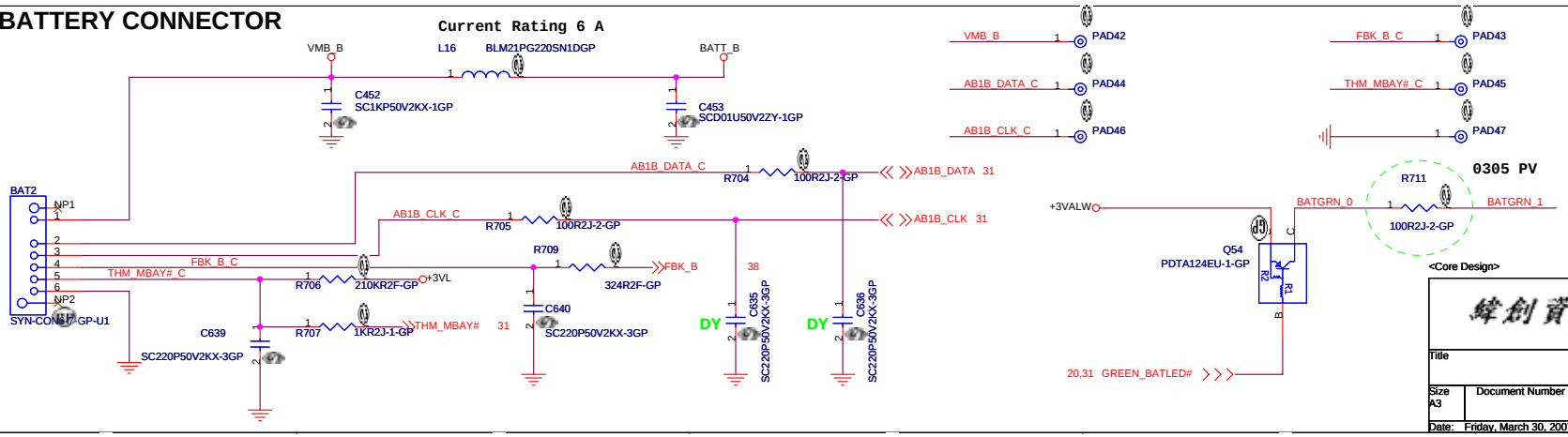
Current Rating 6 A

1017 SI1



BAY BATTERY CONNECTOR

Current Rating 6 A



Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: DC & BATTERT CONN.

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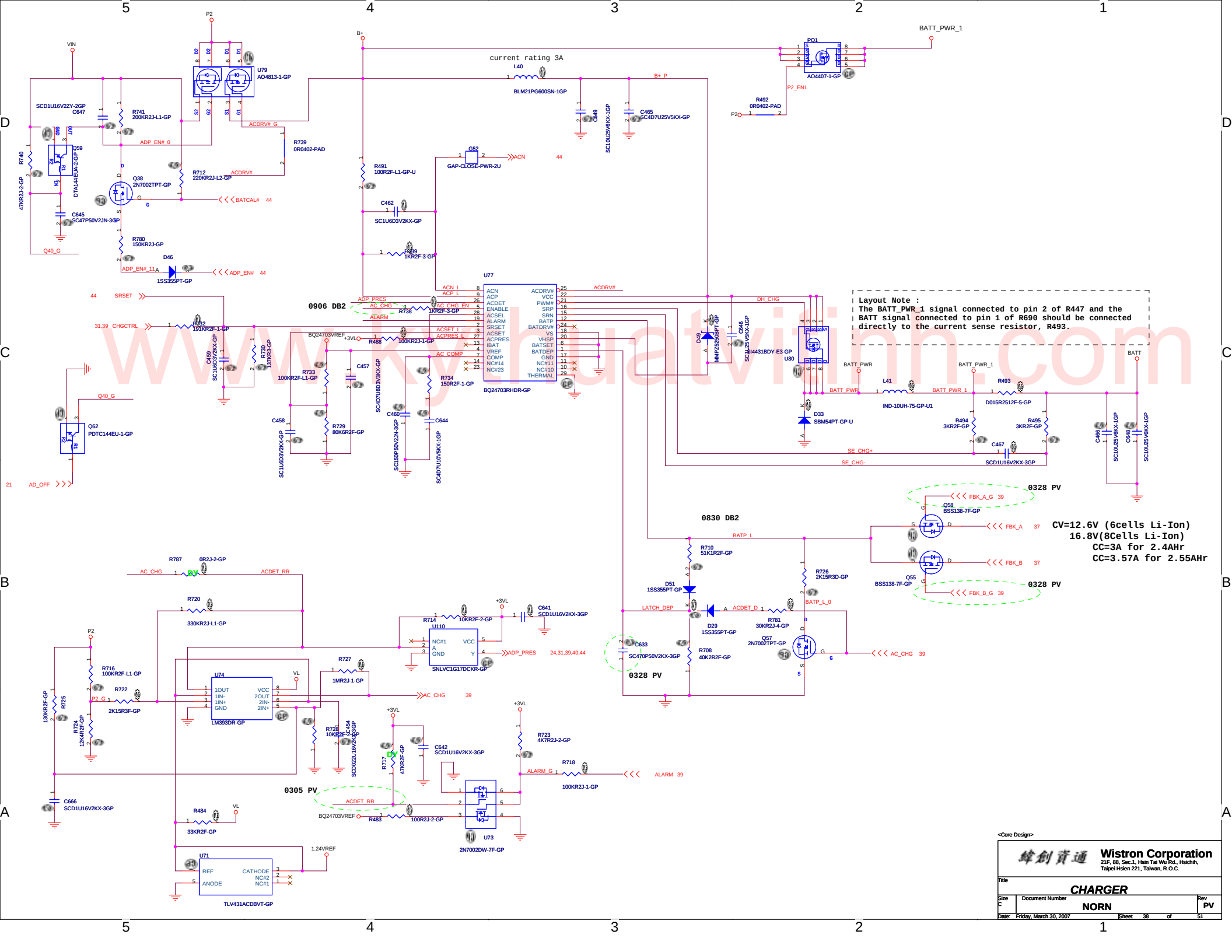
current rating 3A
Layout Note :
The BATT_PWR_1 signal connected to pin 2 of R447 and the BATT signal connected to pin 1 of R690 should be connected directly to the current sense resistor, R493.
0906 DB2
0830 DB2
0328 PV
0305 PV
CV=12.6V (6cells Li-Ion)
16.8V(8Cells Li-Ion)
CC=3A for 2.4AHr
CC=3.57A for 2.55AHr
BQ24703RHDR-GP
TLV431ACDBVT-GP
LM393DR-GP
SNLVC1G17DCKR-GP
2N7002DW-7F-GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
CHARGER
NORN
PV
Friday, March 30, 2007
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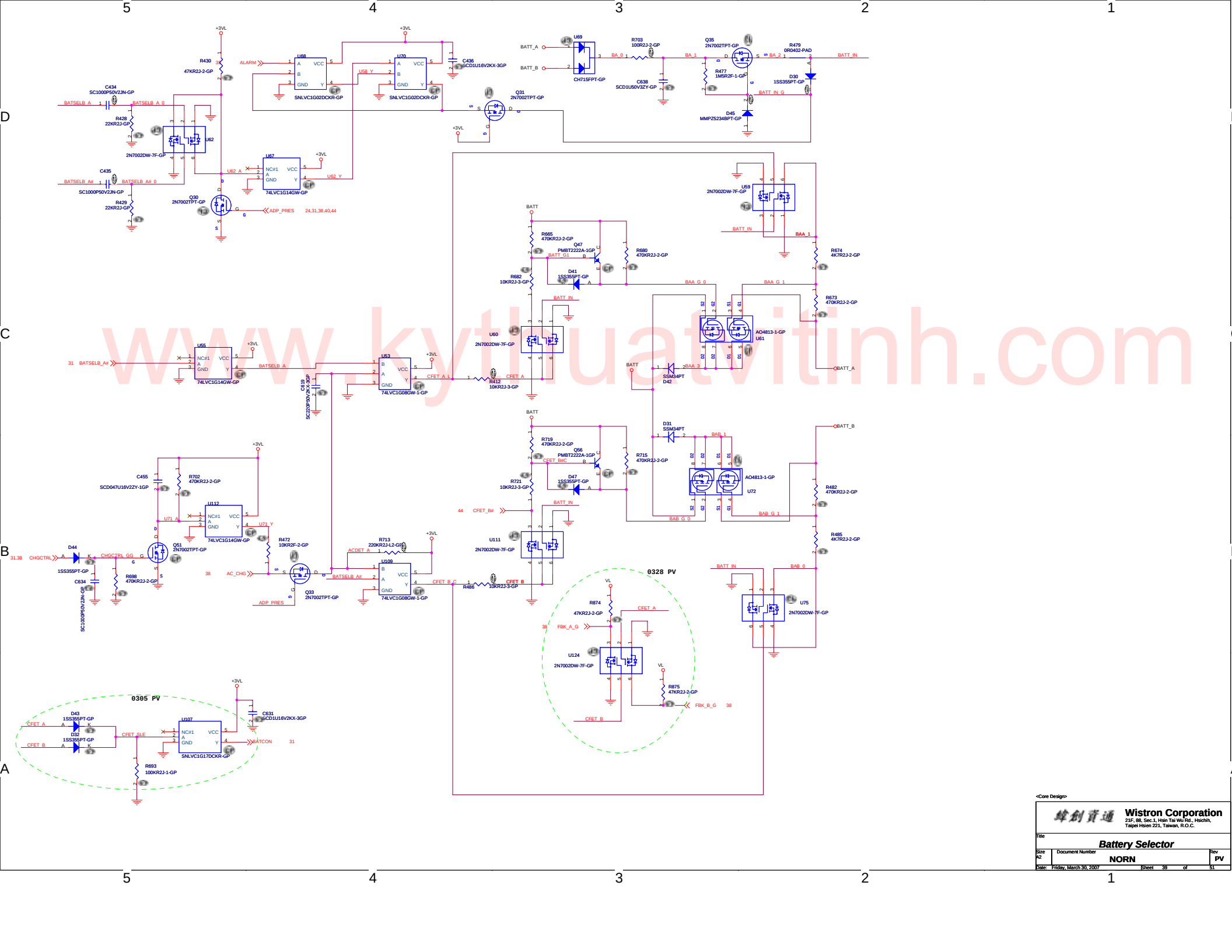

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Battery Selector

Size	Document Number	Rev
A2	NORN	PV

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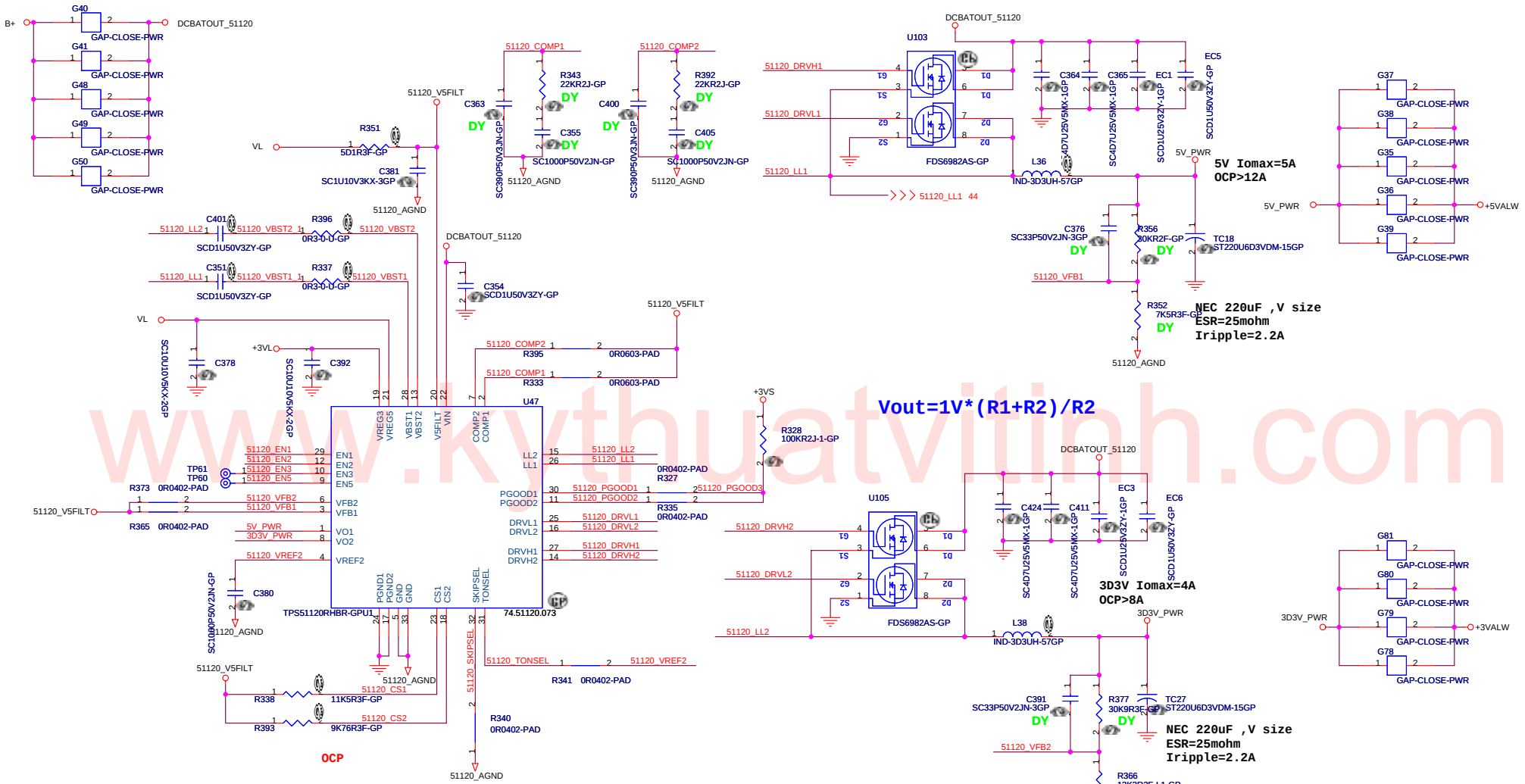


	GND	VREF2	FLOAT	V5FILT
SKIPSEL	**AUTOSKIP**	AUTOSKIP /FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	**D-Cap MODE**
TONSEL	380k/CH1 590k/CH2	290k/CH1 440k/CH2	**220k/CH1 330k/CH2**	180k/CH1 280k/CH2
VFB1	N/A	not use	ADJ.	**5V Fixed Output**
VFB2	N/A	not use	ADJ.	**3.3V Fixed Output**
EN1, EN2	Switcher OFF	not use	**Swithchr ON**	**Switcher ON**
EN3, EN5	LDO OFF	not use	**LDO ON**	VREG3 on

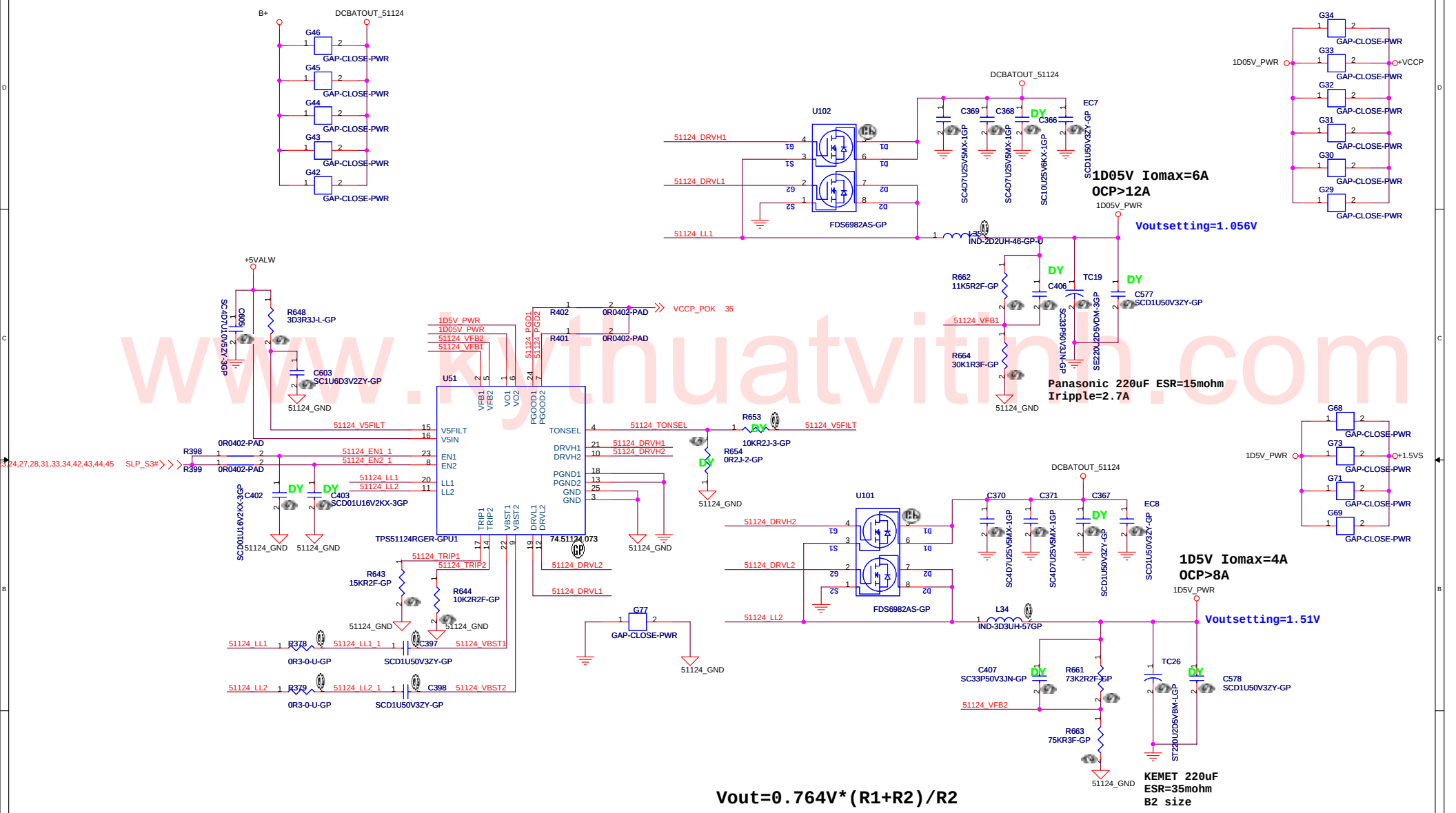
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51120_+3VALW/+5VALW

Size: A3 | Document Number: NORN | Rev: PV

Date: Friday, March 30, 2007 | Sheet 40 of 51



Vout=0.764V*(R1+R2)/R2

	GND	OPEN	V5FILT
TONSEL	230k/CH1 283k/CH2	283k/CH1 346k/CH2	346k/CH1 423k/CH2

Vtrip(mV)=Rtrip(Kohm)*10(uA)
Iocp=(Vtrip/Rdson)+((1/(2*L*f))*((Vin-Vout)*Vout)/Vin))

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51124_+1.05V_VCCP_+1.5VS

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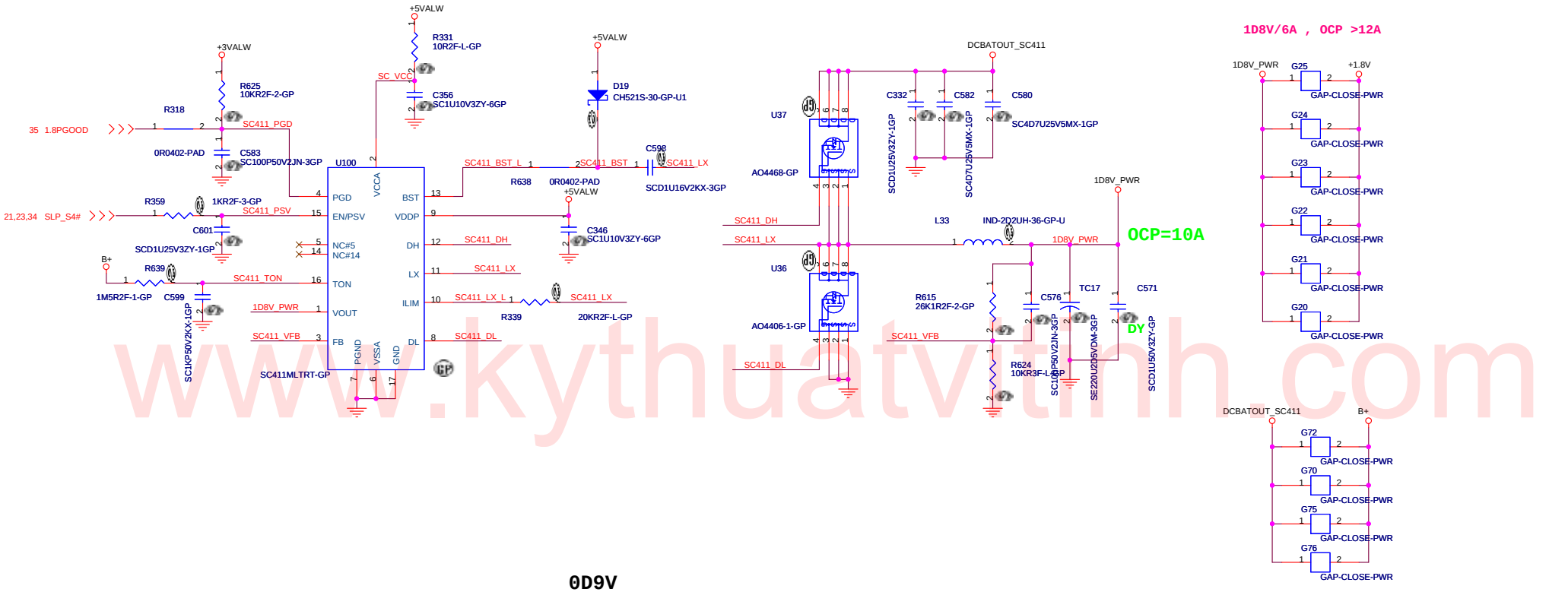
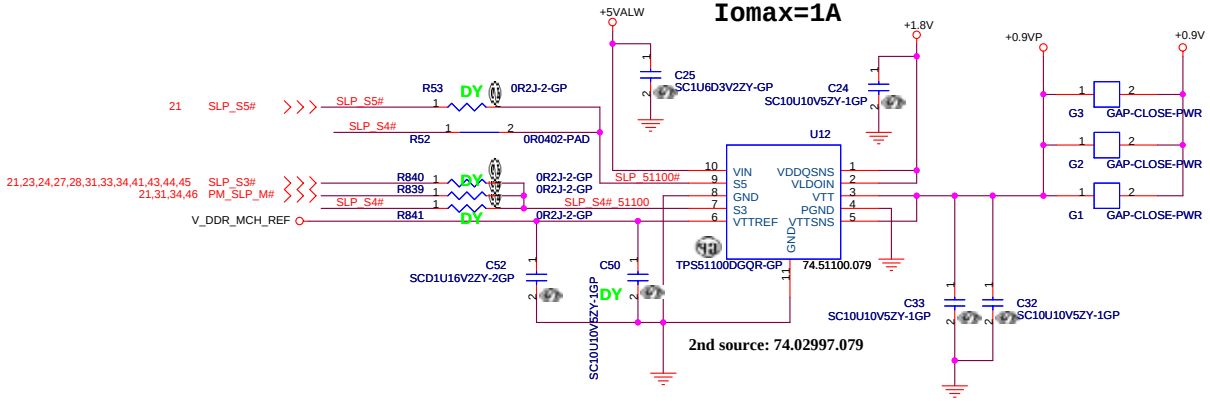
SC411 for 1D8V /TPS51110_0D9V





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SC 411 1D8V/0.9VP TPS51100

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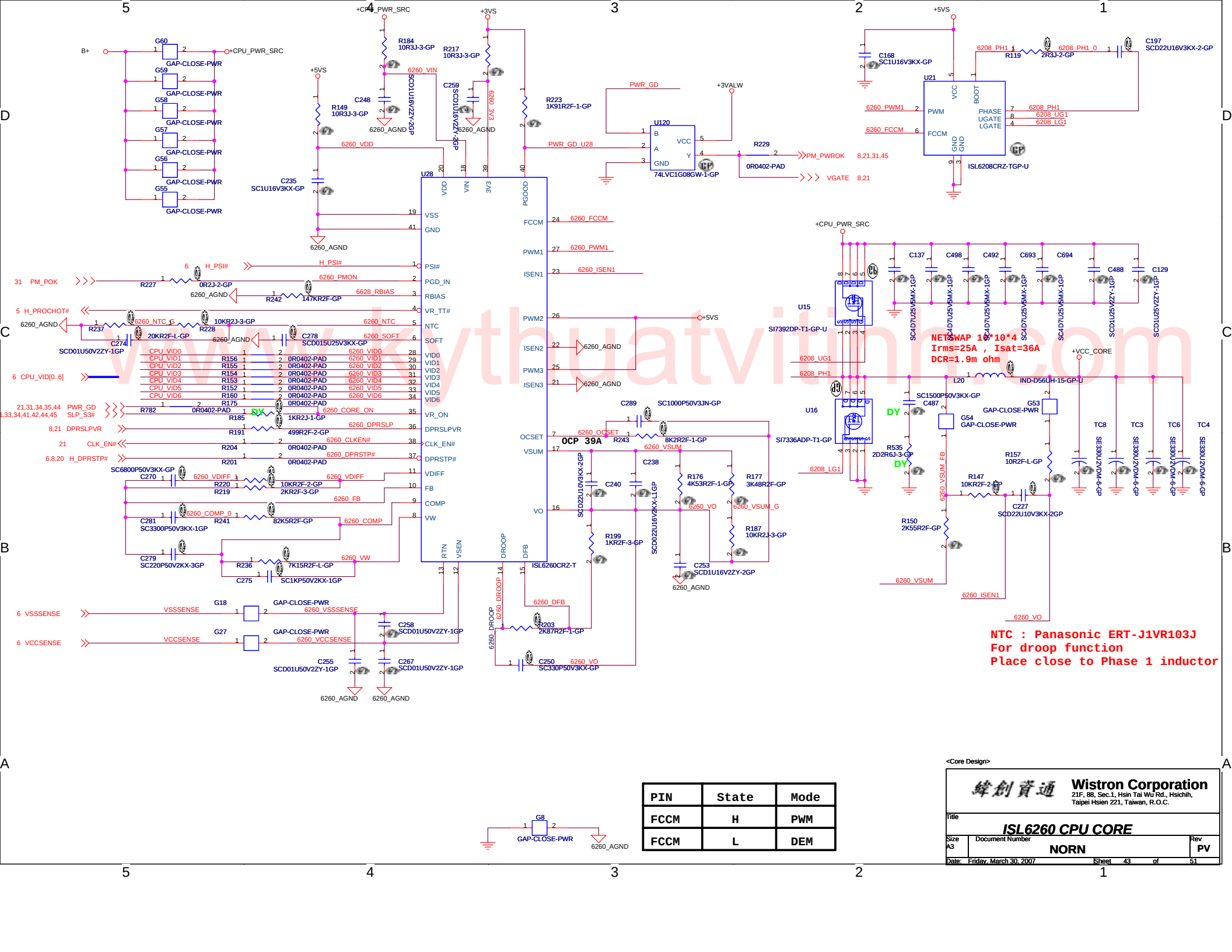
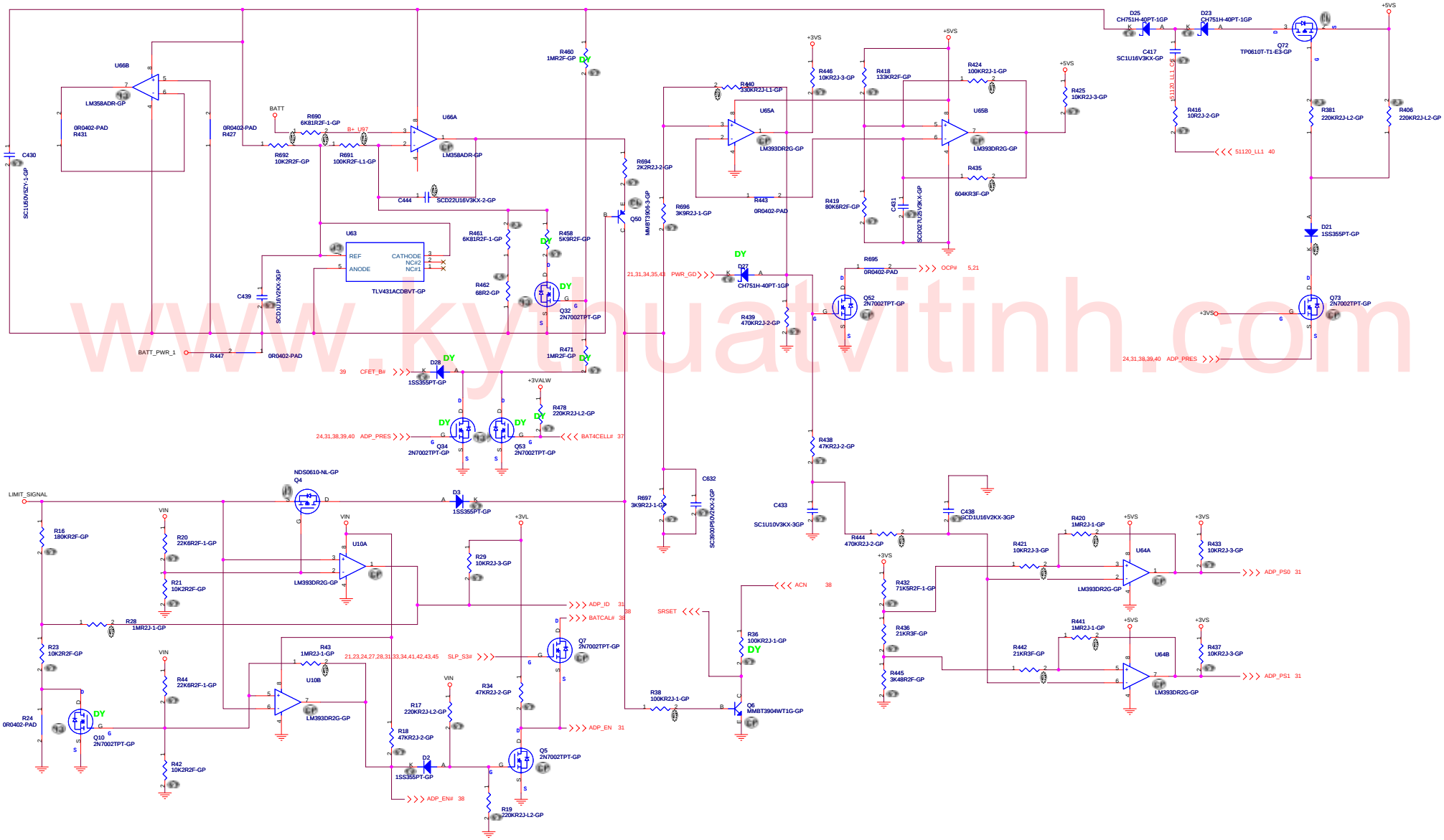


PIN	State	Mode
FCCM	H	PWM
FCCM	L	DEM



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ADP OCP

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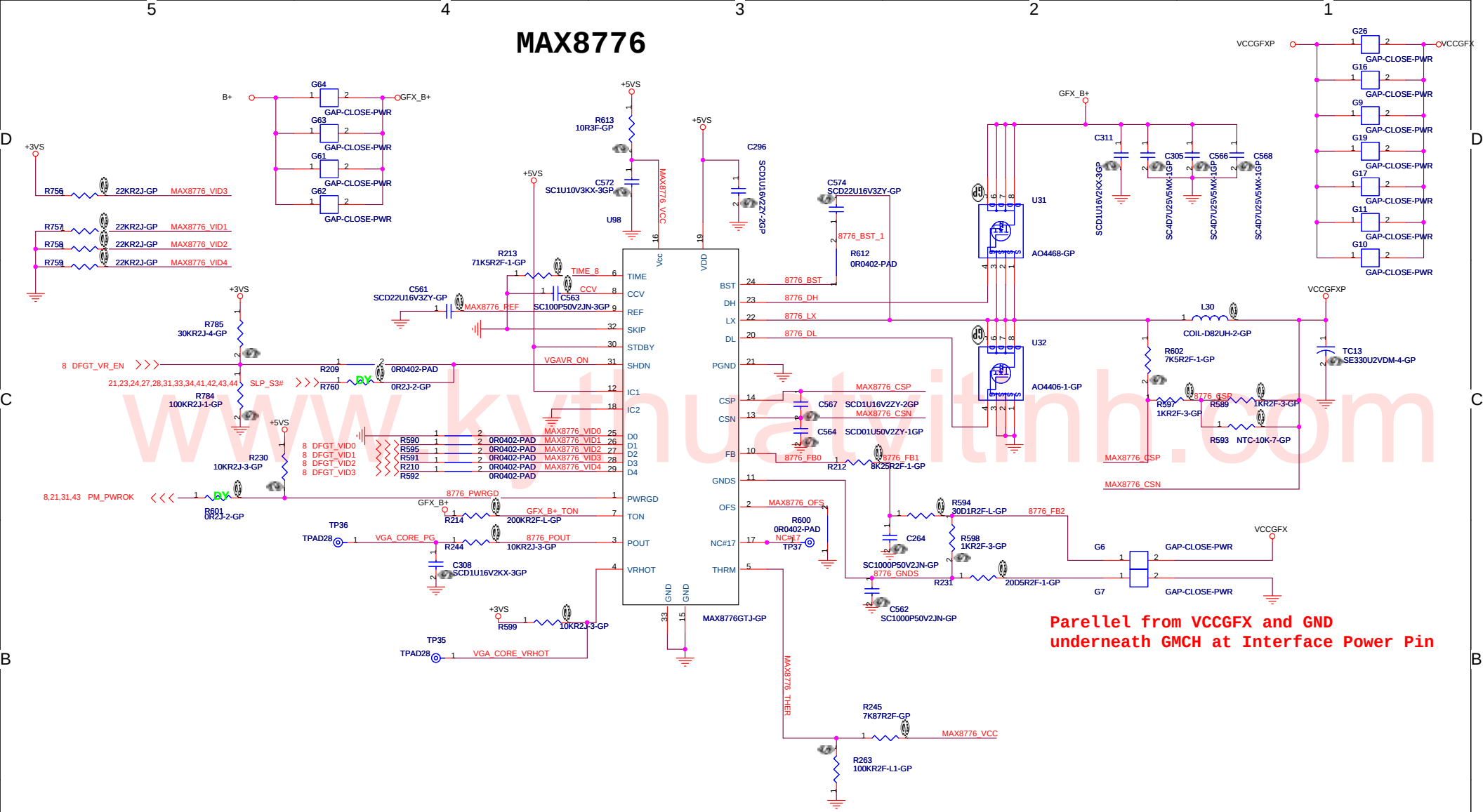
MAX8776



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MAX8776_VCCGFX

Size: A3 | Document Number: NORN | Rev: PV

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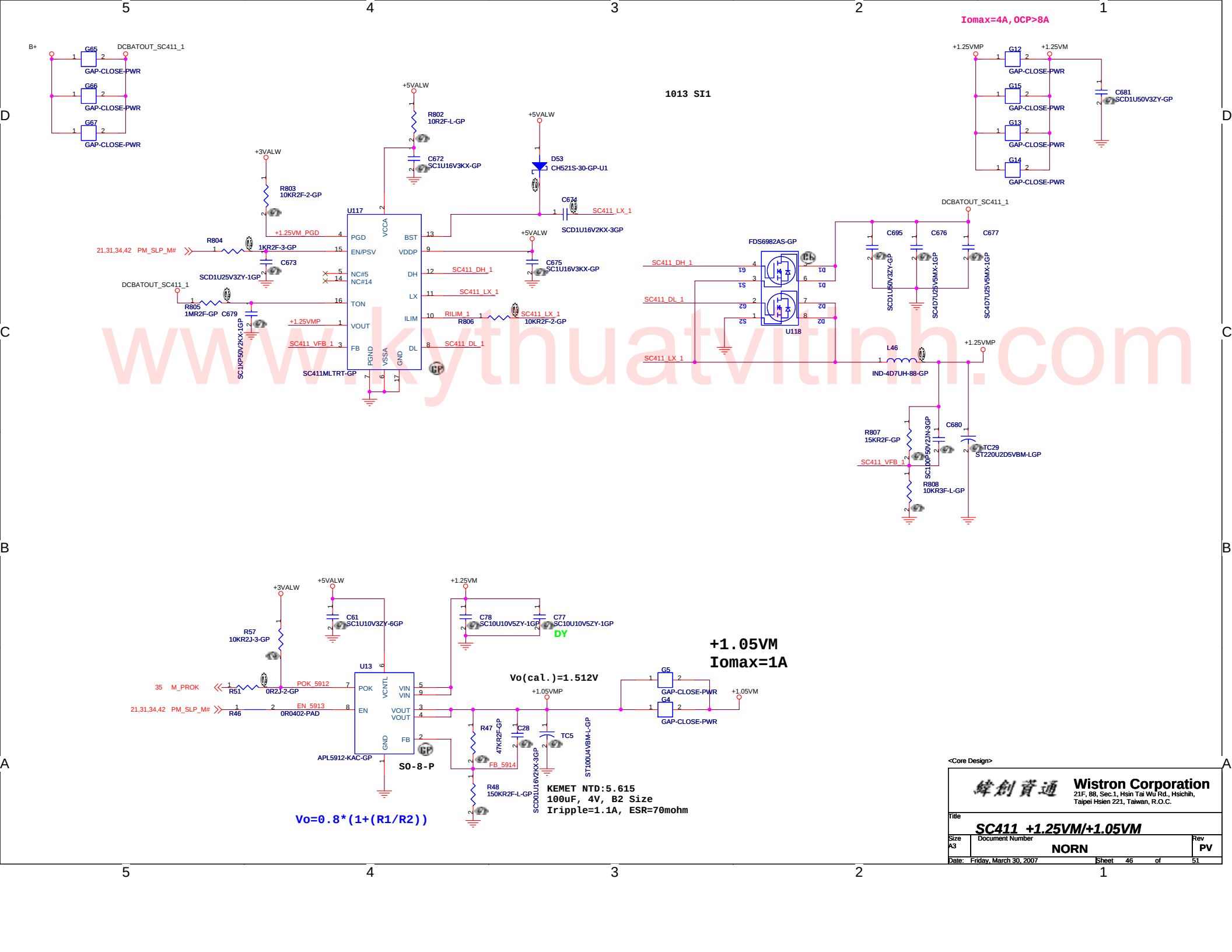

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SC411 +1.25VM/+1.05VM

Size	Document Number	Rev
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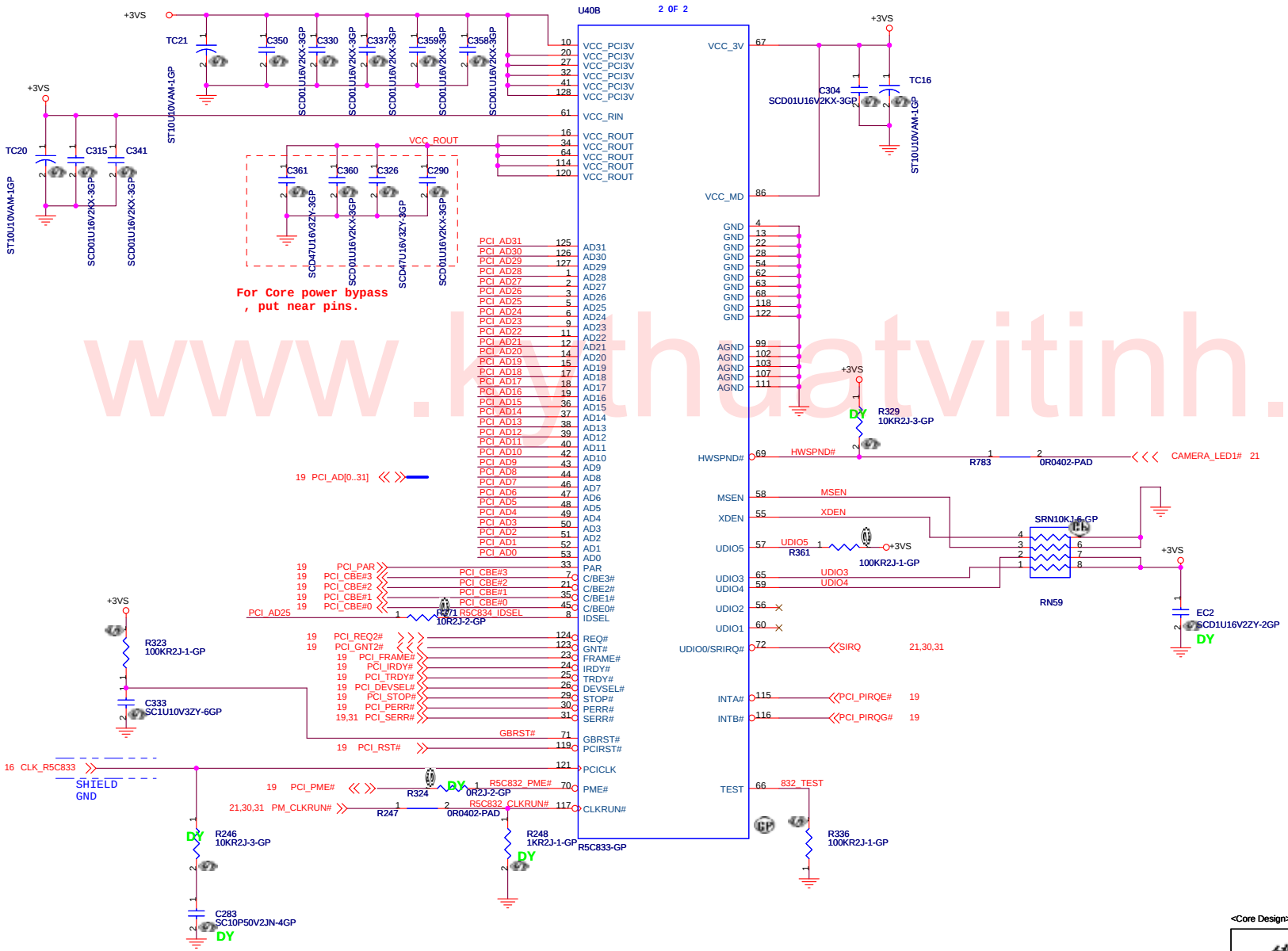

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: R5C833/PCI

Size	Document Number	Rev
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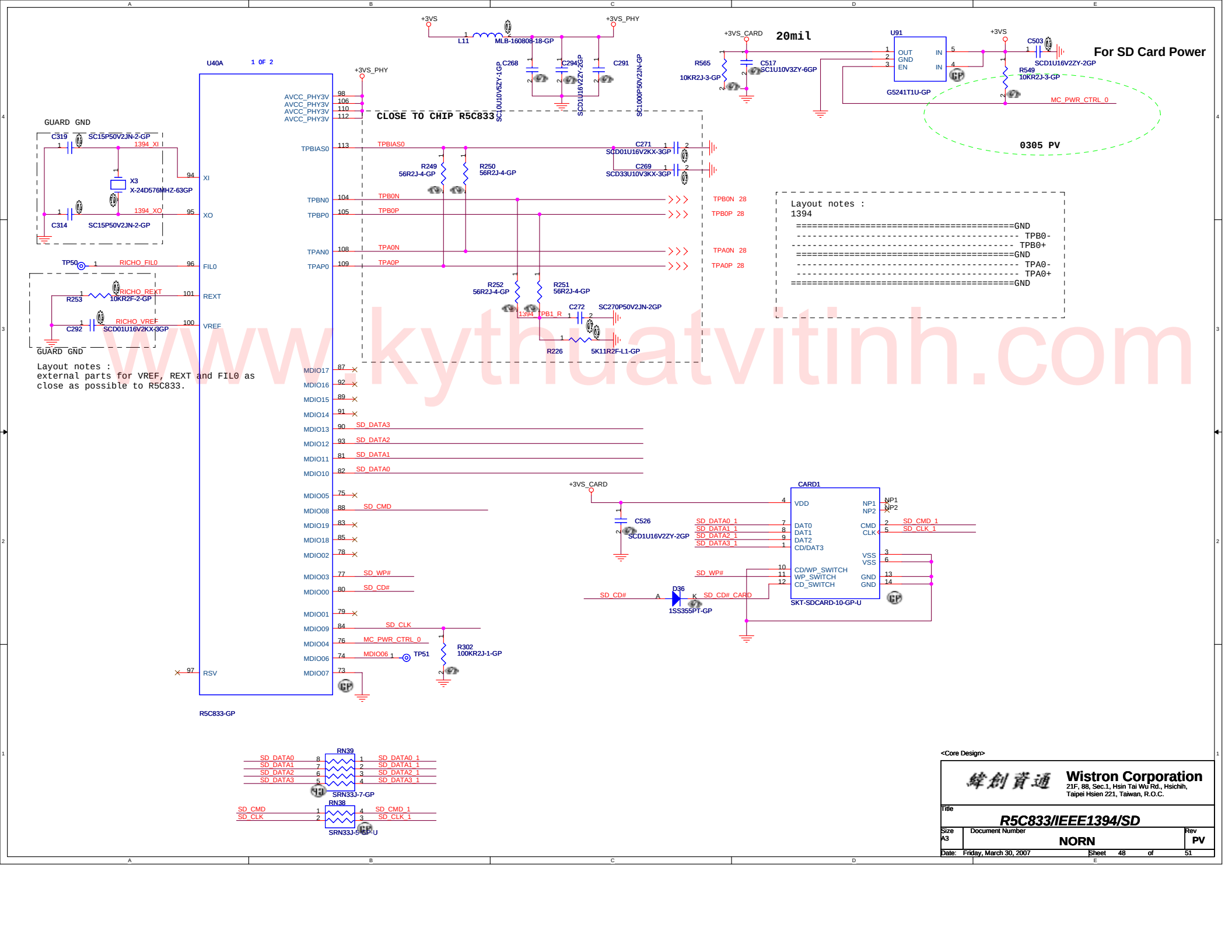

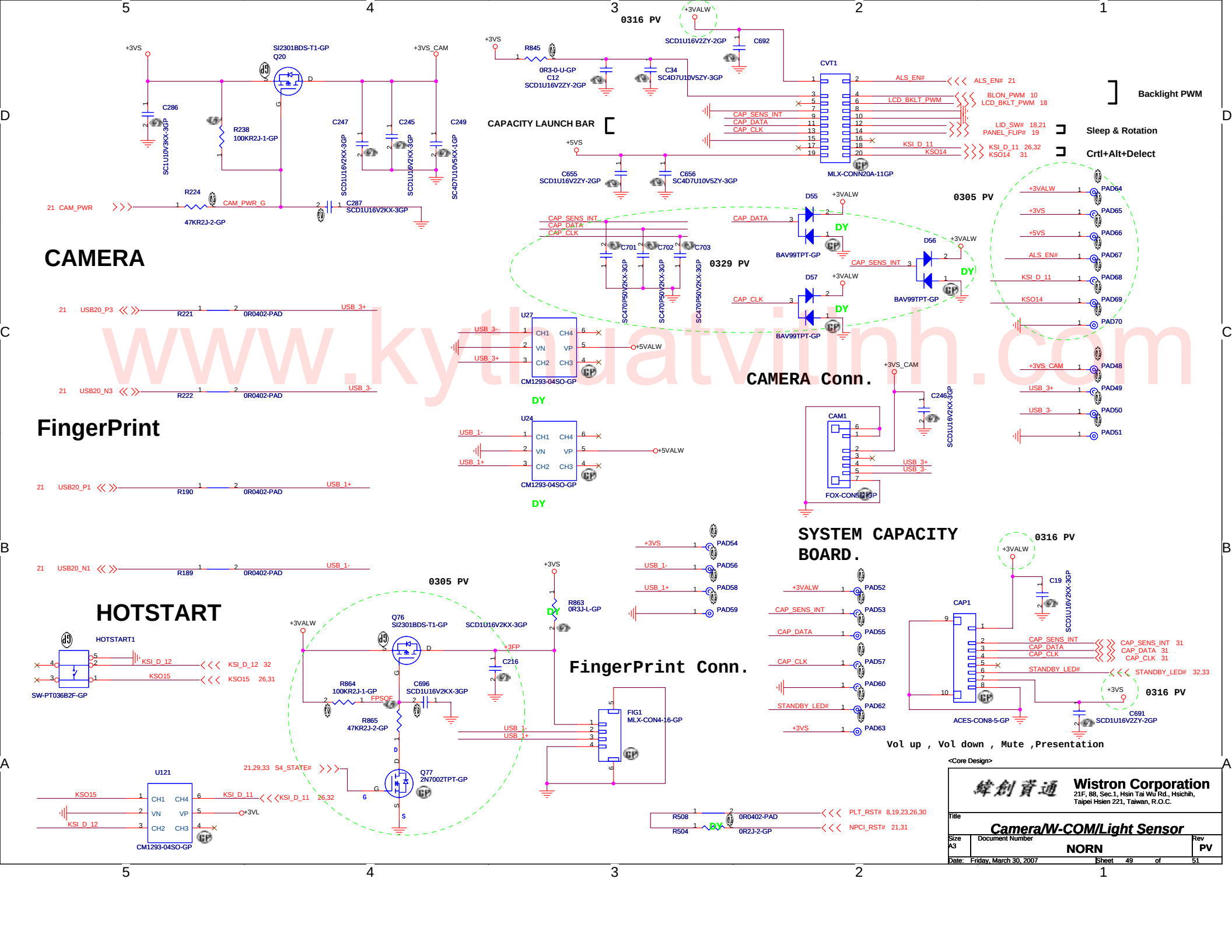
CAMERA
FingerPrint
HOTSTART
CAMERA Conn.
SYSTEM CAPACITY BOARD.
FingerPrint Conn.
CAPACITY LAUNCH BAR
Backlight PWM
Sleep & Rotation
Crtl+Alt+Delect
0316 PV
0305 PV
0329 PV
Vol up , Vol down , Mute ,Presentation
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Camera/W-COM/Light Sensor
NORN
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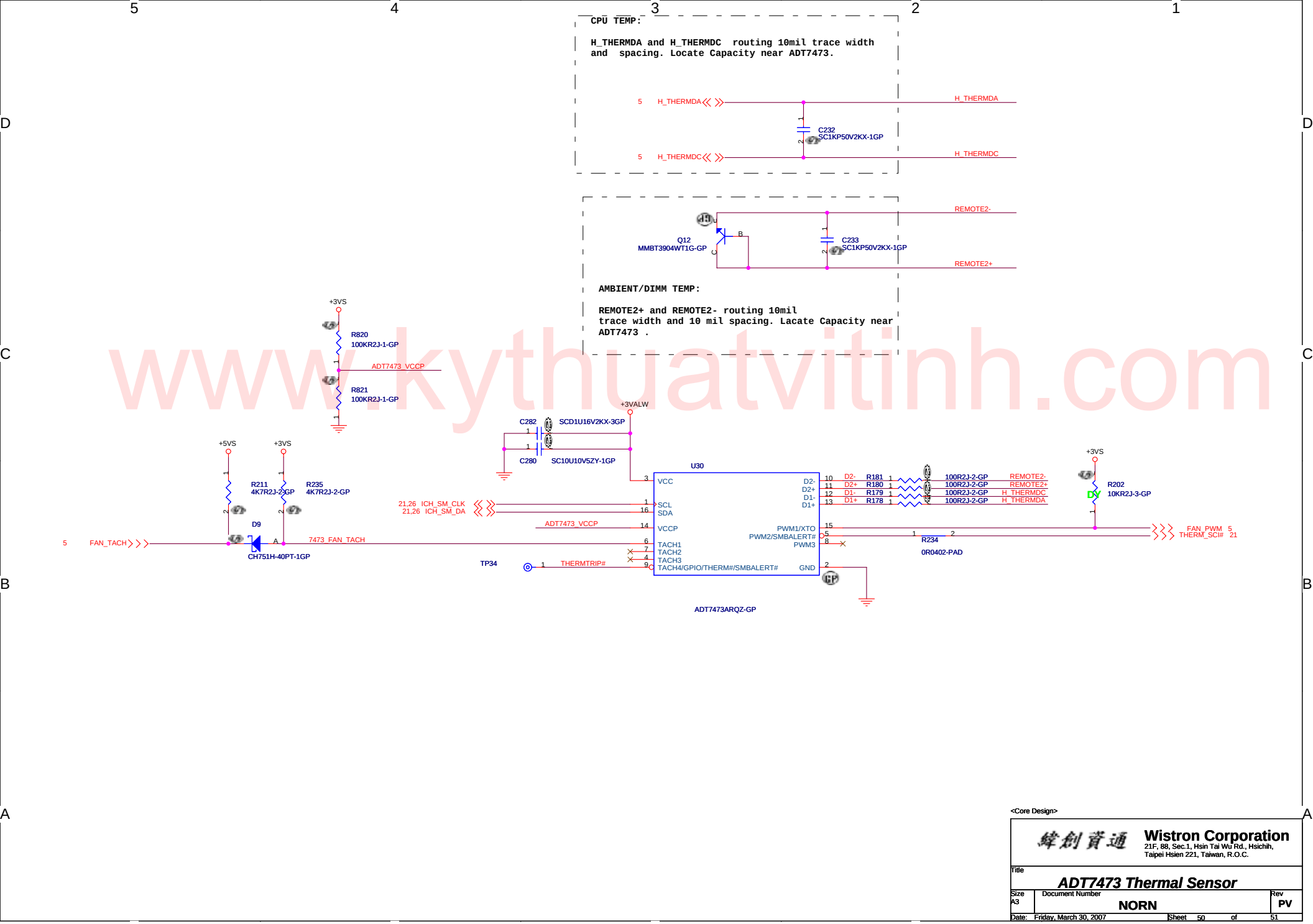

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ADT7473 Thermal Sensor

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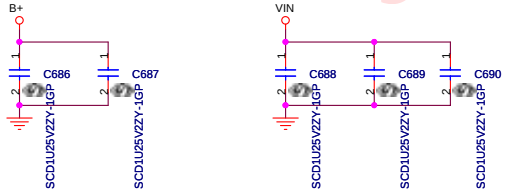
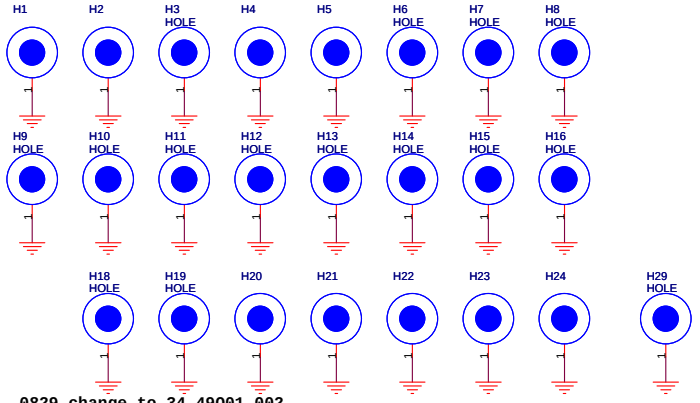
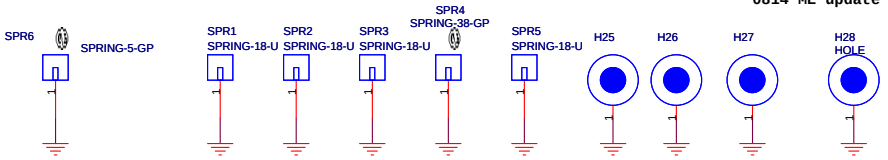
1101 HOLE H1,H2 change part to 34.4R836.001
1101 HOLE H4,H5 change part to 34.4R837.001
1101 HOLE H17 change part to 34.4R838.001
1101 HOLE H20,H21 change part to 34.4R841.001
1101 HOLE H22,H23,H24,H25 change part to 34.4R840.001
1101 HOLE H26,H27 change part to 34.4R839.001



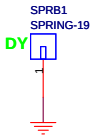


0829 change to 34.49Q01.002

0814 ME update drawing



1018 change SPR4 to 34.47R31.001



<Core Design>

蜂創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: UNUSED PARTS/EMI Capacitors

Size: A3 | Document Number: Norn | Rev: PV

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