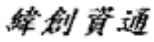


# Wistron Confidential

PV

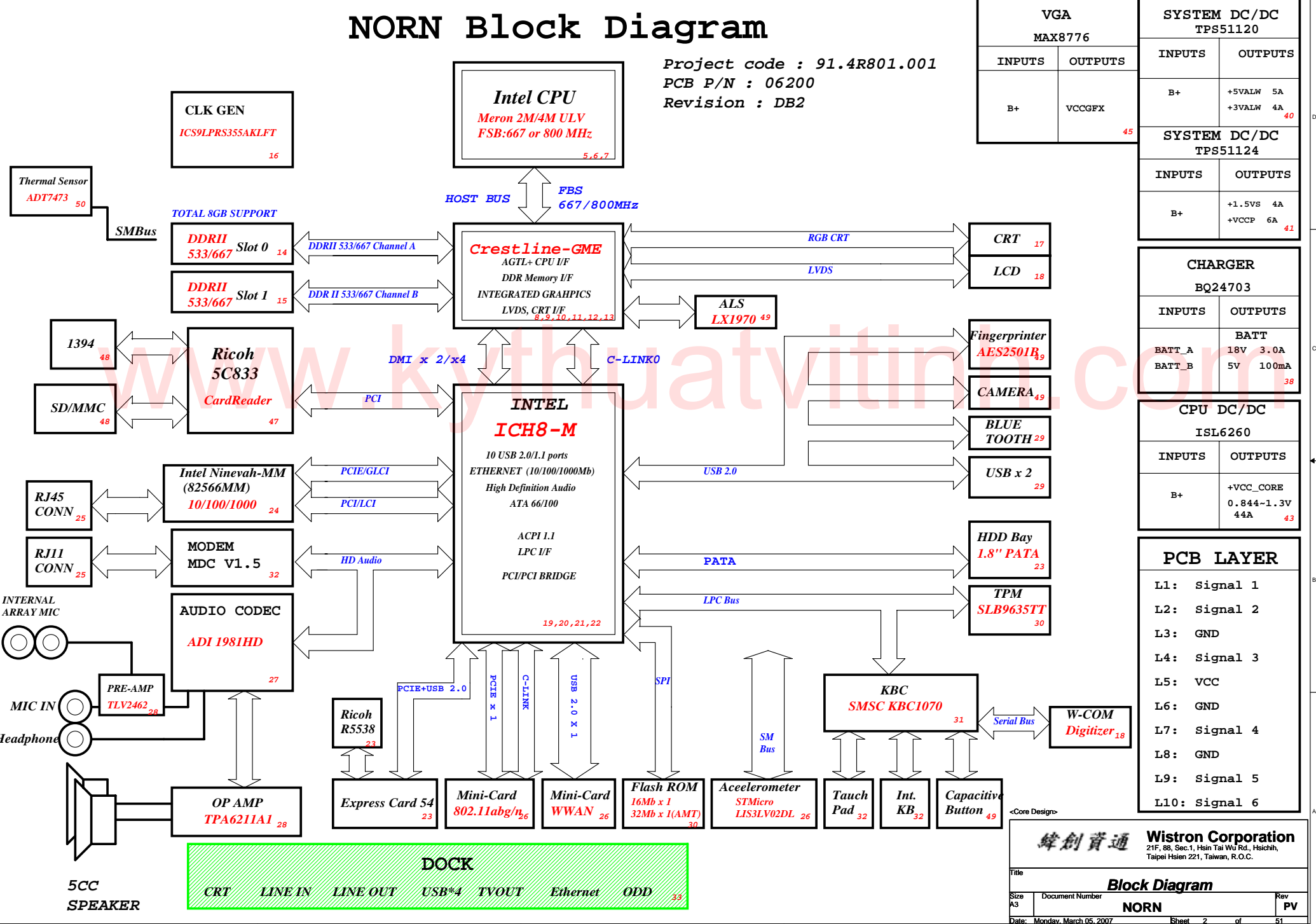
2007/03/30

REV : PV-04

<Variant Name>			
		<b>Wistron Corporation</b> 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>NORN</b>			
Size	Document Number	Rev	
A3	<b>NORN</b>	<b>PV</b>	
Date: Friday, March 30, 2007		Sheet 1	of 51

# NORN Block Diagram

Project code : 91.4R801.001  
 PCB P/N : 06200  
 Revision : DB2



VGA MAX8776	
INPUTS	OUTPUTS
B+	VCCGFX

SYSTEM DC/DC TPS51120	
INPUTS	OUTPUTS
B+	+5VALW 5A +3VALW 4A

SYSTEM DC/DC TPS51124	
INPUTS	OUTPUTS
B+	+1.5VS 4A +VCCP 6A

CHARGER BQ24703	
INPUTS	OUTPUTS
BATT	BATT
BATT_A	1.8V 3.0A
BATT_B	5V 100mA

CPU DC/DC ISL6260	
INPUTS	OUTPUTS
B+	+VCC_CORE 0.844-1.3V 44A

PCB LAYER	
L1:	Signal 1
L2:	Signal 2
L3:	GND
L4:	Signal 3
L5:	VCC
L6:	GND
L7:	Signal 4
L8:	GND
L9:	Signal 5
L10:	Signal 6

<Core Design>

**緯創資通 Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

Title	<b>Block Diagram</b>	
Size A3	Document Number	Rev PV
Date: Monday, March 05, 2007	<b>NORN</b>	

Sheet 2 of 51

www.kythuatvithinh.com

緯創資通		<b>Wistron Corporation</b>	
		21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>Change Notes List</b>			
Size	Document Number	Rev	
A3	<b>NORN</b>	<b>PV</b>	
Date:	Monday, March 05, 2007	Sheet 3	of 51

**Voltage Rails**

o MEANS ON x MEANS OFF

power plane \ State	+BB LDO3 LDO5	+5VALW +5VALW	+1.8V  +0.9V	+5VS +3VS  +1.8VS +1.5VS +1.25VS +VGA_CORE +CPU_CORE +VCCP	+3VM +1.05VM  +1.25VM	CLOCK
S0	O	O	O	O	O	O
S3/M1	O	O	O	X	O	O
S3	O	O	O	X	O	O
S5 S4/AC	O	O	X	X	O	O
S5 S4/Battery only	O	X	X	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X	X	X

**PCI Devices**

EXTERNAL	IDSEL#	REQ/GNT#	PIRQ
Cardreader & 1394	AD22	2	G, E

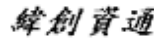
DMA Channel	Device
DMA0	Modem/LAN
DMA1	ECP
DMA2	<del>Floppy Disk</del>
DMA3	Audio
DMA4	(Cascade)
DMA5	Unused
DMA6	Unused
DMA7	Unused

USB PORT#	Destination
0	FREE
1	Fingerprint
2	EXPRESS SLOT
3	Camera
4	Walk-up1 (Right Side)
5	Walk-up2 (Left Side)
6	Bluetooth
7	Dock 1
8	WWAN
9	Dock 2

Symbols	Description
DY/DUMMY	No install
1KR2J	Resistor 1K ohm ,Size 0402 ,5%
1KR3F	Resistor 1K ohm ,Size 0603 ,1%
GP	ROHS parts
NC	Pin no connect to anything

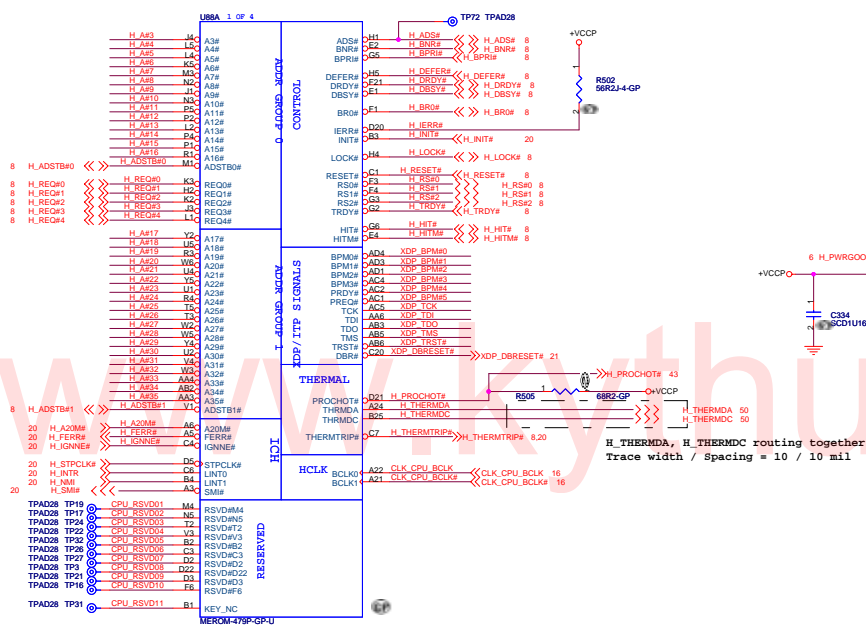
IRQ	Device
0	System Timer
1	Keyboard
2	N/A
3	Serial port (COM2) ,LAN/Modem
4	Serial port (COM1)
5	Audio/VGA
6	<del>Floppy</del>
7	Parallel port
8	System CMOS/Real-time clock
9	Microsoft ACPI
10	N/A,Modem,LAN
11	Mass storage control/PCI simple communication control
12	synactic PS2 port GlidePAD
13	Numeric Data Process
14	Primary IDE interface ,HDD
15	Secondary IDE interface ,CD-ROM
16	Mobile Intel Crestline Express Chipset Family Microsoft UAA Bus Drive for High Definition Audio Intel 82801H (ICH8 Family) PCI Express Root Port -27D0 Broadcom NetXtreme Gigabit Ethernet
17	Intel 82801H (ICH8 Family) PCI Express Root Port -27D2 Broadcom 802.11b/g WLAN Intel 82801H (ICH8 Family) USB Universal Host Control
18	Intel 82801H (ICH8 Family) USB Universal Host Control  Richo R5C853 Integrates FlashMedia Control Richo R5C853 Gemcore based SmartCard Control
19	Intel 82801H (ICH8 Family) PCI Express Root Port -27D6 Intel 82801H (ICH8 Family) USB Universal Host Control
20	Intel 82801H (ICH8 Family) USB Universal Host Control Intel 82801H (ICH8 Family) USB2 Enhanced Host Control
21	Intel 82801H (ICH8 Family) USB Universal Host Control
22	SDA Standard Compliant SD Host Control
23	HP Mobile Data Protection Sensor

<Variant Name>

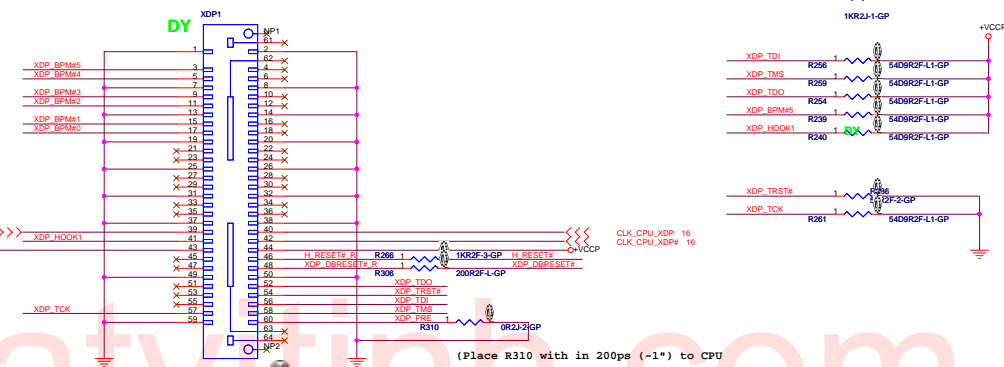
 <b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
<b>Notes List</b>		
Title		
Size A3	Document Number	Rev
	<b>NORN</b>	<b>PV</b>
Date: Friday, March 23, 2007	Sheet 4	of 51

8 H\_AD[3..35] <<< <<<

layout note : Change R305 to 649 ohm if using XTP to ITP adapter

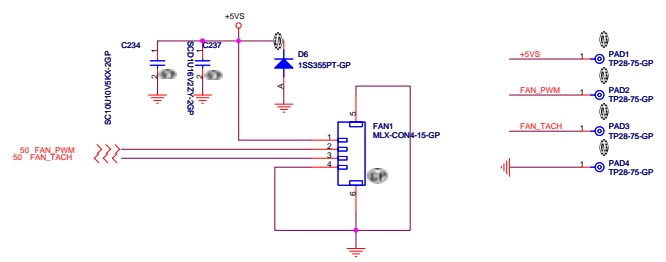
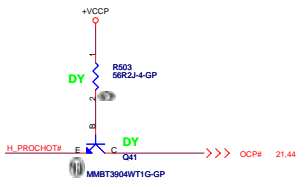


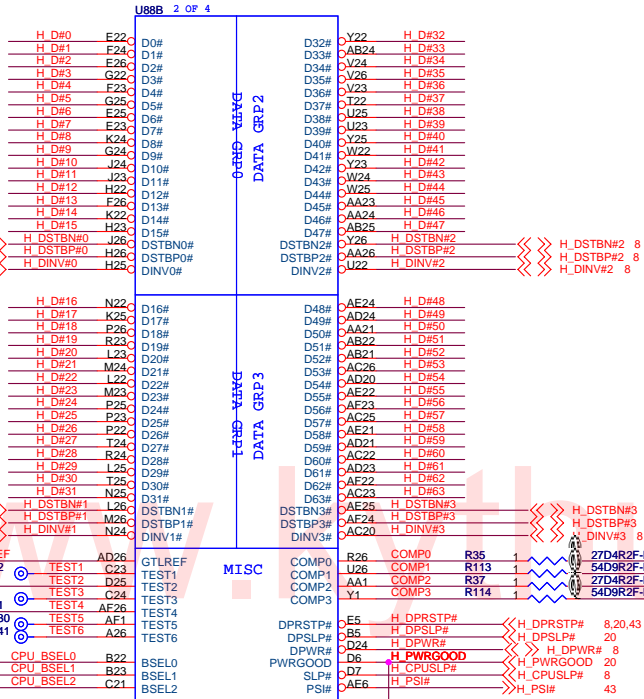
### XDP Connector



0630 Connector Vendor : SmaTec  
Part Number : QSH-030-01-F-D-TR

### 4 WIRE PWM Fan Control circuit



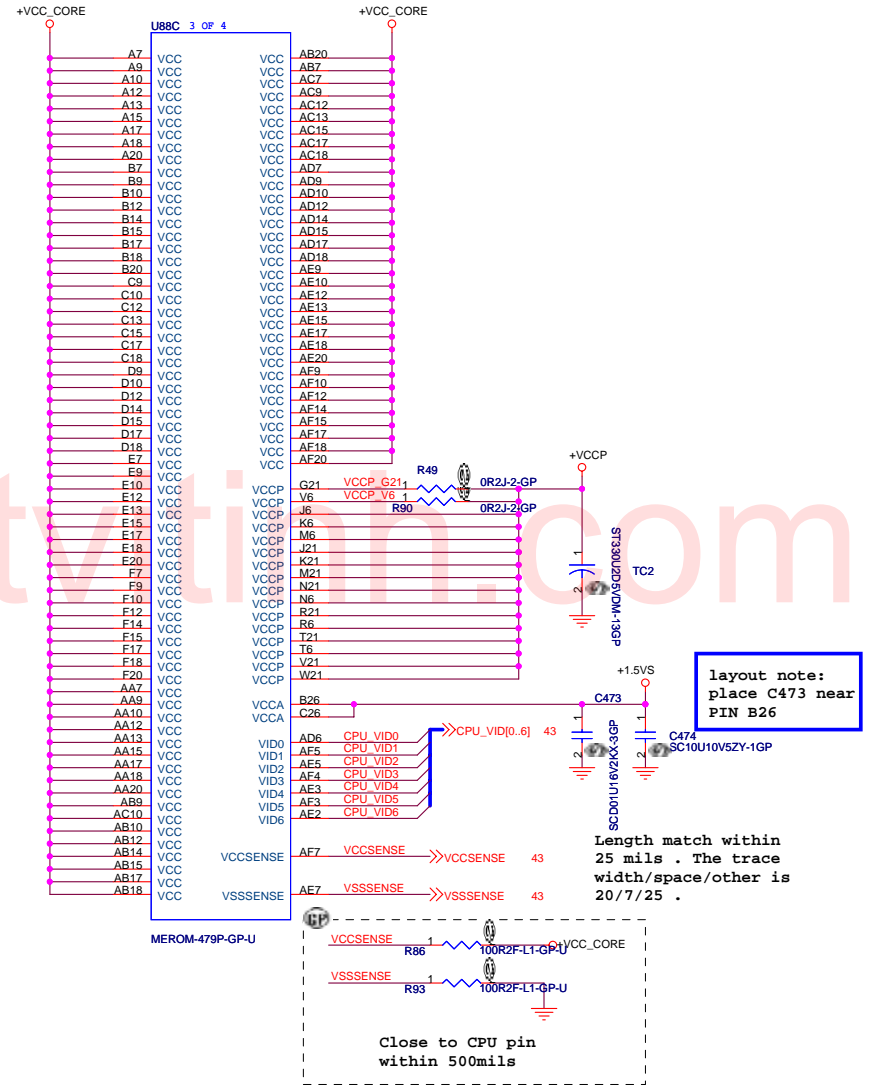


PLACE C470 close to the TEST4 PIN, make sure TEST3,TEST4,TEST5 trace routing is reference to GND and away other noisy signals

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

Resistor Placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal . COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils .

Close to CPU pin AD26  
pin AD26  
Z0=55 ohm  
with in 500mils .



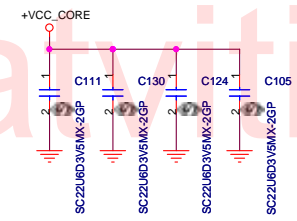
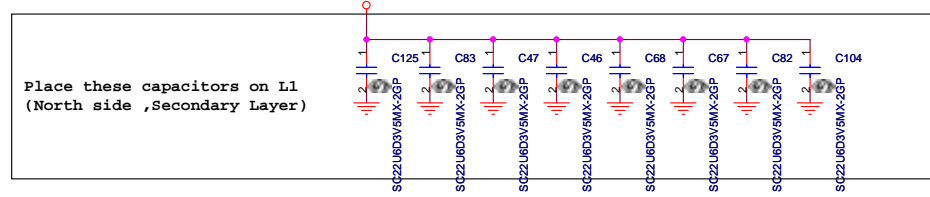
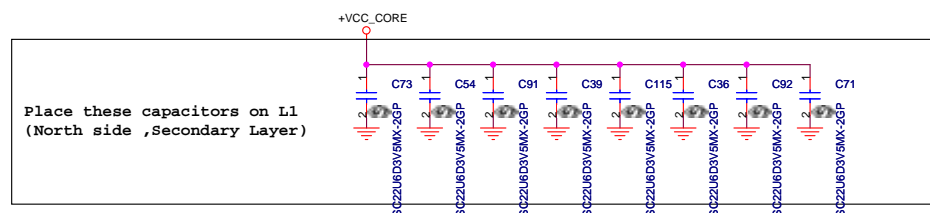
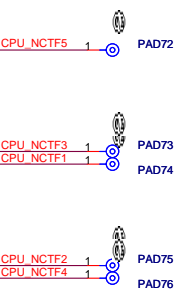
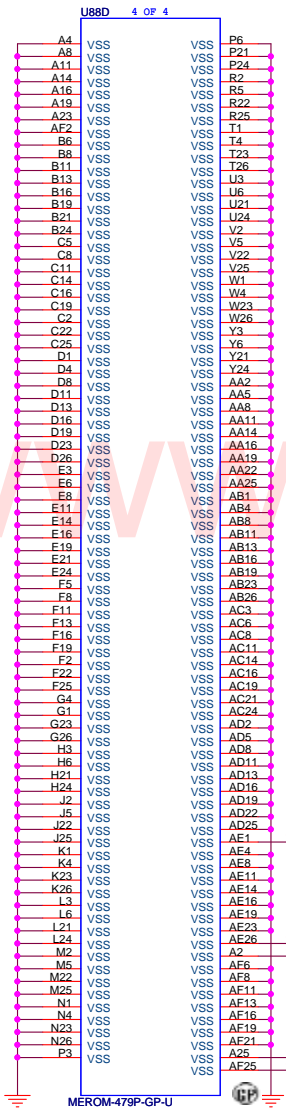
<Core Design>

**緯創資通 Wistron Corporation**  
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichin, Taipei Hsein 221, Taiwan, R.O.C.

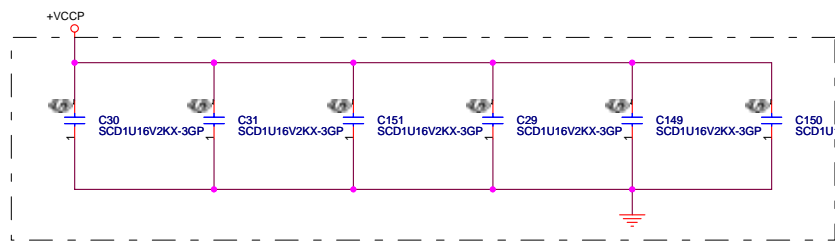
Title: **Meron(2/3)-AGTL+/PWR**

Size A3 Document Number **NORN** Rev **PV**

Date: Friday, March 30, 2007 Sheet 6 of 51

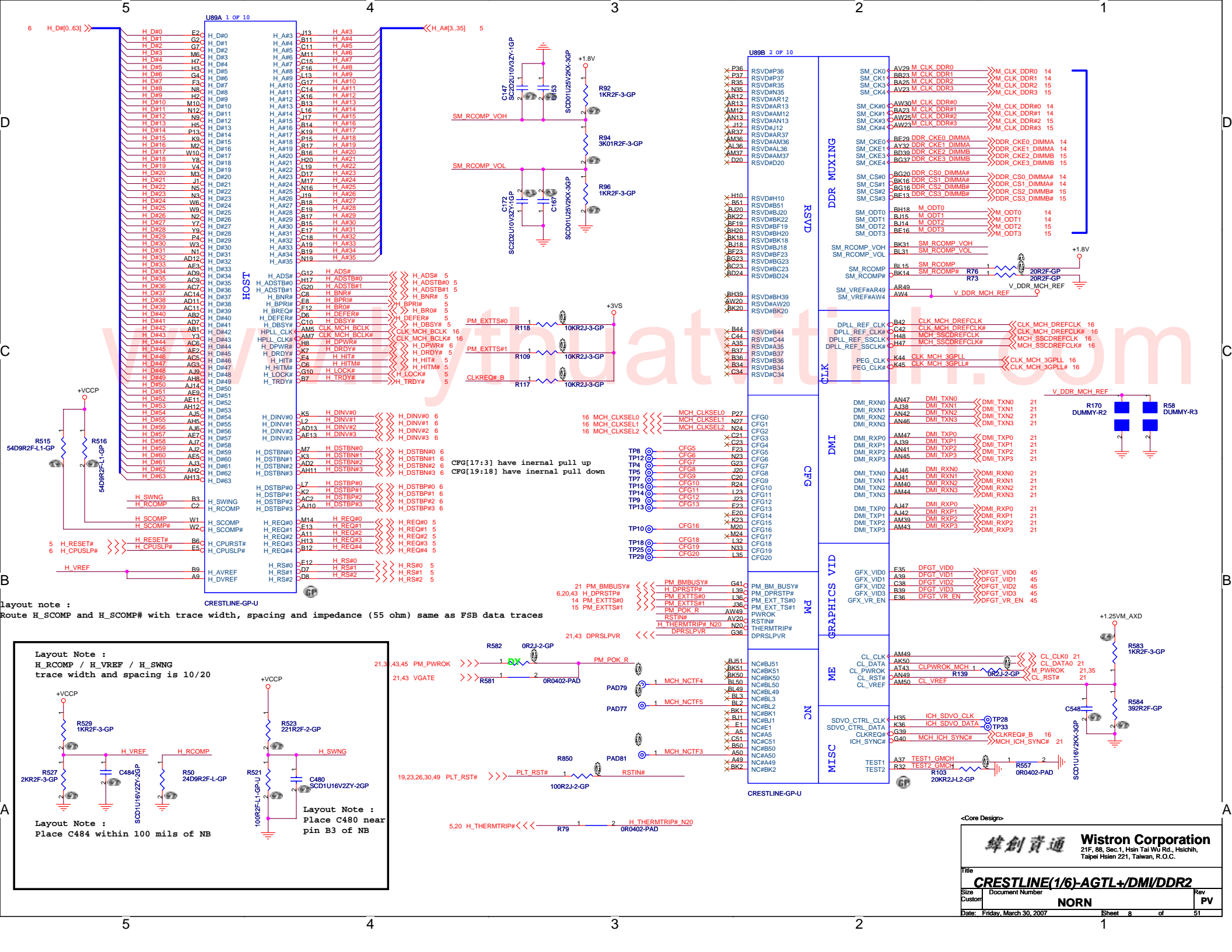


Mid Frequncd Decoupling



<Core Design>

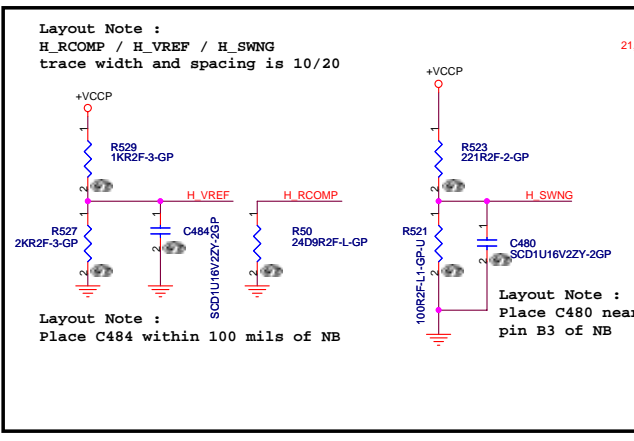
		<b>Wistron Corporation</b> 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.
Title		
<b>Meron(3/3)-GND&amp;Bypass</b>		
Size A3	Document Number	Rev PV
Date: Tuesday, March 27, 2007		Sheet 7 of 51



U89A 1 OF 10

HOST		HOST	
H_D#0	E2	H_A#3	J13
H_D#1	G2	H_A#4	C811
H_D#2	G2	H_A#5	C11
H_D#3	M6	H_A#6	M11
H_D#4	H7	H_A#7	C15
H_D#5	H6	H_A#8	L13
H_D#6	H3	H_A#9	G17
H_D#7	F4	H_A#10	C14
H_D#8	N8	H_A#11	K16
H_D#9	H2	H_A#12	B16
H_D#10	H10	H_A#13	L16
H_D#11	H10	H_A#14	J17
H_D#12	N9	H_A#15	B14
H_D#13	H5	H_A#16	K19
H_D#14	H5	H_A#17	R17
H_D#15	K13	H_A#18	B20
H_D#16	M6	H_A#19	L19
H_D#17	W10	H_A#20	H20
H_D#18	Y8	H_A#21	C18
H_D#19	Y8	H_A#22	L19
H_D#20	M3	H_A#23	D17
H_D#21	J1	H_A#24	M17
H_D#22	N8	H_A#25	N16
H_D#23	N8	H_A#26	J10
H_D#24	W6	H_A#27	E19
H_D#25	W9	H_A#28	B17
H_D#26	W9	H_A#29	B15
H_D#27	Y8	H_A#30	E17
H_D#28	Y9	H_A#31	C18
H_D#29	P4	H_A#32	A19
H_D#30	W3	H_A#33	B19
H_D#31	W3	H_A#34	Q13
H_D#32	AD12	H_A#35	N19
H_D#33	AE3	H_ADS#	AG12
H_D#34	AD9	H_ADSTB#0	AG17
H_D#35	AC7	H_ADSTB#1	G20
H_D#36	AC7	H_ADSTB#2	G20
H_D#37	AC14	H_BNR#	C8
H_D#38	AD11	H_BPR#	E8
H_D#39	AC11	H_BRR#	F12
H_D#40	AD7	H_DEFER#	D6
H_D#41	AD7	H_DBSY#	C10
H_D#42	AB1	H_AM5 CLK MCH BCLK	AM5
H_D#43	YS	H_DPWR#	AM7
H_D#44	YS	H_DPWR#	K8
H_D#45	AE2	H_DRDY#	C7
H_D#46	AC6	H_HIT#	E4
H_D#47	AGC	H_HITM#	C6
H_D#48	AGC	H_HITM#	G10
H_D#49	AH8	H_LOCK#	H10
H_D#50	A114	H_TRDY#	B7
H_D#51	AE3	H_DIN#0	K5
H_D#52	AE11	H_DIN#1	G2
H_D#53	AH12	H_DIN#2	AD13
H_D#54	AJ6	H_DIN#3	AE13
H_D#55	AH6	H_DSTBN#0	M7
H_D#56	AH6	H_DSTBN#1	K3
H_D#57	AJ2	H_DSTBN#2	AD2
H_D#58	AJ7	H_DSTBN#3	AH11
H_D#59	AE1	H_DSTBP#0	L7
H_D#60	AE1	H_DSTBP#1	K2
H_D#61	AJ3	H_DSTBP#2	AC2
H_D#62	AH2	H_DSTBP#3	AJ10
H_D#63	AH13	H_REQ#0	M14
H_D#64	AJ2	H_REQ#1	E13
H_D#65	AH3	H_REQ#2	A11
H_D#66	AJ3	H_REQ#3	H13
H_D#67	AH2	H_REQ#4	B12
H_D#68	AH13	H_RS#0	E12
H_D#69	AH13	H_RS#1	D18
H_D#70	AH13	H_RS#2	D18

Layout note:  
Route H\_SCOMP and H\_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces



U89B 2 OF 10

R527	2KR2F-3-GP	H_VREF
R529	1KR2F-3-GP	H_VREF
R50	24D9R2F-L-GP	H_RCOMP
R521	100R2F-L1-GP-U	H_SWNG
R523	221R2F-2-GP	H_SWNG
C480	SCD1U16V2ZY-2GP	
C484		

Signal	Pin	Value
PM_PWOK	1	21.3
VGATE	1	21.43
DPRSPLVR	1	21.43
PLT_RST#	1	19,23,26,30,49
H_THERMTRIP# N20	1	5.20

Signal	Pin	Value
MCH_CLKSEL0	1	16 MCH_CLKSEL0
MCH_CLKSEL1	1	16 MCH_CLKSEL1
MCH_CLKSEL2	1	16 MCH_CLKSEL2

Signal	Pin	Value
PM_BMBUSY#	1	G41
H DPRSTP#	1	L39
PM_EXTTS#0	1	L37
PM_POK_R	1	J36
RSTIN#	1	AV20
H_THERMTRIP# N20	1	N20
DPRSPLVR	1	G36

Signal	Pin	Value
NC#BJ51	1	BJ51
NC#BK51	1	BK51
NC#BK50	1	BK50
NC#BL50	1	BL50
NC#BL49	1	BL49
NC#BL2	1	BL2
NC#BK1	1	BK1
NC#BJ1	1	BJ1
NC#A5	1	A5
NC#C51	1	C51
NC#A50	1	A50
NC#A49	1	A49
NC#BK2	1	BK2

Signal	Pin	Value
RSVD#P36	1	P36
RSVD#P37	1	P37
RSVD#R35	1	R35
RSVD#M35	1	M35
RSVD#AR12	1	AR12
RSVD#AR13	1	AR13
RSVD#AM12	1	AM12
RSVD#AM13	1	AM13
RSVD#J12	1	J12
RSVD#AR37	1	AR37
RSVD#AM36	1	AM36
RSVD#AM37	1	AM37
RSVD#D20	1	D20
RSVD#H10	1	H10
RSVD#BJ20	1	BJ20
RSVD#BK22	1	BK22
RSVD#BF19	1	BF19
RSVD#BK20	1	BK20
RSVD#BK18	1	BK18
RSVD#BJ18	1	BJ18
RSVD#BF23	1	BF23
RSVD#BG23	1	BG23
RSVD#BC23	1	BC23
RSVD#BD24	1	BD24
RSVD#BH39	1	BH39
RSVD#AW20	1	AW20
RSVD#BK20	1	BK20
RSVD#B44	1	B44
RSVD#C44	1	C44
RSVD#A35	1	A35
RSVD#B37	1	B37
RSVD#B36	1	B36
RSVD#B34	1	B34
RSVD#C34	1	C34
CFG0	1	CFG0
CFG1	1	CFG1
CFG2	1	CFG2
CFG3	1	CFG3
CFG4	1	CFG4
CFG5	1	CFG5
CFG6	1	CFG6
CFG7	1	CFG7
CFG8	1	CFG8
CFG9	1	CFG9
CFG10	1	CFG10
CFG11	1	CFG11
CFG12	1	CFG12
CFG13	1	CFG13
CFG14	1	CFG14
CFG15	1	CFG15
CFG16	1	CFG16
CFG17	1	CFG17
CFG18	1	CFG18
CFG19	1	CFG19
CFG20	1	CFG20
PM_BM_BUSY#	1	PM_BM_BUSY#
PM_DPRSTP#	1	PM_DPRSTP#
PM_EXT_TS#0	1	PM_EXT_TS#0
PM_EXT_TS#1	1	PM_EXT_TS#1
PM_POK_R	1	PM_POK_R
RSTIN#	1	RSTIN#
H_THERMTRIP# N20	1	H_THERMTRIP# N20
DPRSPLVR	1	DPRSPLVR
NC#BJ51	1	NC#BJ51
NC#BK51	1	NC#BK51
NC#BK50	1	NC#BK50
NC#BL50	1	NC#BL50
NC#BL49	1	NC#BL49
NC#BL2	1	NC#BL2
NC#BK1	1	NC#BK1
NC#BJ1	1	NC#BJ1
NC#A5	1	NC#A5
NC#C51	1	NC#C51
NC#A50	1	NC#A50
NC#A49	1	NC#A49
NC#BK2	1	NC#BK2
SM_CK0	1	SM_CK0
SM_CK1	1	SM_CK1
SM_CK3	1	SM_CK3
SM_CK4	1	SM_CK4
SM_CK90	1	SM_CK90
SM_CK91	1	SM_CK91
SM_CK93	1	SM_CK93
SM_CK94	1	SM_CK94
SM_CKE0	1	SM_CKE0
SM_CKE1	1	SM_CKE1
SM_CKE3	1	SM_CKE3
SM_CKE4	1	SM_CKE4
SM_CS0	1	SM_CS0
SM_CS1	1	SM_CS1
SM_CS2	1	SM_CS2
SM_CS3	1	SM_CS3
SM_ODT0	1	SM_ODT0
SM_ODT1	1	SM_ODT1
SM_ODT2	1	SM_ODT2
SM_ODT3	1	SM_ODT3
SM_RCMP#_V0H	1	SM_RCMP#_V0H
SM_RCMP#_VOL	1	SM_RCMP#_VOL
SM_RCMP#_R76	1	SM_RCMP#_R76
SM_RCMP#_R73	1	SM_RCMP#_R73
SM_VREF#AR49	1	SM_VREF#AR49
SM_VREF#AW4	1	SM_VREF#AW4
V_VDR_MCH_REF	1	V_VDR_MCH_REF
AV29 M_CLK_DDR0	1	AV29 M_CLK_DDR0
BA29 M_CLK_DDR2	1	BA29 M_CLK_DDR2
AV23 M_CLK_DDR3	1	AV23 M_CLK_DDR3
AW30 M_CLK_DDR#0	1	AW30 M_CLK_DDR#0
BA23 M_CLK_DDR#1	1	BA23 M_CLK_DDR#1
AW25 M_CLK_DDR#2	1	AW25 M_CLK_DDR#2
AW23 M_CLK_DDR#3	1	AW23 M_CLK_DDR#3
BE20 DDR_CKE0 DIMMA	1	BE20 DDR_CKE0 DIMMA
AY32 DDR_CKE1 DIMMA	1	AY32 DDR_CKE1 DIMMA
BD39 DDR_CKE2 DIMMB	1	BD39 DDR_CKE2 DIMMB
BG37 DDR_CKE3 DIMMB	1	BG37 DDR_CKE3 DIMMB
BG20 DDR_CS0 DIMMA#	1	BG20 DDR_CS0 DIMMA#
BK16 DDR_CS1 DIMMA#	1	BK16 DDR_CS1 DIMMA#
BG16 DDR_CS2 DIMMB#	1	BG16 DDR_CS2 DIMMB#
BE13 DDR_CS3 DIMMB#	1	BE13 DDR_CS3 DIMMB#
BH18 M_ODT0	1	BH18 M_ODT0
BI15 M_ODT1	1	BI15 M_ODT1
BI14 M_ODT2	1	BI14 M_ODT2
BE16 M_ODT3	1	BE16 M_ODT3
BK31 SM_RCMP#_V0H	1	BK31 SM_RCMP#_V0H
BL15 SM_RCMP#_VOL	1	BL15 SM_RCMP#_VOL
CL_CLK	1	CL_CLK
CL_DATA	1	CL_DATA
CL_PWOK	1	CL_PWOK
CL_RST#	1	CL_RST#
CL_VREF	1	CL_VREF
ICH_SDVO_CLK	1	ICH_SDVO_CLK
SDVO_CTRL_CLK	1	SDVO_CTRL_CLK
CLKREQ#_B	1	CLKREQ#_B
MCH_ICH_SYNC#	1	MCH_ICH_SYNC#
TEST1	1	TEST1
TEST2	1	TEST2
DFTGT_VID0	1	DFTGT_VID0
DFTGT_VID1	1	DFTGT_VID1
DFTGT_VID2	1	DFTGT_VID2
DFTGT_VID3	1	DFTGT_VID3
DFTGT_VR_EN	1	DFTGT_VR_EN
CL_CLK0	1	CL_CLK0
CL_DATA0	1	CL_DATA0
M_PWOK	1	M_PWOK
CL_RST#	1	CL_RST#
MCH_ICH_SYNC#	1	MCH_ICH_SYNC#
GMCH	1	GMCH
TEST2	1	TEST2
TEST1	1	TEST1
R583	1	1KR2F-3-GP
R584	1	392R2F-3-GP
C548	1	SCD1U16V2ZY-3GP



<< >> DDR\_A\_D[0..63] 14  
 << >> DDR\_A\_BS[0..2] 14  
 << >> DDR\_A\_DM[0..7] 14  
 << >> DDR\_A\_DQS[0..7] 14  
 << >> DDR\_A\_DQS#[0..7] 14  
 << >> DDR\_A\_MA[0..13] 14

U89D 4 OF 10

DDR A D0	AR43	SA_DQ0	SA_BS0	BB19	DDR A BS0
DDR A D1	AW44	SA_DQ1	SA_BS1	BK19	DDR A BS1
DDR A D2	BA45	SA_DQ2	SA_BS2	BF29	DDR A BS2
DDR A D3	AY46	SA_DQ3			
DDR A D4	AR41	SA_DQ4	SA_CAS#	BL17	DDR A CAS#
DDR A D5	AR45	SA_DQ5			
DDR A D6	AT42	SA_DQ6	SA_DM0	AT45	DDR A DM0
DDR A D7	AW47	SA_DQ7	SA_DM1	BD44	DDR A DM1
DDR A D8	BF45	SA_DQ8	SA_DM2	BD42	DDR A DM2
DDR A D9	BF48	SA_DQ9	SA_DM3	AW38	DDR A DM3
DDR A D10	BG47	SA_DQ10	SA_DM4	AW13	DDR A DM4
DDR A D11	BJ45	SA_DQ11	SA_DM5	BG8	DDR A DM5
DDR A D12	BB47	SA_DQ12	SA_DM6	AY5	DDR A DM6
DDR A D13	BG50	SA_DQ13	SA_DM7	AN6	DDR A DM7
DDR A D14	BH49	SA_DQ14			
DDR A D15	BE45	SA_DQ15	SA_DQS0	AT46	DDR A DQS0
DDR A D16	AW43	SA_DQ16	SA_DQS1	BE48	DDR A DQS1
DDR A D17	BE44	SA_DQ17	SA_DQS2	BB43	DDR A DQS2
DDR A D18	BG42	SA_DQ18	SA_DQS3	BC37	DDR A DQS3
DDR A D19	BE40	SA_DQ19	SA_DQS4	BB16	DDR A DQS4
DDR A D20	BF44	SA_DQ20	SA_DQS5	BH6	DDR A DQS5
DDR A D21	BH45	SA_DQ21	SA_DQS6	BB2	DDR A DQS6
DDR A D22	BG40	SA_DQ22	SA_DQS7	AP3	DDR A DQS7
DDR A D23	BE40	SA_DQ23	SA_DQS#0	AT47	DDR A DQS#0
DDR A D24	AR40	SA_DQ24	SA_DQS#1	CD47	DDR A DQS#1
DDR A D25	AW40	SA_DQ25	SA_DQS#2	BC41	DDR A DQS#2
DDR A D26	AT39	SA_DQ26	SA_DQS#3	CA37	DDR A DQS#3
DDR A D27	AW36	SA_DQ27	SA_DQS#4	CA16	DDR A DQS#4
DDR A D28	AW41	SA_DQ28	SA_DQS#5	BH7	DDR A DQS#5
DDR A D29	AY41	SA_DQ29	SA_DQS#6	BC1	DDR A DQS#6
DDR A D30	AV38	SA_DQ30	SA_DQS#7	AP2	DDR A DQS#7
DDR A D31	AT38	SA_DQ31			
DDR A D32	AV13	SA_DQ32	SA_MA0	BJ19	DDR A MA0
DDR A D33	AT13	SA_DQ33	SA_MA1	BD20	DDR A MA1
DDR A D34	AW11	SA_DQ34	SA_MA2	BK27	DDR A MA2
DDR A D35	AV11	SA_DQ35	SA_MA3	BH28	DDR A MA3
DDR A D36	AU15	SA_DQ36	SA_MA4	BL24	DDR A MA4
DDR A D37	AT11	SA_DQ37	SA_MA5	BK28	DDR A MA5
DDR A D38	BA13	SA_DQ38	SA_MA6	BJ27	DDR A MA6
DDR A D39	BA11	SA_DQ39	SA_MA7	BJ25	DDR A MA7
DDR A D40	BE10	SA_DQ40	SA_MA8	BL28	DDR A MA8
DDR A D41	BD10	SA_DQ41	SA_MA9	BA28	DDR A MA9
DDR A D42	BD8	SA_DQ42	SA_MA10	BC19	DDR A MA10
DDR A D43	AY9	SA_DQ43	SA_MA11	BE28	DDR A MA11
DDR A D44	BG10	SA_DQ44	SA_MA12	BG30	DDR A MA12
DDR A D45	AW9	SA_DQ45	SA_MA13	BJ16	DDR A MA13
DDR A D46	BD7	SA_DQ46	SA_MA14	BJ29	DDR A MA14
DDR A D47	BB9	SA_DQ47			
DDR A D48	BB5	SA_DQ48	SA_RAS#	BE18	DDR A RAS#
DDR A D49	AY7	SA_DQ49	SA_RCVEN#	AY20	SA_RCVEN#
DDR A D50	AT5	SA_DQ50			
DDR A D51	AY5	SA_DQ51	SA_WE#	BA19	DDR A WE#
DDR A D52	AT7	SA_DQ52			
DDR A D53	BB7	SA_DQ53			
DDR A D54	AR5	SA_DQ54			
DDR A D55	AR8	SA_DQ55			
DDR A D56	AR3	SA_DQ56			
DDR A D57	AN3	SA_DQ57			
DDR A D58	AM8	SA_DQ58			
DDR A D59	AN10	SA_DQ59			
DDR A D60	AT3	SA_DQ60			
DDR A D61	AN9	SA_DQ61			
DDR A D62	AM8	SA_DQ62			
DDR A D63	AN11	SA_DQ63			

CRESTLINE-GP-U

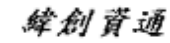
<< >> DDR\_B\_D[0..63] 15  
 << >> DDR\_B\_BS[0..2] 15  
 << >> DDR\_B\_DM[0..7] 15  
 << >> DDR\_B\_DQS[0..7] 15  
 << >> DDR\_B\_DQS#[0..7] 15  
 << >> DDR\_B\_MA[0..13] 15

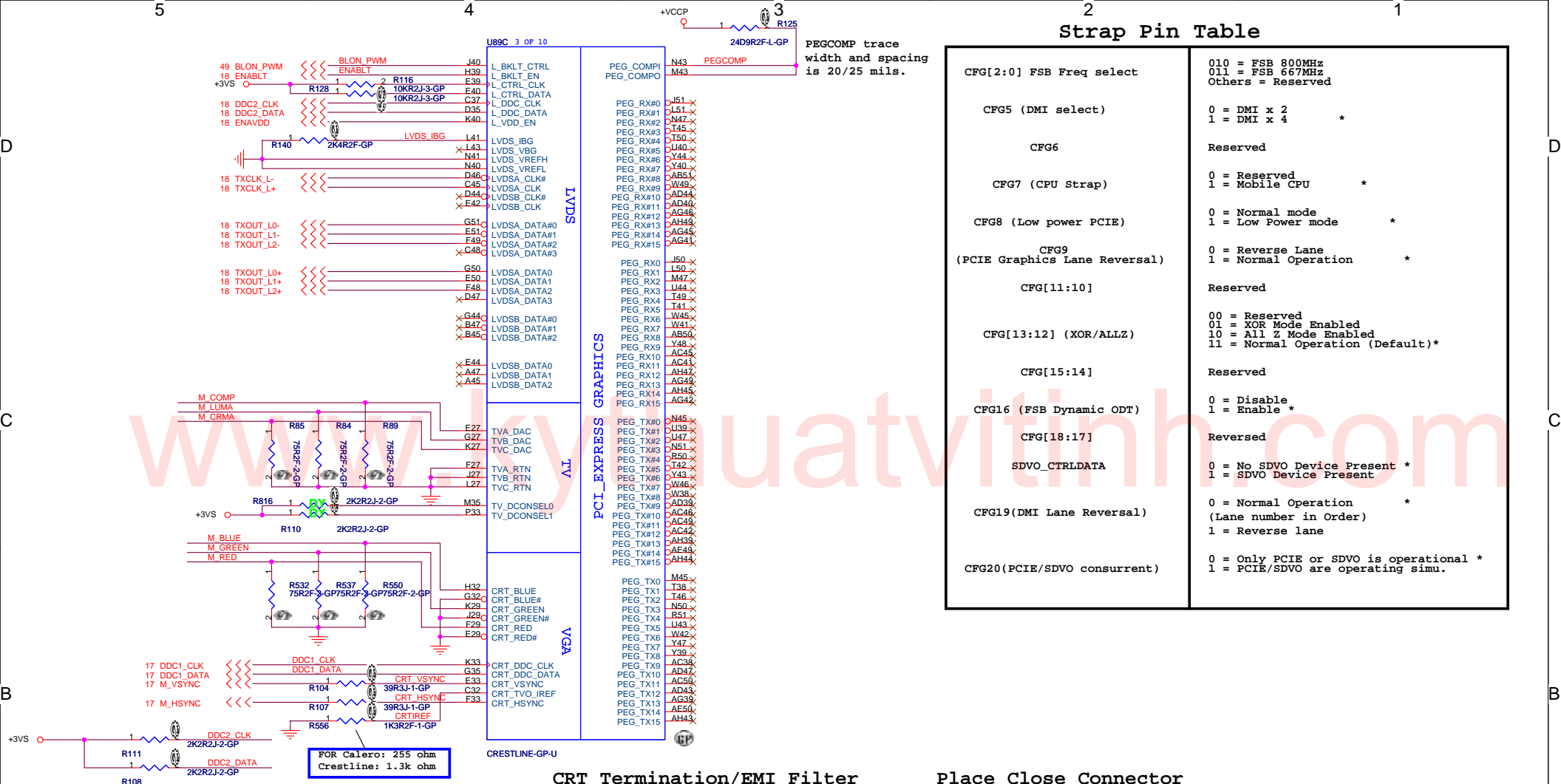
U89E 5 OF 10

DDR B D0	AP49	SB_DQ0	SB_BS0	AY17	DDR B BS0
DDR B D1	AR51	SB_DQ1	SB_BS1	BG18	DDR B BS1
DDR B D2	AW50	SB_DQ2	SB_BS2	BG36	DDR B BS2
DDR B D3	AN51	SB_DQ3			
DDR B D4	AW51	SB_DQ4	SB_CAS#	BE17	DDR B CAS#
DDR B D5	AN50	SB_DQ5			
DDR B D6	AV50	SB_DQ6	SA_DM0	AR50	DDR B DM0
DDR B D7	AV49	SB_DQ7	SA_DM1	BD49	DDR B DM1
DDR B D8	BA50	SB_DQ8	SA_DM2	BK45	DDR B DM2
DDR B D9	B850	SB_DQ9	SA_DM3	BL39	DDR B DM3
DDR B D10	BA49	SB_DQ10	SA_DM4	BH12	DDR B DM4
DDR B D11	BE50	SB_DQ11	SA_DM5	BJ7	DDR B DM5
DDR B D12	BA51	SB_DQ12	SA_DM6	BF3	DDR B DM6
DDR B D13	AY49	SB_DQ13	SA_DM7	AW2	DDR B DM7
DDR B D14	BF50	SB_DQ14			
DDR B D15	BF49	SB_DQ15	SB_DQS0	AT50	DDR B DQS0
DDR B D16	BJ50	SB_DQ16	SB_DQS1	BD50	DDR B DQS1
DDR B D17	BJ44	SB_DQ17	SB_DQS2	BK46	DDR B DQS2
DDR B D18	BL43	SB_DQ18	SB_DQS3	BK39	DDR B DQS3
DDR B D19	BL43	SB_DQ19	SB_DQS4	BJ12	DDR B DQS4
DDR B D20	BK47	SB_DQ20	SB_DQS5	BL7	DDR B DQS5
DDR B D21	BK49	SB_DQ21	SB_DQS6	BE2	DDR B DQS6
DDR B D22	BK42	SB_DQ22	SB_DQS7	AV2	DDR B DQS7
DDR B D23	BK43	SB_DQ23	SB_DQS#0	AU50	DDR B DQS#0
DDR B D24	BJ41	SB_DQ24	SB_DQS#1	BC50	DDR B DQS#1
DDR B D25	BL41	SB_DQ25	SB_DQS#2	BL45	DDR B DQS#2
DDR B D26	BJ37	SB_DQ26	SB_DQS#3	BK38	DDR B DQS#3
DDR B D27	BJ36	SB_DQ27	SB_DQS#4	BK12	DDR B DQS#4
DDR B D28	BK41	SB_DQ28	SB_DQS#5	BK7	DDR B DQS#5
DDR B D29	BJ40	SB_DQ29	SB_DQS#6	BE2	DDR B DQS#6
DDR B D30	BL35	SB_DQ30	SB_DQS#7	AV3	DDR B DQS#7
DDR B D31	BK37	SB_DQ31			
DDR B D32	BK13	SB_DQ32	SB_MA0	BC18	DDR B MA0
DDR B D33	BE11	SB_DQ33	SB_MA1	BG28	DDR B MA1
DDR B D34	BK11	SB_DQ34	SB_MA2	BG25	DDR B MA2
DDR B D35	BC11	SB_DQ35	SB_MA3	AW17	DDR B MA3
DDR B D36	BC13	SB_DQ36	SB_MA4	BF25	DDR B MA4
DDR B D37	BE12	SB_DQ37	SB_MA5	BE25	DDR B MA5
DDR B D38	BC12	SB_DQ38	SB_MA6	BA29	DDR B MA6
DDR B D39	BG12	SB_DQ39	SB_MA7	BC28	DDR B MA7
DDR B D40	BJ10	SB_DQ40	SB_MA8	AY28	DDR B MA8
DDR B D41	BL9	SB_DQ41	SB_MA9	BD37	DDR B MA9
DDR B D42	BK5	SB_DQ42	SB_MA10	BC17	DDR B MA10
DDR B D43	BL5	SB_DQ43	SB_MA11	BE37	DDR B MA11
DDR B D44	BK9	SB_DQ44	SB_MA12	BA39	DDR B MA12
DDR B D45	BK10	SB_DQ45	SB_MA13	BG13	DDR B MA13
DDR B D46	BJ8	SB_DQ46	SB_MA14	BE24	DDR B MA14
DDR B D47	BJ8	SB_DQ47			
DDR B D48	BF4	SB_DQ48	SB_RAS#	AV16	DDR B RAS#
DDR B D49	BH5	SB_DQ49	SB_RCVEN#	AY18	SB_RCVEN#
DDR B D50	BG1	SB_DQ50			
DDR B D51	BC2	SB_DQ51	SB_WE#	BC17	DDR B WE#
DDR B D52	BK3	SB_DQ52			
DDR B D53	BE4	SB_DQ53			
DDR B D54	BD3	SB_DQ54			
DDR B D55	BJ2	SB_DQ55			
DDR B D56	BA3	SB_DQ56			
DDR B D57	BB3	SB_DQ57			
DDR B D58	AR1	SB_DQ58			
DDR B D59	AT3	SB_DQ59			
DDR B D60	AY2	SB_DQ60			
DDR B D61	AY3	SB_DQ61			
DDR B D62	AU2	SB_DQ62			
DDR B D63	AT2	SB_DQ63			

CRESTLINE-GP-U

<Core Design>

 <b>Wistron Corporation</b> 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
<b>CRESTLINE(2/6)-DDR2 A/B CH</b>	
Size	Rev
A3	PV
Date: Friday, March 30, 2007	
Sheet 9 of 51	



### Strap Pin Table

CFG[2:0] FSB Freq select	010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	Reserved
CFG7 (CPU Strap)	0 = Reserved 1 = Mobile CPU *
CFG8 (Low power PCIE)	0 = Normal mode 1 = Low Power mode *
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane 1 = Normal Operation *
CFG[11:10]	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disable 1 = Enable *
CFG[18:17]	Reversed
SDVO_CTRLDATA	0 = No SDVO Device Present * 1 = SDVO Device Present
CFG19(DMI Lane Reversal)	0 = Normal Operation (Lane number in Order) 1 = Reverse lane *
CFG20(PCIE/SDVO consurrent)	0 = Only PCIE or SDVO is operational * 1 = PCIE/SDVO are operating simu.

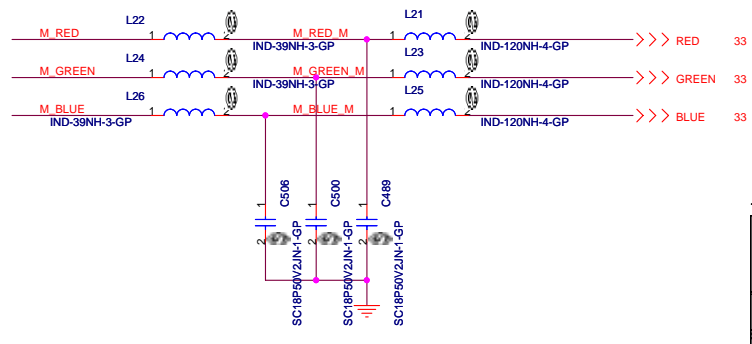
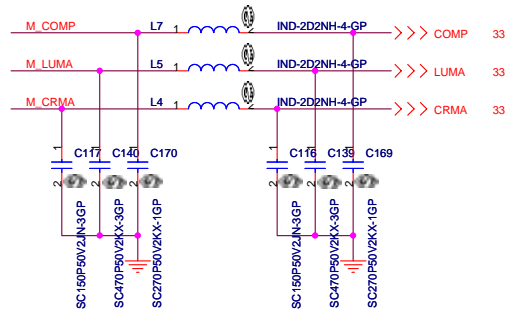
PEGCOMP trace width and spacing is 20/25 mils.

### CRT Termination/EMI Filter

### Place Close Connector

### TV-Out Termination/EMI Filter

Place Close N/B



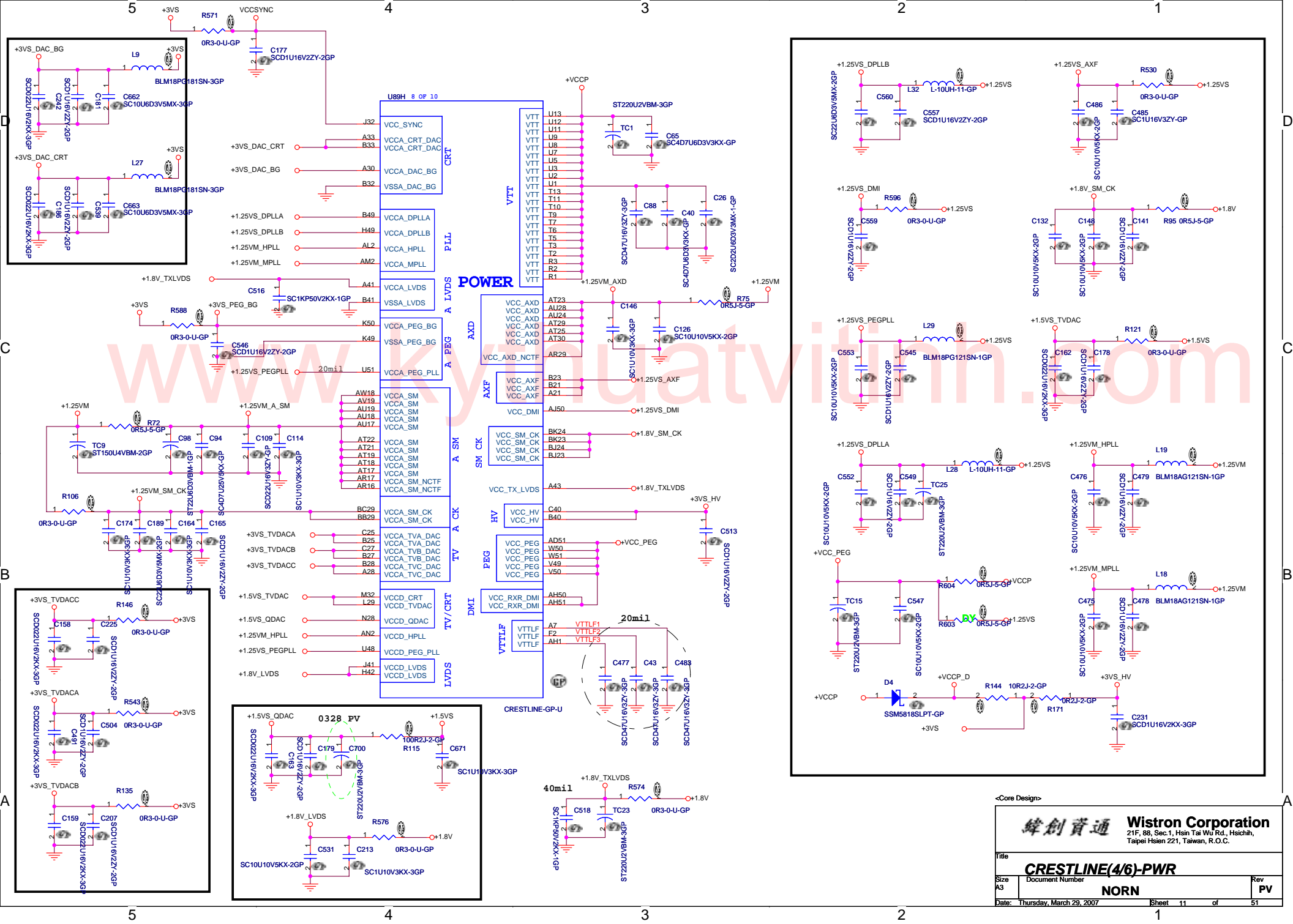
<Core Design>

**緯創資通 Wistron Corporation**  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.

Title: **CRESTLINE(3/6)-VGA/LVDS/TV**

Size A3 Document Number **NORN** Rev **PV**

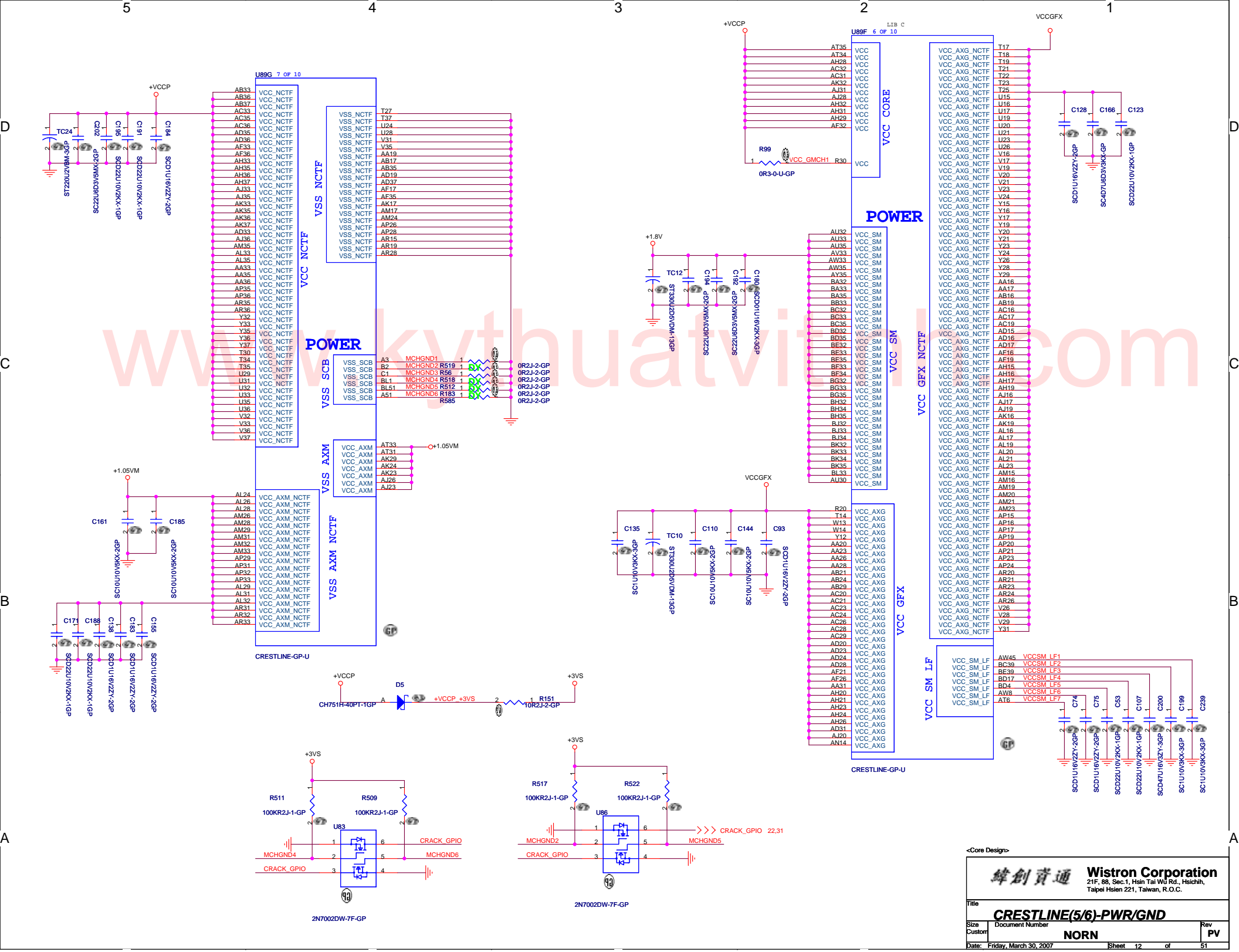
Date: Friday, March 30, 2007 Sheet 10 of 51



<Core Design>

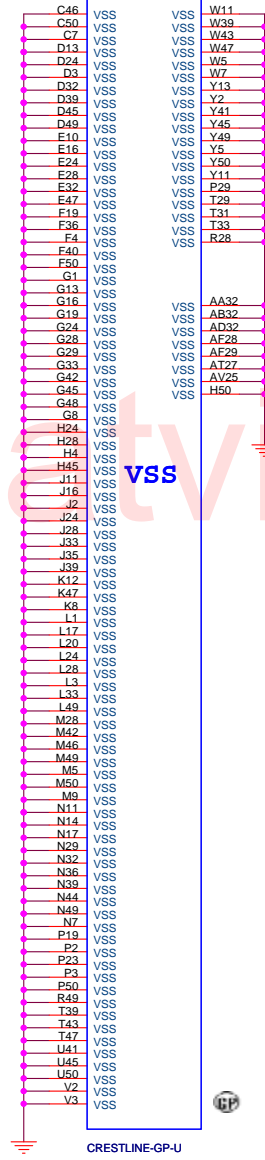
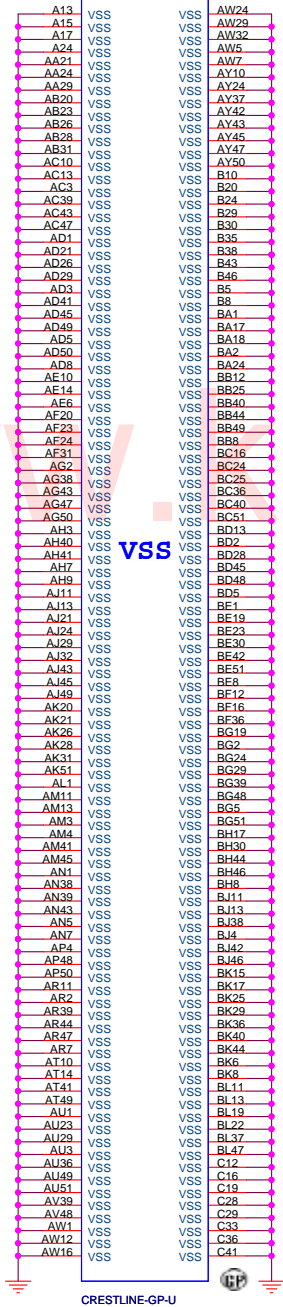
**緯創資通** **Wistron Corporation**  
 21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichin,  
 Taipei Hsin 221, Taiwan, R.O.C.

<b>CRESTLINE(4/6)-PWR</b>			
Title	Document Number	Rev	PV
Size A3	<b>NORN</b>		
Date: Thursday, March 29, 2007	Sheet 11	of	51



U89I 9 OF 10

U89J10 OF 10



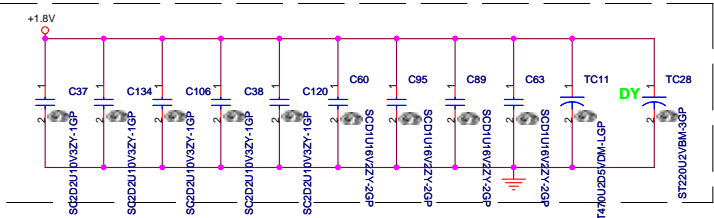
www.tything.com

<Core Design>

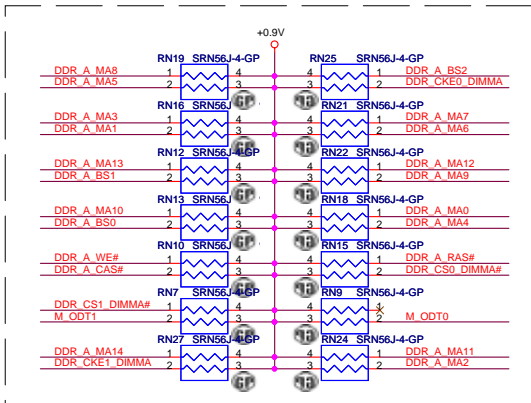
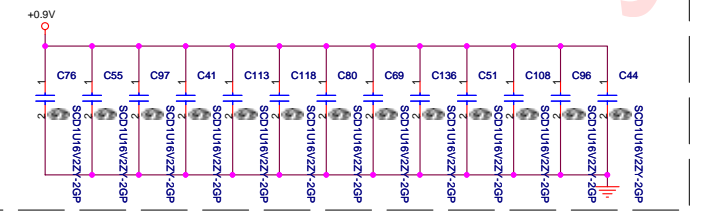
<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>CRESTLINE(6/6)-PWR/GND</b>			
Size	Document Number	Rev	PV
A3			
Date: Monday, March 05, 2007		Sheet 13 of	51

- 9 DDR\_A\_DQS[0..7] <<>>
- 9 DDR\_A\_DQ[0..63] <<>>
- 9 DDR\_A\_DM[0..7] <<>>
- 9 DDR\_A\_DQS[0..7] <<>>
- 9 DDR\_A\_MA[0..13] <<>>
- 9 DDR\_A\_BS[0..2] <<>>

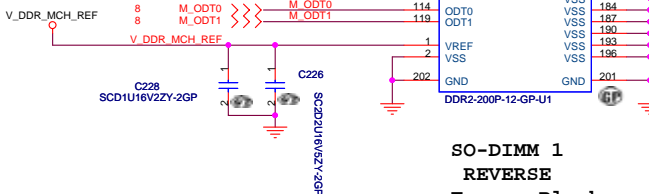
Layout Note:  
Place near DM1



Layout Note:  
Place one cap close to every 2 pullup resistors terminated to +0.9VS



Layout Note:  
Place these resistors closely DM1, all trace length Max=1.5"



DM1

DDR_A MA0	102	A0	108	DDR_A_RAS#	<<>>	DDR_A_RAS# 9
DDR_A MA1	101	A1	109	DDR_A_WE#	<<>>	DDR_A_WE# 9
DDR_A MA2	100	A2	113	DDR_A_CAS#	<<>>	DDR_A_CAS# 9
DDR_A MA3	99	A3	110	DDR_CS0_DIMMA#	<<>>	DDR_CS0_DIMMA# 8
DDR_A MA4	98	A4	115	DDR_CS1_DIMMA#	<<>>	DDR_CS1_DIMMA# 8
DDR_A MA5	97	A5	79	DDR_CKE0_DIMMA	<<>>	DDR_CKE0_DIMMA 8
DDR_A MA6	96	A6	80	DDR_CK1_DIMMA	<<>>	DDR_CK1_DIMMA 8
DDR_A MA7	95	A7				
DDR_A MA8	94	A8				
DDR_A MA9	93	A9				
DDR_A MA10	92	A10				
DDR_A MA11	91	A10/AP				
DDR_A MA12	90	A11				
DDR_A MA13	89	A12				
DDR_A MA14	88	A13				
DDR_A BS2	87	A14				
DDR_A BS0	86	A15				
DDR_A BS1	85	A16/BA2				
DDR_A D0	7	D00				
DDR_A D1	6	D01				
DDR_A D2	5	D02				
DDR_A D3	4	D03				
DDR_A D4	3	D04				
DDR_A D5	2	D05				
DDR_A D6	1	D06				
DDR_A D7	0	D07				
DDR_A D8	23	D08				
DDR_A D9	22	D09				
DDR_A D10	21	D10				
DDR_A D11	20	D11				
DDR_A D12	19	D12				
DDR_A D13	18	D13				
DDR_A D14	17	D14				
DDR_A D15	16	D15				
DDR_A D16	15	D16				
DDR_A D17	14	D17				
DDR_A D18	13	D18				
DDR_A D19	12	D19				
DDR_A D20	11	D20				
DDR_A D21	10	D21				
DDR_A D22	9	D22				
DDR_A D23	8	D23				
DDR_A D24	7	D24				
DDR_A D25	6	D25				
DDR_A D26	5	D26				
DDR_A D27	4	D27				
DDR_A D28	3	D28				
DDR_A D29	2	D29				
DDR_A D30	1	D30				
DDR_A D31	0	D31				
DDR_A D32	123	D32				
DDR_A D33	122	D33				
DDR_A D34	121	D34				
DDR_A D35	120	D35				
DDR_A D36	119	D36				
DDR_A D37	118	D37				
DDR_A D38	117	D38				
DDR_A D39	116	D39				
DDR_A D40	115	D40				
DDR_A D41	114	D41				
DDR_A D42	113	D42				
DDR_A D43	112	D43				
DDR_A D44	111	D44				
DDR_A D45	110	D45				
DDR_A D46	109	D46				
DDR_A D47	108	D47				
DDR_A D48	107	D48				
DDR_A D49	106	D49				
DDR_A D50	105	D50				
DDR_A D51	104	D51				
DDR_A D52	103	D52				
DDR_A D53	102	D53				
DDR_A D54	101	D54				
DDR_A D55	100	D55				
DDR_A D56	99	D56				
DDR_A D57	98	D57				
DDR_A D58	97	D58				
DDR_A D59	96	D59				
DDR_A D60	95	D60				
DDR_A D61	94	D61				
DDR_A D62	93	D62				
DDR_A D63	92	D63				
DDR_A DQS#0	11	/DQ80				
DDR_A DQS#1	29	/DQ81				
DDR_A DQS#2	49	/DQ82				
DDR_A DQS#3	69	/DQ83				
DDR_A DQS#4	89	/DQ84				
DDR_A DQS#5	109	/DQ85				
DDR_A DQS#6	129	/DQ86				
DDR_A DQS#7	149	/DQ87				
DDR_A DQS0	13	DQ80				
DDR_A DQS1	31	DQ81				
DDR_A DQS2	51	DQ82				
DDR_A DQS3	71	DQ83				
DDR_A DQS4	91	DQ84				
DDR_A DQS5	111	DQ85				
DDR_A DQS6	131	DQ86				
DDR_A DQS7	151	DQ87				
M_ODT0	114	ODT0				
M_ODT1	119	ODT1				
VREF	1	VREF				
GND	2	GND				
GND	201	GND				

SO-DIMM 1  
REVERSE  
Foxcon Black  
62.10017.E11

<Variant Name>

**緯創資通** Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichu,  
Taipei Hsien 221, Taiwan, R.O.C.

Title  
**DDRII-SODIMM SLOT1**

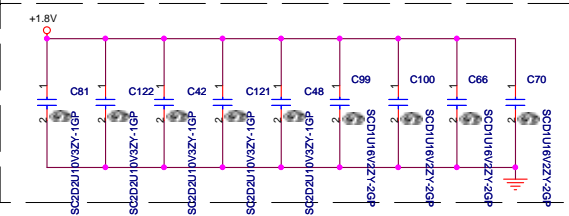
Size Custom Document Number  
**NORN** Rev PV

Date: Friday, March 30, 2007 Sheet 14 of 51

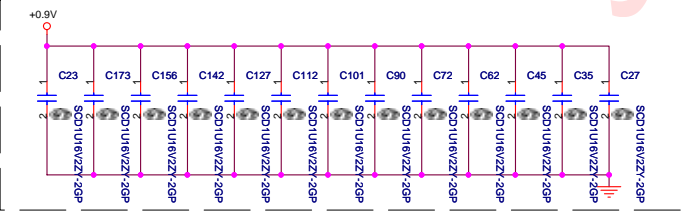


- 9 DDR\_B\_DQS#0..7 <<>
- 9 DDR\_B\_DQ[0..63] <<>
- 9 DDR\_B\_DM0..7 <<>
- 9 DDR\_B\_DQS[0..7] <<>
- 9 DDR\_B\_MA[0..13] <<>
- 9 DDR\_B\_BS[0..2] <<>

Layout Note:  
Place near DM2



Layout Note:  
Place one cap close to every 2 pullup resistors terminated to +0.9VS

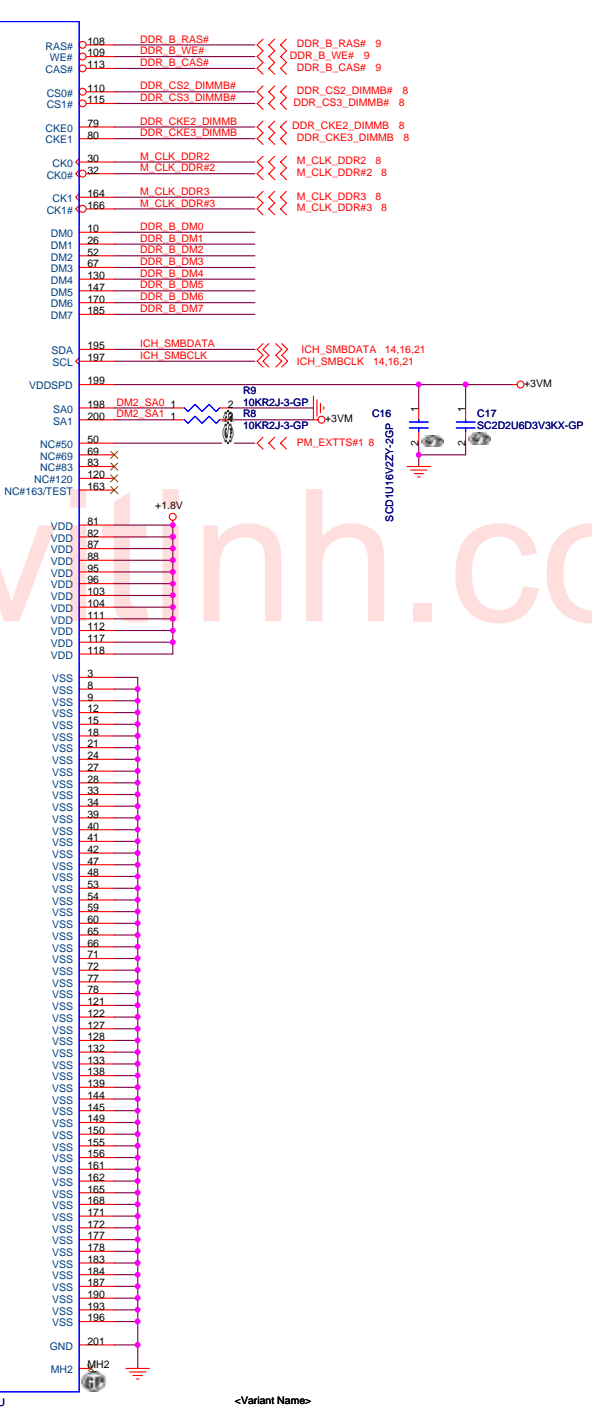
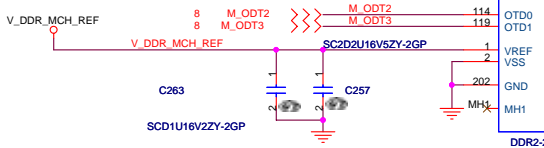
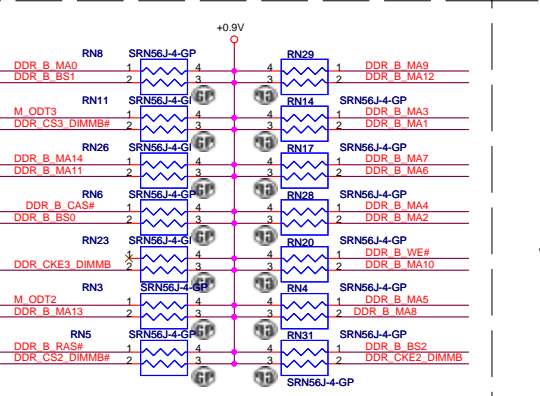


9 DDR\_B\_MA14 <<>

Pin	Signal	Pin	Signal
102	DDR_B_MA0	A0	DM2
101	DDR_B_MA1	A1	DM2
100	DDR_B_MA2	A2	DM2
99	DDR_B_MA3	A3	DM2
98	DDR_B_MA4	A4	DM2
97	DDR_B_MA5	A5	DM2
94	DDR_B_MA6	A6	DM2
92	DDR_B_MA7	A7	DM2
93	DDR_B_MA8	A8	DM2
91	DDR_B_MA9	A9	DM2
105	DDR_B_MA10	A10/AP	DM2
90	DDR_B_MA11	A11	DM2
116	DDR_B_MA13	A13	DM2
86	DDR_B_MA14	A14	DM2
84		A15	DM2
85	DDR_B_BS2	A16/BA2	DM2
107	DDR_B_BS0	BA0	DM2
106	DDR_B_BS1	BA1	DM2
5	DDR_B_D0	DO0	DM2
7	DDR_B_D1	DO1	DM2
17	DDR_B_D2	DO2	DM2
19	DDR_B_D3	DO3	DM2
4	DDR_B_D4	DO4	DM2
6	DDR_B_D5	DO5	DM2
14	DDR_B_D6	DO6	DM2
23	DDR_B_D7	DO7	DM2
25	DDR_B_D8	DO8	DM2
26	DDR_B_D9	DO9	DM2
35	DDR_B_D10	DO10	DM2
20	DDR_B_D11	DO11	DM2
22	DDR_B_D12	DO12	DM2
22	DDR_B_D13	DO13	DM2
22	DDR_B_D14	DO14	DM2
38	DDR_B_D15	DO15	DM2
39	DDR_B_D16	DO16	DM2
43	DDR_B_D17	DO17	DM2
45	DDR_B_D18	DO18	DM2
55	DDR_B_D19	DO19	DM2
57	DDR_B_D20	DO20	DM2
44	DDR_B_D21	DO21	DM2
46	DDR_B_D22	DO22	DM2
58	DDR_B_D23	DO23	DM2
61	DDR_B_D24	DO24	DM2
63	DDR_B_D25	DO25	DM2
73	DDR_B_D26	DO26	DM2
75	DDR_B_D27	DO27	DM2
62	DDR_B_D28	DO28	DM2
64	DDR_B_D29	DO29	DM2
74	DDR_B_D30	DO30	DM2
76	DDR_B_D31	DO31	DM2
123	DDR_B_D32	DO32	DM2
125	DDR_B_D33	DO33	DM2
135	DDR_B_D34	DO34	DM2
137	DDR_B_D35	DO35	DM2
124	DDR_B_D36	DO36	DM2
126	DDR_B_D37	DO37	DM2
134	DDR_B_D38	DO38	DM2
136	DDR_B_D39	DO39	DM2
141	DDR_B_D40	DO40	DM2
143	DDR_B_D41	DO41	DM2
151	DDR_B_D42	DO42	DM2
153	DDR_B_D43	DO43	DM2
140	DDR_B_D44	DO44	DM2
142	DDR_B_D45	DO45	DM2
152	DDR_B_D46	DO46	DM2
154	DDR_B_D47	DO47	DM2
157	DDR_B_D48	DO48	DM2
159	DDR_B_D49	DO49	DM2
173	DDR_B_D50	DO50	DM2
175	DDR_B_D51	DO51	DM2
158	DDR_B_D52	DO52	DM2
176	DDR_B_D53	DO53	DM2
177	DDR_B_D54	DO54	DM2
179	DDR_B_D55	DO55	DM2
181	DDR_B_D56	DO56	DM2
189	DDR_B_D57	DO57	DM2
189	DDR_B_D58	DO58	DM2
191	DDR_B_D59	DO59	DM2
180	DDR_B_D60	DO60	DM2
182	DDR_B_D61	DO61	DM2
192	DDR_B_D62	DO62	DM2
194	DDR_B_D63	DO63	DM2

Layout Note:  
Place these resistors  
closely DM2, all  
trace length Max=1.5"

111	DDR_B_DQS#0	DO50#
112	DDR_B_DQS#1	DO51#
49	DDR_B_DQS#2	DO52#
68	DDR_B_DQS#3	DO53#
129	DDR_B_DQS#4	DO54#
146	DDR_B_DQS#5	DO55#
167	DDR_B_DQS#6	DO56#
186	DDR_B_DQS#7	DO57#
13	DDR_B_DQS0	DO50
31	DDR_B_DQS1	DO51
51	DDR_B_DQS2	DO52
70	DDR_B_DQS3	DO53
131	DDR_B_DQS4	DO54
148	DDR_B_DQS5	DO55
169	DDR_B_DQS6	DO56
188	DDR_B_DQS7	DO57



SO-DIMM 2  
STANDARD

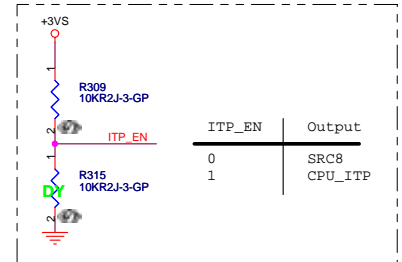
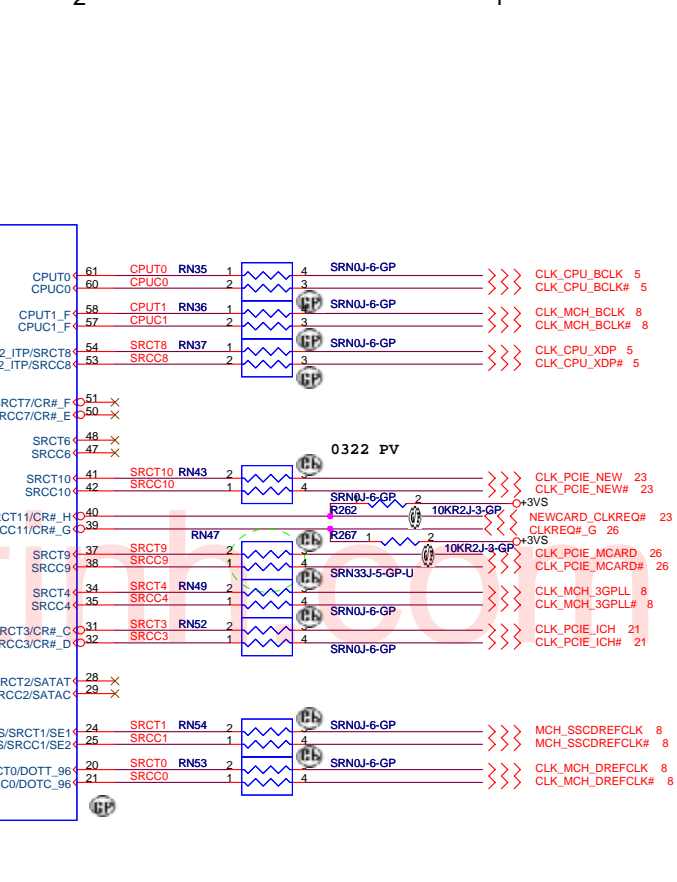
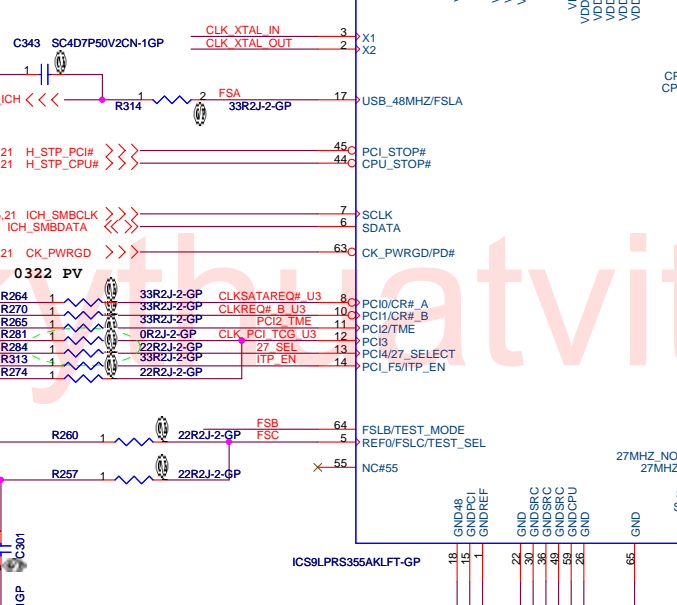
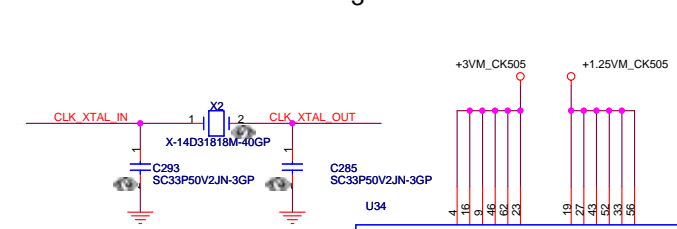
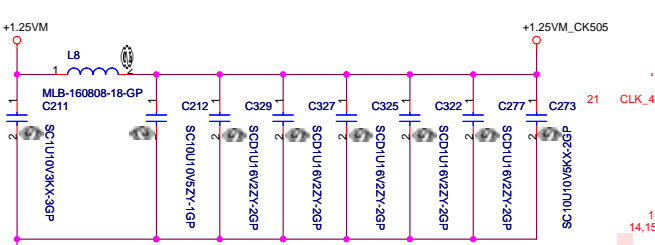
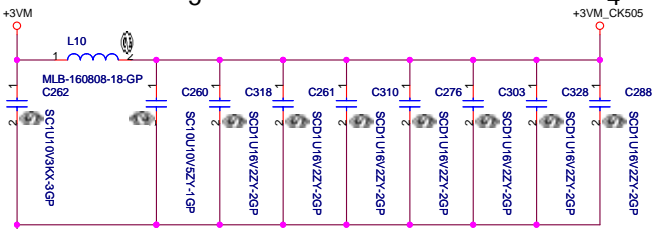
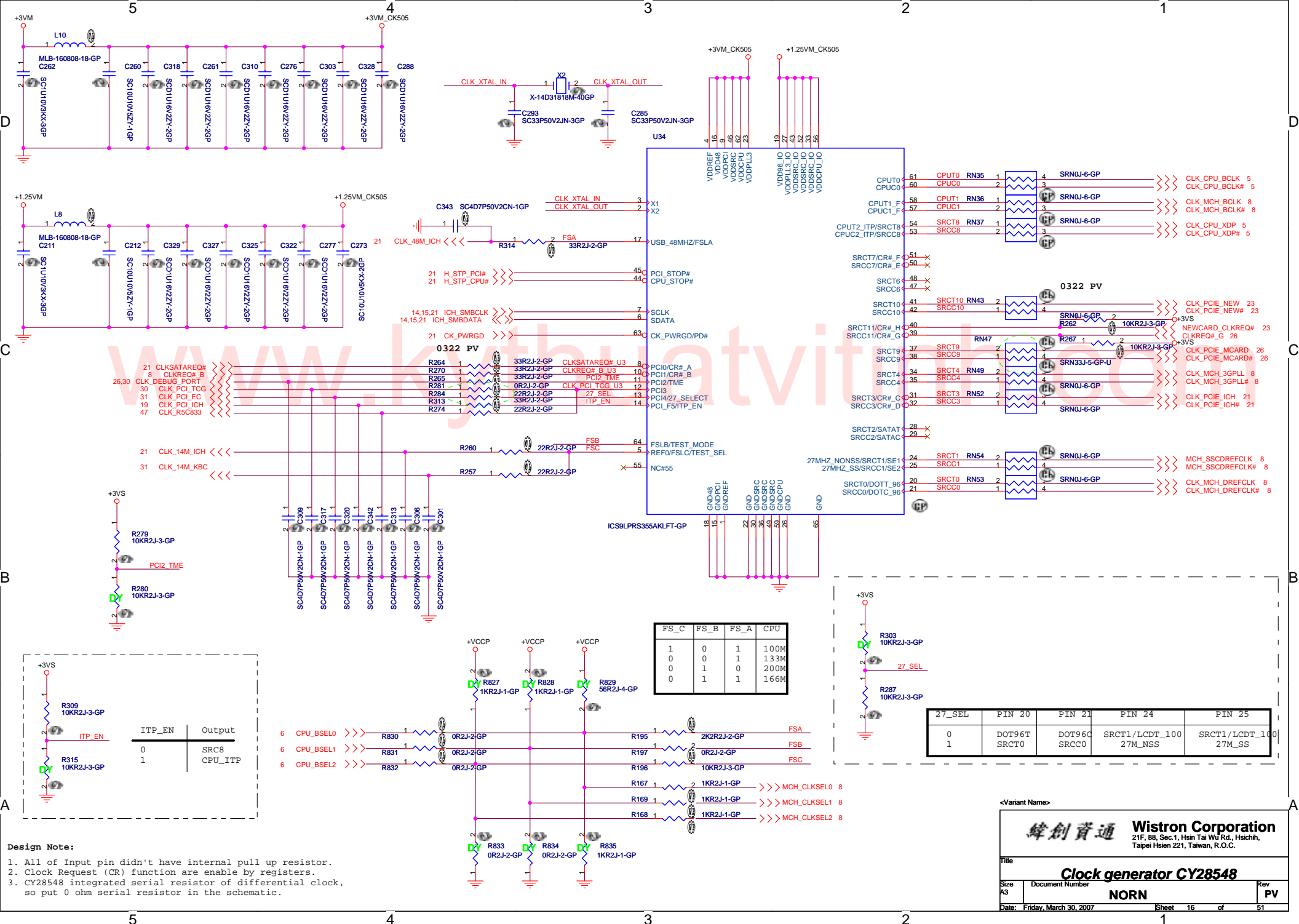
Wistron Corporation  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichu, Taipei Hsien 221, Taiwan, R.O.C.

DDRII-SODIMM SLOT2

Norm

Rev PV

Date: Friday, March 30, 2007



FS_C	FS_B	FS_A	CPU
1	0	1	100M
0	0	1	133M
0	1	0	200M
0	1	1	166M

27_SEL	PIN 20	PIN 21	PIN 24	PIN 25
0	DOT96T	DOT96C	SRCT1/LCDDT_100	SRCT1/LCDDT_100
1			27M_NSS	27M_SS

**Design Note:**

1. All of Input pin didn't have internal pull up resistor.
2. Clock Request (CR) function are enable by registers.
3. CY28548 integrated serial resistor of differential clock, so put 0 ohm serial resistor in the schematic.

<Variant Name>

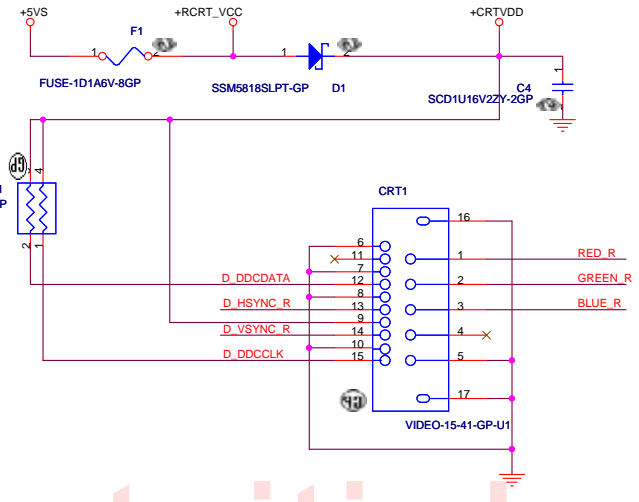
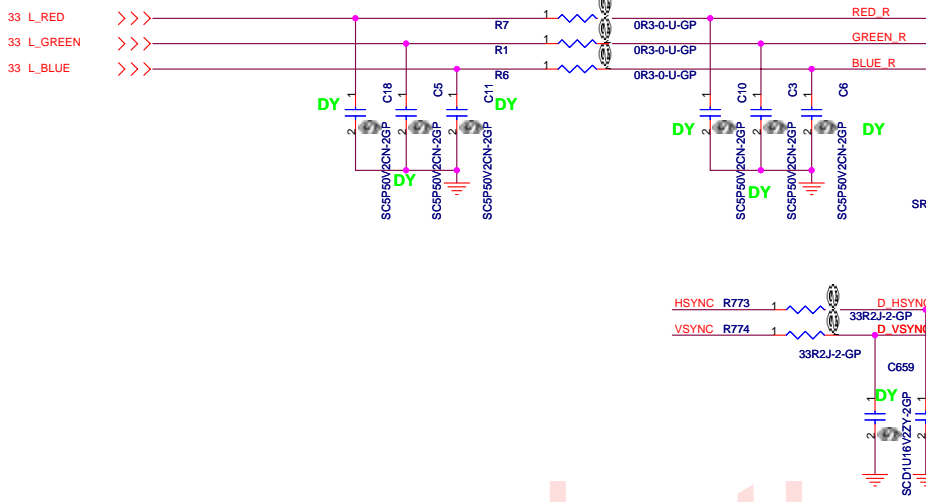
**緯創資通 Wistron Corporation**  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichin, Taipei Hsin 221, Taiwan, R.O.C.

Title: **Clock generator CY28548**

Size A3 Document Number **NORN** Rev **PV**

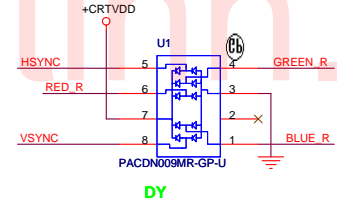
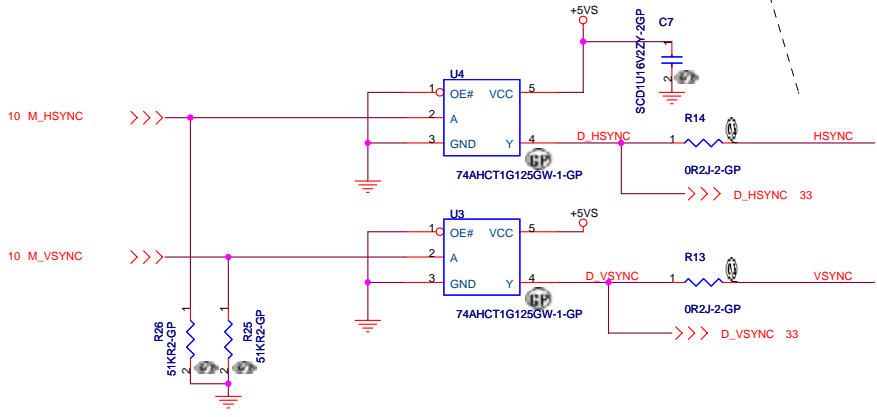
Date: Friday, March 30, 2007 Sheet 16 of 51



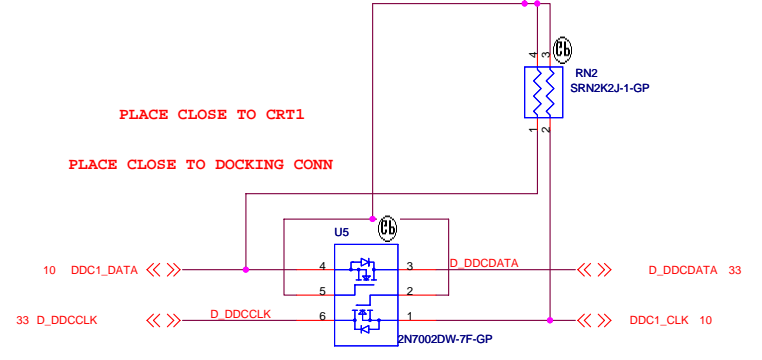


**CRT**

Layout Note : HSYNC & VSYNC SHOULD BE ROUTED TO DOCK CRT CONN. , THEN TO SYSTEM CRT CONN.



PLACE CLOSE TO CRT1  
PLACE CLOSE TO DOCKING CONN



<Core Design>

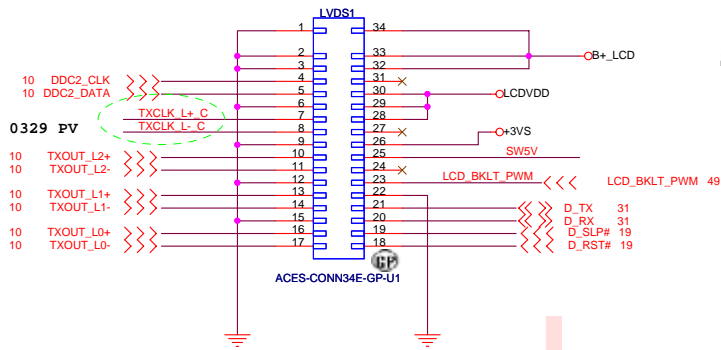
**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **CRT/TV CONNECTOR**

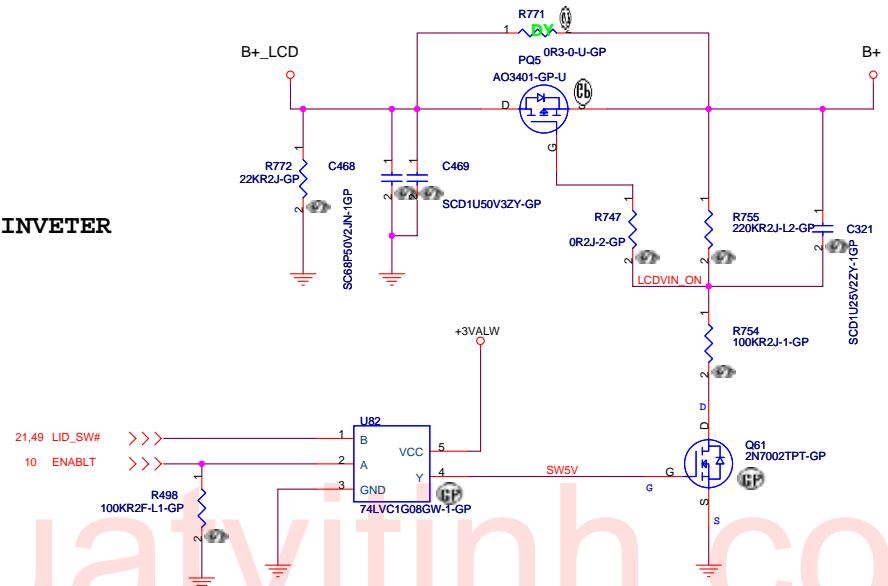
Size A3 Document Number **NORN** Rev **PV**

Date: Friday, March 30, 2007 Sheet 17 of 51

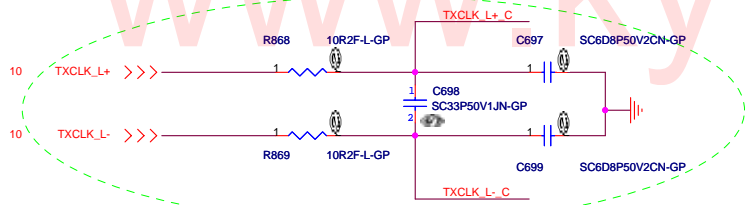
# LVDS CONN



## SUPPORT LED INVETER

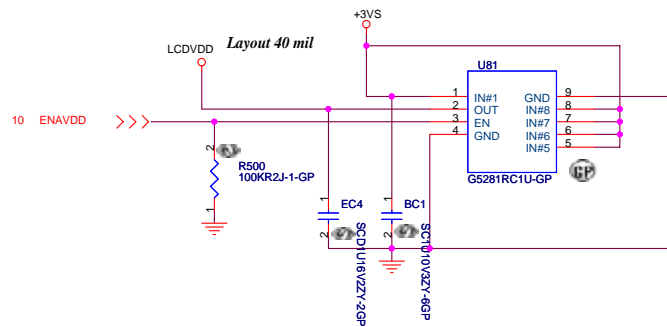
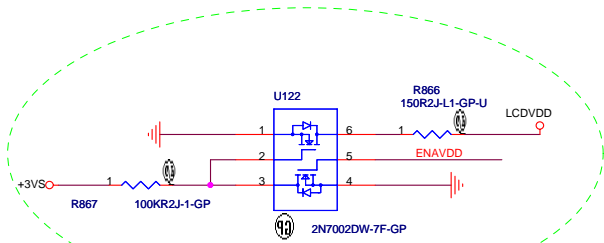


### 0329 PV Near the LVDS1 connector



# LCD POWER CIRCUIT

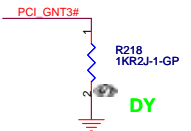
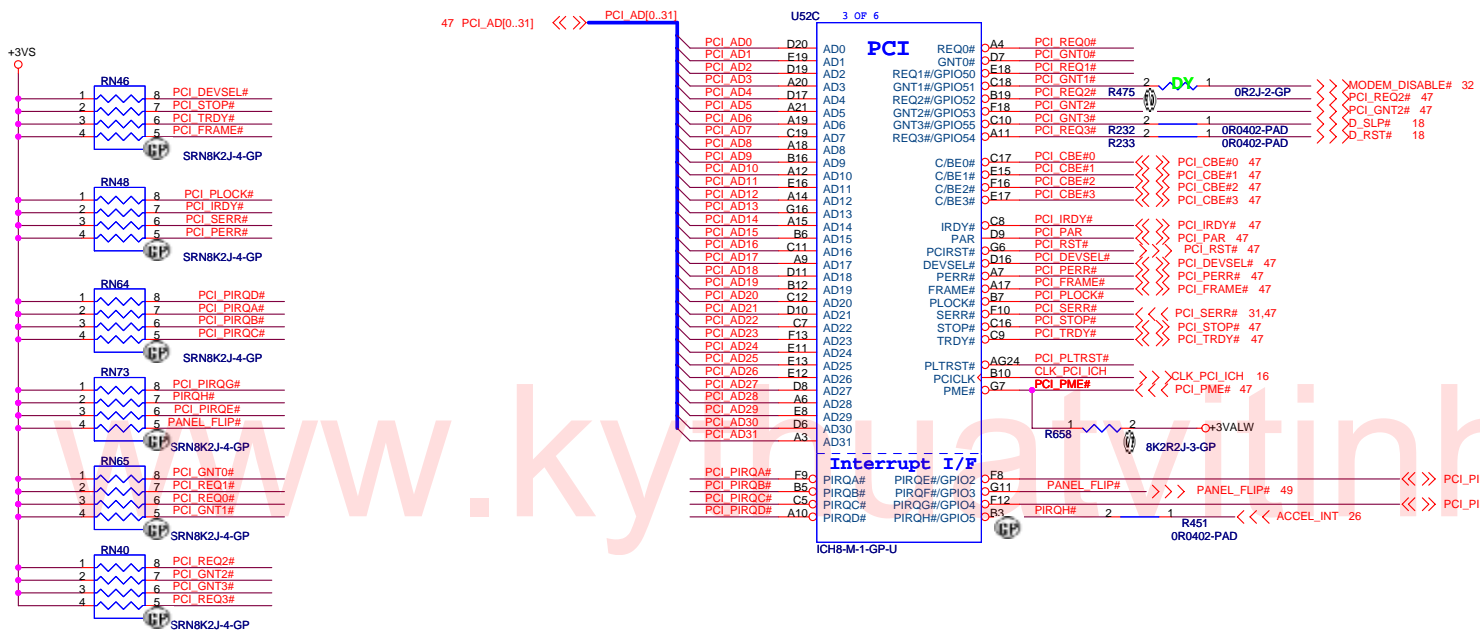
0319 PV



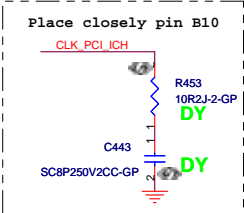
<Core Design>

緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

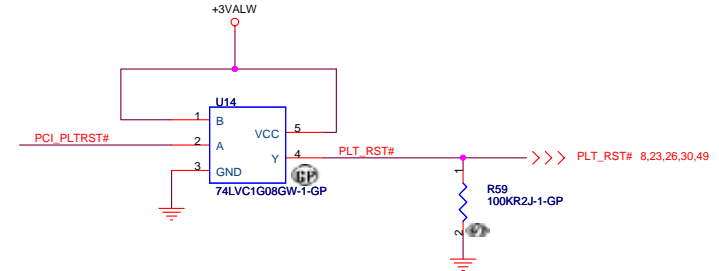
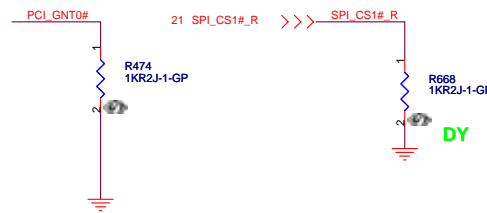
Title		
LCD CONN.		
Size	Document Number	Rev
A3	NORN	PV
Date:	Friday, March 30, 2007	Sheet 18 of 51



A16 swap override Strap	
PCI_GNT3#	Low= A16 swap override Enable High= Default *



Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI *
1	0	PCI
1	1	LPC



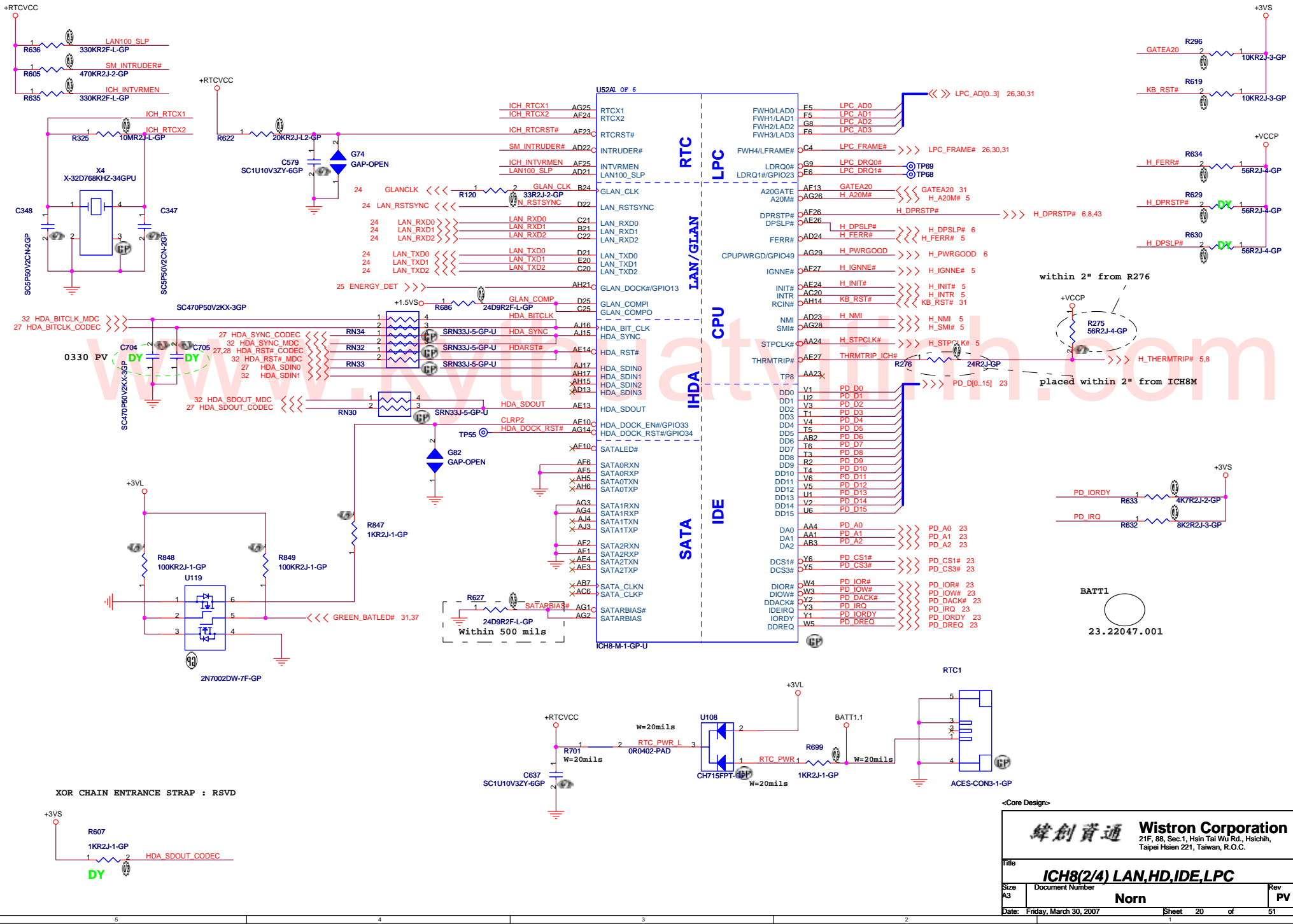
<Core Design>

**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **ICH8(1/4)-PCI/INT**

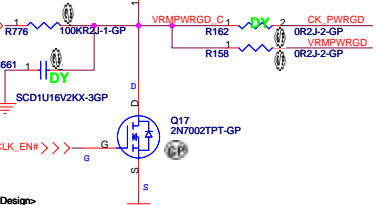
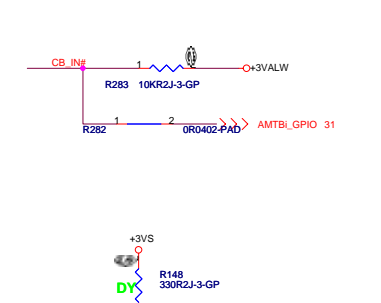
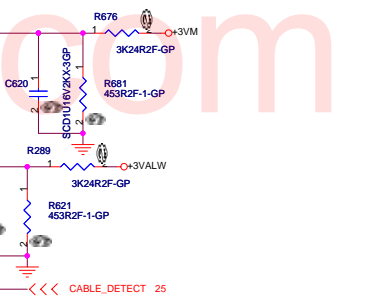
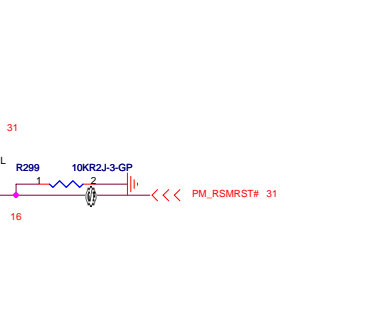
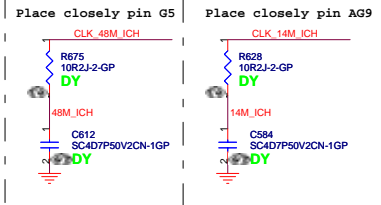
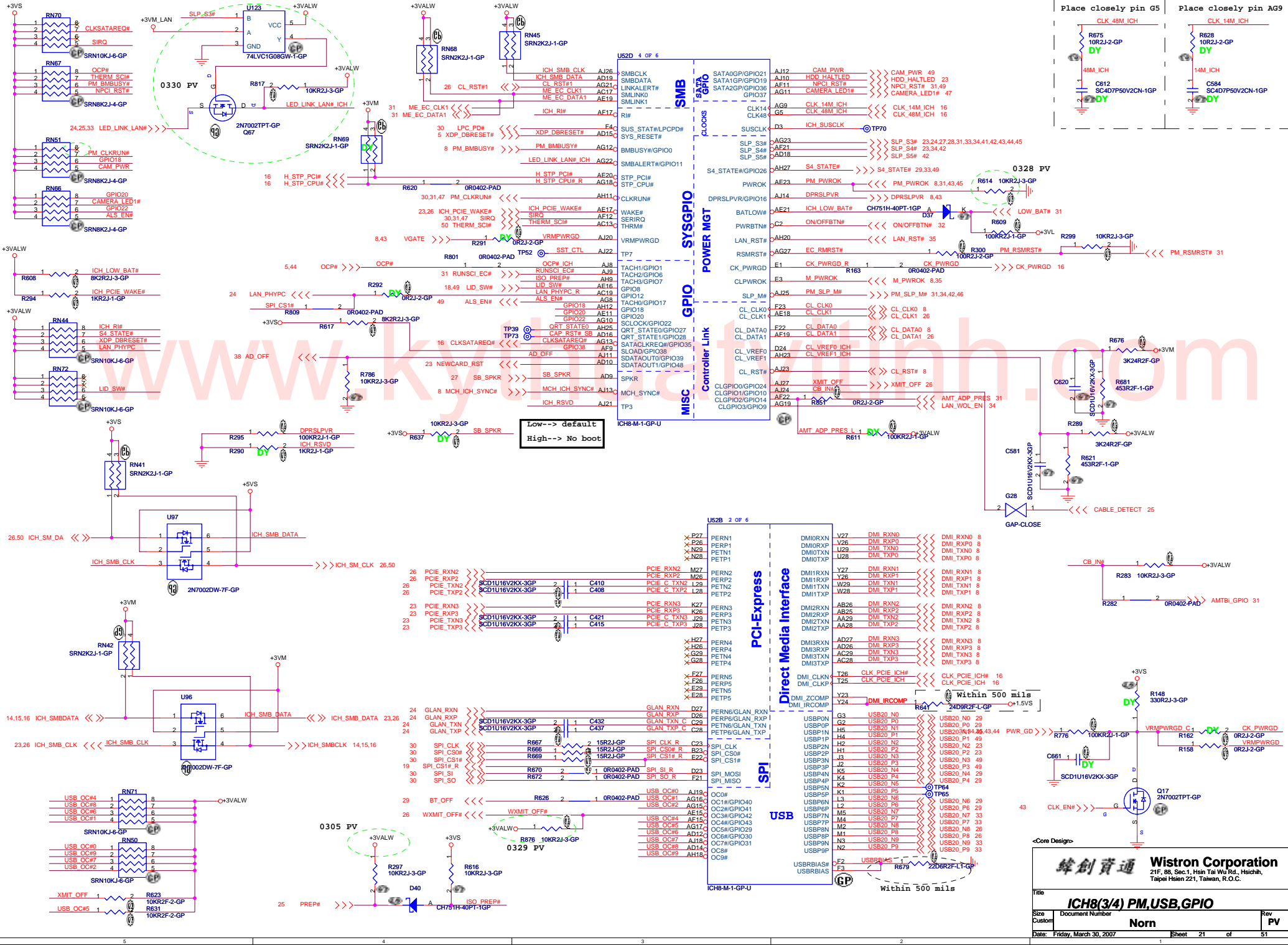
Size A3 Document Number **Norn** Rev **PV**

Date: Friday, March 30, 2007 Sheet 19 of 51



<Core Design>

<b>緯創資通 Wistron Corporation</b>		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
<b>ICH8(2/4) LAN,HD,IDE,LPC</b>		
Size	Document Number	Rev
A3		PV
<b>Norn</b>		
Date:	Friday, March 30, 2007	Sheet 20 of 51

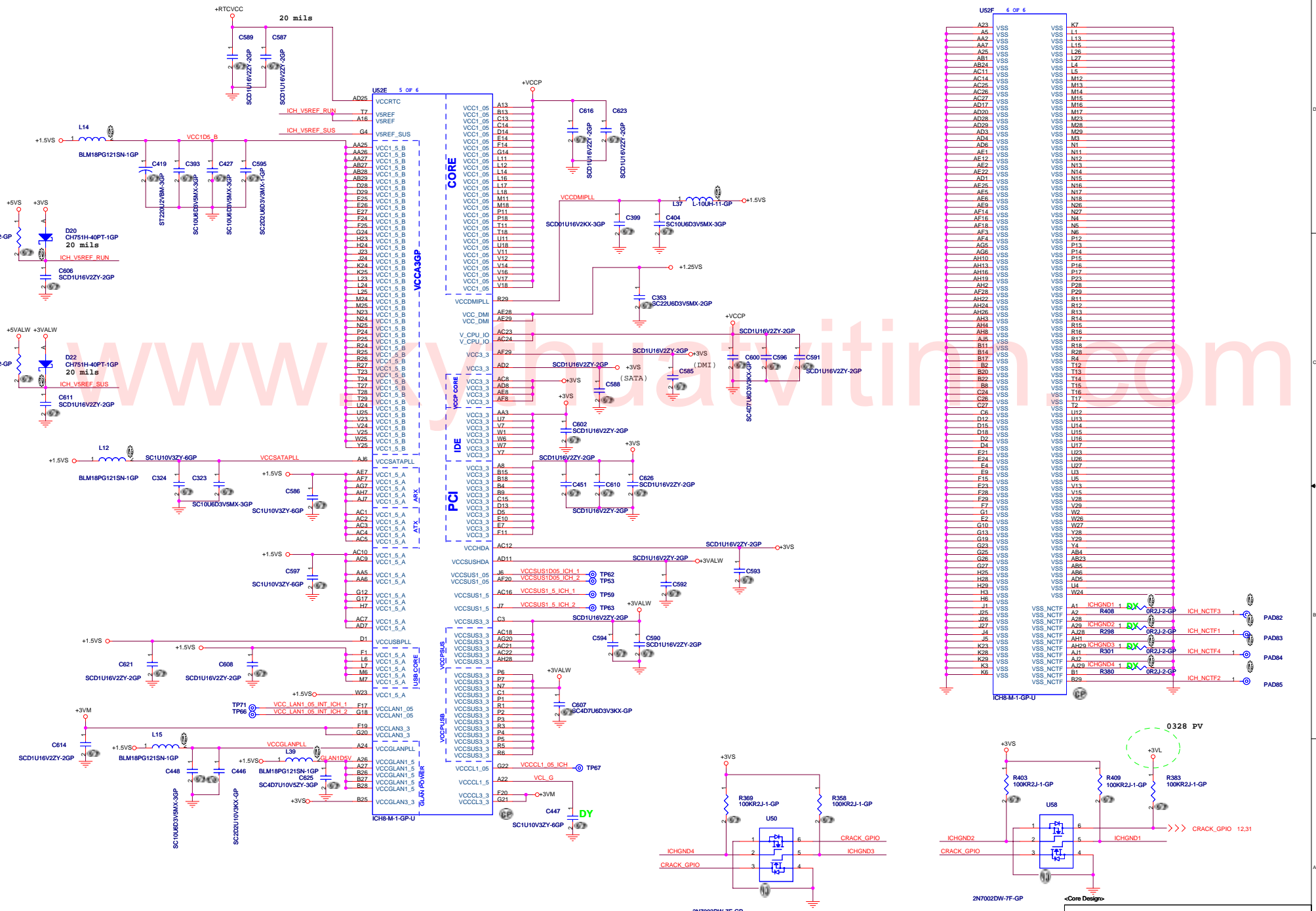


Wistron Corporation  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsiehshih, Taipei Hsien 221, Taiwan, R.O.C.

File: ICH8(3/4) PM,USB,GPIO

Size: Custom Document Number: Norm Rev: PV

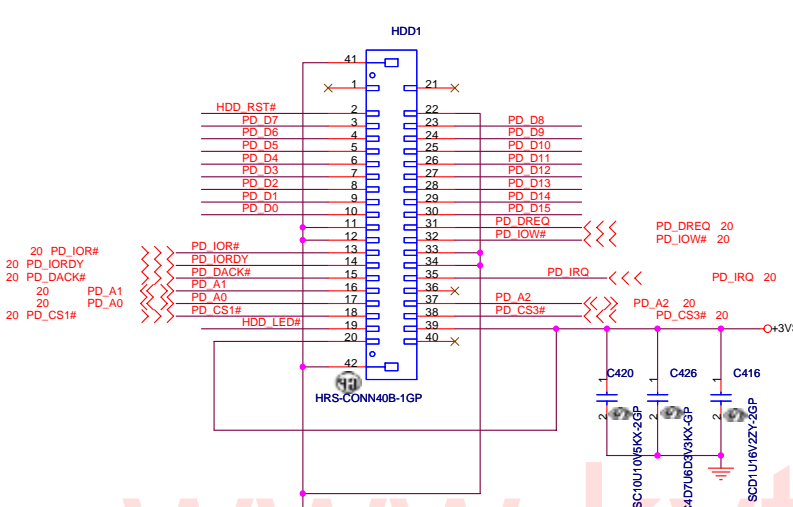
Date: Friday, March 30, 2007 Sheet: 21 of 51



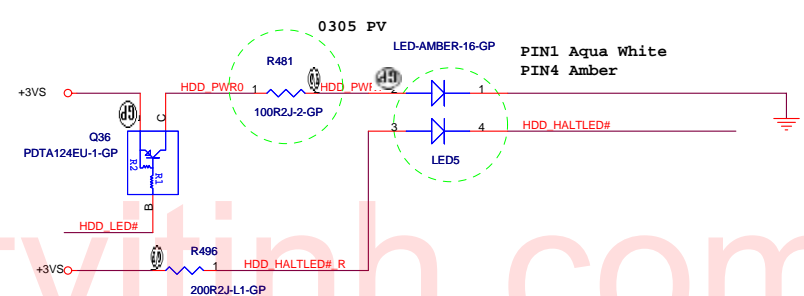
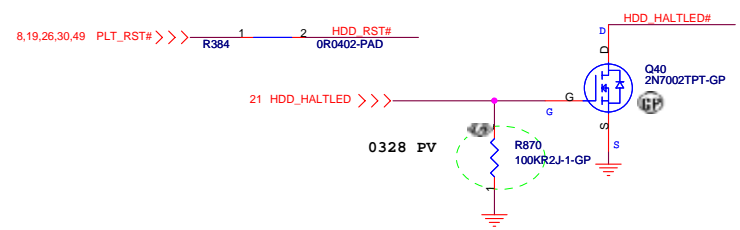
US2F 6 DF 6

A23	VSS	K7
A5	VSS	L1
AA2	VSS	L13
AA7	VSS	L15
A25	VSS	L26
AB1	VSS	L27
AB24	VSS	L4
AC11	VSS	L5
AC14	VSS	M12
AC25	VSS	M13
AC26	VSS	M14
AC27	VSS	M15
AD17	VSS	M16
AD20	VSS	M17
AD28	VSS	M23
AD29	VSS	M28
AD3	VSS	M29
AD4	VSS	M3
AD6	VSS	M3
AE1	VSS	N1
AE12	VSS	N12
AE2	VSS	N13
AE22	VSS	N14
AD1	VSS	N15
AE25	VSS	N16
AE9	VSS	N6
AE5	VSS	N7
AE6	VSS	N18
AF5	VSS	N6
AF14	VSS	N7
AF16	VSS	N4
AF18	VSS	N5
AE3	VSS	N6
AF4	VSS	N12
AGE	VSS	N13
AGR	VSS	P14
AH10	VSS	P15
AH13	VSS	P16
AH16	VSS	P17
AH19	VSS	P23
AH2	VSS	P28
AF28	VSS	P29
AH22	VSS	R11
AH24	VSS	R12
AH26	VSS	R13
AE29	VSS	R14
AH4	VSS	R15
AH8	VSS	R16
AE5	VSS	R17
B11	VSS	R18
B12	VSS	R29
B17	VSS	R4
B2	VSS	T12
B30	VSS	T13
B22	VSS	T14
B8	VSS	T15
C24	VSS	T16
C26	VSS	T17
C27	VSS	T12
D6	VSS	T12
D12	VSS	T13
D15	VSS	T14
D18	VSS	T15
D2	VSS	T16
D4	VSS	T17
E21	VSS	U23
E24	VSS	U26
E4	VSS	U27
E9	VSS	U5
F15	VSS	U6
F23	VSS	U13
F28	VSS	U15
F29	VSS	U28
F7	VSS	U29
G1	VSS	W2
G2	VSS	W26
G10	VSS	W27
G13	VSS	Y28
G19	VSS	Y29
G23	VSS	Y4
G25	VSS	Y8
G26	VSS	AB4
G27	VSS	AB5
H25	VSS	AB6
H28	VSS	AD5
H29	VSS	U4
H5	VSS	W4
J1	VSS_NCTF	A1 ICHGND1 1
J26	VSS_NCTF	A2 ICHGND1 1
J28	VSS_NCTF	A28 ICHGND1 1
J7	VSS_NCTF	A28 ICHGND1 1
J5	VSS_NCTF	A1 ICHGND3 1
K28	VSS_NCTF	A1 ICHGND3 1
K29	VSS_NCTF	A1 ICHGND3 1
K3	VSS_NCTF	A20 ICHGND4 1
K6	VSS_NCTF	B1 ICHGND4 1
B29	VSS_NCTF	B29 ICHGND4 1
A1	ICHGND1 1	0R2J-2-GP
A28	ICHGND1 1	0R2J-2-GP
A1	ICHGND3 1	0R2J-2-GP
A11	ICHGND3 1	0R2J-2-GP
A20	ICHGND4 1	0R2J-2-GP
B1	ICHGND4 1	0R2J-2-GP
B29	ICHGND4 1	0R2J-2-GP
A28	ICHGND1 1	0R2J-2-GP
A28	ICHGND1 1	0R2J-2-GP
A1	ICHGND3 1	0R2J-2-GP
A11	ICHGND3 1	0R2J-2-GP
A20	ICHGND4 1	0R2J-2-GP
B1	ICHGND4 1	0R2J-2-GP
B29	ICHGND4 1	0R2J-2-GP
A1	ICHGND1 1	0R2J-2-GP
A28	ICHGND1 1	0R2J-2-GP
A1	ICHGND3 1	0R2J-2-GP
A11	ICHGND3 1	0R2J-2-GP
A20	ICHGND4 1	0R2J-2-GP
B1	ICHGND4 1	0R2J-2-GP
B29	ICHGND4 1	0R2J-2-GP
A1	ICHGND1 1	0R2J-2-GP
A28	ICHGND1 1	0R2J-2-GP
A1	ICHGND3 1	0R2J-2-GP
A11	ICHGND3 1	0R2J-2-GP
A20	ICHGND4 1	0R2J-2-GP
B1	ICHGND4 1	0R2J-2-GP
B29	ICHGND4 1	0R2J-2-GP
A1	ICHGND1 1	0R2J-2-GP
A28	ICHGND1 1	0R2J-2-GP
A1	ICHGND3 1	0R2J-2-GP
A11	ICHGND3 1	0R2J-2-GP
A20	ICHGND4 1	0R2J-2-GP
B1	ICHGND4 1	0R2J-2-GP
B29	ICHGND4 1	0R2J-2-GP
A1	ICHGND1 1	0R2J-2-GP
A28	ICHGND1 1	0R2J-2-GP
A1	ICHGND3 1	0R2J-2-GP
A11	ICHGND3 1	0R2J-2-GP
A20	ICHGND4 1	0R2J-2-GP
B1	ICHGND4 1	0R2J-2-GP
B29	ICHGND4 1	0R2J-2-GP
A1	ICHGND1 1	0R2J-2-GP
A28	ICHGND1 1	0R2J-2-GP
A1	ICHGND3 1	0R2J-2-GP
A11	ICHGND3 1	0R2J-2-GP
A20	ICHGND4 1	0R2J-2-GP
B1	ICHGND4 1	0R2J-2-GP
B29	ICHGND4 1	0R2J-2-GP
A1	ICHGND1 1	0R2J-2-GP
A28	ICHGND1 1	0R2J-2-GP
A1	ICHGND3 1	0R2J-2-GP
A11	ICHGND3 1	0R2J-2-GP
A20	ICHGND4 1	0R2J-2-GP
B1	ICHGND4 1	0R2J-2-GP
B29	ICHGND4 1	0R2J-2-GP
A1	ICHGND1 1	0R2J-2-GP
A28	ICHGND1 1	0R2J-2-GP
A1	ICHGND3 1	0R2J-2-GP
A11	ICHGND3 1	0R2J-2-GP
A20	ICHGND4 1	0R2J-2-GP
B1	ICHGND4 1	0R2J-2-GP
B29	ICHGND4 1	0R2J-2-GP
A1	ICHGND1 1	0R2J-2-GP
A28	ICHGND1 1	0R2J-2-GP
A1	ICHGND3 1	0R2J-2-GP
A11	ICHGND3 1	0R2J-2-GP
A20	ICHGND4 1	0R2J-2-GP
B1	ICHGND4 1	0R2J-2-GP
B29	ICHGND4 1	0R2J-2-GP
A1	ICHGND1 1	0R2J-2-GP
A28	ICHGND1 1	0R2J-2-GP
A1	ICHGND3 1	0R2J-2-GP
A11	ICHGND3 1	0R2J-2-GP
A20	ICHGND4 1	0R2J-2-GP
B1	ICHGND4 1	0R2J-2-GP
B29	ICHGND4 1	0R2J-2-GP
A1	ICHGND1 1	0R2J-2-GP
A28	ICHGND1 1	0R2J-2-GP
A1	ICHGND3 1	0R2J-2-GP
A11	ICHGND3 1	0R2J-2-GP
A20	ICHGND4 1	0R2J-2-GP
B1	ICHGND4 1	0R2J-2-GP
B29	ICHGND4 1	0R2J-2-GP
A1	ICHGND1 1	0R2J-2-GP
A28	ICHGND1 1	0R2J-2-GP
A1	ICHGND3 1	0R2J-2-GP
A11	ICHGND3 1	0R2J-2-GP
A20	ICHGND4 1	0R2J-2-GP
B1	ICHGND4 1	0R2J-2-GP
B29	ICHGND4 1	0R2J-2-GP
A1	ICHGND1 1	0R2J-2-GP
A28	ICHGND1 1	0R2J-2-GP
A1	ICHGND3 1	0R2J-2-GP
A11	ICHGND3 1	0R2J-2-GP
A20	ICHGND4 1	0R2J-2-GP
B1	ICHGND4 1	0R2J-2-GP
B29	ICHGND4 1	0R2J-2-GP
A1	ICHGND1 1	0R2J-2-GP
A28	ICHGND1 1	0R2J-2-GP
A1	ICHGND3 1	0R2J-2-GP
A11	ICHGND3 1	0R2J-2-GP
A20	ICHGND4 1	0R2J-2-GP
B1	ICHGND4 1	0R2J-2-GP
B29	ICHGND4 1	0R2J-2-GP
A1	ICHGND1 1	0R2J-2-GP
A28	ICHGND1 1	0R2J-2-GP
A1	ICHGND3 1	0R2J-2-GP
A11	ICHGND3 1	0R2J-2-GP
A20	ICHGND4 1	0R2J-2-GP
B1	ICHGND4 1	0R2J-2-GP
B29	ICHGND4 1	0R2J-2-GP
A1	ICHGND1 1	0R2J-2-GP
A28	ICHGND1 1	0R2J-2-GP
A1	ICHGND3 1	0R2J-2-GP
A11	ICHGND3 1	0R2J-2-GP
A20	ICHGND4 1	0R2J-2-GP
B1	ICHGND4 1	0R2J-2-GP
B29	ICHGND4 1	0R2J-2-GP

# BTB PATA HDD

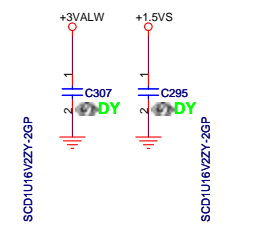


20 PD\_D[0..15] <<< >>>

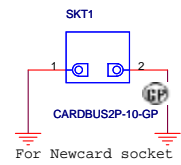
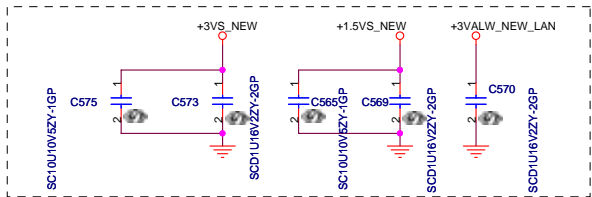


www.kythuatinh.com

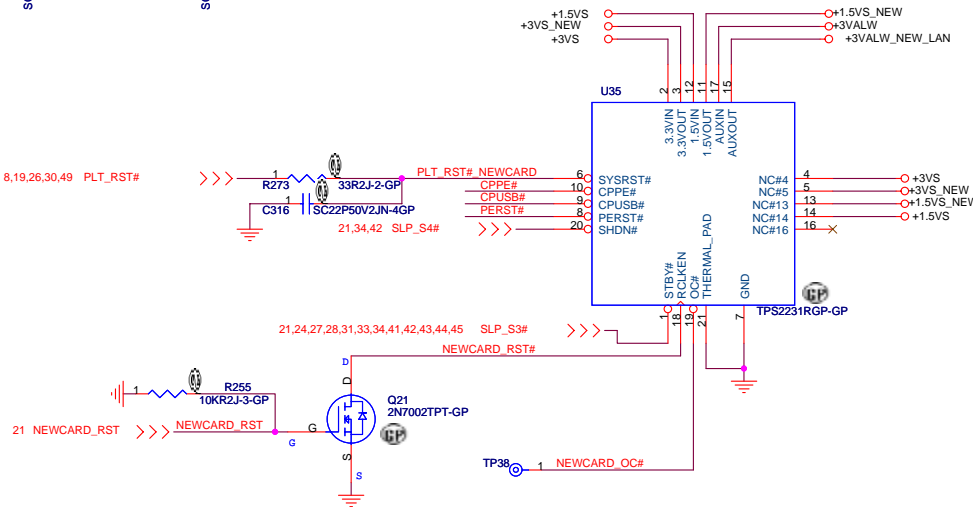
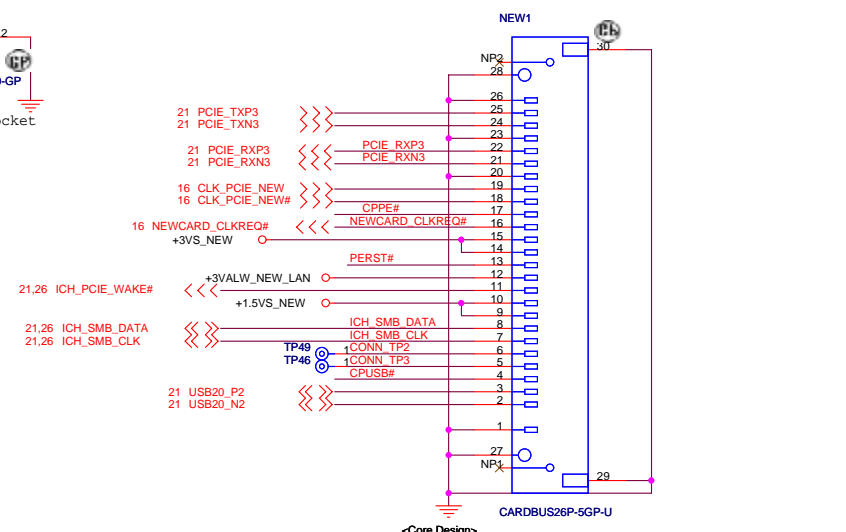
Place them Near to Chip



Place them Near to Connector



## NEWCARD Connector

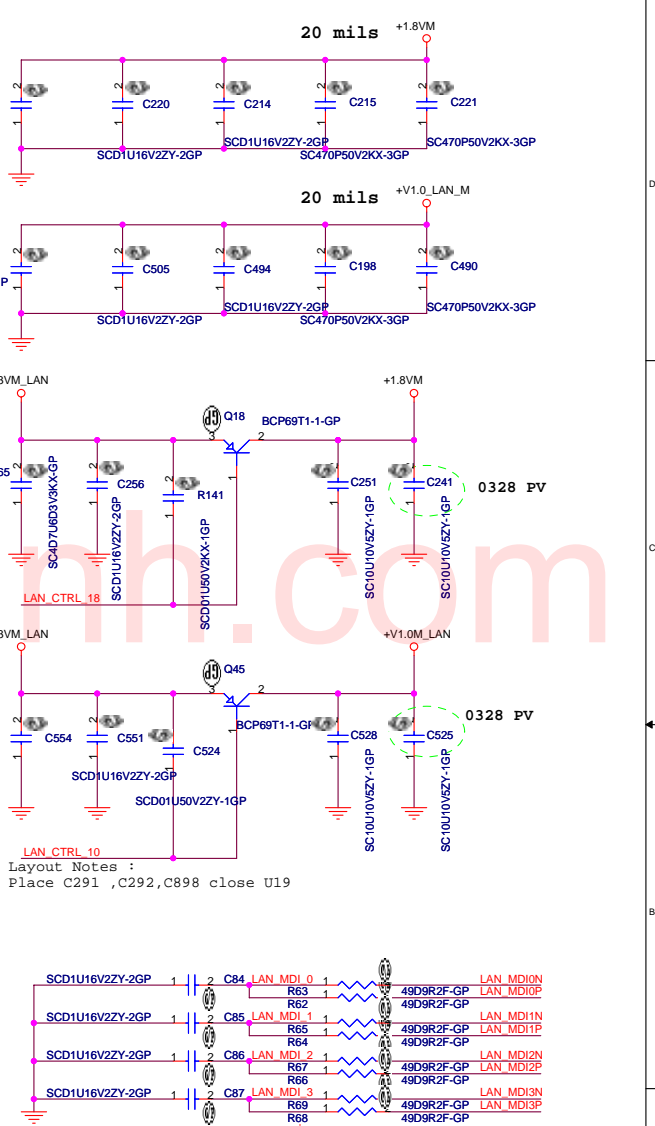
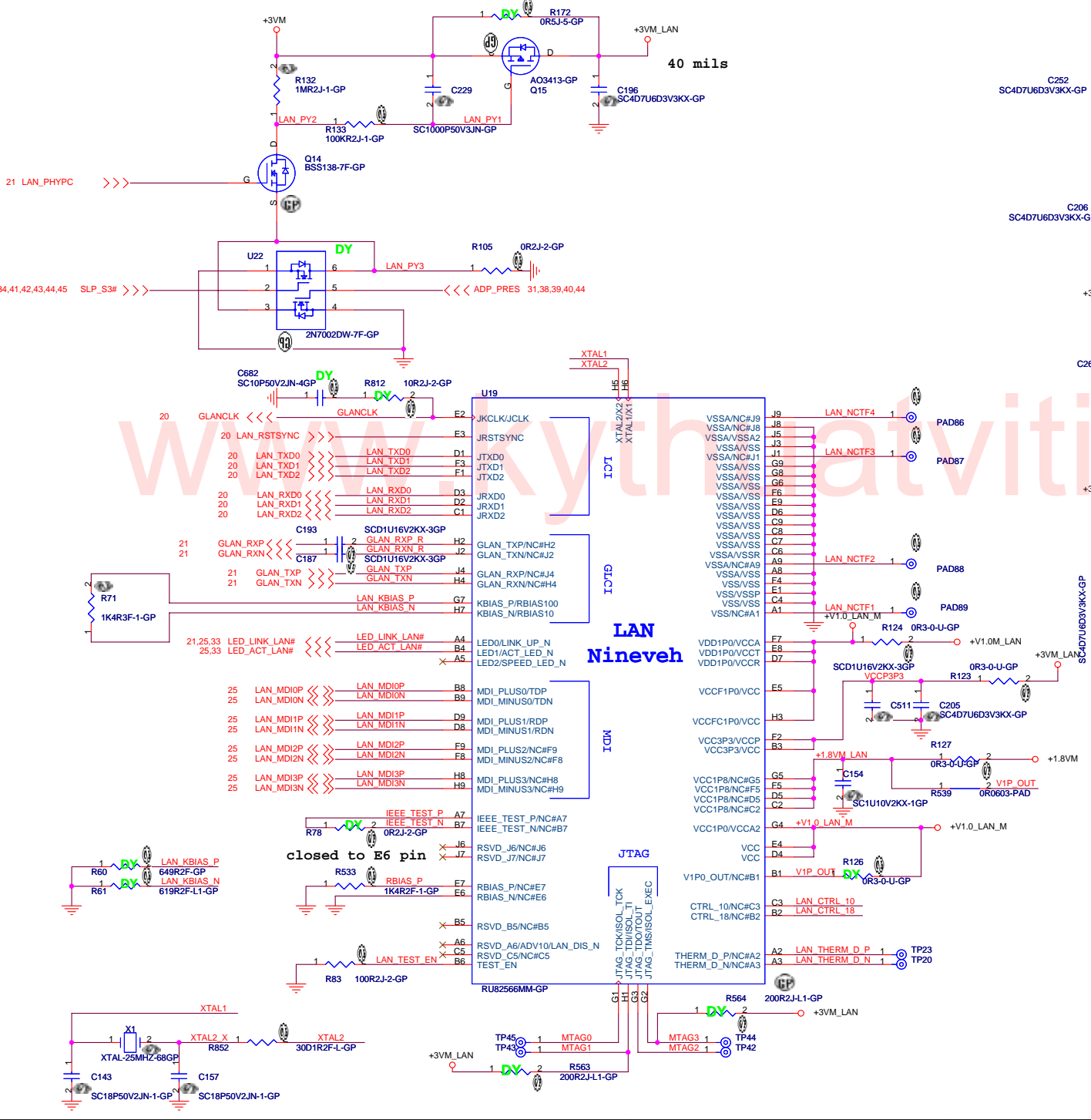


<Core Design>

**緯創資通 Wistron Corporation**  
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichin, Taipei Hsein 221, Taiwan, R.O.C.

Title	<b>HDD /NEW CARD CONN.</b>		
Size A3	Document Number	<b>NORN</b>	Rev <b>PV</b>
Date: Friday, March 30, 2007	Sheet 23	of	51





Layout Notice : Place termination as close as Intel 82566 as possible

<Core Design>

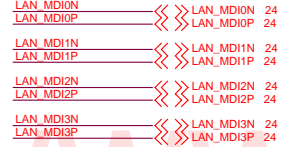
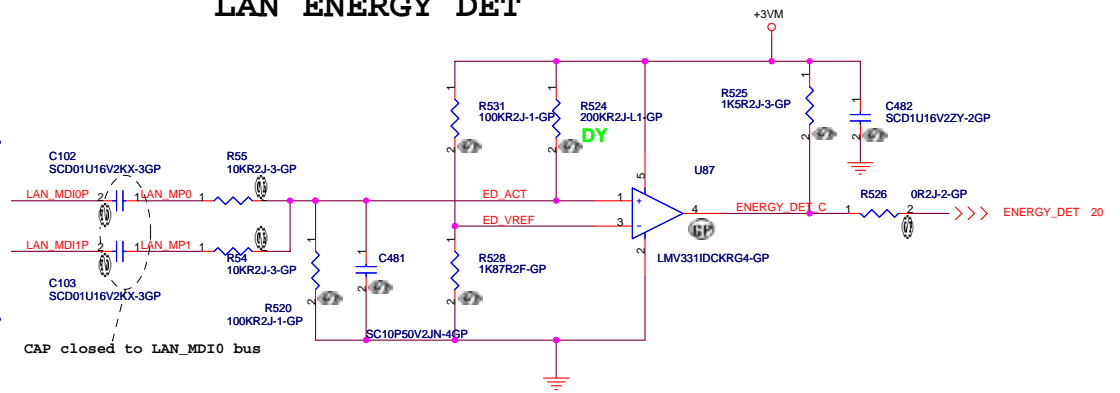
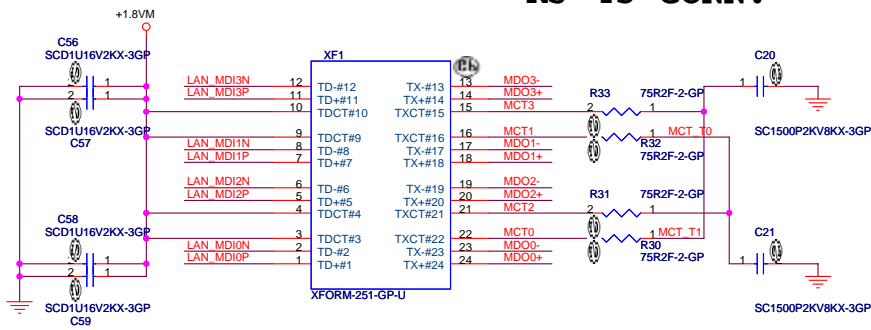
**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title			<b>Intel 82566 Nineveh</b>		
Size	Document Number				Rev
A3	Norn				PV
Date:	Friday, March 30, 2007	Sheet	24	of	51

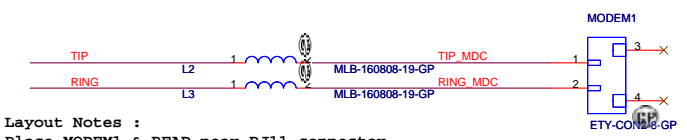
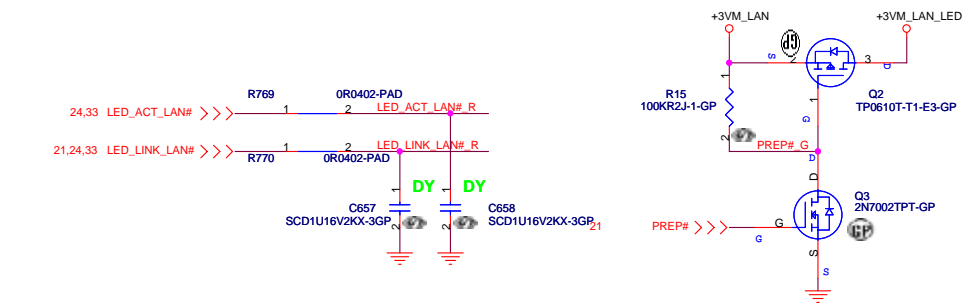
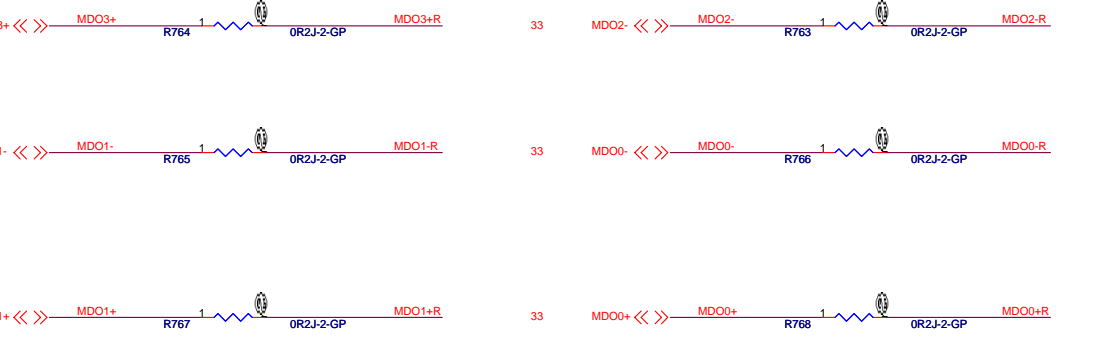
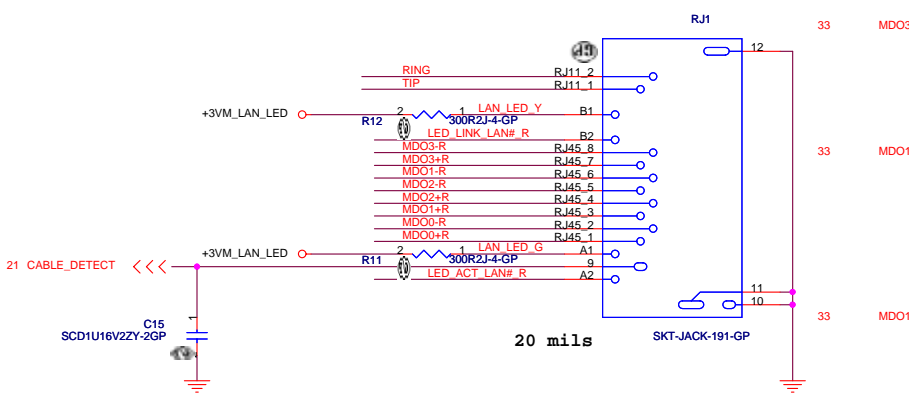


# RJ-45 CONN.

# LAN ENERGY DET



Note : MDO[3..0]+- signals should route to RJ45 first then to DOCK CONN .



Layout Notes :  
Place MODEM1 & BEAD near RJ11 connector

<Core Design>

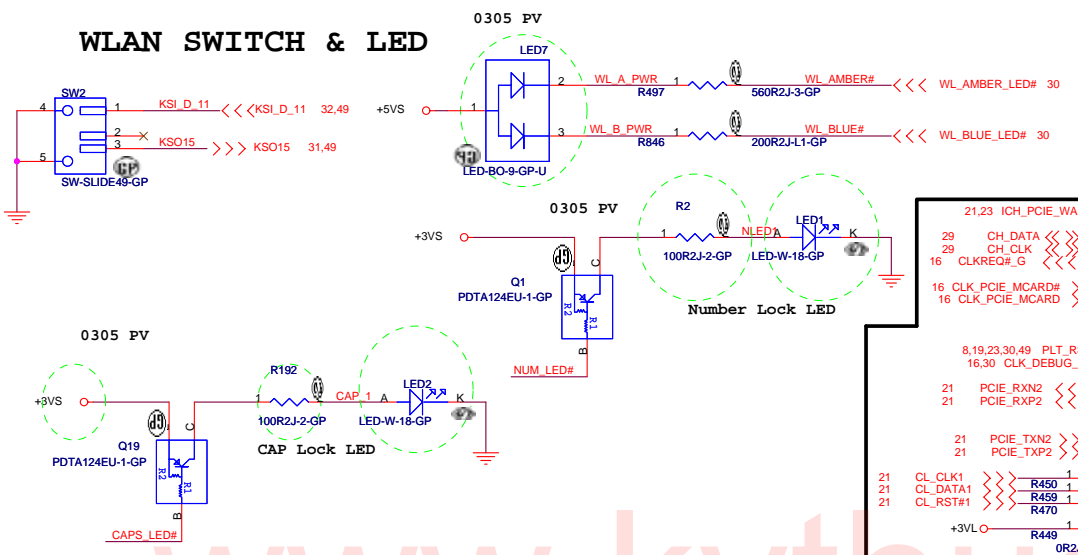
**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Magnetic & RJ45/RJ11**

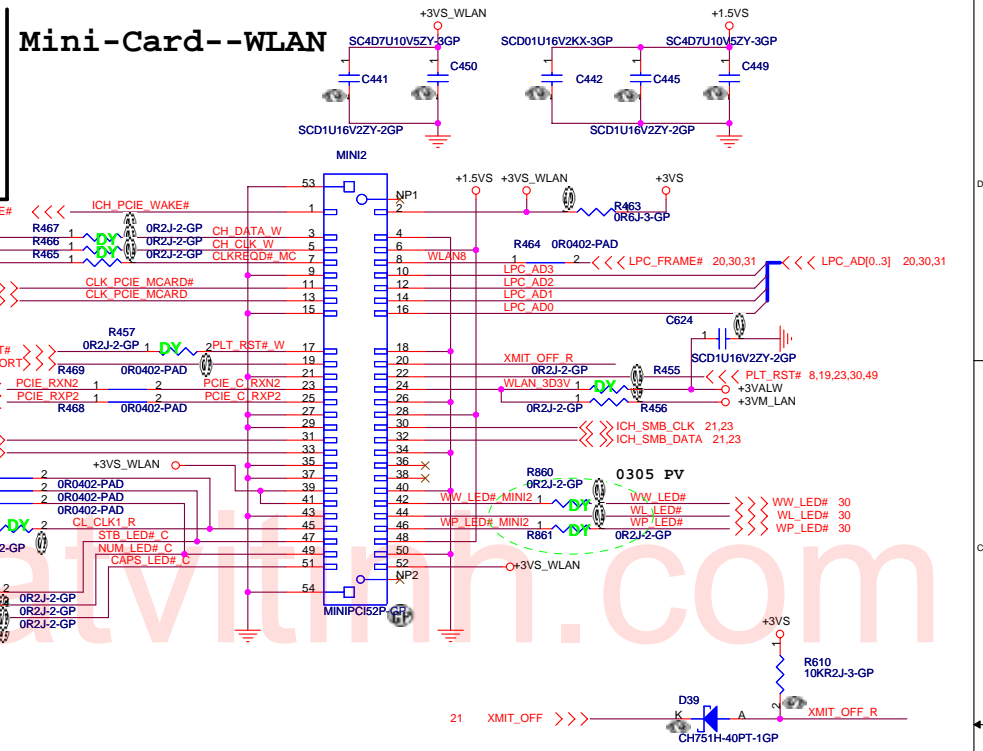
Size: A3 | Document Number: **Norn** | Rev: **PV**

Date: Friday, March 30, 2007 | Sheet: 25 of 51

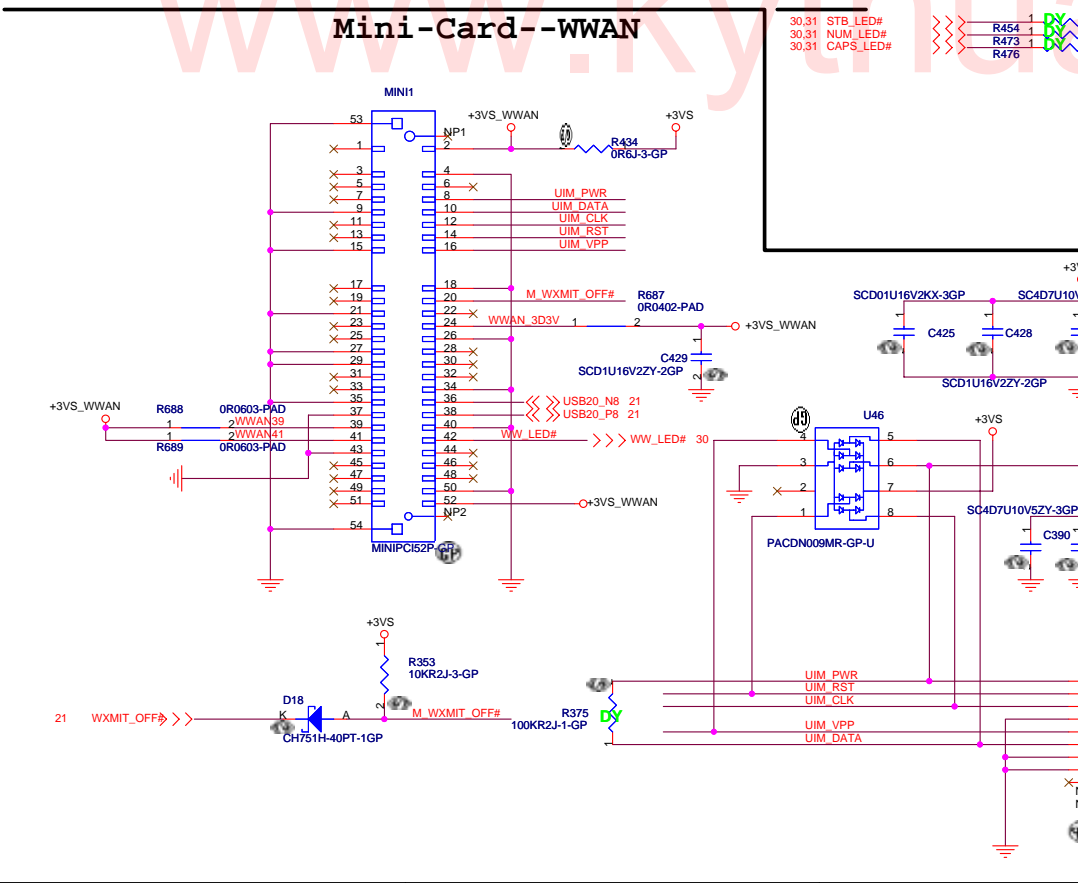
# WLAN SWITCH & LED



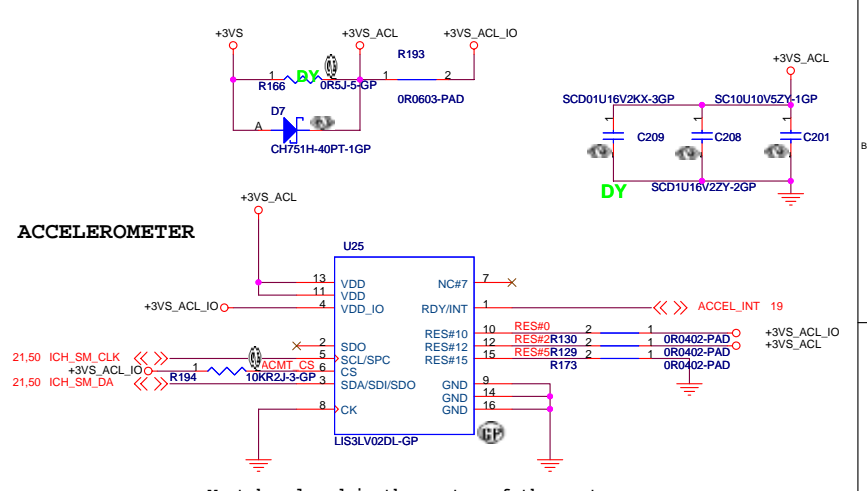
# Mini-Card--WLAN



# Mini-Card--WWAN

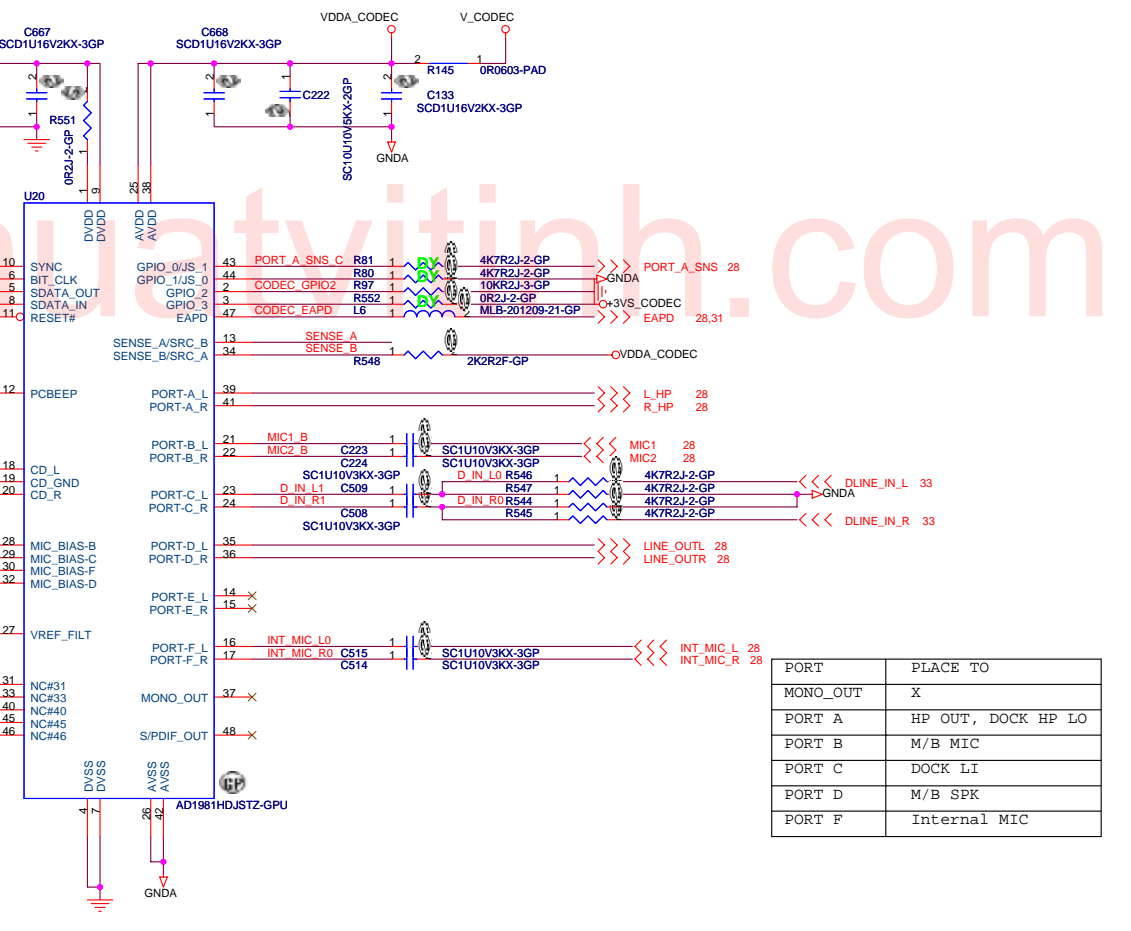
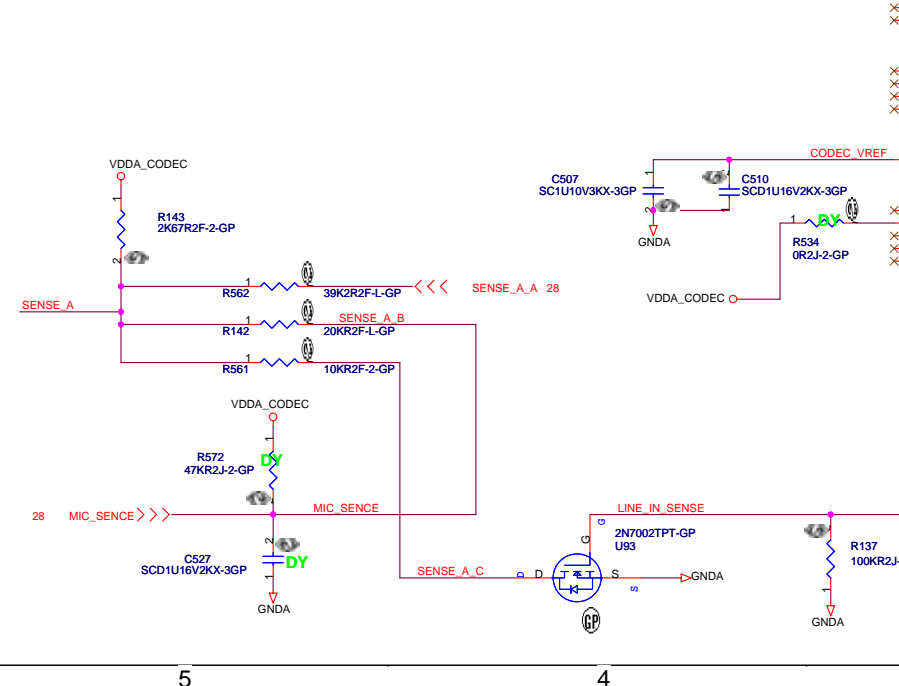
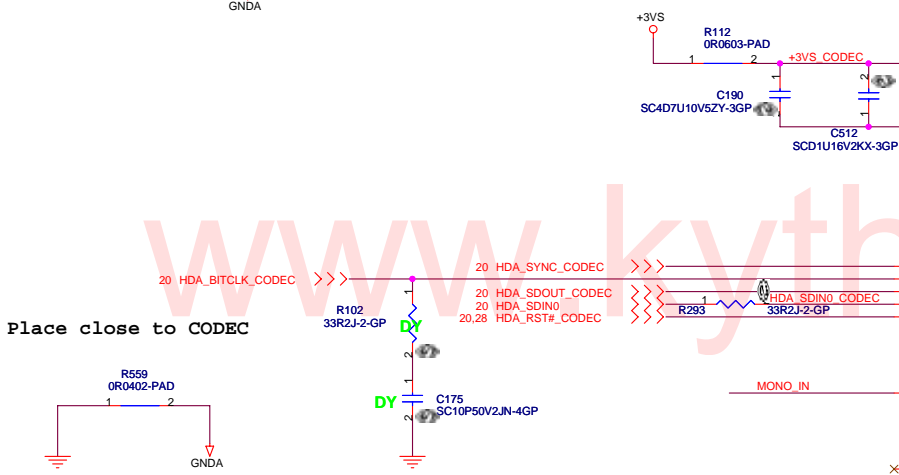
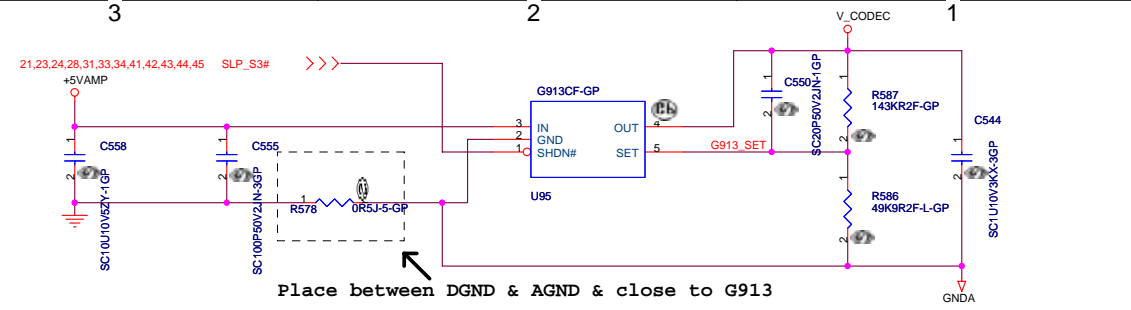
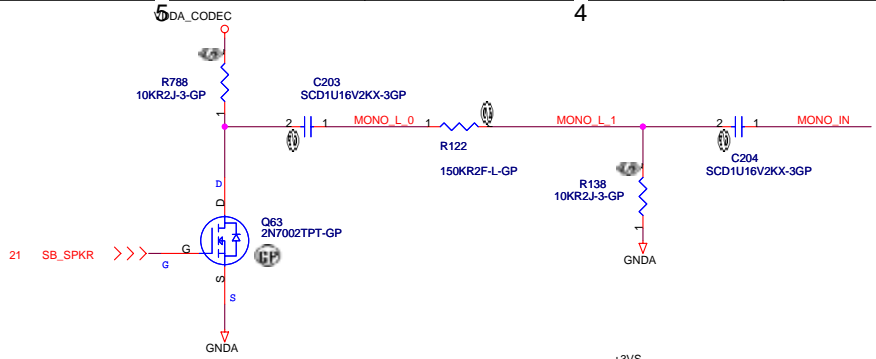


# ACCELEROMETER



緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	Mini-Card/Accelerometer	
Size A3	Document Number	Rev
	Norn	PV
Date: Friday, March 30, 2007	Sheet 26 of 51	



PORT	PLACE TO
MONO_OUT	X
PORT A	HP OUT, DOCK HP LO
PORT B	M/B MIC
PORT C	DOCK LI
PORT D	M/B SPK
PORT F	Internal MIC

<Core Design>

**緯創資通 Wistron Corporation**  
 21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichin, Taipei Hsein 221, Taiwan, R.O.C.

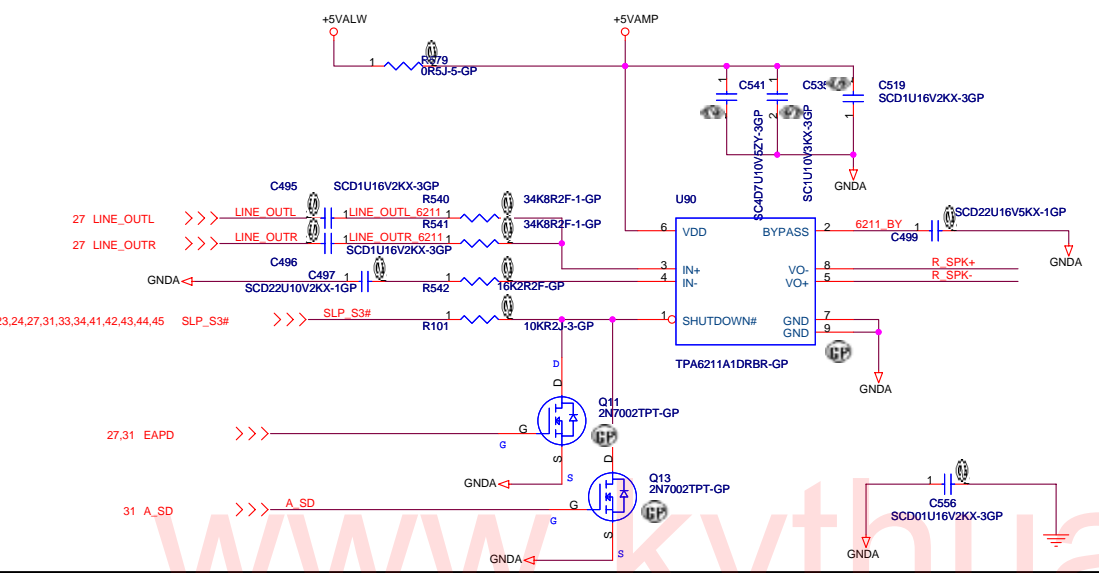
Title: **AC97 CODEC AD1981HD**

Size A3	Document Number	Rev PV
<b>NORN</b>		

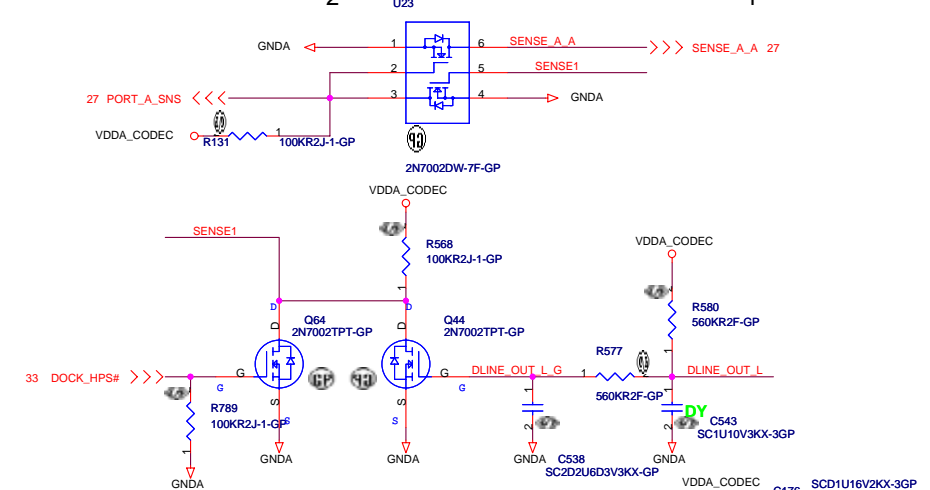
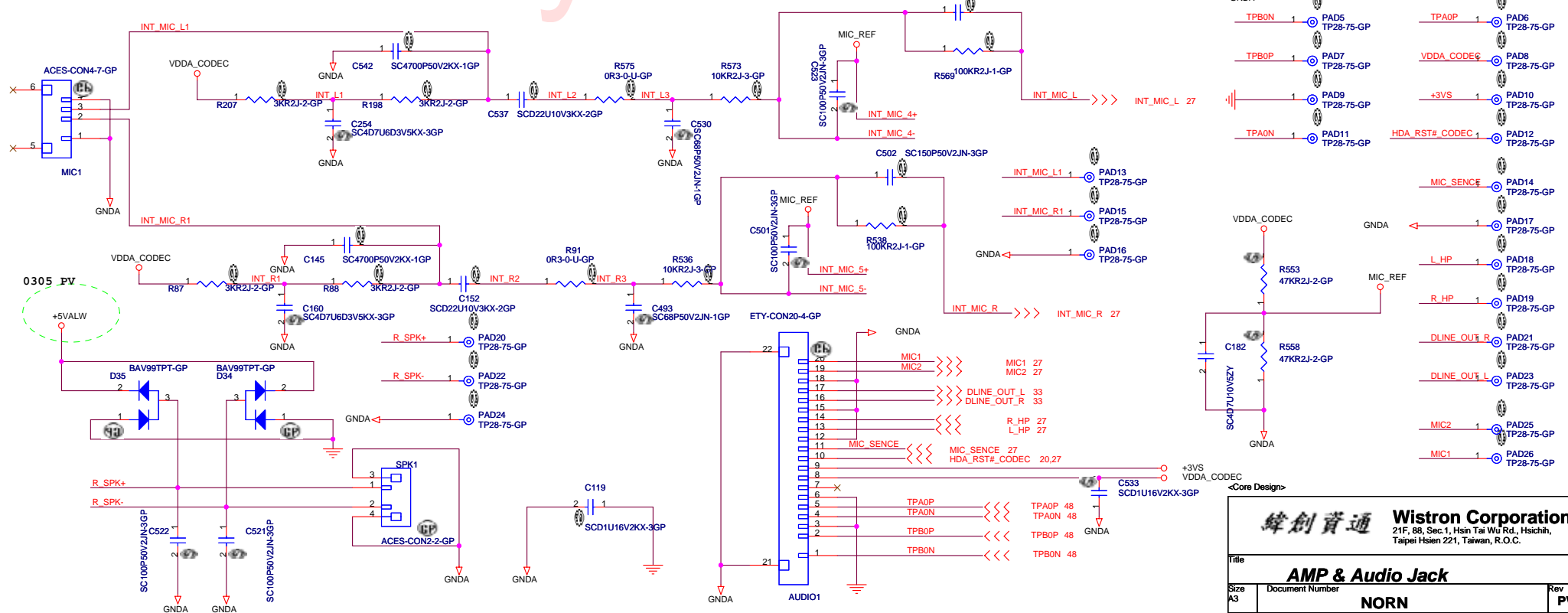
Date: Friday, March 30, 2007 Sheet 27 of 51

20,26,30,31 LPC\_FRAME# <<<<  
 8,19,23,26,30,49 PLT\_RST# <<<<

### AMP. FOR INTERNAL SPEAKER



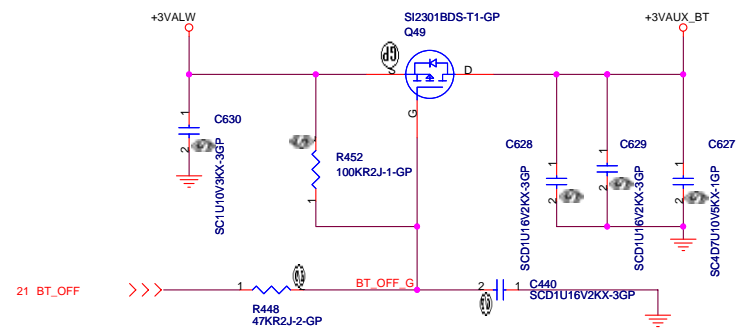
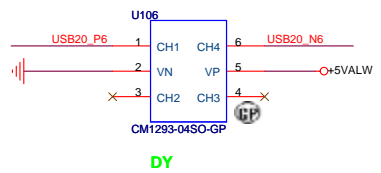
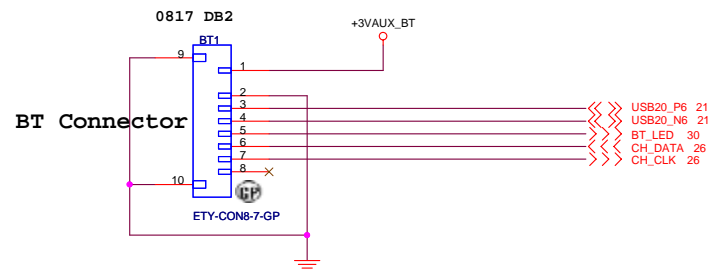
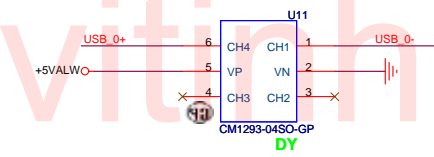
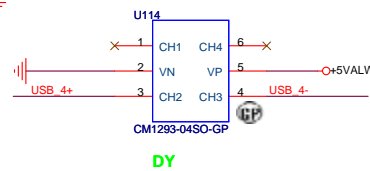
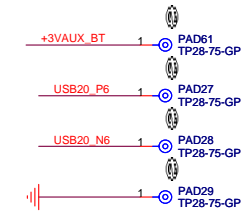
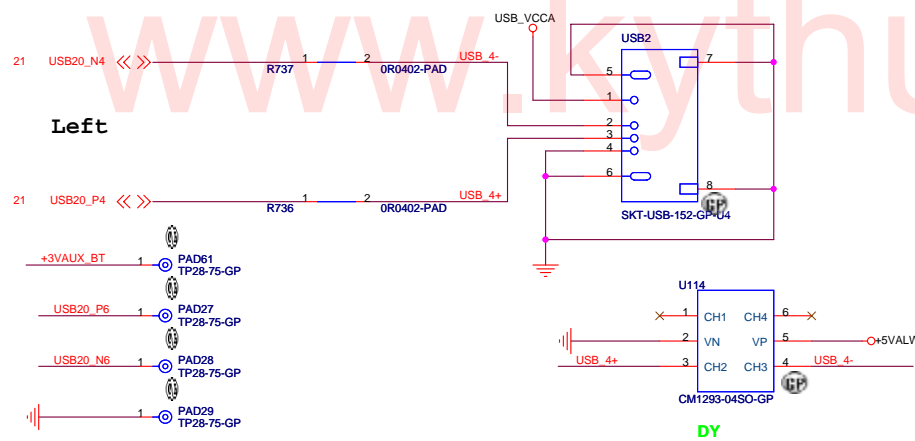
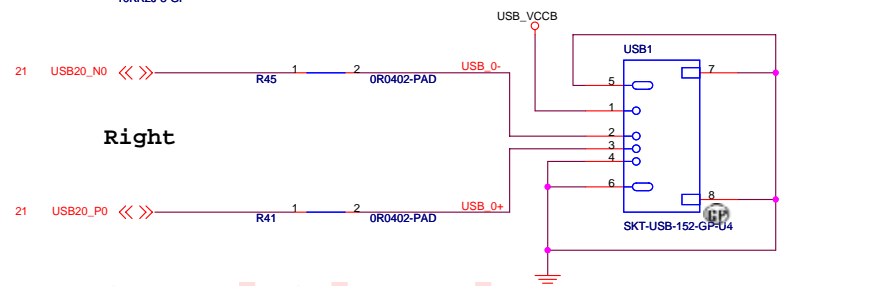
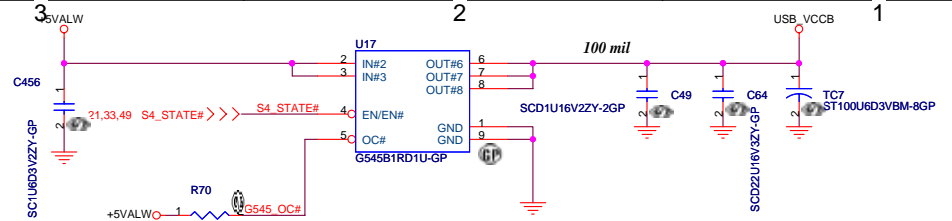
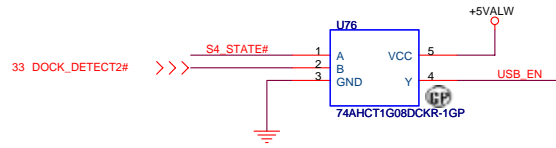
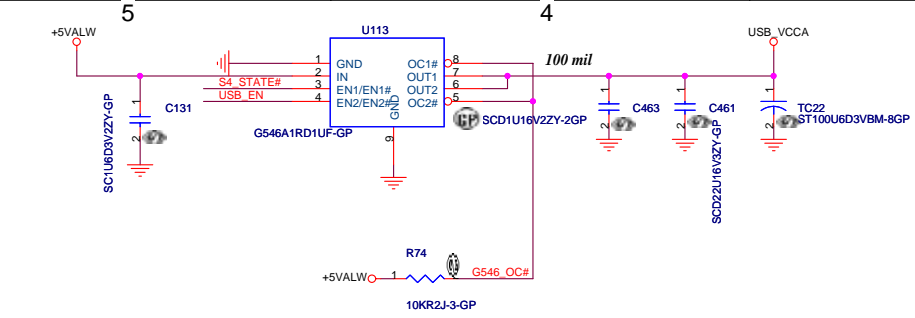
### AMP. FOR INTERNAL ARRAY MICROPHONE




**Wistron Corporation**  
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichin,  
 Taipei Hsin 221, Taiwan, R.O.C.

---

**AMP & Audio Jack**  
 Title: **NORN**  
 Size: A3    Document Number: **NORN**    Rev: **PV**  
 Date: Friday, March 30, 2007    Sheet 28 of 51



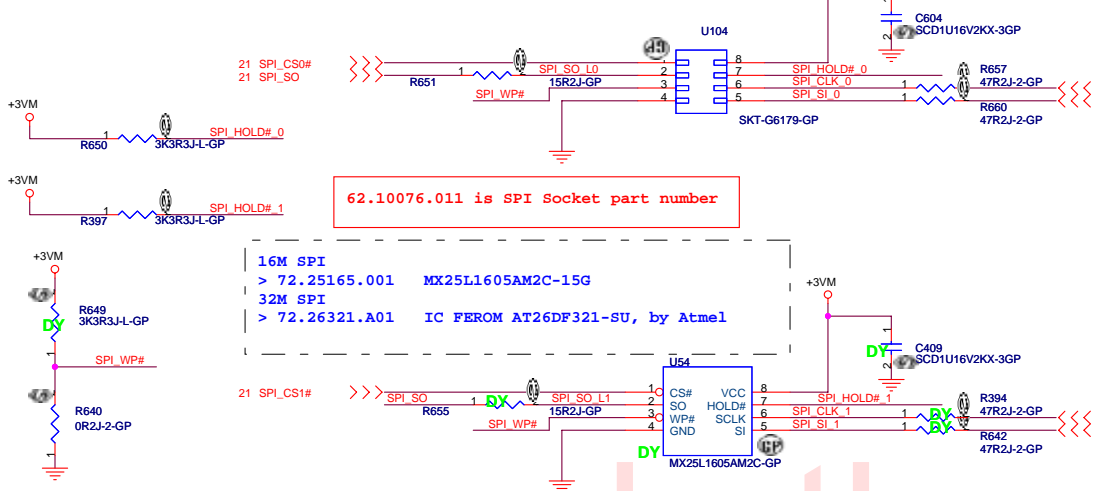
<Core Design>

**緯創資通 Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin,  
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB&1394 & BT Connector**

Size A3	Document Number	Rev PV
Date: Friday, March 30, 2007		Sheet 29 of 51

32Mb x 1

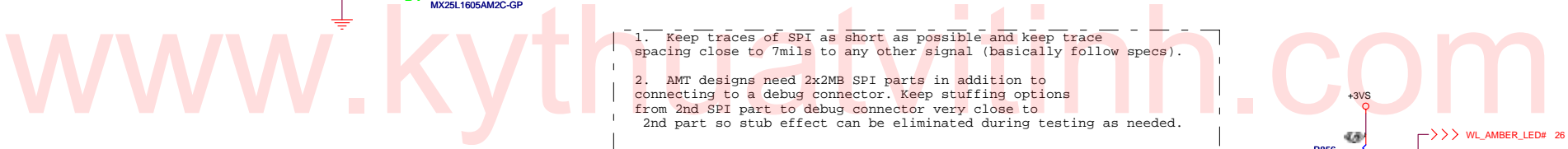
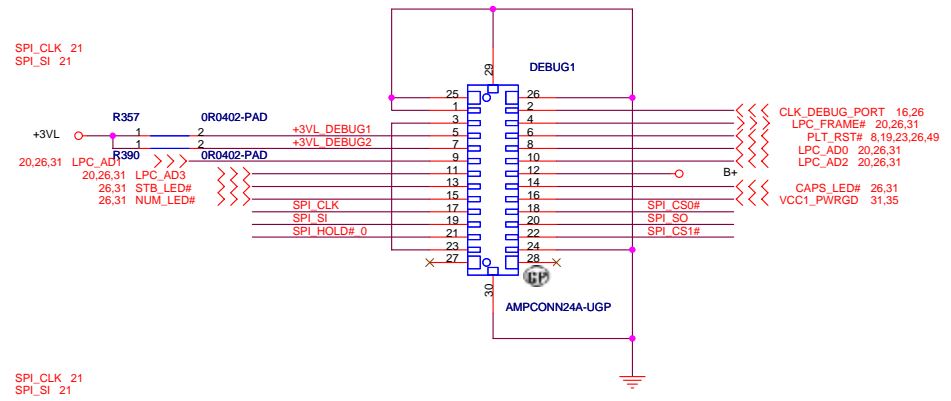


62.10076.011 is SPI Socket part number

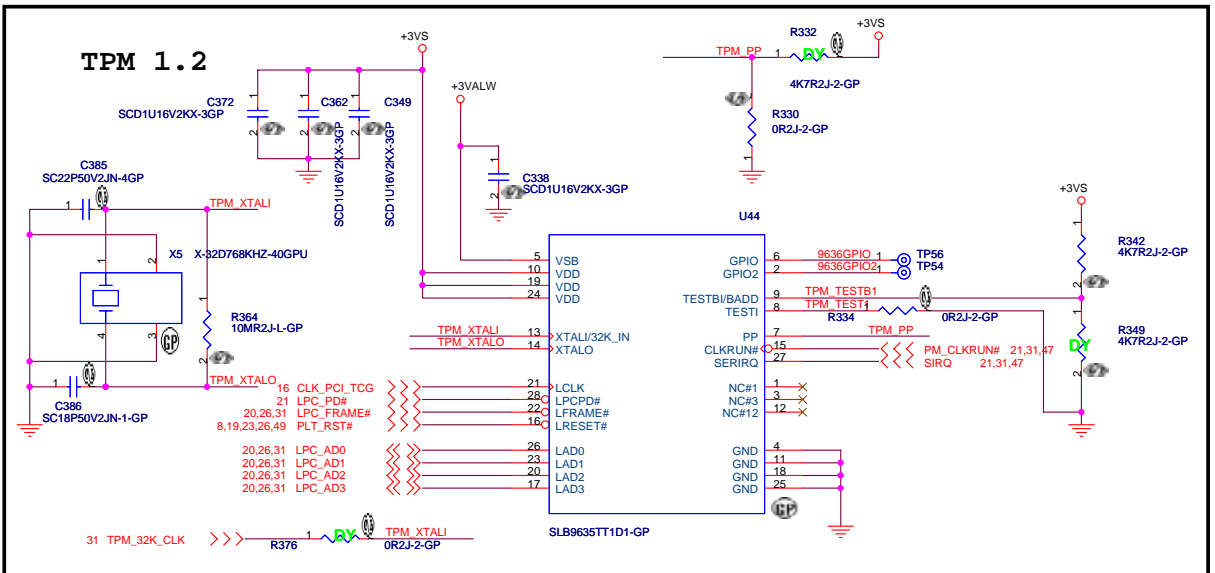
16M SPI  
 > 72.25165.001 MX25L1605AM2C-15G  
 32M SPI  
 > 72.26321.A01 IC FEROM AT26DF321-SU, by Atmel

1. Keep traces of SPI as short as possible and keep trace spacing close to 7mils to any other signal (basically follow specs).
2. AMT designs need 2x2MB SPI parts in addition to connecting to a debug connector. Keep stuffing options from 2nd SPI part to debug connector very close to 2nd part so stub effect can be eliminated during testing as needed.

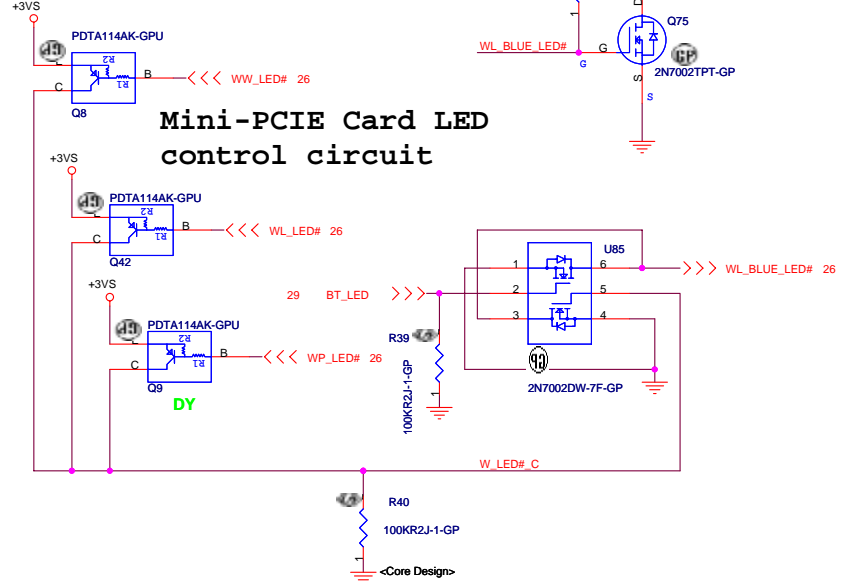
Debug port



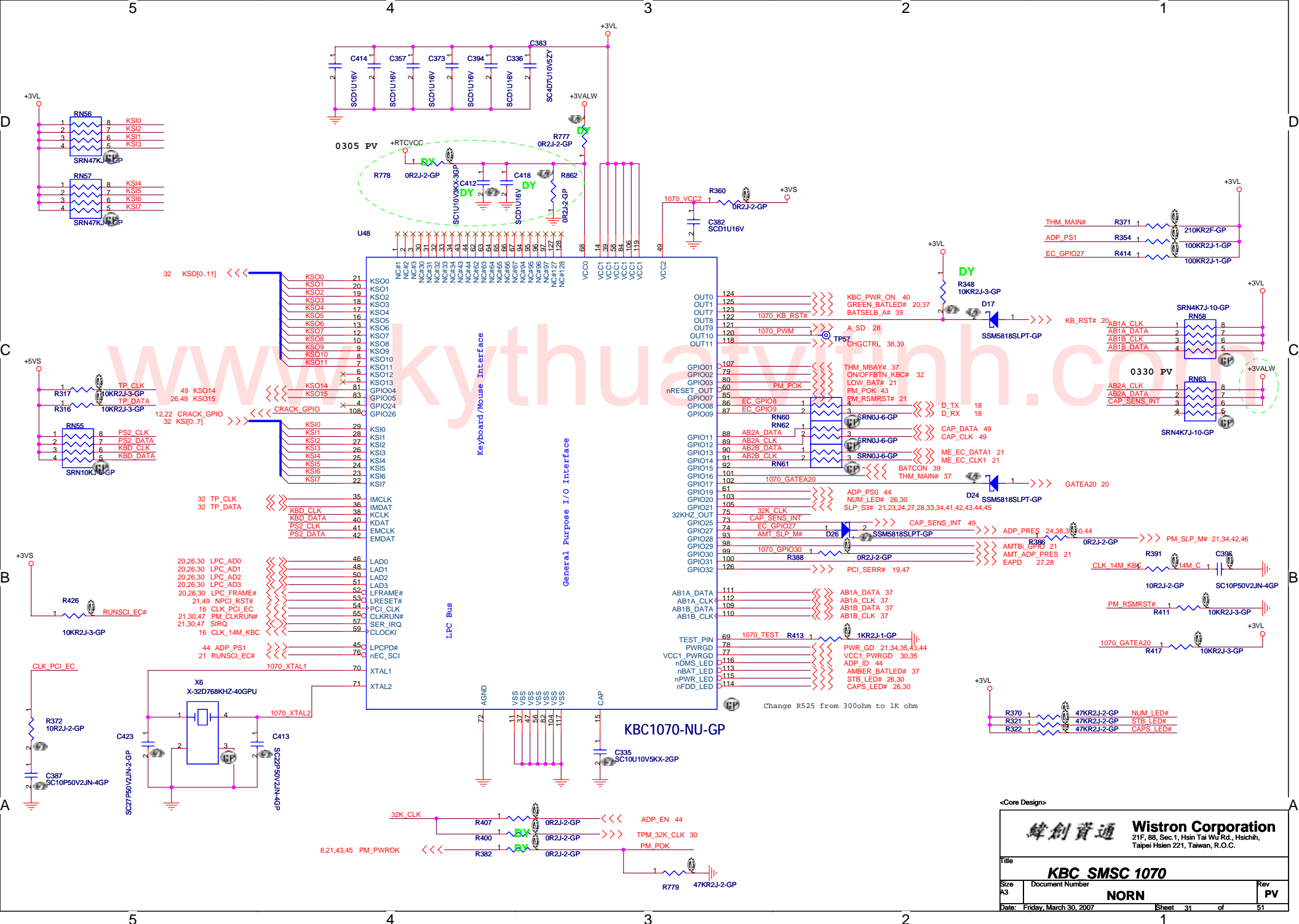
TPM 1.2



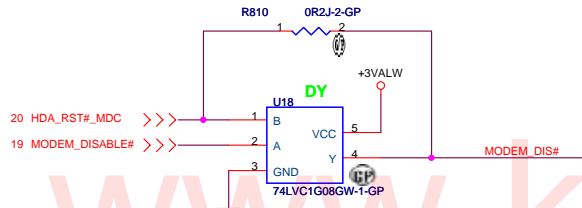
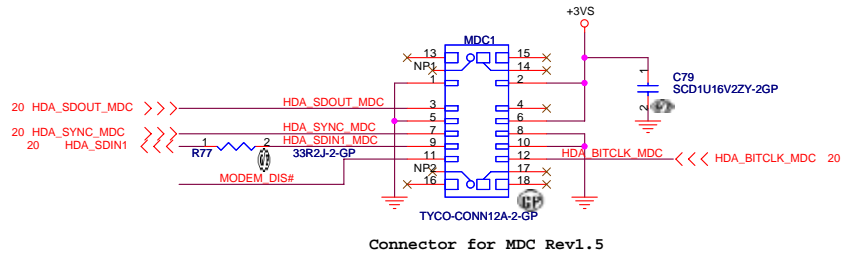
Mini-PCIE Card LED control circuit



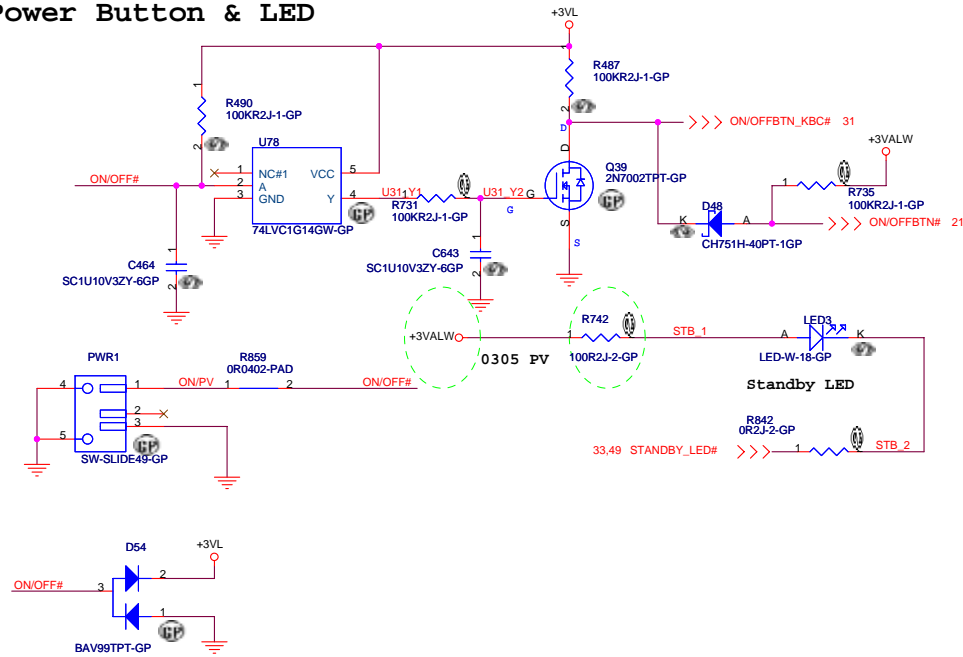
		<b>Wistron Corporation</b> 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>TPM/BIOS/24 DEBUG PORT</b>			
Size	Document Number		Rev
A3		<b>NORN</b>	<b>PV</b>
Date:	Friday, March 30, 2007	Sheet 30	of 51



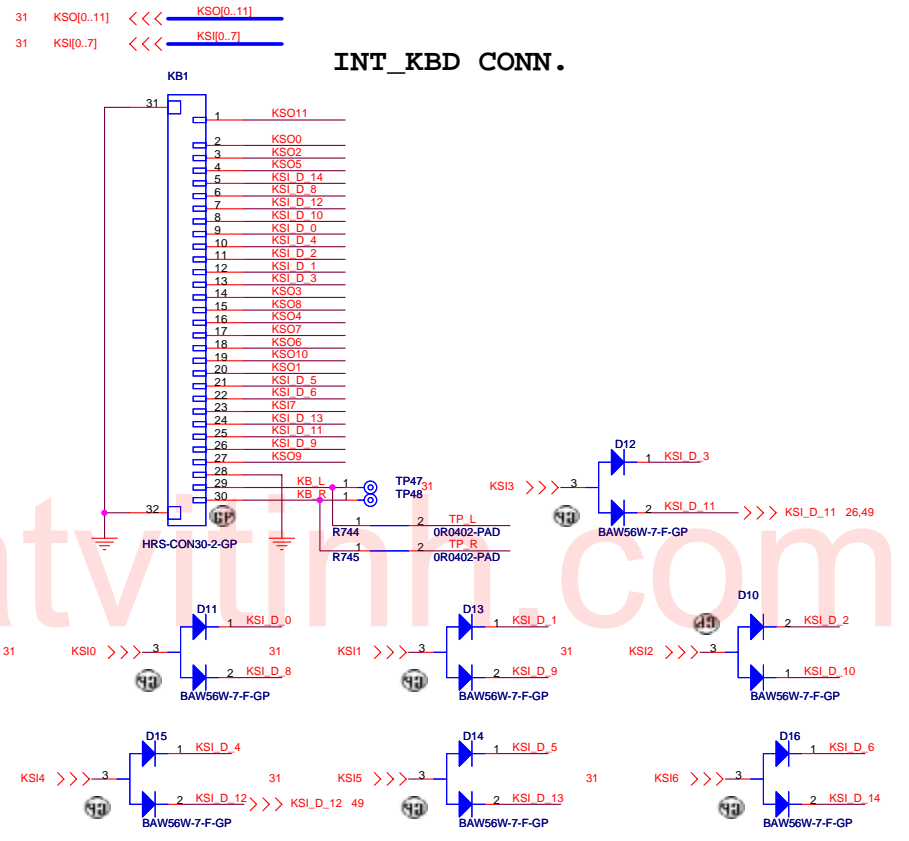
### MDC 1.5 Conn.



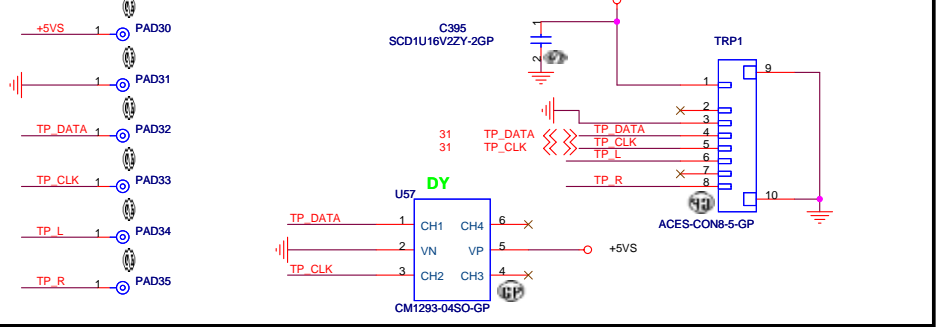
### Power Button & LED



### INT\_KBD CONN.



### TrackPoint CONN.



<Core Design>

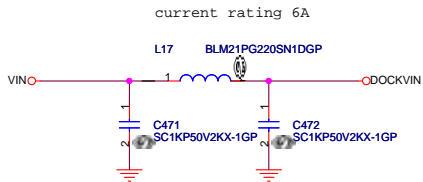
**緯創資通 Wistron Corporation**  
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **MDC/KBD/ON OFF/T.P.**

Size A3 Document Number: **Norn** Rev: **PV**

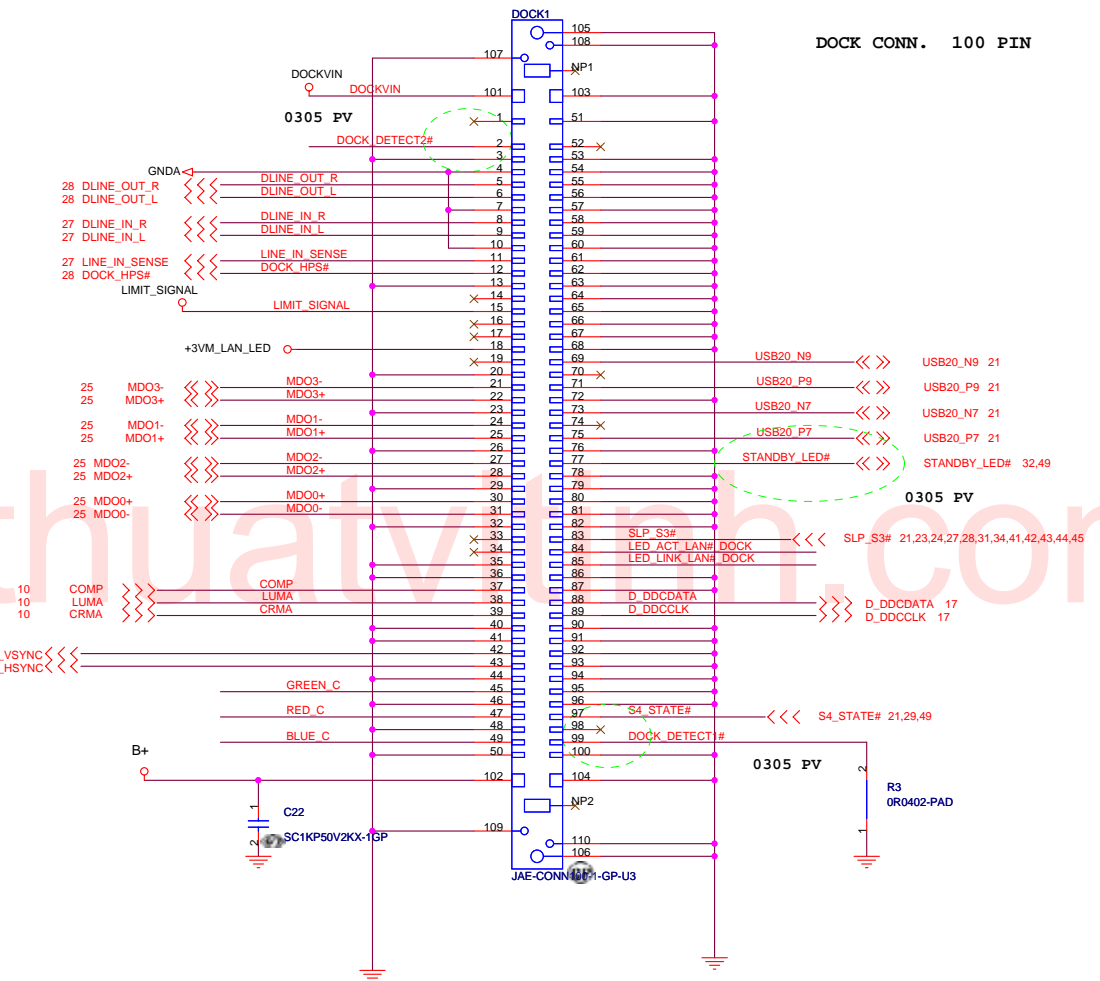
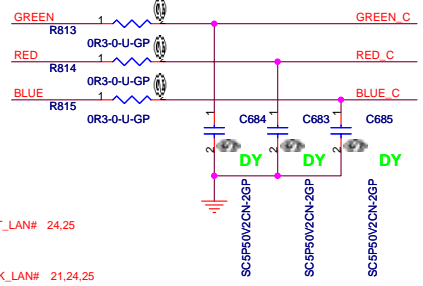
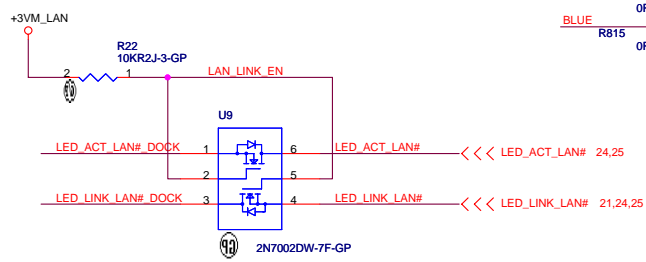
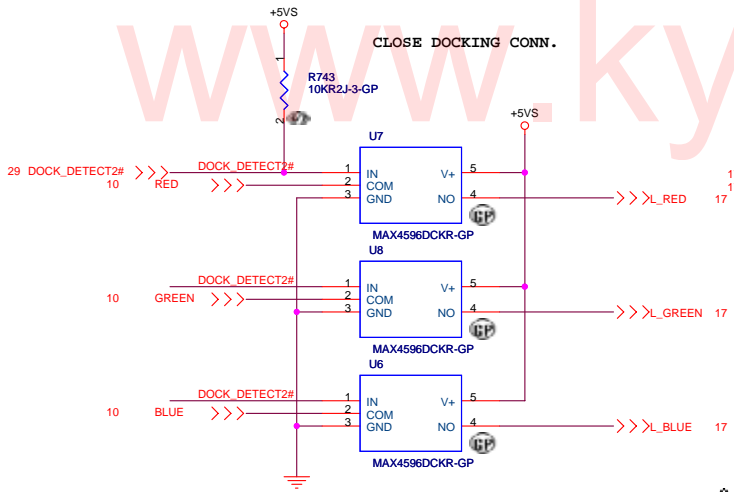
Date: Friday, March 30, 2007 Sheet 32 of 51



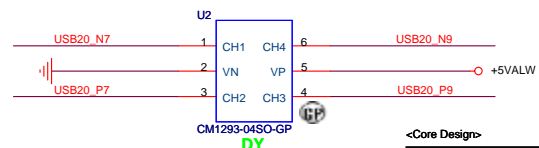


MAX4596

IN	NO TO COM COM TO NO
L	OFF
H	ON



**Power Pins**  
 2 sets  
 Set 1 = 18.5V @ 4A per contact  
 Set 2 = VBATR @ 3A per contact



<Core Design>

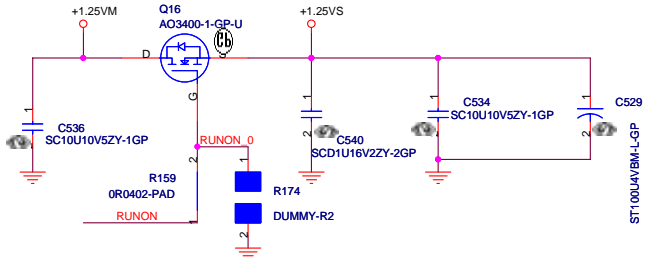
**緯創資通 Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **Docking CONN**

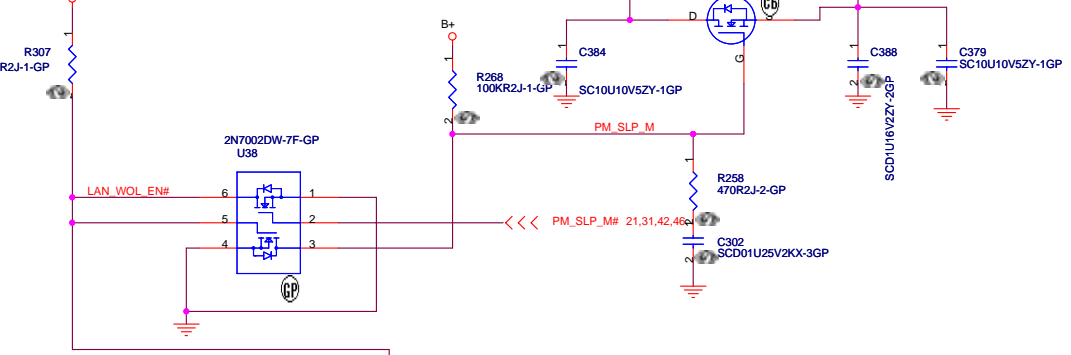
Size A3 Document Number: **Norn** Rev: **PV**

Date: Friday, March 30, 2007 Sheet 33 of 51

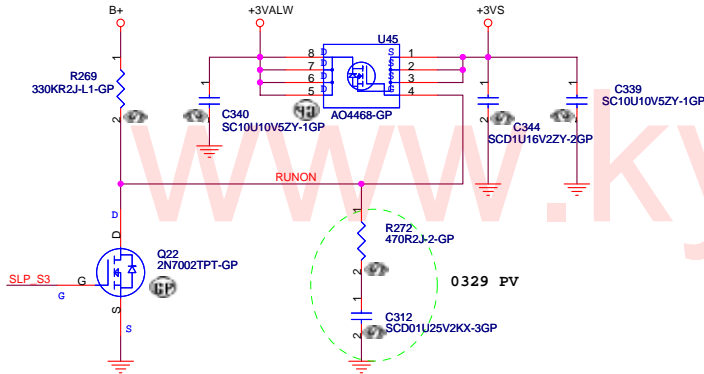
### +1.25VM to +1.25VS Transfer



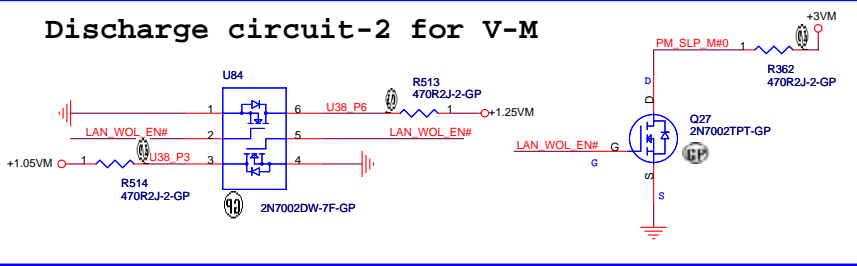
### +3VALW to +3VM Transfer



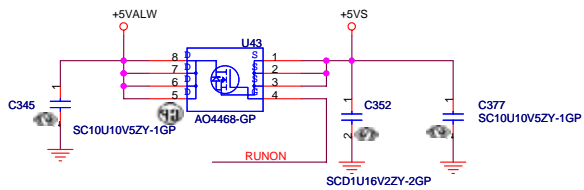
### +3VALW to +3VS Transfer



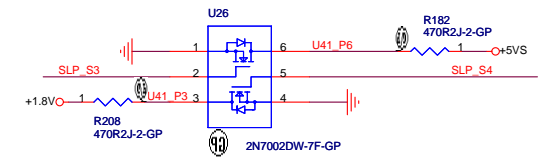
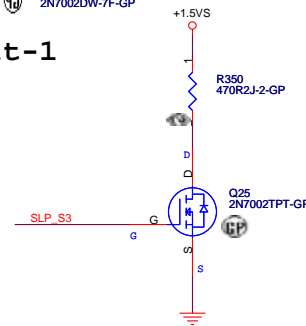
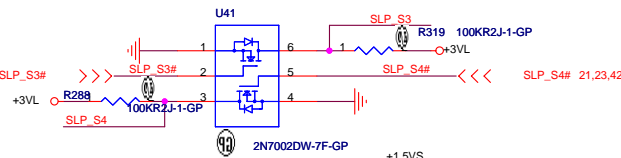
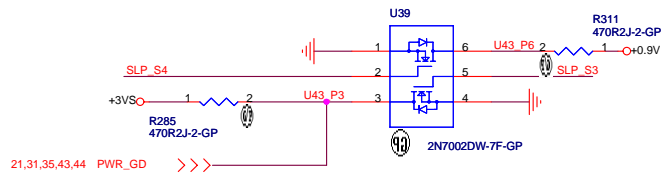
### Discharge circuit-2 for V-M



### +5VALW to +5VS Transfer



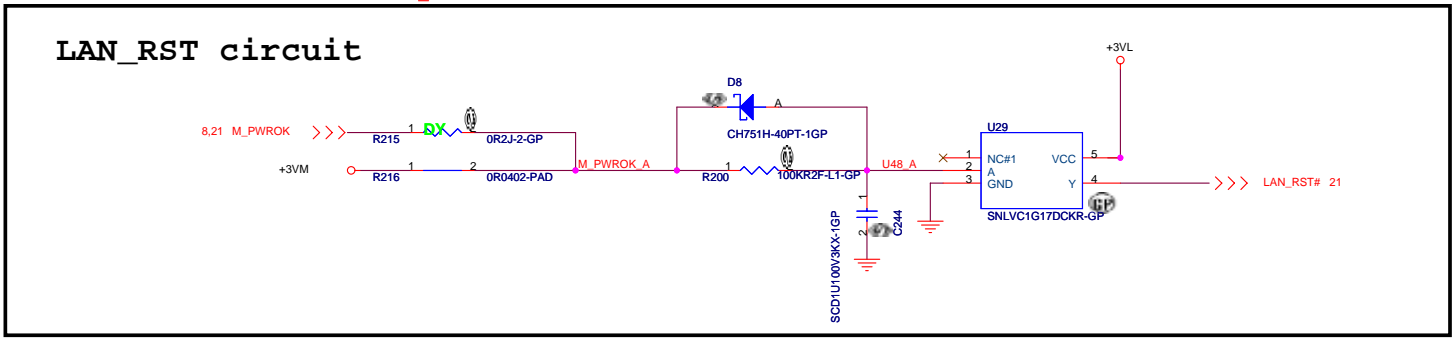
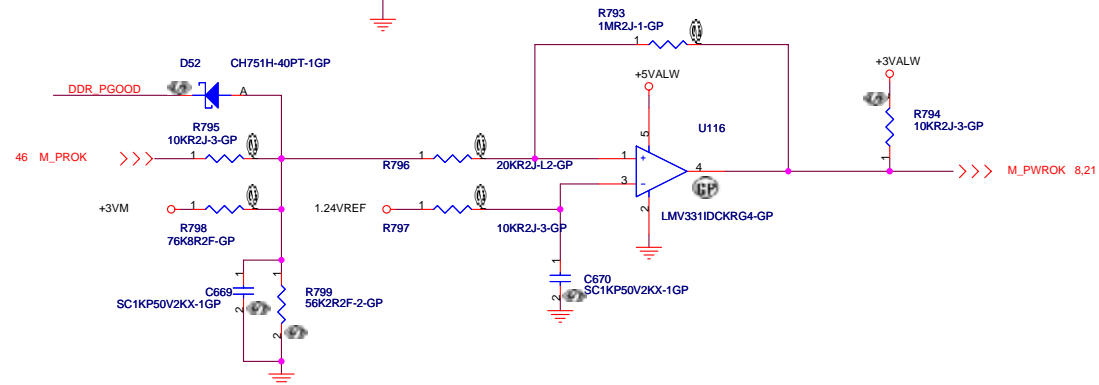
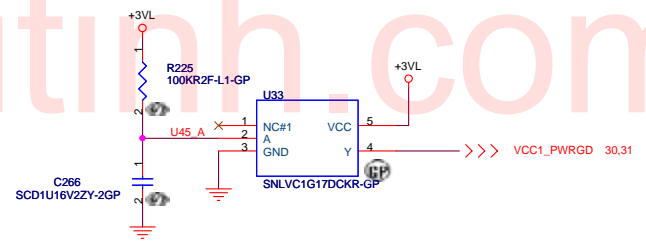
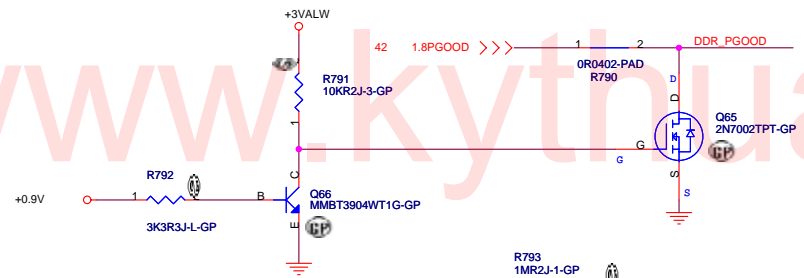
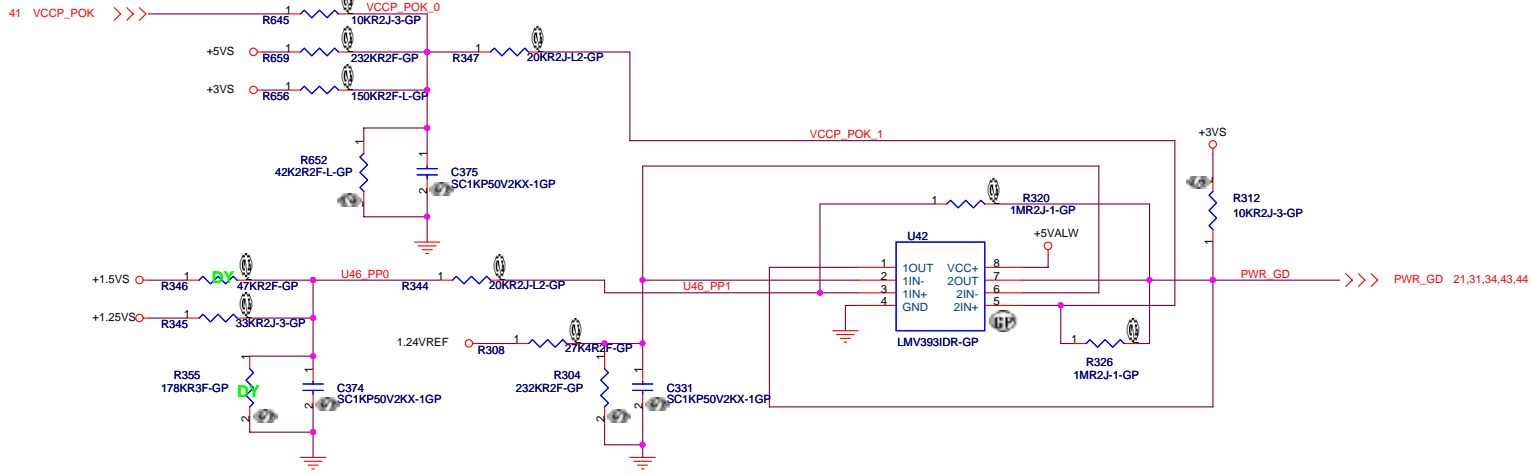
### Discharge circuit-1



<Core Design>

**緯創資通 Wistron Corporation**  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title		
<b>DC/DC Circuit</b>		
Size	Document Number	Rev
A3	NORN	PV
Date: Friday, March 30, 2007	Sheet 34 of 51	



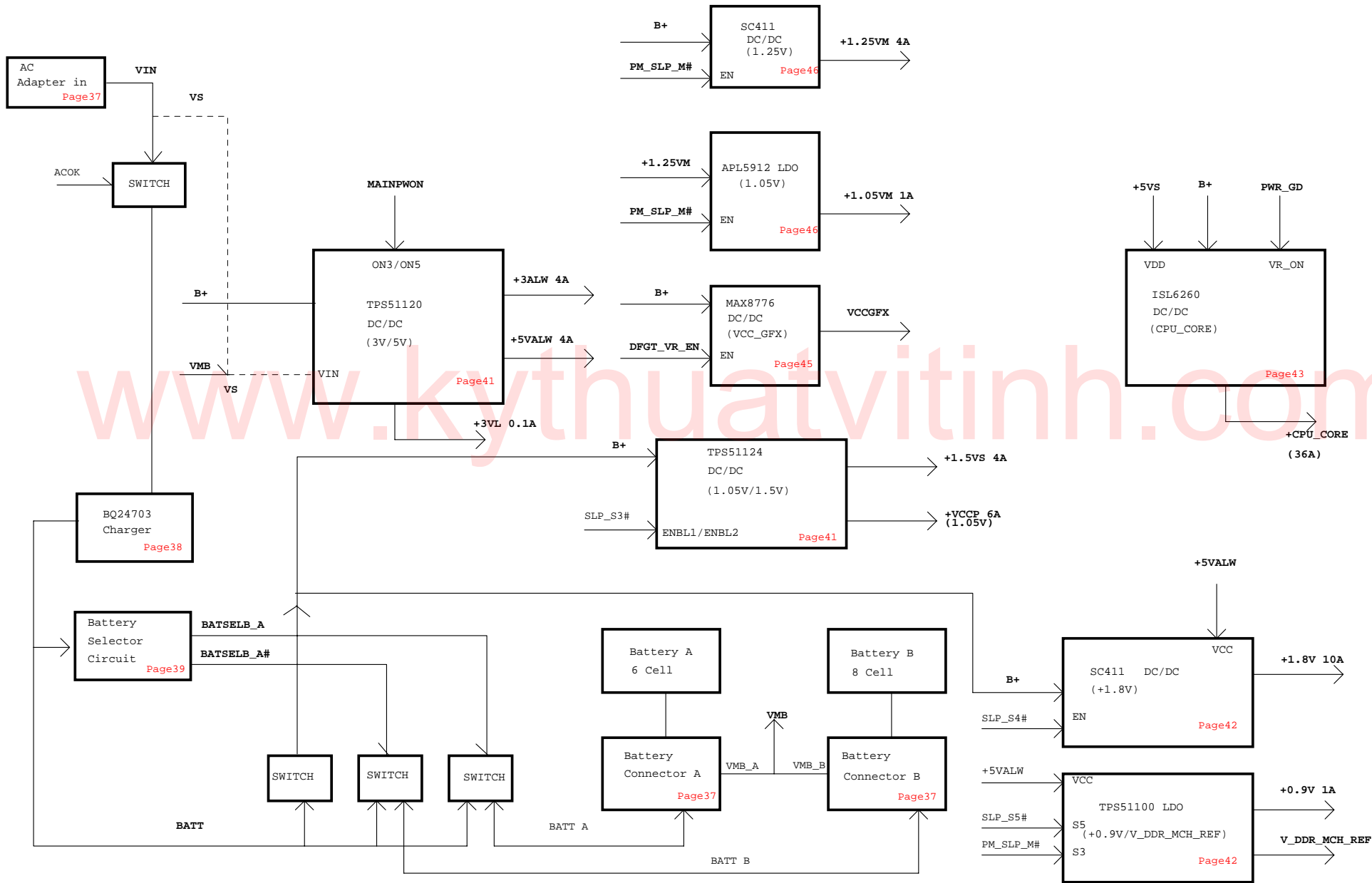
<Core Design>

**緯創資通 Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **POK CKT**

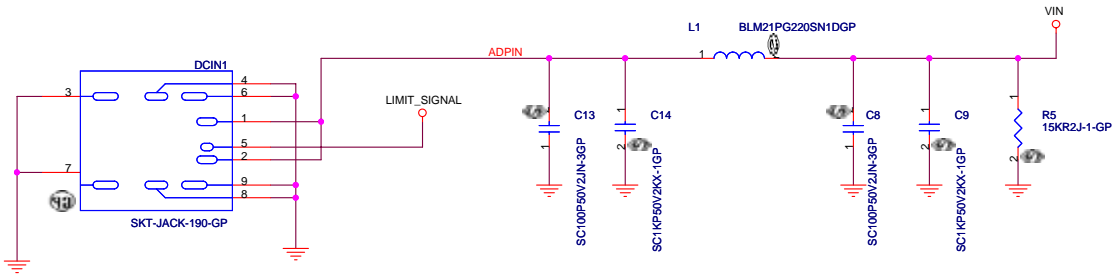
Size: A3	Document Number: <b>NORN</b>	Rev: <b>PV</b>
----------	------------------------------	----------------

Date: Friday, March 30, 2007 Sheet 35 of 51



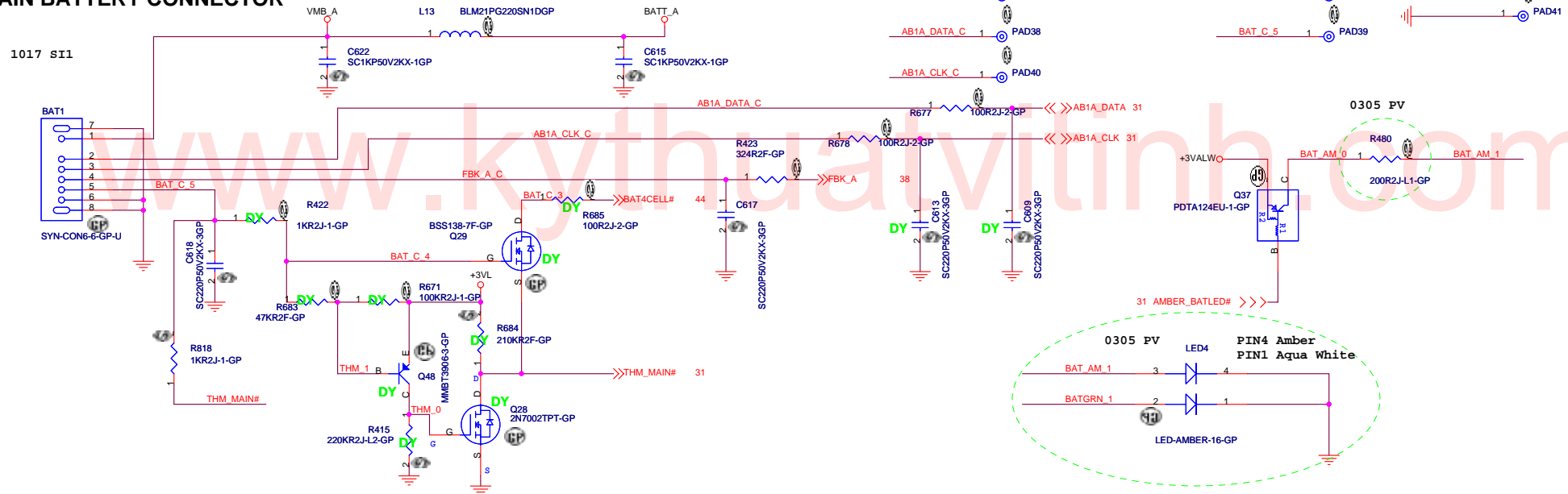
# Adaptor in to generate DCBATOUT

Current Rating 6 A



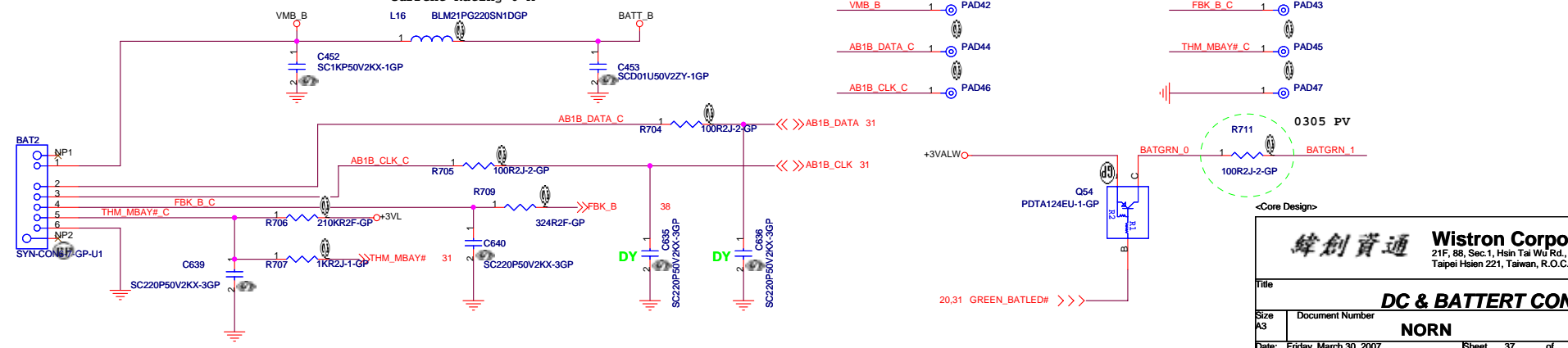
# MAIN BATTERY CONNECTOR

Current Rating 6 A



# BAY BATTERY CONNECTOR

Current Rating 6 A

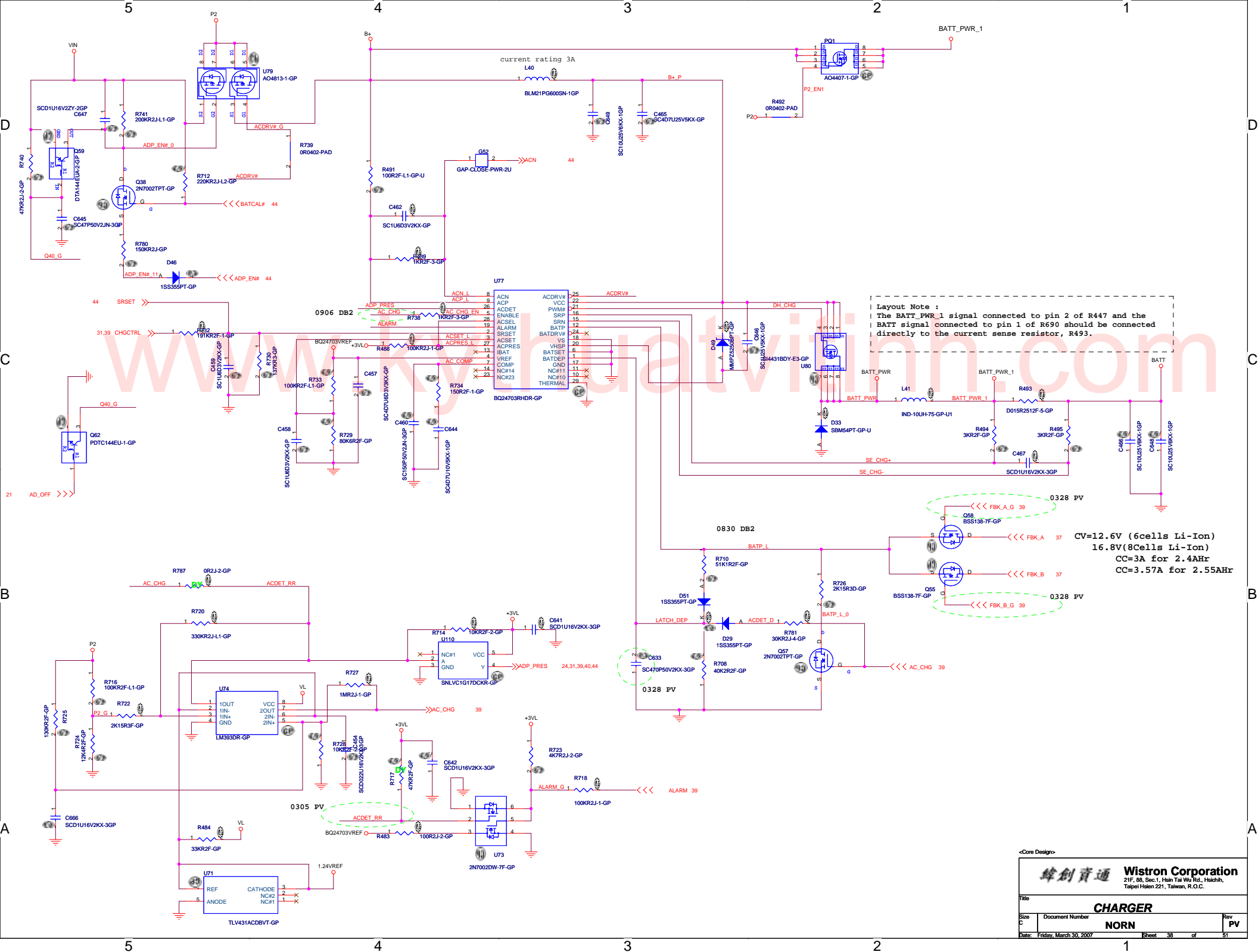


緯創資通 Wistron Corporation  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.

Title: **DC & BATTERY CONN.**

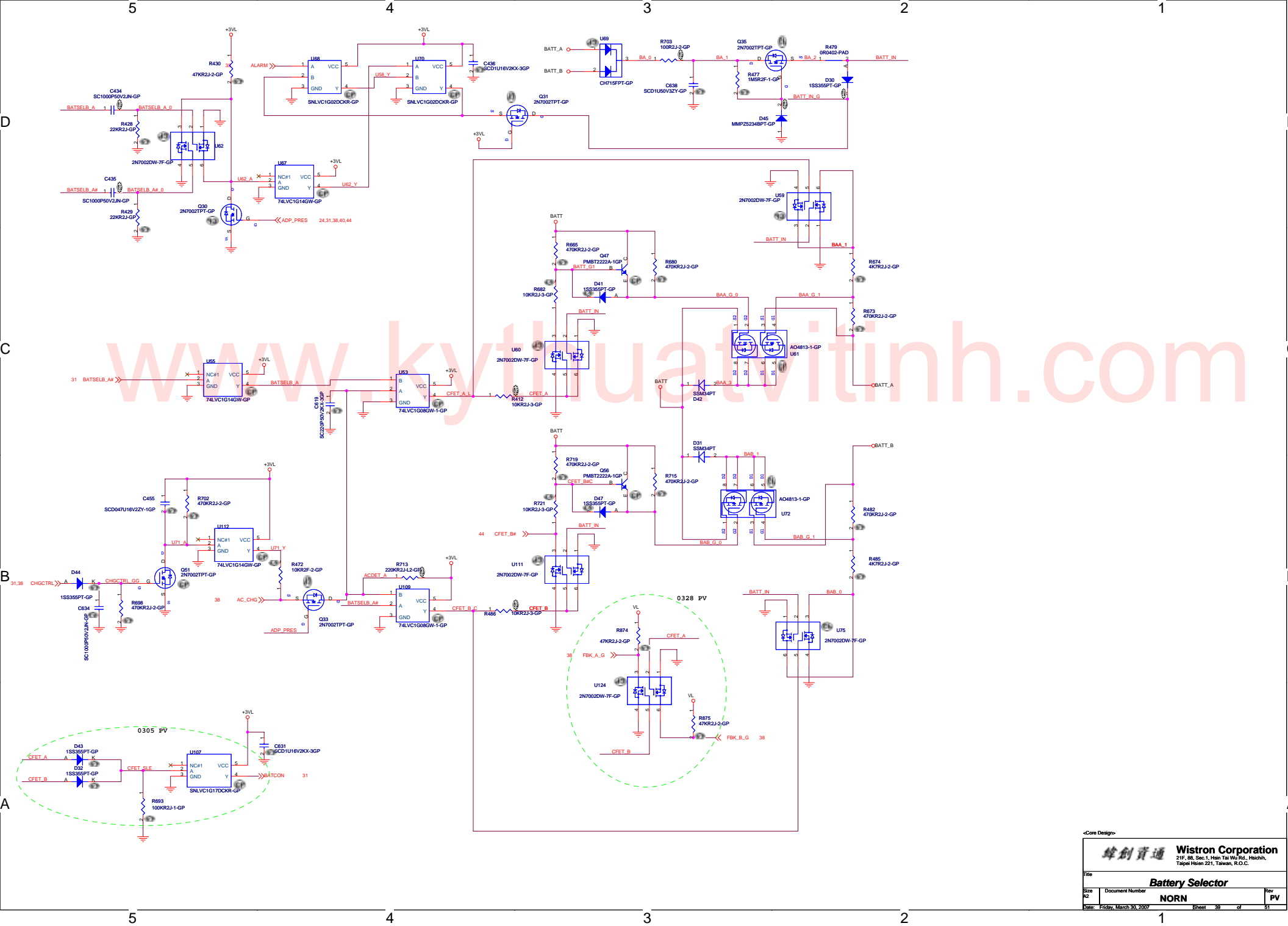
Size: A3 Document Number: **NORN** Rev: **PV**

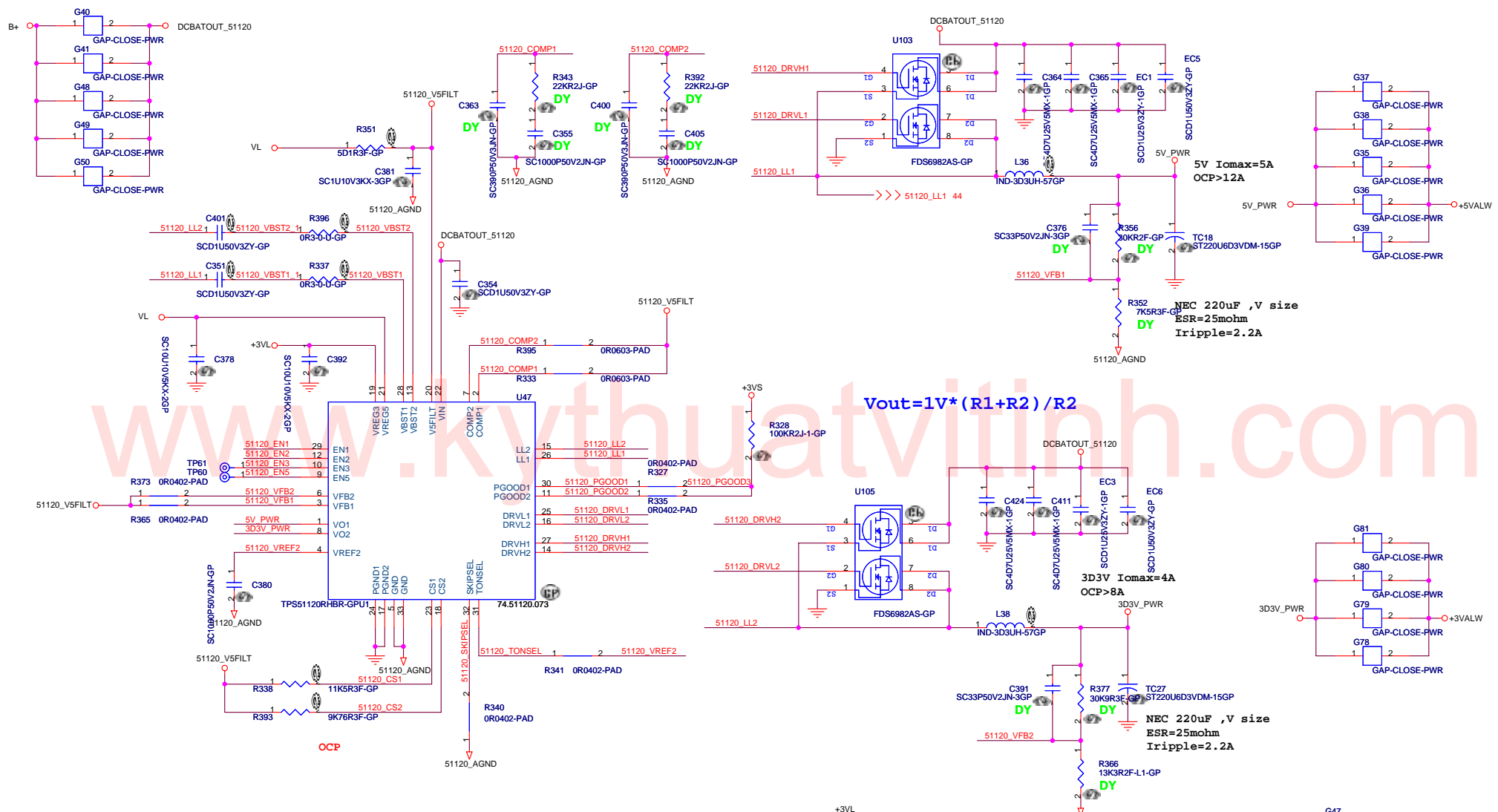
Date: Friday, March 30, 2007 Sheet 37 of 51



**Layout Note :**  
 The BATT\_PWR\_1 signal connected to pin 2 of R447 and the BATT signal connected to pin 1 of R690 should be connected directly to the current sense resistor, R493.

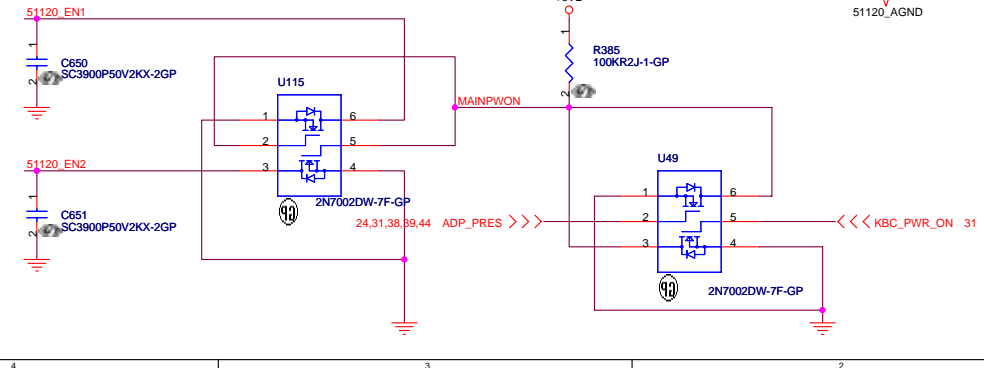
CV=12.6V (6cells Li-Ion)  
 16.8V(8Cells Li-Ion)  
 CC=3A for 2.4Ahr  
 CC=3.57A for 2.55Ahr





$$V_{out} = 1V \cdot (R1 + R2) / R2$$

	GND	VREF2	FLOAT	V5FILT
SKIPSEL	AUTOSKIP	AUTOSKIP / FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	D-Cap MODE
TONSEL	380k/CH1 590k/CH2	290k/CH1 440k/CH2	220k/CH1 330k/CH2	180k/CH1 280k/CH2
VFB1	N/A	not use	ADJ.	5V Fixed Output
VFB2	N/A	not use	ADJ.	3.3V Fixed Output
EN1, EN2	switcher OFF	not use	switchchr ON	Switcher ON
EN3, EN5	LDO OFF	not use	LDO ON	VREG3 on



<Core Design>

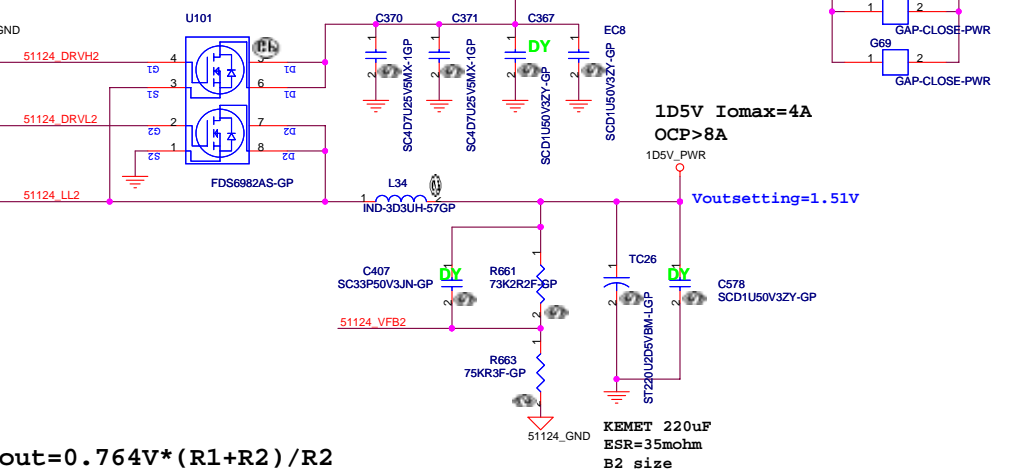
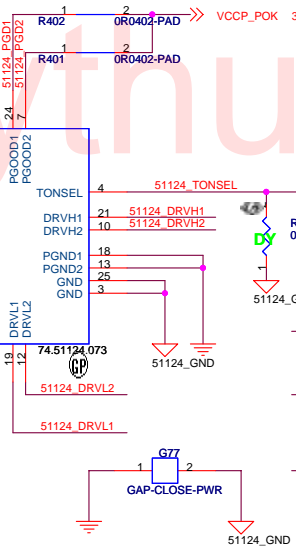
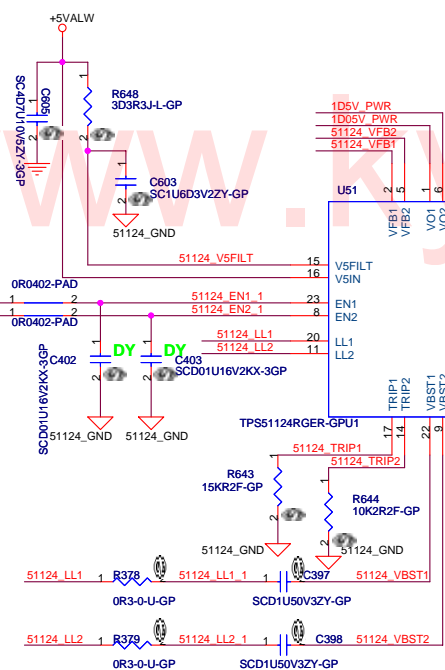
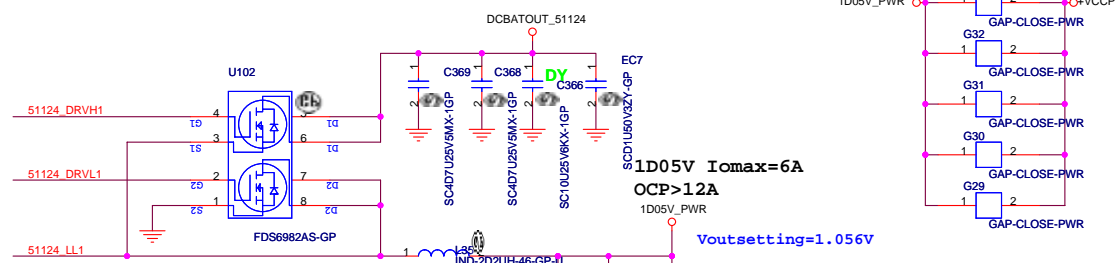
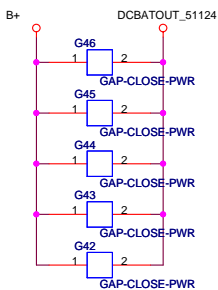
**緯創資通 Wistron Corporation**  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **TPS51120 +3VALW/+5VALW**

Size A3 Document Number **NORN** Rev **PV**

Date: Friday, March 30, 2007 Sheet 40 of 51





$$V_{out} = 0.764V * (R1 + R2) / R2$$

$$V_{trip}(mV) = R_{trip}(Kohm) * 10(\mu A)$$

$$I_{ocp} = (V_{trip}/R_{dson}) + ((1/(2 * L * f)) * ((V_{in} - V_{out}) * V_{out}) / V_{in})$$

	GND	OPEN	V5FILT
TONSEL	230k/CH1 283k/CH2	283k/CH1 346k/CH2	345k/CH1 423k/CH2

<Core Design>

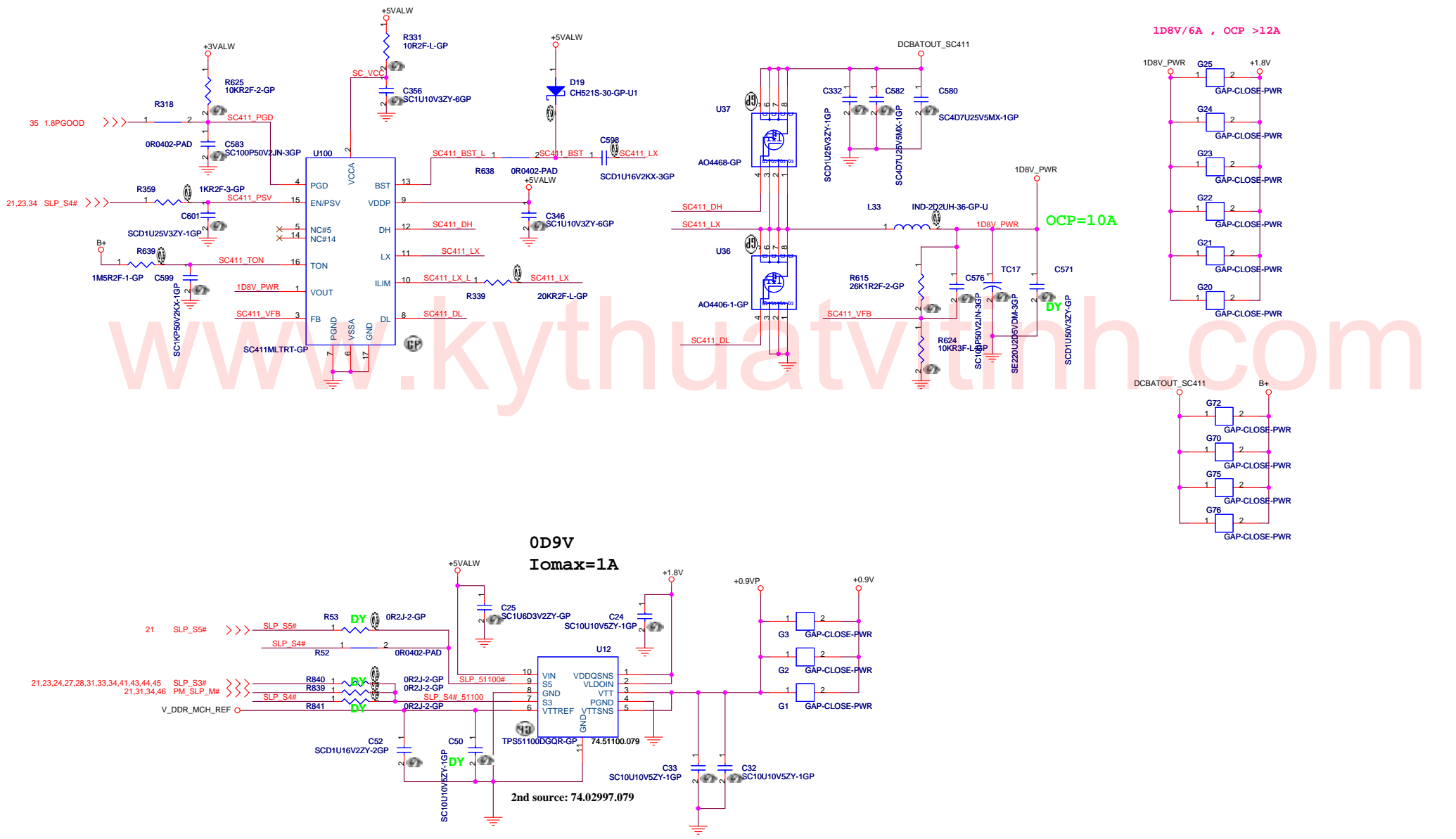
**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **TPS51124 +1.05V\_VCCP\_+1.5VS**

Size: A3 Document Number: **NORN** Rev: **PV**

Date: Friday, March 30, 2007 Sheet 41 of 51

# SC411 for 1D8V /TPS51110\_0D9V

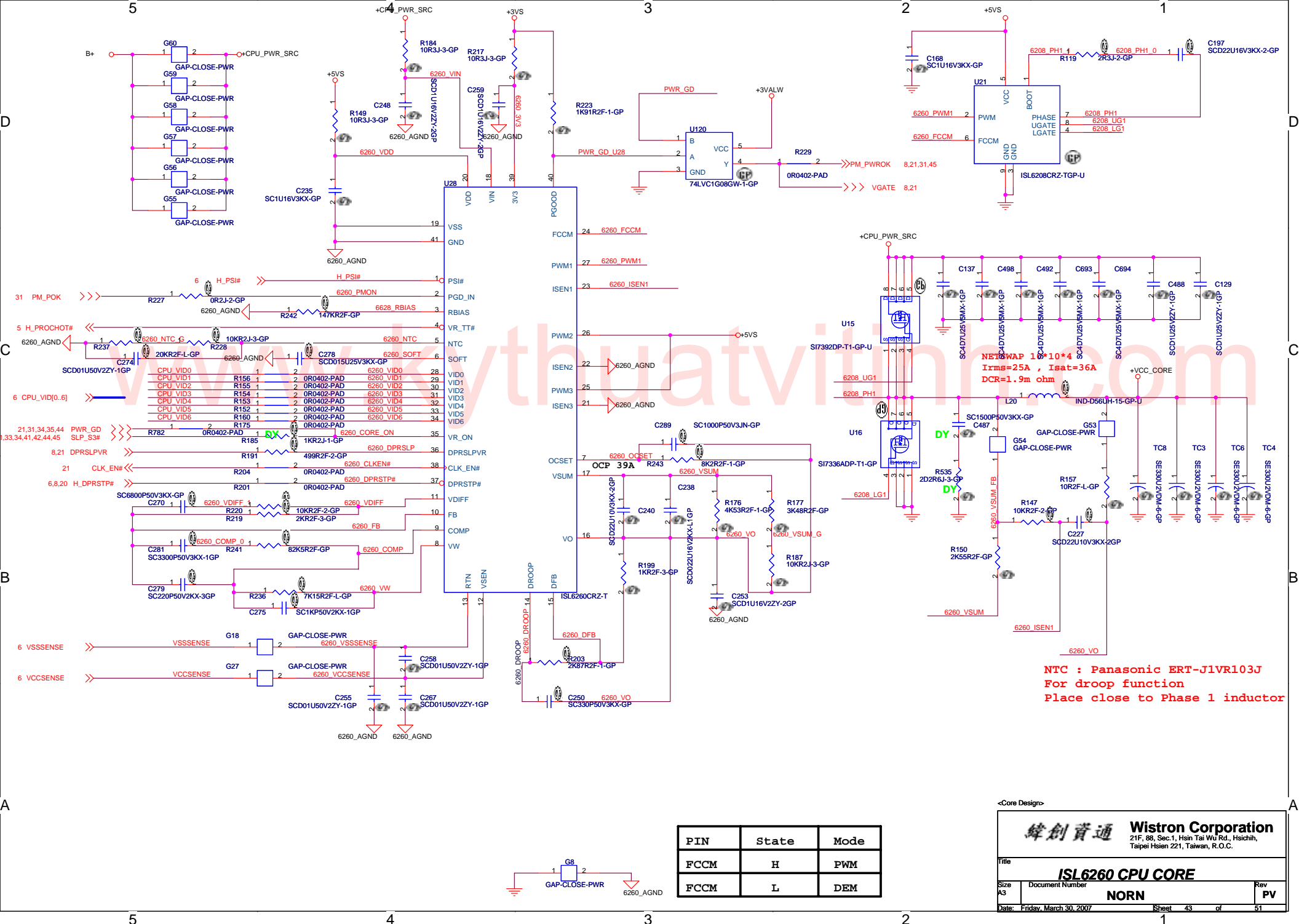


<Core Design>

**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.

Title: **SC 411 1D8V/0.9VP TPS51100**

Size A3	Document Number	Rev
	<b>NORN</b>	<b>PV</b>
Date: Friday, March 30, 2007	Sheet 42 of 51	



**NTC : Panasonic ERT-J1VR103J**  
**For droop function**  
**Place close to Phase 1 inductor**

PIN	State	Mode
FCCM	H	PWM
FCCM	L	DEM

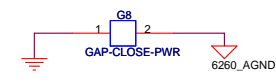
<Core Design>

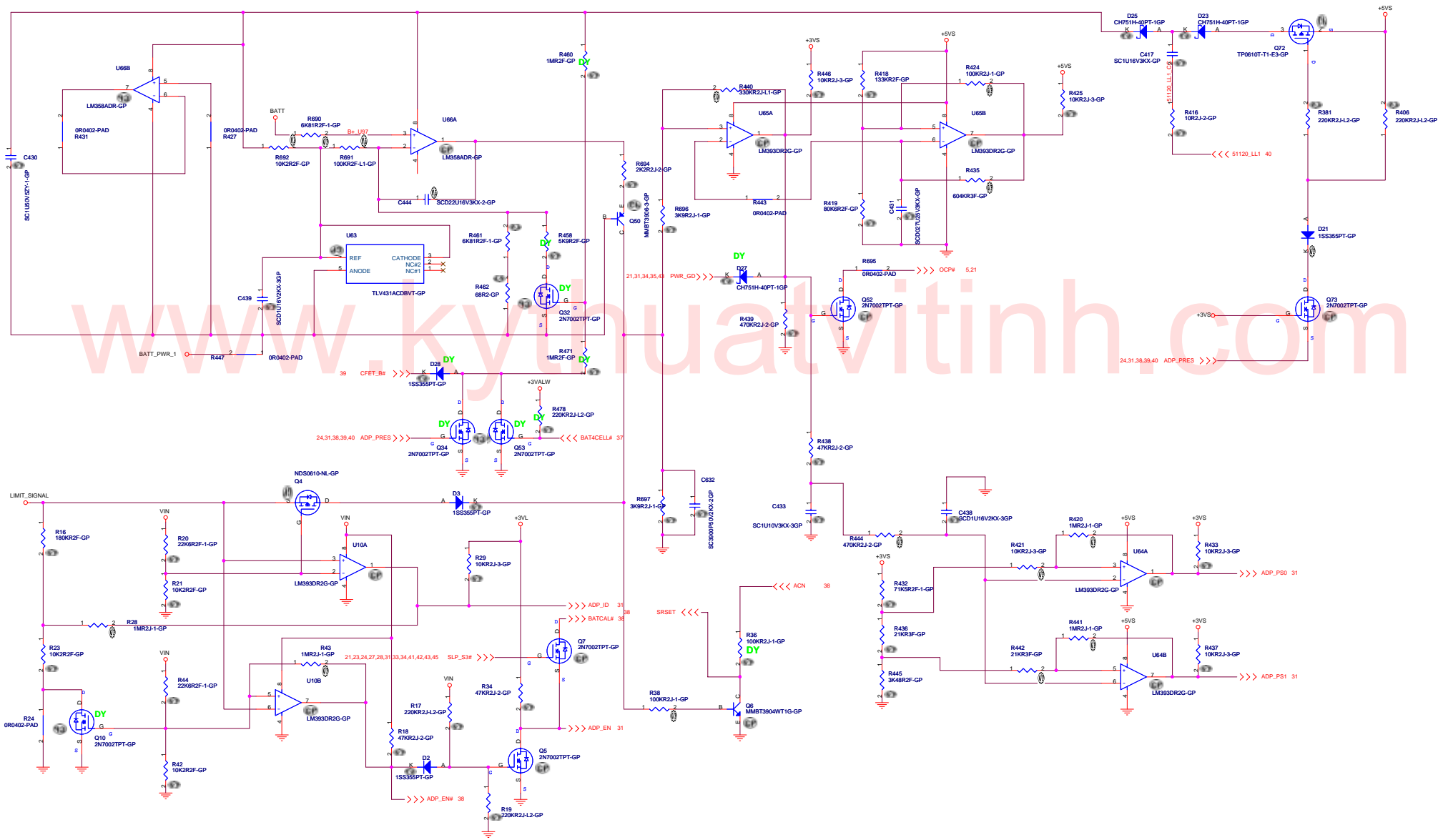
**緯創資通 Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichu, Taipei Hsien 221, Taiwan, R.O.C.

Title: **ISL6260 CPU CORE**

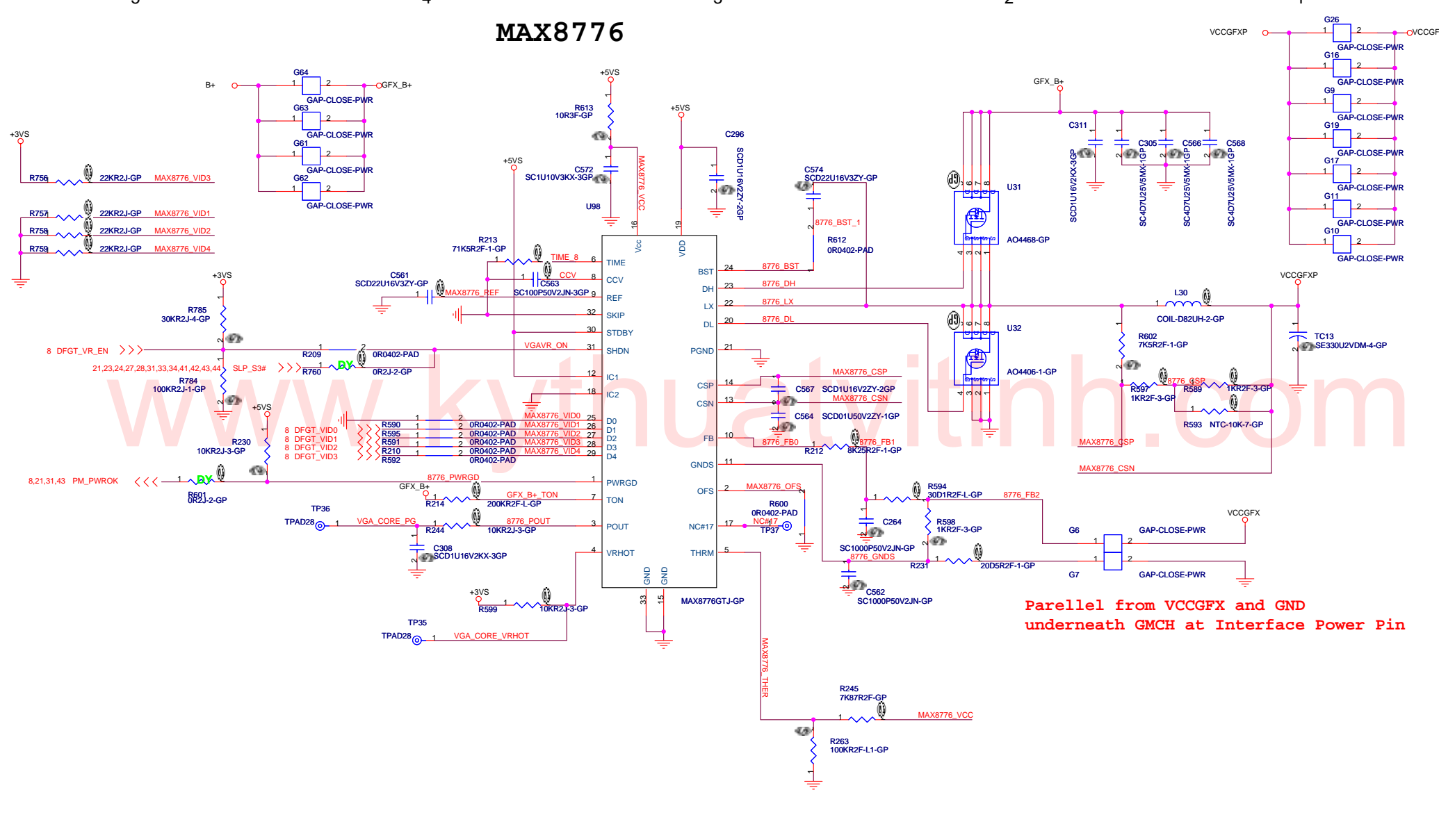
Size A3	Document Number	Rev PV
<b>NORN</b>		

Date: Friday, March 30, 2007 Sheet 43 of 51



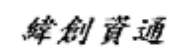


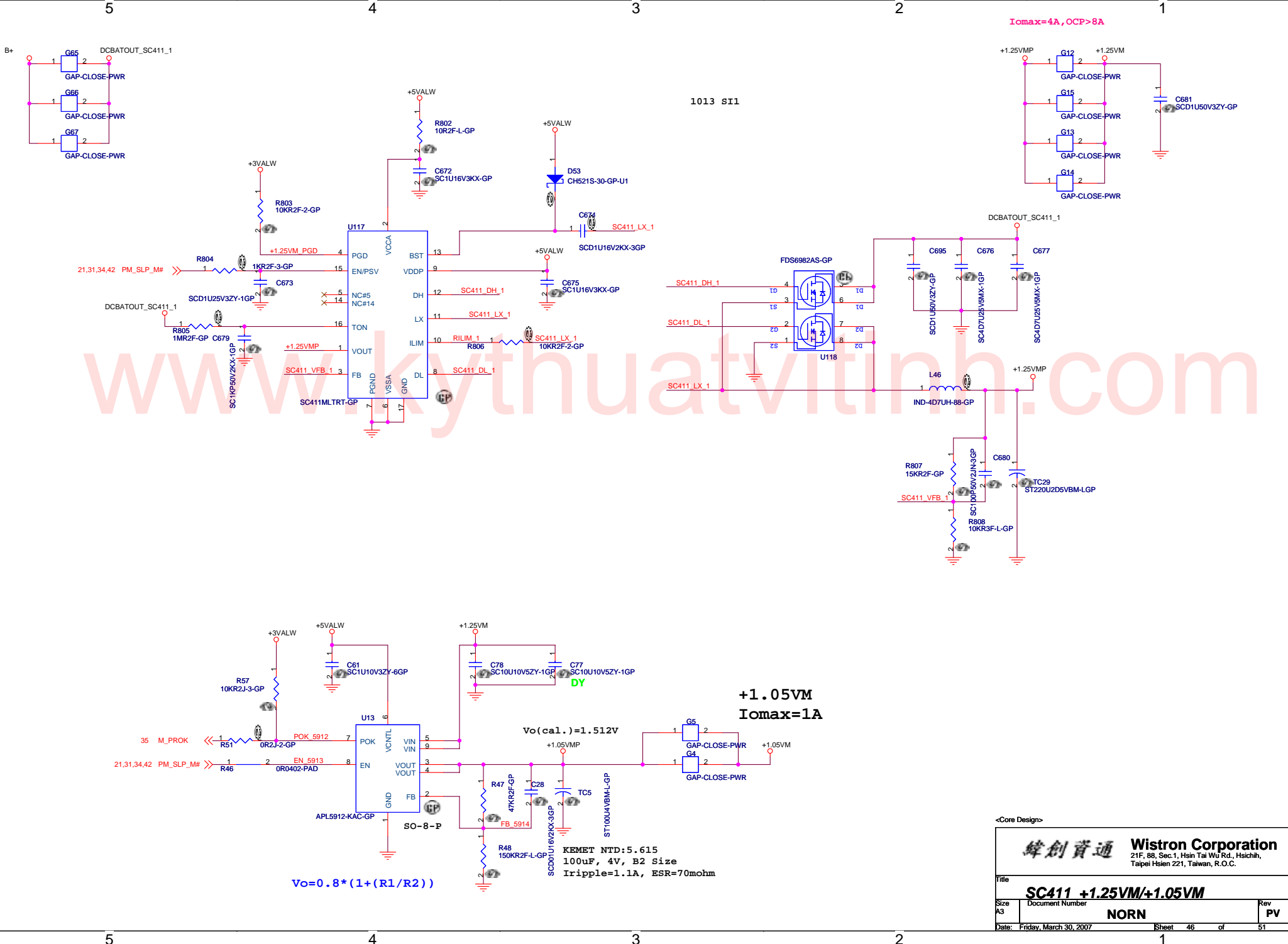
# MAX8776



Parallel from VCCGFX and GND underneath GMCH at Interface Power Pin

<Core Design>

 <b>Wistron Corporation</b> 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.		
<b>MAX8776_VCCGFX</b>		
Size A3	Document Number	Rev PV
Date: Friday, March 30, 2007	Sheet 45 of 51	



<Core Design>

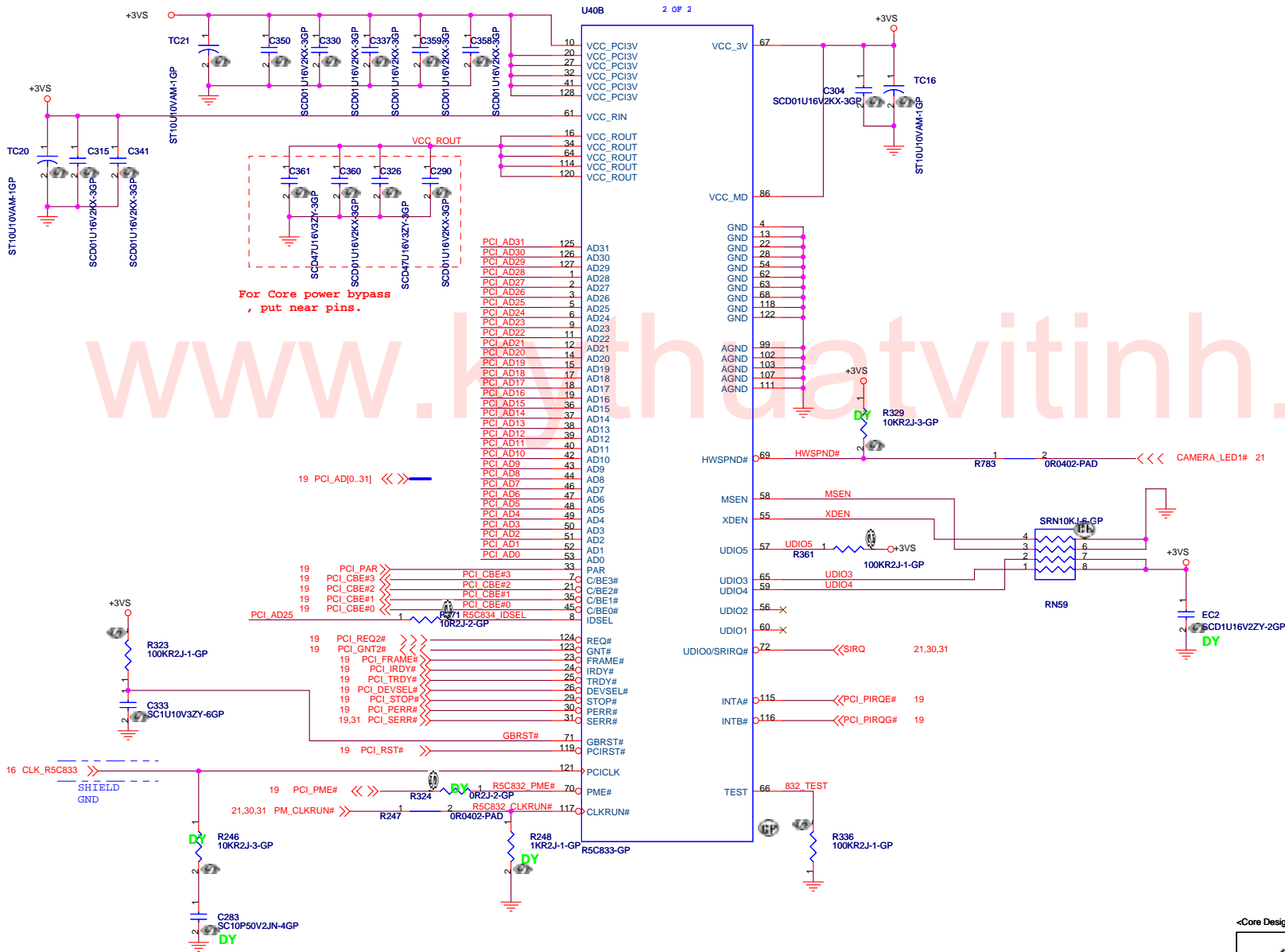
<b>緯創資通 Wistron Corporation</b>	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.	
<b>SC411 +1.25VM/+1.05VM</b>	
Title	Rev
Size A3	Document Number
Date: Friday, March 30, 2007	<b>NORN</b>
Sheet 46	of 51

KEMET NTD:5.615  
100uF, 4V, B2 Size  
Iripple=1.1A, ESR=70mohm

$V_o = 0.8 * (1 + (R1/R2))$

**+1.05VM**  
**Iomax=1A**

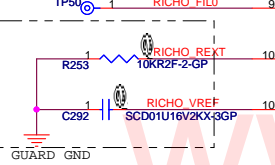
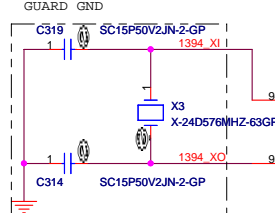
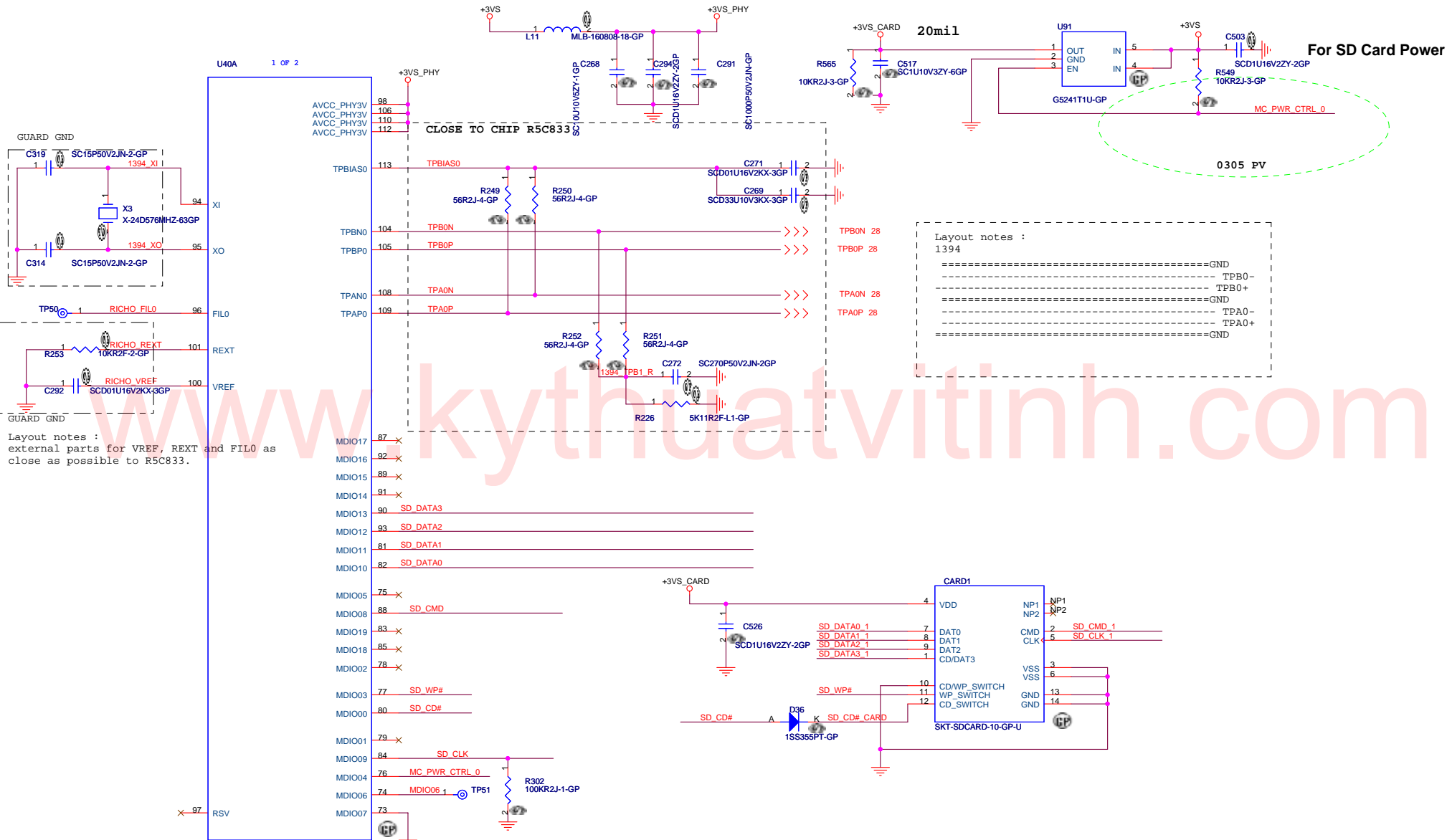
**Iomax=4A, OCP>8A**



<Core Design>

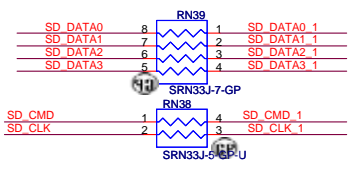
<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien Z21, Taiwan, R.O.C.		
<b>R5C833/PCI</b>		
Size A3	Document Number	Rev PV
<b>NORN</b>		
Date: Friday, March 30, 2007	Sheet 47 of	51





Layout notes :  
external parts for VREF, REXT and FIL0 as  
close as possible to R5C833.

Layout notes :  
1394  
=====GND  
-----TPB0-  
-----TPB0+  
=====GND  
-----TPA0-  
-----TPA0+  
=====GND



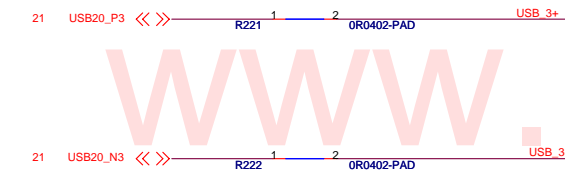
<Core Design>

**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

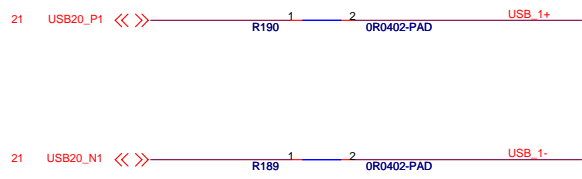
Title: **R5C833/IEEE1394/SD**

Size A3	Document Number	Rev PV
<b>NORN</b>		
Date: Friday, March 30, 2007	Sheet 48 of 51	

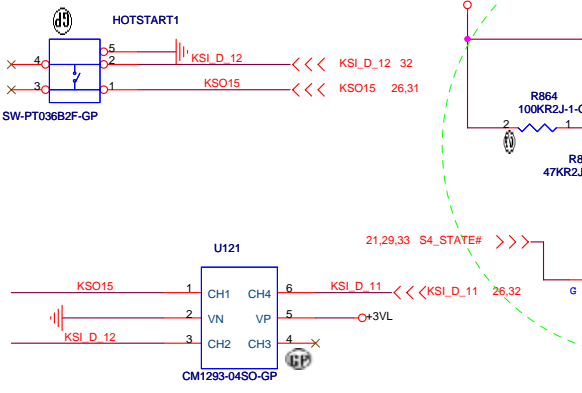
# CAMERA



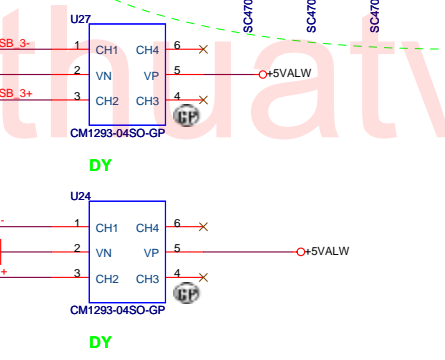
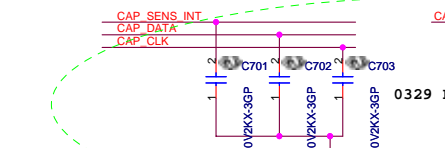
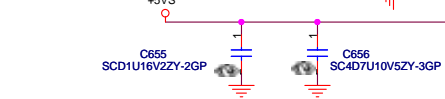
# FingerPrint



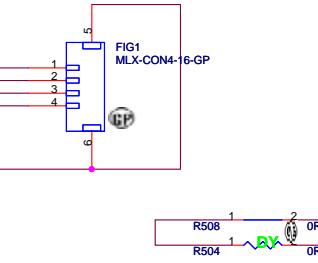
# HOTSTART



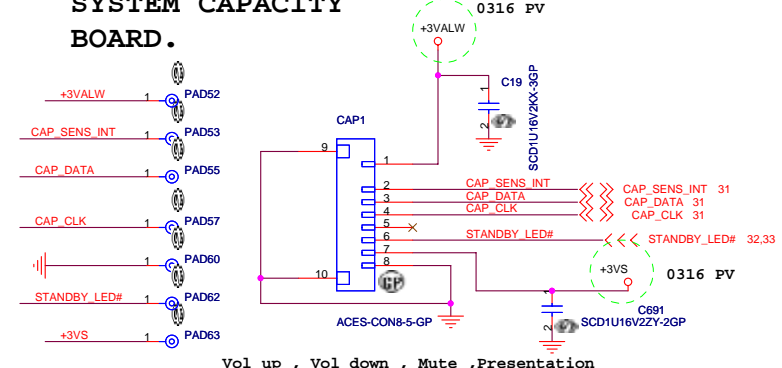
# CAPACITY LAUNCH BAR



# FingerPrint Conn.



# SYSTEM CAPACITY BOARD.



Vol up , Vol down , Mute , Presentation

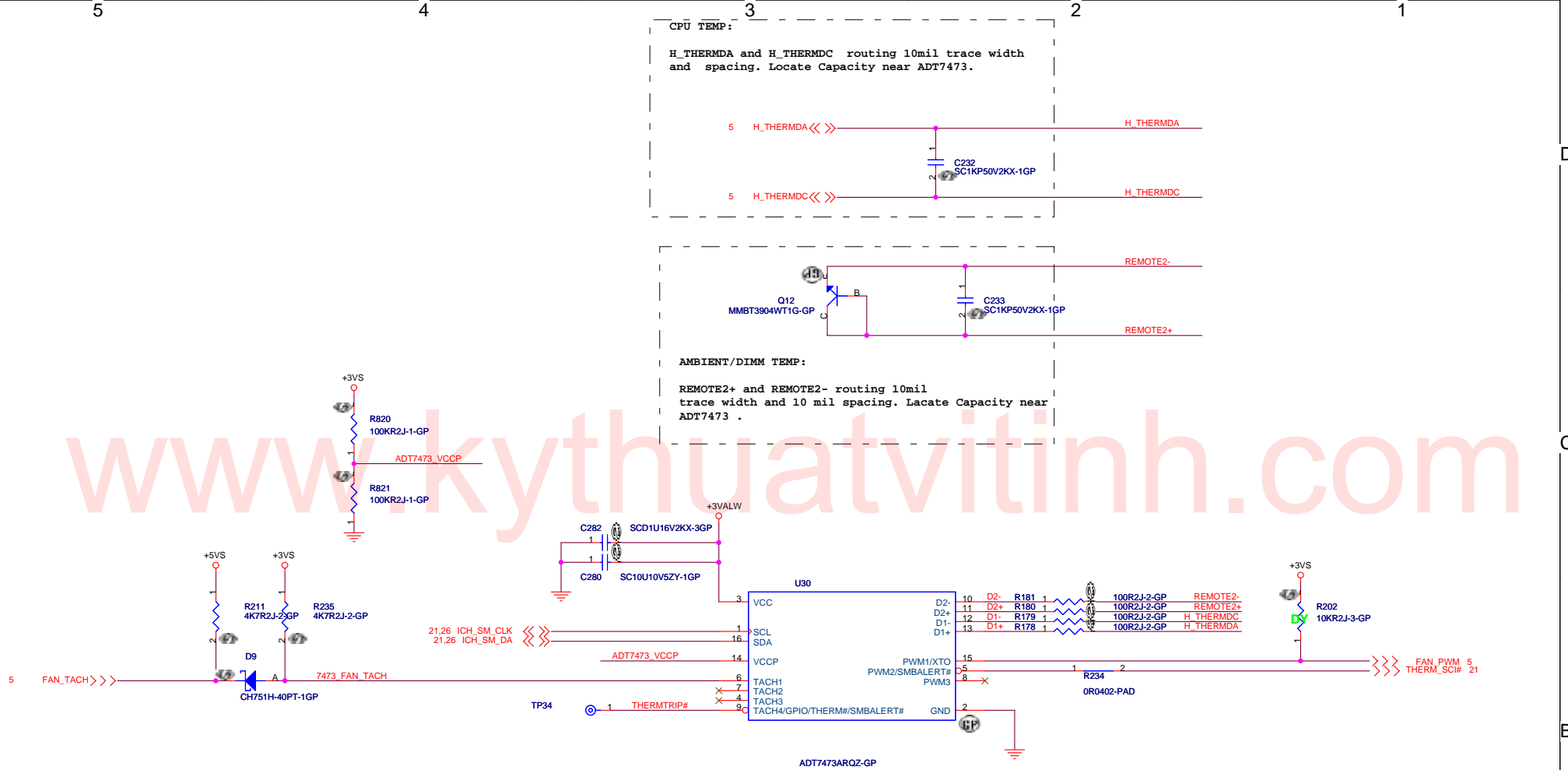
<Core Design>

<b>Wistron Corporation</b> 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichin, Taipei Hsein 221, Taiwan, R.O.C.	
<b>Camera/W-COM/Light Sensor</b>	
Title Size A3 Date: Friday, March 30, 2007	Document Number <b>NORN</b> Sheet 49 of 51
Rev <b>PV</b>	Rev <b>PV</b>

Backlight PWM

Sleep & Rotation

Crtl+Alt+Delct

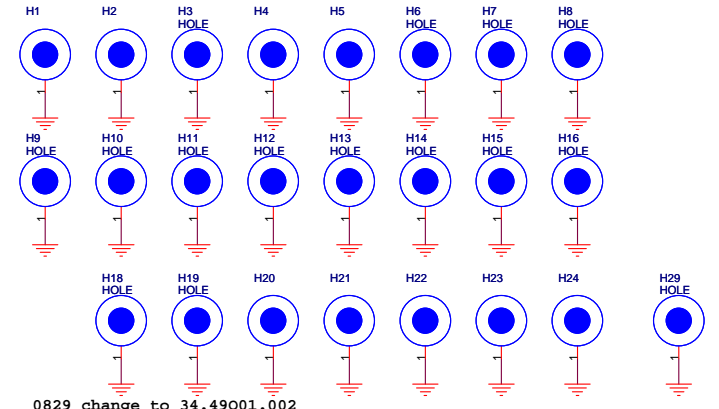
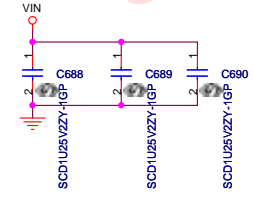
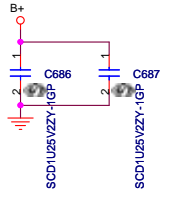


<Core Design>

<b>緯創資通</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>ADT7473 Thermal Sensor</b>			
Size	Document Number	Rev	
A3	NORN	PV	
Date:	Friday, March 30, 2007	Sheet	50 of 51

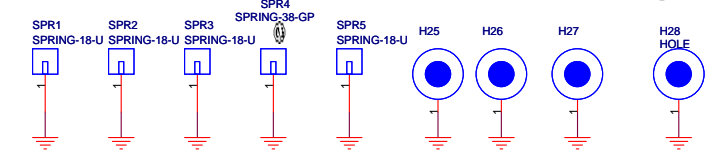
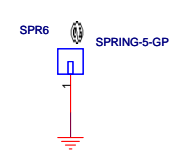
www.kythuatv.com

1101 HOLE H1,H2 change part to 34.4R836.001  
 1101 HOLE H4,H5 change part to 34.4R837.001  
 1101 HOLE H17 change part to 34.4R838.001  
 1101 HOLE H20,H21 change part to 34.4R841.001  
 1101 HOLE H22,H23,H24,H25 change part to 34.4R840.001  
 1101 HOLE H26,H27 change part to 34.4R839.001

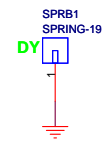


0829 change to 34.49Q01.002

0814 ME update drawing



1018 change SPR4 to 34.47R31.001  
 <Core Design>



		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.	
<b>UNUSED PARTS/EMI Capacitors</b>			
Title			
Size	Document Number	Rev	
A3	Norn		PV
Date:	Tuesday, March 27, 2007	Sheet	51 of 51