

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN2
LAYER 4 : SGND1
LAYER 5 : SVCC
LAYER 6 : IN2
LAYER 7 : SGND2
LAYER 8 : BOT

Cable Docking
VGA
RJ-45
CIR/Pwr btn
SPDIF Out
Stereo MIC
Headphone Jack
USB Port
VOL Cntr
PAGE 40

SYSTEM CHARGER(ISL6251AHAZ-T)
PAGE 41

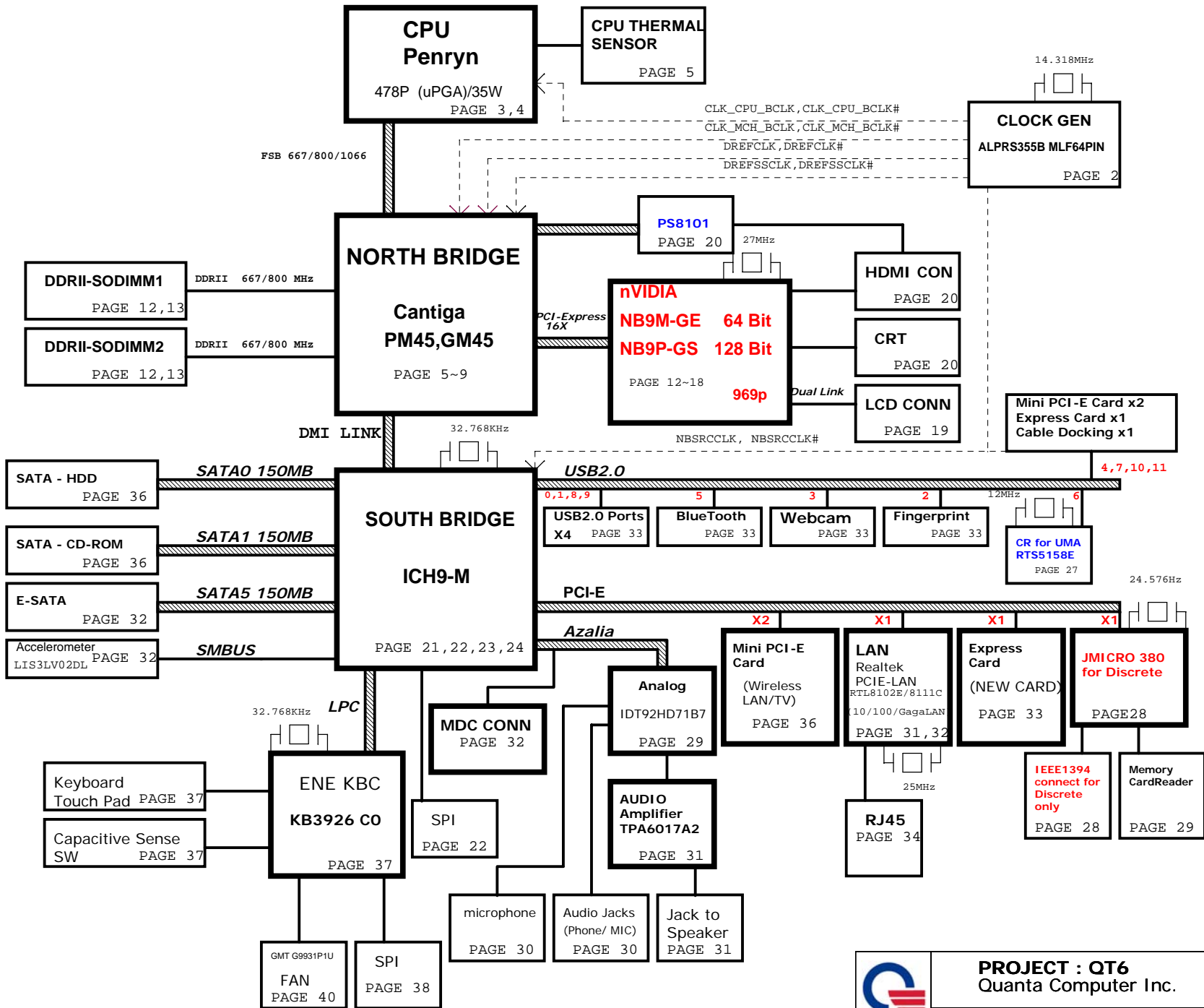
SYSTEM POWER ISL6237IRZ-T
PAGE 42

DDR II SMDR_VTERM
1.8V/1.8VSUS(TPSS51116REGR)
PAGE 46

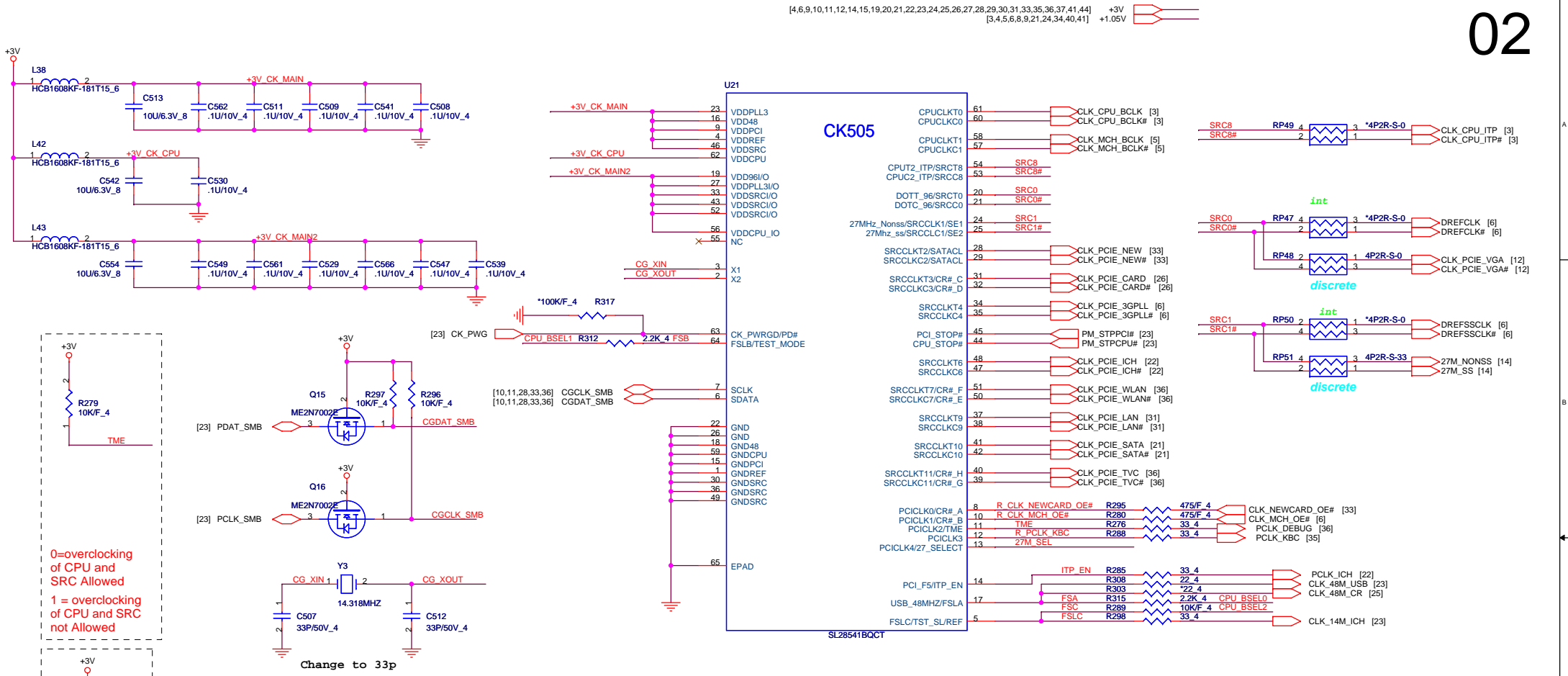
VCCP +1.5V AND GMCH
1.05V(RT8204)
PAGE 43

VGACORE(1.025V)Oz8118
PAGE 45

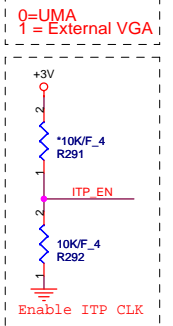
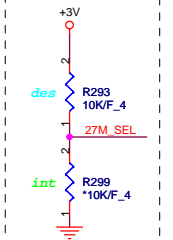
CPU CORE ISL6266A
PAGE 44



| | | | | |
|--|----------------------|---|----------------------------------|---------------|
| | PROJECT : QT6 | | Date: Tuesday, February 26, 2008 | |
| | Quanta Computer Inc. | | | Sheet 1 of 44 |
| | Size Custom | Document Number Block Diagram | | Rev 1A |



0=overclocking of CPU and SRC Allowed
 1 = overclocking of CPU and SRC not Allowed

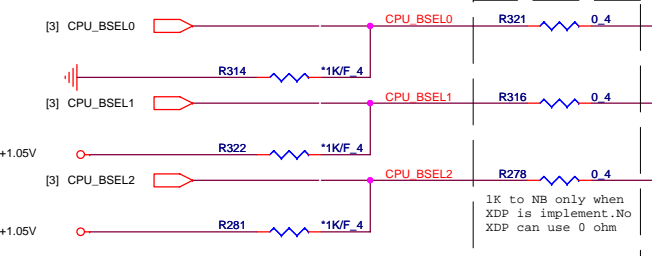


| 27M_SEL PIN13 | PIN20 | PIN21 | PIN24 | PIN25 |
|------------------|--------|--------|----------------|----------------|
| 0=UMA | DOT96T | DOT96C | SRCT1/LCDT_100 | SRCT1/LCDT_100 |
| 1 = External VGA | SRCT0 | SRCC0 | 27Mout-NSS | 27Mout-SS |

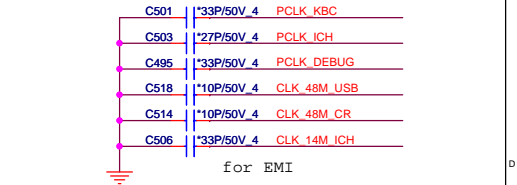
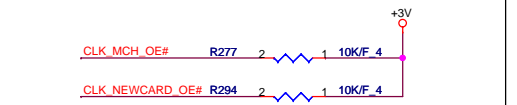
CK505 QFN64

- ICS ICS9LPRS355BKLF ALPRS355000
 Silego SLG8SP513VTR AL8SP513000
 Realtek RTM875N-606-VD-GR AL000875000

CPU Clock select

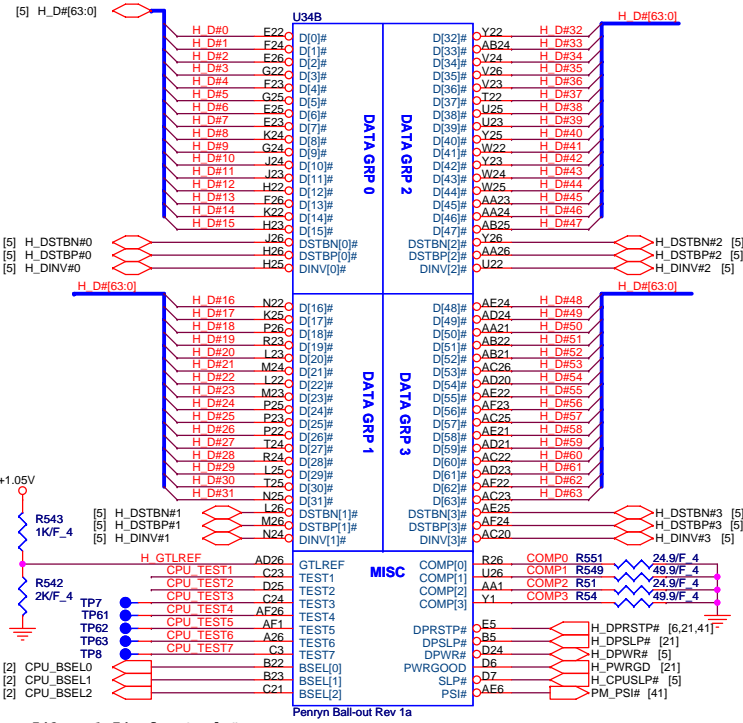
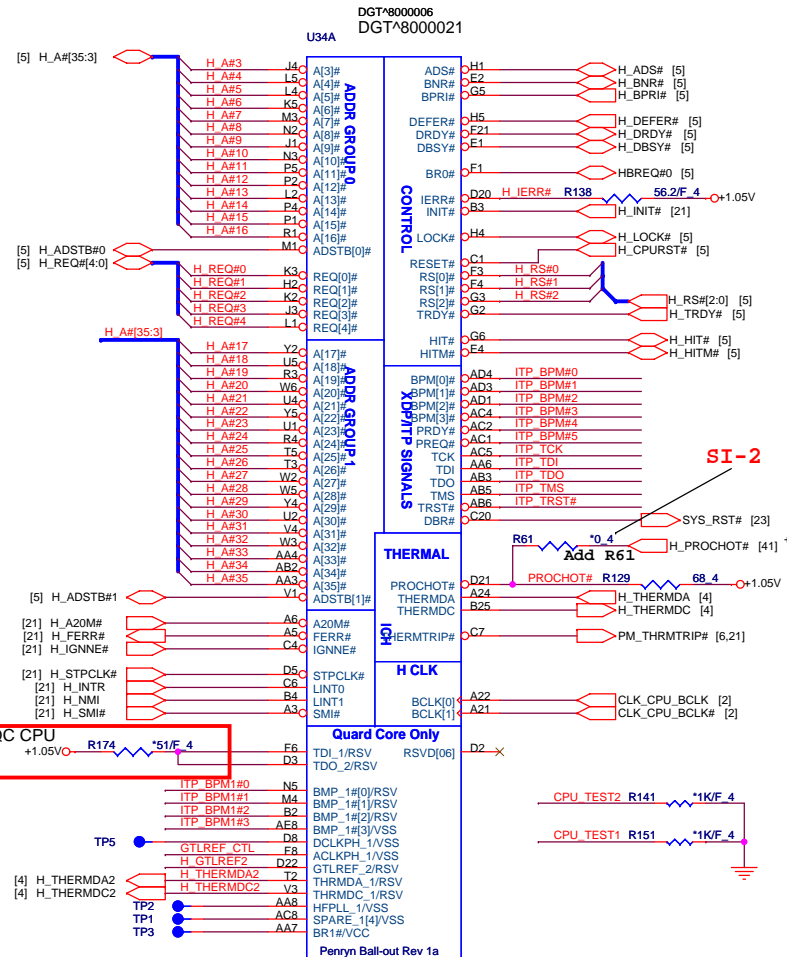


| FSC | FSB | FSA | CPU | SRC | PCI |
|-----|-----|-----|------|-----|-----|
| 1 | 0 | 1 | 100 | 100 | 33 |
| 0 | 0 | 1 | 133 | 100 | 33 |
| 0 | 1 | 1 | 166 | 100 | 33 |
| 0 | 1 | 0 | 200 | 100 | 33 |
| 0 | 0 | 0 | 266 | 100 | 33 |
| 1 | 0 | 0 | 333 | 100 | 33 |
| 1 | 1 | 0 | 400 | 100 | 33 |
| 1 | 1 | 1 | RSVD | 100 | 33 |



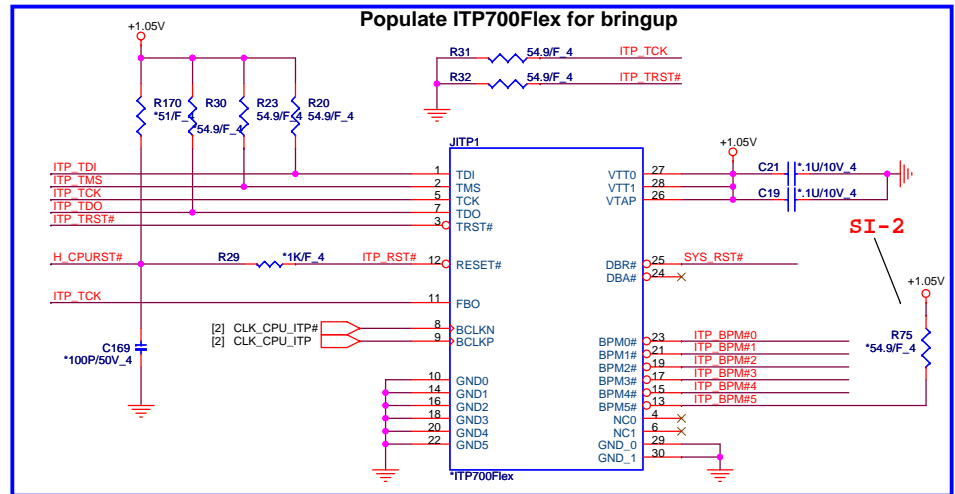
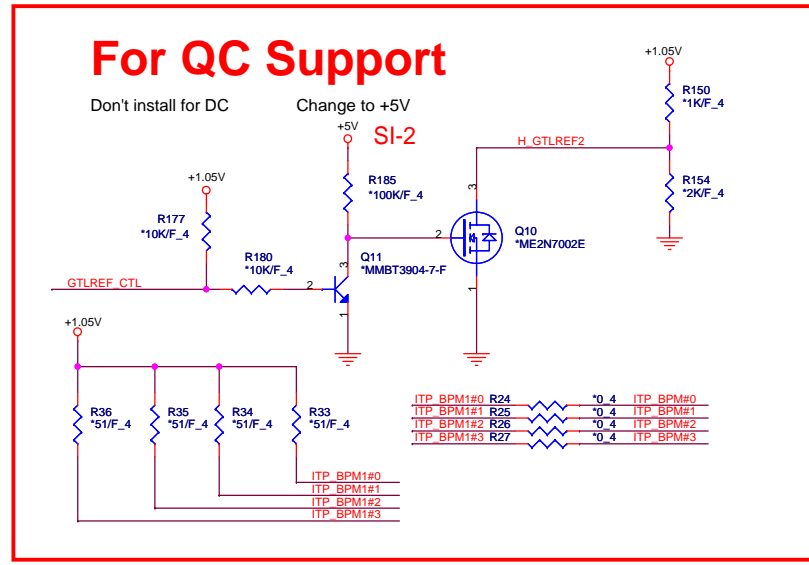
PROJECT : QT6
 Quanta Computer Inc.

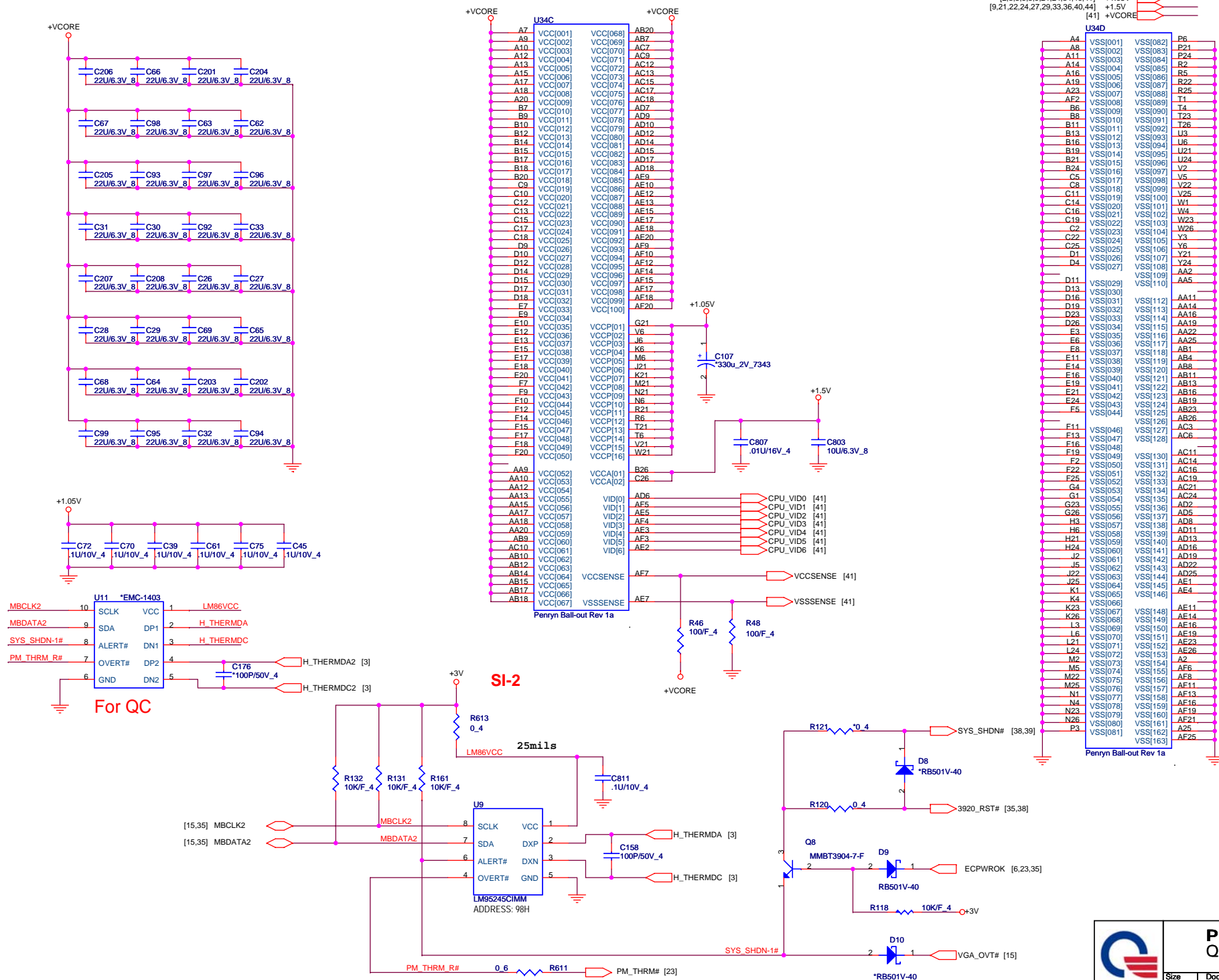
Size Custom Document Number Rev 1A
Clock Generator
 Date: Tuesday, February 26, 2008 Sheet 2 of 44



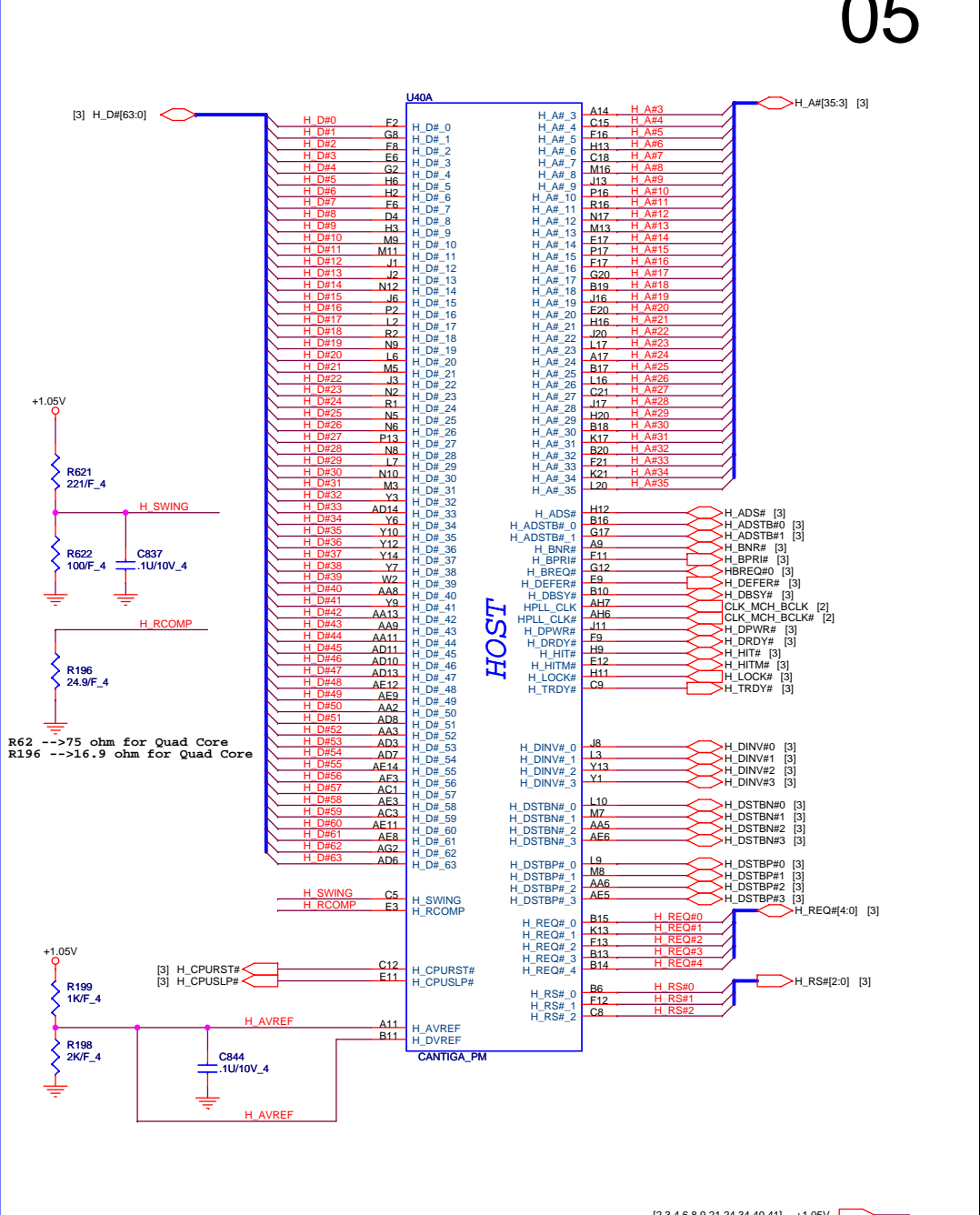
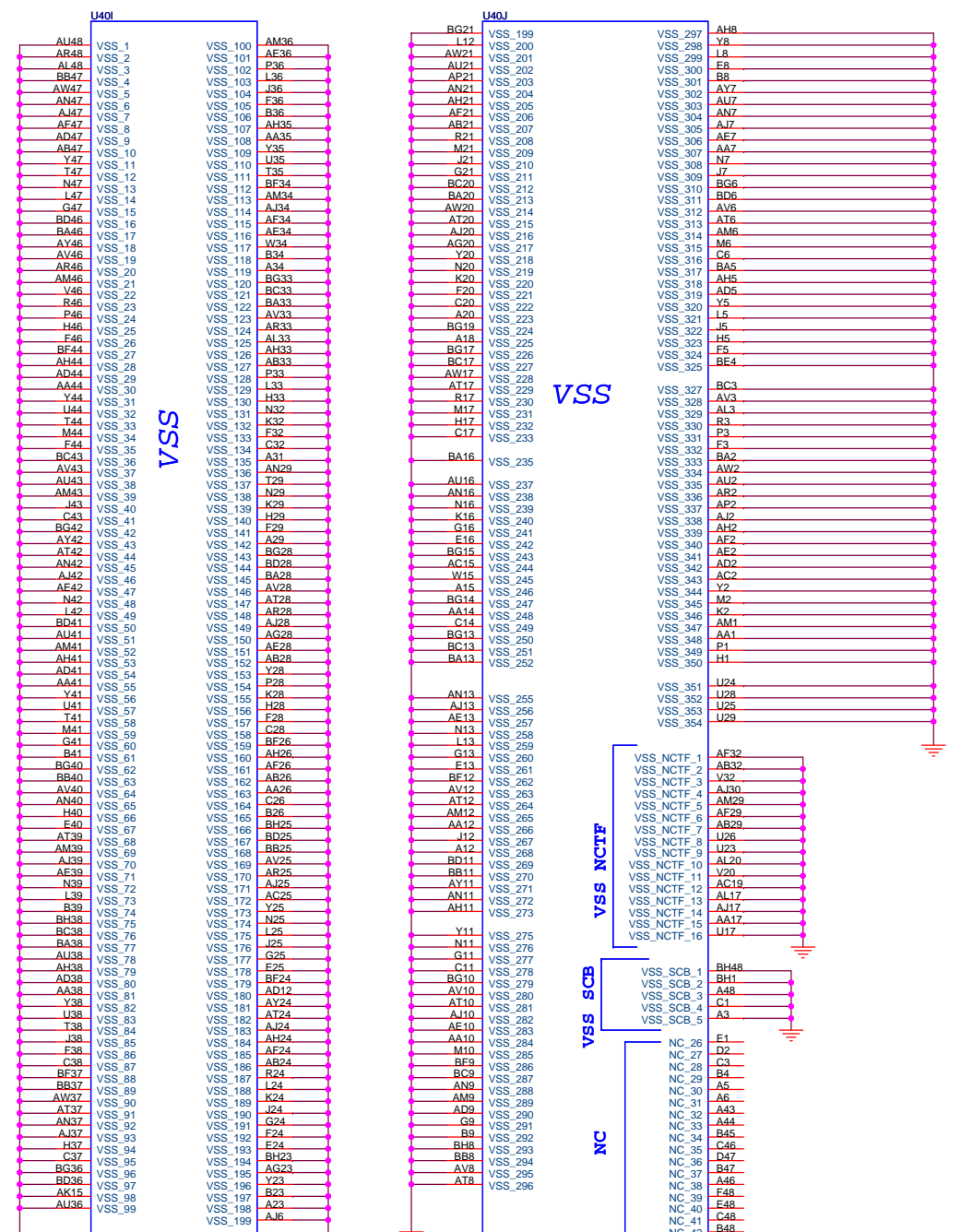
For QC CPU
+1.05V R174 *51/F_4

CPU_TEST2 R141 *1K/F_4
CPU_TEST1 R151 *1K/F_4





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[2,3,4,6,8,9,21,24,34,40,41] +1.05V

[2,4,9,10,11,12,14,15,19,20,21,22,23,24,25,26,27,28,29,30,31,33,35,36,37,41,44] +3V
 [8,9,10,34,40,43] +1.8VSUS
 [2,3,4,5,8,9,21,24,34,40,41] +1.05V
 [2,3,4,5,8,9,21,24,34,40,41] +1.05V_PEG

MCH_CFG_5 DMiX2 selection
 Low = DMi X2
 High = DMi X4 (Default)
MCH_CFG_16 FSB Dynamic ODT
 Low = Dynamic ODT disabled
 High = Dynamic ODT enabled (default)

MCH_CFG_9 PCI Express Graphic Lane
 Low = Reverse Lane
 High = Normal operation(Default)

MCH_CFG_19 DMI Lane Reversal
 Low = Normal operation (Default)
 High = Reverse Lanes

MCH_CFG_6 ITPM Host Interface
 Low = The ITPM Host Interface is enabled2
 High = The ITPM Host Interface is disabled (default)

MCH_CFG_7 Intel(R) Management Engine Crypto
 Low = Intel(R) Management Engine Crypto
 High = Intel(R) Management Engine Crypto
 TLS cipher suite with no confidentiality
 High: Intel(R) Management Engine Crypto
 TLS cipher suite with no confidentiality (Default)

MCH_CFG_10 PCIe Lookback Enable
 Low = Enabled3
 High = Disabled (Default)

MCH_CFG_12/13 (XOR/ALLZ/CLOCK Un-gating)

MCH_CFG_13 MCH_CFG_12 Configuration

| | | |
|---|---|----------------------------|
| 0 | 0 | Reserved |
| 1 | 0 | XOR Mode enabled |
| 0 | 1 | All-Z Mode enabled |
| 1 | 1 | Normal operation (Default) |

MCH_CFG_20

| | | |
|---|---|----------------------------|
| 0 | 0 | Reserved |
| 1 | 0 | XOR Mode enabled |
| 0 | 1 | All-Z Mode enabled |
| 1 | 1 | Normal operation (Default) |

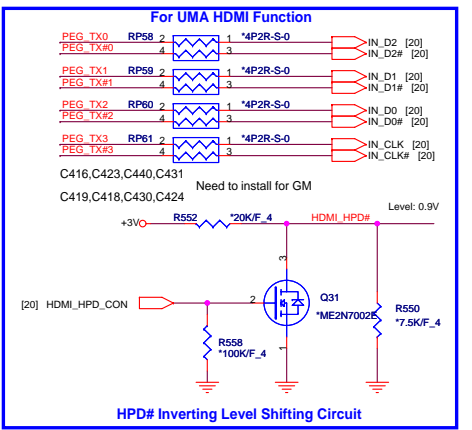
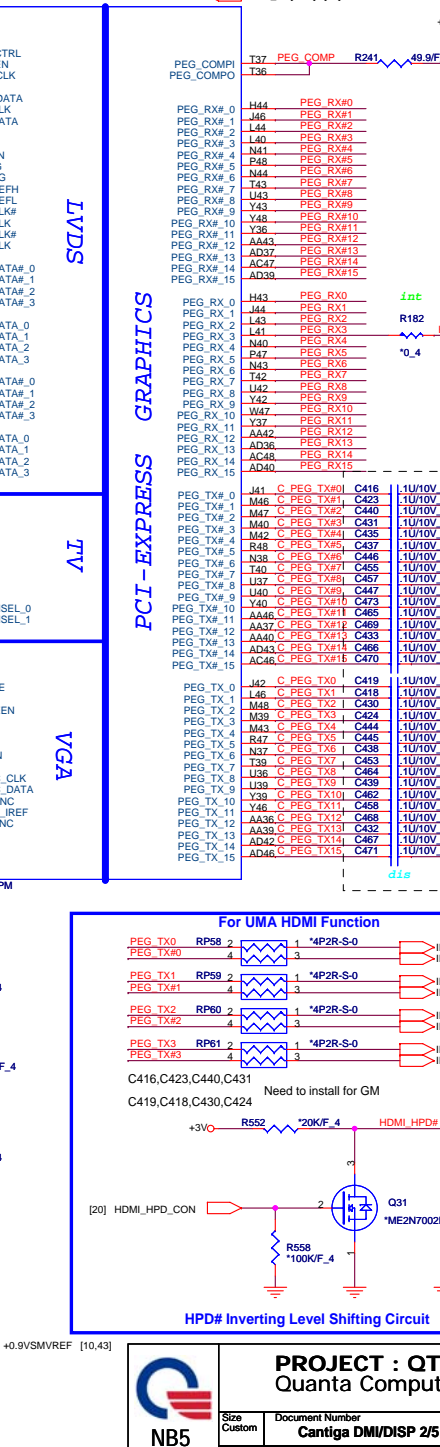
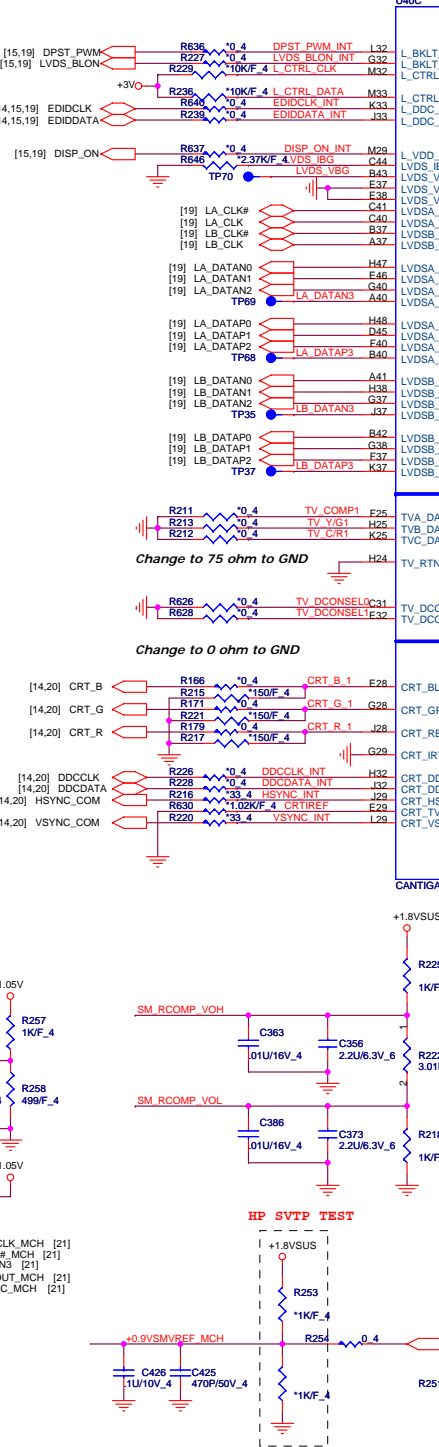
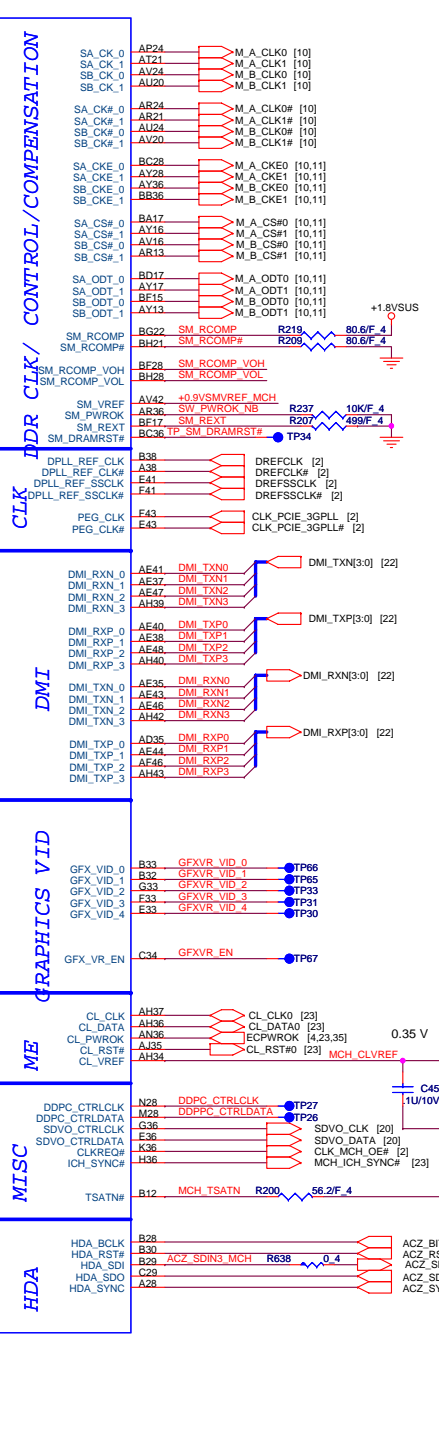
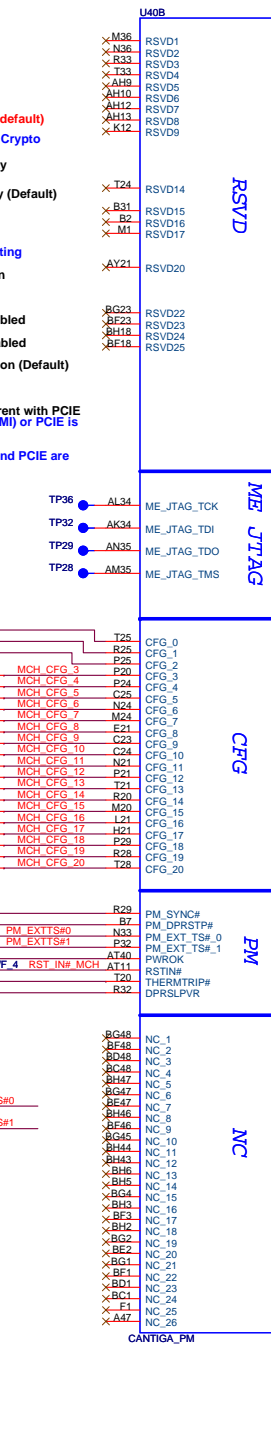
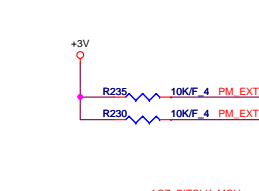
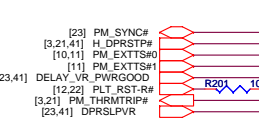
Digital Display Port (SDVO/DP/HDMI) Concurrent with PCIe
 Low = Only digital display port (SDVO/DP/HDMI) or PCIe is operational (default)
 High = Digital display port (SDVO/DP/HDMI) and PCIe are operating simultaneously with the DP port

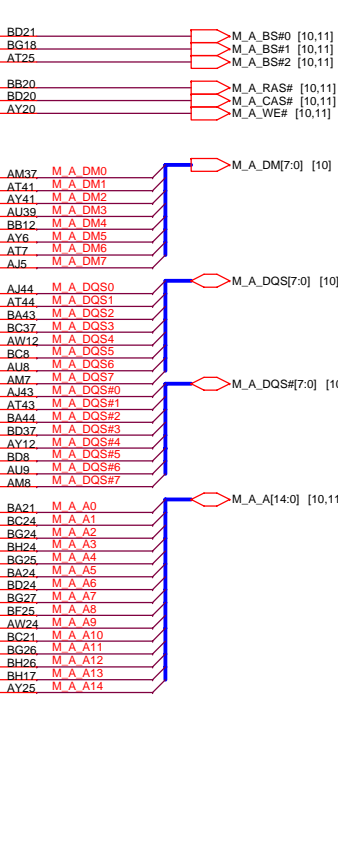
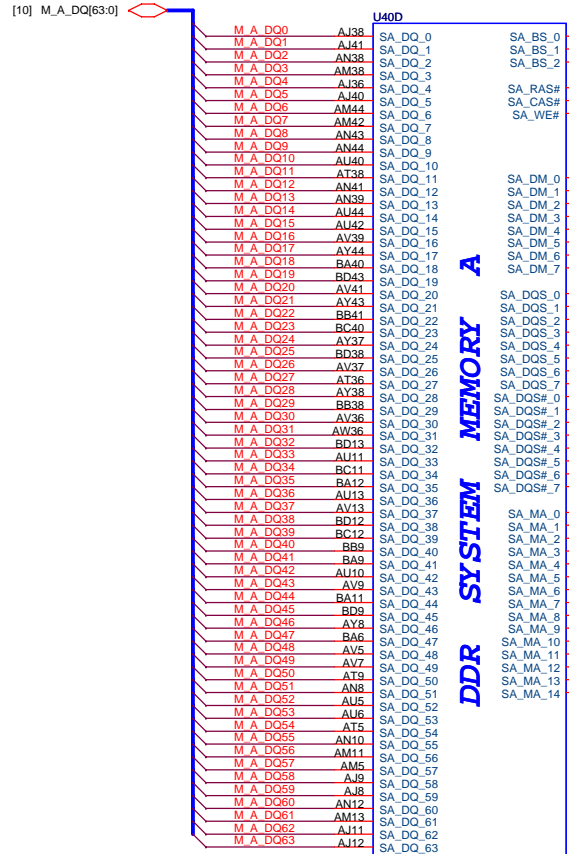
MCH_CFG:0

| |
|-------------------|
| 000 = FSB1066 |
| 010 = FSB800 |
| 011 = FSB667 |
| Others = Reserved |

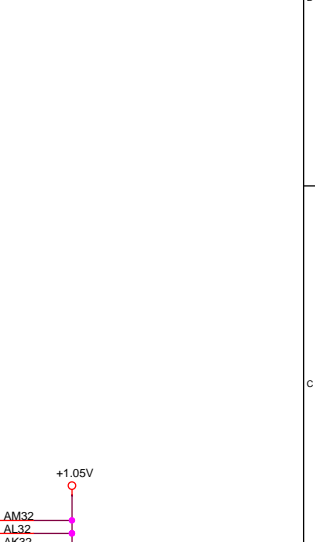
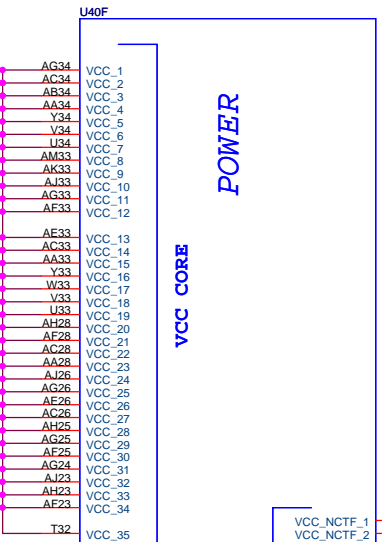
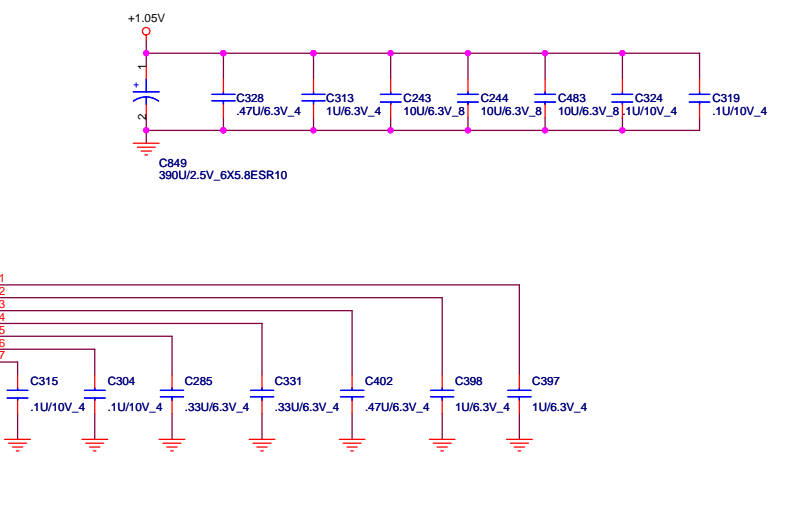
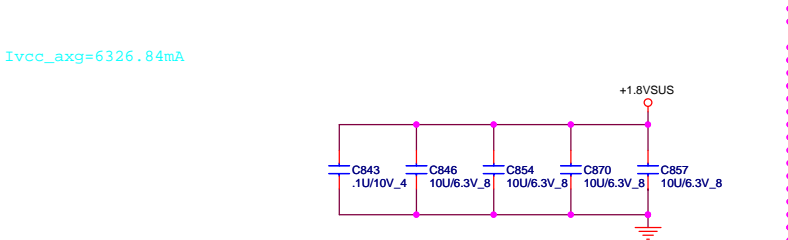
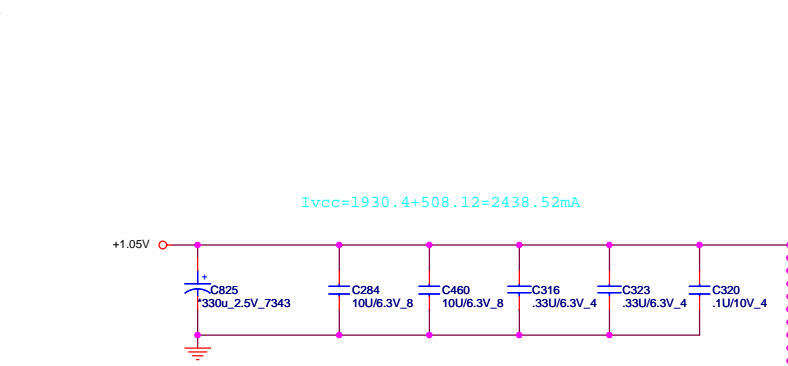
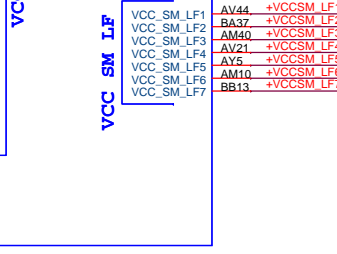
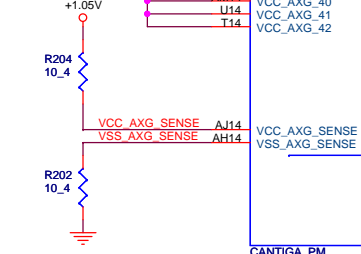
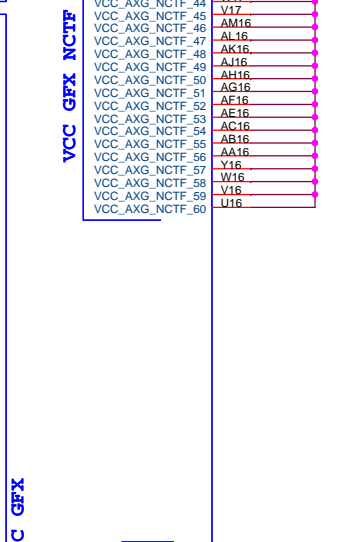
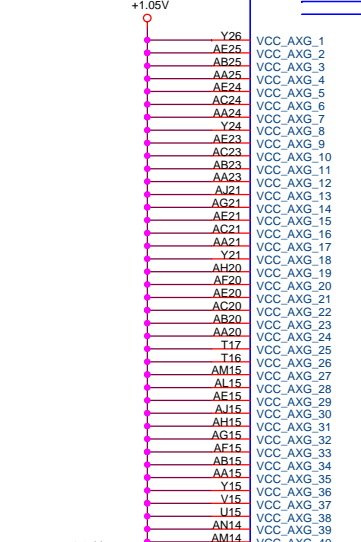
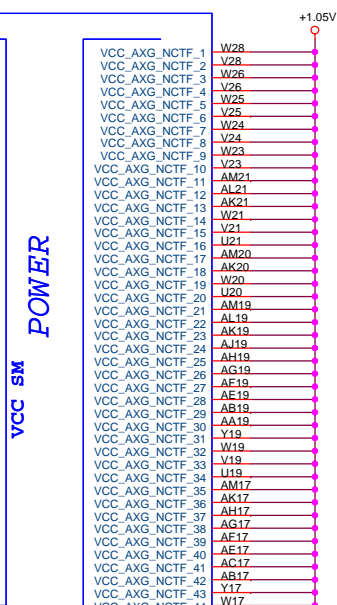
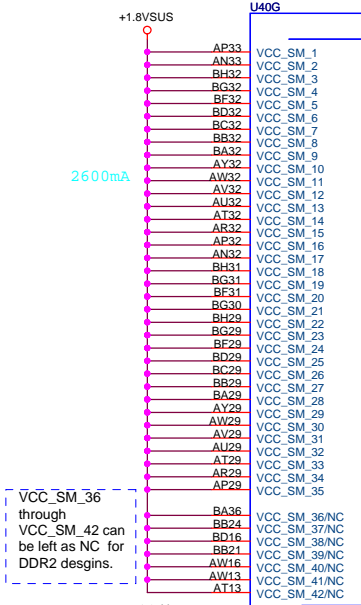
MCH_CFG:0

| | | |
|---------------|---------------|---------------|
| [2] MCH_BSEL0 | [2] MCH_BSEL1 | [2] MCH_BSEL2 |
|---------------|---------------|---------------|





[6,9,10,34,40,43] +1.8VSUS
[2,3,4,5,6,9,21,24,34,40,41] +1.05V

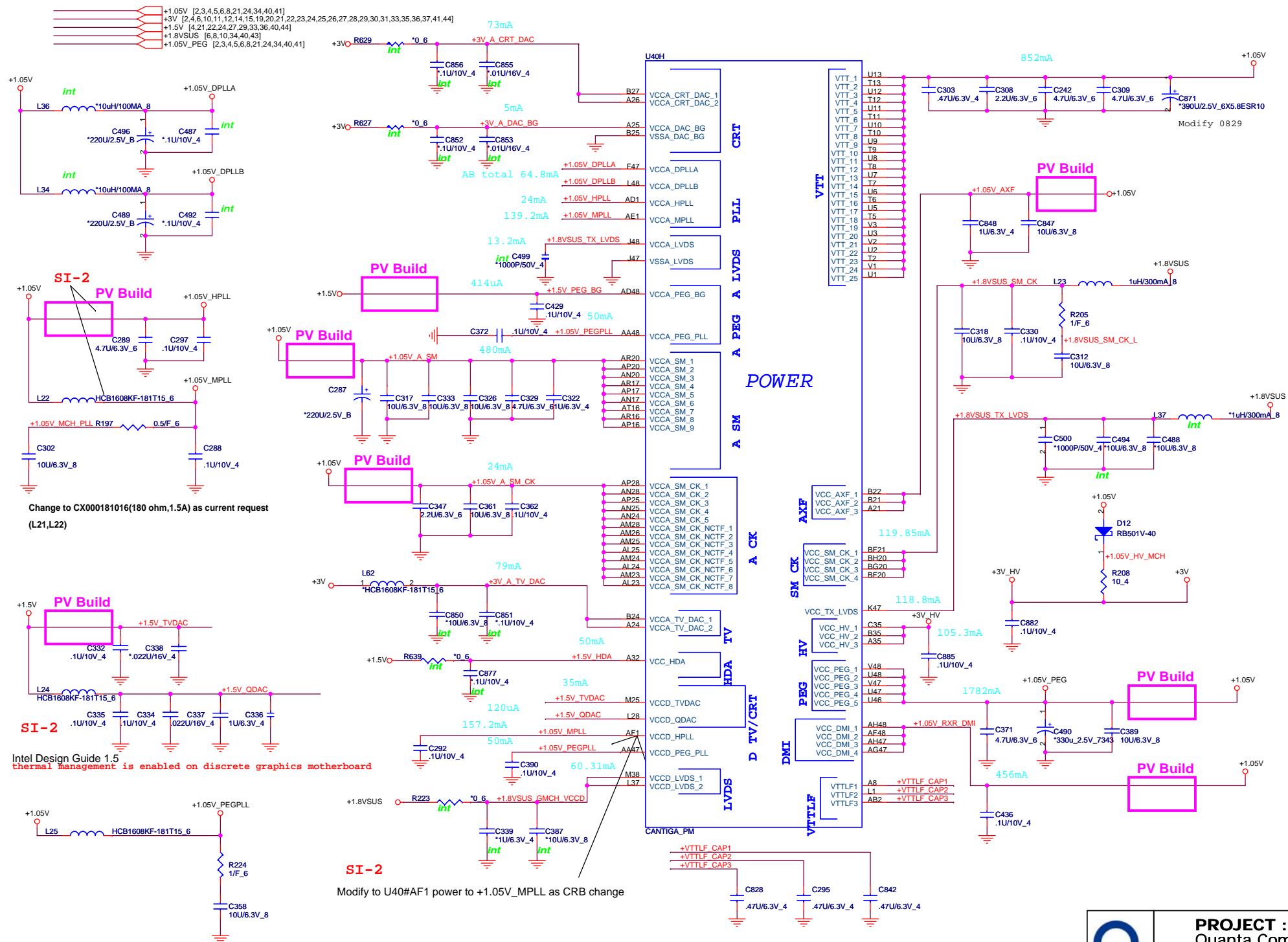


CANTIGA_PM



PROJECT : QT6
Quanta Computer Inc.

| | | |
|----------------------------------|---|--------|
| Size Custom | Document Number Cantiga Vcc 4/5 | Rev 1A |
| Date: Tuesday, February 26, 2008 | Sheet 8 of 44 | |



Change to CX000181016 (180 ohm, 1.5A) as current request (L21, L22)

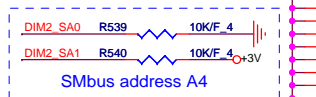
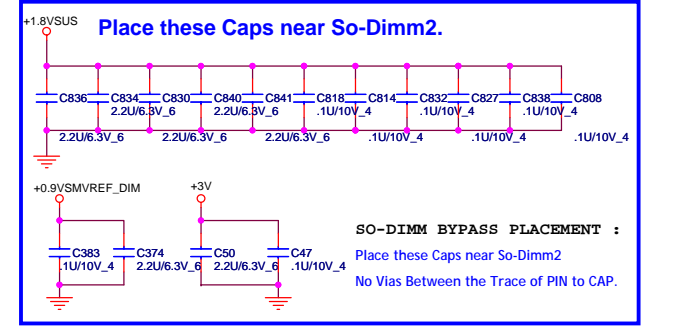
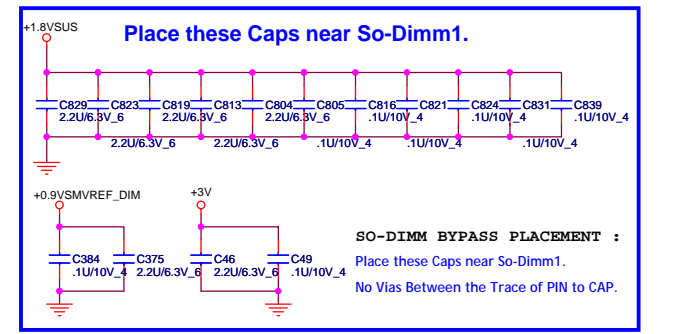
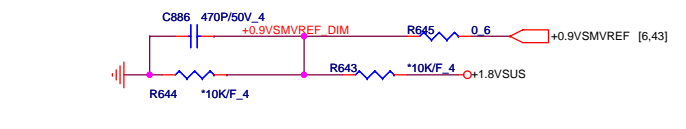
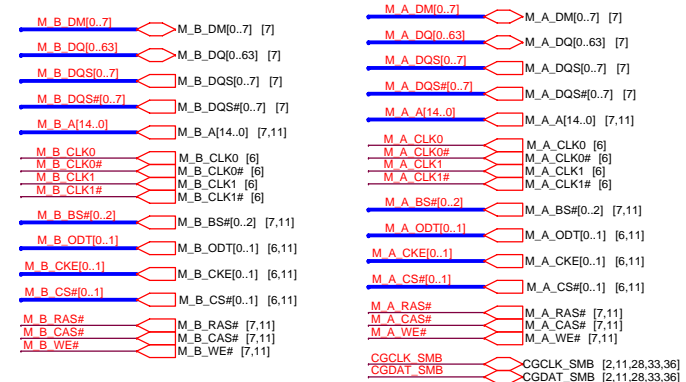
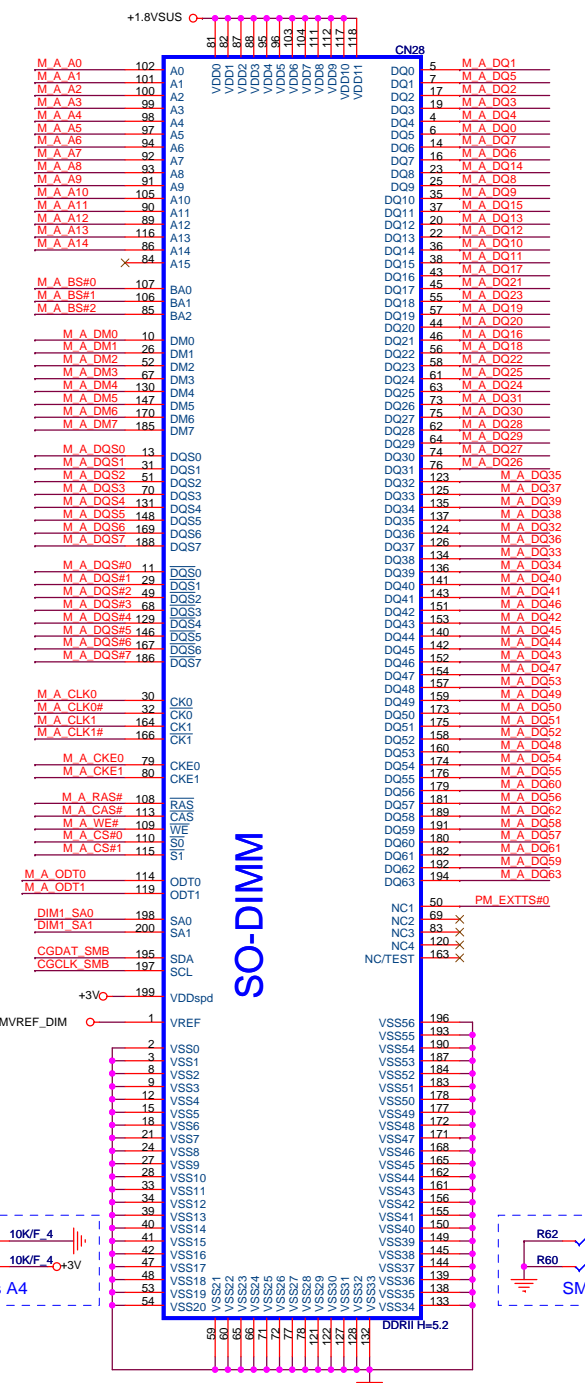
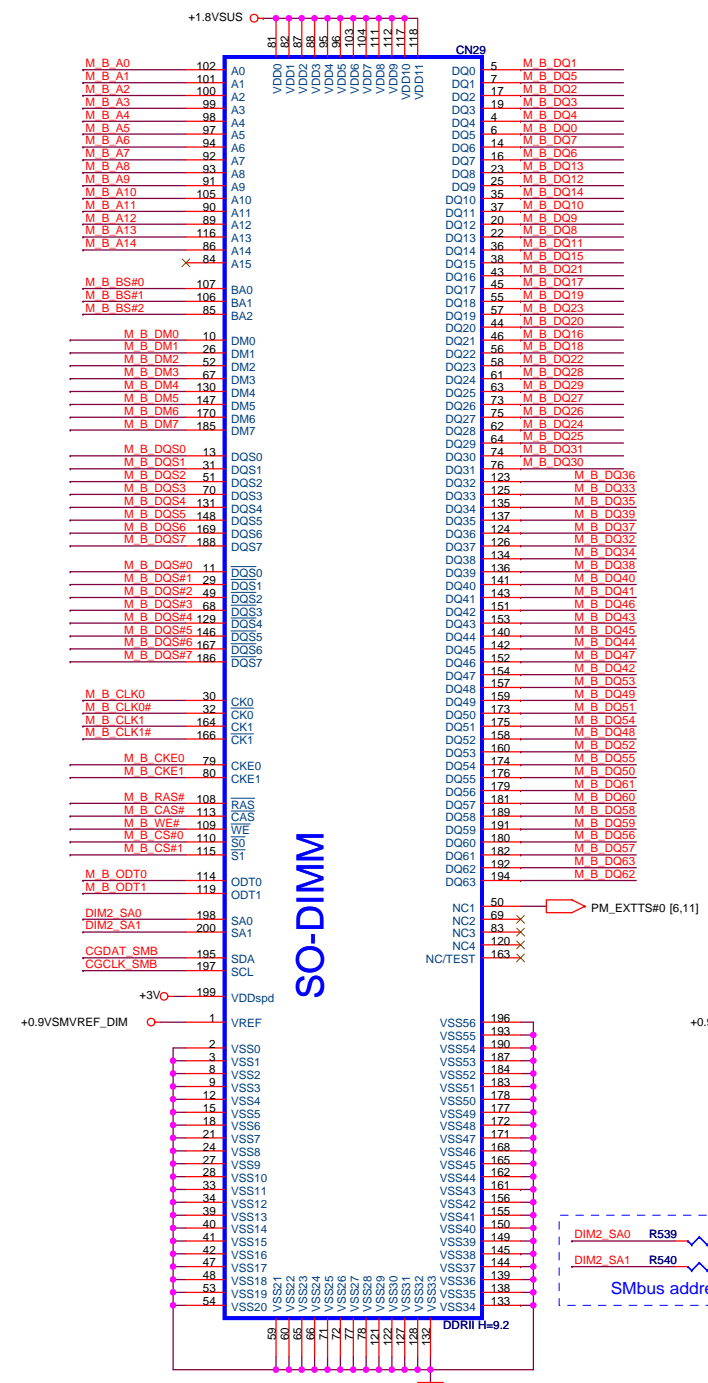
Intel Design Guide 1.5 thermal management is enabled on discrete graphics motherboard

SI-2
Modify to U40#AF1 power to +1.05V_MPLL as CRB change



PROJECT : QT6
Quanta Computer Inc.

| | | |
|----------------------------------|---|---------------|
| Size Custom | Document Number Cantiga Power 5/5 | Rev 3A |
| Date: Tuesday, February 26, 2008 | | Sheet 9 of 44 |



PROJECT : QT6
Quanta Computer Inc.

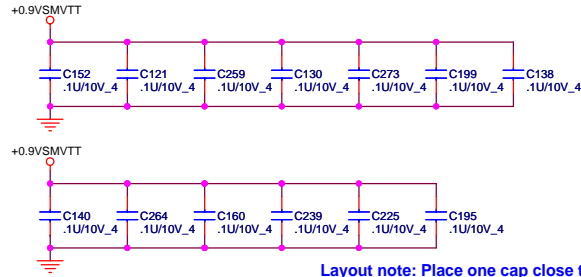
NB5

Size Custom Document Number **DDR2 DIMM** Rev 1A

Date: Tuesday, February 26, 2008 Sheet 10 of 44

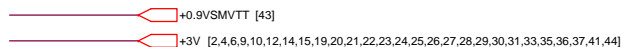
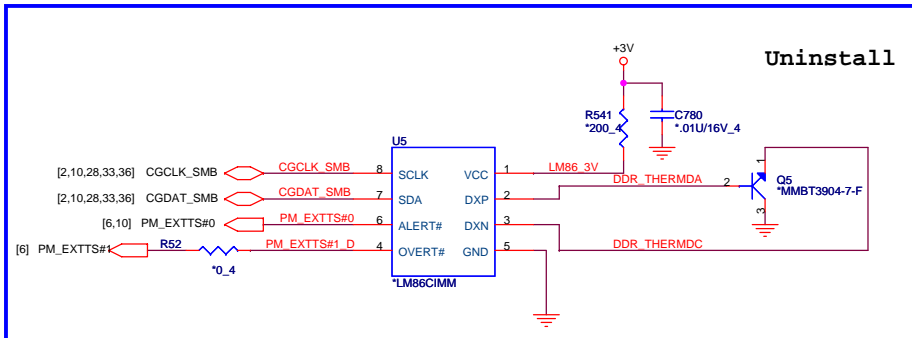
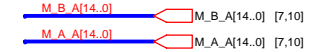
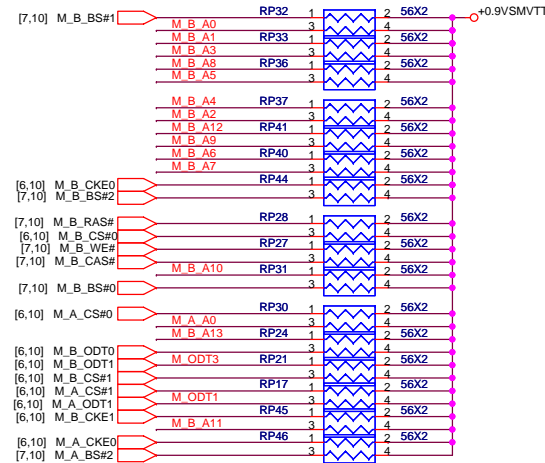
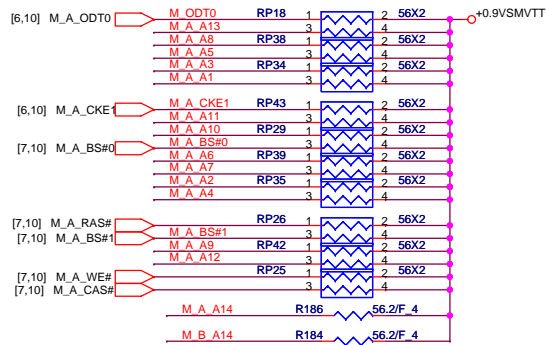
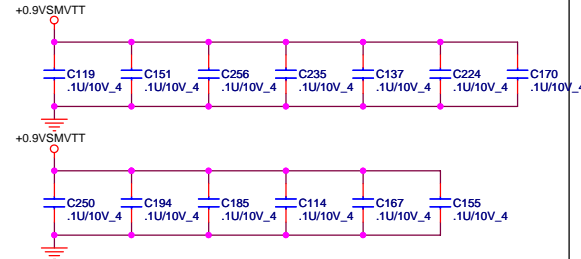
DDRII DUAL CHANNEL A,B.

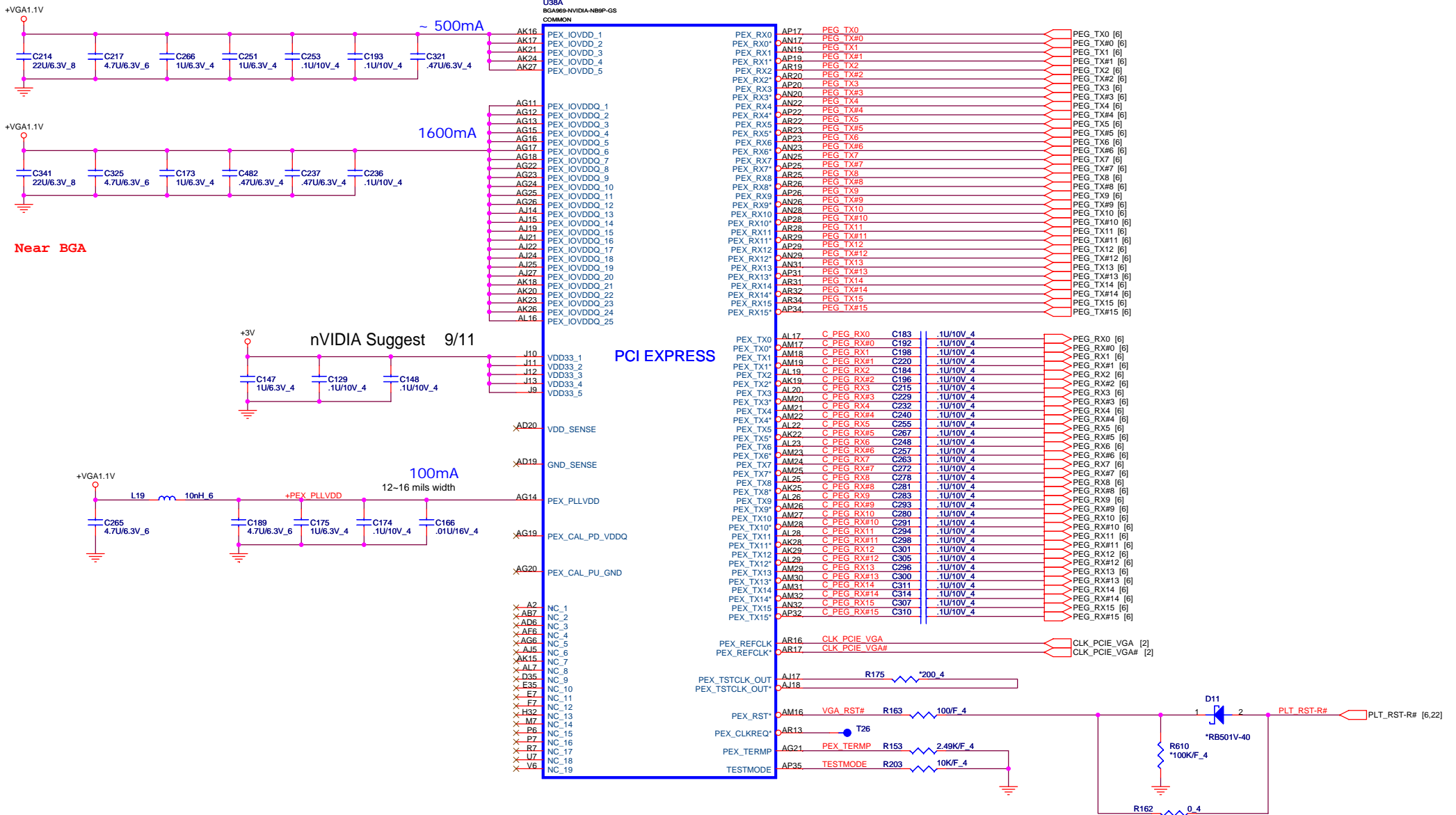
DDRII A CHANNEL

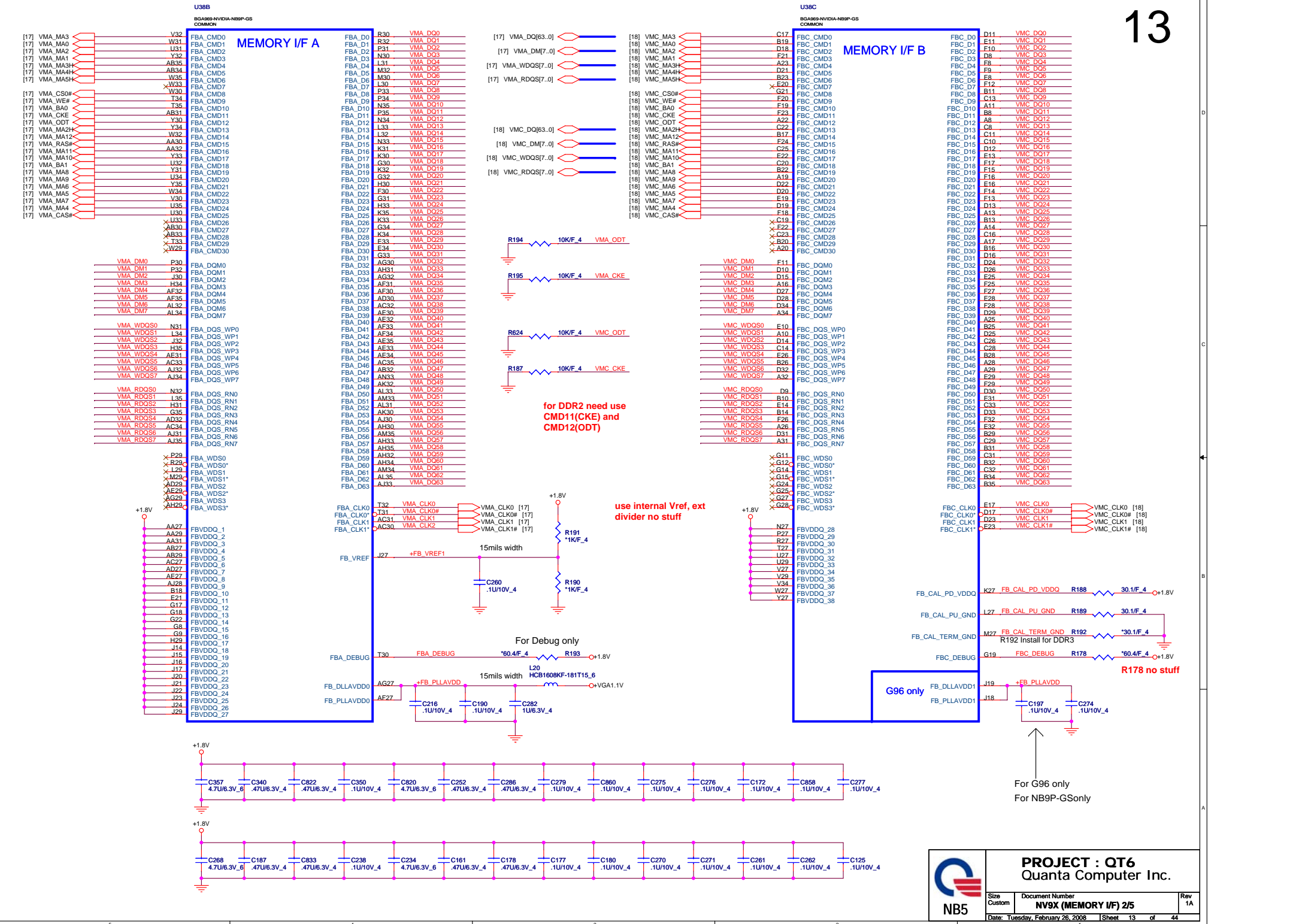


Layout note: Place one cap close to every 2 pullup resistors terminated to SMDR_VTERM

DDRII B CHANNEL







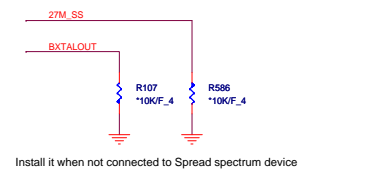
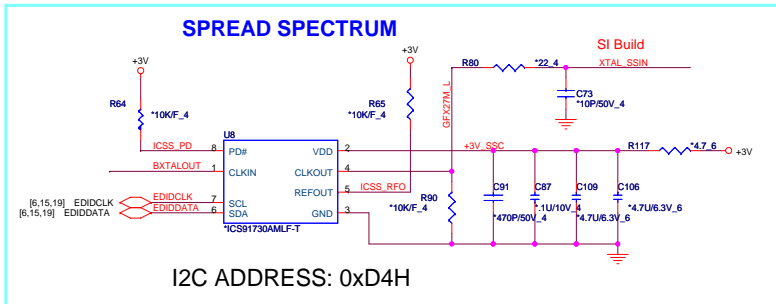
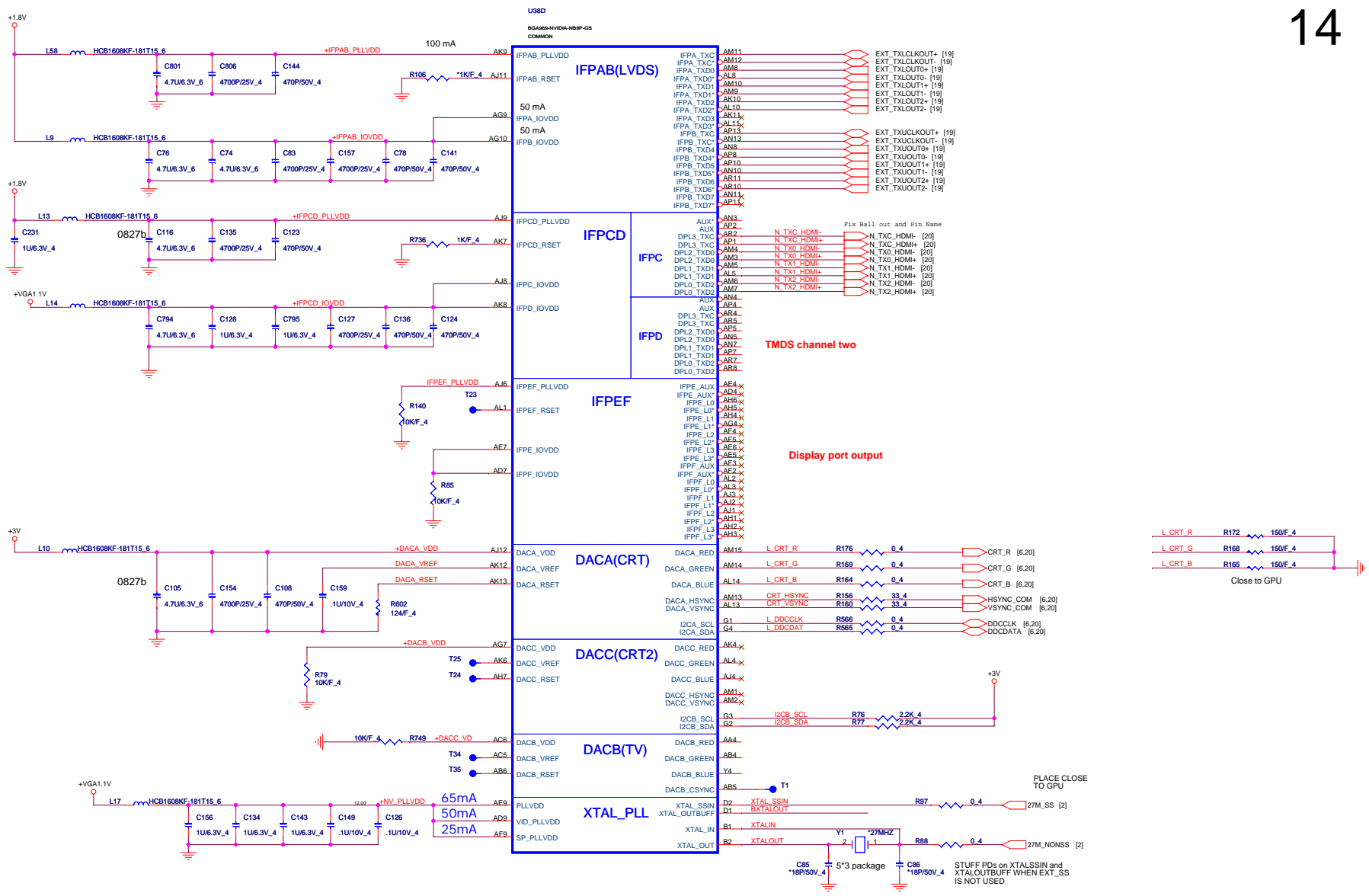
for DDR2 need use
CMD11(CKE) and
CMD12(ODT)

use internal Vref, ext
divider no stuff

G96 only

For G96 only
For NB9P-GSonly

| | | |
|----------------------------------|----------------------|----------------|
| | PROJECT : QT6 | |
| | Quanta Computer Inc. | |
| Size Custom | Document Number | Rev 1A |
| NB9X (MEMORY I/F) 2/5 | | |
| Date: Tuesday, February 26, 2008 | | Sheet 13 of 44 |



NB9P-GS (G96) Straps NB9M-GE (G98) Straps GPIO ASSIGNMENTS

| GPIO | I/O | ACTIVE | USAGE |
|------|-----|--------|------------------------|
| 0 | IN | N/A | PRIMARY DVI HOTPLUG |
| 1 | IN | N/A | SECONDARY DVI HOTPLUG |
| 2 | OUT | HIGH | PANEL BACKLIGHT PWM |
| 3 | OUT | HIGH | PANEL POWER ENABLE |
| 4 | OUT | HIGH | PANEL BACKLIGHT ENABLE |
| 5 | OUT | N/A | NV_VDD VID0 |
| 6 | OUT | N/A | NV_VDD VID1 |
| 7 | OUT | N/A | FB_VDD VID0 |
| 8 | IN | LOW | THERMAL ALERT |
| 9 | OUT | LOW | FAN PWM |
| 10 | OUT | N/A | FBVREF SELECT |
| 11 | OUT | N/A | SLI SYNC0 |
| 12 | IN | N/A | AC DETECT |
| 13 | OUT | LOW | PS CONTROL OR HDMI_CEC |
| 14 | OUT | HIGH | PS CONTROL |

SEE Datasheet for details on G9x Straps!

Logical Strap Bit Mapping

| | PU-VDD | PD |
|-----|--------|------|
| 5K | 1000 | 0000 |
| 10K | 1001 | 0001 |
| 15K | 1010 | 0010 |
| 20K | 1011 | 0011 |
| 25K | 1100 | 0100 |
| 30K | 1101 | 0101 |
| 35K | 1110 | 0110 |
| 45K | 1111 | 0111 |

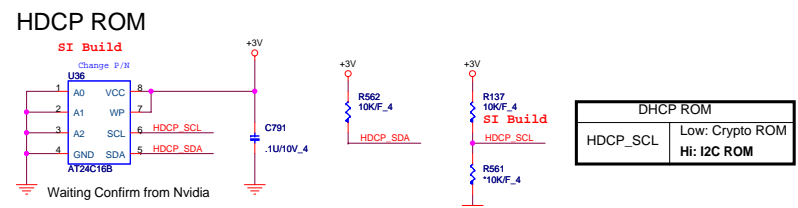
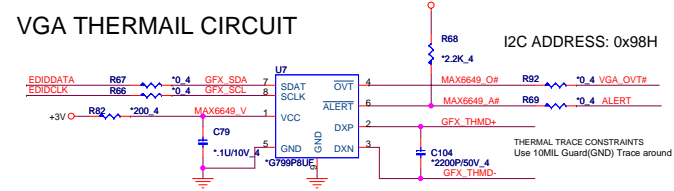
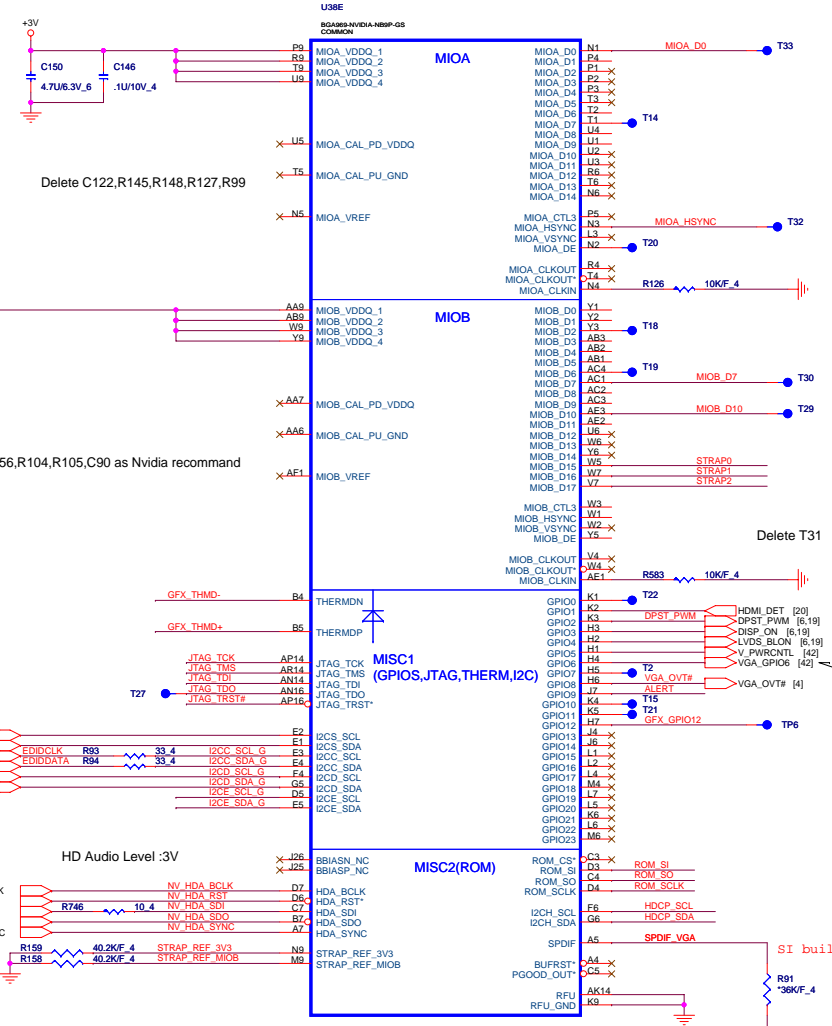
| | Logical Strapping Bit3 | Logical Strapping Bit2 | Logical Strapping Bit1 | Logical Strapping Bit0 | |
|----------|------------------------|------------------------|------------------------|------------------------|------|
| ROM_SO | XCLK_277 | TVMODE[2] | TVMODE[1] | TVMODE[0] | 1000 |
| ROM_SCLK | PCI_DEVIDE[4] | SUB_VENDOR | SLOT_CLK_CFG | PEX_PLL_EN_TERM100 | 0010 |
| ROM_SI | RAMCFG[3] | RAMCFG[2] | RAMCFG[1] | RAMCFG[0] | XXXX |
| STRAP2 | PCI_DEVID[3] | PCI_DEVID[2] | PCI_DEVID[1] | PCI_DEVID[0] | XXXX |
| STRAP1 | 3GIO_PADCFG[3] | 3GIO_PADCFG[2] | 3GIO_PADCFG[1] | 3GIO_PADCFG[0] | 0001 |
| STRAP0 | USER[3] | USER[2] | USER[1] | USER[0] | 1111 |

PCI_DEVID: **STRAP2 R554**
 NB9M-GE 0x06E 8 1000 PU 5K
 NB9M-GS 0x06E 9 1001 PU 10K
 NB9P-GE2 0x064 8 1000 PU 5K
 NB9P-GS 0x064 9 1001 PU 10K

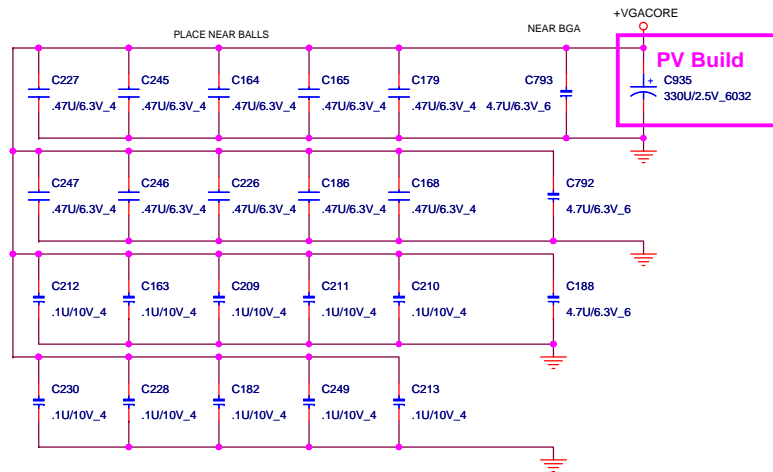
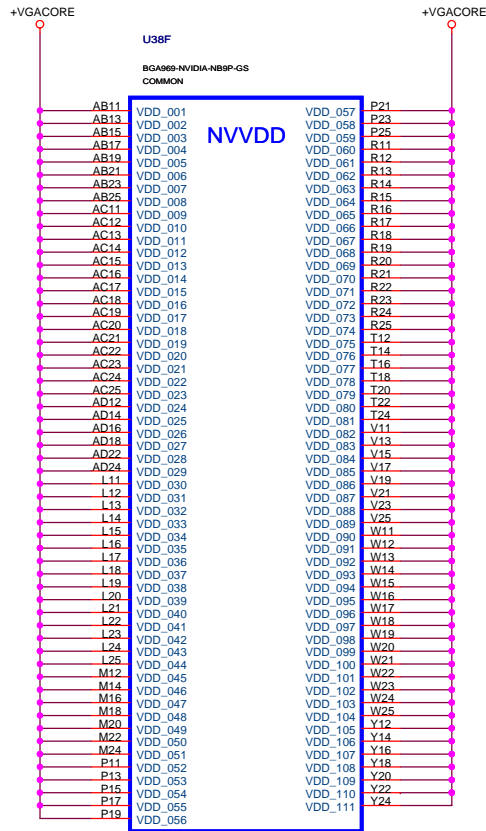
CS33572FB13 RES CHIP 35.7K 1/16W +-1% (0402)
 CS34532FB18 RES CHIP 45.3K 1/16W +-1% (0402)
RAM ID: ROM_SI R585
 SAM 0101 PD 30.1K
 QIM 0110 PD 35.7K
 HYN 0111 PD 45.3K

NB9X VRAM Configuration Table

| RAM_CFG[3:0] | DESCRIPTION | Vendor |
|--------------|------------------------------|----------|
| 0111 | DDR2 32Mx16x8, 128bit, 512MB | Hynix |
| 0110 | DDR2 32Mx16x8, 128bit, 512MB | Gilmonda |
| 0101 | DDR2 32Mx16x8, 128bit, 512MB | Samsung |
| other | Reserved | |

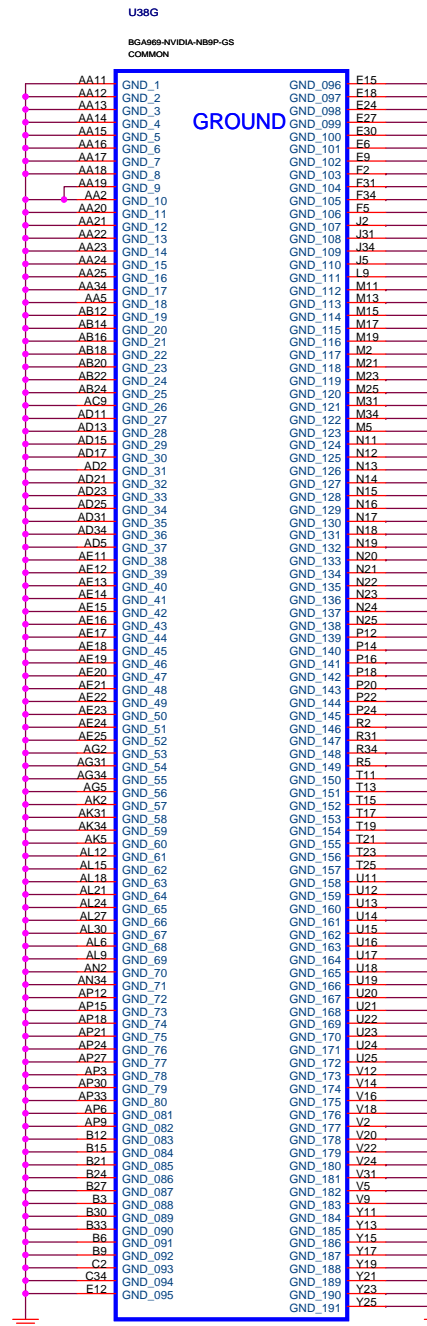
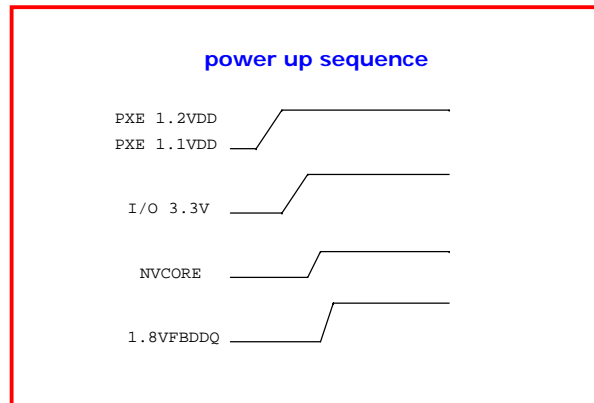


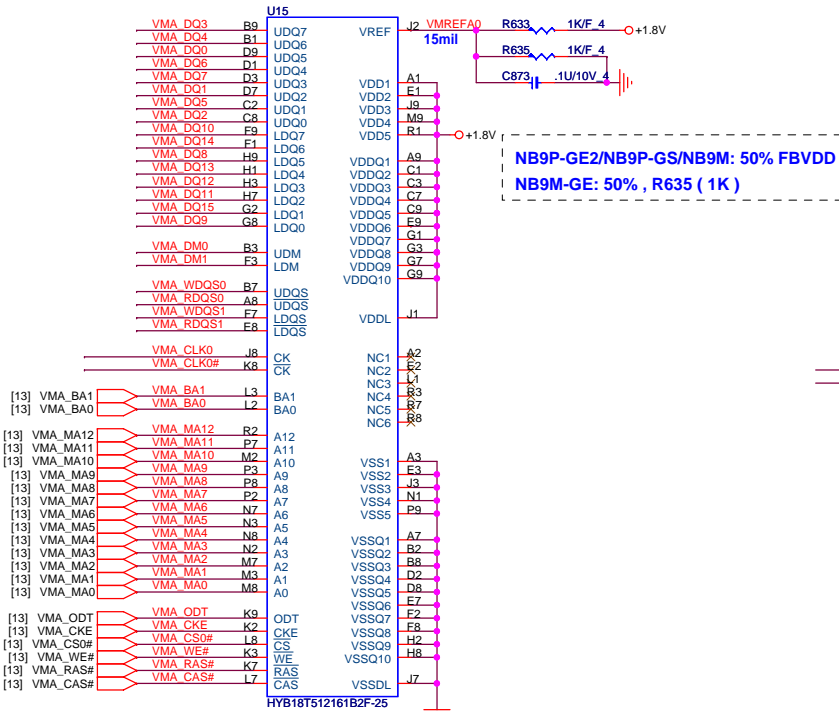
NVVDD Decoupling



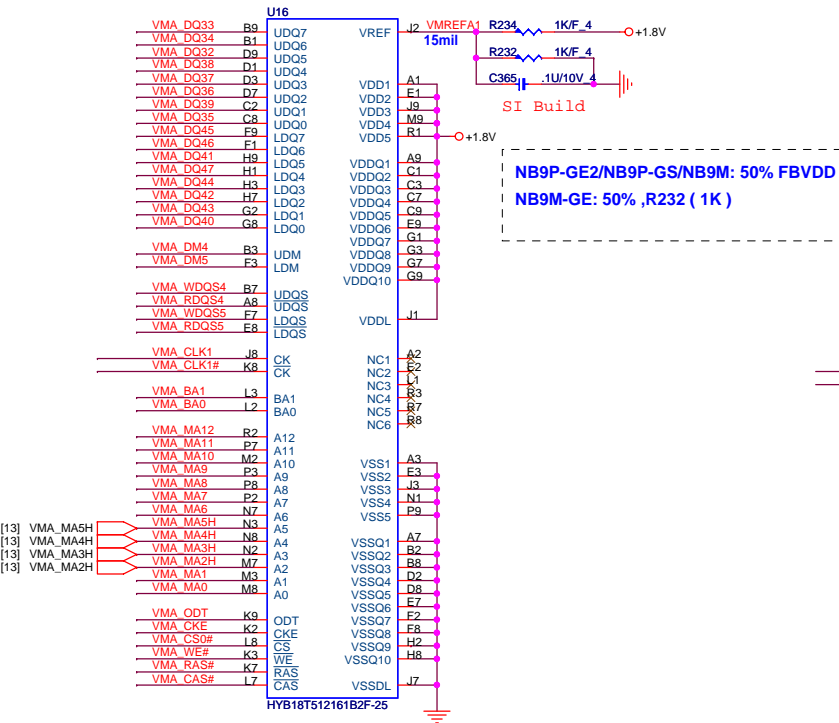
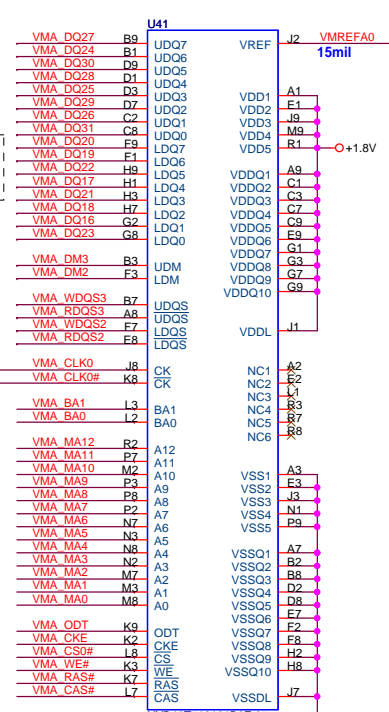
Follow Design Guide DG-03276-001 4.7uF x3 and 0.47x10 uF instead of 0.1uF x10

NB9M: VGACORE +0.90V (Normal) , +1.09V

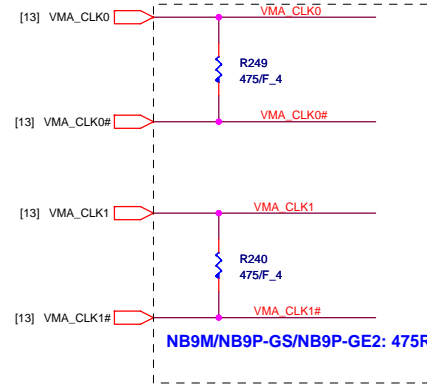
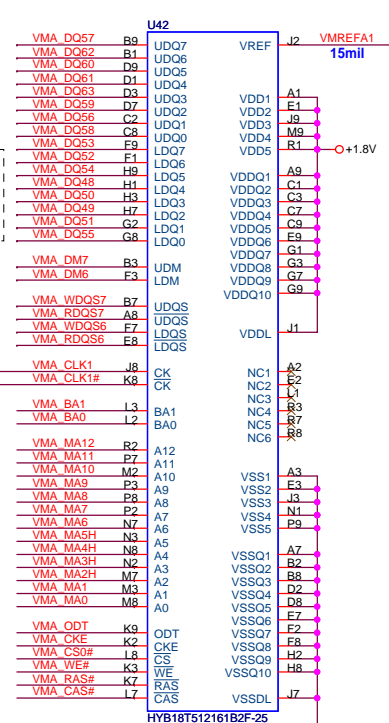




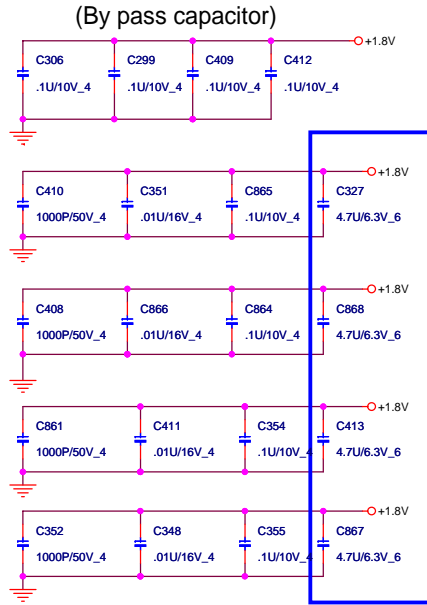
NB9P-GE2/NB9P-GS/NB9M: 50% FBVDD
 NB9M-GE: 50%, R635 (1K)



NB9P-GE2/NB9P-GS/NB9M: 50% FBVDD
 NB9M-GE: 50%, R232 (1K)



CS14752FB11 RES CHIP 475 1/16W +-1%(0402)

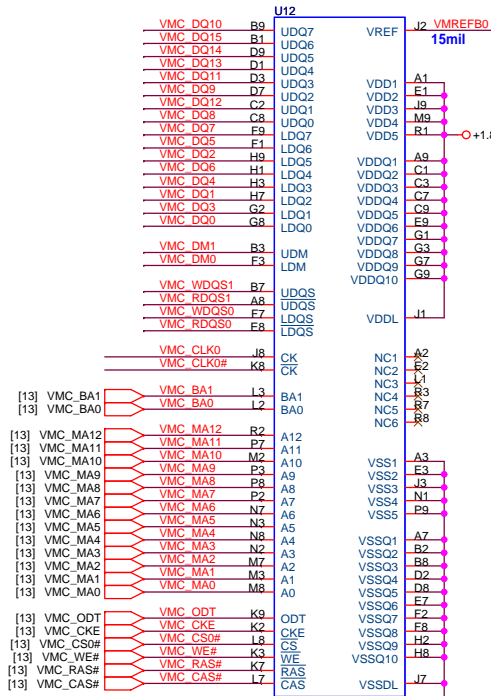


- For DB:
- NB9P : AKD59G-T502(Samsung,32M*16)
 - NB9M : AKD5FG-TW31(Hynix,32M*16)
 - AKD5FG-T*03(Qimonda 32M*16)
 - 256Mb : AKD5JGAT*05
 - 512Mb : AKD59G-T*01

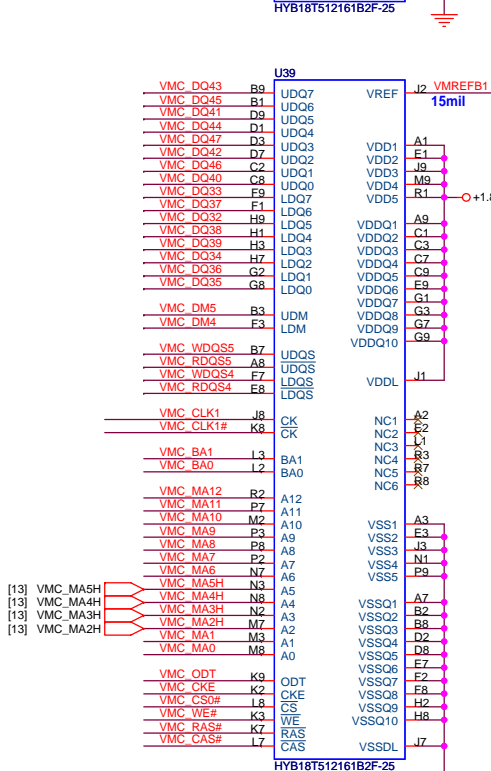


PROJECT : QT6
 Quanta Computer Inc.

| | | |
|----------------------------------|--|--------|
| Size Custom | Document Number NV9X VRAM-1(GDDR2 BGA84) | Rev 1A |
| Date: Tuesday, February 26, 2008 | Sheet 17 of 44 | |



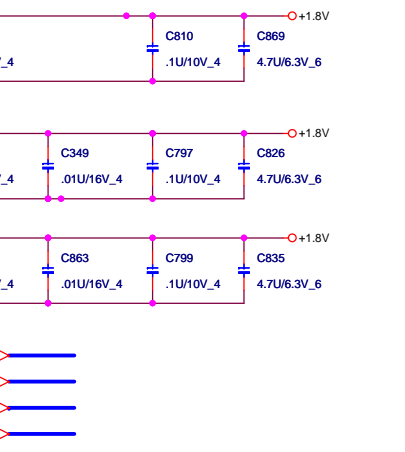
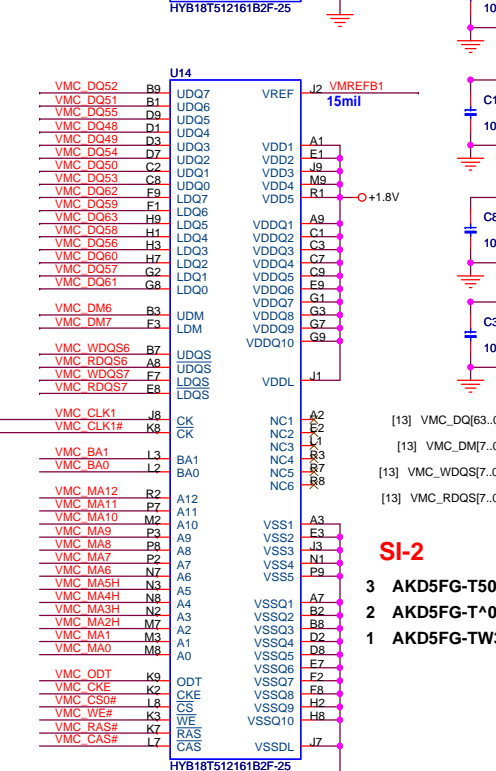
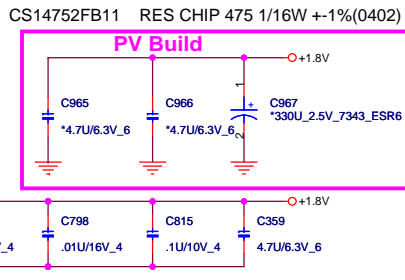
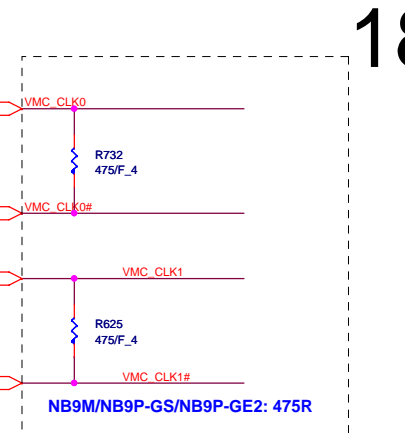
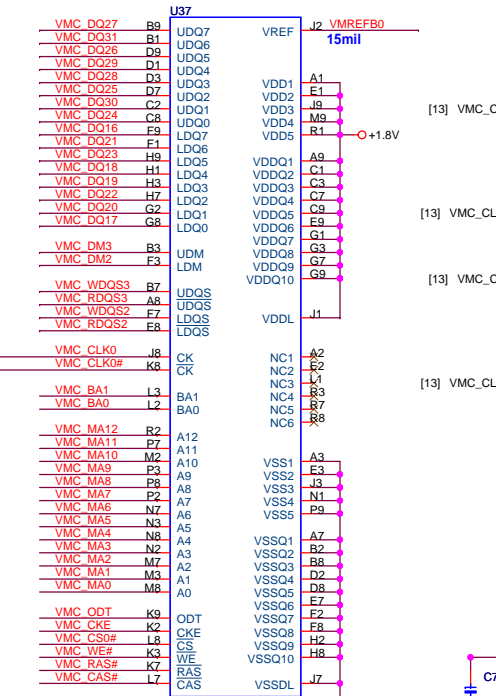
NB9P-GE2/NB9P-GS/NB9M: 50% FBVDD
NB9M-GE: 50%, R133 (1K)



NB9P-GE2/NB9P-GS/NB9M: 50% FBVDD
NB9M-GE: 50%, R632 (1K)

VRAM Vendor

| | | |
|---------|---|---|
| NB9M-GE | 1 | 3 |
| NB9P-GS | 2 | |



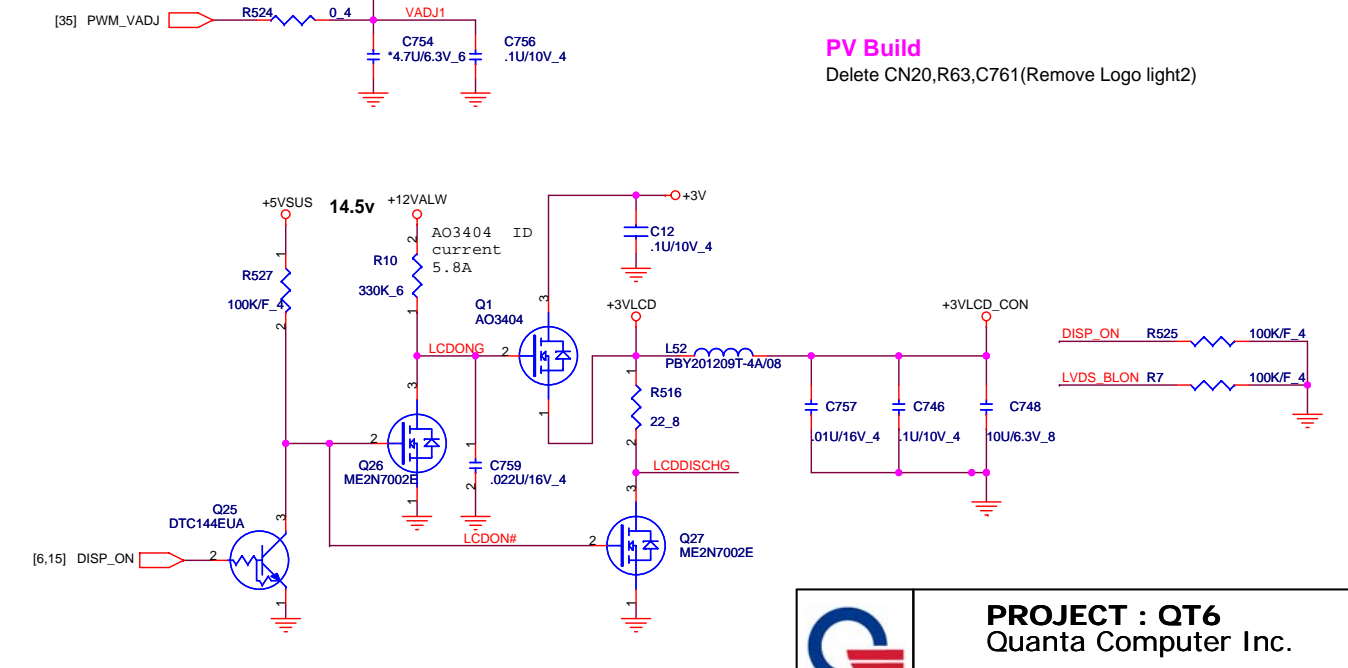
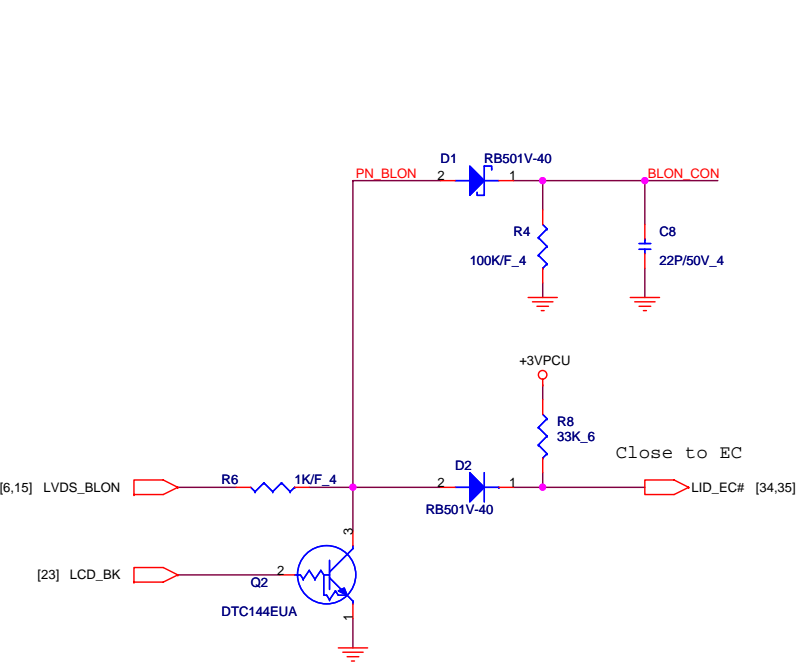
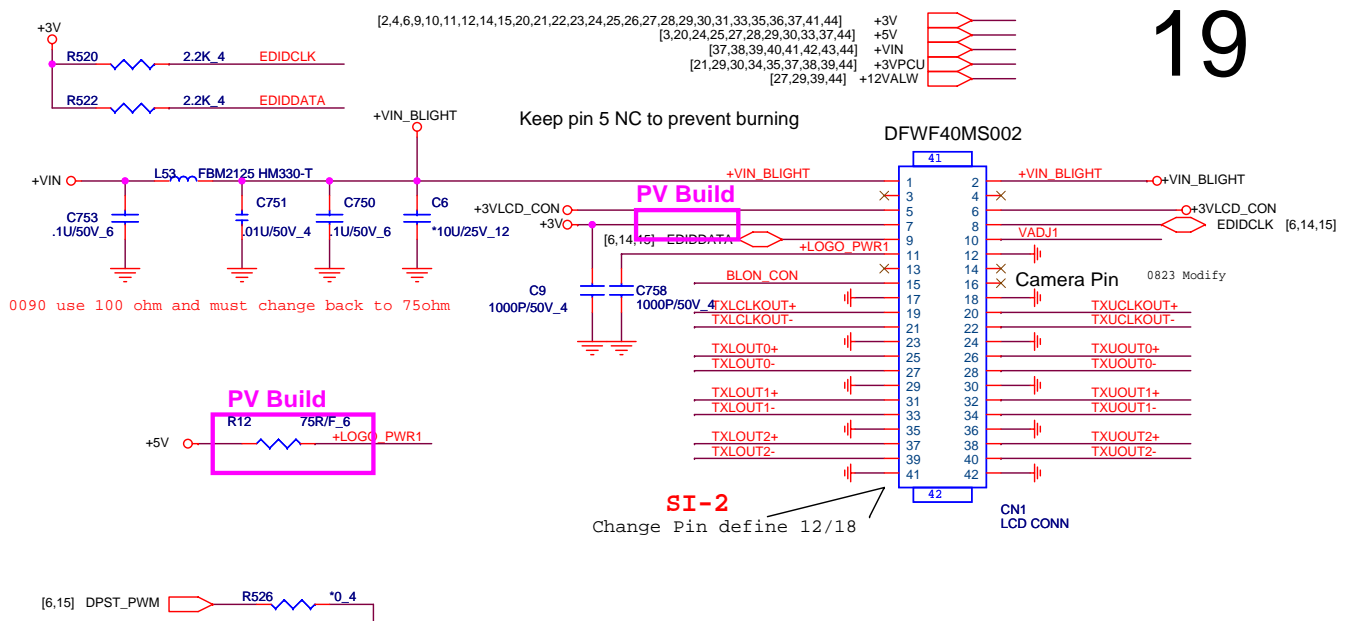
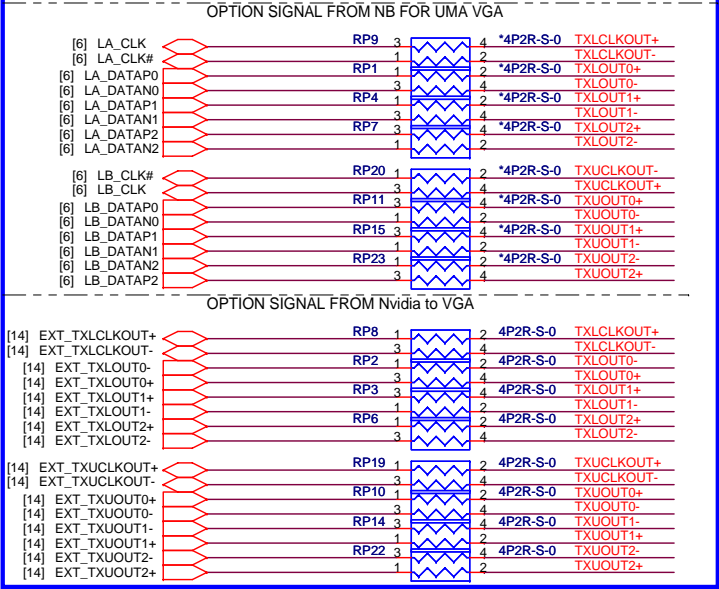
SI-2

| | | | |
|---|-------------|---------------------------------------|---------|
| 3 | AKD5FG-T501 | IC SDRAM(84P) K4N51163QG-HC25(FBGA) | Samsung |
| 2 | AKD5FG-T*03 | IC SDRAM(84P)HYB18T512161B2F-25(FBGA) | Qimonda |
| 1 | AKD5FG-TW31 | IC SDRAM(84P) HY5PS121621CFP-25(FBGA) | Hynix |

PROJECT : QT6
Quanta Computer Inc.

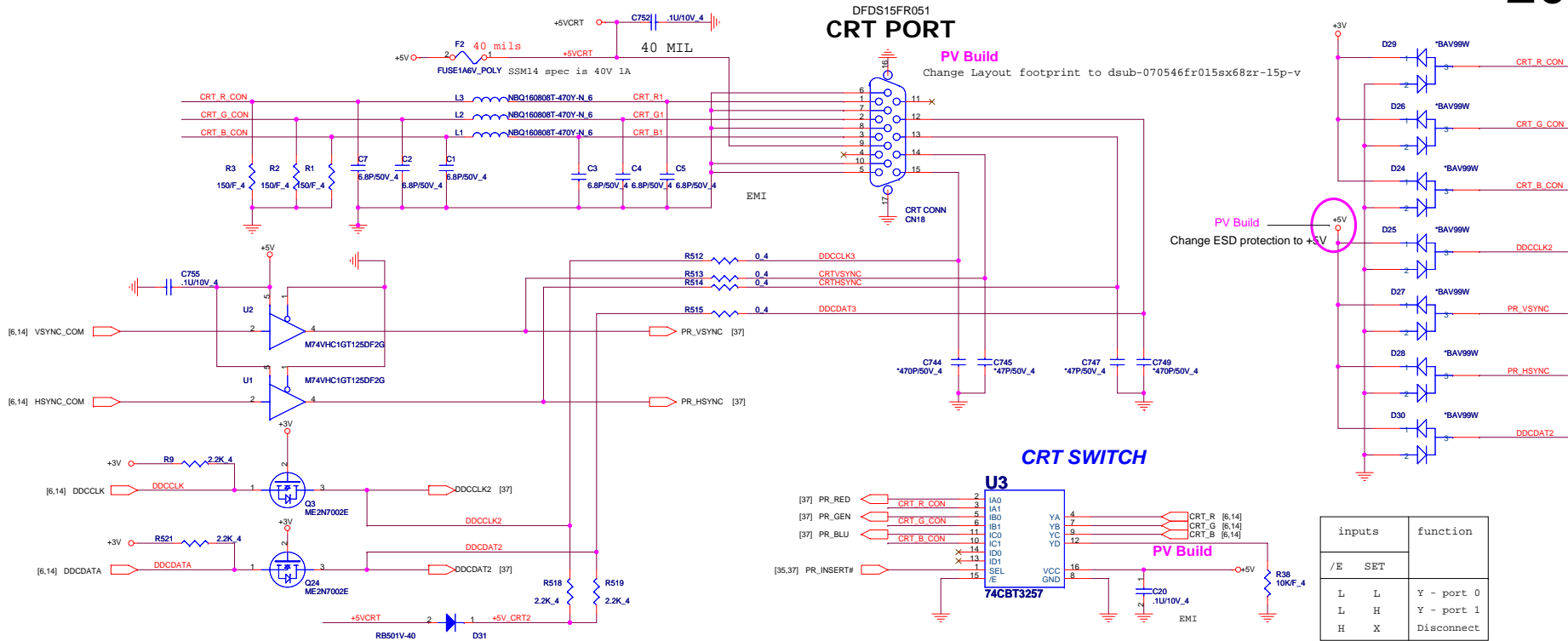
| | | |
|----------------------------------|--|--------|
| Size Custom | Document Number NV9X VRAM-2(GDDR2 BGA84) | Rev 1A |
| Date: Tuesday, February 26, 2008 | Sheet 18 of 44 | |

1. If LCD connector near GPU, then place these series Resistors near GPU
2. If LCD connector near N/B, then place these series Resistors near N/B

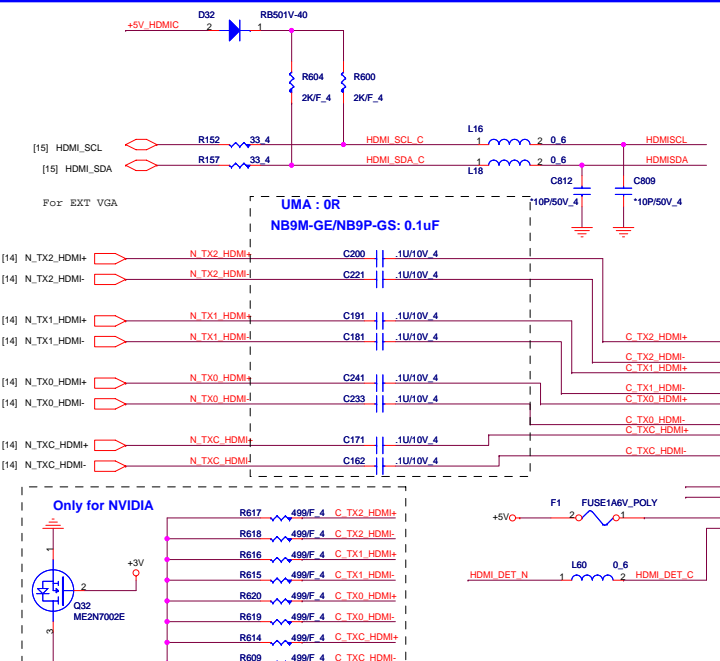
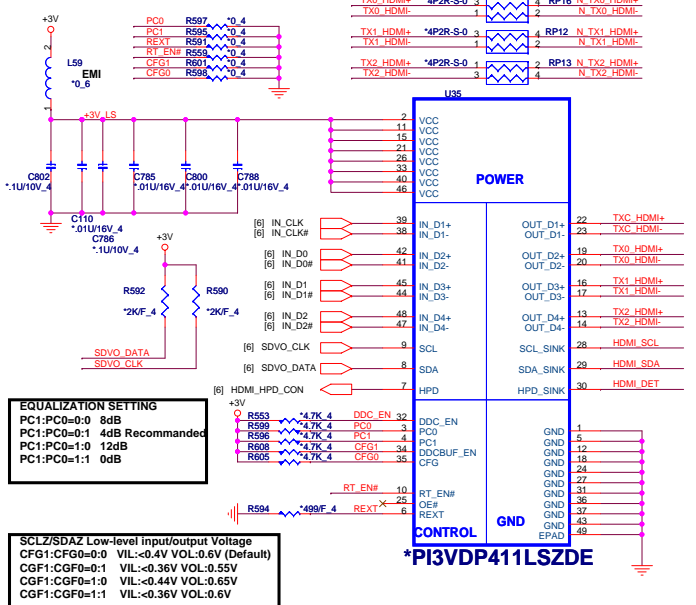


PROJECT : QT6
Quanta Computer Inc.

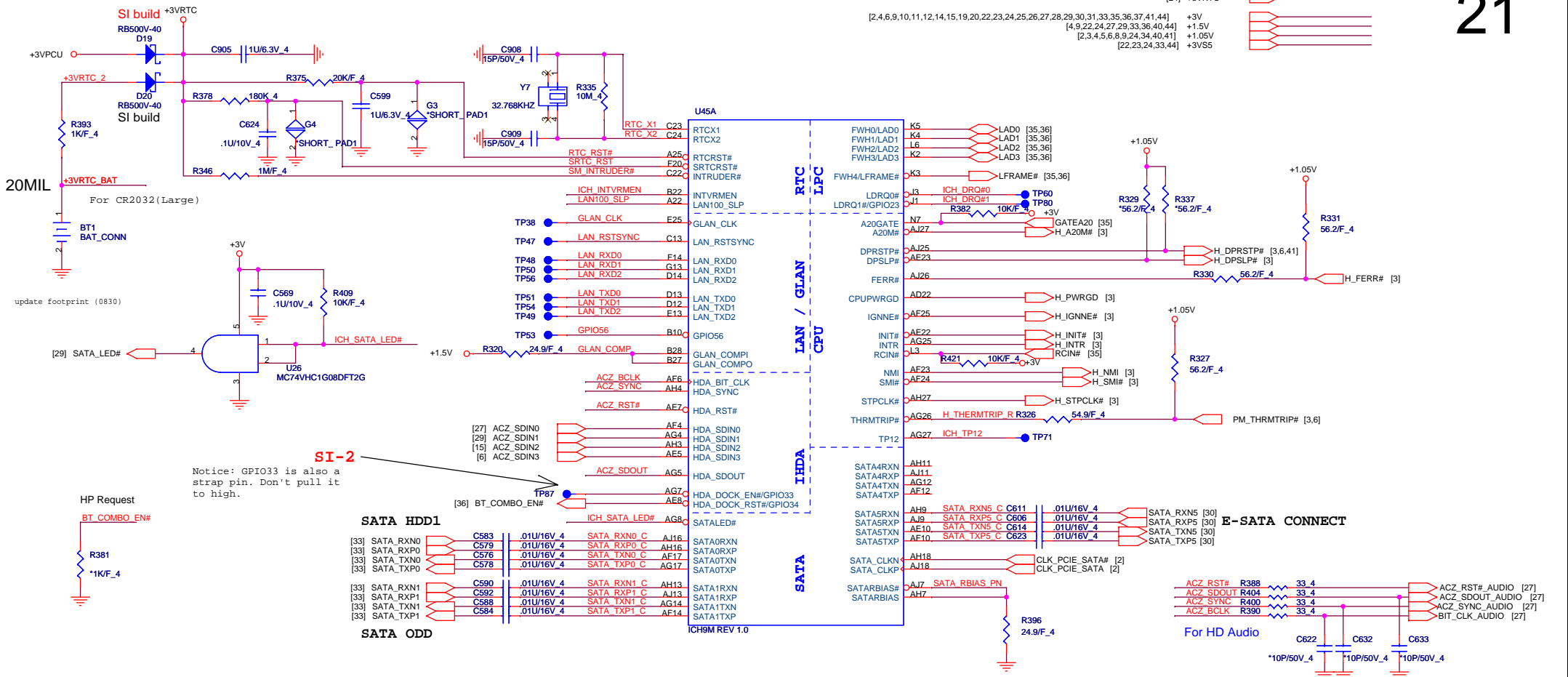
| | | |
|----------------------------------|-----------------|--------|
| Size B | Document Number | Rev 3A |
| LCD CONN/Lid function | | |
| Date: Tuesday, February 26, 2008 | Sheet 19 | of 44 |



For UMA HDMI function



HDMI PORT

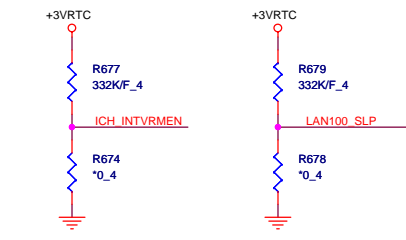


SB Strap

ICH9-M Internal VR Enable strap
(Internal VR for VccLAN1_05 and VccSus1_05, VccSus1_5 and VccCL1_5)

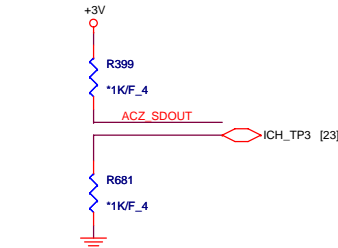
ICH9-M LAN100_SLP Strap
(Internal VR for VccLAN1_05 and VccCL1_05)

| | |
|------------|---|
| INTVRMEN | Low = Internal VR disable High = Internal VR enable(Default) |
| LAN100_SLP | Low = Internal VR disable High = Internal VR enable(Default) |



XOR Chain Entrance Strap

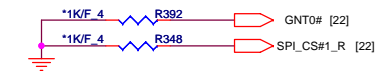
| ICH_TP3 | HDA_SDOUT | Description |
|---------|-----------|----------------------------|
| 0 | 0 | RSVD |
| 0 | 1 | Enter XOR Chain |
| 1 | 0 | Normal operation(Default) |
| 1 | 1 | Set PCIe port config bit 1 |



ICH9 Boot BIOS select

| STRAP | PCI_GNT0# | SPL_CS#1 |
|-------|-----------|----------|
| SPI | 0 | 1 |
| PCI | 1 | 0 |
| LPC | 1 | 1 |

(default)



A16 swap override strap

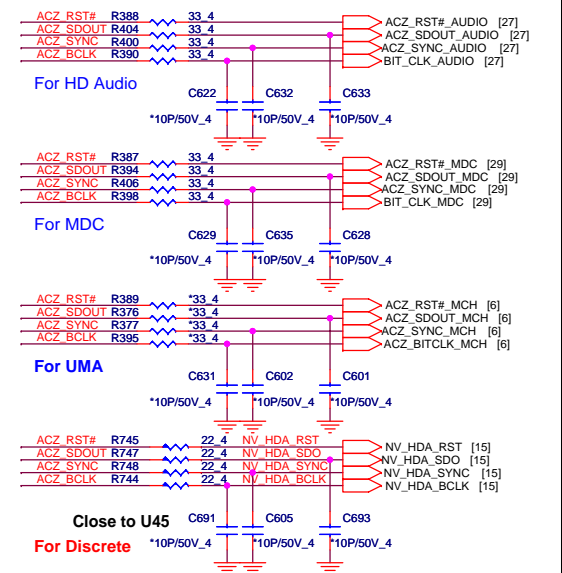
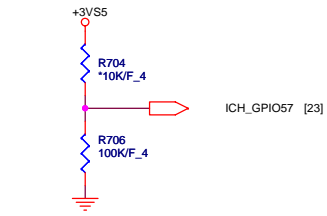
| | |
|-----------|---|
| PCI_GNT#3 | Low = A16 swap override enabled Hi = Default |
|-----------|---|



| | |
|----------|-------------------------------|
| ACZ_SPKR | Low: Default Hi: No reboot |
|----------|-------------------------------|



| | |
|-----------------------|--------------|
| TPM physical presence | Low: Default |
|-----------------------|--------------|



PROJECT : QT6
Quanta Computer Inc.

Size Custom Document Number **ICH9-M Host 1/4** Rev 2B

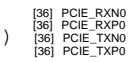
Date: Tuesday, February 26, 2008 Sheet 21 of 44

SWAP PCIE PORT6 TO PORT2 (Lan and New card swap) -->Rename the port name by function and port

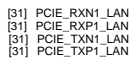
[4,9,21,24,27,29,33,36,40,44] +1.5V
[2,4,6,9,10,11,12,14,15,19,20,21,23,24,25,26,27,28,29,30,31,33,35,36,37,41,44] +3V
[23,25,30,36,40,41,42,44] +3VSUS



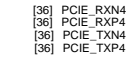
MINI CARD PCI-E(WLAN)



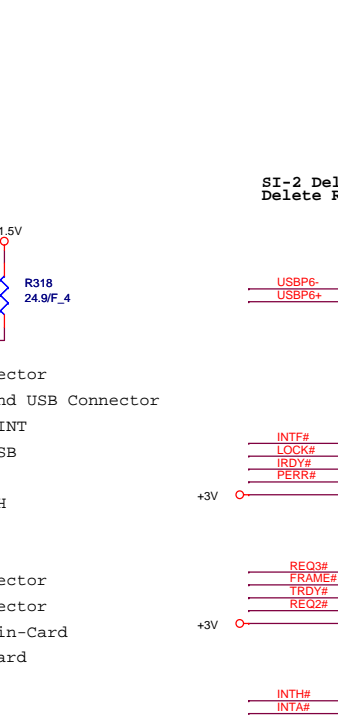
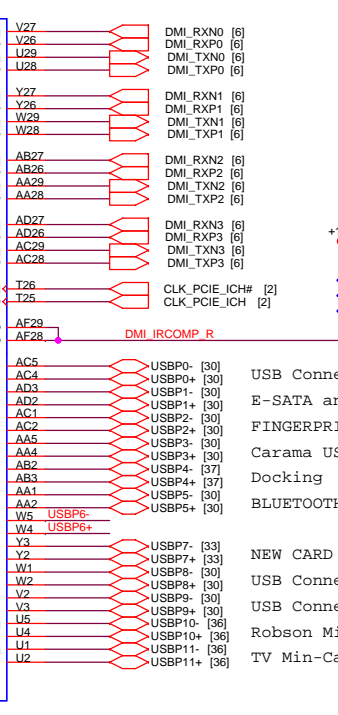
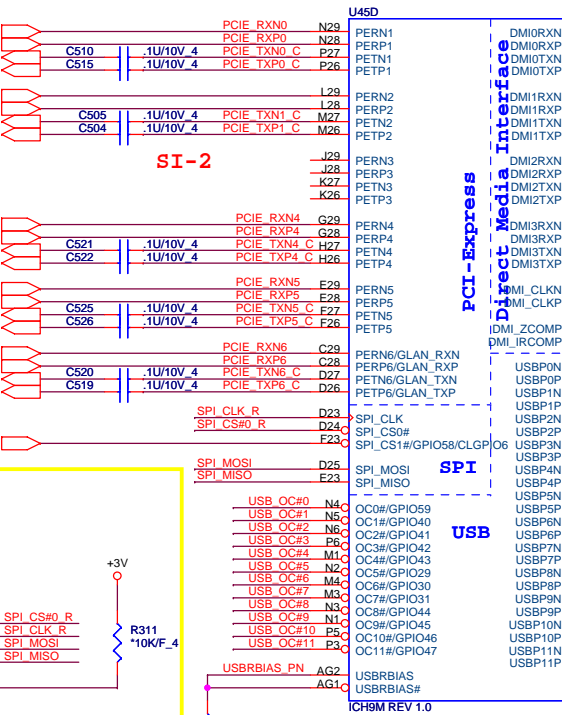
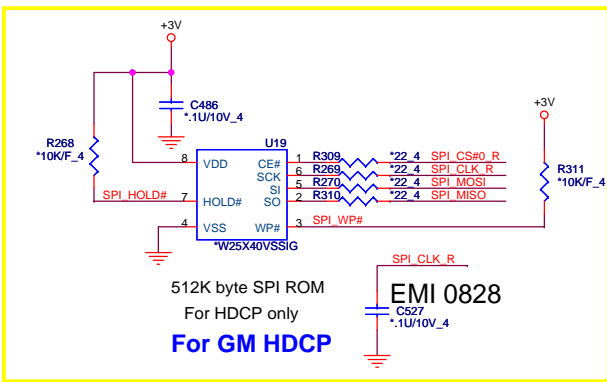
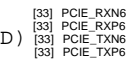
SI-2
PCIE-LAN



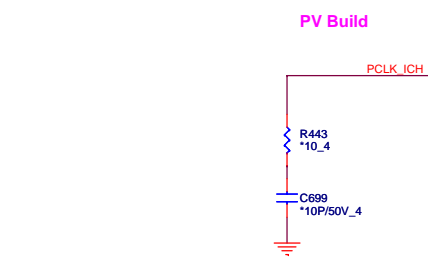
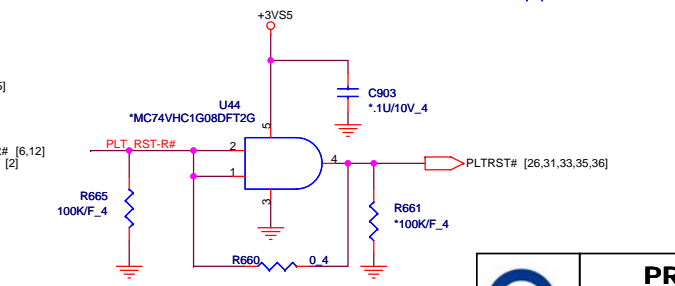
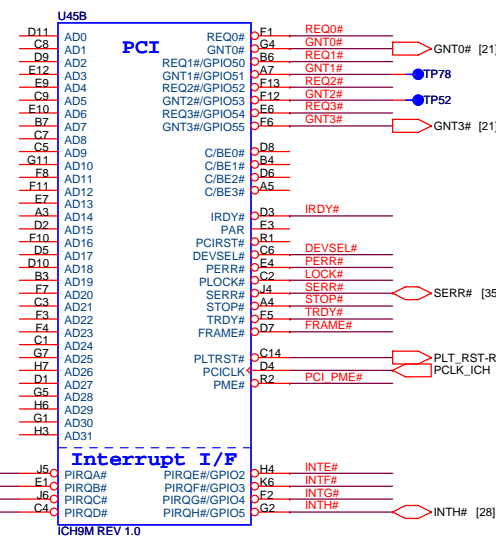
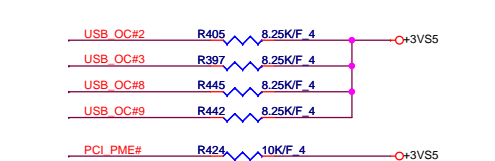
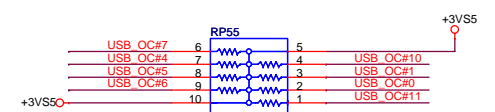
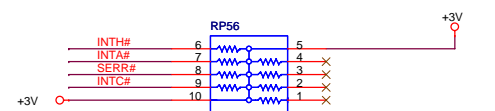
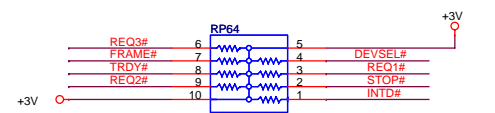
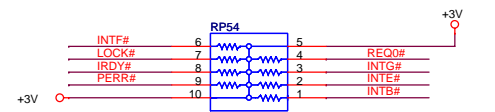
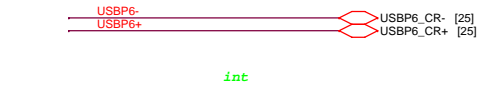
TV CARD PCI-E



SI-2
EXPRESS CARD (NEW CARD)

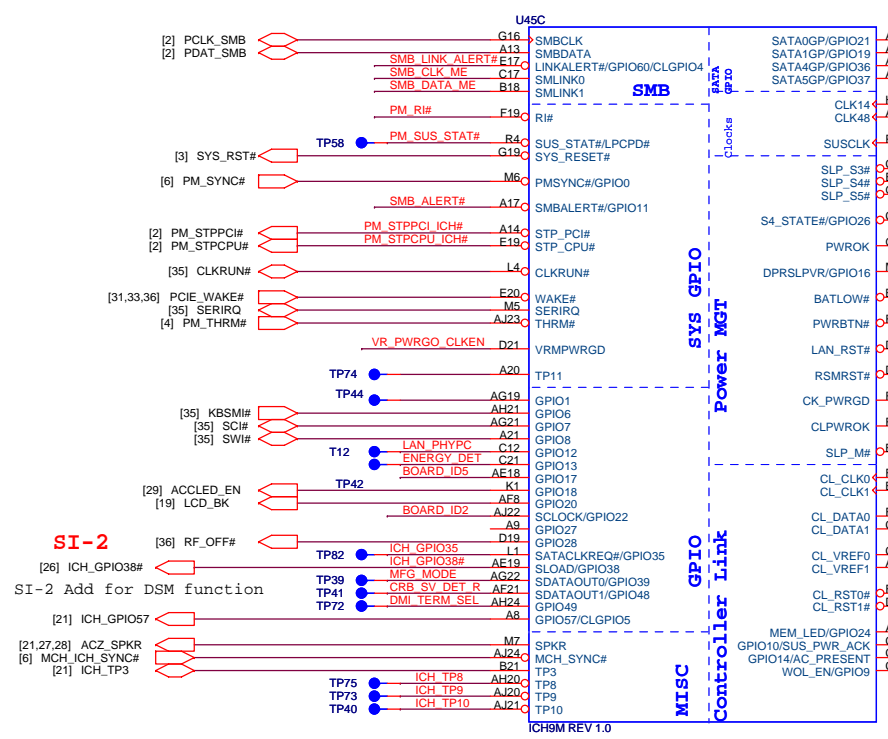


SI-2
SI-2 Delete
Delete RP53,RP57 and tied from SB to CR(USB6)

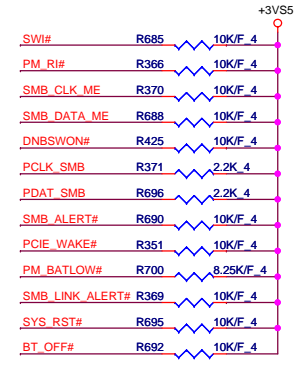
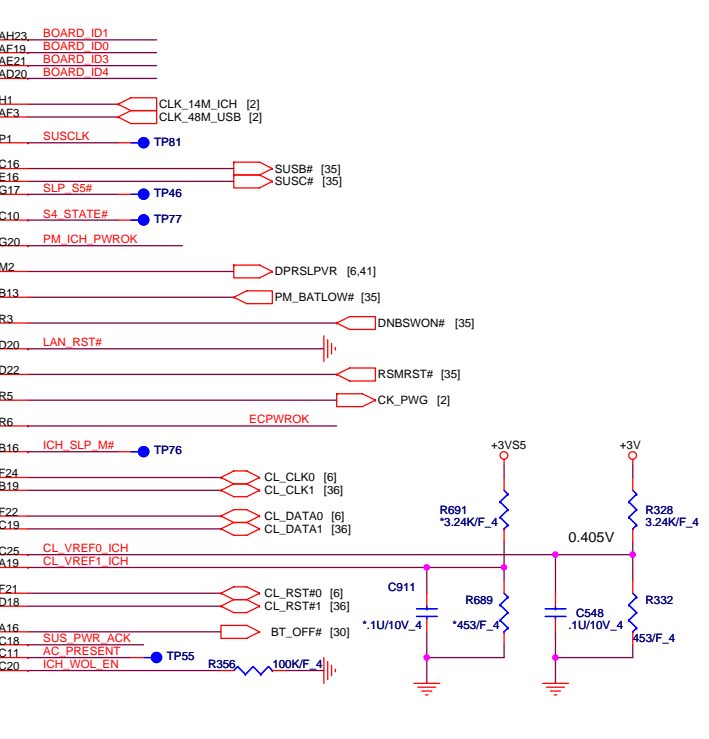


PROJECT : QT6
Quanta Computer Inc.
NB5
Size Custom Document Number ICH9-M PCIE 2/4 Rev 2B
Date: Tuesday, February 26, 2008 Sheet 22 of 44

[4,9,21,22,24,27,29,33,36,40,44] +1.5V
 [2,4,6,9,10,11,12,14,15,19,20,21,22,24,25,26,27,28,29,30,31,33,35,36,37,41,44] +3V
 [21,22,24,33,44] +3VS5
 [25,30,36,40,41,42,44] +3VSUS

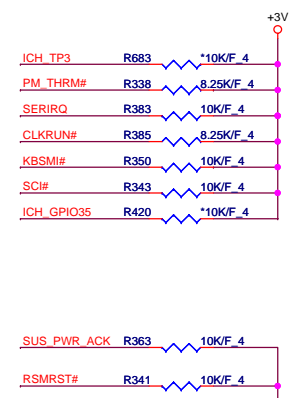
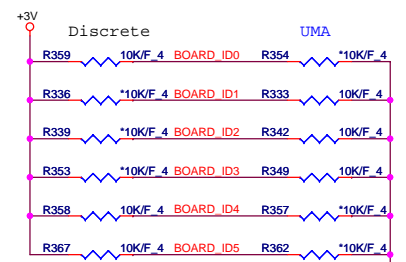
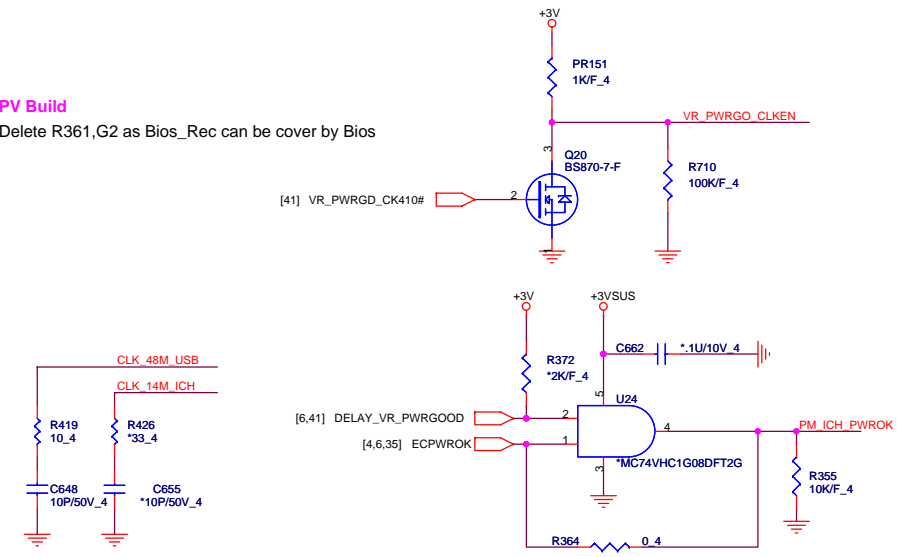


SI-2
 [26] ICH_GPIO38#
 SI-2 Add for DSM function
 [21] ICH_GPIO57#
 [21,27,28] ACZ_SPKR
 [6] MCH_ICH_SYNC#
 [21] ICH_TP3



PV Build

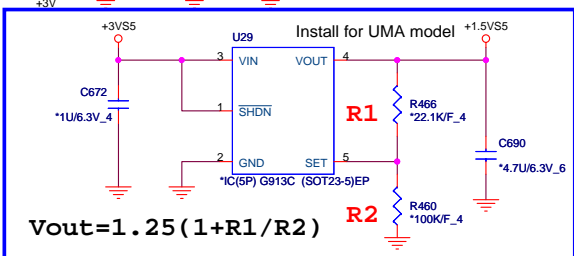
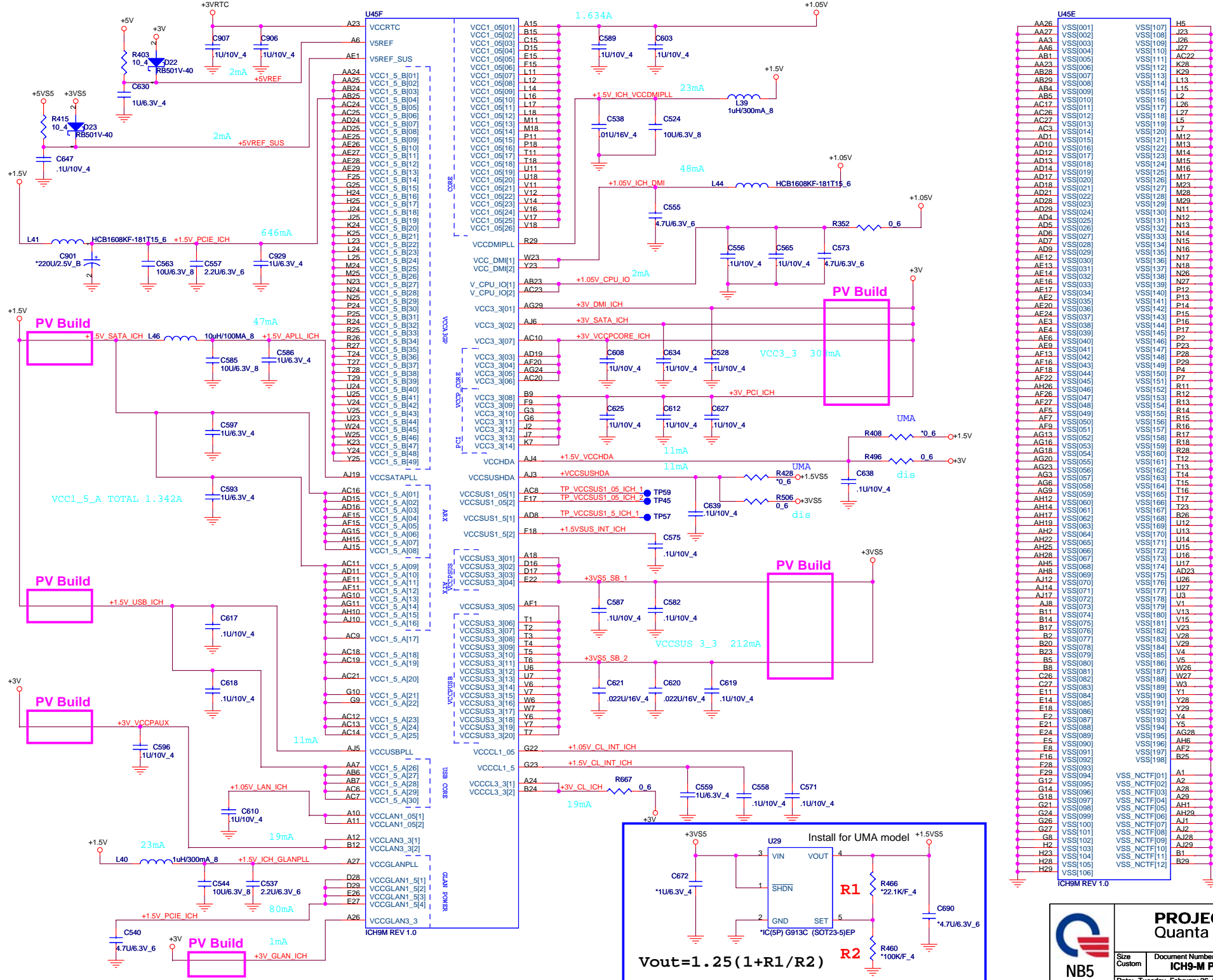
Delete R361,G2 as Bios_Rec can be cover by Bios



Board ID 0: 1-->Discrete , 0-->UMA
 Board ID 1
 Board ID 2
 Board ID 3
 Board ID 4
 Board ID 5

PROJECT : QT6
Quanta Computer Inc.

| | | |
|---|--|--------|
| Size Custom | Document Number ICH9-M GPIO 3/4 | Rev 1A |
| Date: Tuesday, February 26, 2008 Sheet 23 of 44 | | |



PROJECT : QT6
Quanta Computer Inc.

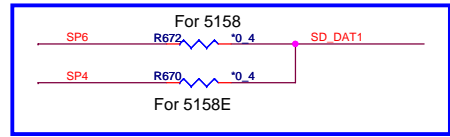
Note:

| SD/MMMC | MS | XD |
|---------|---------|---------------|
| SP0 | | XD CD# |
| SP1 | | XD CD# |
| SP2 | SD_WP | XD CD# |
| SP3 | SD_CD# | |
| SP4 | SD DAT1 | XD D4 |
| SP5 | MS_BS | XD D5 |
| SP6 | SD DAT1 | MS D1 XD D3 |
| SP7 | SD DAT0 | MS D0 XD D6 |
| SP8 | SD DAT7 | MS D2 XD D2 |
| SP9 | MS_INS# | |
| SP10 | SD DAT6 | MS D3 XD D7 |
| SP11 | SD CLK | MS_SCLK XD D1 |
| SP12 | SD DAT5 | XD D0 |
| SP13 | SD DAT4 | XD_WP# |
| SP14 | SD DAT4 | XD_R/# |
| SP15 | SD DAT3 | XD_WE# |
| SP16 | SD DAT2 | XD_RE# |
| SP17 | | XD_ALE |
| SP18 | | XD_CE# |
| SP19 | | XD_CLE |

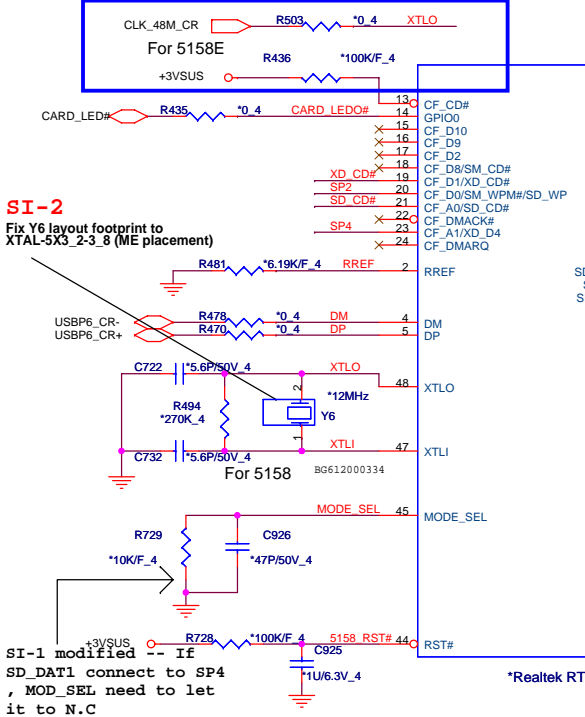
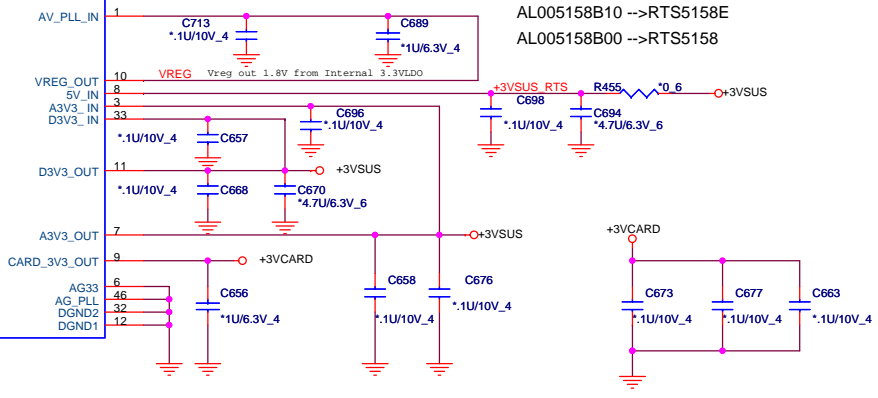
For RTS5158

| | | | | |
|------|------|------|--------------|---------|
| SP7 | R429 | *0.4 | MS DATA0 | XD DAT0 |
| | R437 | *0.4 | | XD D6 |
| SP6 | R431 | *0.4 | MS DATA1 | |
| | R673 | *0.4 | | XD D3 |
| SP8 | | | MS DATA2 | XD D2 |
| SP16 | R497 | *0.4 | | XD DAT2 |
| | R498 | *0.4 | | XD-RE# |
| SP5 | R433 | *0.4 | MS_BS | |
| | R432 | *0.4 | | XD D5 |
| SP15 | R697 | *0.4 | SD DAT3 | |
| | R727 | *0.4 | | XD WE |
| SP11 | R464 | *0.4 | RTS SDMS_CLK | |
| | R461 | *0.4 | | XD D1 |
| SP2 | | | SD_WP | |
| SP13 | | | XD_WP# | |
| SP19 | | | XD_CLE | |
| SP4 | | | XD D4 | |
| SP10 | R451 | *0.4 | MS DATA3 | |
| | R458 | *0.4 | | XD D7 |
| SP14 | | | XD-R/# | |
| SP12 | | | XD-R/# | |
| SP17 | | | XD-ALE | |
| SP18 | | | XD-CE# | |
| | | | SD_CMD_R | SD_CMD |

SI-2
Change net name
as Clk trace layout
T-stub



AL005158B10 -->RTS5158E
AL005158B00 -->RTS5158



JMB 380 Note:

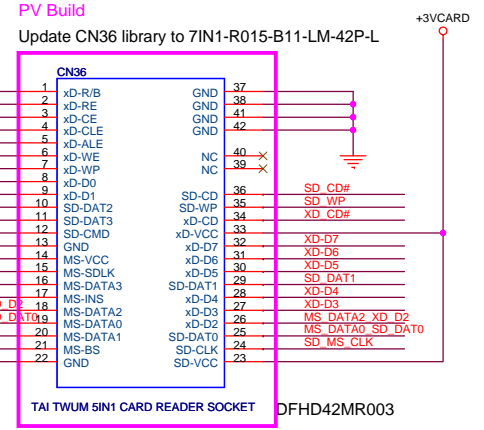
| SD/MMMC | MS | XD |
|-----------|------------|-------------------|
| MDI00 | SD DAT0 | MS D0 XD D0 |
| MDI01 | SD DAT1 | MS D1 XD D1 |
| MDI02 | SD DAT2 | MS D2 XD D2 |
| MDI03 | SD DAT3 | MS D3 XD D3 |
| MDI04 | SD CMD | MS_BS XD WE# |
| MDI05 | SD CLK | MS_SCLK XD CE# |
| MDI06 | SD_WP | XD_WP# |
| MDI07 | | XD_CLE |
| MDI08 | SD DAT4 | XD D4 |
| MDI09 | SD DAT5 | XD D5 |
| MDI10 | SD DAT6 | XD D6 |
| MDI11 | SD DAT7 | XD D7 |
| MDI12 | | XD_RE# |
| MDI13 | | XD_R/# |
| MDI14 | | XD_ALE |
| CR1_LEDV | SD1_LED# | MS1_LED# XD_LED# |
| CR1_PCTLN | SD1_PCTLN# | MS1_PCTLN# PCTLN# |
| CR1_CD0 | SD1_CD# | MS1_CD# XD CV# |
| CR1_CD1 | | MS1_CD# XD CV# |

For JMB380

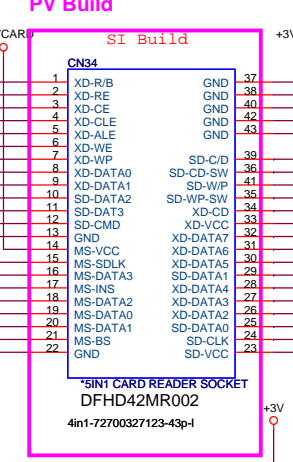
| | | | | |
|--------|------|-------|--------------|---------|
| MDI000 | R686 | *0.4 | MS DATA0 | SD DAT0 |
| | R680 | *0.4 | | XD D0 |
| | R669 | *0.4 | SD DAT1 | |
| MDI001 | R671 | *0.4 | MS DATA1 | |
| | R705 | *0.4 | | XD D1 |
| | R683 | *0.4 | MS DATA2 | XD D2 |
| MDI002 | R702 | *0.4 | SD DAT2 | |
| | R693 | *0.4 | MS DATA3 | |
| MDI003 | R699 | *0.4 | SD DAT3 | |
| | R675 | *0.4 | XD D3 | |
| | R696 | *0.4 | SD CMD | |
| | R682 | *0.4 | MS_BS | |
| | R711 | *0.4 | XD WE | |
| MDI005 | R694 | *22.4 | JMB SDMS_CLK | |
| | R714 | *22.4 | XD-CE# | |
| MDI006 | R662 | *0.4 | SD_WP | |
| | R708 | *0.4 | XD_WP# | |
| MDI007 | R713 | *0.4 | XD_CLE | |
| MDI008 | R678 | *0.4 | XD D4 | |
| MDI009 | R668 | *0.4 | XD D5 | |
| MDI010 | R666 | *0.4 | XD D6 | |
| MDI011 | R663 | *0.4 | XD D7 | |
| MDI012 | R715 | *0.4 | XD-RE# | |
| MDI013 | R716 | *0.4 | XD-R/# | |
| MDI014 | R712 | *0.4 | XD-ALE | |

Close to CN34

From JMB380 **JMB SDMS_CLK** R707 *0.4 SD MS_CLK
From RTS5158E **RTS SDMS_CLK** R717 *0.4 SD MS_CLK
New add R707, R717 for SD/MS CLK trace layout

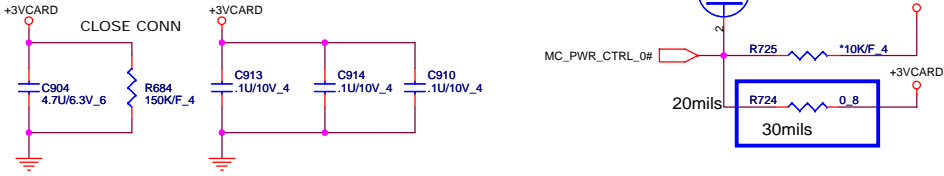


5 IN1 CARD READER
XD, MMC/SD, MS/MSP



SI-2
Change net name
as Clk trace layout
T-stub

R694 andn R714 change to 22 ohm SI-2

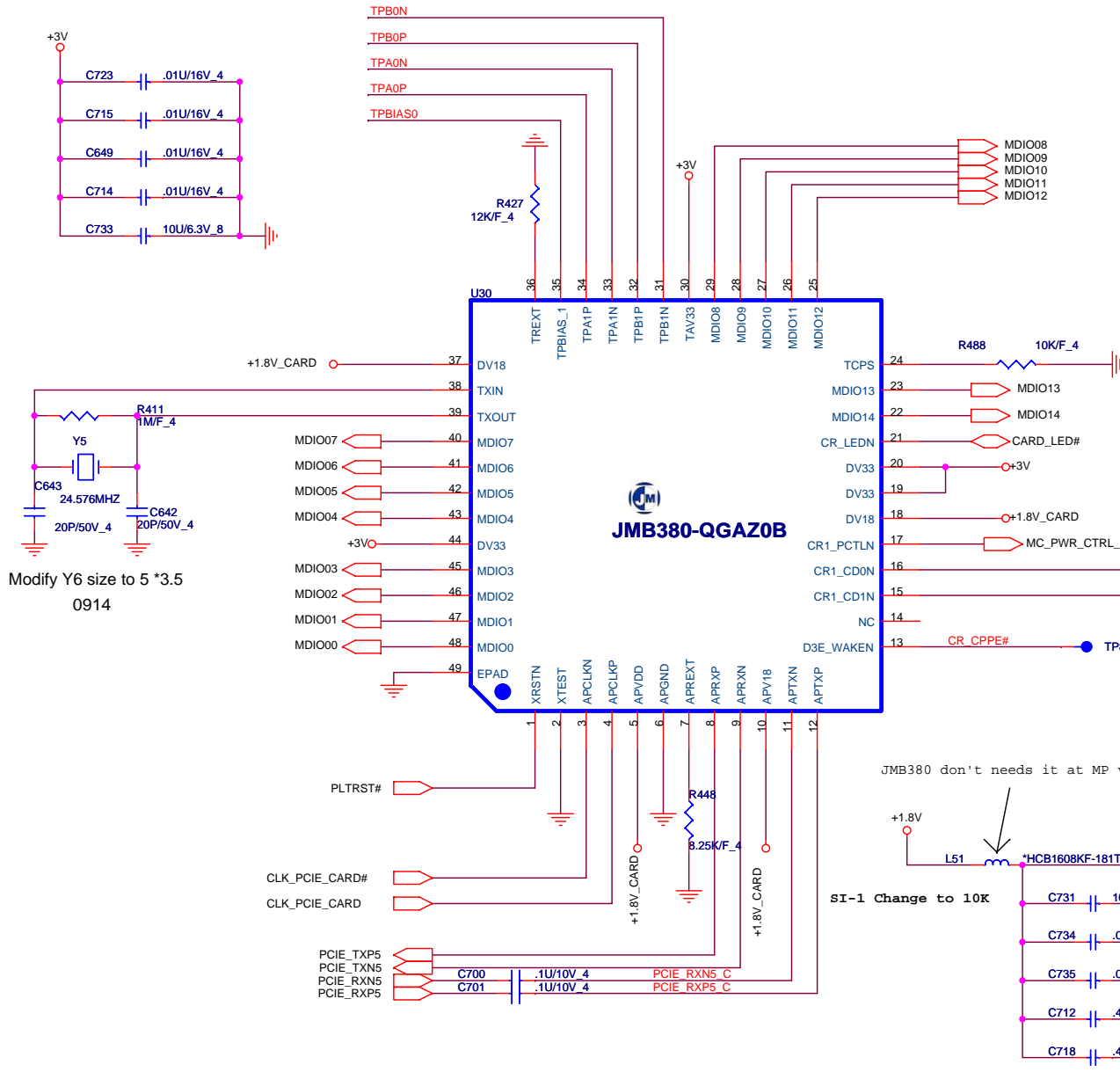


JMB 380 Note:

PROJECT : QT6
Quanta Computer Inc.

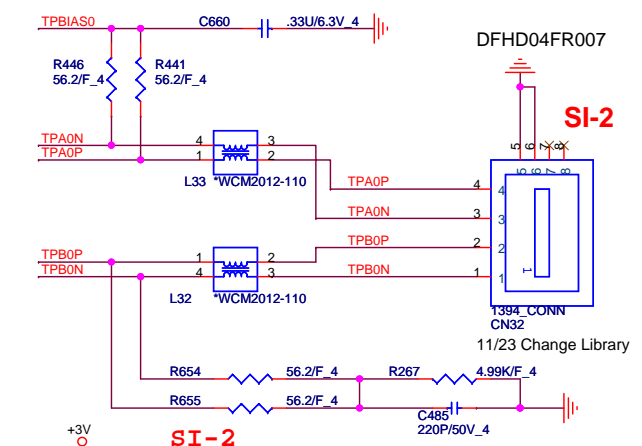
Size Custom Document Number **RTS5158 & CR SOCKET & HOLE** Rev 2B

Date: Tuesday, February 26, 2008 Sheet 25 of 44

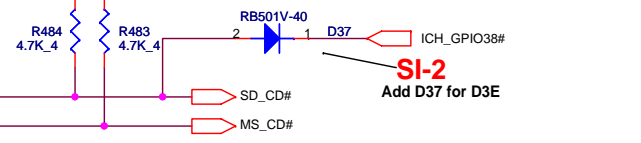


Modify Y6 size to 5 * 3.5
0914

PV Build
Modify CN32 layout footprint to 1394-020115FR004S510ZL-4P-H-QT6



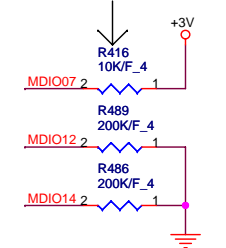
SI-2
Modify CN32 layout footprint to 1394-020115FR004S510ZL-4P-H-QT8 (11/19)



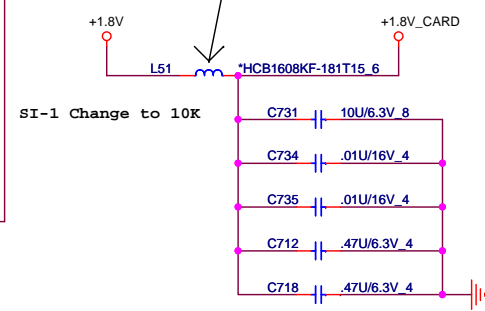
SI-2
Add D37 for D3E

SI-2
TP86 Add TP86 for D3E

SI-1 Change to 10K

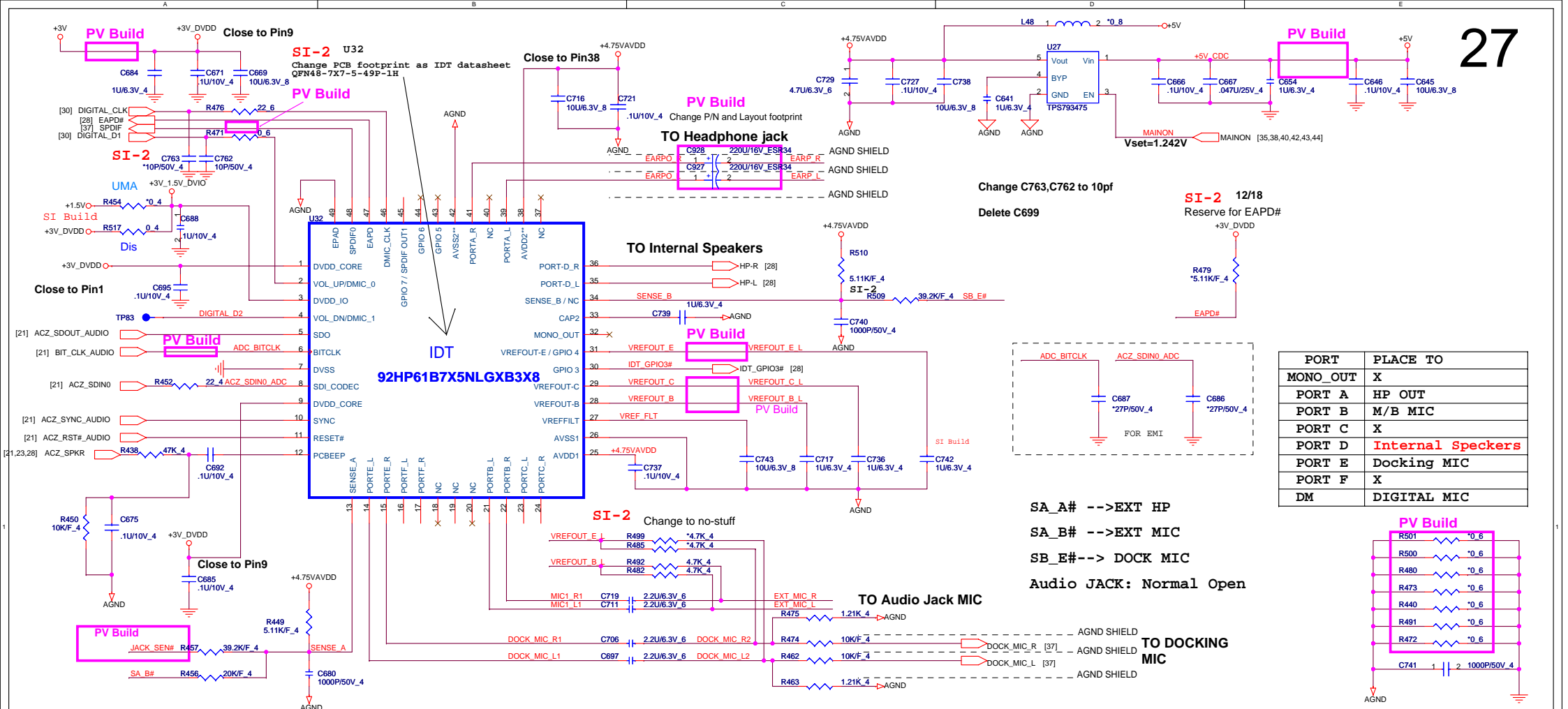


JMB380 don't needs it at MP vesion CHIP

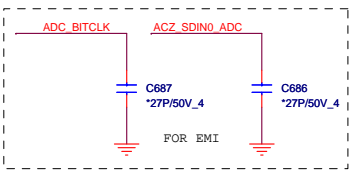
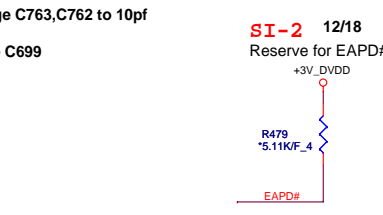


SI-1 Change to 10K

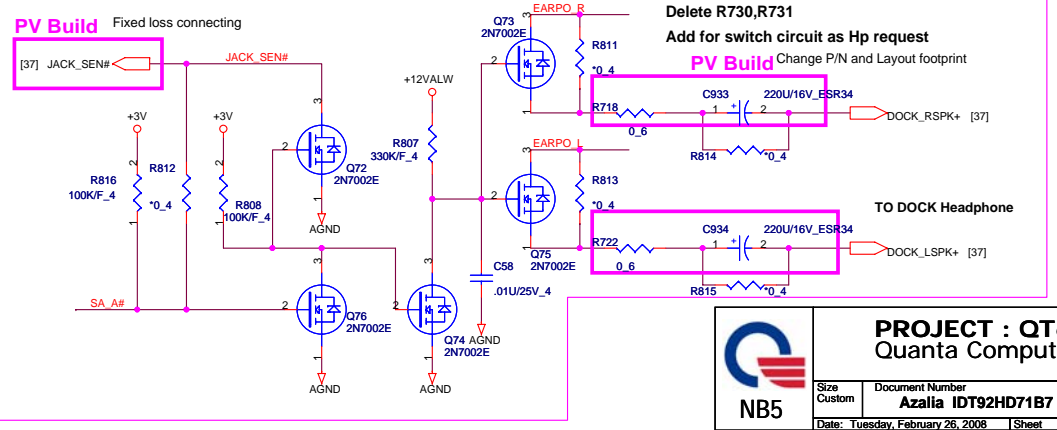
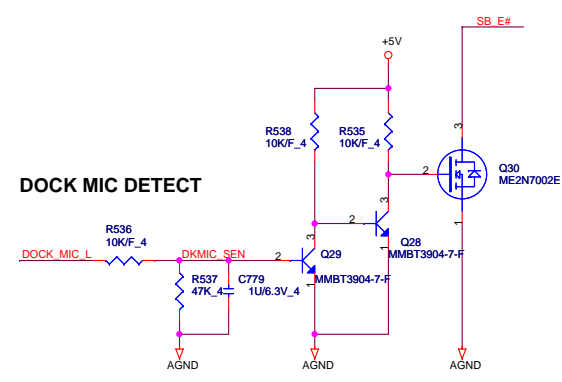
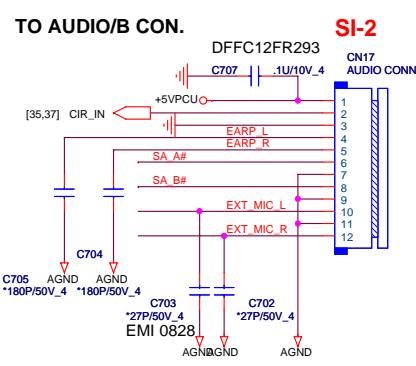
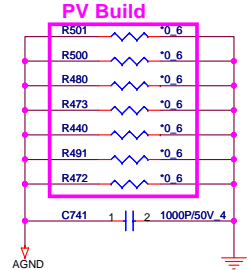
| | | |
|----------------------------------|--|--------|
| | PROJECT : QT6 | |
| | Quanta Computer Inc. | |
| Size B | Document Number JMB380 Controller/1394 | Rev 2B |
| Date: Tuesday, February 26, 2008 | Sheet 26 | of 44 |



| PORT | PLACE TO |
|----------|-------------------|
| MONO_OUT | X |
| PORT A | HP OUT |
| PORT B | M/B MIC |
| PORT C | X |
| PORT D | Internal Speakers |
| PORT E | Docking MIC |
| PORT F | X |
| DM | DIGITAL MIC |



SA_A# -->EXT HP
 SA_B# -->EXT MIC
 SB_E#--> DOCK MIC
 Audio JACK: Normal Open



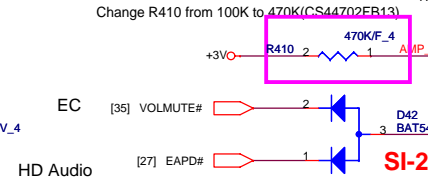
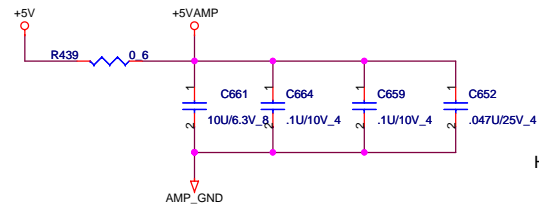
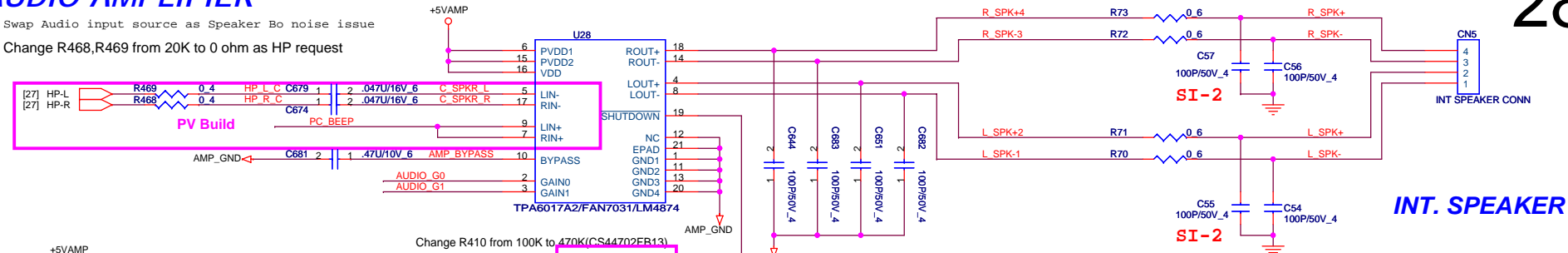
PROJECT : QT6
 Quanta Computer Inc.

| | | |
|---|--|-----------|
| Size Custom | Document Number Azalia IDT92HD71B7 | Rev 3A |
| Date: Tuesday, February 26, 2008 Sheet 27 of 44 | | |

AUDIO AMPLIFIER

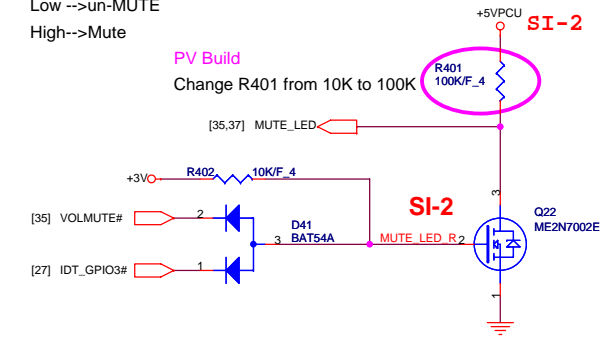
Swap Audio input source as Speaker Bo noise issue

Change R468,R469 from 20K to 0 ohm as HP request



MUTE_LED
Low --> un-MUTE
High --> Mute

Change Power source to +5VPCU as power situation



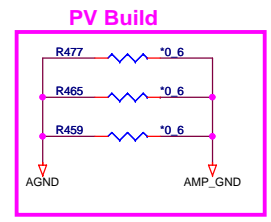
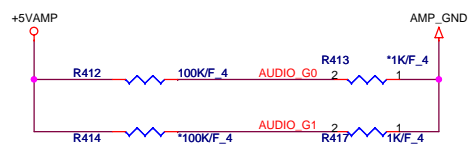
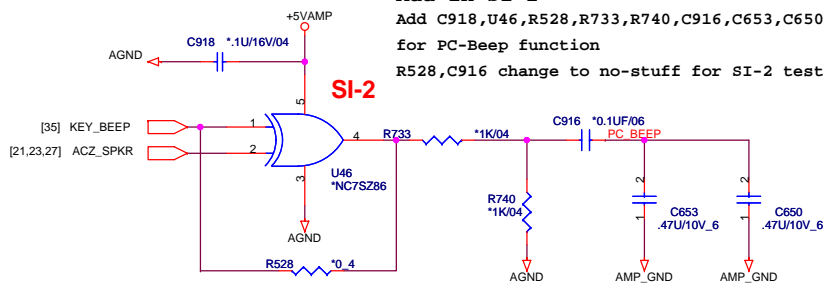
AL001431K04
AL6017A2K12
APA2031 ,AL002031K00

6017A2 Gain Table

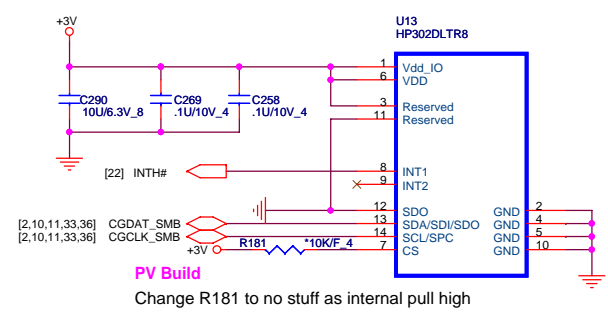
| GAIN0 | GAIN1 | AV | RIN |
|-------|-------|--------|-----|
| 0 | 0 | 6dB | 90K |
| 0 | 1 | 10dB | 70K |
| 1 | 0 | 15.6dB | 45K |
| 1 | 1 | 21.6dB | 25K |

Add in SI-2

Add C918,U46,R528,R733,R740,C916,C653,C650 for PC-BEEP function
R528,C916 change to no-stuff for SI-2 test -->12/6

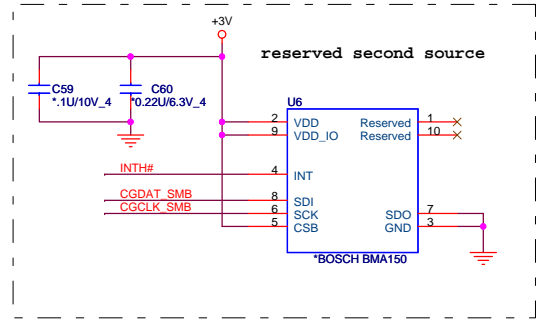


Accelerometer Sensor



PV Build

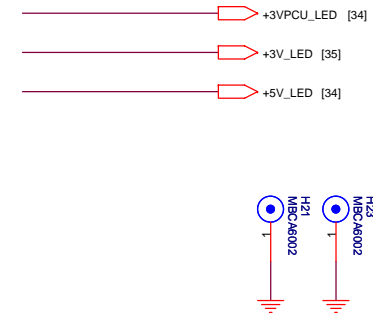
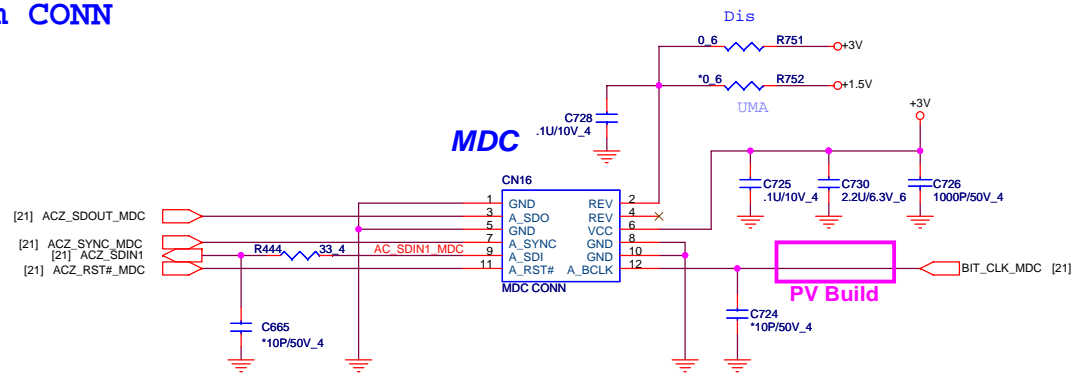
Change R181 to no stuff as internal pull high



Pin 12: Low 38hex
Pin 12: unconnected/floating 3Ahex

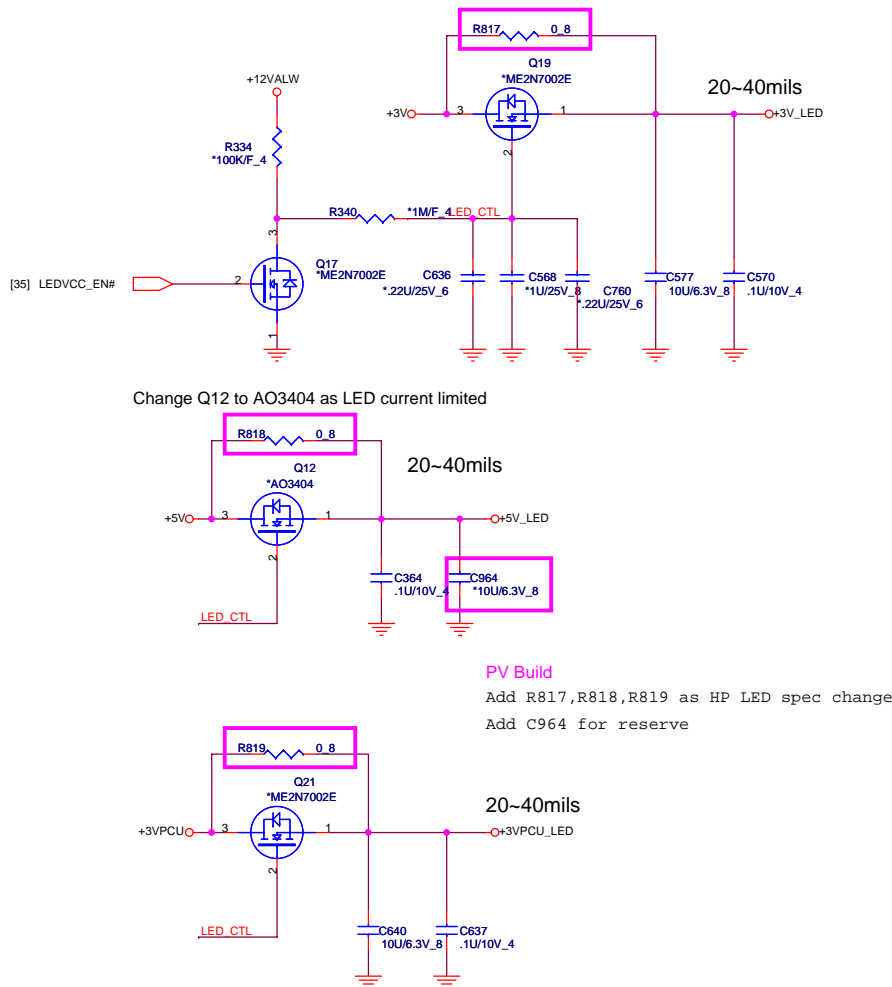
PROJECT : QT6
Quanta Computer Inc.

| | | |
|---|---|--------|
| Size Custom | Document Number AMP_TPA6017/Accelerometer | Rev 3A |
| Date: Tuesday, February 26, 2008 Sheet 28 of 44 | | |

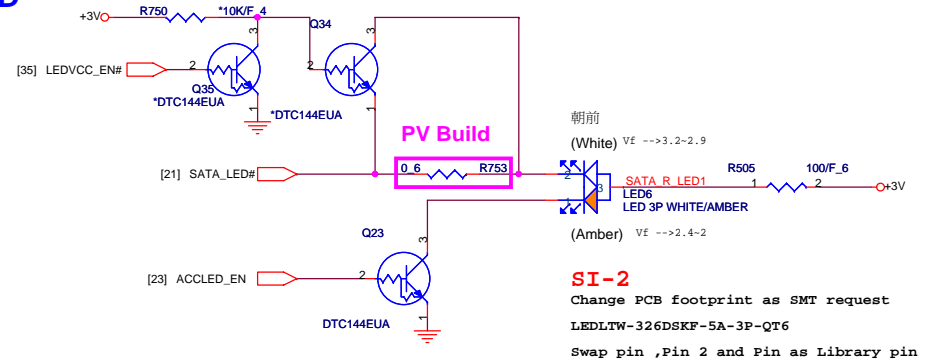


Needs to change Library as ME request

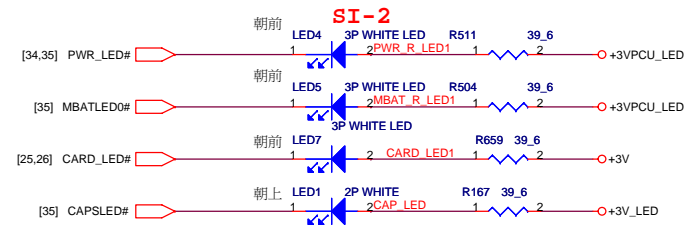
LED PWR CONTROL



LED

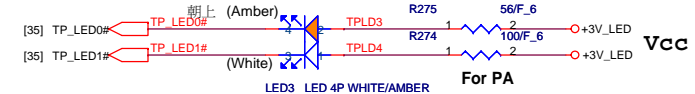


Modify LED4,LED5,LED7 layout footprint to ledl-s110kgct-3p-qt6 (11/19)



LED Vf

R

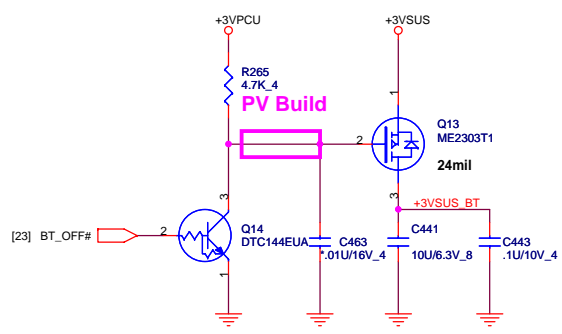


$$I = \frac{V_{cc} - V_f}{R}$$

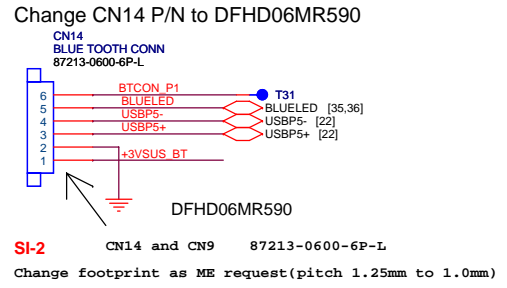


PROJECT : QT6
Quanta Computer Inc.

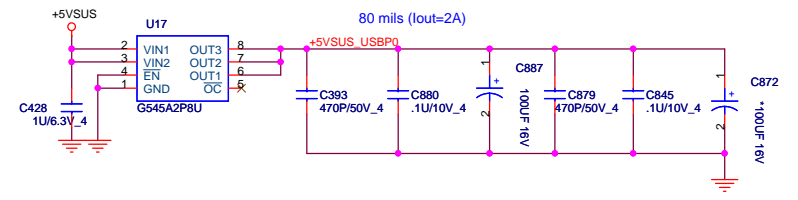
BLUETOOTH



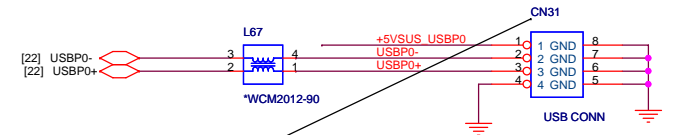
PV Build



LEFT SIDE USBX1 and E-SATA/USB COMBO 30

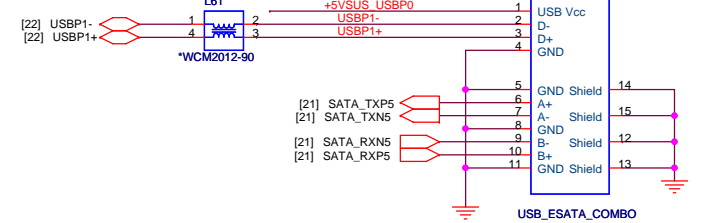


USB 0



SI-2 CN30, CN31
Change Connector layout type from SMD_PAD to Dip as SMT request

USB & ESATA

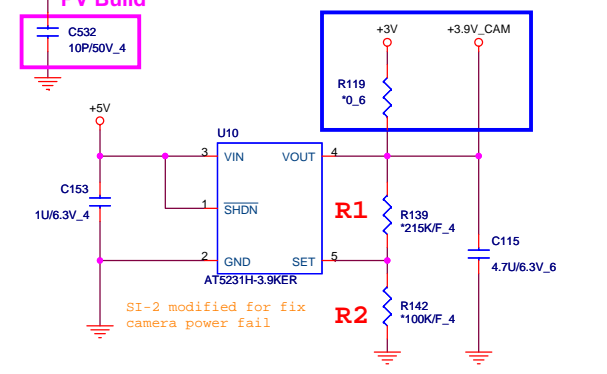
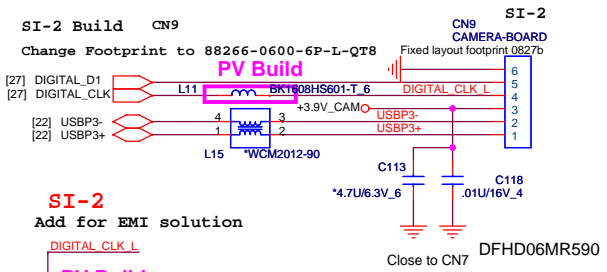


USB-C-2006102-11P-H-QT6

Touch Screen

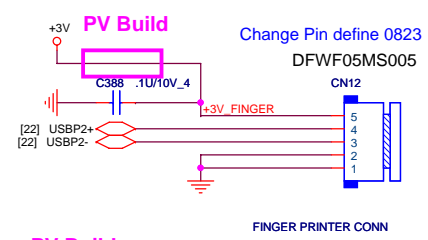
Delete Touch-Screen in SI-2
CN2, C10, L4
SI-2 Build

USB CAMERA /DIGITAL MIC CONNECT



$$V_{out} = 1.25(1 + R1/R2)$$

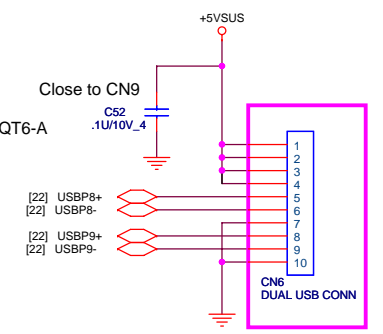
USB fingerprint CON



PV Build
Change CN12 to BL123-05R-5P-L-QT6-A

1. ESD GND
2. SYSTEM GND
3. USB-
4. USB+
5. USB PWR(+3V)

RIGHT SIDE USBX2

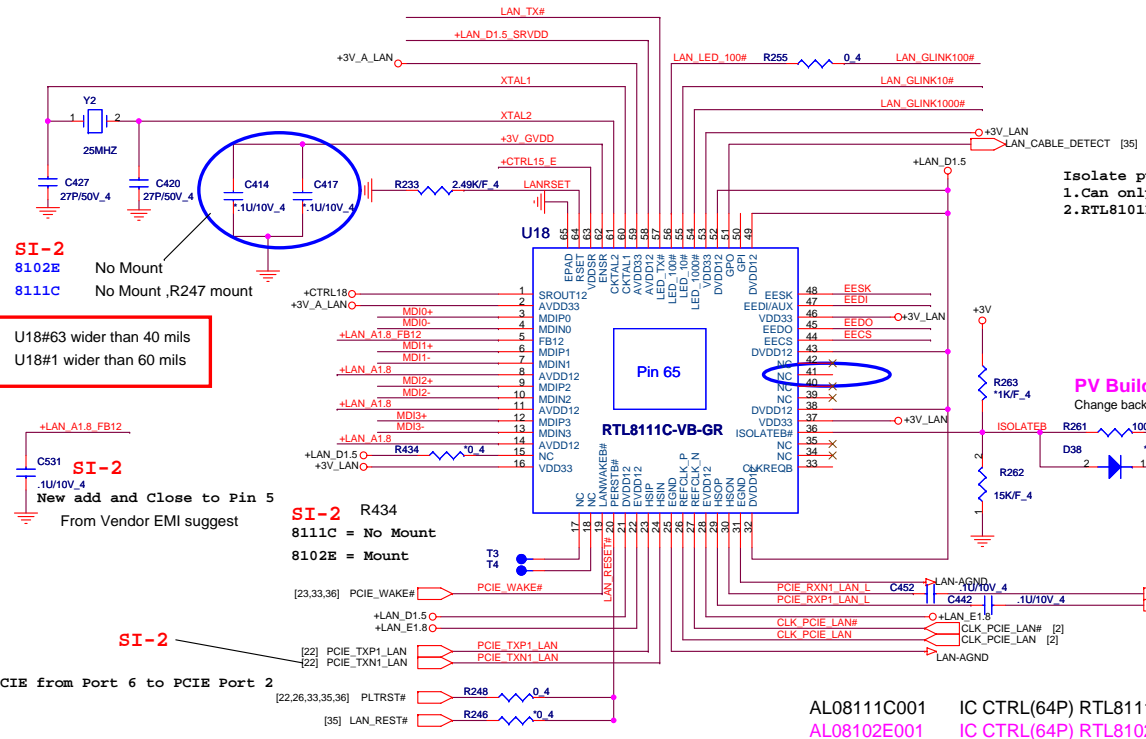
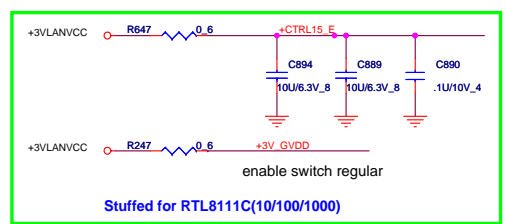
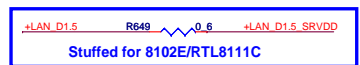


| | | |
|----------------------------------|--|----------------|
| | PROJECT : QT6 Quanta Computer Inc. | |
| | Size Custom Document Number BT/WC/FT/TS/ESATA/USB | Rev 3A |
| Date: Tuesday, February 26, 2008 | | Sheet 30 of 44 |

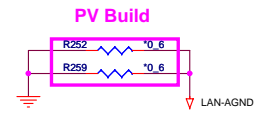
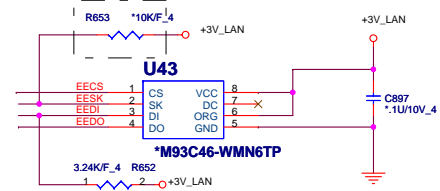
T : Stuffed for RTL8111C(10/100/1000)

E : Stuffed for 8101E/8102E(10/100)

For 8102E/8111C



for 93C56 used. NC if 93C46 is used.



Isolate pull low:
 1.Can only disable RTL8111C.
 2.RTL8101E can't disable

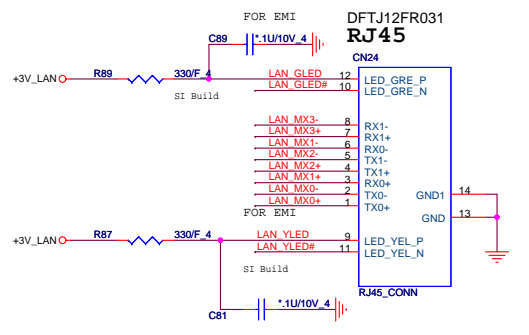
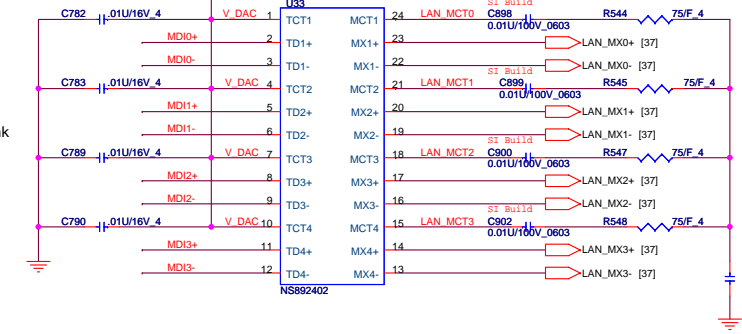
if ISOLATEB pin pull-low,the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)

Swap PCIE from Port 6 to PCIE Port 1

- PV Build**
- Remove 8111B and 8101E support in PV Build
1. Delete R264 (For 8111B)
 2. Delete R650 and T28
 3. Delete R651 and U18#33 for 8111B support
 4. Delete R231 as RSET
 5. Delete R242,R243,R244,R245,C394,C395 8101E support



Add C898,C899,C900,C902 as HP request



NS892402:GIGABIT DB0AT9LAN05

NS892405:10/100 DB0ZB1LAN04

PROJECT : QT6
 Quanta Computer Inc.

Size Custom Document Number **RTL8111C/8101E/RJ45** Rev 2B

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T : Stuffed for RTL8111C(10/100/1000)

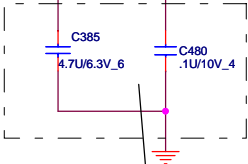
E : Stuffed for 8101E/8102E(10/100)

LANVCC
1.2W
364mA

PV Build

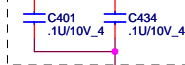
Power trace Layout 寬度 > 30mil

+3VLANVCC



these CAP are for LAN CHIP LANVCC pins--16, 37, 46 and 53.placement close lan chip

PV Build



these CAP are for LAN CHIP LAN_A3.3 pins-- 2 and 59.placement close lan chip

8111C CV-4706MN00
8102E CS00004JA40

For Giga must change L65 to Inductor (Chipset include switch power)
+CTRL18 will become to switch power phase

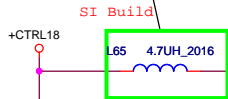
L54 for Giga lan use 4.7uH power choke
A>500mA tolerance ±15%

placement close to lan chipset

Power trace Layout 寬度 > 30mil

Power domain chart

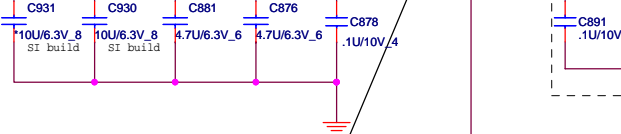
| | RTL8111C(P) RTL8102E |
|----------|-------------------------|
| LANVCC | 3.3V |
| LAN_D1.8 | 1.2V |
| LAN_A1.8 | 1.2V |
| LAN_D1.5 | 1.2V |



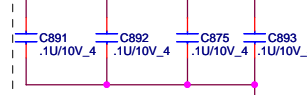
For 8102E

SI-2
Remove R250,L63,L66 --->For 8102E

+FB12 [31]



+LAN_A1.8

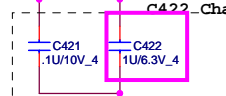


these cap are for lan chip LAN_A1.8 pins--5, 8, 11 and 14. placement close chip

STUFF 100 ohm BEAD

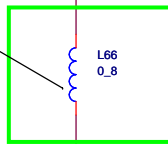
R250 0.8

+LAN_E1.8



these cap are for lan chip LAN_D1.8 pins, such as 22 and 28. placement close lan chip

C422 Change to 1u for 8102E



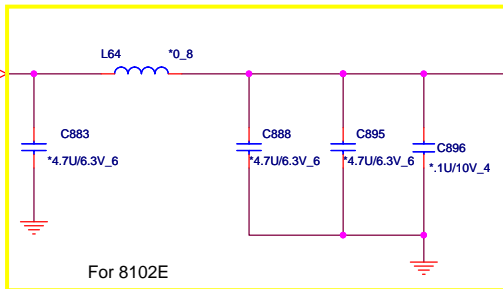
Only For 8111C application

Power trace Layout 寬度 > 30mil

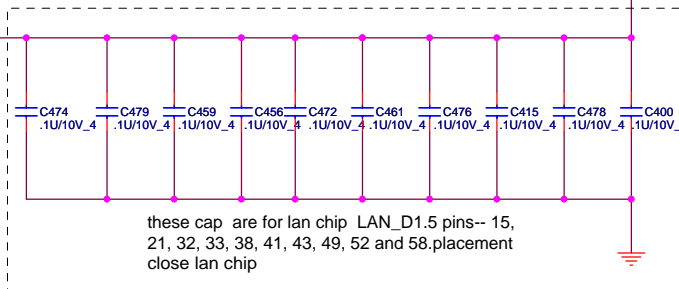
PV Build

C422 change to 1uf

[31] +CTRL15



For 8102E

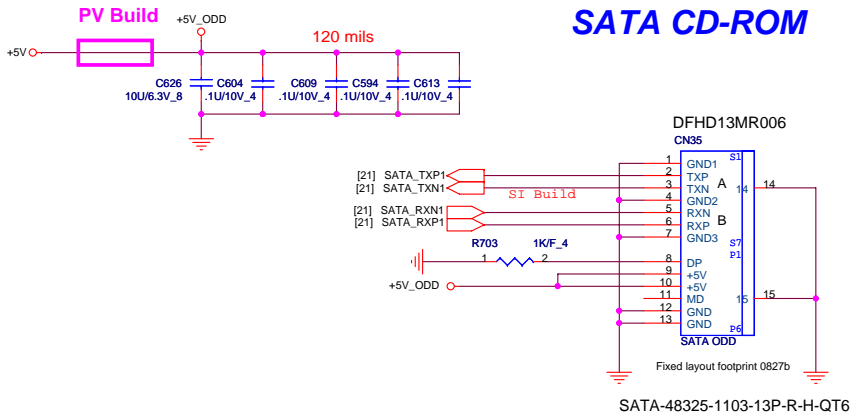


these cap are for lan chip LAN_D1.5 pins-- 15, 21, 32, 33, 38, 41, 43, 49, 52 and 58.placement close lan chip

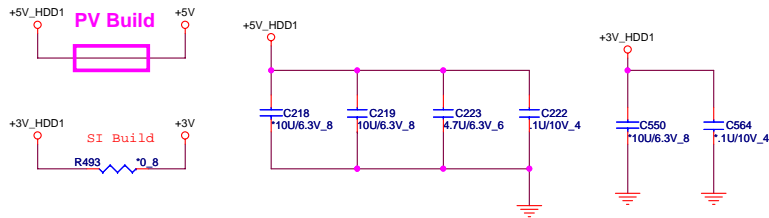
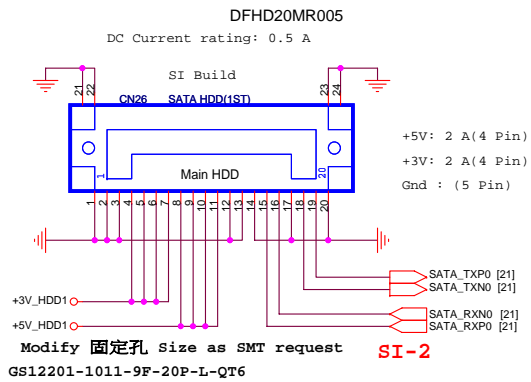


PROJECT : QT6
Quanta Computer Inc.

| | | |
|----------------------------------|-----------------|--------|
| Size A3 | Document Number | Rev 1A |
| LAN Power | | |
| Date: Tuesday, February 26, 2008 | Sheet 32 of 44 | |

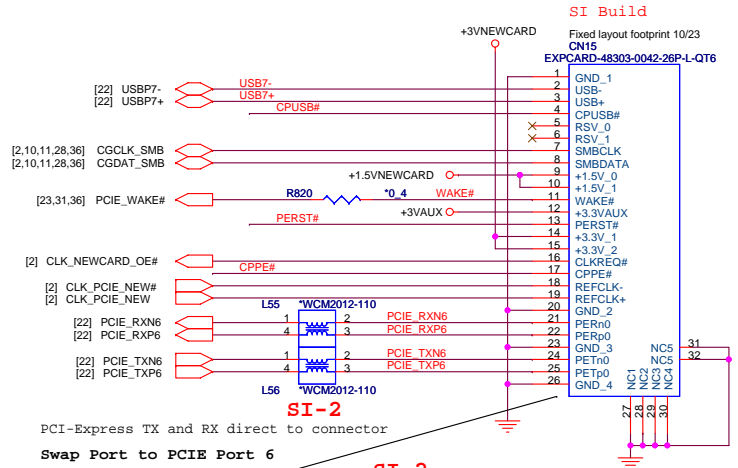


SATA HDD CONNECTOR

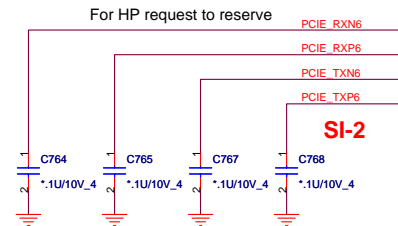
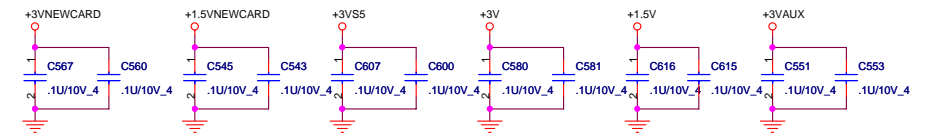
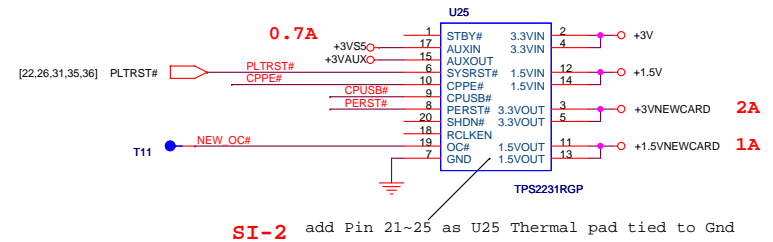


NEWCARD

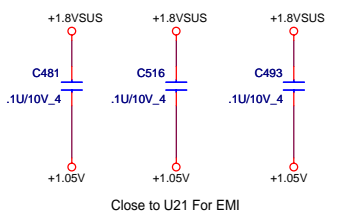
NEWCARD (PCIEXPRESS*1 + USB*1)



Change CN15#31,32 as ME request for Hole pad
expcard-48303-0042-26p-l-qt6 as ME modify Pad size(pin31,32)
Move CN15#29,30 Pin as ME request(Molex confirm drawing)



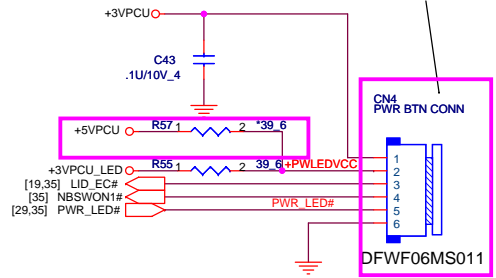
| | | |
|--|---|--|
| | PROJECT : QT6 Quanta Computer Inc. | |
| | Size Custom Document Number ODD/HDD/NEW CARD | Date: Tuesday, February 26, 2008 Sheet 33 of 44 |



Close to U21 For EMI

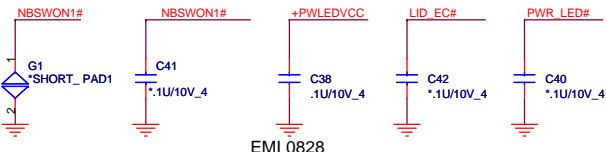
PV Build

Change CN4 to BL123-06R-6P-L-QT6-A



1. +3VPCU(LIDSWITCH PWR)
2. LEDVCC(+3VPCU)
3. LIDSWITCH
4. POWERON#
5. PWRLED#
6. GND

POWER BOTTON CONNECT



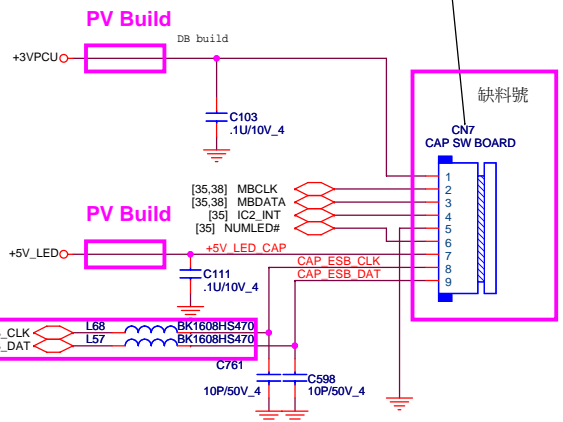
EMI 0828

POWER SW CONNECT

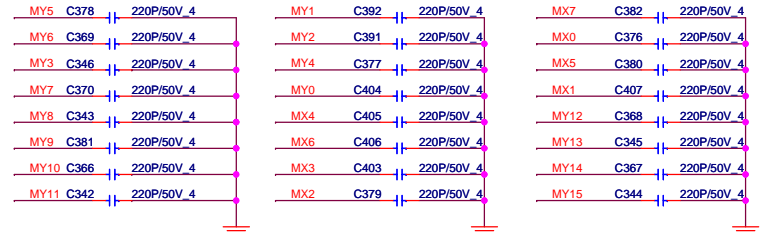
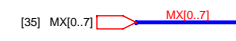
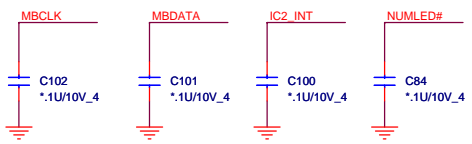
CAP SW CONNECT

PV Build

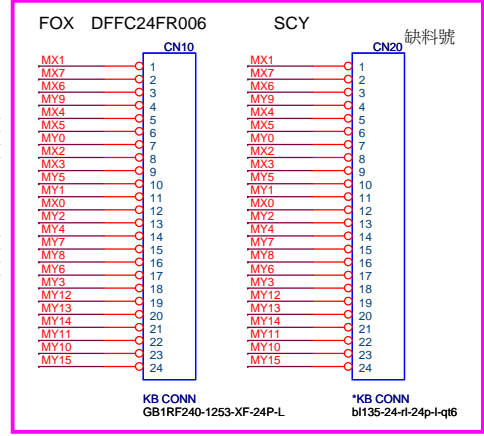
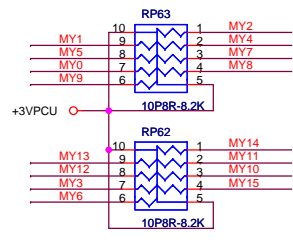
Change CN7 to BL123-09R-9P-L-QT6-A



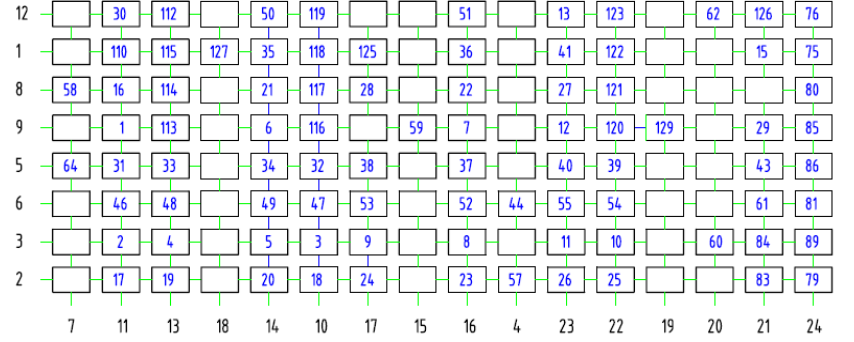
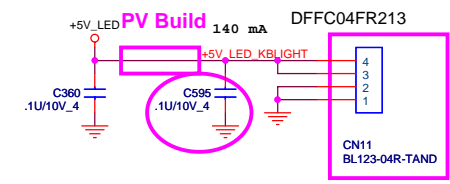
1. +3VPCU
2. MBCLK
3. MBDATA
4. CAP_INT
5. GND
6. NUM LOCK LED
7. +5V_LED
8. ESB_CLK
9. ESB_DAT



KEYBOARD PULL-UP



PV Build
Add C595 and close to CN11
Change CN11 to BL123-04R-4P-L-QT6-A
Change CN10 to GB1RF240-1253-XF-24P-L as Foxconn drawing

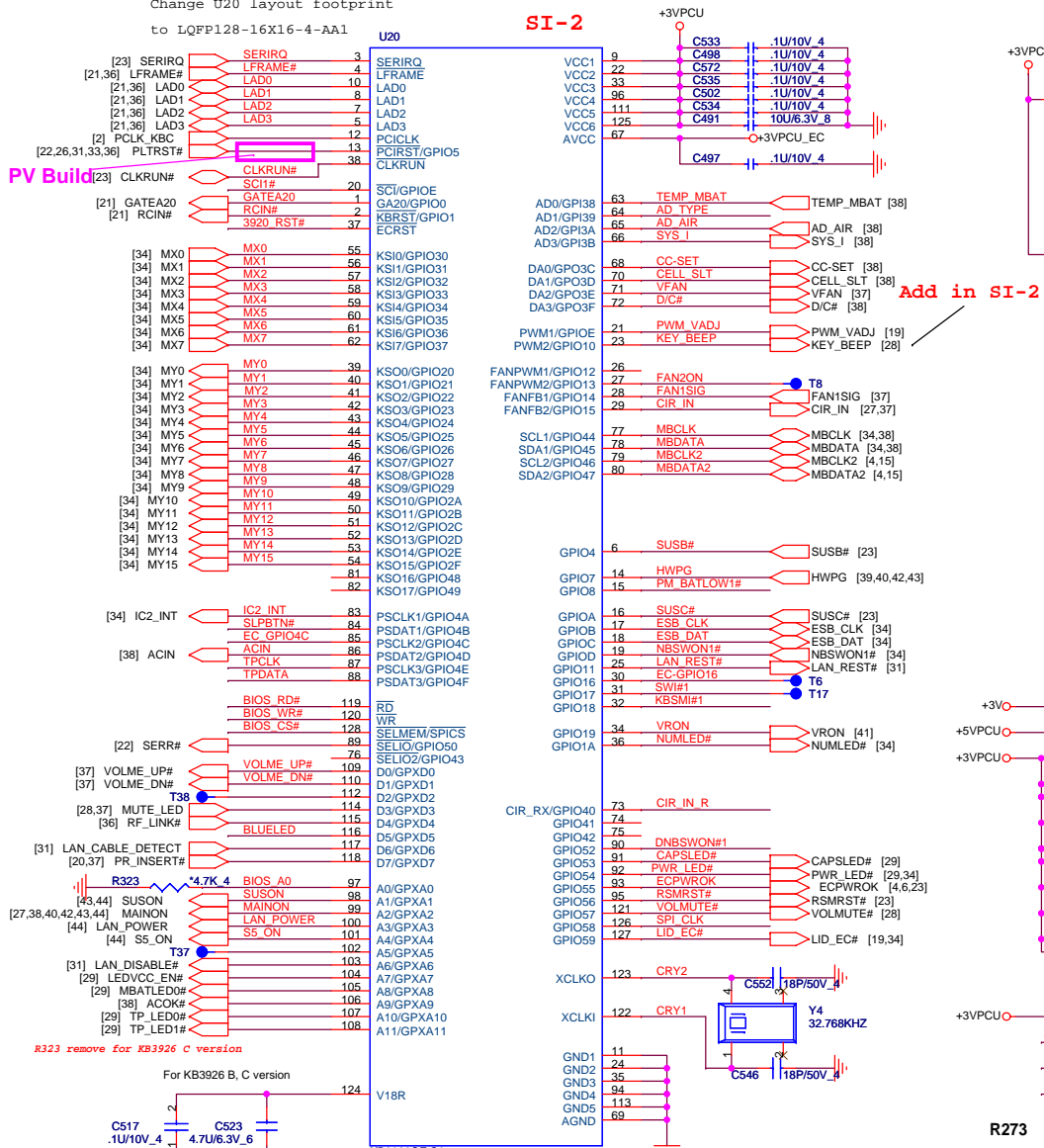


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Size Custom Document Number
KB/CAP/POWER CONN

Date: Tuesday, February 26, 2008 Sheet 34 of 44

Change U20 layout footprint to LQFP128-16X16-4-AA1



PV Build

SI-2

Add in SI-2

PV Build

TOUCH PAD L/R

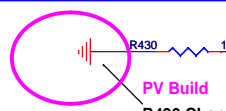
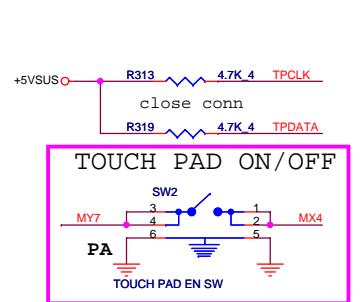
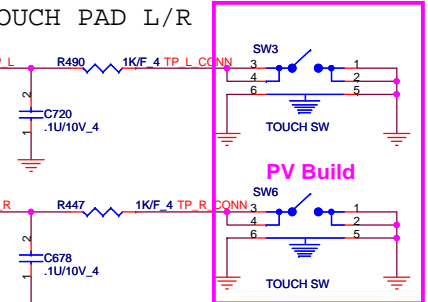
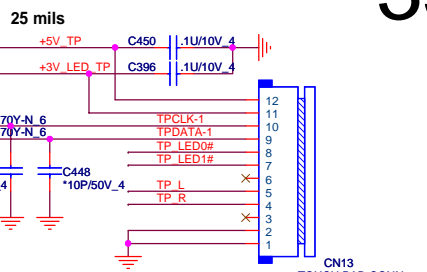
TOUCH PAD CONNECTOR PV Build

PV Build

TOUCH PAD ON/OFF

TOUCH PAD CONN DFFC12FR293

Change to SW2,SW3,SW6 to BA1G as vendor suggesst



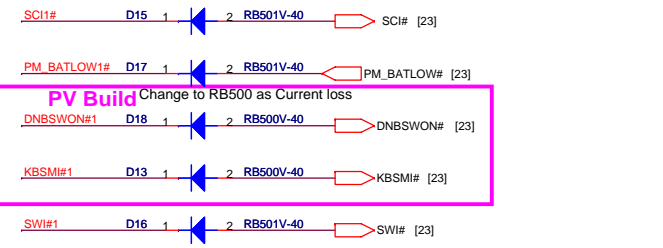
SI-2

Add R430 and tied to U20 Pin 115 and change Q18 footprint to SOT23. Delete Q18 and tied to U20#116 direction

- Socket: DG008000031
- MXIC AKE5GFK0Z09
 - WINBOND AKE3GFPON08
 - PME AKE3GZP0500
 - EON AKE3GZP0Q00
 - AIT AKE3GZP0801

SI-2

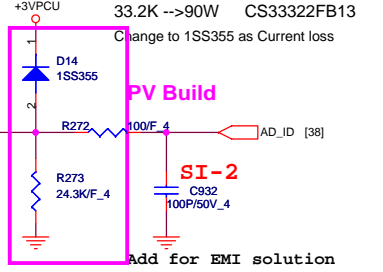
Add Pin 117,103 for DSM,116 for Bluetooth,Pin 23 for Key Beep to Amplifier. Add T37,T38,T39 for EC. Delete T10 and tie pin 117 from Lan for DSM



R273

64.9K -->65W CS36492FB17. 33.2K -->90W CS33322FB13

Change to 1S5355 as Current loss



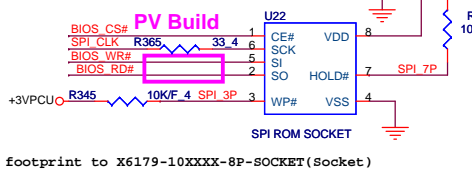
SI-2

Add for EMI solution

SI-2

Add for Power request

1M byte SPI BIOS



SI-2

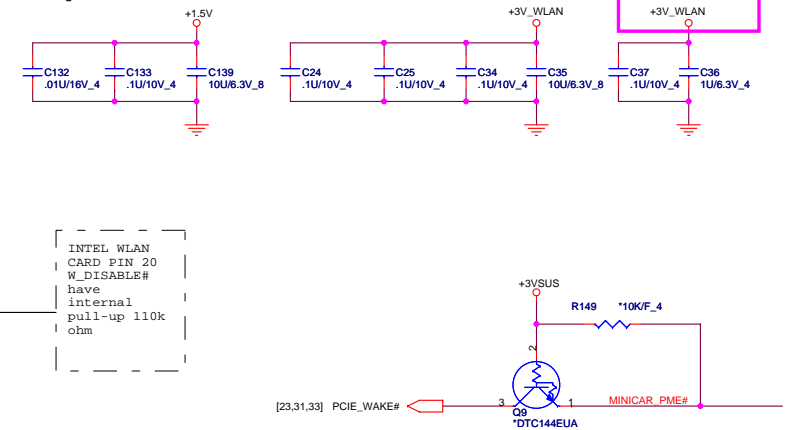
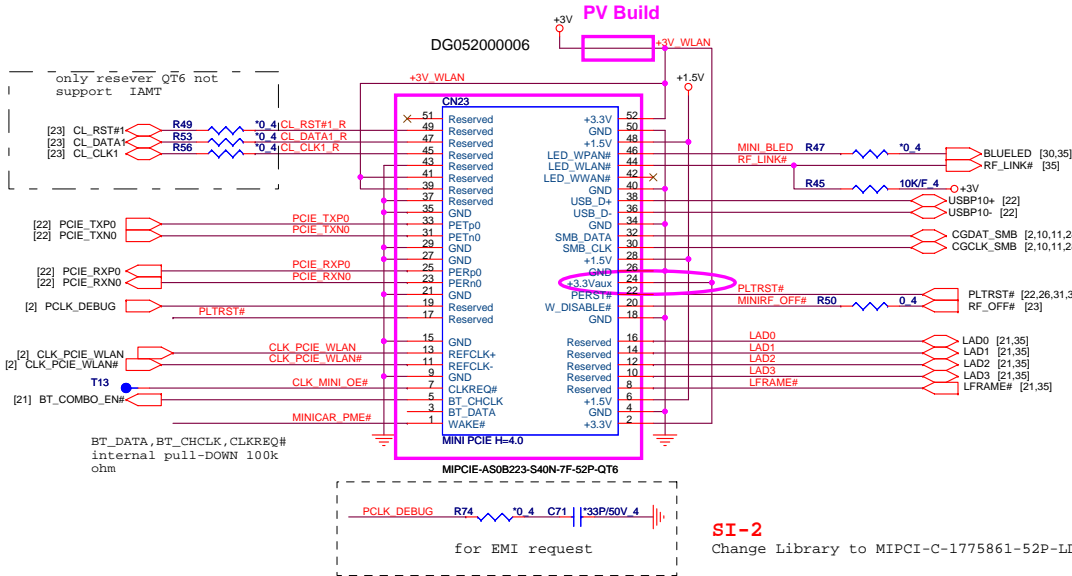
Change Layout footprint to X6179-10XXXX-8P-SOCKET(Socket)



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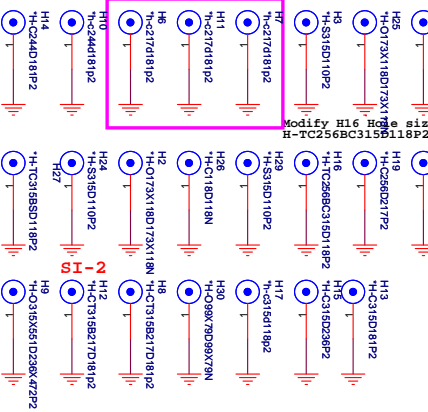
Mini PCI-E Card 1 WLAN

PV Build Delete R78 and tied the CN23#24 to R110 direction
Change CN23 layout footprint to MIPCI-E-AS0B223-S40N-7F-52P-QT6 as ME drawing

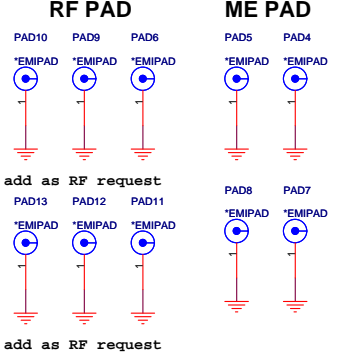


M/B Screw Hole

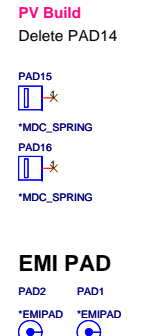
SI-2, h-e276x315d118p2



SI-2 New add as ME request

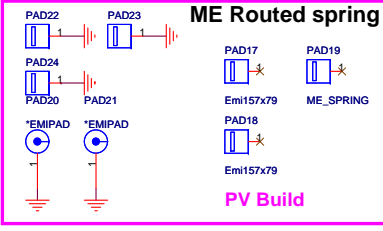


Routed spring

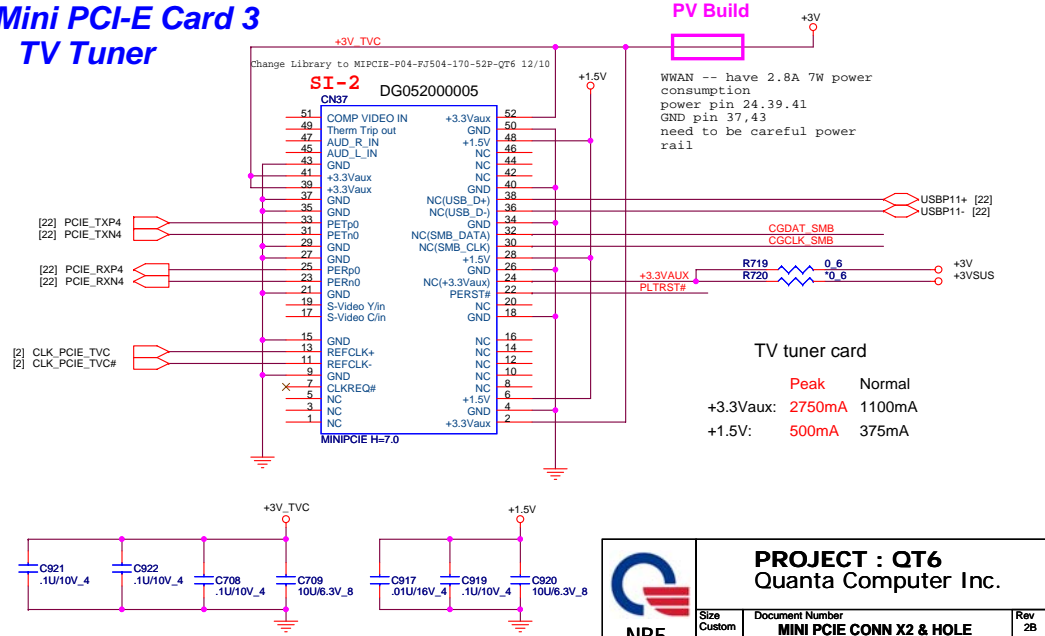


PV Build Change H1 to h-ctsbds118p2

- 1/25 Add PAD17 (Emi157x79)
- Add PAD18 (Emi157x79)
- Add PAD19 (Emi236x59)
- 1/29 Delete H4,H5 and modify battery connector
- 1/31 Change H6,H7,H11 to h-c217d181p2 as ME drawing update



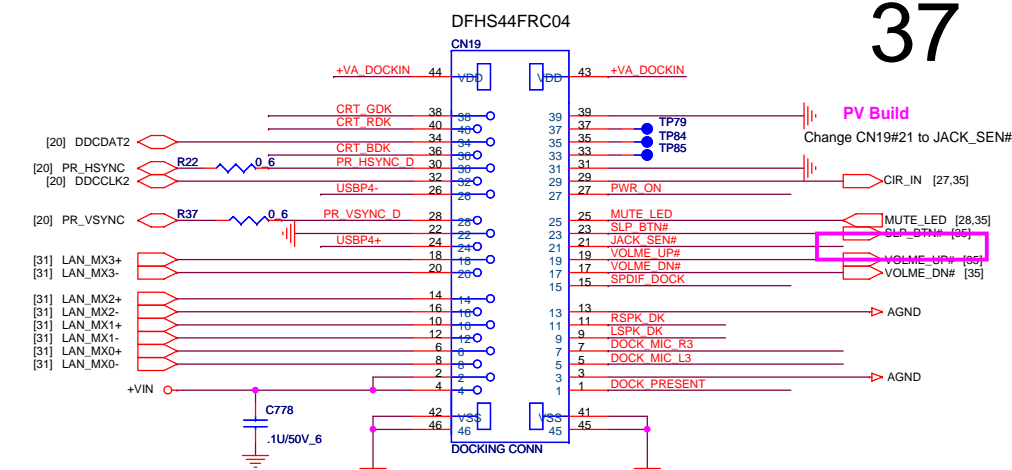
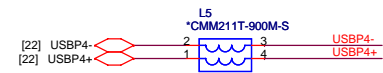
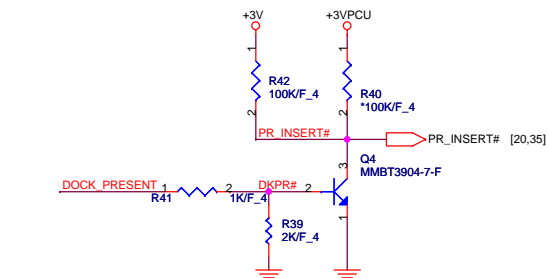
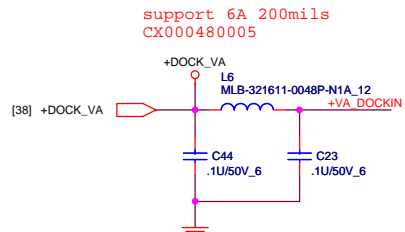
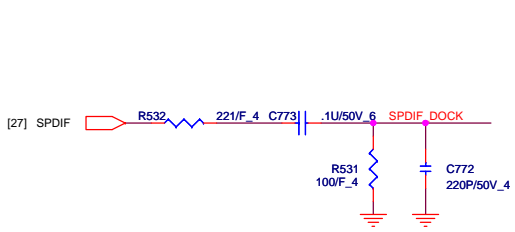
Mini PCI-E Card 3 TV Tuner



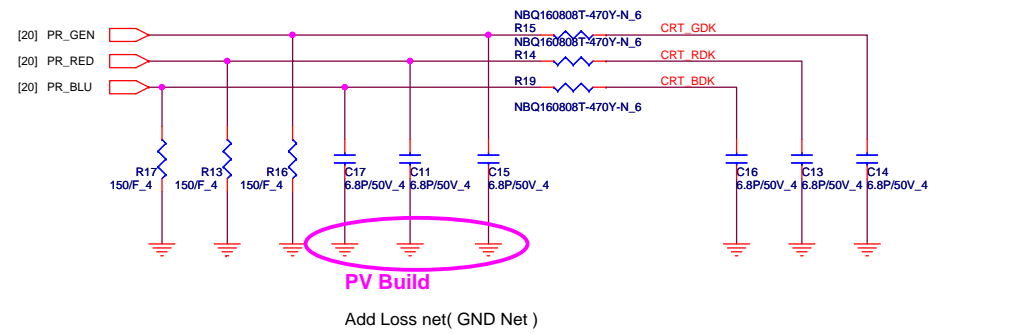
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NBS

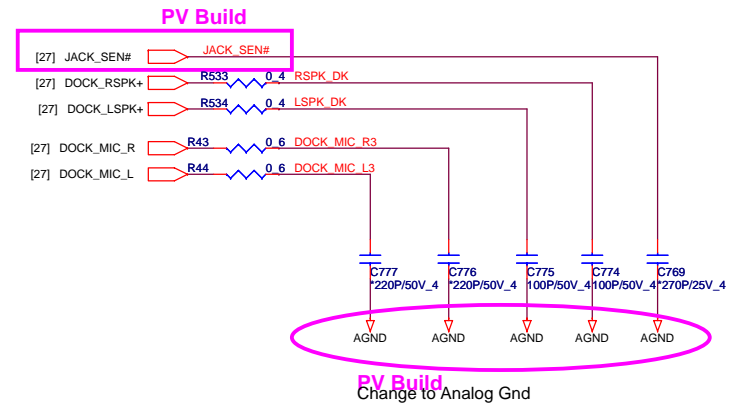
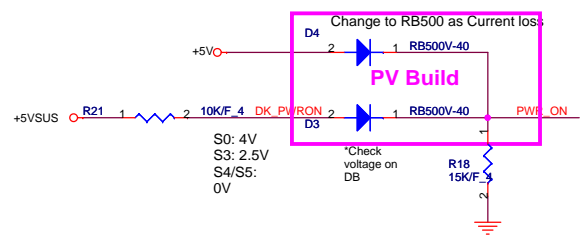
| | | |
|----------------------------------|--|--------|
| Size Custom | Document Number MINI PCIE CONN X2 & HOLE | Rev 2B |
| Date: Tuesday, February 26, 2008 | Sheet 36 of 44 | |



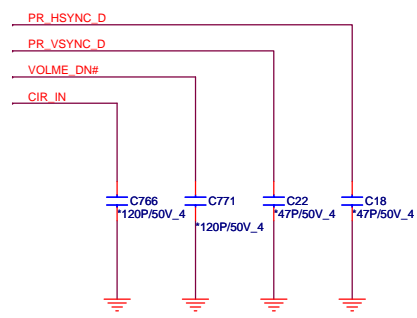
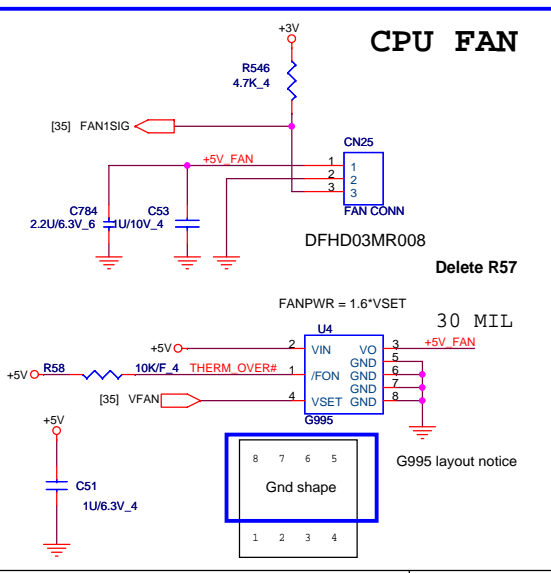
SI-2
R13,R16,R17 Change to install



Add Loss net(GND Net)

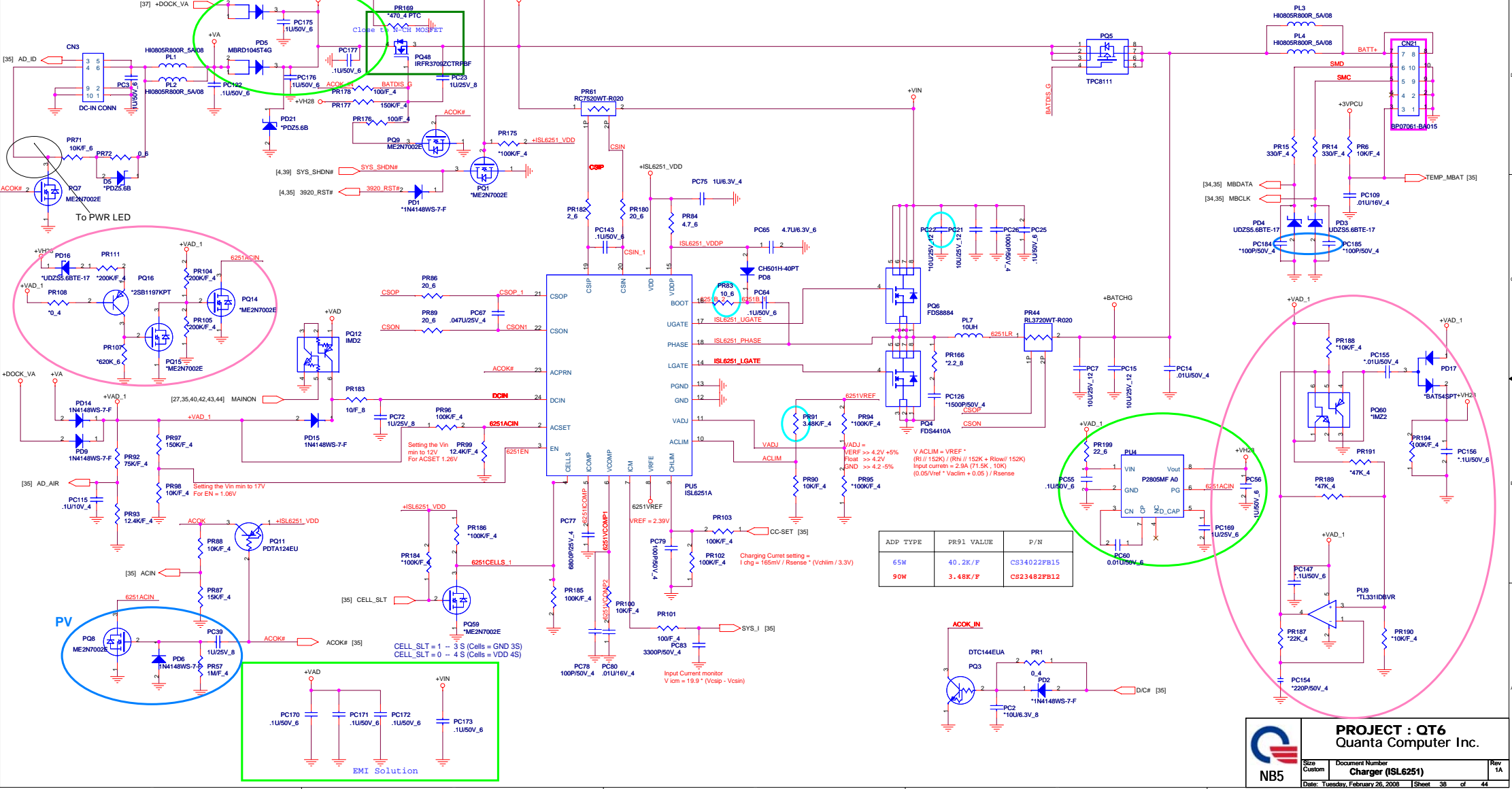


Change to Analog Gnd



| | | | |
|--|--|---|--------|
| | PROJECT : QT6 Quanta Computer Inc. | | Rev 2B |
| | Size Custom | Document Number CABLE DOCKING/FAN | |

Change CN21 to BAT-BP02083-B09065-7F-9P-QT6



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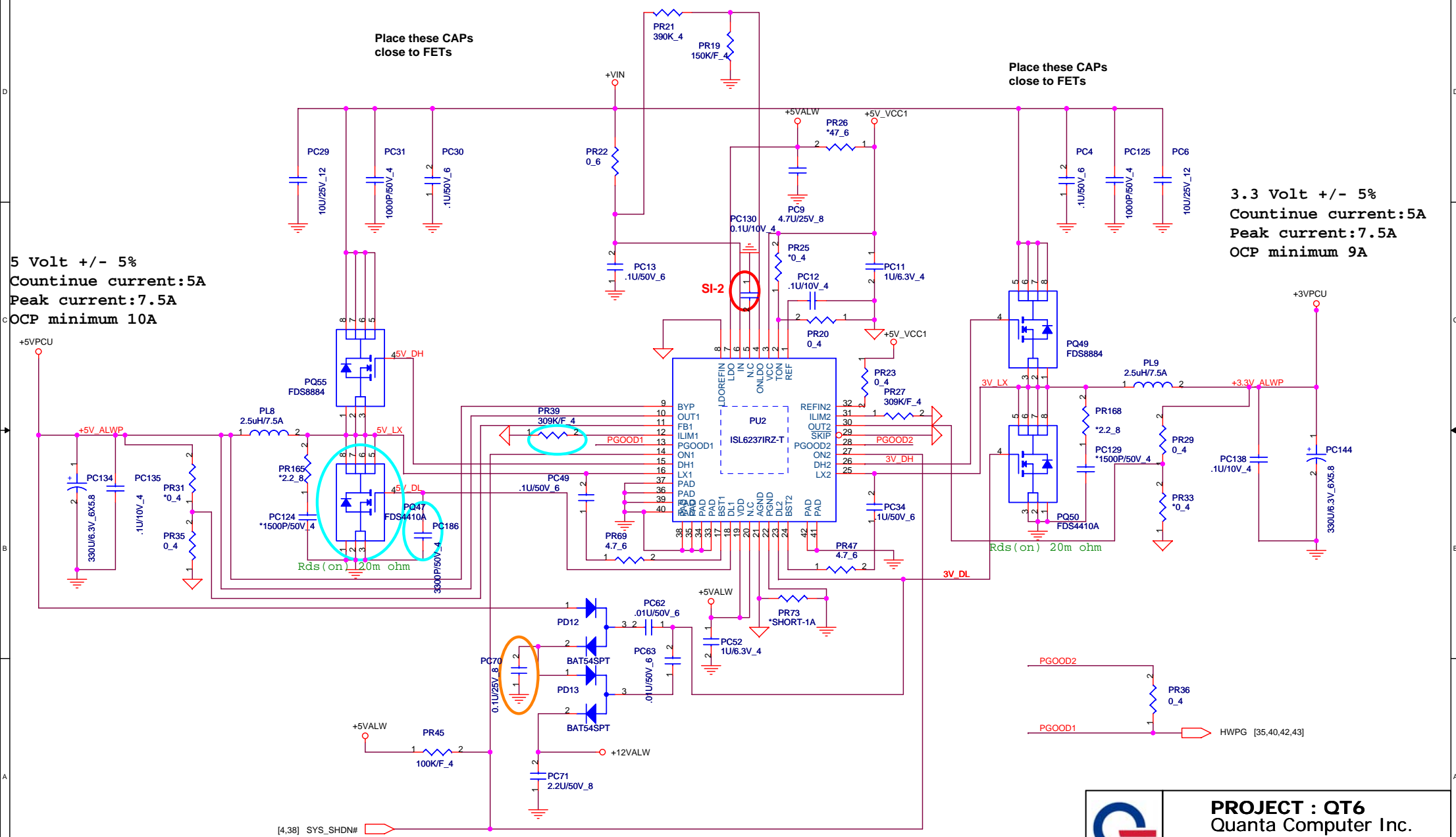
NBS

Size Custom Document Number **Charger (ISL6251)** Rev 1A
Date: Tuesday, February 26, 2008 Sheet 38 of 44

DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+12V_ALW

5 Volt +/- 5%
 Countinue current:5A
 Peak current:7.5A
 OCP minimum 10A

3.3 Volt +/- 5%
 Countinue current:5A
 Peak current:7.5A
 OCP minimum 9A



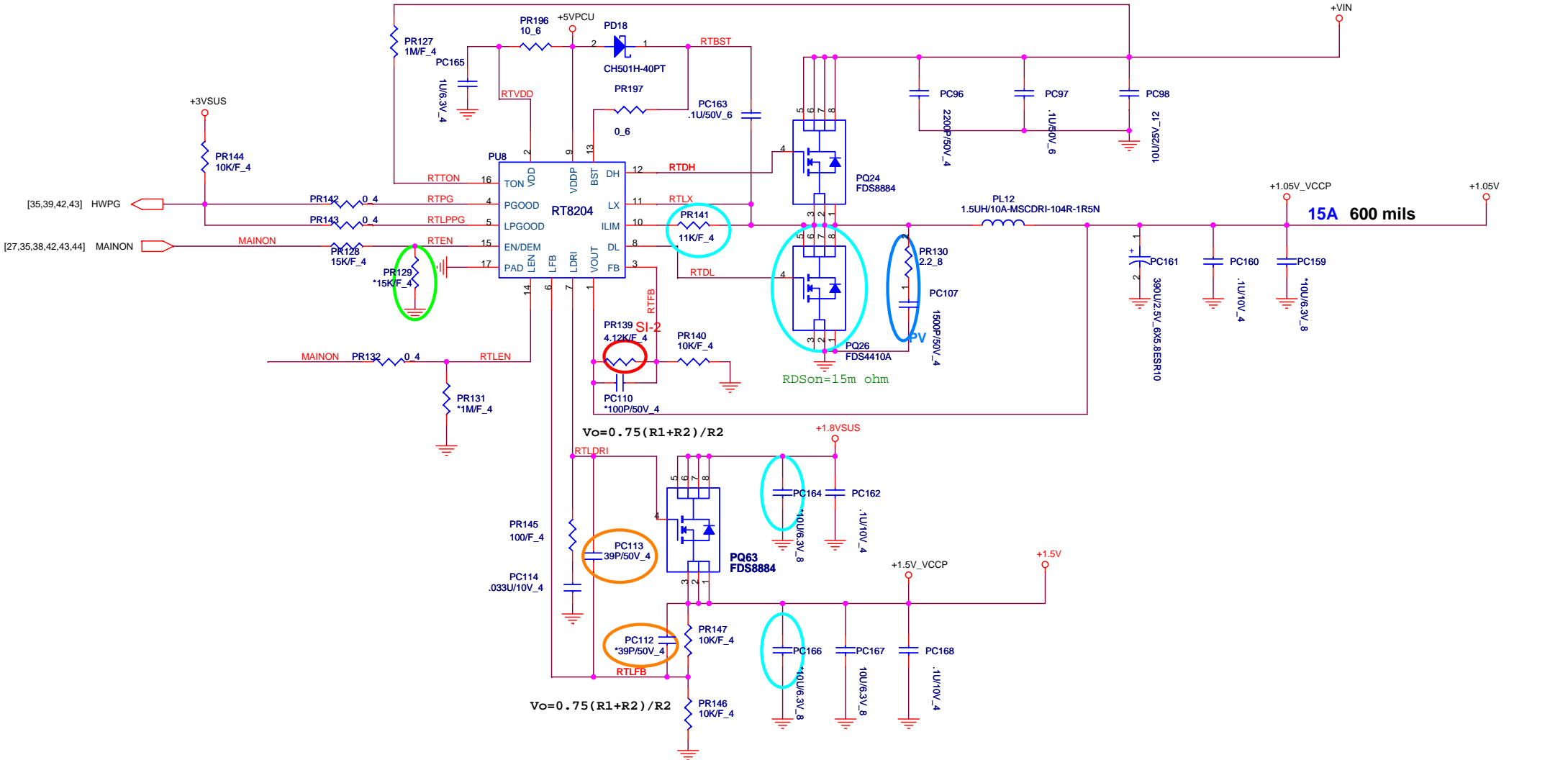
[4,38] SYS_SHDN#



| | | |
|--|---|--------|
| PROJECT : QT6 Quanta Computer Inc. | | |
| Size B | Document Number +5V/+3V (ISL6237) | Rev 1A |
| Date: Tuesday, February 26, 2008 | Sheet 39 | of 44 |


VCCP1.05V & +1.5V

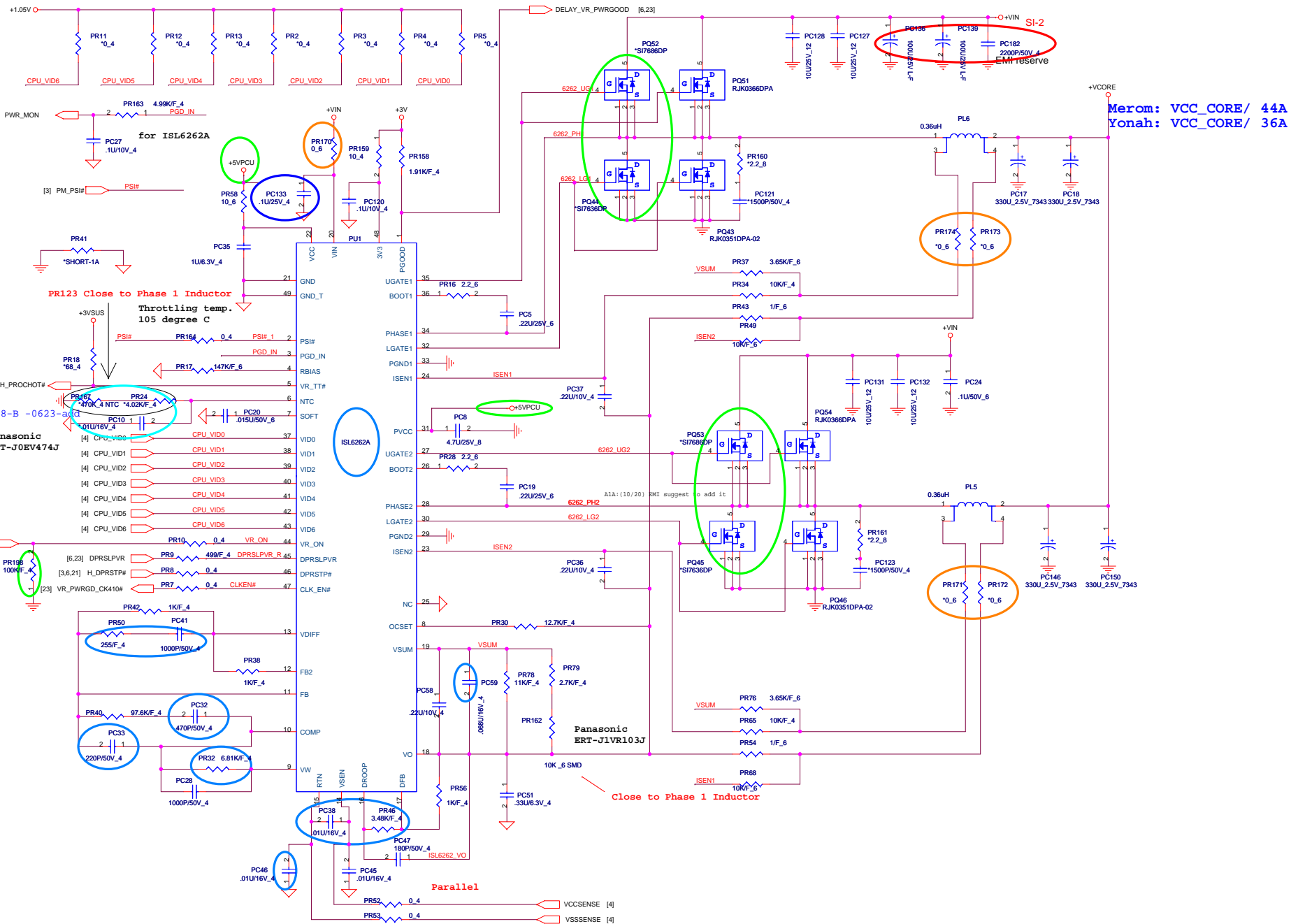
+1.05Volt +/- 5%
 Countinue current:7.5A
 Peak current:10A
 OCP minimum 15A



$$V_o = 0.75 (R1 + R2) / R2$$

$$V_o = 0.75 (R1 + R2) / R2$$

| | | |
|---|--|---|
|  | PROJECT : QT6 Quanta Computer Inc. | |
| | Size B | Document Number +1.05V/+1.5V (RT8204) |
| Date: Tuesday, February 26, 2008 | | Sheet 40 of 44 |

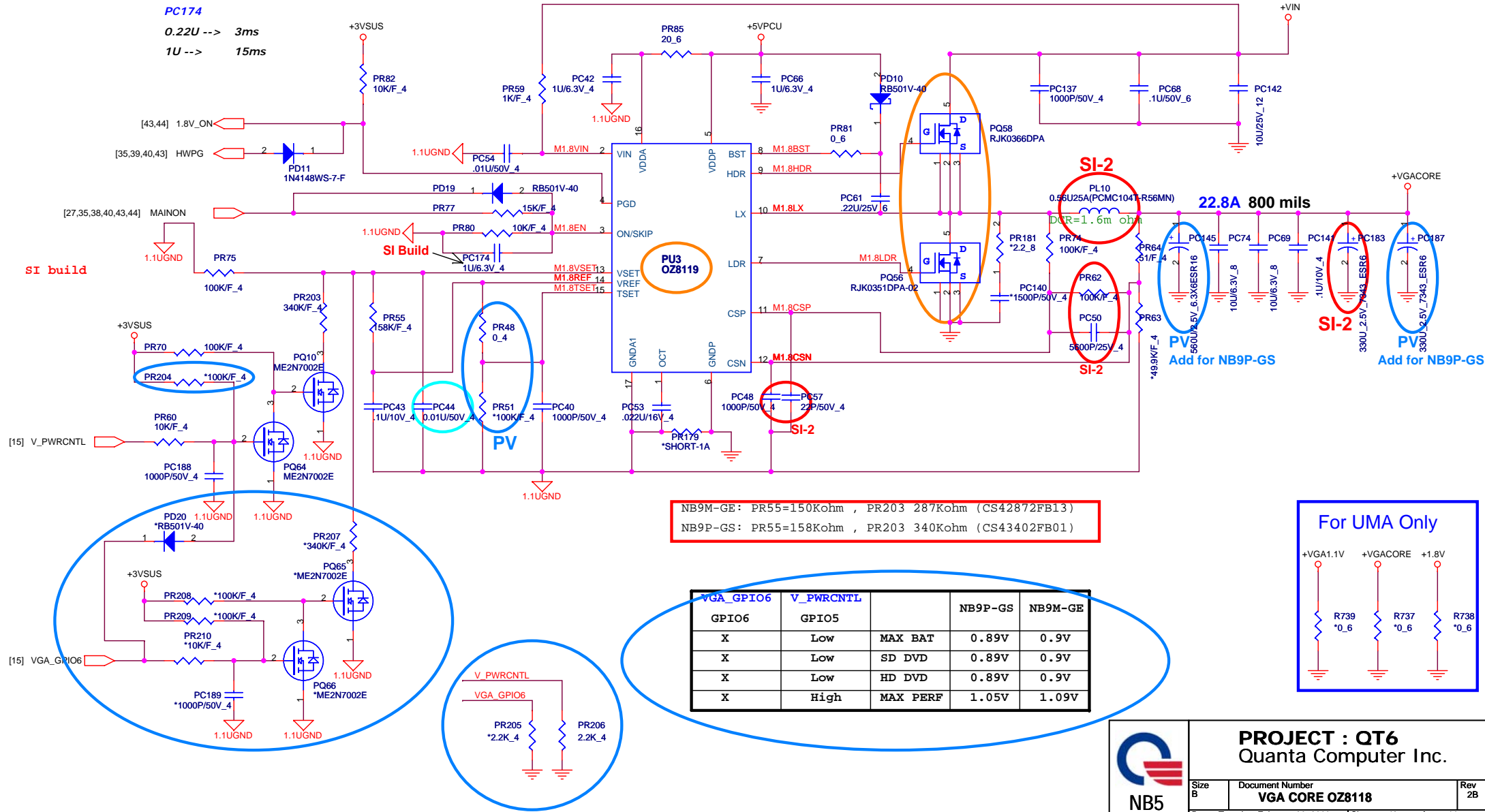


VGA Core & VCC1.1

+1.1Volt +/- 5%
 Countinue current:17.54A
 Peak current:22.8A
 OCP minimum 23A

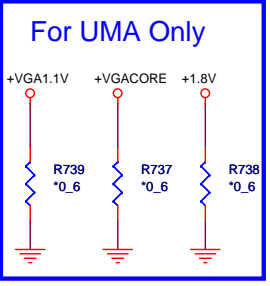
PC174

0.22U --> 3ms
 1U --> 15ms



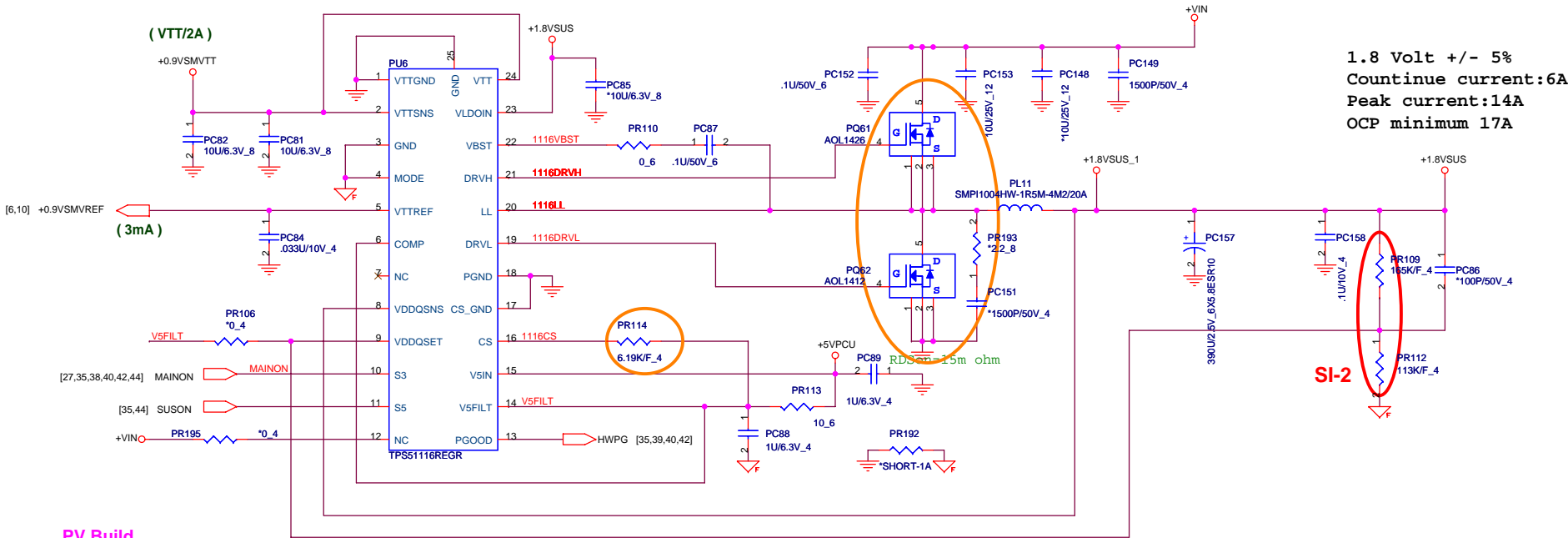
NB9M-GE: PR55=150Kohm , PR203 287Kohm (CS42872FB13)
 NB9P-GS: PR55=158Kohm , PR203 340Kohm (CS43402FB01)

| VGA_GPIO6 | V_PWRCTRL | | NB9P-GS | NB9M-GE |
|-----------|-----------|----------|---------|---------|
| X | Low | MAX BAT | 0.89V | 0.9V |
| X | Low | SD DVD | 0.89V | 0.9V |
| X | Low | HD DVD | 0.89V | 0.9V |
| X | High | MAX PERF | 1.05V | 1.09V |



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| | | |
|----------------------------------|---|--------|
| Size B | Document Number VGA CORE OZ8118 | Rev 2B |
| Date: Tuesday, February 26, 2008 | Sheet 42 | of 44 |



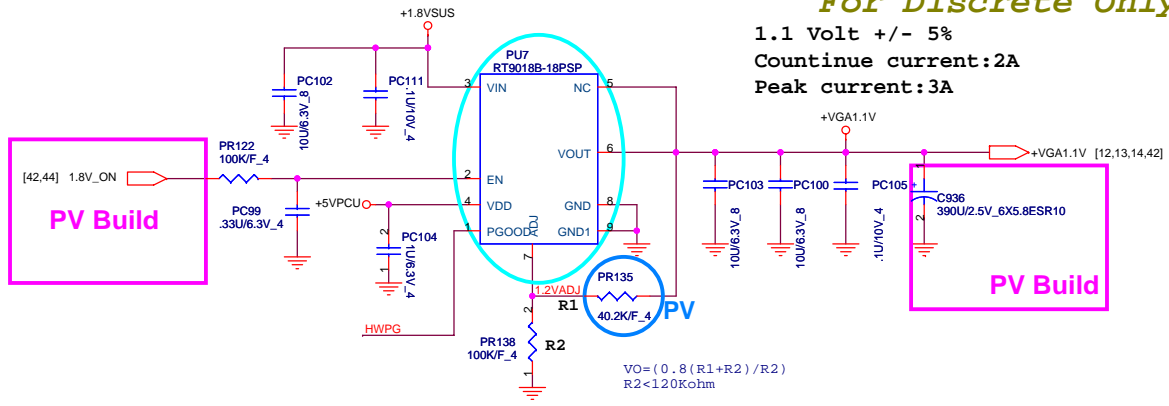
1.8 Volt +/- 5%
 Countinue current:6A
 Peak current:14A
 OCP minimum 17A

PV Build

Change PR122 tied to 1.8V_ON as power sequence reuqest

For Discrete Only

1.1 Volt +/- 5%
 Countinue current:2A
 Peak current:3A

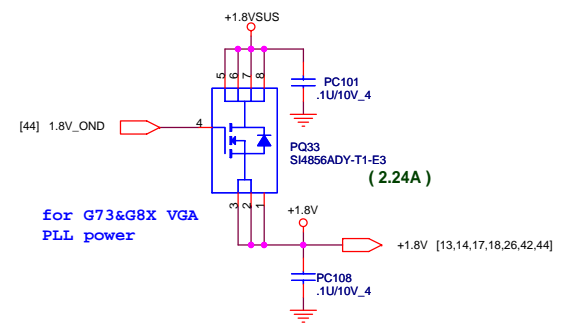


PV Build

PV Build

$$VO = (0.8(R1+R2) / R2)$$

$$R2 < 1.20Kohm$$

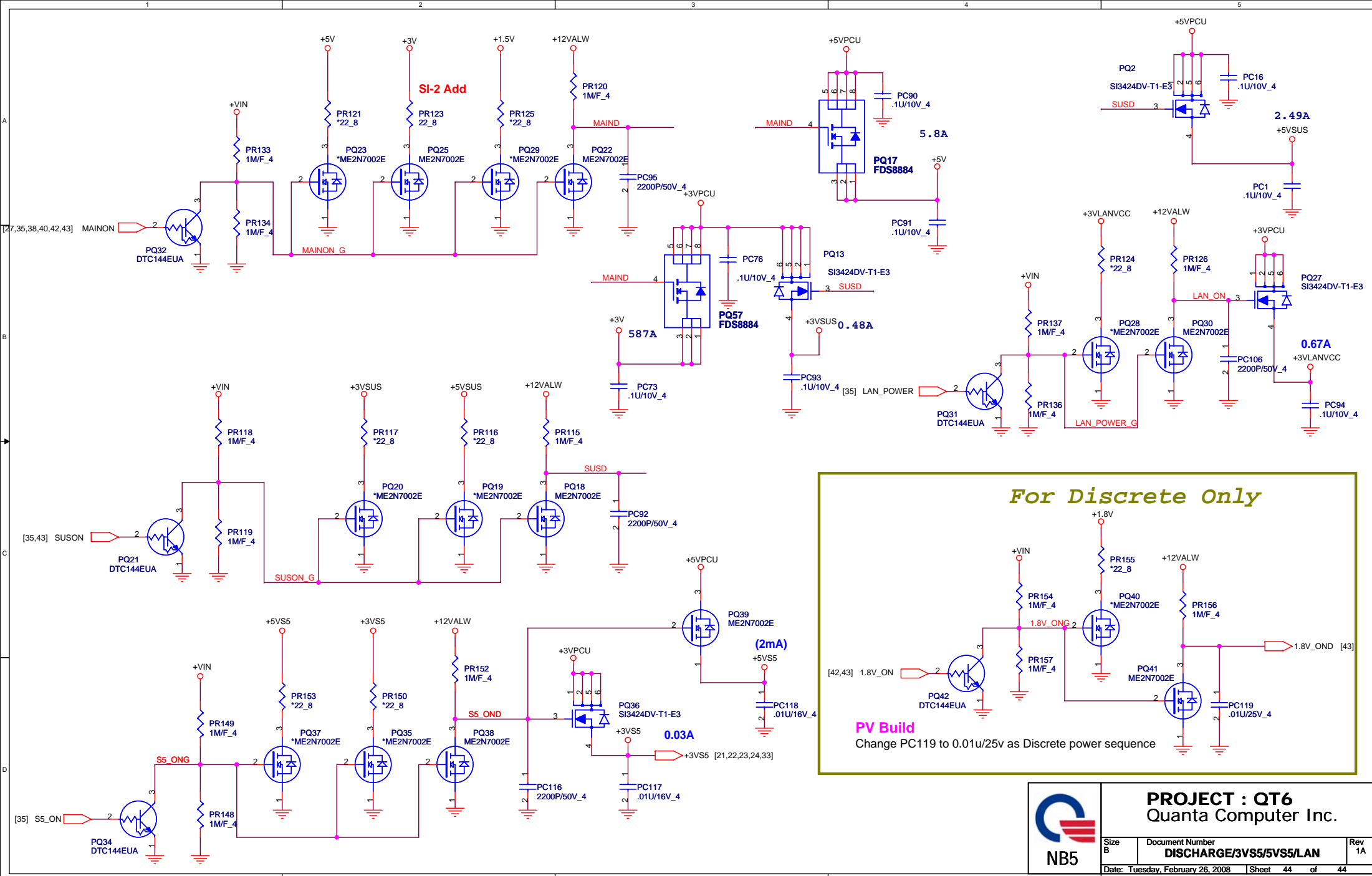


for G73&G8X VGA
 PLL power



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| | | |
|---|---|--------|
| Size Custom | Document Number 1.8V/DDR_VTER/+1.8v/+1.1V | Rev 3A |
| Date: Tuesday, February 26, 2008 Sheet 43 of 44 | | |



SI-2 Add

For Discrete Only

PV Build
Change PC119 to 0.01u/25V as Discrete power sequence



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| | | |
|----------------------------------|---|-----------|
| Size B | Document Number DISCHARGE/3VS5/5VS5/LAN | Rev 1A |
| Date: Tuesday, February 26, 2008 | Sheet 44 of 44 | |