

DDD UMA

SI Build(Final)

2007.03.30

DATE	CHANGE NO.	REV

DRAWER	EE	DATE	POWER	DATE	INVENTEC			
DESIGN					TITLE DDD UMA			
CHECK								
RESPONSIBLE								
SIZE =	3			VER :	SIZE A3	CODE CS	DOC. NUMBER	REV
FILE NAME :	XXXX-XXXXXX-XX						<i>Model No.</i>	<i>AXI</i>
P/N	XXXXXXXXXXXX					SHEET	1	OF 48

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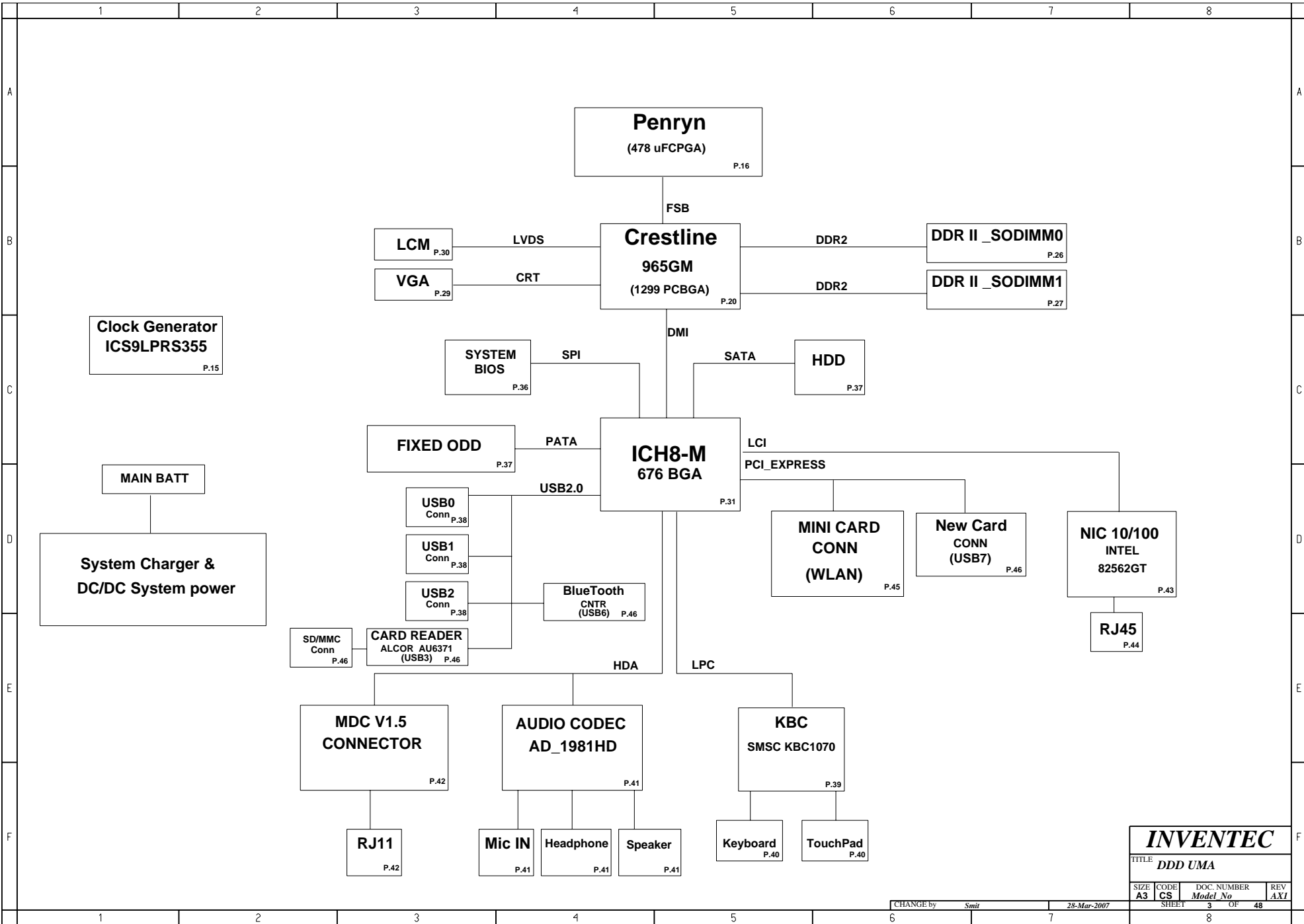
INVENTEC

TITLE
DDD UMA

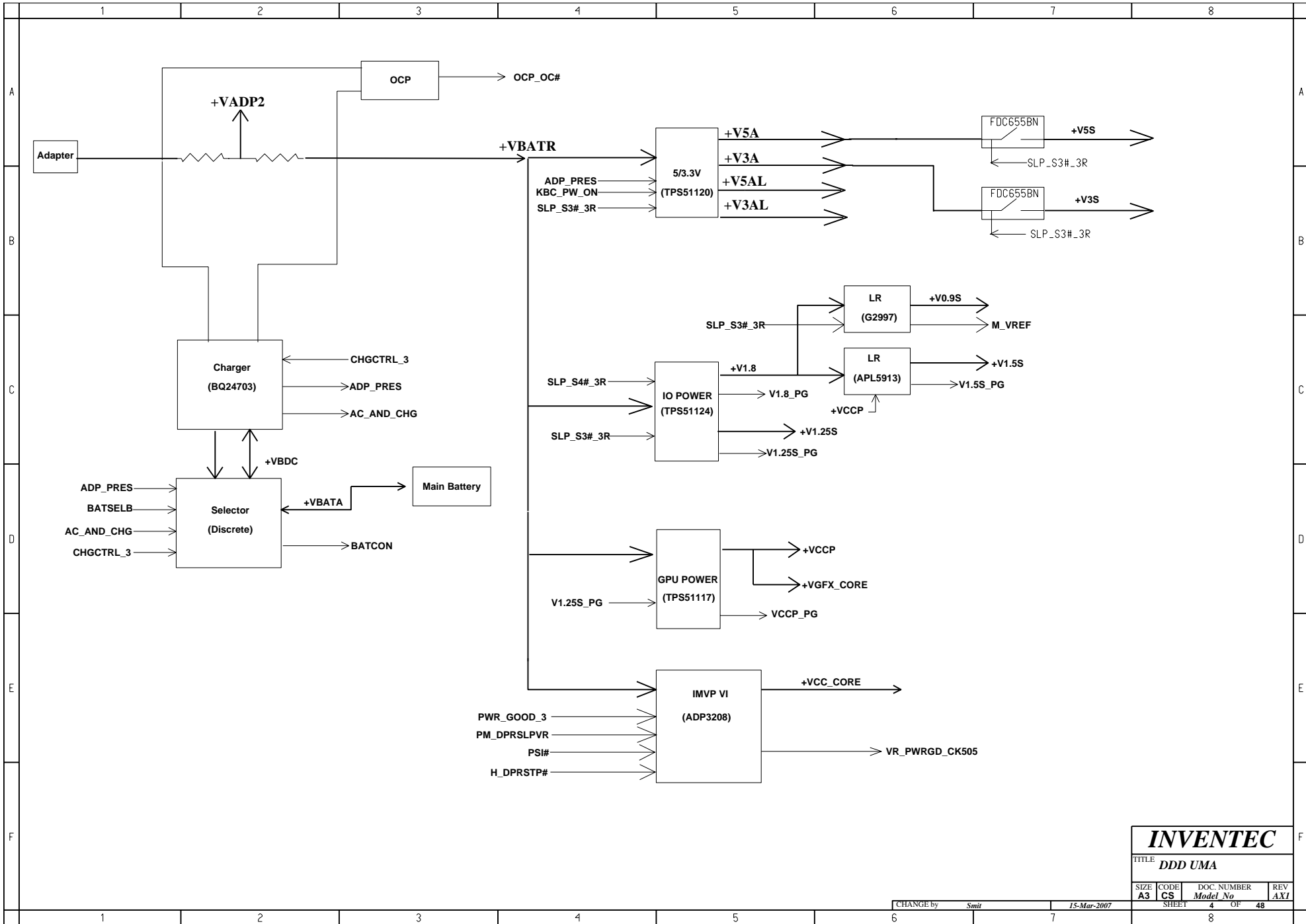
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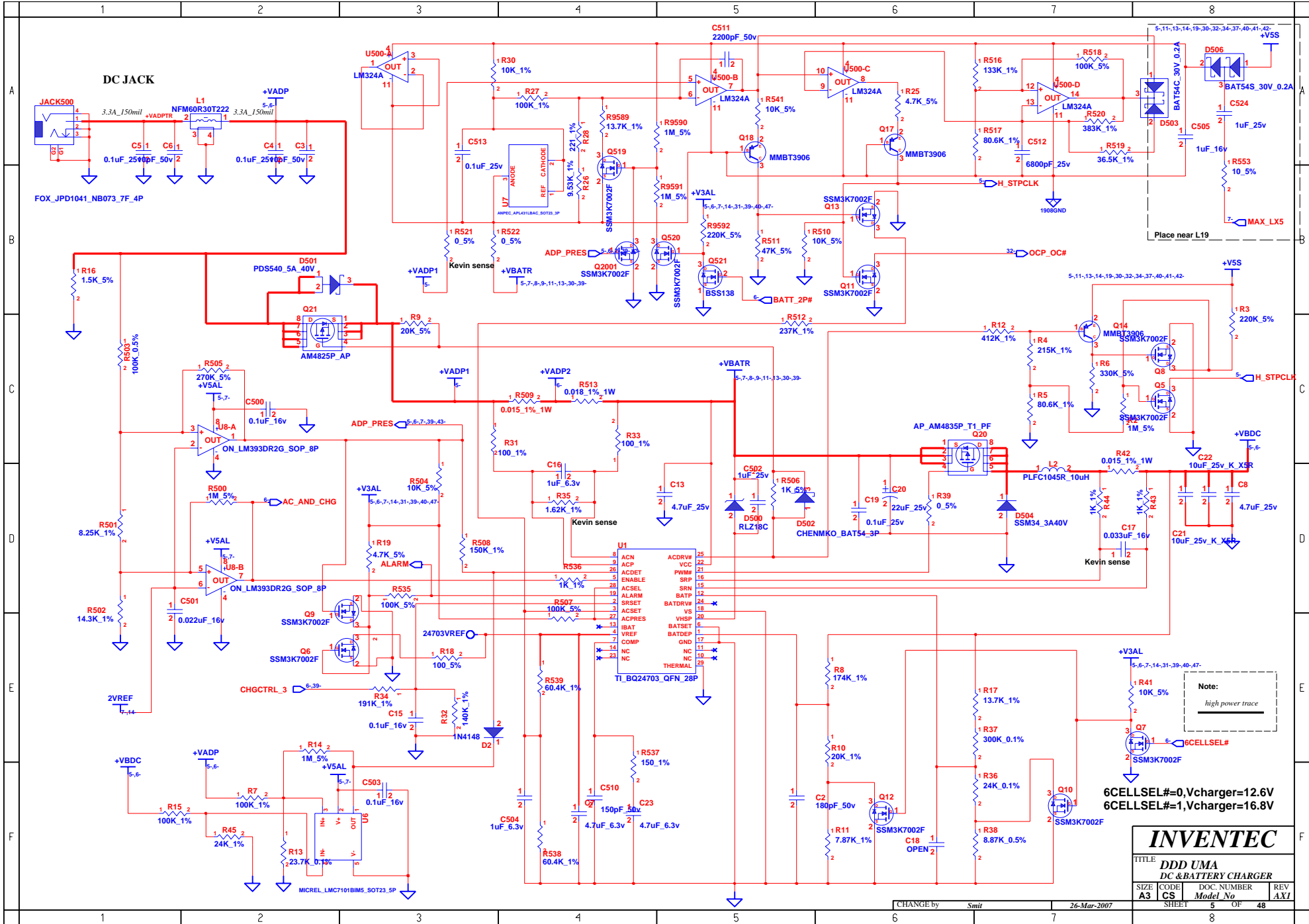
CHANGE by *Smit* 23-Mar-2007

SHEET **2** OF **48**



INVENTEC			
TITLE DDD UMA			
SIZE A3	CODE CS	DOC. NUMBER <i>Model No</i>	REV AX1
CHANGE by <i>Smit</i>		28-Mar-2007	SHEET 3 OF 48

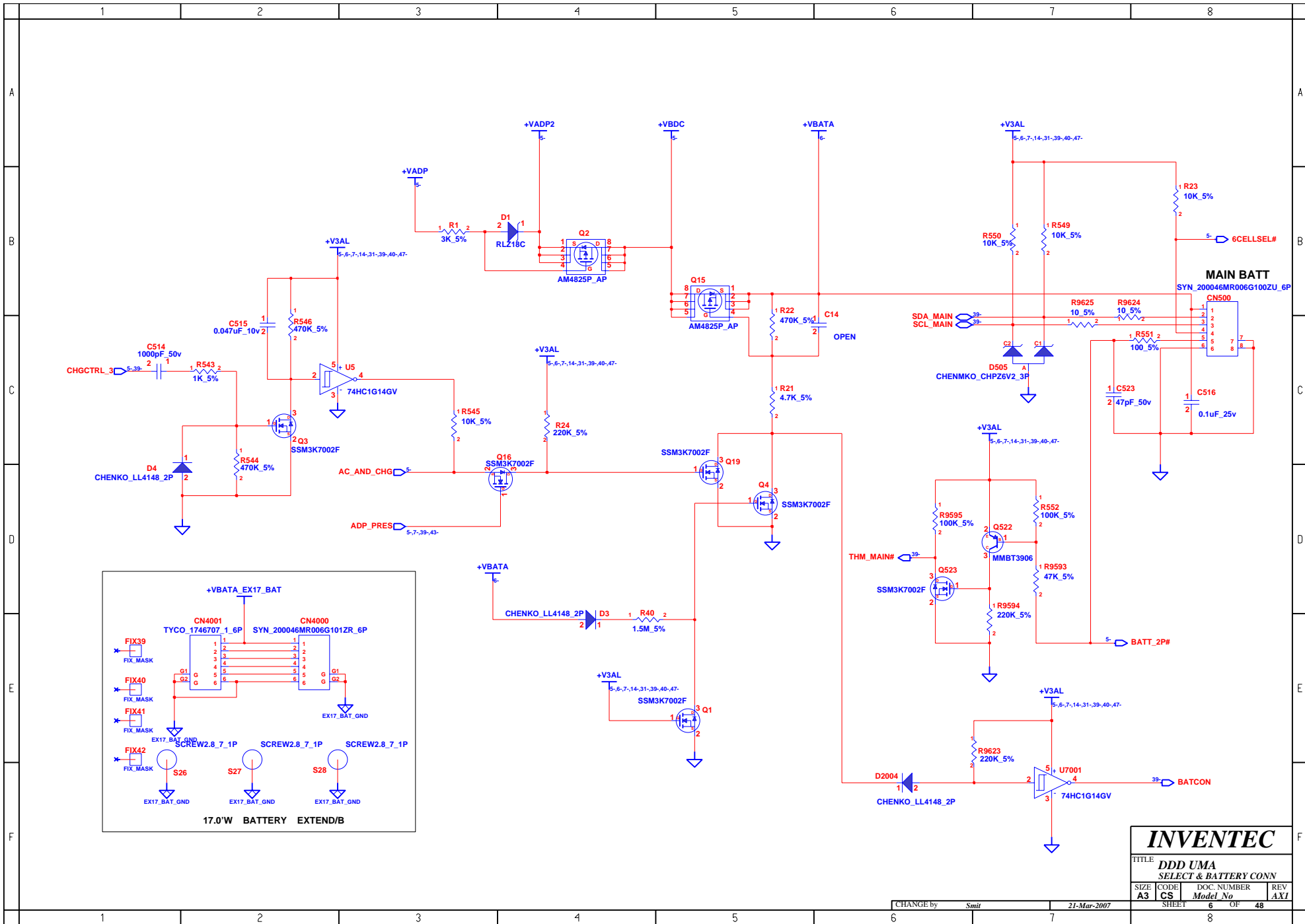




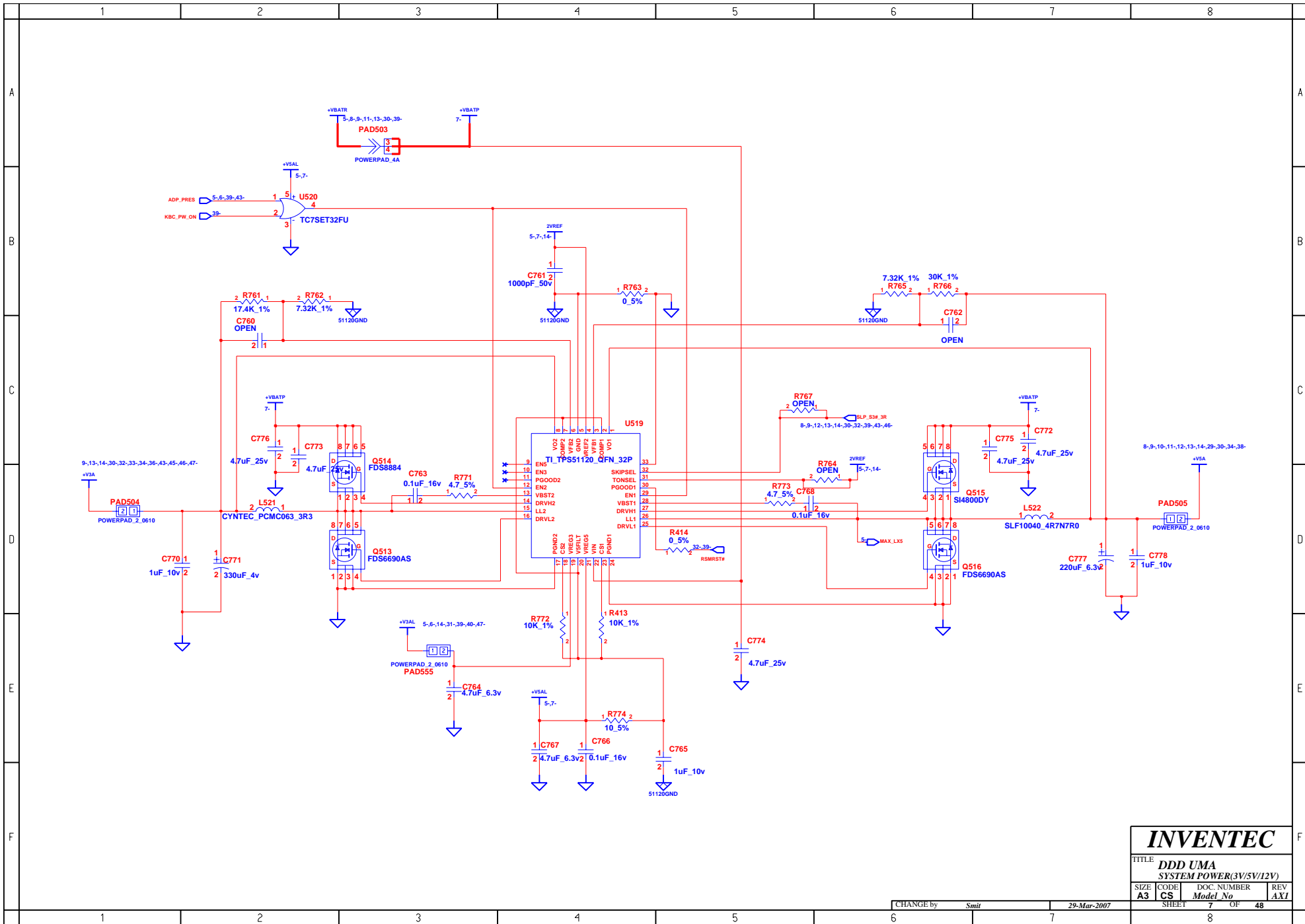
Note:
high power trace

6CELLSEL#=0, Vcharger=12.6V
6CELLSEL#=1, Vcharger=16.8V

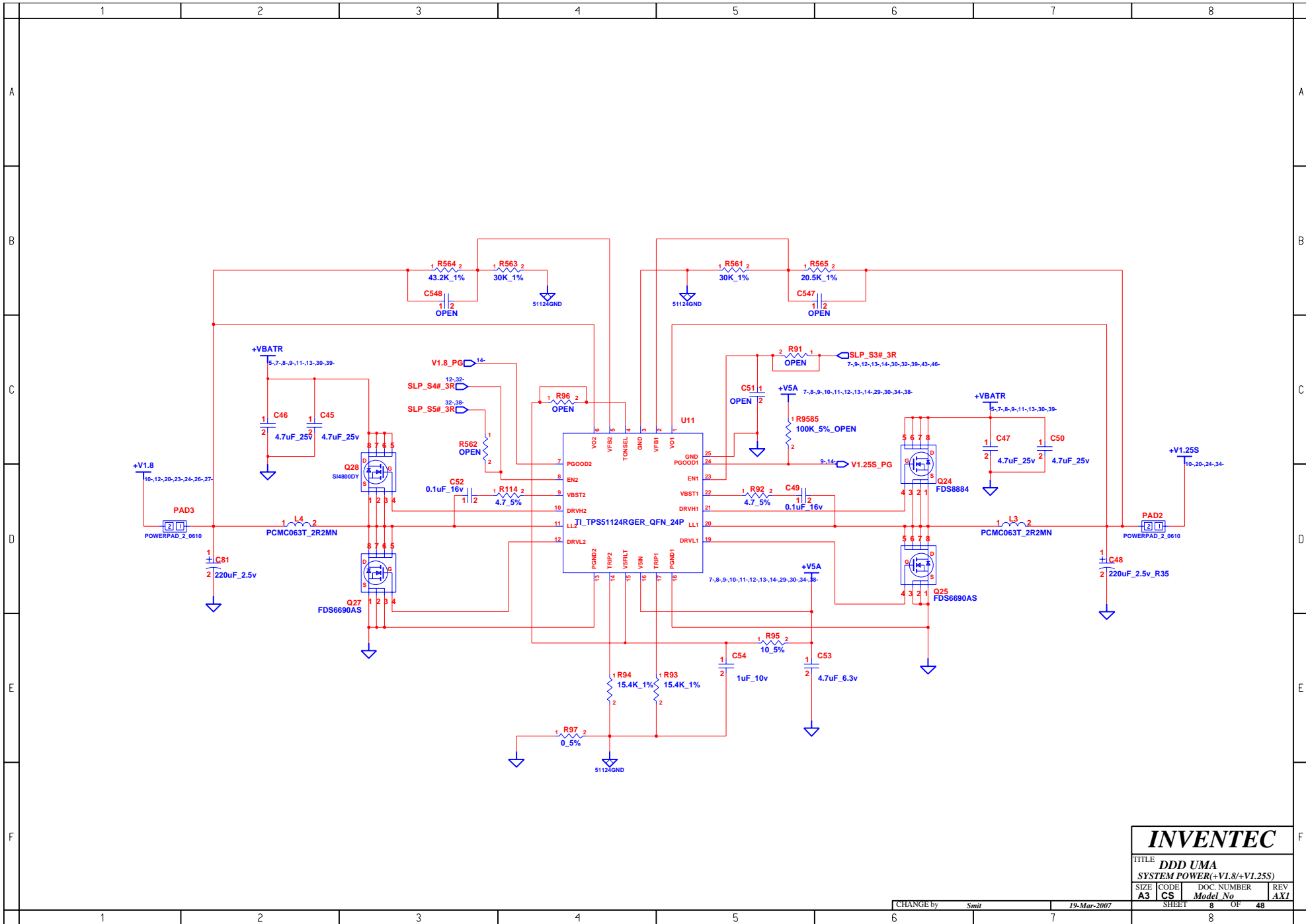
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SIZE A3	CODE CS	DOC NUMBER Model No	REV AX1
CHANGE by Smit		26-Mar-2007	
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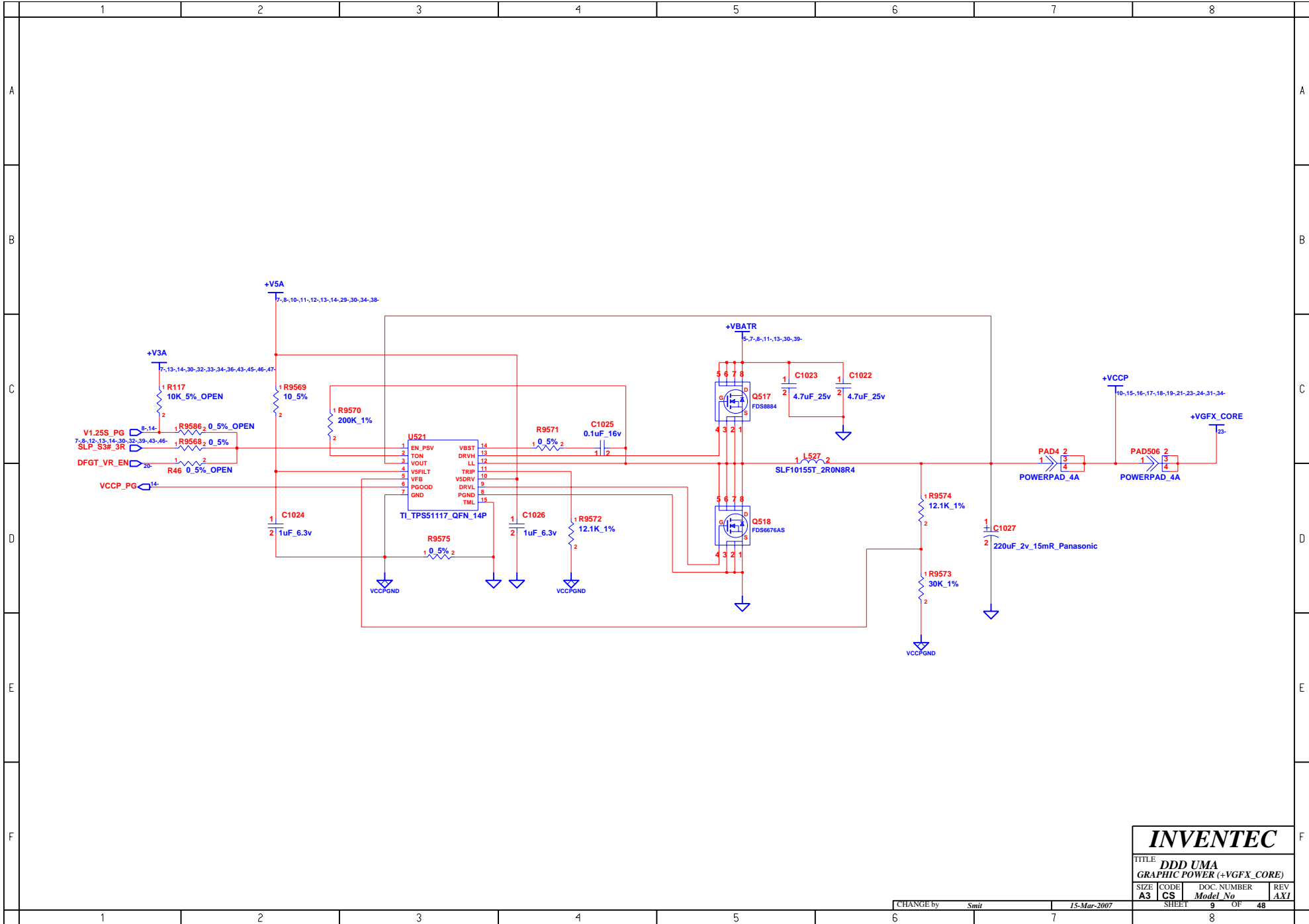
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SIZE A3	CODE CS	DOC. NUMBER <i>Model No</i>	REV AXI
CHANGE by <i>Smit</i>		21-Mar-2007	
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INVENTEC			
TITLE DDD UMA SYSTEM POWER(3V/5V/12V)			
SIZE A3	CODE CS	DOC. NUMBER <i>Model No</i>	REV AXI
CHANGE by <i>Smit</i>		29-Mar-2007	SHEET 7 OF 48



INVENTEC			
TITLE DDD UMA			
SYSTEM POWER(+V1.8/+V1.25S)			
SIZE A3	CODE CS	DOC. NUMBER Model No	REV AXI
CHANGE by <i>Smit</i>		19-Mar-2007	
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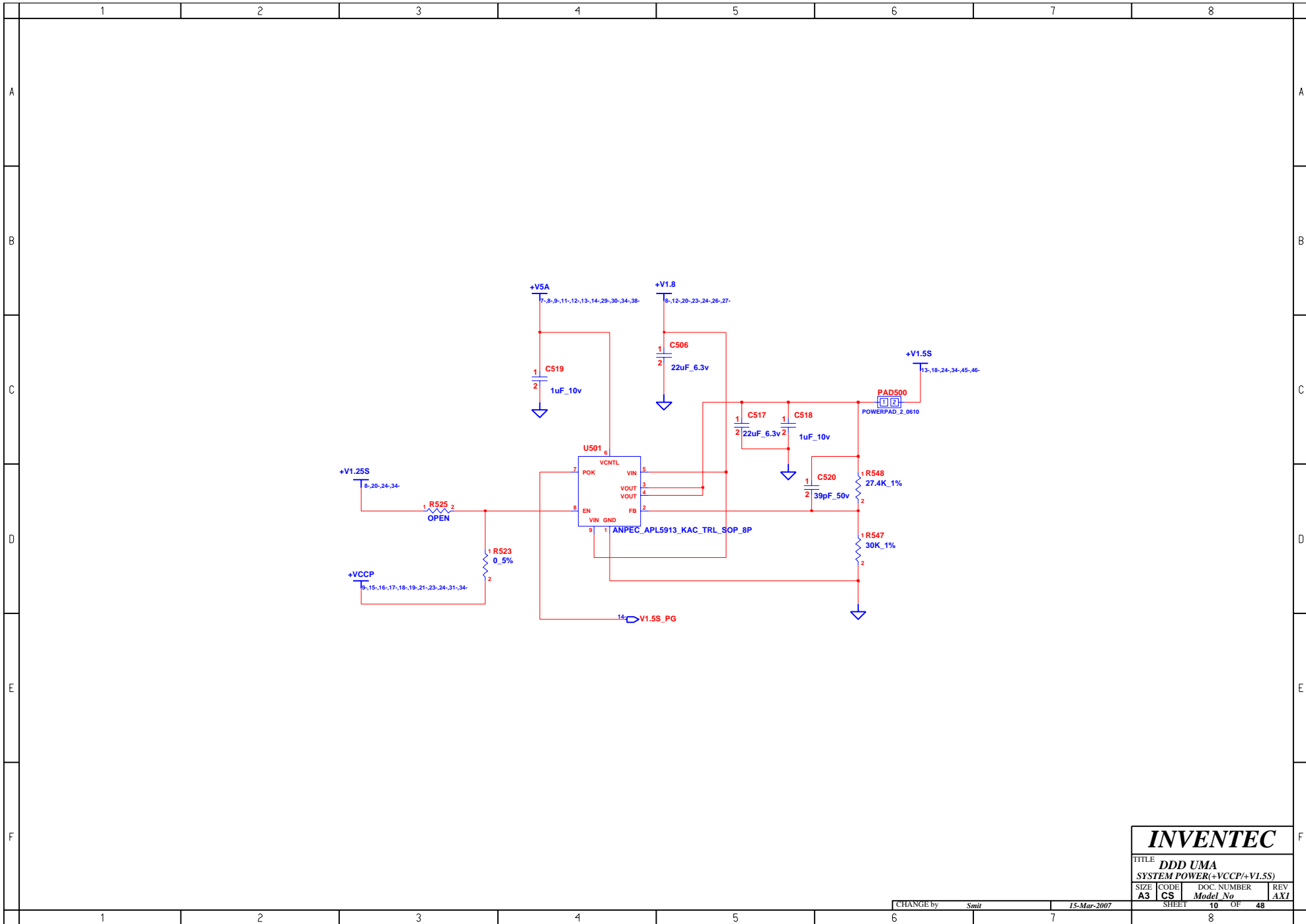
INVENTEC

TITLE **DDD UMA**
GRAPHIC POWER (+VGFX_CORE)

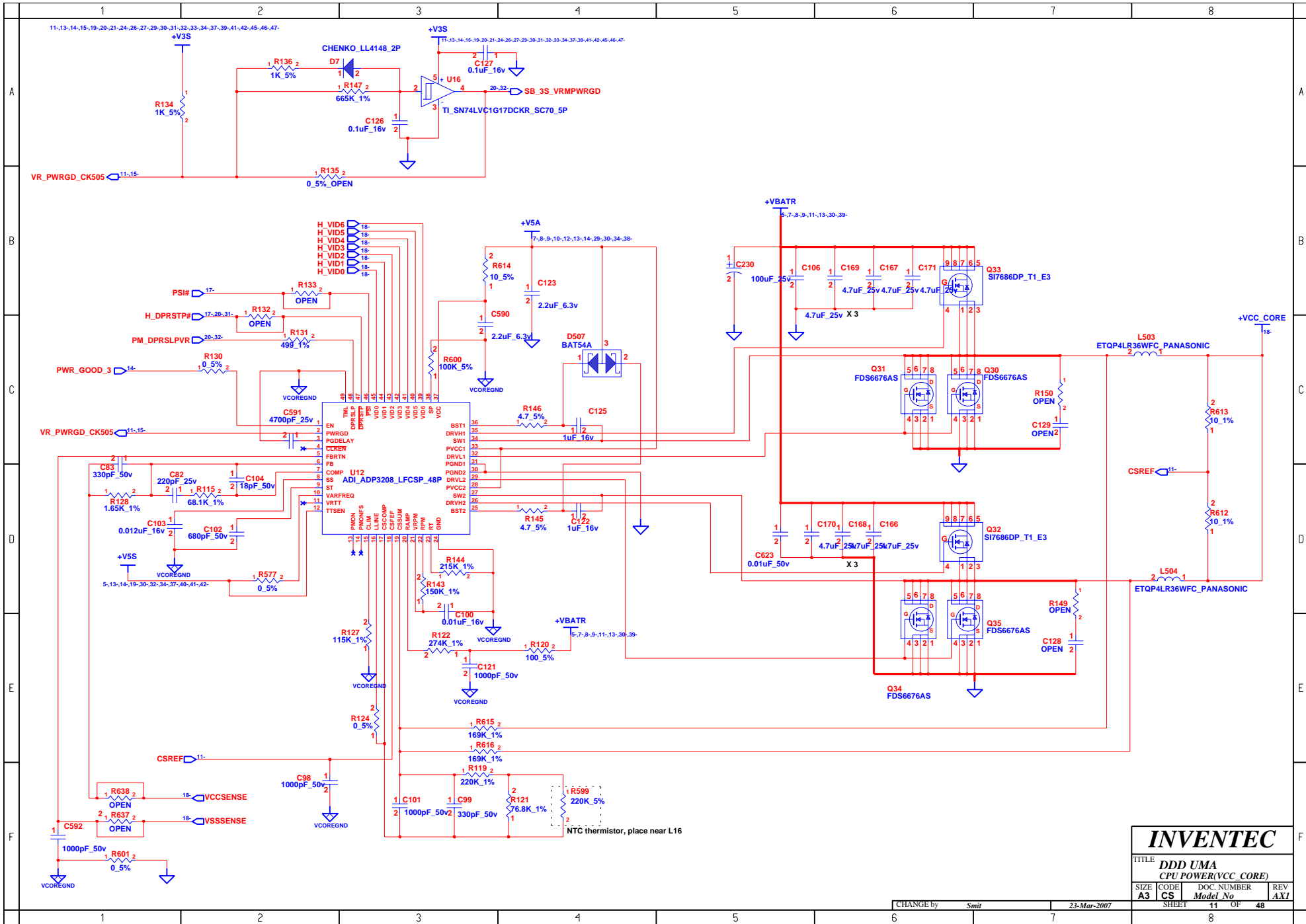
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A3	CS	Model No	AXI

CHANGE by *Smit* 15-Mar-2007

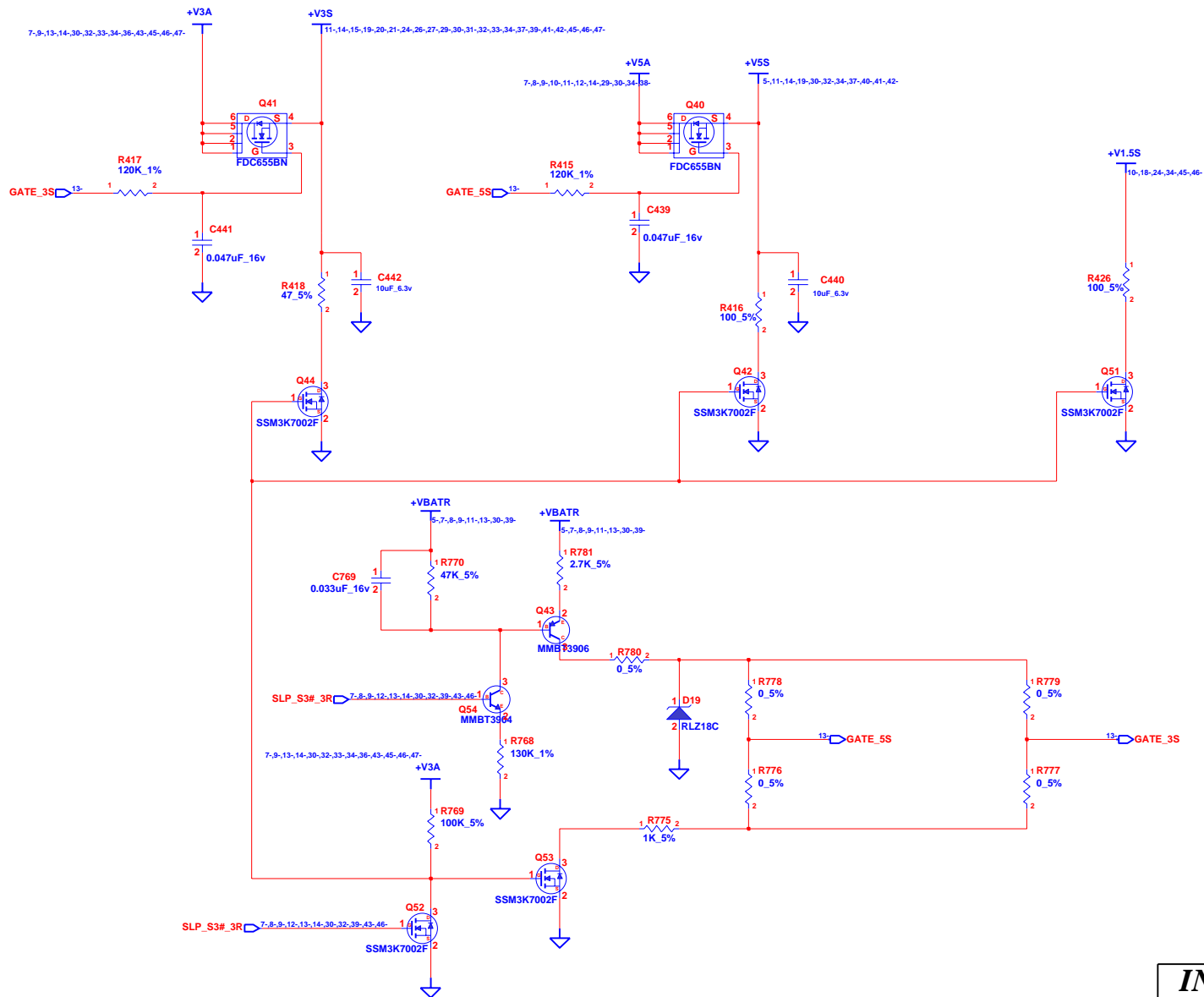
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INVENTEC			
TITLE DDD UMA			
SYSTEM POWER(+VCCP/+V1.5S)			
SIZE A3	CODE CS	DOC. NUMBER	REV AXI
CHANGE by <i>Smit</i>		DATE <i>15-Mar-2007</i>	SHEET 10 OF 48



INVENTEC			
TITLE DDD UMA CPU POWER(VCC_CORE)			
SIZE A3	CODE CS	DOC NUMBER Model No	REV AXI
CHANGE by Smit		23-Mar-2007	
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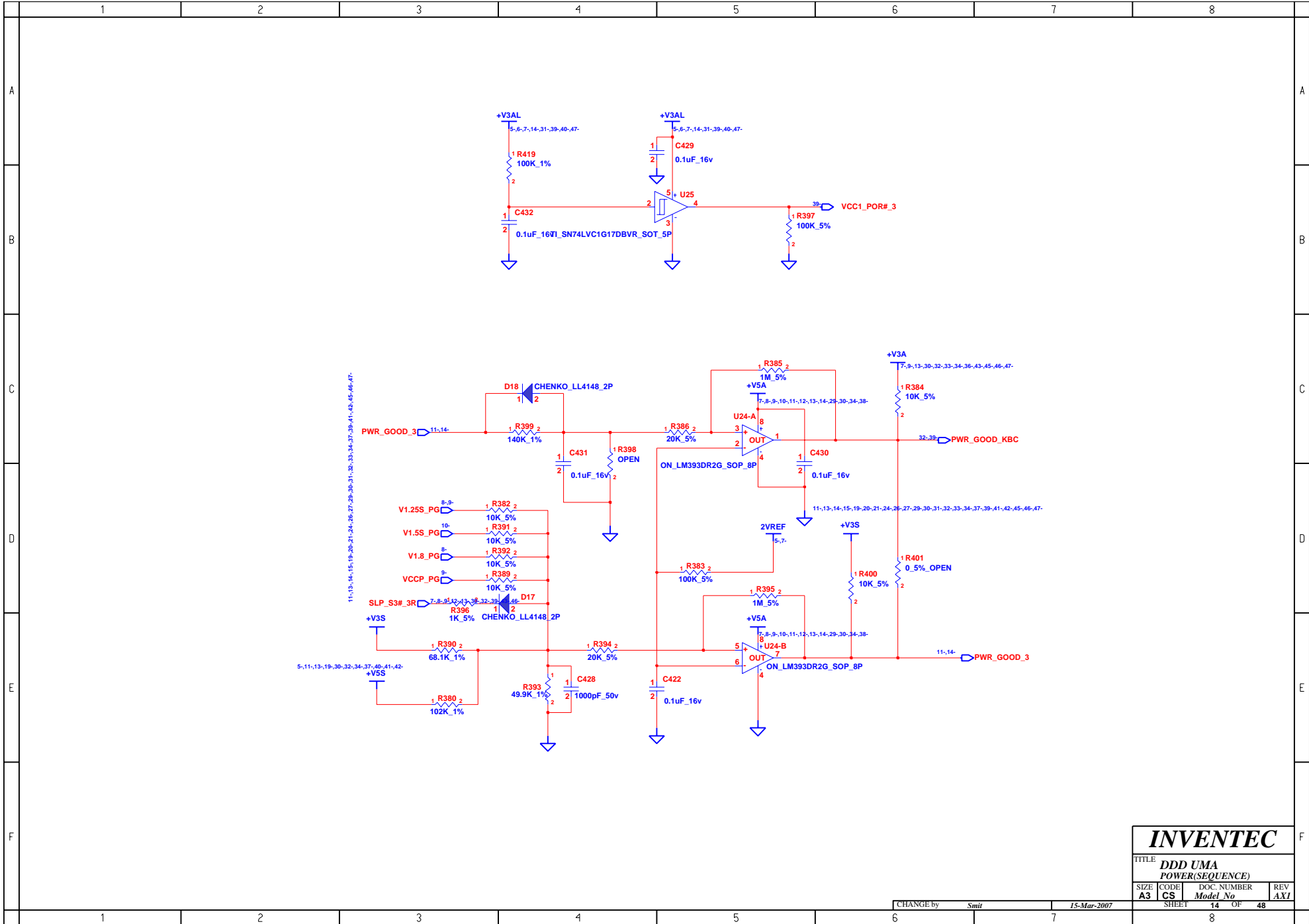


INVENTEC

TITLE			
DDD UMA			
POWER(SLEEP)			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	Model No	AXI

CHANGE by Smit 15-Mar-2007

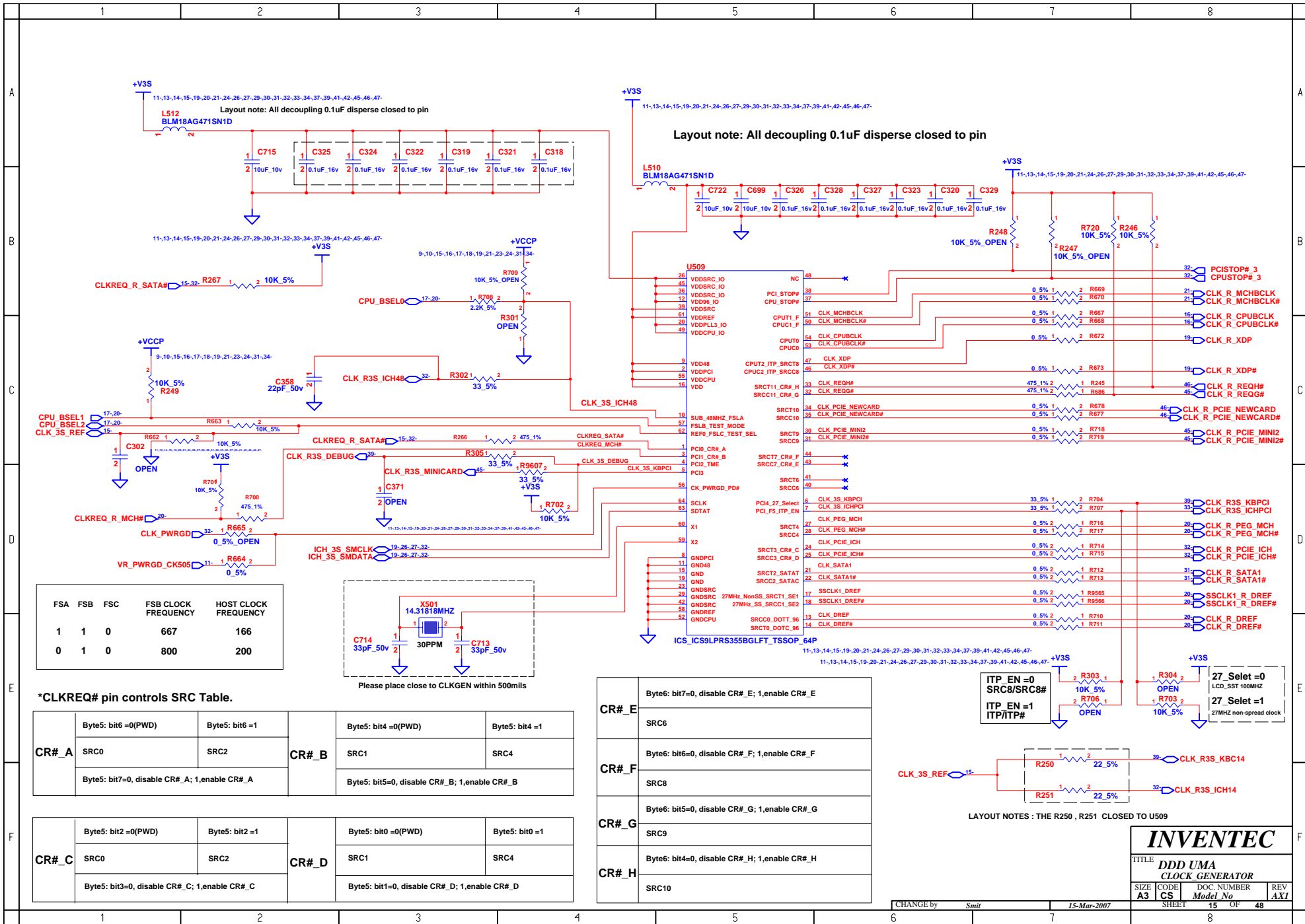
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INVENTEC

TITLE			
DDD UMA			
POWER(SEQUENCE)			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	Model No	AXI

CHANGE by Smit 15-Mar-2007



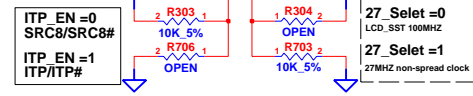
FSA	FSB	FSC	FSB CLOCK FREQUENCY	HOST CLOCK FREQUENCY
1	1	0	667	166
0	1	0	800	200

*CLKREQ# pin controls SRC Table.

CR#_A	Byte5: bit6 =0(PWD)		Byte5: bit6 =1		CR#_B	Byte5: bit4 =0(PWD)		Byte5: bit4 =1	
	SRC0	SRC2	SRC1	SRC4		SRC0	SRC2	SRC1	SRC4
Byte5: bit7=0, disable CR#_A; 1,enable CR#_A		Byte5: bit5=0, disable CR#_B; 1,enable CR#_B							

CR#_C	Byte5: bit2 =0(PWD)		Byte5: bit2 =1		CR#_D	Byte5: bit0 =0(PWD)		Byte5: bit0 =1	
	SRC0	SRC2	SRC1	SRC4		SRC0	SRC2	SRC1	SRC4
Byte5: bit3=0, disable CR#_C; 1,enable CR#_C		Byte5: bit1=0, disable CR#_D; 1,enable CR#_D							

CR#_E	Byte6: bit7=0, disable CR#_E; 1,enable CR#_E	SRC6
CR#_F	Byte6: bit6=0, disable CR#_F; 1,enable CR#_F	SRC8
CR#_G	Byte6: bit5=0, disable CR#_G; 1,enable CR#_G	SRC9
CR#_H	Byte6: bit4=0, disable CR#_H; 1,enable CR#_H	SRC10



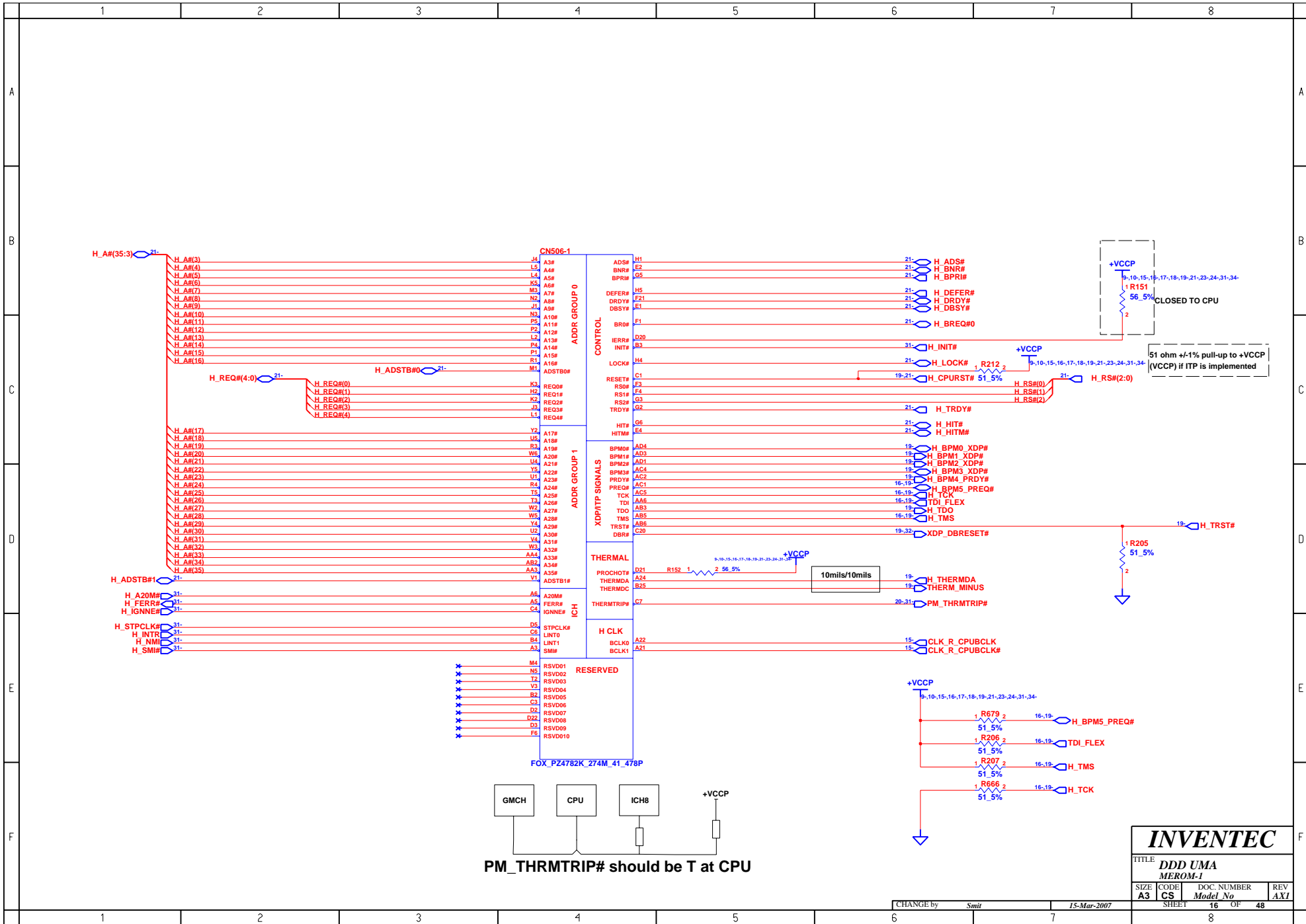
LAYOUT NOTES : THE R250 , R251 CLOSED TO U509

INVENTEC

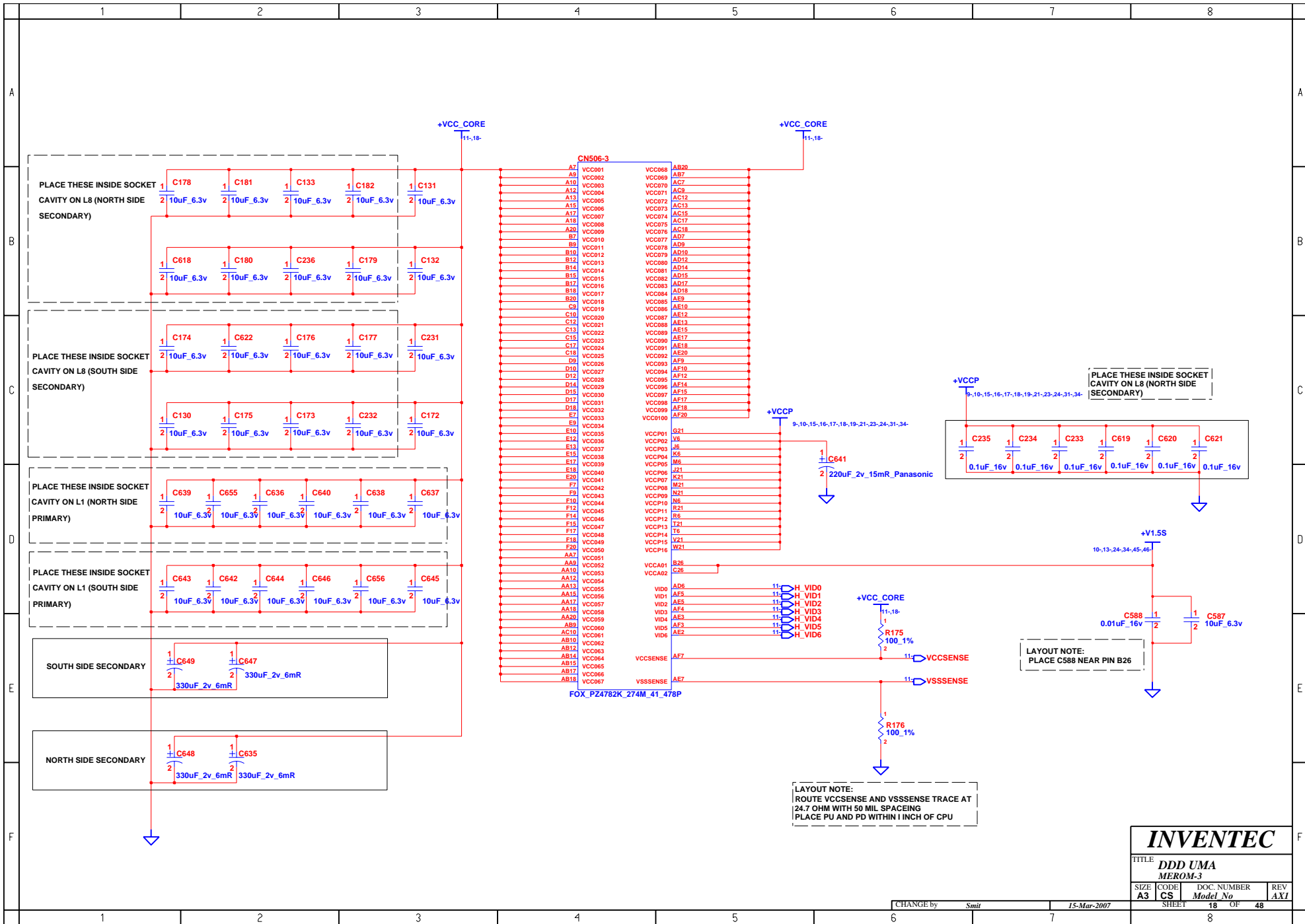
TITLE: **DDD UMA CLOCK GENERATOR**

SIZE	CODE	DOC. NUMBER	REV
A3	CS	Model No	AXI

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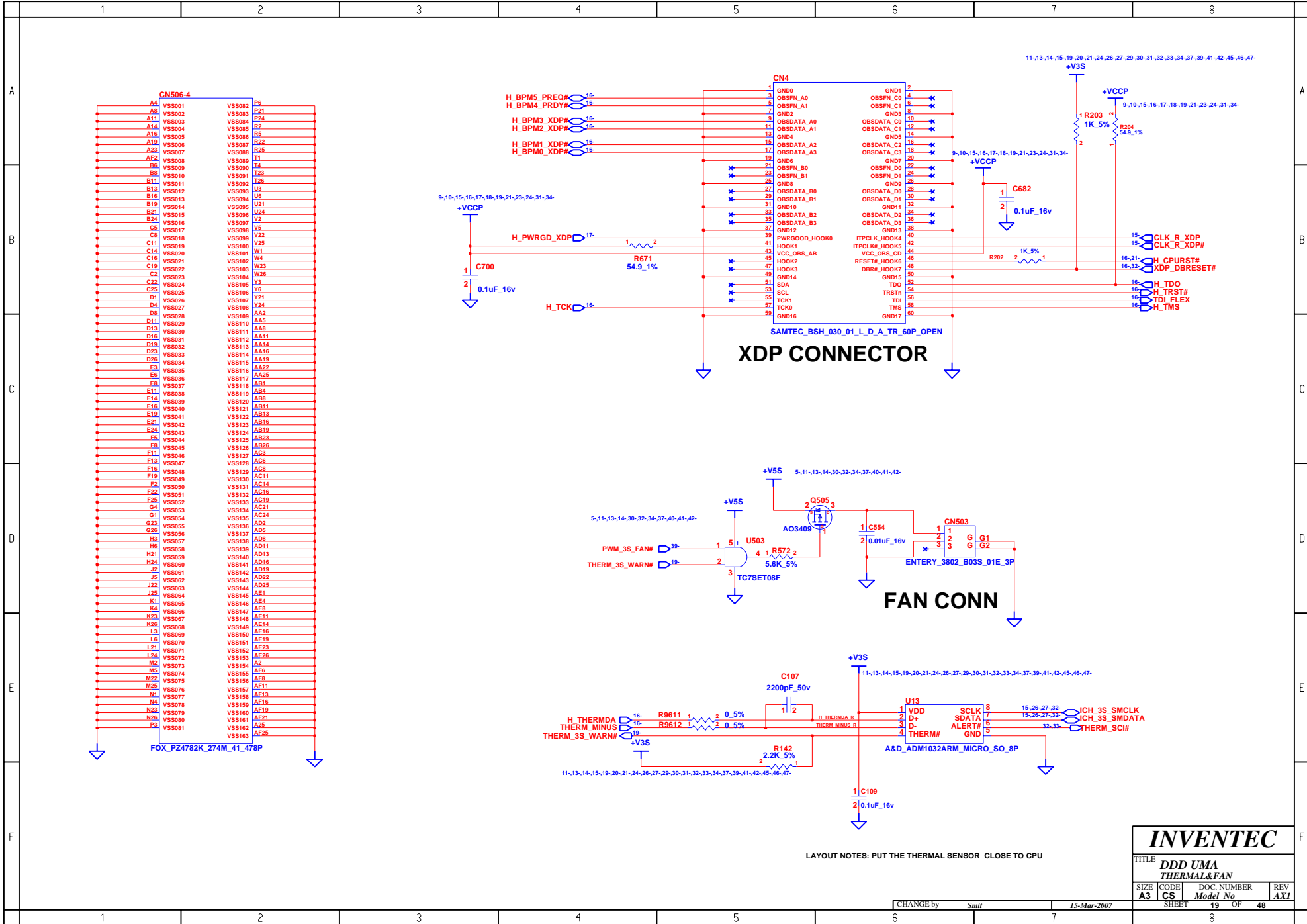
INVENTEC			
TITLE DDD UMA MEROM-1			
SIZE A3	CODE CS	DOC. NUMBER Model No	REV AXI
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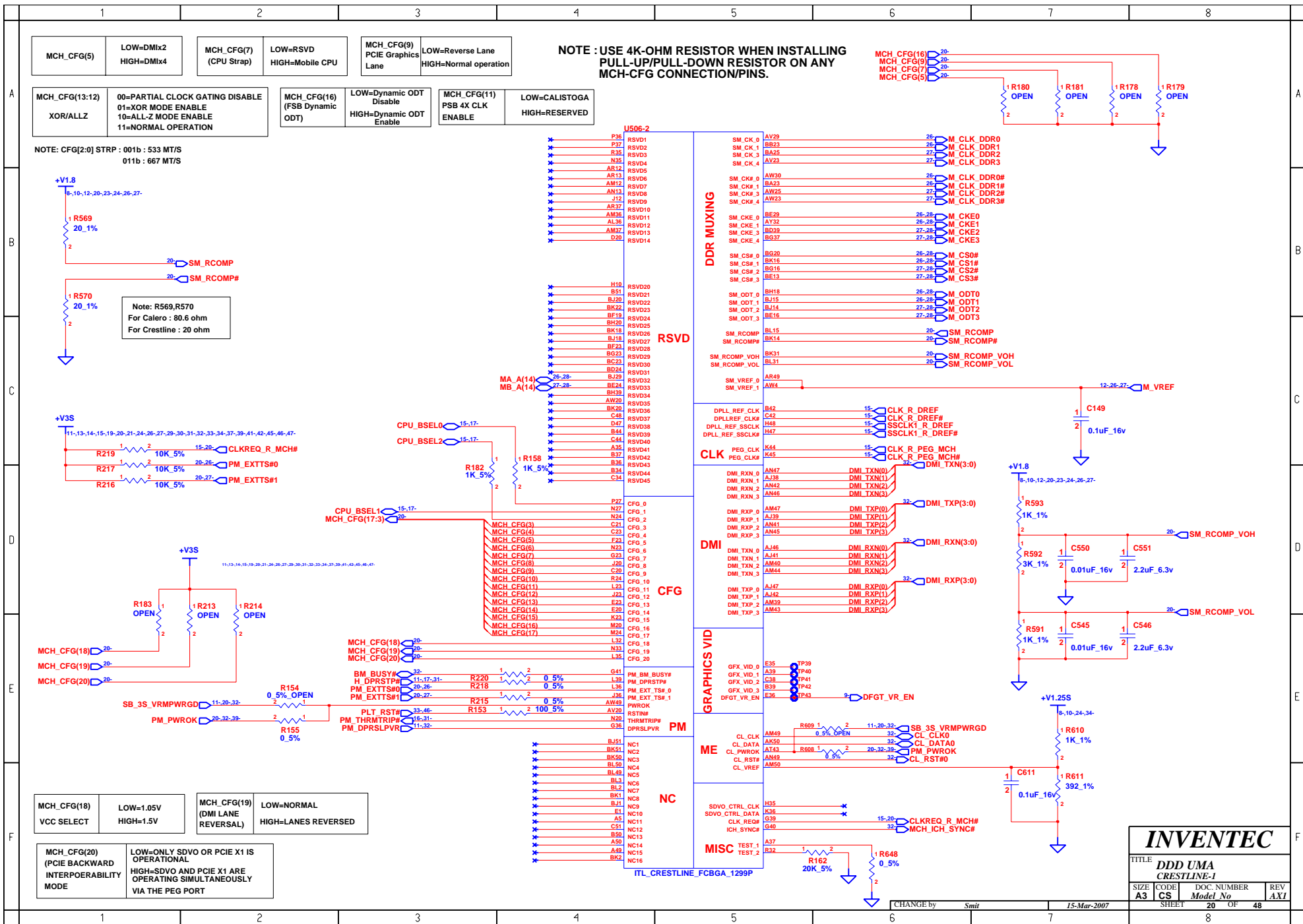
LAYOUT NOTE:
PLACE C588 NEAR PIN B26

LAYOUT NOTE:
ROUTE VCCSENSE AND VSSSENSE TRACE AT
24.7 OHM WITH 50 MIL SPACING
PLACE PU AND PD WITHIN 1 INCH OF CPU

INVENTEC			
TITLE DDD UMA MEROM-3			
SIZE A3	CODE CS	DOC. NUMBER Model No	REV AX1
CHANGE by Smit		15-Mar-2007	SHEET 18 OF 48

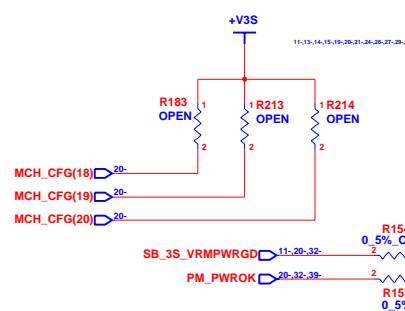
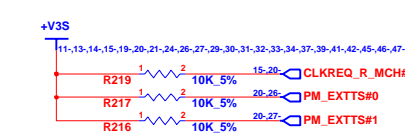
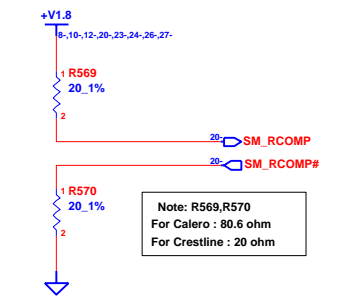


INVENTEC			
TITLE DDD UMA THERMAL&FAN			
SIZE A3	CODE CS	DOC NUMBER Model No	REV AXI
CHANGE by Smit		15-Mar-2007	SHEET 19 OF 48



MCH_CFG(5)	LOW=DMiX2 HIGH=DMiX4	MCH_CFG(7) (CPU Strap)	LOW=RSVD HIGH=Mobile CPU	MCH_CFG(9) PCIe Graphics Lane	LOW=Reverse Lane HIGH=Normal operation
MCH_CFG(13:12)	00=PARTIAL CLOCK GATING DISABLE 01=XOR MODE ENABLE 10=ALL-Z MODE ENABLE 11=NORMAL OPERATION	MCH_CFG(16) (FSB Dynamic ODT)	LOW=Dynamic ODT Disable HIGH=Dynamic ODT Enable	MCH_CFG(11) PSB 4X CLK ENABLE	LOW=CALISTOGA HIGH=RESERVED

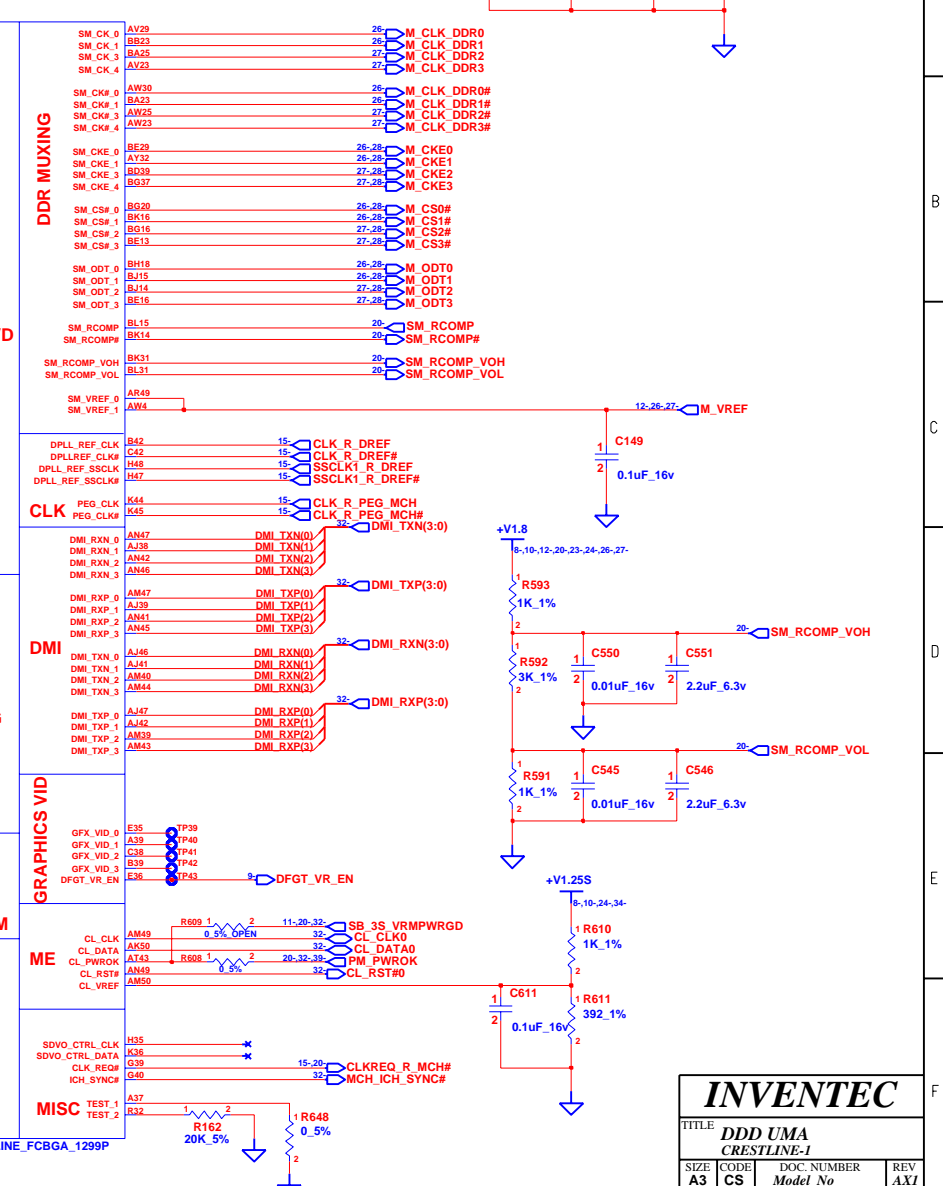
NOTE: CFG[2:0] STRP : 001b : 533 MT/S
011b : 667 MT/S

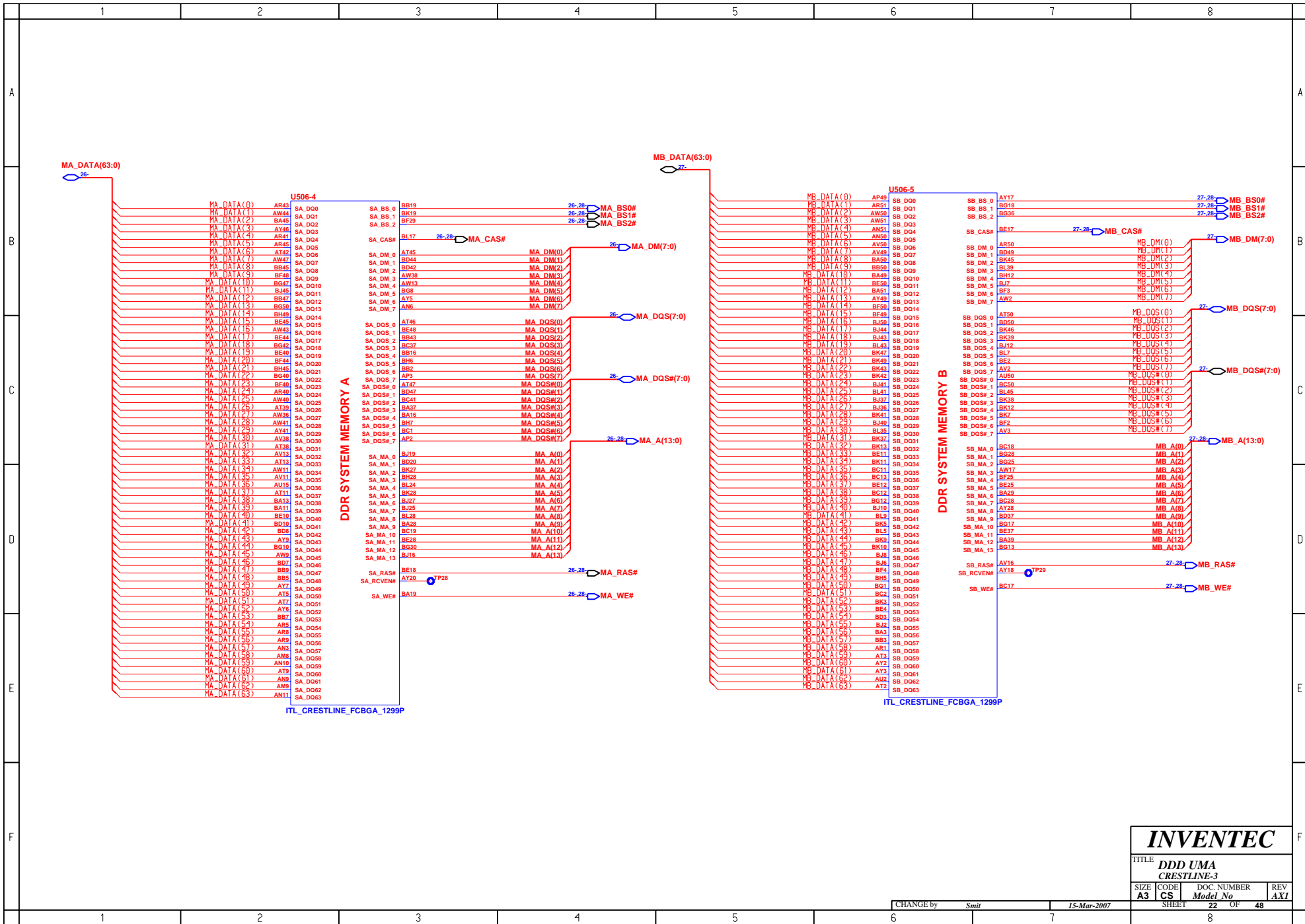


MCH_CFG(18)	LOW=1.05V HIGH=1.5V	MCH_CFG(19) (DMI LANE REVERSAL)	LOW=NORMAL HIGH=LANES REVERSED
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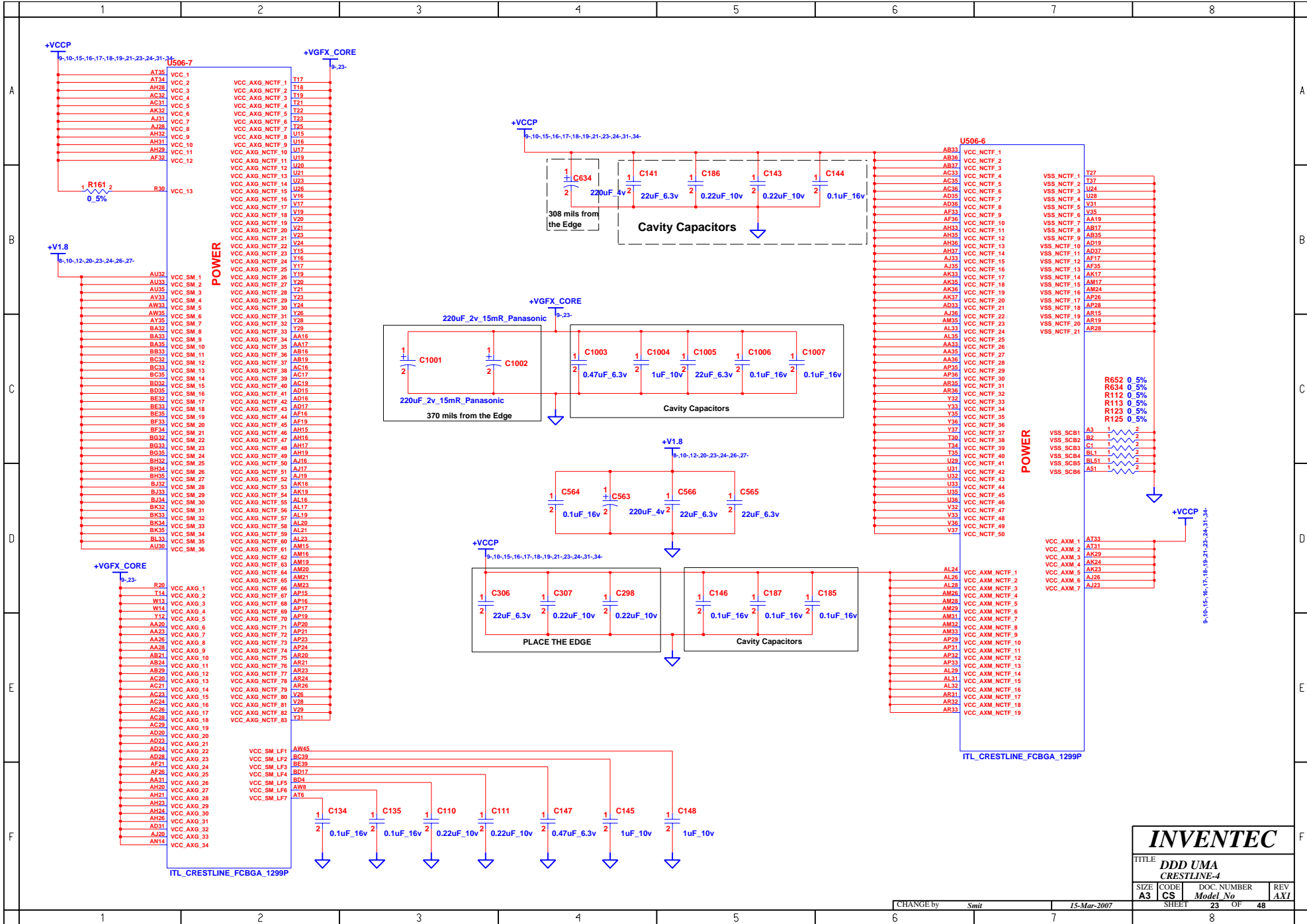
MCH_CFG(20) (PCIe BACKWARD INTEROPERABILITY MODE)	LOW=ONLY SDVO OR PCIe X1 IS OPERATIONAL HIGH=SDVO AND PCIe X1 ARE OPERATING SIMULTANEOUSLY VIA THE PEG PORT
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- P36 RSV1D1
- P37 RSV2D
- R35 RSV3D
- N35 RSV4D
- AR12 RSV5D
- AR13 RSV6D
- AM12 RSV7D
- AN13 RSV8D
- J12 RSV9D
- AR37 RSV10D
- AM36 RSV11D
- AL36 RSV12D
- AM37 RSV13D
- RSV14D
- D20 RSV15D
- H10 RSV20D
- B51 RSV21D
- BJ20 RSV22D
- BK32 RSV23D
- BE18 RSV24D
- BH20 RSV25D
- BK18 RSV26D
- BJ18 RSV27D
- BE23 RSV28D
- BQ23 RSV29D
- BC23 RSV30D
- BD34 RSV31D
- BJ29 RSV32D
- BE24 RSV33D
- BH39 RSV34D
- AW20 RSV35D
- BK20 RSV36D
- AW20 RSV37D
- AW20 RSV38D
- AW20 RSV39D
- AW20 RSV40D
- AW20 RSV41D
- AW20 RSV42D
- AW20 RSV43D
- AW20 RSV44D
- AW20 RSV45D
- P27 CFG_0
- N27 CFG_1
- N24 CFG_2
- C21 CFG_3
- C23 CFG_4
- F24 CFG_5
- MCH_CFG(5) N23 CFG_6
- MCH_CFG(6) N23 CFG_7
- MCH_CFG(7) J23 CFG_8
- MCH_CFG(8) J23 CFG_9
- MCH_CFG(9) E24 CFG_10
- MCH_CFG(10) E24 CFG_11
- MCH_CFG(11) J23 CFG_12
- MCH_CFG(12) E24 CFG_13
- MCH_CFG(13) E24 CFG_14
- MCH_CFG(14) E24 CFG_15
- MCH_CFG(15) K23 CFG_16
- MCH_CFG(16) M20 CFG_17
- M24 CFG_18
- L32 CFG_19
- N33 CFG_20
- L35 CFG_21
- G41 PM_BM_BUSY#
- L39 PM DPRSTP#
- L36 PM_EXTT#0
- J36 PM_EXTT#1
- AW49 PMWROK
- AV20 RSTIN#
- N40 THRMTRIP#
- G36 DPRSLPVR
- BJ51 NC1
- BK51 NC2
- BK50 NC3
- BL50 NC4
- BL49 NC5
- BL2 NCF
- BL2 NCF
- BK1 NC6
- BK1 NC6
- BJ1 NC9
- AL NC10
- AL NC11
- CS1 NC12
- B50 NC13
- A50 NC14
- A49 NC15
- BK2 NC16



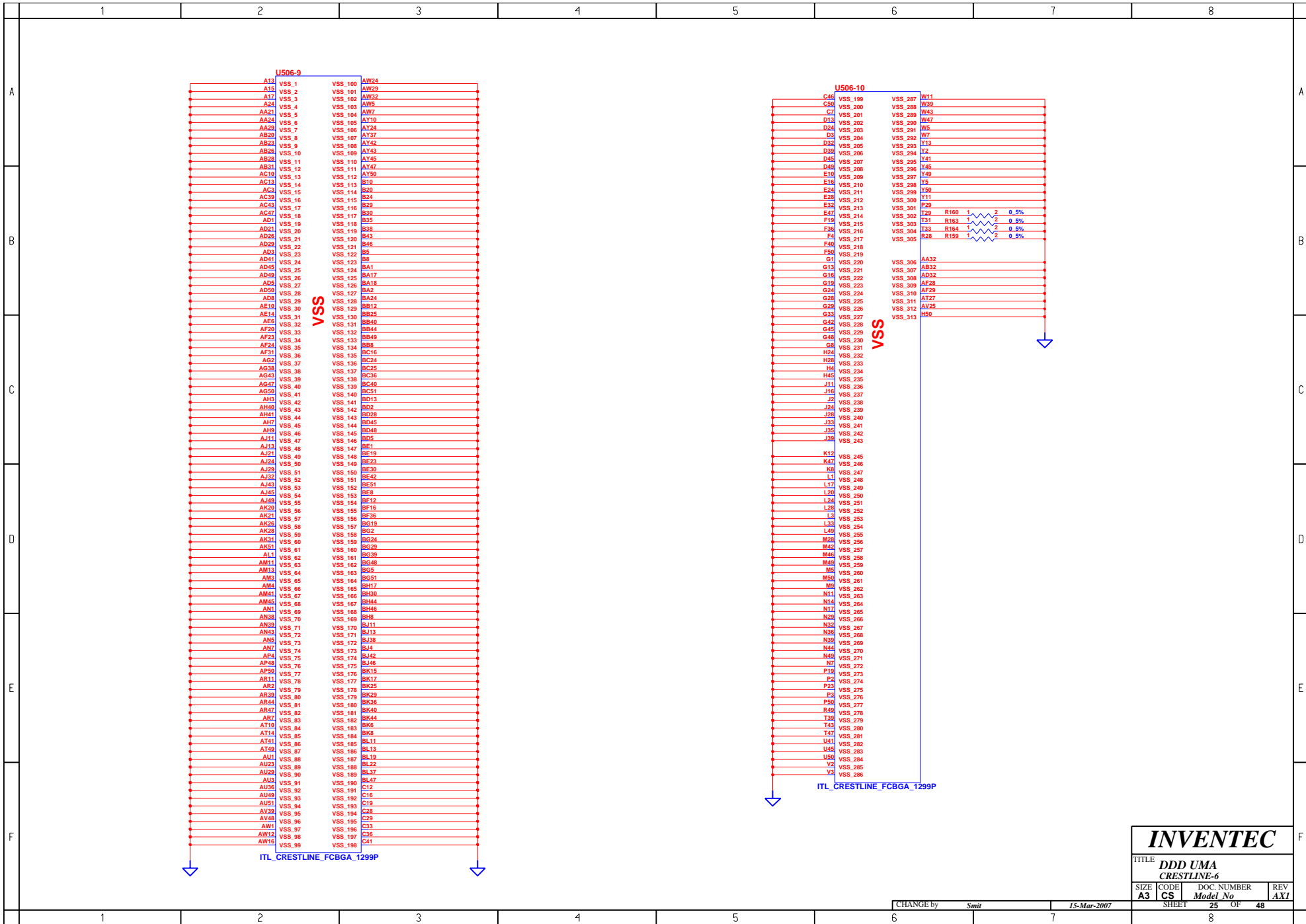


INVENTEC			
TITLE DDD UMA CRESTLINE-3			
SIZE A3	CODE CS	DOC. NUMBER Model No	REV AX1
CHANGE by Smit		15-Mar-2007	SHEET 22 OF 48



INVENTEC			
TITLE DDD UMA CRESTLINE-4			
SIZE A3	CODE CS	DOC. NUMBER Model No	REV AXI
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CHANGE by Smit 15-Mar-2007



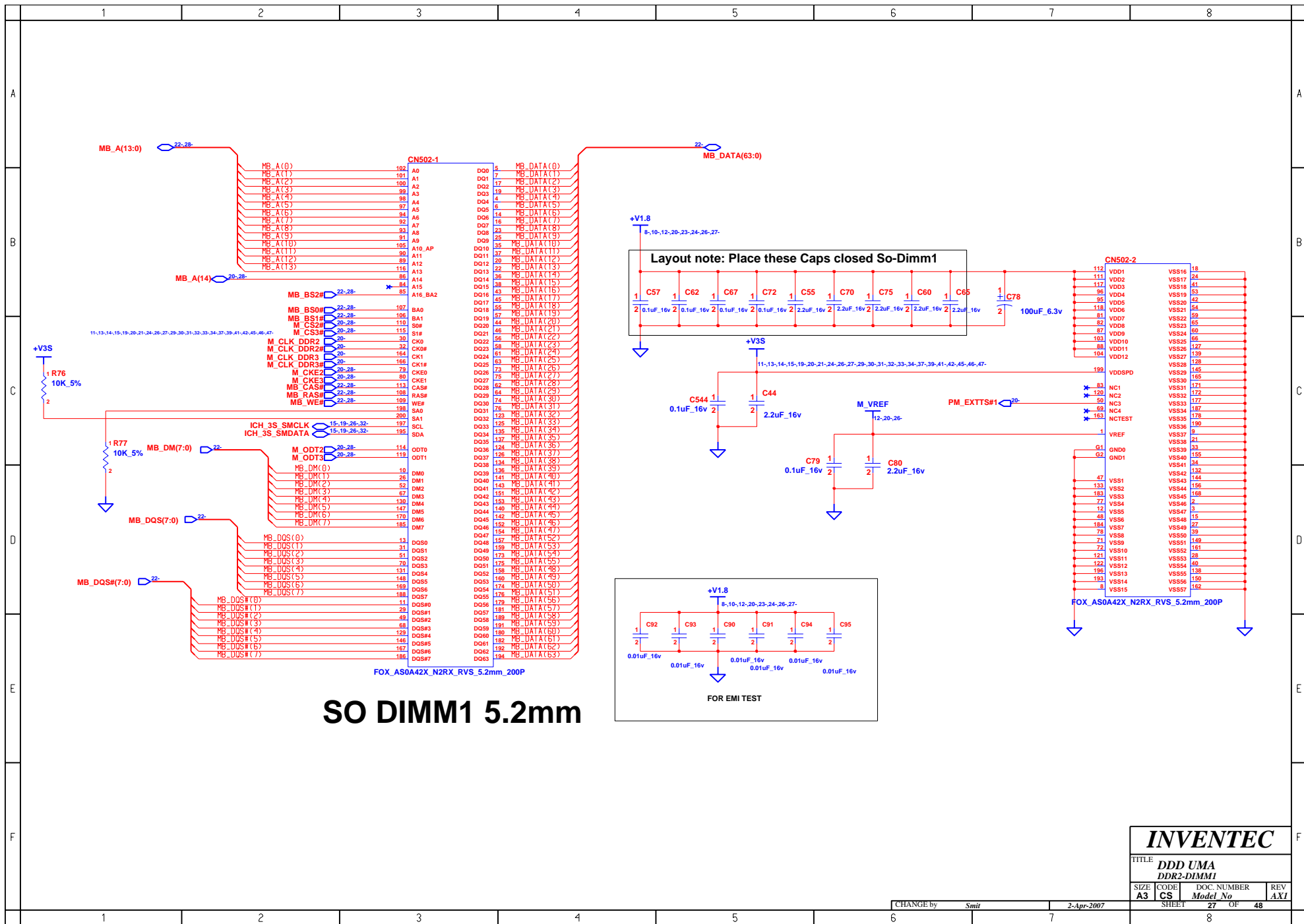
INVENTEC

TITLE
DDD UMA
CRESTLINE-6

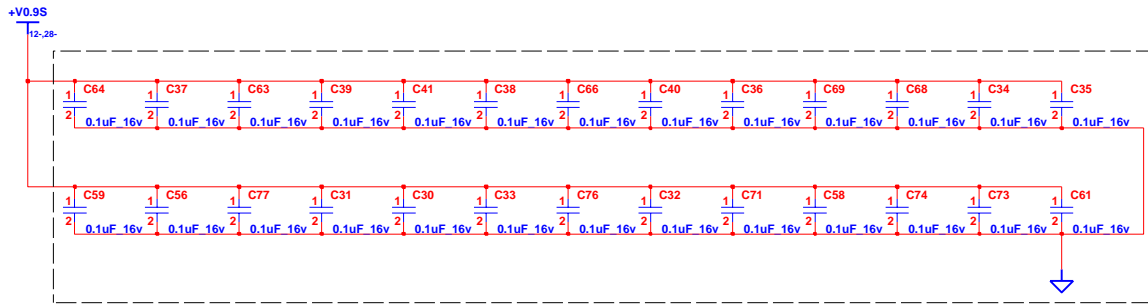
SIZE	CODE	DOC. NUMBER	REV
A3	CS	Model No	AXI

CHANGE by *Smit* 15-Mar-2007

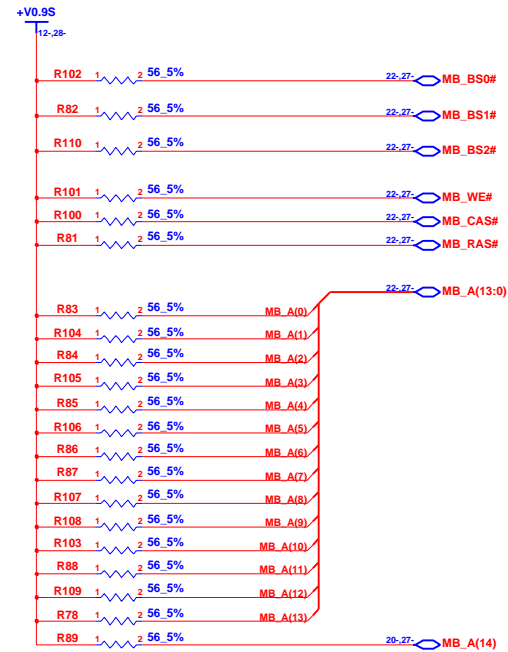
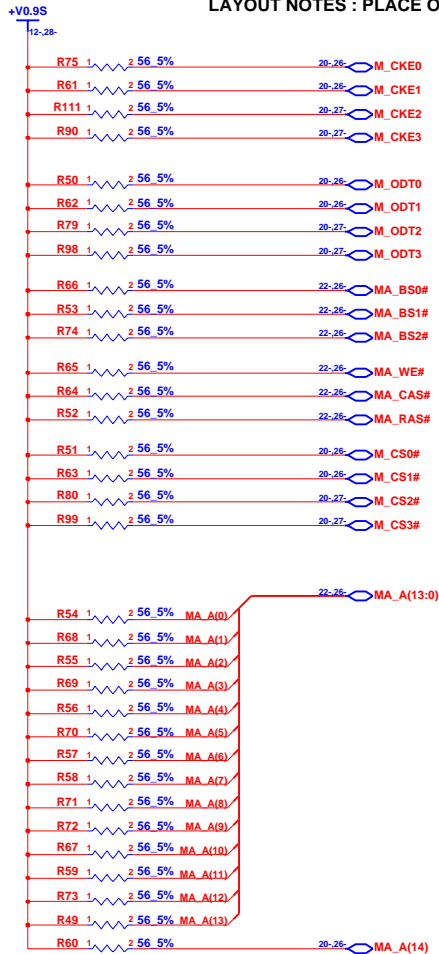
SHEET 25 OF 48



INVENTEC			
TITLE DDD UMA DDR2-DIMM1			
SIZE A3	CODE CS	DOC. NUMBER Model No	REV AX1
CHANGE by Smit		2-Apr-2007	SHEET 27 OF 48



LAYOUT NOTES : PLACE ONE CAP CLOSE TO EVERY 2 PULL UP RESISTOR TERMINATED TO +V0.9S

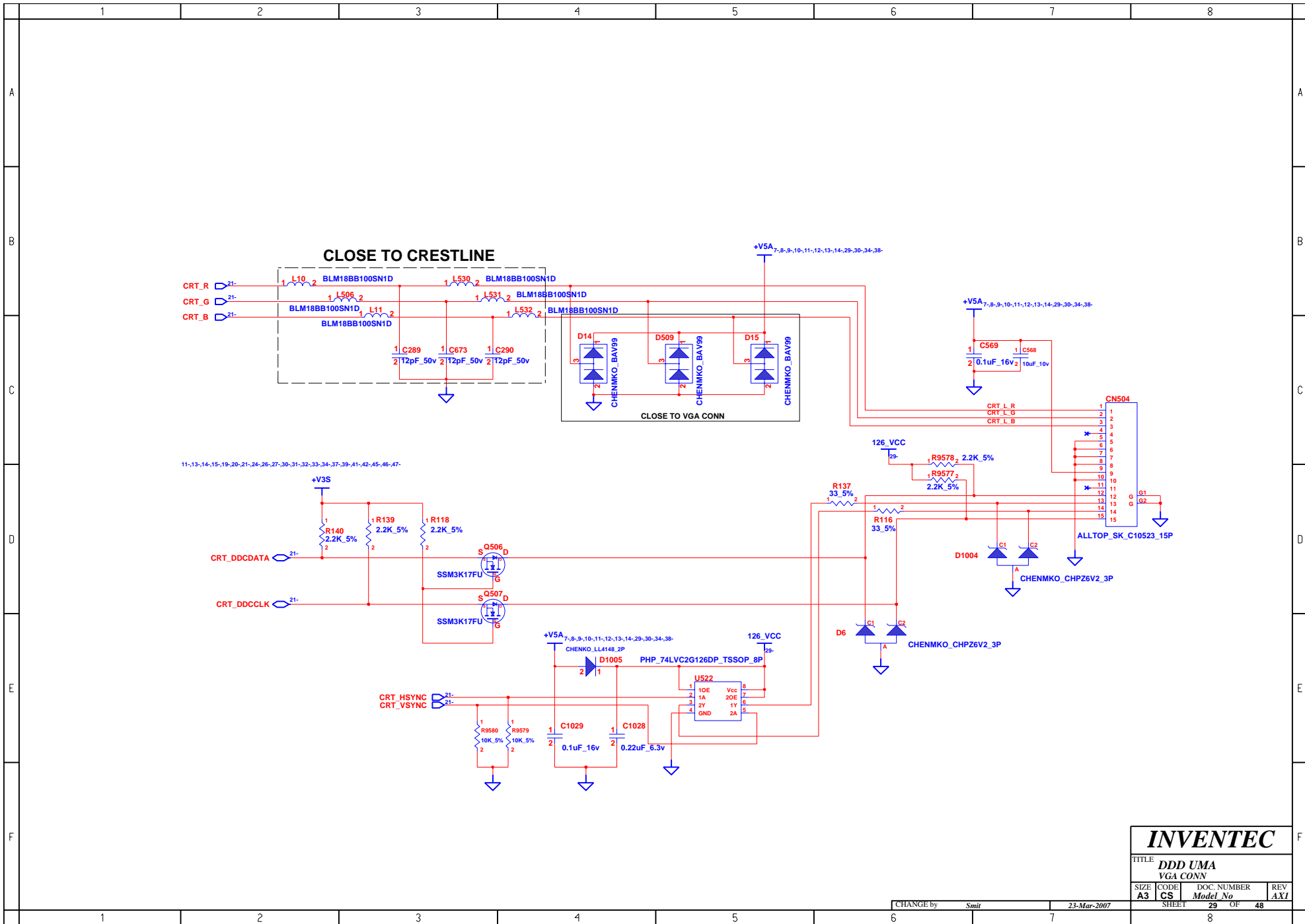


INVENTEC

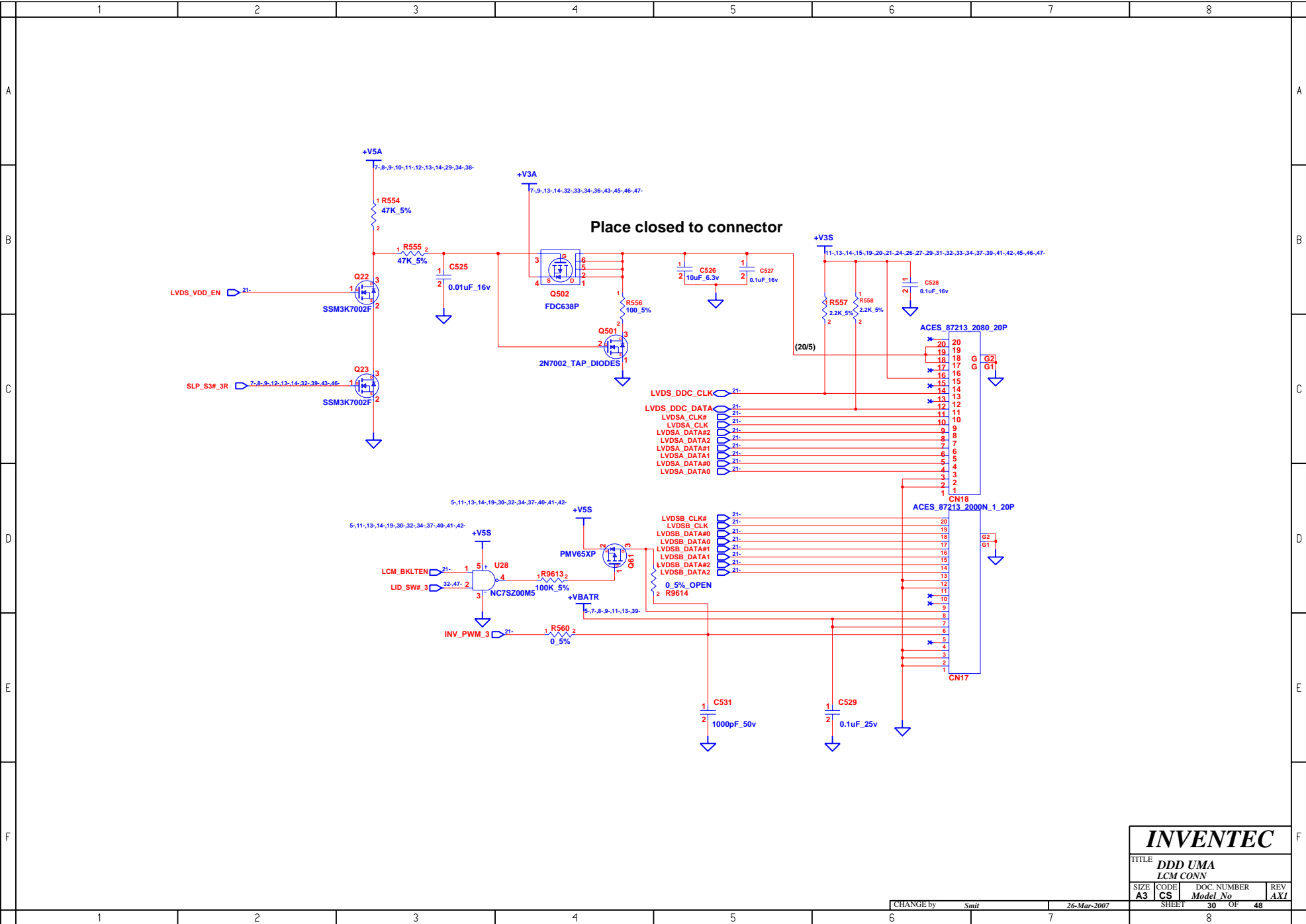
TITLE			
DDD UMA			
DDR2-DAMPING			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	Model No	AXI

CHANGE by *Smit* 27-Sep-2003

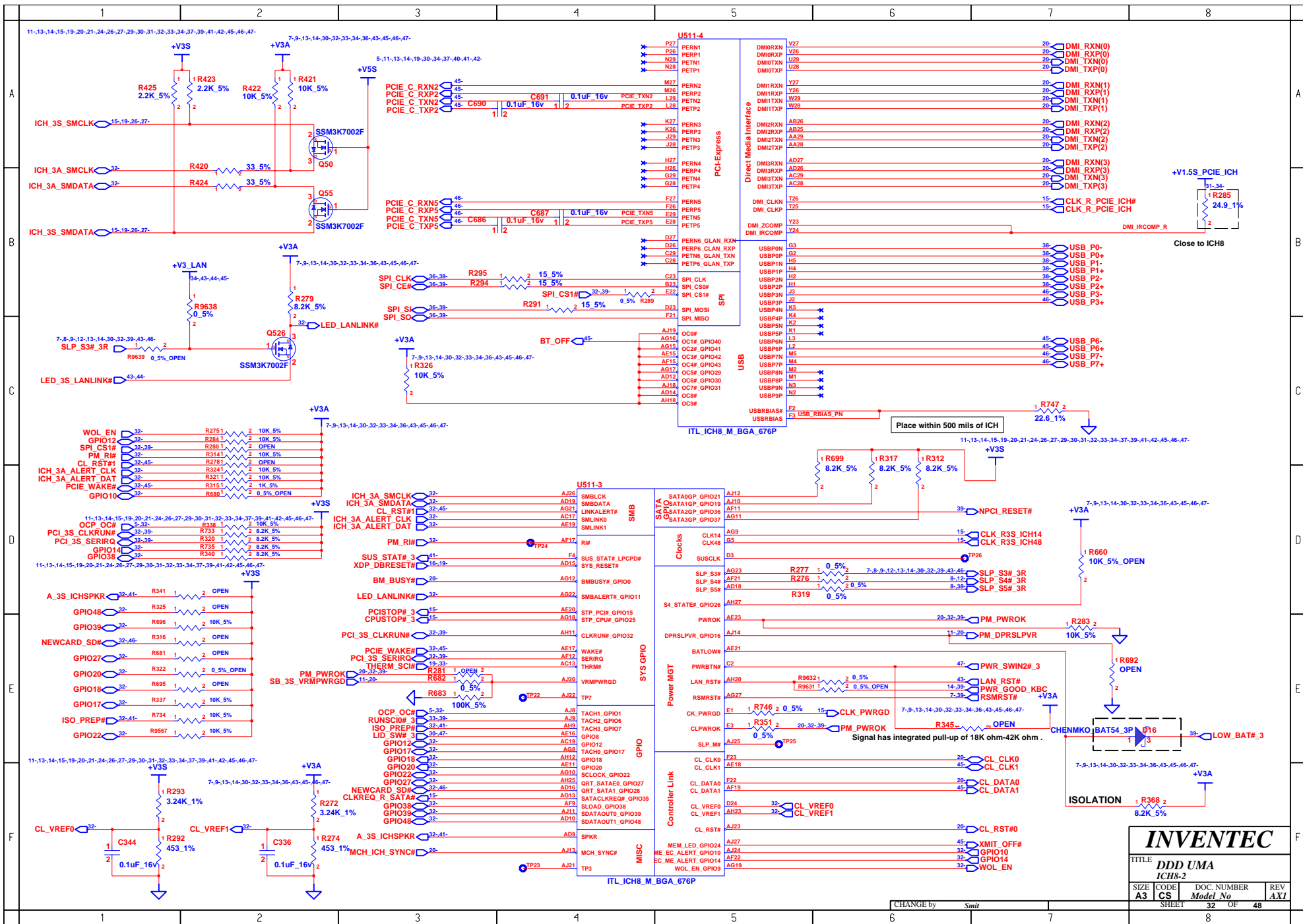
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INVENTEC			
TITLE DDD UMA VGA CONN			
SIZE A3	CODE CS	DOC. NUMBER <i>Model No</i>	REV AXI
CHANGE by <i>Smit</i>		23-Mar-2007	SHEET 29 OF 48



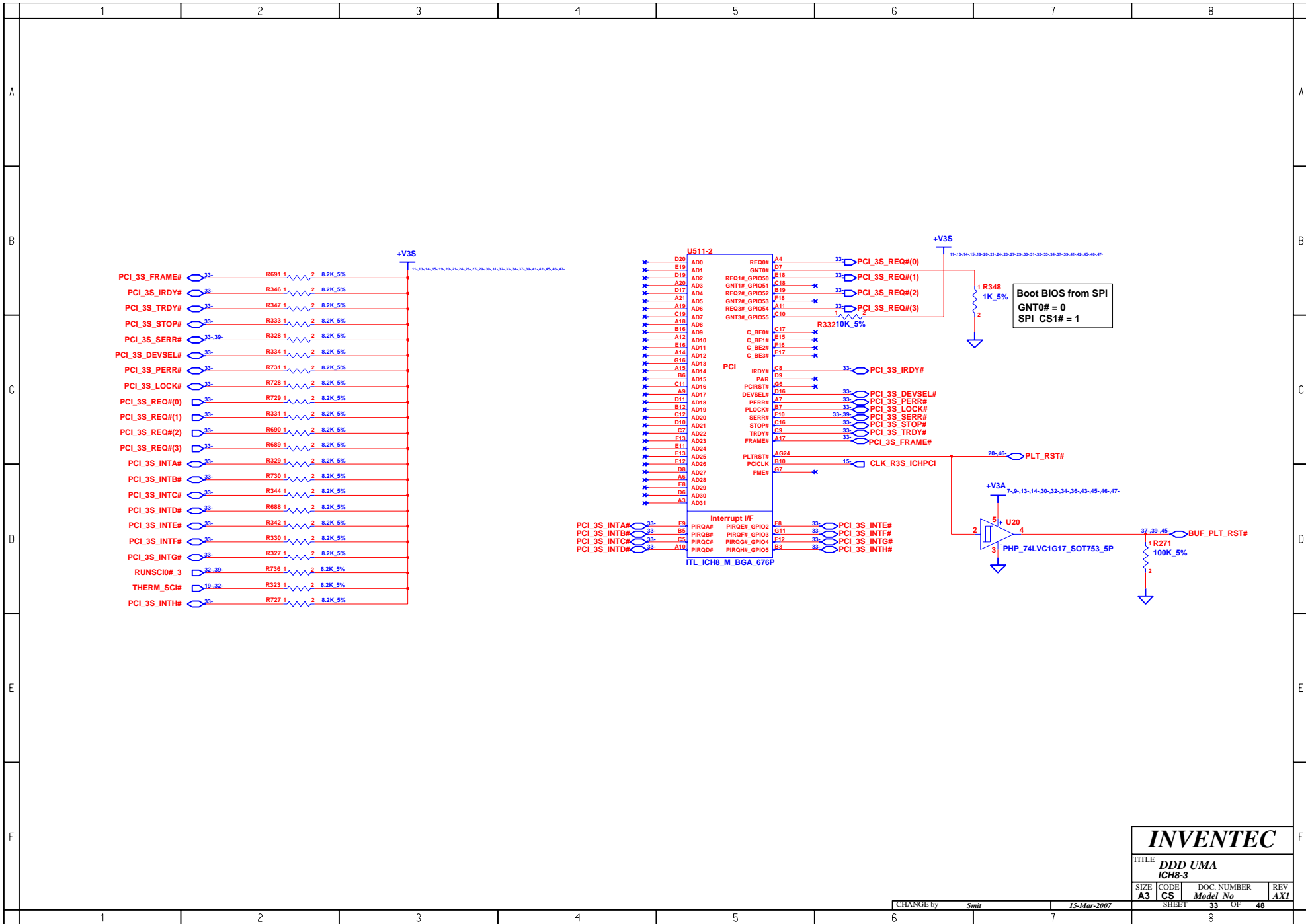
INVENTEC			
TITLE DDD UMA LCM CONN			
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CHANGE by <i>Smit</i>		26-Mar-2007	SHEET 30 OF 48



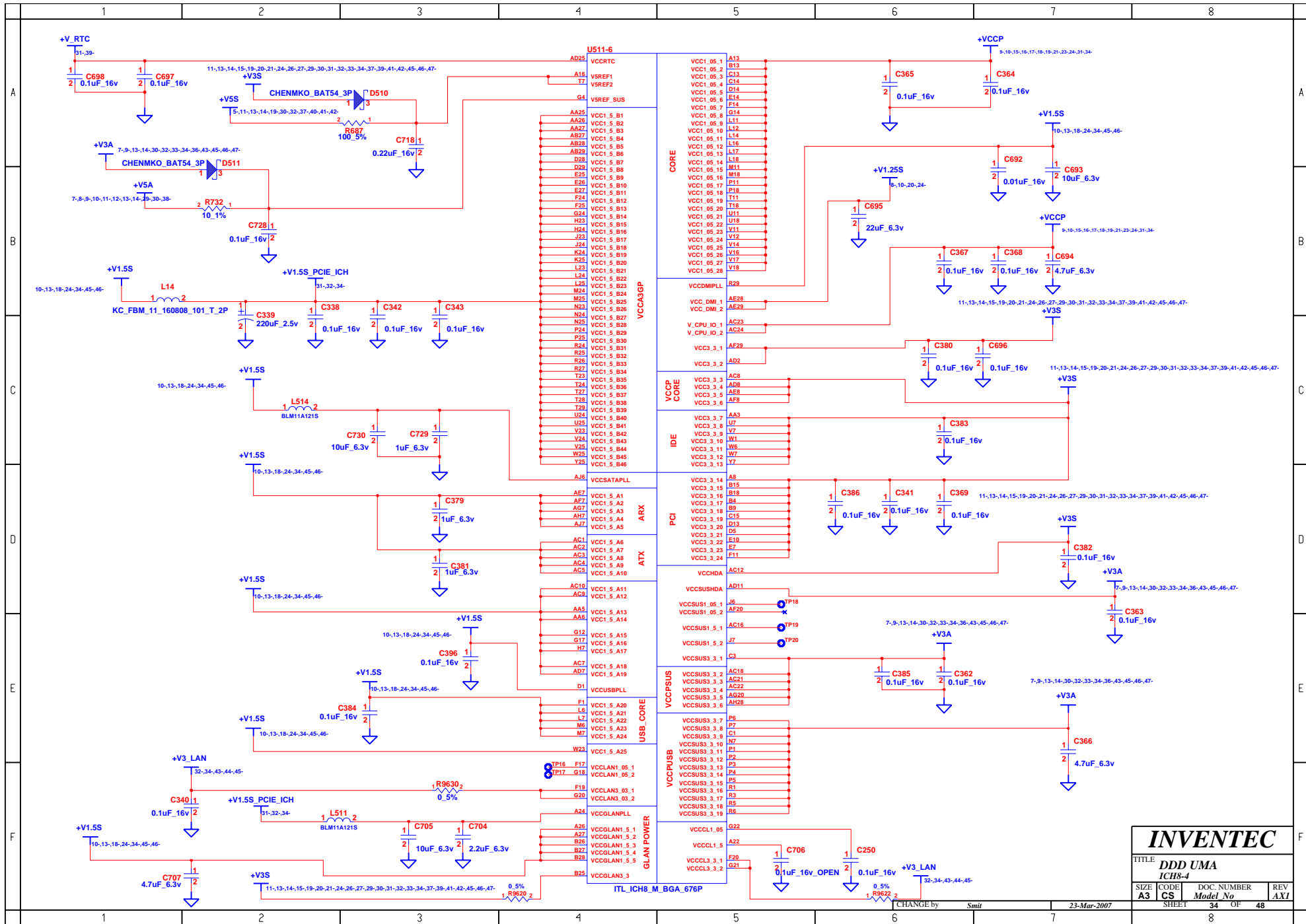
INVENTEC

TITLE			
DDD UMA			
ICH8-2			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	Model No	AXI
SHEET		32	OF 48

CHANGE by *Smit*



INVENTEC			
TITLE DDD UMA ICH8-3			
SIZE A3	CODE CS	DOC. NUMBER <i>Model No</i>	REV AXI
CHANGE by <i>Smit</i>		15-Mar-2007	
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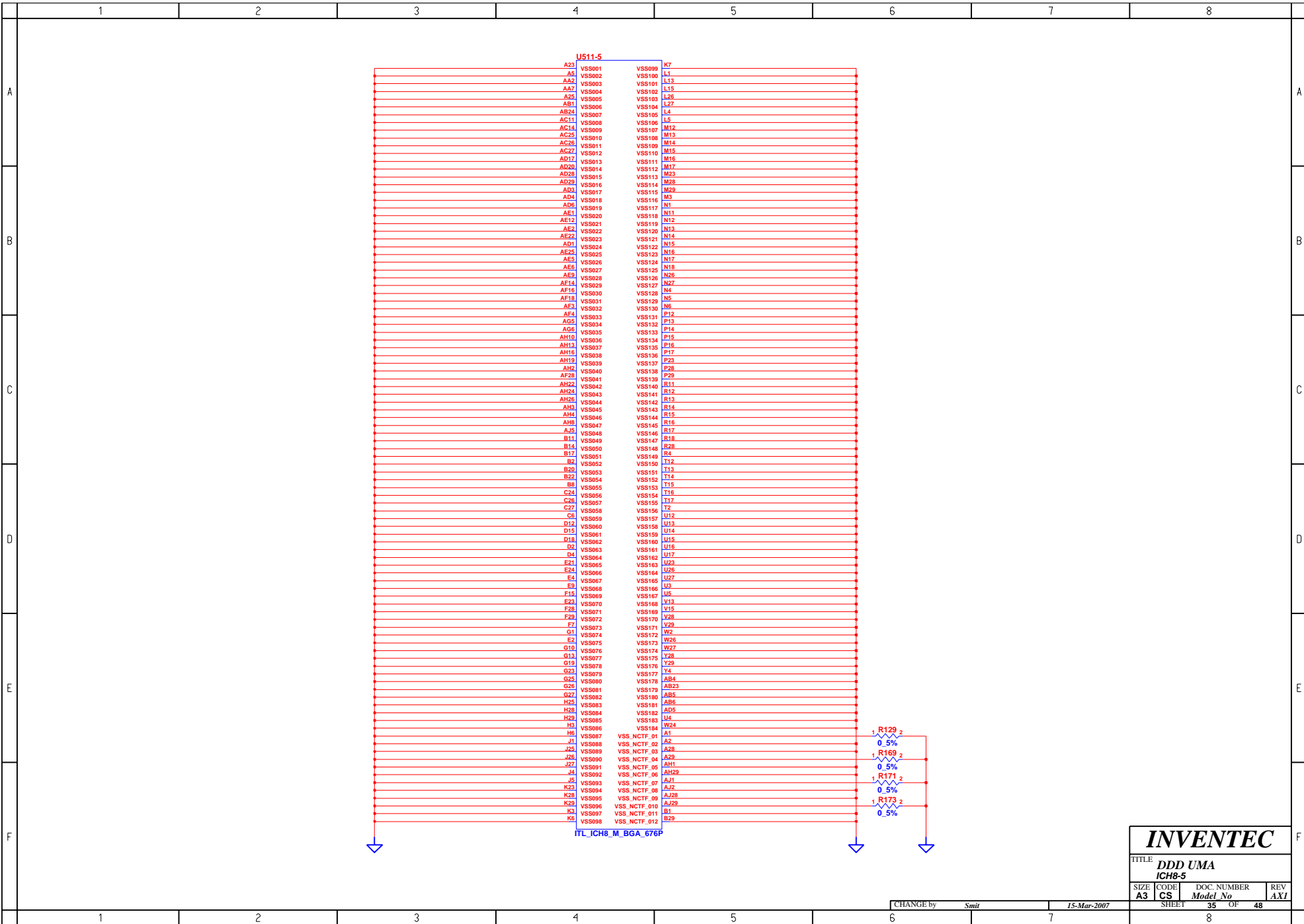
INVENTEC

TITLE: **DDD UMA**
ICH8-4

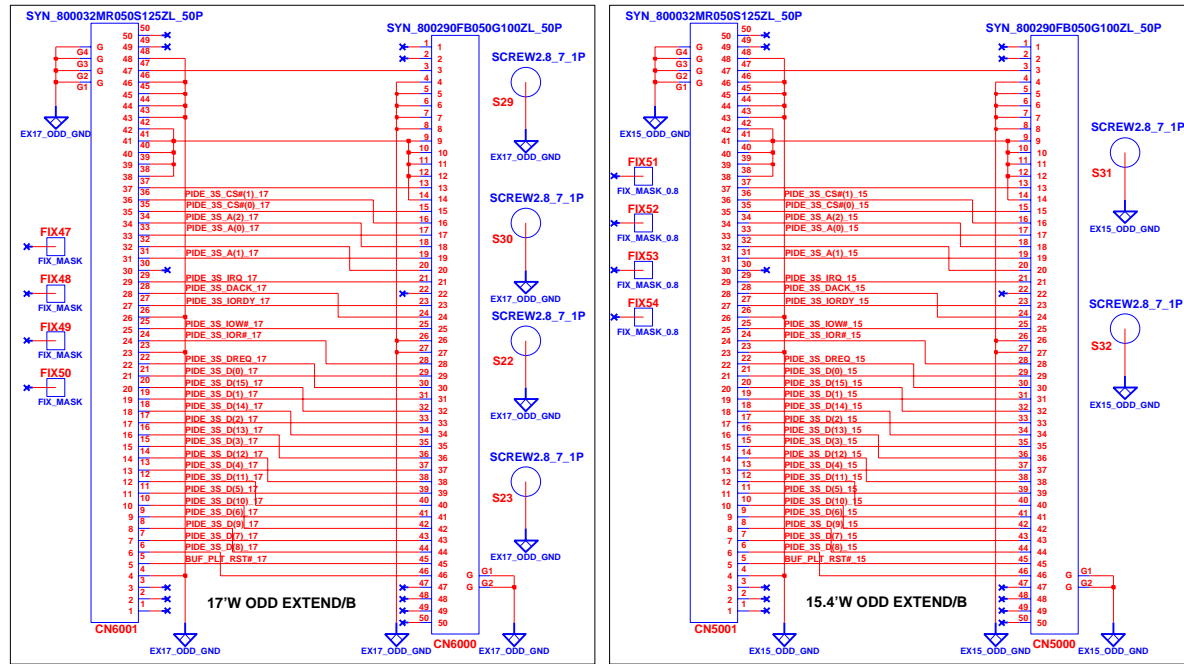
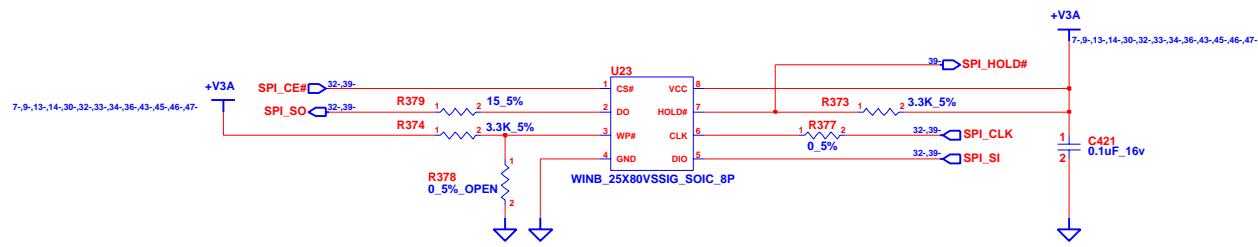
SIZE	CODE	DOC. NUMBER	REV
A3	CS	Model No	AXI

CHANGE by *Smit* 23-Mar-2007

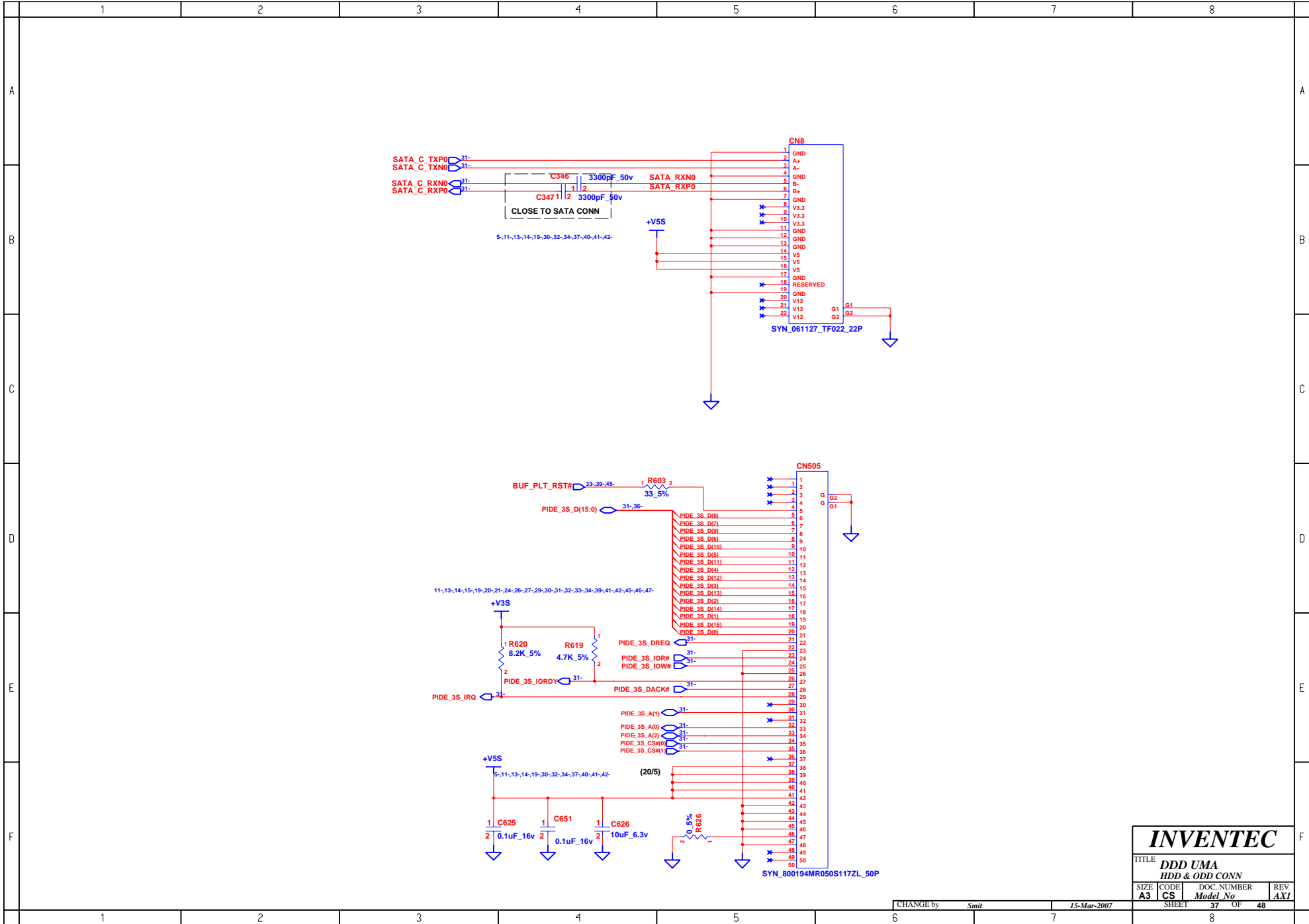
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INVENTEC			
TITLE DDD UMA ICH8-5			
SIZE A3	CODE CS	DOC. NUMBER <i>Model No</i>	REV <i>AXI</i>
CHANGE by <i>Smit</i>		15-Mar-2007	
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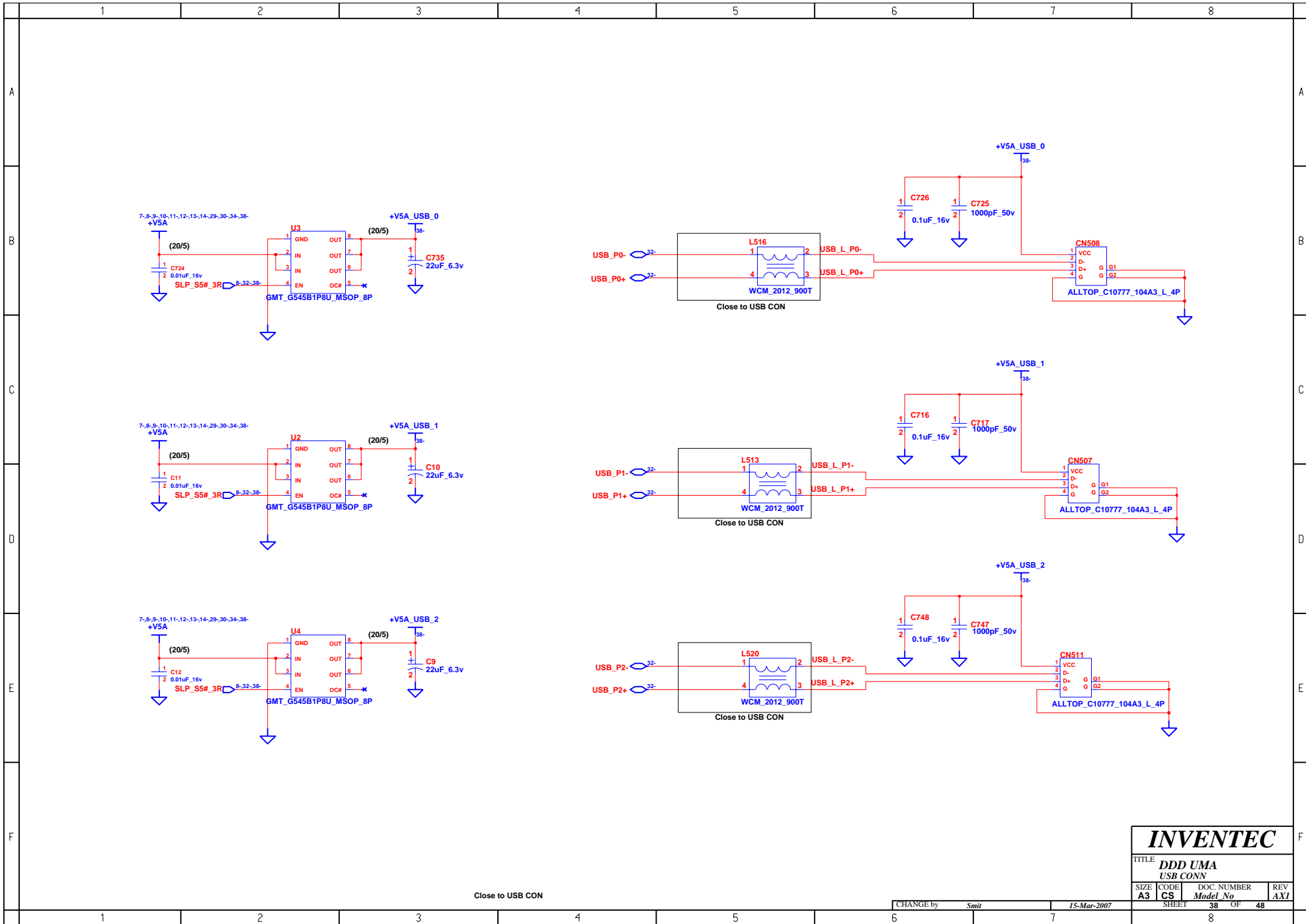


INVENTEC			
TITLE DDD UMA			
SYSTEM BIOS&ODD EXT/B			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	Model No	AX1
CHANGE by		Smit	15-Mar-2007
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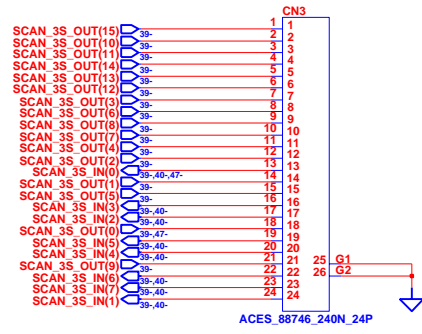
INVENTEC			
TITLE DDD UMA HDD & ODD CONN			
SIZE A3	CODE CS	DOC. NUMBER <i>Model No</i>	REV AX1
SHEET		37	OF 48

CHANGE by *Smit* 15-Mar-2007

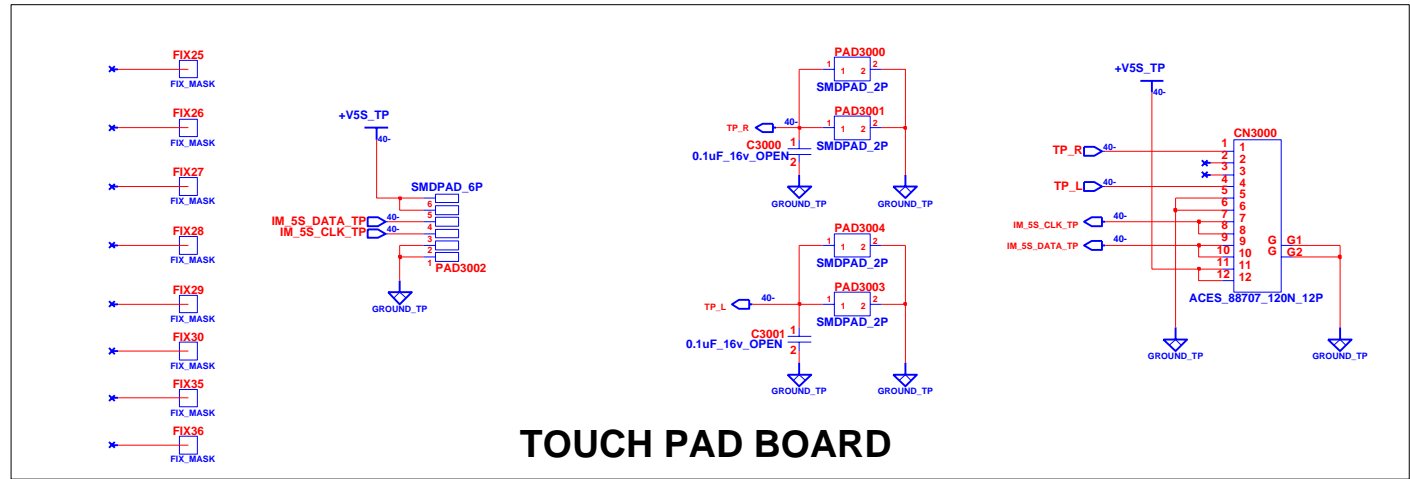
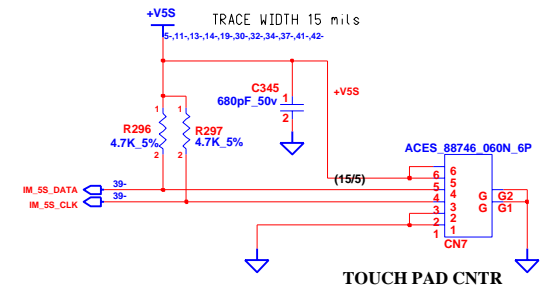
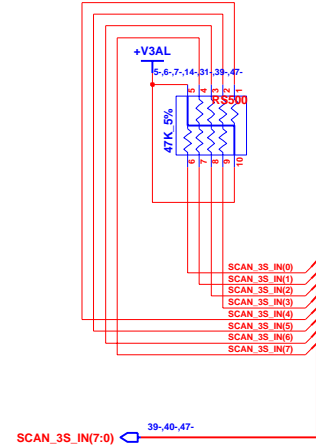


Close to USB CON

INVENTEC			
TITLE DDD UMA USB CONN			
SIZE A3	CODE CS	DOC. NUMBER <i>Model No</i>	REV AXI
CHANGE by <i>Smit</i>		15-Mar-2007	
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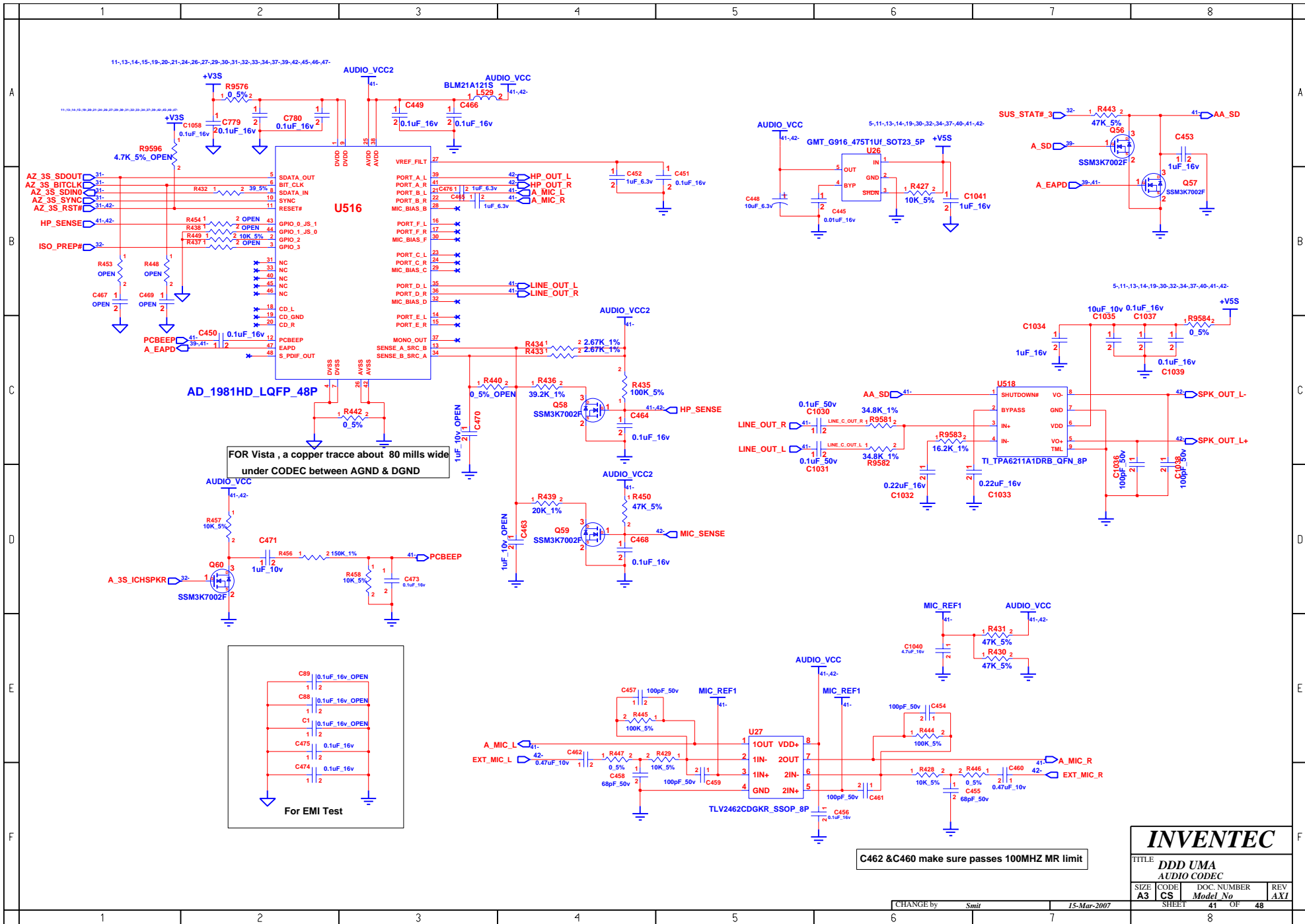


KEYBOARD CONN

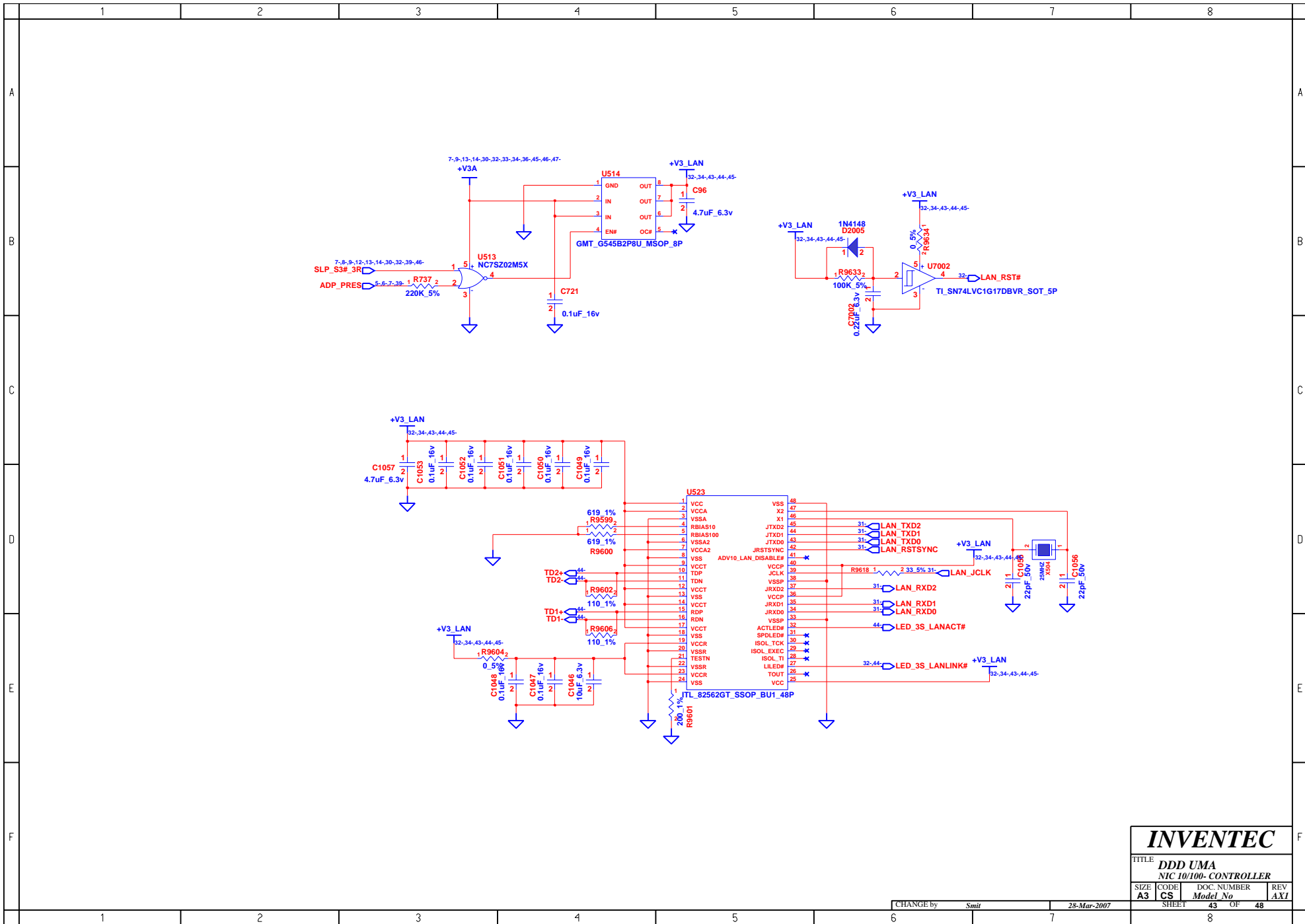


TOUCH PAD BOARD

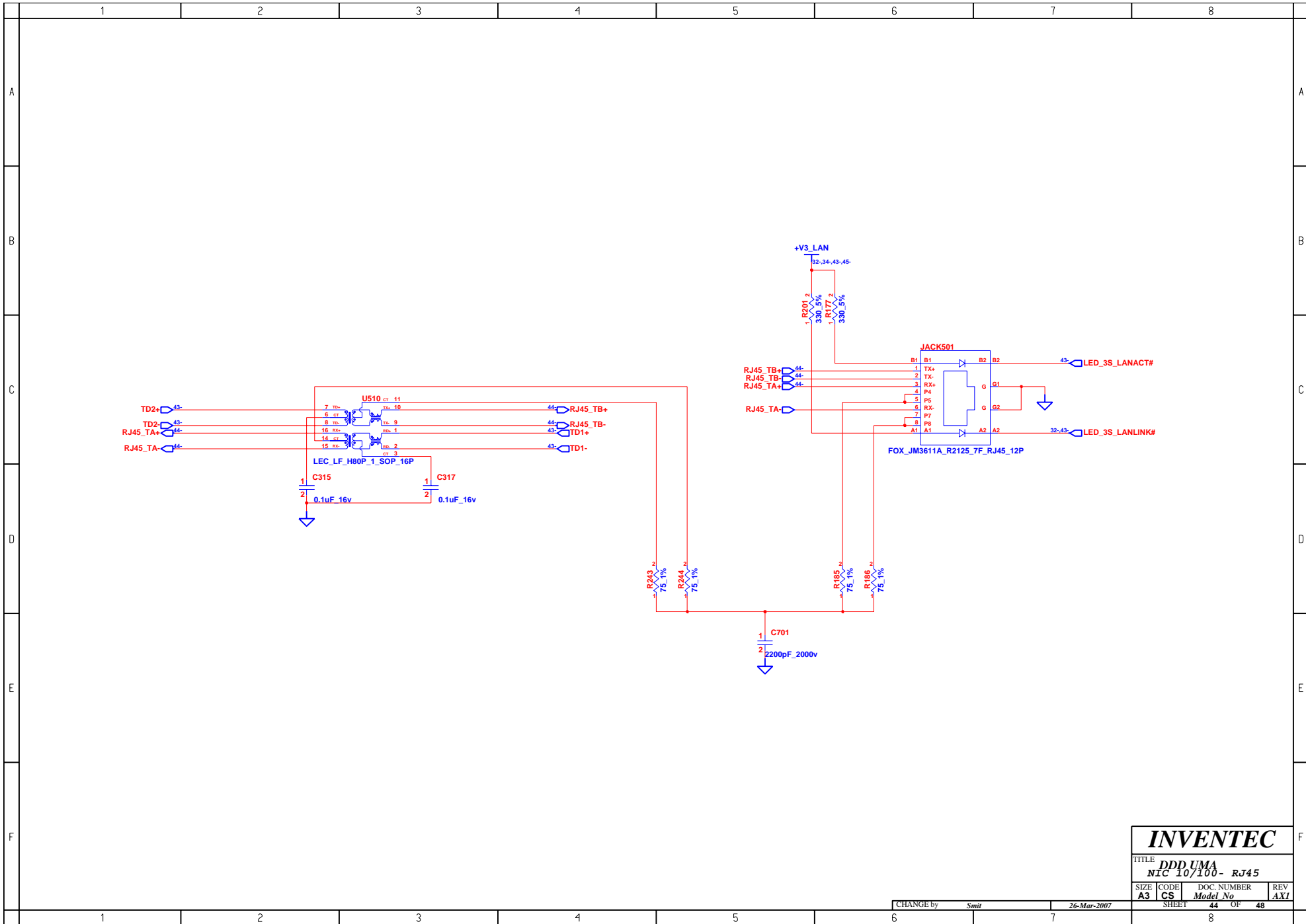
INVENTEC			
TITLE DDD UMA KB & TP CONN			
SIZE A3	CODE CS	DOC. NUMBER <i>Model No</i>	REV AXI
CHANGE by <i>Smit</i>		15-Mar-2007	
SHEET 40		OF 48	



INVENTEC			
TITLE DDD UMA AUDIO CODEC			
SIZE A3	CODE CS	DOC. NUMBER Model No	REV AX1
CHANGE by Smit		15-Mar-2007	
SHEET 41		OF 48	



INVENTEC			
TITLE DDD UMA NIC 10/100-CONTROLLER			
SIZE A3	CODE CS	DOC. NUMBER Model No	REV AXI
CHANGE by Smit		28-Mar-2007	
SHEET 43		OF 48	

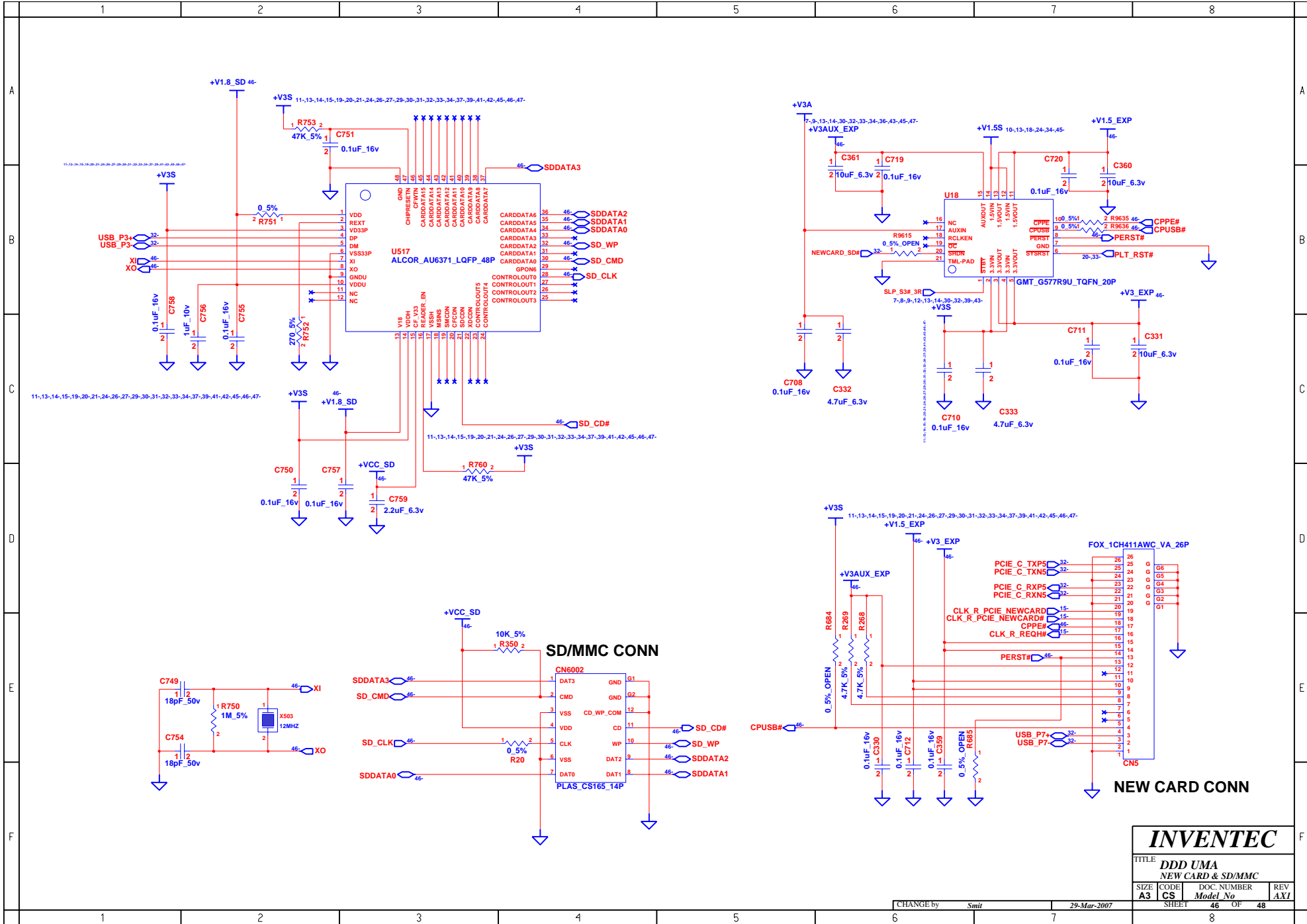


INVENTEC

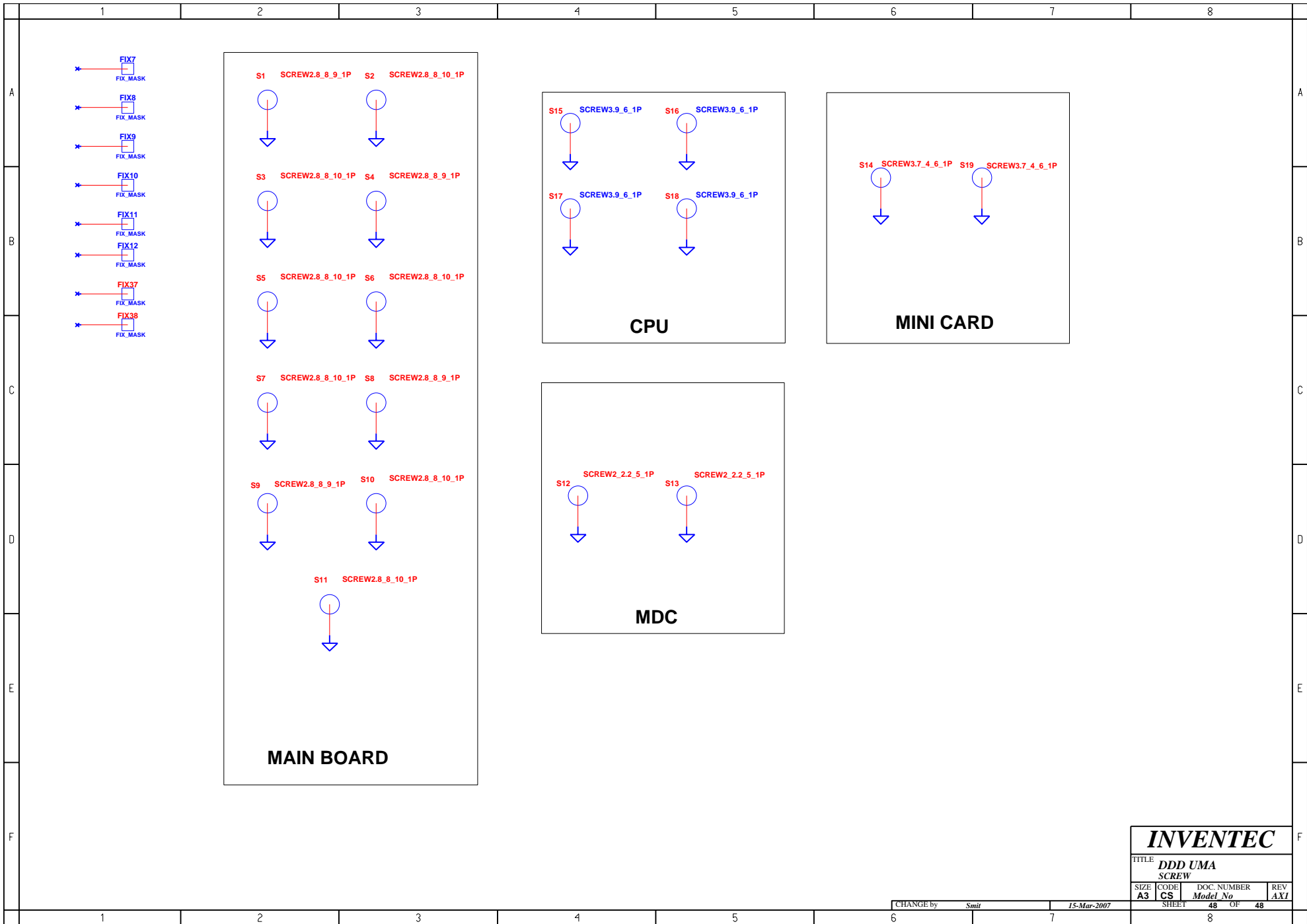
TITLE
DDD UMA
NIC 10/100 - RJ45

SIZE A3	CODE CS	DOC. NUMBER <i>Model No</i>	REV AX1
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CHANGE by *Smit* 26-Mar-2007 SHEET 44 OF 48



INVENTEC			
TITLE DDD UMA NEW CARD & SD/MMC			
SIZE A3	CODE CS	DOC. NUMBER Model No	REV AXI
CHANGE by Smit		29-Mar-2007	
SHEET 46		OF 48	



INVENTEC

TITLE			
DDD UMA			
SCREW			
SIZE	CODE	DOC. NUMBER	REV
A3	CS	Model No	AXI

CHANGE by Smit 15-Mar-2007

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