AT3 BLOCK DIAGRAM

01

04-- 0402 footprint
06-- 0603 footprint
08-- 0805 footprint
12-- 1206 footprint
F-- 1% tolerance

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : SGND1
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : IN3
- LAYER 7 : SGND2
- LAYER 8 : BOT

CPU Merom
478P (uPGA)/35W
PAG 3,4

CPU THERMAL SENSOR
PAG 5

14.318MHz

CLOCK GEN
ICS9LPRS355AGLFT
64pinsTSSOP
PAG 2

CLK_CPU_BCLK, CLK_CPU_BCLK#
CLK_MCH_BCLK, CLK_MCH_BCLK#
DREFCLK, DREFCLK#
DREFSSCLK, DREFSSCLK#

NORTH BRIDGE
Crestline
PAG 7,8,9,10,11,12

DDRII-SODIMM1
PAG 13,14
DDRII 533,667 MHz

DDRII-SODIMM2
PAG 13,14
DDRII 533,667 MHz

PCI-Express 16X

NVDIA G3-64 for 15.4"
NVDIA G3-128 for 17"
820p FCBGA
PAG 15,16,17,18,19,20

Option for 17" only
HDMI CON
PAG 26

TV_OUT
CRT_OUT

CRT / S-VIDEO
PAG 25

LVDS(2 Channel)

Panel Connector
15" / 17" PAG 26

DMI LINK

NBSRCCLK, NBSRCCLK#

Cable Docking
PAG 38
- TV_OUT
- VGA
- RJ-45
- CIR/Pwr btn
- SPDIF Out
- Stereo MIC
- Headphone Jack
- USB Port
- VOL Cntr

USB2.0
5 | 0,1,2 | 3 | 4,6,7

Bluetooth PAG 35
USB2.0 I/O Ports X3 PAG 32
Camera X1 PAG 32
Mini PCI-E Card x1
Express Card x1
Cable Docking x1

Option for 17" only
SATA - HDD PAG 35
SATA2

SATA - HDD PAG 32
SATA0 150MB

PATA- CD-ROM PAG 32
PATA (66/100/133)

SOUTH BRIDGE
ICH-8M
PAG 21,22,23,24

PCI BUS / 33MHz
PCI-E
Azalia
LPC

SYSTEM CHARGER(MAX8724) PAG 41
SYSTEM POWER MAX8778 PAG 42
DDR II SMDDR_VTERM 1.8V/1.8VSUS(TPS51116REGR) PAG 46
VCCP +1.5V AND GMCH 1.05V(MAX8717) PAG 43
VGACORE(1.025V)MAX1992 PAG 45
CPU CORE MAX8771 PAG 44

Realtek
ALC 268
PAG 29

Two-element microphone PAG 29
Audio Jacks (Phone/ MIC) PAG 29

Mini PCI-E Card
PCI Express Mini Card (Wireless LAN/WAN)
PAG 39

LAN
Realtek PCIE-LAN
RTL8101E/8111B
(10/100/GagaLAN)
PAG 33,34

Express Card
(NEW CARD)
PAG 35

RICOH
RICOH 832
PAG 27,28

SIM CARD PAG 32
RJ45 PAG 33
IEEE1394 CONN PAG 28
Memory CardReader PAG 27

Keyboard Touch Pad PAG 36
CIR PAG 36
Capacitive Sense SW PAG 36

ENE KBC
KB3920 Bx
KB3926 Bx
PAG 37,48

X-Bus

FAN PAG 38
Flash PAG 37
SPI PAG 37

AUDIO Amplifier PAG 30
Jack to Speaker PAG 30

MDC DAA
SI3080
PAG 31
MODEM RJ 11 PAG 33

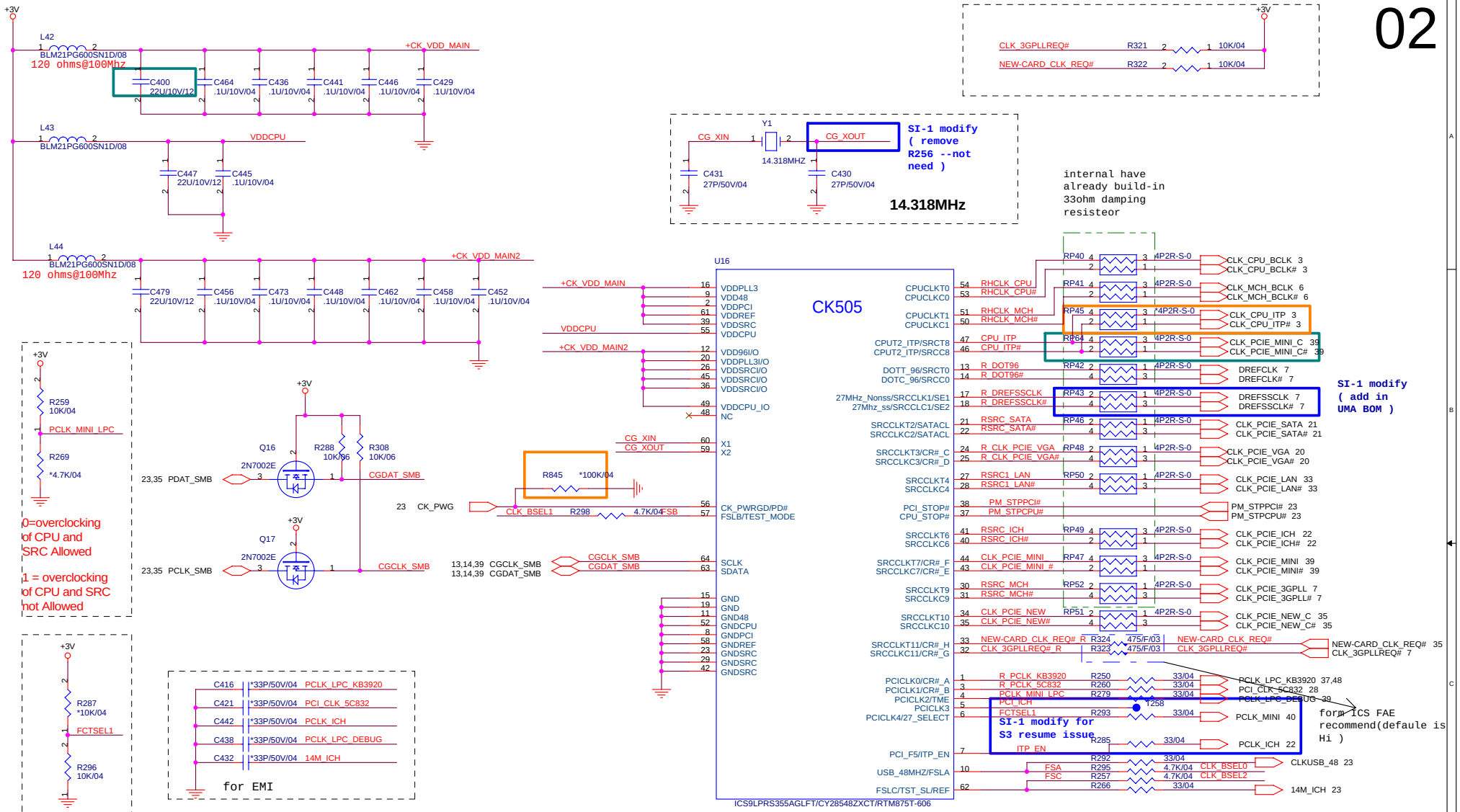
PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD25	INTE#,INTF#	RICOH832
REQ1# / GNT1#	AD22	INTC#,INTD#	MINI PCI for debug

PROJECT : AT3
Quanta Computer Inc.

NB5/RD1/HW2

Size	Document Number	Rev
Custom	BLOCK DIAGRAM	1A

Date: Tuesday, January 09, 2007 Sheet 1 of 48



FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

GCLK_SEL = FCTSEL1

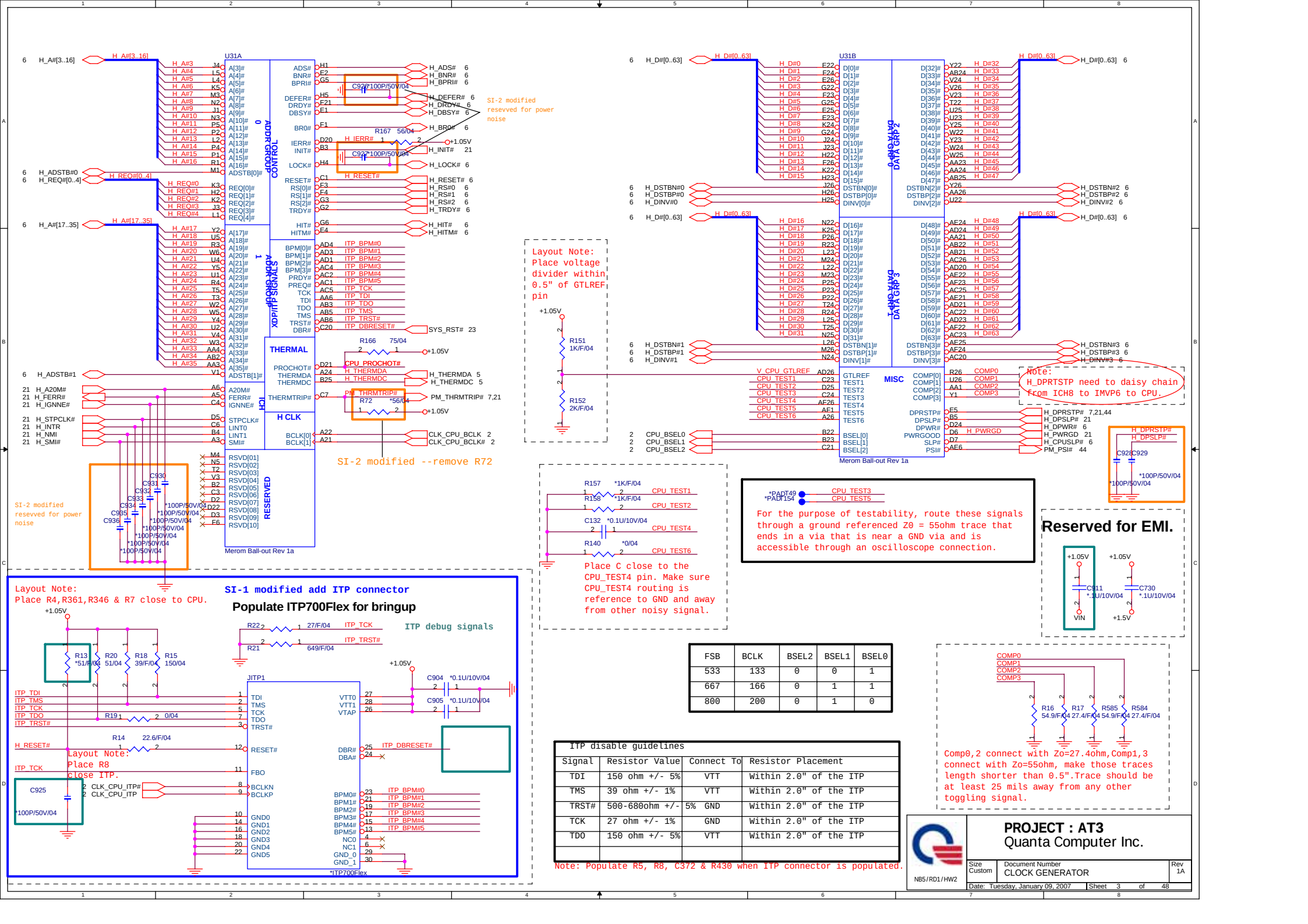
FCTSEL1 (PIN13)	PIN20	PIN21	PIN24	PIN25
0=UMA	DOT96T	DOT96C	SRCT1/LCDT_100	SRCT1/LCDT_100
1 = External VGA	SRCT0	SRCC0	27Mout-NSS	27Mout-SS

PROJECT : AT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CLOCK GENERATOR	1A

NB5/RD1/HW2

Date: Tuesday, January 09, 2007 Sheet 2 of 48



FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0

ITP disable guidelines

Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm +/- 5%	VTT	Within 2.0" of the ITP
TMS	39 ohm +/- 1%	VTT	Within 2.0" of the ITP
TRST#	500-680ohm +/- 5%	GND	Within 2.0" of the ITP
TCK	27 ohm +/- 1%	GND	Within 2.0" of the ITP
TDO	150 ohm +/- 5%	VTT	Within 2.0" of the ITP

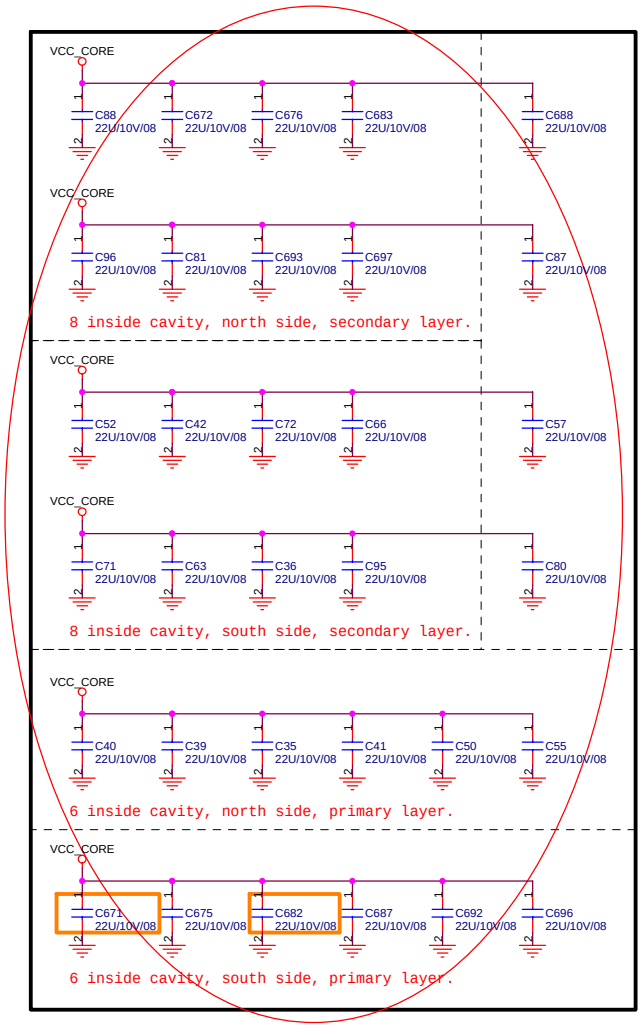
Note: Populate R5, R8, C372 & R430 when ITP connector is populated.

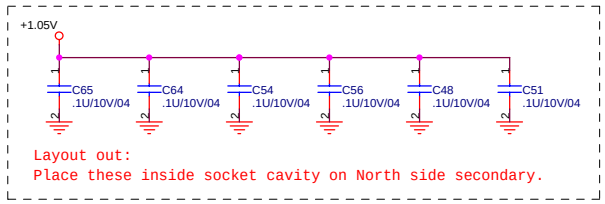
NB5/RD1/HW2

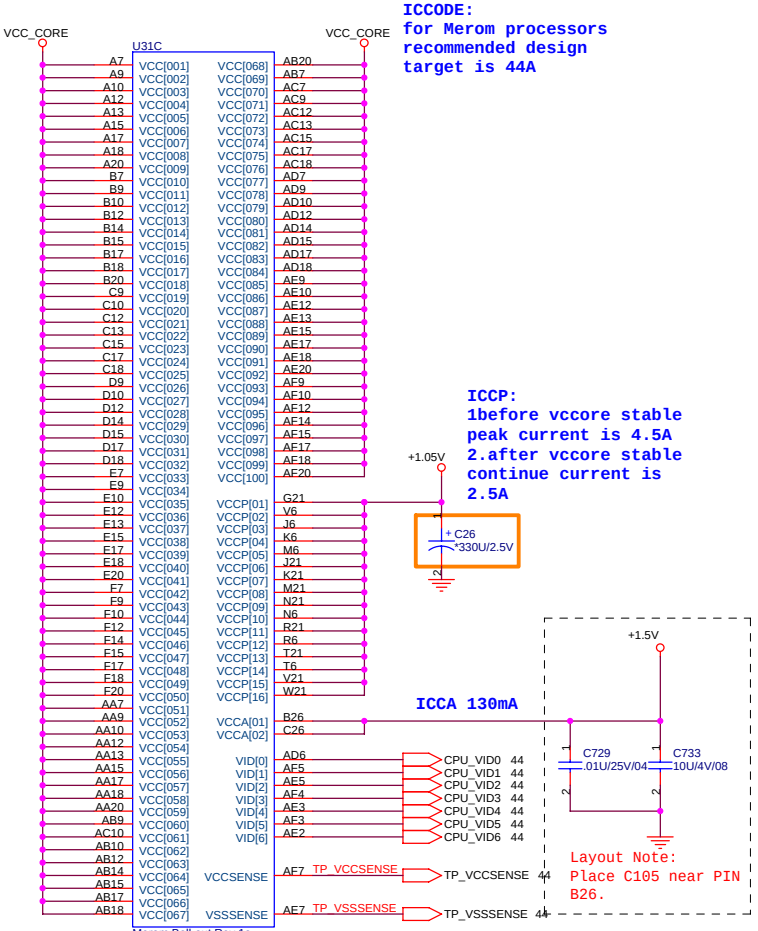
PROJECT : AT3
Quanta Computer Inc.

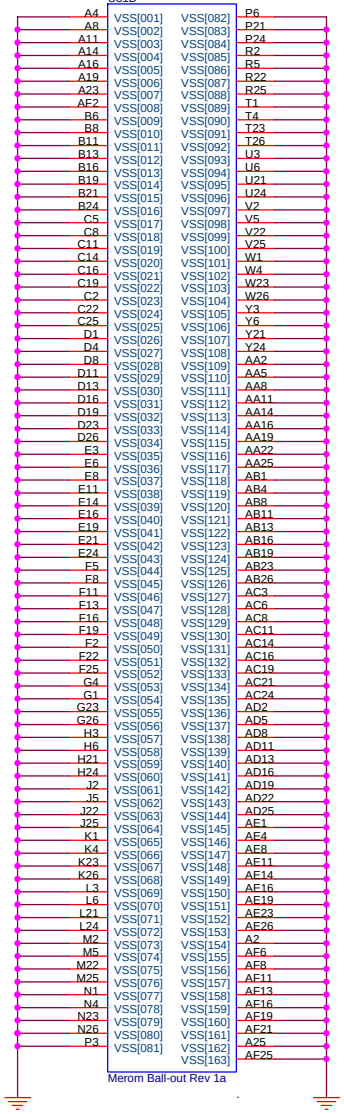
Size	Document Number	Rev
Custom	CLOCK GENERATOR	1A

Date: Tuesday, January 09, 2007 | Sheet 3 of 48

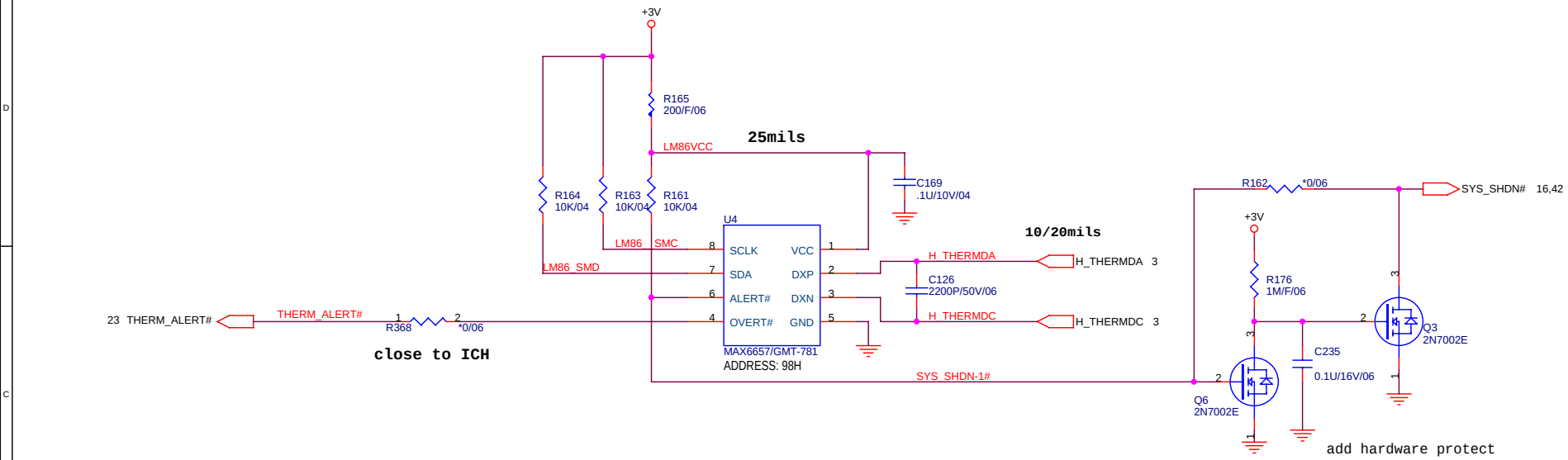


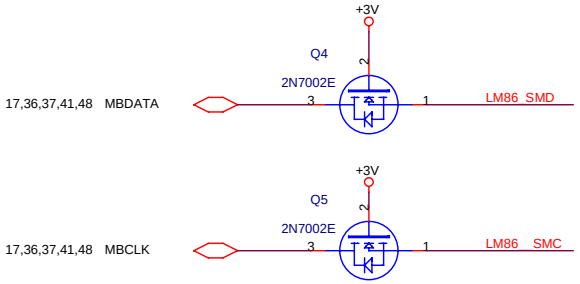






PROJECT : AT3 Quanta Computer Inc.		
Size: Custom	Document Number: Merom Processor (POWER)	Rev: 1A
NB5/RD1/HW2	Date: Tuesday, January 09, 2007	Sheet 4 of 48



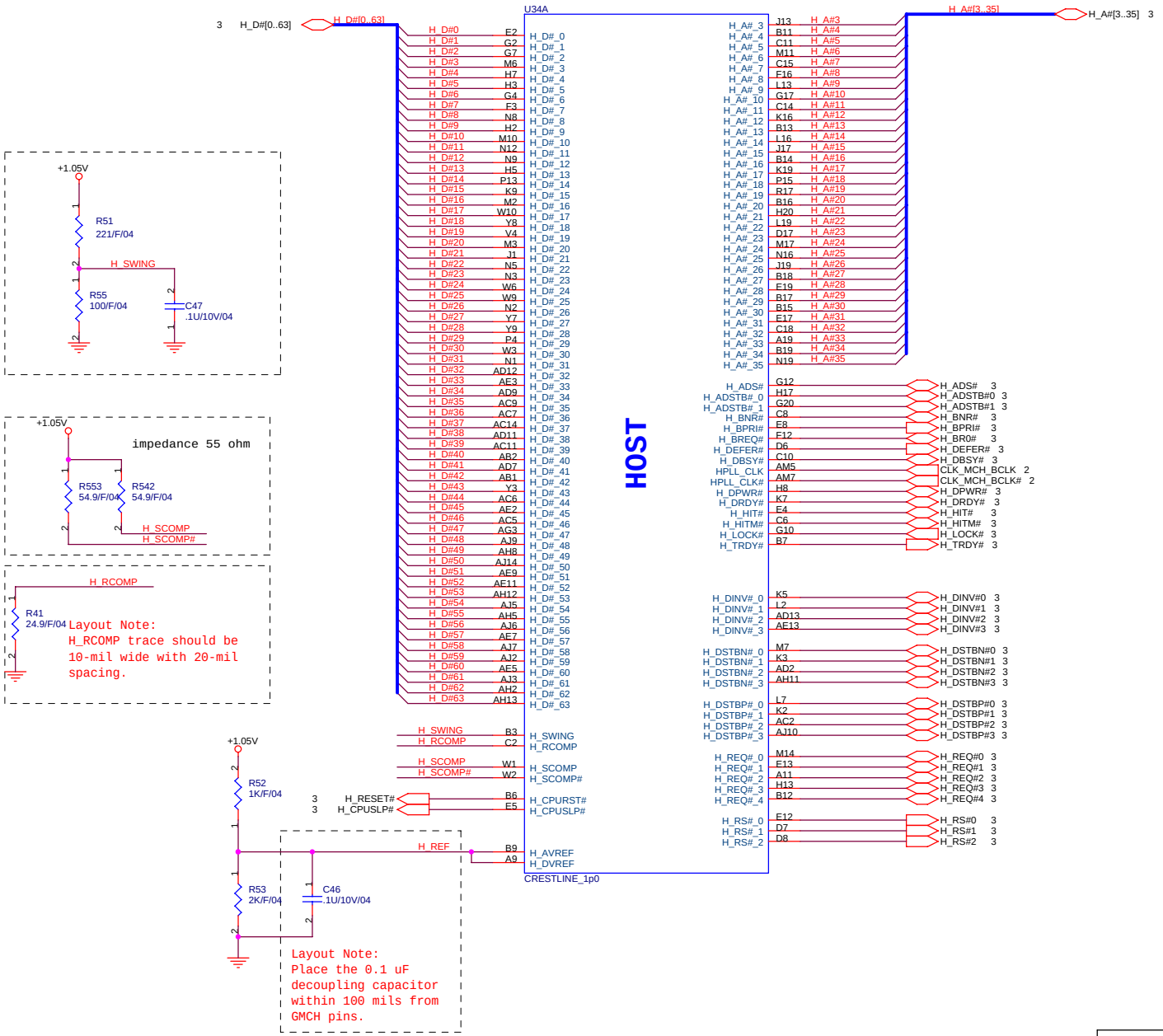


NB5/RD1/HW2

PROJECT : AT3
Quanta Computer Inc.

Size	Document Number	Rev
B	THERMAL LM86	1A

Date: Tuesday, January 09, 2007 Sheet 5 of 48



PROJECT : AT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Crestline (HOST)	1A

NB5/RD1/HW2

Date: Tuesday, January 09, 2007 Sheet 6 of 48

WW22 update
--- MA14 needs
to be routed if
customers are
planning on
using 2Gb
technology and
width=8 (by 8)
DIMMs

CRESTLINE
new pin
define

Layout Note:
Location of all MCH_CFG strap
resistors needs to be close to
minmize stub.

GMCH pwrok is 3.3v
tolerant

<check list & CRB>
For Calero : 1.5K
For
Cresstline:2.4K

IV&EV Dis/Enable
setting

SI-1 modified add 470P

<check lisr & CRB>
For Calero : 255
For Cresstline:1.3K/F
For external VGA:0
ohm

IV&EV Dis/Enable setting

<FAE>
Flexible and safe

<check list>
HSYNC/VSYNC serial R
place close to NB

In Crestline EDS
Rev.1.0, Render
Standby Voltage is
not finalized
yet(TBD), 1.05V for
Graphic Voltage
range(VCC_AXG) is
between 0.9975V(min.)
and 1.1025V(max.).
Vgfx max at 1.1025V @
8A (estimated)

only reserver AT3/5 not
support IAMT,but design
line suggest to connection
these pin ,do not NC

CLKREQ# (MCH drives CLK_REQ# to control the PCI-E diff clk input itself)

<FAE>
If no use DREFCLK PU and
DREFCLK# PD

IV&EV Dis/Enable setting

<design guide>
If no use
DREFCLK PU and
DREFCLK# PD

<check list>
For EV@
Connect to GND
CRT R/G/B
TV A/B/C
HSYNC/VSYNC

<check list>
For IV@
Connect to 150ohm
CRT R/G/B
TV A/B/C
Connect to 39ohm
HSYNC/VSYNC

SI-1 modified
add 150ohm in
the UMA BOM

<check list>
SDVO/PCIE/LVDS not
implement
16 lanes NC

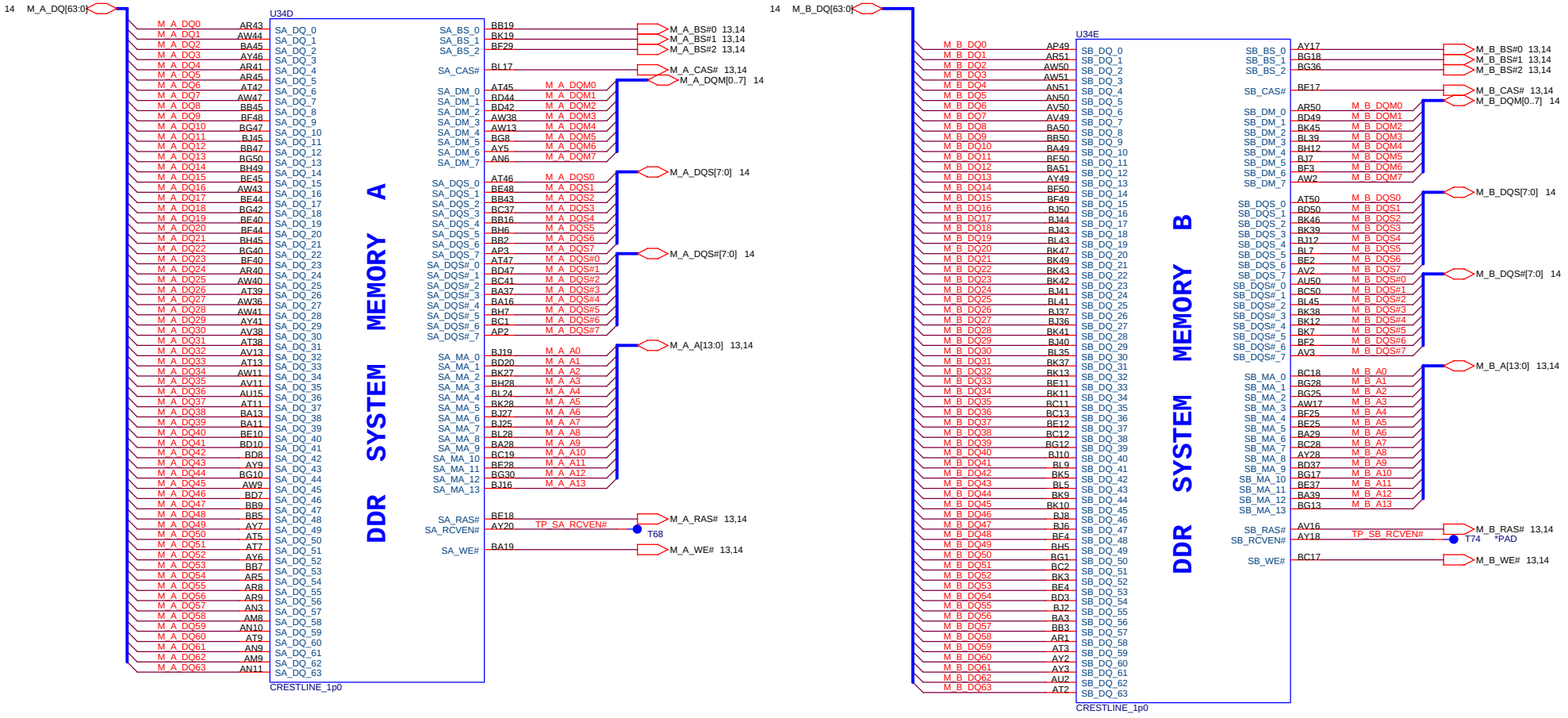
IV&EV Dis/Enable setting

PROJECT : AT3
Quanta Computer Inc.

NB5/RD1/HW2

Size: Custom | Document Number: Crestline (VGA,DMI) | Rev: 1A

Date: Tuesday, January 09, 2007 | Sheet 7 of 48



NB5/RD1/HW2

PROJECT : AT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Crestline (DDR)	1A

Date: Tuesday, January 09, 2007 Sheet 8 of 48

POWER

IVCCSM supply current 1 channel 1.615A 2 channel 3.318A

Ivcc (External GFX 1.310 A, integrate 1.572 A)

Ivcc_AXG Graphics core supply current 7.7A

SI-1 modify (remove R73,R11 --not need)

SI-2 modified --remove C91&C108

Layout Note: 370 mils from edge.

Layout Note: Inside GMCH cavity.

Layout Note: Inside GMCH cavity for VCC_AXG.

for IAMT power if not support need to connection to S0 power

Ivcc_AXM Controller supply current 540mA

Layout Note: Inside GMCH cavity.

Layout Note: Place close to GMCH edge.

Layout Note: Place C901 where LVDS and DDR2 taps.

Layout Note: Place on the edge.

GMCH 1.05V	current(A)	Remark
VCC Core	1.573	(1.3A for external 6bx integrated Gfx
VCC_AXG	7.7	
VCC_AXD	0.2	
VTT	0.85	FSB VCCP
VCC_PEG	1.2	for PCIEG
VCC_AXM	0.54	for IAMT function
VCCR_RX_DMI	0.25	DMI
SUM	**12.313**	

CRESTLINE_1p0

CRESTLINE_1p0

NB5/RD1/HW2

PROJECT : AT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Crestline (VCC, NCTF)	1A

Date: Tuesday, January 09, 2007 Sheet 9 of 48

CRT/TV Disable/Enable guideline

External VGA with EV@part,Internal VGA with IV@ part

Ball	Enable	Disable	Ball	Enable	Disable
VCCA_CRT_DAC	3.3V	GND	VCCA_TVC_DAC	3.3V	GND
VCCD_CRT	1.5V	GND	VCCD_TVDAC	1.5V	1.5V
VCCD_QDAC	1.5V	GND	VCCA_DAC_BG	3.3V	GND
VCCA_TVA_DAC	3.3V	GND	VSS_DAC_BG	GND	GND
VCCA_TVB_DAC	3.3V	GND	VCCSYNC	3.3V	GND

LVDS Disable/Enable guideline

External VGA with EV@part,Internal VGA with IV@ part

Signal	If SDVO Disable LVDS Disable	If LVDS enable
VCCD_LVDS	GND	1.8V
VCCA_LVDS	GND	1.8V
VCC_TX_LVDS	GND	1.8V

IV&EV Dis/Enable setting

<FAE>
INT VGA disable
VCCSYNC connect
to GND

FB_180ohm+-25%_100mHz_1500mA_0.09ohm DC

SI-1 modify
(NET name
wrong)

FB_120ohm+-25%_100mHz
_200mA_0.2ohm DC

10uH+-20%_100mA

0.1Caps should be
placed 200 mils
with in its pins.

Ivcca_PEG_BG
supply current
100mA

Ivcc_VTT FSB
supply
current
0.85A

Place on the edge.

Reserved L81 pad for
inductor.
Place caps close
to VCC_AXD.

Ivcc_DMI supply
current 100mA

Place caps close
to VCC_AXF

Ivcc_PEG
supply current
1.2A

SI-1 modified change

Ivcc_RX_DMI
supply current
250mA

1uH+-20%_300mA

SI-2
modified
for WW44
request

SI-2 add for UMA to
fix TV-out noise

22nF & 0.1uF for
VCC_TVDACA:C_R should
be placed with in 250
mils from Crestline.

FB_220ohm+-25%_100MHz
_2A_0.1ohm DC

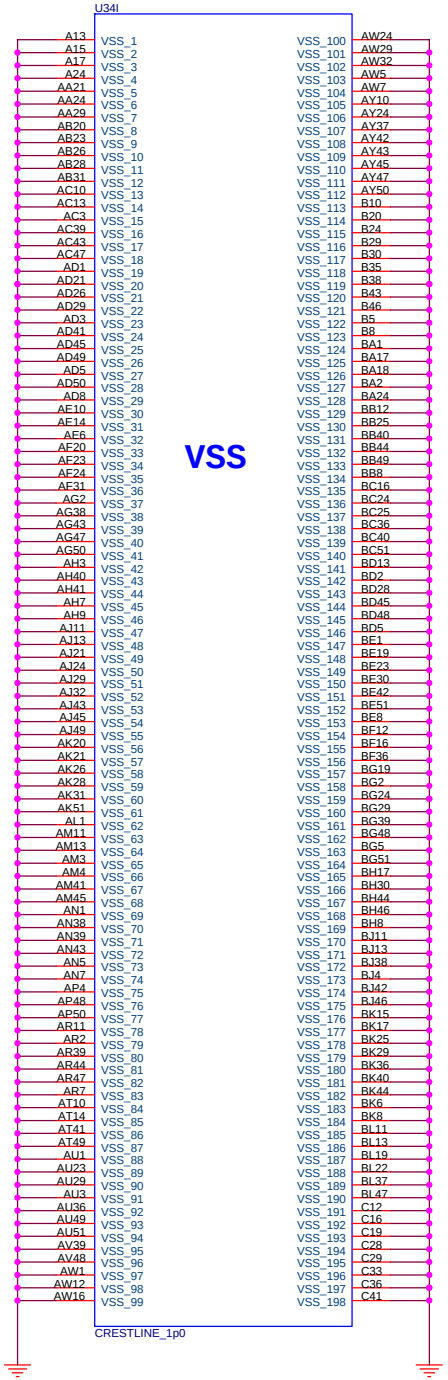
+3V_VCC_HV

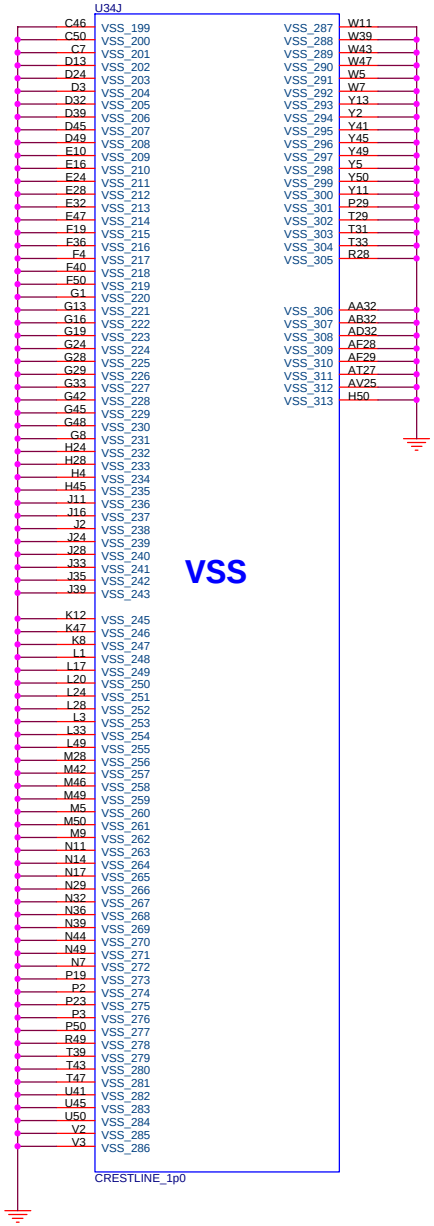
40 mil
wide

U34H
CRESTLINE_1p0

POWER

CRT	VCCSYNC, VCCA_CRT_DAC_1, VCCA_CRT_DAC_2, VCCA_DAC_BG, VSSA_DAC_BG
PLL	VCCA_DPLLA, VCCA_DPLLB, VCCA_HPLL, VCCA_MPLL
A LVDS	VCCA_LVDS, VSSA_LVDS
A PEG	VCCA_PEG_BG, VSSA_PEG_BG, VCCA_PEG_PLL
A SM	VCCA_SM_1 … VCCA_SM_11, VCCA_SM_NCTF_1, VCCA_SM_NCTF_2
A CK	VCCA_SM_CK_1, VCCA_SM_CK_2
D TV/CRT	VCCA_TVA_DAC_1, VCCA_TVA_DAC_2, VCCA_TVB_DAC_1, VCCA_TVB_DAC_2, VCCA_TVC_DAC_1, VCCA_TVC_DAC_2
LVDS	VCCD_CRT, VCCD_TVDAC, VCCD_QDAC, VCCD_HPLL, VCCD_PEG_PLL, VCCD_LVDS_1, VCCD_LVDS_2
VTT	VTT_1 … VTT_22
AXD	VCC_AXD_1 … VCC_AXD_6, VCC_AXD_NCTF
AXF	VCC_AXF_1, VCC_AXF_2, VCC_AXF_3, VCC_DMI
SM CK	VCC_SM_CK_1 … VCC_SM_CK_4
HV	VCC_HV_1, VCC_HV_2
PEG	VCC_PEG_1 … VCC_PEG_5
DMI	VCC_RXR_DMI_1, VCC_RXR_DMI_2
VTTLF	VTTLF1, VTTLF2, VTTLF3





PROJECT : AT3	
Quanta Computer Inc.	
NB5/RD1/HW2	
Size: Custom	Document Number: Crestline (VSS)
Rev: 1A	
Date: Tuesday, January 09, 2007	Sheet 11 of 48

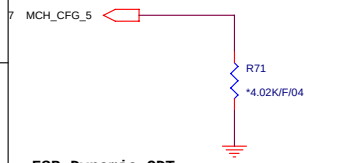
Strap table

All strap are sampled with respect to the leading edge of the GMCH Power OK(PWROK) Signal
CFG[17:3] Have internal Pull-up
CFG[18:19] Have internal Pull-down
Any CFG signal strapping option not list below should be left NC Pin

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 = Mobile CPU(Default)
CFG8	Low power PCI Express	0 = Normal mode 1 = Low Power mode
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALLZ	00 = Reserved 01 = XOR Mode Enable 10 = All-Z Mode Enabled 11 = Normal operation(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card present(Default) 1 = SDVO Card Present
CFG19	DMI Lane Reversal	0 = Normal operation(Default) 1 = Reverse Lanes
CFG20	SDVO/PCIe concurrent	0 = Only SDVO or PCIE x1 is operation(Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port

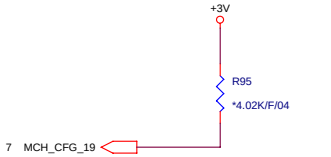
DMI X2 Select

MCH_CFG_5	Low = DMIX2 High = IDMIX4(Default)



DMI Lane Reversal

MCH_CFG_19	Low = Normal operation(Default) High = Reverse Lane

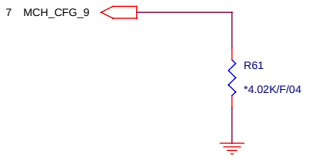


XOR /ALLz /Clock Un-gating

MCH_CFG_12	MCH_CFG_13	Configuration
0	0	Clock gating disable
0	1	XOR Mode Enable
1	0	ALL-z Mode Enable
1	1	Normal operation(Default)

PCI Express Graphics

MCH_CFG_9	Low = Reverse Lane High = Normal operation(Default)

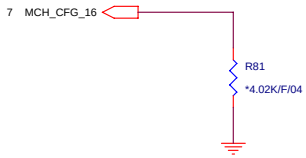


SDVO Present

Strap define at External DVI control page

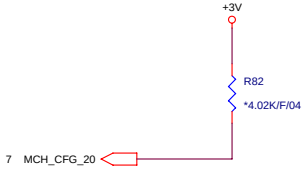
FSB Dynamic ODT

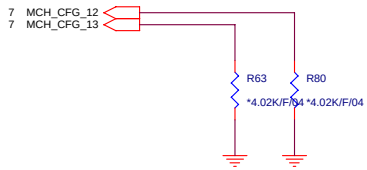
MCH_CFG_16	Low = ODT Disable High = ODT Enable(Default)



SDVO/PCIE Concurrent operation

MCH_CFG_20	Low = Only SDVO or PCIE X1 is operational(Default) High = SDVO andPCIE X1 are operating simultaneously via the PEG port





NB5/RD1/HW2

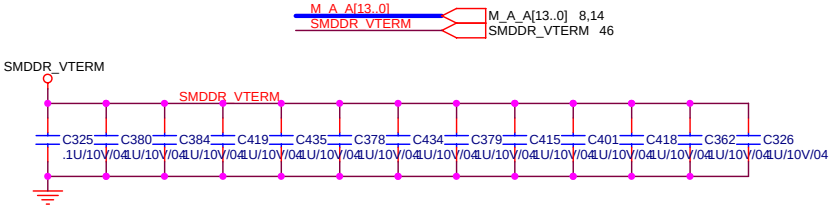
PROJECT : AT3
Quanta Computer Inc.

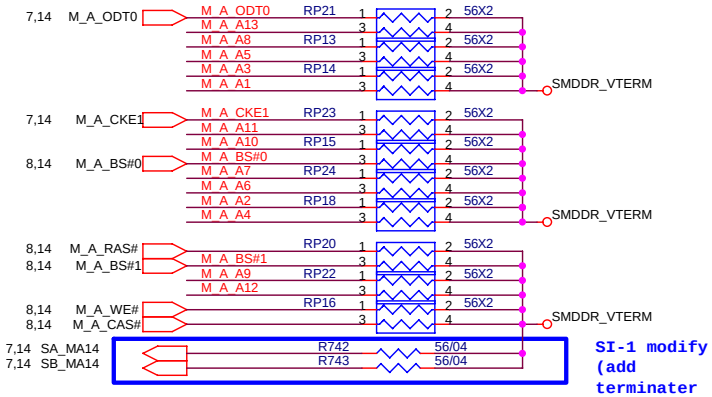
Size	Document Number	Rev
Custom	10 -- GMCH STRAP-3(6 of 6)	1A

Date: Tuesday, January 09, 2007 Sheet 12 of 48

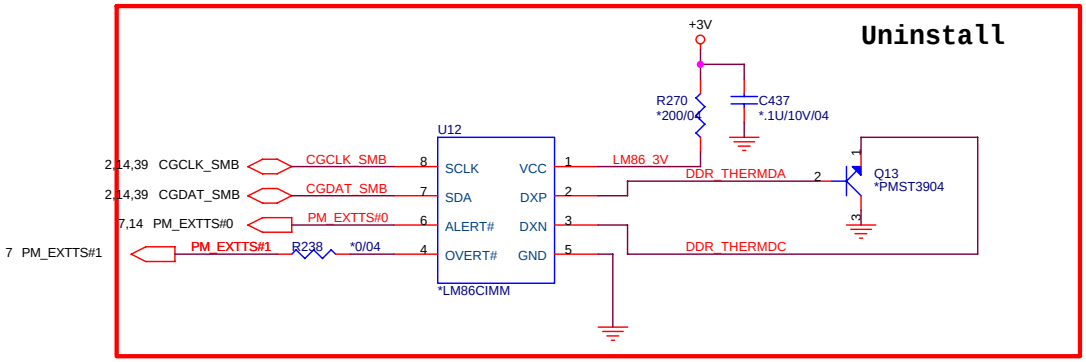
DDRII DUAL CHANNEL A,B.

DDRII A CHANNEL

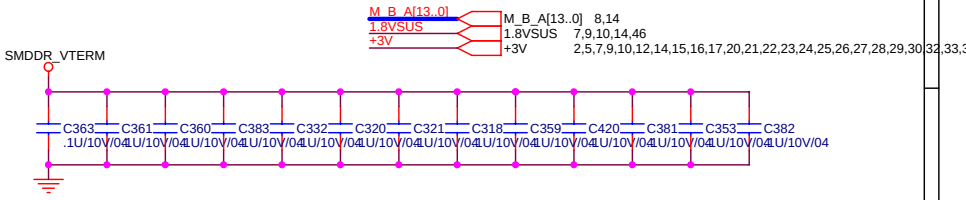




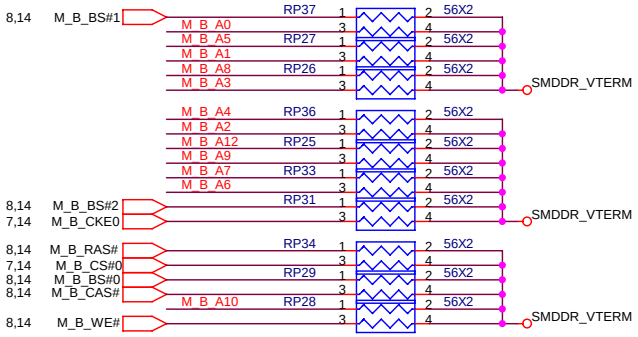
SI-1 modify (add terminater resistor)

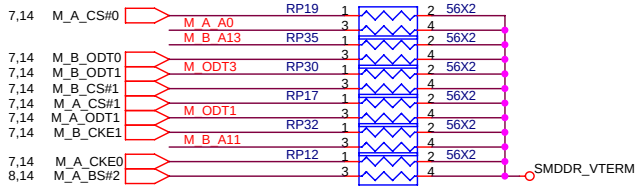


DDRII B CHANNEL



Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM





NB5/RD1/HW2	**PROJECT : AT3** Quanta Computer Inc.	
Size B	Document Number DDRII RES.ARRAY	Rev 1A
Date: Tuesday, January 09, 2007	Sheet 13 of 48	

CGCLK_SMB — CGCLK_SMB 2,13,39
CGDAT_SMB — CGDAT_SMB 2,13,39

M_A_CKE[0..1] — M_A_CKE[0..1] 7,13
M_A_CS#[0..1] — M_A_CS#[0..1] 7,13

M_A_RAS# — M_A_RAS# 8,13
M_A_CAS# — M_A_CAS# 8,13
M_A_WE# — M_A_WE# 8,13

M_A_CLK0 — M_A_CLK0 7
M_A_CLK0# — M_A_CLK0# 7
M_A_CLK1 — M_A_CLK1 7
M_A_CLK1# — M_A_CLK1# 7
M_A_BS#[0..2] — M_A_BS#[0..2] 8,13
M_A_ODT[0..1] — M_A_ODT[0..1] 7,13

M_A_DQM[0..7] — M_A_DQM[0..7] 8
M_A_DQ[0..63] — M_A_DQ[0..63] 8
M_A_DQS[0..7] — M_A_DQS[0..7] 8
M_A_DQS#[0..7] — M_A_DQS#[0..7] 8
M_A_A[13..0] — M_A_A[13..0] 8,13

+3V
1.8VSUS — +3V 1.8VSUS 2,5,7,9,10,12,13,15,16,17,20,21,22,23,24,25,26,27,28,29,30,32,33,35,36,37,38,39,40,42,47 7,9,10,46

M_B_CKE[0..1] — M_B_CKE[0..1] 7,13
M_B_CS#[0..1] — M_B_CS#[0..1] 7,13

M_B_RAS# — M_B_RAS# 8,13
M_B_CAS# — M_B_CAS# 8,13
M_B_WE# — M_B_WE# 8,13

M_B_CLK0 — M_B_CLK0 7
M_B_CLK0# — M_B_CLK0# 7
M_B_CLK1 — M_B_CLK1 7
M_B_CLK1# — M_B_CLK1# 7
M_B_BS#[0..2] — M_B_BS#[0..2] 8,13
M_B_ODT[0..1] — M_B_ODT[0..1] 7,13

M_B_DQM[0..7] — M_B_DQM[0..7] 8
M_B_DQ[0..63] — M_B_DQ[0..63] 8
M_B_DQS[0..7] — M_B_DQS[0..7] 8
M_B_DQS#[0..7] — M_B_DQS#[0..7] 8
M_B_A[13..0] — M_B_A[13..0] 8,13

PC2100 DDR2 SDRAM SO-DIMM (200P) — CKEA 0,1

M_B_DQ1 5 — DQ0
M_B_DQ4 7 — DQ1
M_B_DQ2 17 — DQ2
M_B_DQ3 19 — DQ3
M_B_DQ5 4 — DQ4
M_B_DQ0 6 — DQ5
M_B_DQ7 14 — DQ6
M_B_DQ6 16 — DQ7
M_B_DQ13 23 — DQ8
M_B_DQ12 25 — DQ9
M_B_DQ10 35 — DQ10
M_B_DQ11 37 — DQ11
M_B_DQ8 20 — DQ12
M_B_DQ9 22 — DQ13
M_B_DQ15 36 — DQ14
M_B_DQ14 38 — DQ15
M_B_DQ21 43 — DQ16
M_B_DQ17 45 — DQ17
M_B_DQ19 55 — DQ18
M_B_DQ23 57 — DQ19
M_B_DQ20 44 — DQ20
M_B_DQ16 46 — DQ21
M_B_DQ18 56 — DQ22
M_B_DQ22 58 — DQ23
M_B_DQ28 61 — DQ24
M_B_DQ29 63 — DQ25
M_B_DQ27 73 — DQ26
M_B_DQ26 75 — DQ27
M_B_DQ24 62 — DQ28
M_B_DQ25 64 — DQ29
M_B_DQ31 74 — DQ30
M_B_DQ30 76 — DQ31

M_B_A0 102 — A0
M_B_A1 101 — A1
M_B_A2 100 — A2
M_B_A3 99 — A3
M_B_A4 98 — A4
M_B_A5 97 — A5
M_B_A6 94 — A6
M_B_A7 92 — A7
M_B_A8 93 — A8
M_B_A9 91 — A9
M_B_A10 105 — A10/AP
M_B_A11 90 — A11
M_B_A12 89 — A12

M_B_BS#0 107 — BA0
M_B_BS#1 106 — BA1
M_B_BS#2 85 — NC/BA2

M_B_CLK0 30 — CLK0
M_B_CLK0# 32 — CLK0
M_B_CLK1 164 — CLK1
M_B_CLK1# 166 — CKL1

CGCLK_SMB 197 — SCL
CGDAT_SMB 195 — SDA
DIM2_SA0 198 — SA0
DIM2_SA1 200 — SA1

+3V — 199 VDDSPD

DQ32 123 — M_B_DQ36
DQ33 125 — M_B_DQ33
DQ34 135 — M_B_DQ35
DQ35 137 — M_B_DQ39
DQ36 124 — M_B_DQ37
DQ37 126 — M_B_DQ32
DQ38 134 — M_B_DQ34
DQ39 136 — M_B_DQ38
DQ40 141 — M_B_DQ40
DQ41 143 — M_B_DQ41
DQ42 151 — M_B_DQ46
DQ43 153 — M_B_DQ43
DQ44 140 — M_B_DQ45
DQ45 142 — M_B_DQ44
DQ46 152 — M_B_DQ47
DQ47 154 — M_B_DQ42
DQ48 157 — M_B_DQ55
DQ49 159 — M_B_DQ49
DQ50 173 — M_B_DQ51
DQ51 175 — M_B_DQ53
DQ52 158 — M_B_DQ48
DQ53 160 — M_B_DQ52
DQ54 174 — M_B_DQ50
DQ55 176 — M_B_DQ54
DQ56 179 — M_B_DQ61
DQ57 181 — M_B_DQ60
DQ58 189 — M_B_DQ59
DQ59 191 — M_B_DQ63
DQ60 180 — M_B_DQ56
DQ61 182 — M_B_DQ57
DQ62 192 — M_B_DQ58
DQ63 194 — M_B_DQ62

DM0 10 — M_B_DQM0
DM1 26 — M_B_DQM1
DM2 52 — M_B_DQM2
DM3 67 — M_B_DQM3
DM4 130 — M_B_DQM4
DM5 147 — M_B_DQM5
DM6 170 — M_B_DQM6
DM7 185 — M_B_DQM7
DQS0 13 — M_B_DQS0
DQS0 11 — M_B_DQS#0
DQS1 31 — M_B_DQS1
DQS1 29 — M_B_DQS#1
DQS2 51 — M_B_DQS2
DQS2 49 — M_B_DQS#2
DQS3 70 — M_B_DQS3
DQS3 68 — M_B_DQS#3
DQS4 131 — M_B_DQS4
DQS4 129 — M_B_DQS#4
DQS5 148 — M_B_DQS5
DQS5 146 — M_B_DQS#5
DQS6 169 — M_B_DQS6
DQS6 167 — M_B_DQS#6
DQS7 188 — M_B_DQS7
DQS7 186 — M_B_DQS#7

CS0 110 — M_B_CS#0
CS1 115 — M_B_CS#1
RAS 108 — M_B_RAS#
CAS 113 — M_B_CAS#
WE 109 — M_B_WE#
CKE0 79 — M_B_CKE0
CKE1 80 — M_B_CKE1

FOX=AS0A426-M2S-TR
CN26A

PC2100 DDR2 SDRAM SO-DIMM (200P) — CKEB 0,1

M_A_DQ1 5 — DQ0
M_A_DQ5 7 — DQ1
M_A_DQ3 17 — DQ2
M_A_DQ2 19 — DQ3
M_A_DQ4 4 — DQ4
M_A_DQ0 6 — DQ5
M_A_DQ7 14 — DQ6
M_A_DQ6 16 — DQ7
M_A_DQ13 23 — DQ8
M_A_DQ8 25 — DQ9
M_A_DQ15 35 — DQ10
M_A_DQ10 37 — DQ11
M_A_DQ9 20 — DQ12
M_A_DQ12 22 — DQ13
M_A_DQ14 36 — DQ14
M_A_DQ11 38 — DQ15
M_A_DQ16 43 — DQ16
M_A_DQ21 45 — DQ17
M_A_DQ23 55 — DQ18
M_A_DQ19 57 — DQ19
M_A_DQ20 44 — DQ20
M_A_DQ17 46 — DQ21
M_A_DQ18 56 — DQ22
M_A_DQ22 58 — DQ23
M_A_DQ24 61 — DQ24
M_A_DQ28 63 — DQ25
M_A_DQ31 73 — DQ26
M_A_DQ30 75 — DQ27
M_A_DQ25 62 — DQ28
M_A_DQ29 64 — DQ29
M_A_DQ27 74 — DQ30
M_A_DQ26 76 — DQ31

M_A_A0 102 — A0
M_A_A1 101 — A1
M_A_A2 100 — A2
M_A_A3 99 — A3
M_A_A4 98 — A4
M_A_A5 97 — A5
M_A_A6 94 — A6
M_A_A7 92 — A7
M_A_A8 93 — A8
M_A_A9 91 — A9
M_A_A10 105 — A10/AP
M_A_A11 90 — A11
M_A_A12 89 — A12

M_A_BS#0 107 — BA0
M_A_BS#1 106 — BA1
M_A_BS#2 85 — NC/BA2

M_A_CLK0 30 — CLK0
M_A_CLK0# 32 — CLK0
M_A_CLK1 164 — CLK1
M_A_CLK1# 166 — CKL1

CGCLK_SMB 197 — SCL
CGDAT_SMB 195 — SDA
DIM1_SA0 198 — SA0
DIM1_SA1 200 — SA1

+3V — 199 VDDSPD

DQ32 123 — M_A_DQ32
DQ33 125 — M_A_DQ35
DQ34 135 — M_A_DQ37
DQ35 137 — M_A_DQ38
DQ36 124 — M_A_DQ33
DQ37 126 — M_A_DQ36
DQ38 134 — M_A_DQ39
DQ39 136 — M_A_DQ34
DQ40 141 — M_A_DQ40
DQ41 143 — M_A_DQ41
DQ42 151 — M_A_DQ46
DQ43 153 — M_A_DQ42
DQ44 140 — M_A_DQ45
DQ45 142 — M_A_DQ44
DQ46 152 — M_A_DQ43
DQ47 154 — M_A_DQ47
DQ48 157 — M_A_DQ52
DQ49 159 — M_A_DQ48
DQ50 173 — M_A_DQ55
DQ51 175 — M_A_DQ54
DQ52 158 — M_A_DQ53
DQ53 160 — M_A_DQ49
DQ54 174 — M_A_DQ50
DQ55 176 — M_A_DQ51
DQ56 179 — M_A_DQ60
DQ57 181 — M_A_DQ56
DQ58 189 — M_A_DQ62
DQ59 191 — M_A_DQ58
DQ60 180 — M_A_DQ57
DQ61 182 — M_A_DQ61
DQ62 192 — M_A_DQ59
DQ63 194 — M_A_DQ63

DM0 10 — M_A_DQM0
DM1 26 — M_A_DQM1
DM2 52 — M_A_DQM2
DM3 67 — M_A_DQM3
DM4 130 — M_A_DQM4
DM5 147 — M_A_DQM5
DM6 170 — M_A_DQM6
DM7 185 — M_A_DQM7
DQS0 13 — M_A_DQS0
DQS0 11 — M_A_DQS#0
DQS1 31 — M_A_DQS1
DQS1 29 — M_A_DQS#1
DQS2 51 — M_A_DQS2
DQS2 49 — M_A_DQS#2
DQS3 70 — M_A_DQS3
DQS3 68 — M_A_DQS#3
DQS4 131 — M_A_DQS4
DQS4 129 — M_A_DQS#4
DQS5 148 — M_A_DQS5
DQS5 146 — M_A_DQS#5
DQS6 169 — M_A_DQS6
DQS6 167 — M_A_DQS#6
DQS7 188 — M_A_DQS7
DQS7 186 — M_A_DQS#7

CS0 110 — M_A_CS#0
CS1 115 — M_A_CS#1
RAS 108 — M_A_RAS#
CAS 113 — M_A_CAS#
WE 109 — M_A_WE#
CKE0 79 — M_A_CKE0
CKE1 80 — M_A_CKE1

FOX=AS0A426-MAS-TR
CN24A

PC2100 DDR2 SDRAM SO-DIMM (200P)

SMDDR_VREF_DMM — 1 VREF
1.8VSUS — 81 VDD_1
1.8VSUS — 82 VDD_2
1.8VSUS — 87 VDD_3
1.8VSUS — 88 VDD_4
1.8VSUS — 95 VDD_5
1.8VSUS — 96 VDD_6
1.8VSUS — 103 VDD_7
1.8VSUS — 104 VDD_8
1.8VSUS — 111 VDD_9
1.8VSUS — 112 VDD_10
1.8VSUS — 117 VDD_11
1.8VSUS — 118 VDD_12

M_B_ODT0 — 114 ODT0
M_B_ODT1 — 119 ODT1

7,13 PM_EXTTS#0 — 50 NC_1
SI-1 CHANGE
SB_MA14 — 69 NC_2
M_B_A13 — 83 NC_3
84 NC_4/A15
86 NC_5/A14
NC_6/A13
NC_7
120
163
NC_8

162 VSS_45
165 VSS_46
168 VSS_47
171 VSS_48
172 VSS_49
177 VSS_50
178 VSS_51
183 VSS_52
184 VSS_53
187 VSS_54
190 VSS_55
193 VSS_56
196 VSS_57
201 VSS_58

VSS_1 2
VSS_2 3
VSS_3 8
VSS_4 9
VSS_5 12
VSS_6 15
VSS_7 18
VSS_8 21
VSS_9 24
VSS_10 27
VSS_11 28
VSS_12 33
VSS_13 34
VSS_14 39
VSS_15 40
VSS_16 41
VSS_17 42
VSS_18 47
VSS_19 48
VSS_20 53
VSS_21 54
VSS_22 59
VSS_23 60
VSS_24 65
VSS_25 66
VSS_26 71
VSS_27 72
VSS_28 77
VSS_29 78
VSS_30 121
VSS_31 122
VSS_32 127
VSS_33 128
VSS_34 132
VSS_35 133
VSS_36 138
VSS_37 139
VSS_38 144
VSS_39 145
VSS_40 149
VSS_41 150
VSS_42 155
VSS_43 156
VSS_44 161
VSS_59 202

FOX=AS0A426-M2S-TR
CN26B

SMDDR_VREF_DMM — 1 VREF
1.8VSUS — 81 VDD_1
1.8VSUS — 82 VDD_2
1.8VSUS — 87 VDD_3
1.8VSUS — 88 VDD_4
1.8VSUS — 95 VDD_5
1.8VSUS — 96 VDD_6
1.8VSUS — 103 VDD_7
1.8VSUS — 104 VDD_8
1.8VSUS — 111 VDD_9
1.8VSUS — 112 VDD_10
1.8VSUS — 117 VDD_11
1.8VSUS — 118 VDD_12

M_A_ODT0 — 114 ODT0
M_A_ODT1 — 119 ODT1

7,13 PM_EXTTS#0 — 50 NC_1
SI-1 CHANGE
SA_MA14 — 69 NC_2
M_A_A13 — 83 NC_3
84 NC_4/A15
86 NC_5/A14
NC_6/A13
NC_7
120
163
NC_8

162 VSS_45
165 VSS_46
168 VSS_47
171 VSS_48
172 VSS_49
177 VSS_50
178 VSS_51
183 VSS_52
184 VSS_53
187 VSS_54
190 VSS_55
193 VSS_56
196 VSS_57
201 VSS_58

VSS_1 2
VSS_2 3
VSS_3 8
VSS_4 9
VSS_5 12
VSS_6 15
VSS_7 18
VSS_8 21
VSS_9 24
VSS_10 27
VSS_11 28
VSS_12 33
VSS_13 34
VSS_14 39
VSS_15 40
VSS_16 41
VSS_17 42
VSS_18 47
VSS_19 48
VSS_20 53
VSS_21 54
VSS_22 59
VSS_23 60
VSS_24 65
VSS_25 66
VSS_26 71
VSS_27 72
VSS_28 77
VSS_29 78
VSS_30 121
VSS_31 122
VSS_32 127
VSS_33 128
VSS_34 132
VSS_35 133
VSS_36 138
VSS_37 139
VSS_38 144
VSS_39 145
VSS_40 149
VSS_41 150
VSS_42 155
VSS_43 156
VSS_44 161
VSS_59 202

FOX=AS0A426-MAS-TR
CN24B

C771 470P/50V/04
1 2
SMDDR_VREF_DMM
R226 0/06 — SMDDR_VREF 7,46
R227 — 1.8VSUS
R603 *10K/F/06
*10K/F/06

DIM2_SA0 R267 10K/04
DIM2_SA1 R268 10K/04 +3V
SMbus address A4

R216 10K/04 DIM1_SA0
R217 10K/04 DIM1_SA1
SMbus address A0

Place these Caps near So-Dimm1.

1.8VSUS
C773 2.2U/6.3V/06 C775 2.2U/6.3V/06 C785 2.2U/6.3V/06 C444 2.2U/6.3V/06 C764 2.2U/6.3V/06 C770 .1U/10V/04 C788 .1U/10V/04 C439 .1U/10V/04 C433 .1U/10V/04 C769 .1U/10V/04 C767 .1U/10V/04

SMDDR_VREF_DMM
C772 .1U/10V/04 C768 2.2U/6.3V/06

+3V
C317 2.2U/6.3V/06 C316 .1U/10V/04

SO-DIMM BYPASS PLACEMENT :
Place these Caps near So-Dimm1.
No Vias Between the Trace of PIN to CAP.

Place these Caps near So-Dimm2.

1.8VSUS
C774 2.2U/6.3V/06 C786 2.2U/6.3V/06 C784 2.2U/6.3V/06 C759 2.2U/6.3V/06 C760 .1U/10V/04 C776 .1U/10V/04 C789 .1U/10V/04 C787 .1U/10V/04 C443 .1U/10V/04 C765 .1U/10V/04 C766 .1U/10V/04

SMDDR_VREF_DMM
C371 .1U/10V/04 C373 2.2U/6.3V/06

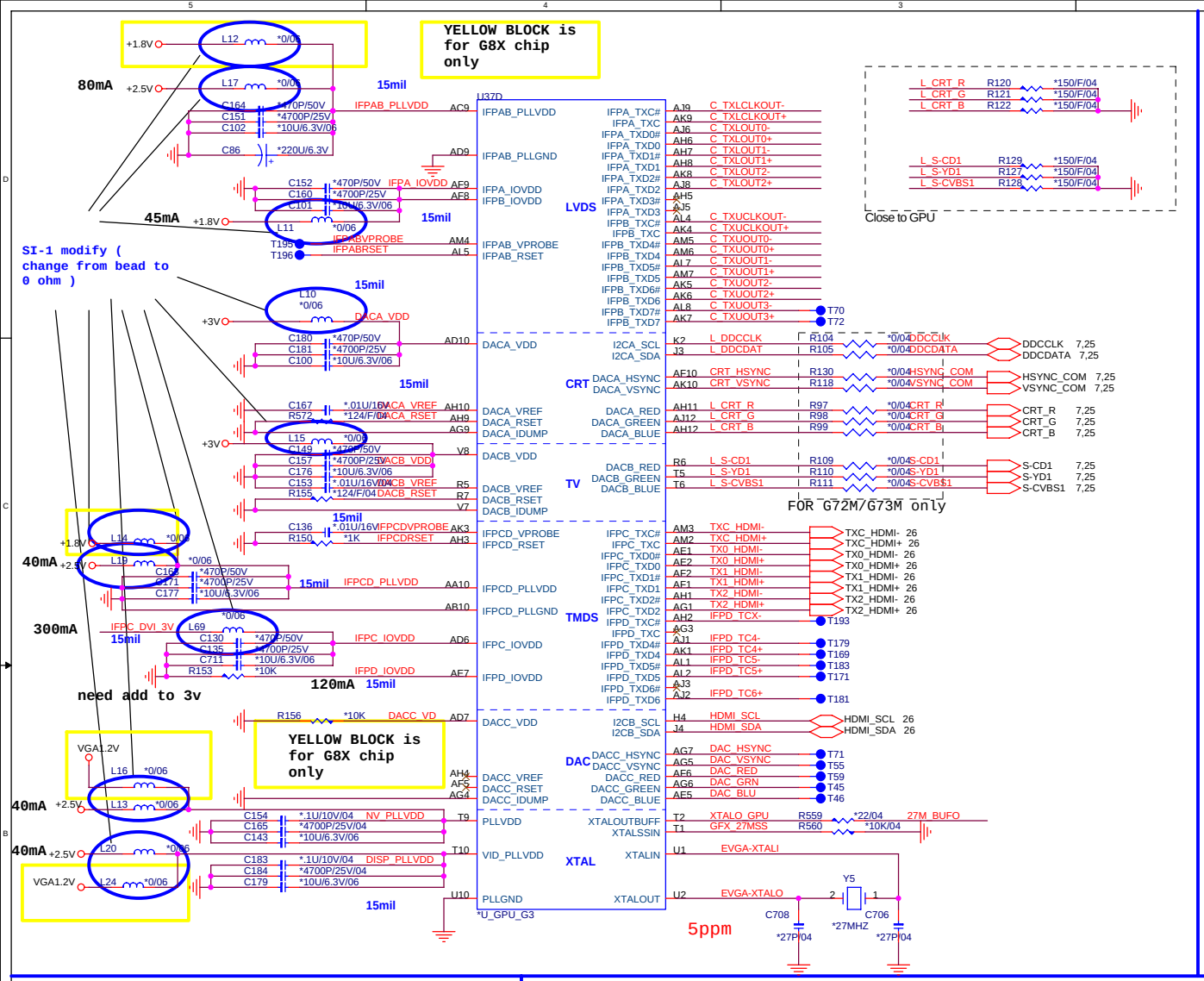
+3V
C372 2.2U/6.3V/06 C385 .1U/10V/04

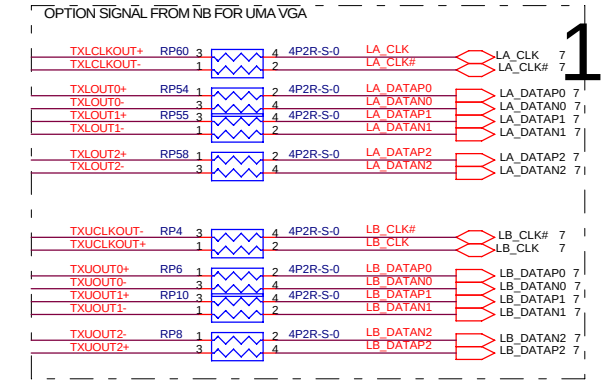
SO-DIMM BYPASS PLACEMENT :
Place these Caps near So-Dimm2
No Vias Between the Trace of PIN to CAP.

NB5/RD1/HW2

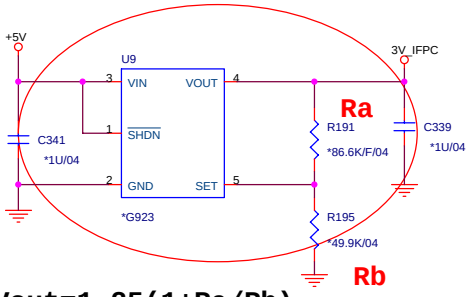
PROJECT : AT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDRII SO-DIMM(200P)	1A
Date: Tuesday, January 09, 2007	Sheet 14 of 48	

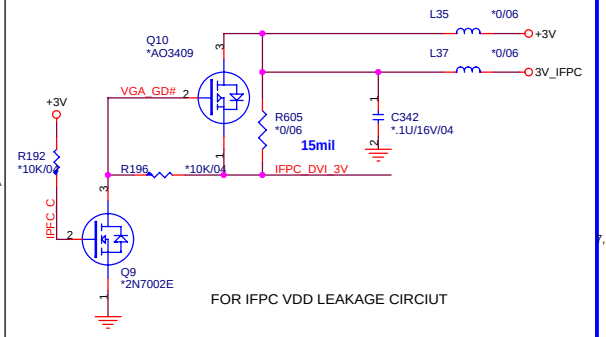




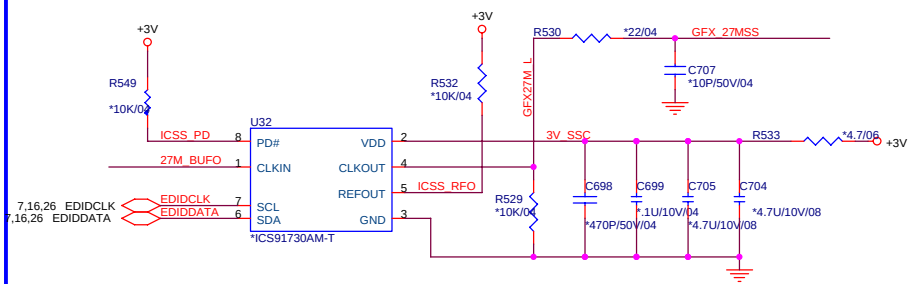
C34: PUN issue reserve
U54,C950,c949,R726,R727



$$Vout=1.25(1+Ra/Rb)$$



SPREAD SPECTRUM



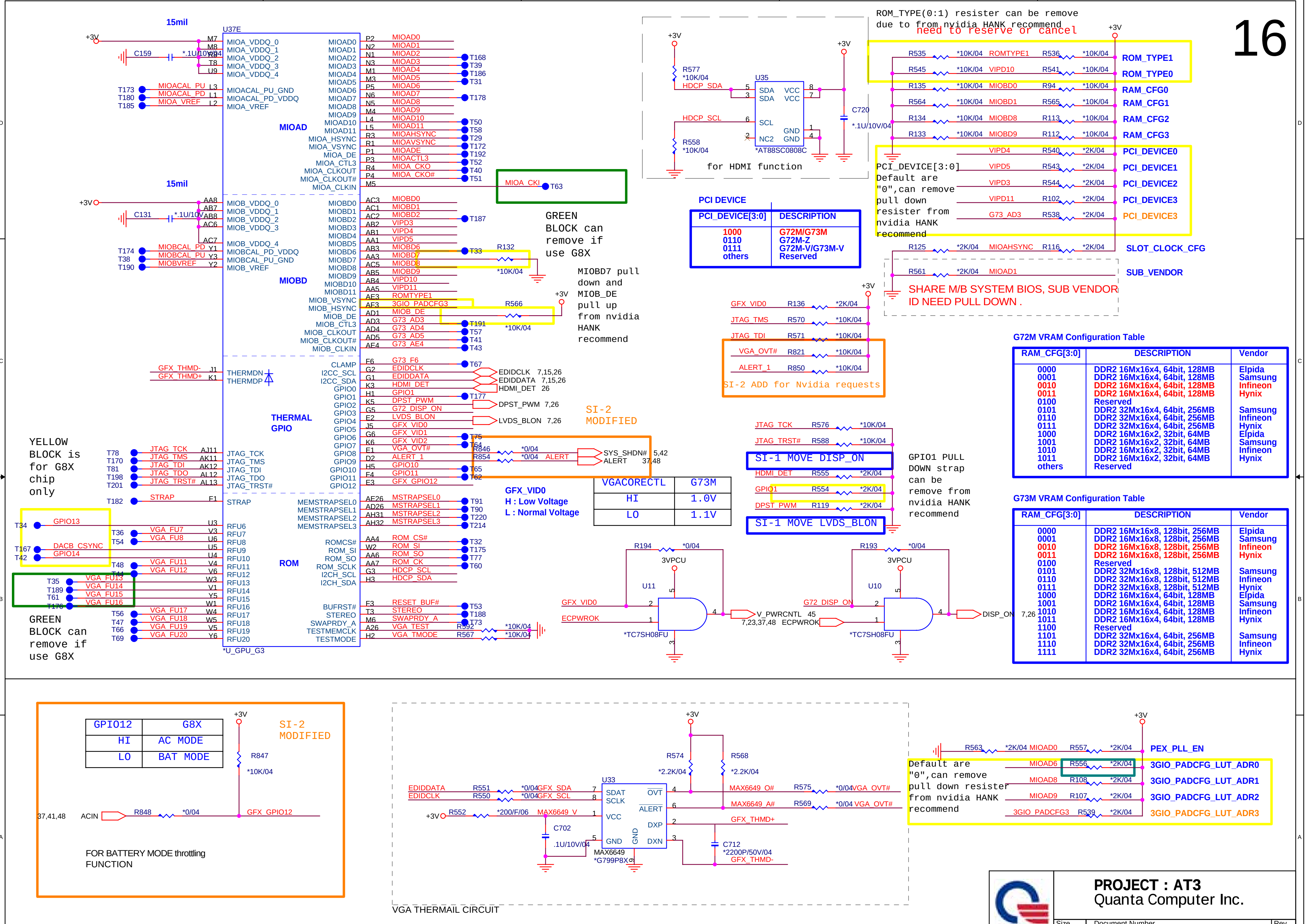
I2C ADDRESS: 0xD4H

PROJECT : AT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NVG73M (LVDS/DVI/CRT/TV)	1A

Date: Tuesday, January 09, 2007 Sheet 15 of 48

NB5/RD1/HW2



PCI DEVICE

PCI_DEVICE[3:0]	DESCRIPTION
1000	G72M/G73M
0110	G72M-Z
0111	G72M-V/G73M-V
others	Reserved

G72M VRAM Configuration Table

RAM_CFG[3:0]	DESCRIPTION	Vendor
0000	DDR2 16Mx16x4, 64bit, 128MB	Elpida
0001	DDR2 16Mx16x4, 64bit, 128MB	Samsung
0010	DDR2 16Mx16x4, 64bit, 128MB	Infineon
0011	DDR2 16Mx16x4, 64bit, 128MB	Hynix
0100	Reserved	
0101	DDR2 32Mx16x4, 64bit, 256MB	Samsung
0110	DDR2 32Mx16x4, 64bit, 256MB	Infineon
0111	DDR2 32Mx16x4, 64bit, 256MB	Hynix
1000	DDR2 16Mx16x2, 32bit, 64MB	Elpida
1001	DDR2 16Mx16x2, 32bit, 64MB	Samsung
1010	DDR2 16Mx16x2, 32bit, 64MB	Infineon
1011	DDR2 16Mx16x2, 32bit, 64MB	Hynix
others	Reserved	

G73M VRAM Configuration Table

RAM_CFG[3:0]	DESCRIPTION	Vendor
0000	DDR2 16Mx16x8, 128bit, 256MB	Elpida
0001	DDR2 16Mx16x8, 128bit, 256MB	Samsung
0010	DDR2 16Mx16x8, 128bit, 256MB	Infineon
0011	DDR2 16Mx16x8, 128bit, 256MB	Hynix
0100	Reserved	
0101	DDR2 32Mx16x8, 128bit, 512MB	Samsung
0110	DDR2 32Mx16x8, 128bit, 512MB	Infineon
0111	DDR2 32Mx16x8, 128bit, 512MB	Hynix
1000	DDR2 16Mx16x4, 64bit, 128MB	Elpida
1001	DDR2 16Mx16x4, 64bit, 128MB	Samsung
1010	DDR2 16Mx16x4, 64bit, 128MB	Infineon
1011	DDR2 16Mx16x4, 64bit, 128MB	Hynix
1100	Reserved	
1101	DDR2 32Mx16x4, 64bit, 256MB	Samsung
1110	DDR2 32Mx16x4, 64bit, 256MB	Infineon
1111	DDR2 32Mx16x4, 64bit, 256MB	Hynix

VGACORECTL	G73M
HI	1.0V
LO	1.1V

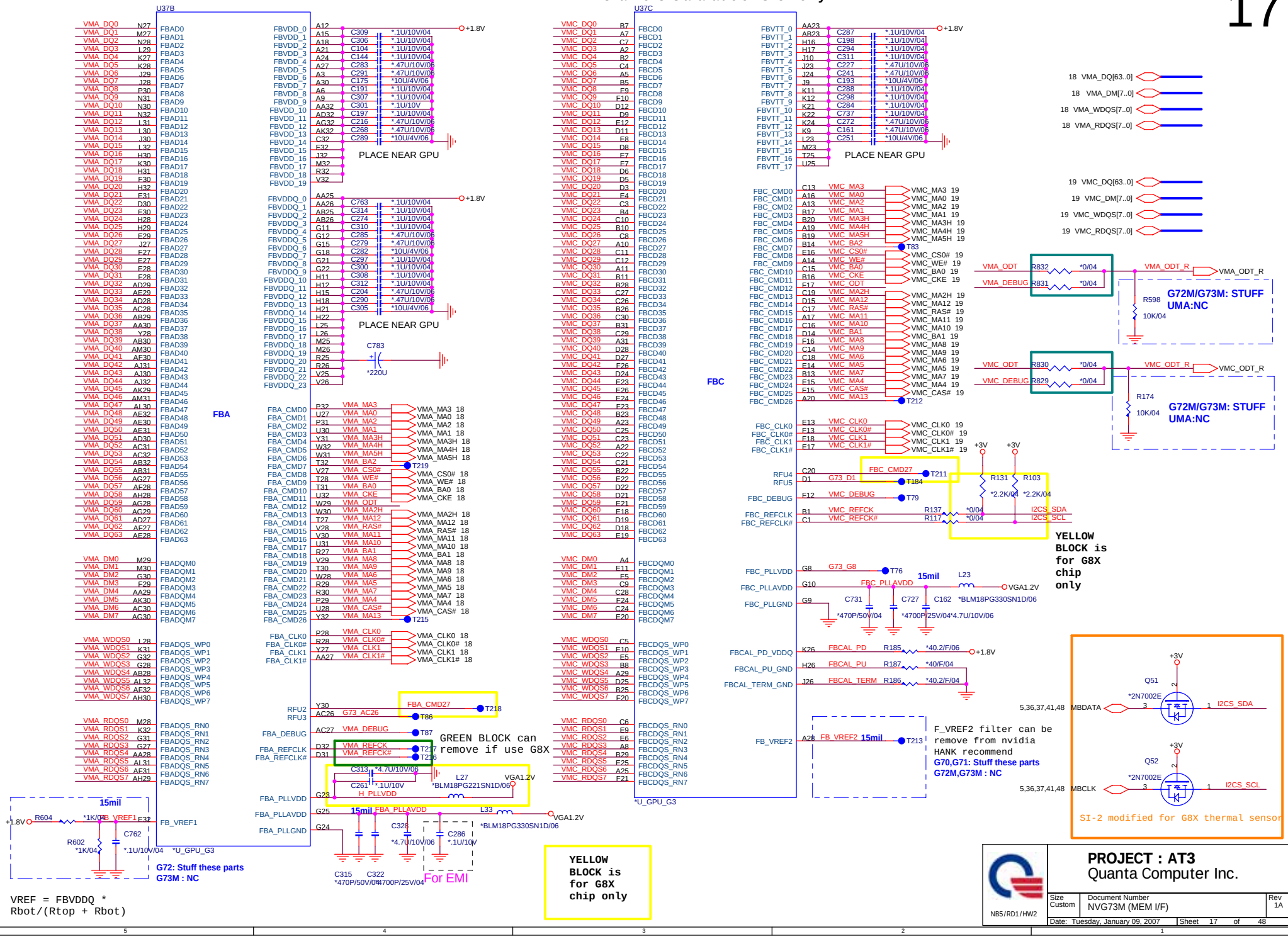
GPIO12	G8X
HI	AC MODE
LO	BAT MODE

PROJECT : AT3
Quanta Computer Inc.
NB5/RD1/HW2

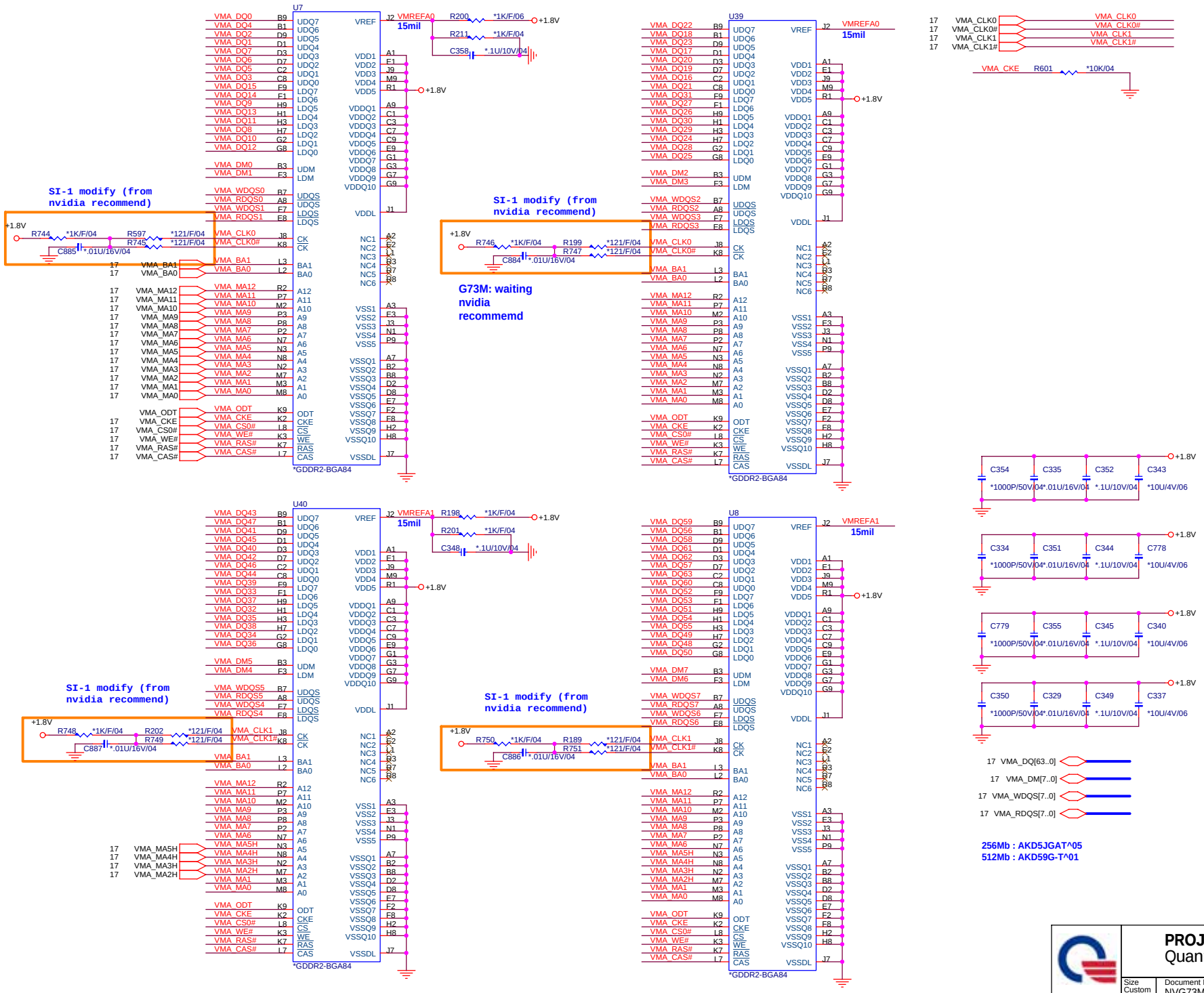
Size	Document Number	Rev
Custom	NVG73M (ROM/GPIO/STRAP)	1A

Date: Tuesday, January 09, 2007 Sheet 16 of 48

Channel C is available on G73M only



PROJECT : AT3		
Quanta Computer Inc.		
NB5/RD1/HW2	Size: Custom	Document Number: NVG73M (MEM I/F)
	Rev: 1A	
	Date: Tuesday, January 09, 2007	Sheet 17 of 48

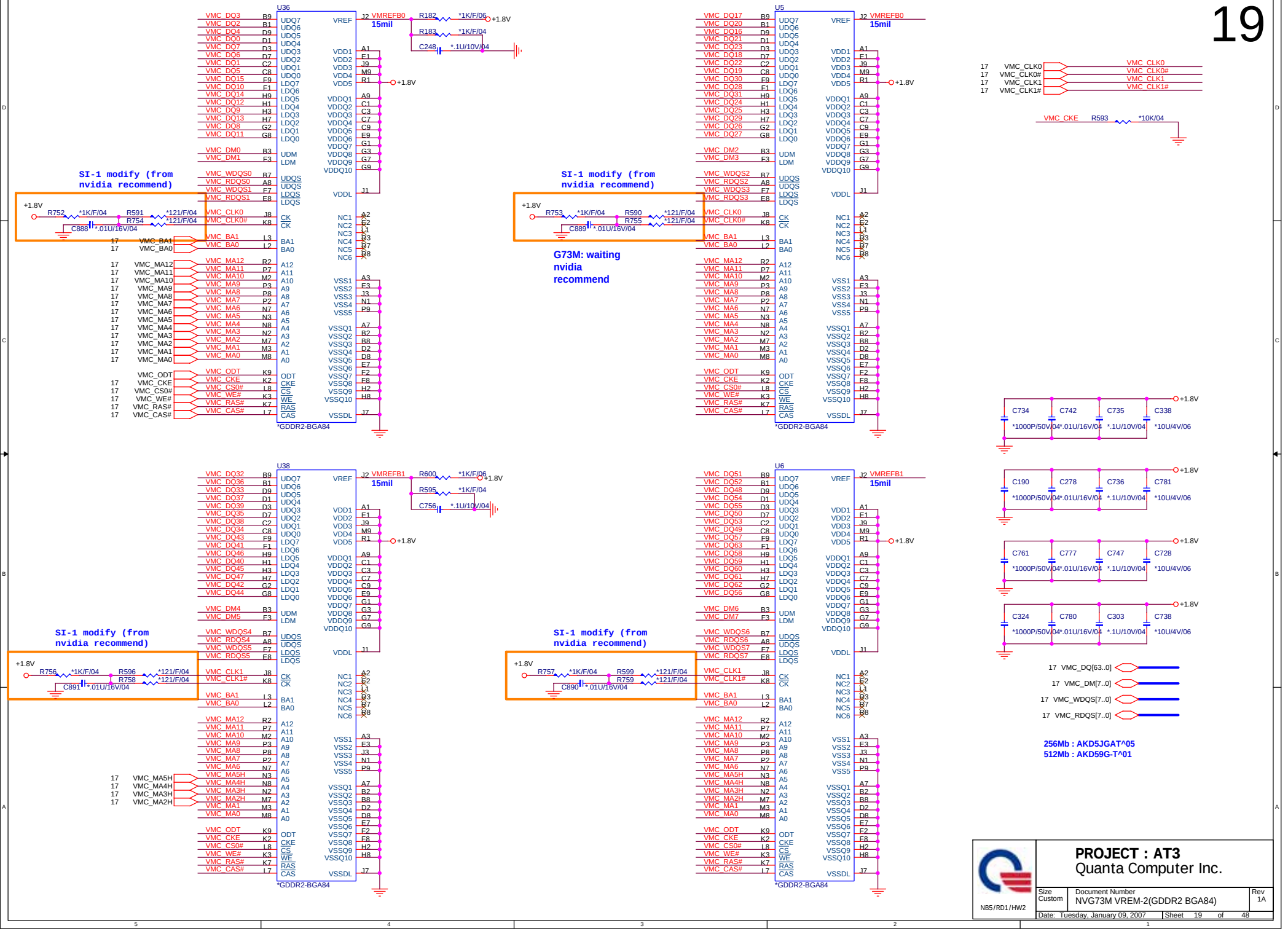


PROJECT : AT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NVG73M VRAN-1(GDDR2 BGA84)	1A

NB5/RD1/HW2

Date: Tuesday, January 09, 2007 Sheet 18 of 48



PROJECT : AT3	
Quanta Computer Inc.	
NB5/RD1/HW2	Size: Custom; Document Number: NVG73M VREM-2(GDDR2 BGA84); Rev: 1A
	Date: Tuesday, January 09, 2007; Sheet 19 of 48

U37F

*U_GPU_G3

U37A

PCIE

*U_GPU_G3

500mA

1500mA

180mA

20mA

PLACE NEAR GPU

G8X Total power consumption
1.NVDD CORE POWER 1.2 - 1.0 -- 11.01A
2.PCIE VGA1.2V -- 1.75A
3.FBVDDQ 1.8V ----- 3.12A
4.VDD I/O 3.3V ---- 0.49A
5.PLL 2.5V ---

power up sequence

I/O 3.3V
NVCORE
1.8VFBDDQ
1.2V
2.5V

For 3.3V swing, we can remove R97, R104 and R98 and replace R? with 0 Ohm resistor.

SI-1 modify (change part number)

SI-2 modify for Nvidia requests del R823,R824

*TC7SH08FU

*CH501H-40PT L-F

PROJECT : AT3	
Quanta Computer Inc.	
NB5/RD1/HW2	
Size: Custom	Document Number: NVG73M (PCIE I/F)
Rev: 1A	
Date: Tuesday, January 09, 2007	Sheet 20 of 48

RTC

CKL:C1/C2: 18pF -> CL:12.5pF
C1/C: 10pF -> CL Value = 8.5pF

Place near to Mini-door

add RTC Bat rechargeable circuit

20MIL 20MIL

SI-1 modified

SI-2 add for fix ESD issue

Should be 2" close ICH7

Place within 500 mils of ICH7

25mils/15mils

intel check list define to stuff 33ohm

ICH8M REV 1.0

SB Strap

ICH8-M Internal VR Enable strap (Internal VR for Vccsus1_05,VccSus1_5 and VccCL1_5)

INTVRMEN	Low = Internal VR disable High = Internal VR enable(Default)

ICH8-M LAN100_SLP Strap (Internal VR for VccLAN1_05 and VccCL1.05)

LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)

XOR Chain Entrance Strap

ICH_RSV0	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal opration(Default)
1	1	Set PCIE port config bit 1

PROJECT : AT3
Quanta Computer Inc.

Size: Custom	Document Number: ICH7-M HOST(1/4)	Rev: 1A
NB5/RD1/HW2	Date: Tuesday, January 09, 2007	Sheet 21 of 48

MINI CARD PCI-E

EXPRESS CARD (NEW CARD)

MINI CARD PCI-E

SI-2 Add for support RBSON card

PCIE-LAN

U42D

PCI-Express Direct Media Interface

SPI

USB

ICH8M REV 1.0

15/15mils

Place within 500 mils of ICH7

R379 24.9/F/06

+1.5V

DRI_IRCOMP_R

USB Connector

USB Connector

FINGERPRINT

Carama USB

Docking

BLUETOOTH

WWAN

NEW CARD

USB Connector

SI-2-1 swaped for fix dash issue

SI-1 modified from HP request

USB_RBIAS_PN

25mils/15mils

Place within 500 mils of ICH8

R632 22.6/F/06

RP61 8.2KX8

RP62 8.2KX8

RP63 8.2KX8

RP53 10P8R-10K

R676 10K/04

R426 10K/04

3VSUS

CHECK LIST suggest pull up 10k

A16 SWAP Override strap

PCI_GNT#3	Low = A16 swap override enabled High = Default

GNT3# R332 *1K

ICH8 Boot BIOS select

PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI(Default)
1	0	PCI
1	1	LPC

SPI_CS1# R337 *1K

GNT0# R331 *1K

U42B

PCI

Interrupt I/F

ICH8M REV 1.0

PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD25	INTE#,INTF#	RICOH832
REQ1# / GNT1#	AD22	INTC#,INTD#	MINI PCI for debug

U41 TC7SH08FU

C792 0.1U/16V/06

PLT_RST-R# 7,20

PLTRST# 23,32,33,35,37,39

Don't connect to PCI device / Express card

PCLK_ICH R328 *0 C484 *33P/50V

for EMI request

PROJECT : AT3
Quanta Computer Inc.

NB5/RD1/HW2

Size	Document Number	Rev
Custom	ICH7-M M PCI E(2/4)	1A

Date: Tuesday, January 09, 2007 Sheet 22 of 48

SI-2 Add for fix re-boot fail

R833 2K/F/04

U26 NL17SZ14DFT2G

C608 .1U/16V/04

44 VR_PWRGD_CK410#

VR_PWRGD_CK410

R809 100K/04

SI-1 has modified it ,please measure BOM has add(intel checklist add)

SI-1 add

PCLK_SMB R617 2.2K/06
PDAT_SMB R272 2.2K/06
PCIE_WAKE# R399 1K/06
PM_BATLOW#_R R387 8.2K/06

SMB_LINK_ALERT# R621 10K/06
SMLINK0 R619 10K/06
SMLINK1 R618 10K/06

RI# R624 8.2K/06
DNBSWON# R271 10K/06
SYS_RST#-1 R615 10K/06
SMB_ALERT# R273 10K/06

KBSMI# R281 10K/06

SI-1 modified

SWI# R280 10K/06

CLKRUN# R433 8.2K/06
SERIRQ R656 8.2K/06
SCI# R662 10K/06

PM_RSMRST# R658 10K/06

these pin if unused require 8.2k to 10k pull-up to +3v

U42C ICH8M REV 1.0

SMB: SMBCLK, SMBDATA, LINKALERT#, SMLINK0, SMLINK1

SATA GPIO: SATA0GP/GPIO21, SATA1GP/GPIO19, SATA2GP/GPIO36, SATA3GP/GPIO37

Clocks: CLK14, CLK48

SYS GPIO: RI#, SUS_STAT#/LPCPD#, SYS_RESET#, BMBUSY#/GPIO0, SMBALERT#/GPIO11, STP_PCI#/GPIO15, STP_CPU#/GPIO25, CLKRUN#/GPIO32

Power MGT: SUSCLK, SLP_S3#, SLP_S4#, SLP_S5#, S4_STATE#/GPIO26, PWROK, DPRSLPVR/GPIO16, BATLOW#, PWRBTN#, LAN_RST#, RSMRST#, CK_PWRGD, CLPWROK, SLP_M#

GPIO: WAKE#, SERIRQ, THRM#, VRMPWRGD, TP7, TACH1/GPIO1, TACH2/GPIO6, TACH3/GPIO7, GPIO8, GPIO12, TACH0/GPIO17, GPIO18, GPIO20, SCLOCK/GPIO22, QRT_STATE0/GPIO27, QRT_STATE1/GPIO28, SATACLKREQ#/GPIO35, SLOAD/GPIO38, SDATAOUT0/GPIO39, SDATAOUT1/GPIO48

Controller Link: CL_CLK0, CL_CLK1, CL_DATA0, CL_DATA1, CL_VREF0, CL_VREF1, CL_RST#

MISC: SPKR, MCH_SYNC#, TP3, MEM_LED/GPIO24, ME_EC_ALERT/GPIO10, EC_ME_ALERT/GPIO14, WOL_EN/GPIO9

BOARD_ID1, BOARD_ID0, BOARD_ID3, BOARD_ID4

14M_ICH, CLKUSB_48

SUSB# 37,48
SUSC# 37,48

SI-2 change from 100ohm to 499 ohm check list -- series 500ohm to IMVP6+

ICH_PWROK R677 *100K/04

DPRSLPVR R620 499/F DPRSLPVR 7,44

PM_BATLOW# R642 0/04 PM_BATLOW# 37

DNBSWON# C819 *.1U/16V/04 R665 *100/F/06 DNBSWON# 37

PLTRST_LAN# R666 100/F/06 LAN_REST 33,37,48 PLTRST# 22,32,33,35,37,39

PM_RSMRST# R659 100/F/06 RSMRST# 37,48

LAN_RST pin : 1.if used pci LAN please tie to PLTRST# 2.if used PHY LAN please tie to RSMRST#

CK_PWG 2

ECPWROK 7,16,37,48

SUSM# T251

CL_CLK0 7 ICH_CL_CLK1 39

CL_DATA0 7 ICH_CL_DATA1 39

CL_VREF0_SB CL_VREF1_SB

CL_RST#0 7,39

BT_OFF# 35

ME_SMC_ALERT# T250 T141 T144

R819 10K/04 3VSUS

SI-1 ADD (ww36 request)

Controller Link 1 VREF for IAMT support only

R631 3.24K/F/06 R633 453/F/04 C798 .1U/10V/04

Controller Link 0 VREF for IAMT support only

R338 3.24K/F/06 R344 453/F/04 C511 .1U/10V/04

CRB STUFF 2K%1

R657 2K/F/04 C818 .047U/10V/04

U43 TC7SH08FU

7,44 DELAY_VR_PWRGOOD

7,16,37,48 ECPWROK

R661 100K/06

ICH_PWROK R667 10K/06

No Reboot strap

HDA_SPKR	Low = Default High = No Reboot

ACZ_SPKR R411 *10K

SI-2 Change

SI-1 modify (for board ID select)

R660 *10K/06 BOARD_ID3 R760 10K/06

R652 *10K/06 BOARD_ID4 R761 10K/06

R692 *10K/06 BOARD_ID0 R693 10K/06

R688 *10K/06 BOARD_ID1 R448 10K/06

R690 *10K/06 BOARD_ID2 R689 10K/06

Board ID	15 " PAV UMA 965GM (0:0:0)	15" PRE UMA 965GM (0:0:1)	15”PAV Discrete 965PM+G86MV+128M (0:1:0)	17” PAV Discrete 965PM+G86MV+128M (0:1:1)	17” PAV Discrete 965PM+G84MV+256M (1:0:0)	17” PAV UMA 965GM (1:0:1)
ID0	R693 Stuff	R692 Stuff	R693 Stuff	R692 Stuff	R693 Stuff	R692 Stuff
ID1	R448 Stuff	R448 Stuff	R688 Stuff	R688 Stuff	R448 Stuff	R448 Stuff
ID2	R689 Stuff	R689 Stuff	R689 Stuff	R689 Stuff	R690 Stuff	R690 Stuff

NB5/RD1/HW2

PROJECT : AT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ICH7-M GPIO(3/4)	1A

Date: Tuesday, January 09, 2007 Sheet 23 of 48

1.5V_A 1.5A
1.5V_B 675mA
VCC1.05 1.13A

V5REF 1mA
V5REF_SUS 1mA
VCCSATAPLL 47mA
SI-2 modified (remove R374)
VCCUSBPLL 10mA
VCCGLAN3.3 1mA
VCCGLLAN_PLL --23mA
VCCGLAN1.5 80mA
VCCGLAN3.3 18mA
VCCDMIPLL 23mA
VCC_DMI 50mA
VCPU_IO 1mA
VCC3.3 278mA
VCCHDA 32mA
VCC_SUSHDA 32mA
VCC_SUS3.3 177mA
VCCL3.3 18mA - 64mA (S3)

Can be connect to +3V_S5 or +1.5V_S5

Can be connect to +3V or +1.5V

ICH8M REV 1.0

PROJECT : AT3
Quanta Computer Inc.
NB5/RD1/HW2
Size Custom
Document Number ICH7-M POWER(4/4)
Rev 1A
Date: Tuesday, January 09, 2007
Sheet 24 of 48

CRT PORT

25

5V_CRT2 C7 .1U/10V/04

+5V F1 40 mils +5VCRT 40 MIL

FUSE1A6V_POLY SSM14 spec is 40V 1A

SI-1 modified for fix CRT rise time issue

CRT_R_1 L60 BK1608HS470/06 CRT_R1

CRT_G_1 L59 BK1608HS470/06 CRT_G1

CRT_B_1 L58 BK1608HS470/06 CRT_B1

R496 150/F/04 R495 150/F/04 R492 150/F/04

C649 C647 C645 5.6P/06

C646 C648 C650 5.6P/06

EMI

close conn within 600mils

CN14 070546FR015S202CR

+3V

D30 *BAV99W CRT_R1

D27 *BAV99W CRT_G1

D26 *BAV99W CRT_B1

D23 *BAV99W DDCCLK2

D24 *BAV99W CRTVSYNC

D25 *BAV99W CRTHSYNC

D29 *BAV99W DDCDAT2

+5V C27 .1U/10V/04 U30 AHCT1G125DCH

7,15 VSYNC_COM VSYNC1 PR_VSYNC 38

U29 AHCT1G125DCH

7,15 HSYNC_COM HSYNC1 PR_HSYNC 38

R5 0/04 DDCCLK2

R491 39/04 CRTVSYNC

R490 39/04 CRTHSYNC

R7 0/04 DDCDAT2

C8 *470P/50V/04 C14 *47P/50V/06 C15 *47P/50V/06 C18 *470P/50V/04

+3V R12 2.2K/04 7,15 DDCCLK DDCCLK Q2 2N7002E DDCCLK2 38

DDCCLK2

+3V R10 2.2K/04 7,15 DDCDATA DDCDATA Q1 2N7002E DDCDAT2 DDCDAT2 38

38 PR_RED

38 PR_GEN

38 PR_BLU

38 PR_INSERT#

R4 2.2K/04 R494 2.2K/04

+5VCRT CH501H-40PT L-F D22 +5V_CRT2

CRT SWITCH

SI-1 modified for fix CRT rise time issue

U51

PR_RED CRT_R_1 PR_GEN CRT_G_1 PR_BLU CRT_B_1

IA0 IA1 IB0 IB1 IC0 IC1 ID0 ID1 SEL /E

YA YB YC YD

VCC GND

74CBT3257

CRT_R CRT_G CRT_B

CRT_R 7,15 CRT_G 7,15 CRT_B 7,15

+5V_SW R834 0/06 +5V

C937 0.1uF/10V/04

EMI

R835 10K/F/04

inputs		function
/E	SET	
L	L	Y - port 0
L	H	Y - port 1
H	X	Disconnect

38 S-CVBS-DO

38 S-YD-DO

38 S-CD-DO

filter for HDTV

C870 8.2P/50V/06

C871 8.2P/50V/06

C872 8.2P/50V/06

7,15 S-CD1 S-CD

7,15 S-YD1 S-YD

7,15 S-CVBS1 S-CVBS

L1 0.56uH/08 TV_CHROMA

L3 0.56uH/08 TV_LUMA

L2 0.56uH/08 TV_COMP

SI-1 MODIFY

R1 150/F/04 R489 150/F/04 R486 150/F/04

C642 82P/04 C643 82P/04 C641 82P/04

C640 82P/X7R/04 C2 82P/X7R/04 C1 82P/X7R/04

TV_OUT

CN13

CHROMA LUMA GND GND SHIELD COMP SHIELD

SUY-030005FR007S102FU

+3V

TV_CHROMA D19 *BAV99W

TV_LUMA D21 *BAV99W

TV_COMP D20 *BAV99W

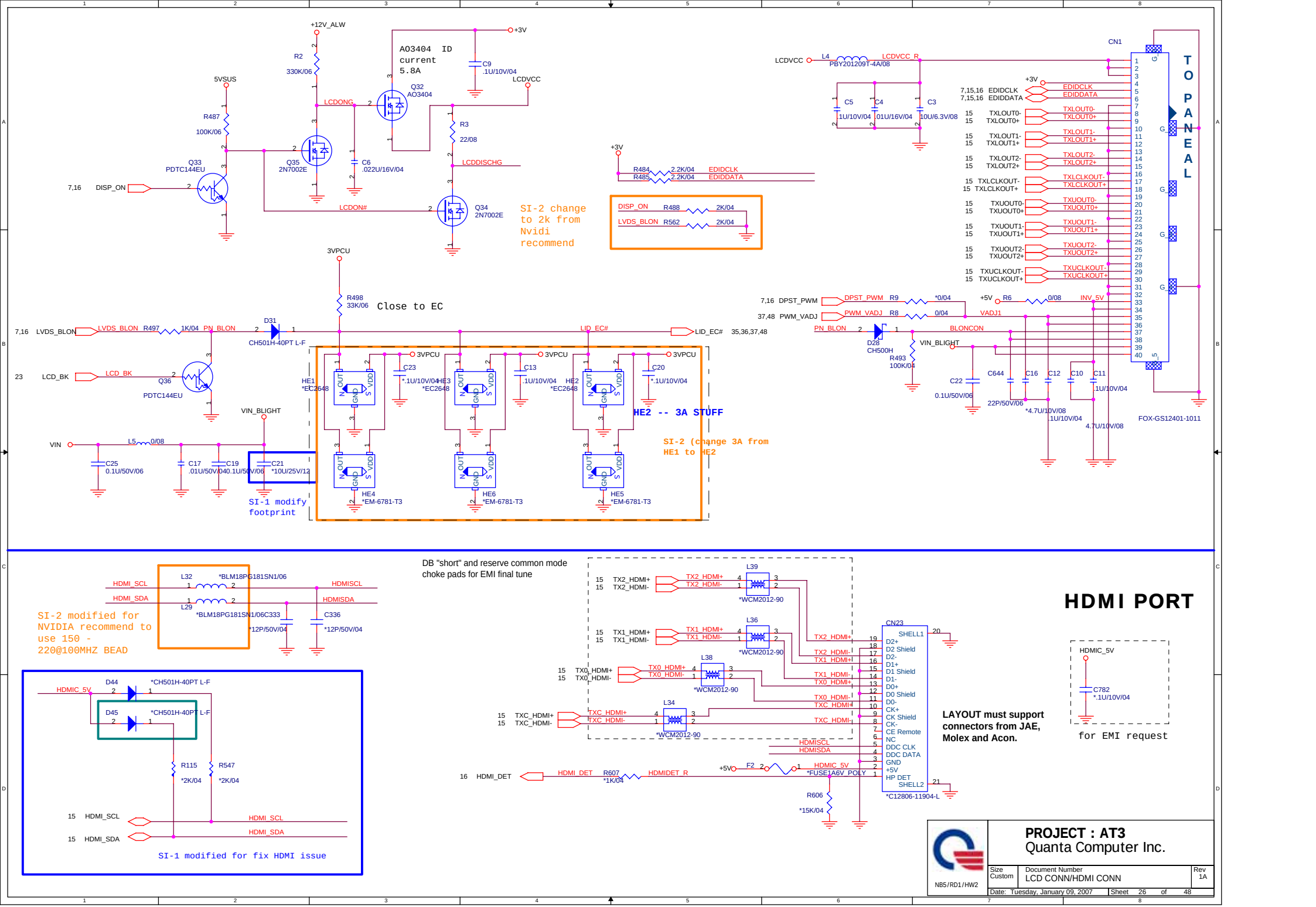
NB5/RD1/HW2

PROJECT : AT3

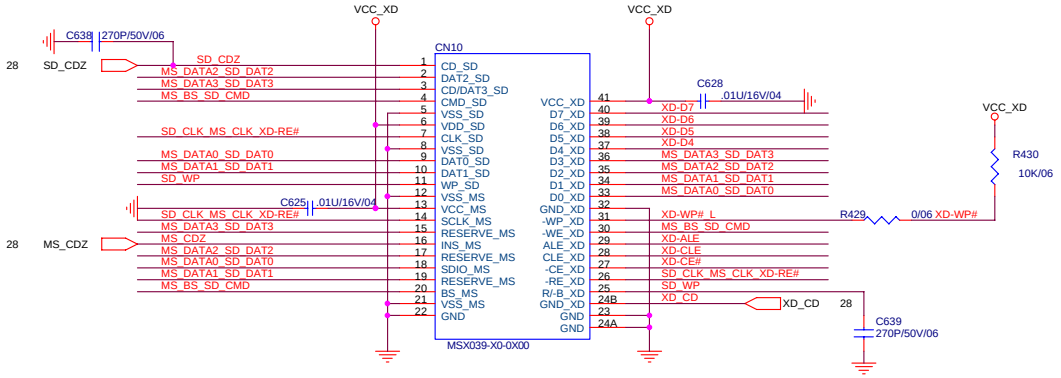
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CRT/TV_OUT	1A

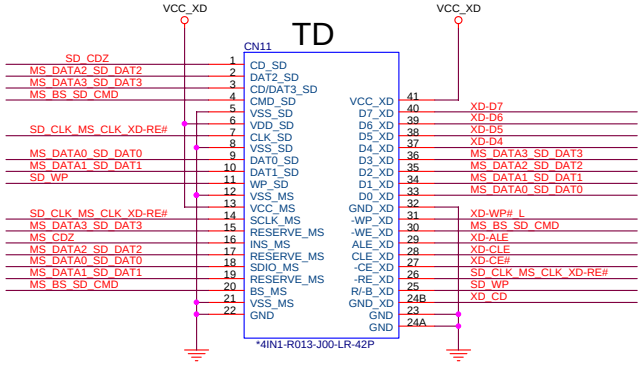
Date: Tuesday, January 09, 2007 Sheet 25 of 48


+12V_ALW
R2
330K/06
AO3404 ID current 5.8A
+3V
C9 .1U/10V/04
LCDVCC
5VSUS
Q32 AO3404
LCDONG
R487
100K/06
R3
22/08
LCDDISCHG
Q33 PDTC144EU
Q35 2N7002E
C6 .022U/16V/04
7,16 DISP_ON
LCDON#
Q34 2N7002E
SI-2 change to 2k from Nvidi recommend
R484 2.2K/04 EDIDCLK
R485 2.2K/04 EDIDDATA
DISP_ON R488 2K/04
LVDS_BLON R562 2K/04
LCDVCC L4 PBY201209T-4A/08 LCDVCC_R
C5 1U/10V/04
C4 01U/16V/04
C3 10U/6.3V/08
CN1
TO PANEL
7,15,16 EDIDCLK
7,15,16 EDIDDATA
15 TXLOUT0-
15 TXLOUT0+
15 TXLOUT1-
15 TXLOUT1+
15 TXLOUT2-
15 TXLOUT2+
15 TXLCLKOUT-
15 TXLCLKOUT+
15 TXUOUT0-
15 TXUOUT0+
15 TXUOUT1-
15 TXUOUT1+
15 TXUOUT2-
15 TXUOUT2+
15 TXUCLKOUT-
15 TXUCLKOUT+
3VPCU
R498 33K/06
Close to EC
7,16 LVDS_BLON
LVDS_BLON R497 1K/04 PN_BLON
D31 CH501H-40PT L-F
LID_EC#
LID_EC# 35,36,37,48
23 LCD_BK
LCD_BK Q36 PDTC144EU
VIN_BLIGHT
VIN
L5 0/08
C25 0.1U/50V/06
C17 .01U/50V/04
C19 0.1U/50V/06
C21 *10U/25V/12
HE1 *EC2648
HE2 *EC2648
HE3 *EC2648
C23 *.1U/10V/04
C13 .1U/10V/04
C20 *.1U/10V/04
HE2 -- 3A STUFF
SI-2 (change 3A from HE1 to HE2
HE4 *EM-6781-T3
HE6 *EM-6781-T3
HE5 *EM-6781-T3
SI-1 modify footprint
7,16 DPST_PWM
DPST_PWM R9 *0/04
37,48 PWM_VADJ
PWM_VADJ R8 0/04
+5V R6 0/08 INV_5V
VADJ1
PN_BLON
D28 CH500H
R493 100K/04
BLONCON
C22 0.1U/50V/06
C644 22P/50V/06
C16 *4.7U/10V/08
C12 .1U/10V/04
C10
C11 4.7U/10V/08
FOX-GS12401-1011
HDMI_SCL
HDMI_SDA
L32 *BLM18PG181SN1/06
L29 *BLM18PG181SN1/06C333
HDMISCL
HDMISDA
C336 *12P/50V/04
*12P/50V/04
SI-2 modified for NVIDIA recommend to use 150 - 220@100MHZ BEAD
DB "short" and reserve common mode choke pads for EMI final tune
L39 *WCM2012-90
L36 *WCM2012-90
L38 *WCM2012-90
L34 *WCM2012-90
15 TX2_HDMI+
15 TX2_HDMI-
15 TX1_HDMI+
15 TX1_HDMI-
15 TX0_HDMI+
15 TX0_HDMI-
15 TXC_HDMI+
15 TXC_HDMI-
CN23
SHELL1
D2+
D2 Shield
D2-
D1+
D1 Shield
D1-
D0+
D0 Shield
D0-
CK+
CK Shield
CK-
CE Remote
NC
DDC CLK
DDC DATA
GND
+5V
HP DET
SHELL2
*C12806-11904-L
HDMIC_5V
F2 *FUSE1A6V_POLY
16 HDMI_DET
HDMI_DET R607 *1K/04
HDMIDET_R
R606 *15K/04
HDMIC_5V C782 *.1U/10V/04
for EMI request
HDMI PORT
LAYOUT must support connectors from JAE, Molex and Acon.
D44 *CH501H-40PT L-F
D45 *CH501H-40PT L-F
R115 *2K/04
R547 *2K/04
15 HDMI_SCL
15 HDMI_SDA
SI-1 modified for fix HDMI issue
PROJECT : AT3
Quanta Computer Inc.
NB5/RD1/HW2
Size Custom
Document Number LCD CONN/HDMI CONN
Rev 1A
Date: Tuesday, January 09, 2007
Sheet 26 of 48

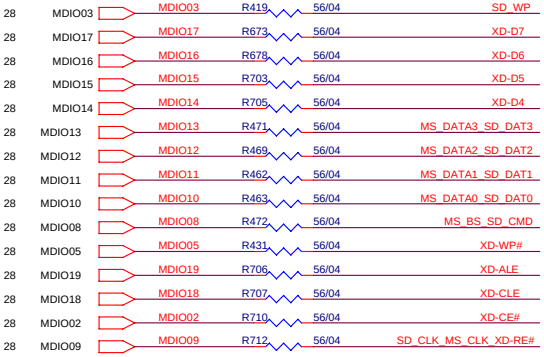
5 IN1 CARD READER
XD,MMC/SD,MS/MSP

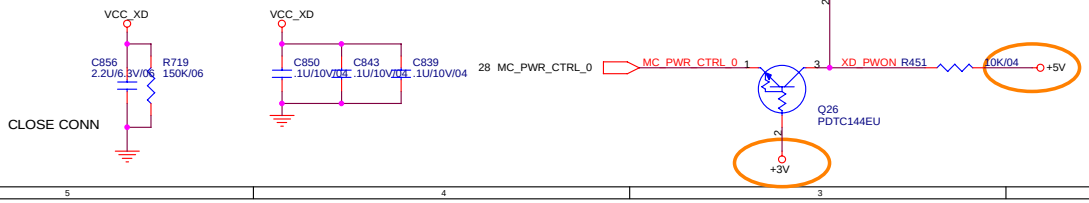


TD

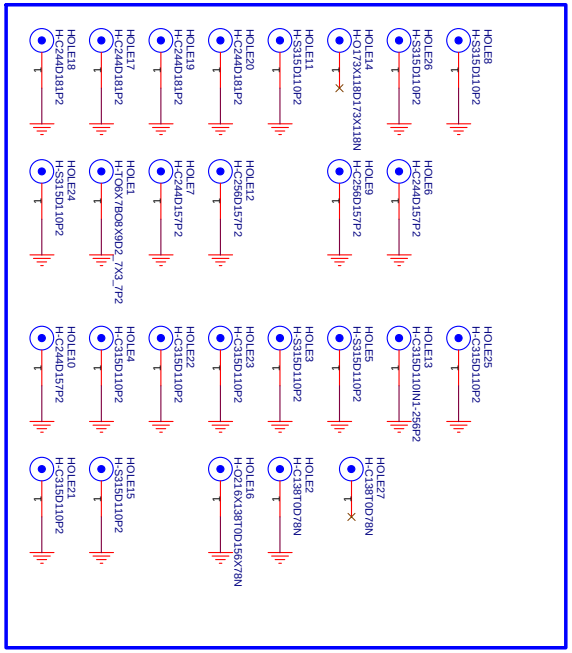


bom create 2'nd source

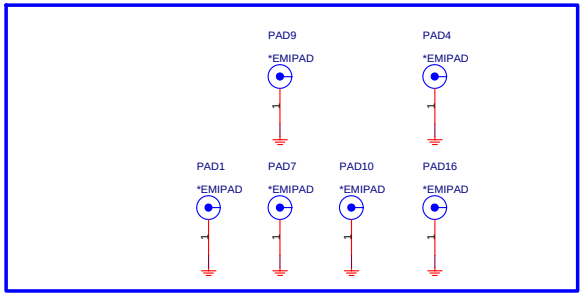


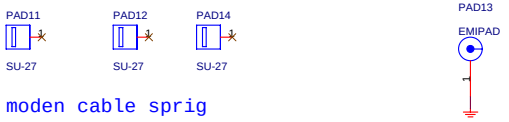


SCREW HOLE



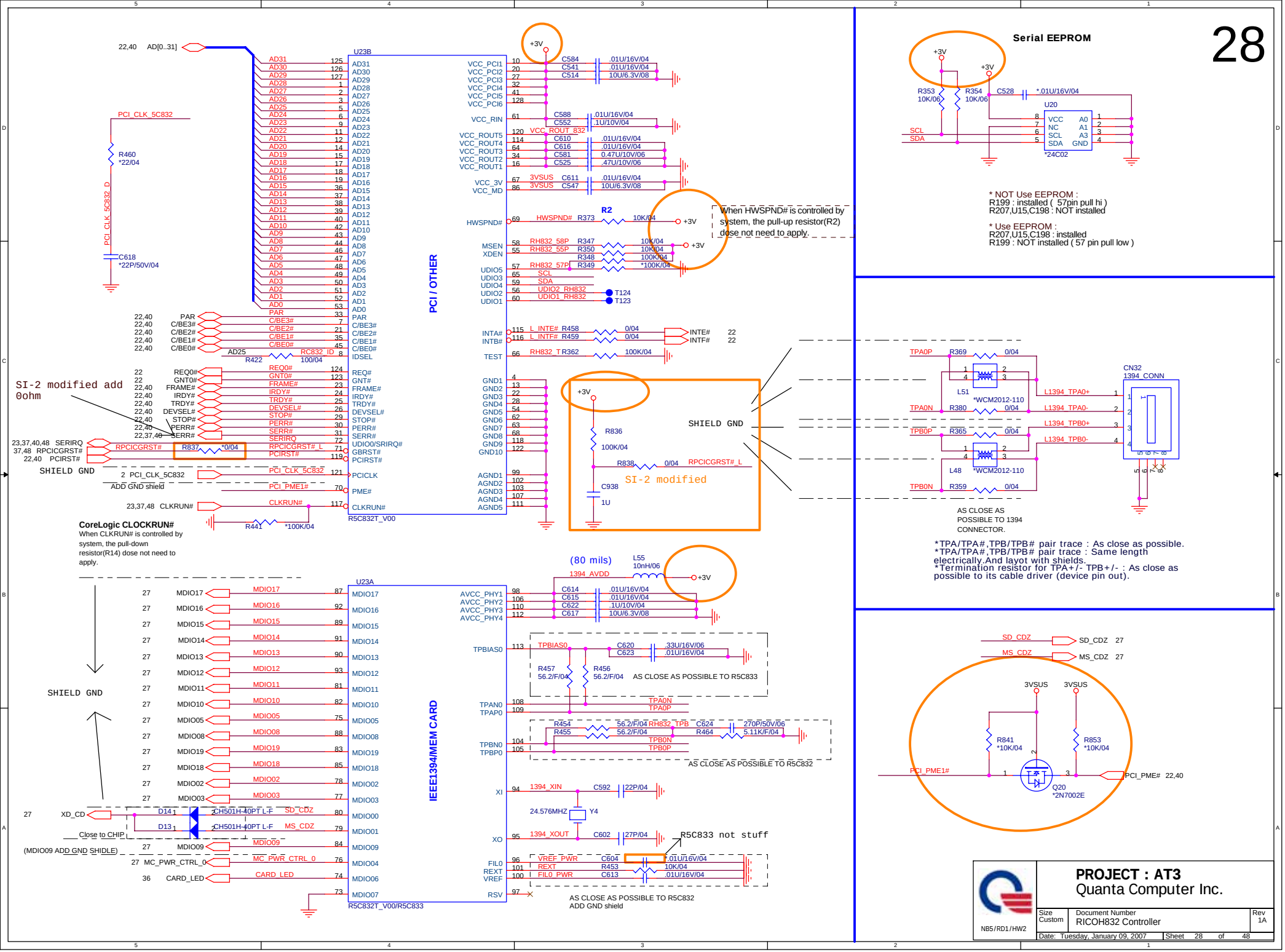
EMI PAD

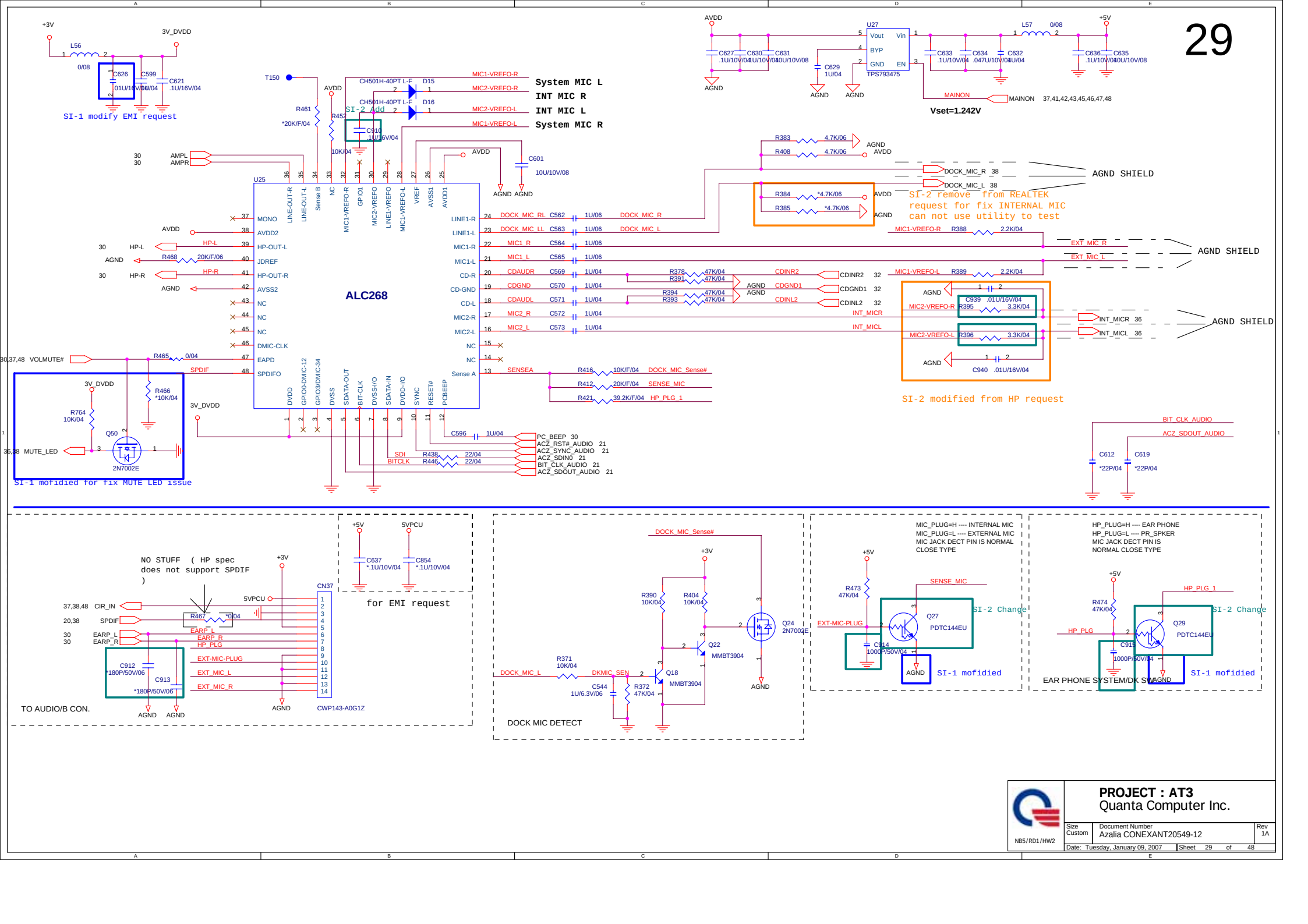




moden cable sprig

NB5/RD1/HW2	**PROJECT : AT3** Quanta Computer Inc.		
	Size: Custom	Document Number: CARD READER/HOLE	Rev: 1A
	Date: Tuesday, January 09, 2007	Sheet 27 of 48	


U23B
PCI / OTHER
SI-2 modified add 0ohm
SHIELD GND
ADD GND shield
CoreLogic CLOCKRUN#
When CLKRUN# is controlled by system, the pull-down resistor(R14) dose not need to apply.
When HWSPND# is controlled by system, the pull-up resistor(R2) dose not need to apply.
R2
SHIELD GND
SI-2 modified
AS CLOSE AS POSSIBLE TO 1394 CONNECTOR.
*TPA/TPA#,TPB/TPB# pair trace : As close as possible.
*TPA/TPA#,TPB/TPB# pair trace : Same length electrically.And layot with shields.
*Termination resistor for TPA+/- TPB+/- : As close as possible to its cable driver (device pin out).
U23A
IEEE1394/MEM CARD
(80 mils)
AS CLOSE AS POSSIBLE TO R5C833
AS CLOSE AS POSSIBLE TO R5C832
AS CLOSE AS POSSIBLE TO R5C832
ADD GND shield
R5C833 not stuff
Close to CHIP
(MDIO09 ADD GND SHIDLE)
Serial EEPROM
* NOT Use EEPROM :
R199 : installed (57pin pull hi)
R207,U15,C198 : NOT installed
* Use EEPROM :
R207,U15,C198 : installed
R199 : NOT installed (57 pin pull low)
PROJECT : AT3
Quanta Computer Inc.
RICOH832 Controller
NB5/RD1/HW2
Date: Tuesday, January 09, 2007
Sheet 28 of 48



PROJECT : AT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Azalia CONEXANT20549-12	1A
NB5/RD1/HW2	Date: Tuesday, January 09, 2007	Sheet 29 of 48

AUDIO AMPLIFIER

INT. SPEAKER

SI-2 remove r739 ,r731 from realtek request for fix BO voice when audio jack unplug

0312 Gain Table

GAIN0	GAIN1	SE/BTL	AV(INV)
0	0	0	6dB
0	1	0	10dB
1	0	0	15.6dB
1	1	0	21.6dB
x	x	1	4.1dB

SI-1 ADD EMI request

SI-1 DEL EMI request

SI-1 DEL EMI request

SI-1 ADD EMI request

PCSPK BEEP

TO CODE

TO AMP

SI-1 add R765 and remove * part

SI-1 add R807 and remove *part

(AMP BEEP ENABLE AT SYSTEM BOOT)
H=ENABLE
L=DISABLE

LINE OUT Amplifier

LINE OUT Amplifier

MAX4411 EP can NOT be connected to GND. Please leave EP pins floating.

SI-2 modified from HP recommend

QFN20-4X4-5-25P

PROJECT : AT3
Quanta Computer Inc.

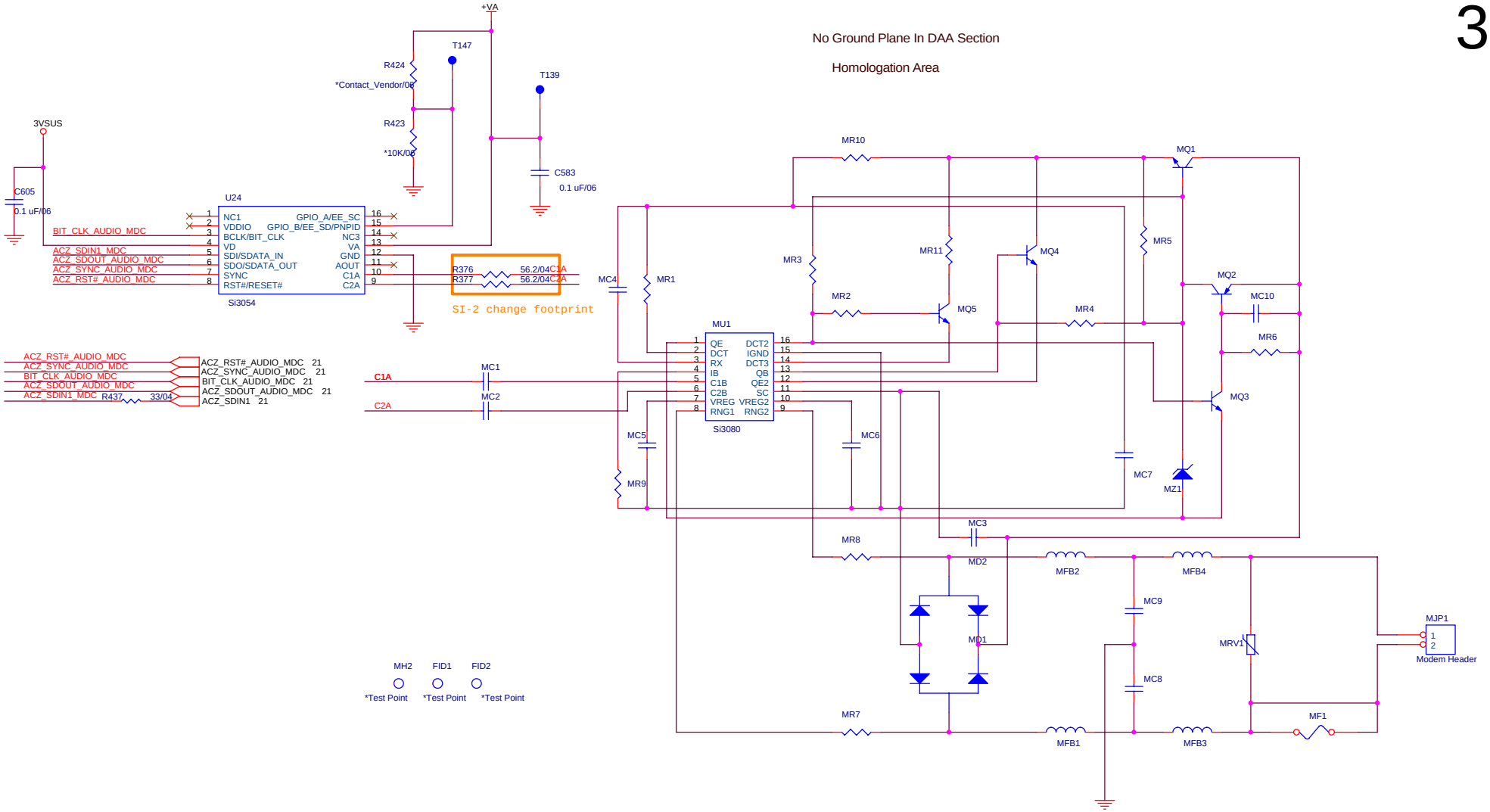
Size	Document Number	Rev
Custom	JACK/AMP_TAP0312	1A

Date: Tuesday, January 09, 2007 Sheet 30 of 48

NB5/RD1/HW2

No Ground Plane In DAA Section

Homologation Area

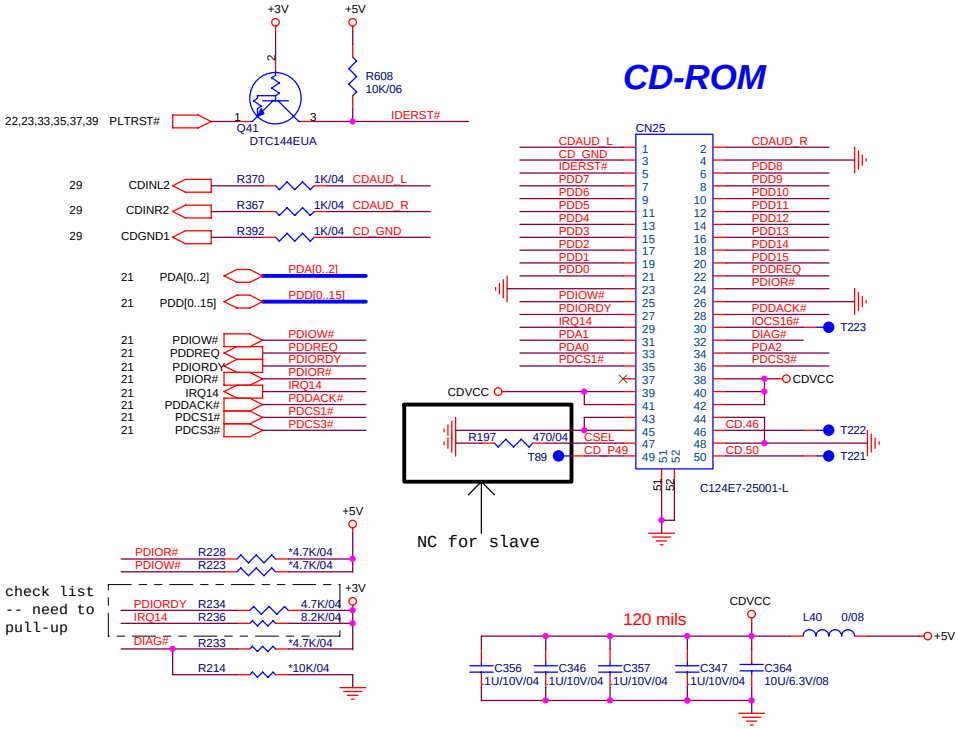


DESIGN SUBJECT TO CHANGE

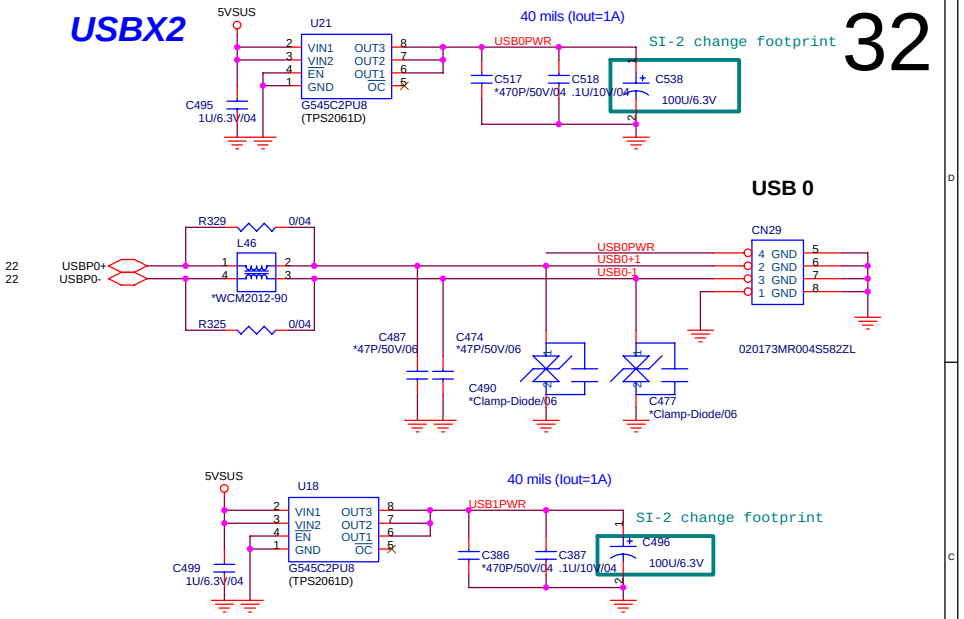
SILICON LABORATORIES CONFIDENTIAL

NB5/RD1/HW2	**PROJECT : AT3** Quanta Computer Inc.	
Size: Custom	Document Number: MODEM(DAA)	Rev: 1A
Date: Tuesday, January 09, 2007	Sheet 31 of 48	

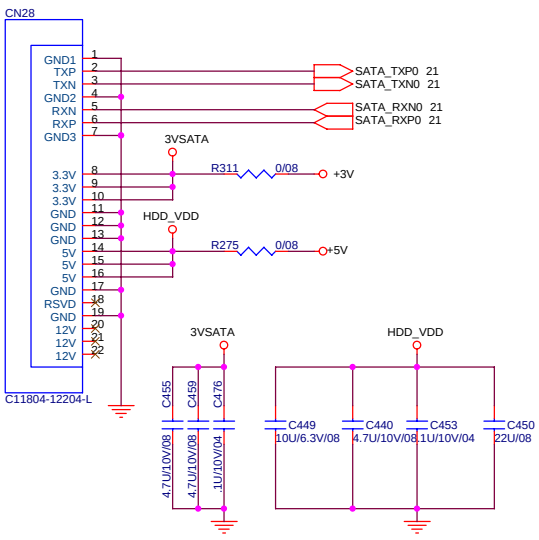
CD-ROM



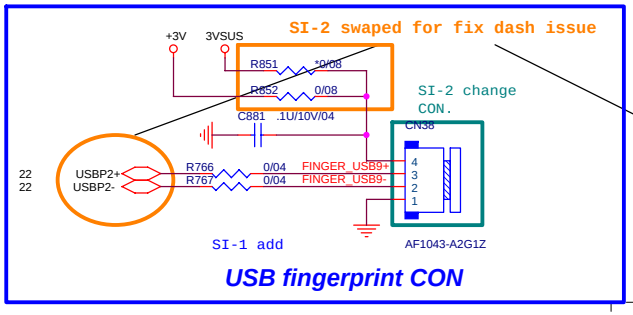
USBX2



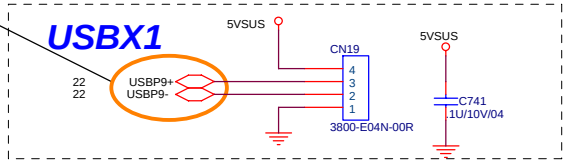
SATA_1 CONNECTOR



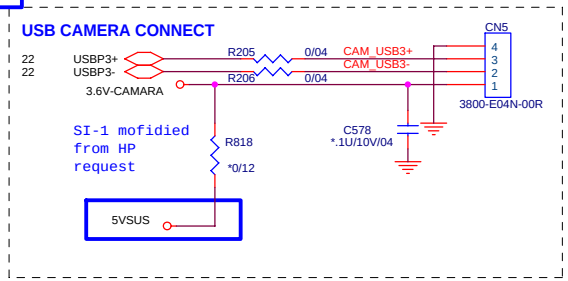
USB fingerprint CON

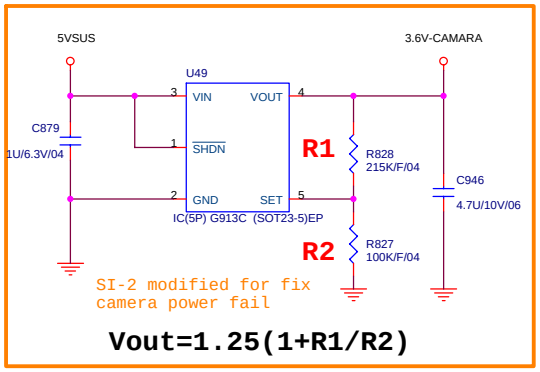


USBX1



USB CAMERA CONNECT





NB5/RD1/HW2	**PROJECT : AT3** Quanta Computer Inc.	
Size: Custom	Document Number: SATA HDD/CD-ROM/USBX3	Rev: 1A
Date: Tuesday, January 09, 2007	Sheet 32 of 48	

T : Stuffed for RTL8111B(10/100/1000)

E : Stuffed for 8101E(10/100)

giga LAN part number AJ081110006

SI-1 BOM add to fix
10/100 LAN LED issue

R21 value should be 2.49K (1%) for 8111B/8111C application. R21 should be 2.0K(1%) for 8101E application

BLOCK A is only for RTL8101E application.

Block A

RJ45

SI-1 modified to fix giga LAN LED issue

Remove R70 for 8111B and 8111C

for 93C56 used. NC if 93C46 is used.

93C46-3GR

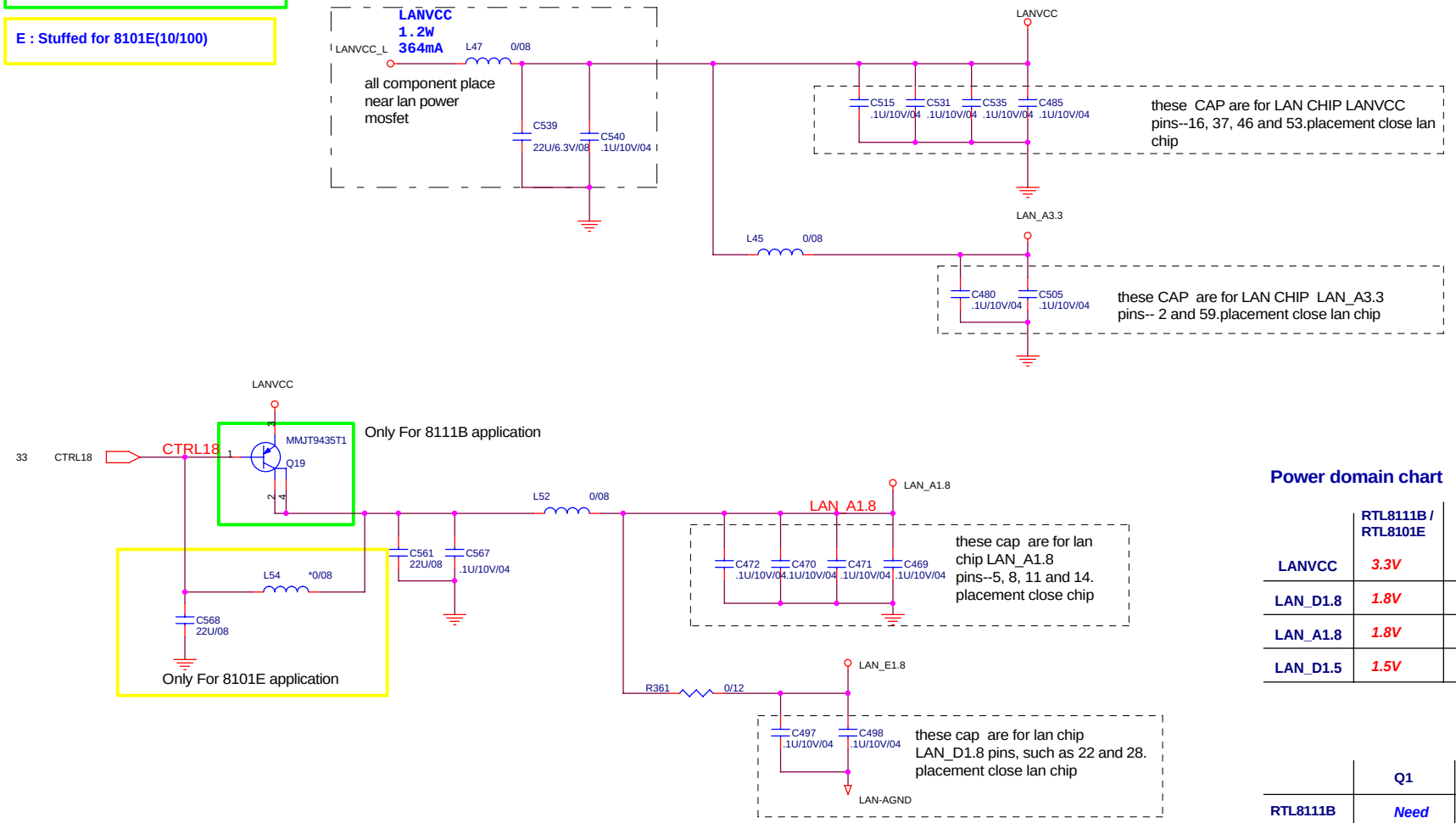
if ISOLATEB pin pull-low,the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)

NS892403:GIGABIT
NS892405:10/100

close U6

T : Stuffed for RTL8111B(10/100/1000)

E : Stuffed for 8101E(10/100)



Power domain chart

	RTL8111B / RTL8101E	
LANVCC	3.3V	
LAN_D1.8	1.8V	
LAN_A1.8	1.8V	
LAN_D1.5	1.5V	

	Q1	Q3
RTL8111B	Need	Need
RTL8101E	N/A	N/A

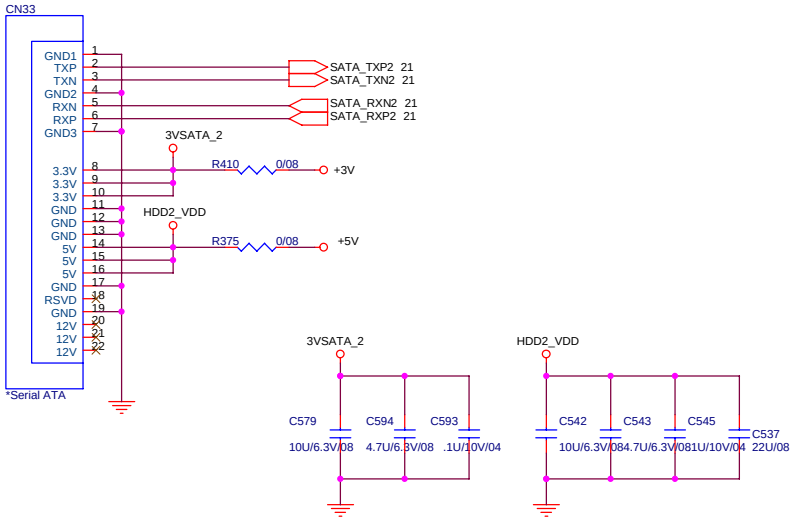
PROJECT : AT3
Quanta Computer Inc.

Size	Document Number	Rev
A3	LAN POWER	1A

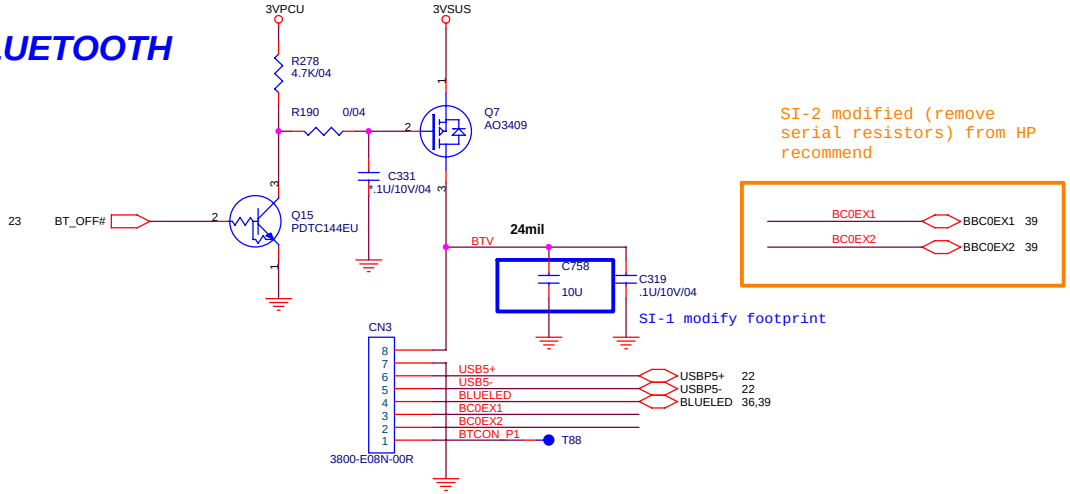
NB5/RD1/HW2

Date: Tuesday, January 09, 2007 Sheet 34 of 48

SATA_2 CONNECTOR
For 17"W Second HDD



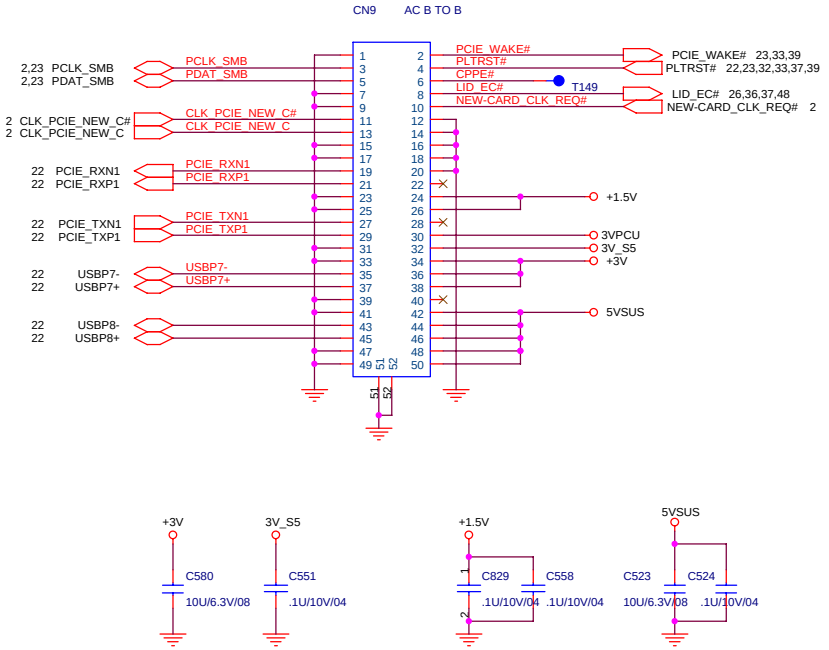
BLUETOOTH



SI-2 modified (remove serial resistors) from HP recommend

SI-1 modify footprint

NEWCARD

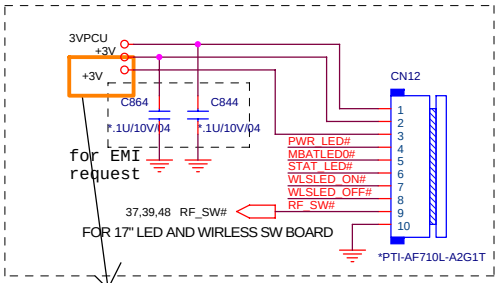


PROJECT : AT3
Quanta Computer Inc.

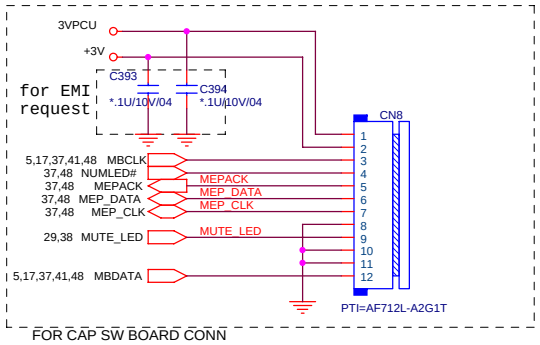
Size	Document Number	Rev
Custom	NEW CARD/BT	1A

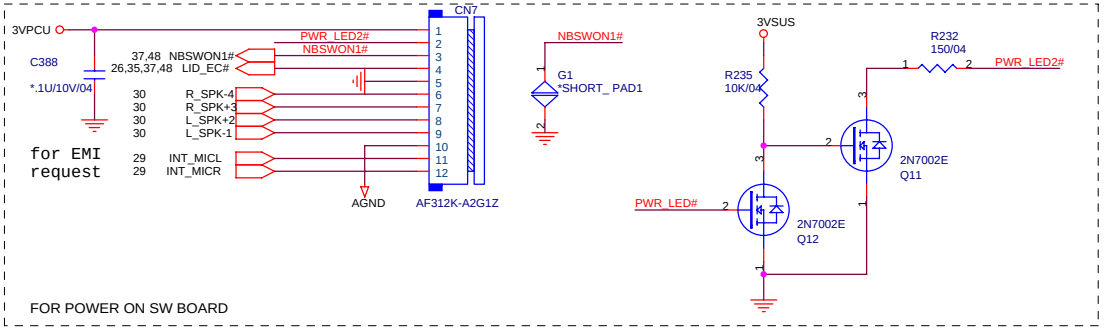
NB5/RD1/HW2

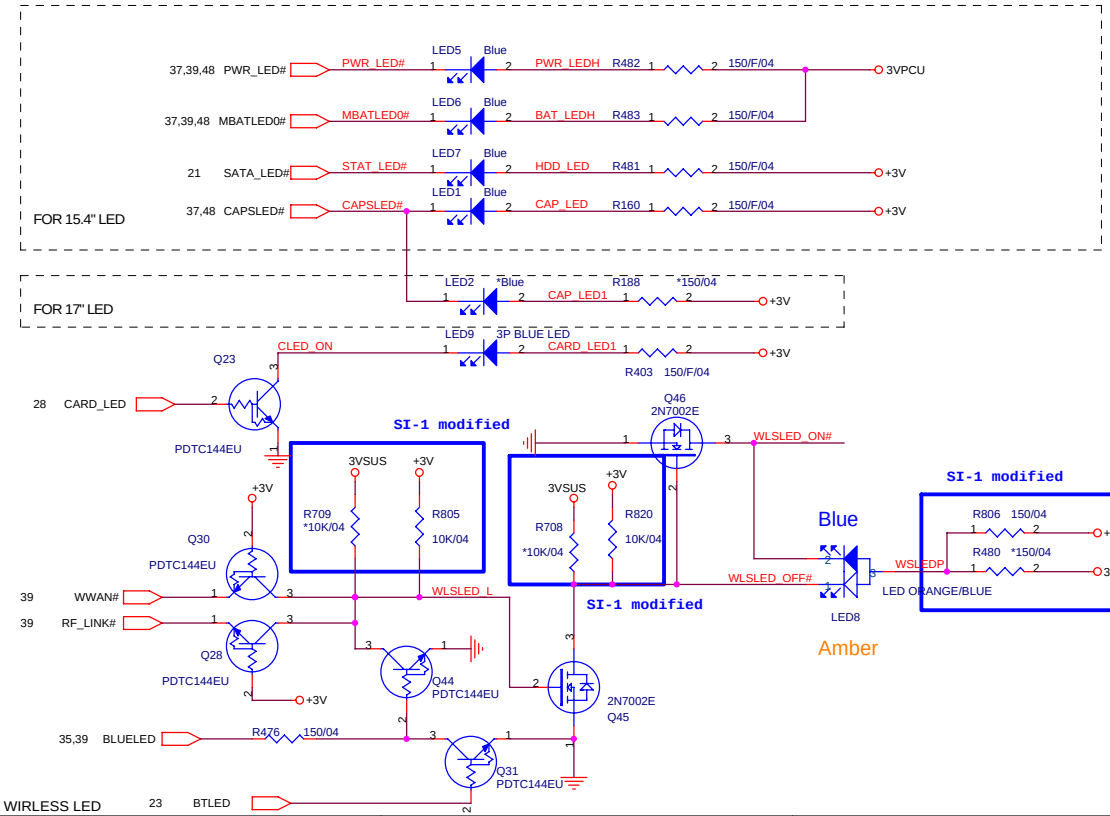
Date: Tuesday, January 09, 2007 | Sheet 35 of 48

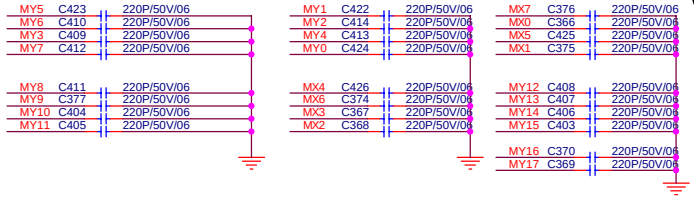


SI-2 modified for fix s3 not support wirless LED

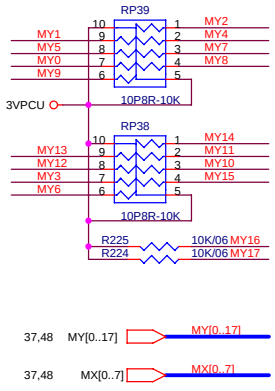


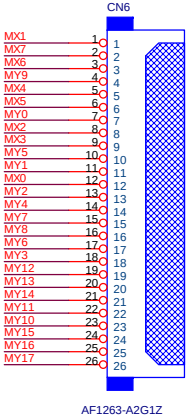


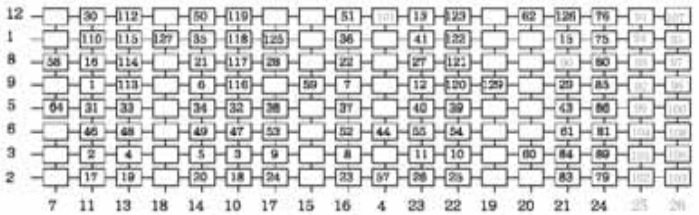




KEYBOARD PULL-UP







PROJECT : AT3	Quanta Computer Inc.
NB5/RD1/HW2	Size: Custom; Document Number: LED/KEYBOARD/SW; Rev: 1A
Date: Tuesday, January 09, 2007	Sheet 36 of 48

STRAP PIN

MY2	49	TP_SPI: Default flash access Low: Boot from SPI flash part HIGH: Boot from ISA flash part
MY3	50	TP_ISP: In System Programming Mode Low: ISP mode HIGH: Normal Mode

SI-1 DEL R209,R210,R218,R219,R220

MY2 R208 *10K/04

MY3 R212 *0/04

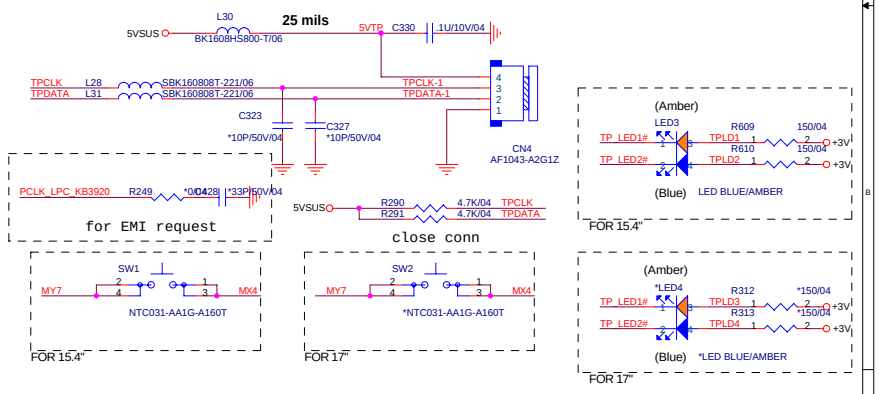
All hardware straps default internal pull-up, so don't need pull-UP outside. A TEST need try --andrew ????

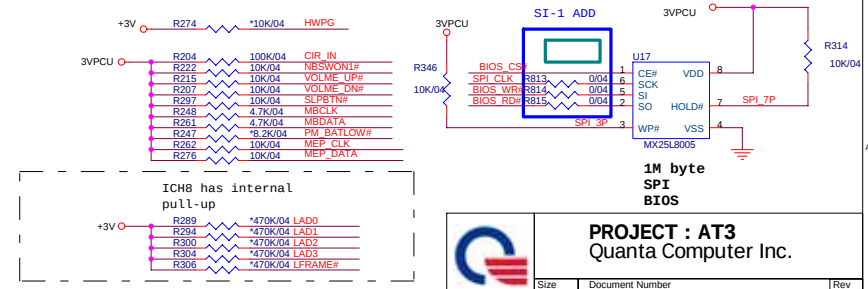
SELECT KBC TPYE

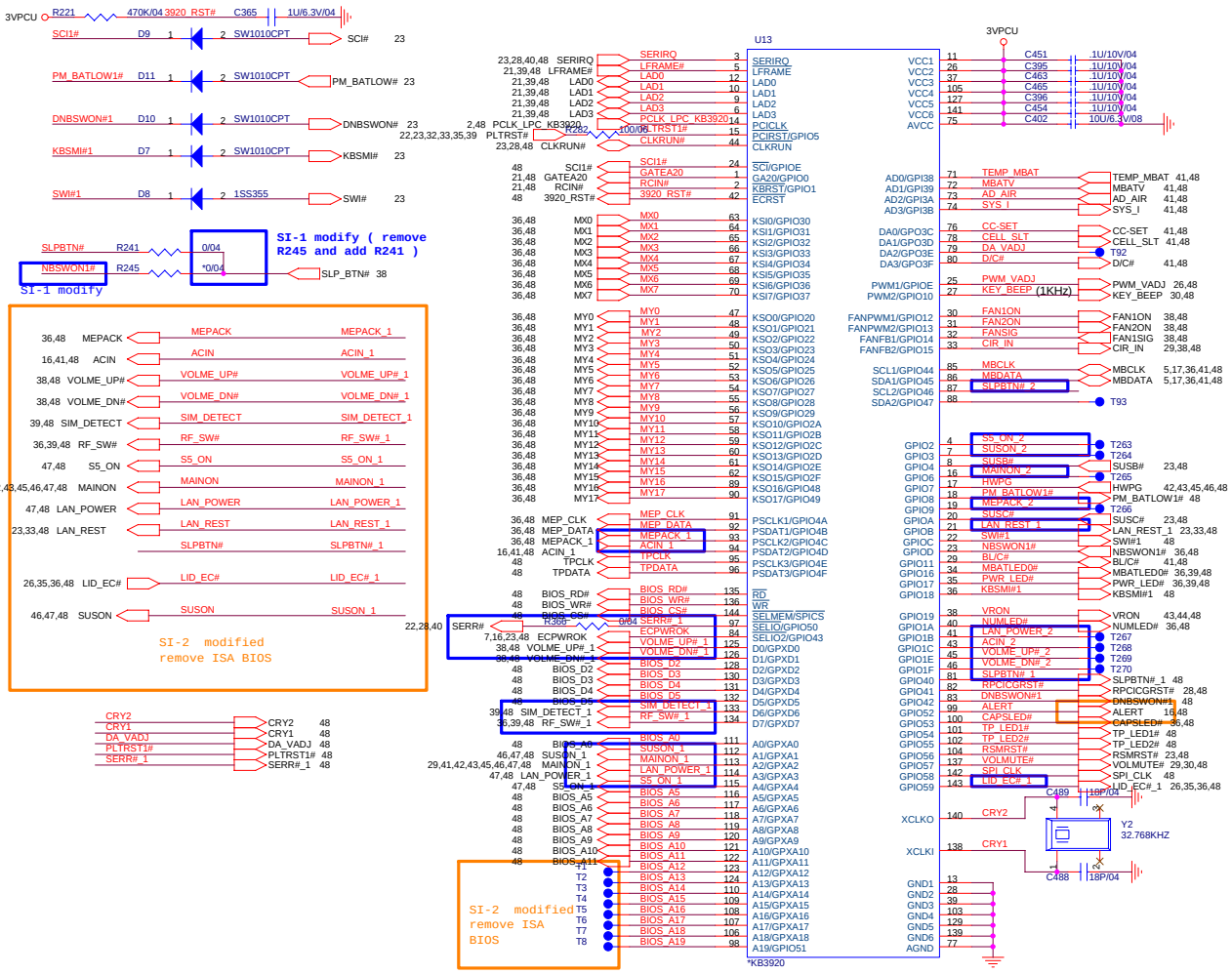
PIN NAME	USE KBC3920	USE KBC3926
MY2	R208	REMOVE R208
BIOS_A0	REMOVE R808	R808

SI-2 modified remove ISA BIOS

TOUCH PAD CONNECTOR







PROJECT :	AT3
Quanta Computer Inc.	
Size: Custom	Document Number: KB3920/ROM/TP
Rev: 1A	
Date: Tuesday, January 09, 2007	Sheet 37 of 48

NB5/RD1/HW2

CABLE DOCK

support 6A 200mils
CX000480005

SI-1 mofidied (BOM add for support docking SPIDF

+1.5V, R522 33/04, C883 .1U/10V/04, SPDDK_V, Q37 MMBT3904, SPDIF, R531 510/F/04, SPDIF_DK, R525 510/F/04, C681 68P/50V/04, SPD_DK, L68 0/06, SPDIF_DOCK

DOCK_VA, L61 FBMJ3216HS480NT/12, VA_P, C658 0.1U/50V/06, C651 0.1U/50V/06

CN18

PR_GEN, PR_RED, DDCDAT2, PR_BLU, PR_HSYNC, DDCCLK2, PR_VSYNC, R45 0/04, R38 0/04, R54 0/04, R811 0/06, R812 0/06, CRT_GDK, CRT_RDK, CRT_BDK, PR_HSYNC_D, PR_VSYNC_D, USB4-1, USB4+1

SI-1 ADD EMI request

+3V, 3VPCU, R844 100K/04, R548 *100K/04, PR_INSERT#, docking insert is HI voltage, DOCK_PRESENT, R579, DKPR# 1K/04, R573 2K/F/06, Q40 2N7002E

USBP4-, USBP4+, R528 0/04, L67 *CMM211T-900M-S, R526 0/04, USB4-1, USB4+1

PR_HSYNC_D, PR_VSYNC_D, C892 *47P/50V/06, C893 *47P/50V/06

SI-1 ADD EMI request

+5V, 5VSUS, R520 10K/04, DK_PWRON, D33 SW1010CPT, D34 SW1010CPT, PWR_ON, R527 15K/04

S0: 4V
S3: 2.5V
S4/S5: 0V
*Check voltage on DB

DOCK_MIC_R, DOCK_MIC_L, RSPK_DK, LSPK_DK, JACK_DETECT#, VOLME_DN#, CIR_IN, C673 *120P/50V/04, C677 *120P/50V/04, C674 270P/25V/04, C897 180P/50V/04, C898 180P/50V/04, C902 180P/50V/04, C903 180P/50V/04

SI-1 ADD EMI request

VIN, C894 0.1U/50V/06

SI-1 ADD EMI request

QL1122L-H212AR-7F

PR_GEN, PR_RED, PR_BLU, CRT_GDK, CRT_RDK, CRT_BDK, C918 5.6P/06, C919 5.6P/06, C920 5.6P/06, C941 5.6P/06, C942 5.6P/06, C943 5.6P/06

SI-2 modified for fix docking R.G.B signals measure fail

R56 150/F/04, R30 150/F/04, R39 150/F/04

S-YD-DO-PR, S-CD-DO-PR, S-CVBS-DO-PR, R519 *150/F/04, R517 *150/F/04, R506 *150/F/04

FAN

EXTERNAL VGA FAN RESEVRE

+5V, L72 *0/08, 20 mil, 5VFAN2, CN20, C739 *2.2U/6.3V/06, C740 *.1U/10V/04, 37,48 FAN2ON, *PTI=CWP043-A0G1T

near to connector.

FAN2 PWM CONNECTOR

CPU FAN

+5V, L73 0/08, 20 mil, D39 *SSM34PT L-F, 5VFAN1, CN22, C749 2.2U/6.3V/06, C748 1U/10V/04, 37,48 FAN1ON, PTI=CWP043-A0G1T, R594 4.7K/06, FAN1SIG, FAN1SIG 37,48

FAN1 PWM CONNECTOR

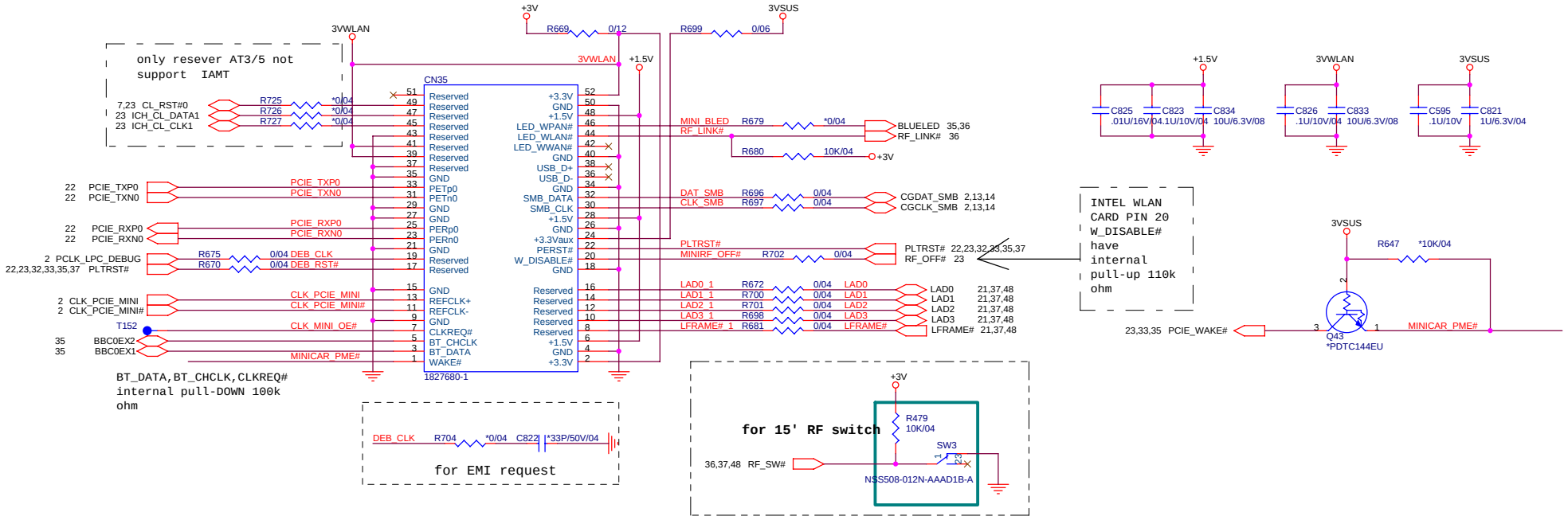
NB5/RD1/HW2

PROJECT : AT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CABLE DOCKING/FAN	1A

Date: Tuesday, January 09, 2007 Sheet 38 of 48

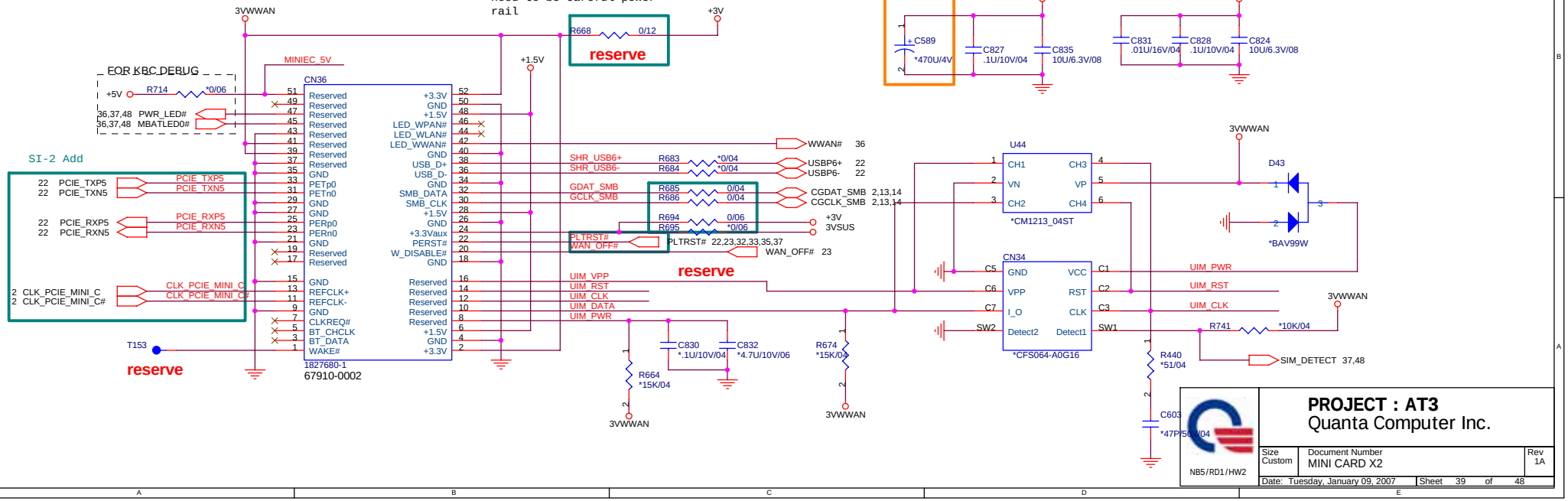
Mini PCI-E Card 1
WLAN



Mini PCI-E Card 2
WWAN(W/SIM)

WWAN -- have 2.8A 7W power consumption
power pin 24.39.41
GND pin 37,43
need to be careful power rail

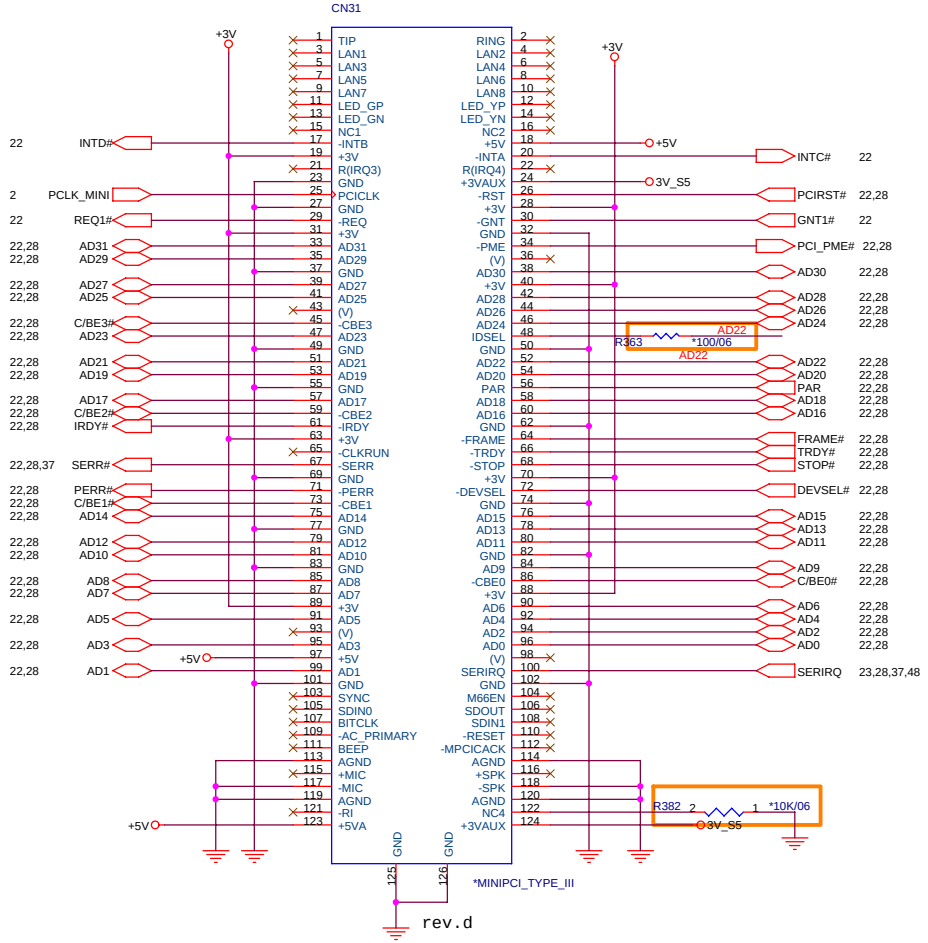
SI-2 modified
(BOM remove C589
)



	PROJECT : AT3 Quanta Computer Inc.	
Size Custom	Document Number MINI CARD X2	Rev 1A
NB5/RD1/HW2	Date: Tuesday, January 09, 2007	Sheet 39 of 48

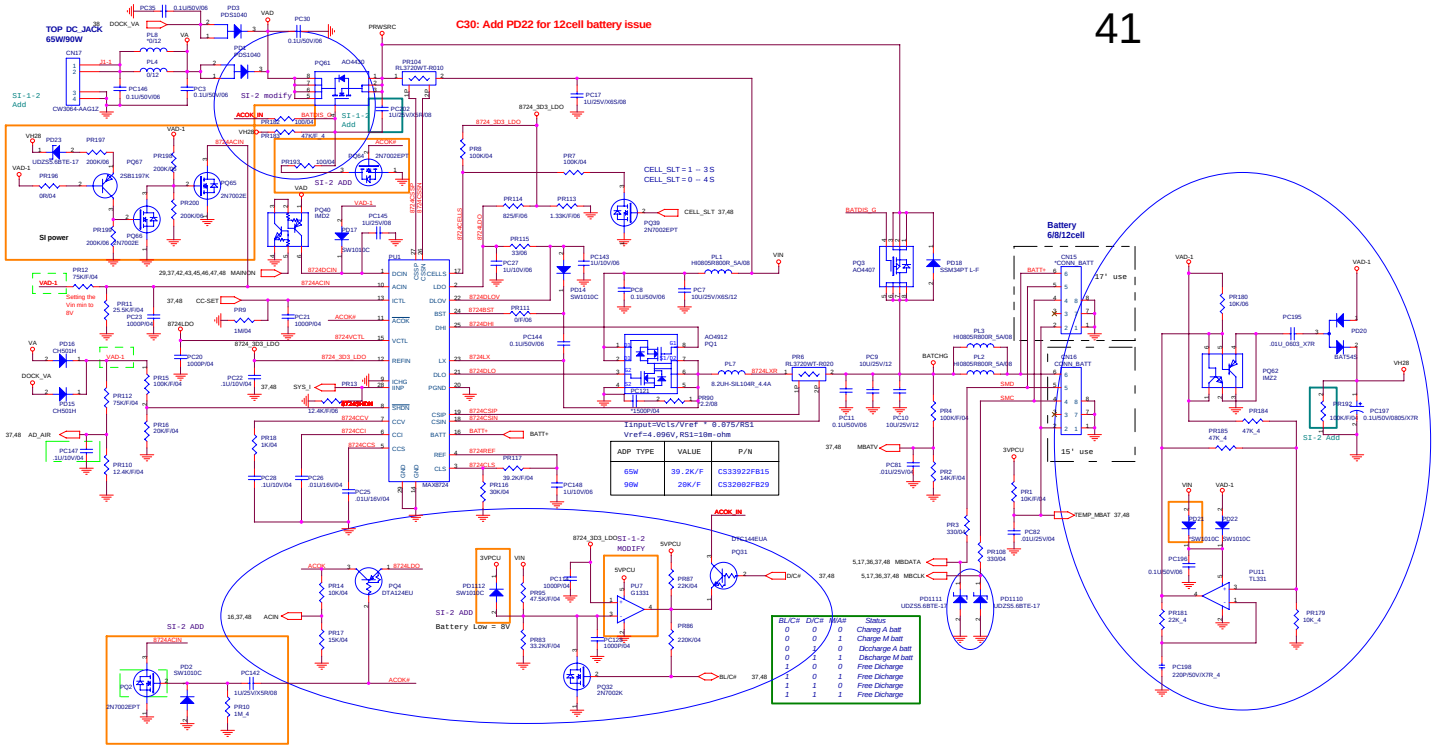
MINI PCI TYPE III SLOT

INTC#, INTD#
REQ1#/GNT1#
D_ID : AD22



PROJECT : AT3	
Quanta Computer Inc.	
Size: Custom	Document Number: MINI PCI TYPE III SLOT
Rev: 1A	
NB5/RD1/HW2	Date: Tuesday, January 09, 2007 Sheet 40 of 48

C30: Add PD22 for 12cell battery issue



ADP TYPE	VALUE	P/N
65W	39.2K/F	CS33922FB15
90W	20K/F	CS32002FB29

BLC#	D/C#	MAH	Status
0	0	0	Charg A batt
0	0	1	Charge M batt
0	1	0	Discharge A batt
0	1	1	Discharge M batt
1	0	0	Free Dicharge
1	0	1	Free Dicharge
1	1	0	Free Dicharge
1	1	1	Free Dicharge

PROJECT : AT3
Quanta Computer Inc.

NB5/R01/HW2

Size	Document Number	Rev
D	SYSTEM CHARGER(MAX8724)	1A

Date: Tuesday, January 09, 2007 Sheet 41 of 46

DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+12V_ALW

Place these CAPs close to FETs

Place these CAPs close to FETs

5 Volt +/- 5%
Countinue current:8A
Peak current:11A
OCP minimum 13A

3.3 Volt +/- 5%
Countinue current:5A
Peak current:7.5A
OCP minimum 10A

Rds(on) 13m ohm

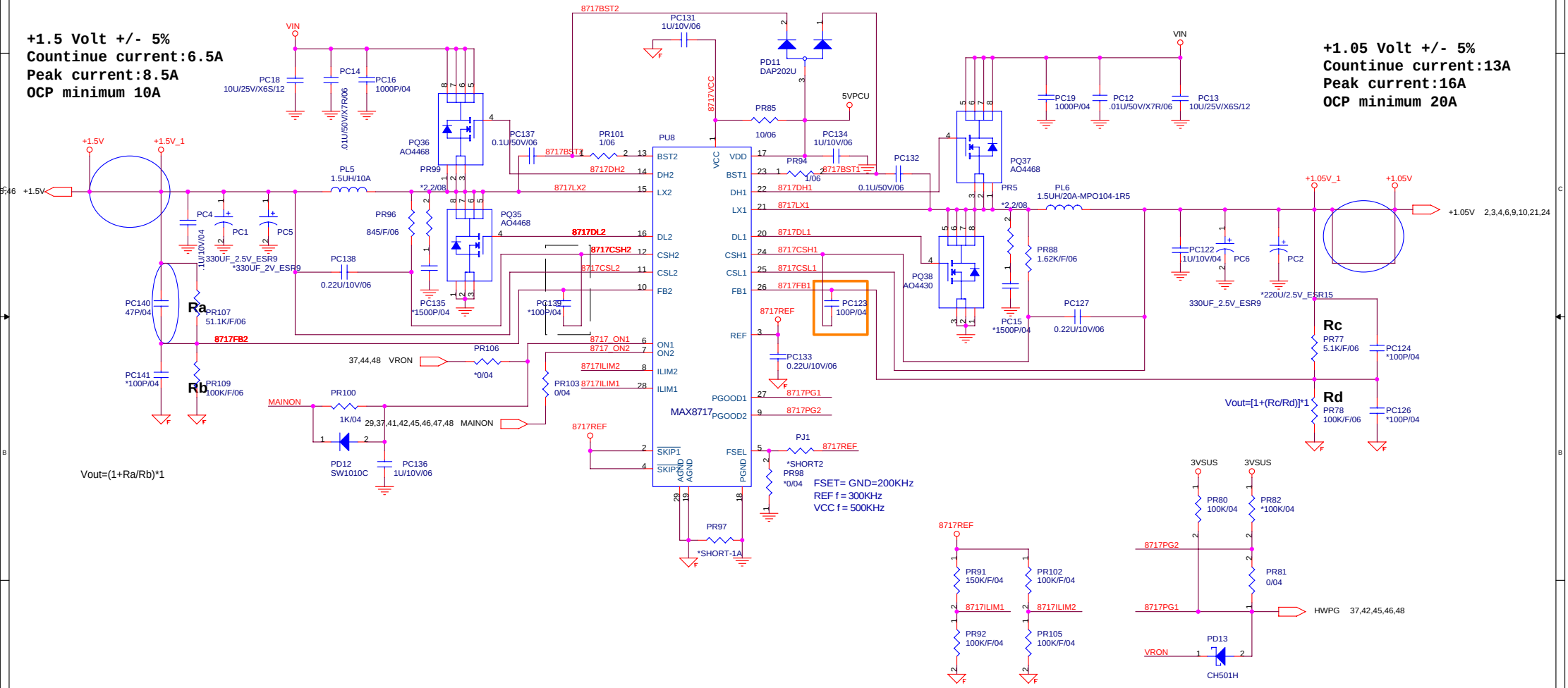
Rds(on) 15m ohm

Max Power Consumption 1.6W

For G73 Only

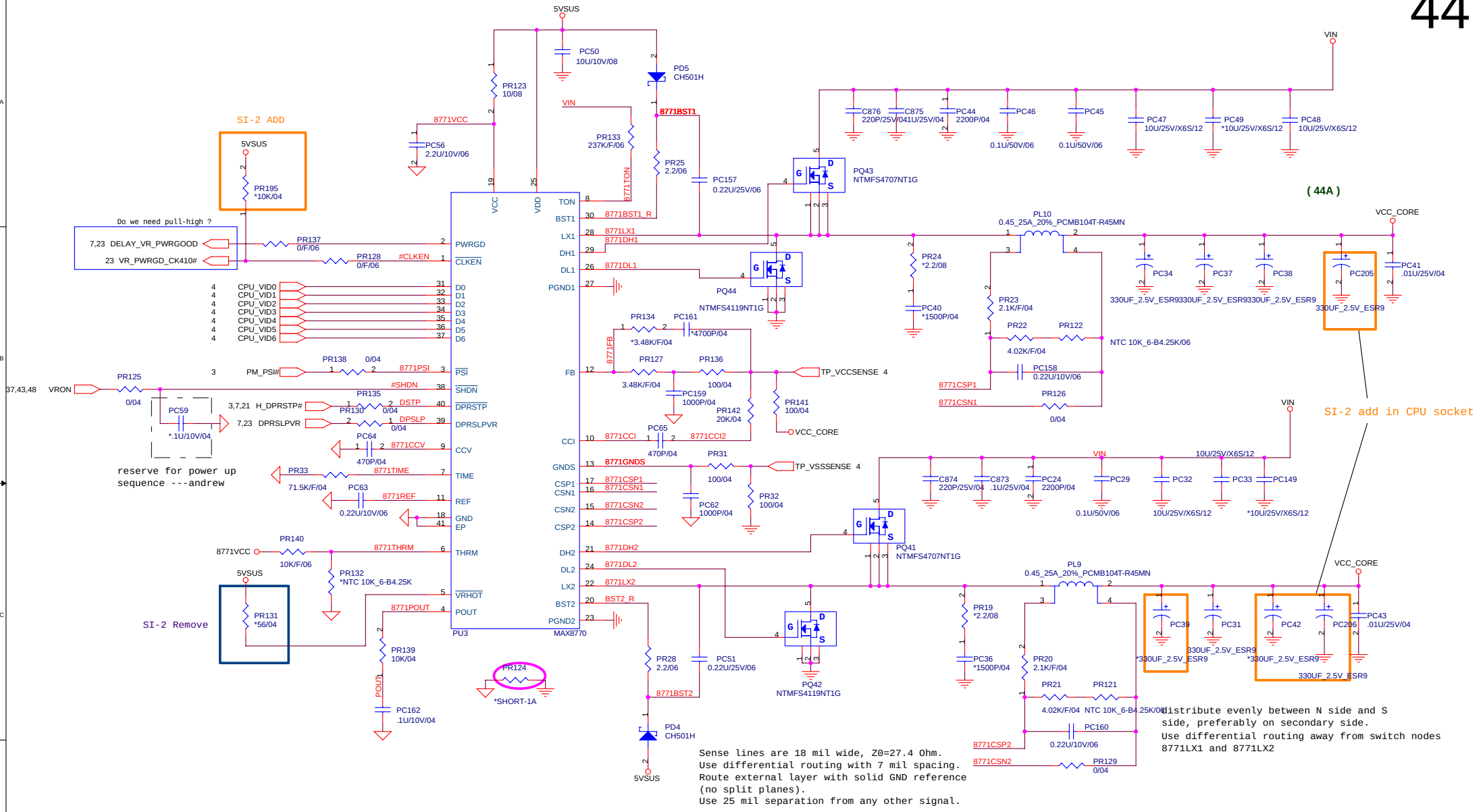
PROJECT : AT3	Quanta Computer Inc.
NB5/RD1/HW2	Size: Custom; Document Number: 3v/5v; Rev: 1A
Date: Tuesday, January 09, 2007	Sheet 42 of 48

+1.5 Volt +/- 5%
Countinue current:6.5A
Peak current:8.5A
OCP minimum 10A



+1.05 Volt +/- 5%
Countinue current:13A
Peak current:16A
OCP minimum 20A

PROJECT : AT3		
Quanta Computer Inc.		
Size: Custom	Document Number: +-1.5V &VCCP+1.05V(MAX8743)	Rev: 1A
NB5/RD1/HW2	Date: Tuesday, January 09, 2007	Sheet 43 of 48



PROJECT : AT3
Quanta Computer Inc.

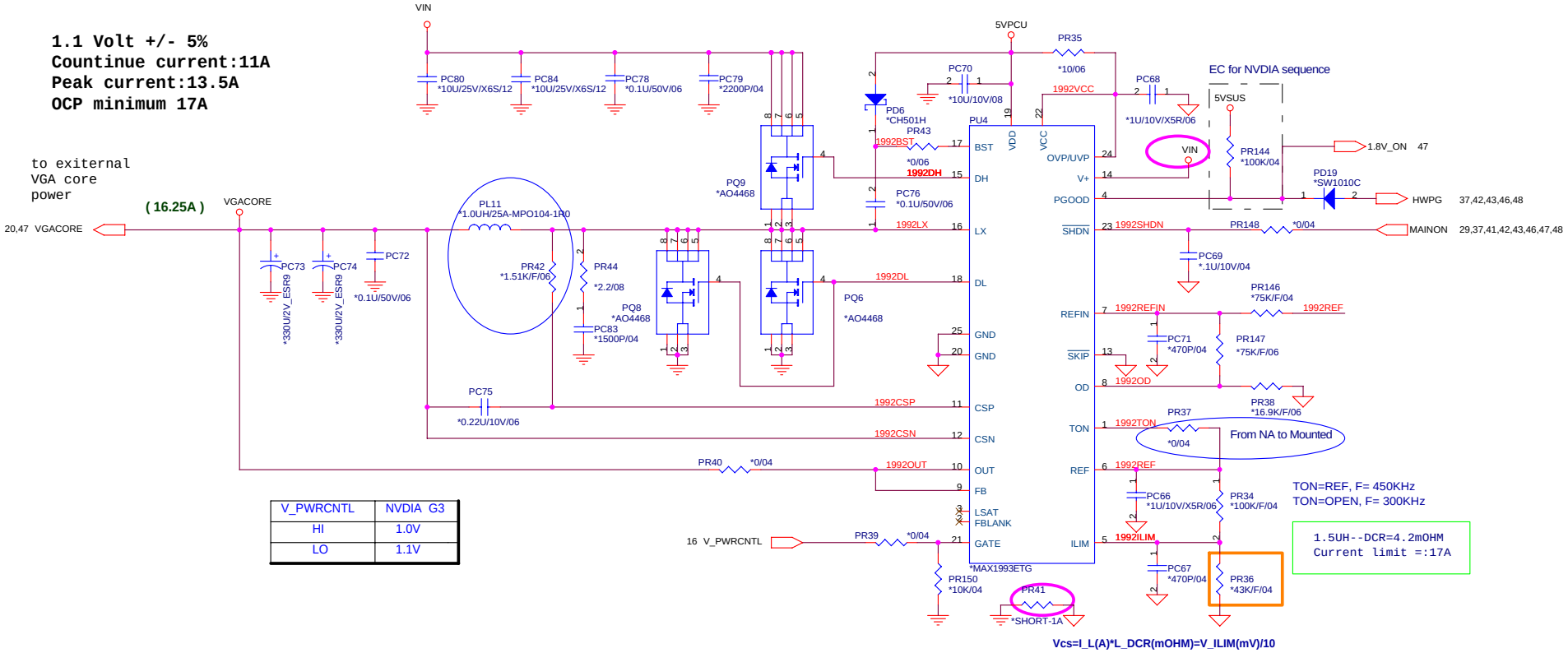
Size	Document Number	Rev
Custom	CPU_CORE(MAX8771)	1A
Date: Tuesday, January 09, 2007	Sheet 44 of 48	

NB5/RD1/HW2

1.1 Volt +/- 5%
Countinue current:11A
Peak current:13.5A
OCP minimum 17A

to exiternal
VGA core
power

(16.25A)

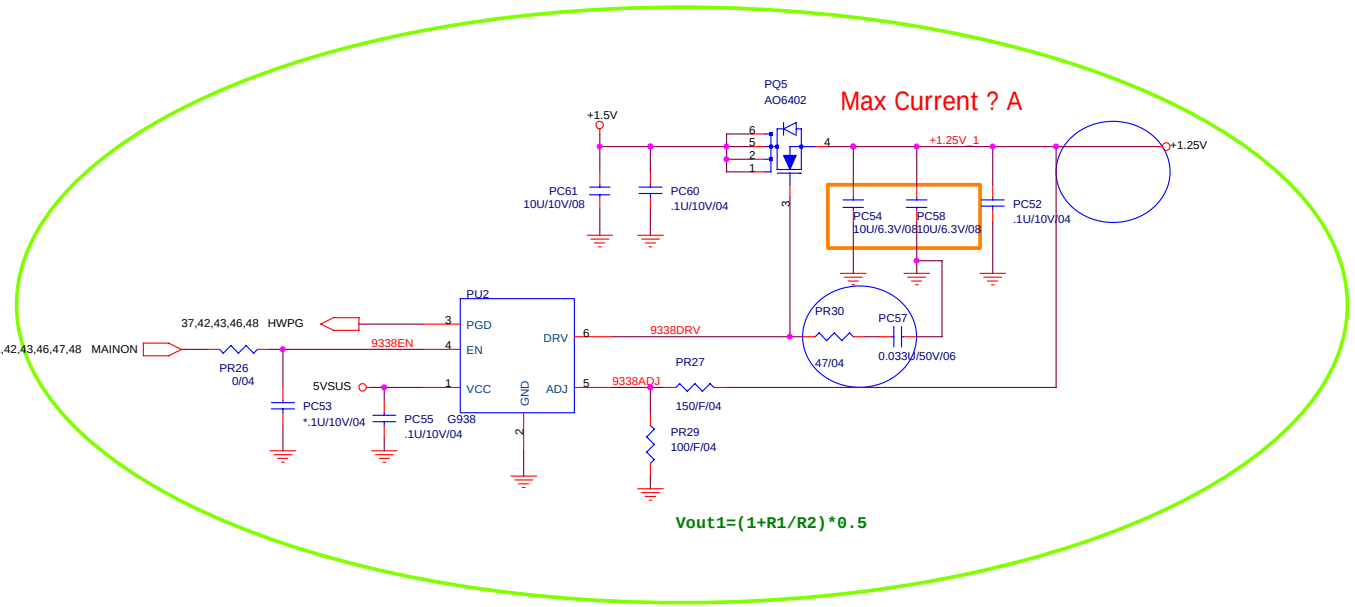


V_PWRCNTL	NVDIA G3
HI	1.0V
LO	1.1V

TON=REF, F= 450KHz
TON=OPEN, F= 300KHz

1.5UH--DCR=4.2mOHM
Current limit =:17A

Vcs=I_L(A)*L_DCR(mOHM)=V_ILIM(mV)/10

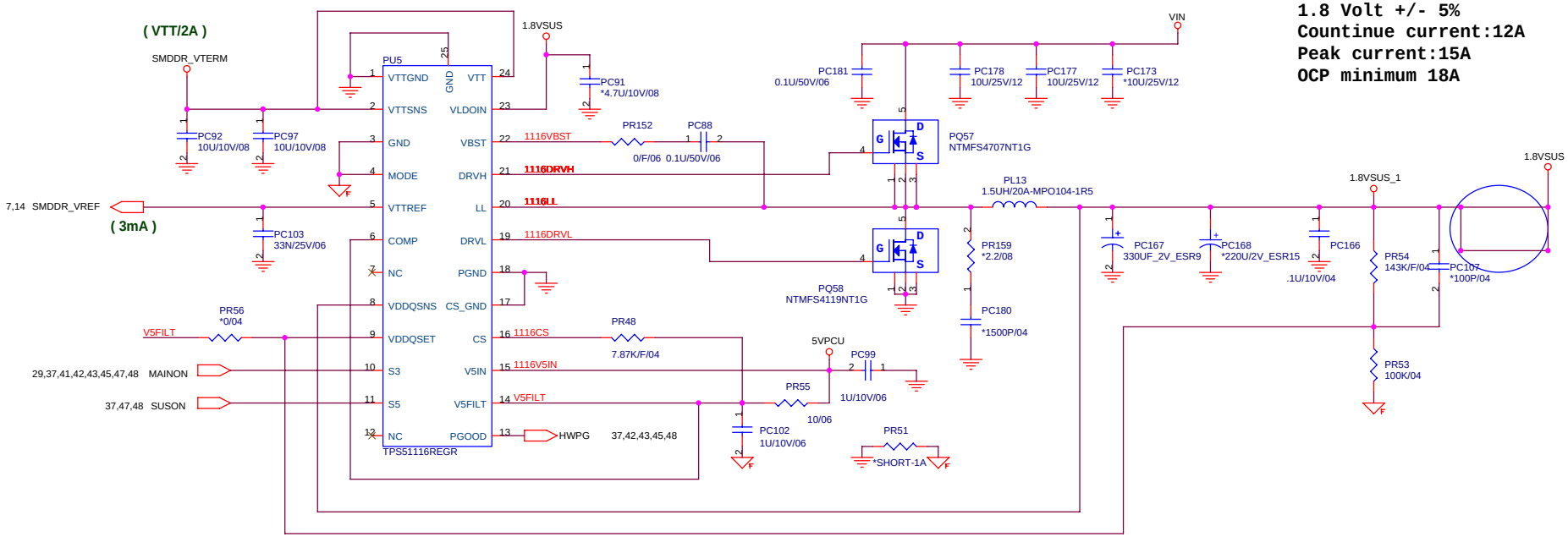


Vout1=(1+R1/R2)*0.5

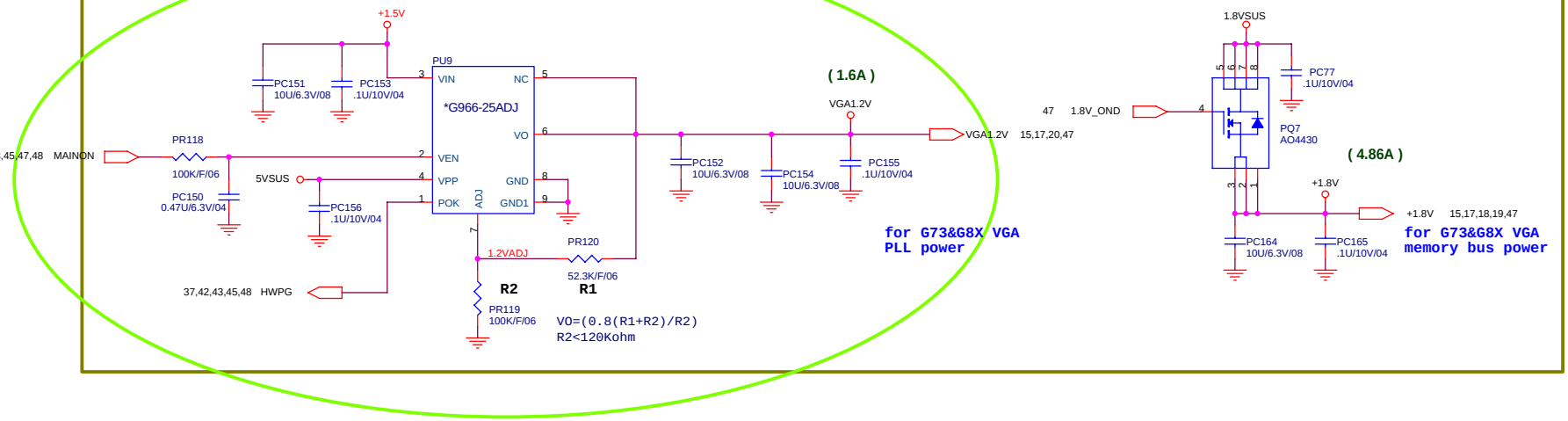
PROJECT : AT3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	VGACORE (MAX1993)	1A
Date: Tuesday, January 09, 2007	Sheet 45 of 48	

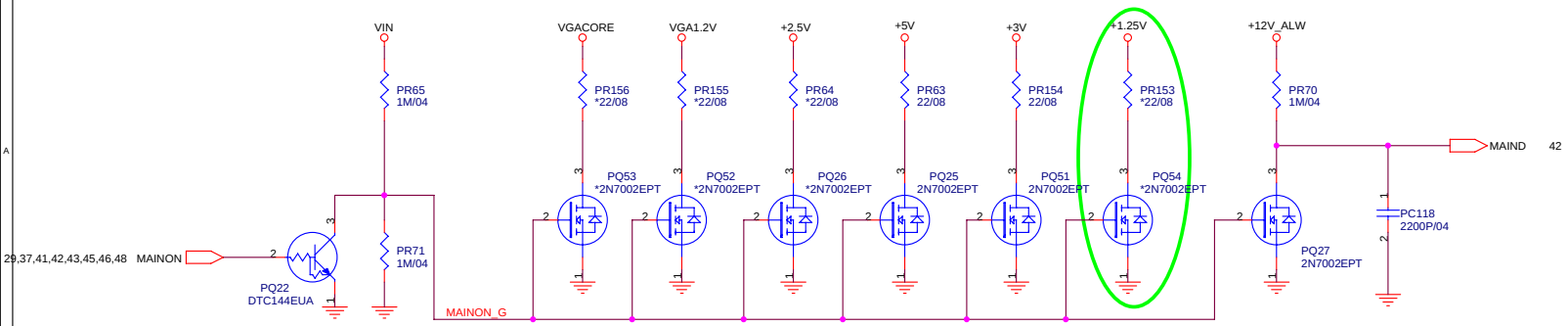
NB5/RD1/HW2

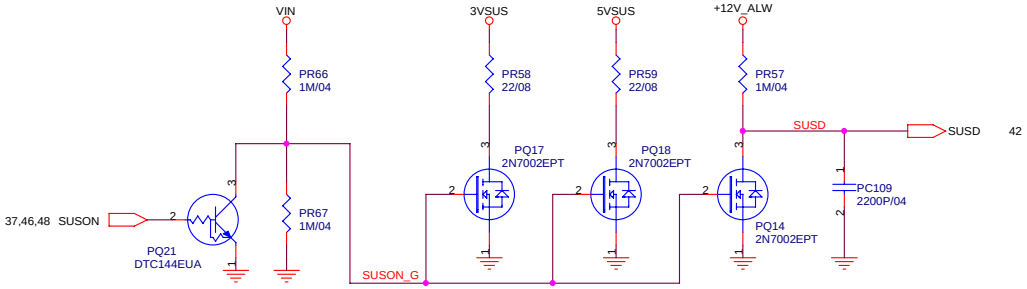


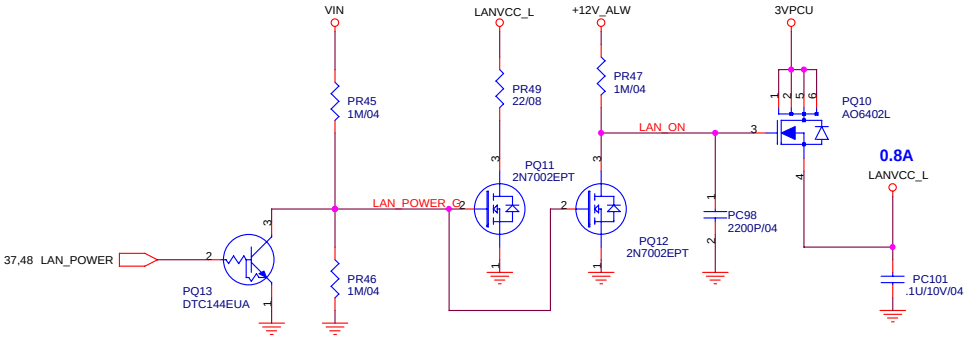
For Discrete Only

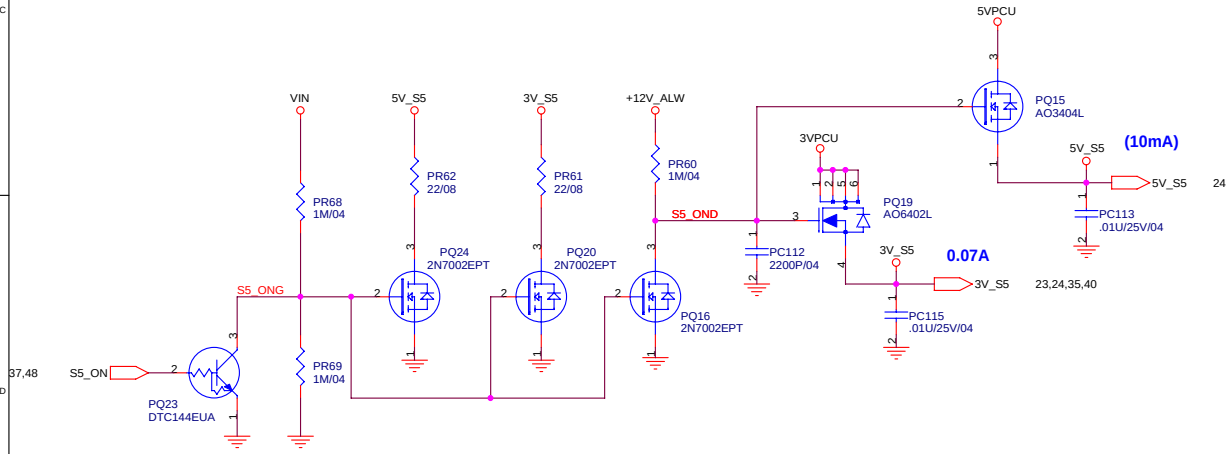


NB5/RD1/HW2	**PROJECT : AT3** Quanta Computer Inc.	
	Size: Custom Document Number: DDRII 1.8VSUS/SMDDR_VTERM	Rev: 1A
	Date: Tuesday, January 09, 2007	Sheet 46 of 48

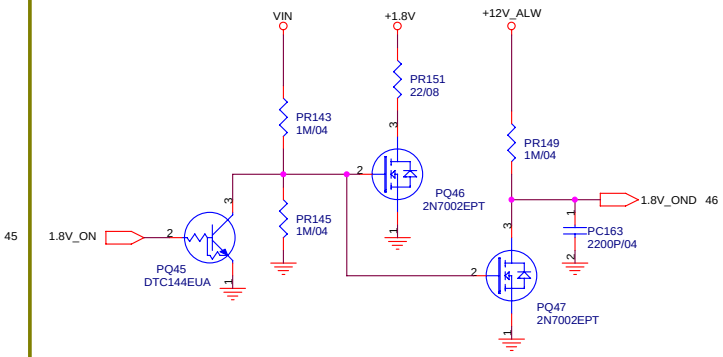




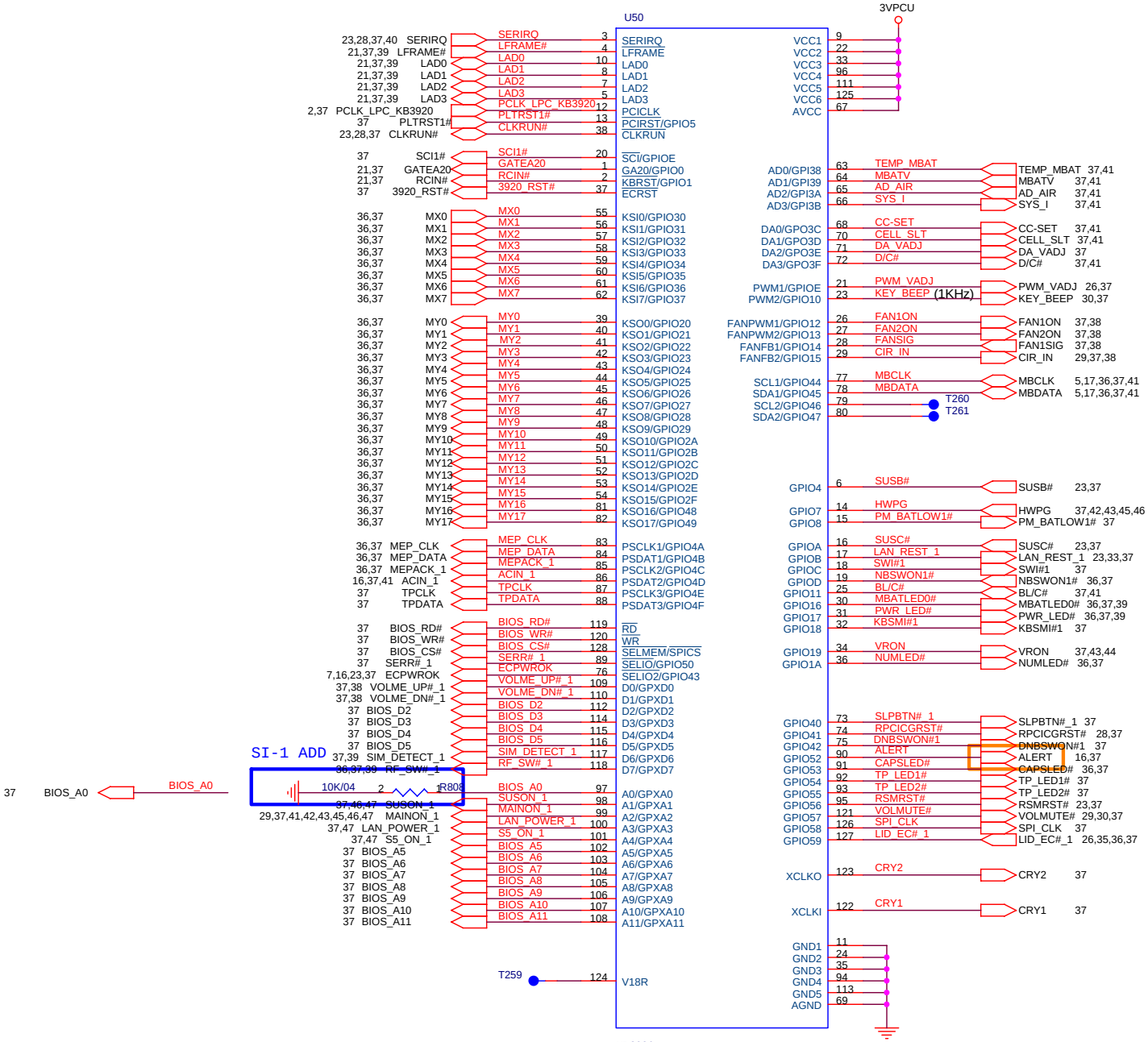




For Discrete Only



NB5/RD1/HW2	**PROJECT : AT3** Quanta Computer Inc.	
	Size: Custom — Document Number: DISCHARGE	Rev: 1A
	Date: Tuesday, January 09, 2007 — Sheet 47 of 48	



PROJECT : AT3
Quanta Computer Inc.

NB5/RD1/HW2

Size	Document Number	Rev
B	KB3926	1A

Date: Tuesday, January 09, 2007 | Sheet 48 of 48