



## INDEX

Pg#	Description	NOTE
1	Schematic Block Diagram	
2	System Information	
3	System Power Block Diagram	
4	CLOCL GENERATOR	
5-6	Intel ULV Peutium-M / ULV Celeron-M	
7-12	Calistoga-GM	
13	DDR II SO-DIMM	
14-17	ICH7-M	
18	LCD CONNECTOR / LCD PWR	
19	MINI CARD	
20-21	CARDBUS CONTROLLER	
22	GIGA-LAN	
23-24	AUDIO CODEC / AUDIO JACK	
25	KBC	
26	CRT PORT	
27	HDD / CD-ROM	
28	USB,BLUE TOOTH,FINGER PRINT, MDC,TPM	
29	FAN,KB,LEDs,TRACK POINT	
30	POWER SEQUENCE,BIOS	
31	CABLE DOCKING	
32	DISCHARGE,+2.5V	
33	CHARGE(MAX8724/1908)	
34	SYSTEM POWER(3V/5V)	
35	SYSTEM POWER(1.8V/0.9V)	
36	SYSTEM POWER(1.05V/1.5V)	
37	CPU POWER	
38	CHANGE HISTORY	

## Power & Ground

Label	ACTIVE	Description	Control Signal
VIN	S0, S3, S4, S5	AC ADAPTER (19V)	
MBAT	S0, S3, S4, S5	MAIN BATTERY + (10-17V)	
VCCRTC	S0, S3, S4, S5	RTC & KBC POWER (3_3V)	
+15V	S0, S3, S4, S5	+15V	
CPU_CORE	S0	CPU CORE POWER (1.25/1.15V)	VRON
+1.05V	S0	FSB POWER (1.05V)	VRON
+3V	S0		MAIND
3VSUS	S0, S3		SUSON
3V_S5	S0, S3, S4, S5		S5_ON
3VPCU	S0, S3, S4, S5	ALWAYS POWER (3V)	
+5V	S0		MAIND
5VSUS	S0, S3		SUSON
5V_S5	S0, S3, S4, S5		S5_ON
5VPCU	S0, S3, S4, S5	ALWAYS POWER (5V)	
+1.5V	S0		MAIND
1.5V_S5	S0, S3, S4, S5		S5_ON
1.8VSUS	S0, S3	DDR CORE POWER	SUSON
+2.5V	S0		MAINON
SMDDR_VTERM	S0	DDR COMMAND & CONTROL PULL UP POWER	MAINON
SMDDR_VREF	S0, S3	DDR REF POWER	SUSON
VDDA	S0	AUDIO ANALOG POWER (5V)	MAINON
⏏ GND	ALL PAGES	DIGITAL GROUND	
⏏ AGND		AUDIO GND	
⏏ T-GND		AUDIO JACK GND	
⏏ 6260AGND		CPU ANALOG GROUND	

## PCI DEVICES IRQ ROUTING

DEVICE	IDSEL #	REQ/GNT #	PCL_INT
GBIT ETHERNET	AD16	0	B
CardBus	AD25	1	C,D,E

## PCB STACK UP

**LAYER 1 : TOP**  
**LAYER 2 : GND**  
**LAYER 3 : IN1**  
**LAYER 4 : IN2**  
**LAYER 5 : VCC**  
**LAYER 6 : IN3**  
**LAYER 7 : GND**  
**LAYER 8 : BOT**

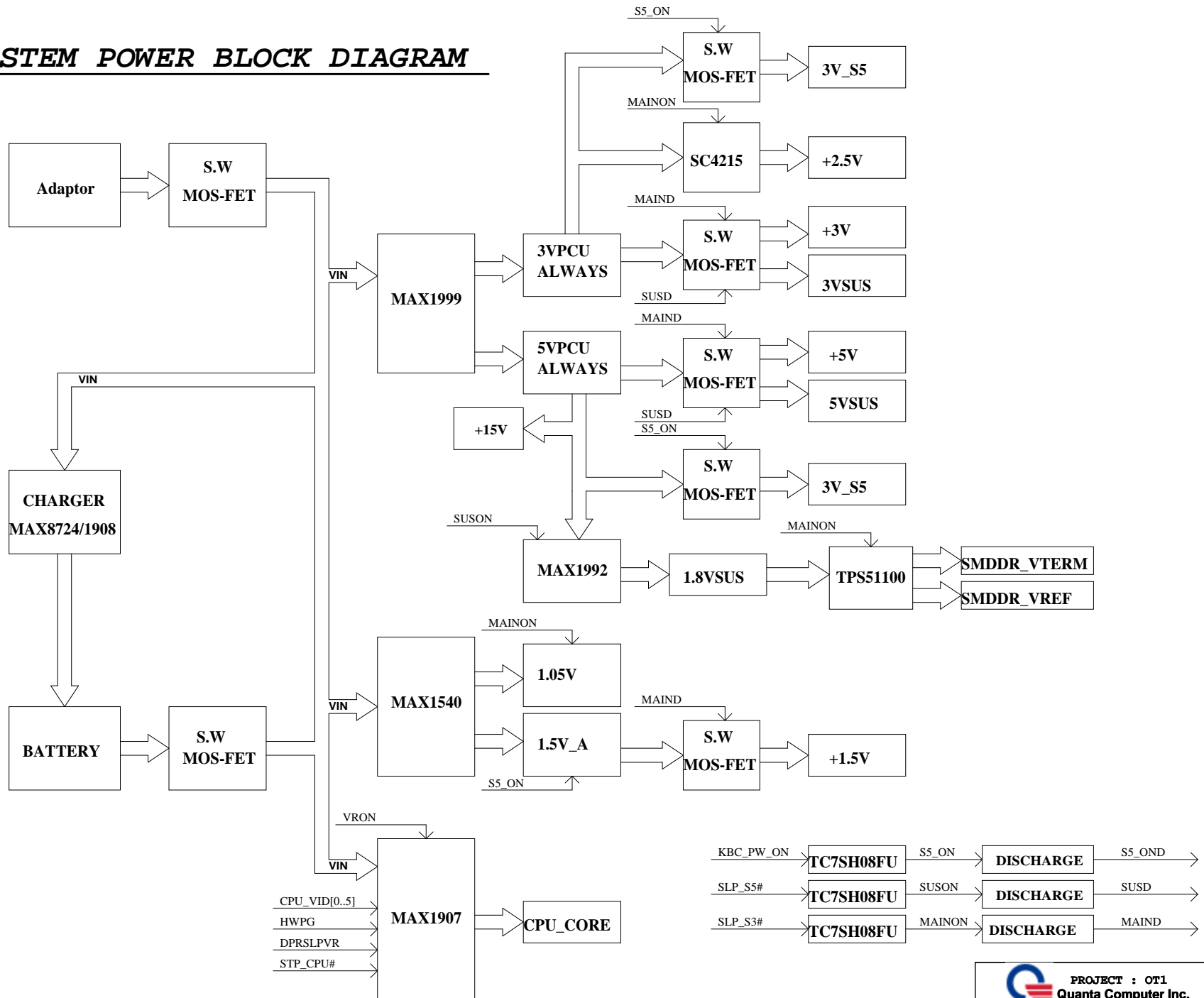
## SM BUS

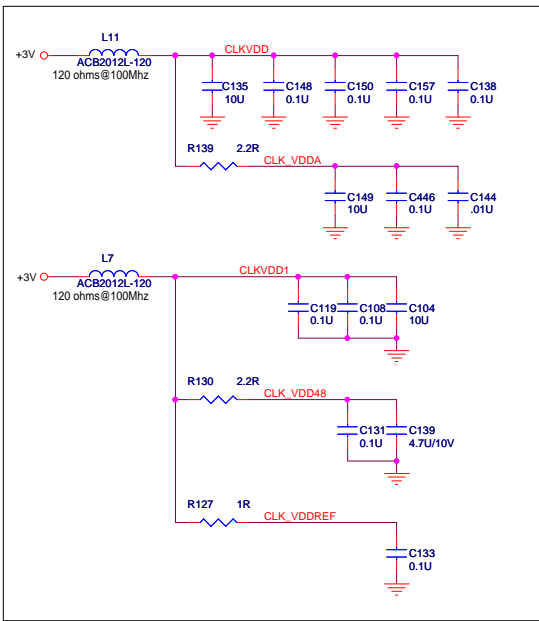
DEVICE	ADDRESS	BUS
CLOCK GENERATOR	D2H	( ICH6 ) PCLK_SMB , PCLK_SMB
DDR II	A0H	( ICH6 ) PCLK_SMB , PCLK_SMB
LCD EDID	TBD	GMCH
CHARGER	16H	(KBC) MBDATA, MBCLK
CPU THERMAL SENSOR	98H	(KBC) MBDATA, MBCLK



**PROJECT : OT1**  
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# SYSTEM POWER BLOCK DIAGRAM

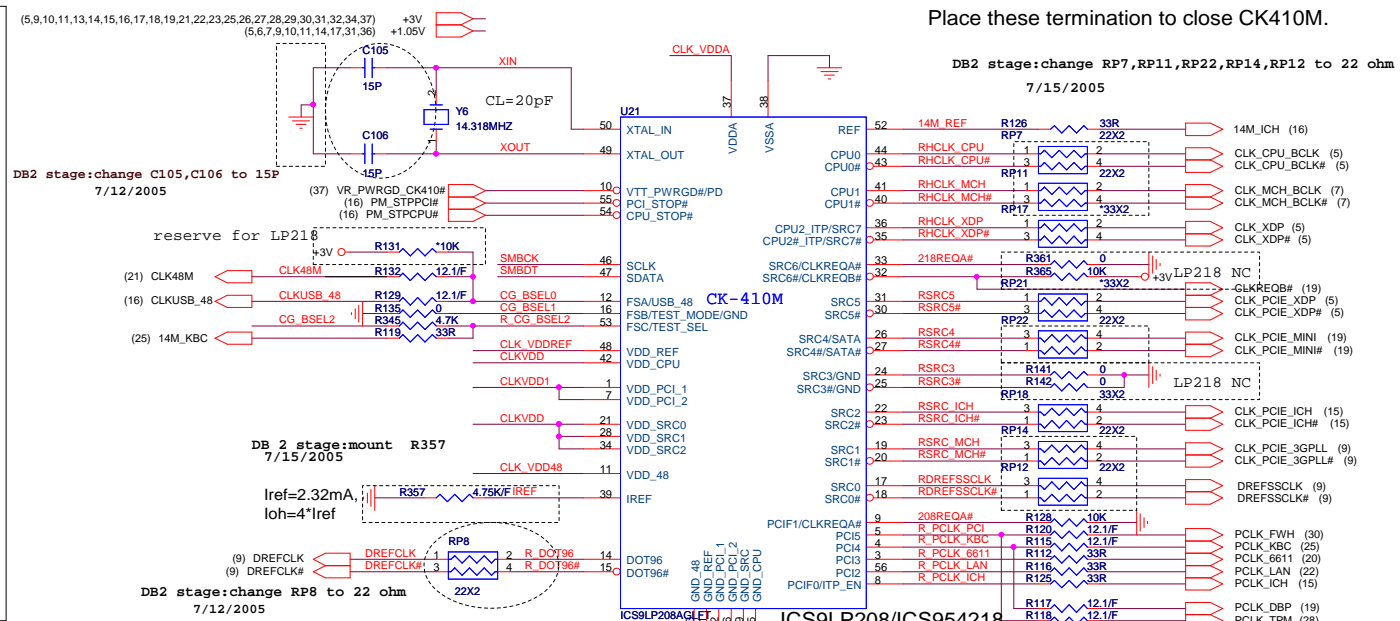




FSC	FSB	FSA	CPU	SRC	PCI	
1	0	1	100	100	33	DO THAN FSB 400
0	0	1	133	100	33	DO THAN FSB 533
0	1	1	166	100	33	
0	1	0	200	100	33	
0	0	0	266	100	33	
1	0	0	333	100	33	
1	1	0	400	100	33	
1	1	1	RESERVED			

\* Frequency select by CPU auto sense.

ICS9LP208 DEFAULT SETTING		ICS954218	
pin NO.		pin NO.	
12	CPU Freq. FIXED	12	CPU Freq. SELECT
16	-----	16	-----
53	SELECT	53	SELECT
39	VREF NC.	39	IREF PULL LO
9	CLKREQA#*	9	*SELSRC_LDCCLK#/PCICLK_F1
33	GND	33	CLKREQA#*
24	GND	24	SRCCLKT3
25		25	SRCCLKC3
52	REF0/*SELSRC_LDCCLK#	52	REF0



Place these termination to close CK410M.

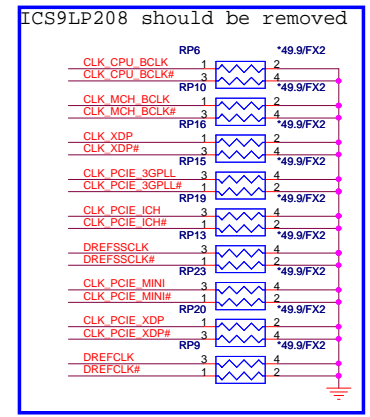
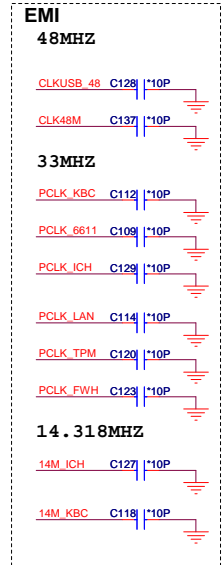
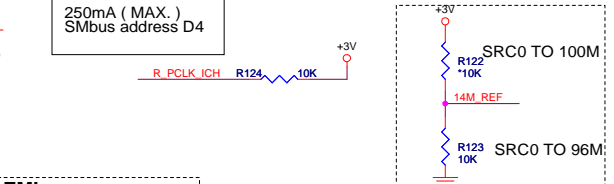
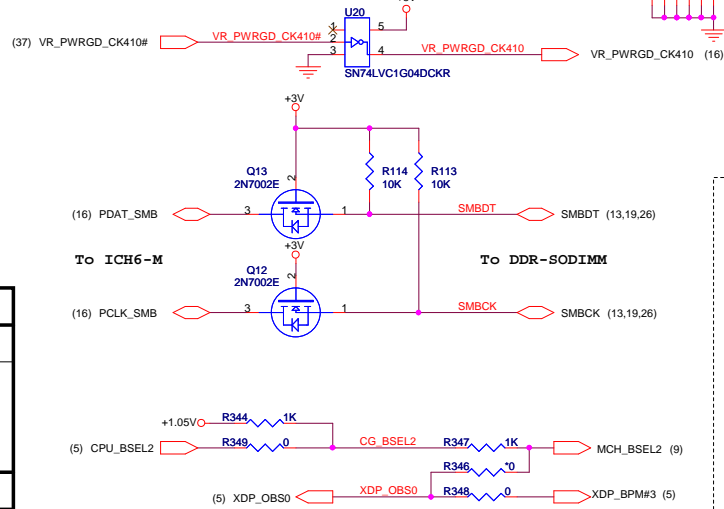
DB2 stage:change RP7,RP11,RP22,RP14,RP12 to 22 ohm  
7/15/2005

DB2 stage:change C105,C106 to 15P  
7/12/2005

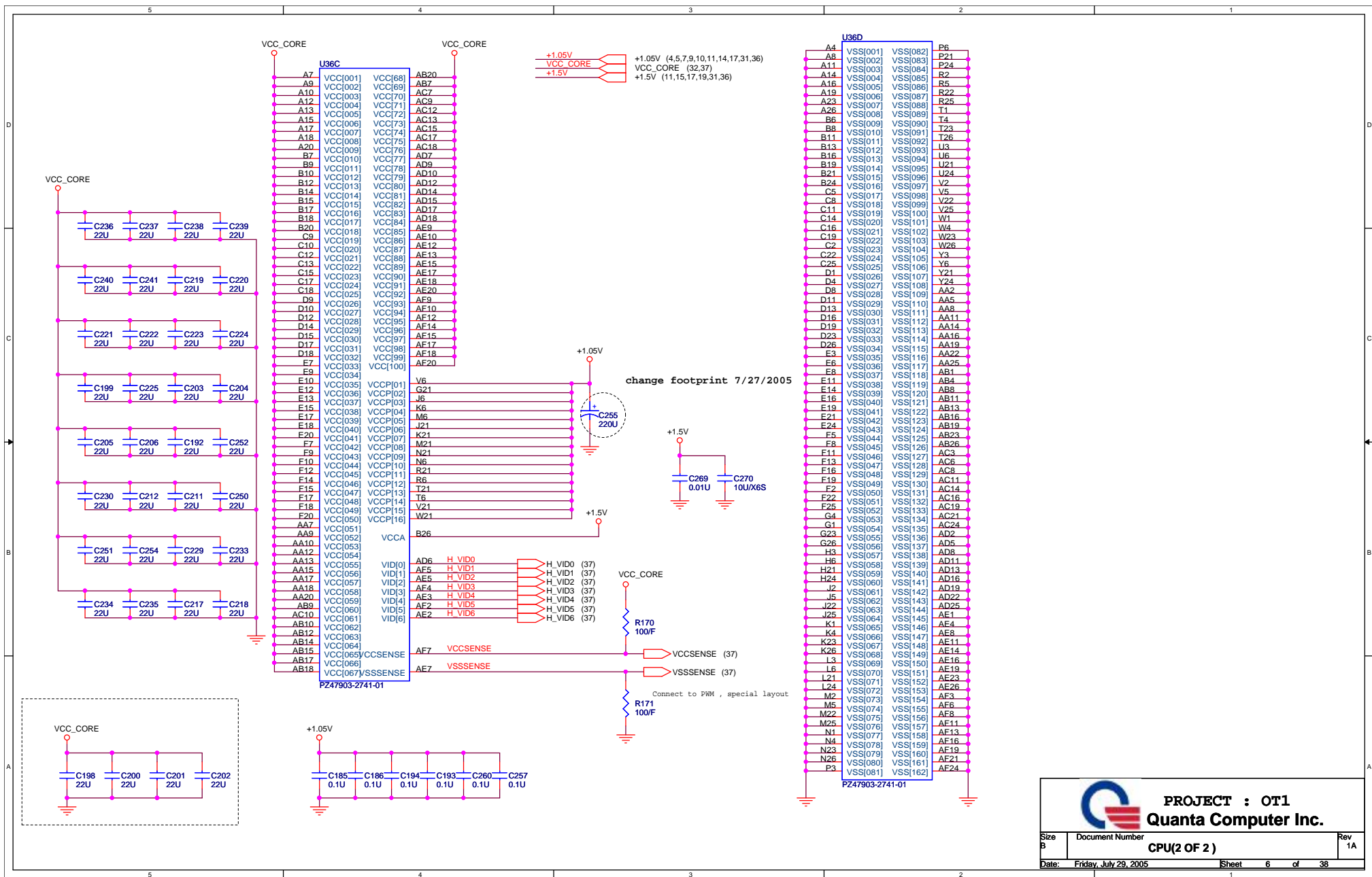
reserve for LP218

DB 2 stage:mount R357  
7/15/2005

DB2 stage:change RP8 to 22 ohm  
7/12/2005

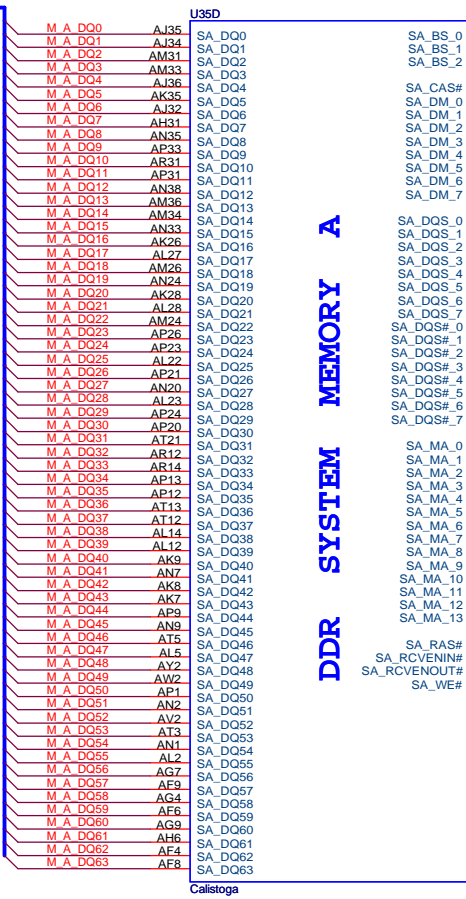






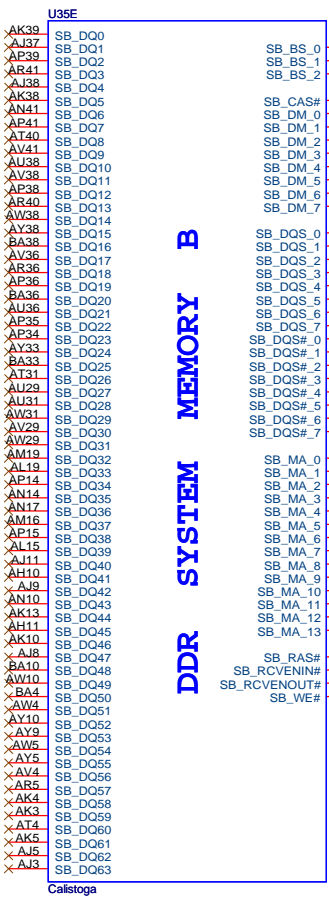
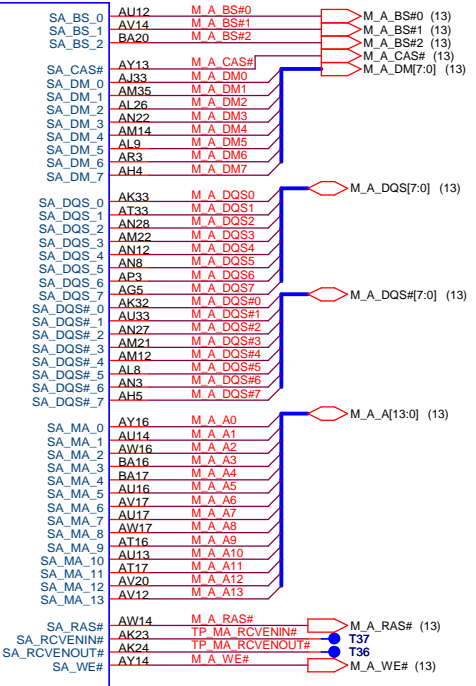


(13) M\_A\_DQ[63:0]




DDR SYSTEM MEMORY A

Calistoga



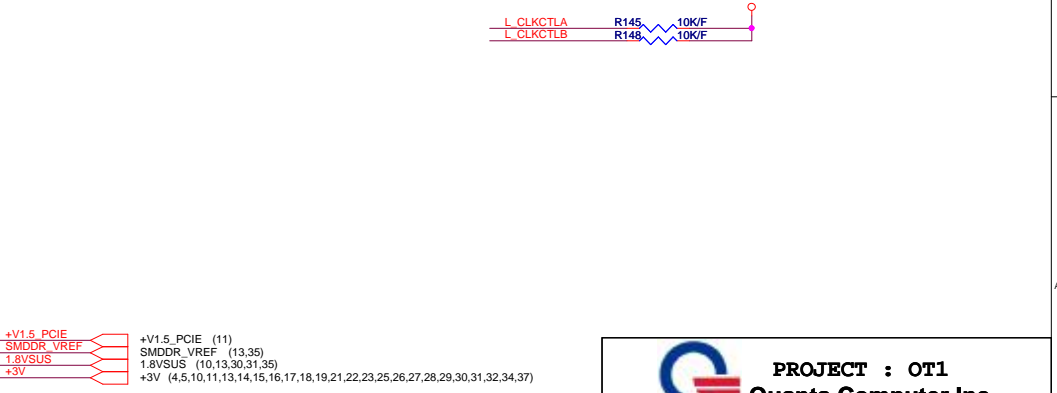
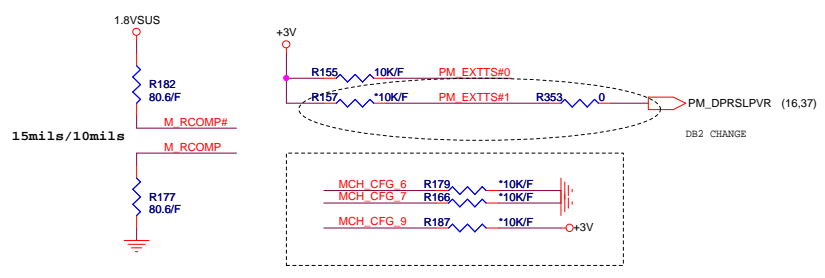
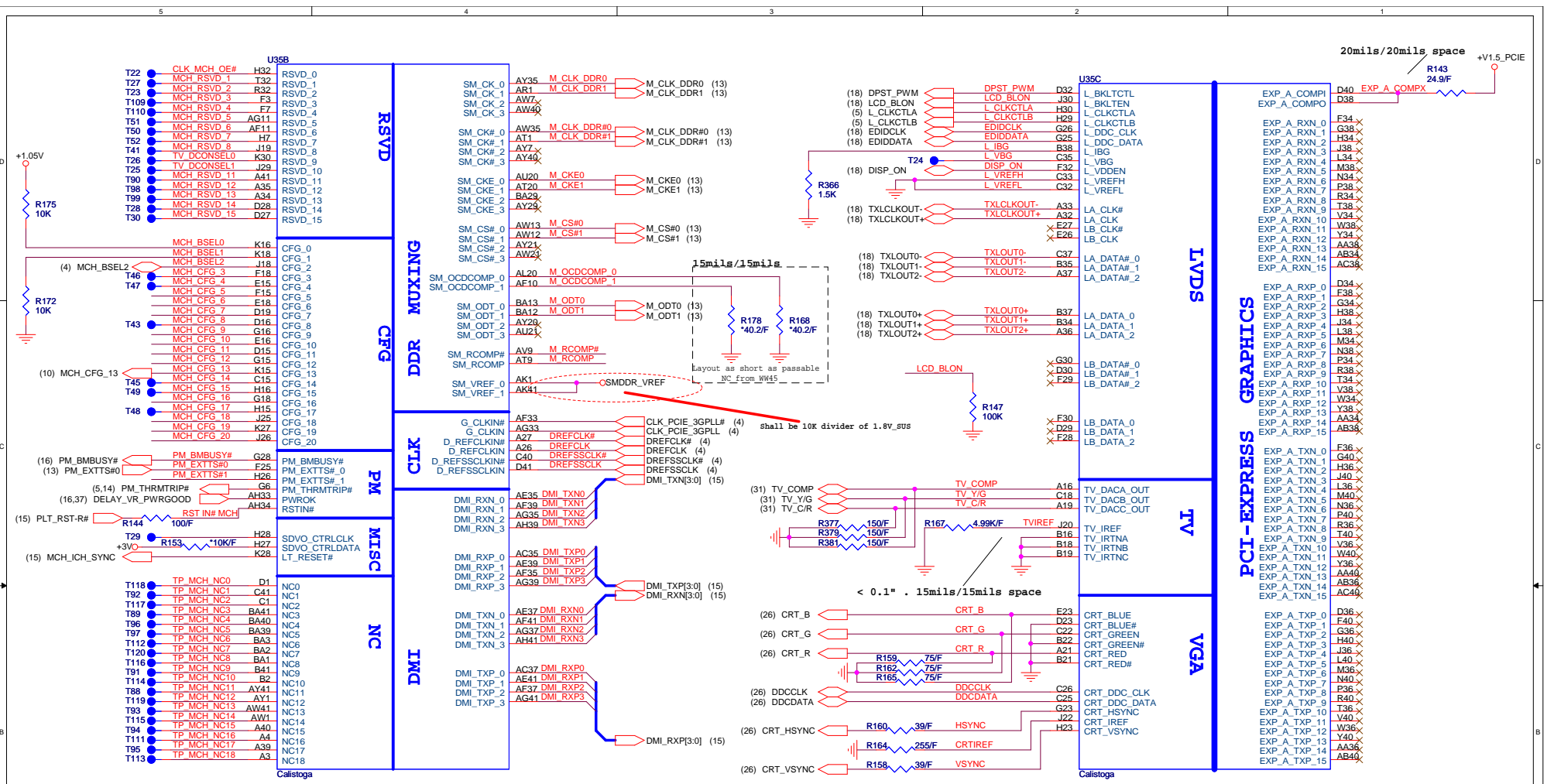
DDR SYSTEM MEMORY B

Calistoga

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Size B	Document Number <b>GMCH DDR(2 OF 6)</b>	Rev 1A
Date: Friday, July 29, 2005		
Sheet 8 of 38		1





(10) MCH\_CFG [12-15] MCH\_CFG [12-15]

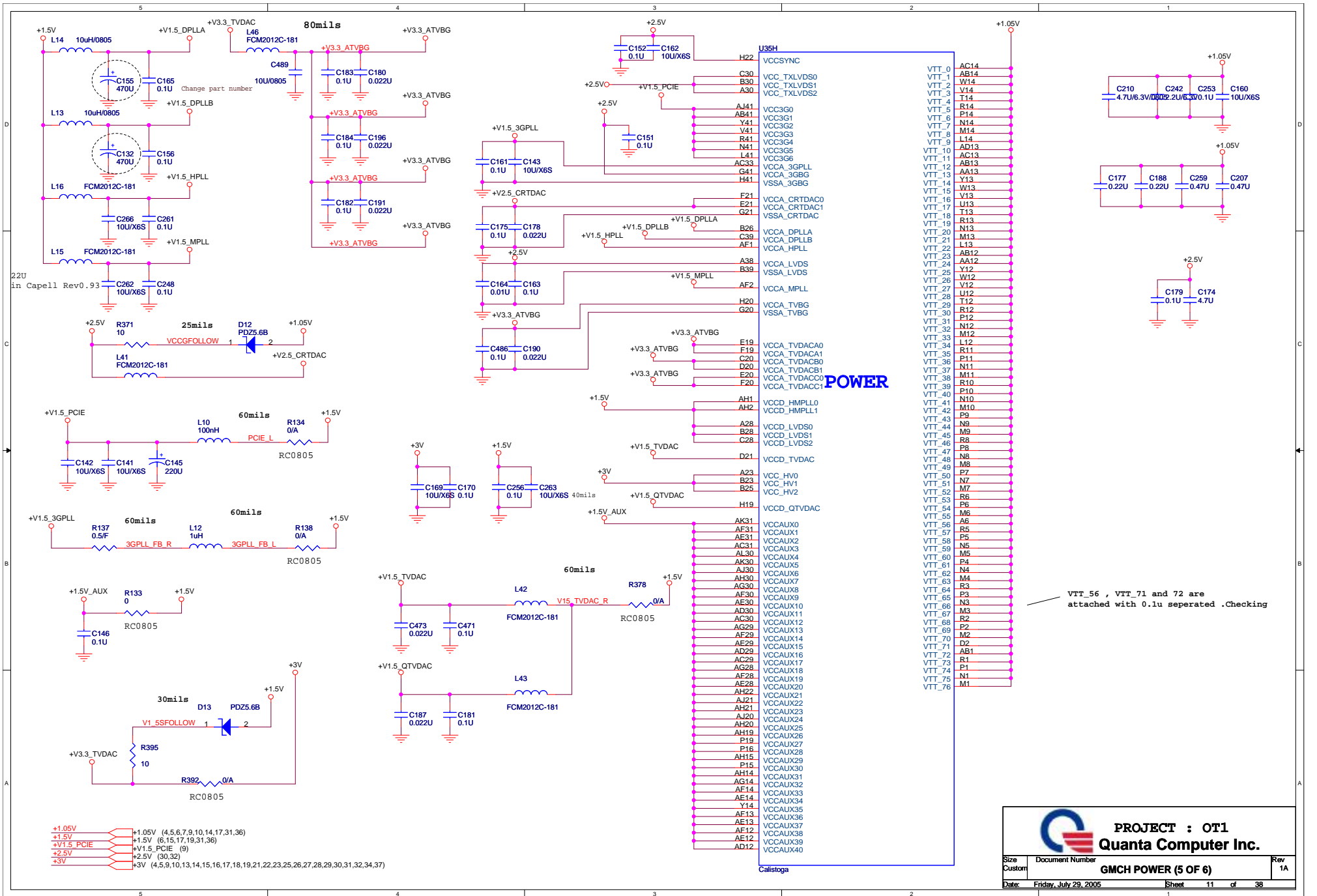
(10) MCH\_CFG [20-16] MCH\_CFG [20-16]

**PROJECT : OT1**  
**Quanta Computer Inc.**

Size: Custom Document Number: GMCH DMI VEDIO(3 OF 6) Rev: 1A

Date: Friday, July 29, 2005 Sheet: 9 of 38





**PROJECT : OT1**  
**Quanta Computer Inc.**

Size Custom	Document Number <b>GMCH POWER (5 OF 6)</b>	Rev 1A
Date: Friday, July 29, 2005		Sheet 11 of 38

U35I		VSS	
AC41	VSS_0	VSS_97	AK34
AA41	VSS_1	VSS_98	AG34
W41	VSS_2	VSS_99	AF34
T41	VSS_3	VSS_100	AE34
P41	VSS_4	VSS_101	AC34
M41	VSS_5	VSS_102	C34
J41	VSS_6	VSS_103	AW33
F41	VSS_7	VSS_104	AV33
AV40	VSS_8	VSS_105	AR33
AP40	VSS_9	VSS_106	AE33
AN40	VSS_10	VSS_107	AB33
AK40	VSS_11	VSS_108	Y33
AJ40	VSS_12	VSS_109	V33
AH40	VSS_13	VSS_110	T33
AG40	VSS_14	VSS_111	R33
AF40	VSS_15	VSS_112	M33
AE40	VSS_16	VSS_113	H33
B40	VSS_17	VSS_114	G33
AY39	VSS_18	VSS_115	F33
AW39	VSS_19	VSS_116	D33
AV39	VSS_20	VSS_117	B33
AR39	VSS_21	VSS_118	AH32
AN39	VSS_22	VSS_119	AG32
AJ39	VSS_23	VSS_120	AF32
AK39	VSS_24	VSS_121	AE32
AB39	VSS_25	VSS_122	AC32
AA39	VSS_26	VSS_123	AB32
Y39	VSS_27	VSS_124	G32
W39	VSS_28	VSS_125	AY31
V39	VSS_29	VSS_126	AV31
T39	VSS_30	VSS_127	AN31
R39	VSS_31	VSS_128	AK31
P39	VSS_32	VSS_129	AJ31
N39	VSS_33	VSS_130	AG31
M39	VSS_34	VSS_131	AB31
L39	VSS_35	VSS_132	Y31
J39	VSS_36	VSS_133	AB30
H39	VSS_37	VSS_134	E30
G39	VSS_38	VSS_135	AT29
F39	VSS_39	VSS_136	AN29
D39	VSS_40	VSS_137	AB29
AT38	VSS_41	VSS_138	T29
AM38	VSS_42	VSS_139	N29
AH38	VSS_43	VSS_140	K29
AG38	VSS_44	VSS_141	G29
AF38	VSS_45	VSS_142	D18
AE38	VSS_46	VSS_143	A18
C38	VSS_47	VSS_144	AY17
AK37	VSS_48	VSS_145	AR17
AH37	VSS_49	VSS_146	AP17
AG37	VSS_50	VSS_147	AM17
AA37	VSS_51	VSS_148	AK17
Y37	VSS_52	VSS_149	AV16
W37	VSS_53	VSS_150	AN16
V37	VSS_54	VSS_151	AL16
T37	VSS_55	VSS_152	J16
R37	VSS_56	VSS_153	F16
P37	VSS_57	VSS_154	C16
N37	VSS_58	VSS_155	AN15
M37	VSS_59	VSS_156	AM15
L37	VSS_60	VSS_157	AK15
J37	VSS_61	VSS_158	N15
H37	VSS_62	VSS_159	M15
G37	VSS_63	VSS_160	L15
F37	VSS_64	VSS_161	B15
D37	VSS_65	VSS_162	A15
AY36	VSS_66	VSS_163	BA14
AW36	VSS_67	VSS_164	AT14
AV36	VSS_68	VSS_165	AK14
AR36	VSS_69	VSS_166	K26
AN36	VSS_70	VSS_167	F26
AJ36	VSS_71	VSS_168	AD14
AH36	VSS_72	VSS_169	AA14
AG36	VSS_73	VSS_170	U14
AF36	VSS_74	VSS_171	K14
AE36	VSS_75	VSS_172	H14
C36	VSS_76	VSS_173	E14
B36	VSS_77	VSS_174	AV13
BA35	VSS_78	VSS_175	AR13
AV35	VSS_79	VSS_176	AN13
AR35	VSS_80	VSS_177	AM13
AH35	VSS_81	VSS_178	AL13
AG35	VSS_82	VSS_179	AG13
AF35	VSS_83		P13
AE35	VSS_84		F13
AA35	VSS_85		D13
Y35	VSS_86		B13
W35	VSS_87		AV12
V35	VSS_88		AC12
T35	VSS_89		K12
R35	VSS_90		H12
P35	VSS_91		E12
N35	VSS_92		AD11
M35	VSS_93		AA11
L35	VSS_94		Y11
J35	VSS_95		
H35	VSS_96		
G35			
F35			
D35			
AN34			

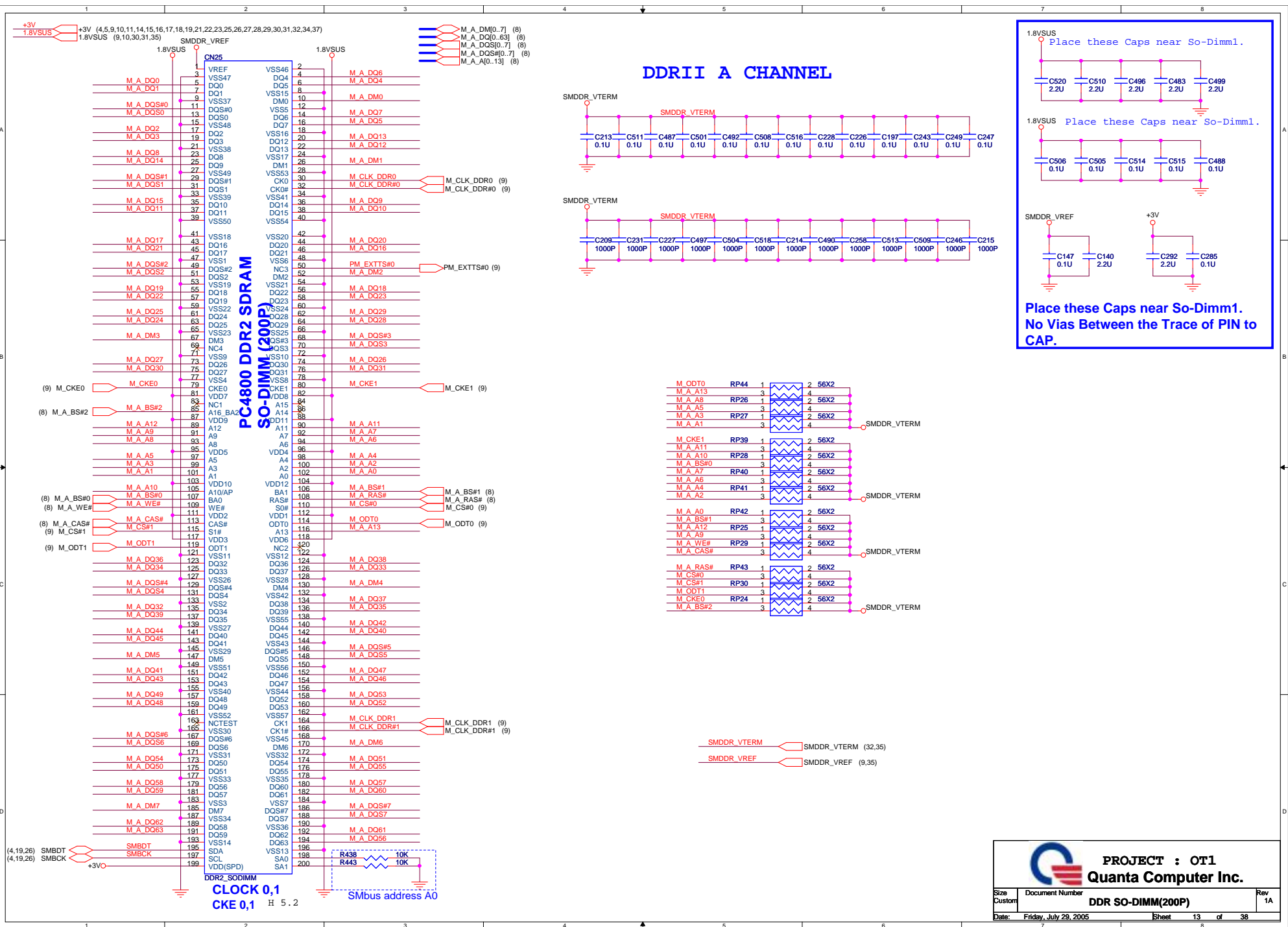
Calistoga

U35J		VSS	
AT23	VSS_180	VSS_273	J11
AN23	VSS_181	VSS_274	D11
AM23	VSS_182	VSS_275	B11
AH23	VSS_183	VSS_276	AV10
AC23	VSS_184	VSS_277	AF10
W23	VSS_185	VSS_278	AL10
K23	VSS_186	VSS_279	AJ10
J23	VSS_187	VSS_280	AG10
F23	VSS_188	VSS_281	AC10
C23	VSS_189	VSS_282	W10
AA22	VSS_190	VSS_283	U10
K22	VSS_191	VSS_284	BA9
G22	VSS_192	VSS_285	AW9
F22	VSS_193	VSS_286	AR9
E22	VSS_194	VSS_287	AH9
D22	VSS_195	VSS_288	AB9
A22	VSS_196	VSS_289	Y9
BA21	VSS_197	VSS_290	R9
AV21	VSS_198	VSS_291	G9
AR21	VSS_199	VSS_292	E9
AN21	VSS_200	VSS_293	A9
AL21	VSS_201	VSS_294	AG8
AB21	VSS_202	VSS_295	AD8
Y21	VSS_203	VSS_296	AA8
P21	VSS_204	VSS_297	U8
K21	VSS_205	VSS_298	K8
J21	VSS_206	VSS_299	C8
H21	VSS_207	VSS_300	BA7
C21	VSS_208	VSS_301	AV7
AW20	VSS_209	VSS_302	AP7
AR20	VSS_210	VSS_303	AL7
AM20	VSS_211	VSS_304	AJ7
AA20	VSS_212	VSS_305	AH7
K20	VSS_213	VSS_306	AF7
B20	VSS_214	VSS_307	AC7
A20	VSS_215	VSS_308	R7
AN19	VSS_216	VSS_309	G7
AC19	VSS_217	VSS_310	D7
W19	VSS_218	VSS_311	AG6
K19	VSS_219	VSS_312	AD6
G19	VSS_220	VSS_313	AB6
C19	VSS_221	VSS_314	Y6
AH18	VSS_222	VSS_315	U6
P18	VSS_223	VSS_316	N6
H18	VSS_224	VSS_317	K6
D18	VSS_225	VSS_318	H6
A18	VSS_226	VSS_319	B6
AY17	VSS_227	VSS_320	AV5
AR17	VSS_228	VSS_321	AF5
AP17	VSS_229	VSS_322	AD5
AM17	VSS_230	VSS_323	AY4
AV16	VSS_231	VSS_324	AR4
AN16	VSS_232	VSS_325	AP4
AL16	VSS_233	VSS_326	AL4
J16	VSS_234	VSS_327	AJ4
F16	VSS_235	VSS_328	Y4
C16	VSS_236	VSS_329	R4
AN15	VSS_237	VSS_330	J4
AM15	VSS_238	VSS_331	JA
AK15	VSS_239	VSS_332	F4
N15	VSS_240	VSS_333	C4
M15	VSS_241	VSS_334	AY3
L15	VSS_242	VSS_335	AW3
B15	VSS_243	VSS_336	AV3
A15	VSS_244	VSS_337	AL3
BA14	VSS_245	VSS_338	AH3
AT14	VSS_246	VSS_339	AG3
AK14	VSS_247	VSS_340	AF3
K26	VSS_248	VSS_341	AD3
F26	VSS_249	VSS_342	AC3
D26	VSS_250	VSS_343	AA3
AK25	VSS_251	VSS_344	G3
P25	VSS_252	VSS_345	AT2
K25	VSS_253	VSS_346	AR2
H25	VSS_254	VSS_347	AP2
E25	VSS_255	VSS_348	AK2
D25	VSS_256	VSS_349	AJ2
A25	VSS_257	VSS_350	AD2
BA24	VSS_258	VSS_351	AB2
AU24	VSS_259	VSS_352	Y2
AL24	VSS_260	VSS_353	T2
AW23	VSS_261	VSS_354	N2
	VSS_262	VSS_355	I2
	VSS_263	VSS_356	J2
	VSS_264	VSS_357	H2
	VSS_265	VSS_358	F2
	VSS_266	VSS_359	C2
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	VSS_268		
	VSS_269		
	VSS_270		
	VSS_271		
	VSS_272		

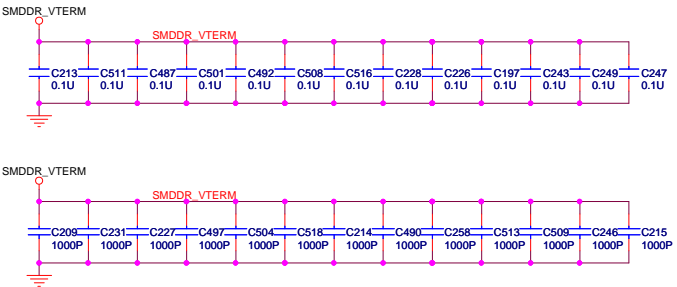
Calistoga

**PROJECT : OT1**  
**Quanta Computer Inc.**

Size	Document Number	Rev
Custom	GMCH GND(6 OF 6)	1A
Date:	Friday, July 29, 2005	Sheet 12 of 38



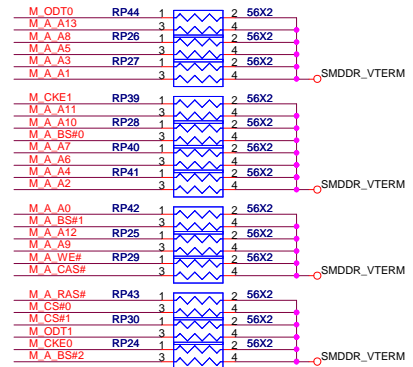
### DDR II A CHANNEL



Place these Caps near So-Dimm1.

Place these Caps near So-Dimm1.

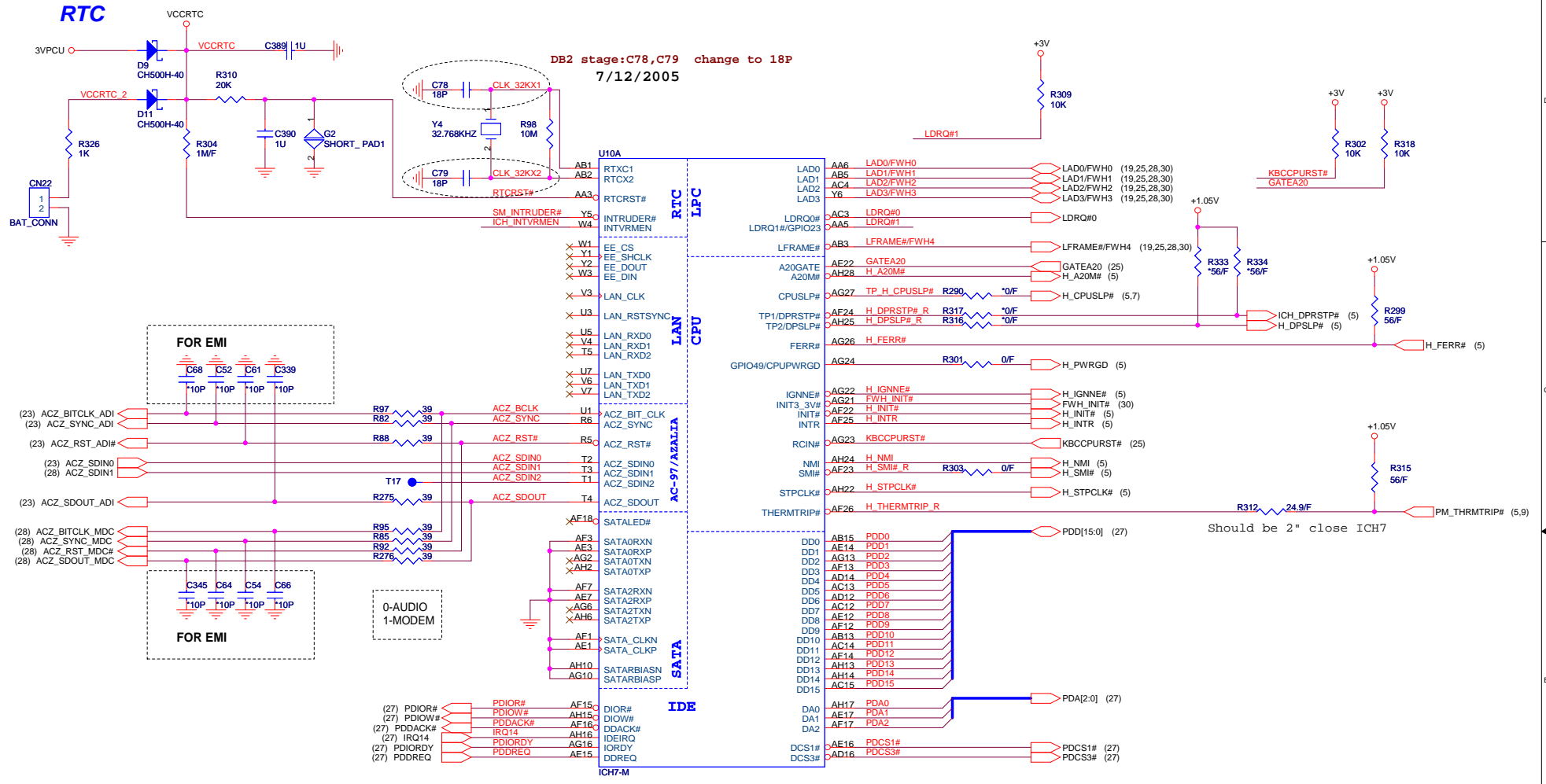
Place these Caps near So-Dimm1.  
No Vias Between the Trace of PIN to CAP.



**PROJECT : OT1**  
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Size	Document Number	Rev
Custom	DDR SO-DIMM(200P)	1A
Date:	Friday, July 29, 2005	Sheet 13 of 38

DB2 stage:C78,C79 change to 18P  
7/12/2005



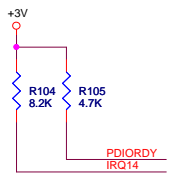
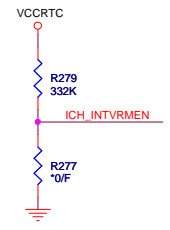
FOR EMI


FOR EMI

0-AUDIO 1-MODEM

ICH7 internal VR enable strap

STATUS	INTVRMEN
Enable (default)	1
Disable	0

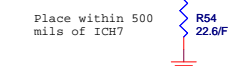
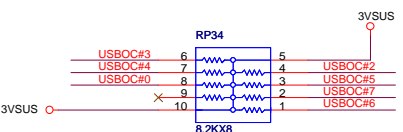
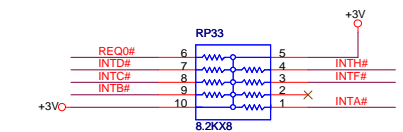
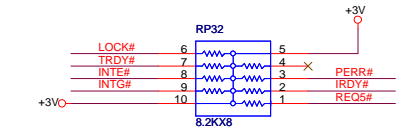
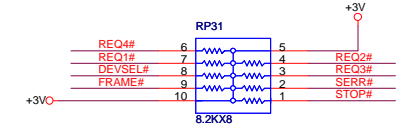
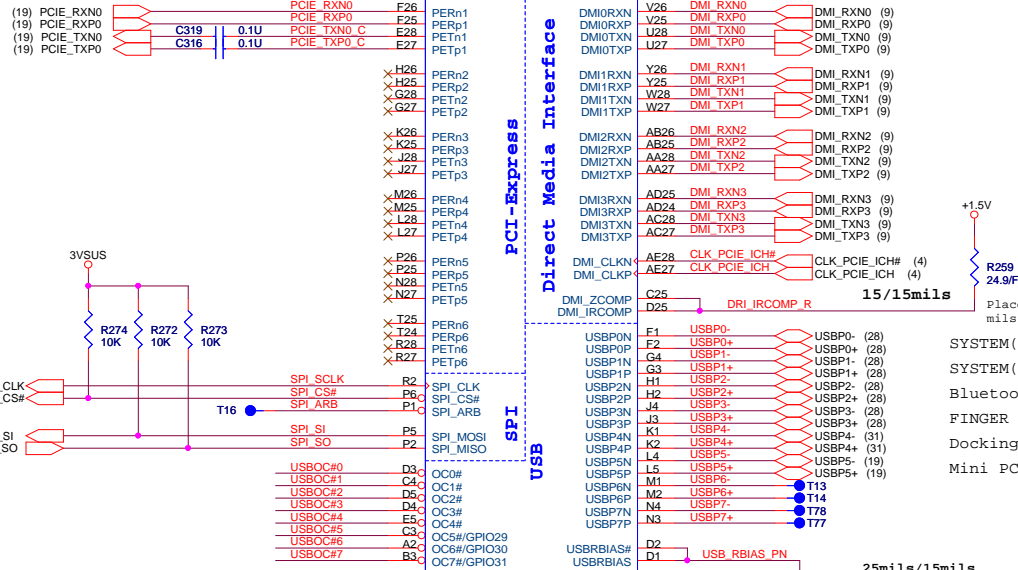




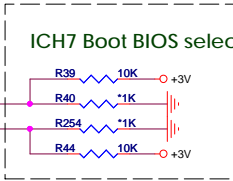
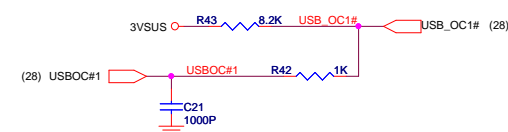
**PROJECT : OT1**  
**Quanta Computer Inc.**

Size Custom	Document Number	<b>ICH7-M HOST (1 OF 4)</b>	Rev 1A
Date: Friday, July 29, 2005	Sheet	14 of	38

MINI CARD PCI-E



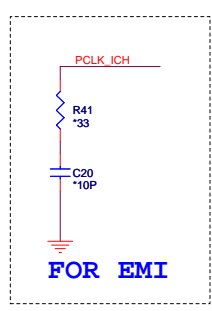
SYSTEM(RIGHT)  
 SYSTEM(LEFT)  
 Bluetooth Module  
 FINGER PRINT  
 Docking  
 Mini PCI-E 1



**ICH7 Boot BIOS select**

STRAP	GNT4#	GNT5#
LPC	1	1
SPI	0	1

(default)



**PCI DEVICES IRQ ROUTING**

DEVICE	IDSEL #	REQ/GNT #	PCI_INT
GBIT ETHERNET	AD16	0	B
CardBus	AD25	1	C,D,E

**PROJECT : OT1**  
**Quanta Computer Inc.**

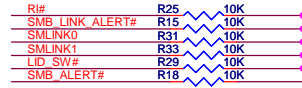
Size: Custom Document Number: ICH7-M PCI-E (2 OF 4) Rev 1A

Date: Friday, July 29, 2005 Sheet 15 of 38

Don't connect to PCI device / Express card

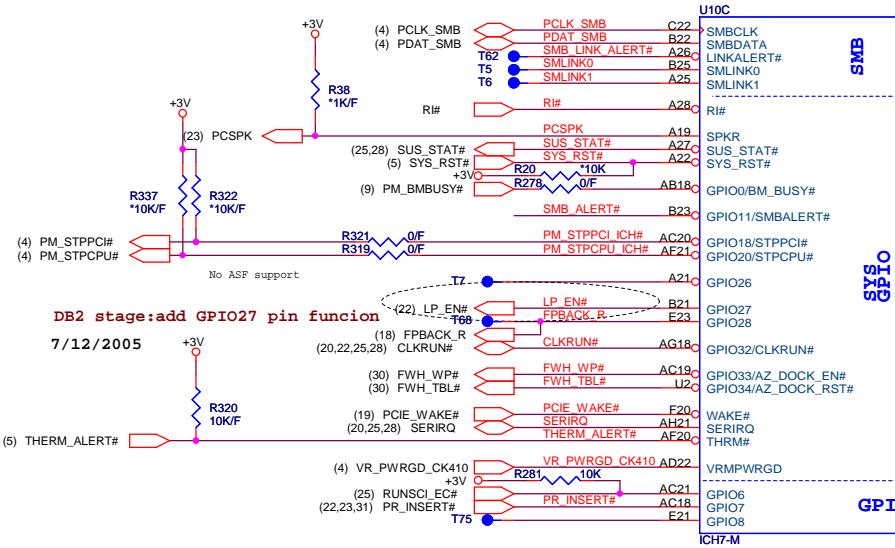
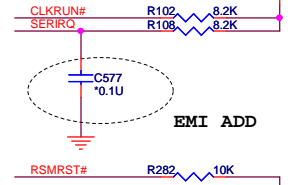
DB2 stage:R26 pull hi to 3V\_S5  
 DB2 stage>Delete R36

7/12/2005



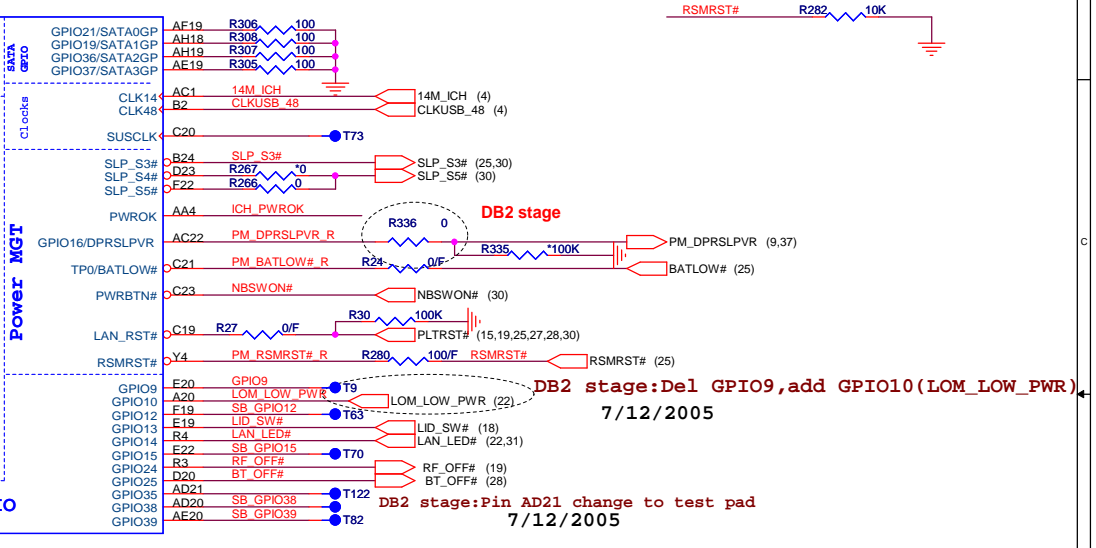
DB2 stage>Delete R28

7/12/2005



DB2 stage:add GPIO27 pin funcion

7/12/2005



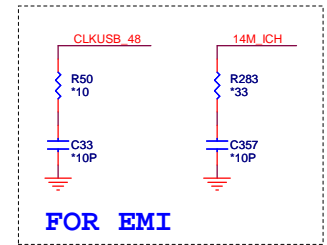
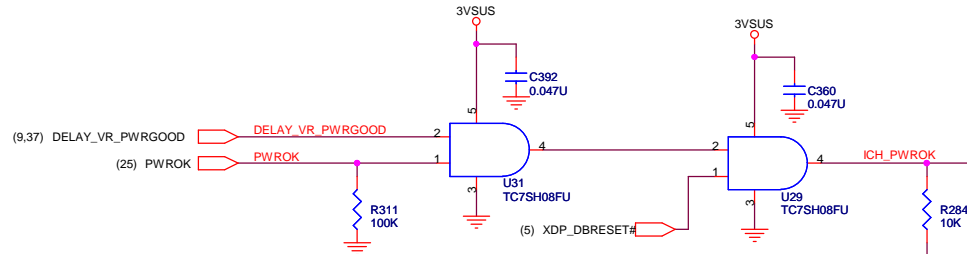
DB2 stage:Del GPIO9,add GPIO10(LOM\_LOW\_PWR)

7/12/2005

DB2 stage:Pin AD21 change to test pad

7/12/2005

DB2 stage:R37 pull hi to 3V\_S5  
 7/12/2005



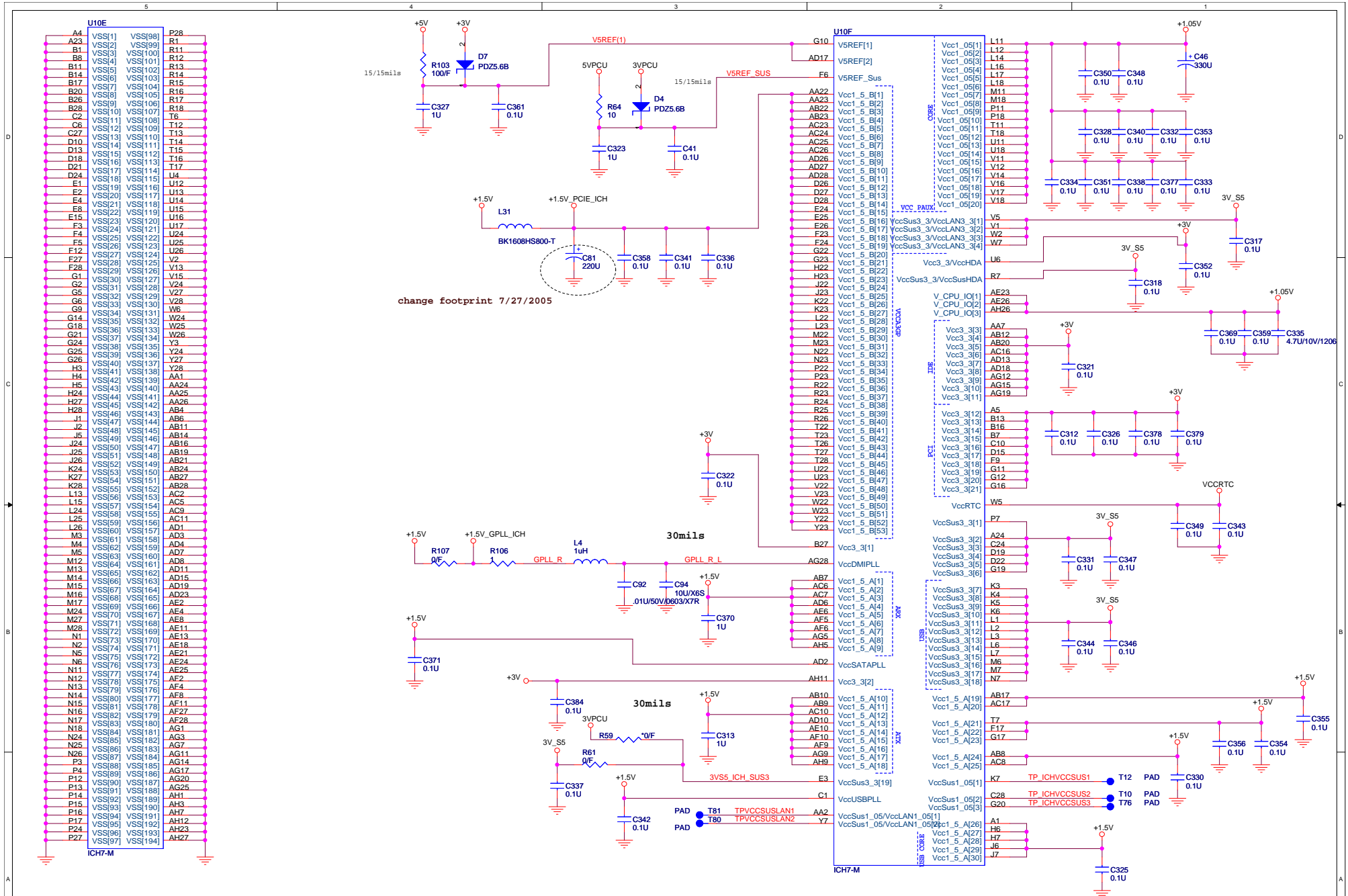
FOR EMI




PROJECT : OT1  
 Quanta Computer Inc.

Size B	Document Number	Rev 1A
ICH7-M GPIO (3 OF 4)		
Date: Friday, July 29, 2005	Sheet 16 of 38	







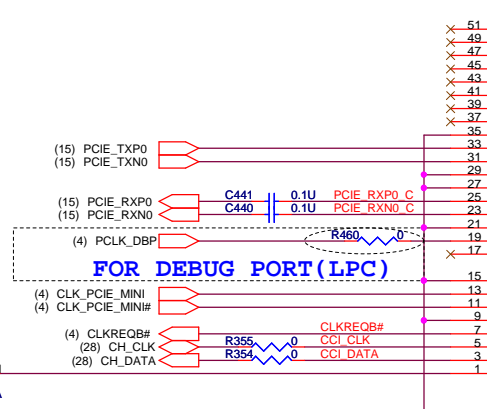
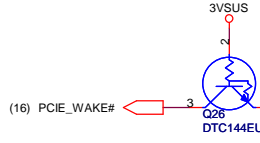
**PROJECT : OT1**  
**Quanta Computer Inc.**

Size	Document Number	Rev
Custom	<b>ICH7-M POWER (4 OF 4)</b>	1A
Date:	Friday, July 29, 2005	Sheet 17 of 38

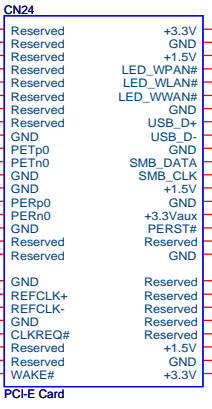


# Mini PCI-E Card

DB2 stage: Delete Pin17, RP38 ,add R460  
7/12/2005

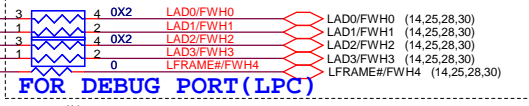


**FOR DEBUG PORT (LPC)**

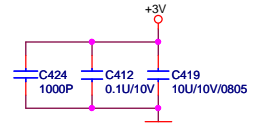
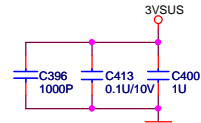
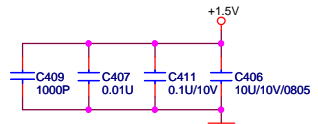


DB2 stage:  
Chaned the footprint.  
Elsion 7/11/2005

DB2 stage:  
Del CN5.  
7/11/2005



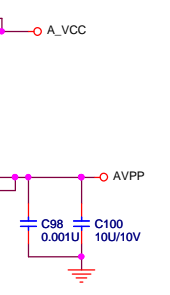
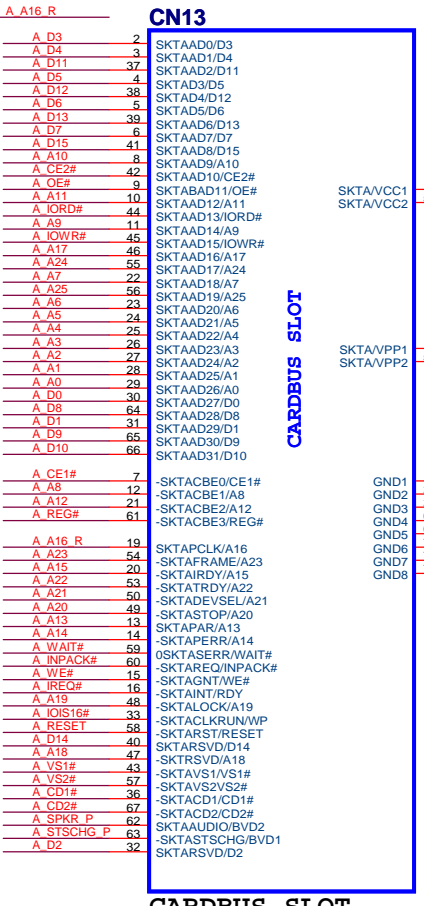
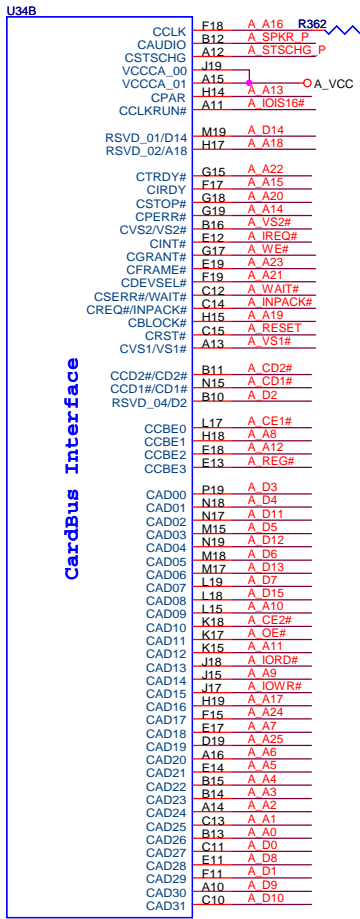
**FOR DEBUG PORT (LPC)**



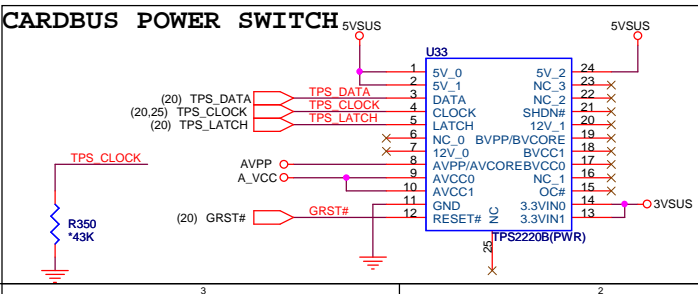
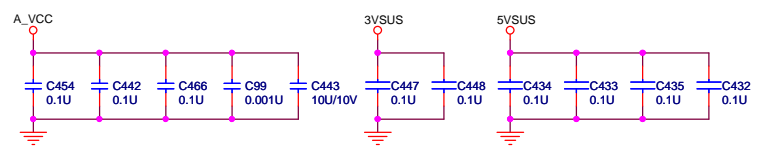
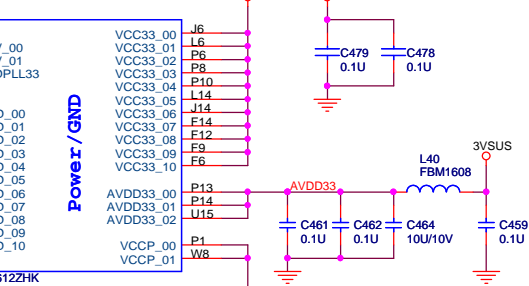
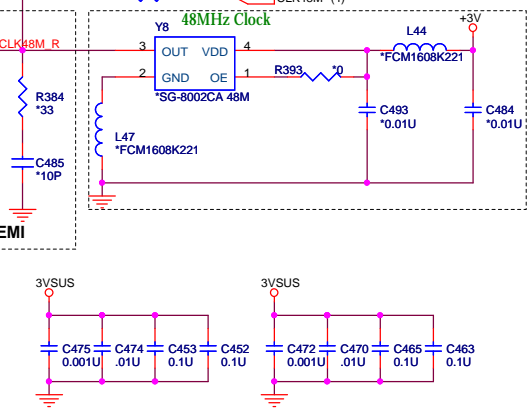
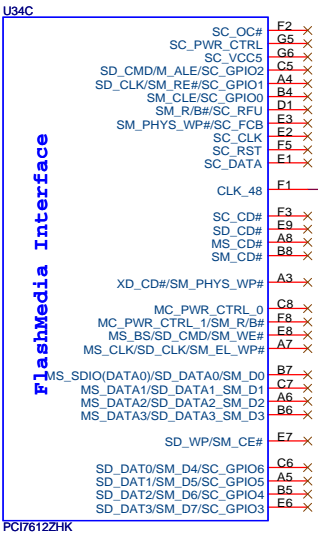
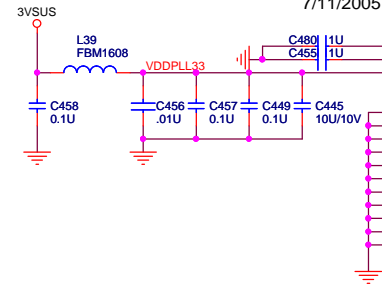
**PROJECT : OT1**  
**Quanta Computer Inc.**

Size B	Document Number	Rev 1A
<b>MINI CARD</b>		
Date: Wednesday, August 03, 2005	Sheet 19 of 38	





DB2 stage:  
Modify CN13#71.  
7/11/2005

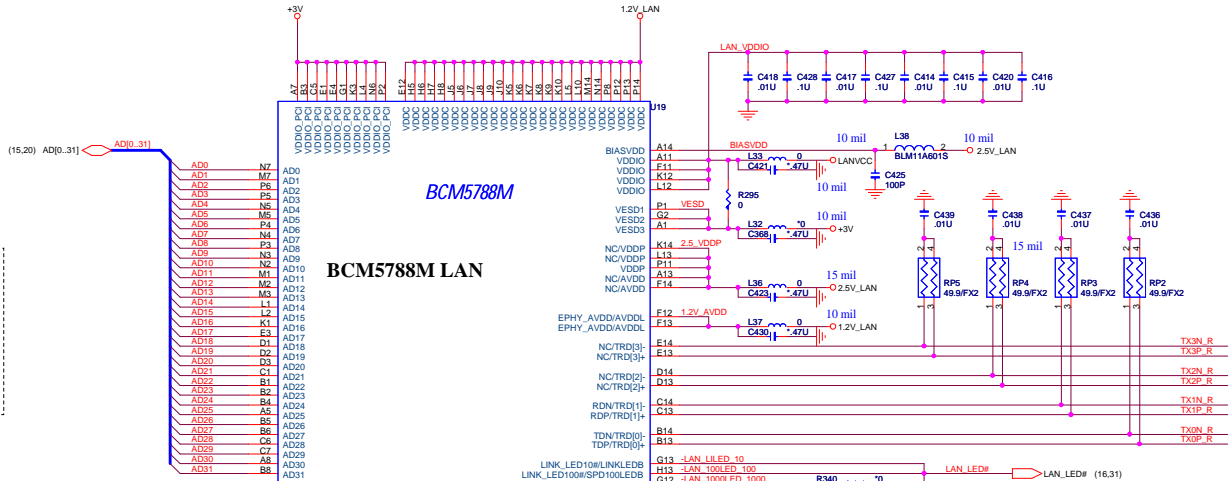


**PROJECT : OT1**

**Quanta Computer Inc.**

Size B	Document Number	Rev 1A
CardBus		
Date: Friday, July 29, 2005	Sheet 21 of 38	

# LAN



## BCM5788M LAN

## 15mm x 15mm BGA196

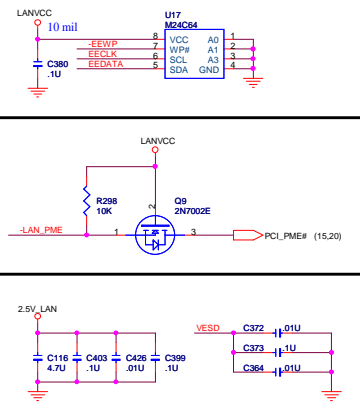
DB stage:add R339  
7/12/2005

40mils  
2.5V@88mA 0.564W

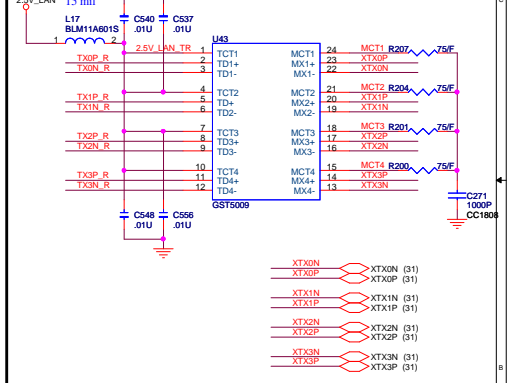
40mils  
1.2V@618mA 0.803W

1.5" AWAY FROM CHIP  
Use Philips BCP69-16, hfe=75-275

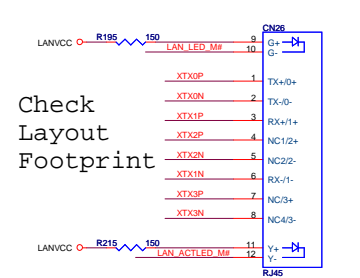
DB2 stage:add NIC power down circuitry



## Check Layout Footprint LAN Transformer

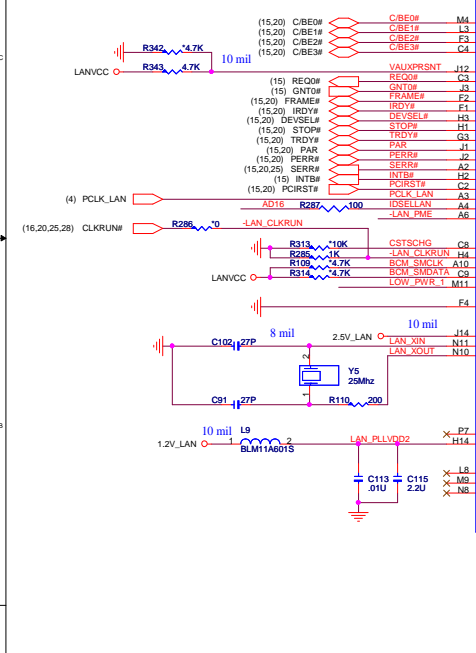


## RJ45 Connector



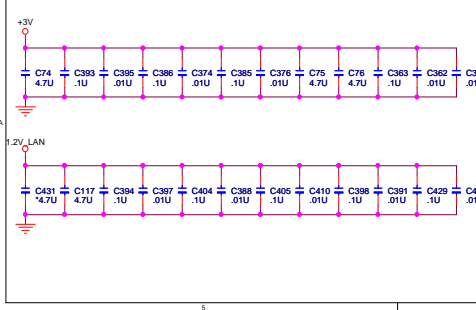
## Check Layout Footprint

DB2 stage:For test only .when do not mount, low power enable

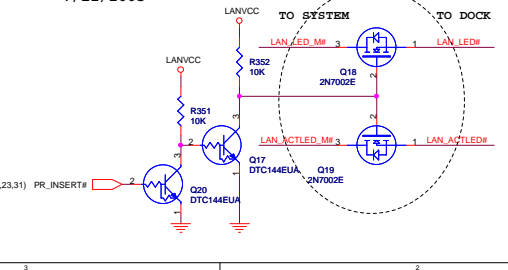


## LANVCC

DB2 stage:U16 power source change to 3V\_S5  
7/12/2005



DB2 stage:change Q18,Q19 PIN1,PIN3  
7/12/2005





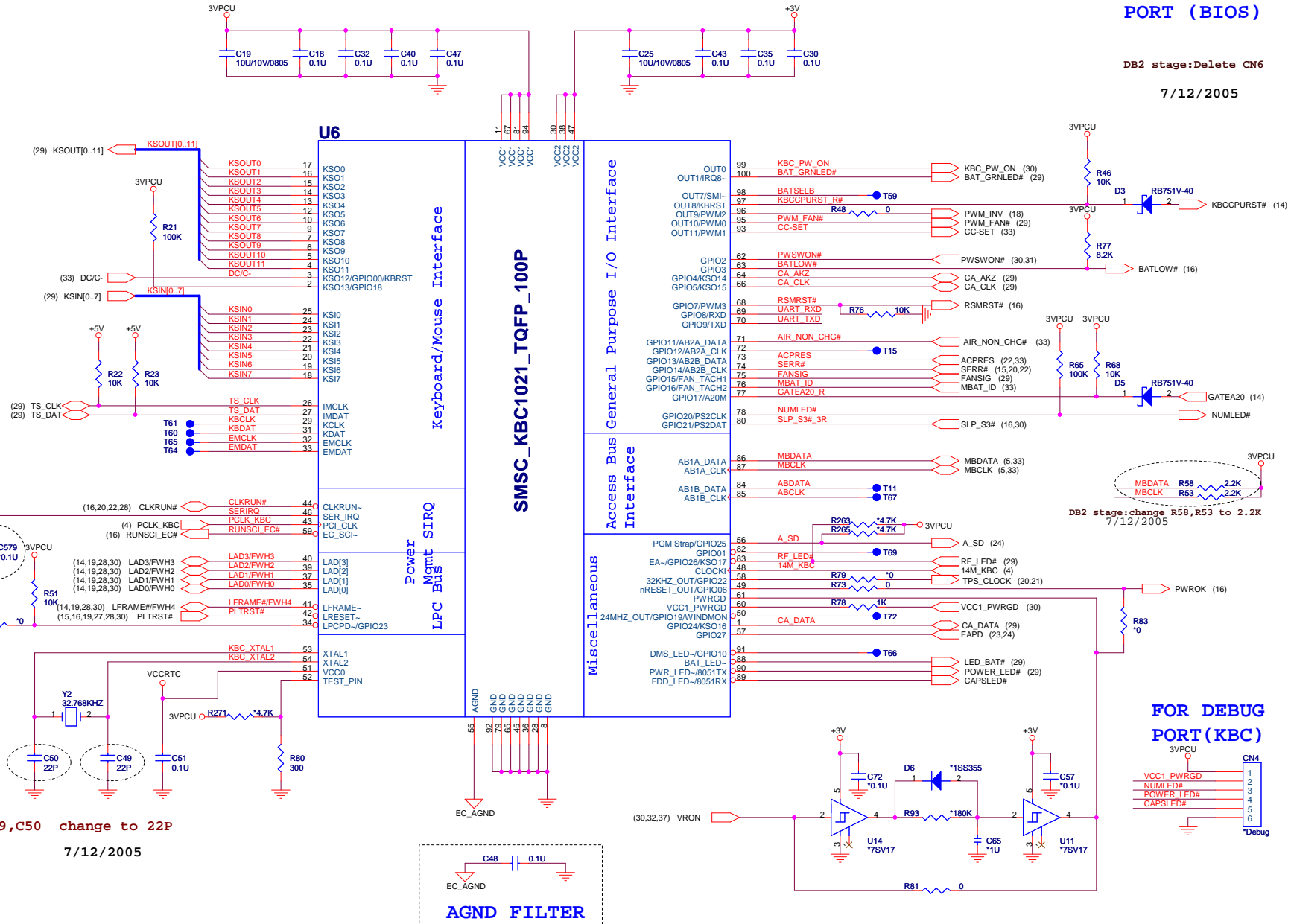
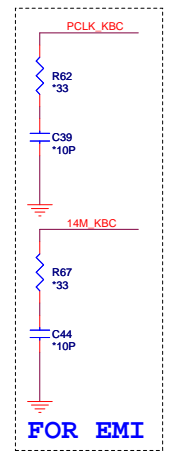




**FOR DEBUG PORT (BIOS)**

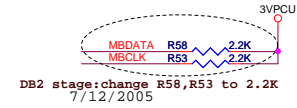
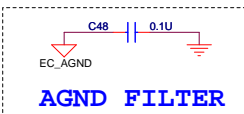
DB2 stage:Delete CN6

7/12/2005

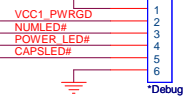


DB2 stage:C49,C50 change to 22P

7/12/2005

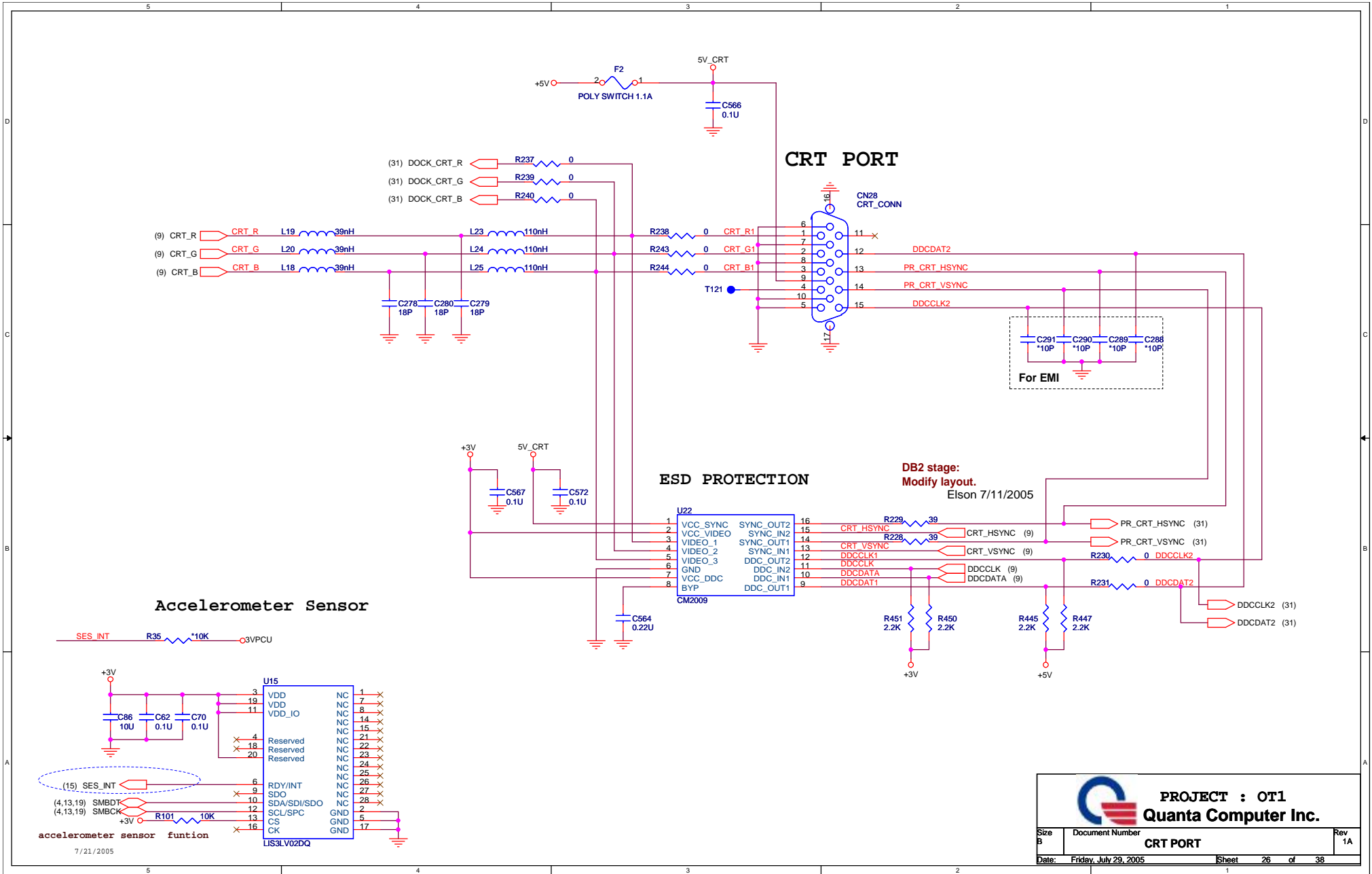


**FOR DEBUG PORT (KBC)**



**PROJECT : OT1**  
**Quanta Computer Inc.**

Size Custom	Document Number <b>SMSC_KBC1021</b>	Rev 1A
Date: Friday, July 29, 2005	Sheet 25	of 38

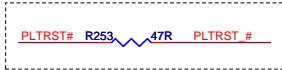
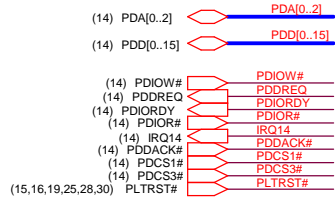


**PROJECT : OT1**  
**Quanta Computer Inc.**

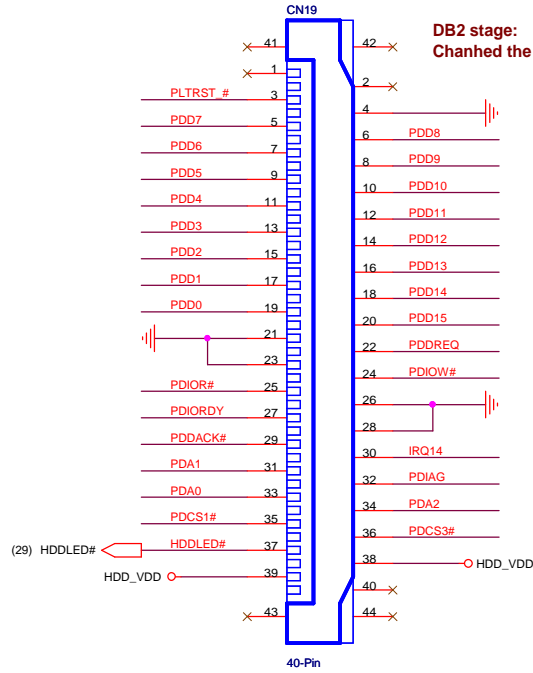
Size B	Document Number <b>CRT PORT</b>	Rev 1A
Date: Friday, July 29, 2005		Sheet 26 of 38

# HDD, CD-ROM

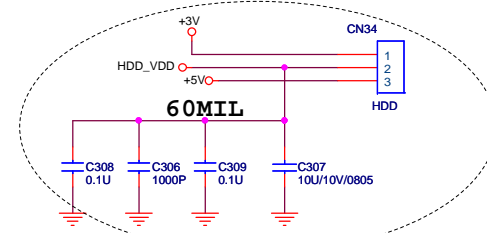
## 1.8 inch HDD CONNECTOR



DB2 stage:  
Chaned the footprint.  
7/11/2005

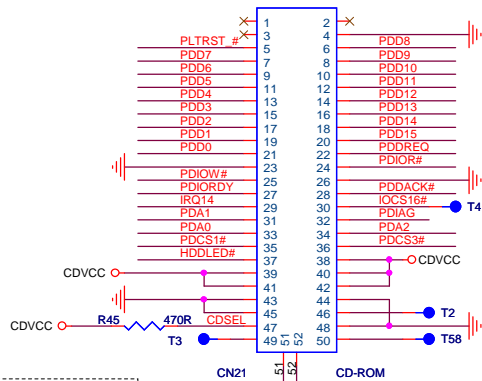


DB2 stage:  
Chaned the footprint.  
7/11/2005

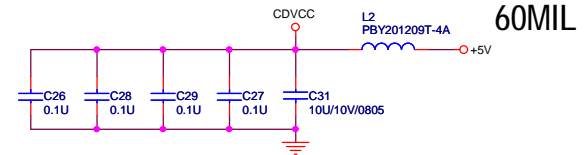


DB2 stage:DELETE L29,L30,ADD CN34  
7/21/2005

## CD-ROM



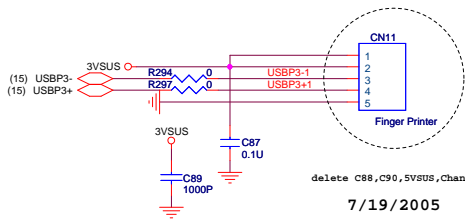
CDSEL  
--> High, Slave device



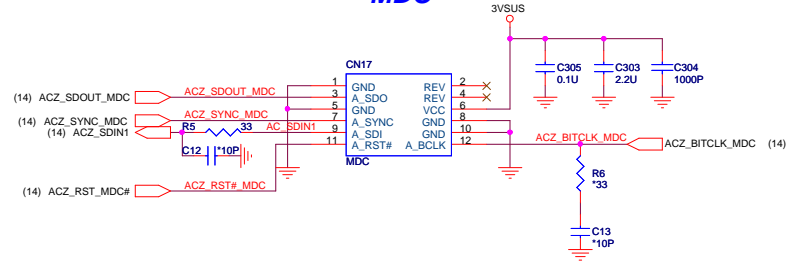
**PROJECT : OT1**  
**Quanta Computer Inc.**

Size B	Document Number	Rev 1A
<b>HDD&amp;ODD CONN.</b>		
Date: Friday, July 29, 2005	Sheet 27 of 38	

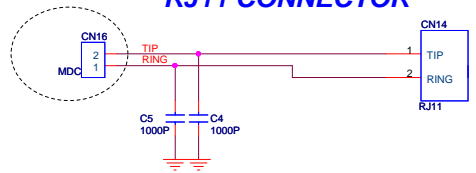
### FINGER PRINT



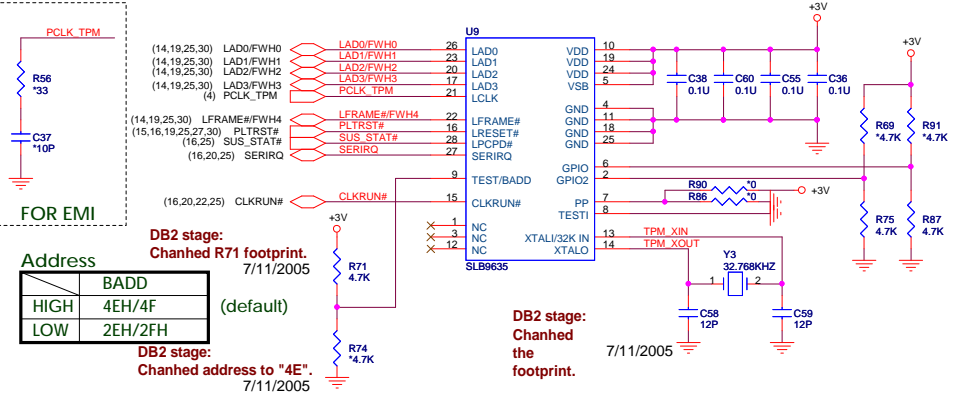
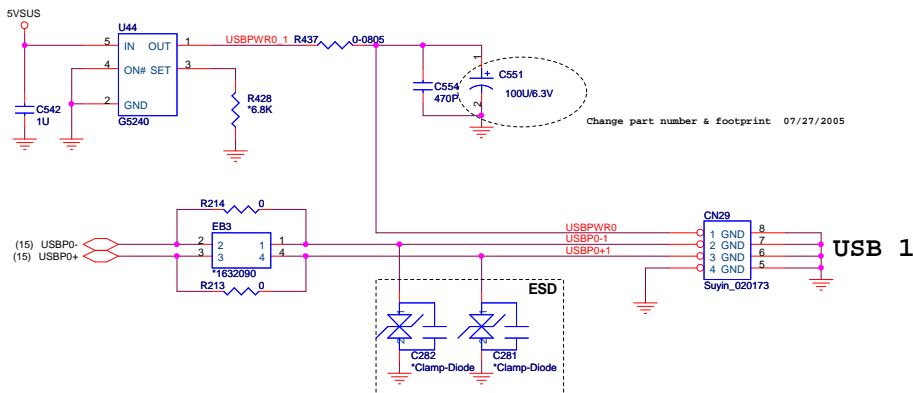
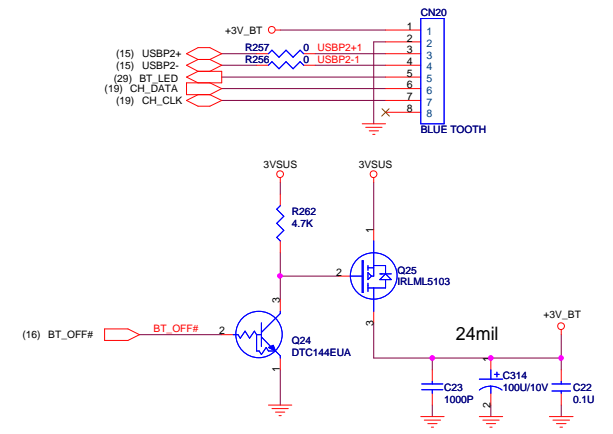
### MDC



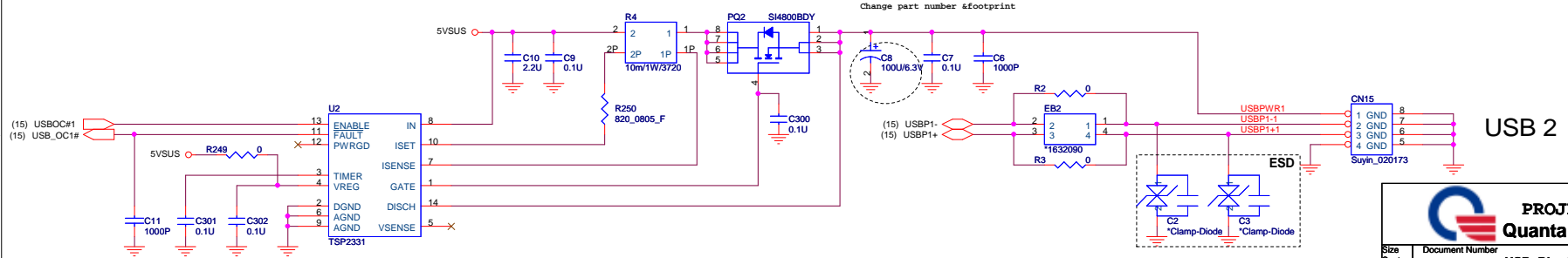
### RJ11 CONNECTOR



### BLUE TOOTH



### POWER USB (LEFT SIDE)

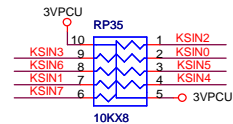
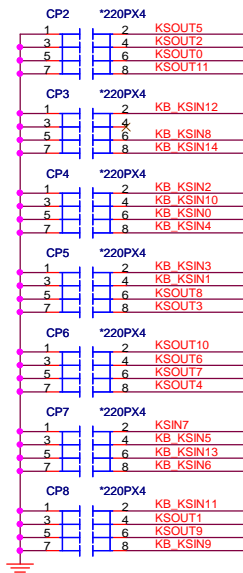
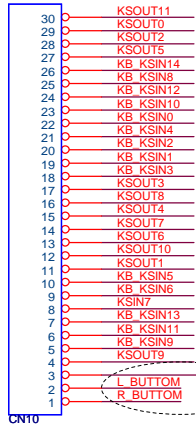


**PROJECT : OT1**  
**Quanta Computer Inc.**

Size: Custom  
Document Number: USB, Blue Tooth, Finger Print  
Date: Thursday, August 04, 2005  
Sheet: 28 of 38  
Rev: 1A

# KEYBOARD

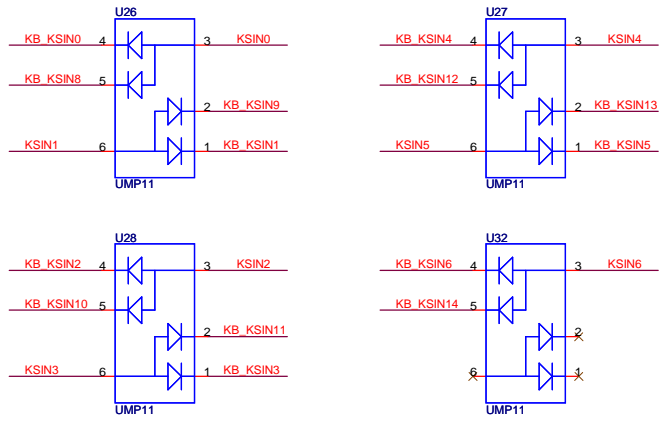
KEYBOARD



(25) KROUT[0..11] → KROUT[0..11]  
 (25) K SIN[0..7] → K SIN[0..7]

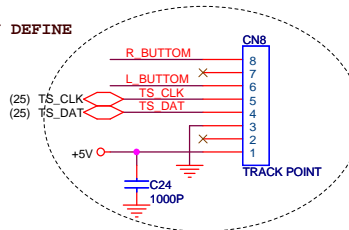
DB2 stage:add Pin1,2,3  
 7/15/2005  
 Change CN10 PINDEFINE  
 7/21/2005

## Check K/B Matrix

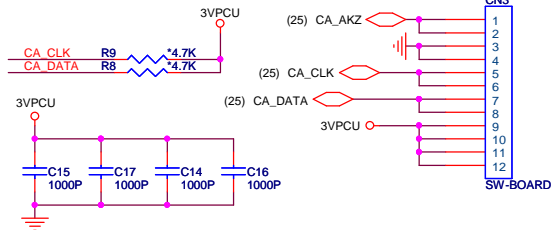


# TRACK POINT

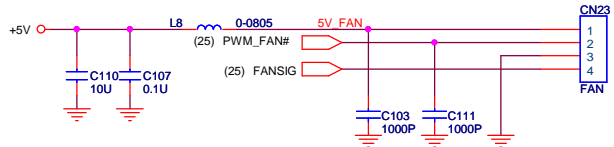
DB2 stage:add Pin1,3  
 7/21/2005  
 Change CN8 PIN DEFINE  
 7/27/2005



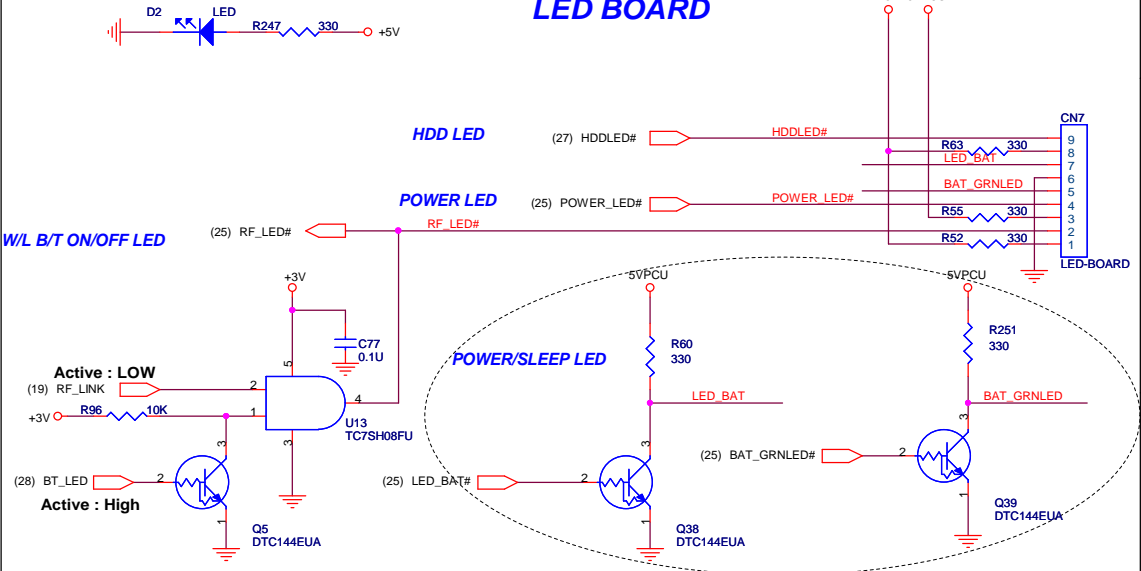
# APPLICATION BUTTON BOARD




# FAN OUT PWM CONTROL



# LED BOARD



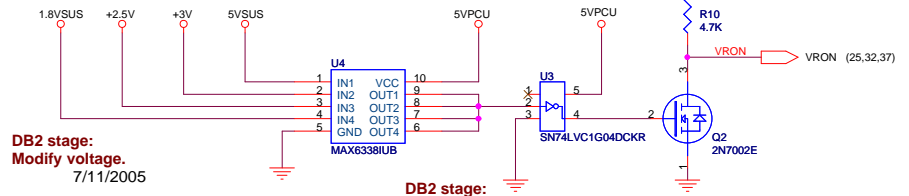
DB2 stage:add Q38 ,Q39 for Battery LED change to common cathode  
 7/12/2005



**PROJECT : OT1**  
**Quanta Computer Inc.**

Size B	Document Number	Rev
<b>FAN, KEYBOARD, TRACK POINT, LEDs</b>		1A
Date: Friday, July 29, 2005	Sheet 29 of 38	1

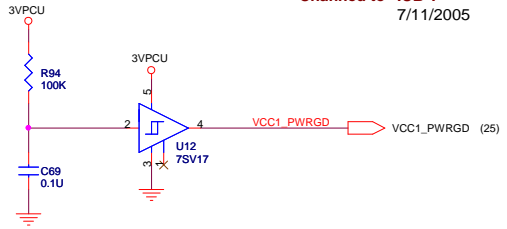
# POWER SEQUENCE



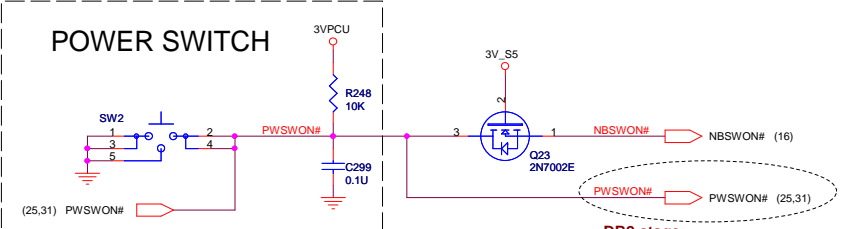
DB2 stage:  
Modify voltage.  
7/11/2005

DB2 stage:  
Chanched to "IUB".  
7/11/2005

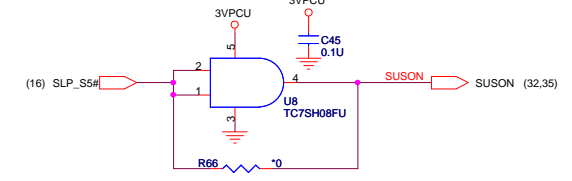
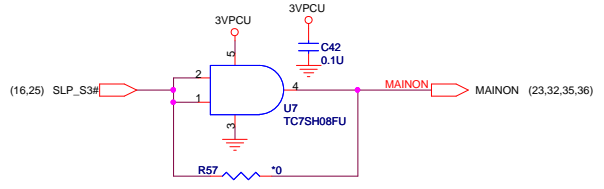
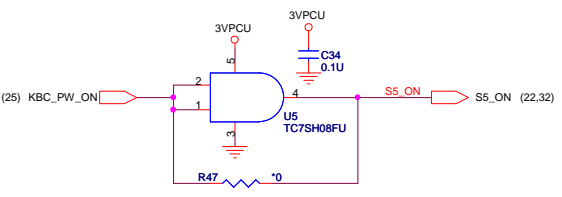
DB2 stage:  
Del R11,R12,R13,R14.  
7/11/2005



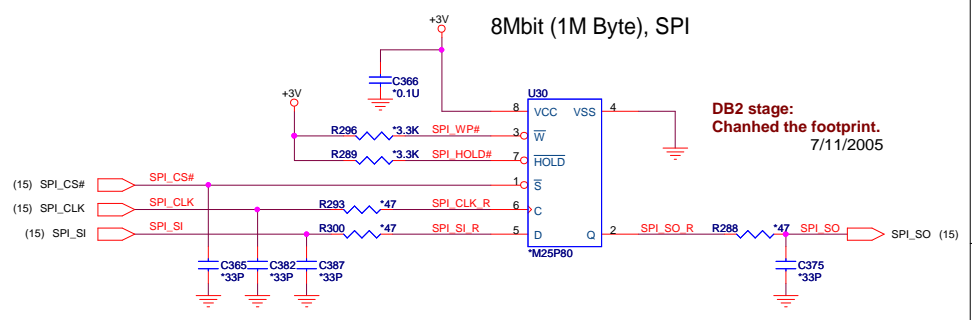
# POWER SWITCH



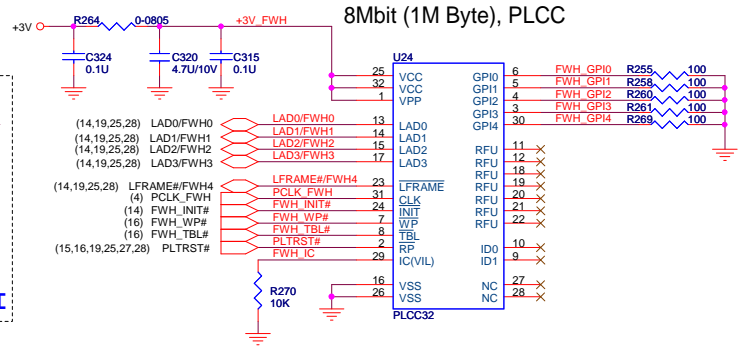
DB2 stage:  
Modify the net.  
7/11/2005



# FLASH ROM(BIOS)



DB2 stage:  
Chanched the footprint.  
7/11/2005



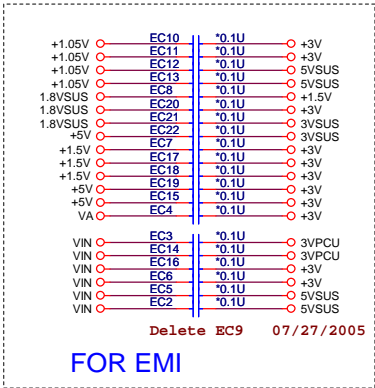
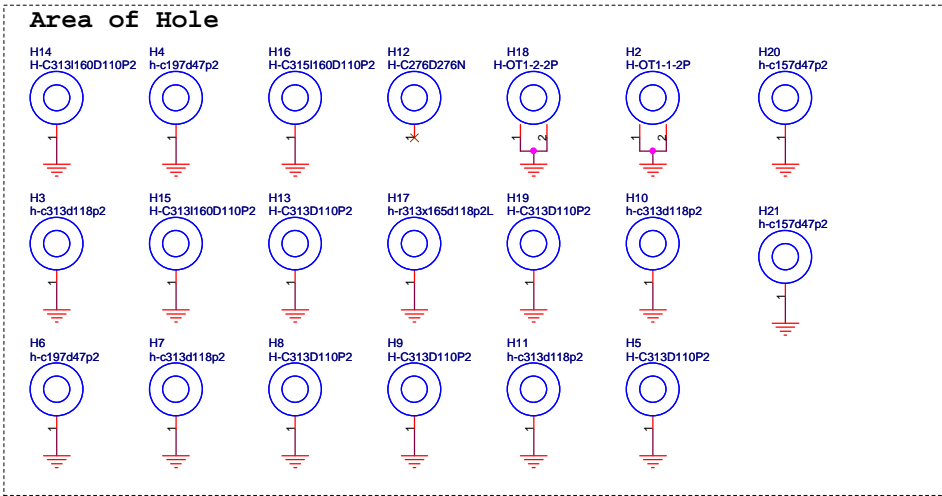
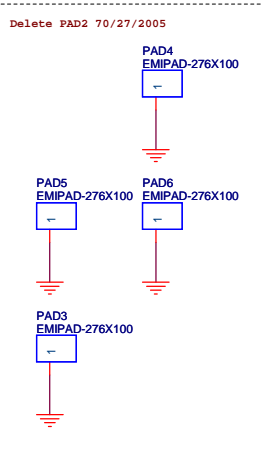
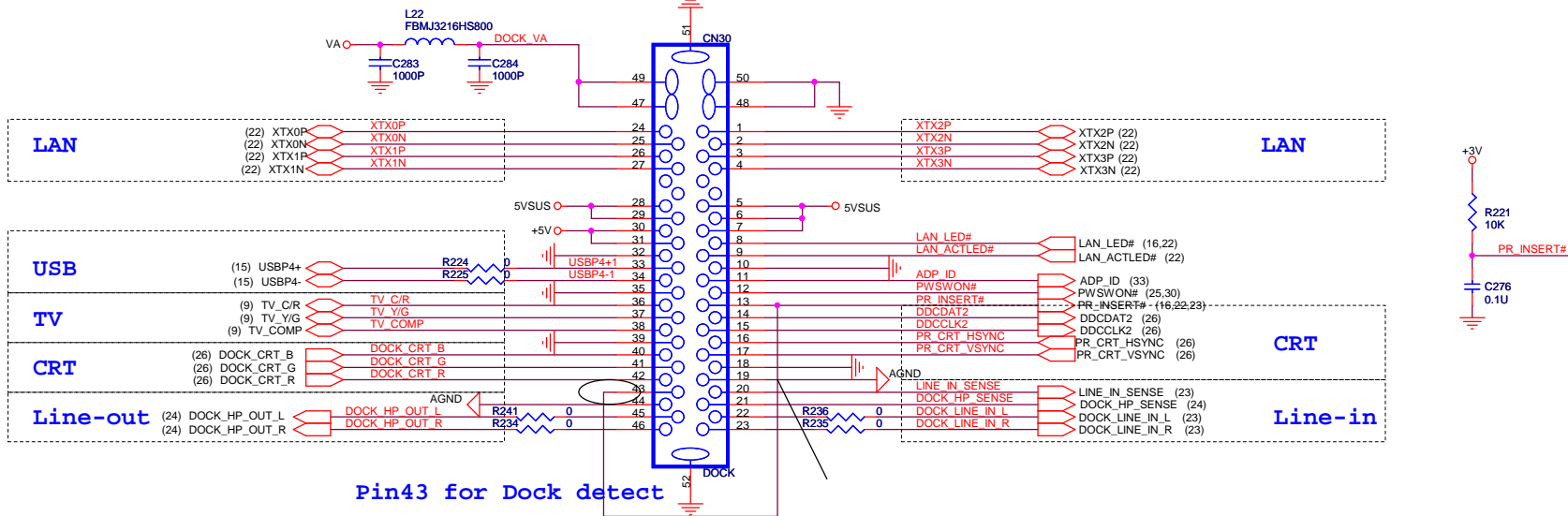
FOR EMI

DB2 stage:  
Del U25.  
7/11/2005

PROJECT : OT1  
Quanta Computer Inc.

Size Custom	Document Number <b>POWER SEQUENCE / LPC BIOS</b>	Rev 1A
Date: Friday, July 29, 2005	Sheet 30	of 38

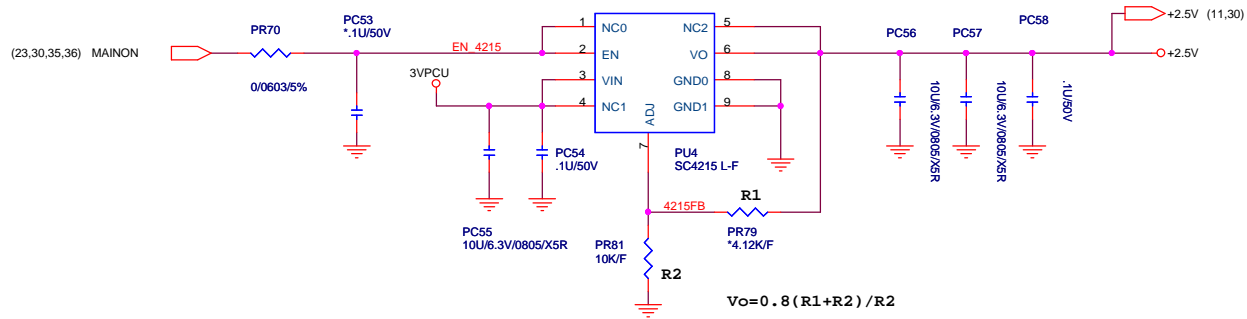
# DOCKING BOARD CONNECT



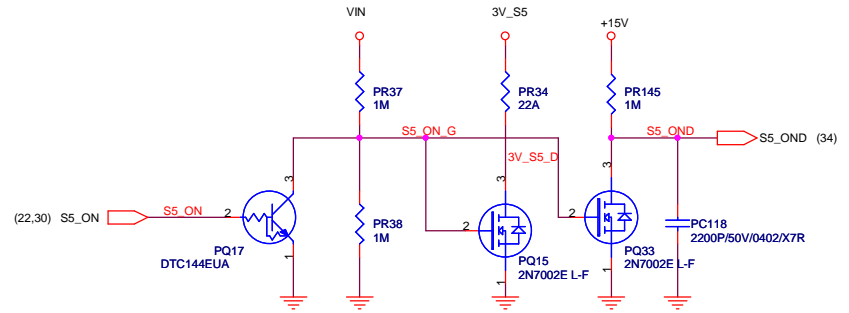
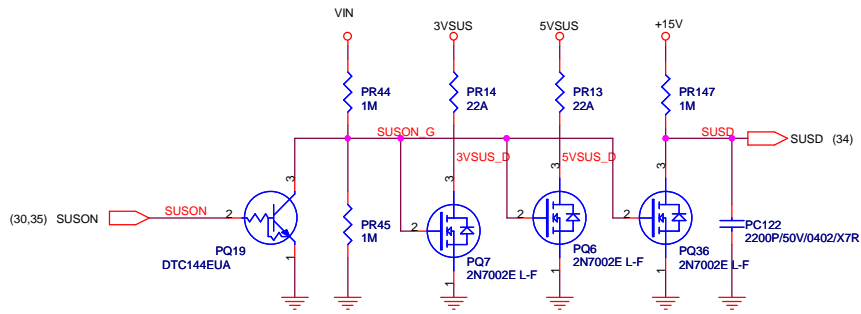
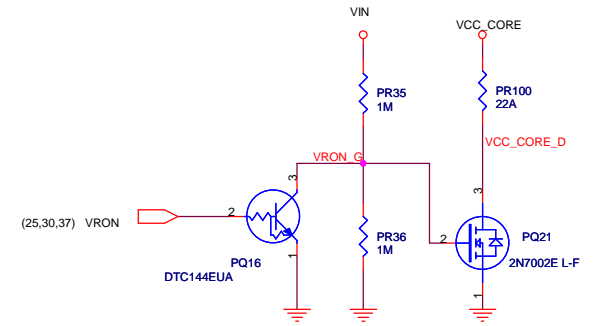
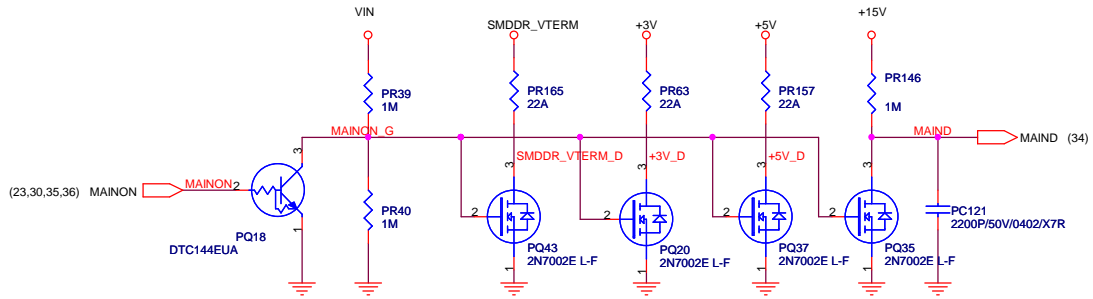
**PROJECT : OT1**  
**Quanta Computer Inc.**

Size B Document Number **CABLE DOCKING** Rev 1A

Date: Friday, July 29, 2005 Sheet 31 of 38



**2.5V**  
**0.6A**  
**S0**



**PROJECT : OT1**  
**Quanta Computer Inc.**

Size	Document Number	Rev
Custom	<b>+2.5V/DISCHARGE</b>	1A
Date:	Friday, July 29, 2005	Sheet 32 of 38



**ADAPTER 65W 19.5 Volts 3.33A**  
**ADAPTER 50W 19.5 Volts 2.56A**

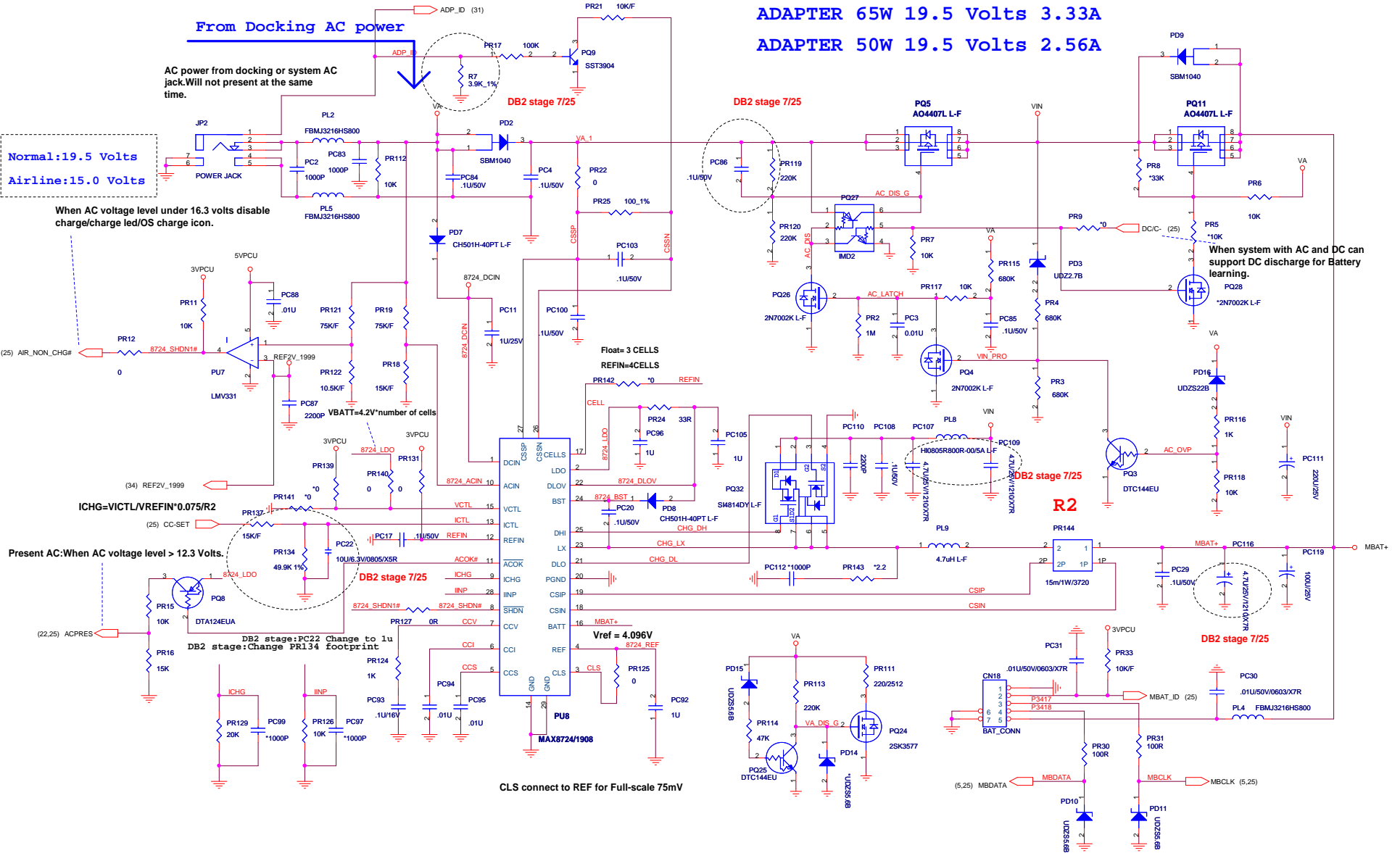
From Docking AC power

AC power from docking or system AC jack. Will not present at the same time.

Normal: 19.5 Volts  
 Airline: 15.0 Volts

When AC voltage level under 16.3 volts disable charge/charge led/OS charge icon.

When system with AC and DC can support DC discharge for Battery learning.



$ICHG = VICTL / VREFIN * 0.075 / R2$

Present AC: When AC voltage level > 12.3 Volts.

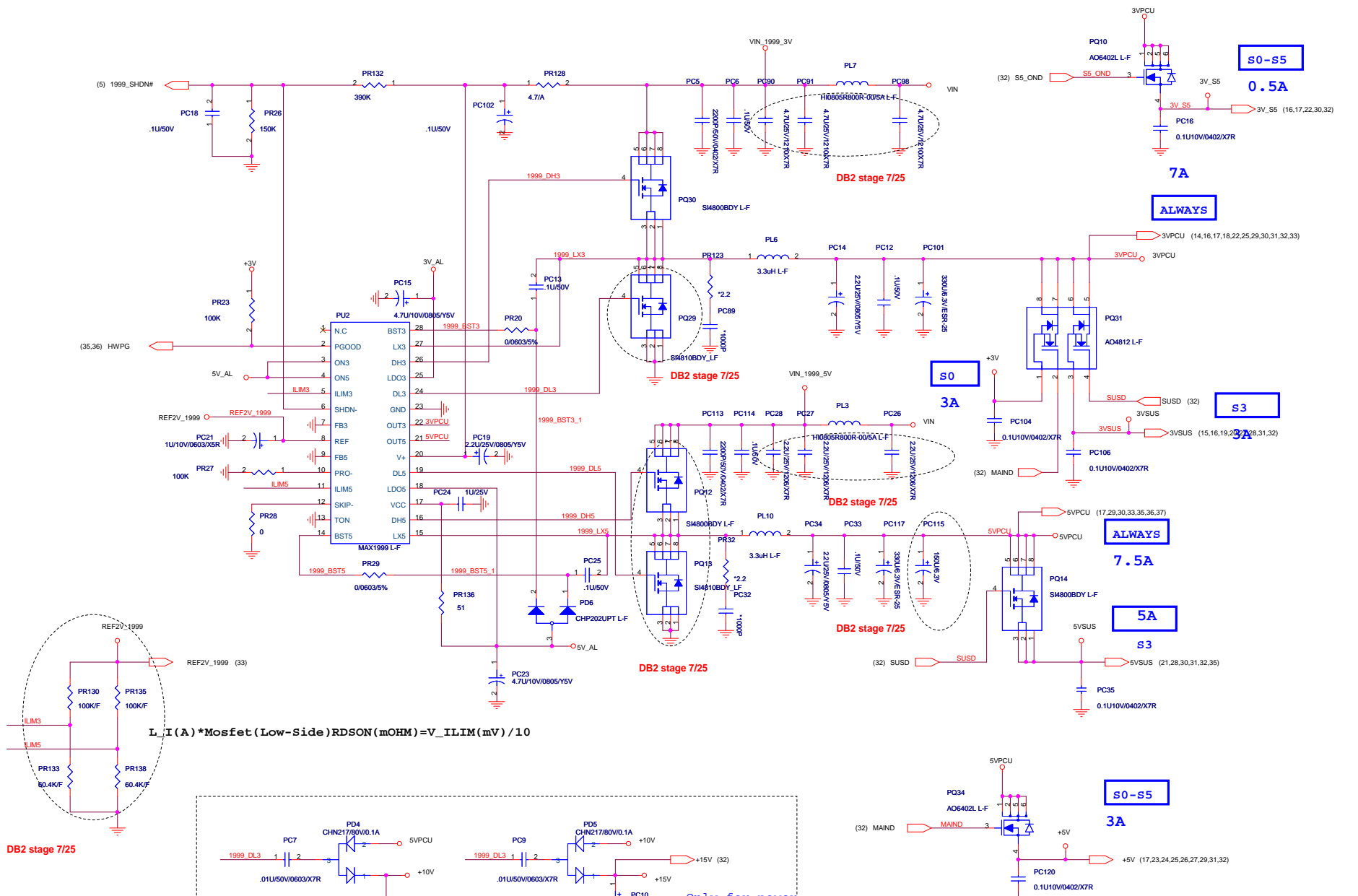
Float = 3 CELLS  
 REFIN = 4 CELLS

Vref = 4.096V

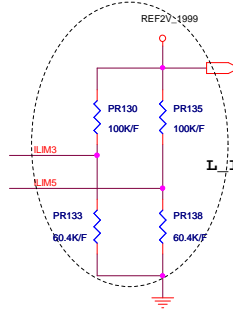
CLS connect to REF for Full-scale 75mV

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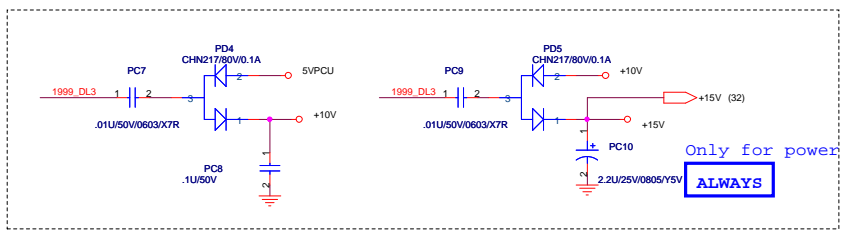
Size: Custom  
 Document Number: CHARGING  
 Date: Friday, July 29, 2005  
 Sheet: 33 of 38  
 Rev: 1A



$L_I(A) * \text{Mosfet (Low-Side) RDSON (m\Omega)} = V\_ILIM(mV) / 10$



DB2 stage 7/25



Only for power ALWAYS

S0-S5  
0.5A

ALWAYS

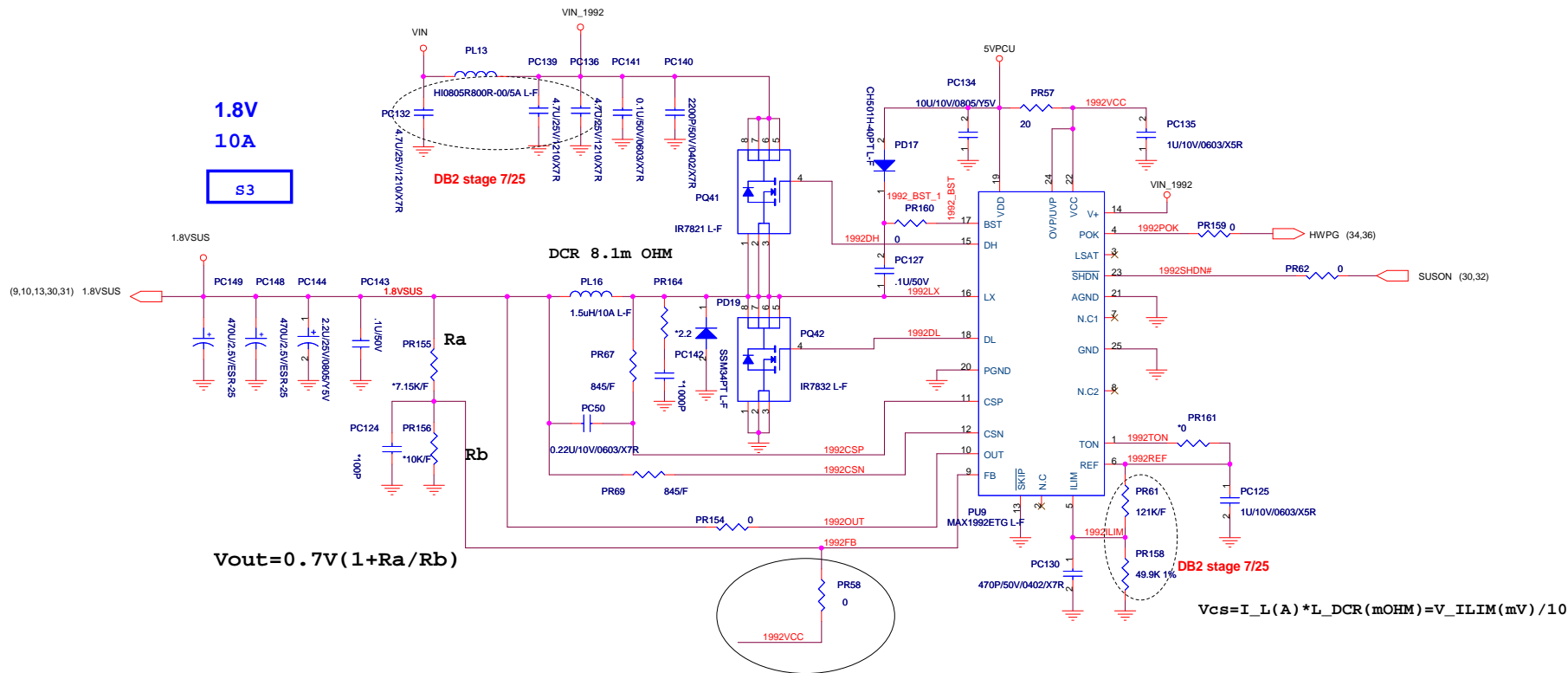
S0  
3A

S3  
3A

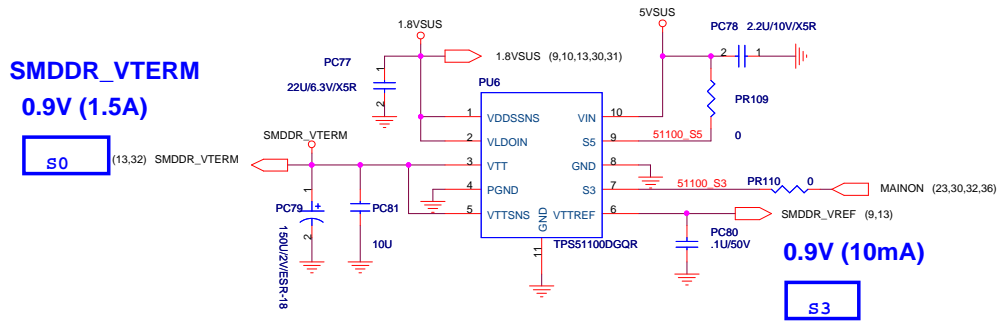
ALWAYS  
7.5A

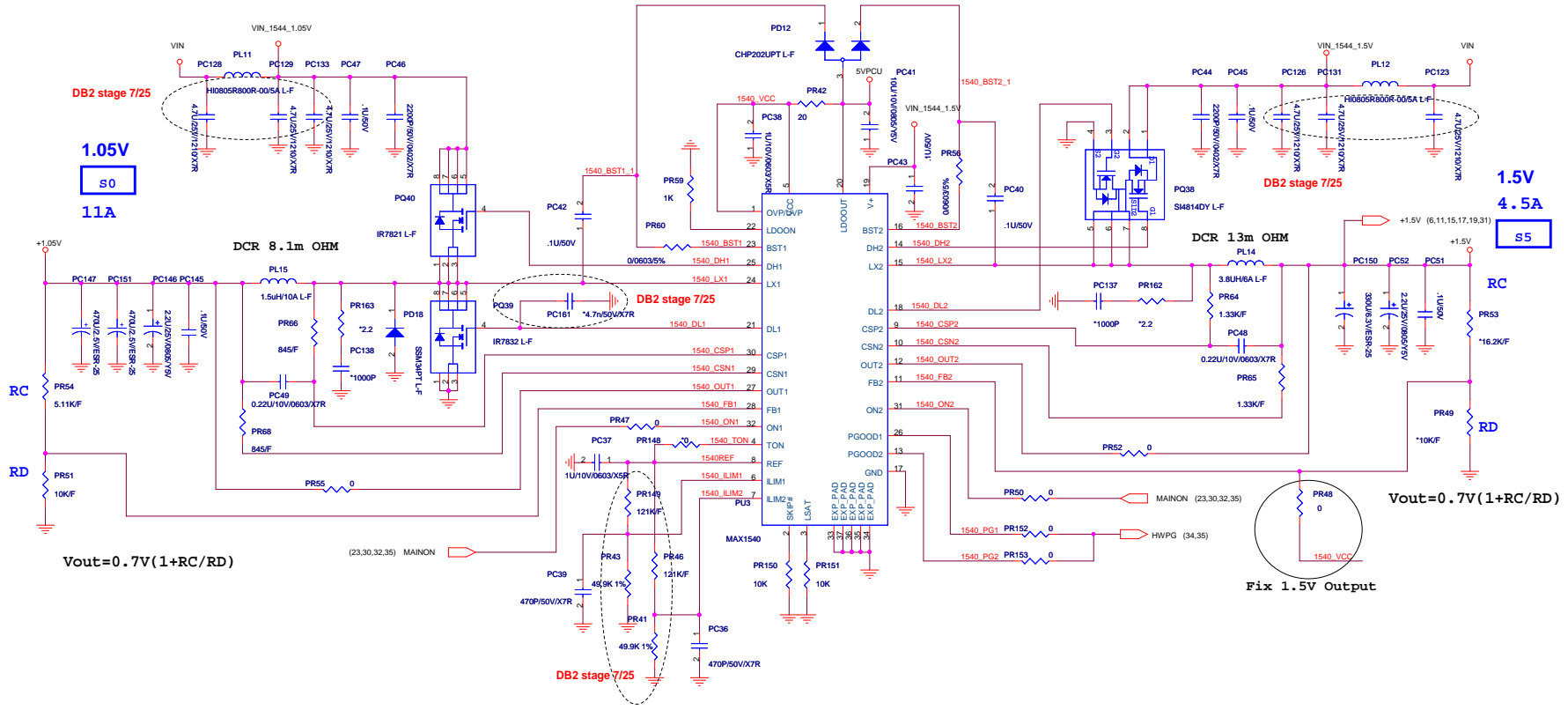
5A  
S3

S0-S5  
3A



**Fix 1.8V Output**

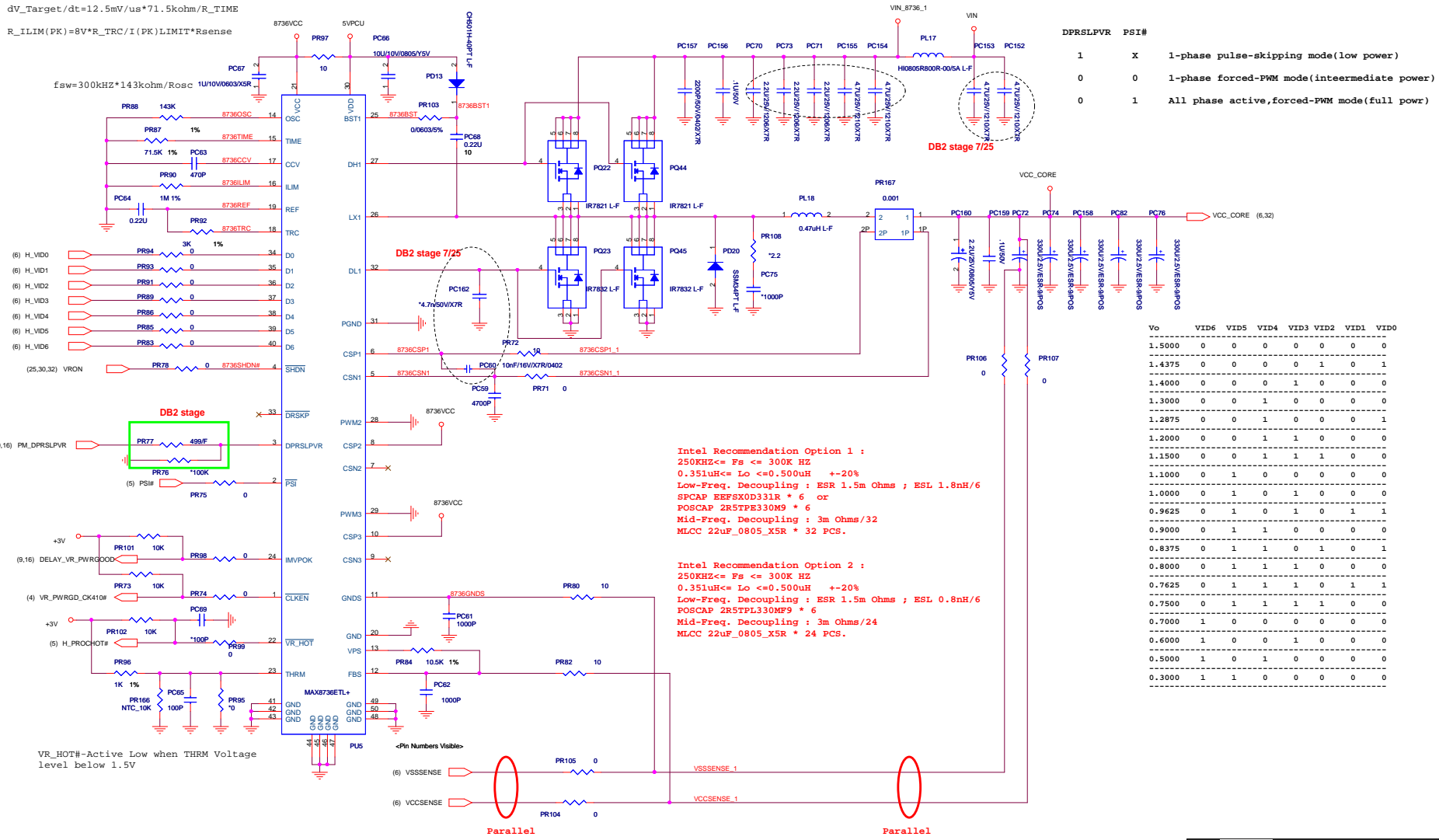




$$V_{cs} = I_L(A) * L_{DCR}(mOHM) = V_{ILIM}(mV) / 10$$

DPRSLPVR	DPRSTP#	PSI#	State	CPU Current
1	0	0	Deeper Sleep	< 3A
1	0	1	Deeper Sleep	> 3A
0	1	0	Active Mode	< 18A
0	1	1	Active Mode	> 15A

$dV_{Target}/dt = 12.5mV/us * 71.5kohm/R\_TIME$   
 $R\_ILIM(PK) = 8V * R\_TRC / I(PK) LIMIT * R_{sense}$



DPRSLPVR	PSI#	State
1	X	1-phase pulse-skipping mode (low power)
0	0	1-phase forced-PWM mode (intermediate power)
0	1	All phase active, forced-PWM mode (full power)

Vo	VID6	VID5	VID4	VID3	VID2	VID1	VID0
1.5000	0	0	0	0	0	0	0
1.4375	0	0	0	0	1	0	1
1.4000	0	0	0	1	0	0	0
1.3000	0	0	1	0	0	0	0
1.2875	0	0	1	0	0	0	1
1.2000	0	0	1	1	0	0	0
1.1500	0	0	1	1	1	0	0
1.1000	0	1	0	0	0	0	0
1.0000	0	1	0	1	0	0	0
0.9625	0	1	0	1	0	1	1
0.9000	0	1	1	0	0	0	0
0.8375	0	1	1	0	1	0	1
0.8000	0	1	1	1	0	0	0
0.7625	0	1	1	1	0	1	1
0.7500	0	1	1	1	1	0	0
0.7000	1	0	0	0	0	0	0
0.6000	1	0	0	1	0	0	0
0.5000	1	0	1	0	0	0	0
0.3000	1	1	0	0	0	0	0

**Intel Recommendation Option 1 :**  
 250KHZ <= Fs <= 300K HZ  
 0.351uH <= Lo <= 0.500uH +-20%  
 Low-Freq. Decoupling : ESR 1.5m Ohms ; ESL 1.8nH/6  
 SPCAP EEP5X0D331R \* 6 or  
 POSCAP 2R5TPE330M9 \* 6  
 Mid-Freq. Decoupling : 3m Ohms/32  
 MLCC 22uF\_0805\_X5R \* 32 PCS.

**Intel Recommendation Option 2 :**  
 250KHZ <= Fs <= 300K HZ  
 0.351uH <= Lo <= 0.500uH +-20%  
 Low-Freq. Decoupling : ESR 1.5m Ohms ; ESL 0.8nH/6  
 POSCAP 2R5TPL330MF9 \* 6  
 Mid-Freq. Decoupling : 3m Ohms/24  
 MLCC 22uF\_0805\_X5R \* 24 PCS.

<Pin Numbers Visible>

Parallel

Parallel

**PROJECT : OT1**  
**Quanta Computer Inc.**

Size: Document Number  
 Custom: MAX9736ETL+(CPU)  
 Date: Friday, July 29, 2006 Sheet 37 of 38

