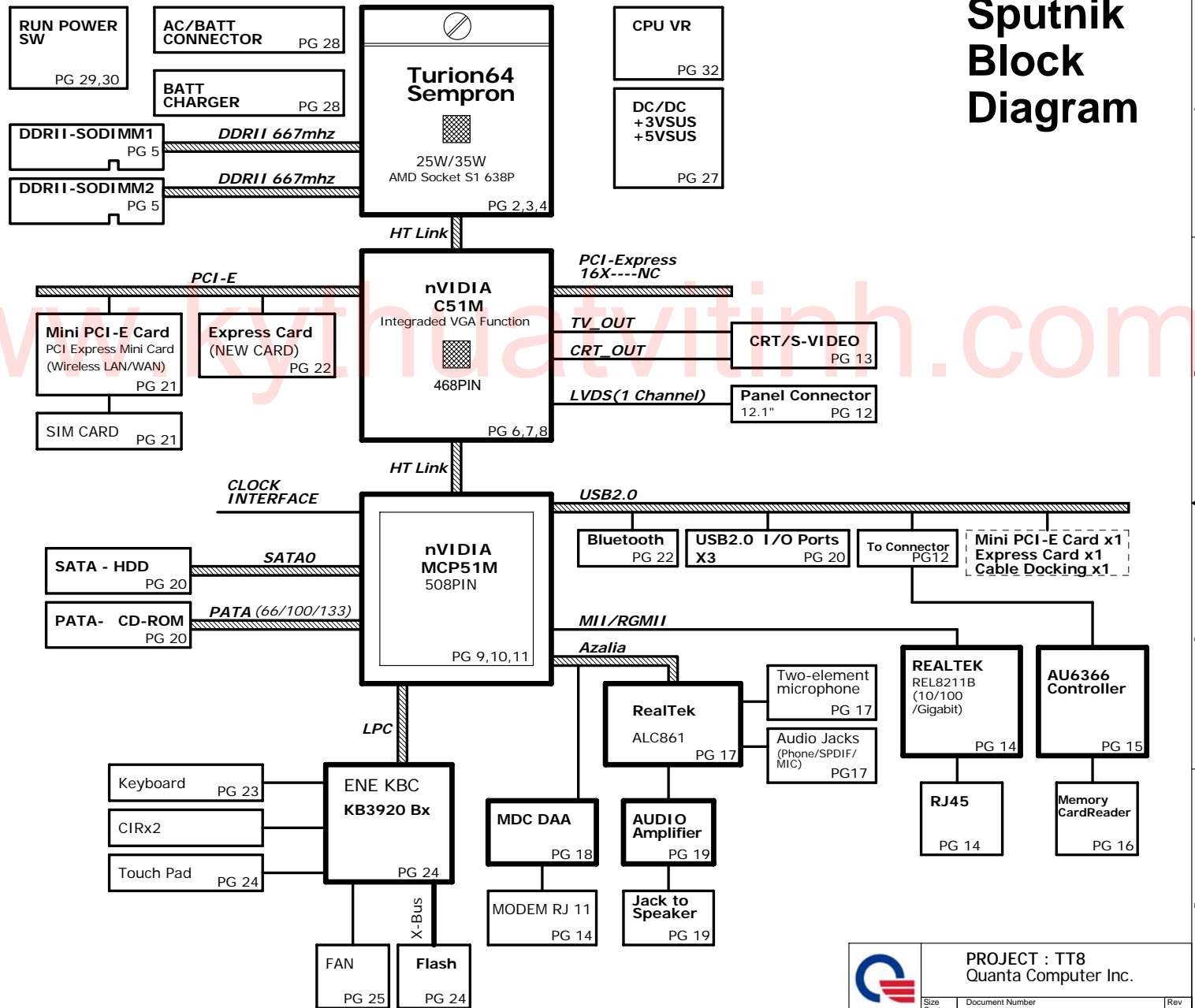


Sputnik Block Diagram

PCB STACK UP

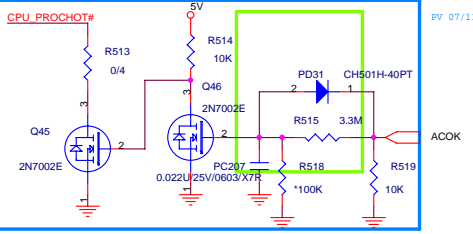
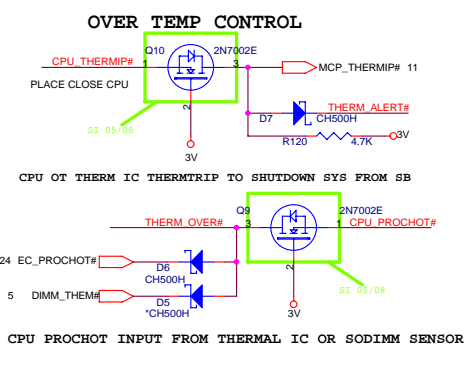
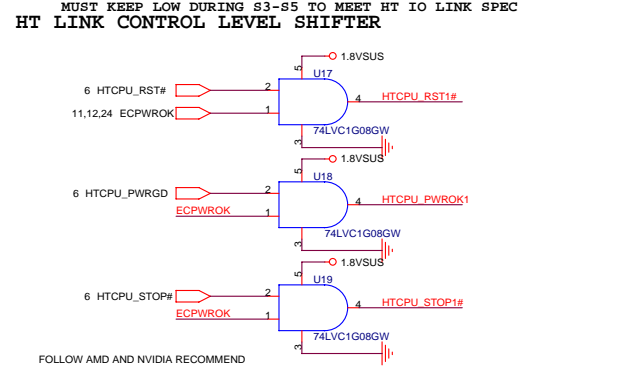
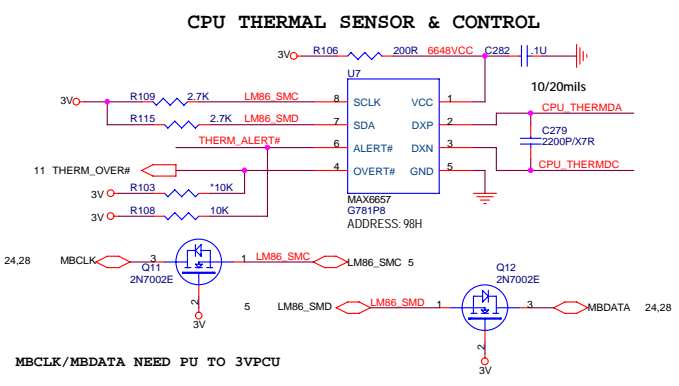
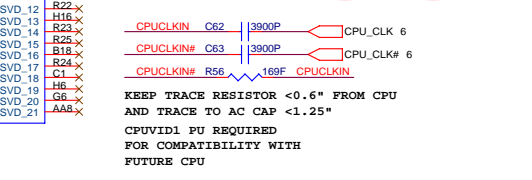
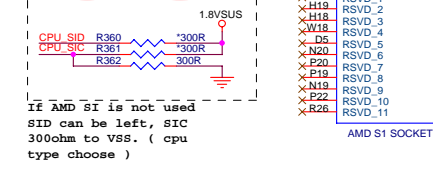
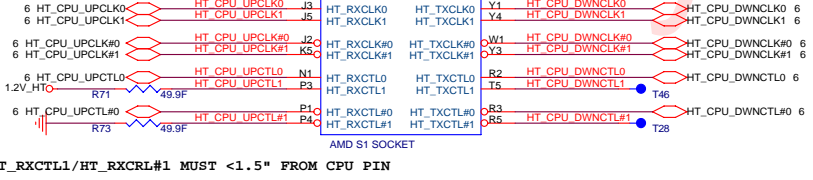
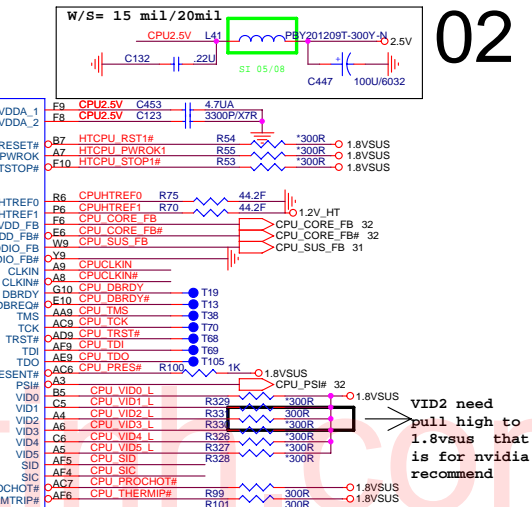
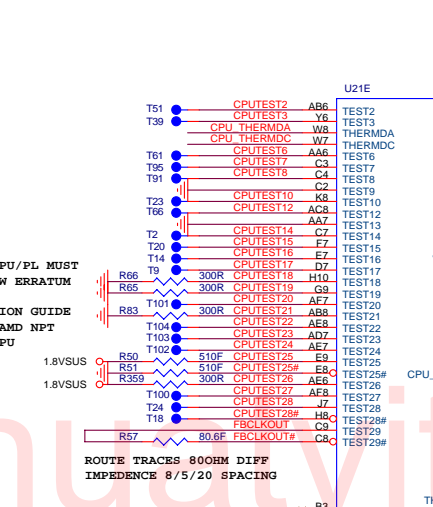
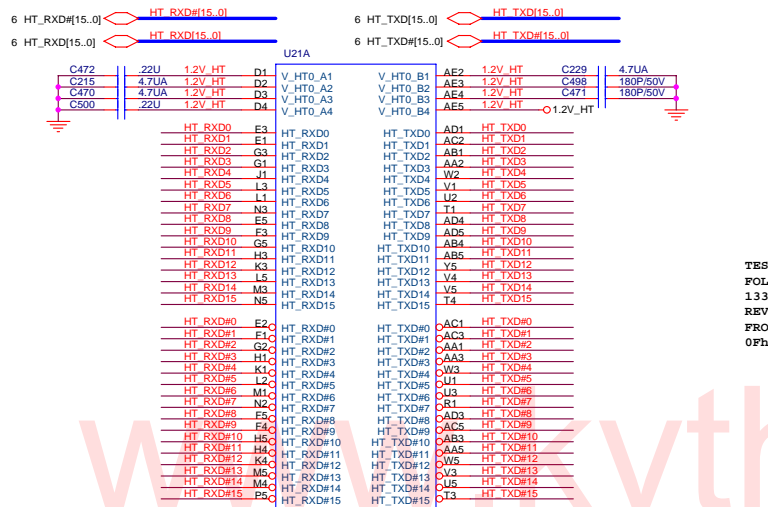
- LAYER 1 : TOP
- LAYER 2 : SGND1
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : IN3
- LAYER 7 : SGND2
- LAYER 8 : BOT

- ### Cable Docking
- TV_OUT
 - VGA
 - RJ-45
 - CIR/Pwr btn
 - SPDIF Out
 - Stereo MIC
 - Headphone Jack
 - USB Port
 - VOL Cntr
- PG 25



VAULE DEFINE
 A=0603,B=0805,C=1206,F=1%,
 OTHER IS 0402

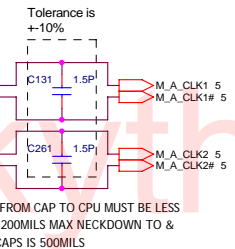
EXAMPLE
 10R=10ohm(0402)
 10A=10ohm(0603)
 10B=10ohm(0805)
 10C=10ohm(1206)
 10/F=10ohm(0402 and 1%)



U21B

Table of pin assignments for U21B, including signals like M_A DQ63, M_A DQ62, M_A DQ61, M_A DQ60, M_A DQ59, M_A DQ58, M_A DQ57, M_A DQ56, M_A DQ55, M_A DQ54, M_A DQ53, M_A DQ52, M_A DQ51, M_A DQ50, M_A DQ49, M_A DQ48, M_A DQ47, M_A DQ46, M_A DQ45, M_A DQ44, M_A DQ43, M_A DQ42, M_A DQ41, M_A DQ40, M_A DQ39, M_A DQ38, M_A DQ37, M_A DQ36, M_A DQ35, M_A DQ34, M_A DQ33, M_A DQ32, M_A DQ31, M_A DQ30, M_A DQ29, M_A DQ28, M_A DQ27, M_A DQ26, M_A DQ25, M_A DQ24, M_A DQ23, M_A DQ22, M_A DQ21, M_A DQ20, M_A DQ19, M_A DQ18, M_A DQ17, M_A DQ16, M_A DQ15, M_A DQ14, M_A DQ13, M_A DQ12, M_A DQ11, M_A DQ10, M_A DQ9, M_A DQ8, M_A DQ7, M_A DQ6, M_A DQ5, M_A DQ4, M_A DQ3, M_A DQ2, M_A DQ1, M_A DQ0.

Table of pin assignments for U21B, including signals like MA_DM[7:0], MA_DM[6], MA_DM[5], MA_DM[4], MA_DM[3], MA_DM[2], MA_DM[1], MA_DM[0], MA_DQS[7:0], MA_DQS[6], MA_DQS[5], MA_DQS[4], MA_DQS[3], MA_DQS[2], MA_DQS[1], MA_DQS[0], MA_DQ[7:0], MA_DQ[6], MA_DQ[5], MA_DQ[4], MA_DQ[3], MA_DQ[2], MA_DQ[1], MA_DQ[0], MA_ADD[15:0], MA_ADD[14], MA_ADD[13], MA_ADD[12], MA_ADD[11], MA_ADD[10], MA_ADD[9], MA_ADD[8], MA_ADD[7], MA_ADD[6], MA_ADD[5], MA_ADD[4], MA_ADD[3], MA_ADD[2], MA_ADD[1], MA_ADD[0], MA_BANK[2], MA_BANK[1], MA_BANK[0], MA_RAS#, MA_CAS#, MA_WE#, MA_CS[3:0], MA_CS[2], MA_CS[1], MA_CS[0], MA_CKE[1], MA_CKE[0], MA_ODT[1], MA_ODT[0].

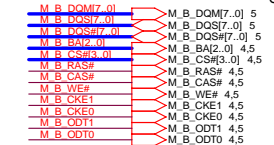
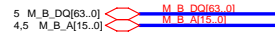
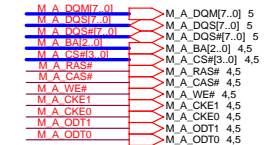
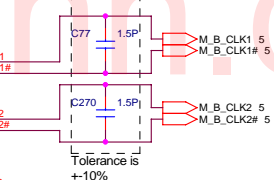


U21C

Table of pin assignments for U21C, including signals like M_B DQ63, M_B DQ62, M_B DQ61, M_B DQ60, M_B DQ59, M_B DQ58, M_B DQ57, M_B DQ56, M_B DQ55, M_B DQ54, M_B DQ53, M_B DQ52, M_B DQ51, M_B DQ50, M_B DQ49, M_B DQ48, M_B DQ47, M_B DQ46, M_B DQ45, M_B DQ44, M_B DQ43, M_B DQ42, M_B DQ41, M_B DQ40, M_B DQ39, M_B DQ38, M_B DQ37, M_B DQ36, M_B DQ35, M_B DQ34, M_B DQ33, M_B DQ32, M_B DQ31, M_B DQ30, M_B DQ29, M_B DQ28, M_B DQ27, M_B DQ26, M_B DQ25, M_B DQ24, M_B DQ23, M_B DQ22, M_B DQ21, M_B DQ20, M_B DQ19, M_B DQ18, M_B DQ17, M_B DQ16, M_B DQ15, M_B DQ14, M_B DQ13, M_B DQ12, M_B DQ11, M_B DQ10, M_B DQ9, M_B DQ8, M_B DQ7, M_B DQ6, M_B DQ5, M_B DQ4, M_B DQ3, M_B DQ2, M_B DQ1, M_B DQ0.

Table of pin assignments for U21C, including signals like MB_DM[7:0], MB_DM[6], MB_DM[5], MB_DM[4], MB_DM[3], MB_DM[2], MB_DM[1], MB_DM[0], MB_DQS[7:0], MB_DQS[6], MB_DQS[5], MB_DQS[4], MB_DQS[3], MB_DQS[2], MB_DQS[1], MB_DQS[0], MB_DQ[7:0], MB_DQ[6], MB_DQ[5], MB_DQ[4], MB_DQ[3], MB_DQ[2], MB_DQ[1], MB_DQ[0], MB_ADD[15:0], MB_ADD[14], MB_ADD[13], MB_ADD[12], MB_ADD[11], MB_ADD[10], MB_ADD[9], MB_ADD[8], MB_ADD[7], MB_ADD[6], MB_ADD[5], MB_ADD[4], MB_ADD[3], MB_ADD[2], MB_ADD[1], MB_ADD[0], MB_BANK[2], MB_BANK[1], MB_BANK[0], MB_RAS#, MB_CAS#, MB_WE#, MB_CS[3:0], MB_CS[2], MB_CS[1], MB_CS[0], MB_CKE[1], MB_CKE[0], MB_ODT[1], MB_ODT[0], VTT Sense, V_M_VREF, M_ZN, M_ZP.

TRACE FROM CAP TO CPU MUST BE LESS THAN 1200MILS MAX NECKDOWN TO & FROM CAPS IS 500MILS



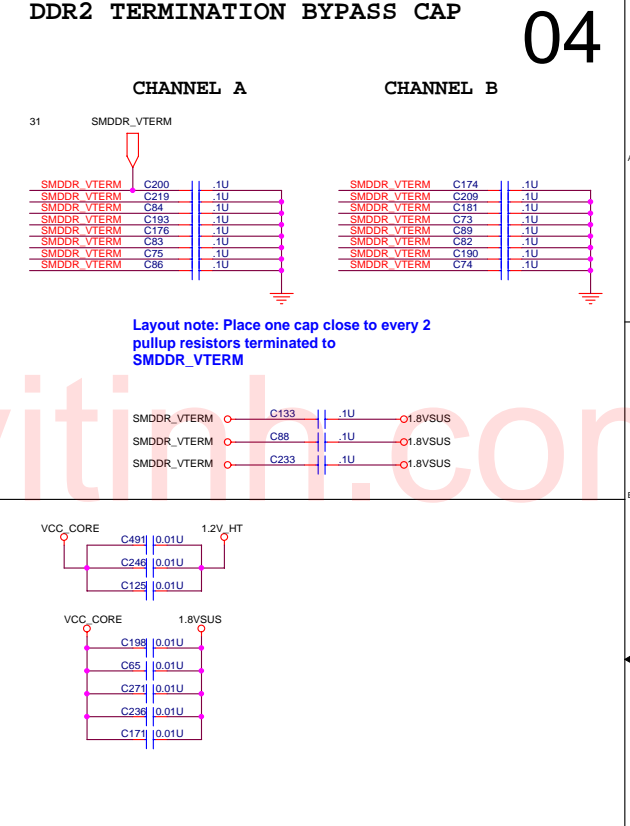
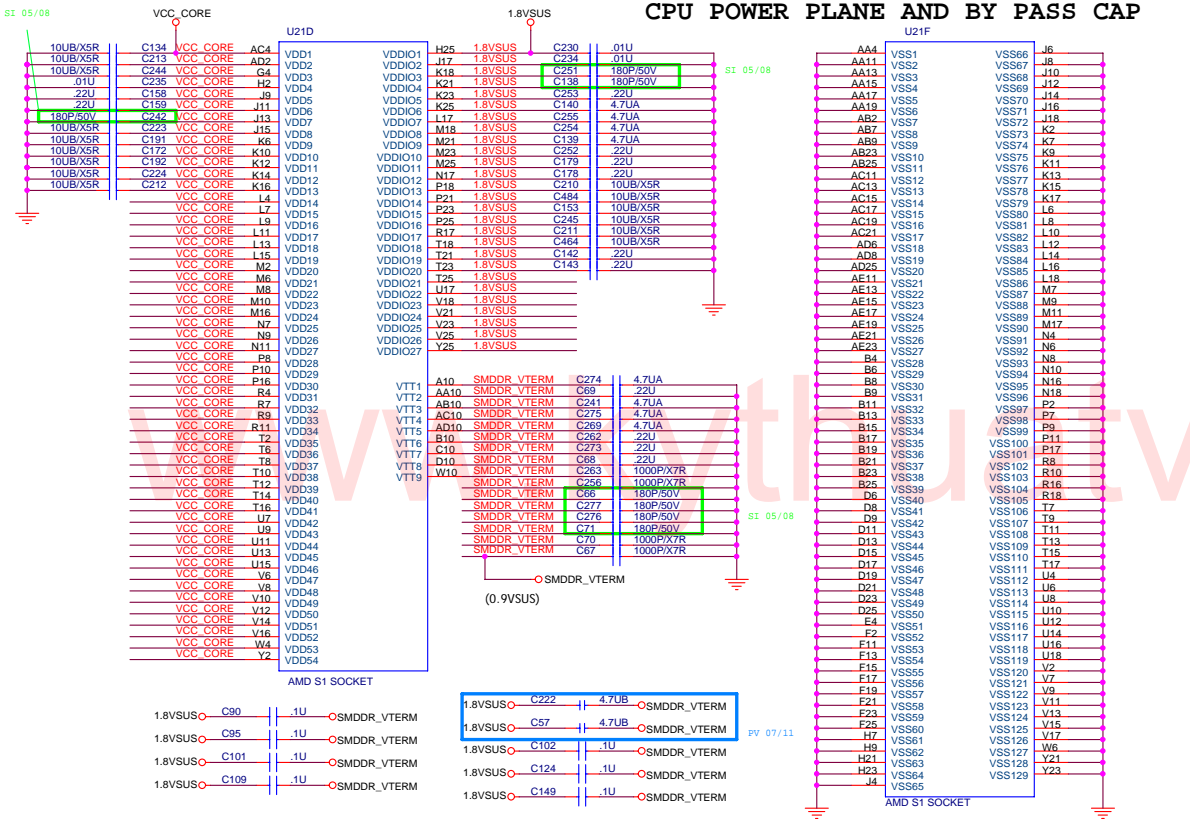
C51MVREF : W = 20MIL AND SPACE = 20MIL



PROJECT : TT8
Quanta Computer Inc.

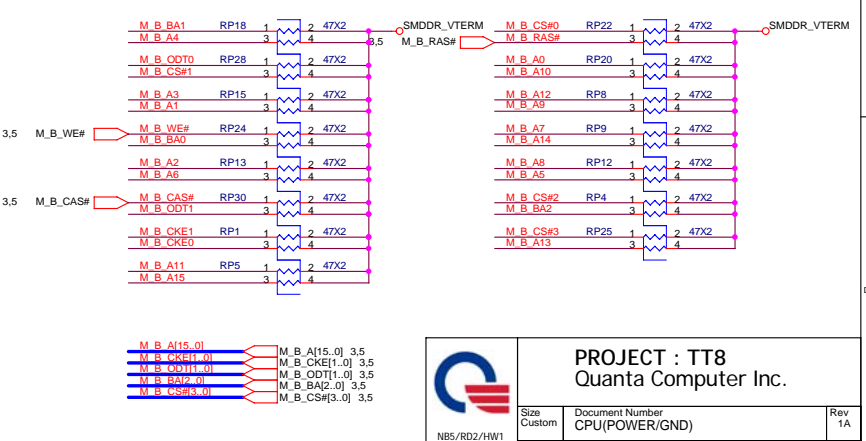
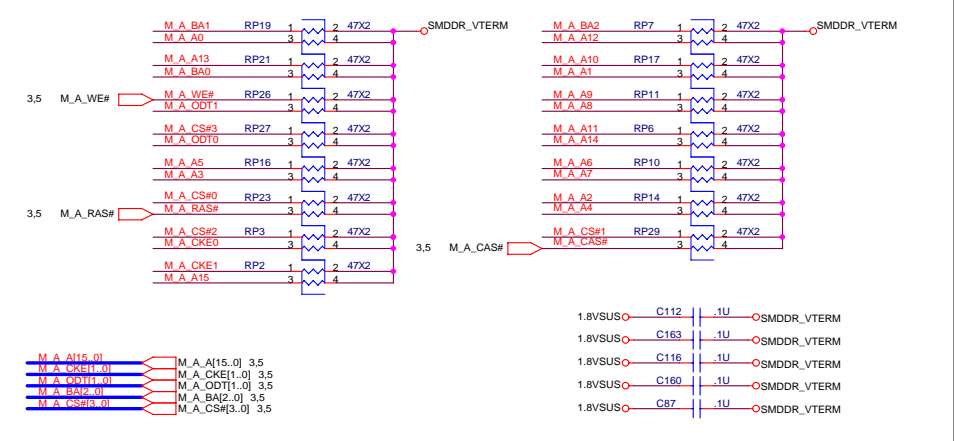
CPU POWER PLANE AND BY PASS CAP

DDR2 TERMINATION BYPASS CAP



DDR1 CHANNEL A TERMINATION

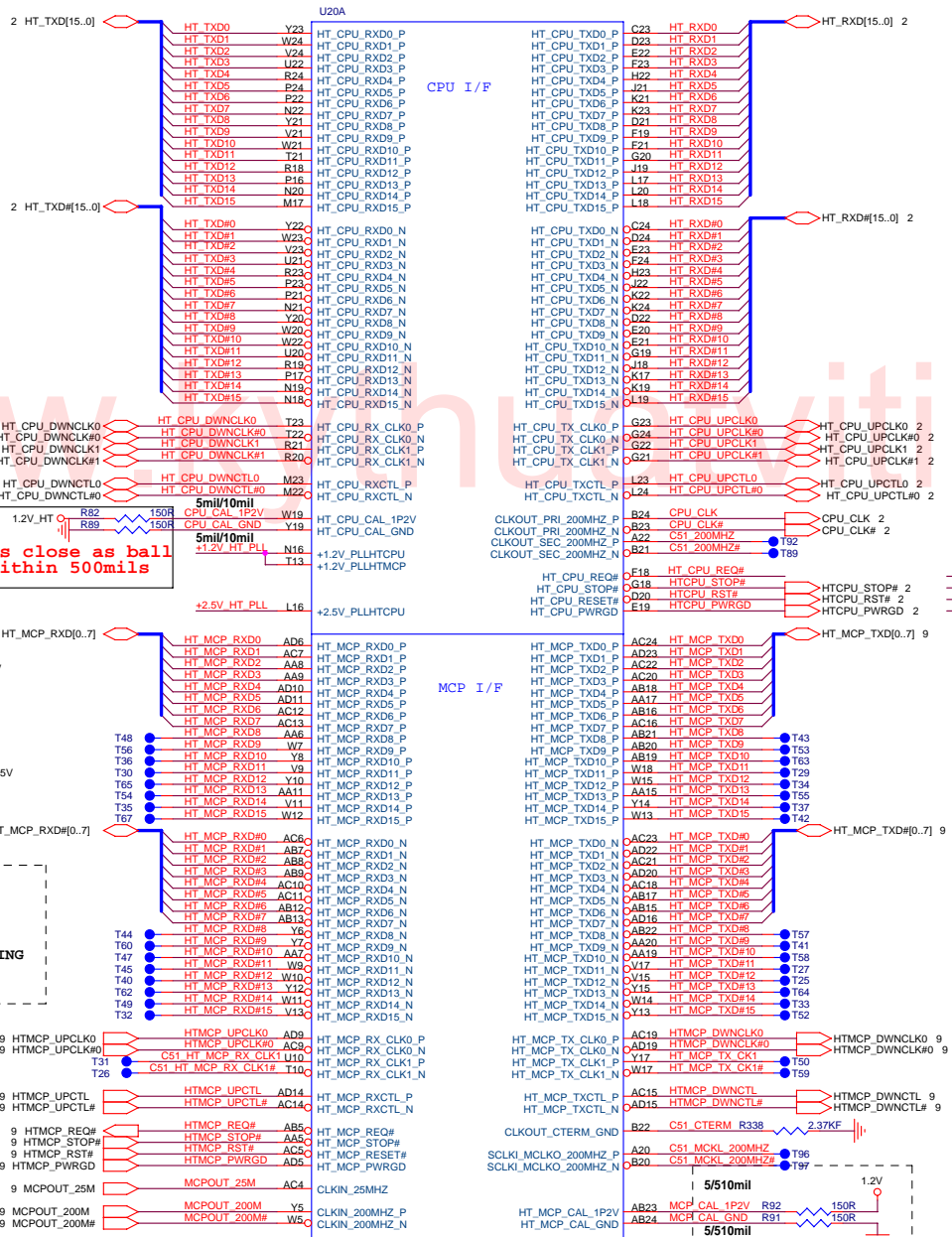
DDR1 CHANNEL B TERMINATION



PROJECT : TT8
Quanta Computer Inc.

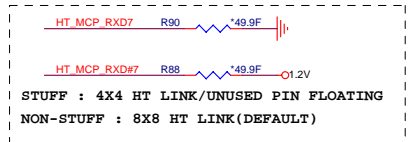
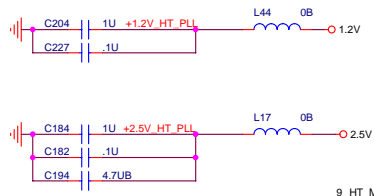
Size Custom Document Number CPU(POWER/GND) Rev 1A

Date: Friday, November 24, 2006 Sheet 4 of 36

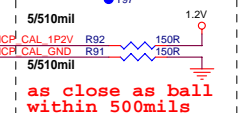


as close as ball within 500mils

#note from nv design guide
Pull-Hi for rise time
0.25V



STUFF : 4X4 HT LINK/UNUSED PIN FLOATING
NON-STUFF : 8X8 HT LINK(DEFAULT)

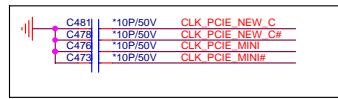
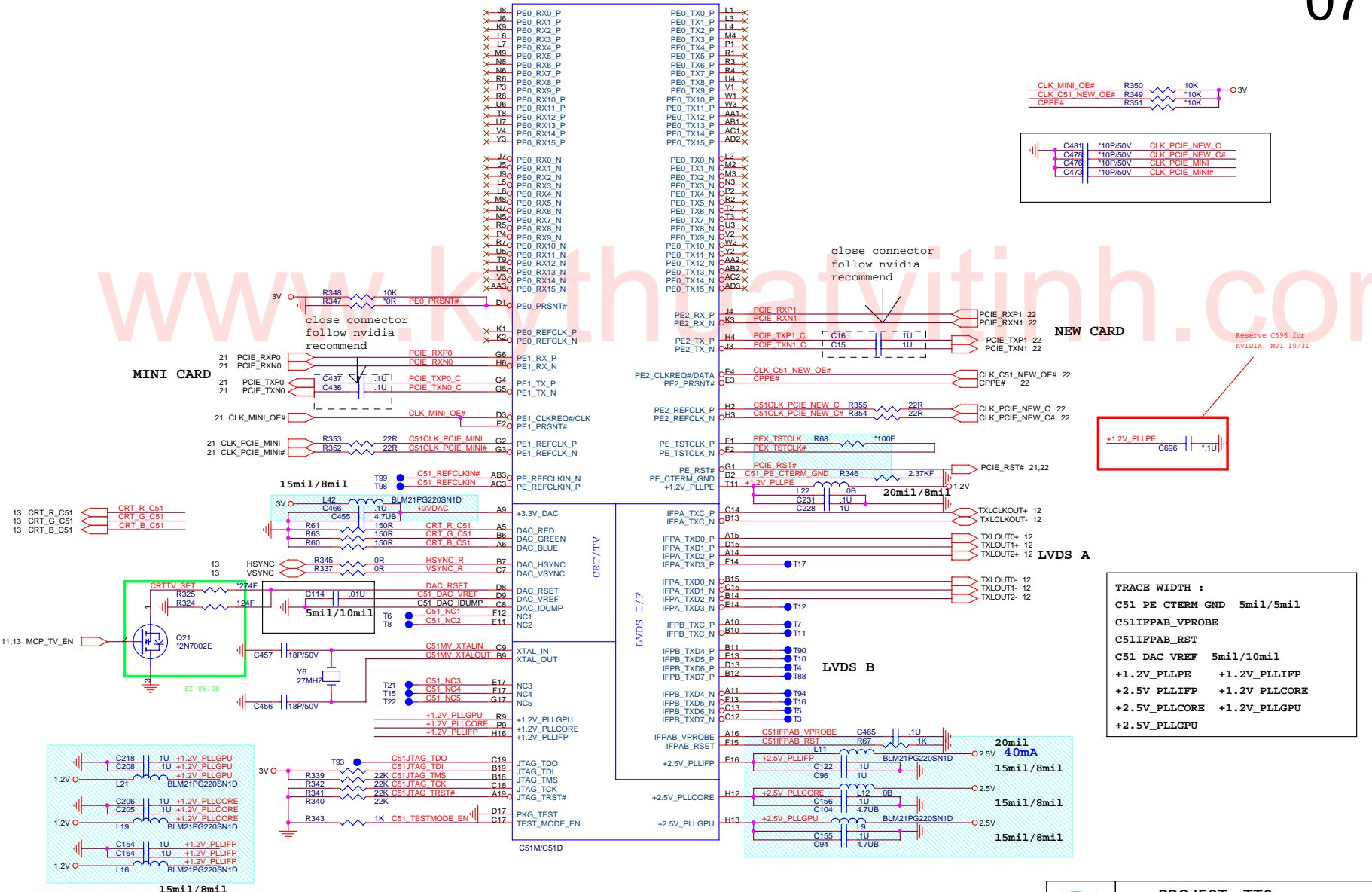


as close as ball within 500mils

PROJECT : TT8
Quanta Computer Inc.

Size Custom	Document Number C51MV (HT LINK)	Rev 1A
Date: Friday, November 24, 2006 Sheet 6 of 36		

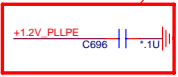
U20B



close connector
follow nvidia
recommend

NEW CARD

Reserve C696 for
nVIDIA NV1 10/31



TRACE WIDTH :

C51_PE_CTERM_GND	5mil/5mil
C51IFPAB_VPROBE	
C51IFPAB_RST	
C51_DAC_VREF	5mil/10mil
+1.2V_PLLPE	+1.2V_PLLIFF
+2.5V_PLLIFF	+1.2V_PLLCORE
+2.5V_PLLCORE	+1.2V_PLFGPU
+2.5V_PLFGPU	



PROJECT : TT8
Quanta Computer Inc.

HT MCP_TXD0[0..7] HT MCP_TXD1[0..7] HT MCP_TXD2[0..7] HT MCP_TXD3[0..7] HT MCP_TXD4[0..7] HT MCP_TXD5[0..7] HT MCP_TXD6[0..7] HT MCP_TXD7[0..7]

HT MCP_RXD0[0..7] HT MCP_RXD1[0..7] HT MCP_RXD2[0..7] HT MCP_RXD3[0..7] HT MCP_RXD4[0..7] HT MCP_RXD5[0..7] HT MCP_RXD6[0..7] HT MCP_RXD7[0..7]

HT MCP_TX_CLK# HT MCP_RX_CLK# HT MCP_TX_CTL# HT MCP_RX_CTL# HT MCP_REQ# HT MCP_STOP# HT MCP_COMP_GND1 HT MCP_COMP_GND2

HT MCP_RXD0_N HT MCP_RXD1_N HT MCP_RXD2_N HT MCP_RXD3_N HT MCP_RXD4_N HT MCP_RXD5_N HT MCP_RXD6_N HT MCP_RXD7_N

PCI_A00 PCI_A01 PCI_A02 PCI_A03 PCI_A04 PCI_A05 PCI_A06 PCI_A07 PCI_A08 PCI_A09 PCI_A10 PCI_A11 PCI_A12 PCI_A13 PCI_A14 PCI_A15 PCI_A16 PCI_A17 PCI_A18 PCI_A19 PCI_A20 PCI_A21 PCI_A22 PCI_A23 PCI_A24 PCI_A25 PCI_A26 PCI_A27 PCI_A28 PCI_A29 PCI_A30 PCI_A31

HT MCP_RXD0_P HT MCP_RXD1_P HT MCP_RXD2_P HT MCP_RXD3_P HT MCP_RXD4_P HT MCP_RXD5_P HT MCP_RXD6_P HT MCP_RXD7_P

HT MCP_TXD0_P HT MCP_TXD1_P HT MCP_TXD2_P HT MCP_TXD3_P HT MCP_TXD4_P HT MCP_TXD5_P HT MCP_TXD6_P HT MCP_TXD7_P

HT MCP_RXD0_N HT MCP_RXD1_N HT MCP_RXD2_N HT MCP_RXD3_N HT MCP_RXD4_N HT MCP_RXD5_N HT MCP_RXD6_N HT MCP_RXD7_N

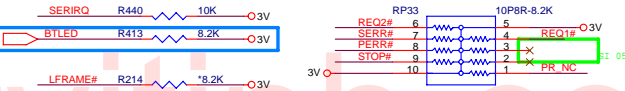
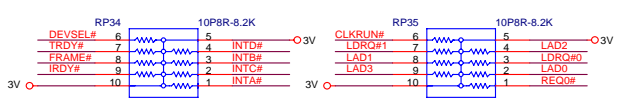
HT MCP_TXD0_N HT MCP_TXD1_N HT MCP_TXD2_N HT MCP_TXD3_N HT MCP_TXD4_N HT MCP_TXD5_N HT MCP_TXD6_N HT MCP_TXD7_N

5 MIL (75mA) C585 .1U 1.5V_PLL_CPU HT R436 0A 1.5V

1.5V_PLL_CPU_HT

5 MIL (20mA) C587 .1U 3V_PLL_CPU HT L30 BLM21PG220SNTD 0.3V

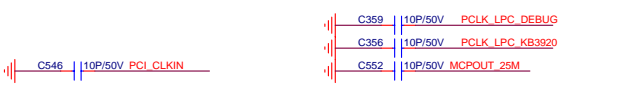
3V_PLL_CPU_HT



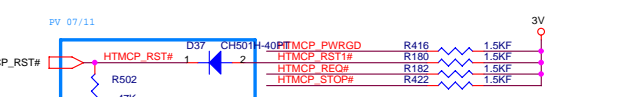
PCI/LPC PULL-UP

HT MCP_TXD7 R195 .49.9F 1.2V HT MCP_TXD7 R192 .49.9F

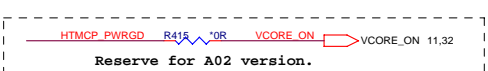
STUFF : 4X4 HT LINK/UNUSED PIN FLOATING (DEFAULT) NON-STUFF : 8X8 HT LINK



CLOCK BYPASS



HTMCP_RST# R502 47K



HTMCP_PWRGD R415 0R VCORE_ON 11.32 Reserve for A02 version.

HT LINK

PCI

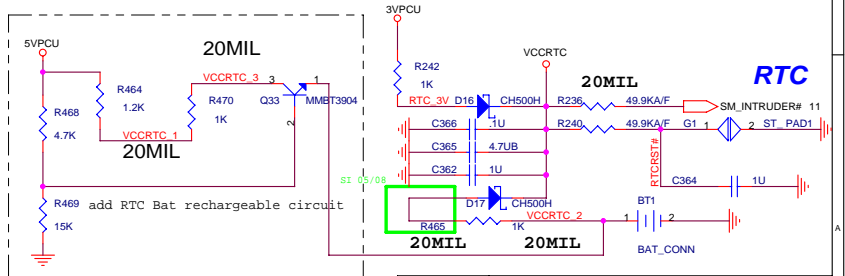
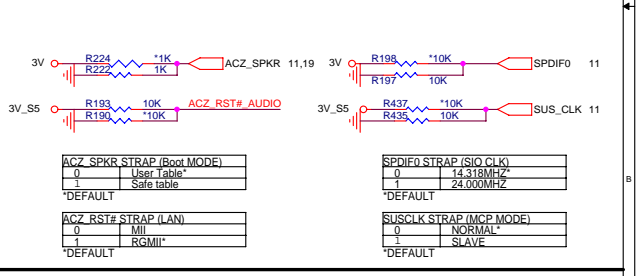
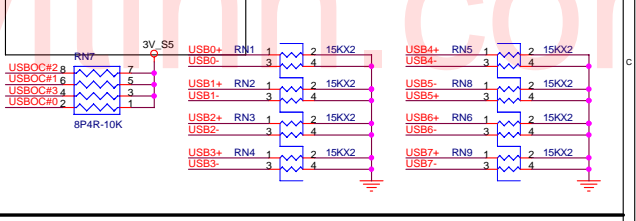
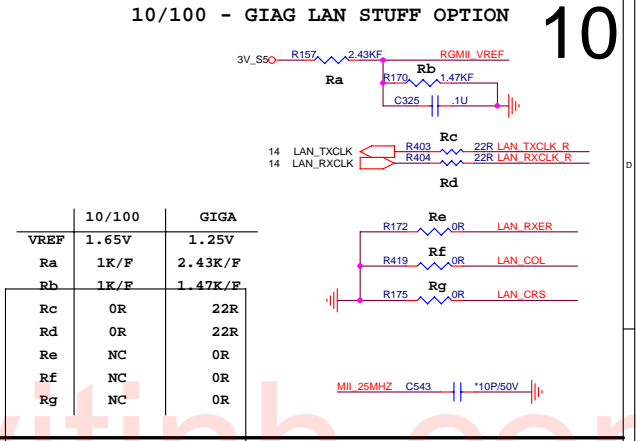
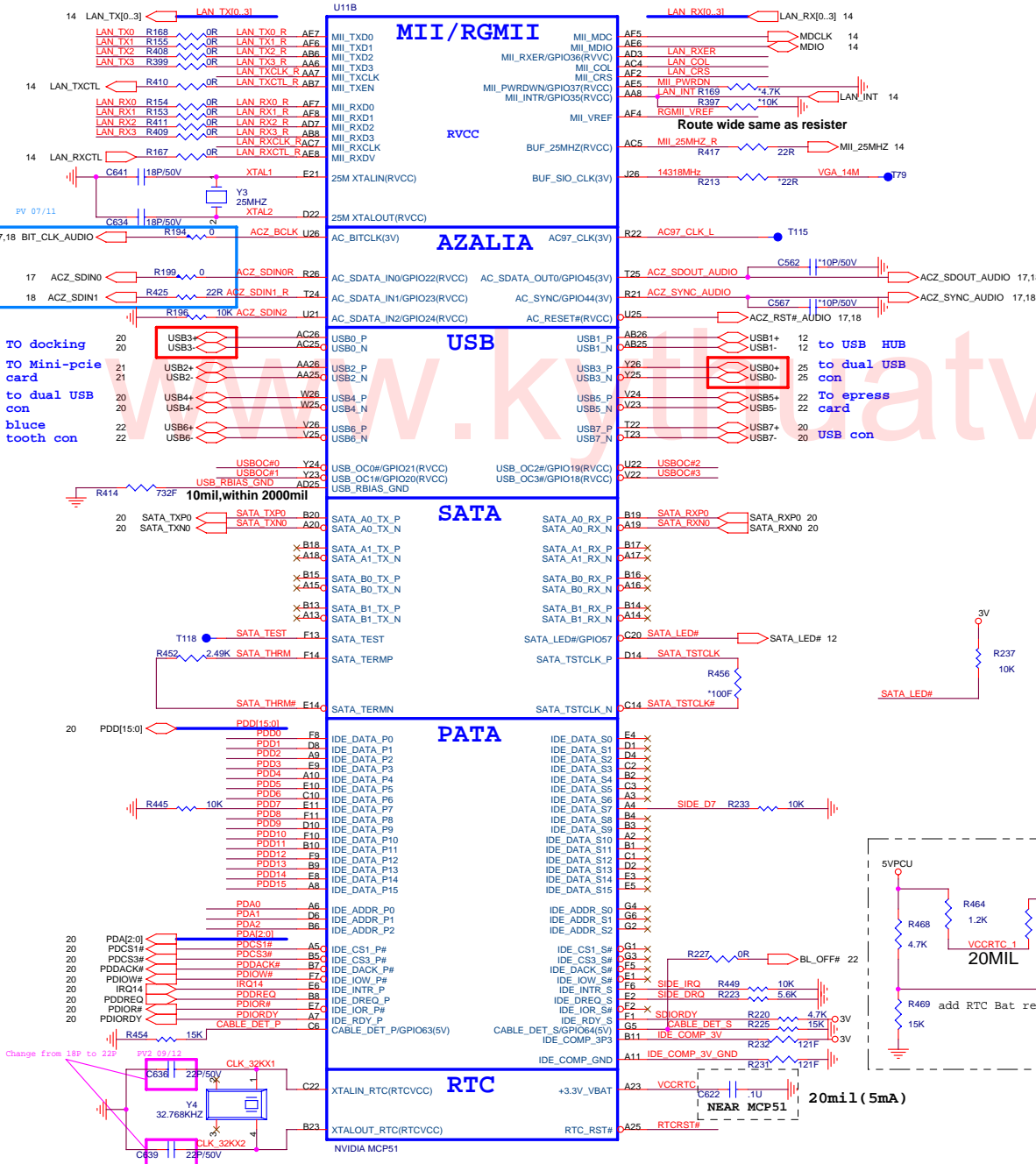
LPC

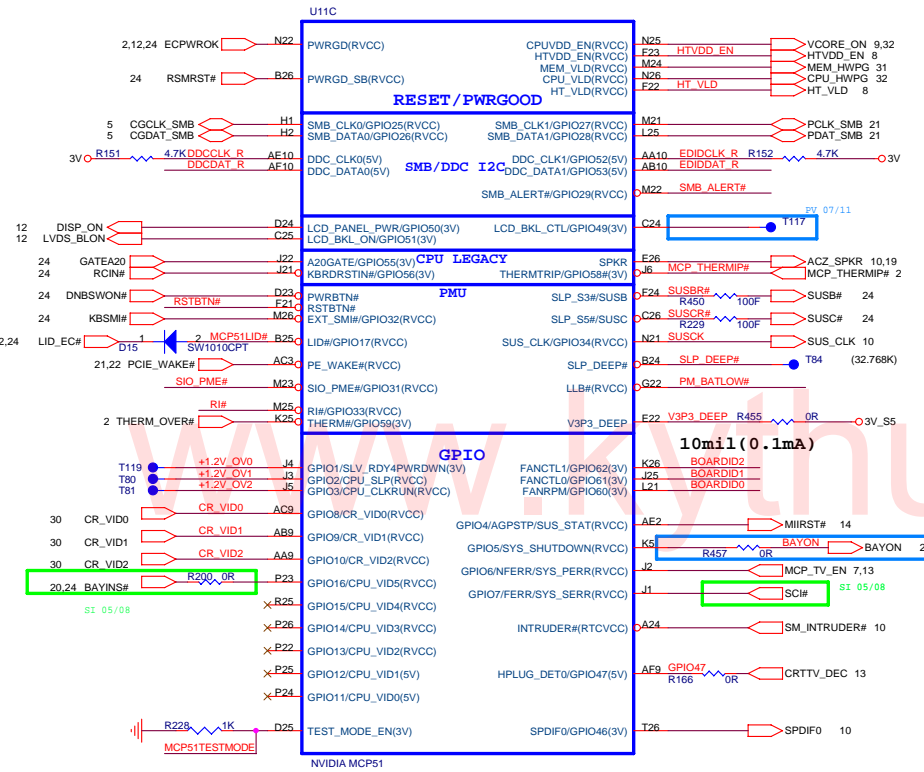
JTAG



PROJECT : TT8 Quanta Computer Inc.

Table with project details: Size Custom, Document Number MCP51 (1 of 3), Date: Friday, November 24, 2006, Sheet 9 of 36, Rev 1A.



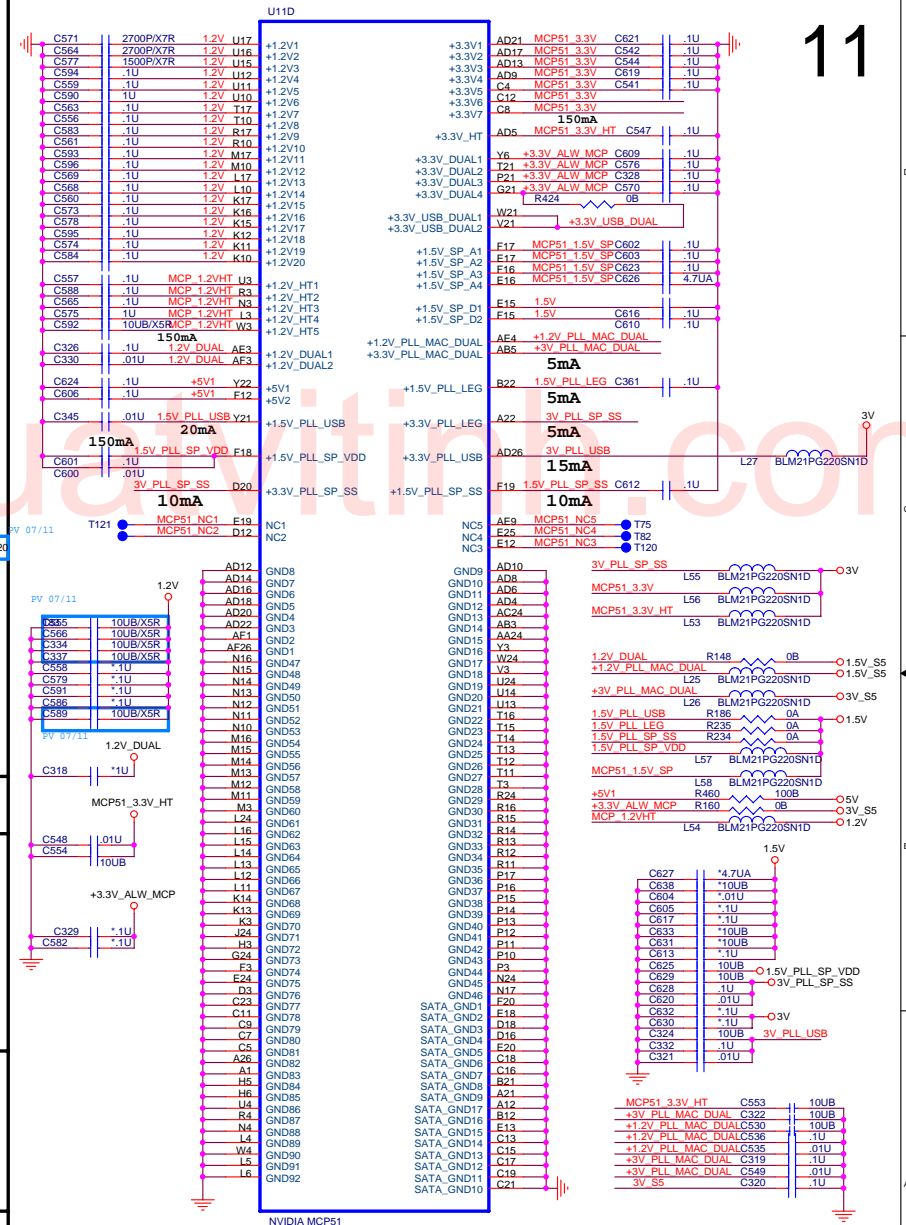


SYS BOARD ID

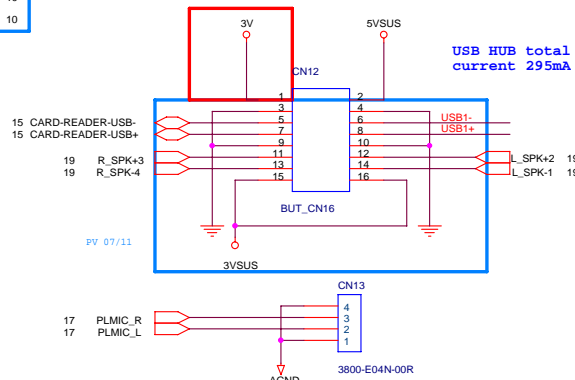
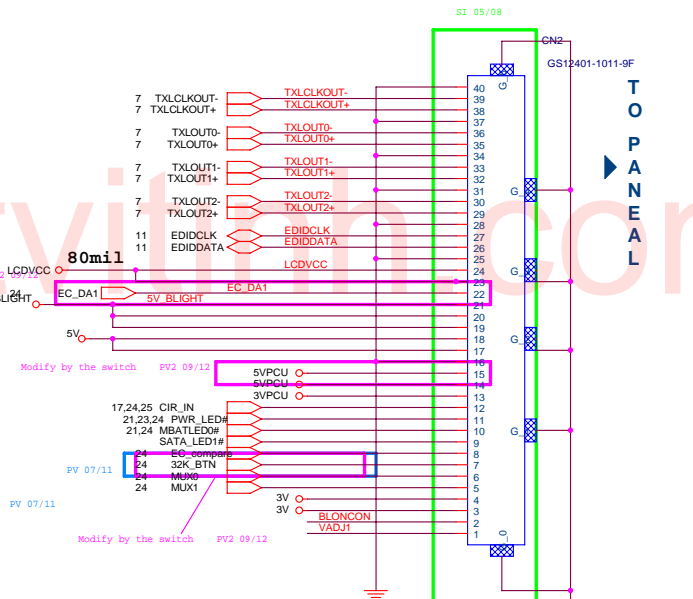
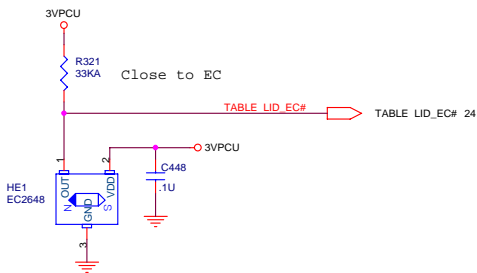
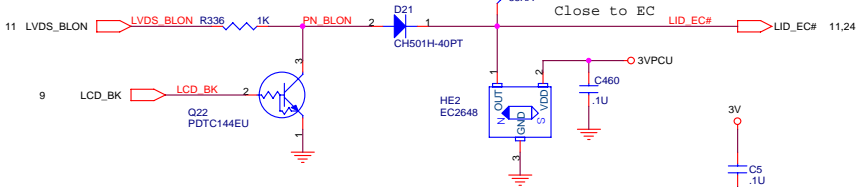
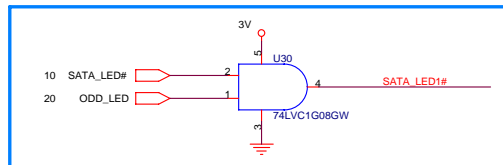
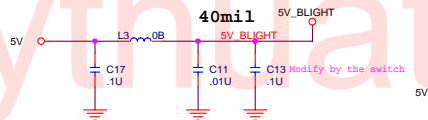
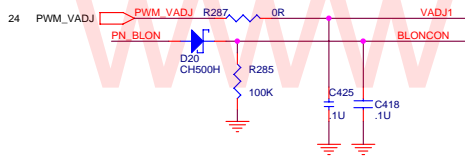
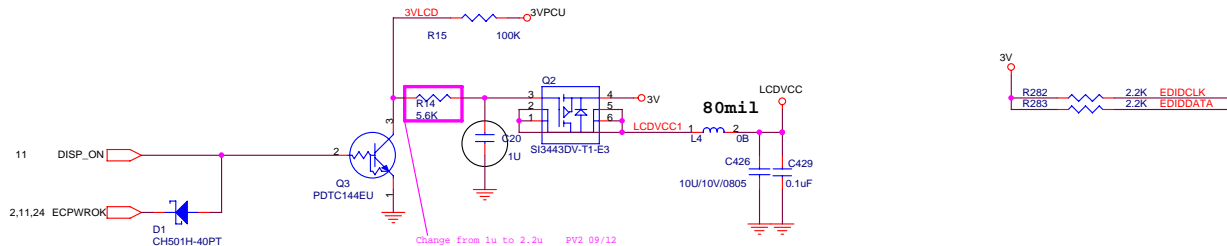
Board ID0	Board ID1	Board ID2	Board ID3
WWAN/SIM	Low	High	High
W/O WWAN	High	High	High

SMB/I2C PULL-UP

PCLK_SMB	R434	2.7K	
PDAT_SMB	R204	2.7K	
SMB_ALERT#	R431	2.7K	
CGCLK_SMB	R215	2.7K	
CGDAT_SMB	R217	2.7K	



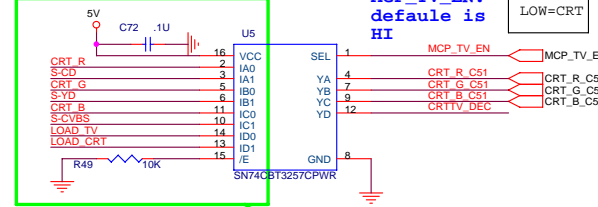
PROJECT : TT8
Quanta Computer Inc.



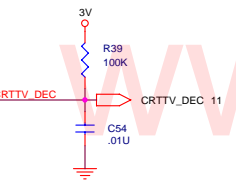
PROJECT : TT8
Quanta Computer Inc.

Size: Custom
Date: Friday, November 24, 2006
Sheet: 12 of 36
Rev: 1A

CRT/TV SWITCH



LOAD_CRT -- TV WORK
 LOAD_TV -- CRT WORK



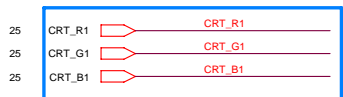
close within 600mils (close data switch)



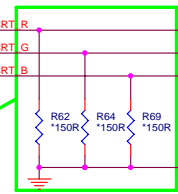
S-CVBS	R47	10K	LOAD_TV
S-YD	R45	10K	LOAD_TV
CRT_B	R46	10K	LOAD_CRT

That is for CRT and TV choose.. used impedance and driver to choose

PV 07/11

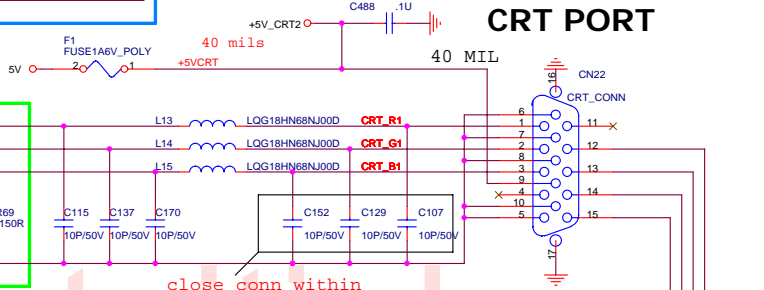


150-R as possible as closed to CRT connector (close with in 600 mil)



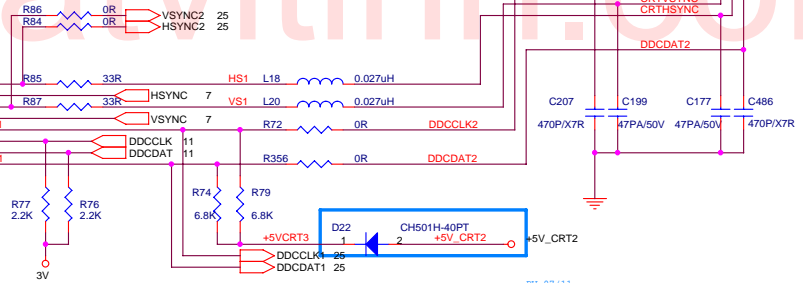
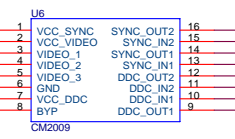
Change from nVIDIA for B-test

CRT PORT

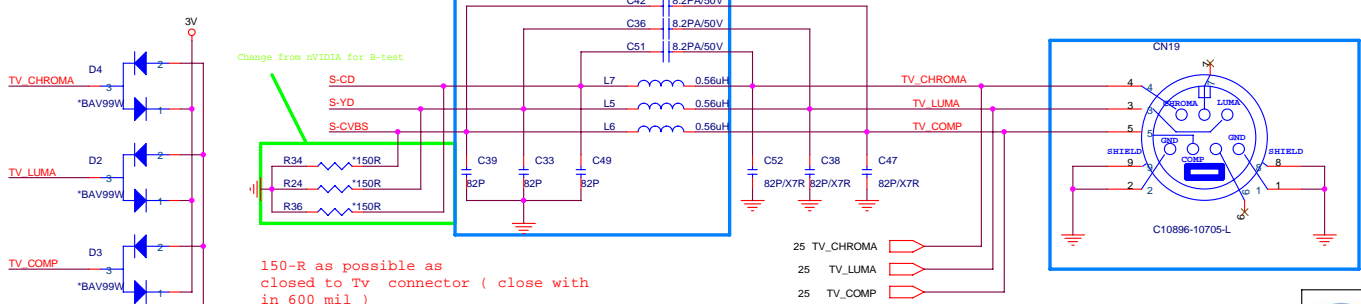


close conn within 600mils

ESD PROTECTION

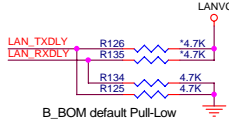


TV_OUT

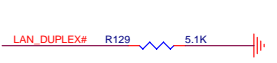
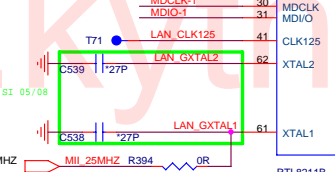
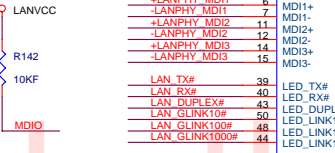
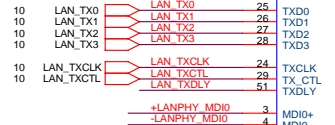
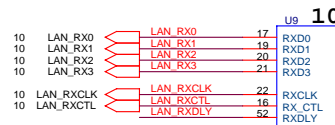
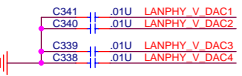
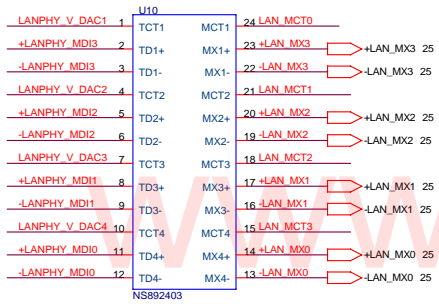


Change from nVIDIA for B-test

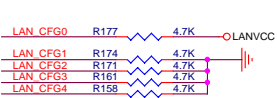
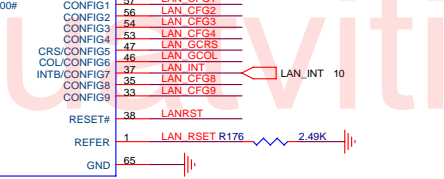
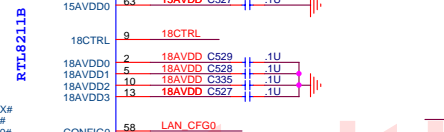
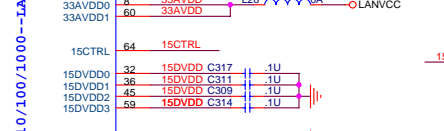
150-R as possible as closed to Tv connector (close with in 600 mil)



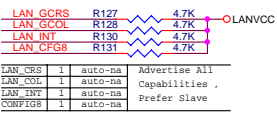
NS892403 : GIGABIT



10/100/1G

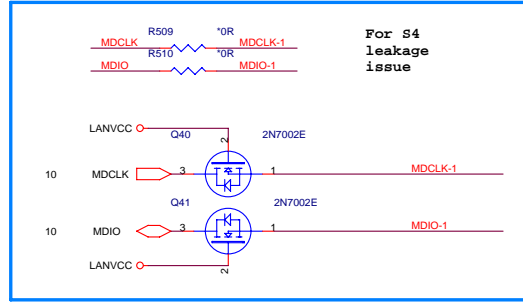
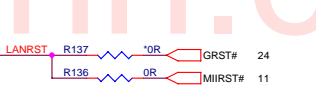
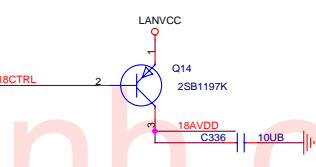
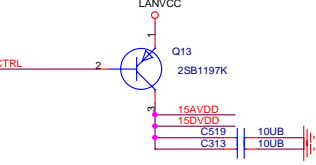


PHY Address: 00001

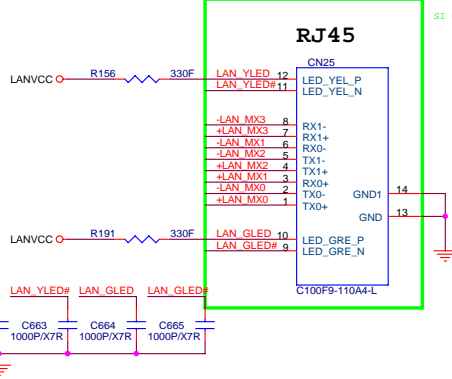
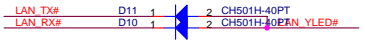
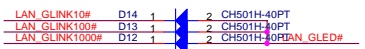


LAN_CRS 1 auto-na Advertise All
 LAN_COL 1 auto-na Capabilities
 LAN_INT auto-na Prefer Slave
 CONF18 1 auto-na

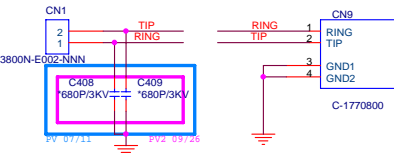
1:RGMII/MII TO COPPER



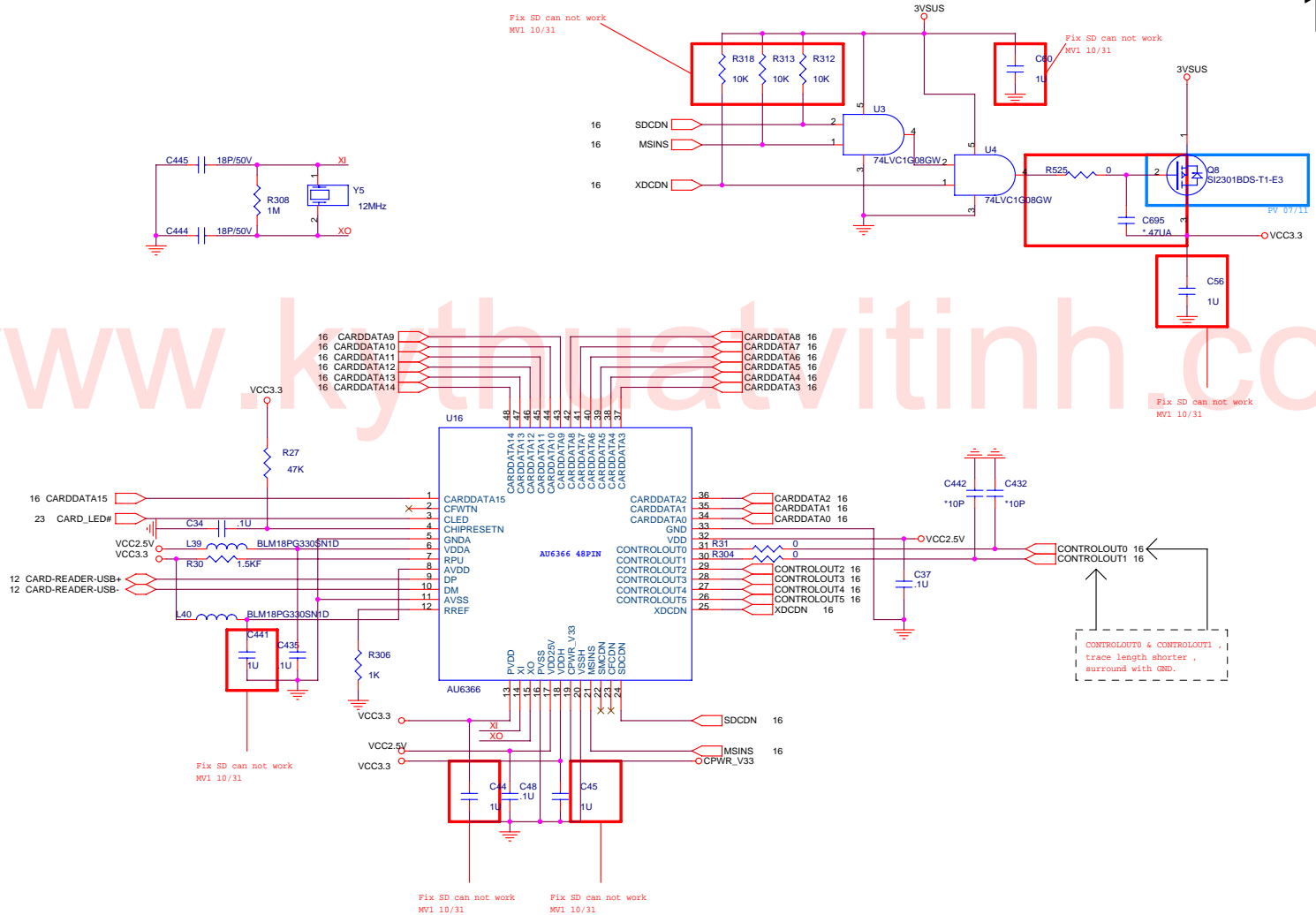
RJ45



RJ11

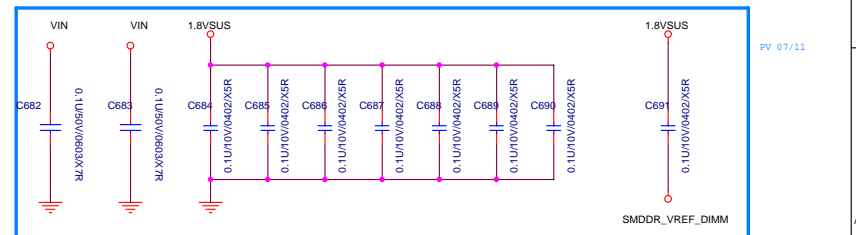
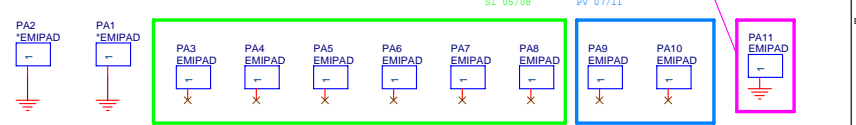
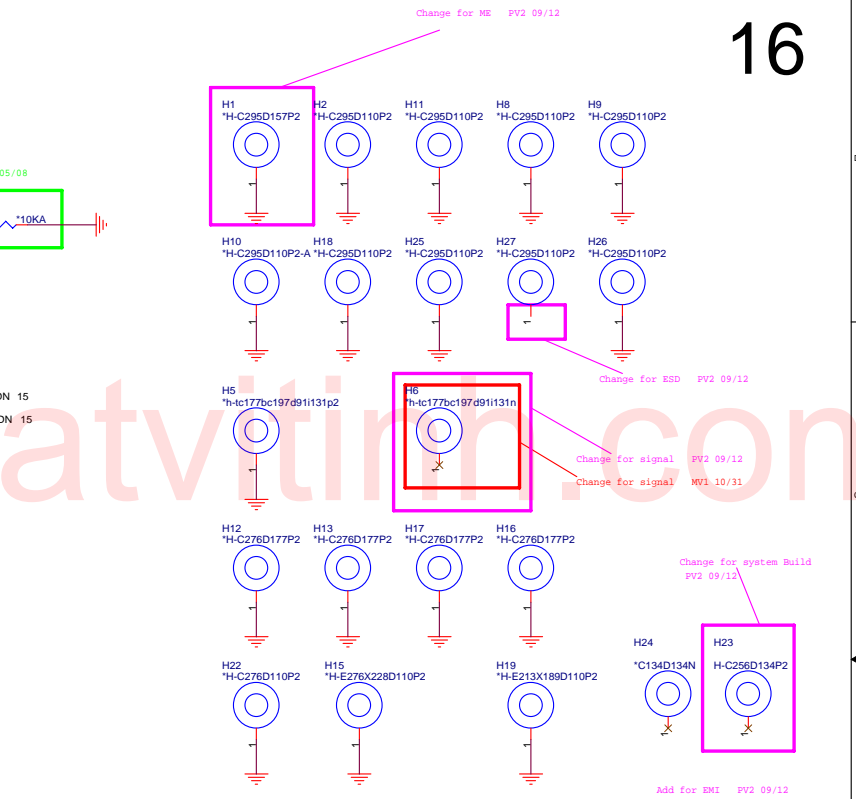
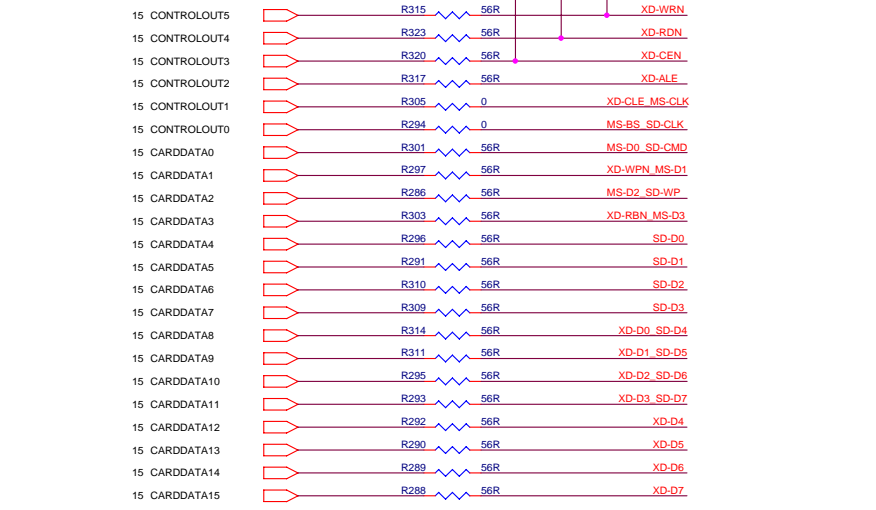
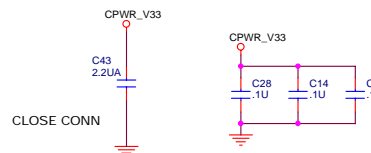
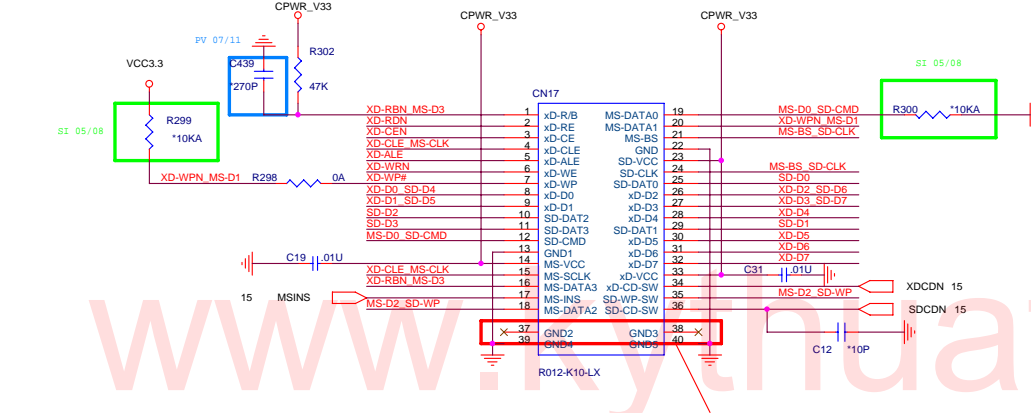


PROJECT : TT8
 Quanta Computer Inc.

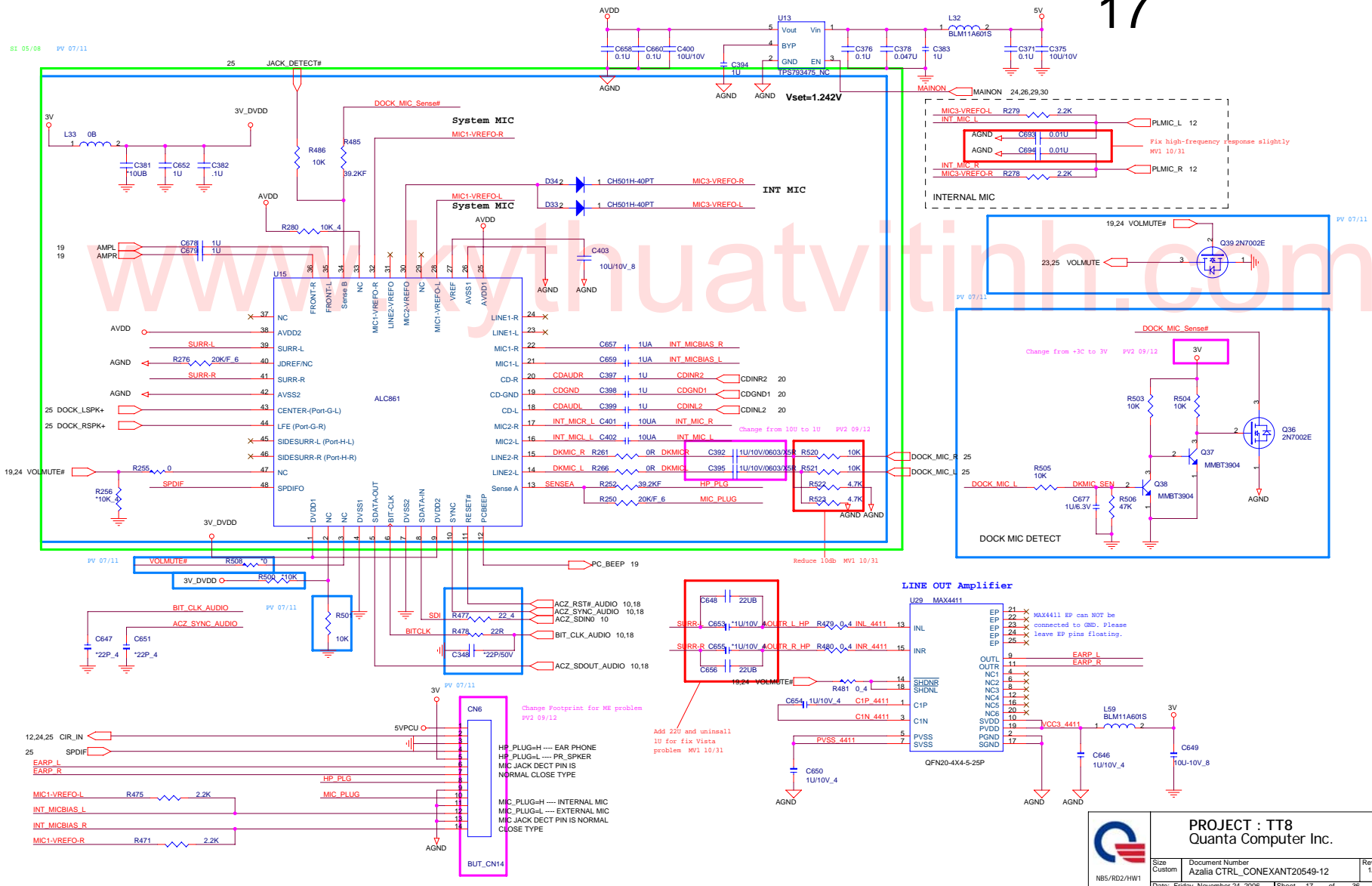


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4 IN1 CARD READER
XD, MMC/SD, MS/MS-P



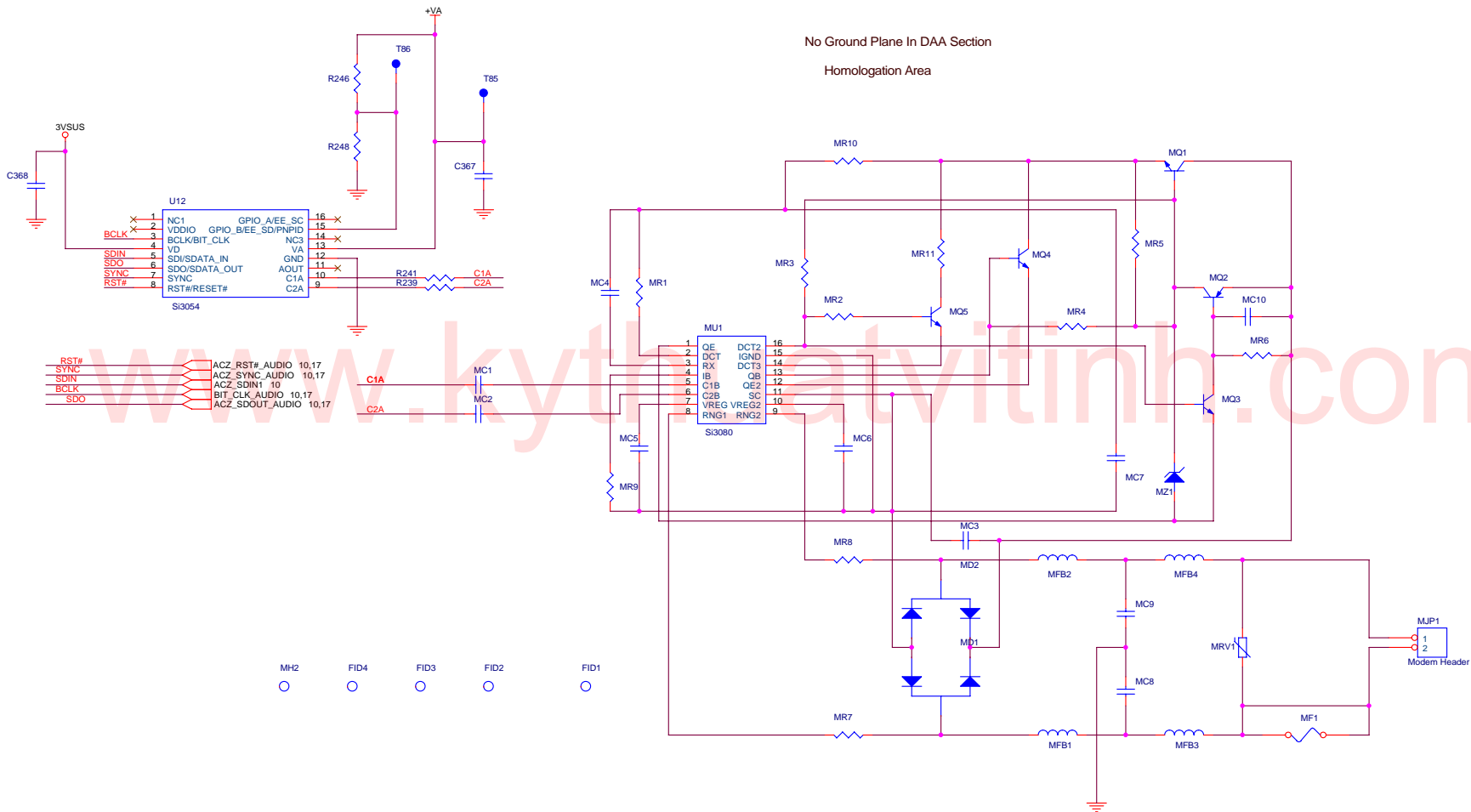
SI 05/08 PV 07/11



PROJECT : TT8
Quanta Computer Inc.

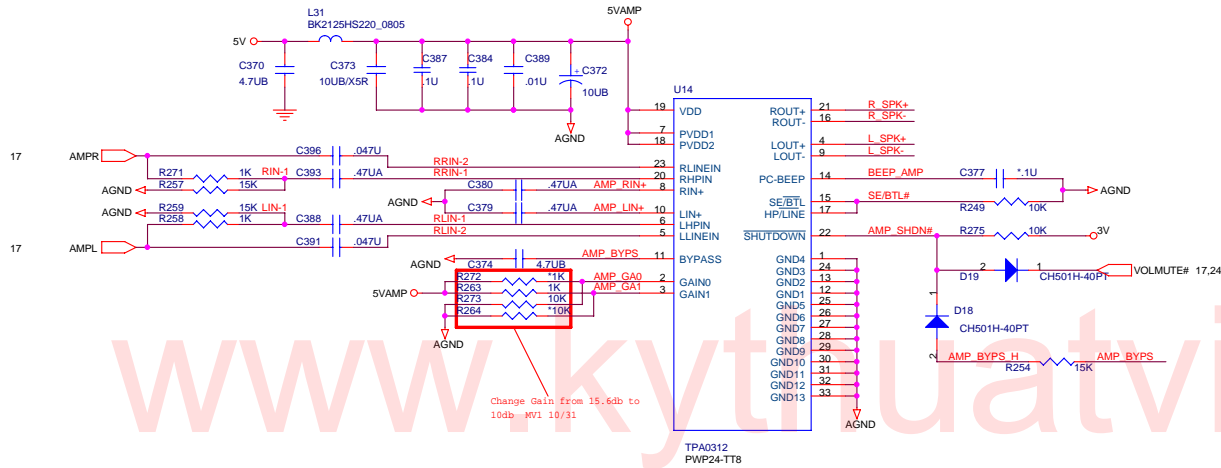
NBS/RD01/HW1

Size Custom	Document Number Azalia CTRL_CONEXANT20549-12	Rev 1A
Date: Friday, November 24, 2006		Sheet 17 of 36



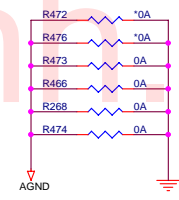
DESIGN SUBJECT TO CHANGE

SILICON LABORATORIES CONFIDENTIAL



0312 Gain Table

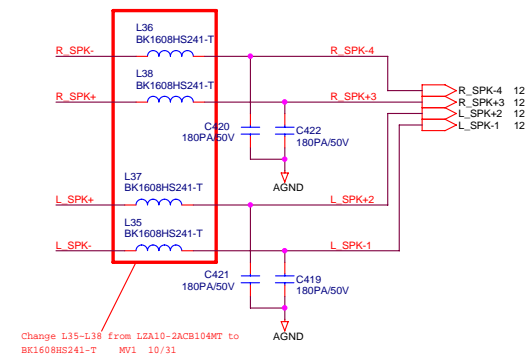
GAIN0	GAIN1	SE/BTL	AV(INV)
0	0	0	6dB
0	1	0	10dB
1	0	0	15.6dB
1	1	0	21.6dB
x	x	1	4.1dB



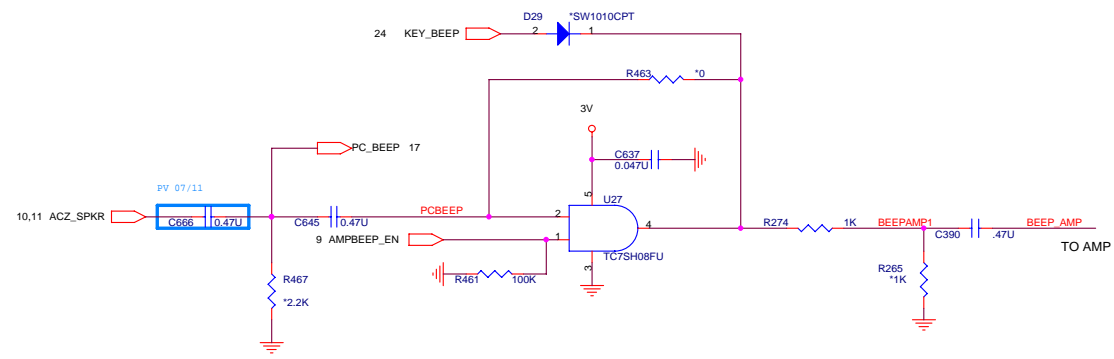
Change Gain from 15.6db to 10db - MV1 10/31

INT. SPEAKER

PCSPK BEEP

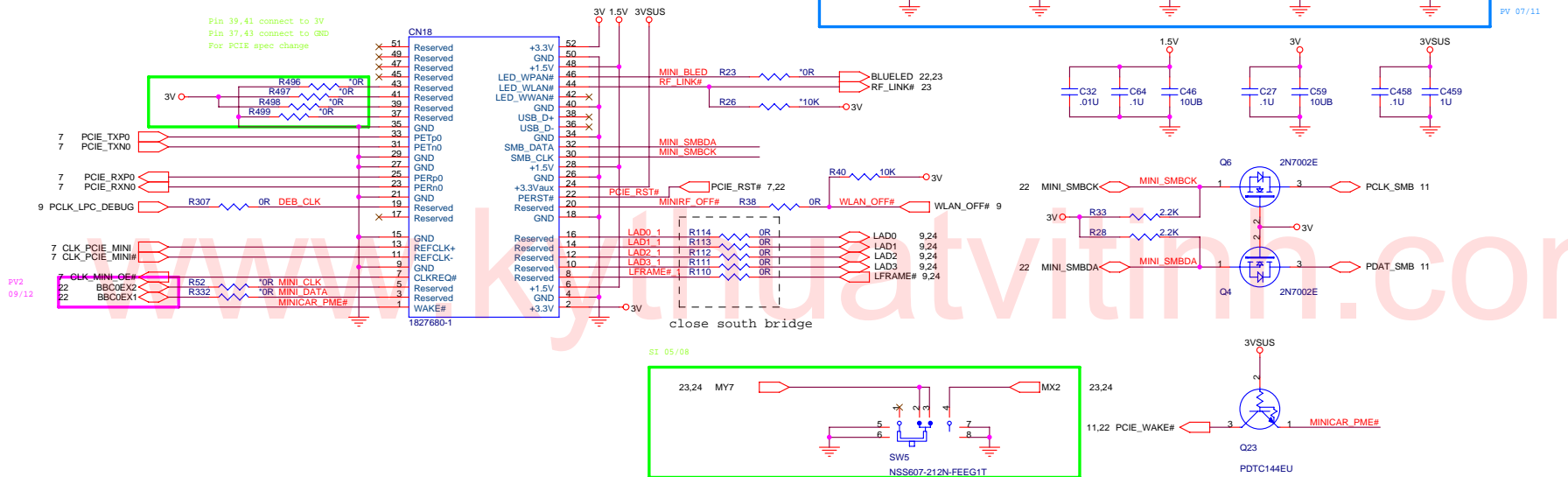


Change L35-L38 from LZA10-2ACB104MT to BK1608HS241-T MV1 10/31



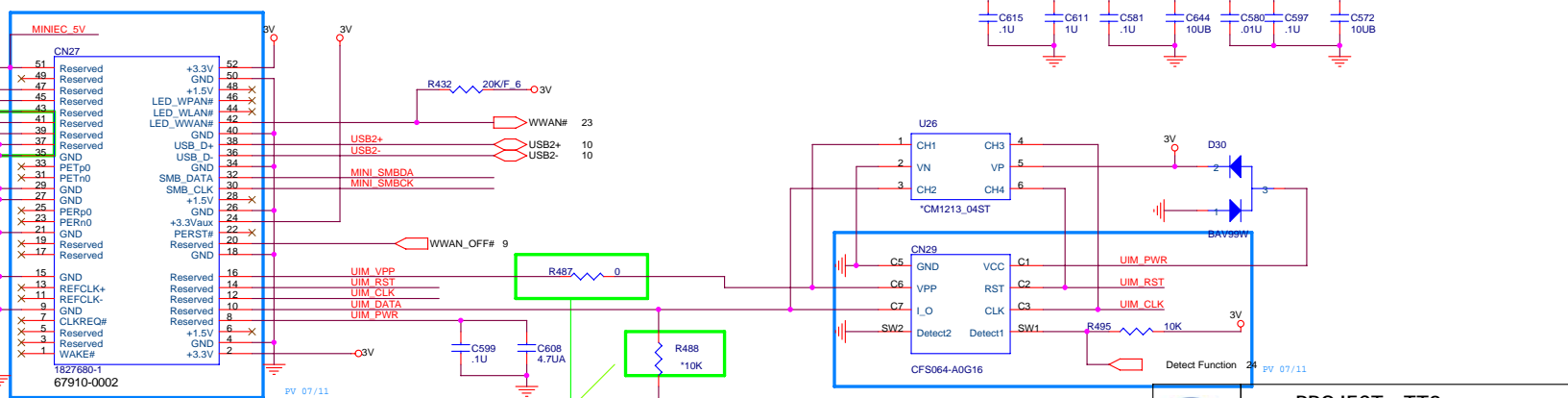
Mini PCI-E Card 1 WLAN

Pin 39,41 connect to 3V
Pin 37,43 connect to GND
For PCIe spec change



Mini PCI-E Card 2 WWAN(W/SIM)

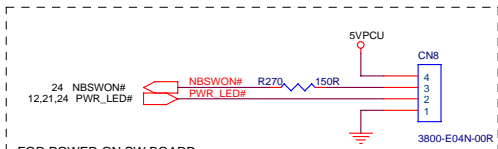
FOR KBC DEBUG
5V R459 0A
13,23,24 PWR_LED#
12,24 MBATLED0#
3V
Pin 39,41 connect to 3V
Pin 37,43 connect to GND
For PCIe spec change



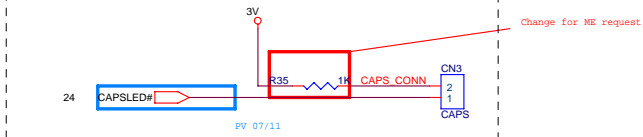
PROJECT : TT8
Quanta Computer Inc.

Size: Custom
Document Number: MINI CARD
Rev: 1A

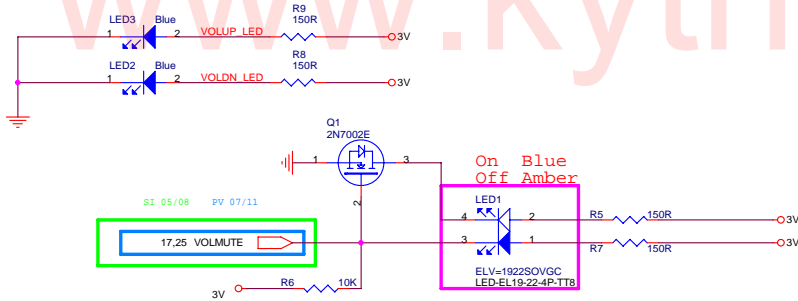
NBS/RD2/HW1
Date: Friday, November 24, 2006 | Sheet 21 of 36



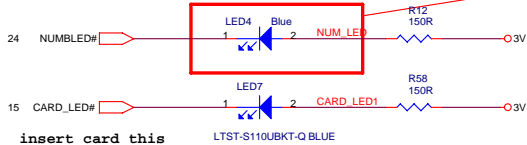
FOR POWER ON SW BOARD



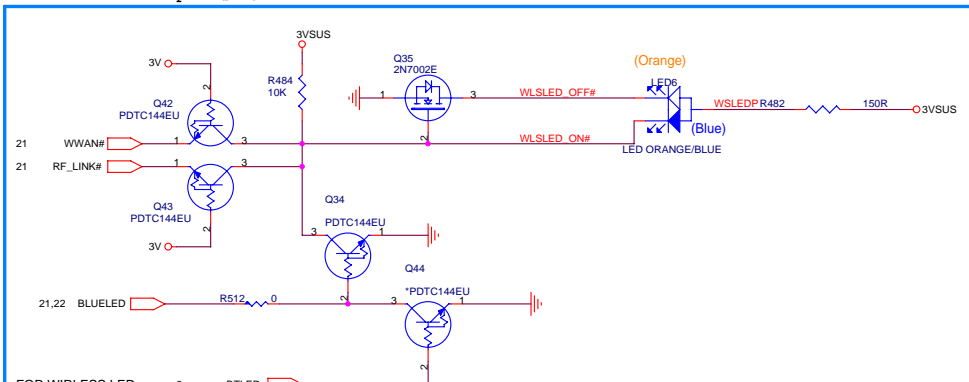
for caps lock LED board



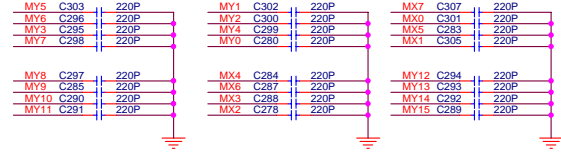
Change the LED for MB requests MW1 10/31



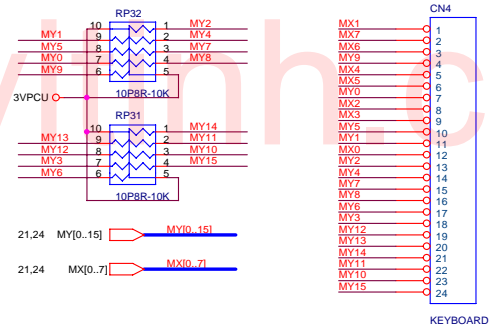
insert card this pin is low



FOR WIRELESS LED

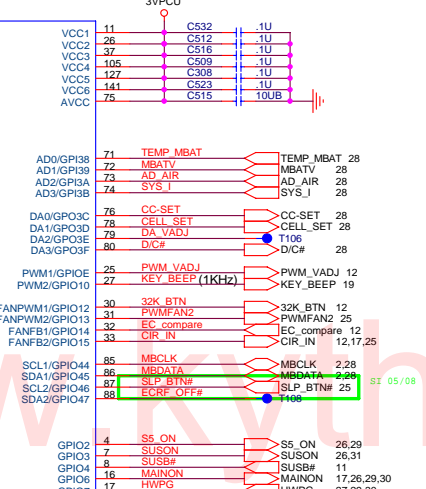
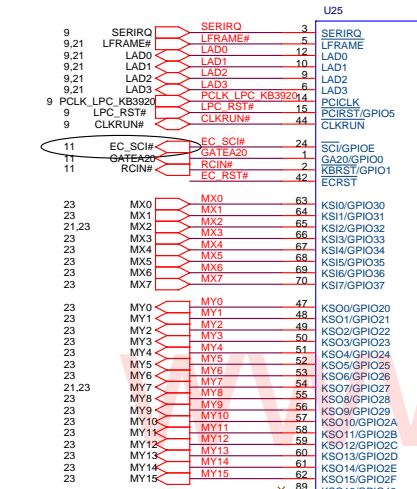
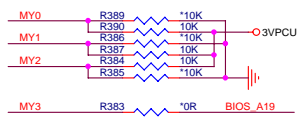


KEYBOARD PULL-UP

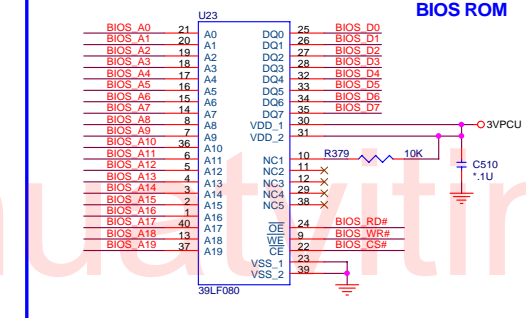


STRAP PIN

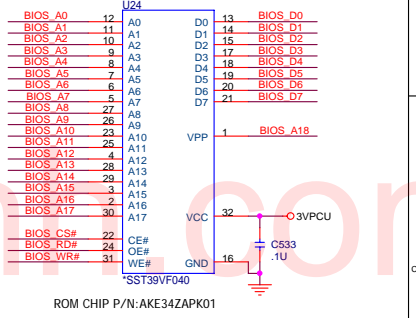
MY0	47	TP_TEST: Clock Test Mode Low: Test Mode HIGH: 32KHz clock in normal running
MY1	48	TP_PLL: DPPLL Test Mode Low: Test Mode HIGH: Normal operation
MY2	49	TP_SPI: Default flash access Low: Boot from SPI flash part HIGH: Boot from ISA flash part
MY3	50	TP_ISP: In System Programming Mode Low: ISP mode HIGH: Normal Mode



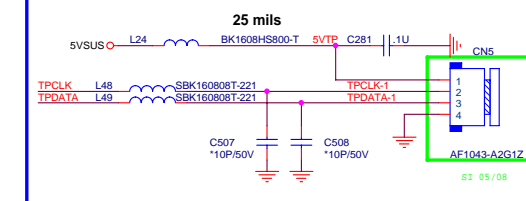
BIOS ROM



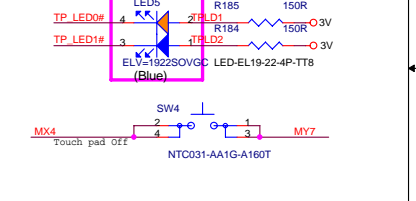
4Mbit (512k Byte), PLCC



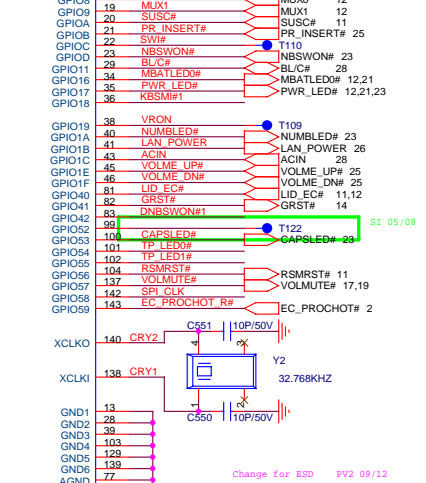
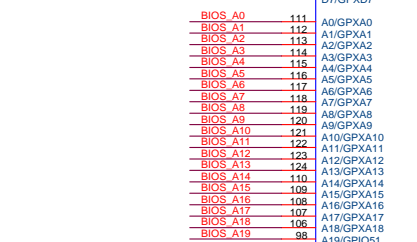
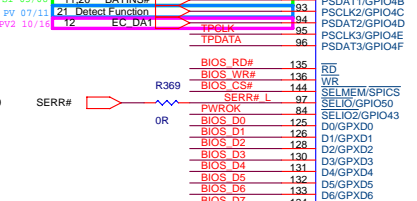
TOUCH PAD CONNECTOR



ROM CHIP P/N: AKE34ZAPK01



BIOS ROM



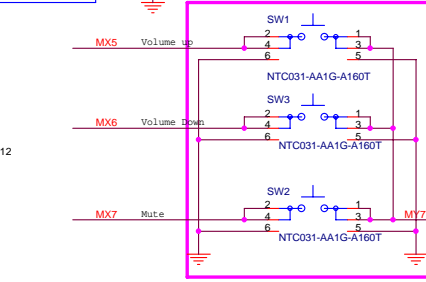
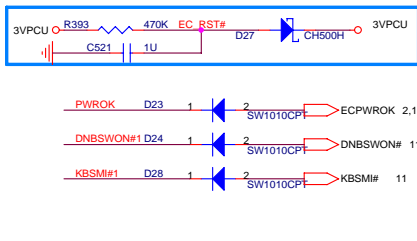
TOUCH PAD CONNECTOR



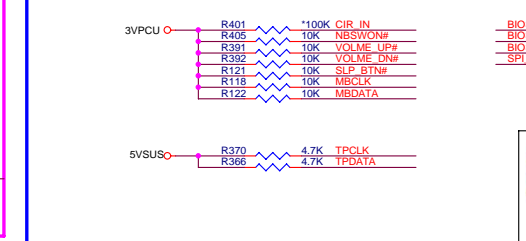
ROM CHIP P/N: AKE34ZAPK01



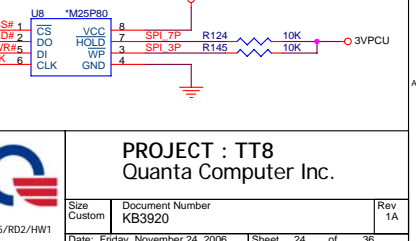
BIOS ROM



TOUCH PAD CONNECTOR

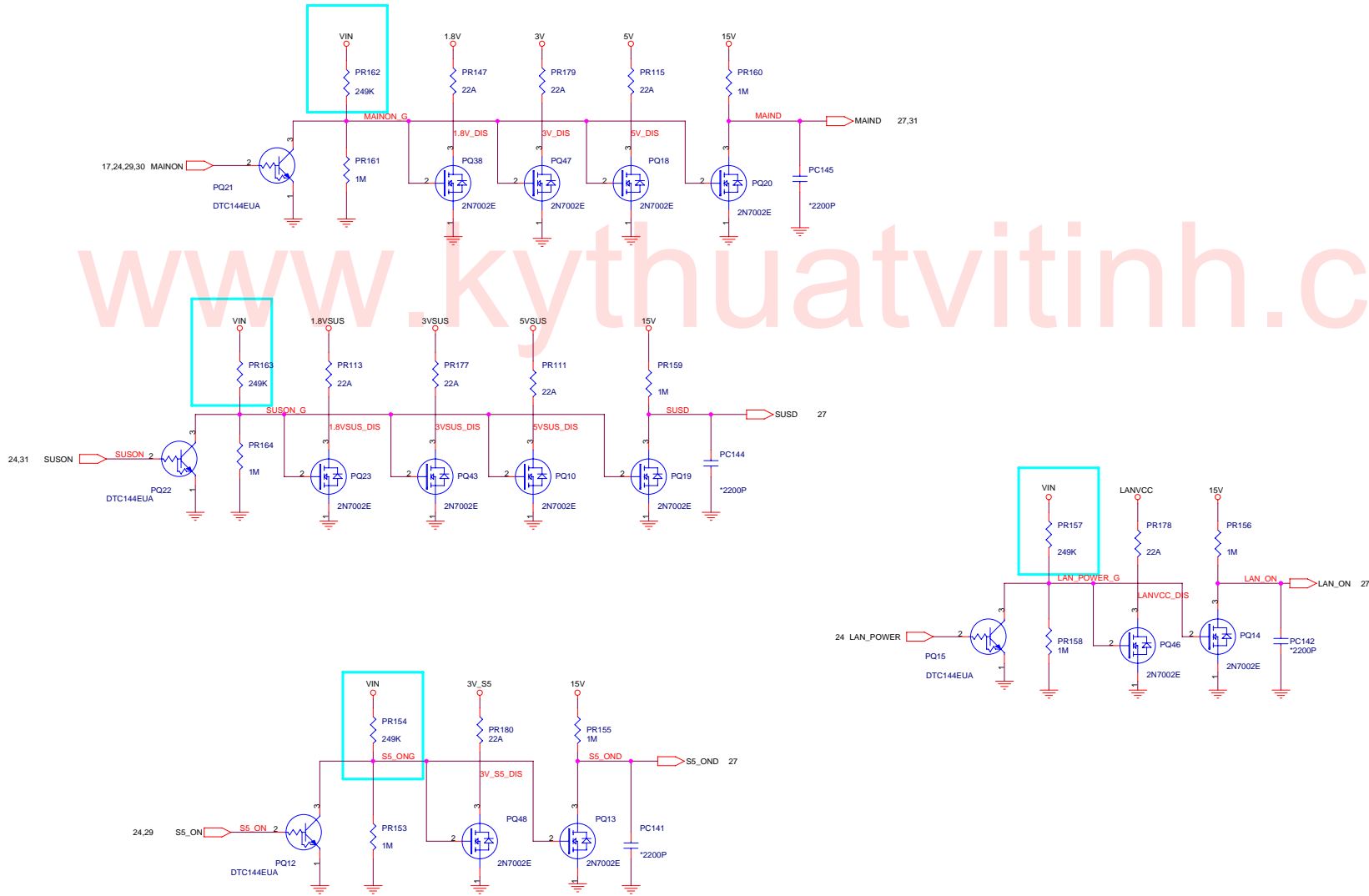


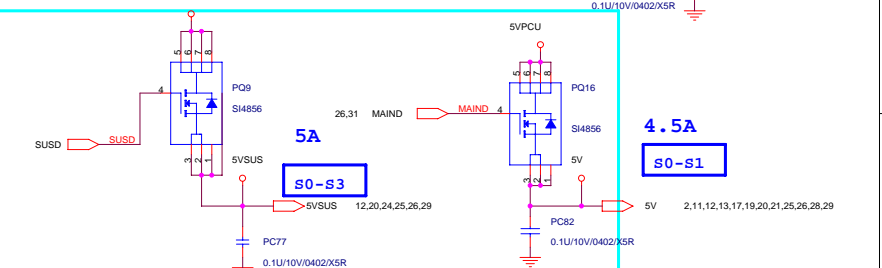
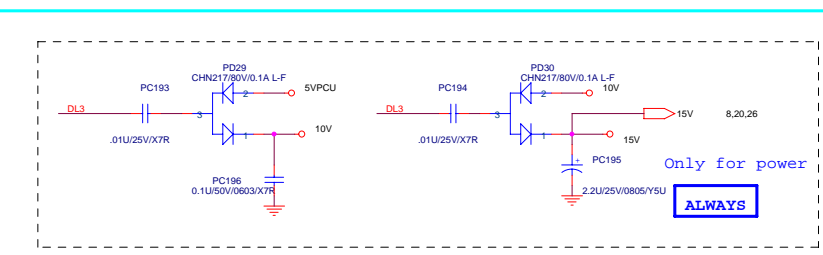
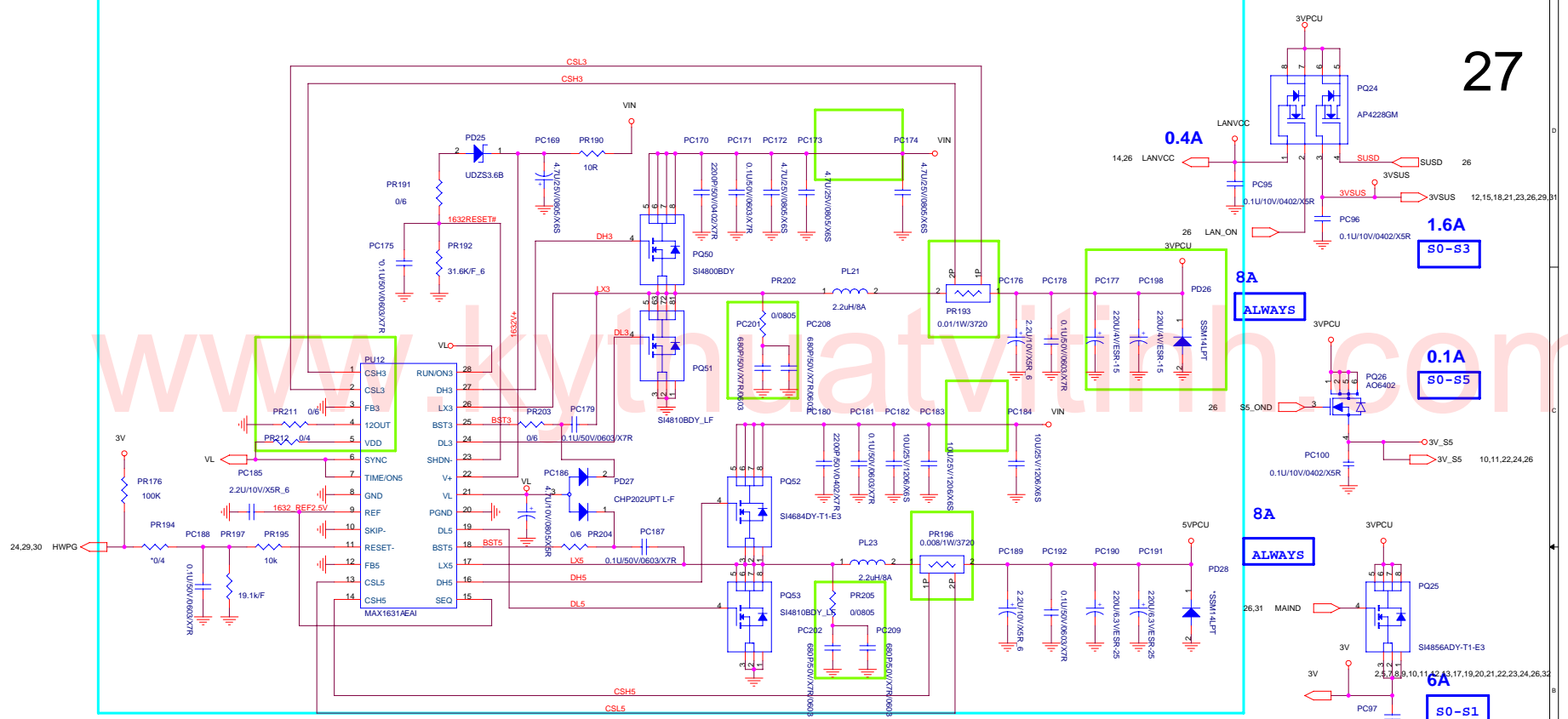
ROM CHIP P/N: AKE34ZAPK01



PROJECT : TT8
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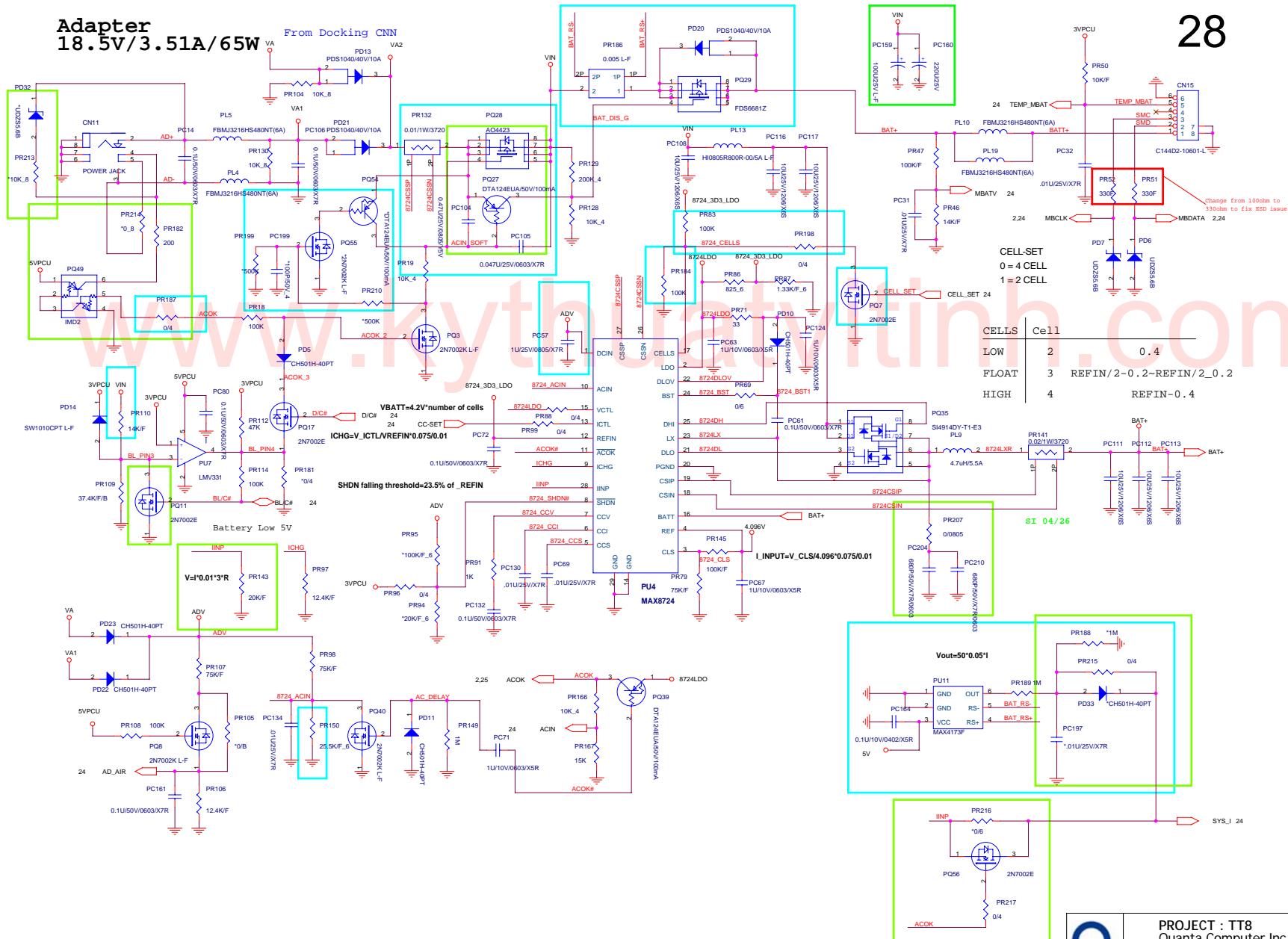
Size Custom | Document Number KB3920 | Rev 1A
Date: Friday, November 24, 2006 | Sheet 24 of 36





Adapter 18.5V/3.51A/65W

From Docking CNN

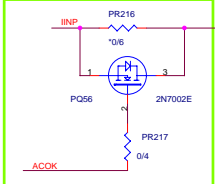
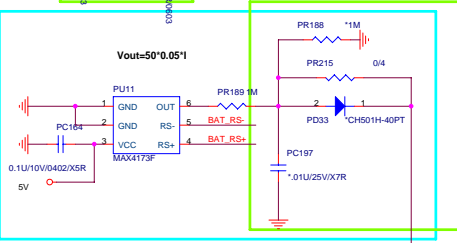


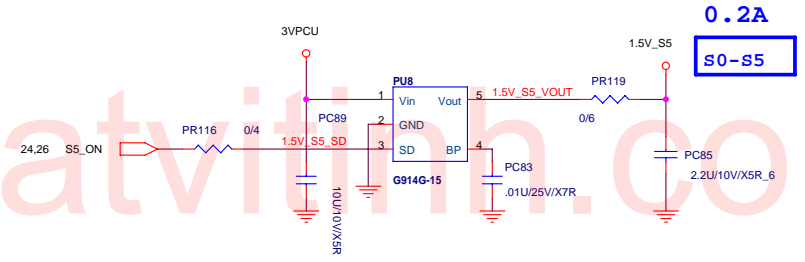
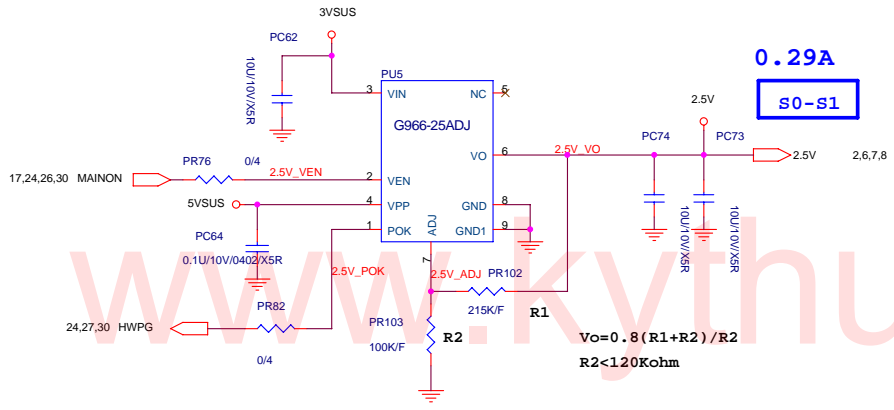
CELL-SET
0 = 4 CELL
1 = 2 CELL

CELLS Cell

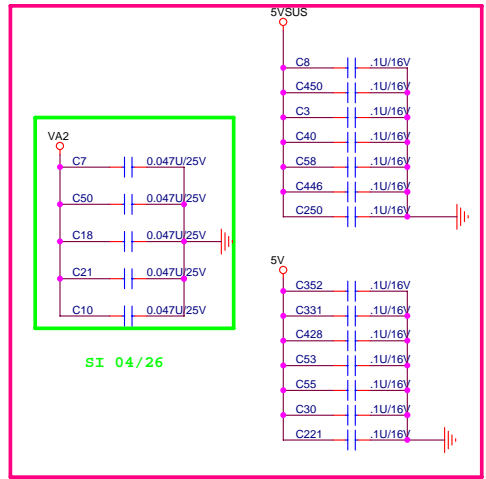
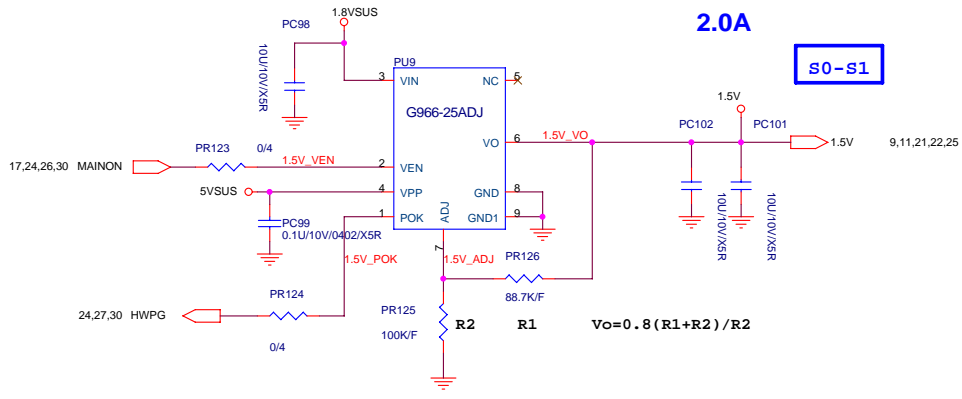
LOW	2	0.4
FLOAT	3	REFIN/2-0.2-REFIN/2_0.2
HIGH	4	REFIN-0.4

SI 04/26





EMI

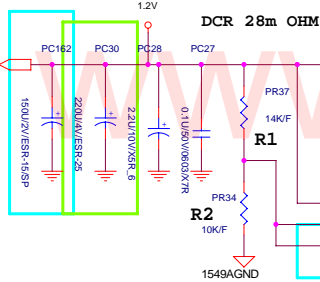


MAX1549

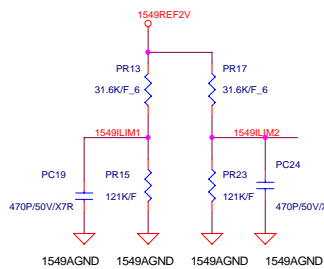
S0-S1

3A

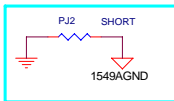
$$V_{cs} = I_L(A) * L_{DCR}(m\Omega) = V_{ILIM}(mV) / 10$$



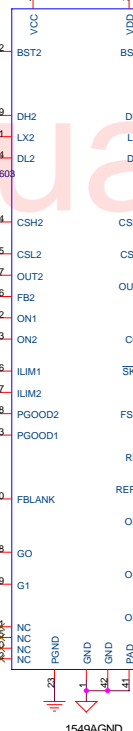
$$V_{out} = 0.5V(1 + R1/R2)$$



SI-2 modified



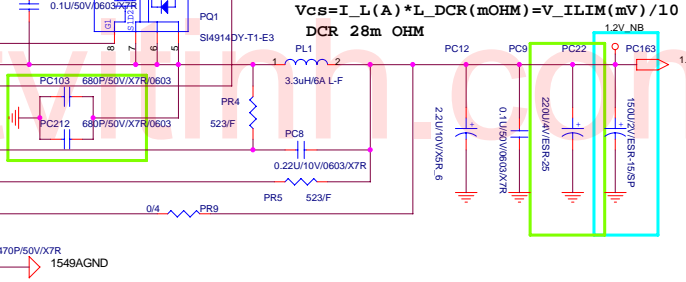
FBLANK			
VCC	OPEN	REF	GND
150us	100us	50us	blanking disabled
150us	100us	50us	100us



S0-S1

3.7A

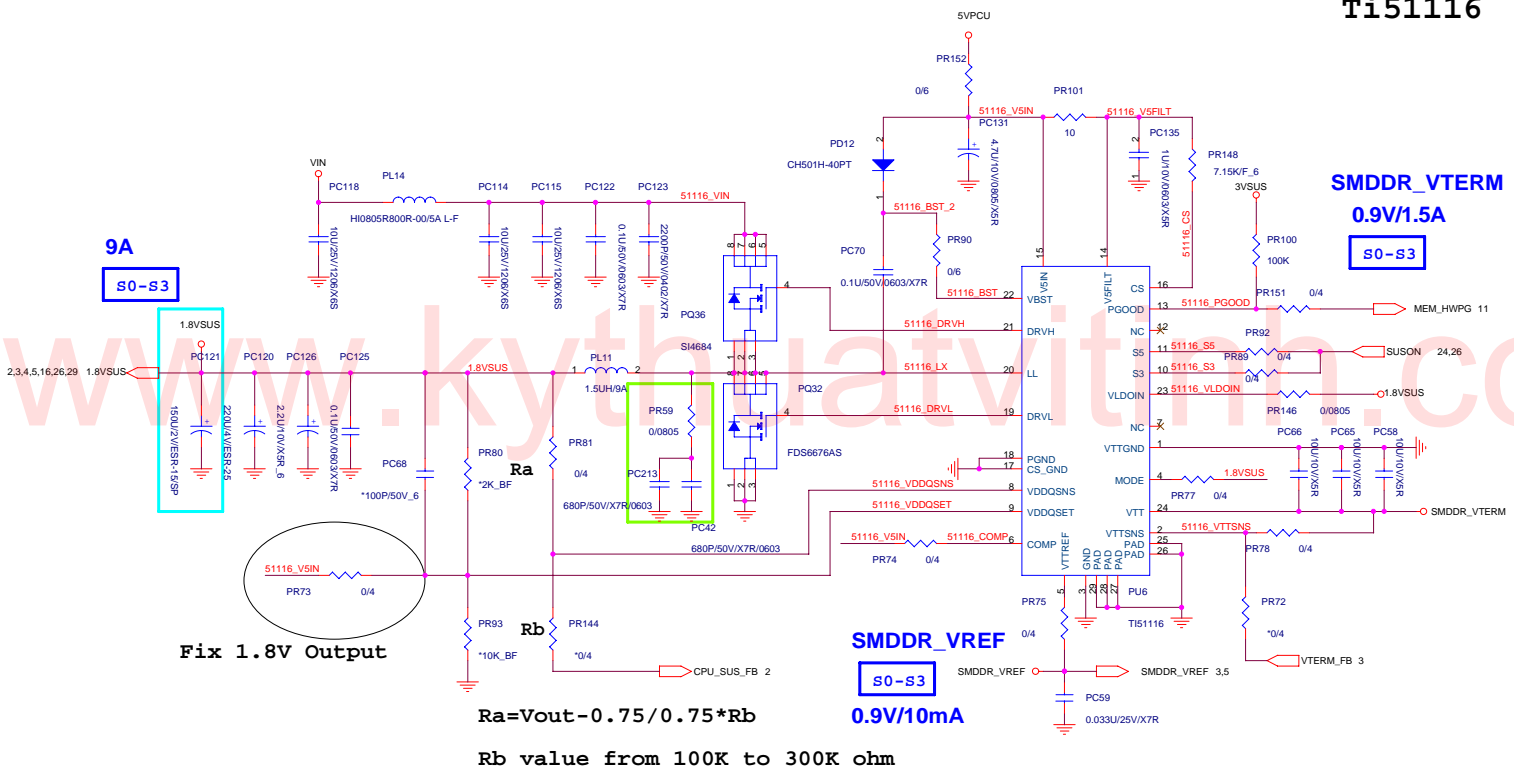
$$V_{cs} = I_L(A) * L_{DCR}(m\Omega) = V_{ILIM}(mV) / 10$$



FSEL: VCC=400kHz, open=300kHz

$$V_{out1} = 2.0V(REQ / (Rb + REQ))$$

INPUTS		OUTPUTS			REQ	VOUT1
G1	G0	OD1	OD2	OD3		
0	0	High-Z	High-Z	Hight-Z	Ra=150K	1.2V
1	0	0	High-Z	Hight-Z	Ra / ROD1=100.1K	1.0V
0	1	High-Z	0	Hight-Z	Ra / ROD2=122.4K	1.1V
1	1	High-Z	High-Z	0	Ra / ROD3=82.02K	



Fix 1.8V Output

$$R_a = V_{out} - 0.75 / 0.75 * R_b$$

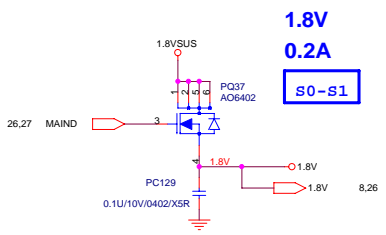
$$R_b \text{ value from } 100K \text{ to } 300K \text{ ohm}$$

Mode	Discharge Mode
V5IN	No discharge
VDDQ	Tracking discharge
Gnd	Non-tracking discharge

$$V_TRIP(mV) = R_TRIP(Kohm) * 10(uA)$$

$$I_OCP = V_trip / Rds_on + I_Ripple / 2$$

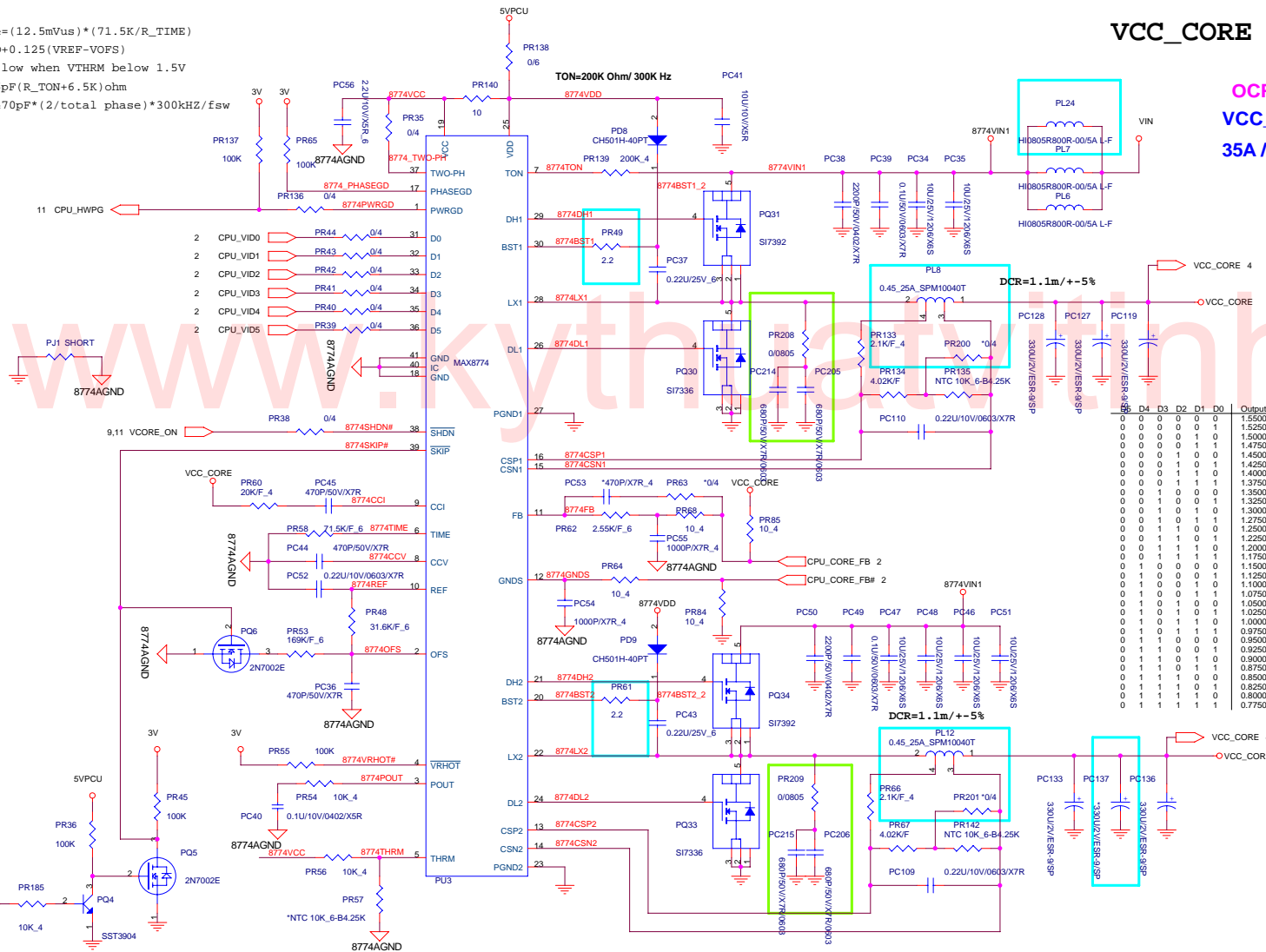
VDDQSET	VDDQ(V)	VTTREF and Vtt	Note
GND	2.5	V_ vddqsnss/2	DDR
V5IN	1.8	V_ vddqsnss/2	DDR2
FB	adjustable	V_VDDQSNSS/2	1.5V < VDDQ < 3V



VCC_CORE MAX8774

Slew rate=(12.5mV/us)*(71.5K/R_TIME)
 VFB=V_VID+0.125*(VREF-V_OFS)
 VRHOT is low when VTHRM below 1.5V
 Tsw=16.26pF*(R_TON+6.5K)ohm
 CCV CAP=470pF*(2/total phase)*300KHZ/fsw

OCp=44A
 VCC_CORE
 35A / 1.05V



D6	D4	D3	D2	D1	D0	Output	D5	D4	D3	D2	D1	D0	Output
0	0	0	0	0	0	1.5500V	1	0	0	0	0	0	0.7625V
0	0	0	0	0	1	1.5200V	1	0	0	0	0	1	0.7500V
0	0	0	0	1	0	1.5000V	1	0	0	0	1	0	0.7375V
0	0	0	0	1	1	1.4750V	1	0	0	0	1	1	0.7250V
0	0	0	1	0	0	1.4500V	1	0	0	1	0	0	0.7125V
0	0	0	1	0	1	1.4250V	1	0	0	1	0	1	0.7000V
0	0	0	1	1	0	1.4000V	1	0	0	1	1	0	0.6875V
0	0	0	1	1	1	1.3750V	1	0	0	1	1	1	0.6750V
0	0	1	0	0	0	1.3500V	1	0	1	0	0	0	0.6625V
0	0	1	0	0	1	1.3250V	1	0	1	0	0	1	0.6500V
0	0	1	0	1	0	1.3000V	1	0	1	0	1	0	0.6375V
0	0	1	0	1	1	1.2750V	1	0	1	0	1	1	0.6250V
0	0	1	1	0	0	1.2500V	1	0	1	0	1	1	0.6125V
0	0	1	1	0	1	1.2250V	1	0	1	1	0	1	0.6000V
0	0	1	1	1	0	1.2000V	1	0	1	1	1	0	0.5875V
0	0	1	1	1	1	1.1750V	1	0	1	1	1	1	0.5750V
0	1	0	0	0	0	1.1500V	1	1	0	0	0	0	0.5625V
0	1	0	0	0	1	1.1250V	1	1	0	0	0	1	0.5500V
0	1	0	0	1	0	1.1000V	1	1	0	0	1	0	0.5375V
0	1	0	0	1	1	1.0750V	1	1	0	0	1	1	0.5250V
0	1	0	1	0	0	1.0500V	1	1	0	1	0	0	0.5125V
0	1	0	1	0	1	1.0250V	1	1	0	1	0	1	0.5000V
0	1	0	1	1	0	1.0000V	1	1	0	1	1	0	0.4875V
0	1	0	1	1	1	0.9750V	1	1	0	1	1	1	0.4750V
0	1	1	0	0	0	0.9500V	1	1	1	0	0	0	0.4625V
0	1	1	0	0	1	0.9000V	1	1	1	0	0	1	0.4500V
0	1	1	0	1	0	0.8750V	1	1	1	0	1	0	0.4375V
0	1	1	0	1	1	0.8500V	1	1	1	0	1	1	0.4250V
0	1	1	1	0	0	0.8250V	1	1	1	1	0	0	0.4125V
0	1	1	1	0	1	0.8000V	1	1	1	1	0	1	0.4000V
0	1	1	1	1	0	0.7750V	1	1	1	1	1	0	0.3875V
0	1	1	1	1	1	0.7500V	1	1	1	1	1	1	0.3750V



PROJECT : TT8
 Quanta Computer Inc.

MODEL

DB1 --->SI1

CHANGE LIST

**TT8 MB
31TT8MB0006**

4/17-4/20

- 1.Change Audio port and senser pin resistor.
Internal MIC change from Pin14,15 to Pin16,17
Docking Mic Change from Pin16,17 to Pin14,15
Docking spk change from Pin23,24 to Pin 43,44
Swap Pin30 and Pin31
Change R486 from Pin 13 to Pin 34 and change from 5.1KK to 10K
Change R251 10K to R485 5.1K
- 2.Change WWAN and WLAN Pin define
Add R487 and R488
- 3.Change TEMP Control chip for leakage, Change Q9 and Q10 to BAM70020074
- 4.Change HDD connector type, RJ45/CRT connector footprint
- 5.Swap LCD connector signal from machine require
- 6.Swap U5 CRT/TV singnal from nVIDIA require
- 7.Change battery and D30 footprint
- 8.Change C251,C242,C138,C66,C71,C276,C277 footprint from 0603 to 0402
- 9.Add Q36,Q37,R489,C661,R490 for Docking MIC detect
- 10.Change SW5 and CN8 footprint for machinecal request
- 11.Change L41 to PBY201209T-300Y-N (Footprint : 0805)
- 12.Delect H3 and H4 for machinecal change
- 13.Change C20 from 0.1U to 1U (Fix LCD rise time)
- 14.Move Net "SLP_BTN#" from pin99 to pin87
- 15.Modify Docking mute LED circuit
- 16.Modify U25 SCI# signal from BIOS request, AddR491,R492
- 17.Modify Buletooth switch and ODD BAYINS# to EC
- 18.Change caps lock connector footprint from machencal request
- 19.Add U30,R495,R494,R493,Q38 for reserve SIM card
- 20.Change 4-in-1 card footprint
- 21.Add R44,R43,R48 Remove R62,R64,R69,R34,R24,R36
- 22.Change L45,L46,L47 to 0 ohm
Del C503,C504,C505,C493,C494,C495 for D-SUB function

Model OT1 MB BOARD

Page FROM TO

1	1A	
2	1A	
3	1A	
4	1A	
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**PROJECT : TT8
Quanta Computer Inc.**

MODEL

S11 ---->PV1

CHANGE LIST

**TT8 MB
31TT8MB0006**

5/17-7/11

- 1.Exchange Audio port
- External MIC Exchange Pin22 and Pin21
- CD Line Exchange Pin18 and Pin20
- Internal MIC Exchange Pin16 and Pin17
- Docking Mic Exchange Pin14 and Pin15
- 3.Change R478 from 22ohm to 0ohm
- 4.Change R462 0ohm to C666 0.47u for Audio chip distortion
- 5.Exchange R272 and R263, R273 and R264 for amplifier gain change
- 6.Change Q8 from BAM51030Z15 to BAM23010Z30 for Rdson issue
- 7.Remove C439 for MS pro card can not detect
- 8.Add C667,C668,C669,C670,C671,C672,C673,C674,C675,C676 for WLAN con not detect issue
- 9.Add reverse circuit for LED issue
- 10.Delect Q7 for Cap lock LED
- 11.Add EMI Cap C93,C118,C496,C497,C499,C566,C589,C555,C334,C337
- 12.Change CN19,CN27,CN28,CN29 footprint
- 14.Change Sim connector (Add detect pin)
- 15.Move Docking CRT signal after PI circuit
- 16.Add R500, R501 for Audio chip function
- 17.Add D37 and R502 for nVIDIA solution
- 18.Move D22 from +5VCRT to +5VCRT3
- 19.Change Docking detect circuit
- 20.Delet H20 H21
- 21.Exchange MINI_DATA and MINI_CLK
- 22.Add Diode for SATA and ODD LED control
- 23.Add power controller for 5V shutdown
- 24.Change WLAN LED circuit
- 25.Add Res for ACZ signal
- 26.Delete H7 and H14 for ME change
- 27.Modify SB to Audio and Modem signal

Model OT1 MB BOARD

Page FROM TO

Page	FROM	TO
1	1A	
2	1A	
3	1A	
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MODEL

CHANGE LIST

**TT8 MB
31TT8MB0006**

PV1 --->PV2
9/8-10/17

1. Page17 change voltage from +3V to 3V fix the Mic can not work
2. Page17 change R14 from 4.7K to 5.6K to fix LCCVDD rise time
3. Page17 change LCD cable Pin22 and Pin15 for switch function, Pin7 change to 32K_BTN
4. Page24 add GPIO for switch function
5. Page10 Change cap from 18p to 22p
6. Page17 Change C392 and C395 from 10U to 1U to fix Docking noise
7. Page16 add PA11(EMI spring)
8. Page21 Exchange BBC0EX1 and BBC0EX2
9. Page20 remove C614, C607, C406, C414, C404, C405
10. Page20 Change C635, C415, C416 from TAN to ELEC
11. Page11 Del R205 and Add R207 for Bios check

Model OT1 MB BOARD

Page FROM TO

Page	FROM	TO
1	1A	
2	1A	
3	1A	
4	1A	
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MODEL

CHANGE LIST

Model OT1 MB BOARD

Page FROM TO

**TT8 MB
31TT8MB0006**

PV2 --->MV1
10/17-11/15

- 1.Page10 Exchange USB0+/- with USB3+/- signal
- 2.Page12 Change CN12 Pin1 from 5VSUS to 3V
- 3.Page17 Change C648 and C656 from 4.7U to 22U to fix Vista issue
- 4.Page19 Change L35-L38 from LZA10-2ACB104MT to BK1608HS241-T
- 5.Page19 Change Gain from 15.6db to 10db
- 6.Page17 Del R260,R267,D312,D322 for Docking MIC
- 7.Page17 ADD R520,R521,R522,R523 for Docking MIC
- 8.Page21 Change PR51 PR52 from 100ohm to 330ohm to fix ESD issue
- 9.Page20 unstuff R188 to fix ODD problem
- 10.Page11 Change the board ID1 from low to high
- 11.Page15 Change Cap (C60,C56,C441,C44,C45)from 0.1u to 1u
- 12.Page15 Change Res (R318,R313,R312)from 39K to 10K
- 13.Page17 Add 0.01u(C693, C694) to fix high frequency problem
- 14.Page14 remove the cap(C408,C409) from MV build
- 15.Page7 Reserve C696 for nVIDIA
- 16.Page15 Reserve R525 and C695 for 3VSUS drop
- 17.Page23 Change LED4 for ME requests

Page	FROM	TO
1	1A	
2	1A	
3	1A	
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