

# Compal confidential

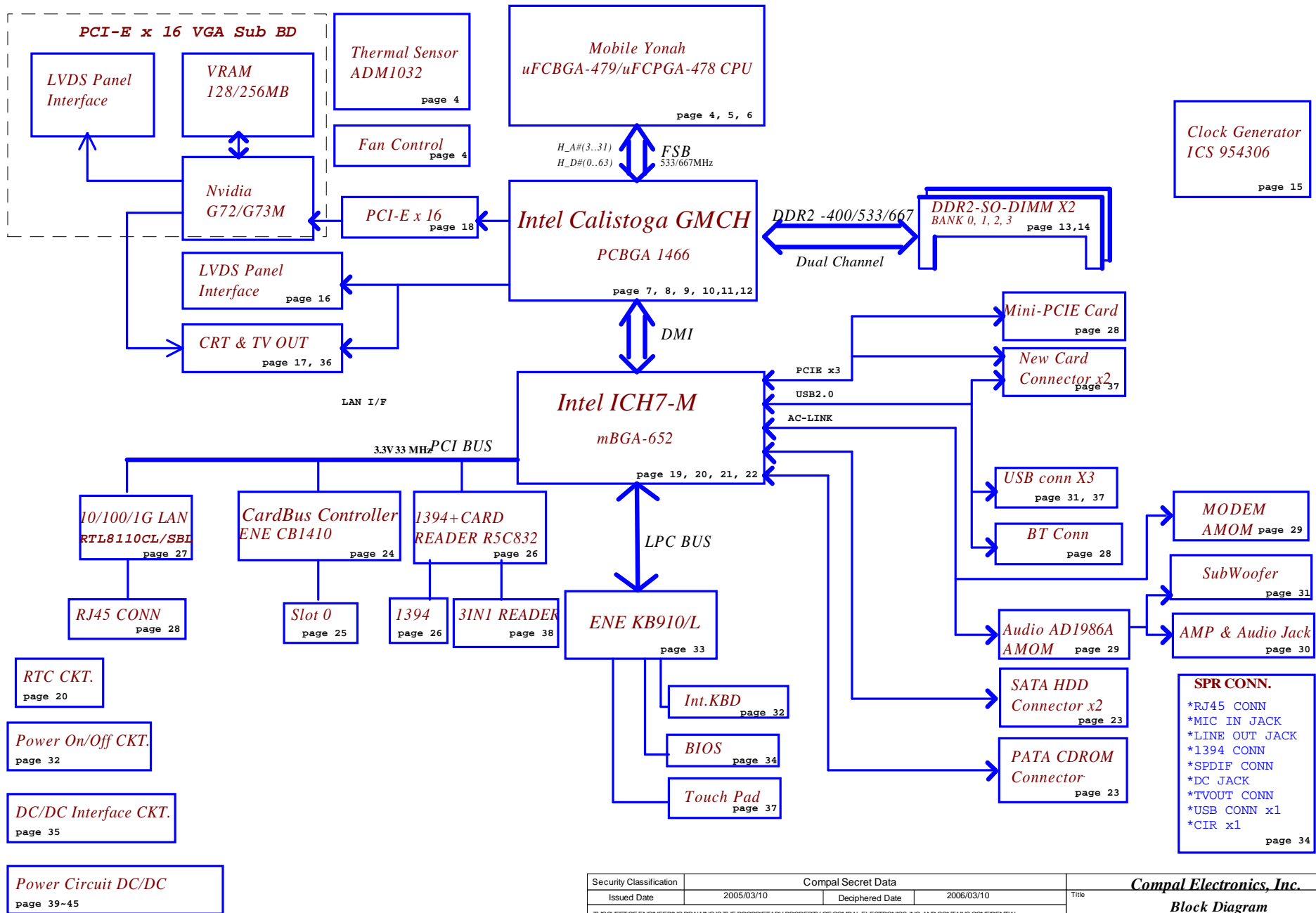
## HGT30/31 Schematics Document

Mobile Yonah uFCPGA with Intel  
Calistoga\_GM/PM+ICH7-M core logic

2006-02-15

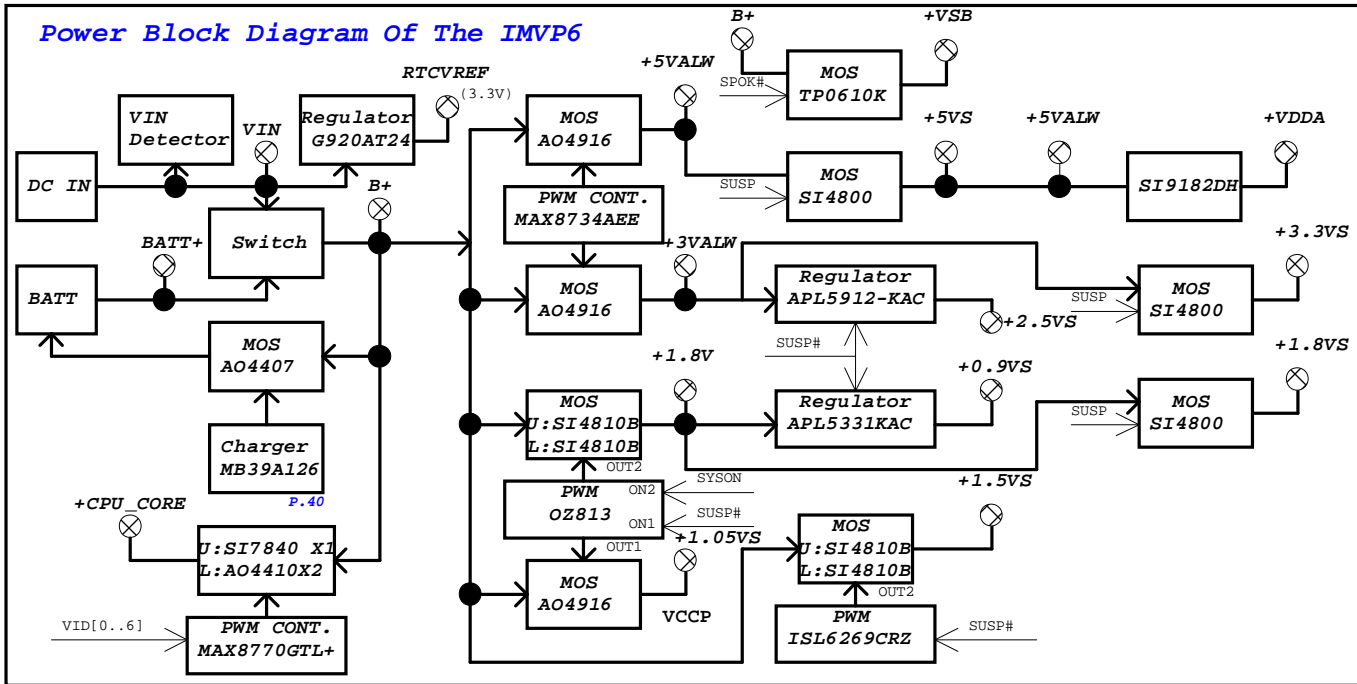
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### Power Block Diagram Of The IMVP6



### PCI DEVICES

EXTERNAL	IDSEL#	REQ/GNT#	PIRQ
CARD BUS CB1410	AD20	2	PCI_PIRQA#
CARD READER & 1394 R5C832	AD22	0	PCI_PIRQ# PCI_PIRQH#
LAN CONTROLLER RTL8110SBL/CL	AD17	3	PCI_PIRQF#

### PCIE LANE

LANE	DEVICE
1	Express Card
2	Mini Card

### USB

PORT	DEVICE
0	LEFT SIDE
1	BLUE TOOTH
2	RIGHT SIDE
3	NC
4	RIGHT SIDE
5	NC
6	NC

### I2C / SMB Address

<b>KB910/L (SM1-Pulled-Up 5V)</b>	
DEVICE	ADDRESS R/W
AT24C16AN	A3/A2 H
SMART BATTERY	17/16 H
<b>KB910/L (SM2-Pulled-Up 3.3V)</b>	
ADM1032AR	99/98 H
<b>G7xM (I2C-Pulled-Up 3.3V)</b>	
G781-1 (RESERVED)	9B/9A
<b>ICH7M SM Bus</b>	
ICS9LPR325AKLFT	D3/D2 H (3.3V)
DDR II DIMMO	A1/AO H (3.3V)
DDR II DIMM1	A3/A2 H (3.3V)
Express Card	NC (2.5V)
Mini-Express	NC (2.5V)

### BOM Structure

MARK	FUNCTION
@	NC FOR ALL
EXP@	PCIE-NEW CARD
BT@	BLUE TOOTH
UMA@	Internal 945GM
VGA@	External G7xM
SUBWOOFER@	SUBWOOFER
HGT30@	HGT30
CB@	PCMCIA/CARD BUS
GIGA@	8110SBL(SCL)Giga LAN
10/100@	8110CL 10/100Mb LAN

### Voltage Rails

power plane	+B LDO3 LDO5	+5VALW +3VALW	+1.8V +5V	+5VS +3VS +2.5VS +1.8VS +1.5VS +VGA CORE +1.2VS +0.9VS +CPU CORE +VCCP
State				
S4 : STD				
S5 : SOFT OFF				
s0	O	O	O	O
s1	O	O	O	O
s3 : STR	O	O	O	X
s5 S4/AC	O	O	X	X
s5 S4/ Battery only	O	X	X	X
s5 S4/AC & Battery don't exist	X	X	X	X

### MB ID

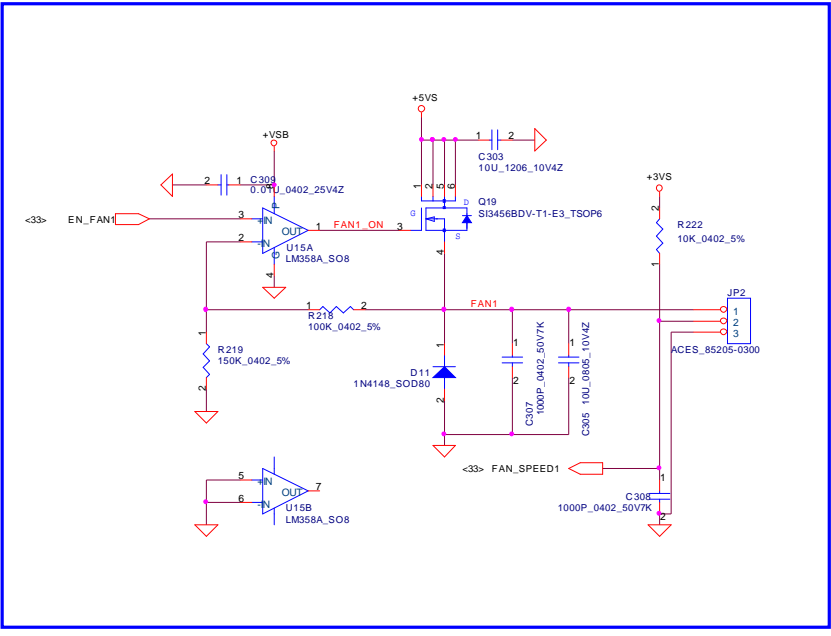
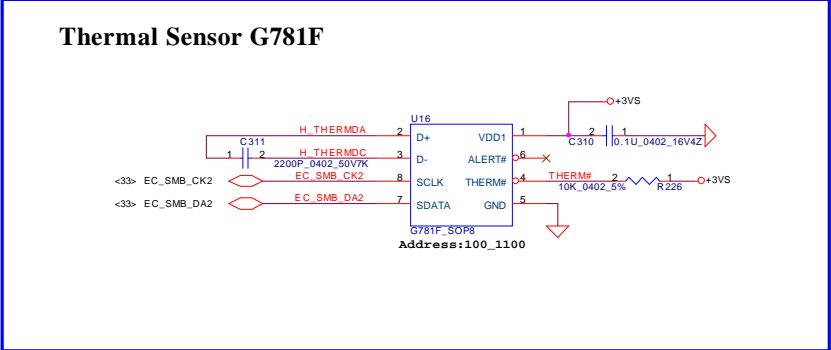
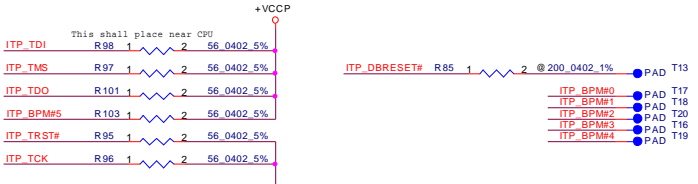
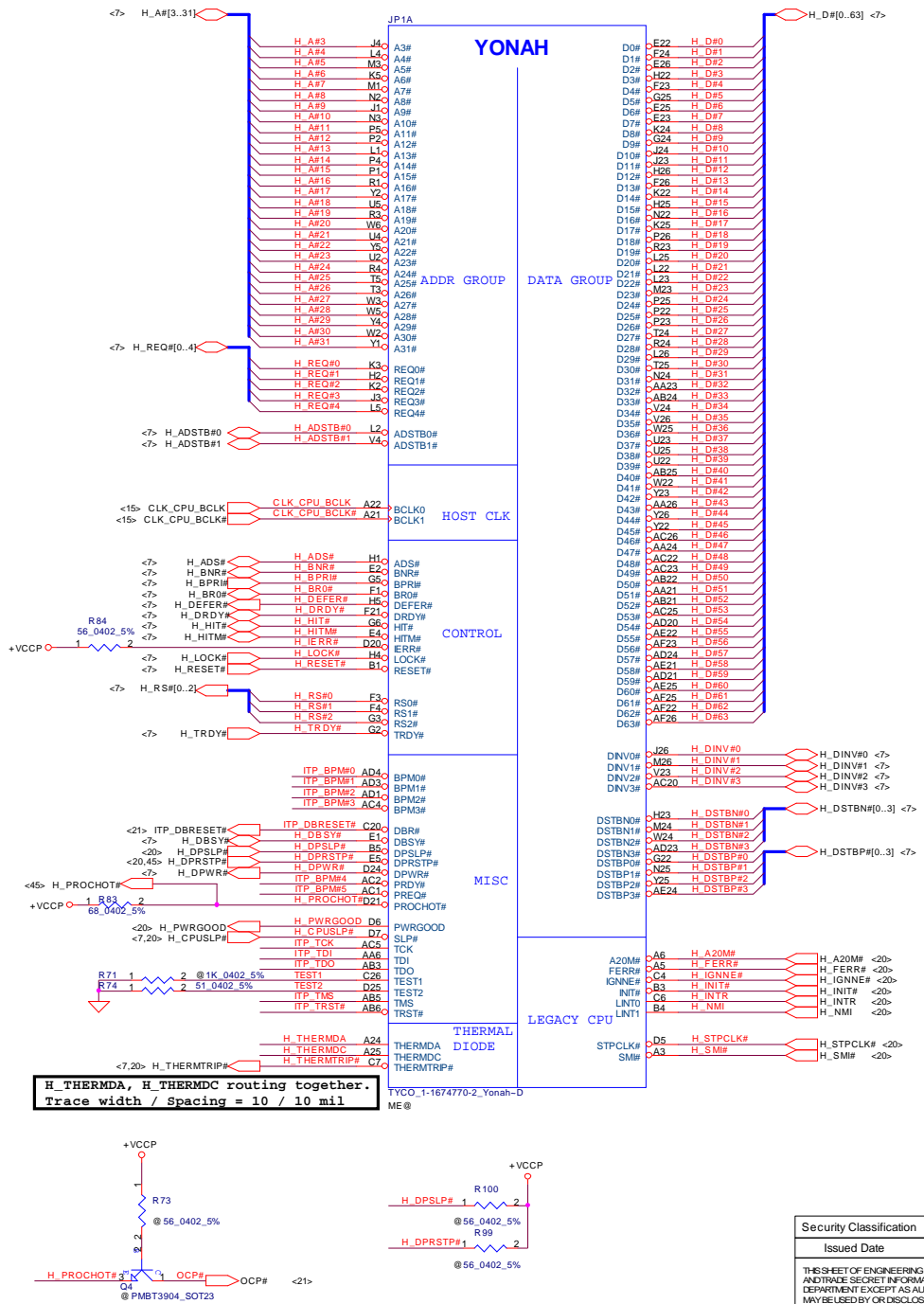
MB ID	P NAME
0	HGT-30
1	HGT-31

### BRD ID

ID	MB REV#	R115(Rb)	Vab
0	R01 (EVT)	0	0V
1	R02 (DVT)	8.2K	0.25V
2	R03	18K	0.50V
3	R04	33K	0.82V
4		56K	1.19V
5		100K	1.65V
6		200K	2.20V
7		NC	3.30V

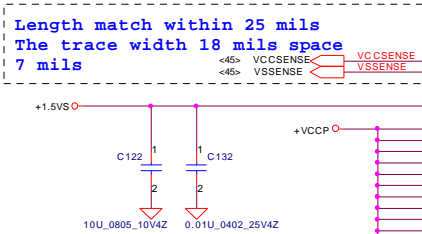
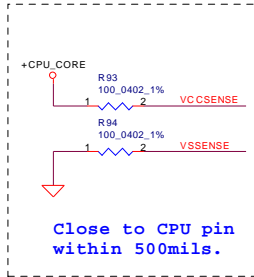
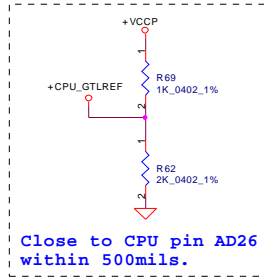
+3VALW	KB910L SB RTL8110SBL/CL	mA 160mA
+CPU_CORE	CPU	36A
+VCCP	CPU NB	2.5A 9.8A (14.7A)
+5VS	EXPRESS CARD HDD ODD MDC APA2066 TPA0211 AD1986 USB PORT * 6	1A 1.5A 1.8A 300mA 1A mA 70mA 3A
+3VS	NB EXPRESS CARD CLK_GEN LCDVCC VGA CARD (G7XM) SB R5C832 BIOS ROM KB910L CB1410	480mA 1A 200mA 1A 655mA 680mA mA 15mA 200mA mA
+2.5VS	VGA CARD (G7XM) NB	130mA (143mA)
+1.8V	DDR2_DIMM NB (667Mhz)	8A 3.1A
+1.8VS	GDDR2 VGA CARD (G7XM)	6A 4.06A
+0.9VREF	DDR2_DIMM	10mA
+0.9VS	GDDR2 DDR2_DIMM	1A 2A
+1.5V	SB	40mA
+1.5VS	NB SB MiniCard EXPRESS CARD VGA CARD (G7XM)	8.9A (13.8A) 3.8A 1A 0.65A 2A

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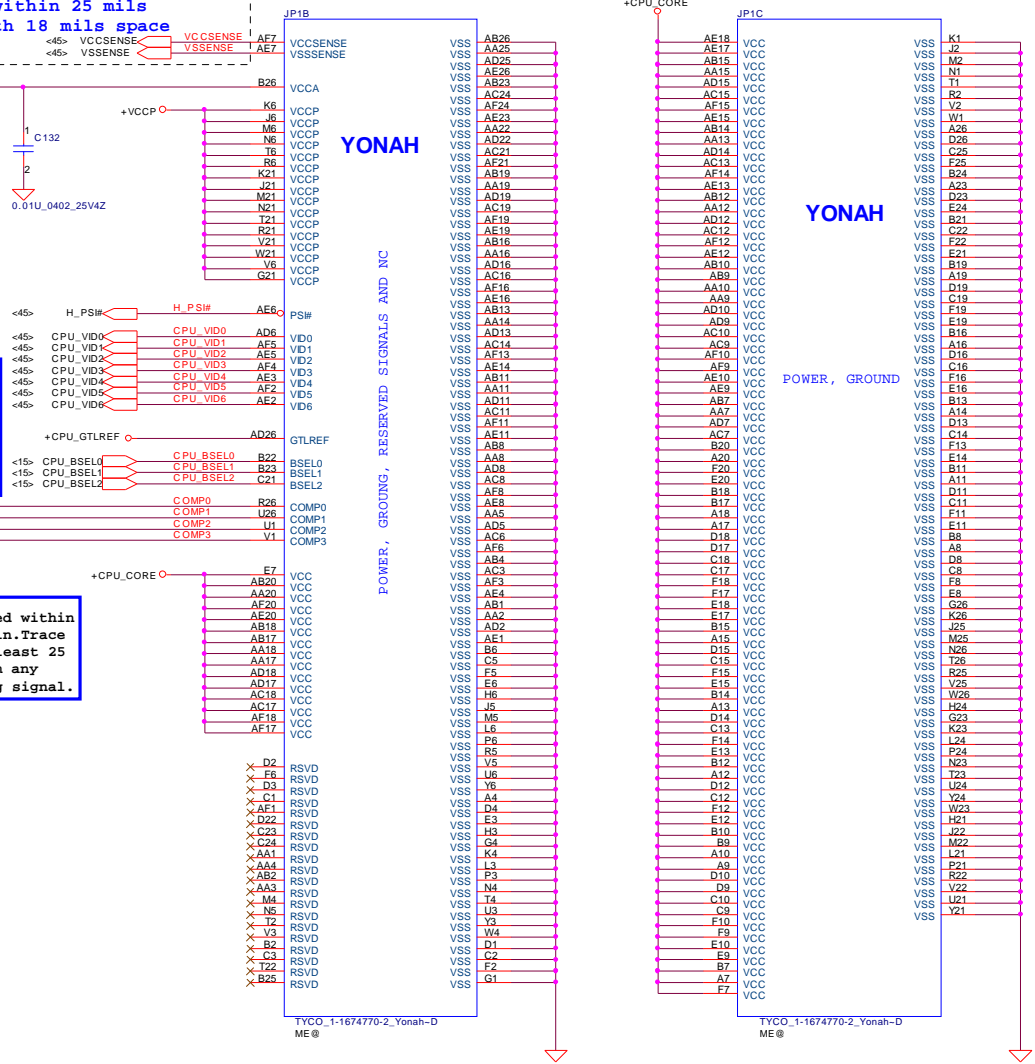
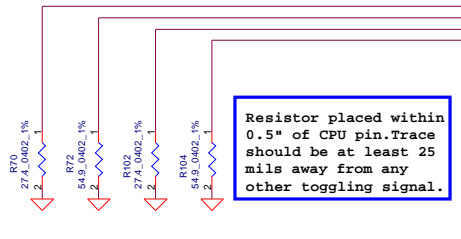


H\_THERMDA, H\_THERMDC routing together.  
Trace width / Spacing = 10 / 10 mil

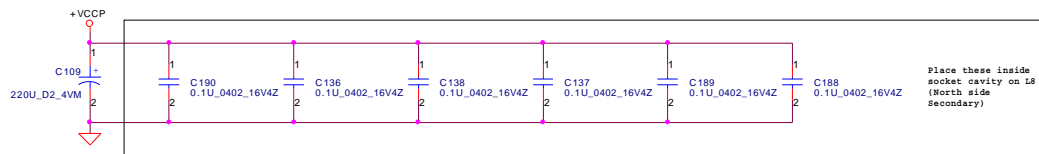
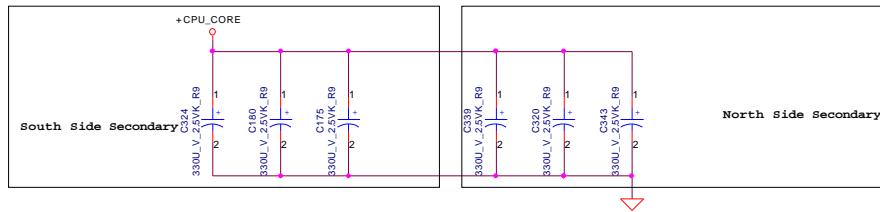
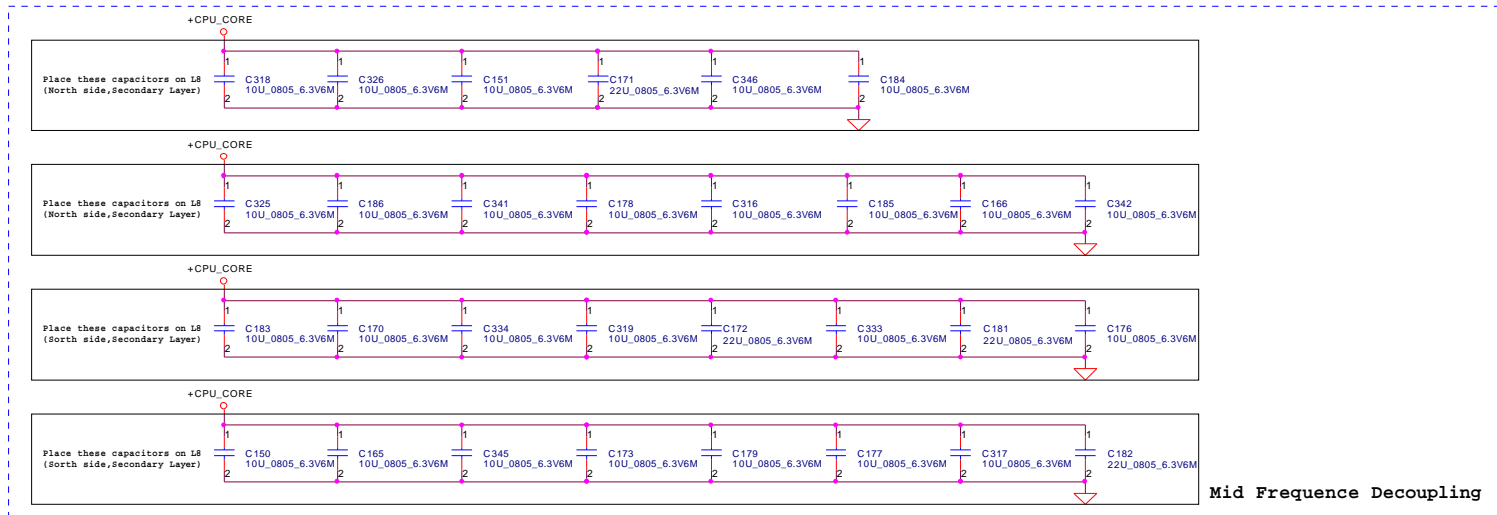
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CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
133	0	0	1
166	0	1	1

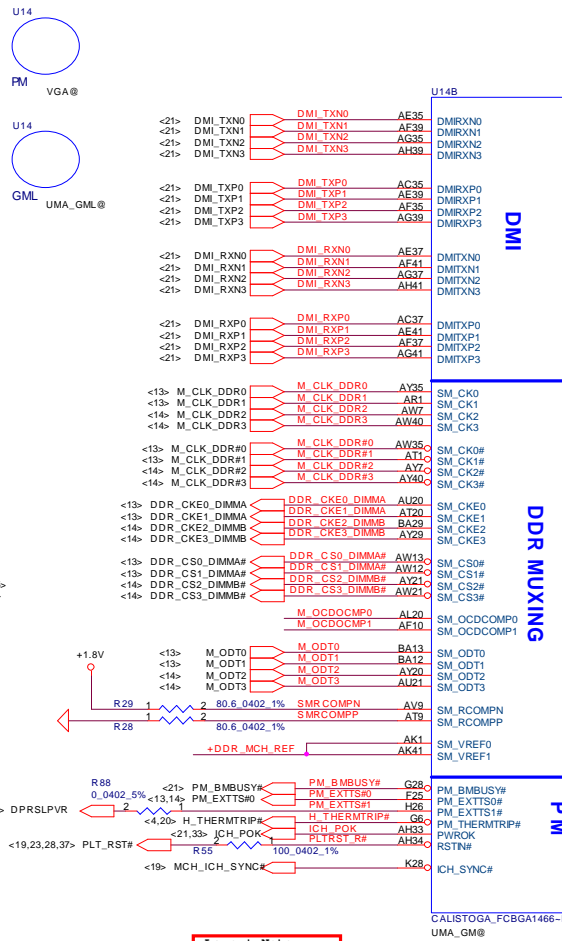
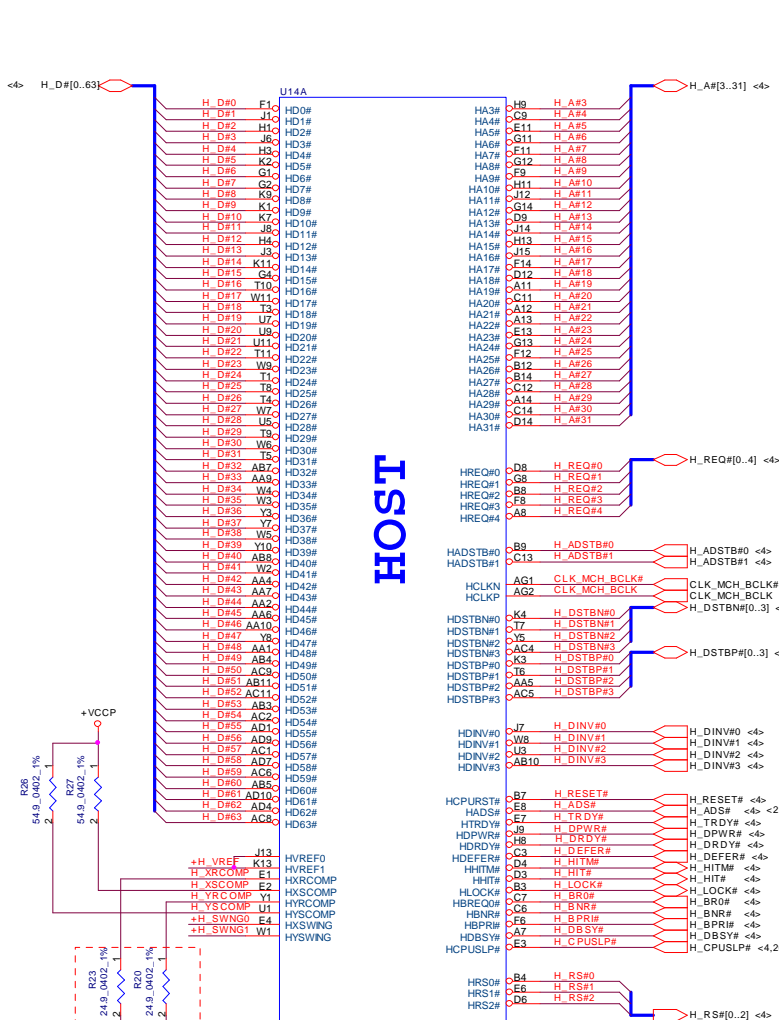


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<b>CPU Bypass capacitors</b>		
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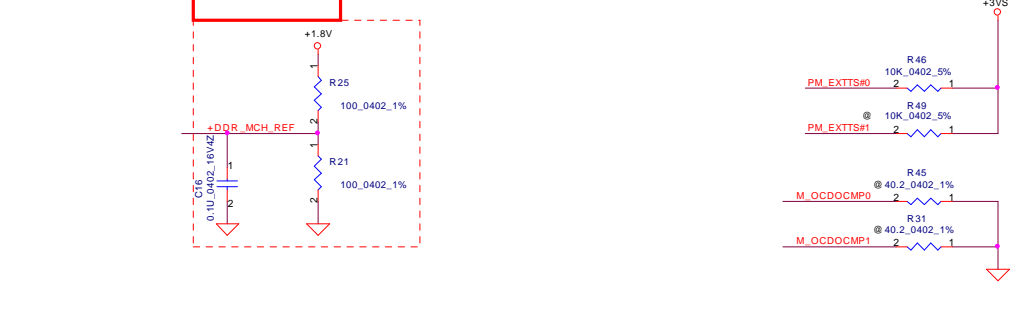
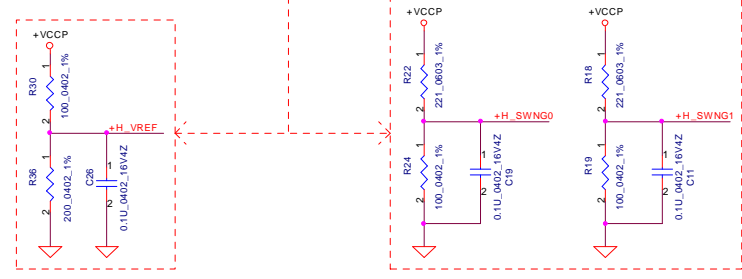


Description at page15

Signal	Pin	Function
K16	MCH_CLKSEL0	MCH_CLKSEL0 <15>
K18	MCH_CLKSEL1	MCH_CLKSEL1 <15>
J18	MCH_CLKSEL2	MCH_CLKSEL2 <15>
F18	CFG3	CFG3
E15	CFG4	CFG4
F15	CFG5	CFG5 <11>
E18	CFG6	CFG6
D19	CFG7	CFG7 <11>
D16	CFG8	CFG8
G18	CFG9	CFG9 <11>
D15	CFG10	CFG10
G15	CFG12	CFG12 <11>
C15	CFG14	CFG14 <11>
H16	CFG15	CFG15 <11>
G18	CFG16	CFG16 <11>
H15	CFG17	CFG17 <11>
K27	CFG19	CFG19 <11>
J26	CFG20	CFG20 <11>
G_CLKP	AG33 CLK MCH 3GPLL	CLK_MCH_3GPLL <15>
G_CLKN	AF33 CLK MCH 3GPLL#	CLK_MCH_3GPLL# <15>
D_REF_CLKN	A27 CLK MCH DREFCLK#	CLK_MCH_DREFCLK# <15>
D_REF_CLKP	A26 CLK MCH DREFCLK	CLK_MCH_DREFCLK <15>
D_REF_SSCLKN	C40 MCH SSCDREFCLK#	CLK_MCH_SSCDREFCLK# <15>
D_REF_SSCLKP	D41 MCH SSCDREFCLK	CLK_MCH_SSCDREFCLK <15>
CLK_REQ#	H32 MCH CLKREQ#	MCH_CLKREQ# <15>
A3	NC0	NC0
A39	NC1	NC1
A4	NC2	NC2
A40	NC3	NC3
AW1	NC4	NC4
AW4	NC5	NC5
AY1	NC6	NC6
BA1	NC7	NC7
BA2	NC8	NC8
BA3	NC9	NC9
BA4	NC10	NC10
BA41	NC11	NC11
C1	NC12	NC12
AY4	NC13	NC13
B2	NC14	NC14
B41	NC15	NC15
C41	NC16	NC16
D1	NC17	NC17
D1	NC18	NC18
T32	RESERVED1	RESERVED1
R32	RESERVED2	RESERVED2
F3	RESERVED3	RESERVED3
AG1	RESERVED4	RESERVED4
AF11	RESERVED5	RESERVED5
H7	RESERVED6	RESERVED6
J19	RESERVED7	RESERVED7
A41	RESERVED8	RESERVED8
A24	RESERVED9	RESERVED9
D27	RESERVED10	RESERVED10
D27	RESERVED11	RESERVED11
A35	RESERVED12	RESERVED12
A35	RESERVED13	RESERVED13

Layout Note:  
+DDR\_MCH\_REF trace width and spacing is 20/20.

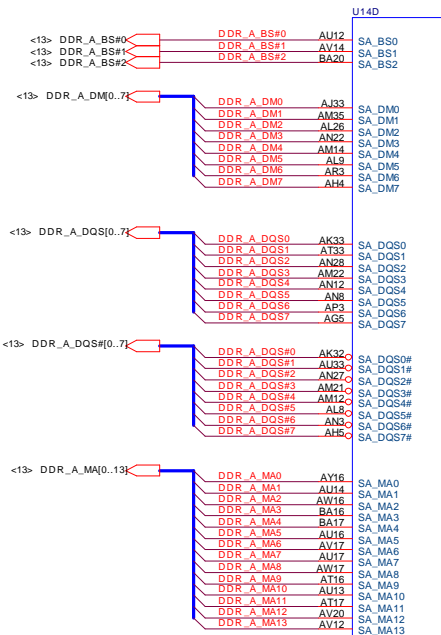
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H\_XRCOMP / H\_YRCOMP / H\_VREF / H\_SWNG0 / H\_SWNG1 trace width and spacing is 10/20.



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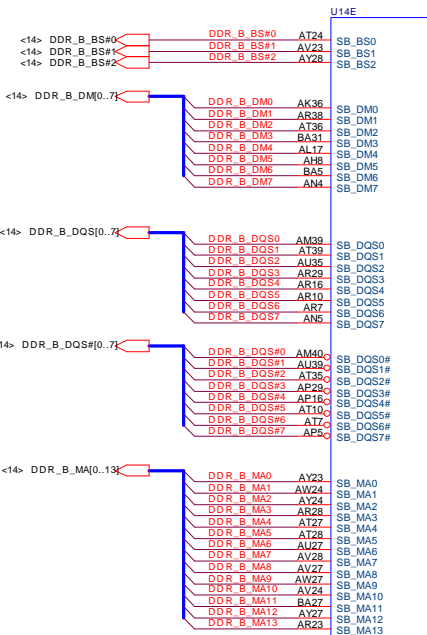




**DDR SYS MEMORY A**

CALISTOGA\_FCBGA1466-D  
UMA\_GM®

check layout



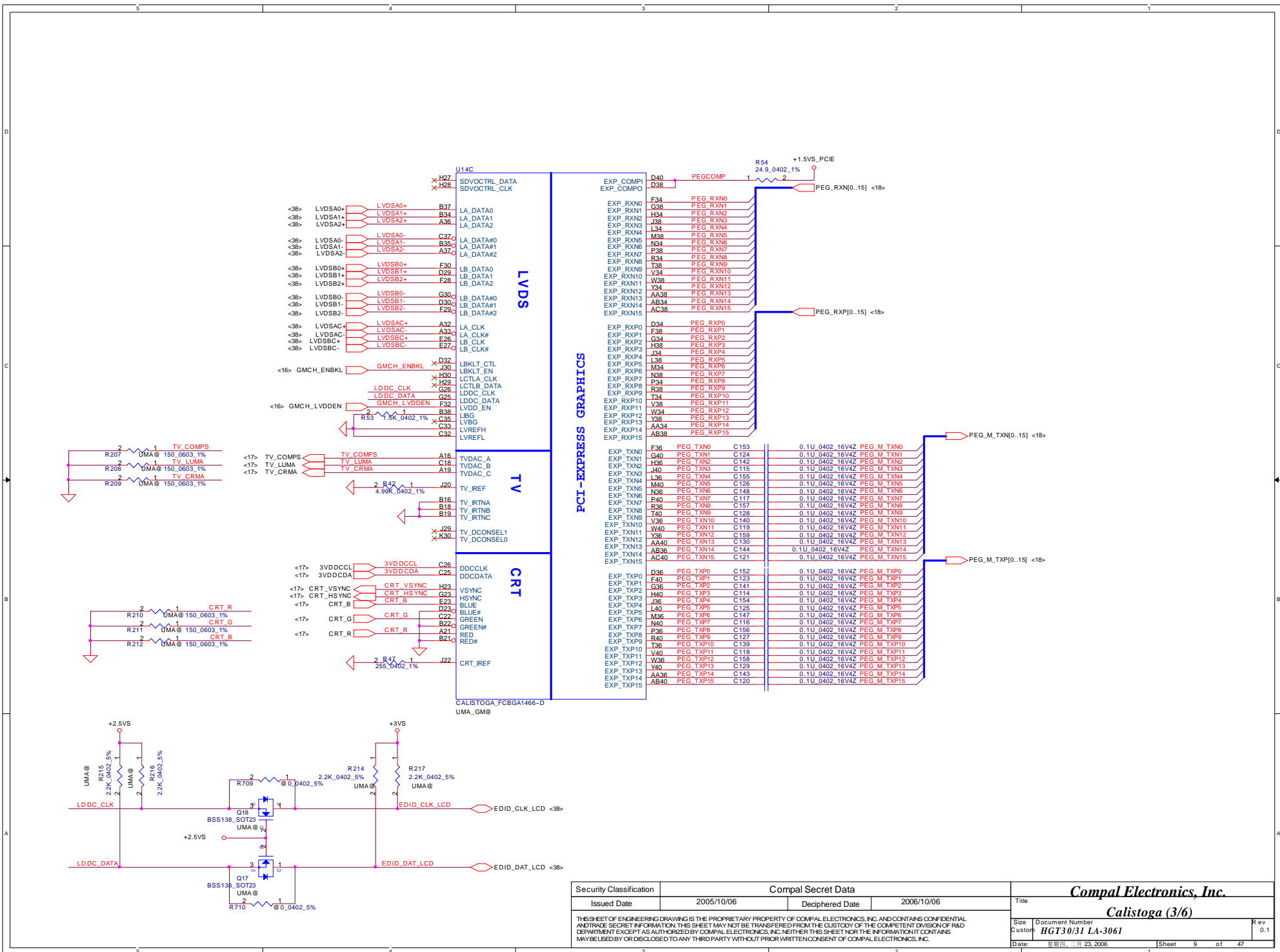
**DDR SYS MEMORY B**

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UMA\_GM®

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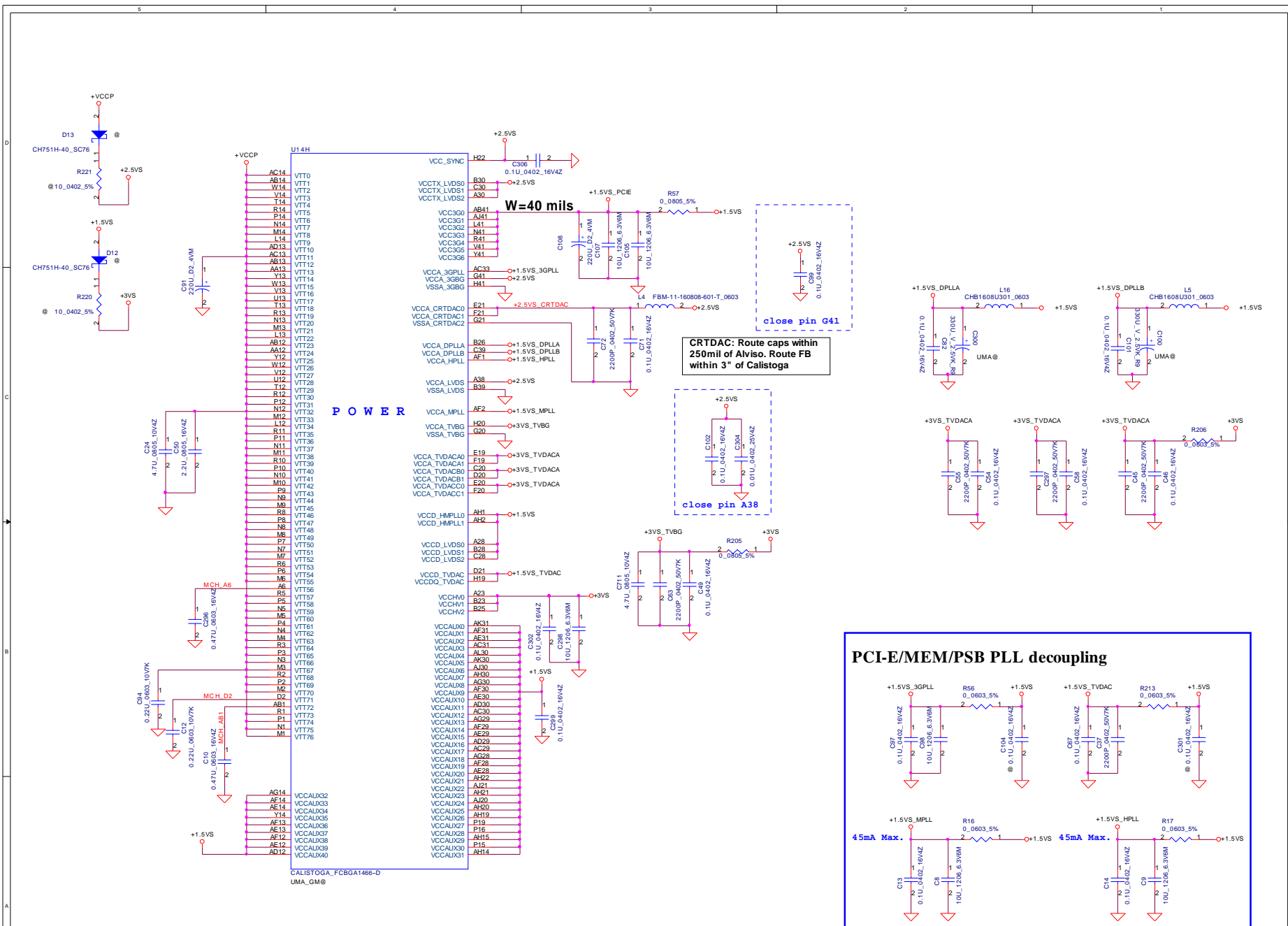
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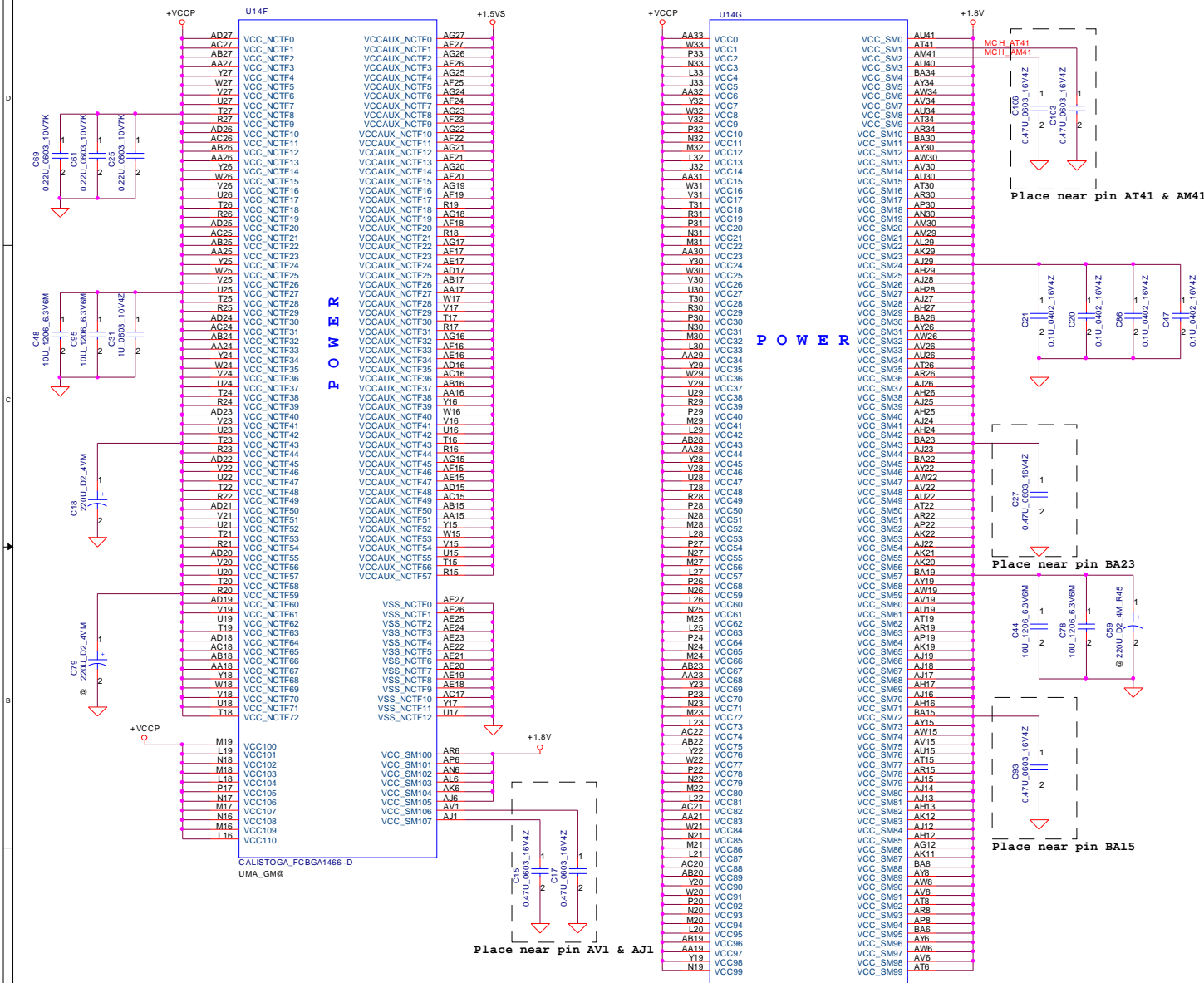
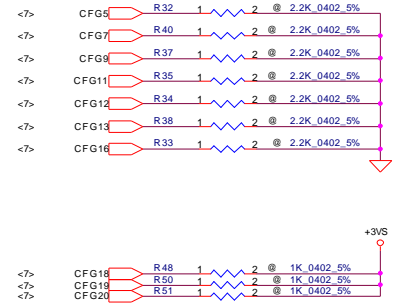
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### Strap Pin Table

CFG[3:17] have internal pull up

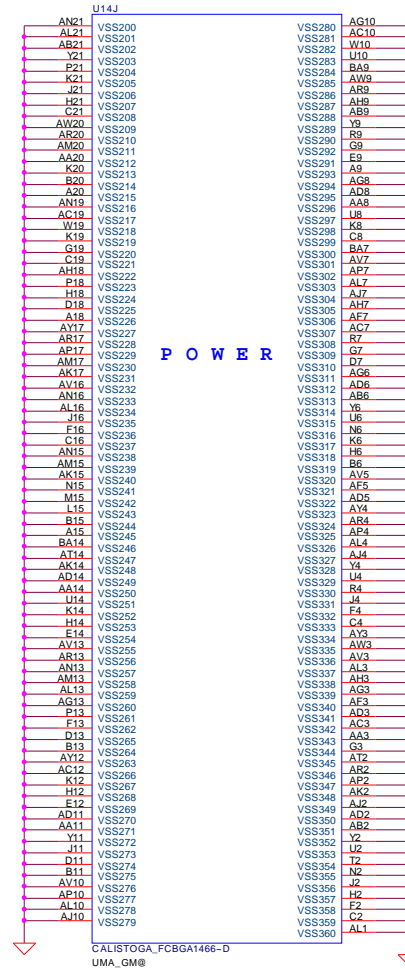
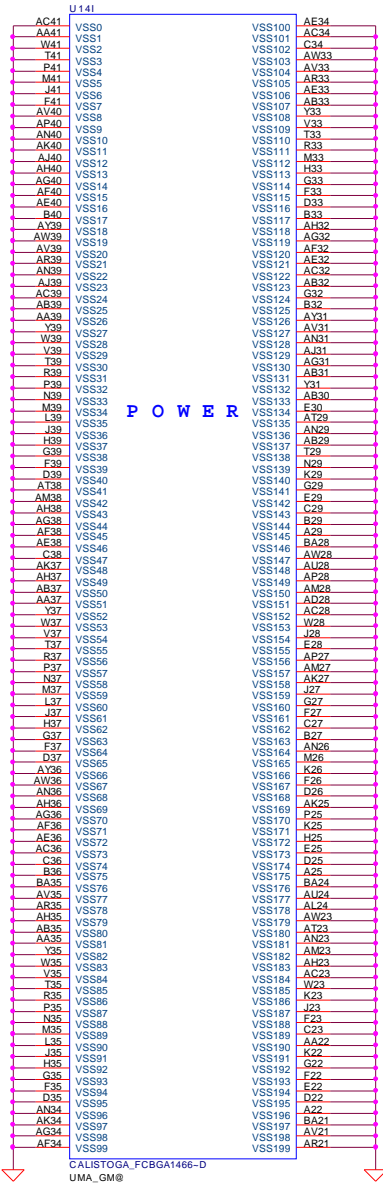
CFG[19:18] have internal pull down

CFG[2:0]	011 = 667MT/s FSB 001 = 533MT/s FSB
CFG5	0 = DMI x 2 1 = DMI x 4 * (Default)
CFG7	0 = Reserved 1 = Mobile Yonah CPU * (Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation (Default) *
CFG6	0 = Reserved
PSB 4X CLK Enable	1 = Calistoga *
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation * (Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled * (Default)
CFG10 CFG18	10 = 1.05V * (Default) 01 = 1.5V
CFG19	0 = Normal Operation * (Default) 1 = DMI Lane Reversal Enable
SDVO_CTRLDATA	0 = No SDVO Device Present * (Default) 1 = SDVO Device Present
CFG20 (PCIE/SDVO select)	0 = Only PCIE or SDVO is operational. * (Default) 1 = PCIE/SDVO are operating simu.



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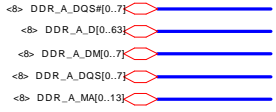
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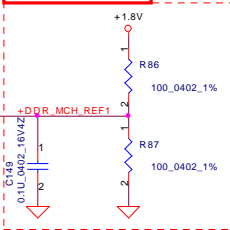
POWER

POWER

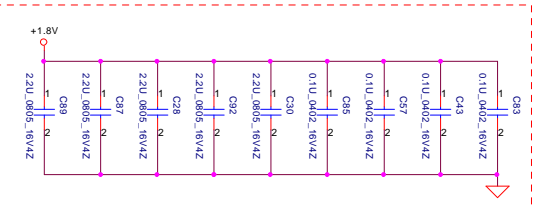
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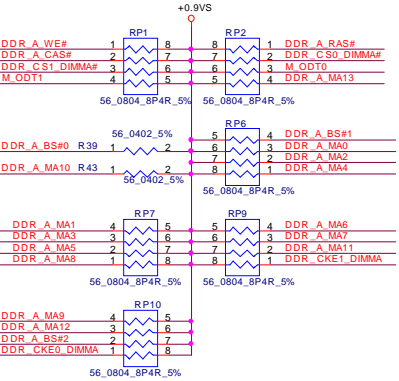
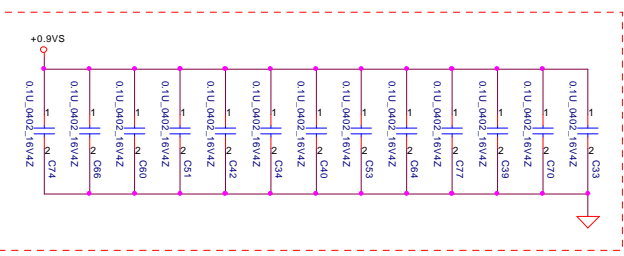
**Layout Note:**  
+DDR\_MCH\_REF  
trace width and  
spacing is 20/20.



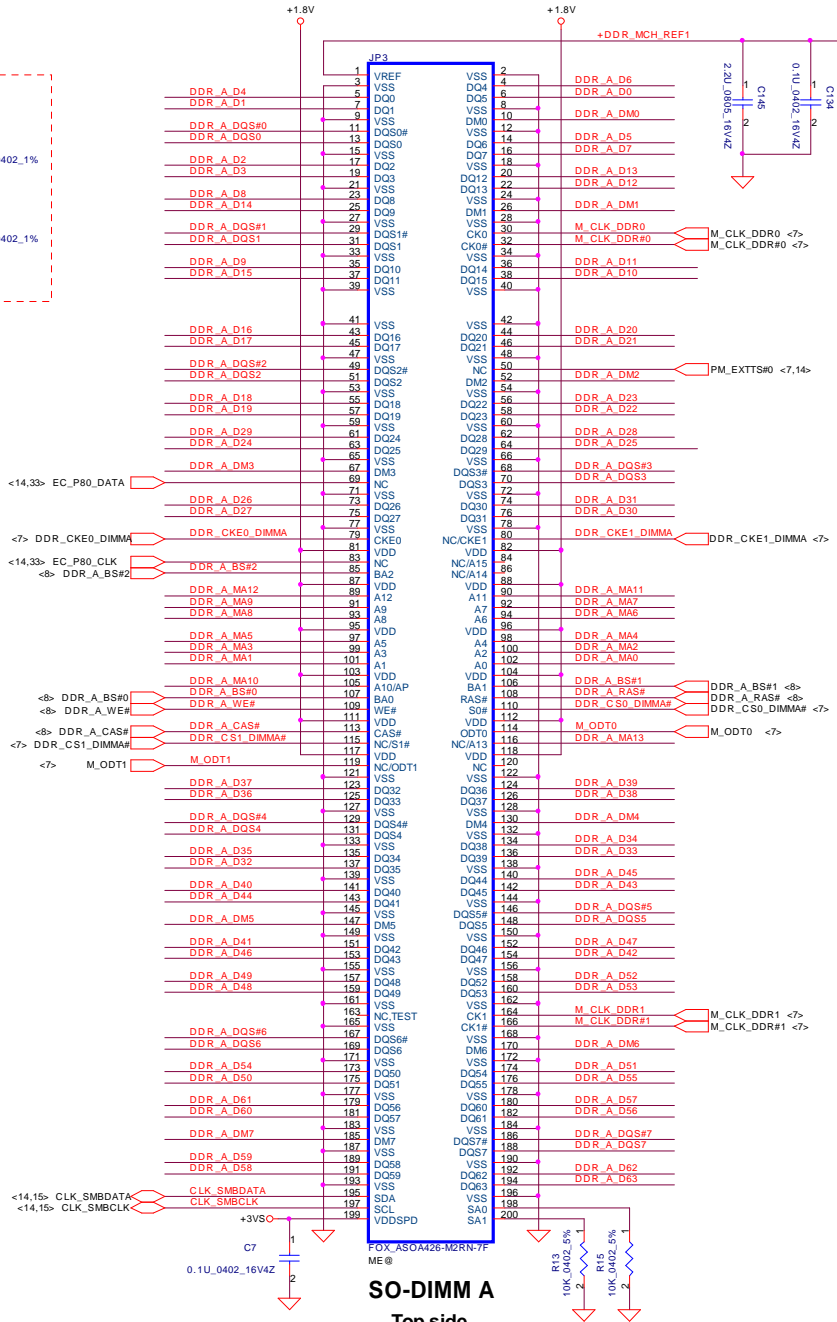
**Layout Note:**  
Place near JP41



**Layout Note:**  
Place one cap close to every 2 pullup  
resistors terminated to +0.9VS



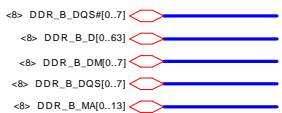
**Layout Note:**  
Place these resistor  
closely JP41,all  
trace length Max=1.5"



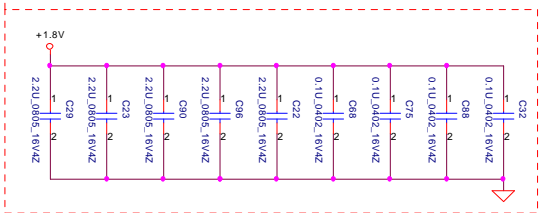
**SO-DIMM A**  
Top side

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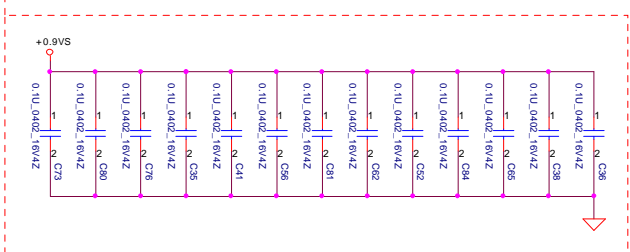
Compal Electronics, Inc.		
<b>DDR II - SODIMM SLOT I</b>		
Title	Document Number	Rev
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2006.02.23	13	47



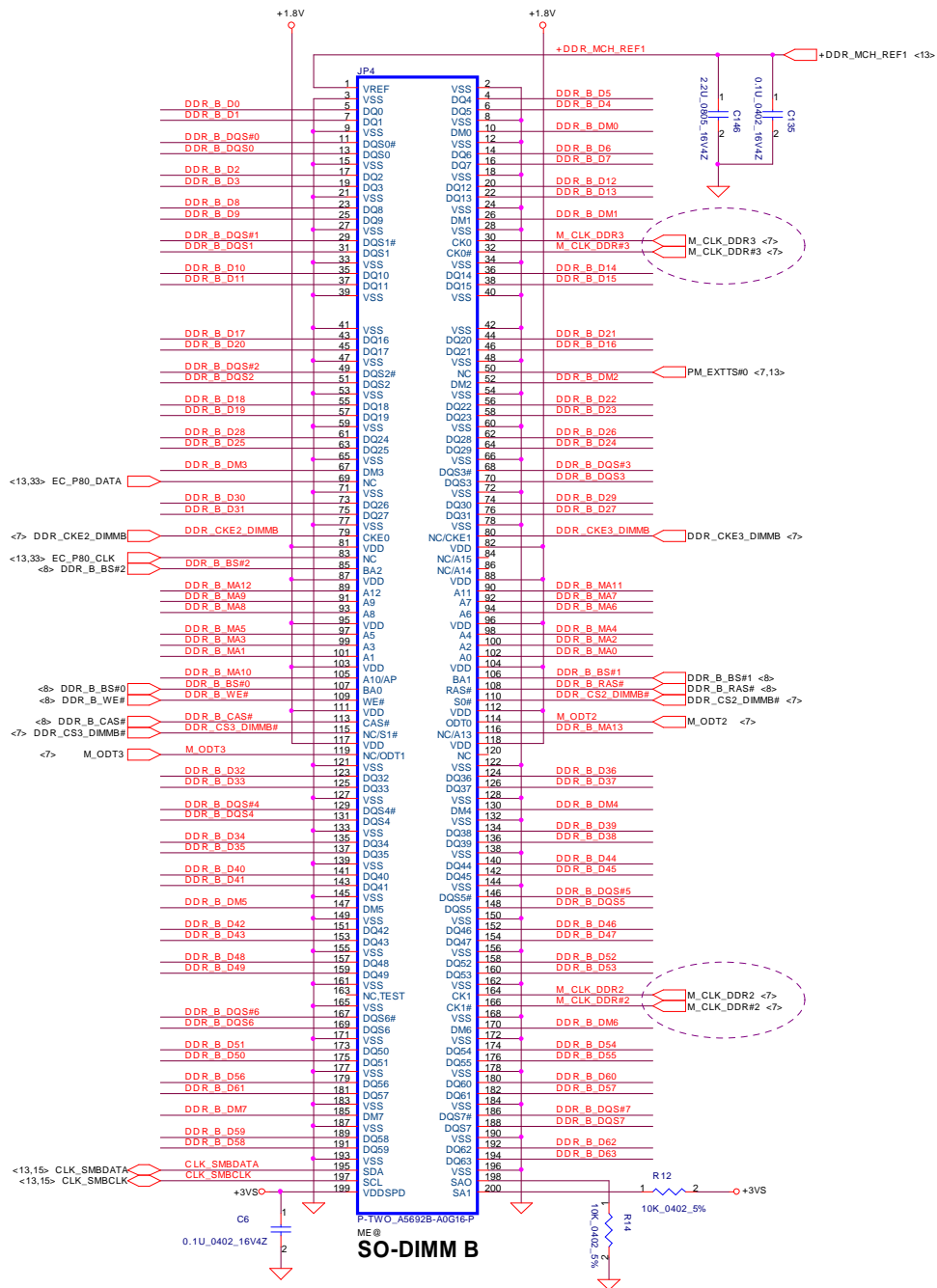
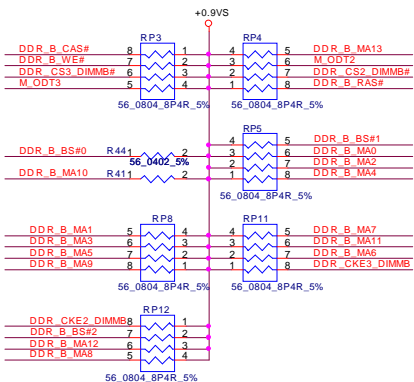
**Layout Note:**  
Place near JP4



**Layout Note:**  
Place one cap close to every 2 pullup resistors terminated to +0.9VS



**Layout Note:**  
Place these resistor closely JP4, all trace length Max=1.5"

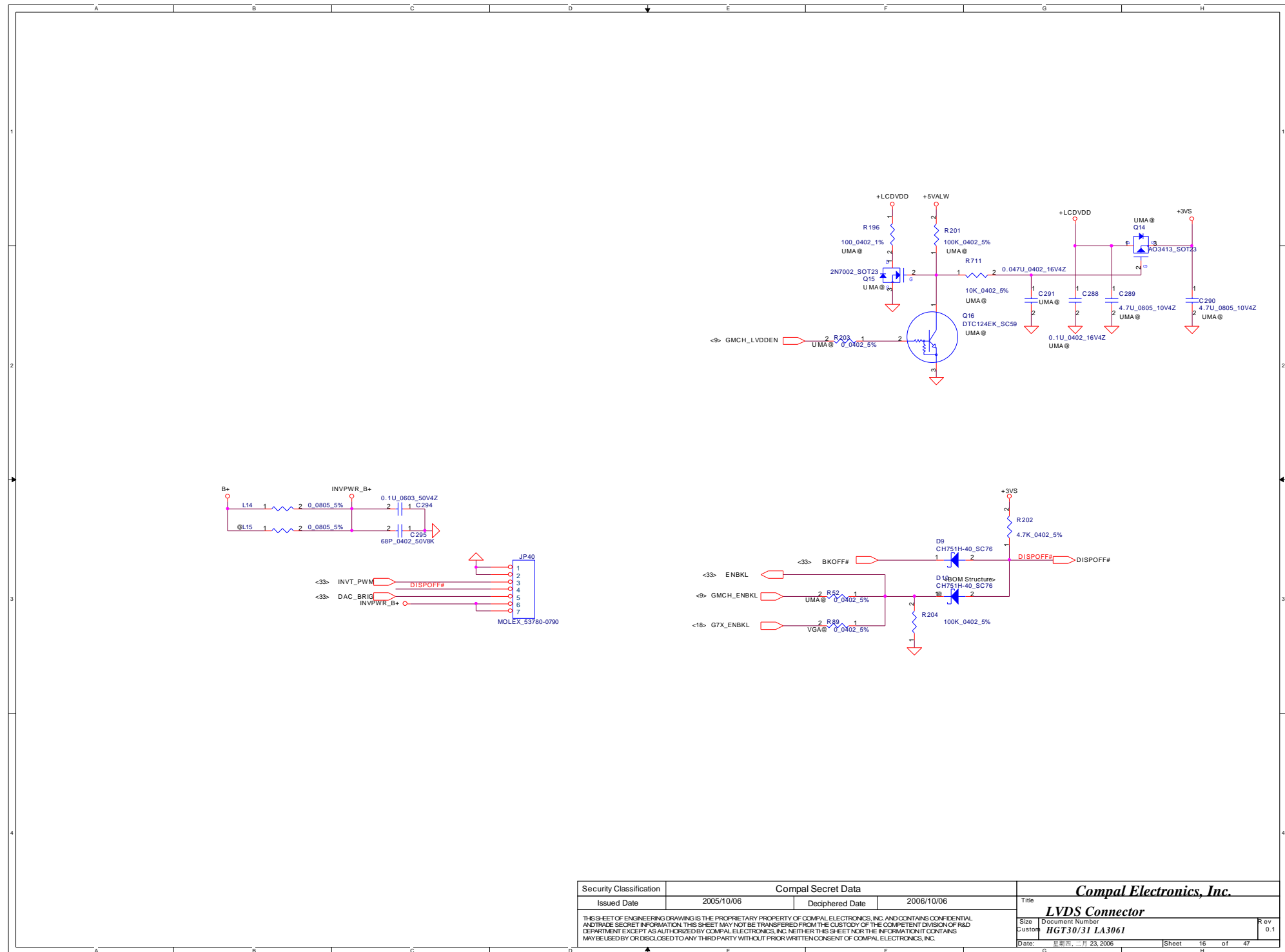


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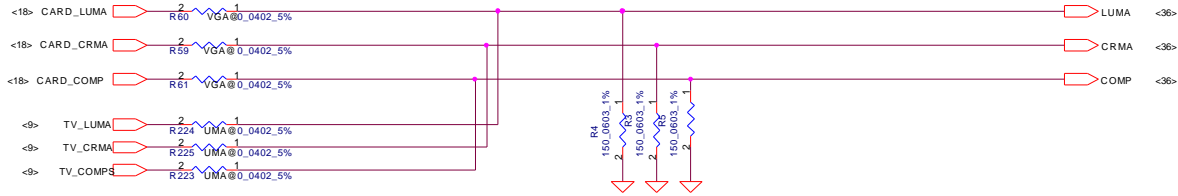




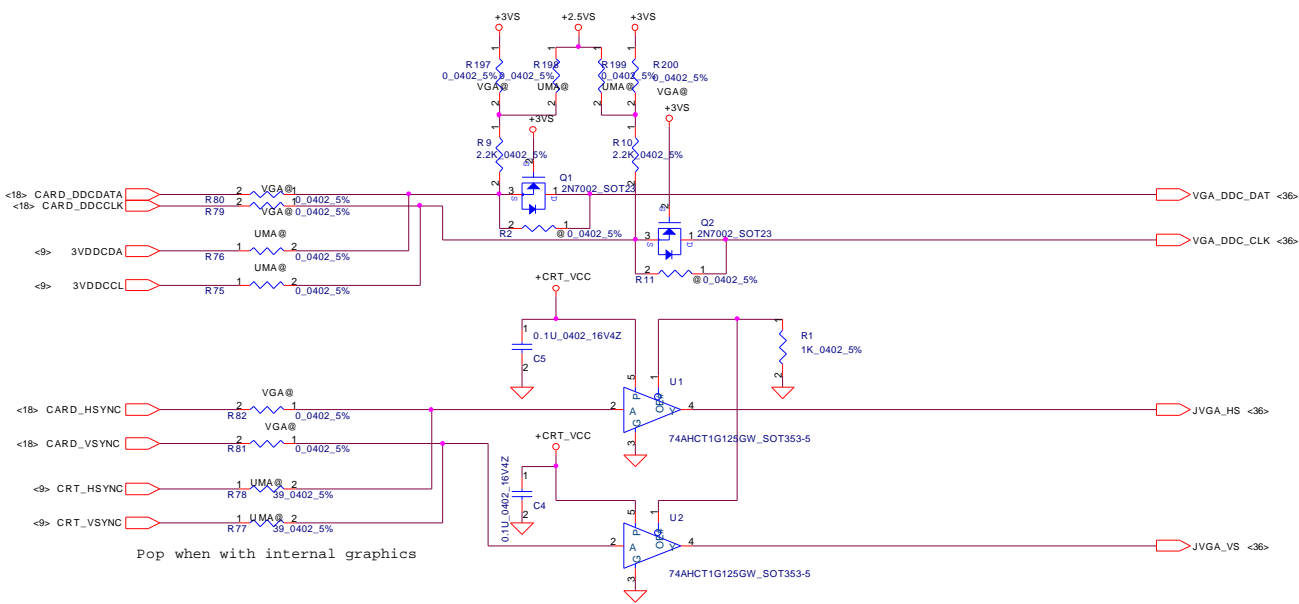
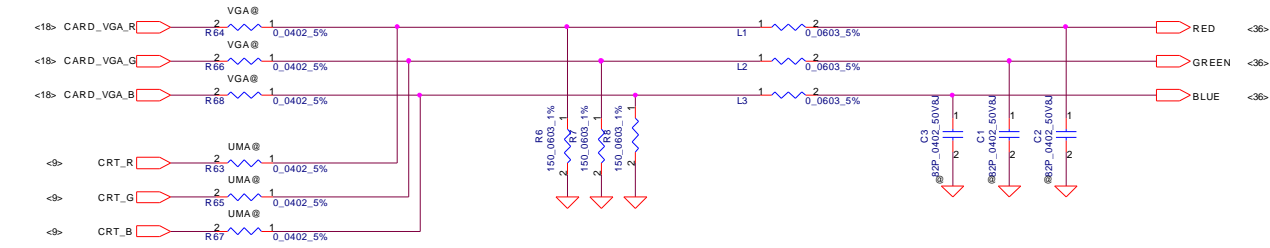
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<b>LVDS Connector</b>		
Size	Document Number	
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**TV-OUT Conn.**



**CRT Conn.**

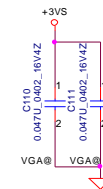
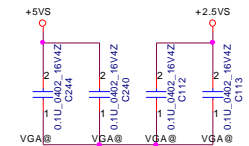
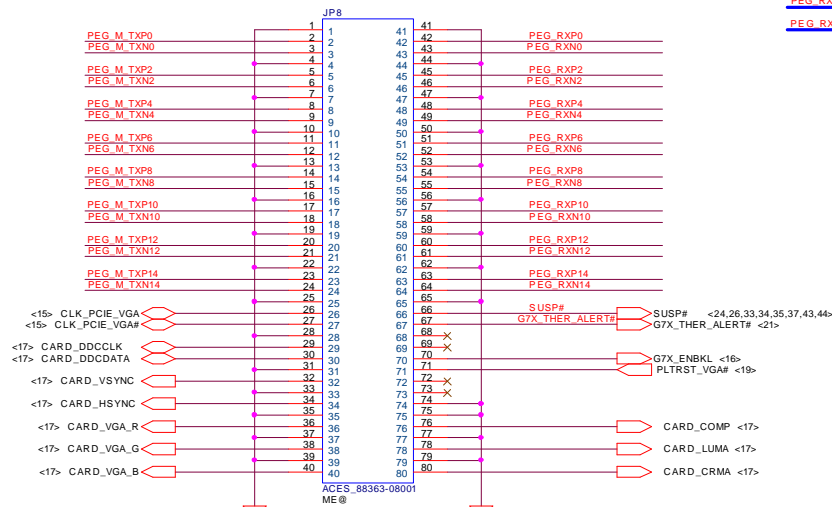
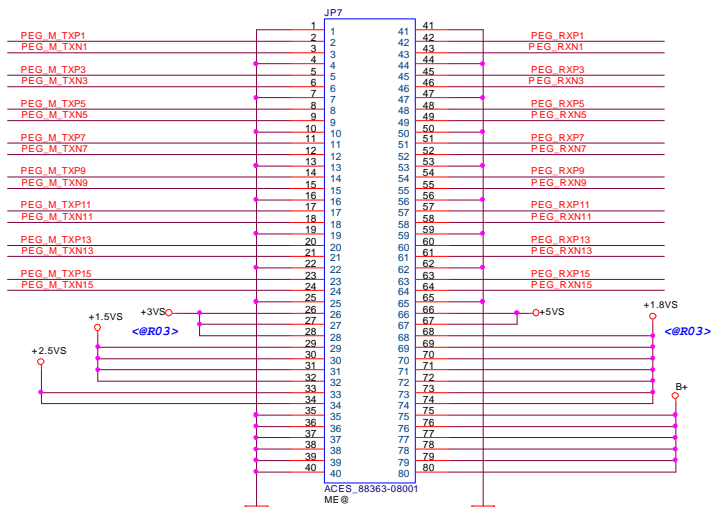


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<b>Compal Electronics, Inc.</b>		
<b>CRT &amp; TVout</b>		
Size	Document Number	Rev
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MAX. 4.06A @ 1.8V  
 MAX. 130mA @ 2.5V  
 MAX. 655mA @ 3.3V

PEG\_M\_TXP[0..15] PEG\_M\_TXP[0..15] <@>  
 PEG\_M\_TXN[0..15] PEG\_M\_TXN[0..15] <@>  
 PEG\_RXP[0..15] PEG\_RXP[0..15] <@>  
 PEG\_RXN[0..15] PEG\_RXN[0..15] <@>



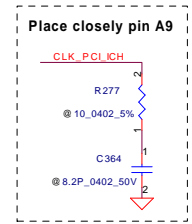
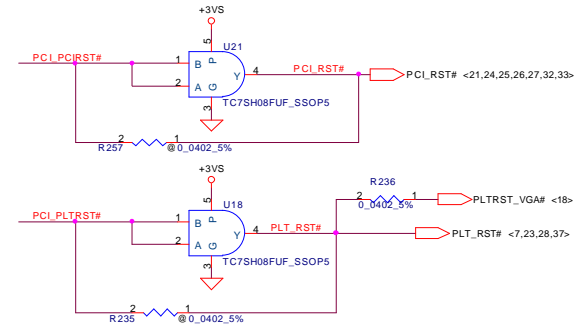
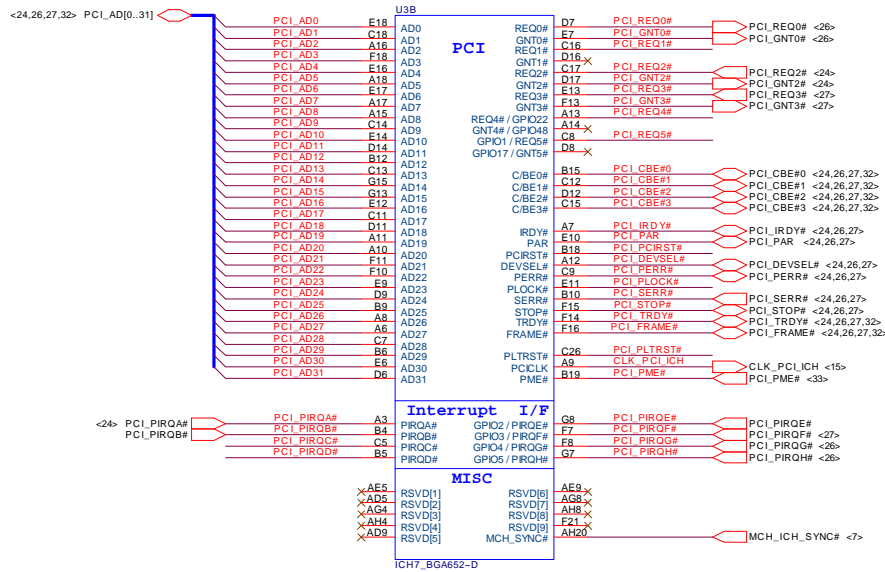
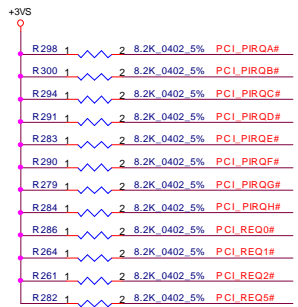
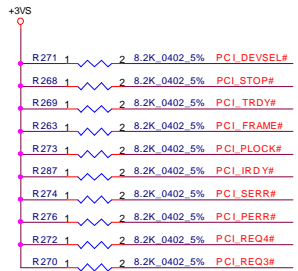
< New Add Pin.28 for +3VS, Pin.68 for +1.8VS @R03 >

Compal Electronics, Inc.

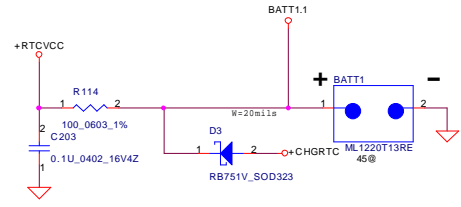
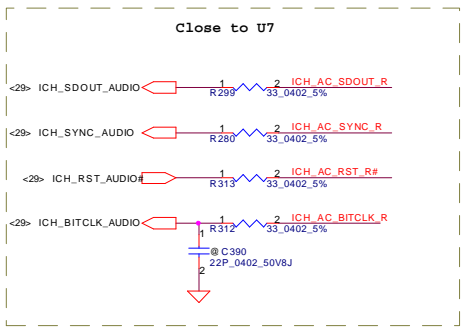
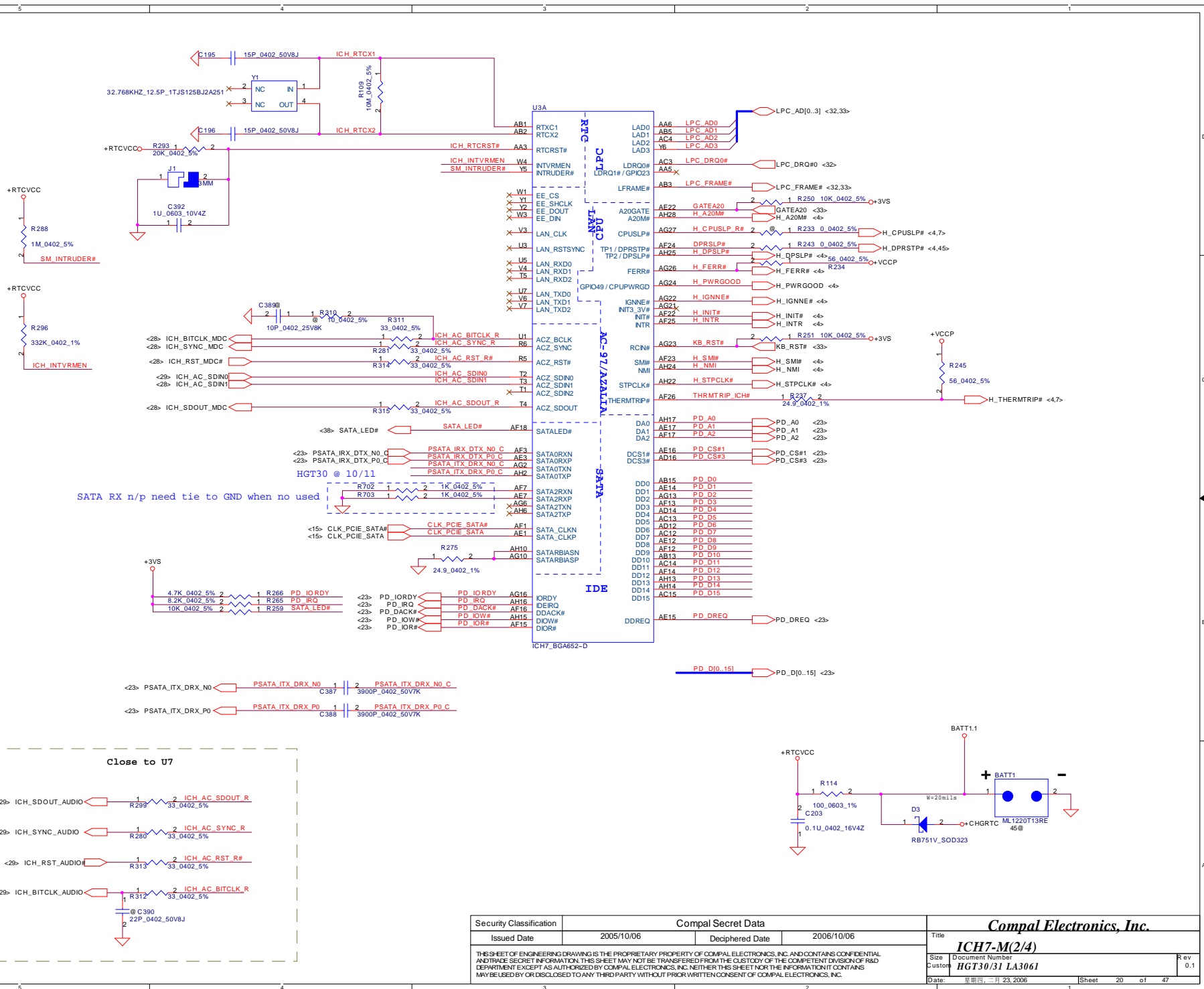
VGA/B connector

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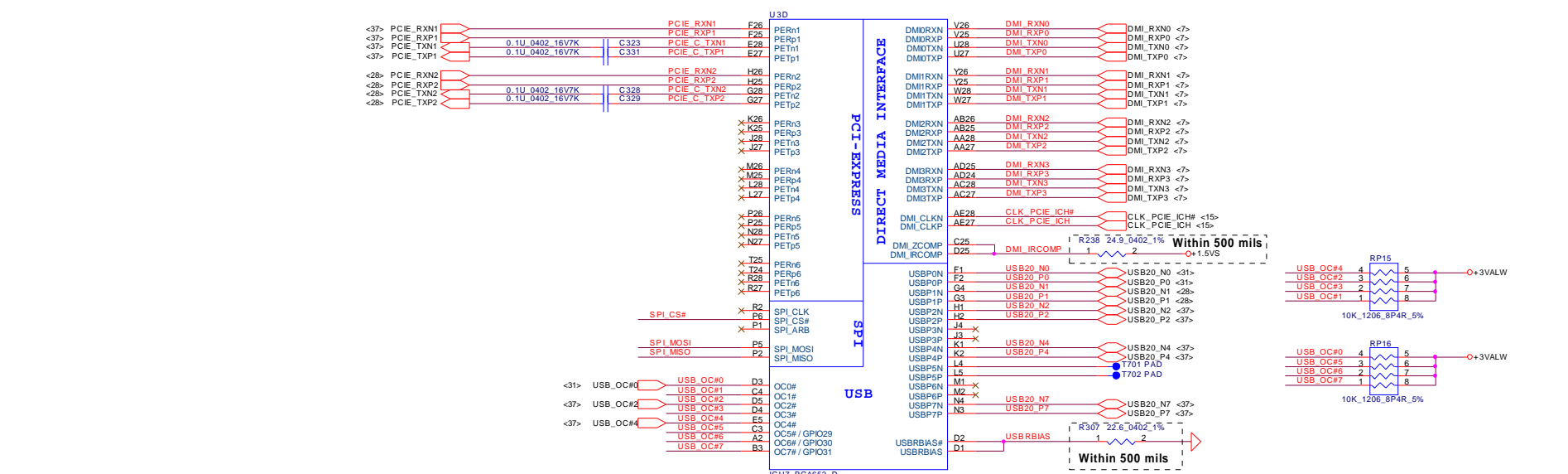
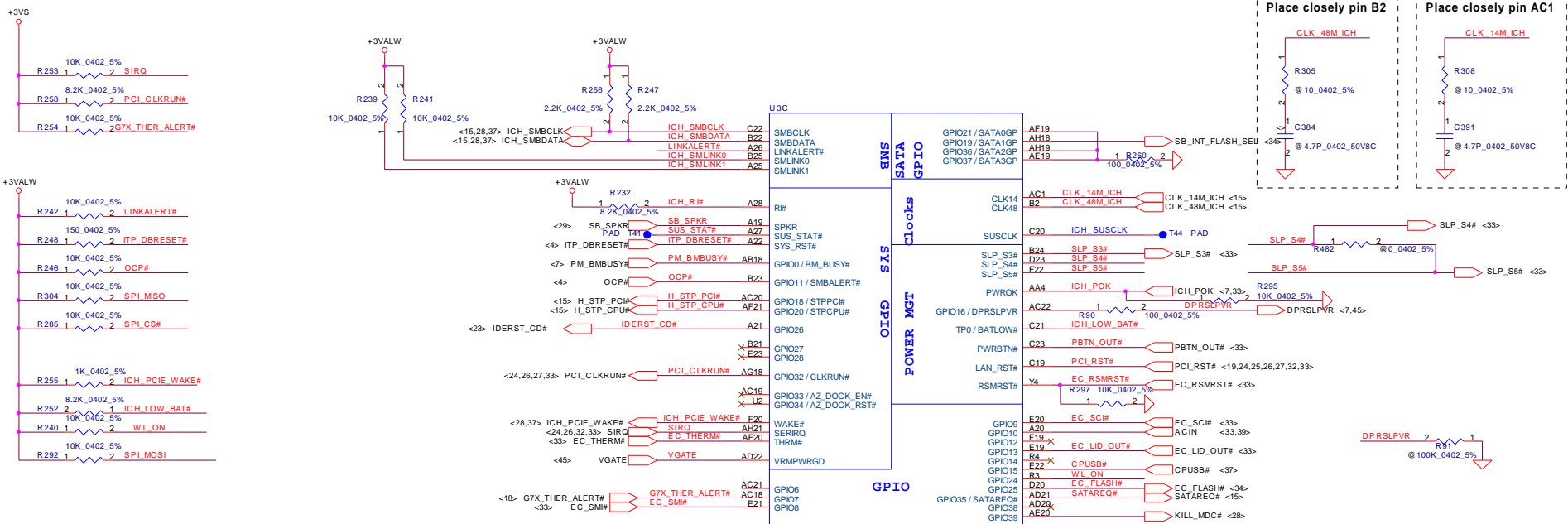
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Custor	HGT30/31 LA3061		
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				Date	Rev
				日期: 二月 23, 2006	0.1
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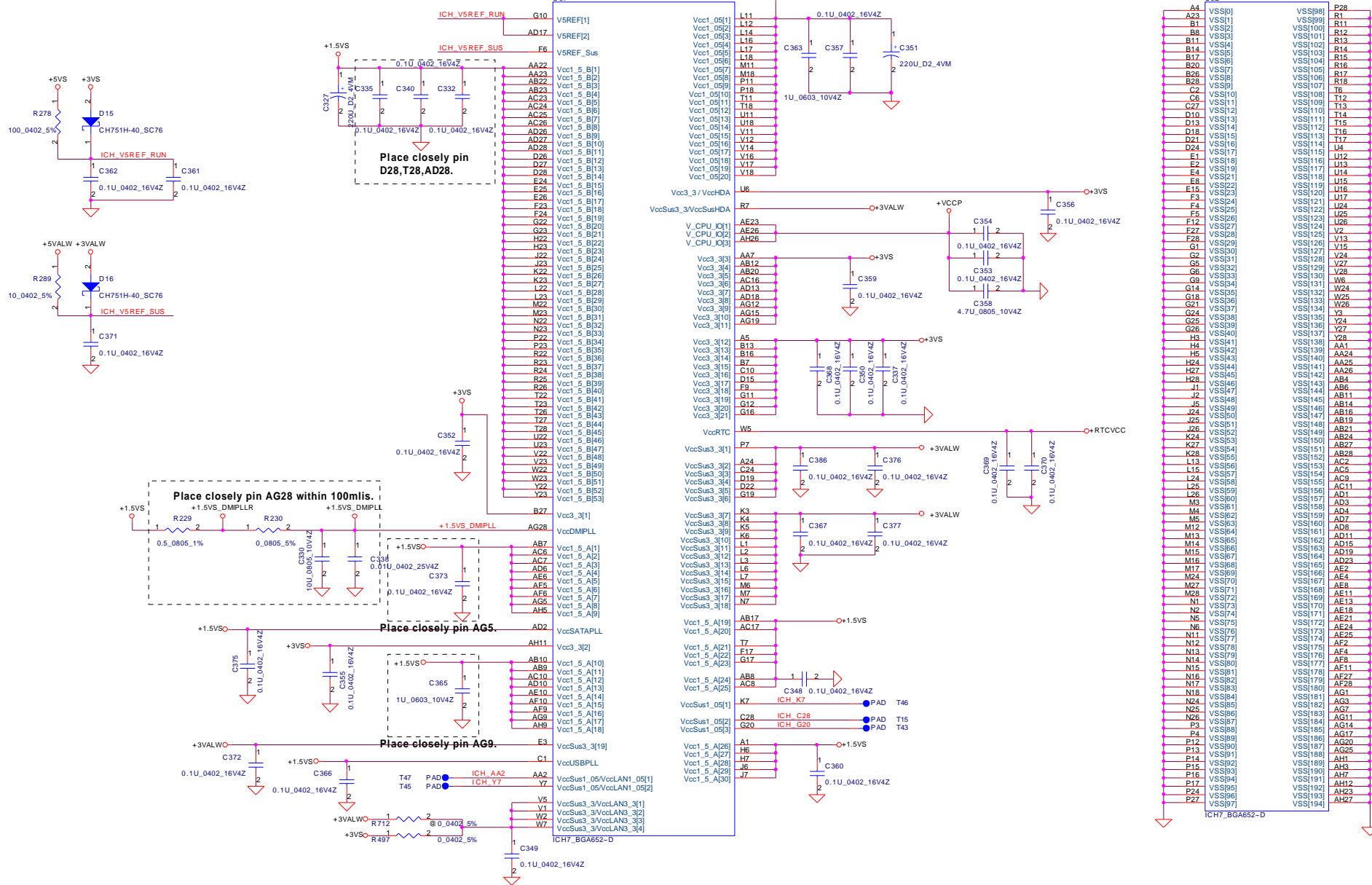


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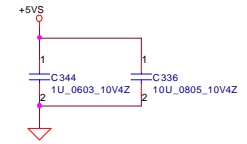
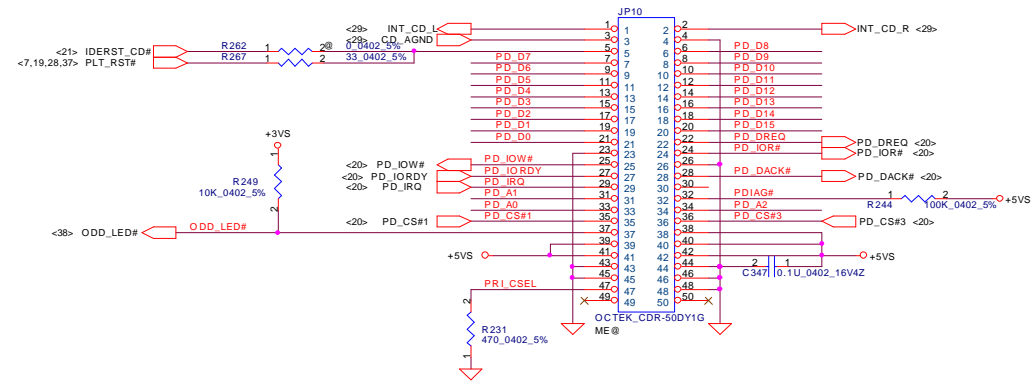
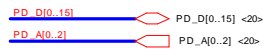
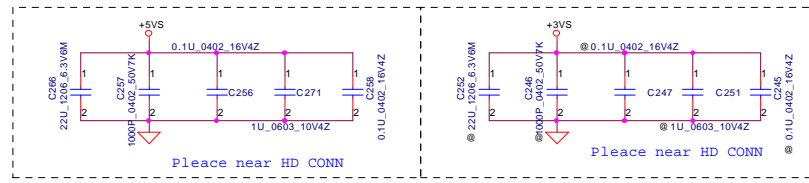
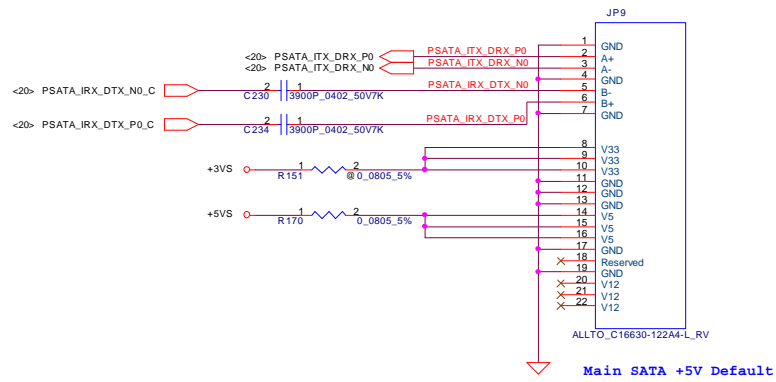
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<b>ICH7-M(3/4)</b>		
Title	Document Number	Rev
	<b>HGT30/31 LA3061</b>	0.1
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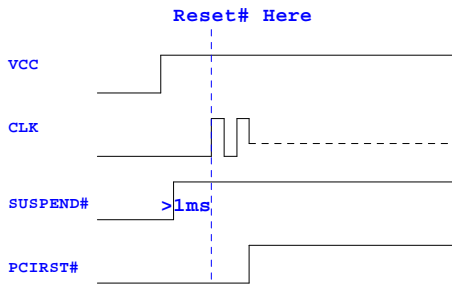
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<b>ICH7-M(4/4)</b>		
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	<b>HGT30/31 LA3061</b>	0.1
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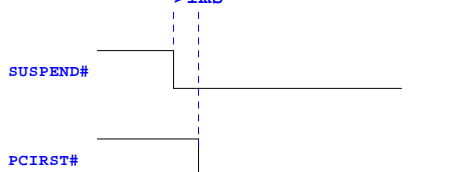


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**Power on RESET#**

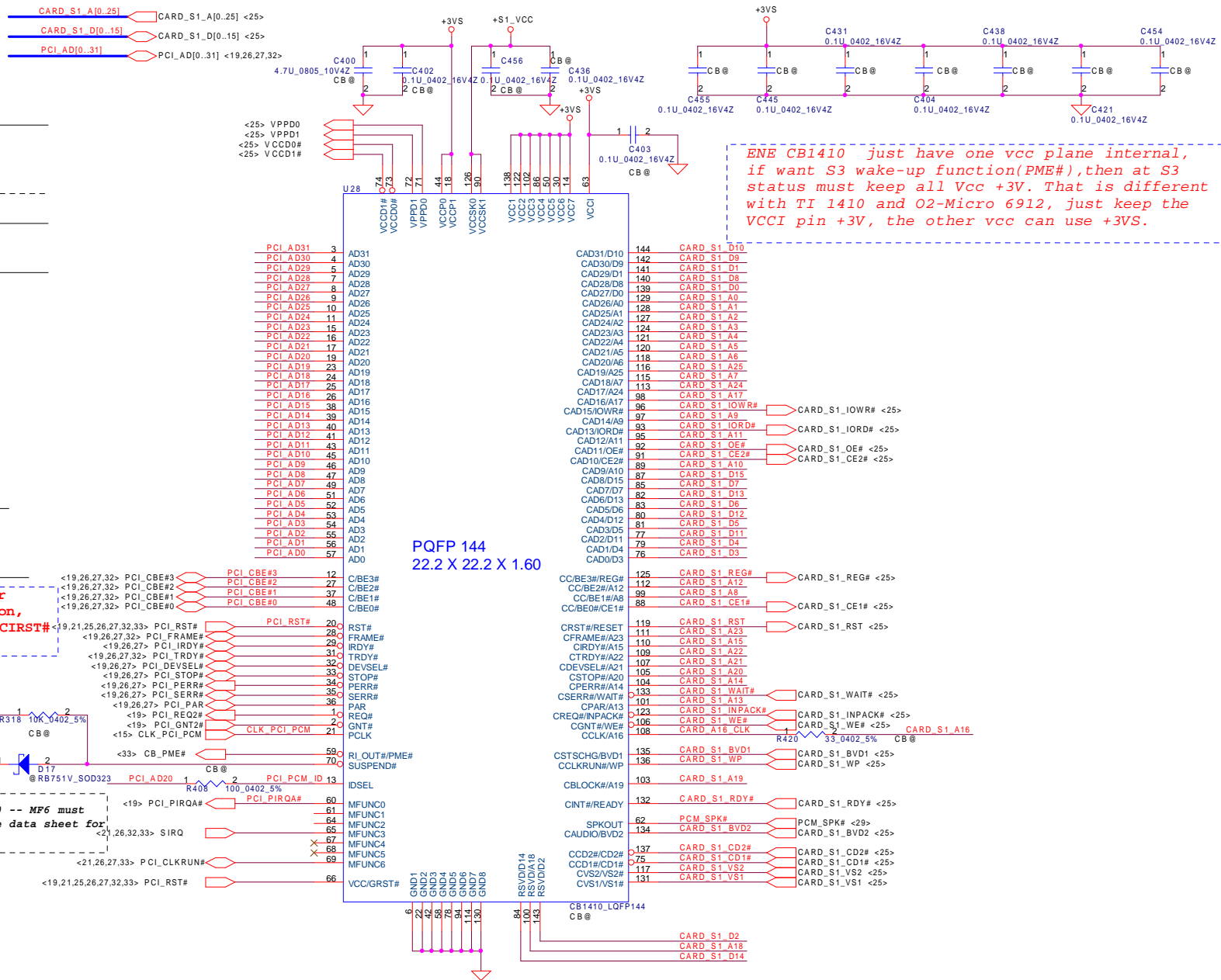


**Entry S3**



SUSPEND# will gate the PCIRST# or GRST#, so need S3 wake-up function, SUSPEND# must be LOW ahead the PCIRST# about 1ms.

Note: MF0 -- MF6 must refer the data sheet for design.



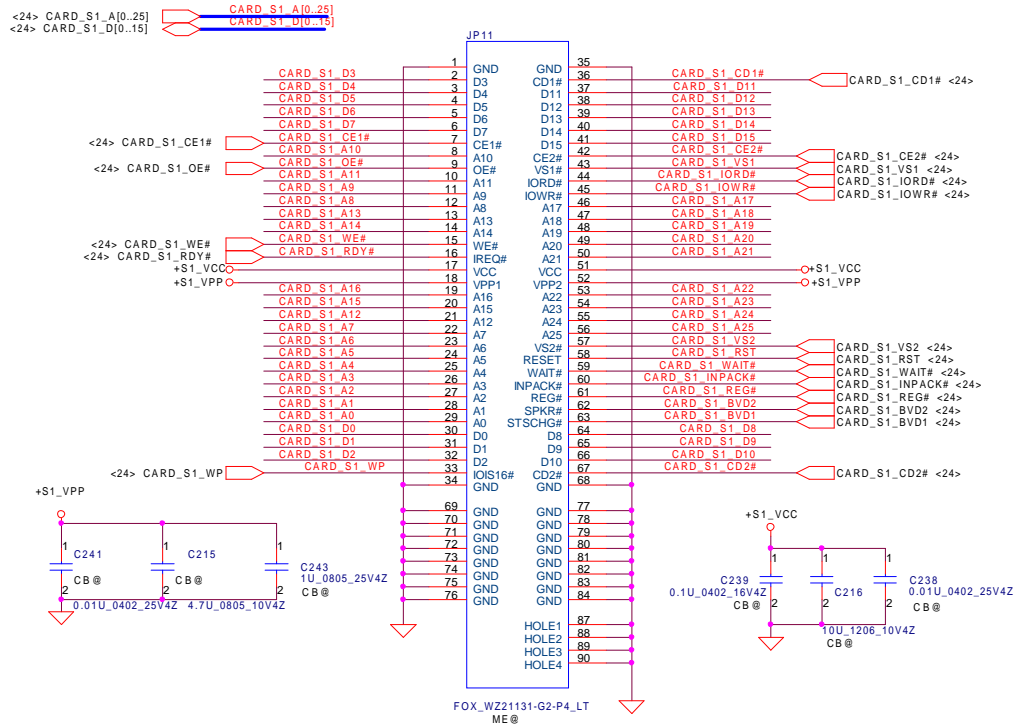
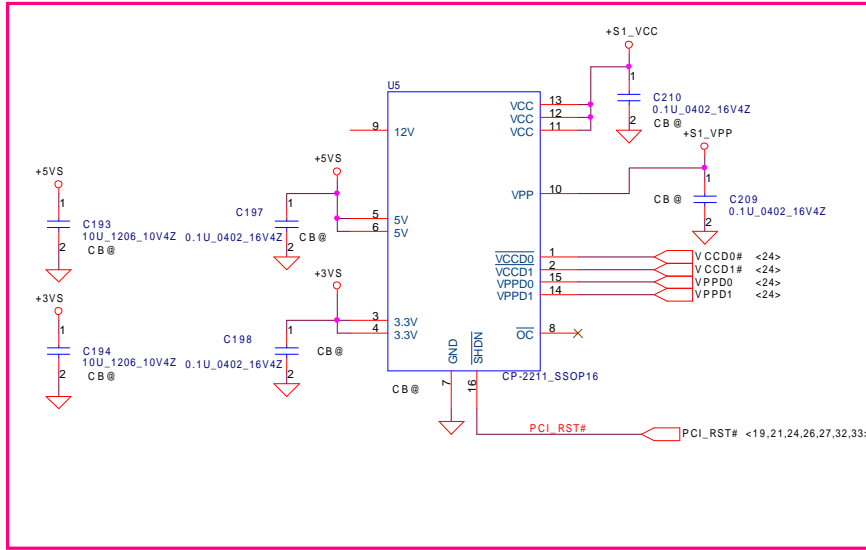
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PCI AD30	4	AD30	CAD30/D9	142	CARD S1 D9
PCI AD29	5	AD29	CAD29/D1	141	CARD S1 D1
PCI AD28	7	AD28	CAD28/D8	140	CARD S1 D8
PCI AD27	8	AD27	CAD27/D0	138	CARD S1 D0
PCI AD26	9	AD26	CAD26/A0	129	CARD S1 A0
PCI AD25	10	AD25	CAD25/A1	128	CARD S1 A1
PCI AD24	11	AD24	CAD24/A2	127	CARD S1 A2
PCI AD23	15	AD23	CAD23/A3	124	CARD S1 A3
PCI AD22	16	AD22	CAD22/A4	121	CARD S1 A4
PCI AD21	17	AD21	CAD21/A5	120	CARD S1 A5
PCI AD20	19	AD20	CAD20/A6	118	CARD S1 A6
PCI AD19	23	AD19	CAD19/A25	116	CARD S1 A25
PCI AD18	24	AD18	CAD18/A7	115	CARD S1 A7
PCI AD17	25	AD17	CAD17/A24	98	CARD S1 A17
PCI AD16	26	AD16	CAD16/A17	96	CARD S1 IOWR#
PCI AD15	38	AD15	CAD15/IOR#	97	CARD S1 IOR#
PCI AD14	39	AD14	CAD14/A9	93	CARD S1 A9
PCI AD13	40	AD13	CAD13/IORD#	95	CARD S1 IORD#
PCI AD12	41	AD12	CAD12/A11	92	CARD S1 A11
PCI AD11	43	AD11	CAD11/OE#	89	CARD S1 OE#
PCI AD10	45	AD10	CAD10/CE2#	91	CARD S1 CE2#
PCI AD9	46	AD9	CAD9/A10	87	CARD S1 A10
PCI AD8	47	AD8	CAD8/D15	85	CARD S1 D15
PCI AD7	49	AD7	CAD7/D7	82	CARD S1 D7
PCI AD6	51	AD6	CAD6/D13	83	CARD S1 D13
PCI AD5	52	AD5	CAD5/D6	80	CARD S1 D6
PCI AD4	53	AD4	CAD4/D12	81	CARD S1 D12
PCI AD3	54	AD3	CAD3/D5	77	CARD S1 D5
PCI AD2	55	AD2	CAD2/D11	79	CARD S1 D11
PCI AD1	56	AD1	CAD1/D4	76	CARD S1 D4
PCI AD0	57	AD0	CAD0/D3		
PCI CBE#3	12	CBE#3	CC/BE3#/REG#	125	CARD S1 REG#
PCI CBE#2	27	CBE#2	CC/BE2#A12	112	CARD S1 A12
PCI CBE#1	37	CBE#1	CC/BE1#A8	99	CARD S1 A8
PCI CBE#0	48	CBE#0	CC/BE0#/CE1#	88	CARD S1 CE1#
PCI RST#	20	RST#	CRST#/RESET	119	CARD S1 RST
PCI FRAME#	28	FRAME#	CFRAME#A23	111	CARD S1 A23
PCI IRDY#	29	IRDY#	CRDY#A15	110	CARD S1 A15
PCI TRDY#	31	TRDY#	CTRDY#A22	109	CARD S1 A22
PCI DEVSEL#	32	DEVSEL#	CDVSEL#A21	107	CARD S1 A21
PCI STOP#	33	STOP#	CSTOP#A20	104	CARD S1 A14
PCI PERR#	34	PERR#	CPERR#A14	102	CARD S1 WAIT#
PCI SERR#	35	SERR#	CSERR#A17	101	CARD S1 A13
PCI PAR#	36	PAR#	CPAR/A13	123	CARD S1 INPACK#
PCI REQ2#	1	REQ#	CREQ#/INPACK#	108	CARD S1 WE#
PCI GNT2#	2	GNT#	CGNT#/WE#	108	CARD S1 WE#
CLK_PCI_PCM	21	CLK_PCI_PCM	CLCLK/A16	108	CARD S1 A16
CB_PME#	59	RL_OUT#/PME#	CSTSCHG/BVD1	135	CARD S1 BVD1
PCI AD20	1	SUSPEND#	CCLKRUN#/WP	136	CARD S1 WP
PCI PIRQA#	60	IDSEL	CBLOCK#/A19	103	CARD S1 A19
PCI PIRQB#	61	MFUNC0	CINT#/READY	132	CARD S1 RDY#
PCI PIRQC#	62	MFUNC1			
PCI PIRQD#	63	MFUNC2			
PCI PIRQE#	64	MFUNC3	SPKOUT	62	PCM_SPK#
PCI PIRQF#	65	MFUNC4	AUDIO/BVD2	134	CARD S1 BVD2
PCI PIRQG#	66	MFUNC5			
PCI PIRQH#	67	MFUNC6			
PCI CLKRUN#	68		CCD2#/CD2#	137	CARD S1 CD2#
PCI CLKRUN#	69		CCD1#/CD1#	147	CARD S1 CD1#
PCI RST#	66		CVS2/VS2#	147	CARD S1 VS2
			CVS1/VS1#	131	CARD S1 VS1

PQFP 144  
22.2 X 22.2 X 1.60

ENE CB1410 just have one vcc plane internal, if want S3 wake-up function(PME#), then at S3 status must keep all Vcc +3V. That is different with TI 1410 and O2-Micro 6912, just keep the VCCI pin +3V, the other vcc can use +3VS.

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PROPRIETARY NOTE		Document Number		Size	
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		Date: 日期: 07/23/2006		Sheet 24 of 47	

PCMCIA Power Controller

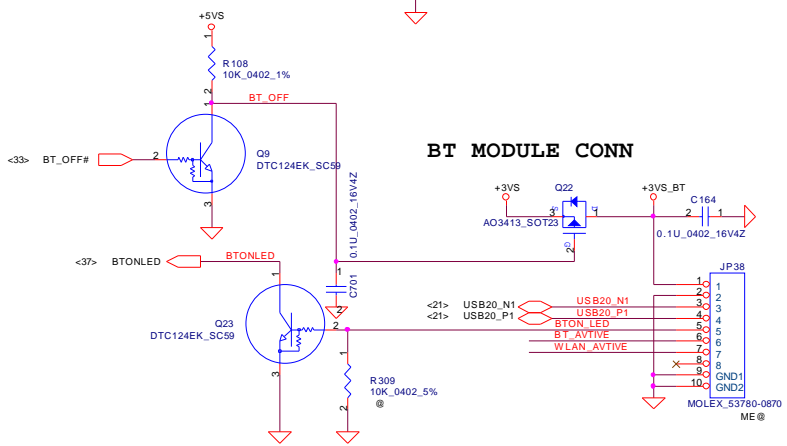
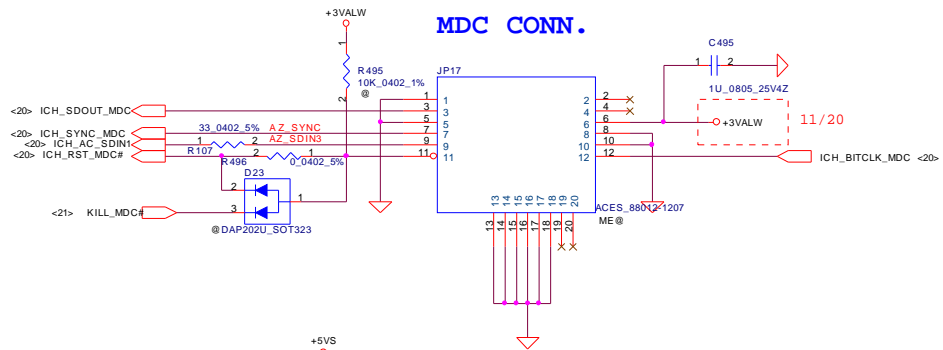
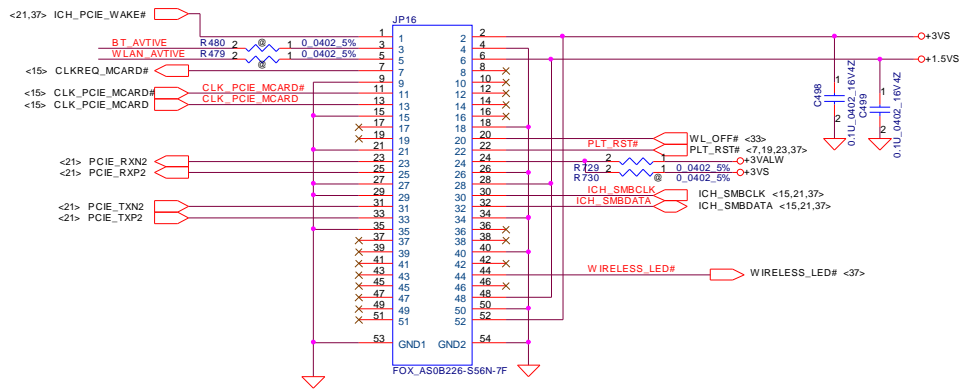


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Issued Date	2005/10/06	Deciphered Date	2006/10/06	Title CardBus Socket	
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				Customer	HGT30/31 LA3061
Date:	日期: 07/23/2006	Sheet	25 of 47		





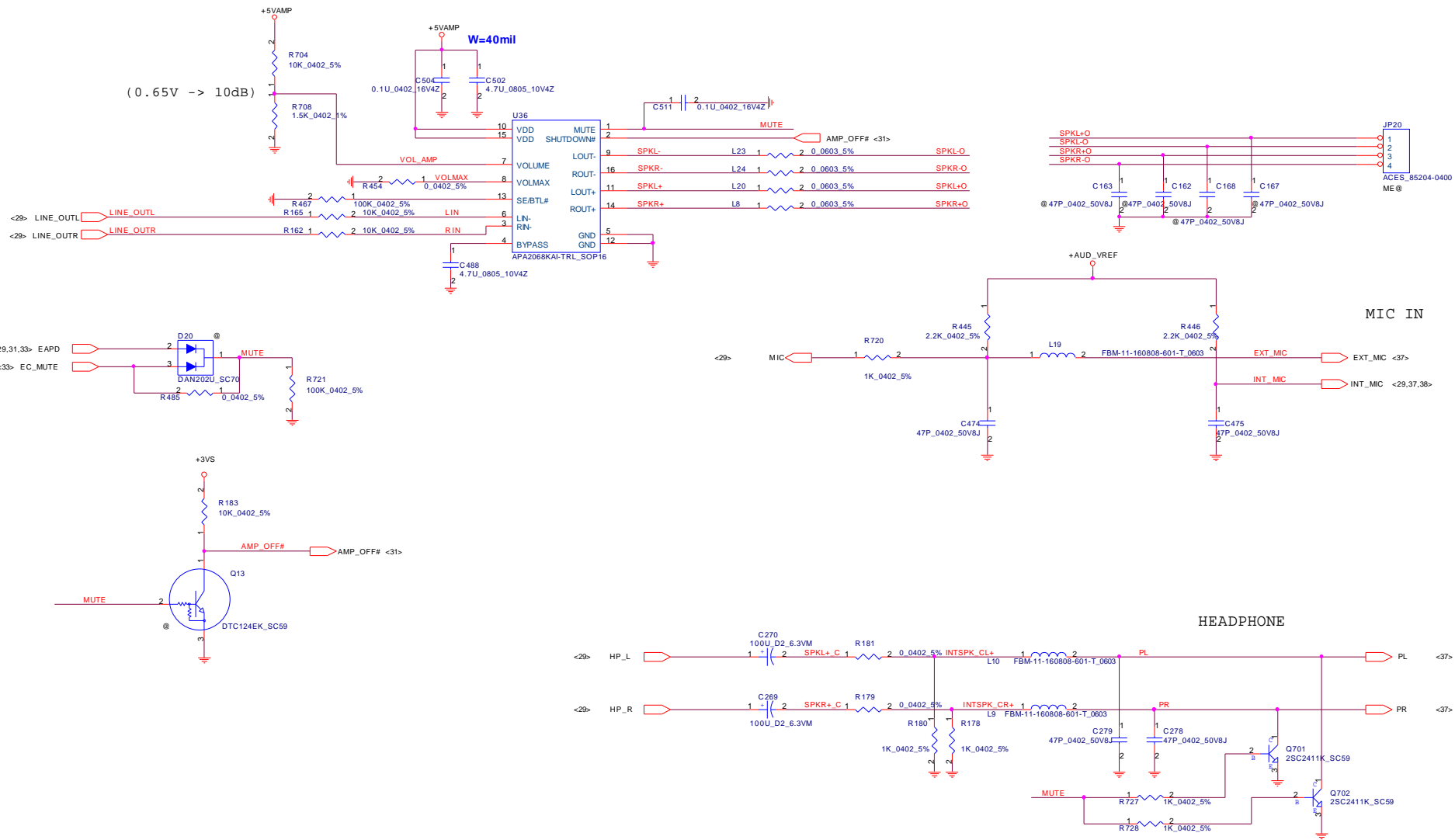
# Mini-Express Card(Slot 1-WLAN)



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Issued Date	2005/10/06	Deciphered Date	2006/10/06	Title
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Size	Document Number		Rev	
Custom	HGT30/31 LA3061		0.1	
Date:	日期: 二月 23, 2006	Sheet	28	of 47





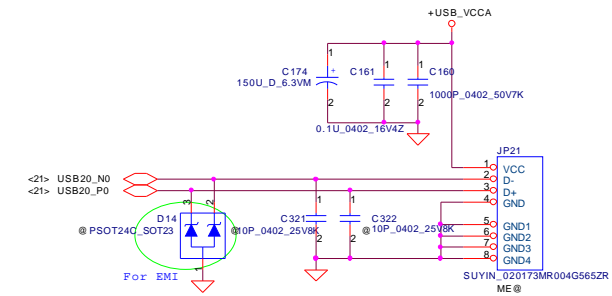
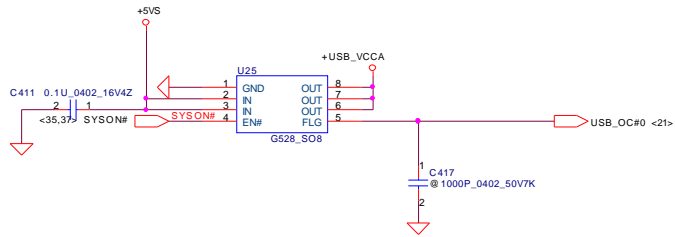
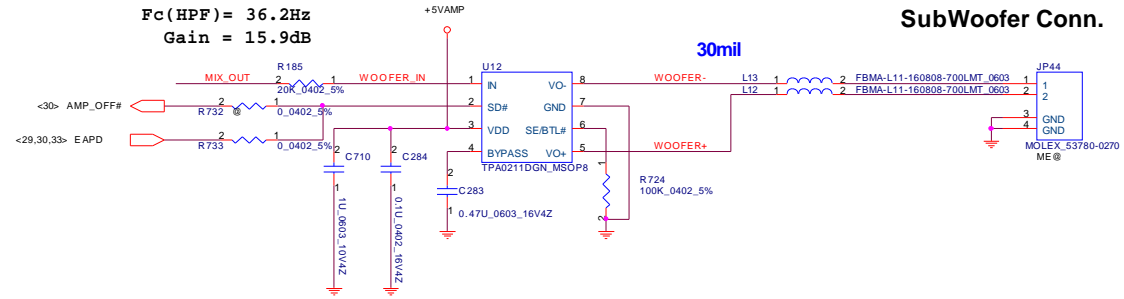
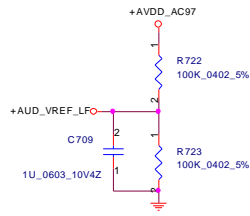
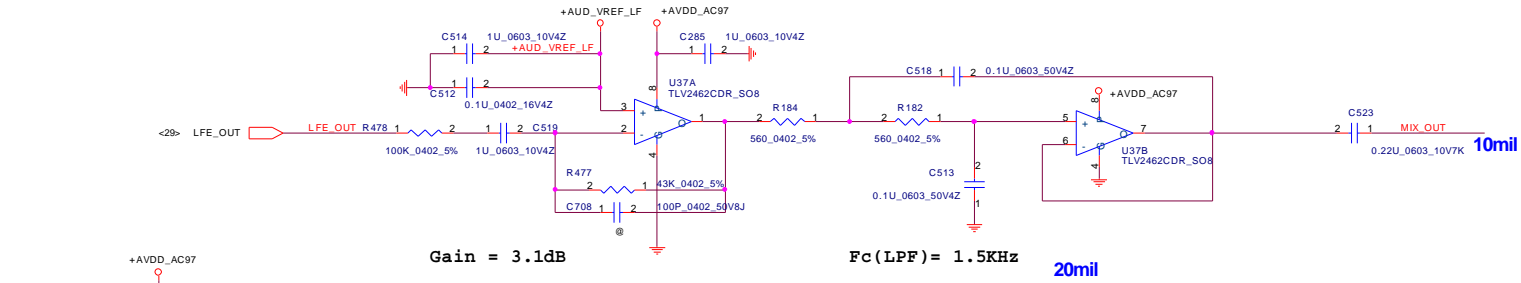


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Issued Date	2005/10/06	Deciphered Date
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<b>Compal Electronics, Inc.</b>	
<b>AMP &amp; Audio Jack</b>	
Size	Document Number
Customer	HGT30/31 LA3061
Date:	日期: 二月 23, 2006
Sheet	30 of 47
Rev	0.1

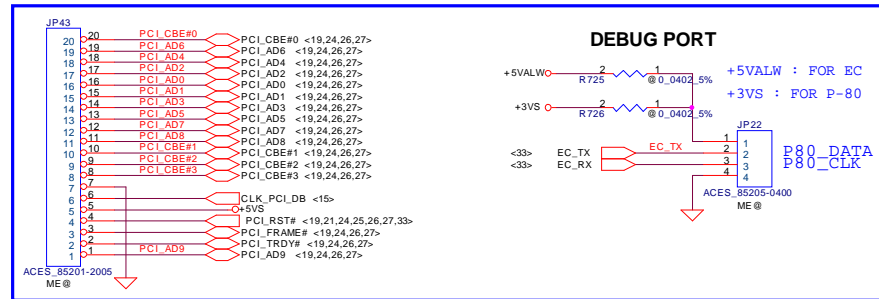
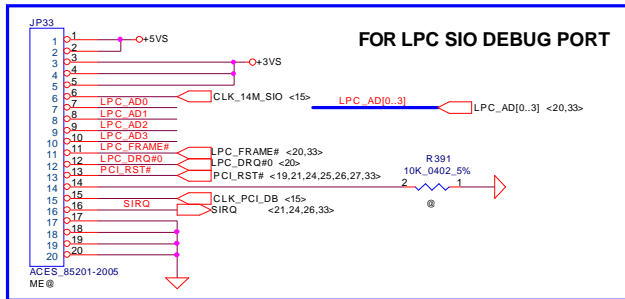
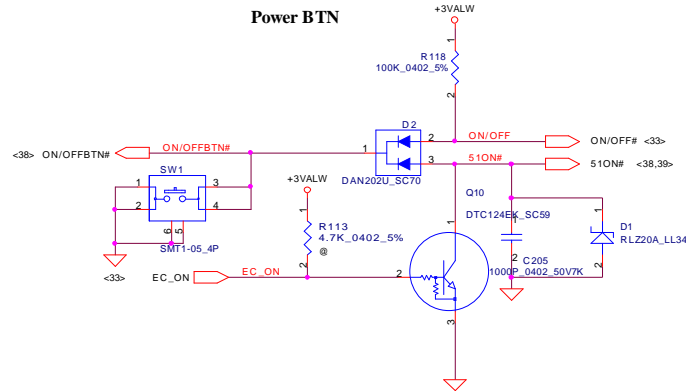
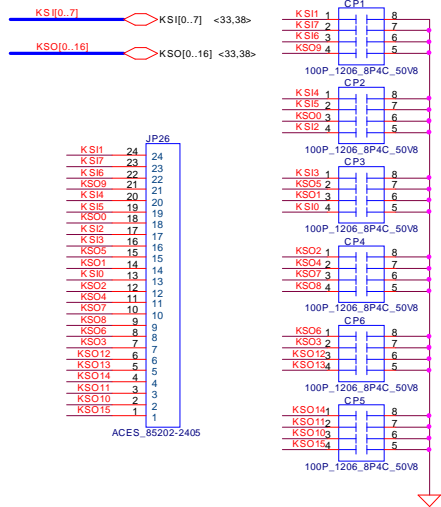
# SUBWOOFER (Reserved for C38)

WOOFER@



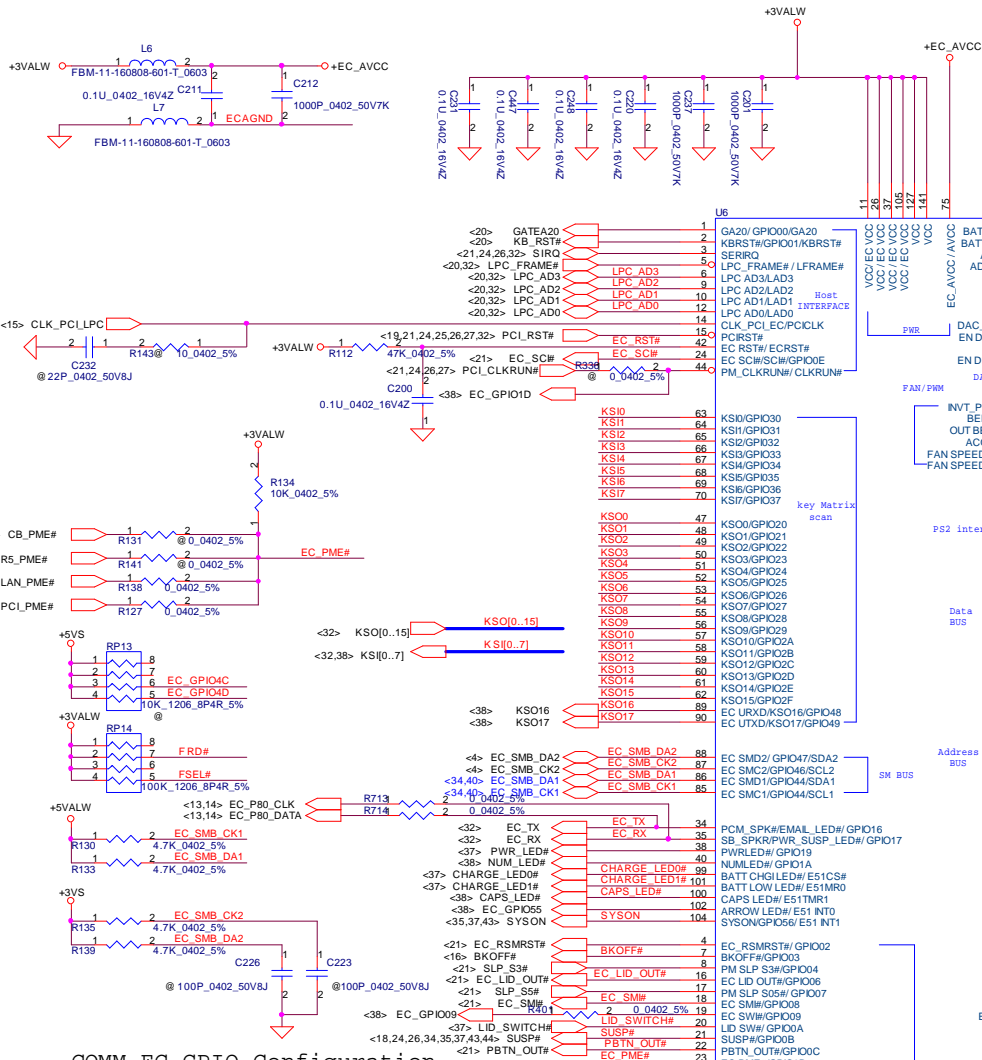
Security Classification	Compal Secret Data		Title	
Issued Date	2005/10/06	Deciphered Date	2006/10/06	Bluetooth & USB CONN.
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				Document Number HGT30/31 LA3061
				Rev 0.1
				Date: 星期二, 二月 23, 2006
				Sheet 31 of 47

### INT\_KBD CONN.( TYPE "D" KB)



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		2006/10/06
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<b>Compal Electronics, Inc.</b>	
<b>KBD_ON/OFF,T/P,LED/B,DEBUG</b>	
Size	Document Number
Customer	HGT30/31 LA3061
Date:	Rev
日期: 06/23/2006	0.1
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Analog Board ID definition, Please see page 3.

ID	BRD ID	R115 (Rb)	Vab
0	R01 (EVT)	0	0V
1	R02 (DVT)	8.2K	0.25V
2	R03 (PVT)	18K	0.50V
3	R04	33K	0.82V
4		56K	1.19V
5		100K	1.65V
6		200K	2.20V
7		NC	3.30V

R119 (Ra) = 100K Ohm  
MB\_ID

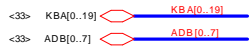
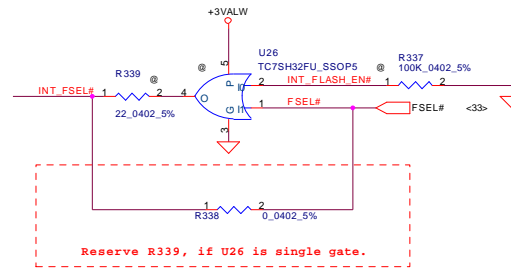
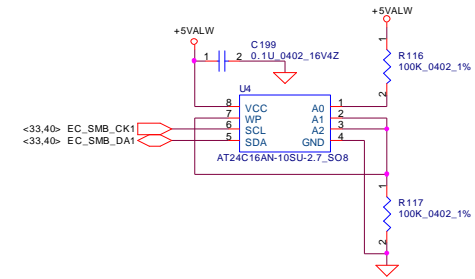
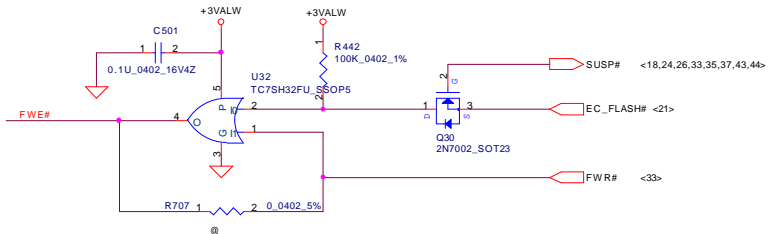
ID	MB	R125 (Ra)	R126 (Rb)
0	HGT30 (VGA)	NC	0 Ohm
1	HGT31 (UMA)	100K Ohm	NC

COMM EC\_GPIO Configuration

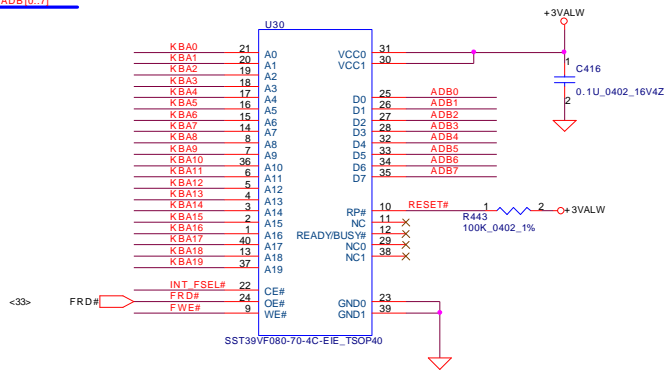
PIN	GPIO	HDL00/HDL10	HGT30/HGT31
80	EC_GPIO3F	NC	TP_ACT_LED#
19	EC_GPIO09	EASY_KEY1#	LED6#
35	EC_GPIO17	SUSP_LED#	EC_P80_DATA
44	EC_GPIO1D	NC	LED3#
91	EC_GPIO4A	NC	LED4#
92	EC_GPIO4B	NC	NC
93	EC_GPIO4C	NC	LED1#
94	EC_GPIO4D	NC	LED2#
102	EC_GPIO55	NC	LED5#
97	EC_GPIO50	MEDIA#	BT_OFF#
137	EC_GPIO57	VOL_UP#	NOVO_BTN#
142	EC_GPIO58	VOL_DOWN#	SLP_S4#
143	EC_GPIO59	KILL_SW#	WIRE_LAN_BTN#
30	EC_GPIO12	AMP_MUTE	TP_LOCK_LED#

Security Classification		Compal Secret Data	
Issued Date	2005/10/06	Deciphered Date	2006/10/06

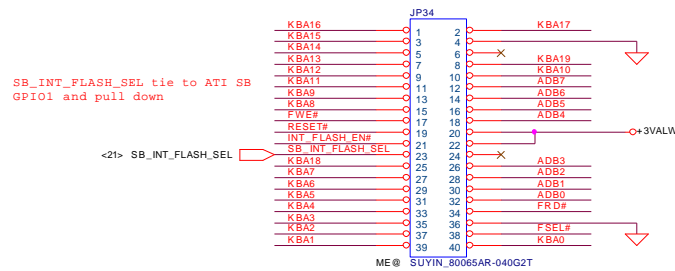
Compal Electronics, Inc.	
Title	ENE-KB910L
Size	Document Number
Customer	HGT30/31 LA3061
Date	Rev 0.1



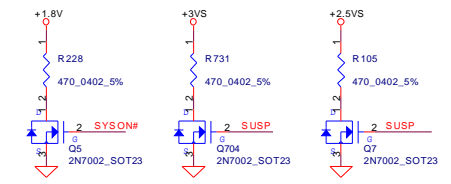
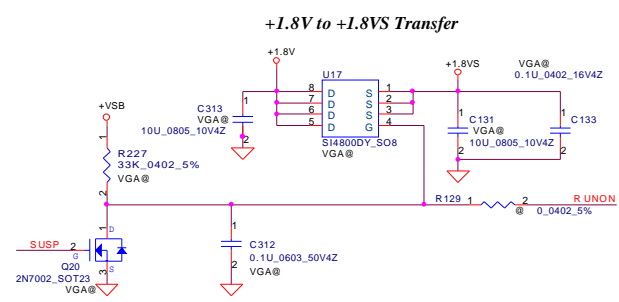
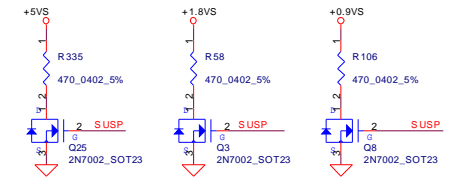
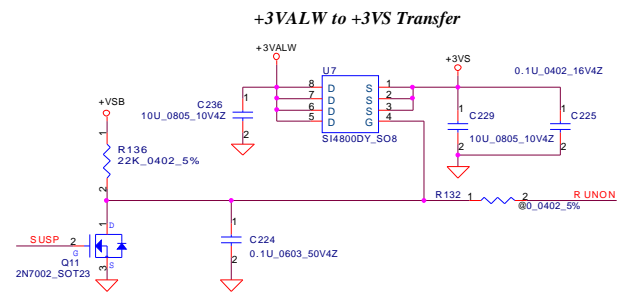
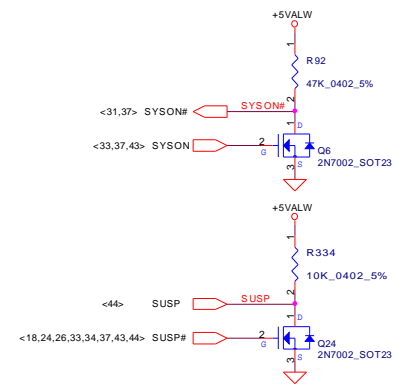
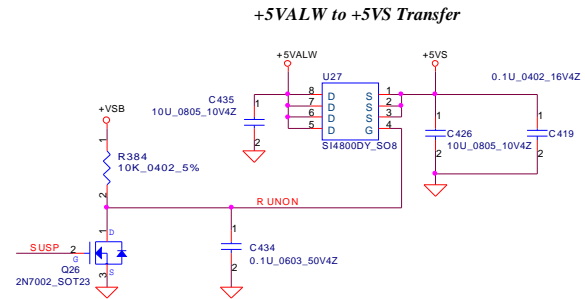
### 1MB Flash ROM



### 1MB ROM Socket



Security Classification	Compal Secret Data		Title <b>Compal Electronics, Inc.</b> <b>BIOS &amp; EC I/O Port</b>
Issued Date	2005/10/06	Deciphered Date	
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			Document Number <b>HGT30/31 LA3061</b> Rev 0.1
			Date: 星期日, 二月 23, 2006   Sheet 34 of 47

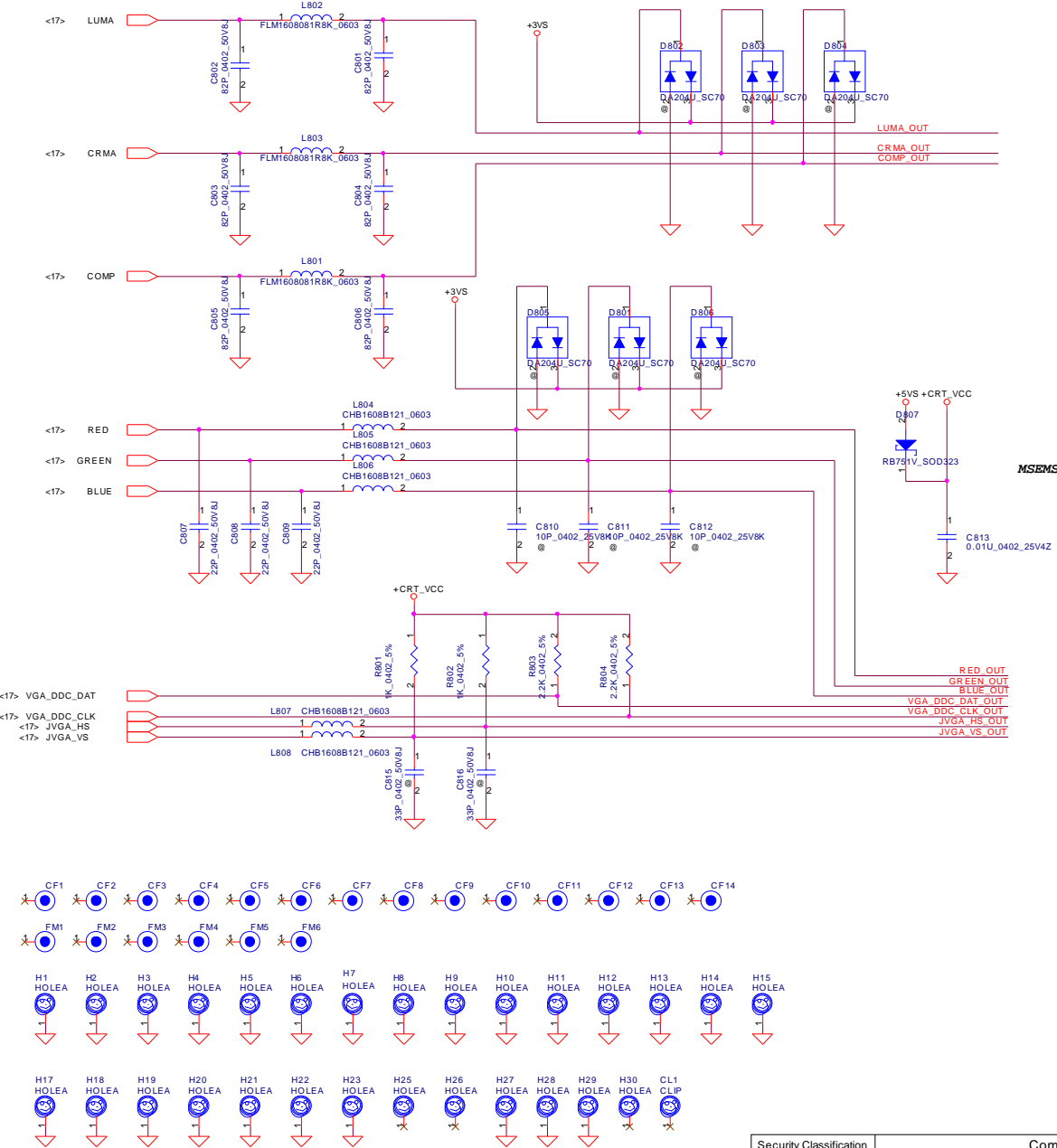


Security Classification	Compal Secret Data	
Issued Date	2005/10/06	Deciphered Date
		2006/10/06
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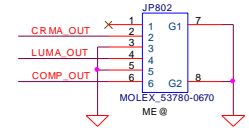
<b>Compal Electronics, Inc.</b>	
<b>DC/DC Circuit</b>	
Size	Document Number
Custody	HGT30/31 LA3061
Date:	星期四, 三月 23, 2006
Sheet	35 of 47

# VGA I/O PORT Connector

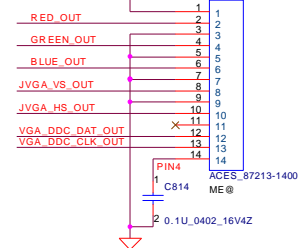
CLOSE TO JTVOUT1



## S-VIDEO



## DSUB



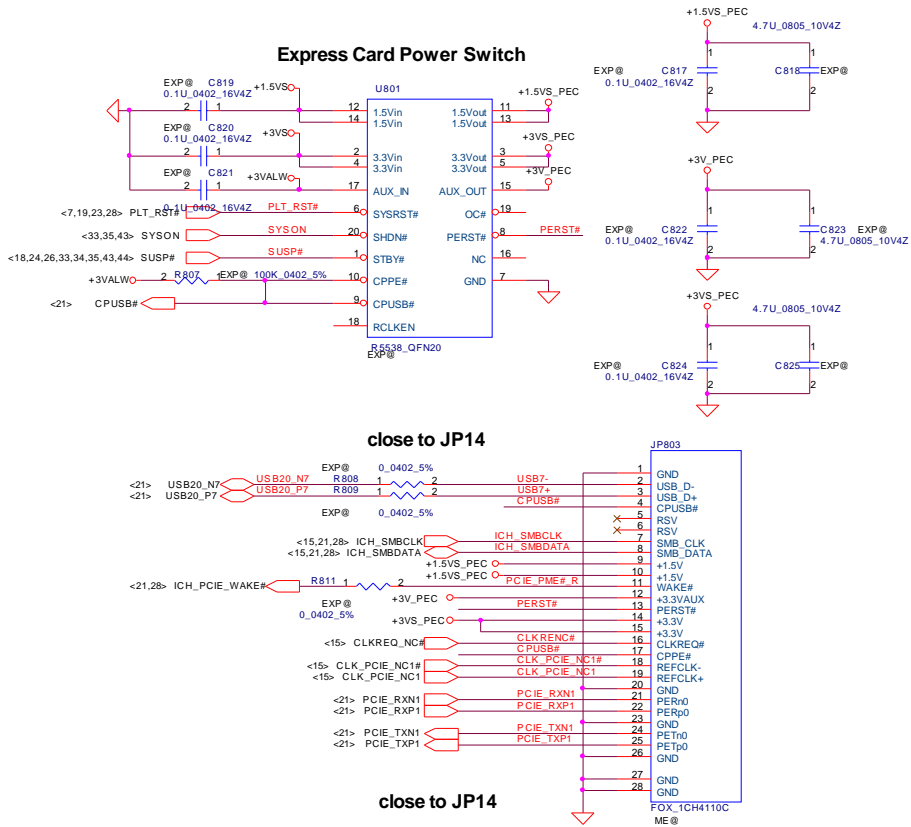
## PIN ASSIGNMENT

PIN	D-SUB	FUNCTION	PIN	SVIDEO	FUNCTION
1	9	+CRT_VCC	1	1	NC
2	1	RED	2	4	CRMA
3	6	GND	3	2	GND
4	2	GREEN	4	3	LUMA
5	7	GND	5	5	GND
6	3	BLUE	6	6	CVBS
7	8	GND			
8	14	VSYNC			
9	10	GND			
10	13	HSYNC			
11	11	SENSE			
12	12	SM_DAT			
13	15	SM_CLK			
14	4	PIN4			

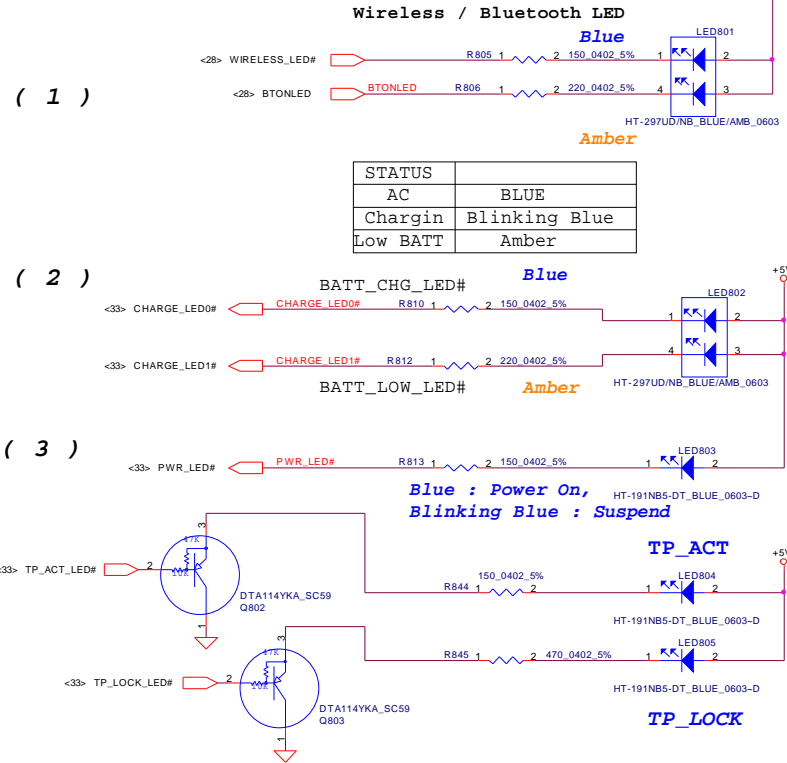
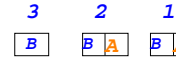
Security Classification: Compal Secret Data  
 Issued Date: 2005/03/10  
 Deciphered Date: 2006/03/10  
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Compal Electronics, Inc.  
**CRT & TVout Connector**  
 Size: Document Number  
 Custom: HGT30/31 LA3061  
 Date: 2006年03月23日  
 Sheet: 36 of 47  
 Rev: 0.1

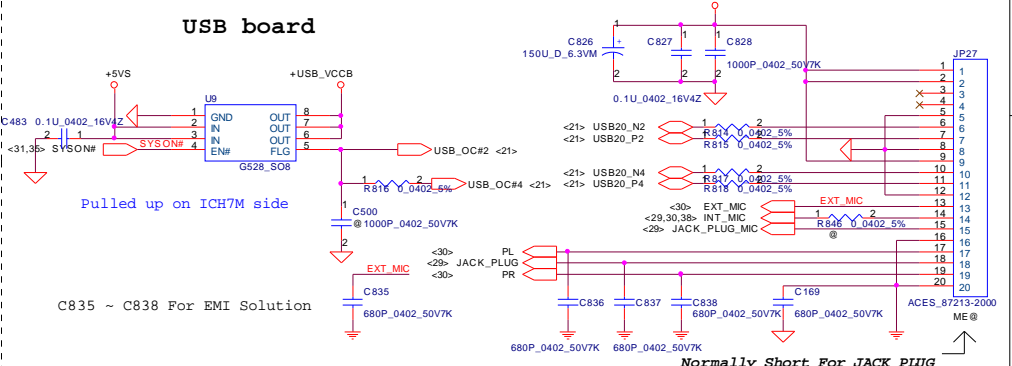
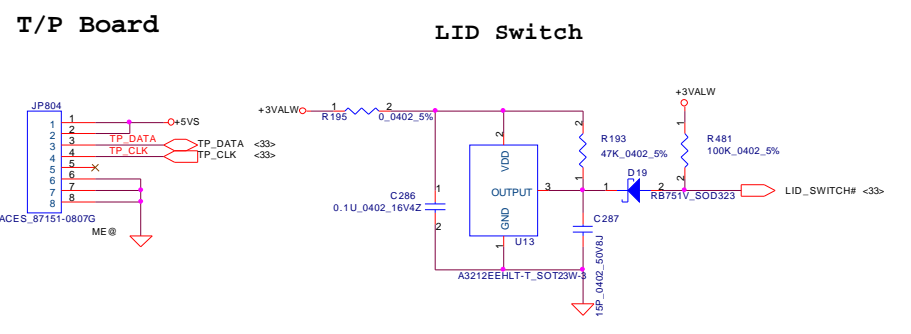
# NEW CARD FOR C38



# LED Indicator ON M/B



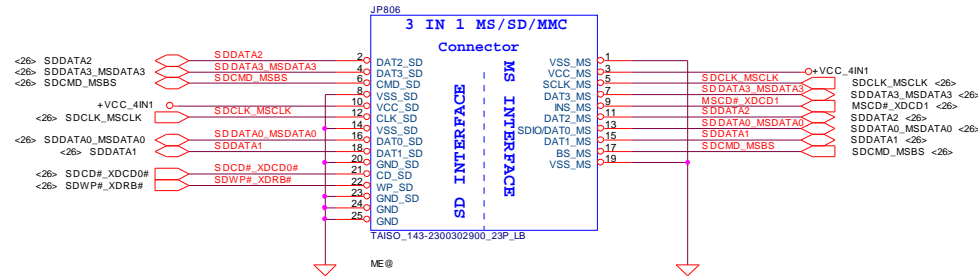
STATUS	LED
AC	BLUE
Chargin	Blinking Blue
Low BATT	Amber



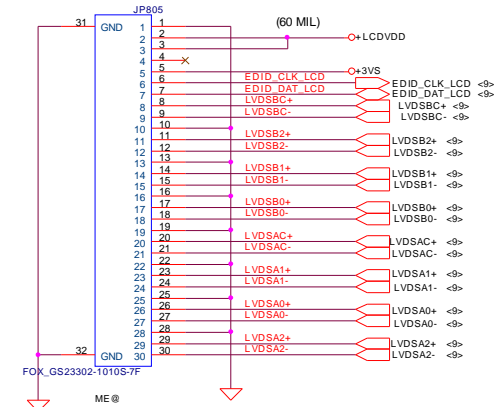
Security Classification		Compal Secret Data		Title	
Issued Date	2005/03/10	Deciphered Date	2006/03/10	INDICATE LED	
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				Customer	HGT30/31 LA3061
				Date	Rev
				2006/03/23	0.1
				Sheet	37 of 47



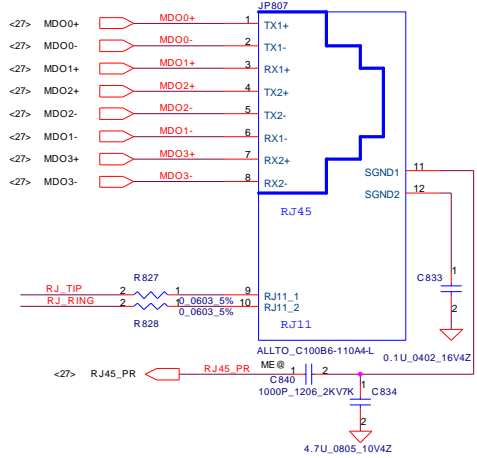
# 3 IN 1 Card Reader



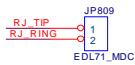
# UMA LCD/PANEL Conn.



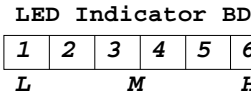
# RJ11+RJ45 CONN



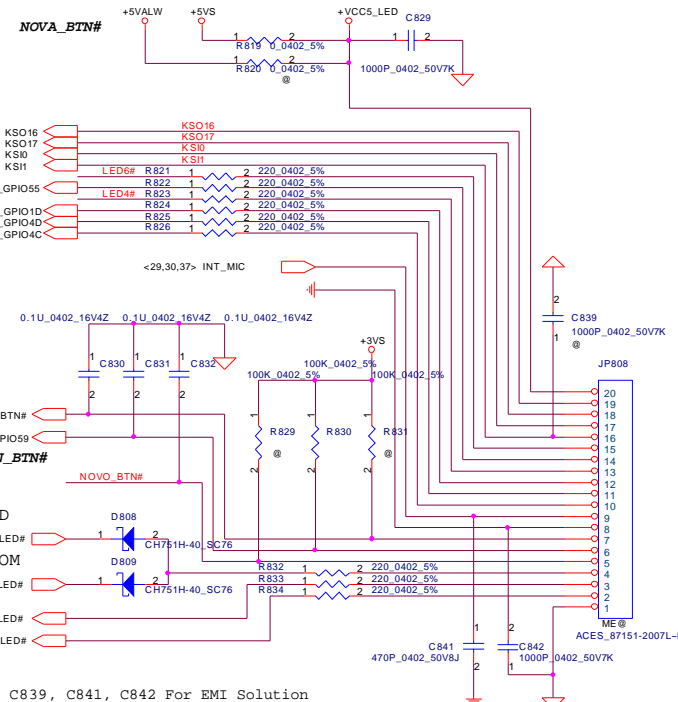
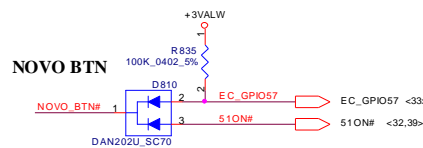
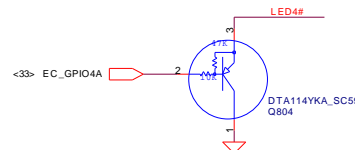
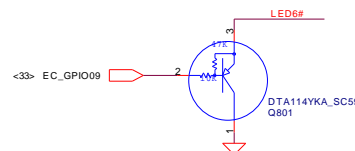
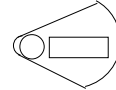
# MDC CONN



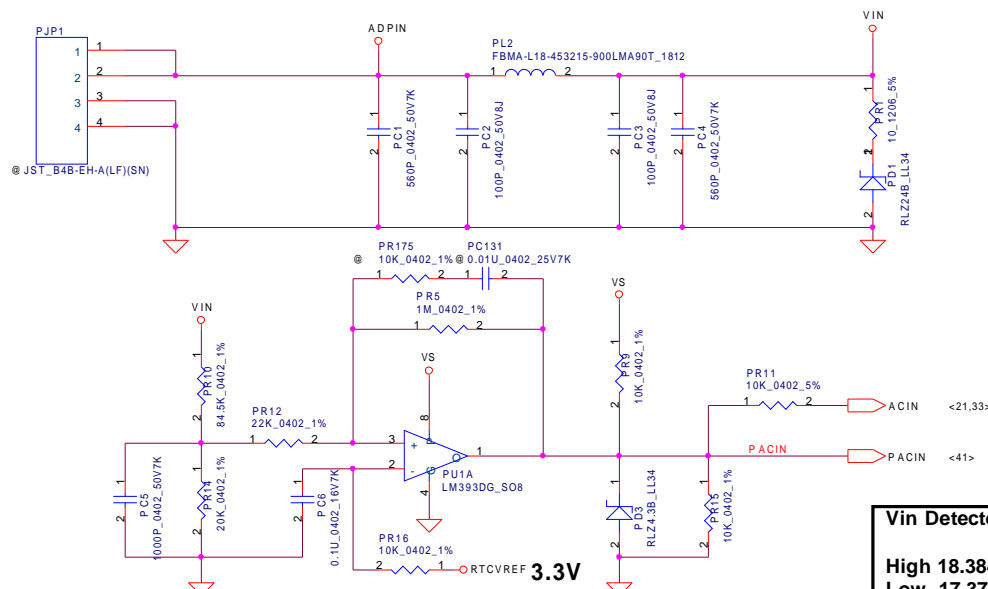
# SWITCH BD



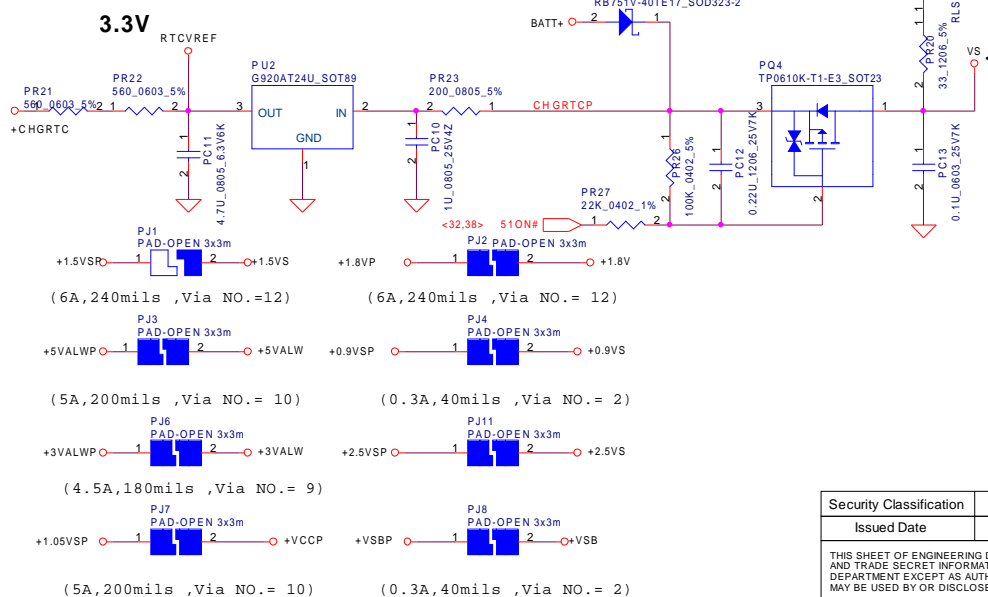
# Dial Wheel



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2005/03/10	Deciphered Date	2006/03/10	Title	INDICATE LED
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				Customer	HGT30/31 LA3061
				Date:	Rev 0.1
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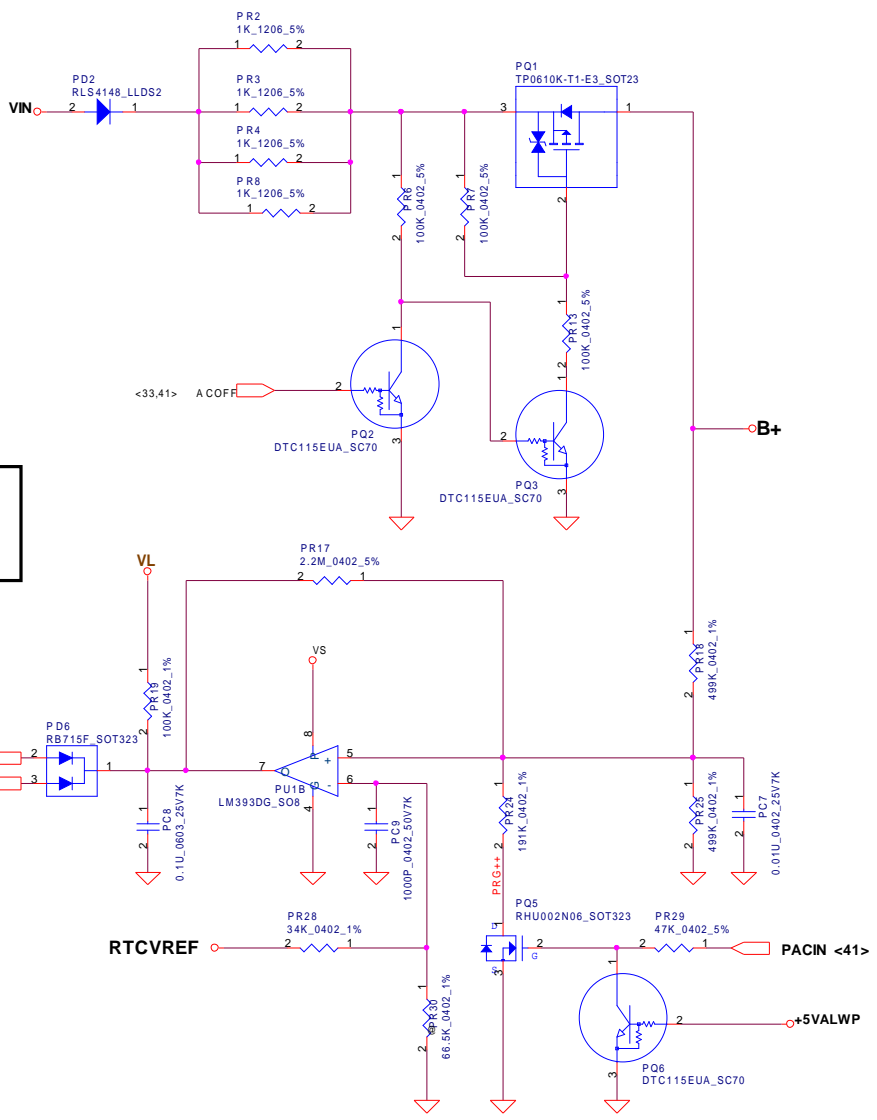


Vin Detector		
High	18.384	17.901 17.430
Low	17.370	16.907 16.630



ACIN			
Precharge detector			
	Min.	typ.	Max.
H-->L	14.620V	14.853V	15.245V
L-->H	15.534V	15.970V	16.421V

BATT ONLY			
Precharge detector			
	Min.	typ.	Max.
H-->L	6.169V	6.231V	6.361V
L-->H	7.168V	7.349V	7.537V



Security Classification	Compal Secret Data	
Issued Date	2005/08/01	Deciphered Date
		2006/08/01

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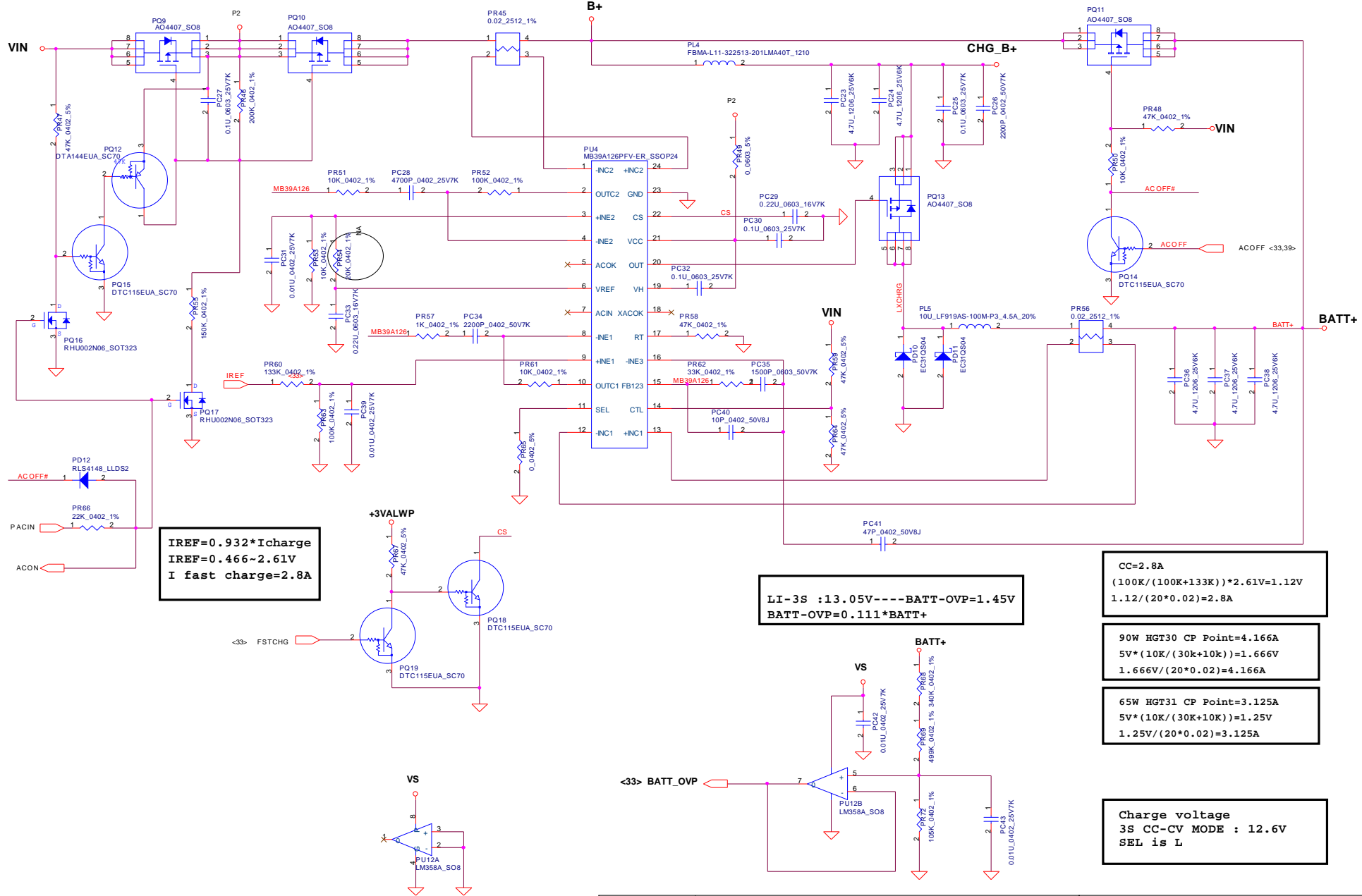
Compal Electronics, Inc.		
Title		
DCIN/DECTOR		
Size	Document Number	Rev
B		0.1
Date:	星期一, 二月 20, 2006	Sheet 39 of 48



65W PR45=0.02\_2512\_1% PR54=30K\_0402\_1% Iadp=0~3.125A  
 90W PR45=0.02\_2512\_1% PR54=20K\_0402\_1% Iadp=0~4.166A

Fosc=14100/Rt=14100/47=300KHz

Charger



$I_{REF} = 0.932 \cdot I_{charge}$   
 $I_{REF} = 0.466 \sim 2.61V$   
 $I \text{ fast charge} = 2.8A$

LI-3S : 13.05V --- BATT-OVP=1.45V  
 BATT-OVP=0.111\*BATT+

CC=2.8A  
 $(100K / (100K + 133K)) \cdot 2.61V = 1.12V$   
 $1.12V / (20 \cdot 0.02) = 2.8A$

90W HGT30 CP Point=4.166A  
 $5V \cdot (10K / (30K + 10K)) = 1.666V$   
 $1.666V / (20 \cdot 0.02) = 4.166A$

65W HGT31 CP Point=3.125A  
 $5V \cdot (10K / (30K + 10K)) = 1.25V$   
 $1.25V / (20 \cdot 0.02) = 3.125A$

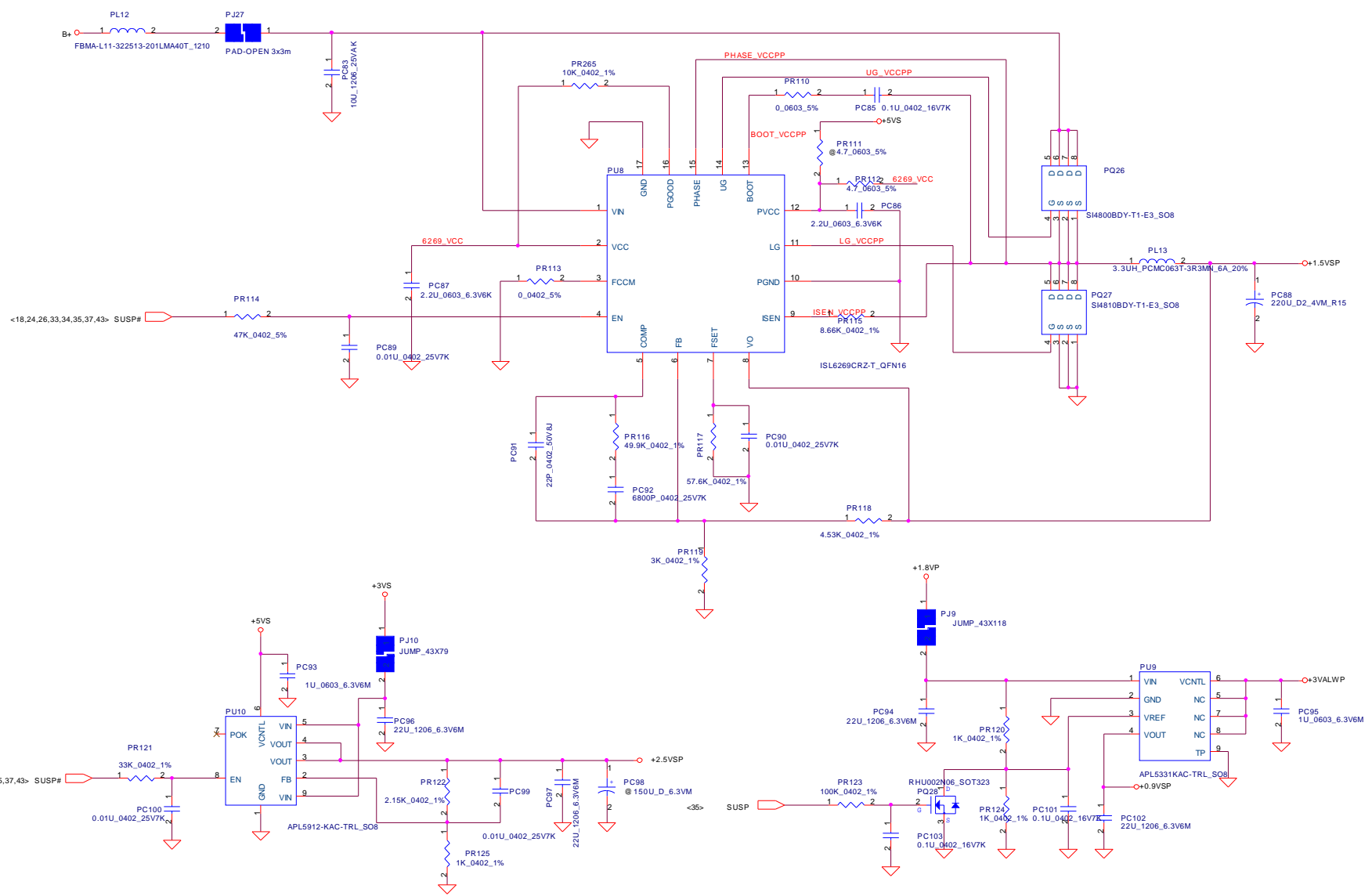
Charge voltage  
 3S CC-CV MODE : 12.6V  
 SEL is L

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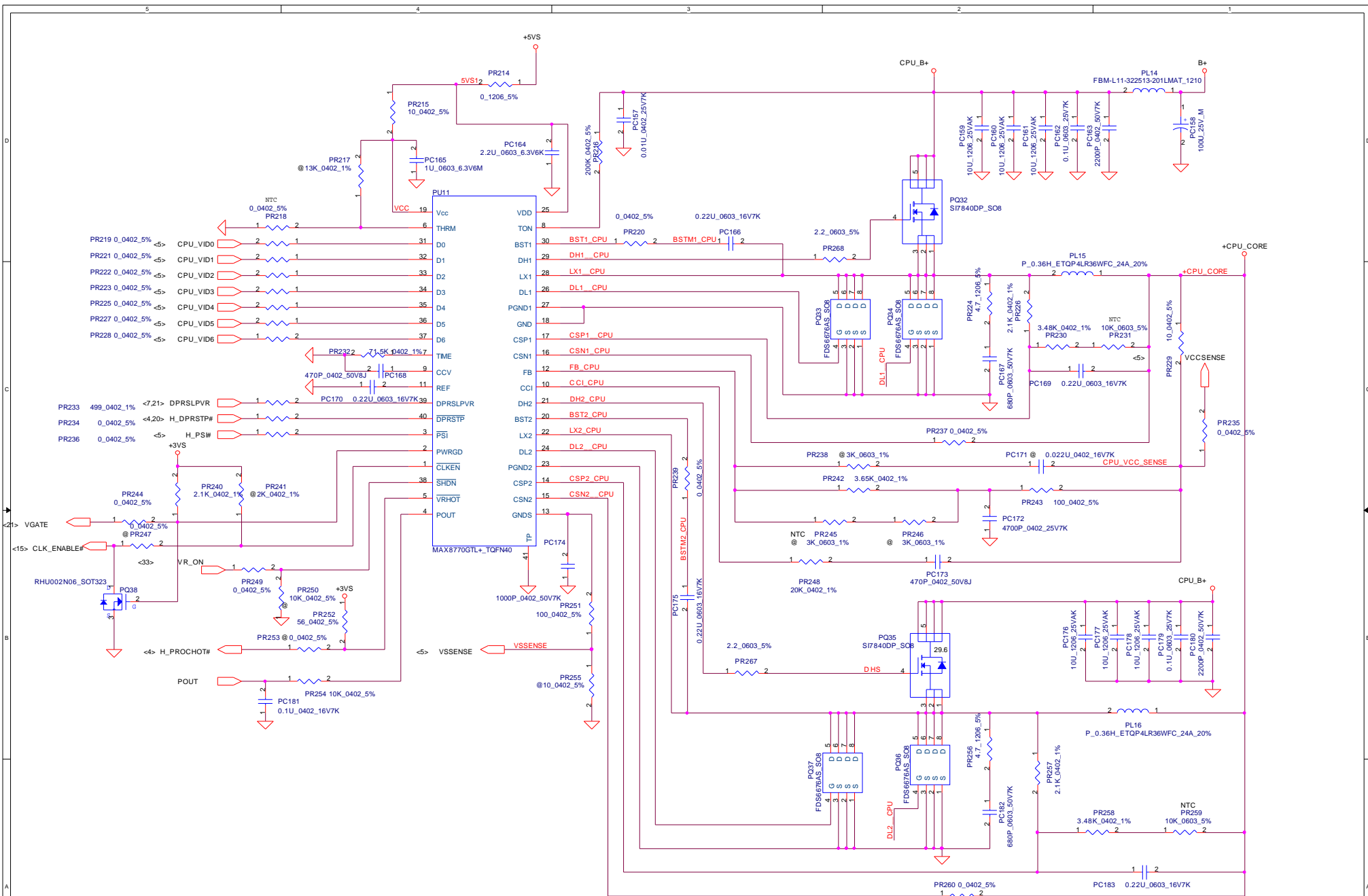


+1.5VSP Ilimit = 9.38A-12.5A



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Issued Date	2005/06/20	Deciphered Date	2006/06/20	+CPU CORE
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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	VER	Phase
1		MODIFY 3V/5V current limit to 6.5A~8.1A/6.5A to 10.2A		42	MODIFY PR83/PR84 FROM 499K TO 374K		DVT
2		ADD or decrease CPU CORE ring with EMI solution : snubber		45	Reserve PR224//PR256: 4.7 1206 ,add PC167/PC182:680P		DVT
3		Reserve PR267,PR268 seperate in CPU CORE high side gate for EMI require		45	Reserve PR267,PR268:0 0603		DVT
4		change PJP1 from 5 pin to 4 pin		39	change PJP1 from 5 pin to 4 pin		DVT
5		modify sequecce		43	change PR179 to 100k, PC132 =0.1U		DVT
6		modify Vgate		45	add PQ38:RHU002N06,PR240:2K,delete PR247		
7							
8							
9							
10							
11							
8							
9							

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<b>PIR (PWR)</b>			
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			0.2
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Version change list (P.I.R. List)

Item	Fixed Issue	Rev.	PG#	Modify List	B.Ver#	Phase
1	Add EC_Port80 Signals to DDR2 DIMM1 & DIMM2	0.2	P.13 P.14	1.Connect U6.91 (EC_P80_CLK) through a 0 Ohm R to JP3.83 & JP4.83 2.Connect U6.92 (EC_P80_DATA) through a 0 Ohm R to JP3.69 & JP4.69	0.2	DVT
2	Impedance not match for both CRT & TV Out	0.2	P.17	R3, R4, R5, R6, R7, R8 Change from NC to 150 Ohm	0.2	DVT
3	LCD Panel will flash white frame when power on	0.2	P.16	no stuff D10 (CH751H), stuff R204 (100K)	0.2	DVT
4	ICH7's GPIO configuration modification	0.2	P.21	GPIO10 connect to ACIN GPIO7 connect to G7X_THER_ALERT# GPIO39 connect to KILL_MDCH#	0.2	DVT
5	<New Add> MDC supports S4/S5 resuming	0.2	P.28	MDC power connection change to +3VALW from +3VS	0.2	DVT
6	Audio Circuit modification for : 1. Line-Out connection change from Pin.35/Pin.36 to Pin.43/Pin.45 2. Audio-OUT Auto-Switch by HP Plugging In 3. MicPhone Noise Reduction 4. Cleared off BO Sound from both entry of Windows XP & Power Off	0.2	P.29-31	Line-Out connection change from Pin.35/Pin.36 to Pin.43/Pin.45 Connect Pin.32 (LFE_OUT) through 2 luF Cap to Pin.43/Pin.45 +Audio_VREF_LF connection change to 1/2 +AVDD_AC97 Int.MIC connection changes to Pin31/Pin32 through luF for each New Add a JACK_PLUG_MIC signal from MIC JACK EAPD signal connect to EC'sGPIO4B APA2068's I3PIN(SE/BTL#) connect to GND	0.2	DVT
7	EC GPIO configuration modification	0.2	P.33	New add Port80 information OUT from Pin34(CLK), pin35(DATA) LED4 connection changes from GPIO17(35 PIN) to GPIO4A(91 PIN) New Add DAC's EAPD connect to EC's GPIO4B (92PIN). SKU_ID (GPIO3B) Changes to BRD_ID New Add WL_OFF# (GPIO1F, 46PIN) New Add BT_OFF# (GPIO50, 84PIN) New Add TP_ACT_LED# (GPIO3F, 80PIN) New Add TP_LOCK_LED# (GPIO12, 30PN)	0.2	DVT
8	Lid Switch changes from USB BD to M/B	0.2	P.37	Circuit of Lid SW changes from USB BD to M/B (DEL Lid SW on USB BD)	0.2	DVT
9	Blue LED too dark when active due to VF too High on blue LED	0.2	P.37-38	Changes LED power from +3VS(+3VALW) to +5VS(+5VALWS)	0.2	DVT
10	New Add LED Buffer for LED4, TP_LOCK_LED#, TP_ACT_LED#	0.2	P.37  P.38	TP_ACT_LED# connect to Q802.2, and Q802.1 to GND, then connect to LED804 through a 220 Ohm R  TP_LOCK_LED# connect to Q803.2, and Q802.1 to GND, then connect to LED805 through a 220 Ohm R  EC_GPIO4A connect to Q804.2, and Q804.1 to GND, then connect to R283 (220 Ohm)	0.2	DVT
11	leakage of electricit when System is running S3 mode	0.2		NC For R458, R402, R411, R128, R831, R829	0.2	DVT

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Version change list (P.I.R. List)

Item	Fixed Issue	Rev.	PG#	Modify List	B.Ver#	Phase
12	GIGA LAN function failed for both Loopback or PXE on RTL8110SCL solution	0.3	P.27	1. Add a R734 (0 Ohm) resistor between +2.5V_LAN & VTCT for MAC 2. Removed all of the bypass Cap.(C398, C396, C418, C408) for MAC's TCT pins 3. Removed all of pulled down resistors (49.9 Ohm) & Cap.(0.01u)	0.3	PVT
13	Subwoofer still make POP Sound	0.3	P.31	1. Add 0 Ohm resistors, R732 (0 Ohm) connection between AMP_OFF# & U12.2 (SD#) for reserved 2. a 0 Ohm connection between EAPD & U12.2(SD#)	0.3	PVT
14	Mic Switch between Int. & Ext. be Failed	0.3	P.29	1. R717.1 Disconnect from U11.17 2. R717.1 connect to U11.16	0.3	PVT
15	Wrong parts	0.3	P.35	Change package of C434, C224 & C312 from 0402 to 0603	0.3	PVT
16	Add a discharging path of +3.3VS	0.3	P.35	1. Connect +3.3VS to R731.1 2. Connect R731.2 to Q704.1 3. Connect Q704.2 to NET : SUSP signal 4. Connect Q704.3 to GND	0.3	PVT

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