

JITR1/R2_DDR3

Schematics Document

Mobile Penryn uFCPGA with Intel
Cantiga_GM/PM+ICH9-M core logic

Friday, April 18, 2008

REV:1.0

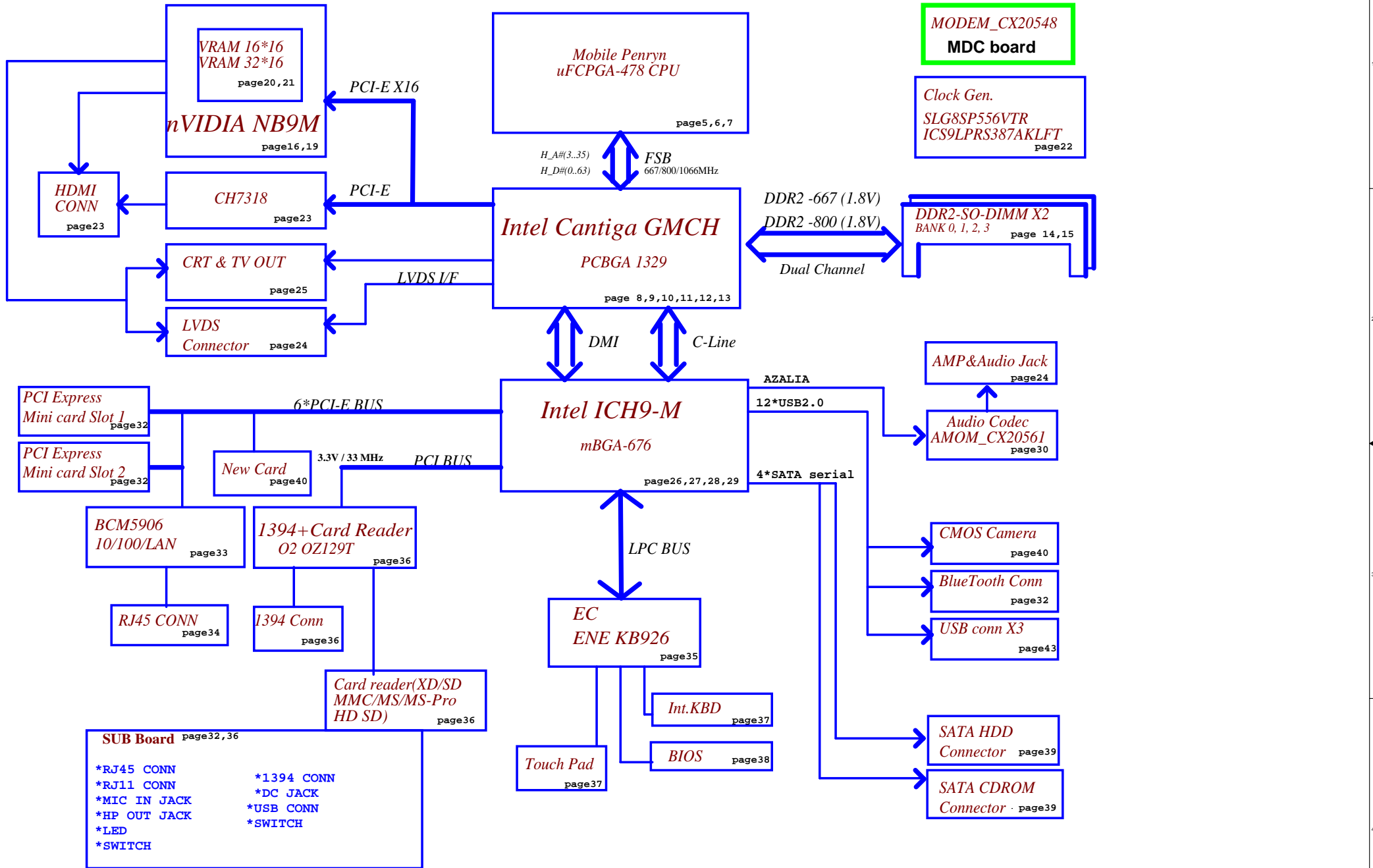
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Issued Date	2007/10/15	Deciphered Date	2008/10/15	<i>Cover Sheet</i>		
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POWER Board

CAP SENSE LEDs Board

CONTROL Board



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				MB Block Diagram		
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DDR2 Voltage Rails

power plane	+B	+5VALW +3VALW	+1.8V	+5VS +3VS +1.5VS +0.9VS +VCCP +CPU_CORE +VGA_CORE +1.8VS
				State
s0	o	o	o	o
s1	o	o	o	o
s3	o	o	o	X
s5 S4/AC	o	o	X	X
s5 S4/ Battery only	o	X	X	X
s5 S4/AC & Battery don't exist	X	X	X	X

SMBUS, SPI and I2C Control Table

	SOURCE	HDMI	LVDS	CRT	HDCP	SERIAL EEPROM	NEW CARD	CLK GEN	CAP sensor	Mini CARD1	Mini CARD2	BATT	THERMAL SENSOR (VGA)	THERMAL SENSOR (CPU)
EC_SMB_CK1 EC_SMB_DA1	KB926	X	X	X	X	V	X	X	X	X	X	V	V	X
EC_SMB_CK2 EC_SMB_DA2	KB926	X	X	X	X	X	X	X	V	X	X	X	V	V
ICH_SMBCLK ICH_SMBDAT	ICH9	X	X	X	X	X	V	V	X	V	V	X	X	X
LVDS_SCL LVDS_SDA	Cantiga	X	V	X	X	X	X	X	X	X	X	X	X	X
GMCH_CRT_CLK GMCH_CRT_DAT	Cantiga	X	X	V	X	X	X	X	X	X	X	X	X	X
HDMICLK_NB HDMIDAT_NB	Cantiga	V	X	X	X	X	X	X	X	X	X	X	X	X
VGA_DDCCLK VGA_DDCDATA	VGA	X	X	V	X	X	X	X	X	X	X	X	X	X
VGA_LVDS_SCL VGA_LVDS_DAT	VGA	X	V	X	X	X	X	X	X	X	X	X	X	X
VGA_HDMI_SCL VGA_HDMI_DAT	VGA	V	X	X	X	X	X	X	X	X	X	X	X	X
HDCP_SMB_CK1 HDCP_SMB_DA1	VGA	X	X	X	X	V	X	X	X	X	X	X	X	X
FSEL#SPICS#_SB FRD#SPI_SO_SB SPI_CLK_SB FWR#SPI_SI_SB	ICH9	X	X	X	X	V	X	X	X	X	X	X	X	X
FSEL#SPICS# FRD#SPI_SO SPI_CLK FWR#SPI_SI	KB926	X	X	X	X	V	X	X	X	X	X	X	X	X

DDR3 Voltage Rails

power plane	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +0.75V +VCCP +CPU_CORE +VGA_CORE +1.8VS
				State
s0	o	o	o	o
s1	o	o	o	o
s3	o	o	o	X
s5 S4/AC	o	o	X	X
s5 S4/ Battery only	o	X	X	X
s5 S4/AC & Battery don't exist	X	X	X	X

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				MB Notes List		
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VGA and DDR2 Voltage Rails (NB9M-GS)

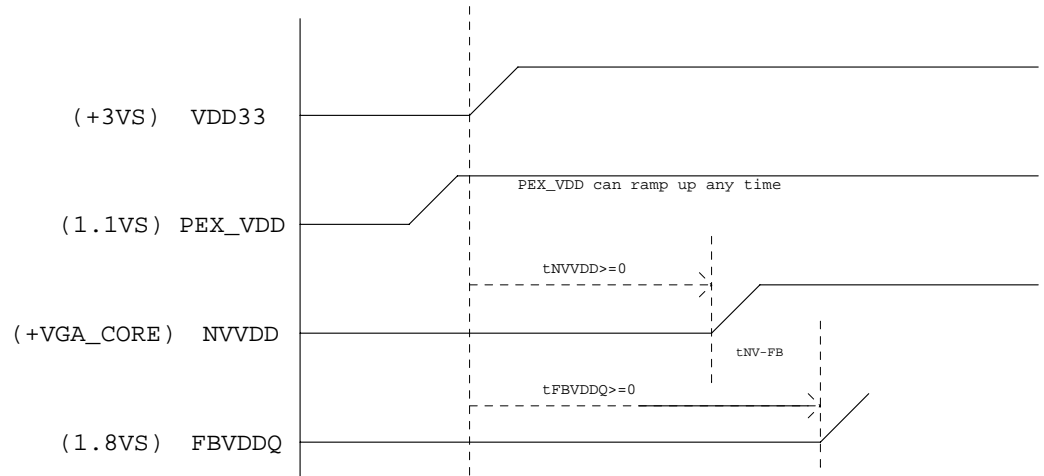
power plane			+1.8V	+3VS +VGA_CORE
S0	○	○	○	○
S1	○	○	○	○
S3	○	○	○	✗
S5 S4/AC	○	○	✗	✗
S5 S4/ Battery only	○	✗	✗	✗
S5 S4/AC & Battery don't exist	✗	✗	✗	✗

EDP at Tj = 97C*

Power Supply Rail		NB9M-GS		NB9M-GE	
(V)		GDDR3	DDR2	GDDR3	DDR2
NVVDV	Variable	11.22A	10.87A	9.2A	8.88A
FB_DLLAVDD	1.1	25mA			
FB_PLLAVDD	1.1	10mA			
IFPC_IOVDD	1.1	385mA			
IFPD_IOVDD	1.1	385mA			
IFPE_IOVDD	1.1	385mA			
IFPF_IOVDD	1.1	385mA			
PEX_IOVDD/Q	1.1	1550mA			
PEX_PLLVDD	1.1	165mA			
PLLVDV	1.1	55mA			
SP_PLLVDV	1.1	25mA			
VID_PLLVDV	1.1	50mA			
TOTAL	1.1	3.425A			
FBVDV/Q	1.8	2.24A	1.65A	2.17A	1.63A
IFPA_IOVDD	1.8	50mA			
IFPB_IOVDD	1.8	50mA			
IFPAB_PLLVDV	1.8	100mA			
IFPCD_PLLVDV	1.8	160mA			
IFPEF_PLLVDV	1.8	160mA			
TOTAL	1.8	2.76A	2.17A	2.69A	2.15A
DACA_VDD	3.3	110mA			
DACB_VDD	3.3	125mA			
DACC_VDD	3.3	110mA			
MIOA_VDDQ	3.3	10mA			
MIOB_VDDQ	3.3	10mA			
VDD33	3.3	80mA			
TOTAL	3.3	0.445A			

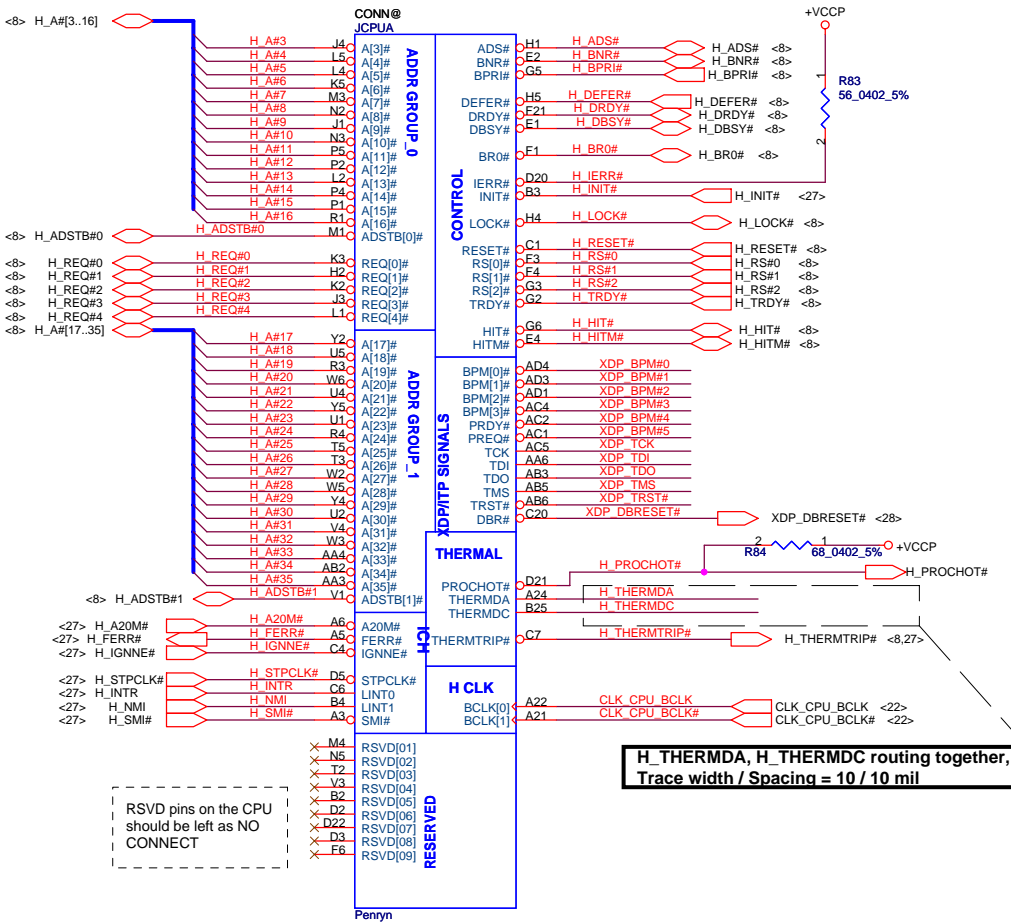
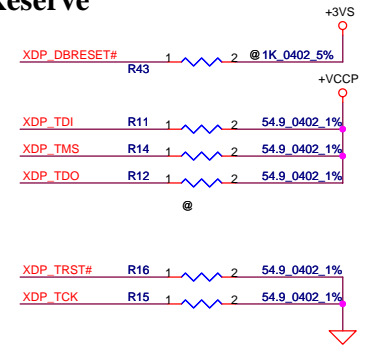
POWER SQUENCE

The ramp time for any rail must be more than 40us

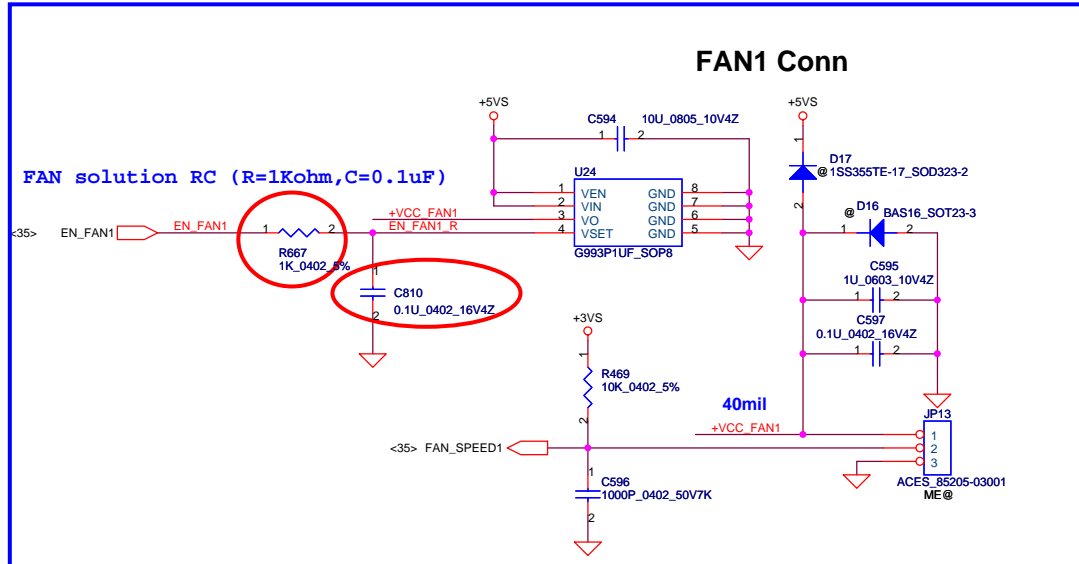
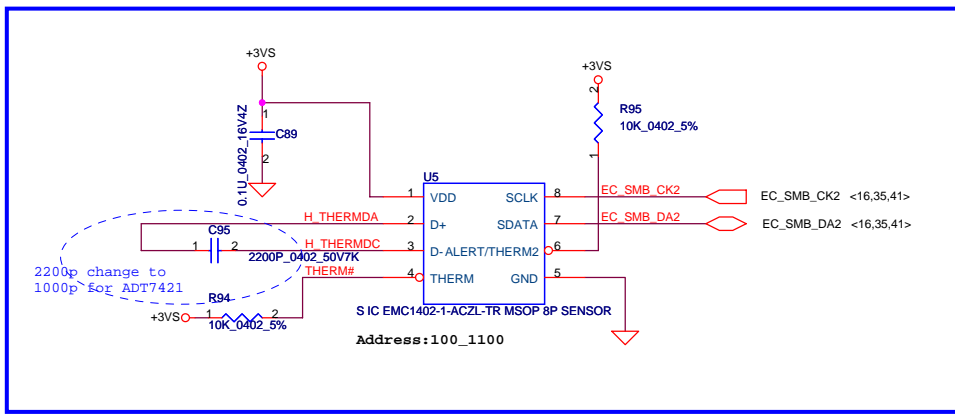


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XDP Reserve

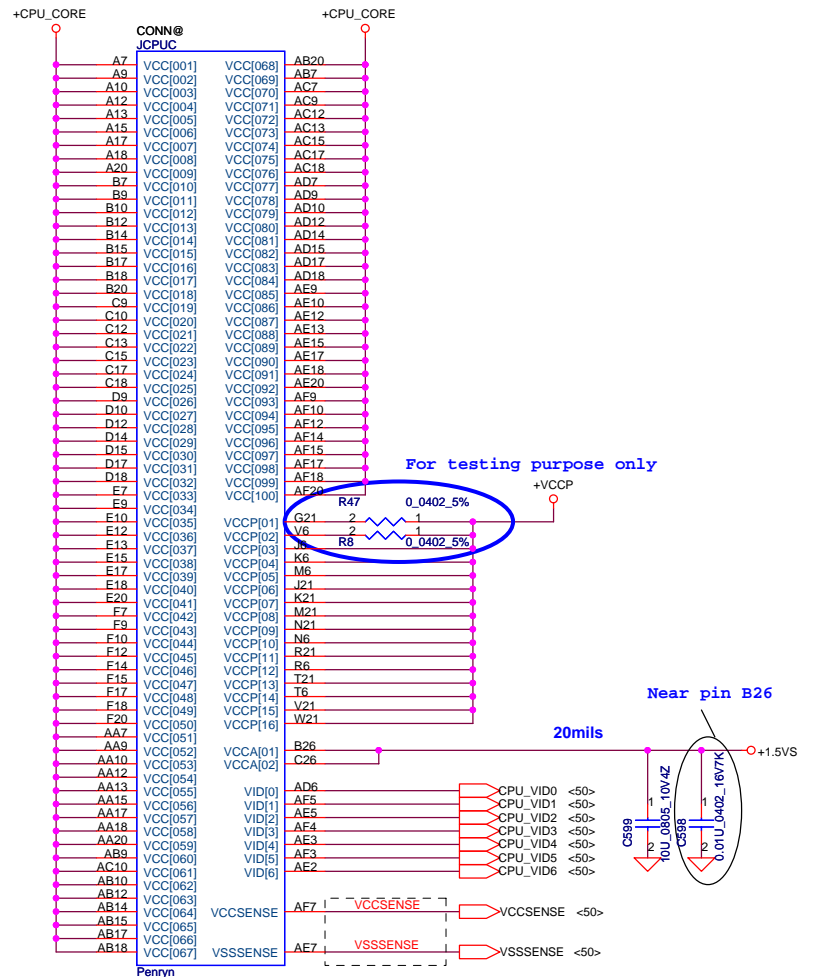
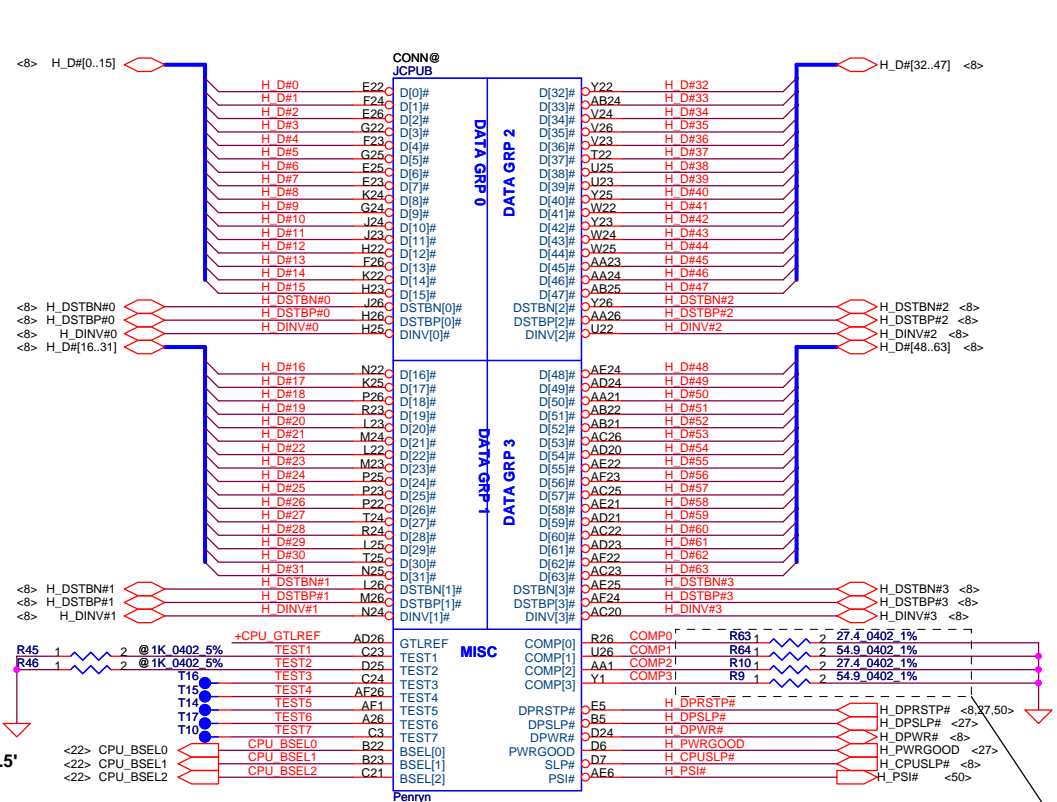


H_THERMDA, H_THERMDC routing together, Trace width / Spacing = 10 / 10 mil



RSVD pins on the CPU should be left as NO CONNECT

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Trace Close CPU < 0.5'

Width=4 mil ,
Spacing: 15mil
(55Ohm)

TRACE CLOSELY CPU < 0.5'

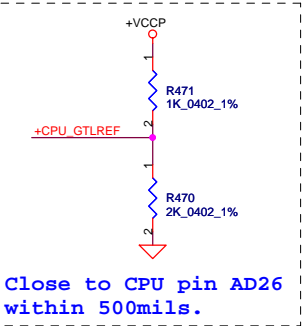
COMP0, COMP2 layout : Width 18mils and Space 25mils (27.4Ohms)
COMP1, COMP3 layout : Width 4mils and Space 25mils (55Ohms)

layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

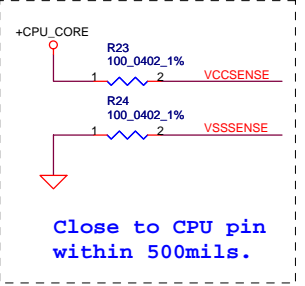
FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0
1067	266	0	0	0

Length match within 25 mils.
The trace width/space/other is 16/7/25.

Layout Note:
Route VCCSSENSE and VSSSENSE traces at 27.4 Ohms with 50 mil spacing.
Place PU and PD within 1 inch of CPU.
Length matched to within 25 mils.



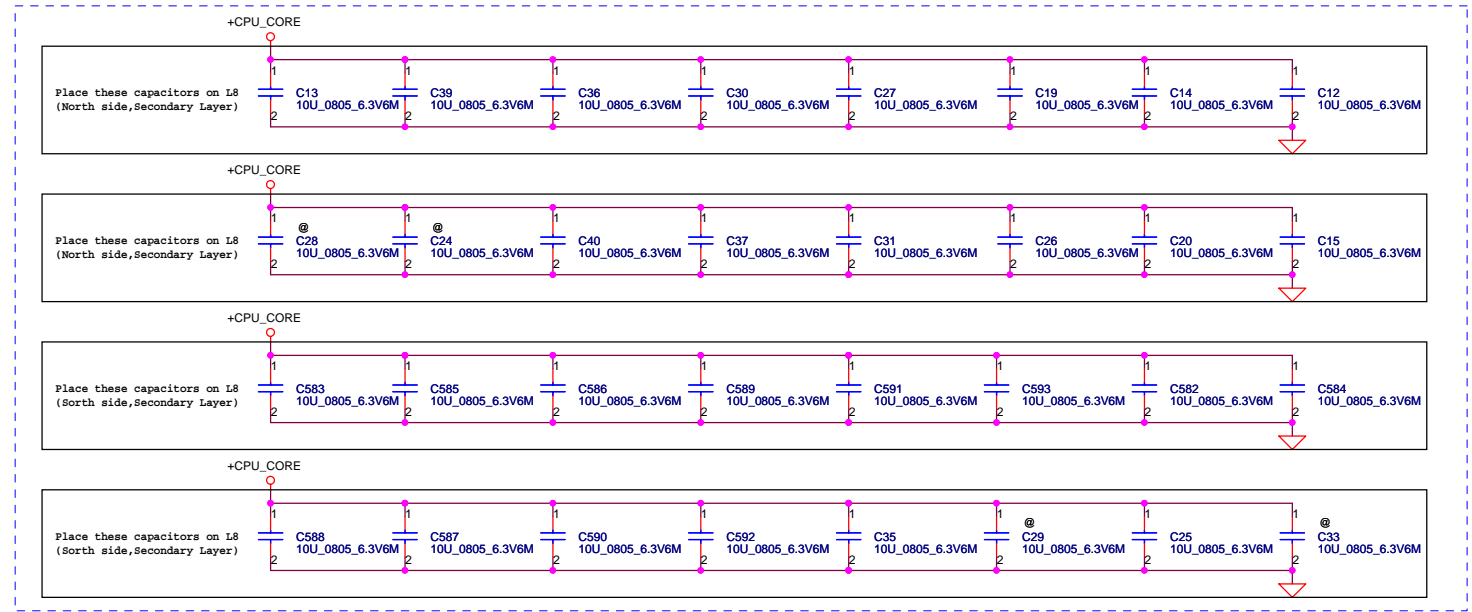
Close to CPU pin AD26 within 500mils.



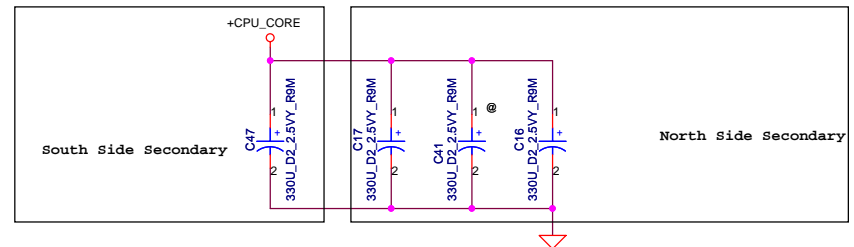
Close to CPU pin within 500mils.

Layout note: Z0=55 ohm
0.5" max for GTLREF.

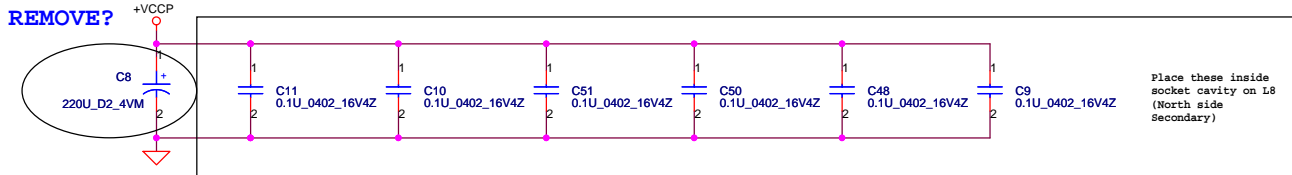
CONN@	JCPU	VSS	PCB
A4	VSS[001]	VSS[082]	P6
A8	VSS[002]	VSS[083]	P21
A11	VSS[003]	VSS[084]	P24
A14	VSS[004]	VSS[085]	R2
A16	VSS[005]	VSS[086]	R5
A19	VSS[006]	VSS[087]	R22
A23	VSS[007]	VSS[088]	R25
AF2	VSS[008]	VSS[089]	T1
B6	VSS[009]	VSS[090]	T4
B8	VSS[010]	VSS[091]	T23
B11	VSS[011]	VSS[092]	T26
B13	VSS[012]	VSS[093]	U3
B16	VSS[013]	VSS[094]	U6
B19	VSS[014]	VSS[095]	U21
B21	VSS[015]	VSS[096]	U24
B24	VSS[016]	VSS[097]	V2
C5	VSS[017]	VSS[098]	V5
C8	VSS[018]	VSS[099]	V22
C11	VSS[019]	VSS[100]	V25
C14	VSS[020]	VSS[101]	W1
C16	VSS[021]	VSS[102]	W4
C19	VSS[022]	VSS[103]	W23
C2	VSS[023]	VSS[104]	W26
C22	VSS[024]	VSS[105]	Y3
C25	VSS[025]	VSS[106]	Y6
D1	VSS[026]	VSS[107]	Y21
D4	VSS[027]	VSS[108]	Y24
D8	VSS[028]	VSS[109]	AA2
D11	VSS[029]	VSS[110]	AA5
D13	VSS[030]	VSS[111]	AA8
D16	VSS[031]	VSS[112]	AA11
D19	VSS[032]	VSS[113]	AA14
D23	VSS[033]	VSS[114]	AA16
D26	VSS[034]	VSS[115]	AA19
E3	VSS[035]	VSS[116]	AA22
E6	VSS[036]	VSS[117]	AA25
E8	VSS[037]	VSS[118]	AB1
E11	VSS[038]	VSS[119]	AB4
E14	VSS[039]	VSS[120]	AB8
E16	VSS[040]	VSS[121]	AB11
E19	VSS[041]	VSS[122]	AB13
E21	VSS[042]	VSS[123]	AB16
E24	VSS[043]	VSS[124]	AB19
F5	VSS[044]	VSS[125]	AB23
F8	VSS[045]	VSS[126]	AB26
F11	VSS[046]	VSS[127]	AC3
F13	VSS[047]	VSS[128]	AC6
F16	VSS[048]	VSS[129]	AC8
F19	VSS[049]	VSS[130]	AC11
F2	VSS[050]	VSS[131]	AC14
F22	VSS[051]	VSS[132]	AC16
F25	VSS[052]	VSS[133]	AC19
G4	VSS[053]	VSS[134]	AC21
G1	VSS[054]	VSS[135]	AC24
G23	VSS[055]	VSS[136]	AD2
H3	VSS[056]	VSS[137]	AD5
H6	VSS[057]	VSS[138]	AD8
H21	VSS[058]	VSS[139]	AD11
H24	VSS[059]	VSS[140]	AD13
H24	VSS[060]	VSS[141]	AD16
J2	VSS[061]	VSS[142]	AD19
J5	VSS[062]	VSS[143]	AD22
J22	VSS[063]	VSS[144]	AD25
J25	VSS[064]	VSS[145]	AE1
K1	VSS[065]	VSS[146]	AE4
K4	VSS[066]	VSS[147]	AE8
K23	VSS[067]	VSS[148]	AE11
K26	VSS[068]	VSS[149]	AE14
L3	VSS[069]	VSS[150]	AE16
L6	VSS[070]	VSS[151]	AE19
L21	VSS[071]	VSS[152]	AE23
L24	VSS[072]	VSS[153]	AE26
M2	VSS[073]	VSS[154]	A2
M5	VSS[074]	VSS[155]	AF6
M22	VSS[075]	VSS[156]	AF8
M25	VSS[076]	VSS[157]	AF11
N1	VSS[077]	VSS[158]	AF13
N4	VSS[078]	VSS[159]	AF16
N23	VSS[079]	VSS[160]	AF19
N26	VSS[080]	VSS[161]	AF21
P3	VSS[081]	VSS[162]	A25
		VSS[163]	AF25



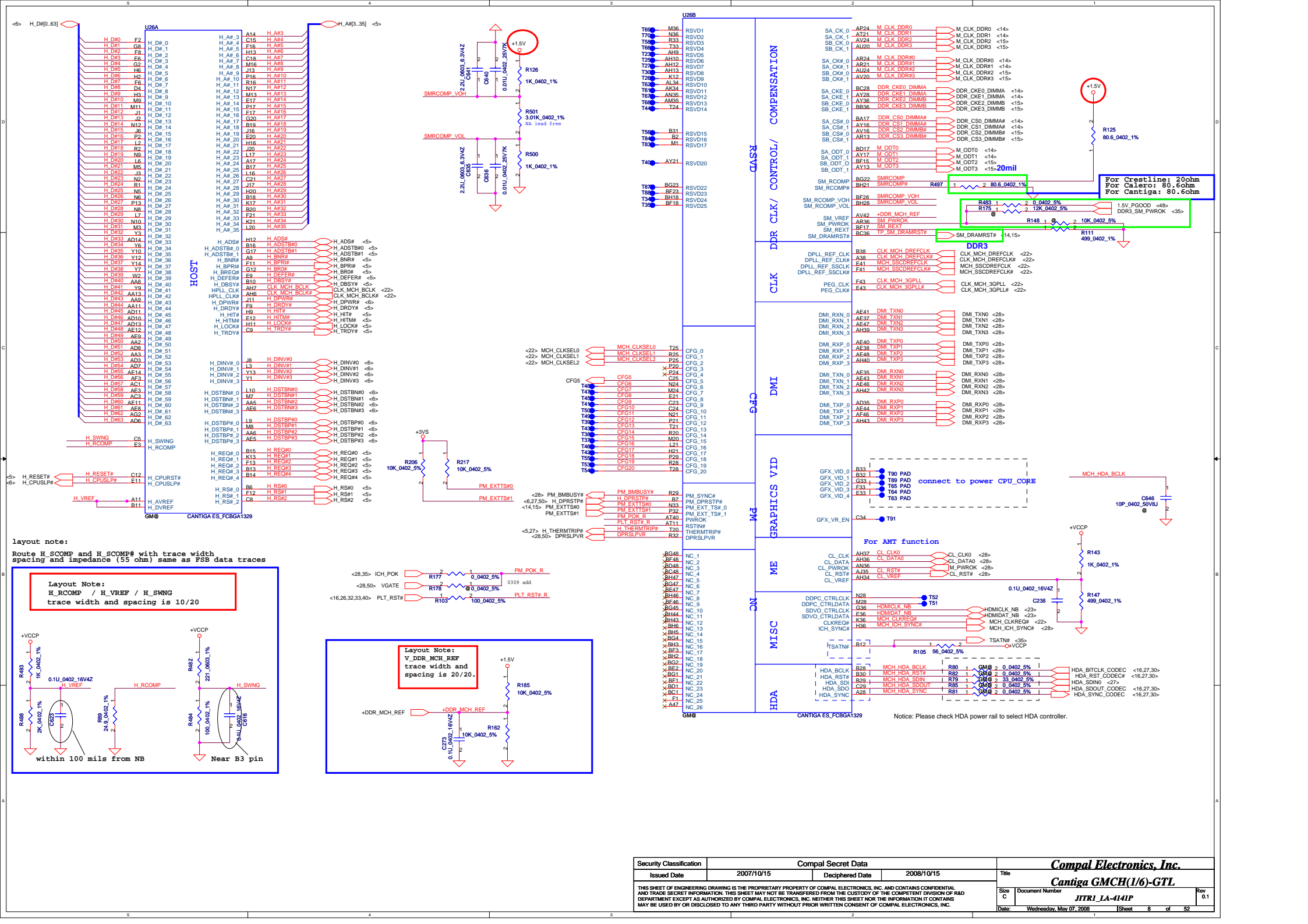
Mid Frequency Decoupling



ESR <= 1.5m ohm
Capacitor > 1980uF

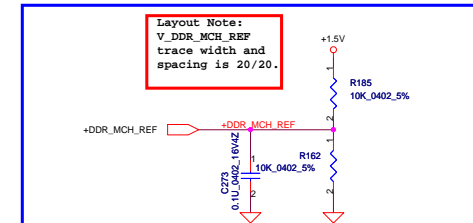
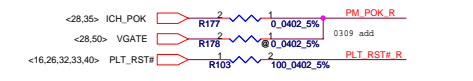
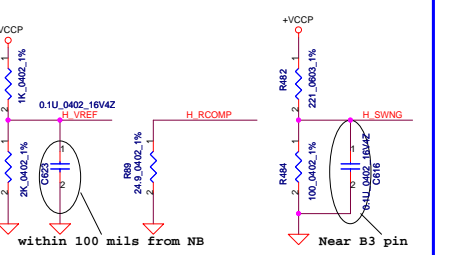


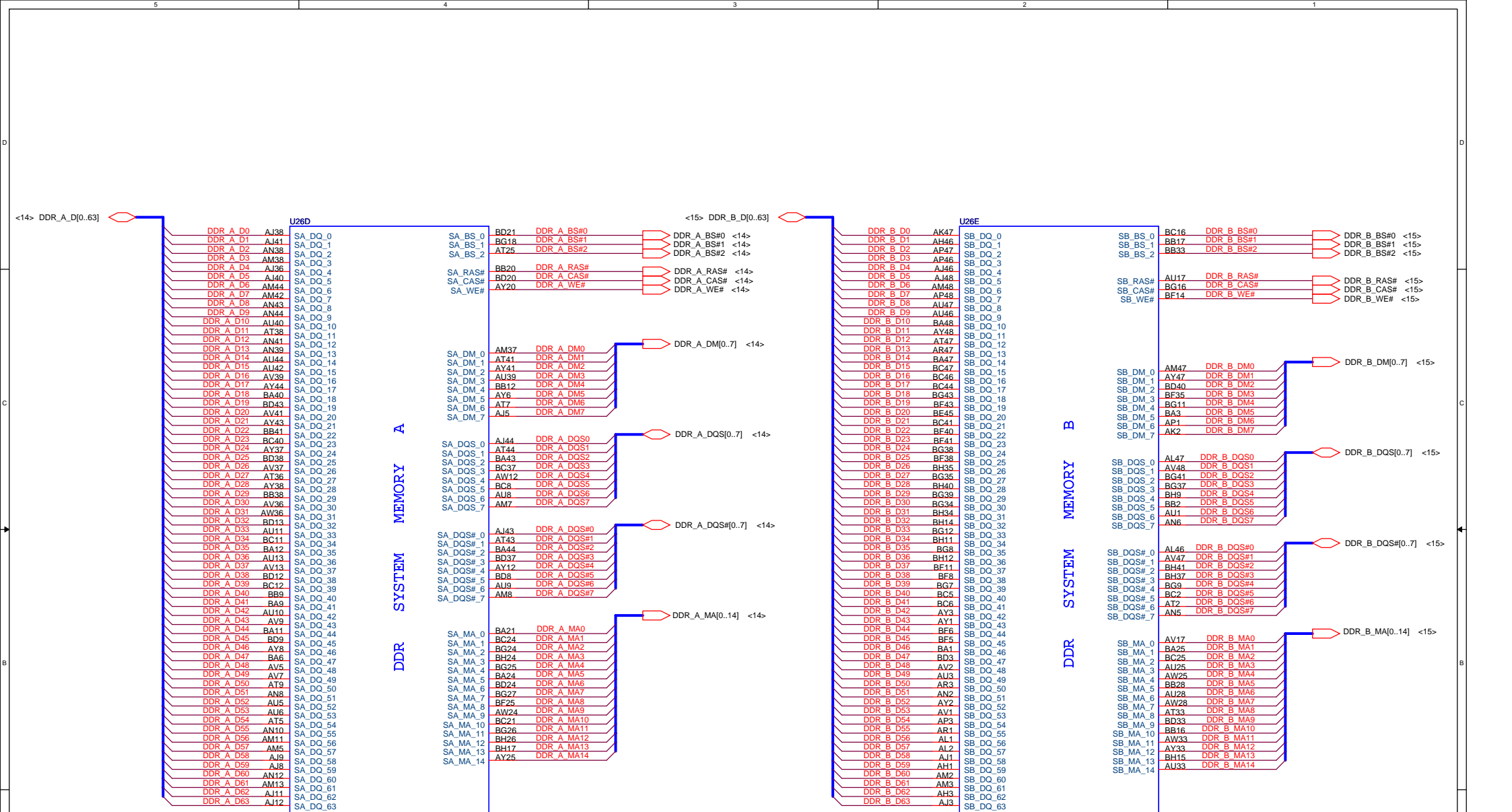
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layout note:
Route H_SCAMP and H_SCAMP# with trace width spacing and impedance (55 ohm) same as FSB data traces

Layout Note:
H_RCAMP / H_VREF / H_SWING
trace width and spacing is 10/20

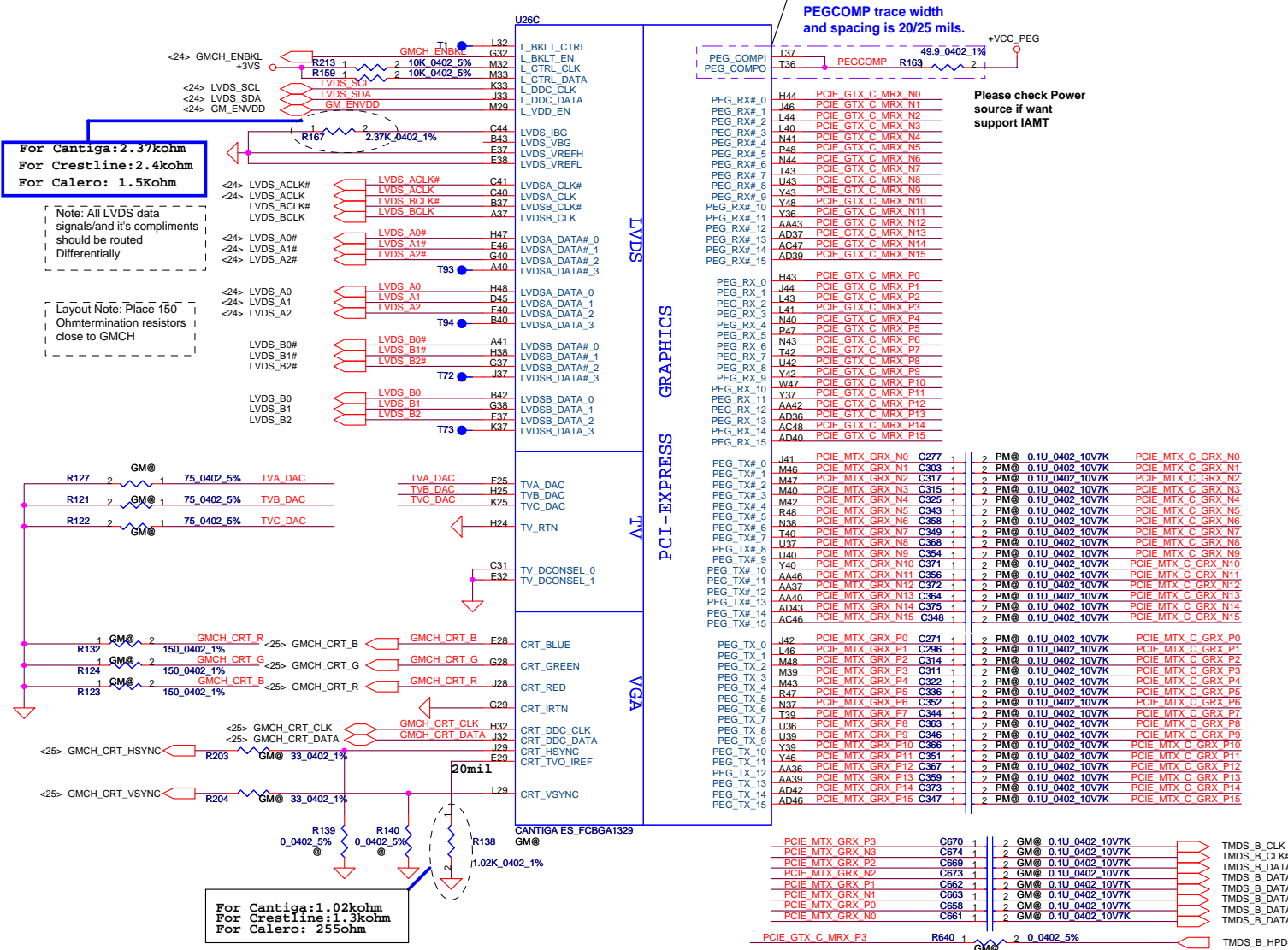




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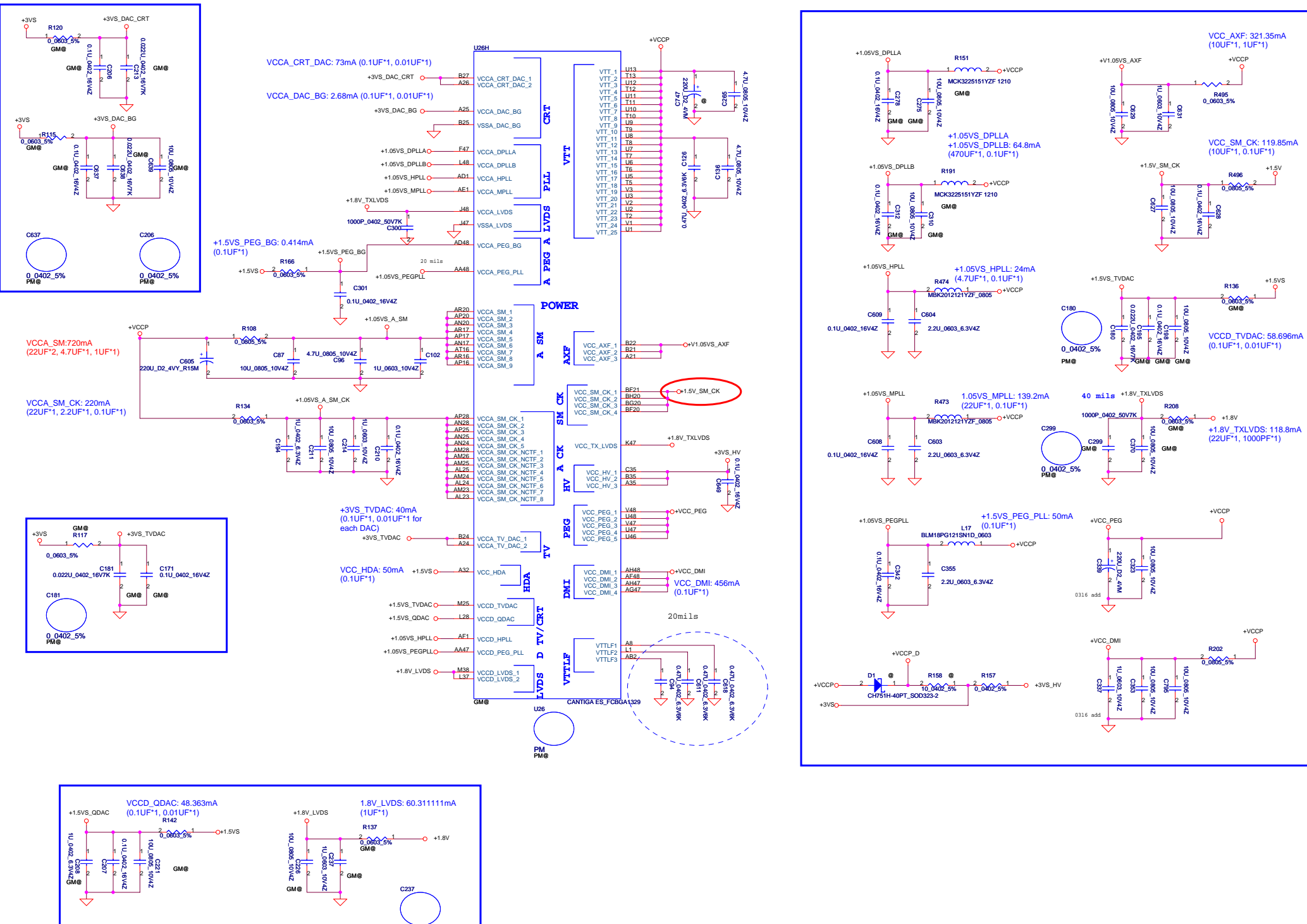
Strap Pin Table

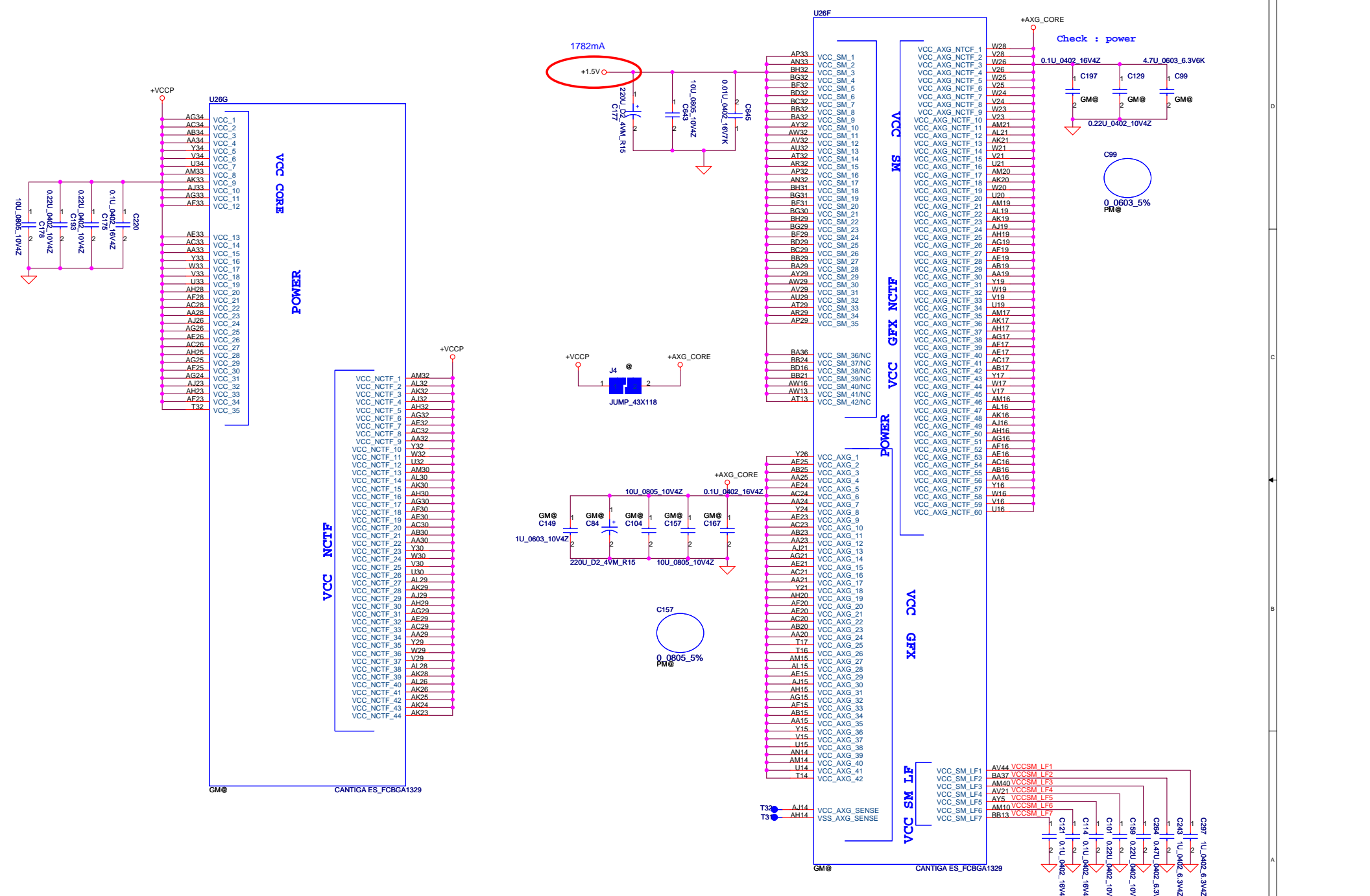
CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The iTPM Host Interface is enable 1 = The iTPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0=(TLS)chipset suite with no confidentiality 1=(TLS)chipset suite with confidentiality
CFG8	Reserved
CFG9 (PCIe Graphics Lane Reversal)	0 = Reverse Lane,15->0, 14->1 1 = Normal Operation, Lane Number in order *
CFG10 (PCIe Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse Lane
CFG20 (PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operational. 1 = PCIe/SDVO are operating simu. *



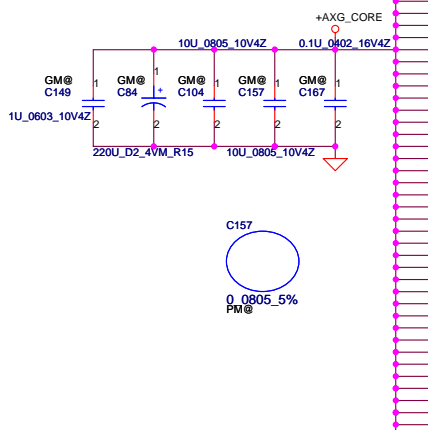
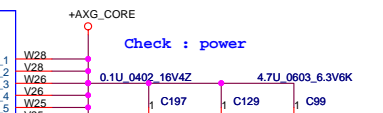
PCIe MTX GRX P3	C670	1	2	GM@ 0.1U 0402 10V7K	TMDS_B_CLK <23>
PCIe MTX GRX N3	C674	1	2	GM@ 0.1U 0402 10V7K	TMDS_B_CLK# <23>
PCIe MTX GRX P2	C669	1	2	GM@ 0.1U 0402 10V7K	TMDS_B_DATA0 <23>
PCIe MTX GRX N2	C673	1	2	GM@ 0.1U 0402 10V7K	TMDS_B_DATA0# <23>
PCIe MTX GRX P1	C662	1	2	GM@ 0.1U 0402 10V7K	TMDS_B_DATA1 <23>
PCIe MTX GRX N1	C663	1	2	GM@ 0.1U 0402 10V7K	TMDS_B_DATA1# <23>
PCIe MTX GRX P0	C658	1	2	GM@ 0.1U 0402 10V7K	TMDS_B_DATA2 <23>
PCIe MTX GRX N0	C661	1	2	GM@ 0.1U 0402 10V7K	TMDS_B_DATA2# <23>
PCIe GTX C_MRX P3	R640	1	2	GM@ 0.1U 0402 5%	TMDS_B_HPD# <23>

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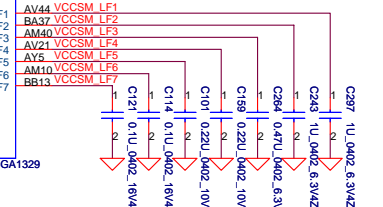




1782mA
+1.5V @



U26G	AG34	VCC_1	AE33	VCC_13	AM32	VCC_NCTF_1	AM32	VCC_NCTF_1	Y26	VCC_AXG_1
	AC34	VCC_2	AC33	VCC_14	AL32	VCC_NCTF_2	AL32	VCC_NCTF_2	AE25	VCC_AXG_2
	AB34	VCC_3	AC34	VCC_15	AK32	VCC_NCTF_3	AK32	VCC_NCTF_3	AB25	VCC_AXG_3
	AA34	VCC_4	Y33	VCC_16	AH32	VCC_NCTF_4	AH32	VCC_NCTF_4	AA25	VCC_AXG_4
	Y34	VCC_5	W33	VCC_17	AG32	VCC_NCTF_5	AG32	VCC_NCTF_5	AC24	VCC_AXG_5
	U34	VCC_6	V33	VCC_18	AE32	VCC_NCTF_6	AE32	VCC_NCTF_6	AA24	VCC_AXG_6
	U34	VCC_7	U33	VCC_19	AC32	VCC_NCTF_7	AC32	VCC_NCTF_7	Y24	VCC_AXG_8
	AM33	VCC_8	U34	VCC_20	AE32	VCC_NCTF_8	AE32	VCC_NCTF_8	AE23	VCC_AXG_9
	AK33	VCC_9	AF28	VCC_21	AA32	VCC_NCTF_9	AA32	VCC_NCTF_9	AB23	VCC_AXG_10
	AM33	VCC_10	AC28	VCC_22	Y32	VCC_NCTF_10	Y32	VCC_NCTF_10	AA23	VCC_AXG_12
	AC33	VCC_11	AA28	VCC_23	U32	VCC_NCTF_11	U32	VCC_NCTF_11	AJ21	VCC_AXG_13
	AE33	VCC_12	AH28	VCC_24	AM30	VCC_NCTF_12	AM30	VCC_NCTF_12	AE21	VCC_AXG_14
			AF28	VCC_25	AL30	VCC_NCTF_13	AL30	VCC_NCTF_13	AC21	VCC_AXG_16
			AC28	VCC_26	AK30	VCC_NCTF_14	AK30	VCC_NCTF_14	AE21	VCC_AXG_18
			AA28	VCC_27	AH30	VCC_NCTF_15	AH30	VCC_NCTF_15	AA21	VCC_AXG_19
			AJ28	VCC_28	AF30	VCC_NCTF_16	AF30	VCC_NCTF_16	AE20	VCC_AXG_20
			AC28	VCC_29	AE30	VCC_NCTF_17	AE30	VCC_NCTF_17	AC20	VCC_AXG_21
			AH28	VCC_30	AA30	VCC_NCTF_18	AA30	VCC_NCTF_18	AB20	VCC_AXG_22
			AC28	VCC_31	Y30	VCC_NCTF_19	Y30	VCC_NCTF_19	AA20	VCC_AXG_24
			AA28	VCC_32	U30	VCC_NCTF_20	U30	VCC_NCTF_20	T17	VCC_AXG_25
			AJ28	VCC_33	Y30	VCC_NCTF_21	Y30	VCC_NCTF_21	T16	VCC_AXG_26
			AC28	VCC_34	U30	VCC_NCTF_22	U30	VCC_NCTF_22	AM15	VCC_AXG_27
			AH28	VCC_35	U30	VCC_NCTF_23	U30	VCC_NCTF_23	AL15	VCC_AXG_28
			AC28			VCC_NCTF_24		VCC_NCTF_24	AE15	VCC_AXG_29
			AA28			VCC_NCTF_25		VCC_NCTF_25	AJ15	VCC_AXG_30
			AJ28			VCC_NCTF_26		VCC_NCTF_26	AH15	VCC_AXG_31
			AC28			VCC_NCTF_27		VCC_NCTF_27	AG15	VCC_AXG_32
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			AA28			VCC_NCTF_34		VCC_NCTF_34	AM14	VCC_AXG_39
			AJ28			VCC_NCTF_35		VCC_NCTF_35	U14	VCC_AXG_40
			AC28			VCC_NCTF_36		VCC_NCTF_36	U14	VCC_AXG_41
			AA28			VCC_NCTF_37		VCC_NCTF_37	T14	VCC_AXG_42
			AJ28			VCC_NCTF_38		VCC_NCTF_38		
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			AA28			VCC_NCTF_40		VCC_NCTF_40		
			AJ28			VCC_NCTF_41		VCC_NCTF_41		
			AC28			VCC_NCTF_42		VCC_NCTF_42		
			AA28			VCC_NCTF_43		VCC_NCTF_43		
			AJ28			VCC_NCTF_44		VCC_NCTF_44		
			AC28							
			AA28							
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			AC28							
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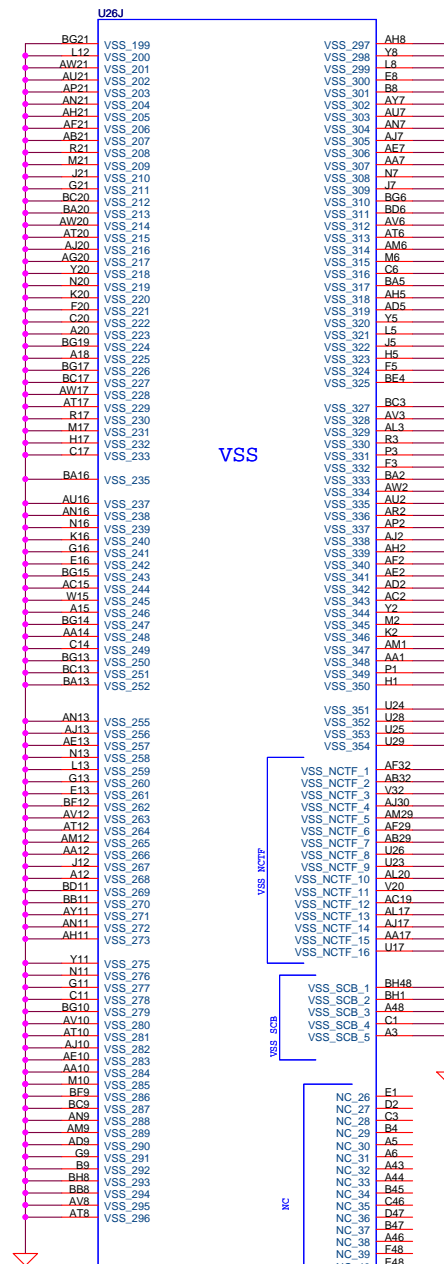
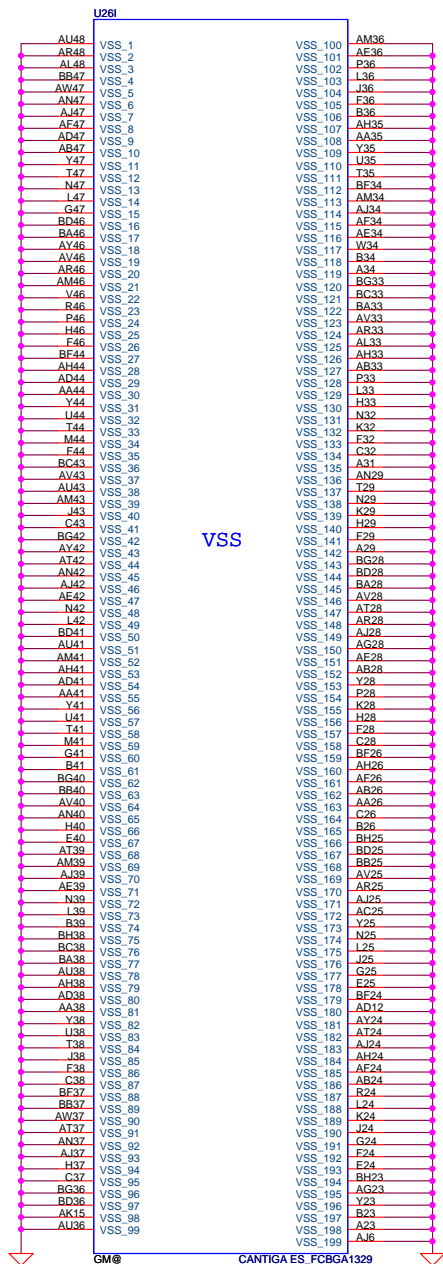
Crestline GMCH (5/6)-VCC

JITRI_LA-414P

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Cantiga GMCH (6/6)-GND			
Size	Document Number	Rev	
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Date:	Friday, April 18, 2008	Sheet	13 of 52

<9> DDR_A_DQS#[0..7]

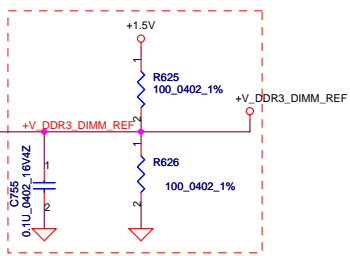
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<9> DDR_A_DM[0..7]

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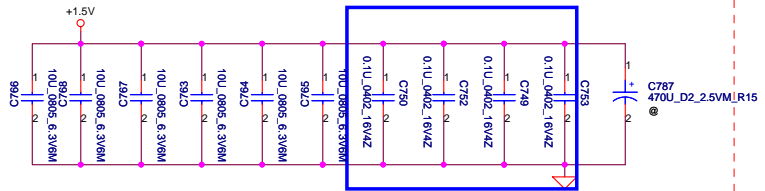
<9> DDR_A_MA[0..14]

<15> +V_DDR3_DIMM_REF

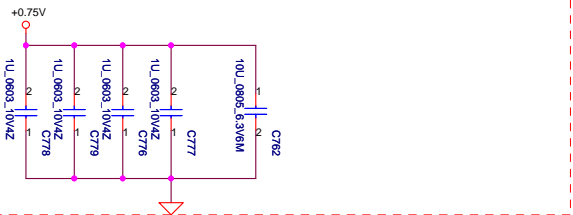


Layout Note:
Place near JP4

Layout Note: Place these 4 Caps near Command and Control-signals of DIMMA

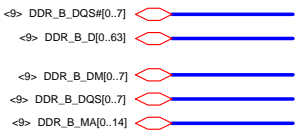


Layout Note:
Place near JP4.203 & JP4.204



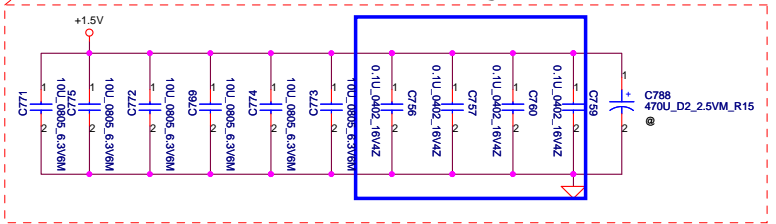
DDR3 SO-DIMM A REVERSE

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				Montevina UMA DDR3	
				Date:	Friday, May 02, 2008
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				Rev	1.0

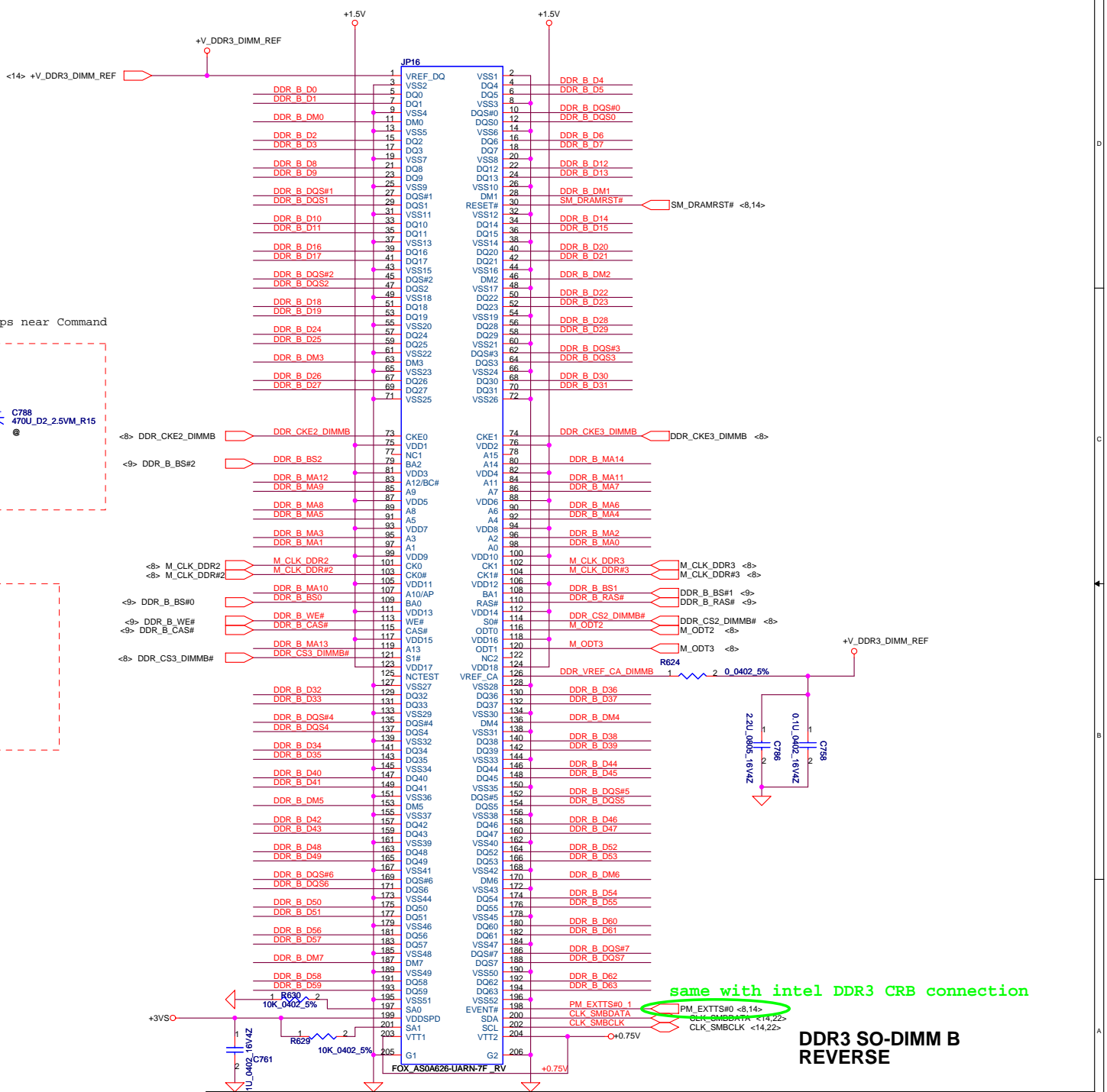
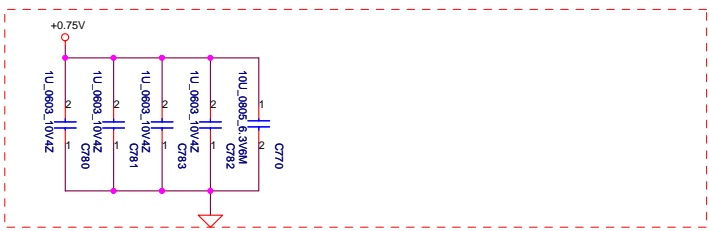


Layout Note:
Place near JP5

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA



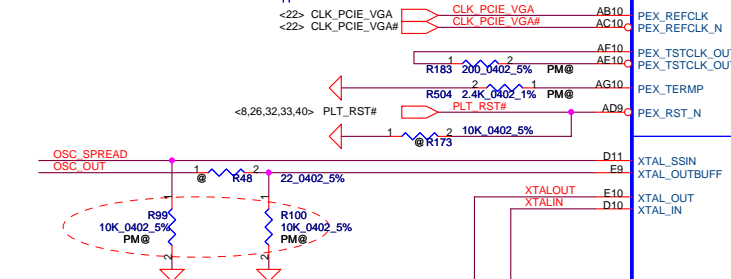
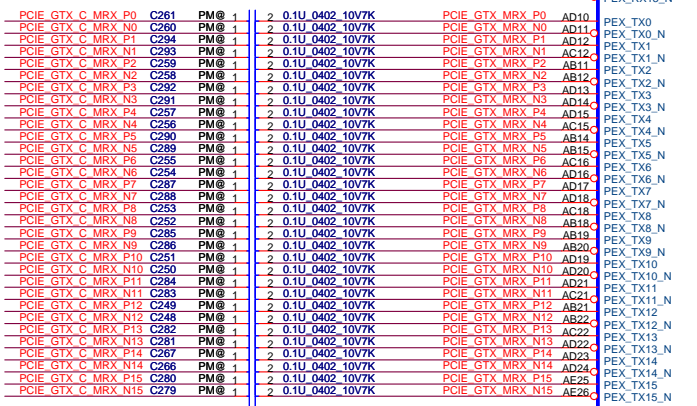
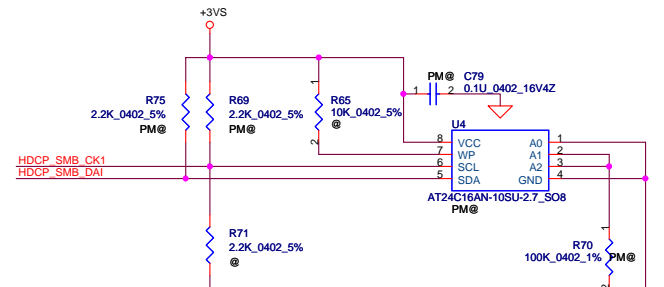
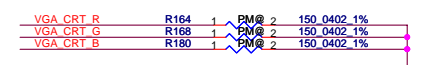
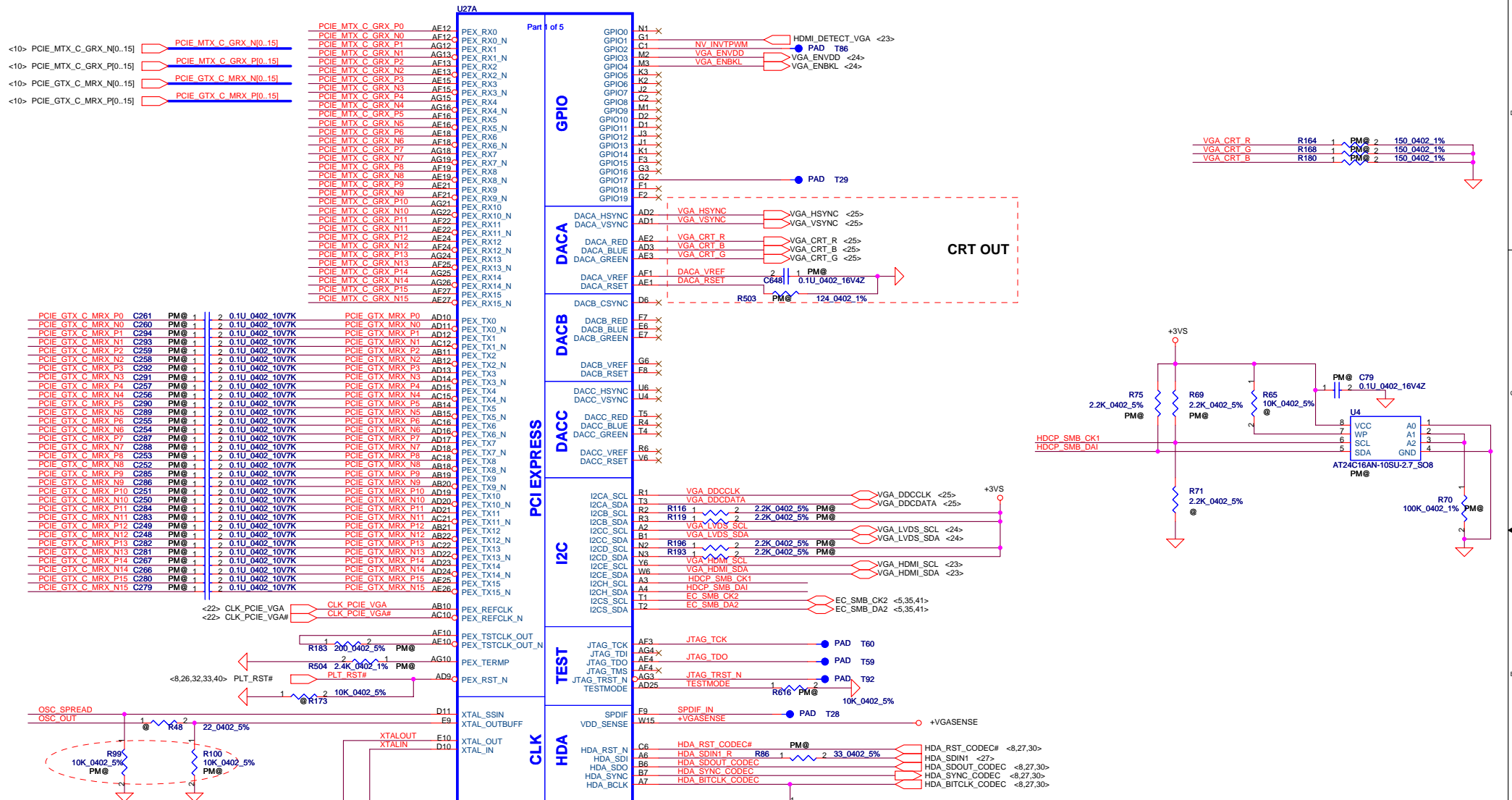
Layout Note:
Place near JP5.203 & JP5.204



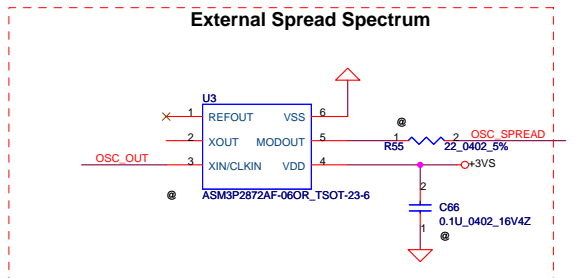
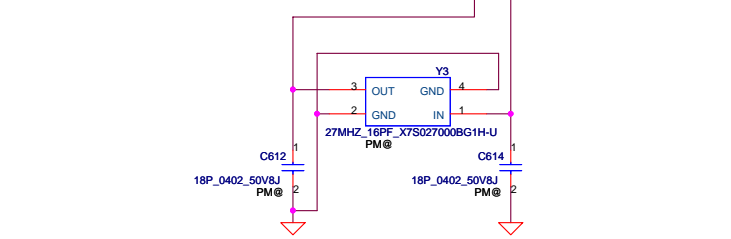
same with intel DDR3 CRB connection

DDR3 SO-DIMM B REVERSE

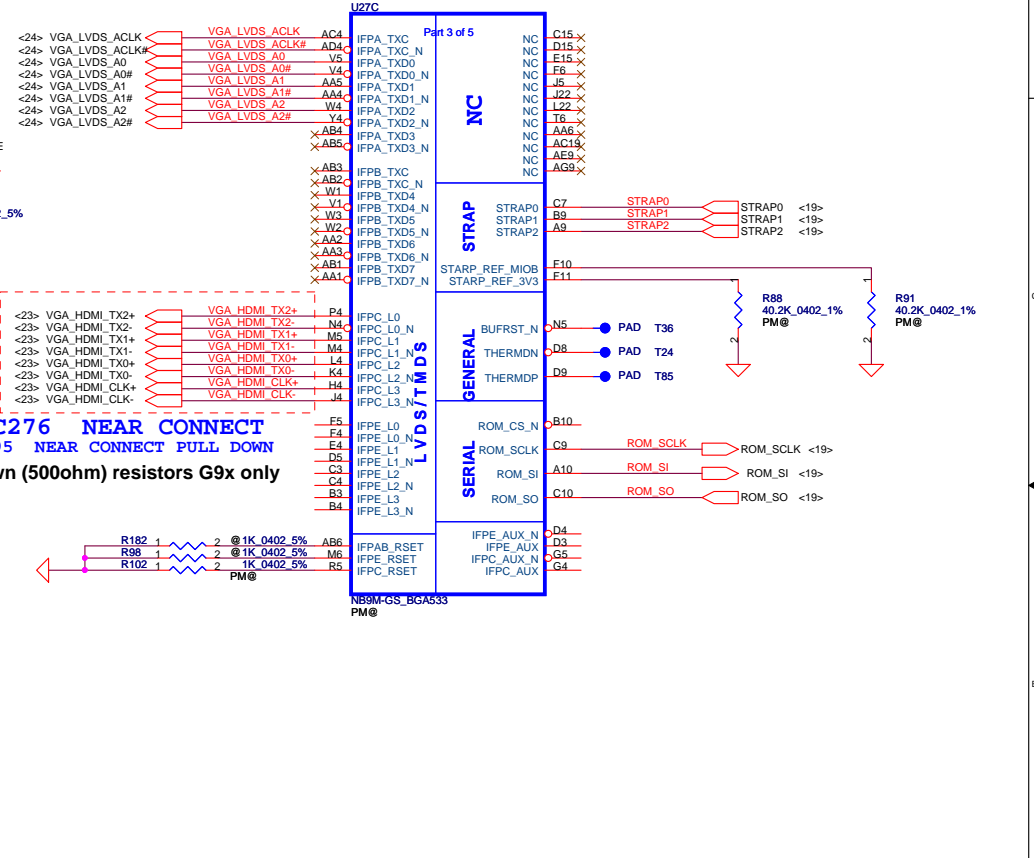
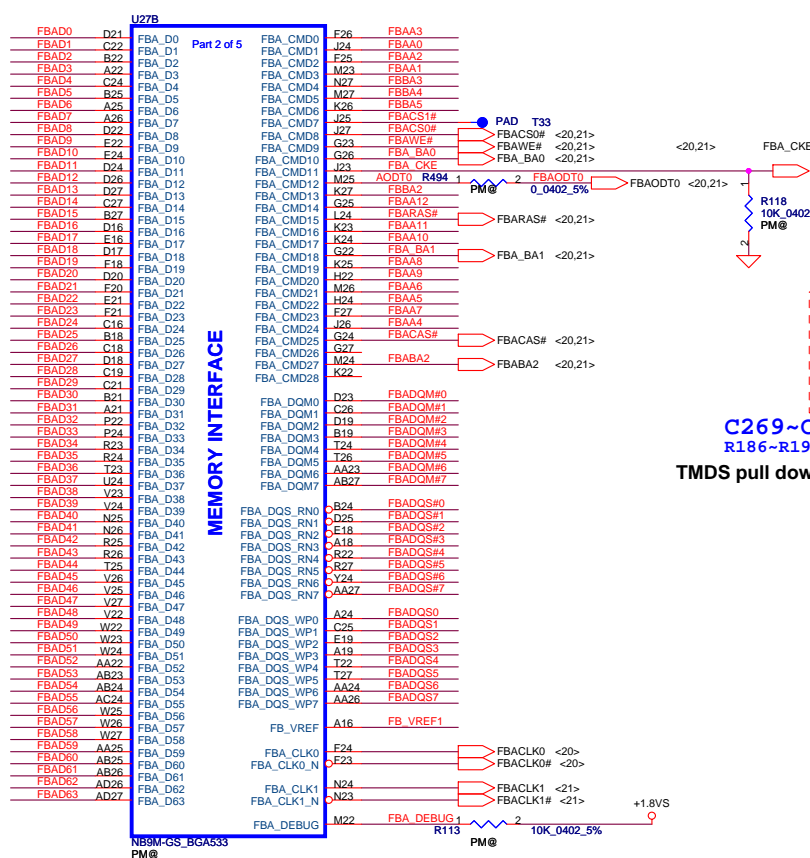
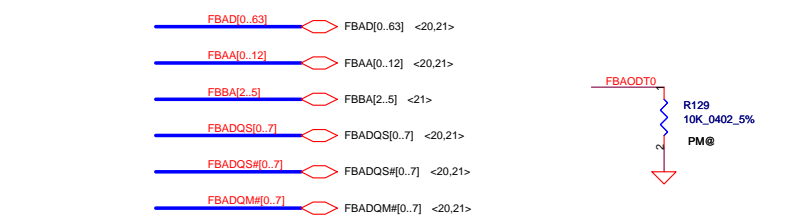
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				DDR3III-SODIMM SLOT2	
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If External Spread Spectrum not stuff than stuff resistor



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Issued Date	2007/10/15	Deciphered Date	2008/10/15	NB9M-GS PCIe, LVDS, GPIO, CLK	
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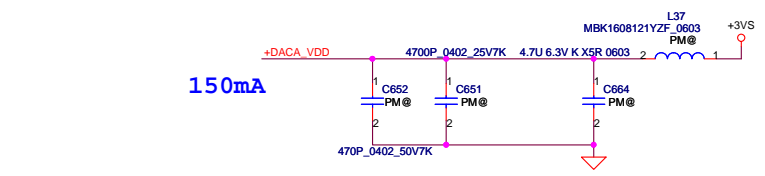
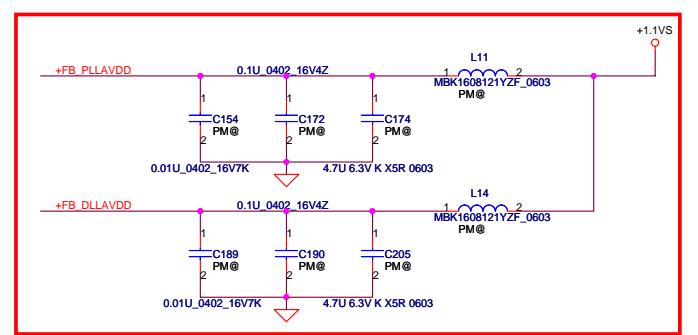
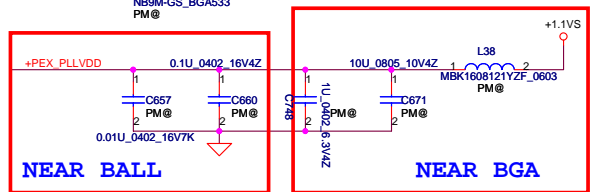
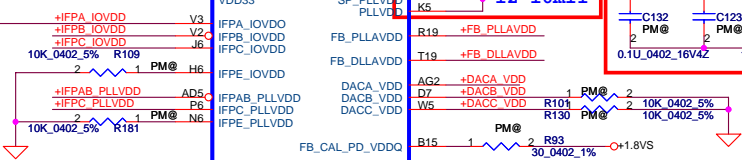
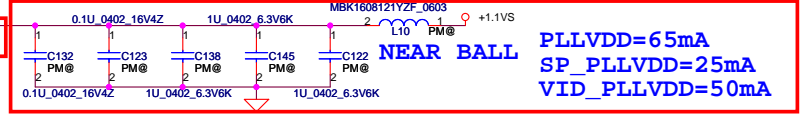
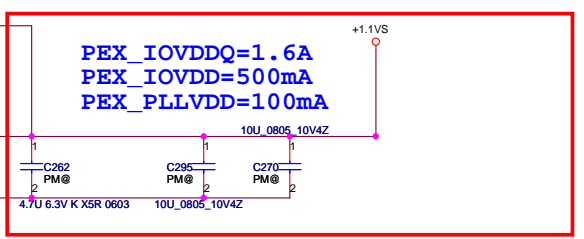
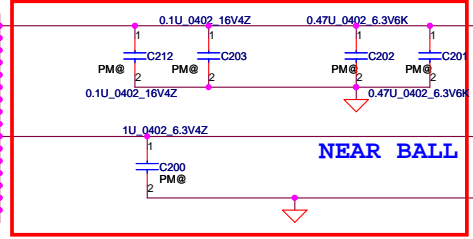
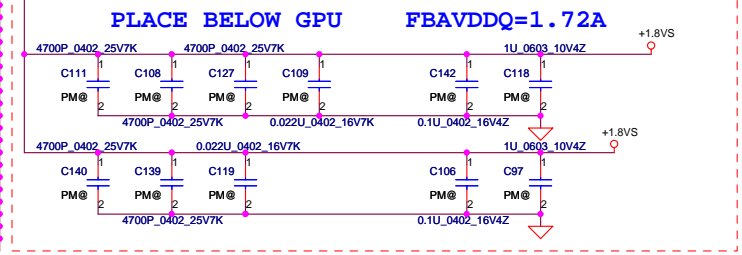
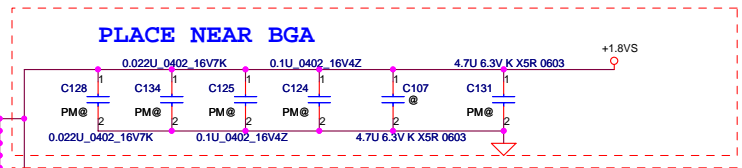
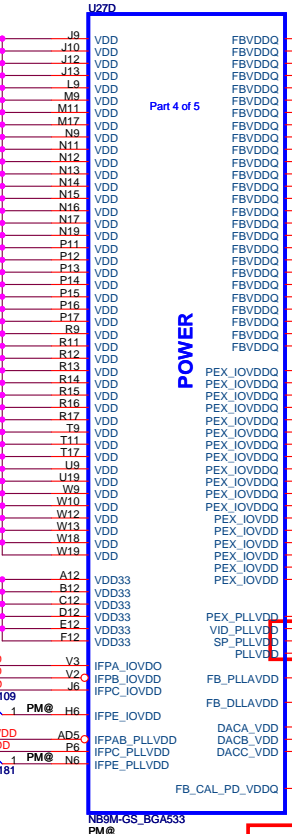
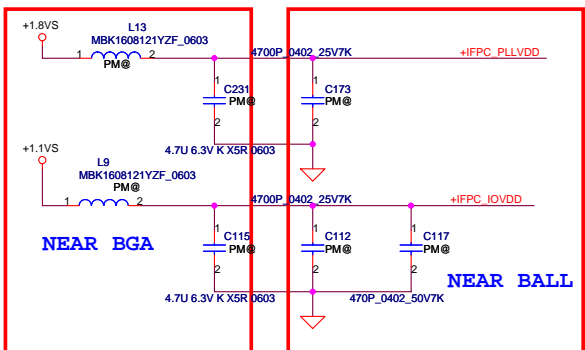
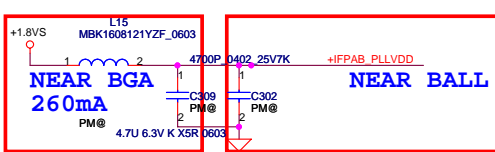
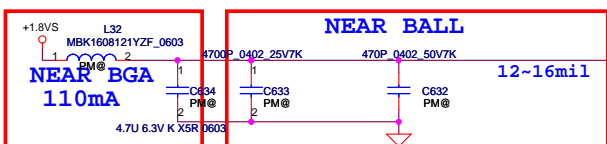
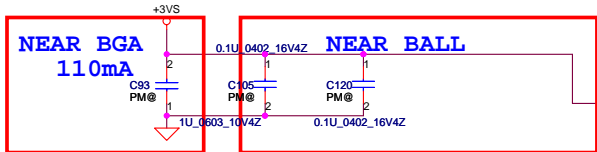
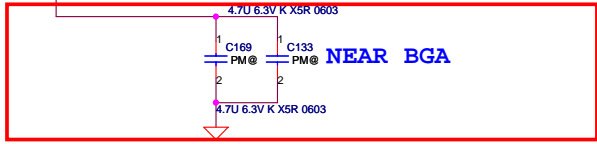
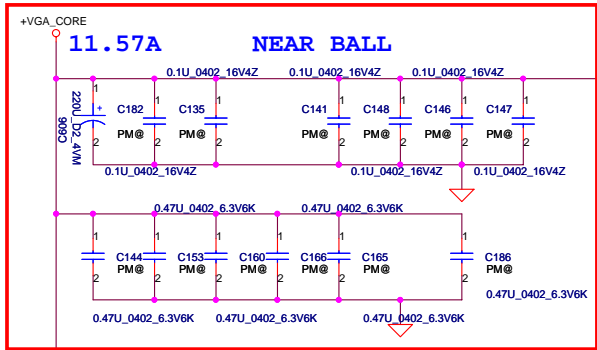


C269~C276 NEAR CONNECT
R186-R195 NEAR CONNECT PULL DOWN
TMDs pull down (500ohm) resistors G9x only

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		2008/10/15

Compal Electronics, Inc.		
NB9M-GS Memory		
Title	NB9M-GS Memory	
Size B	Document Number	Rev
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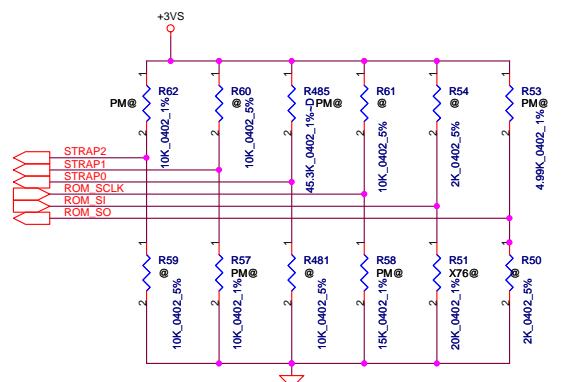
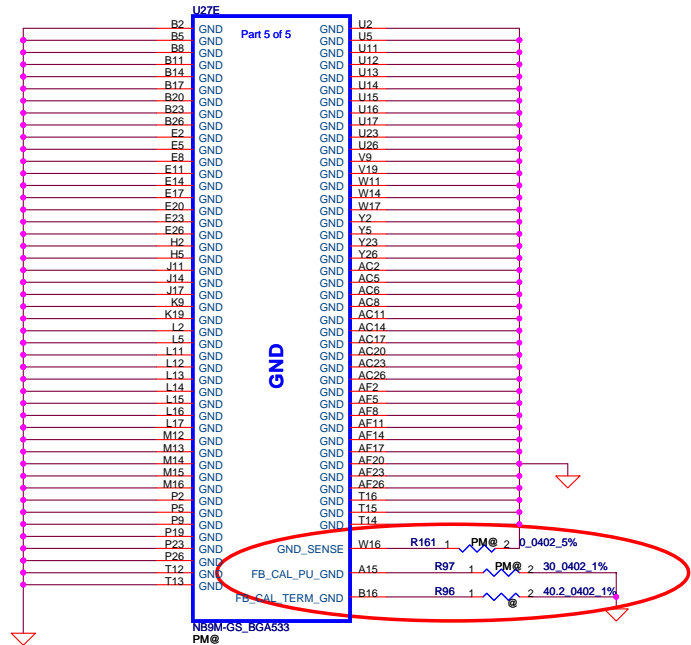
A total of 8 signals are required for GB1 strapping this includes

2 reference signals

6 physical strapping pins

4 logical strapping bits

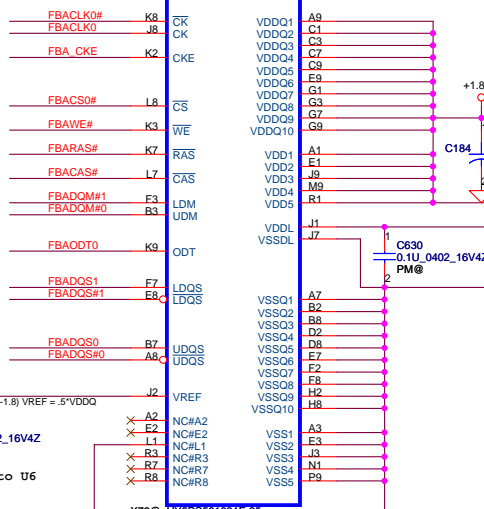
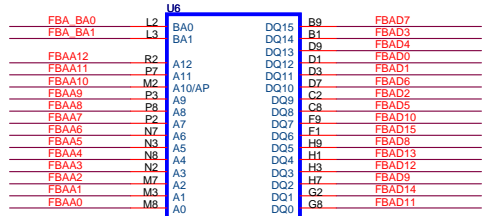
A total of 24 logical strapping bits are available



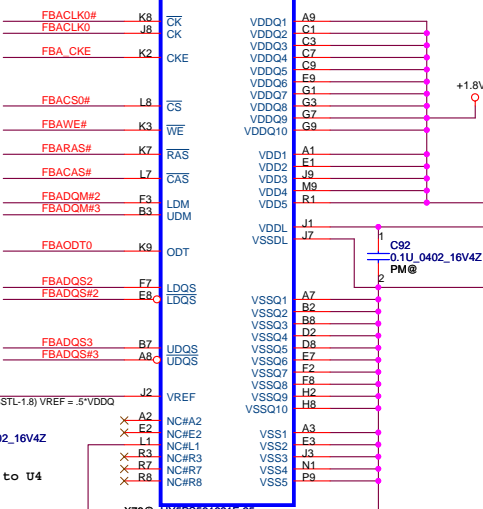
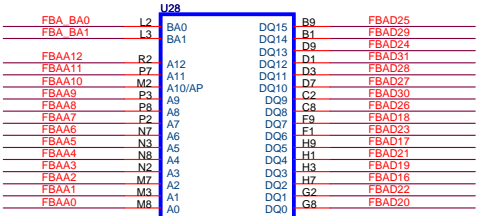
GB1 Family GPU Strap Options

GPU	FB Memory	ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0	
NB9M-GS (0x06E9)	Samsung	16Mx16(1)	PU 5K	PD 15K	PD 10K	PD 10K	PU 45K	
		32Mx16(5)	PU 5K	PD 15K	PD 30K	PD 10K	PD 10K	PU 45K
	Hynix	16Mx16(3)	PU 5K	PD 15K	PD 20K	PD 10K	PD 10K	PU 45K
		32Mx16(7)	PU 5K	PD 15K	PD 45K	PD 10K	PD 10K	PU 45K
	Qimonda	16Mx16(2)	PU 5K	PD 15K	PD 15K	PD 10K	PD 10K	PU 45K
		32Mx16(6)	PU 5K	PD 15K	PD 35K	PD 10K	PD 10K	PU 45K

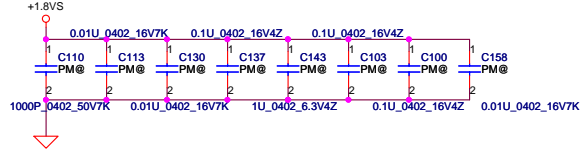
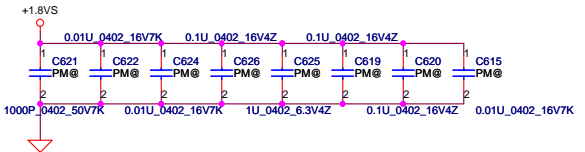
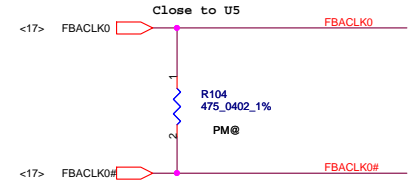
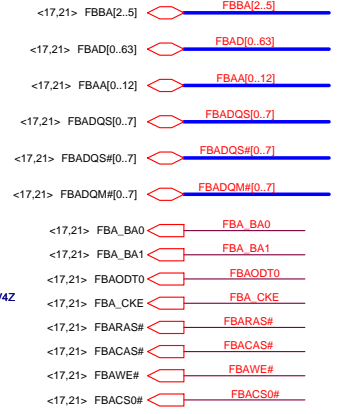
Component	Manufacturer	Compal PN	Compal X76 PN
DDR2 VRAM (32M*16)	Hynix	SA000012G30	X7611338L04
	Qimonda	SA00001YF10	X7611338L05
	Samsung	SA00001KH10	X7611338L06



DDR2 BGA MEMORY

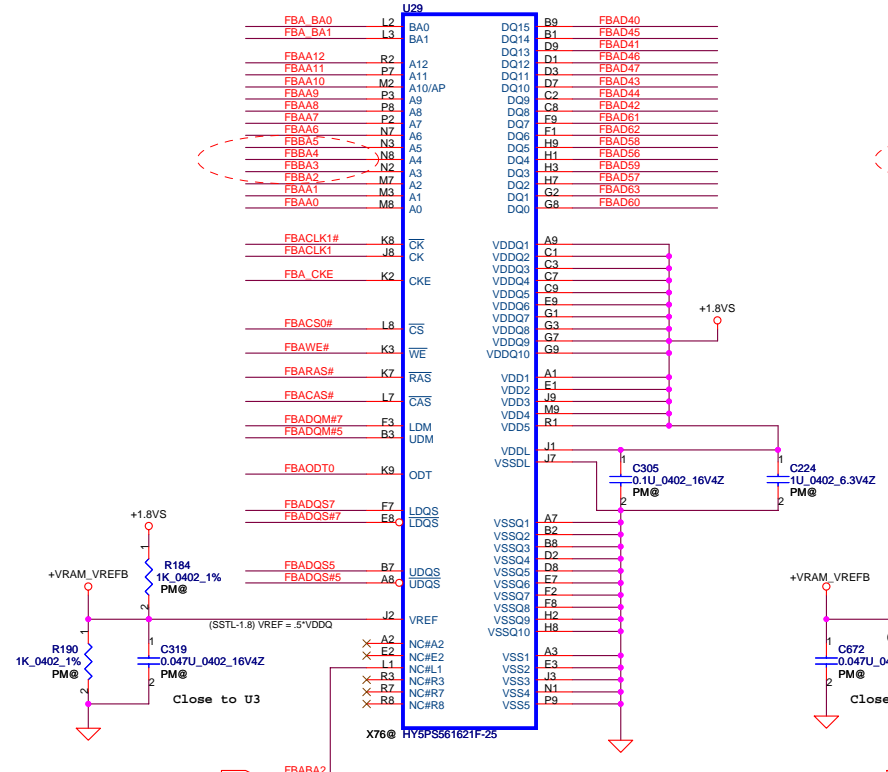


DDR2 BGA MEMORY

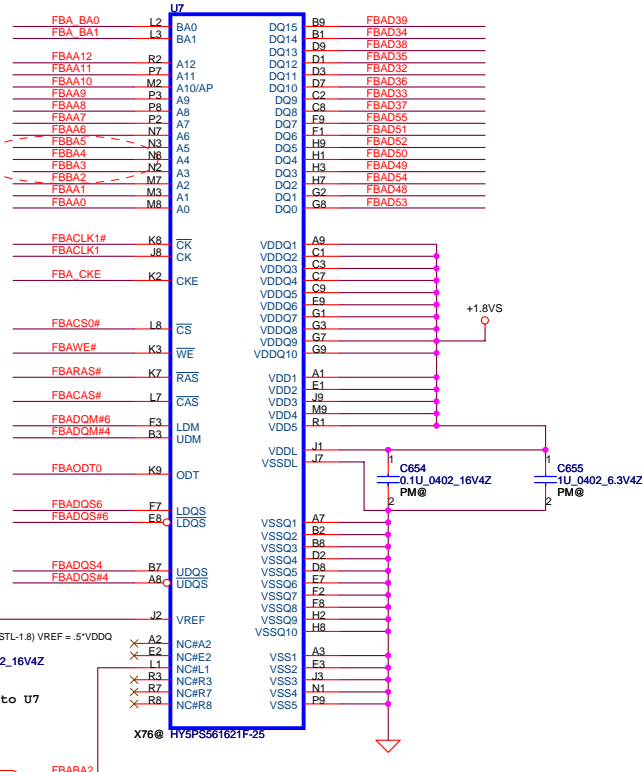


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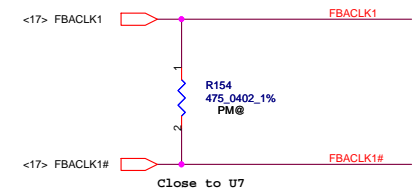
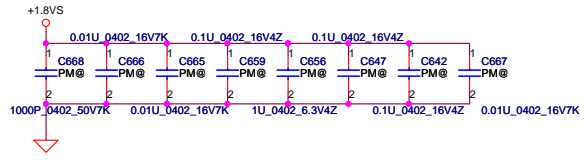
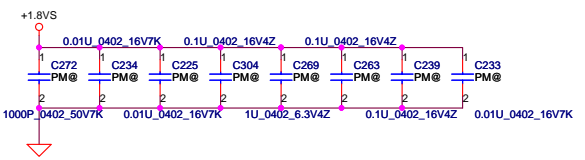
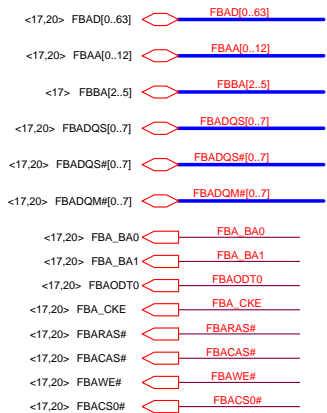
Compal Electronics, Inc. VRAM DDRA		
Title	Size	Rev
	Custom	0.1
Date:	Document Number	
Friday, May 02, 2008	JITRI_LA-4141P	
		Sheet 20 of 52



DDR2 BGA MEMORY



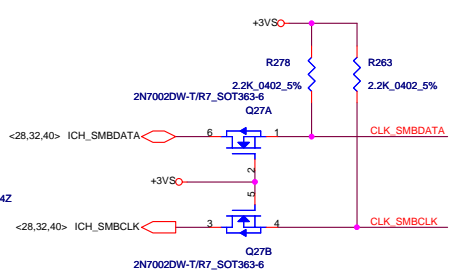
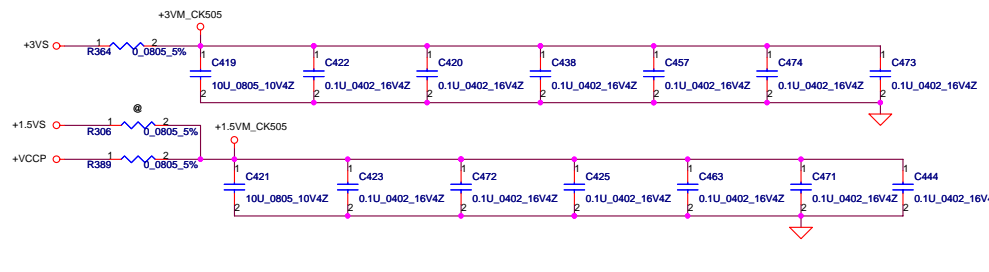
DDR2 BGA MEMORY



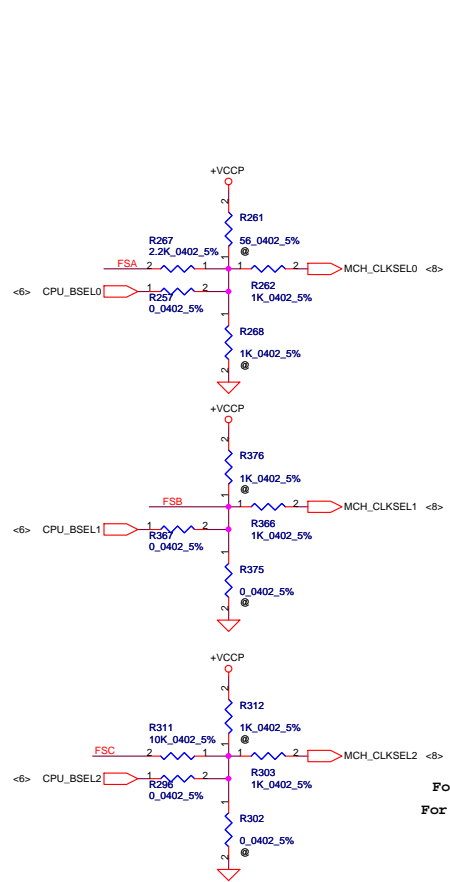
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Issued Date	2007/10/15	Deciphered Date
		2008/10/15
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Title			Compal Electronics, Inc.	
			VRAM DDRB	
Size	Document Number		Rev	
Custom	JITRI_LA-4141P		0.1	
Date:	Friday, May 02, 2008	Sheet	21	of 52

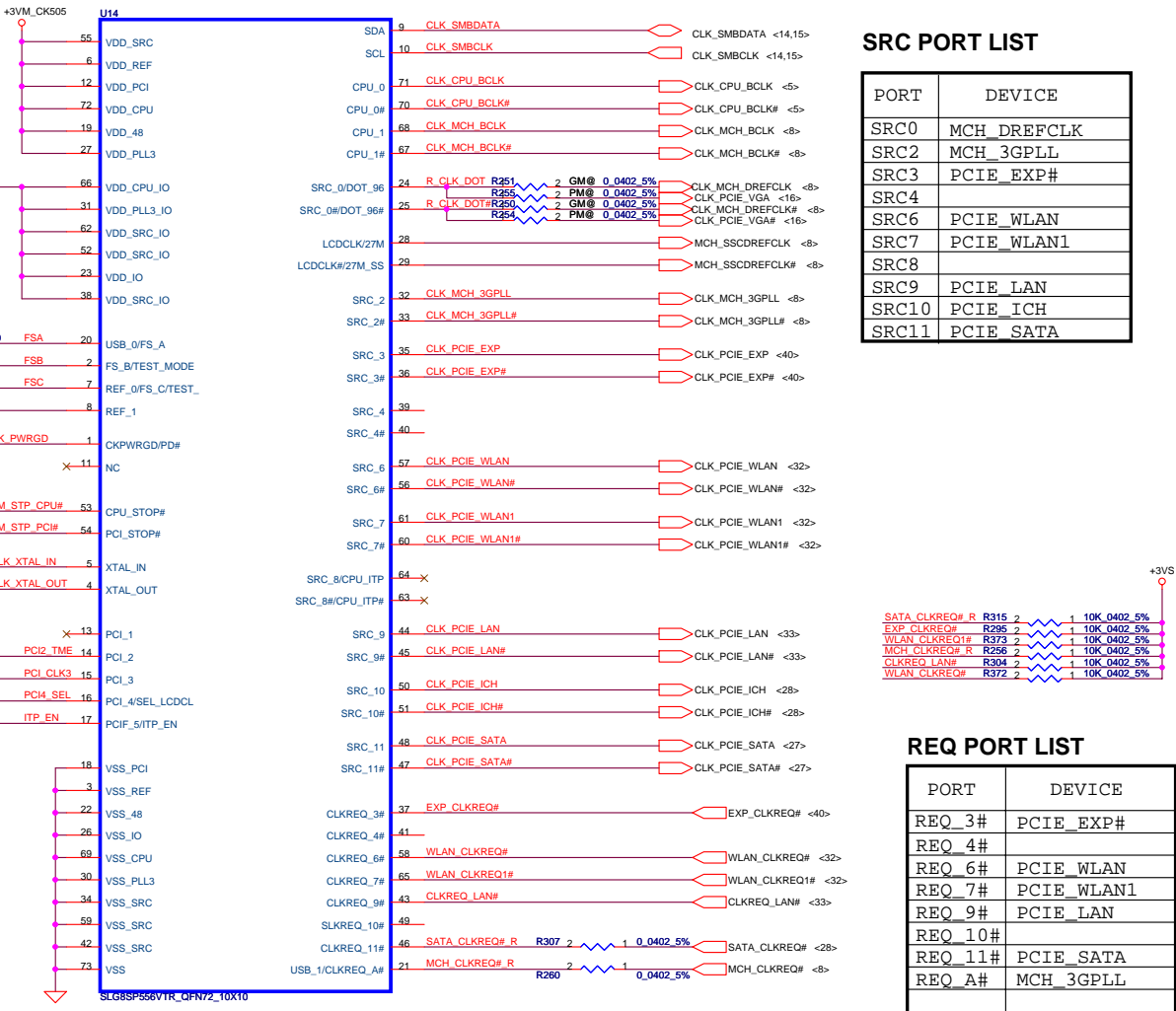
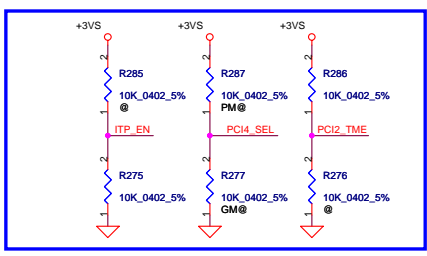
FSC	FSB	FSA	CPU	SRC	PCI	REF	DOT_96	USB
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz	MHz	MHz	MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1						
Reserved								



SA000020K00 (Silego : SLG8SP556VTR)
SA000020H00 (ICS : ICS9LPRS387AKLFT)



For ITP_EN, 0 = SRC8/SRC8#; 1 = ITP/ITP#
For PCI4_SEL, 0 = Pin24/25 : DOT96 / DOT96#
Pin28/29 : LCDCLK / LCDCLK#
1 = Pin24/25 : SRC_0 / SRC_0#
Pin28/29 : 27M/27M_SS

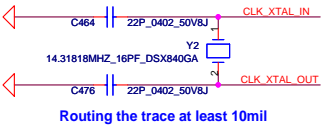


SRC PORT LIST

PORT	DEVICE
SRC0	MCH_DREFCLK
SRC2	MCH_3GPLL
SRC3	PCI_E_EXP#
SRC4	
SRC6	PCI_E_WLAN
SRC7	PCI_E_WLAN1
SRC8	
SRC9	PCI_E_LAN
SRC10	PCI_E_ICH
SRC11	PCI_E_SATA

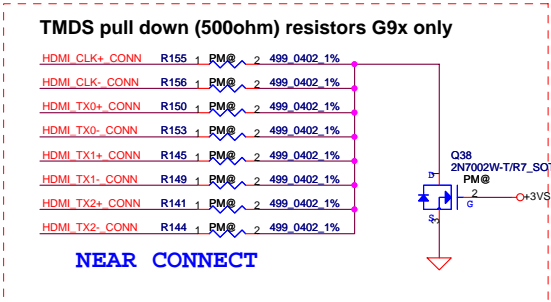
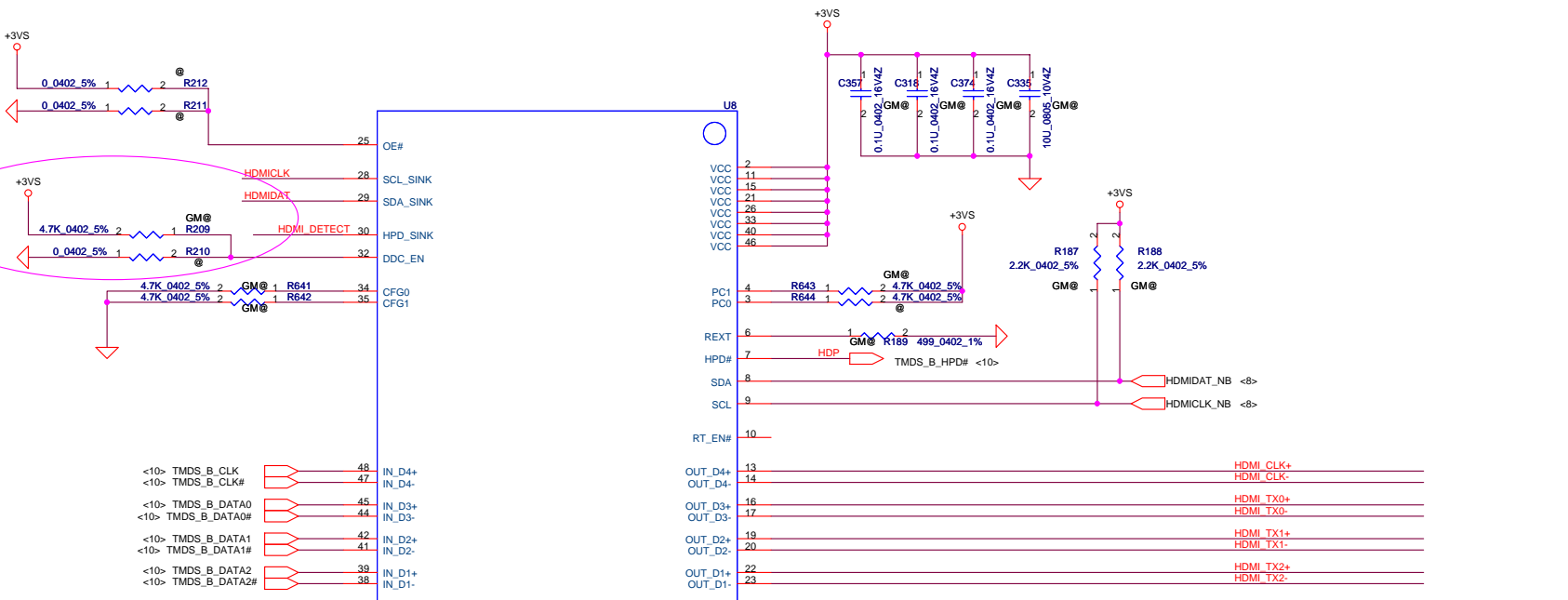
REQ PORT LIST

PORT	DEVICE
REQ_3#	PCI_E_EXP#
REQ_4#	
REQ_6#	PCI_E_WLAN
REQ_7#	PCI_E_WLAN1
REQ_9#	PCI_E_LAN
REQ_10#	
REQ_11#	PCI_E_SATA
REQ_A#	MCH_3GPLL

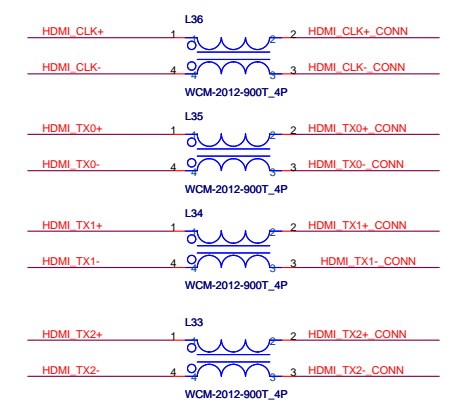


Routing the trace at least 10mil

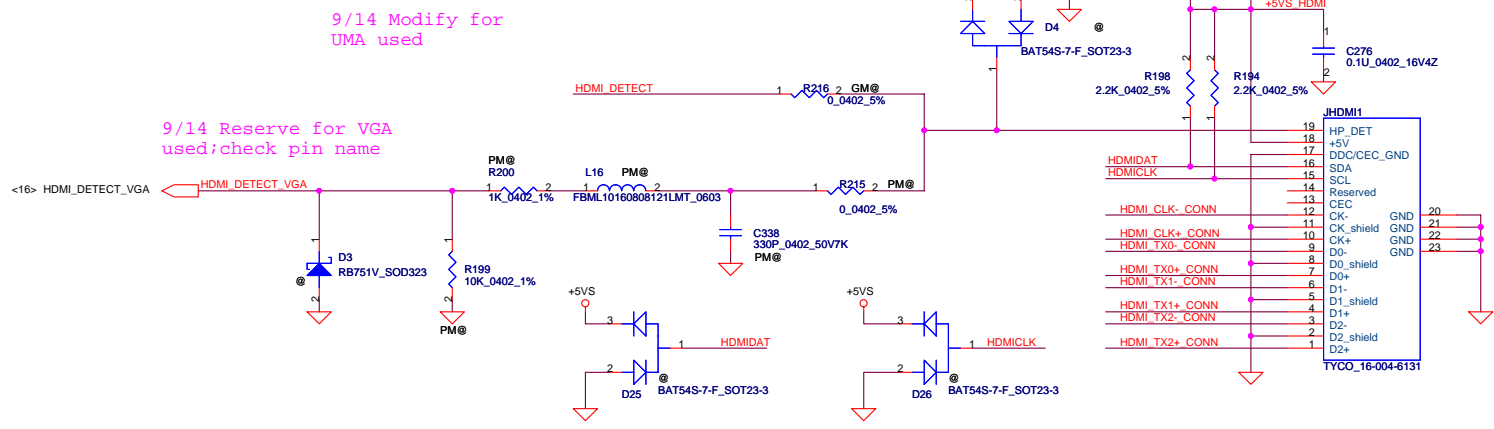
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Date: Monday, May 05, 2008		Sheet 22 of 52		



P/N:SA00002D700 (8101T)
P/N:SA00001U900



HDMI_CLK+	0_0402_5%	1	2	@	R645	HDMI_CLK+ CONN
HDMI_CLK-	0_0402_5%	1	2	@	R646	HDMI_CLK- CONN
HDMI_TX0+	0_0402_5%	1	2	@	R647	HDMI_TX0+ CONN
HDMI_TX0-	0_0402_5%	1	2	@	R648	HDMI_TX0- CONN
HDMI_TX1+	0_0402_5%	1	2	@	R649	HDMI_TX1+ CONN
HDMI_TX1-	0_0402_5%	1	2	@	R650	HDMI_TX1- CONN
HDMI_TX2+	0_0402_5%	1	2	@	R651	HDMI_TX2+ CONN
HDMI_TX2-	0_0402_5%	1	2	@	R652	HDMI_TX2- CONN



9/14 Modify for UMA used

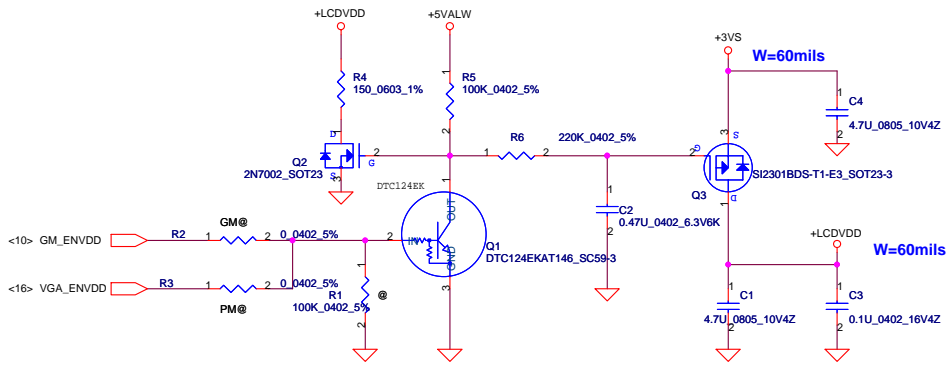
9/14 Reserve for VGA used;check pin name

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		2008/10/15

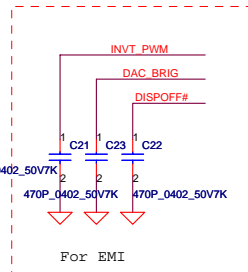
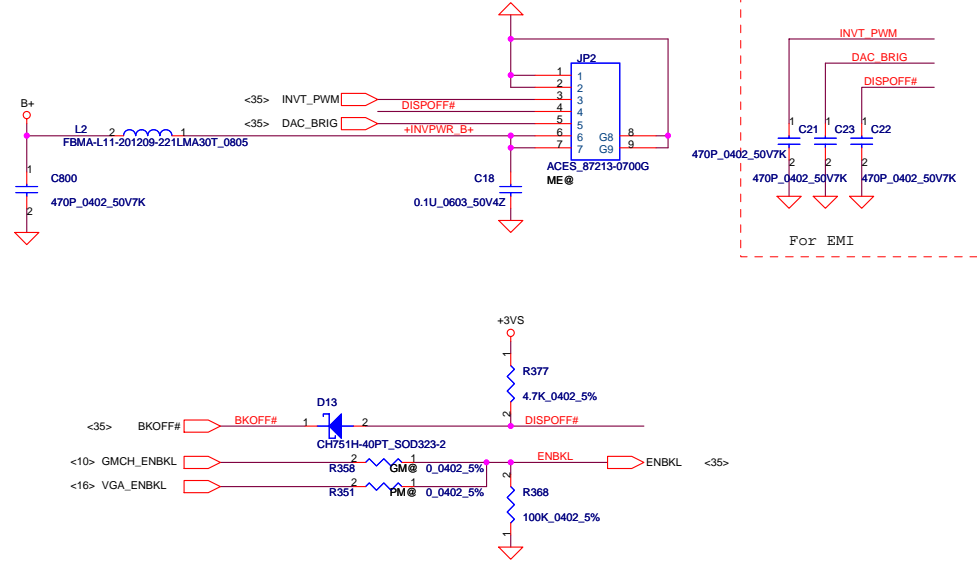
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Compal Electronics, Inc.		
Level shifter-CH7318		
Title		
Size	Document Number	Rev
	JITRI_LA-4141P	1.0
Date:	Friday, May 02, 2008	Sheet 23 of 52

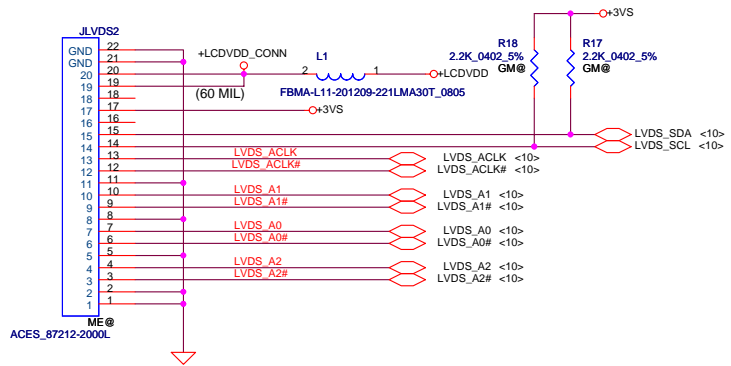
LCD POWER CIRCUIT



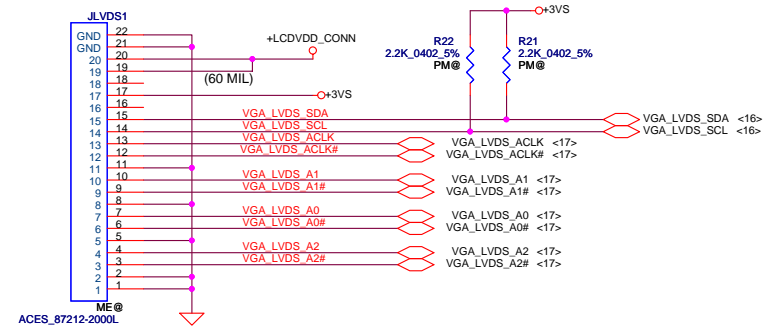
INVERTER Conn.



LCD/PANEL BD. Conn.



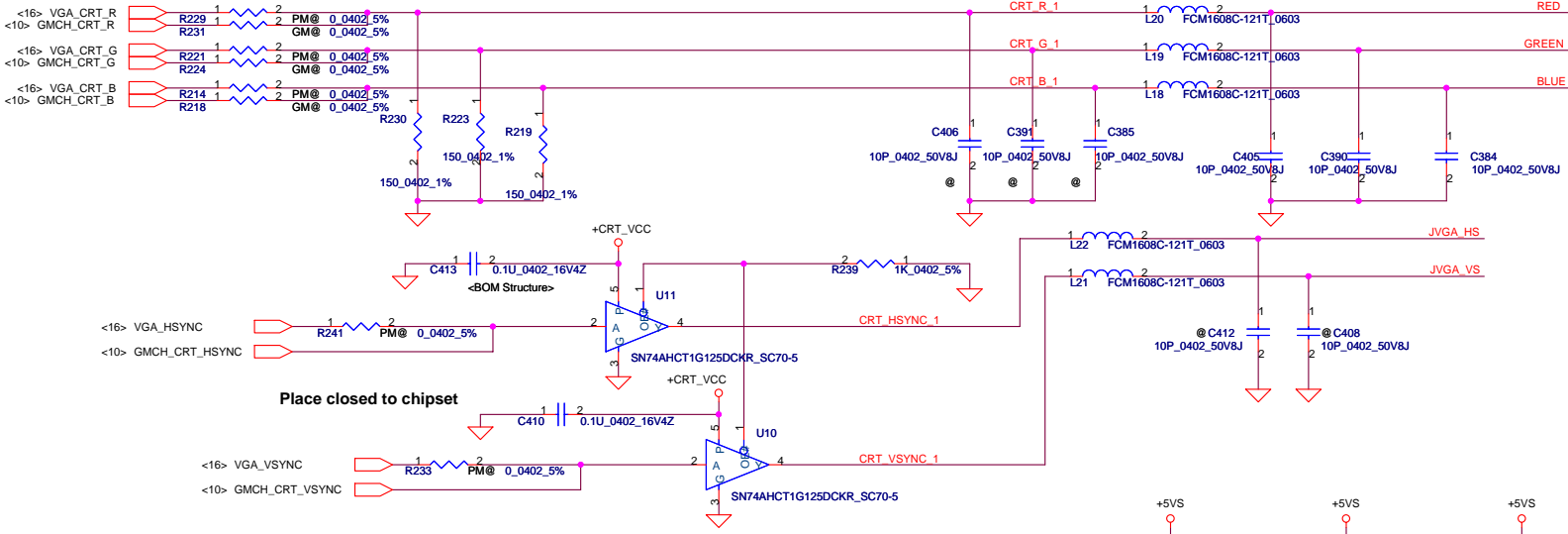
LCD/PANEL BD. Conn.



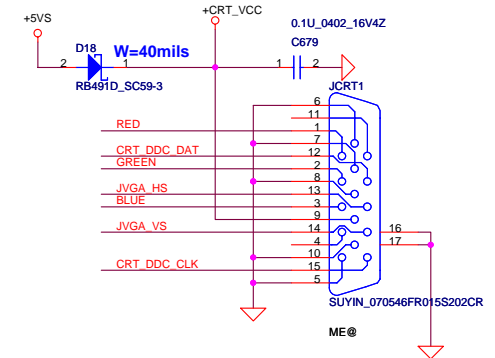
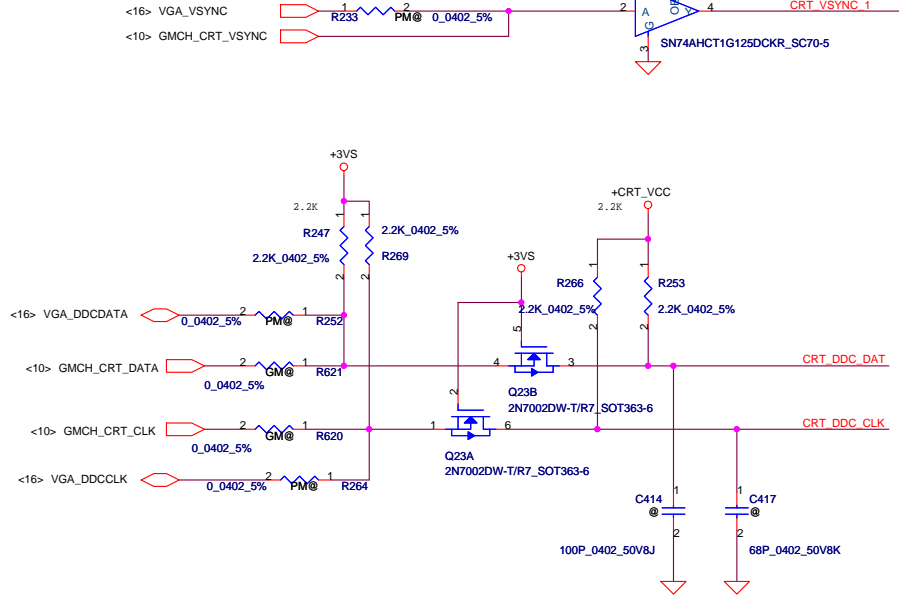
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				Size B	Document Number
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CRT Connector

Place closed to chipset

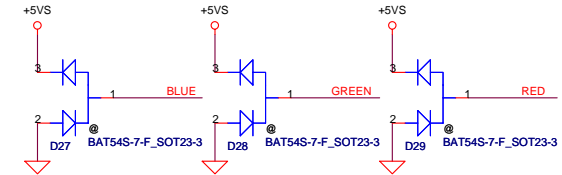


Place closed to chipset

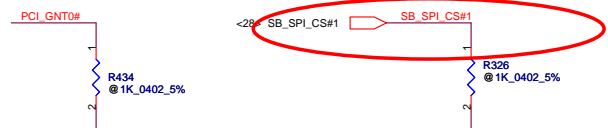
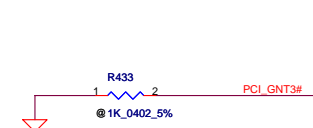
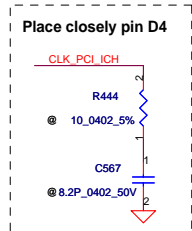
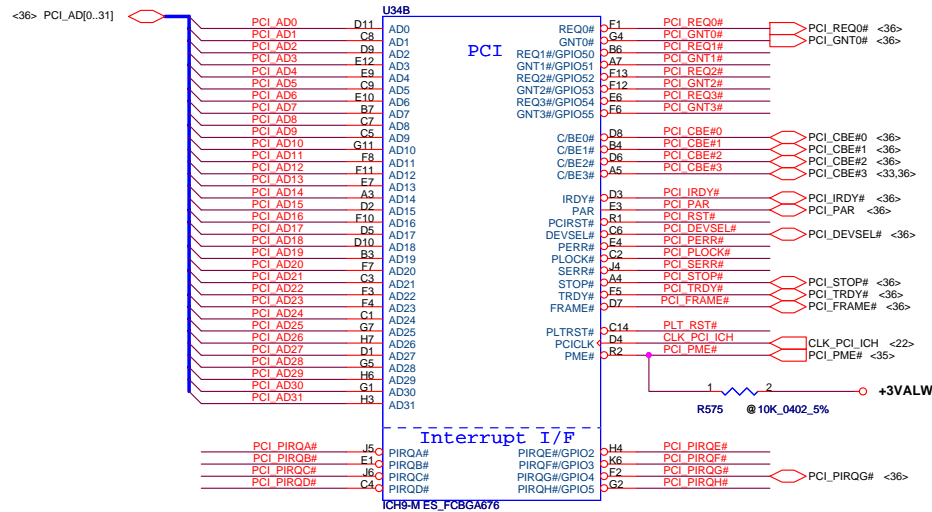
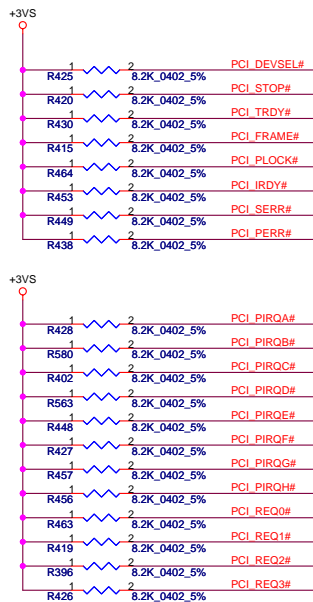


PIN ASSIGNMENT

D-SUB	FUNCTION
9	+CRT_VCC
1	RED
6	GND
2	GREEN
7, 5	GND
3	BLUE
8	GND
14	VSYNC
10	GND
13	HSYNC
11	SENSE
12	SM_DAT
15	SM_CLK
4	PIN4

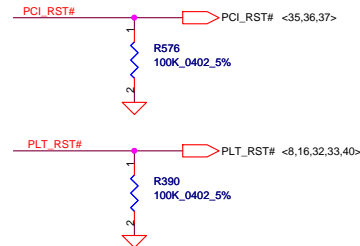


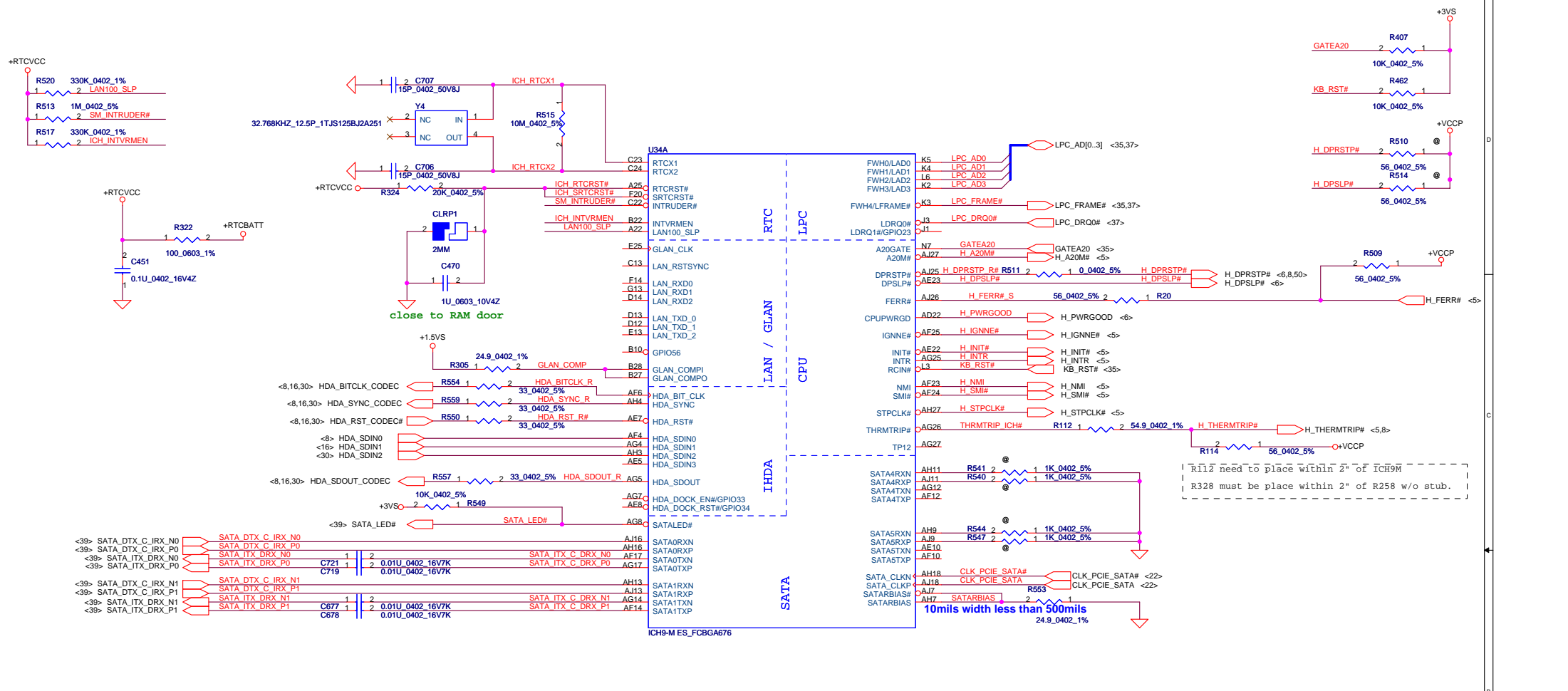
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			CRT & TV-OUT Connector	
Size	Document Number	Rev		
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A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*

Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC*

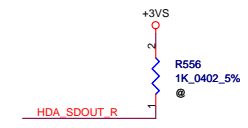




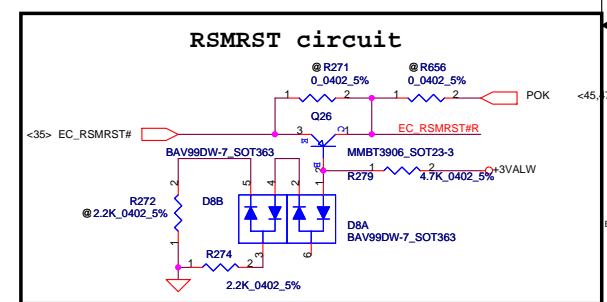
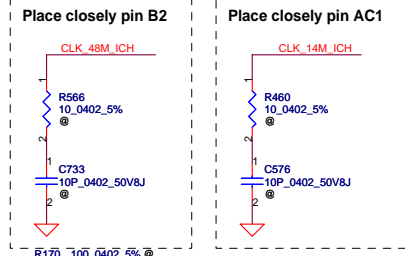
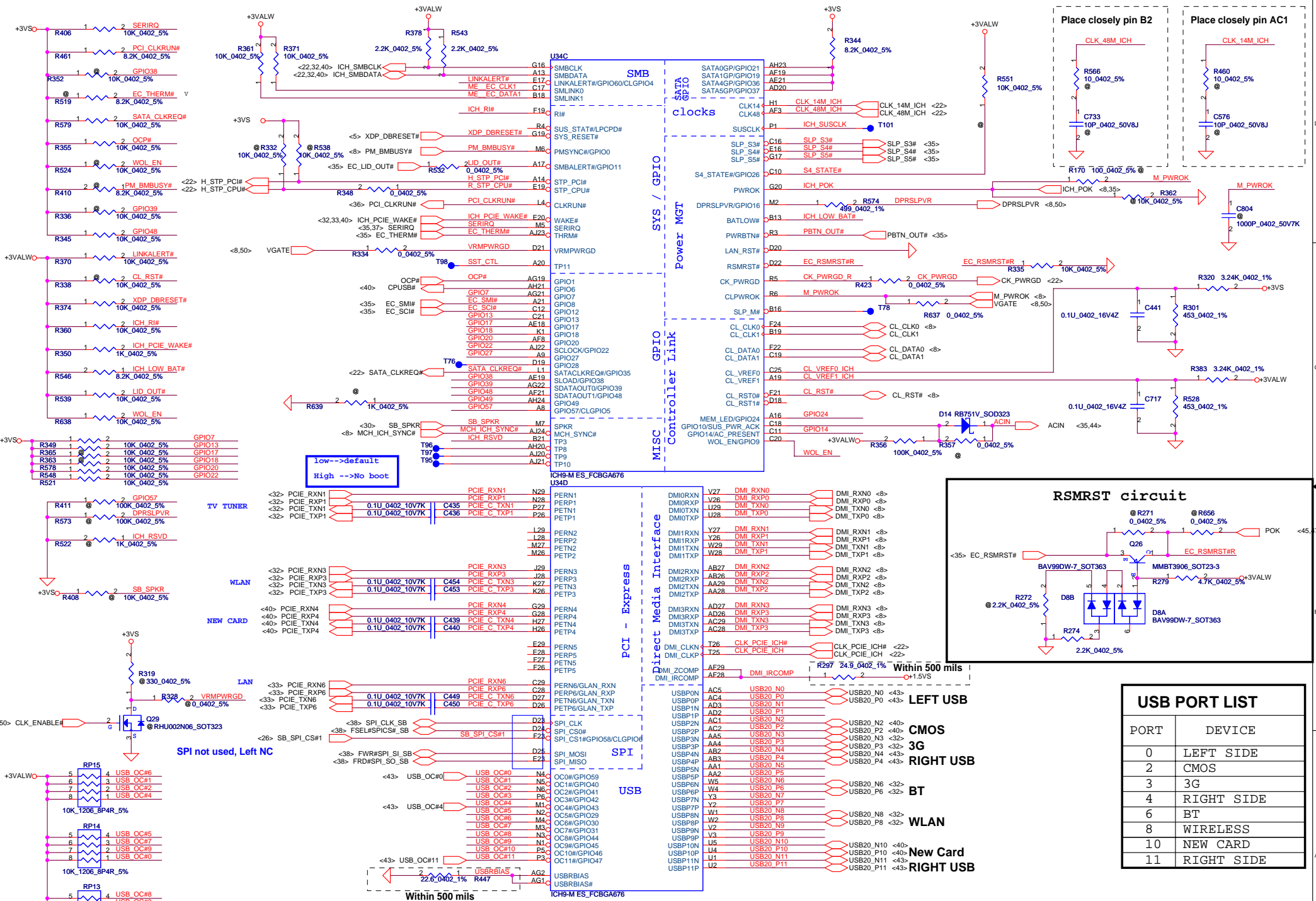
close to RAM door

R112 need to place within 2" of ICH9M
R328 must be place within 2" of R258 w/o stub.

Need check

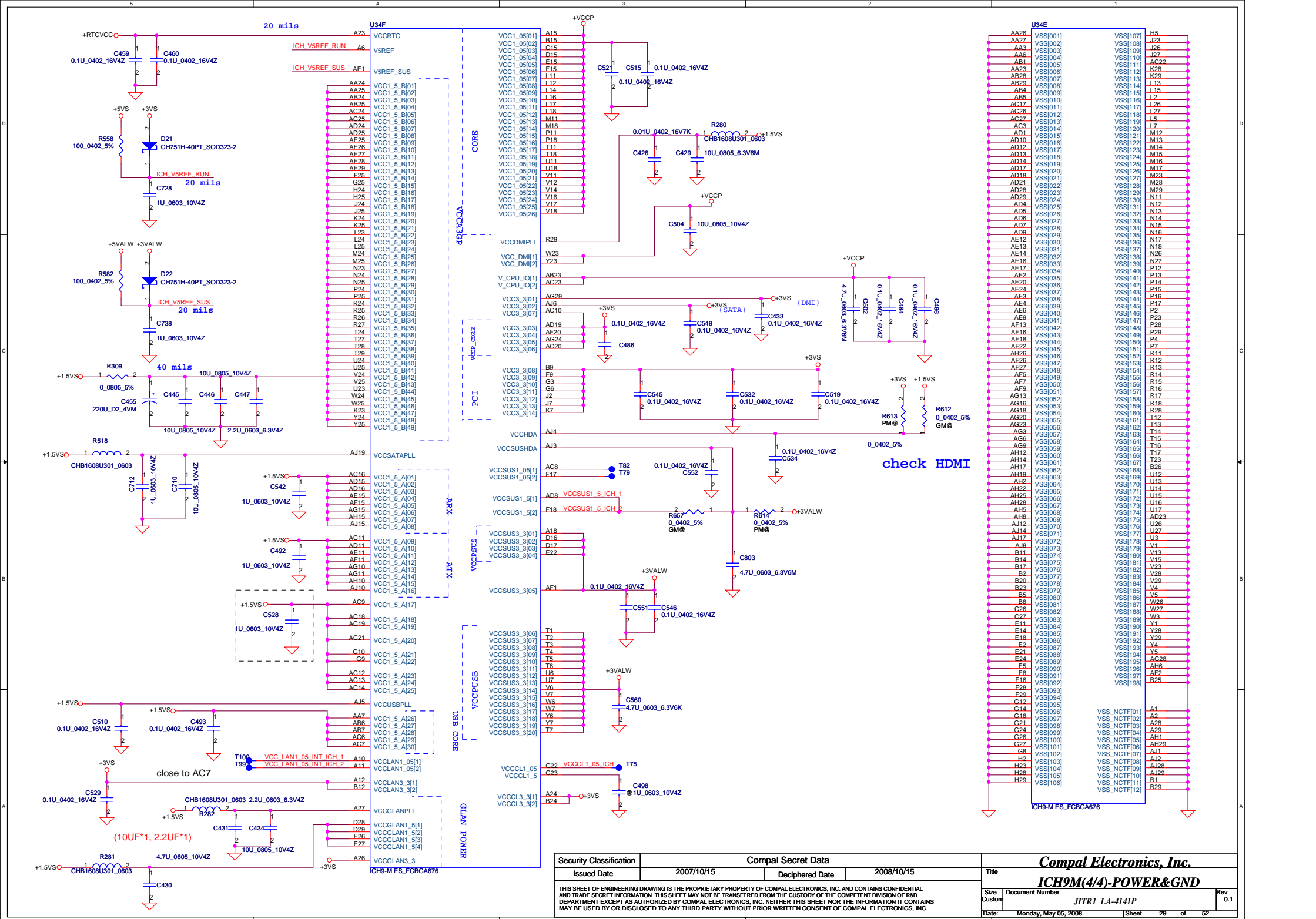


XOR Chain Entrance Strap		
ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation
1	1	Set PCIE port config bit 1



USB PORT LIST	
PORT	DEVICE
0	LEFT SIDE
2	CMOS
3	3G
4	RIGHT SIDE
6	BT
8	WLAN
10	NEW CARD
11	RIGHT SIDE

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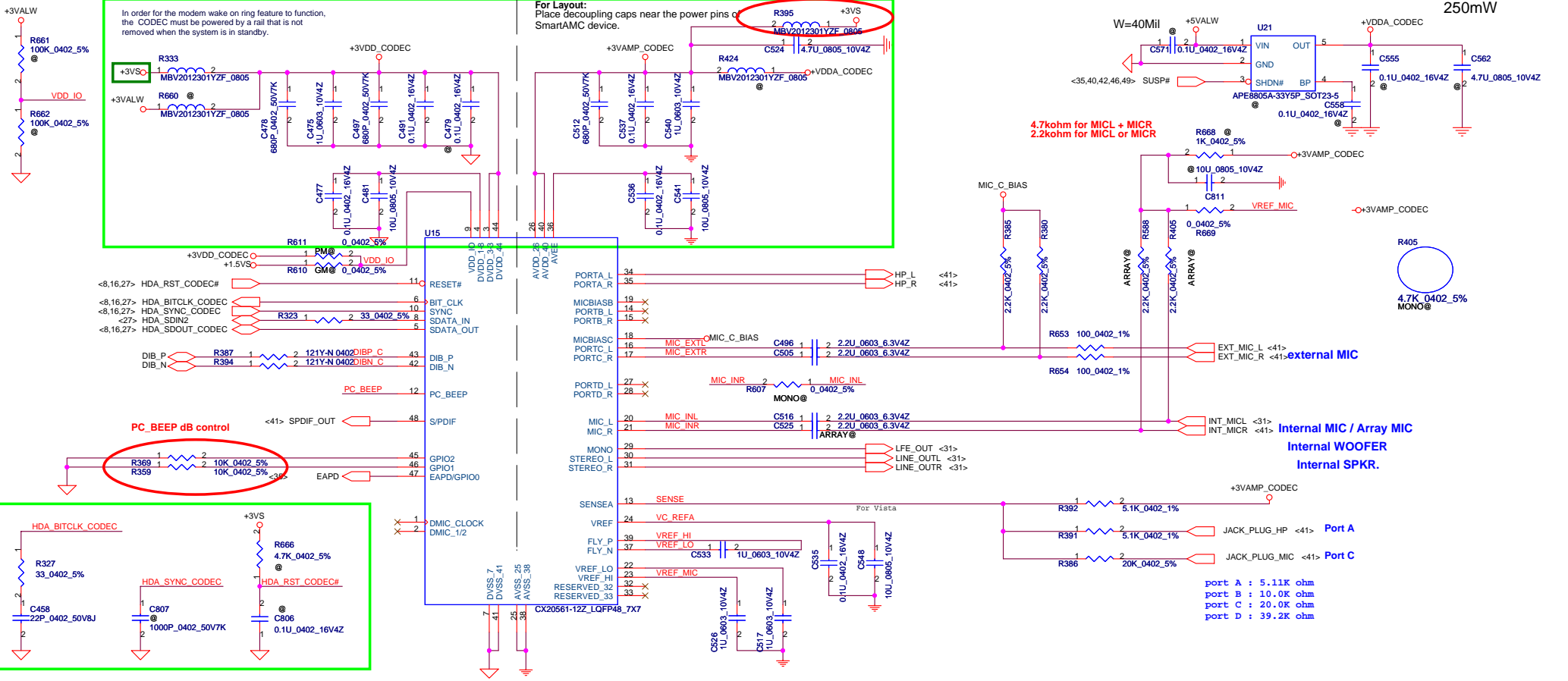
AUDIO CODEC

0308_Change R294 and R295 from 0 ohm to bead, C363 from 10uF to 680pF, C365 and C368 from 0.1uF to 680pF CHANGE TO 0ohm (2008/05/05)

CODEC POWER (3.33V) 250mW

In order for the modem wake on ring feature to function, the CODEC must be powered by a rail that is not removed when the system is in standby.

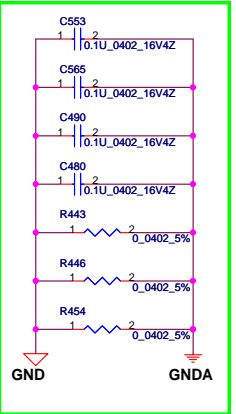
For Layout: Place decoupling caps near the power pins of U15 SmartAMC device.



4.7kohm for MICL + MICR
2.2kohm for MICL or MICR

- port A : 5.11K ohm
- port B : 10.0K ohm
- port C : 20.0K ohm
- port D : 39.2K ohm

DIGITAL ANALOG



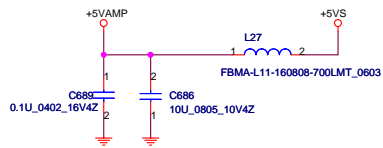
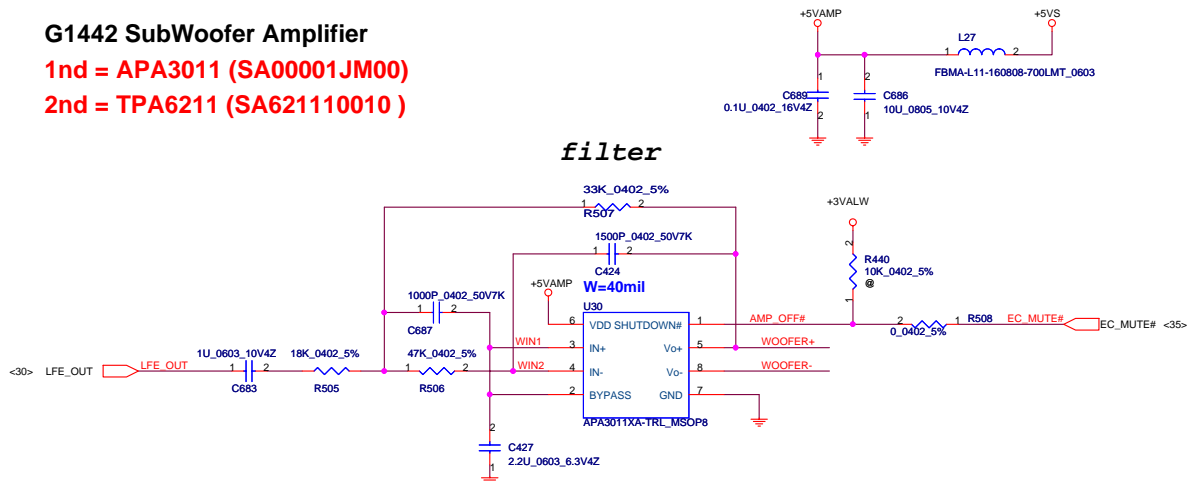
Place these C and R around AGND and DGND, then choose the one which is close to Codec to populate

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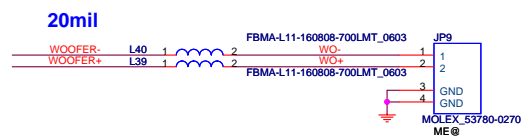
Compal Electronics, Inc.			
Title: CX20561-AMOM Codec			
Size	Document Number	Rev	
Custort	JITRI_LA-4141P	0.1	
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G1442 SubWoofer Amplifier

1nd = APA3011 (SA00001JM00)
 2nd = TPA6211 (SA621110010)

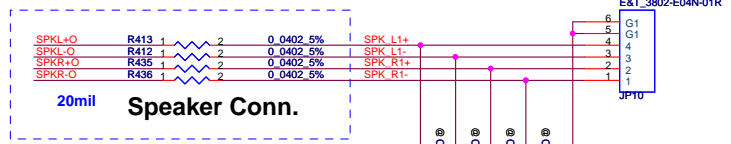
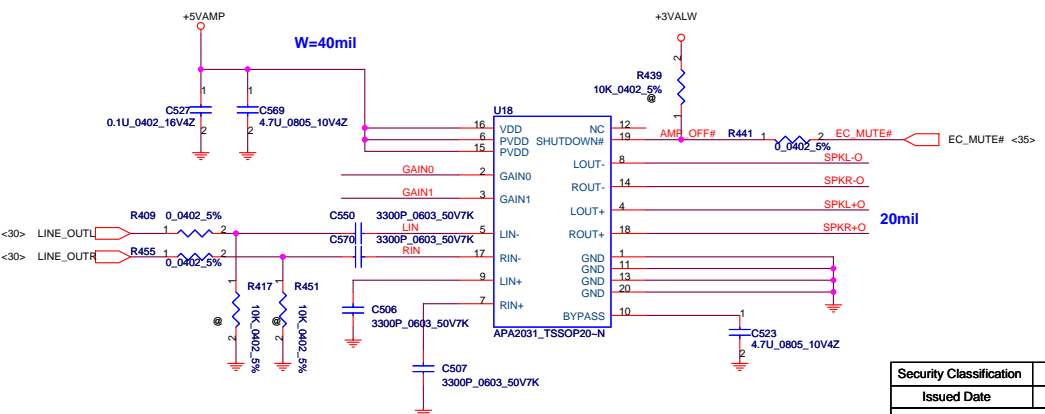
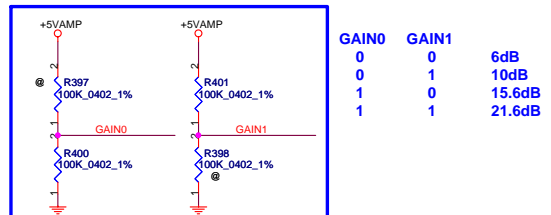


SubWoofer Conn.

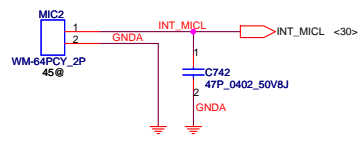


Speaker Amplifier

1nd = APA2031 (SA00001RZ00)
 2nd = G1431F2U (SA000012Y00)

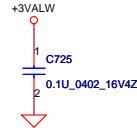
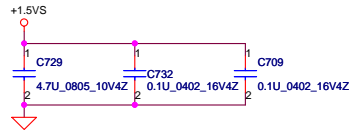
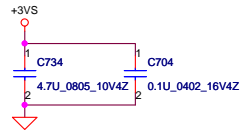


INT MIC

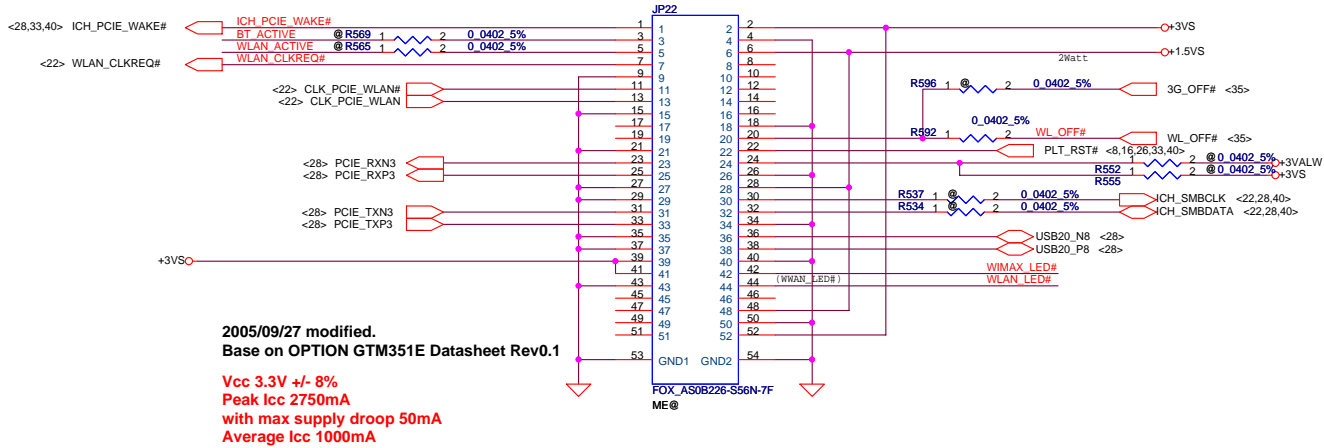


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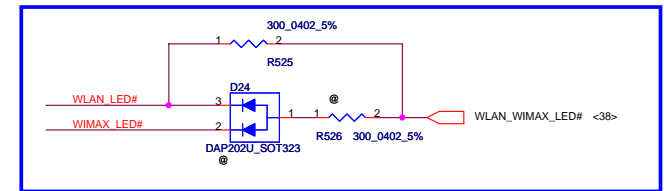
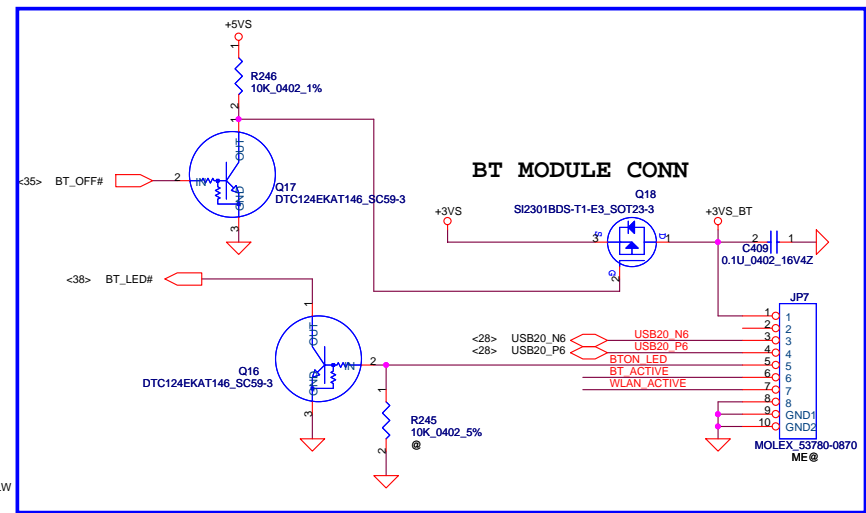
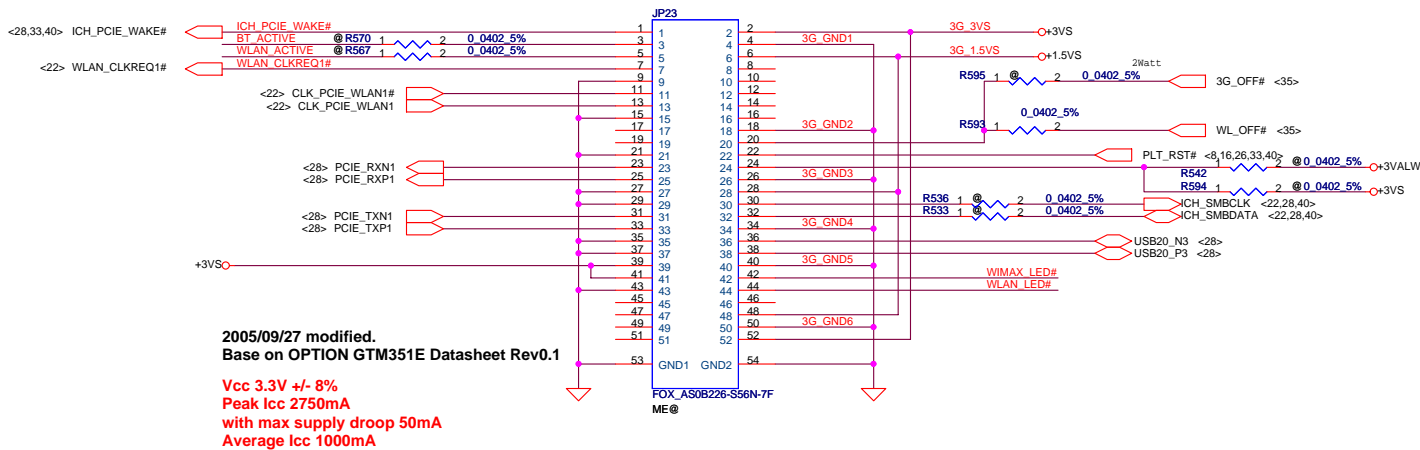
Mini-Express Card for 3G Or TV Tuner Mini-Express Card for WLAN



Mini-Express Card(Slot 1-WLAN WIMAX)

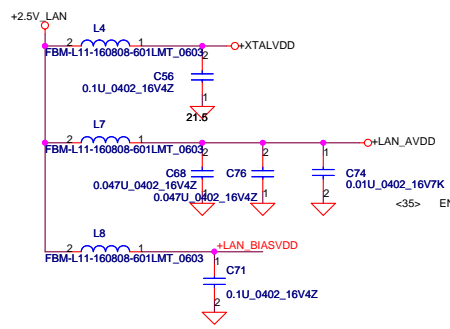


Mini-Express Card(Slot 2-WLAN WIMAX)

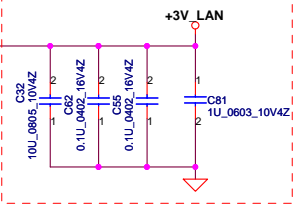


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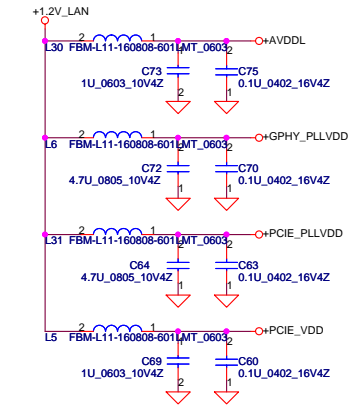
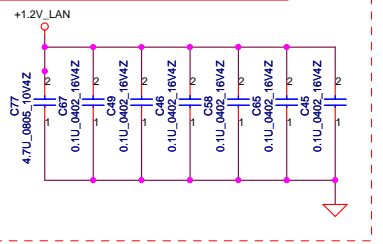
Layout Notice : Filter place as close chip as possible.



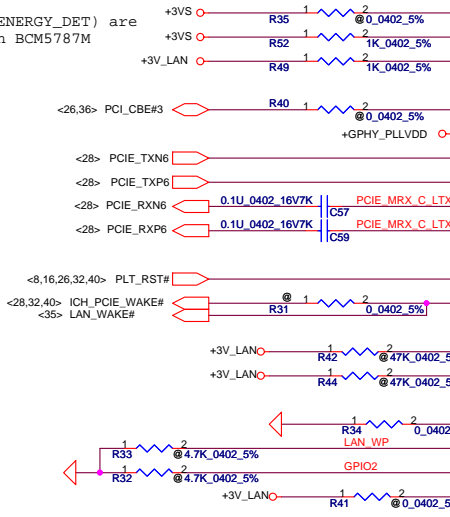
Layout Notice : Place as close chip as possible.



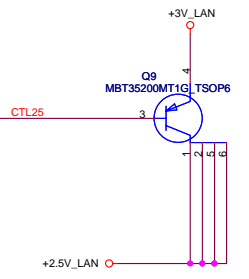
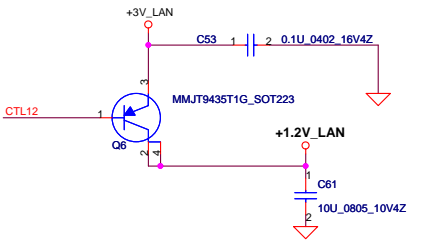
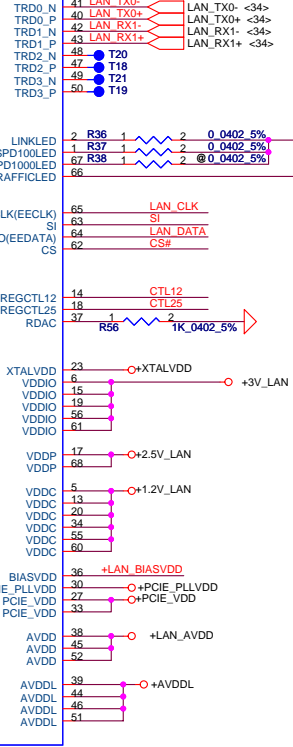
Layout Notice : 1.2V filter. Place as close chip as possible.



(CLKREQ#) and (ENERGY_DET) are only supported in BCM5787M



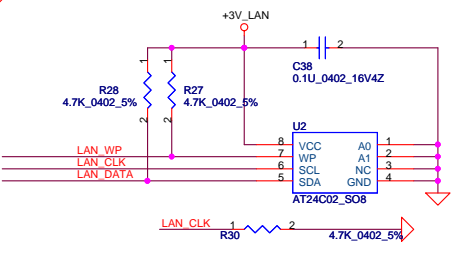
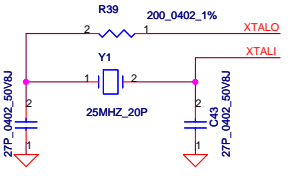
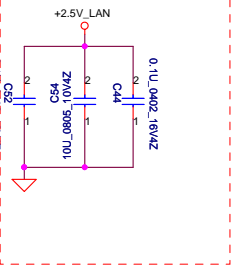
U1



Notice : 4.7u 6.3V capacitor Thickness 1.25mm

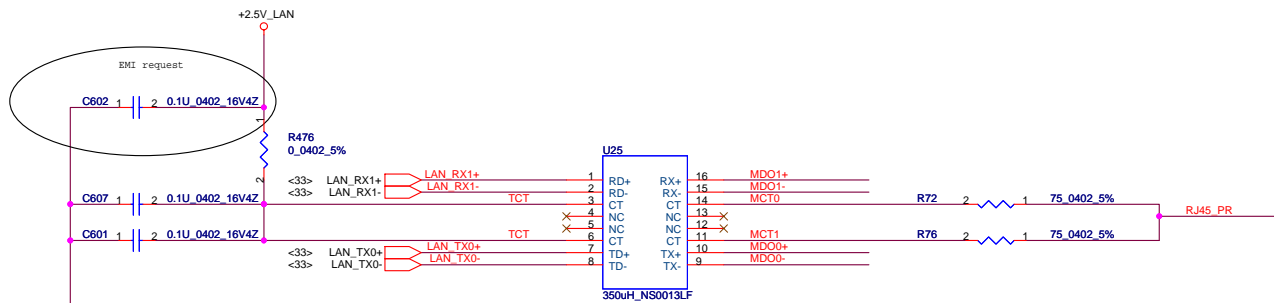
Layout Notice : Filter place as close chip as possible.

Layout Notice : Place as close chip as possible.

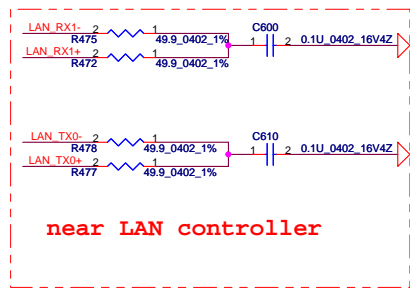


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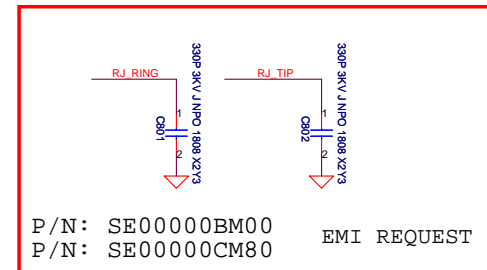
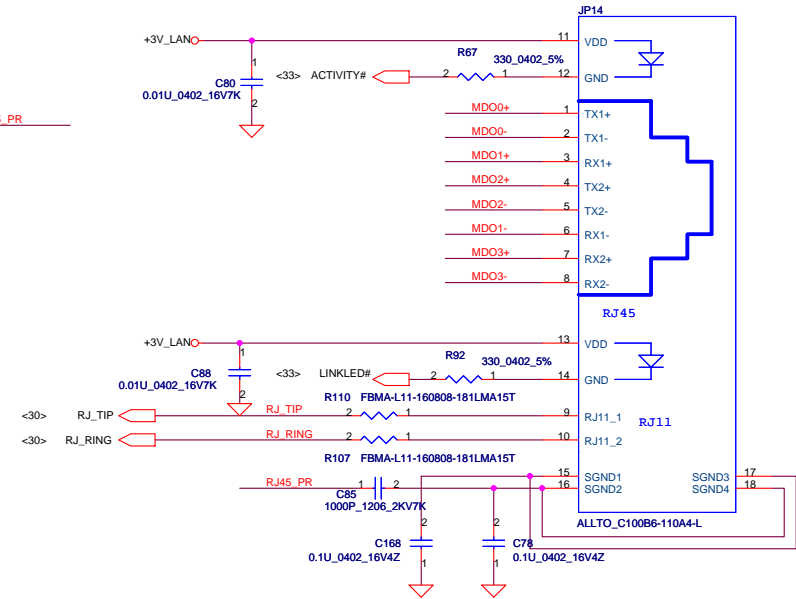
Title			
Compal Electronics, Inc.			
BCM5787MKML			
Size	Document Number	Rev	
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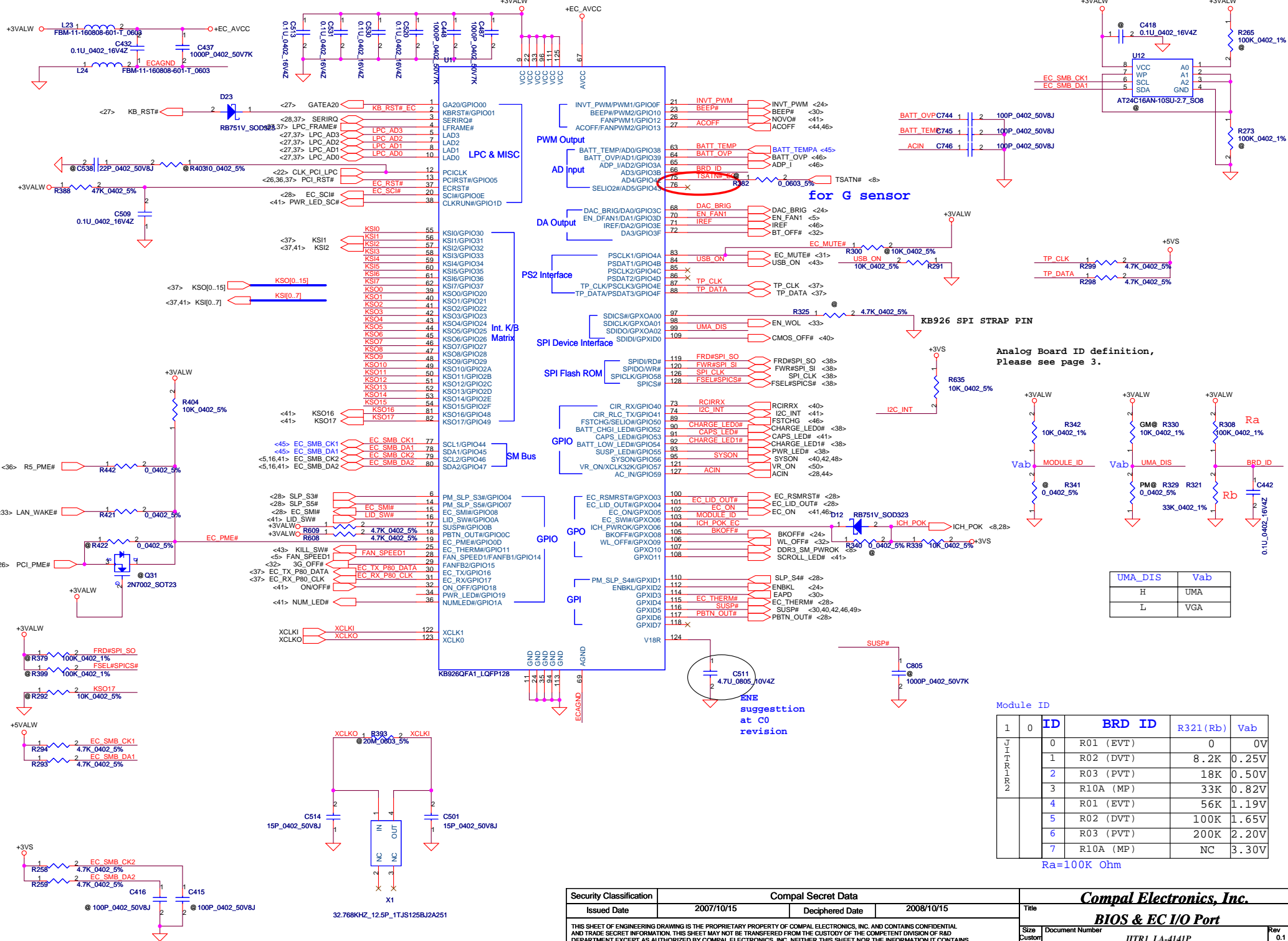
Change C468,C470,C473,C474,C475,C476 from 0.01uF to 0.1uF



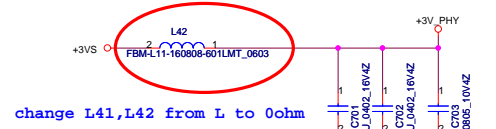
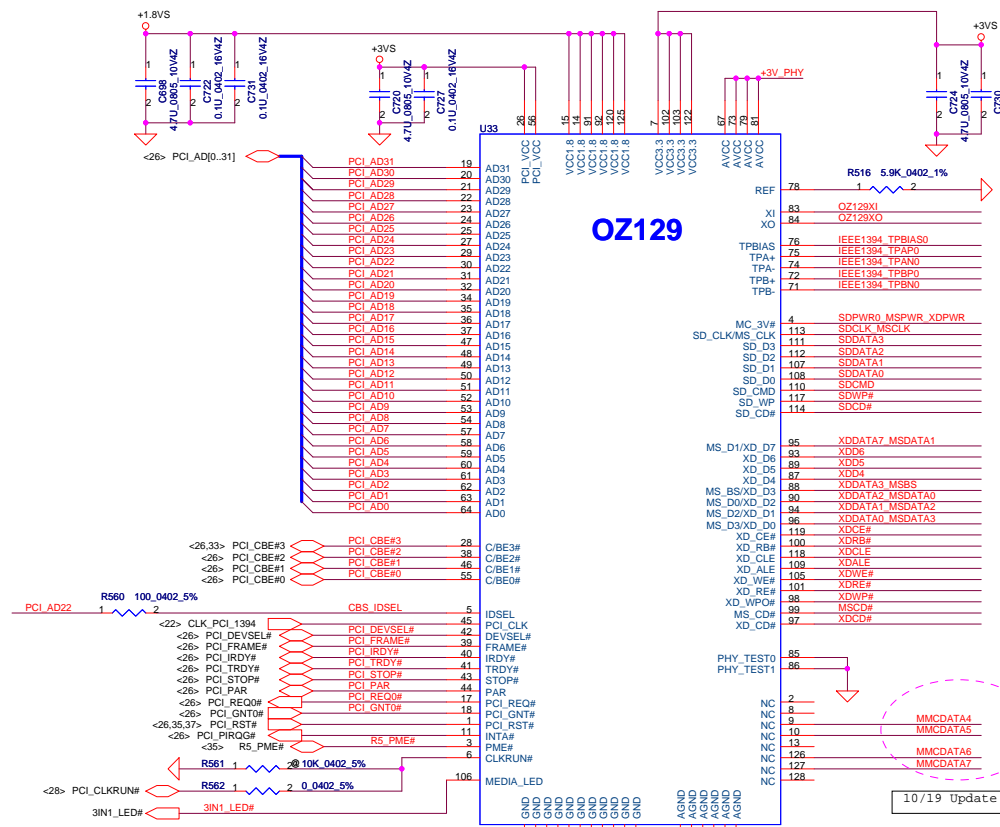
RJ11+RJ45 CONN



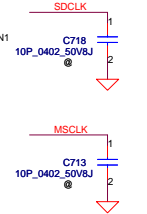
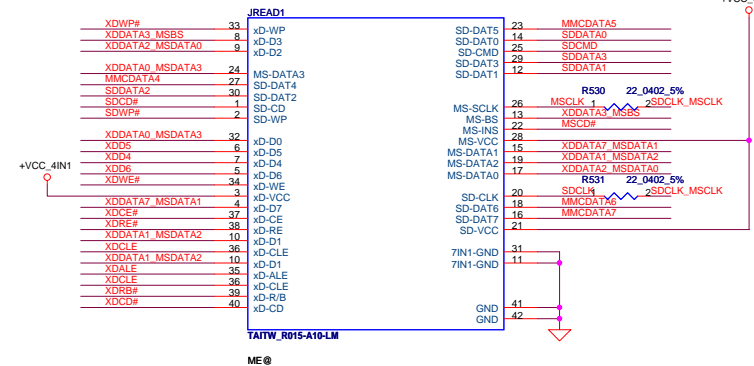
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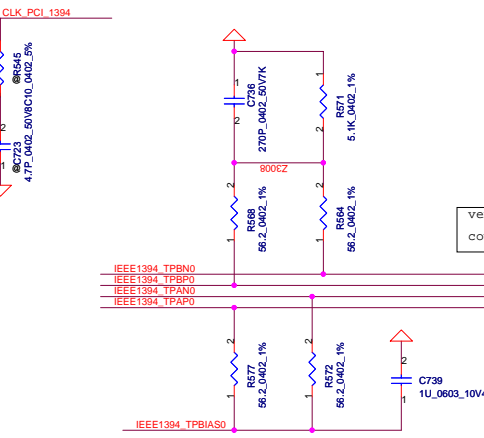
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change L41, L42 from L to 0ohm



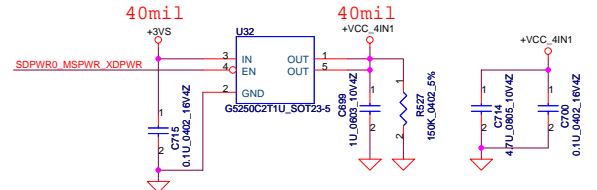
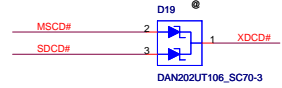
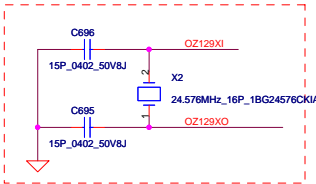
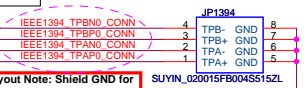
LED behave:
 Idle -----> low
 Access data --> always high



vendor request rserve
 common check or 0 ohm

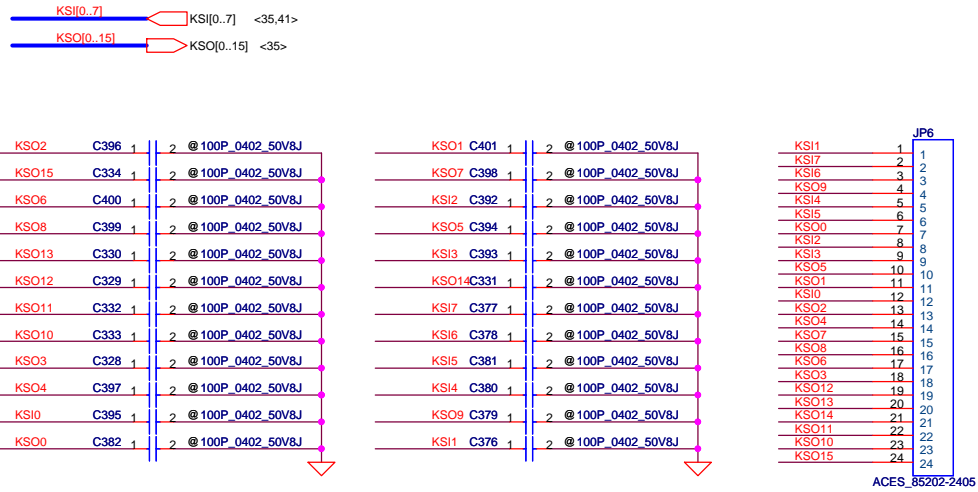
UPDATE 1394 SYMBOL

Layout Note: Shield GND for
 IEEE1394_TPA and TPB

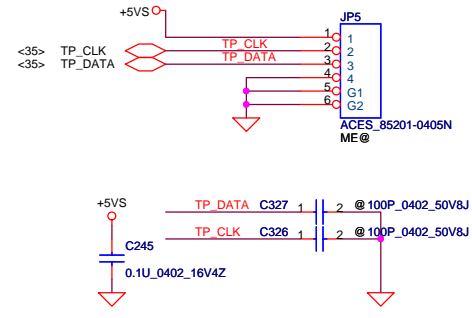


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Document Number 1394+3 in 1 Card		Rev 0.1	

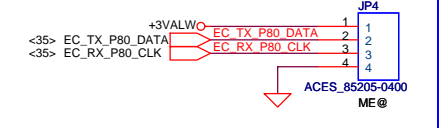
INT_KBD Conn.



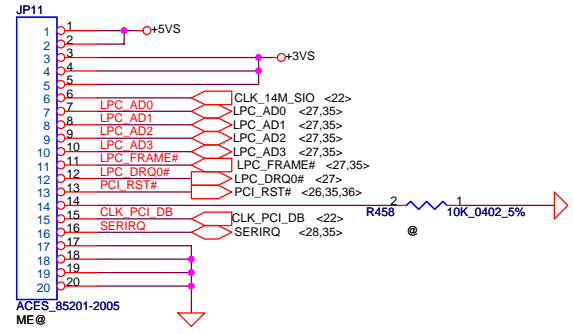
To TP/B Conn.



EC DEBUG PORT

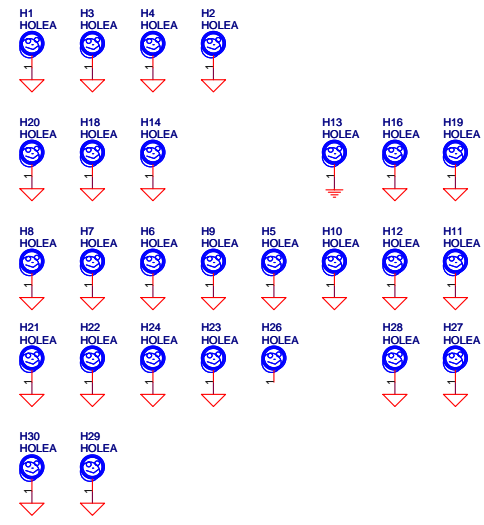
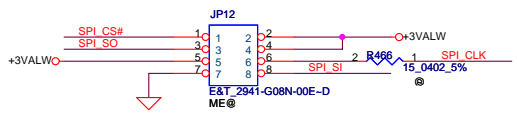
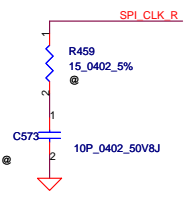
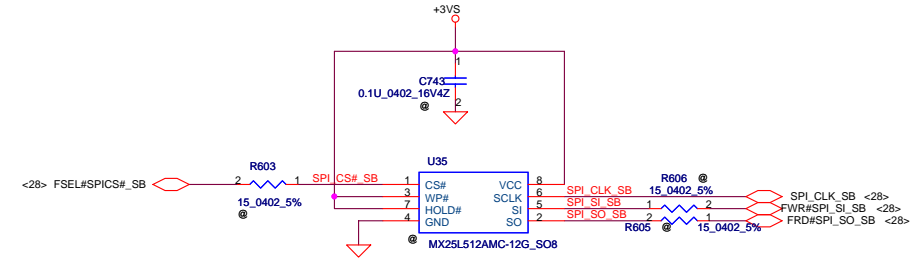
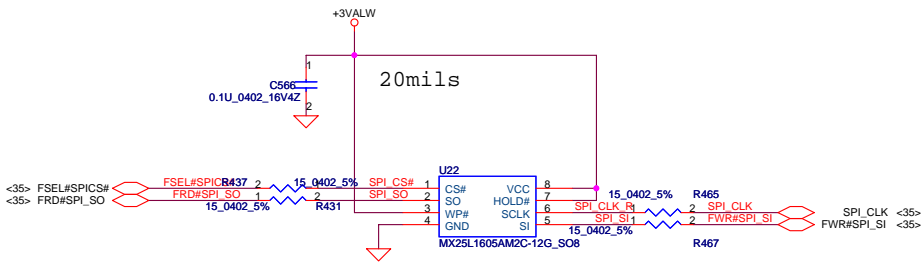


FOR LPC SIO DEBUG PORT

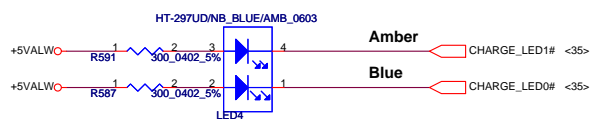


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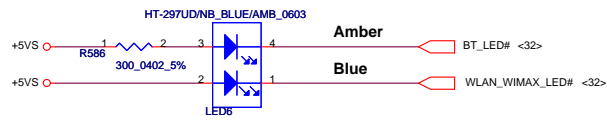
FOR EC 16M SPI ROM



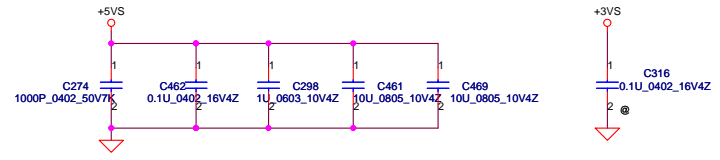
LED



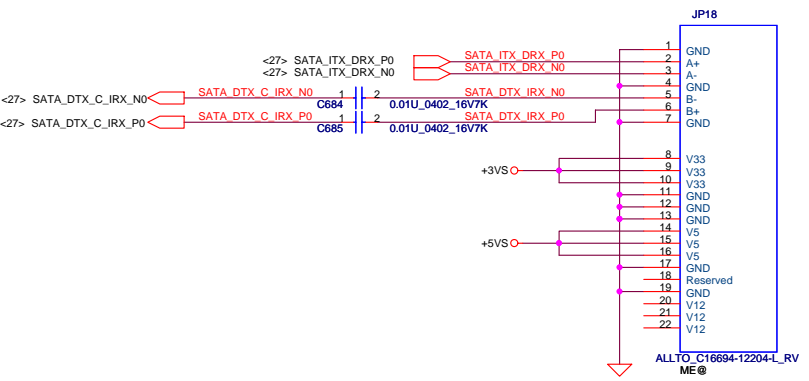
Blue&Amber



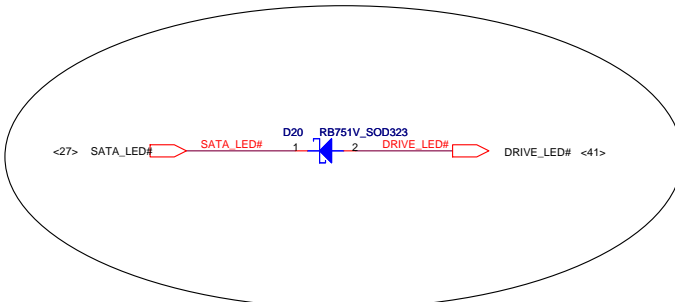
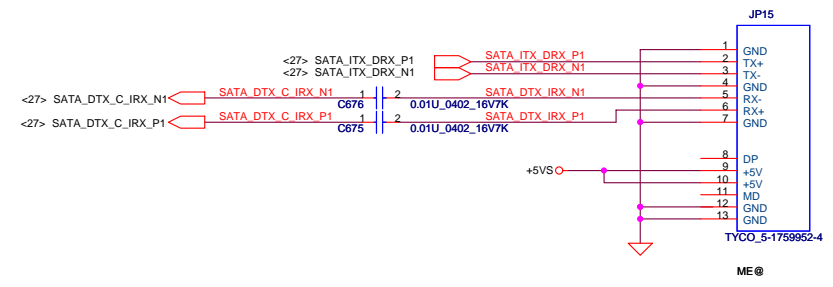
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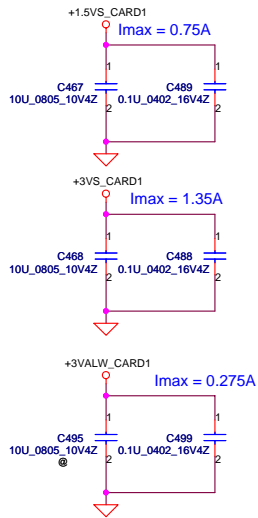
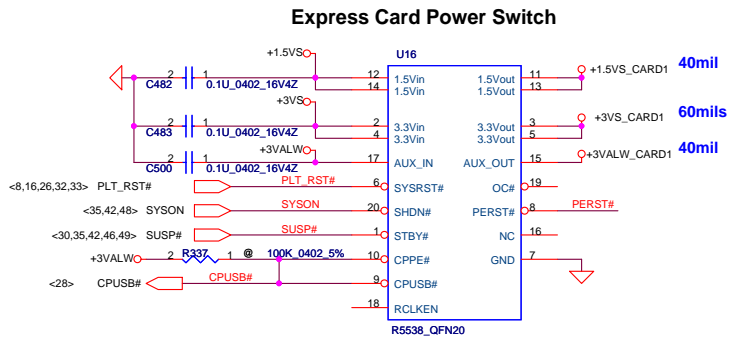
SATA HDD Conn.



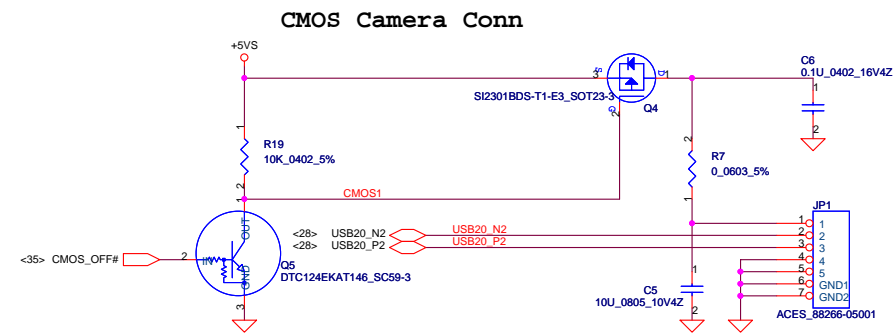
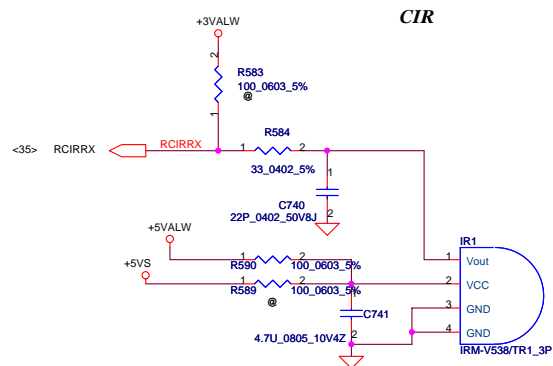
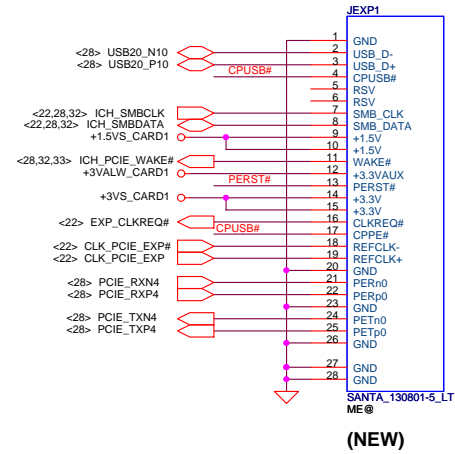
SATA ODD Conn.



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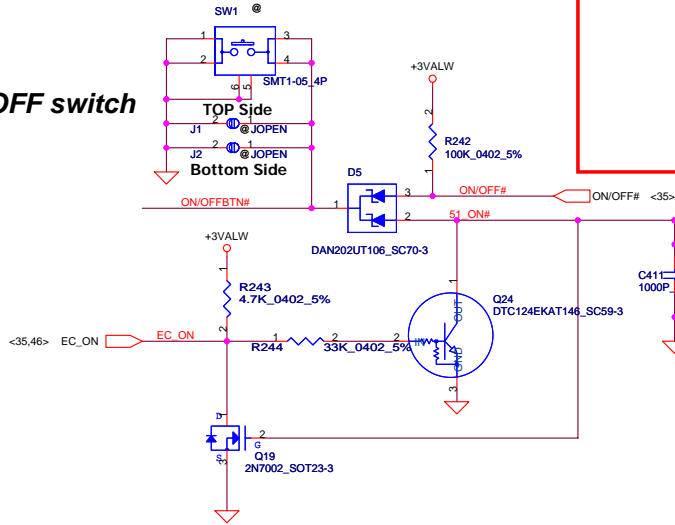
New Card Socket (Left/TOP)



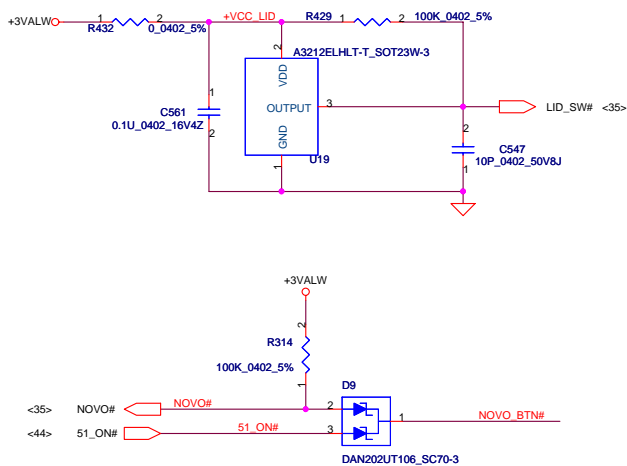
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Issued Date	2007/10/15	Deciphered Date	2008/10/15	NEW CARD & CMOS Connector	
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Power Button

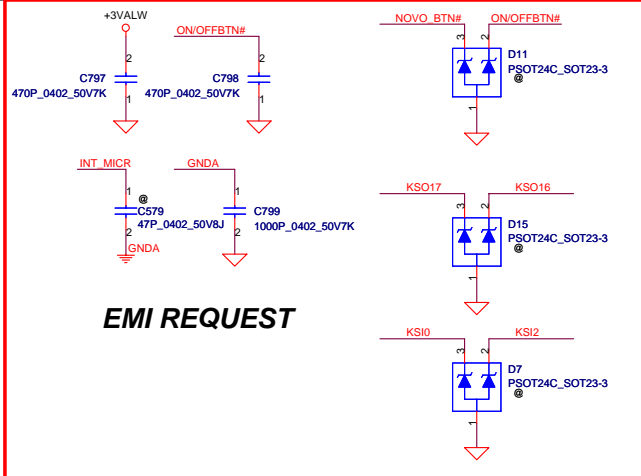
ON/OFF switch



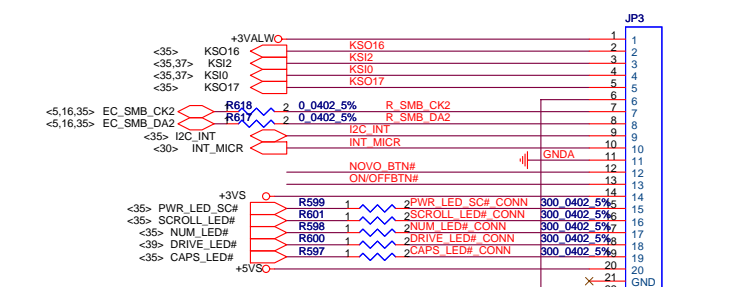
Lid Switch



EMI REQUEST

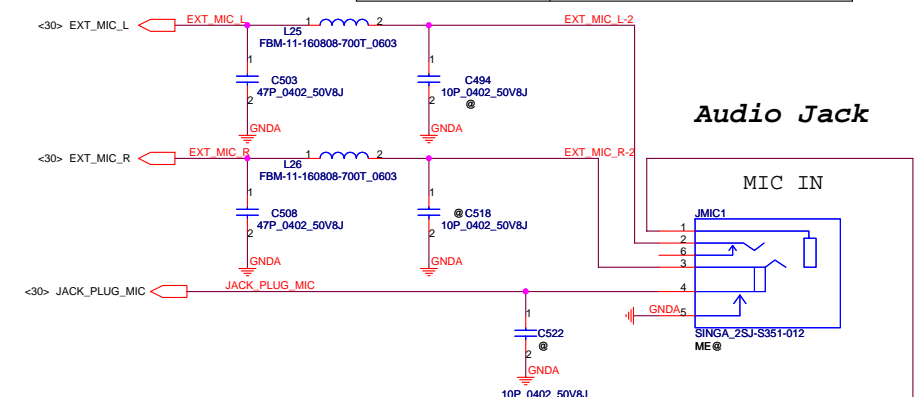


Switch Board Conn.

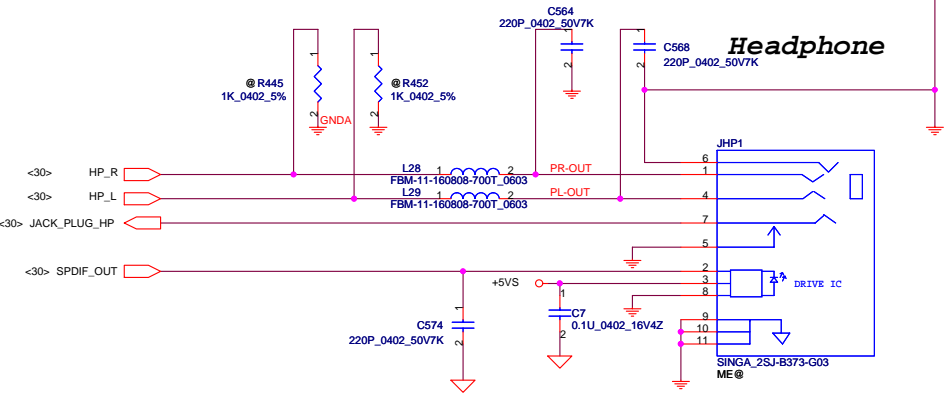


BTN FUNCTION	KEY MATRIX	
	IN	OUT
UP	KSO16	KSI2
DOWN	KSO17	KSI0
OK	KSO17	KSI0

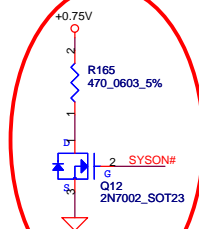
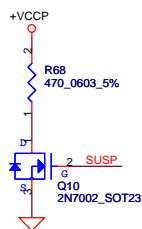
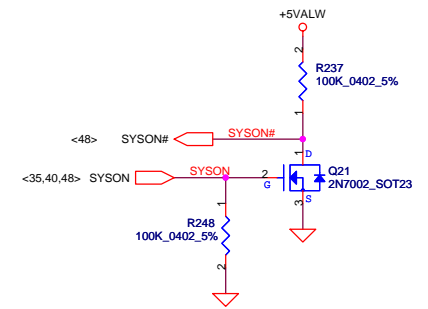
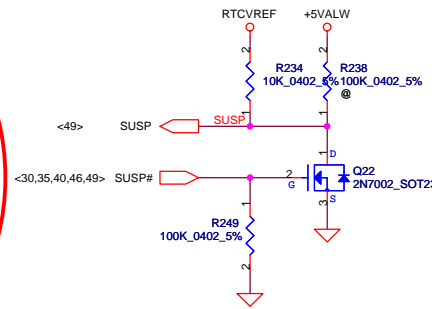
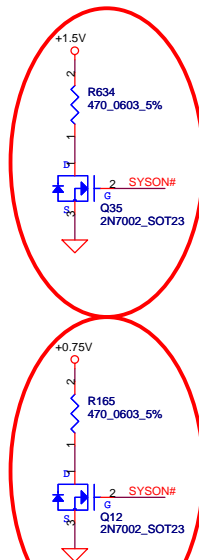
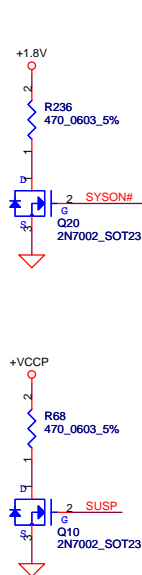
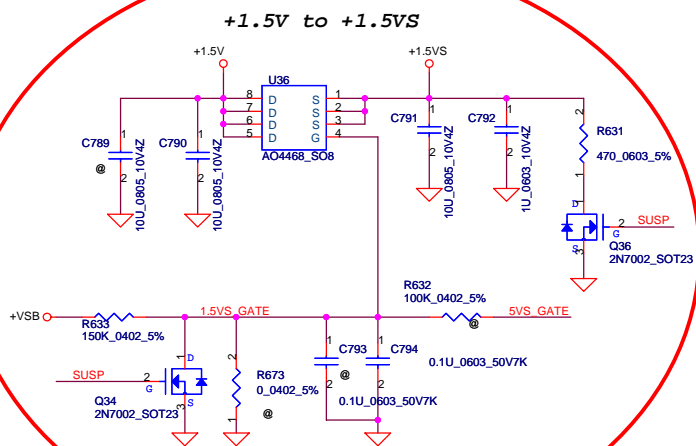
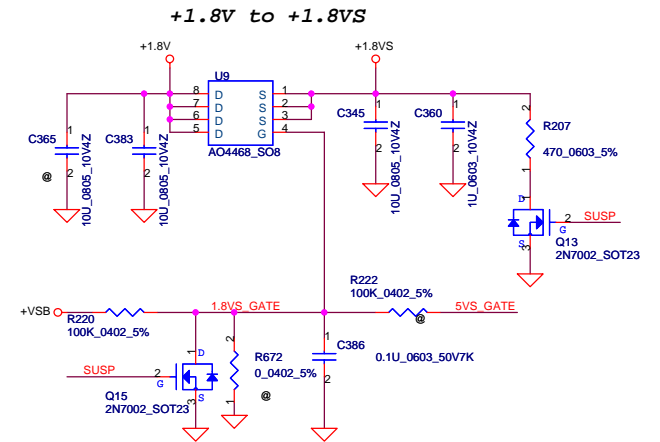
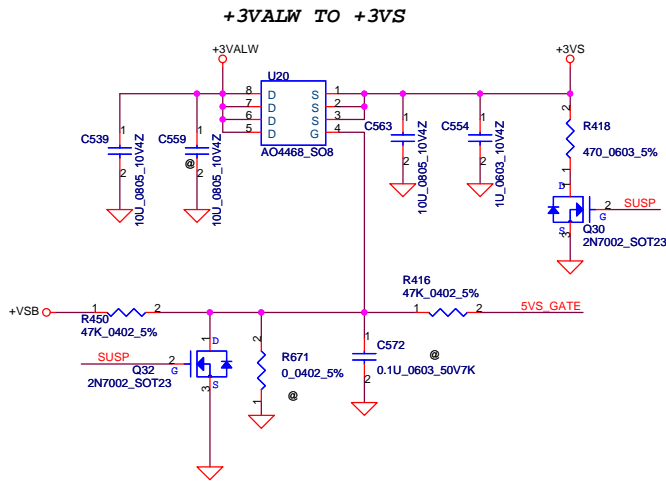
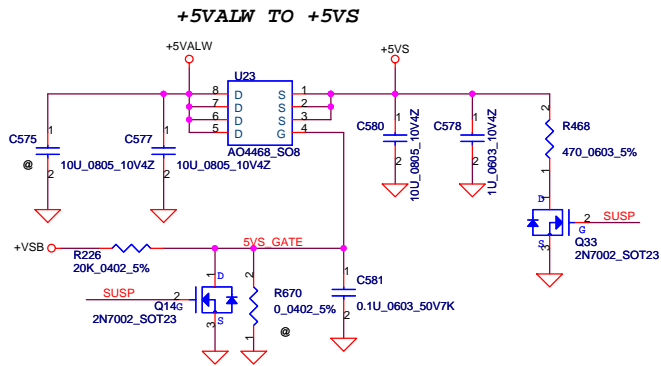
Audio Jack



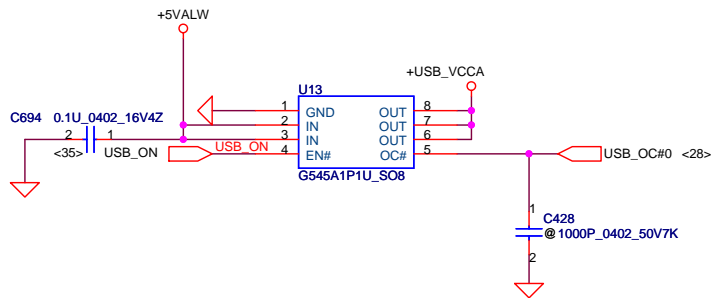
Headphone



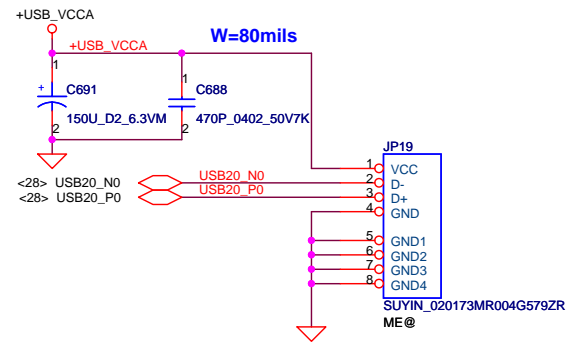
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Issued Date	2007/10/15	Deciphered Date	2008/10/15	Title	
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				Document Number	
				JITR1_LA-4141P	
				Rev 0.1	
				Date: Wednesday, May 07, 2008	
				Sheet 41 of 52	



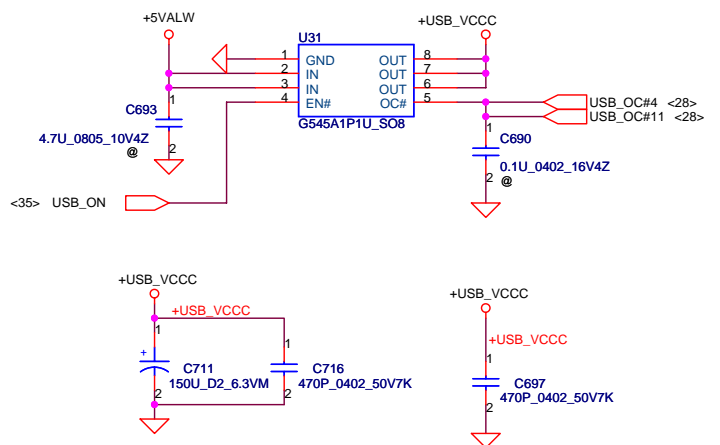
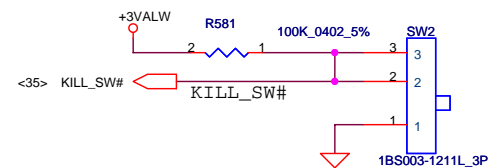
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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title
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Size	Document Number	Rev		
Custom	LA-3691P	1.0		
Date	Monday, May 05, 2008	Sheet	42 of 52	



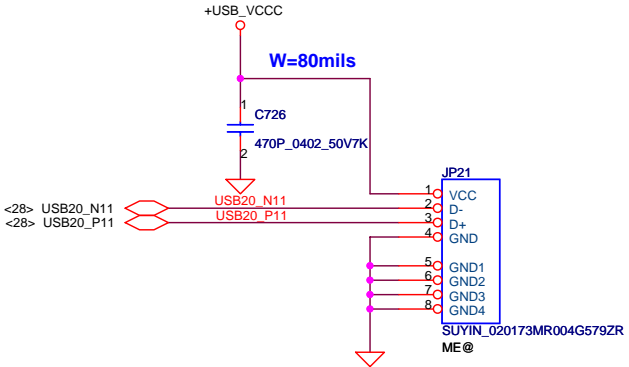
LIFT USB CONN. 1



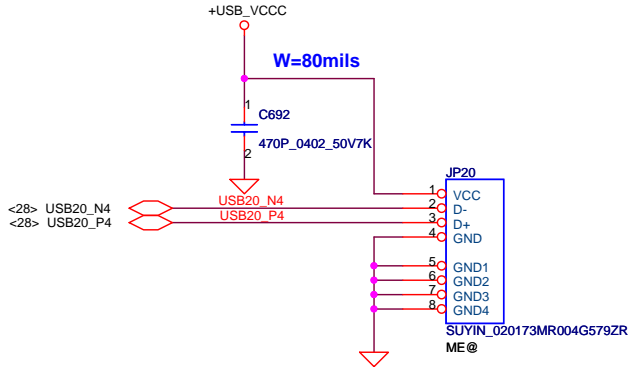
Kill Switch



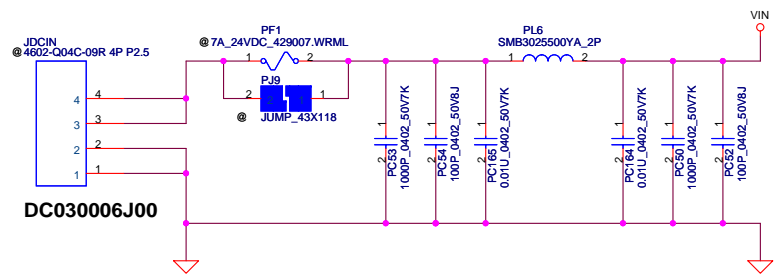
RIGHT USB CONN. 3



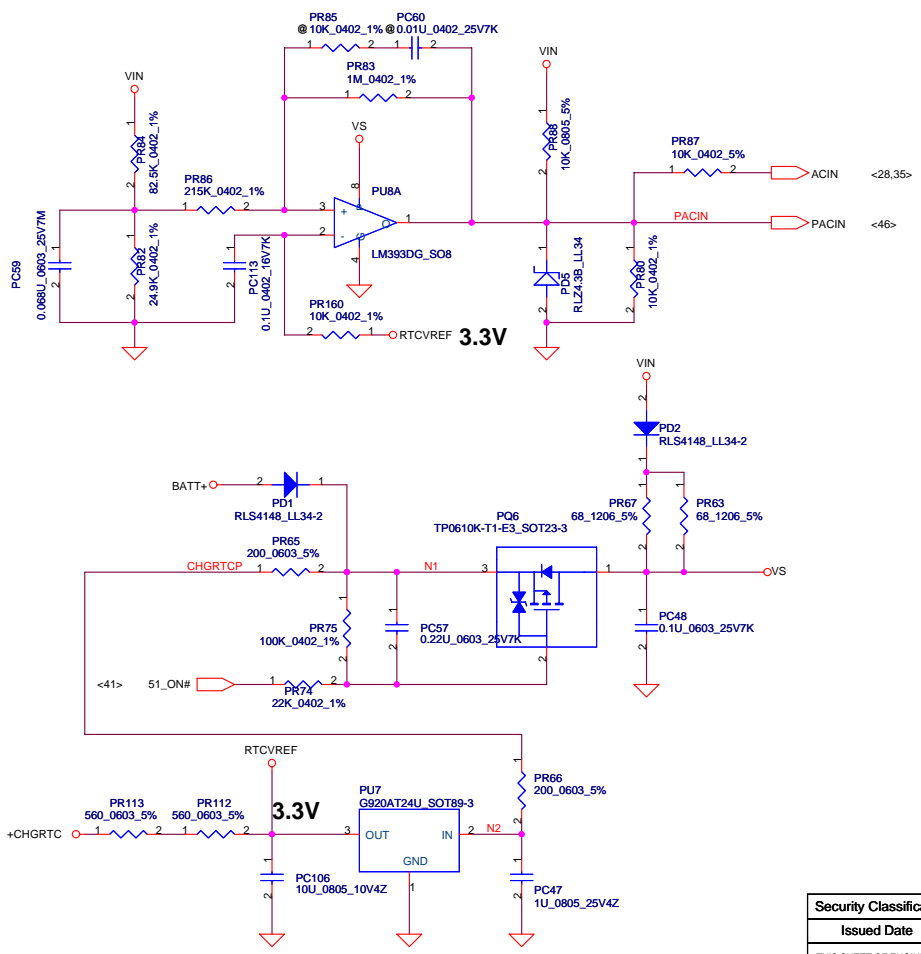
RIGHT USB CONN. 2



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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	
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				Size	Document Number
				Custom	LA-3691P
				Date:	Monday, May 05, 2008
				Sheet	43 of 52

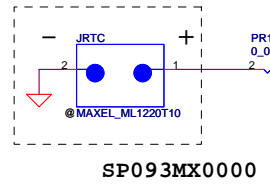
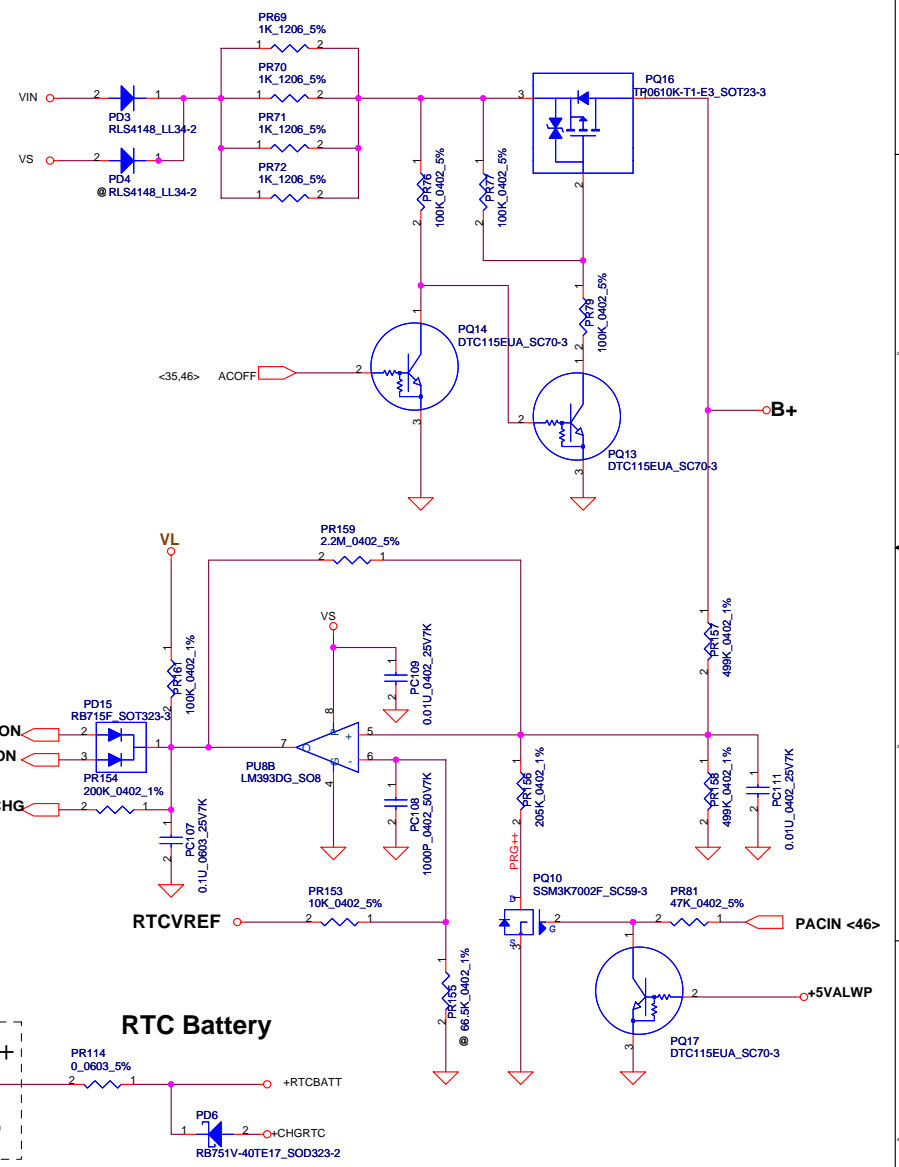


Vin Detector		
High	18.135	17.566
Low	14.866	14.355
	17.011	14.063



ACIN				
	Precharge detector	Min.	typ.	Max.
H-->L		13.843V	14.247V	14.636V
L-->H		14.936V	15.381V	15.814V

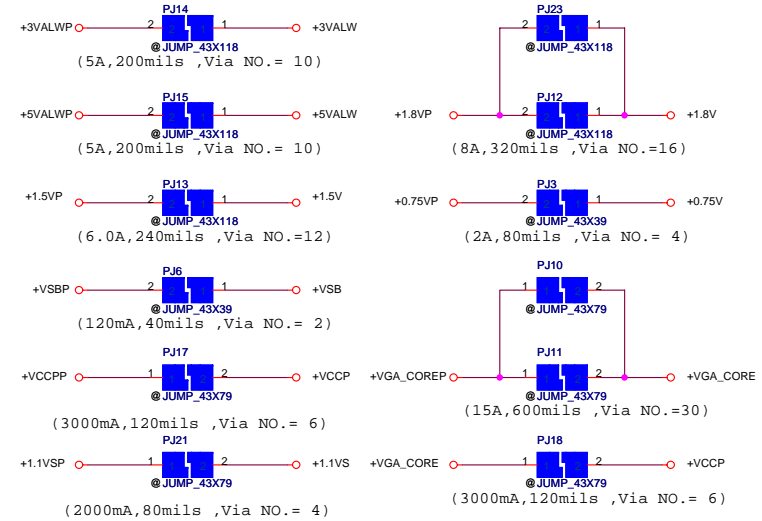
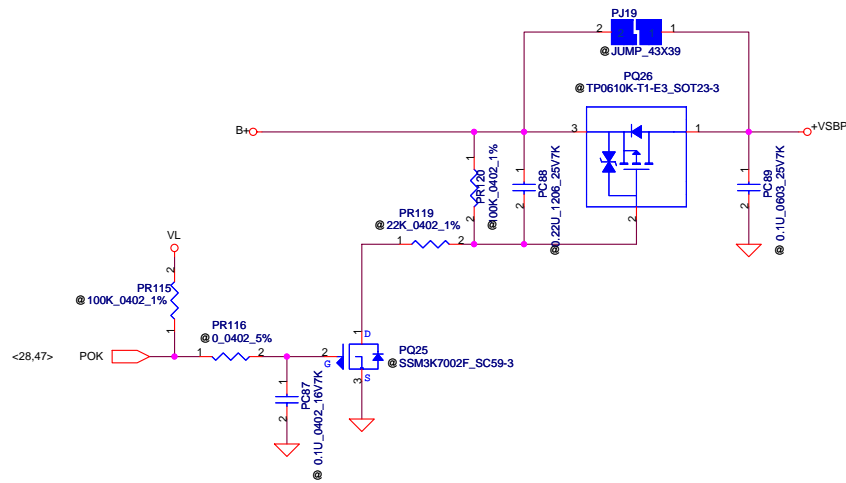
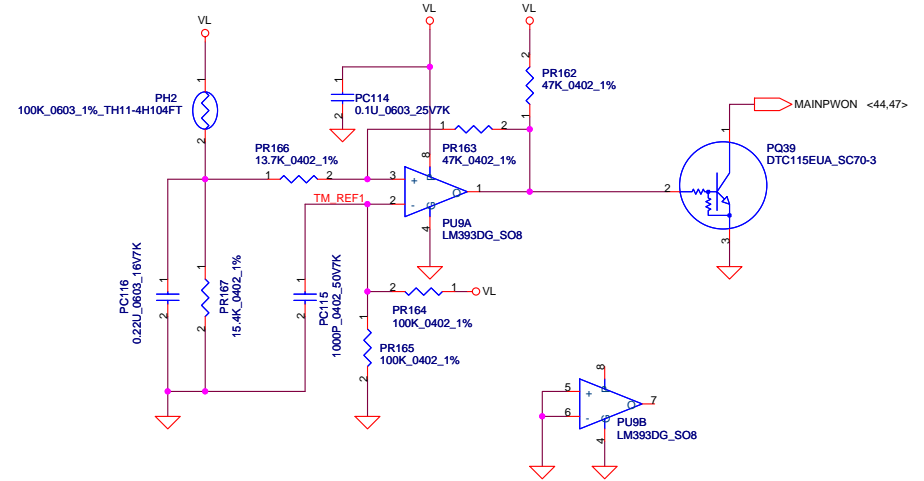
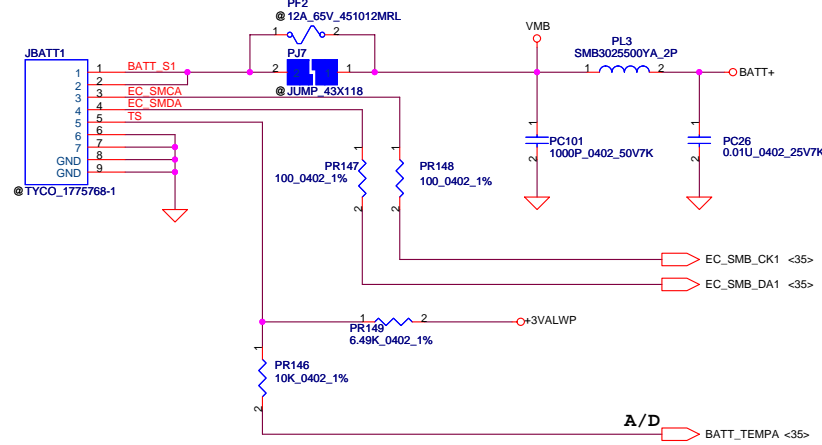
BATT ONLY				
	Precharge detector	Min.	typ.	Max.
H-->L		6.138V	6.214V	6.359V
L-->H		7.196V	7.349V	7.505V



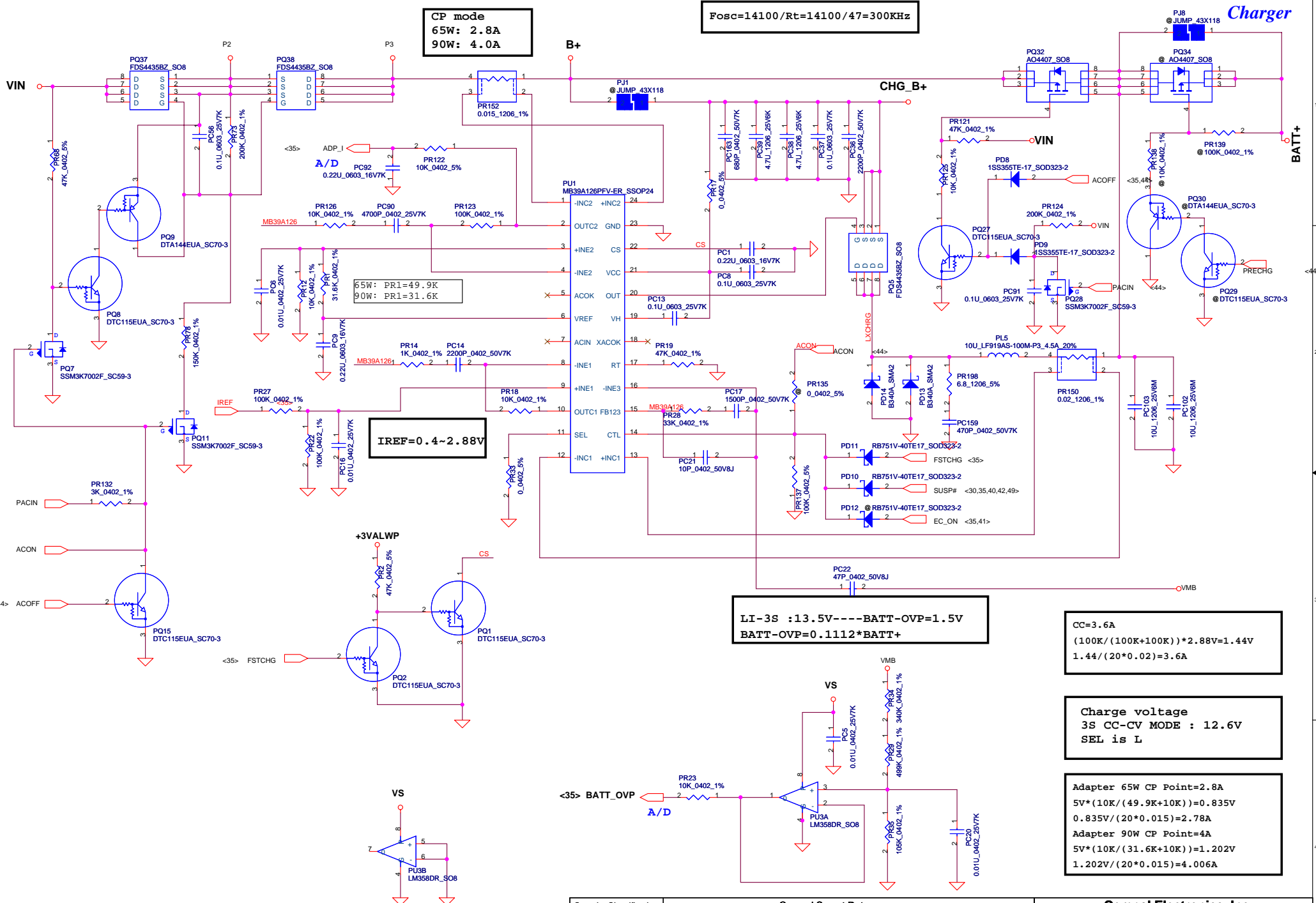
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2007/06/22	Deciphered Date	2008/06/22	
Title: DCIN & DETECTOR				
Size	Document Number			Rev 0.1
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PH1 under CPU bottom side :
 CPU thermal protection at 92 degree C
 Recovery at 56 degree C



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Issued Date	2007/6/22	Deciphered Date	2008/6/22	Title	BATTERY CONN / OTP
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				Rev	0.1



CP mode
 65W: 2.8A
 90W: 4.0A

$F_{osc} = 14100 / R_t = 14100 / 47 = 300\text{KHz}$

Charger

IREF = 0.4 ~ 2.88V

LI-3S : 13.5V --- BATT-OVP = 1.5V
BATT-OVP = 0.1112 * BATT+

CC=3.6A
 $(100K / (100K + 100K)) * 2.88V = 1.44V$
 $1.44V / (20 * 0.02) = 3.6A$

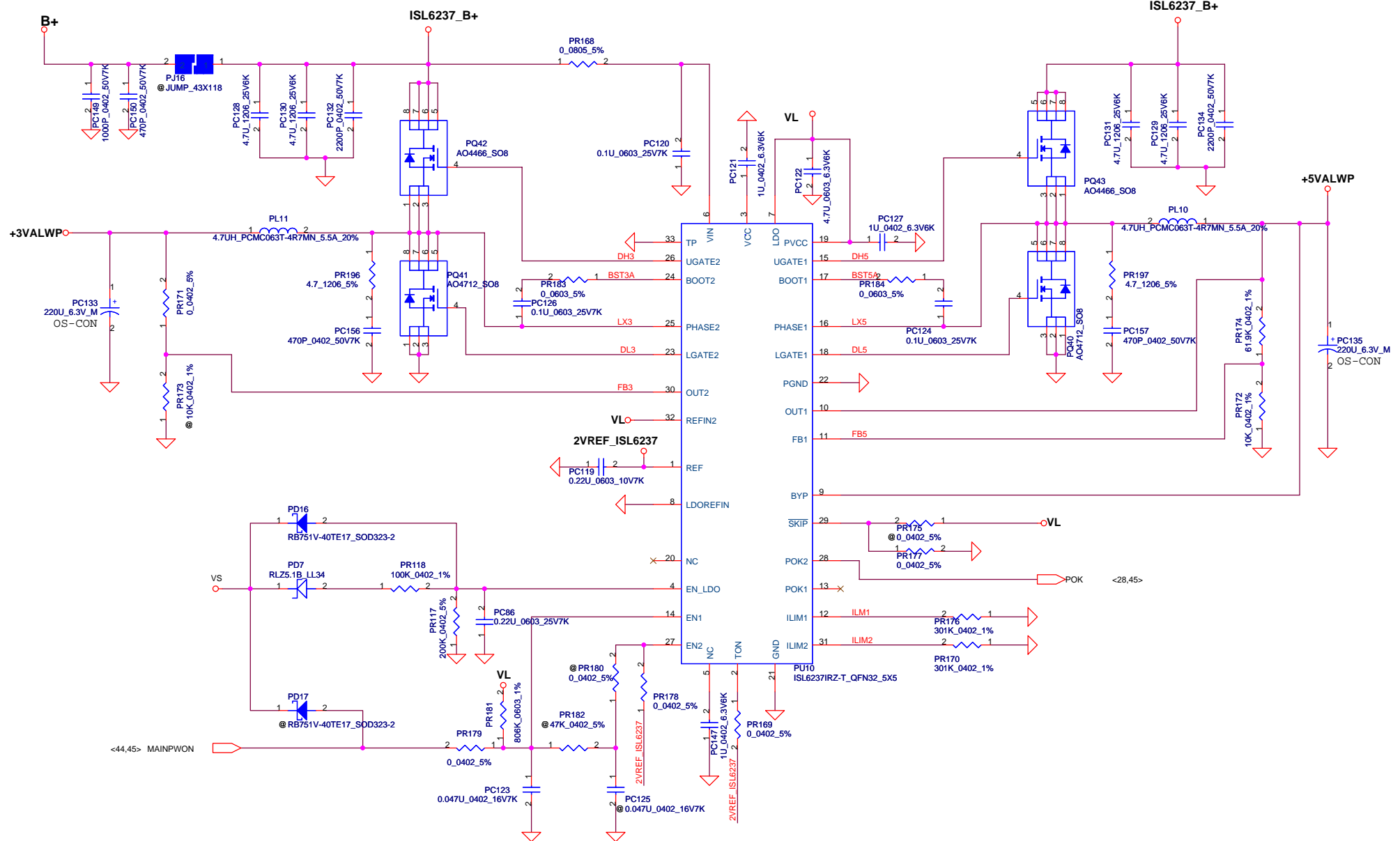
Charge voltage
 3S CC-CV MODE : 12.6V
 SEL is L

Adapter 65W CP Point=2.8A
 $5V * (10K / (49.9K + 10K)) = 0.835V$
 $0.835V / (20 * 0.015) = 2.78A$
 Adapter 90W CP Point=4A
 $5V * (10K / (31.6K + 10K)) = 1.202V$
 $1.202V / (20 * 0.015) = 4.006A$

Security Classification	Compal Secret Data	
Issued Date	2006/08/04	Deciphered Date
		2006/10/06

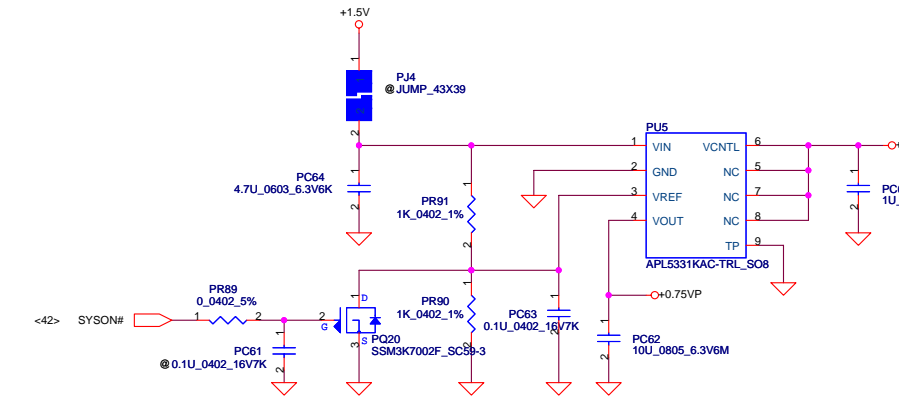
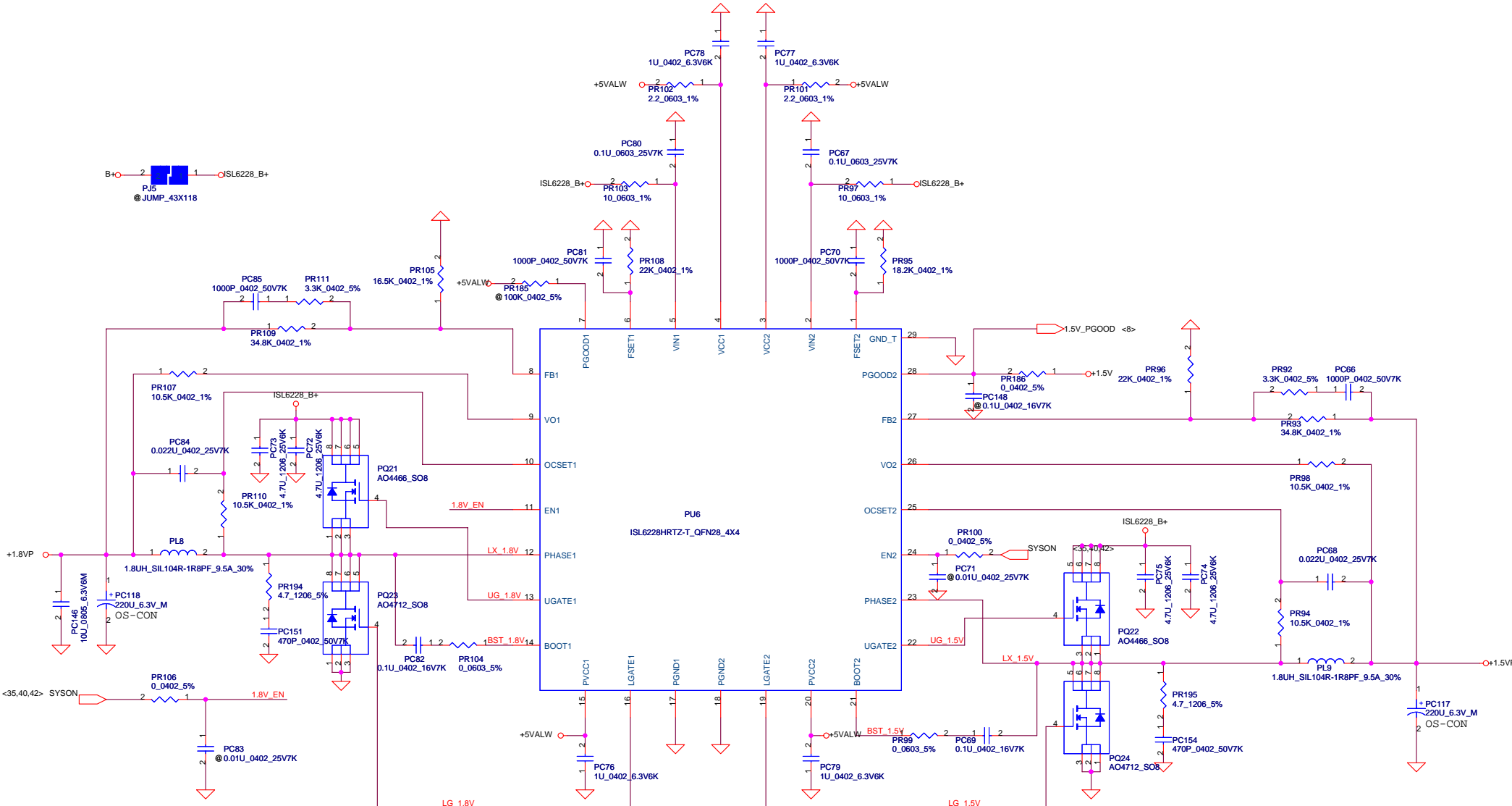
Compal Electronics, Inc.		
CHARGER		
Size B	Document Number	Rev 0.1

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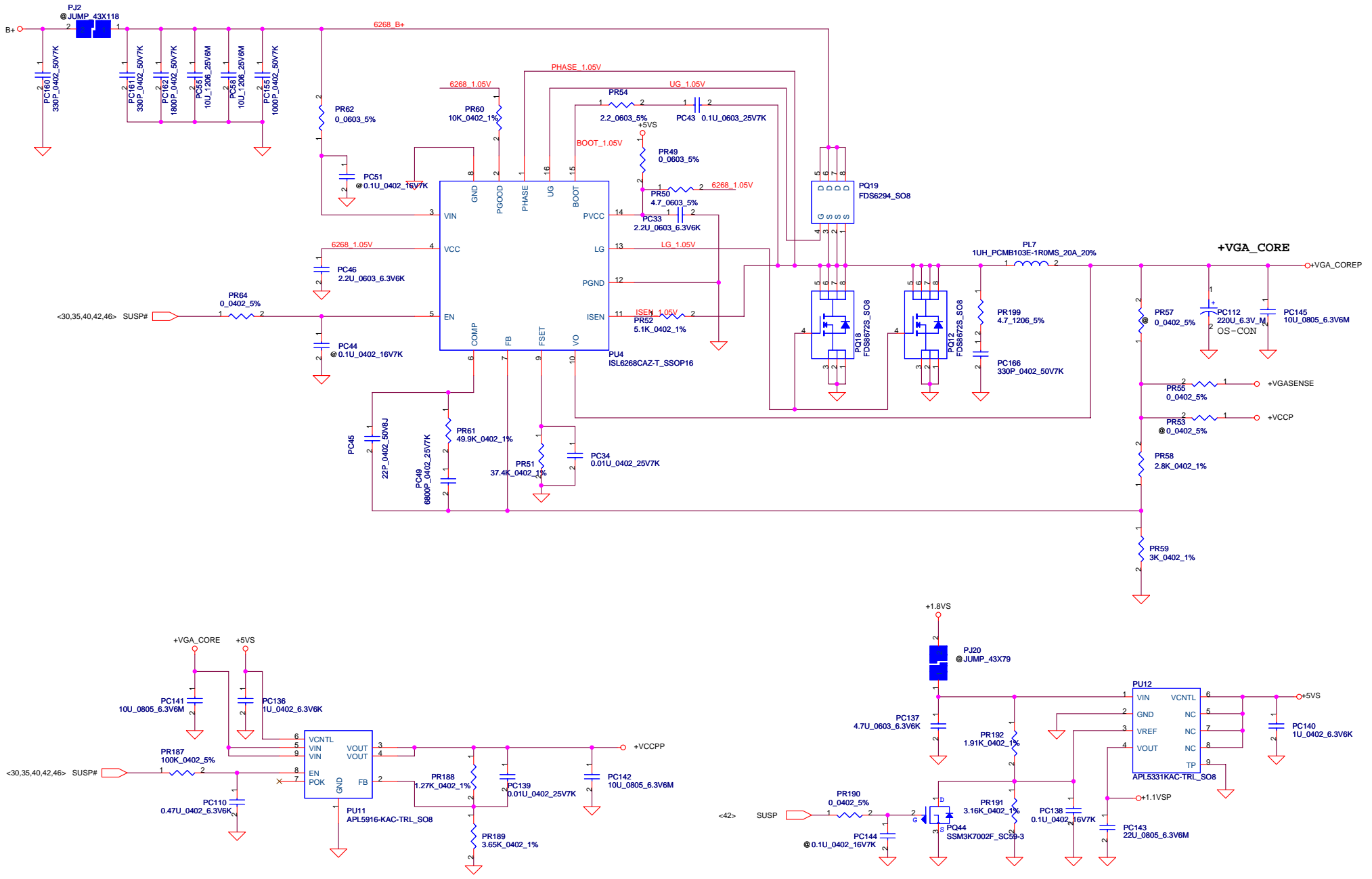
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Issued Date	2007/06/22	Deciphered Date	2008/06/22	+5V/+3V	
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Compal Electronics, Inc.

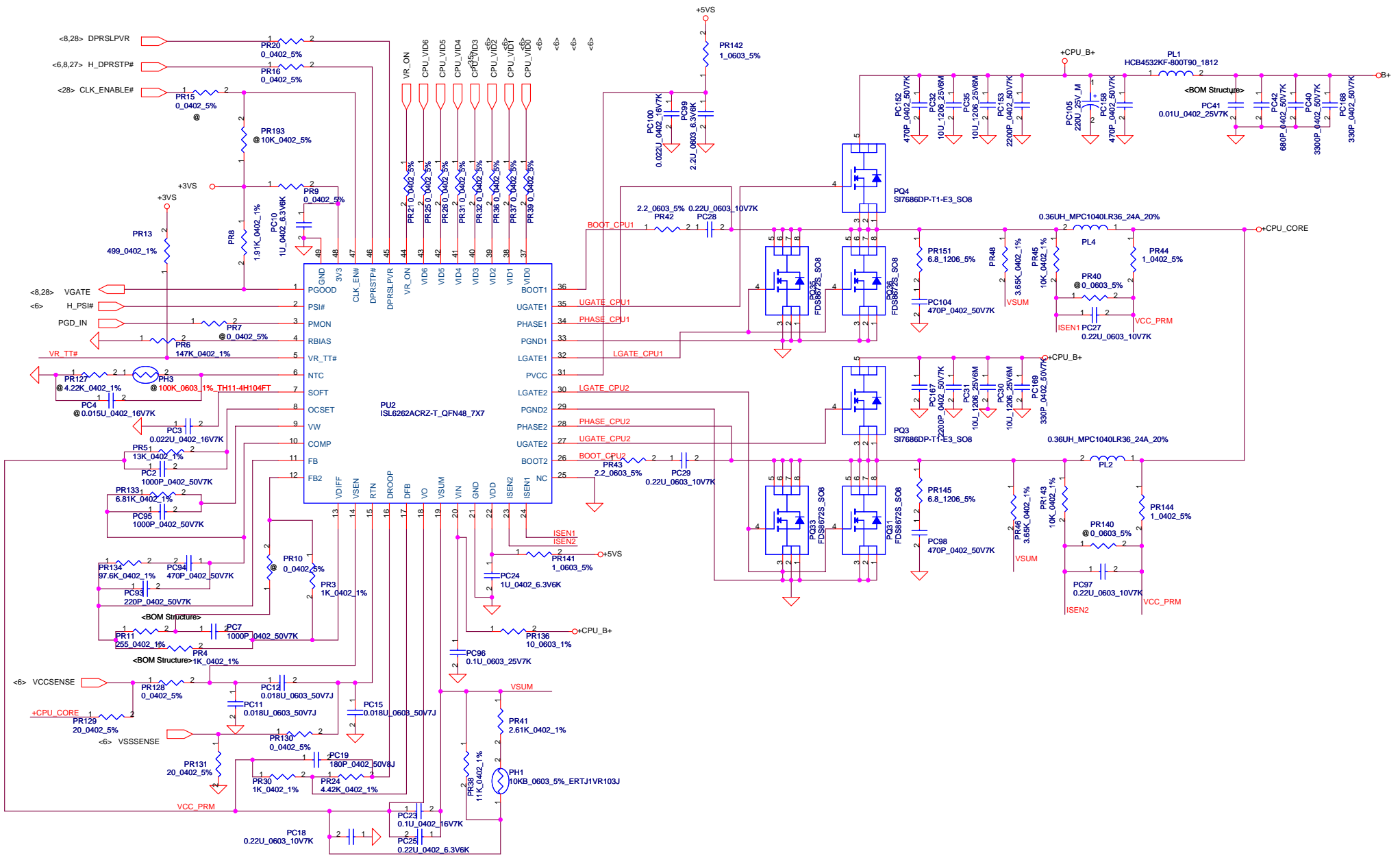


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Compal Electronics, Inc.		
Title 1.8V / 1.5V / 0.75V		
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Title				VGA_CORE/VCCP/1.1V			
Size	Document Number					Rev	
						0.1	
Date: Friday, May 02, 2008				Sheet 49 of 52			



Security Classification		Compal Secret Data		Title	
Issued Date	2007/6/22	Deciphered Date	2008/6/22	+CPU_CORE	
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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
10/12		P48	Add PR185, PR186	Reserve for debug use.
10/12		P49	Delete PC110	Because HW reserve enough CAP.
10/17		P49	Add PU11, PC136, PC141, PC142, PC139, PC110, PR187, PR188, PR189	Because need separate +VCCP and +VGA_CORE
10/17		P49	Change PR58 from 2.7k_0402_1% to 2.8k_0402_1% PR59 from 3.24k_0402_1% to 3k_0402_1%.	HW request change VGA_CORE from 1.1V to 1.16V
11/02		P49	Add PU12, PR190, PR191, PR192, PC137, PC138, PC140, PC143, PC144, PQ44	HW request add VCCIO(1.1V) for VGA use.
11/12		P47	Add PD16, PD17	To solve 3/5VALW reboot after remove AC.
11/21		P49	Add PC145	To reduce VGA_CORE ripple.
11/21		P49	Change PR51 from 44.4k to 37.4k.	To change VGA_CORE frequency to 350KHz
12/03		P48	Add PC146	To reduce 1.8VP ripple.
12/03		P47	Add PC147	To reserve for 3/5V IC 2nd source.
12/17		P48	Change PR105 from 16.9k_0402_1% to 16.5k_0402_1%, PR96 from 16.9k_0402_1% to 22k_0402_1%, PR93 from 25.5k_0402_1% to 34.8k_0402_1%.	Adjust 1.5V to 1.549V, 1.8V to 1.8V to 1.865V
12/17		P48	Add PC148.	Reserve for HW adjust power sequence.
12/27		P47, P48, P49, P50	Add PC149, PC150, PC152, PC153, PC155, PC151, PC154, PC156, PC157, PC158, PR194, PR195, PR196, PR197	For EMI request, to decrease power broadband.
12/31		P49	Change PR58 from 2.8k_0402_1% to 3k_0402_1% PR188 from 1.27k_0402_1% to 1.4k_0402_1%.	For intel request, ES2 NB need adjust VCCP to 1.1V.
02/29		P46	Add PR198, PC159.	Reserve charger sunbber.
02/29		P46	Change PR192 from 1.87k_0402_1% to 1.91k_0402_1%.	HW request adjust 1.1V to 1.12V.
02/29		P49	Change PR64 from 0_0402_5% to 100k_0402_1%, PC44 to 0.47u.	HW adjust power sequence.
03/11		P44, 46, 49	Add PC160, PC161, PC162, PC163, PC164, PC165.	EMI reqesst to solve power broadband.
03/12		P49	Add PR199, PC166.	Reserve charger sunbber.
03/11		P44, 46, 49	Add PC160, PC161, PC162, PC163, PC164, PC165.	EMI reqesst to solve power broadband.
03/12		P49	Add PR199, PC166.	Reserve charger sunbber.
04/29		P50	Add PC167, PC168, PC169	For EMI request, to decrease power broadband.

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				Document Number
				Power PIR
				LA-4141P
				0.1
Date: Tuesday, April 29, 2008				Sheet 51 of 51

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
11/12		P24	Change LVDS1 & LVDS2 connect type	
11/12		P23	Change HDMI channel	
11/12		P30	Change MDC connect JP8 , Add JP24	
11/14		P16	Remove R492, R490, R489 & R491 (I2C pull- up resistor) ,Remove R66 (HDCP)	
11/14		P16	Unstaff R486, R487, R483, R195, R192, R172, R106, R171, C116 & C183 (unused DACB & DACC)	
11/14		P17	Remove R499 (FB commend14)	
11/14		P17	Unstaff R87, R90 & C90 (FB_VREF)	
11/14		P31	MIC P/N CHANGE FROM CY000000S00 TO CYWM64P0110	
11/15		P18	Add pull down 10kohm (single LVDS signal)	
11/15		P36	Update U32 for card reader power SW (SA000024X00)	
11/22		P32	Add D24 , R526 (add WIMAX_LED# of JP22 JP23 42PIN)	
11/22		P32	delete C737,C735,708,705,C682,C681,680 (for 3G issue)	
12/05		P23	ADD R636 IN TMDS_B_HPD#	
12/11		P8	DELETE R502,R498,RR160 (DELETE DDR2 FUNCTION)	
12/11		P11	R186 CHANGE FROM 0603 TO 0805	
12/11		P28	ADD R638 CONNECT "WOL_EN" TO 3VALW	
12/17		P28	GPIO49 add 1k Ohm pulled-down resistor	
12/17		P7	REMOVE C41	
12/21		P5	U5 CHANGE FROM ADI TO SMSC (SA00001Z700)	
12/21		P10	UMA HDMI TMDS CHANGE FROM C306 TO R640 (0OHM)	
12/21		P16	ADD External Spread Spectrum (ADD U3,R55,C66,R48;DEL R99,R100)	
12/26		P30	ADD R653,R654 TO EXTERNAL MIC	
12/27		P43	CHANGE KILL SW POWER FOR +3VS TO +3VALW	
12/31		P16	UPDATE VGA_HDMI_SCL,VGA_HDMI_SDA FROM I2CD TO I2CE	
2/13		P8	CHANGE R147 FROM 511ohm TO 499ohm 1%	
2/13		P23	CHANGE THE D4 LOCATION	
2/13		P23	ADD D25,D26	
2/13		P25	ADD D27,D28,D29	
2/14		P38	CHANGE LED	
2/14		P29	CHANGE R558,R582 FROM 10ohm TO 100ohm	
2/14		P29	CHANGE C728,C738 FROM 0.1uF TO 0.1uF	
2/14		P32	JP22,JP23 PIN37,PIN43 CONNECT TO GROUND	
2/14		P23	DELETE LEVEL SHIFT CIRCUIT	
2/14		P23	ADD R659	
3/3		P10	REMOVE R240,R235 (GHCH_CRT_HSYNC,GHCH_CRT_VSYNC)	
3/3		P11	REMOVE R186 (+VCCP_PEG)	
3/3		P11	+1.5VS_TVDAC PULL DOWN	
3/3		P28	TO USE THE RSMRST CIRCUIT	
3/3		P28	ADD C804,C805,C806,C807 (ESD REQUESTION)	
3/17		P16	CHANGE R69,R71 FROM 10Kohm TO 2.2Kohm	
4/18		P36	change L41,L42 from L to 0ohm	
5/2		P5	ADD R667,C810 FOR FAN solution RC (R=1Kohm,C=10nF)	
5/2		P30	ADD R668,C811,R669 FOR MIC solution RC (R=1Kohm,C=10uF) , INT_MIC CONNECT TO U15 PIN23	
5/2		P42	ADD R670,R671,R672 FOR AO4468 VGS ISSUE solution	

Title			<Title>
Size	Document Number	Rev	
B	<Doc>	<RevCode>	
Date:	Friday, May 02, 2008	Sheet	52 of 52