

ACL10 LA-1331 Schematics Document

REV 2.0 (For 030)

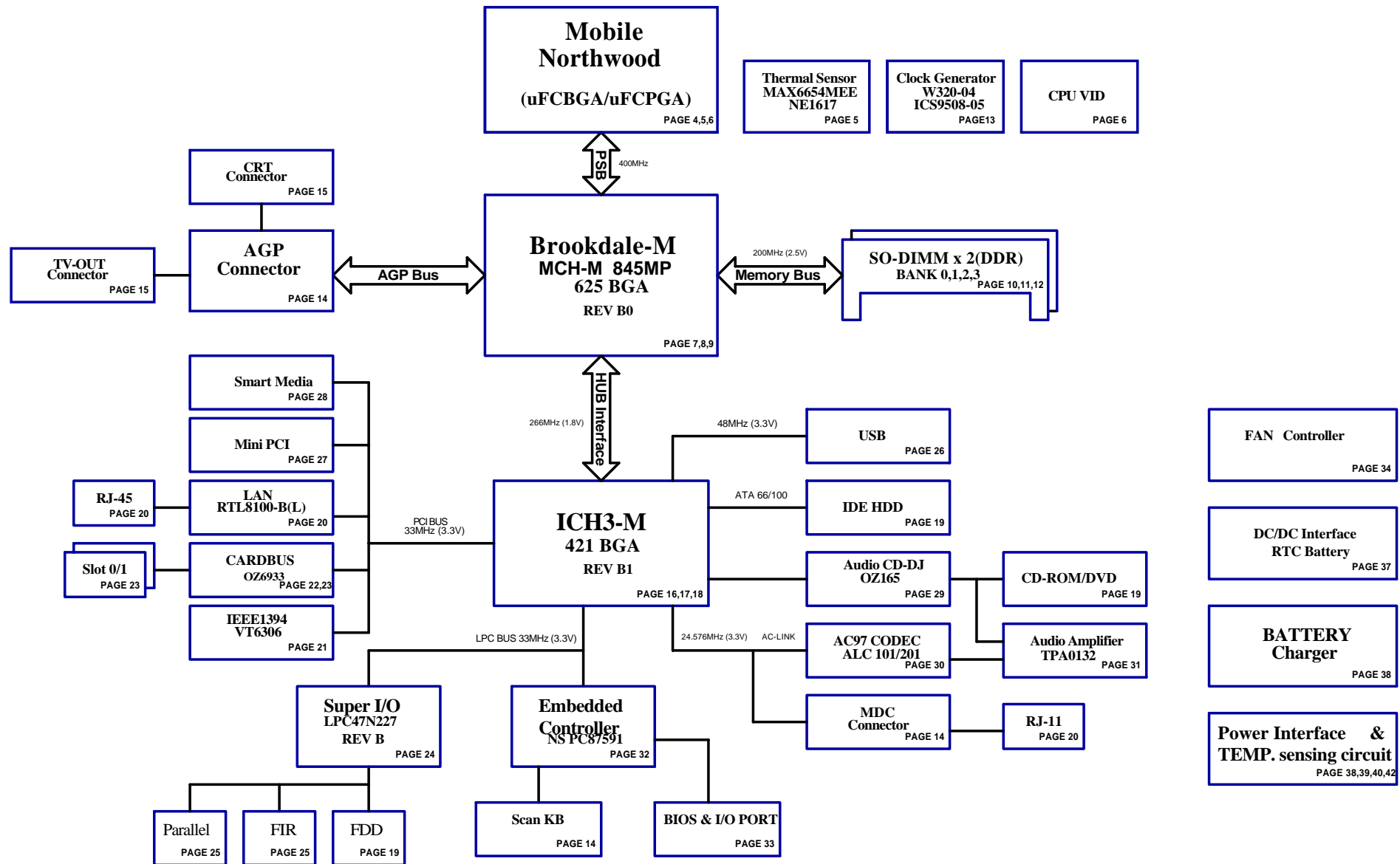
**INTEL Mobile P4 uFCBGA/uFCPGA Northwood
MCH-M(845-MP) + ICH3-M + SQ17**

COMPAL ELECTRONICS, INC		
Title		
SCHEMATIC, WB LA-1331		
Size	Document Number	Rev
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ACL10 LA-1331 BLOCK DIAGRAM



Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	NA	NA	NA
B+	AC or battery power rail for power circuit.	NA	NA	NA
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
1.2VP	1.2VP switched power rail for CPU VID	ON	OFF	OFF
+1.25VS	1.25VS power rail	ON	OFF	OFF
+1.5VS	AGP 4X	ON	OFF	OFF
+1.8VALW	1.8V always power rail	ON	ON	ON*
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5V	2.5V power rail	ON	ON	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5V	5V power rail	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
+12V	12V power rail	ON	ON	OFF
+12VS	12V switched power rail	ON	OFF	OFF
RTCVCC	RTC power	ON	ON	ON
+SDREF	+SDREF power	ON	ON	OFF

Note : "ON*" means that this power plane is "ON" only with AC power available, otherwise it is "OFF".

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
IEEE 1394	AD16	0	PIRQA
Mini-PCI	AD18	1/4	PIRQC/PIRQD
CardBus	AD20	2	PIRQA/PIRQB
LAN	AD17	3	PIRQB
SM	AD22	-	PIRQC/PIRQD

EC SM Bus1 address

Device	Address
Smart Battery	0001 011Xb
EEPROM(24C16/02)	1010 000Xb
(24C04)	1011 000Xb

EC SM Bus2 address

Device	Address
MAX6654MEE	1001 110Xb
OZ165	1011 0100b (B4h)
Smart Battery	0001 011Xb
Docking	0011 011Xb
DOT Board	XXXX XXXXb

ICH3-M SM Bus address

Device	Address
Clock Generator W320-04 / ICS9508-05	1101 0000

DDR SODIMM SM Bus address

DDR SLOT	SA2	SA1	SA0
DDR SODIMM0 (REVERSE)	0	0	0
DDR SODIMM1 (NORMAL)	0	0	1

PIR

REV 0.1

Date	Page	Description
2001/12/29	7	Change R212,R214 & R213 to 8.2K ohm for Intel recommend
2001/12/29	14	Stuff R361=22 Ohm and no-stuff R360 for Data-IN1 of MDC module.
2001/12/29	15	Change L28 & L29 to 0 Ohm for EMI issue.
2001/12/29	16	Change R39 power-plane to +3VALW for Resume-well Power-plane(+3VALW)
2001/12/29	17	DEL C73, C87, C371 for EMI issue.
2001/12/29	17	Change L37 power-plane to +1.8VS for Intel recommend.
2001/12/29	17	Change R279 power-plane to +3VS for Intel recommend.
2001/12/29	17	Change U29 pinV22,U18 & P14 power-plane to +CPU_CORE for Intel recommend.
2001/12/29	17	Change R284 power-plane to +3VALW for Intel recommend.
2001/12/29	18	Change "SMB_ALERT#" power-plane to +3VALW for "RESUME-WELL" power-plane(+3VALW).
2001/12/29	18	Exchang D13,D14,D16,D17,D18 and R28,R34,R30,R29 to RP135,R466,R468 for cost-down.
2001/12/29	20	Add D43 for leakage.
2001/12/29	21	Exchang L42 to L52,L53, L54, L55 for ME limitation.
2001/12/29	27	Add D42 for leakage.
2001/12/29	31	Add R465 for PC99 Spec.
2001/12/29	34	Add C368, C369 for EMI solution.
2001/12/29	35	EC control "EC_RSMRST#". ->DEL R92, Stuff R48.
2001/12/29	35	Change R97 to 100K for "VGATE" of Max1718A issue.-> Change PR134= 0 Ohm.
2002/01/07	39	Change PR68 from 10k_1% to 10.5k_1%.(increase 5valwp to 5.125v).
2002/01/07	40	Change PR81 from 2.15k_1% to 1.87k_1%.(CPU thermal OTP from 83+-3C to 85+-3C).
2002/01/07	42	Add PR147, PR161 to 2.7_0805. for EMI requirement.
2002/01/07	42	Add PC120, PC121, PC122 to 1000pf. for ESD.
2002/01/07	42	Add PQ44 to 2N7002 for CPU SPEED STEP.
2002/01/07	42	Change PR130, PR152 from 0 to 2.2. for EMI requirement.
2002/01/07	42	Change PR143 from 53.6k_1% to 100k_1%. for CPU OCP.
2002/01/07	42	Change PR145 from 100k_1% to 53.6k_1%. for CPU OCP.
2002/01/07	42	Change PR148 from 30k_1% to 48.7k_1%. for CPU OCP.
2002/01/07	42	Change PU12 VIN from +2.5VP to +3VALWP.

REV 0.2

Date	Page	Description
2002/01/11	40	Change PH1 and PH2 design by high active for AC-IN issue.

REV 0.3

Date	Page	Description
None		

REV 1.0

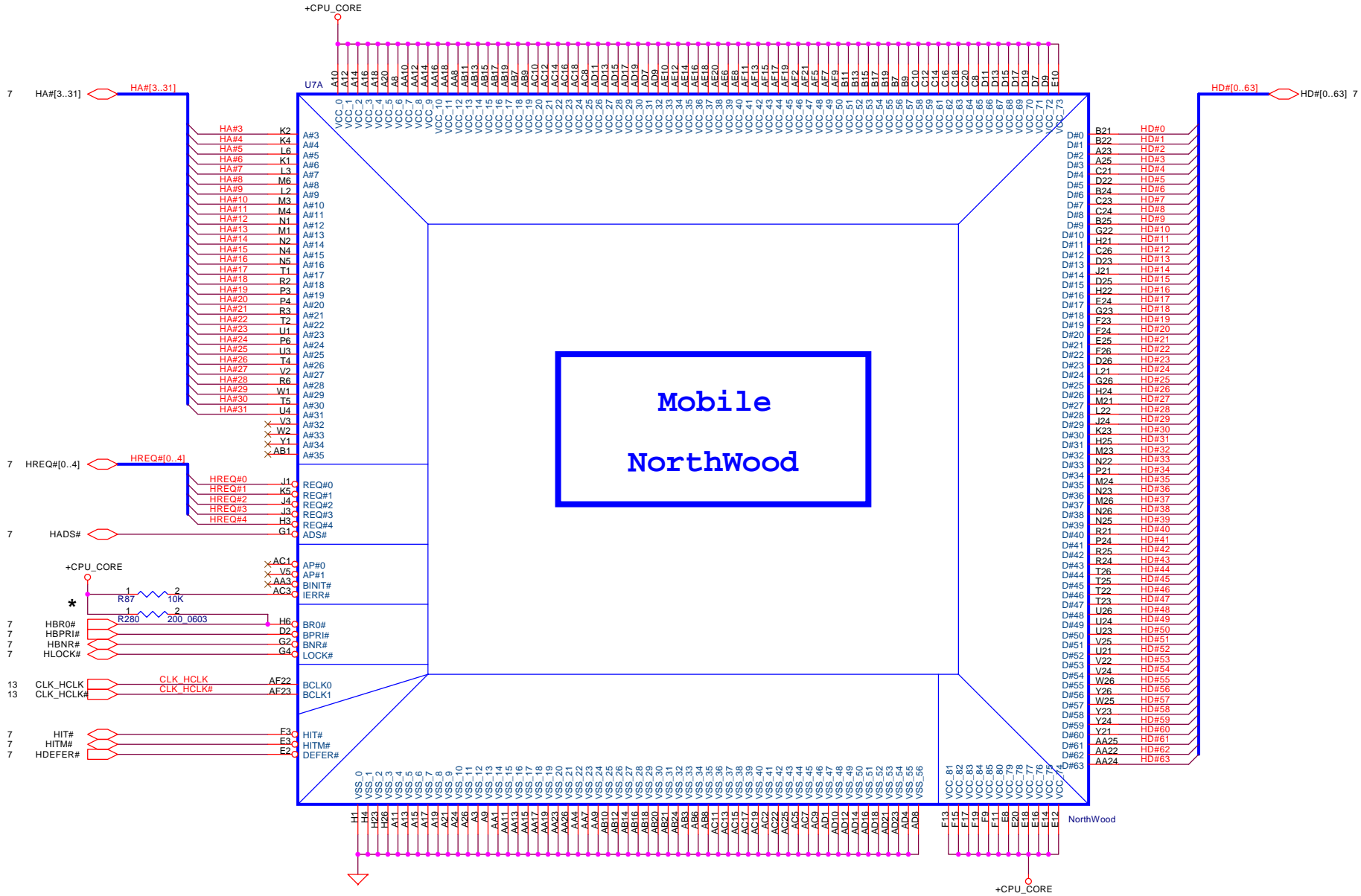
Date	Page
None	

REV 2.0

Date	Page	Description
2002/04/10	20	GCR: (For LAN Issue) <1>-Isolation U18 pin6 for Realtek application notice. <2>-Change R204 from 5.9K+-1% to 5.6K +-1%. <3>-Change L23 from 4.7UH to 0 ohm.

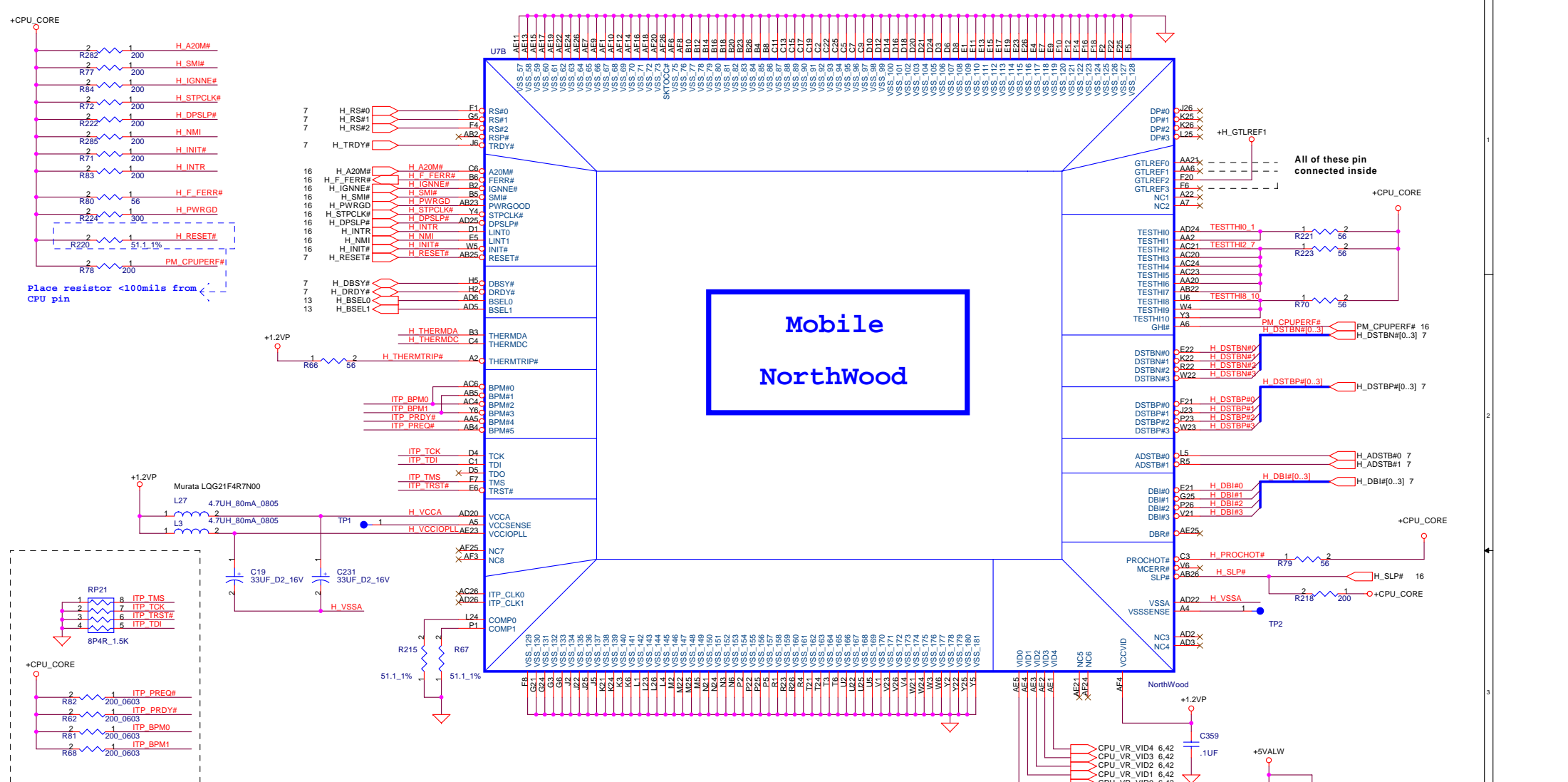
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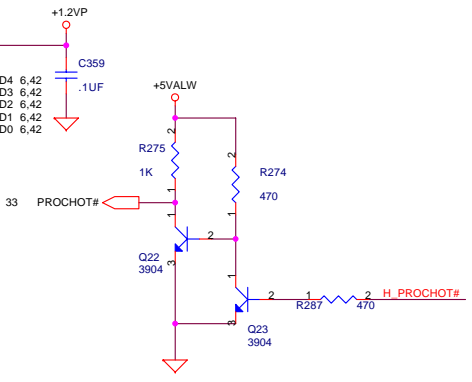
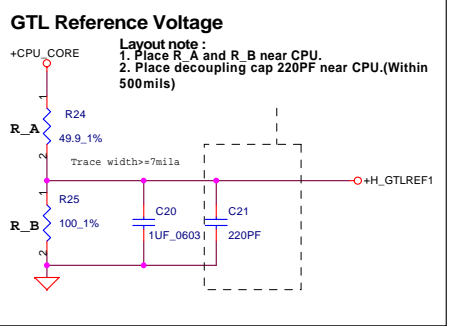
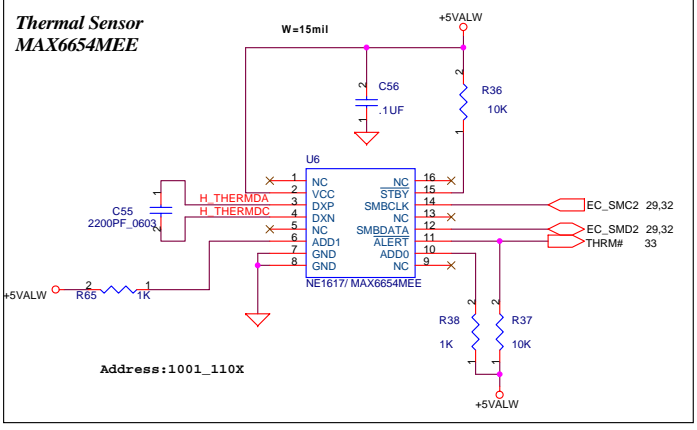
**Mobile
NorthWood**

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Place resistor <100mils from CPU pin

Mobile NorthWood

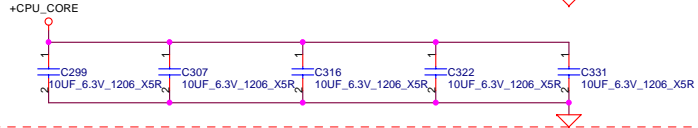
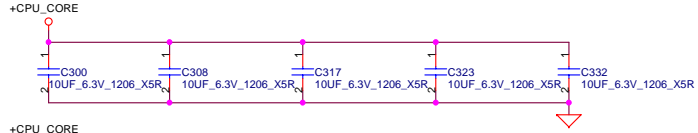


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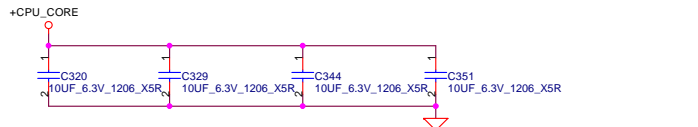
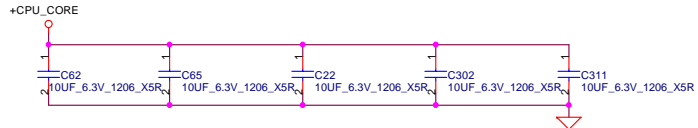
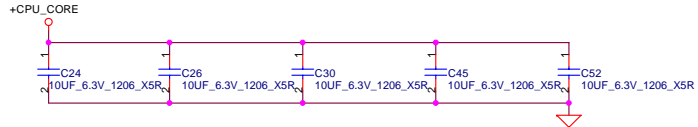
Layout note :

Place close to CPU. Use 2-3 vias per PAD.
 Place 22uF caps underneath balls on solder side.
 Place 10uF caps on the peripheral near balls.
 Use 2-3 vias per PAD.

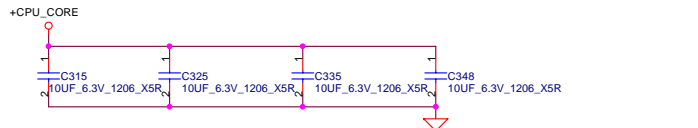
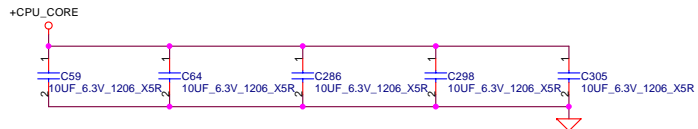
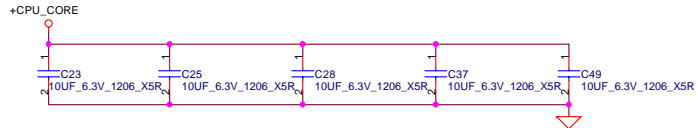
Please place these cap in the socket cavity area



Please place these cap on the socket north side



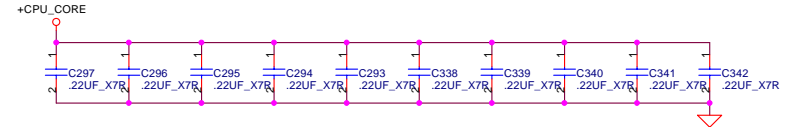
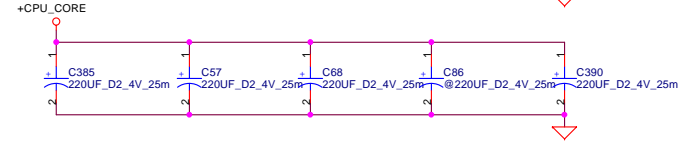
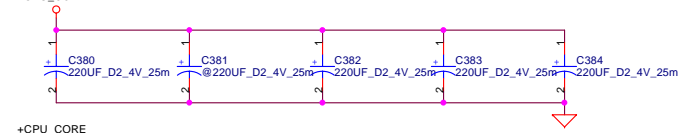
Please place these cap on the socket south side



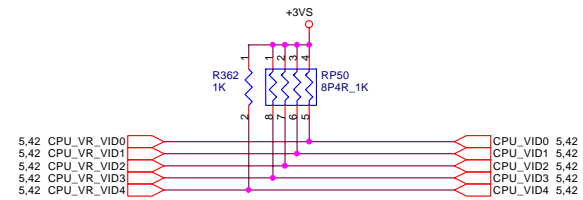
Layout note :

Place close to CPU power and ground pin as possible (<1inch)

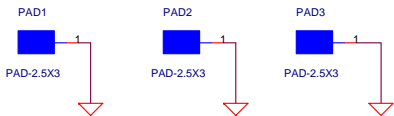
Used ESR 25m ohm cap total ESR=2.5m ohm



CPU Voltage ID



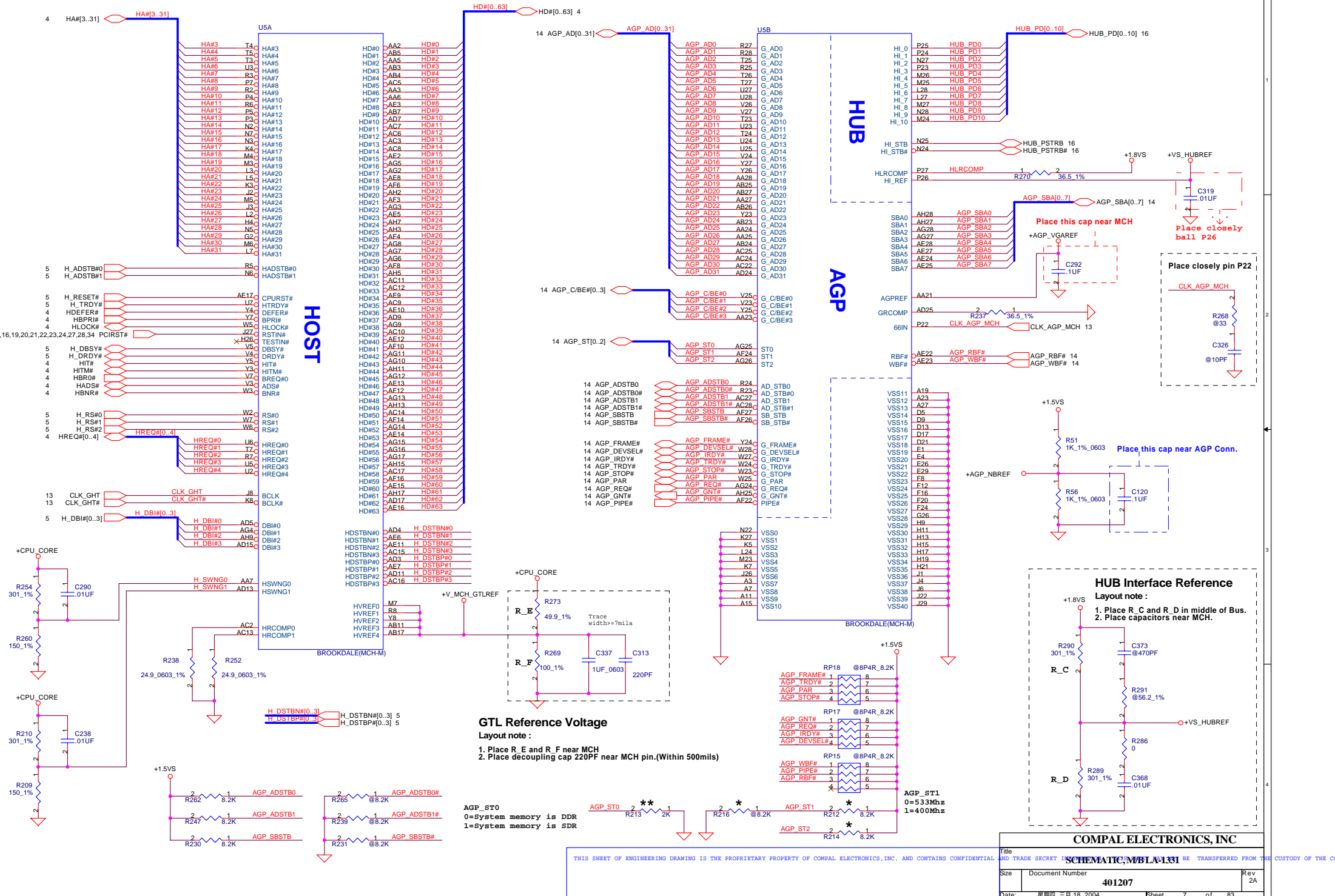
EMI Clip PAD for CPU



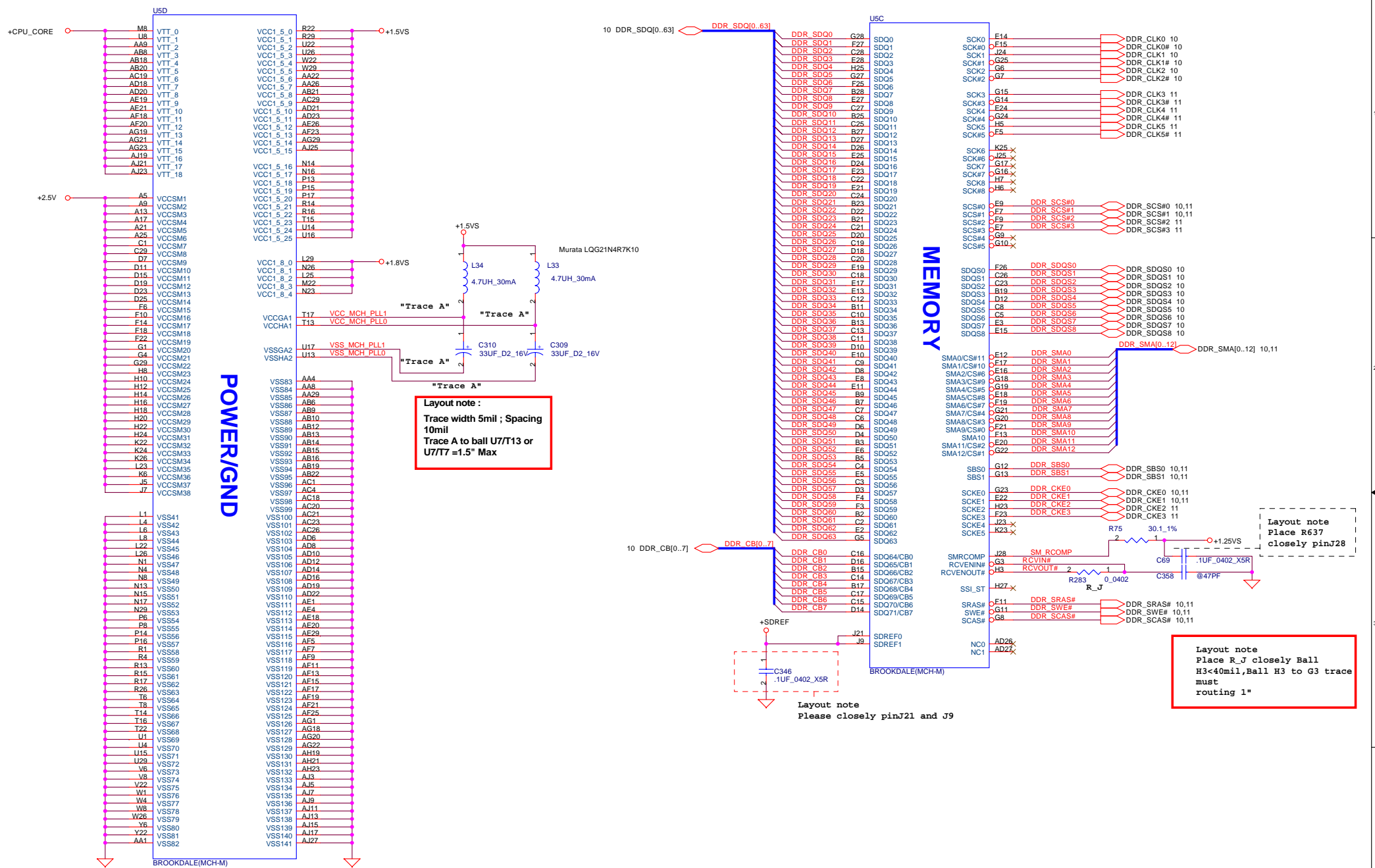
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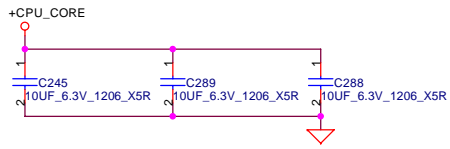
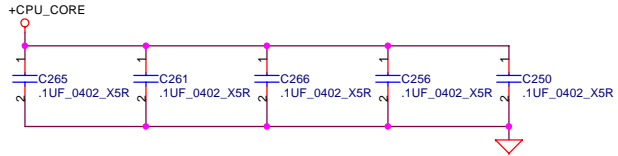
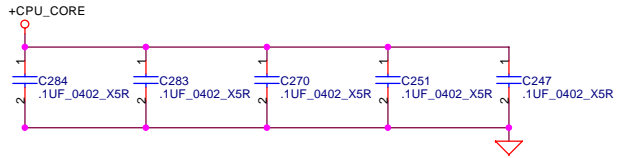
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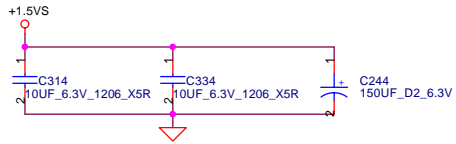
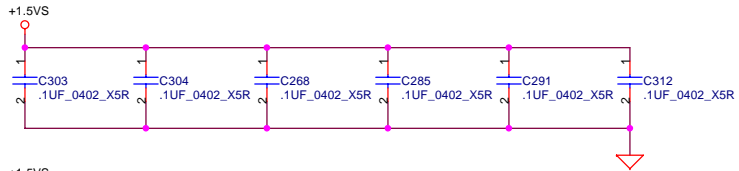
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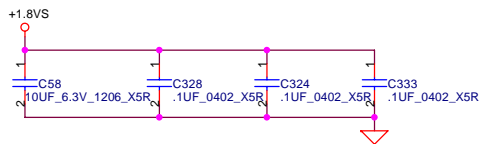
Layout note : Processor system bus
 Distribute as close as possible
 to MCH Processor Quadrant.(between VTTF5B and VSS pin)



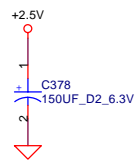
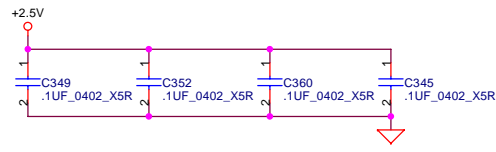
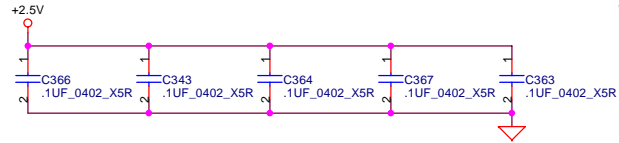
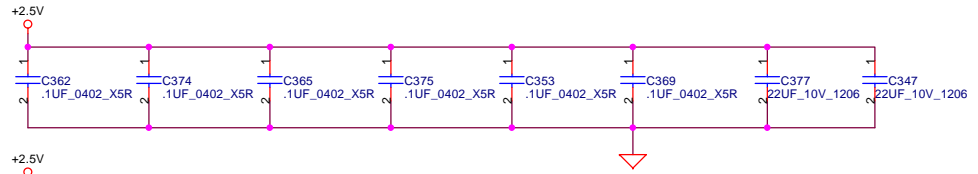
Layout note : AGP/CORE
 Distribute as close as possible
 to MCH Processor Quadrant.(between VCCAGP/VCCCORE
 and VSS pin)



Layout note : Hub-Link
 Distribute as close as possible
 to MCH Processor Quadrant.(between VCCHL and VSS pin)

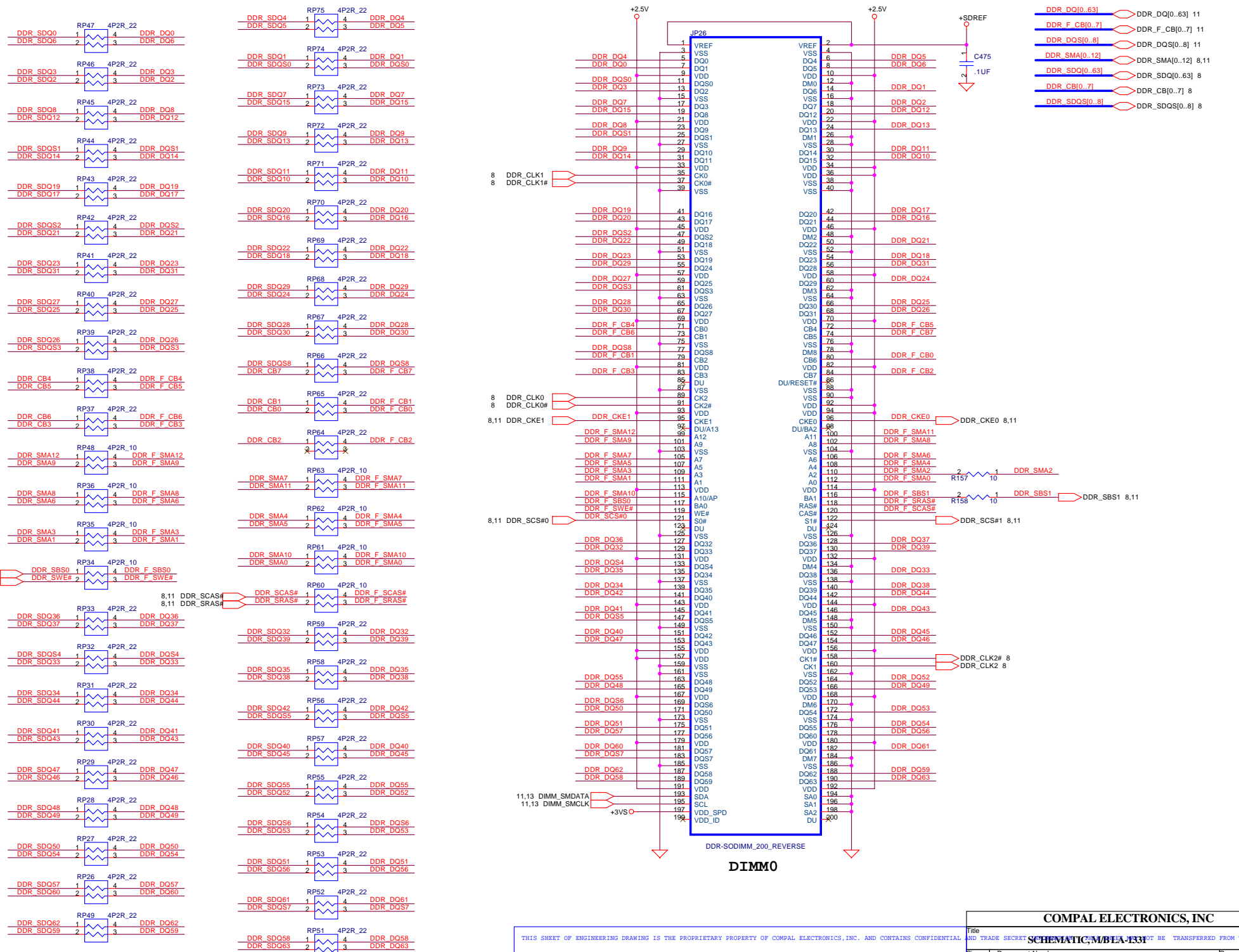


Layout note : DDR Memory interface
 Distribute as close as possible
 to MCH Processor Quadrant.(between VCCSM and VSS pin)



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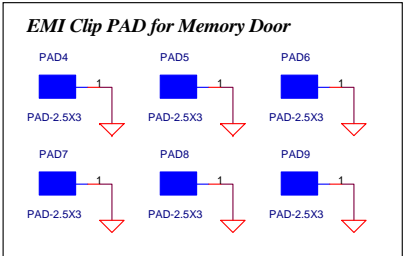
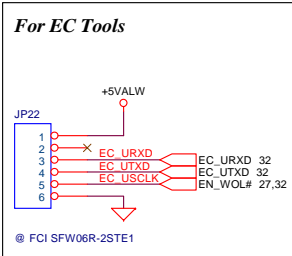
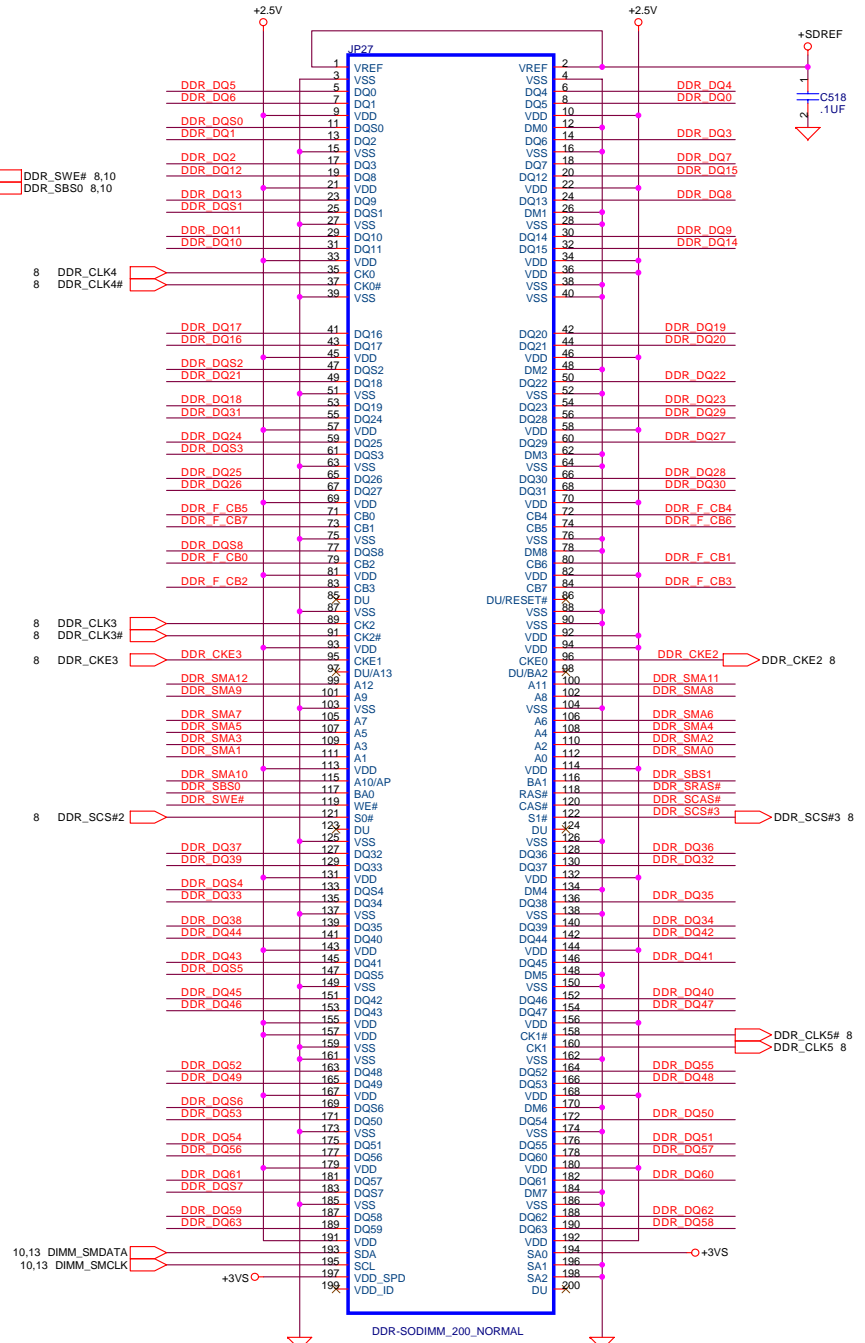
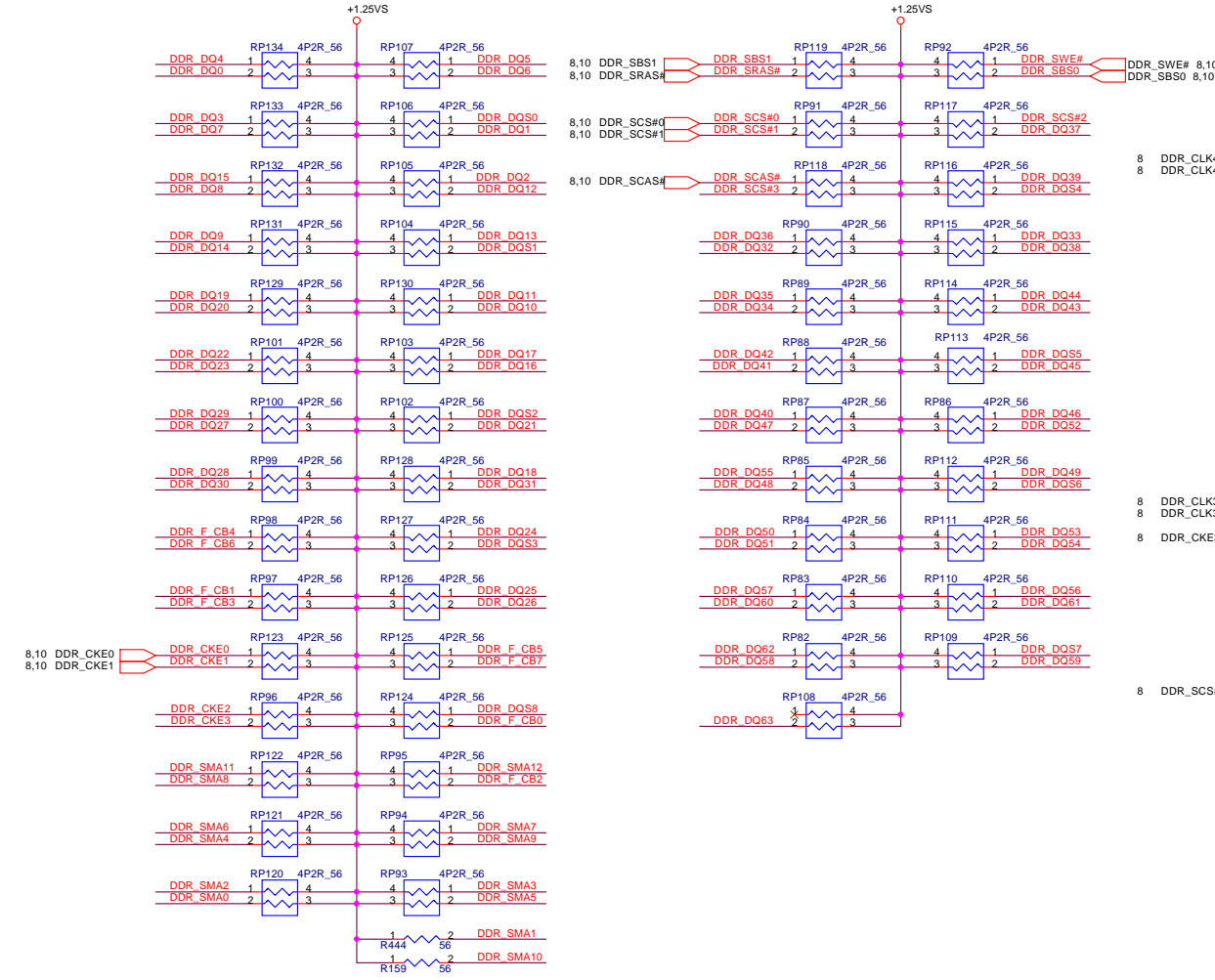
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- 10 DDR_F_CB[0..7] \rightarrow DDR_F_CB[0..7]
- 10 DDR_DQS[0..8] \rightarrow DDR_DQS[0..8]
- 10 DDR_DQ[0..63] \rightarrow DDR_DQ[0..63]
- 8,10 DDR_SMA[0..12] \rightarrow DDR_SMA[0..12]



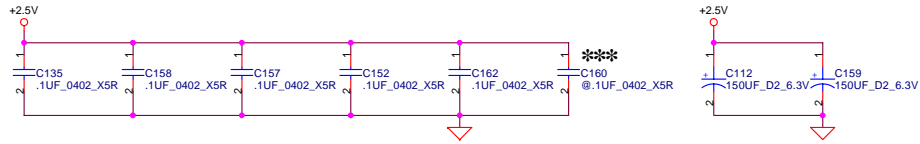
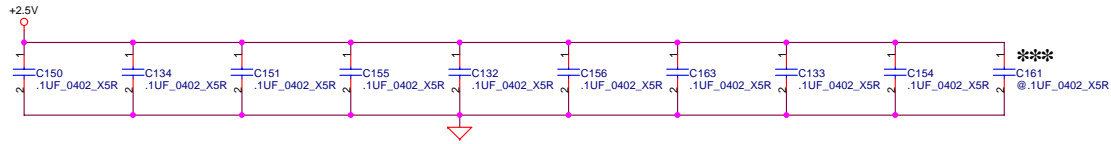
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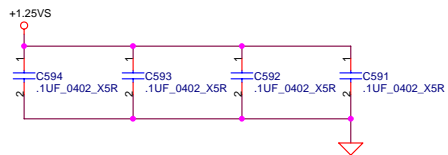
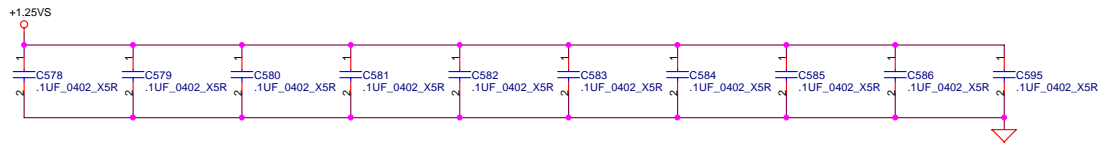
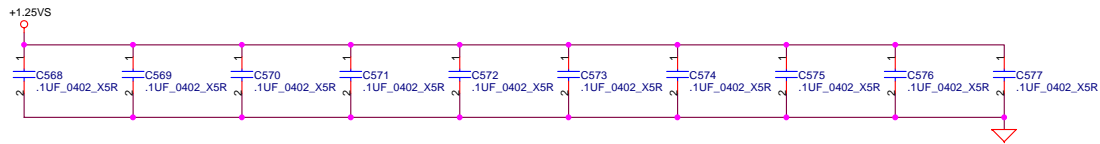
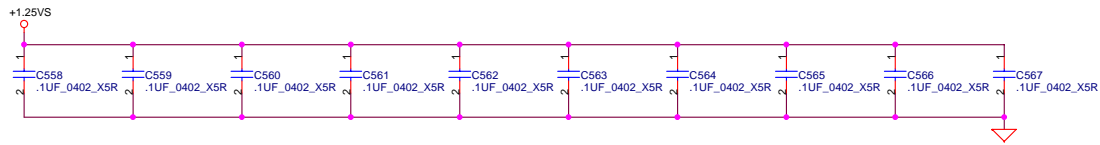
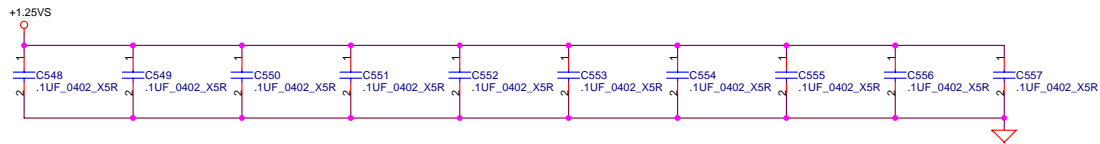
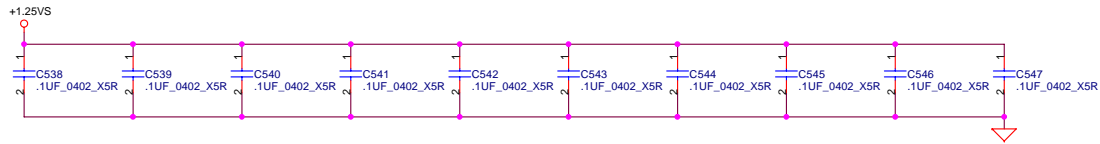
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Layout note :
Distribute as close as possible to DDR-SODIMM.



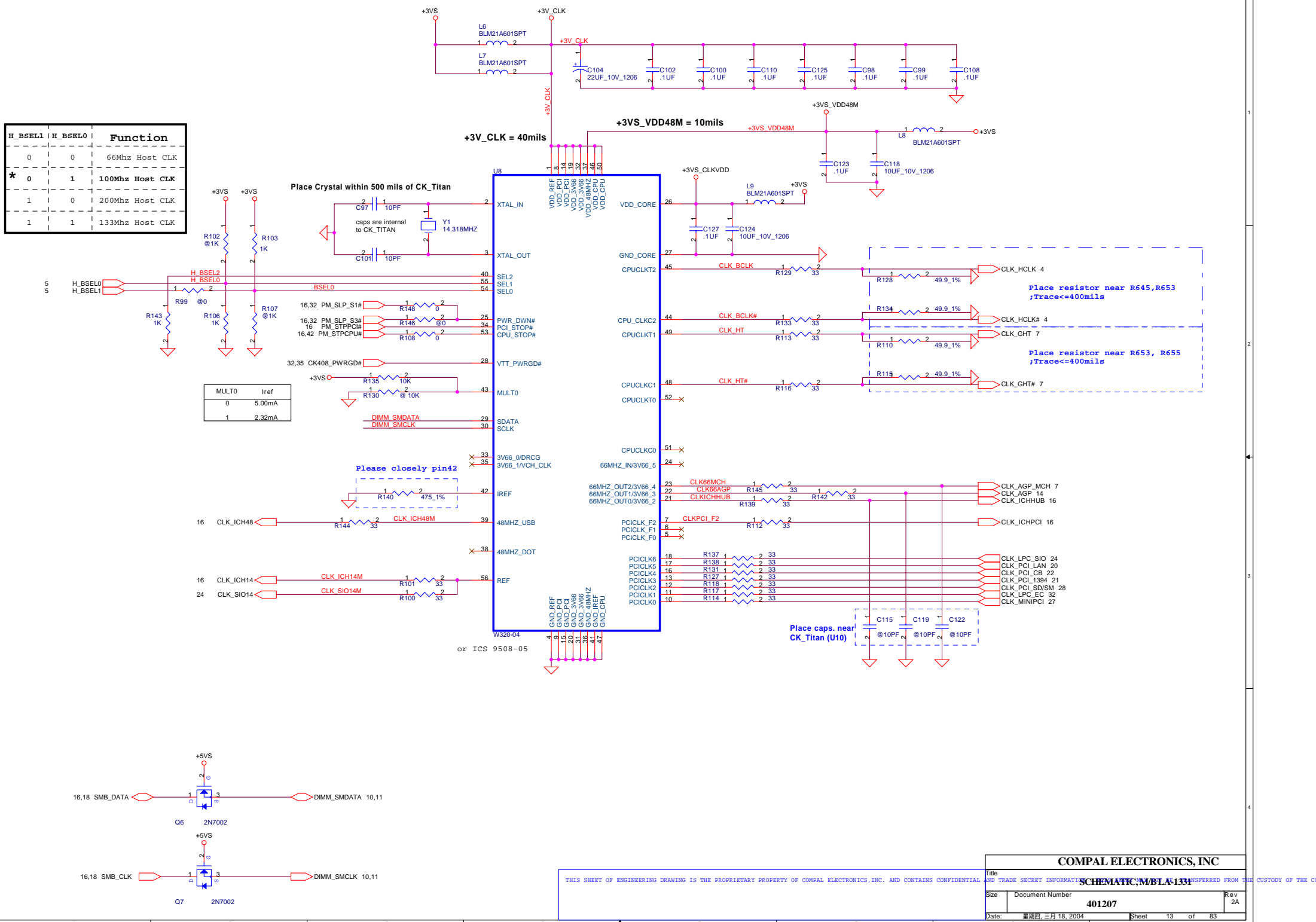
Layout note :
Place one cap close to every 2 pull up resistors termination to +1.25V



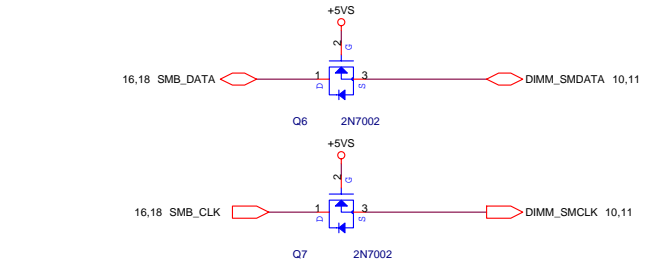
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H_BSEL1	H_BSEL0	Function
0	0	66Mhz Host CLK
* 0	1	100Mhz Host CLK
1	0	200Mhz Host CLK
1	1	133Mhz Host CLK



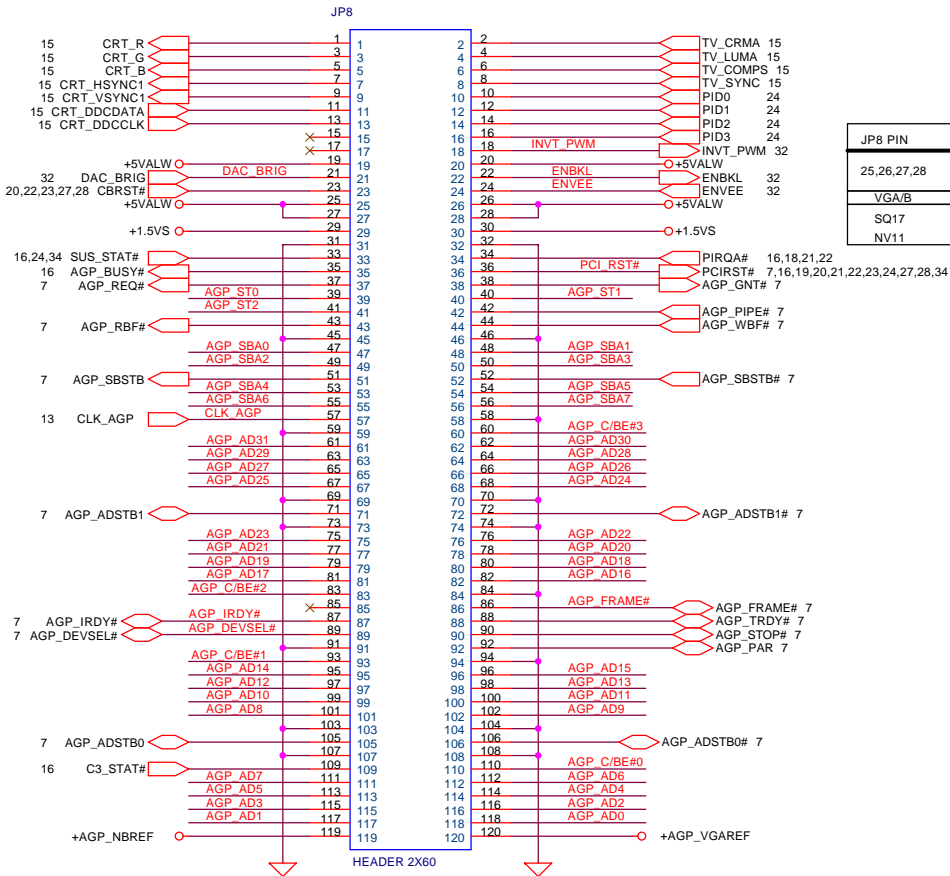
MULT0	Iref
0	5.00mA
1	2.32mA



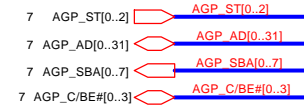
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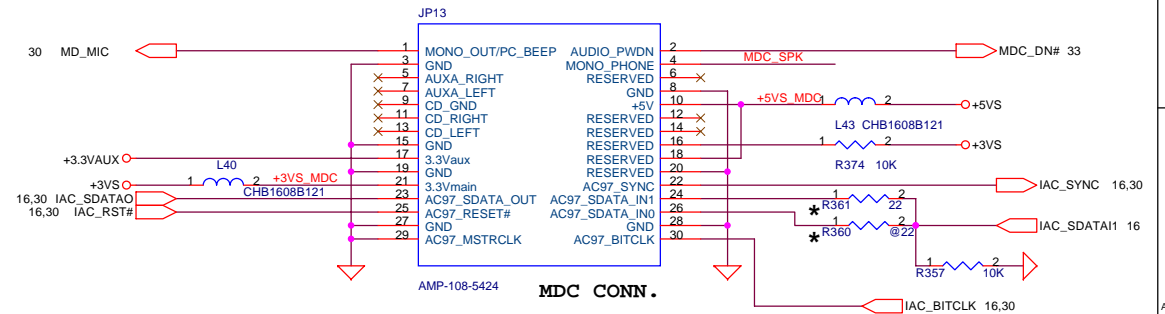
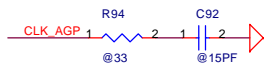
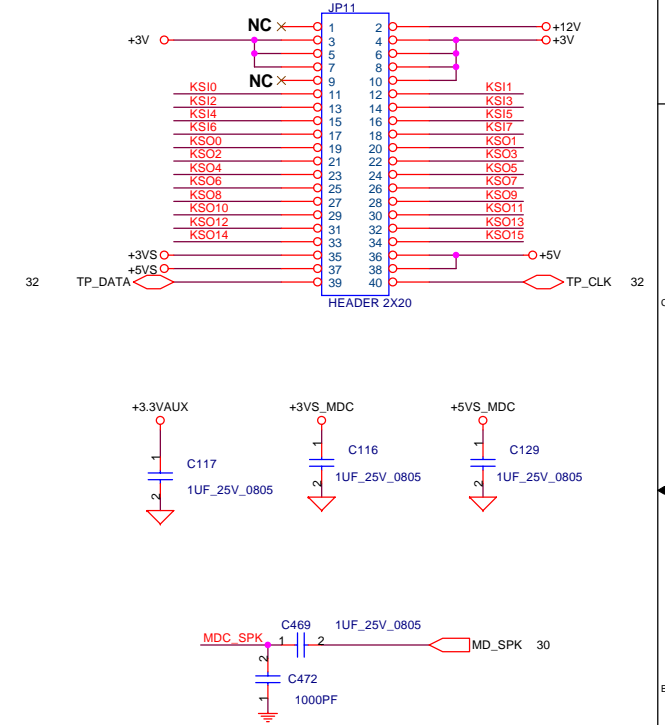
AGP CONN.



JP8 PIN	ACL10	ATL02/ACL00
25,26,27,28	+5VALW	+1.5V
VGA/B		
SQ17	V	X
NV11	V	V



Int. Keyboard CONN.

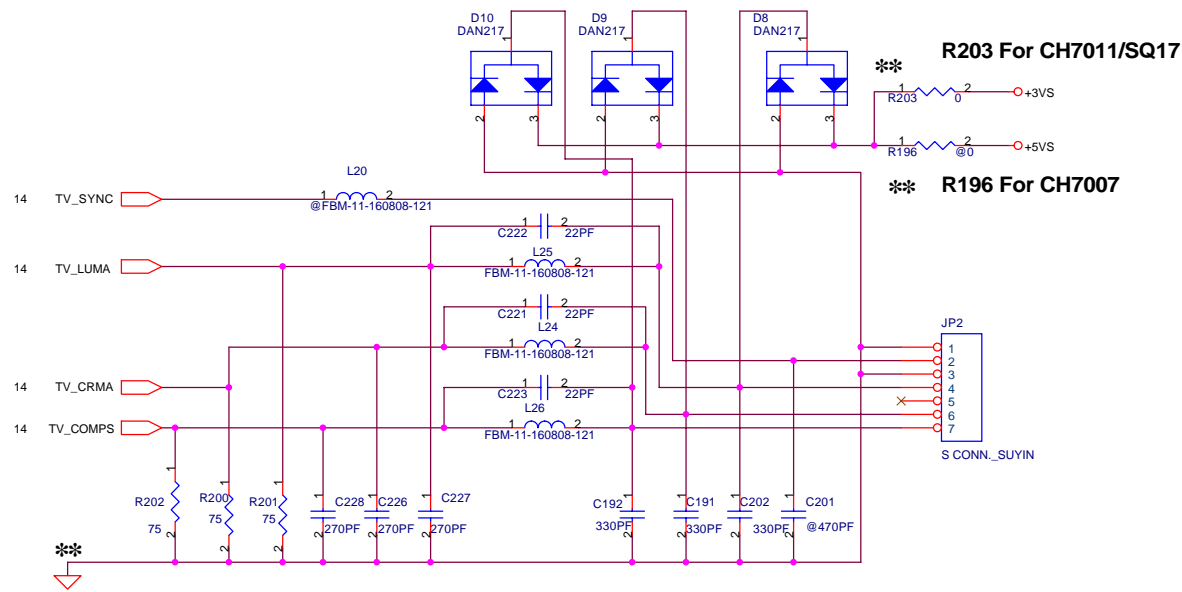


COMPAL ELECTRONICS, INC

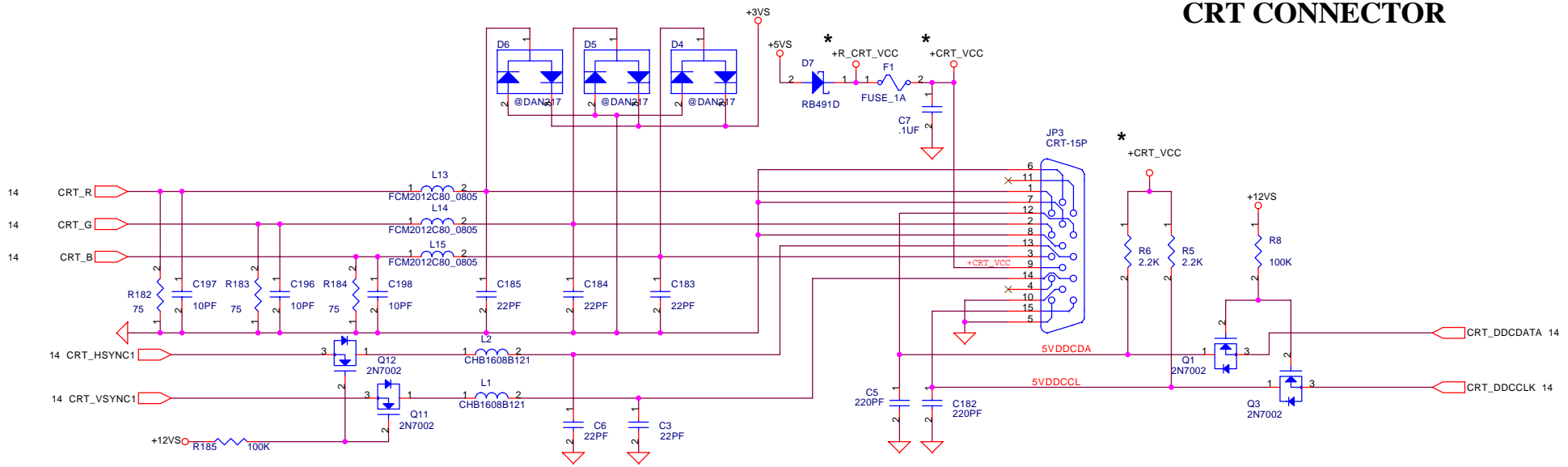
SCHEMATIC, M/B LA-1331

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TV_OUT CONNECTOR



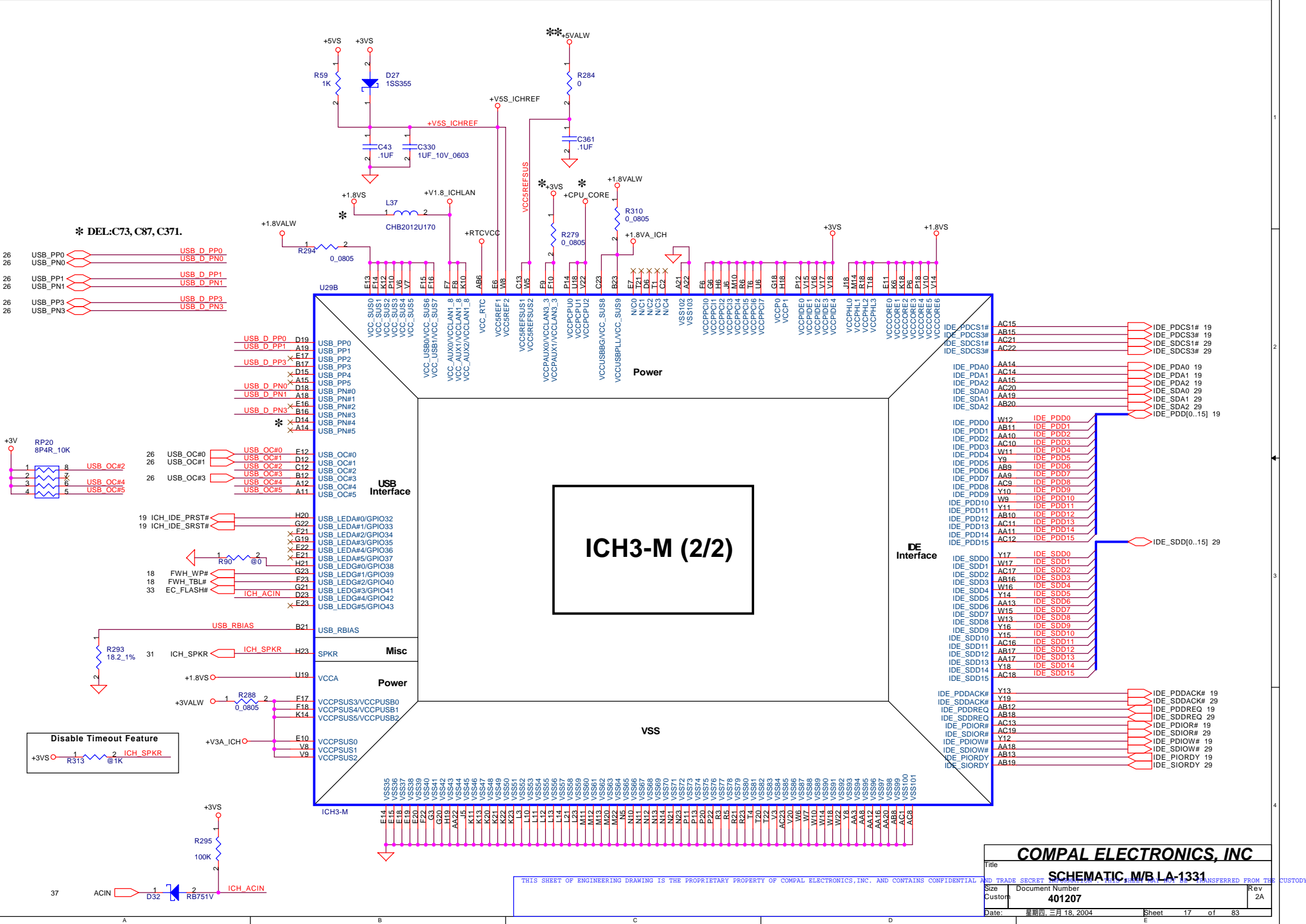
CRT CONNECTOR

COMPAL ELECTRONICS, INC

SCHEMATIC, M/B LA-1331

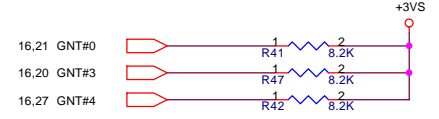
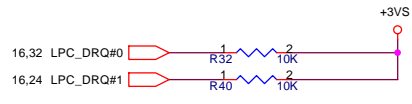
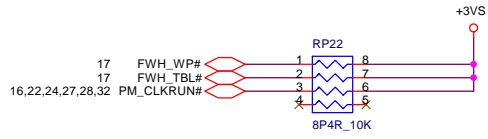
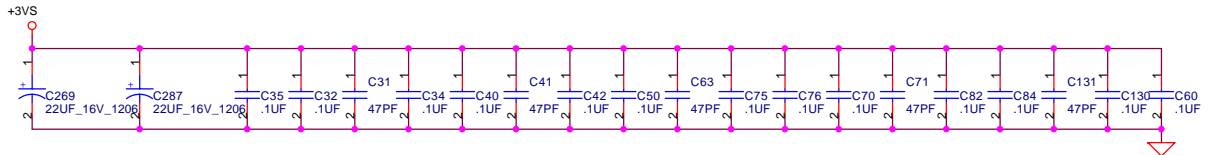
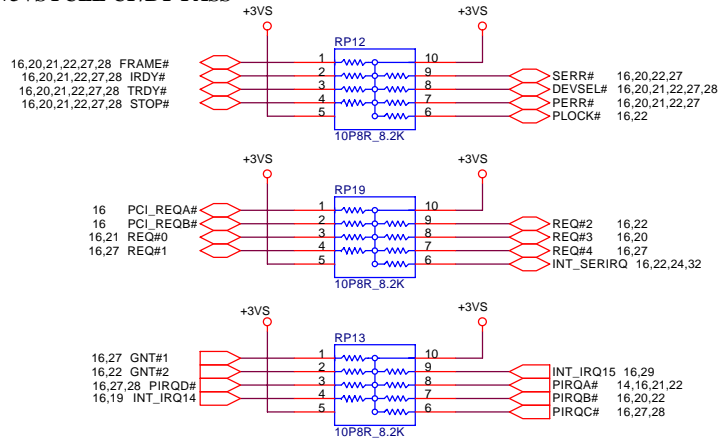
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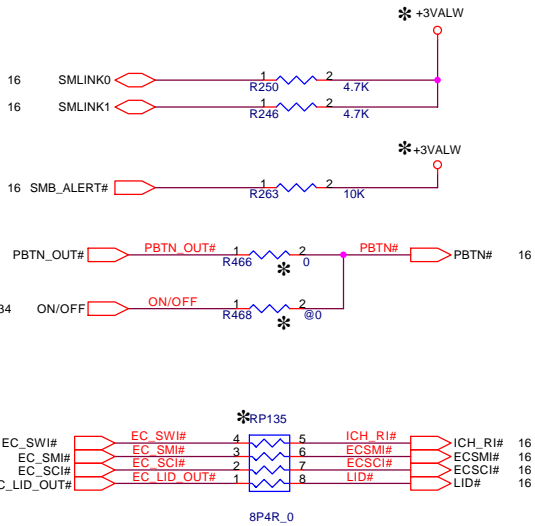


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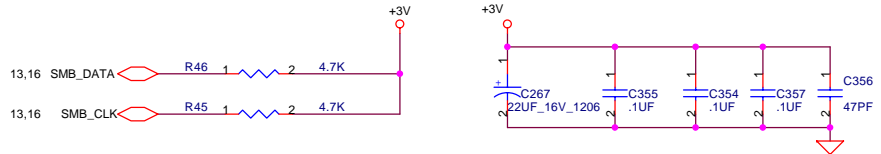
+3VS PULL-UP/BY-PASS



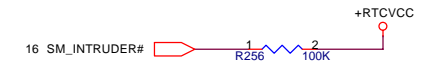
+3VALW PULL-UP



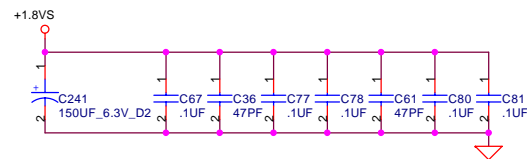
+3V PULL-UP/BY-PASS



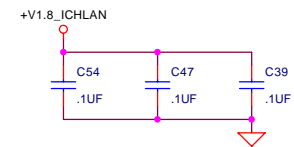
+RTCVCC PULL-UP



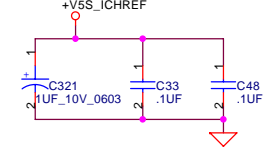
+1.8SV BY-PASS



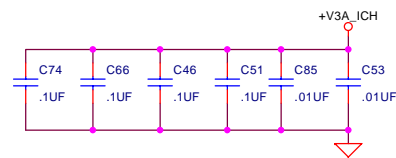
+V1.8S_ICHLAN BY-PASS



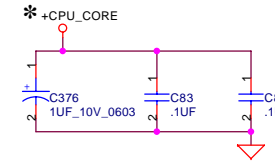
+V5S_ICHREF BY-PASS



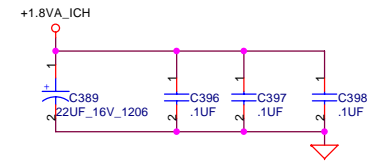
+V3A_ICH BY-PASS



+CPU_CORE BY-PASS



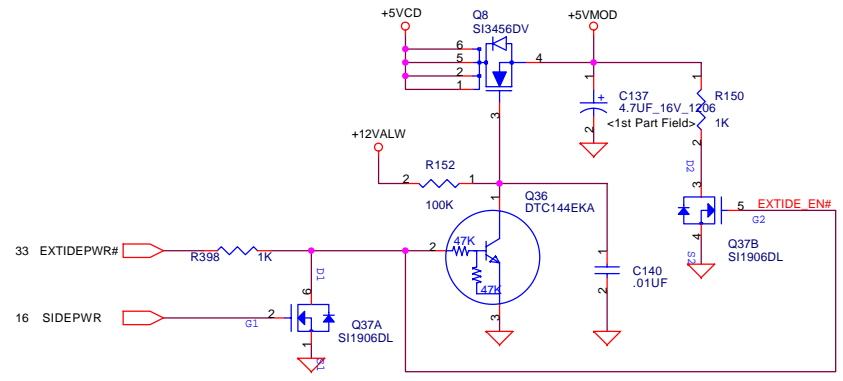
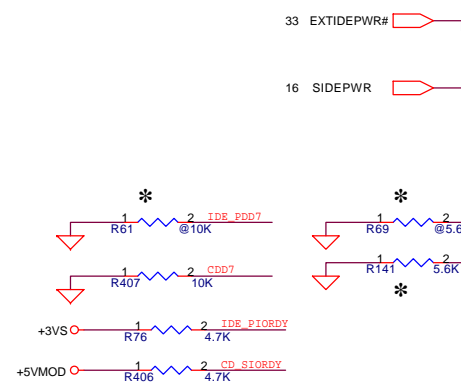
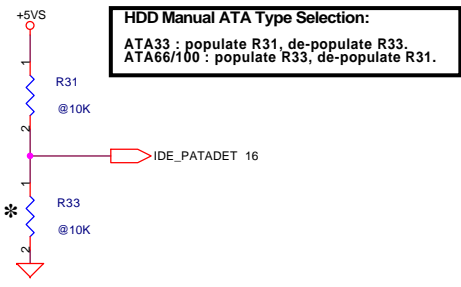
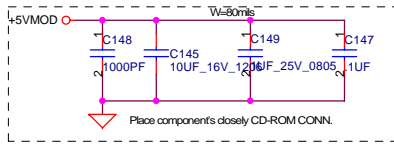
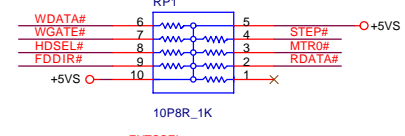
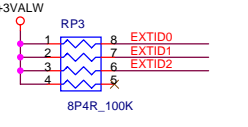
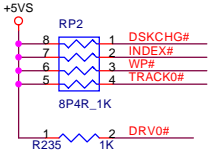
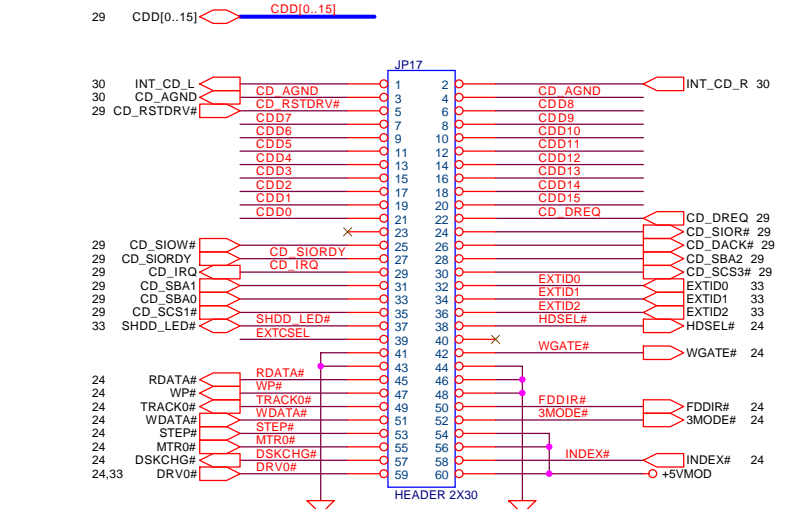
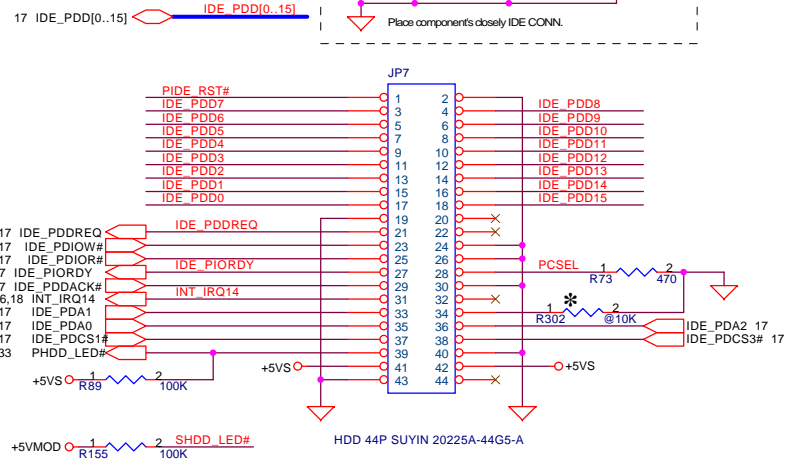
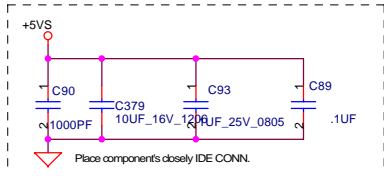
+1.8VA_ICH BY-PASS



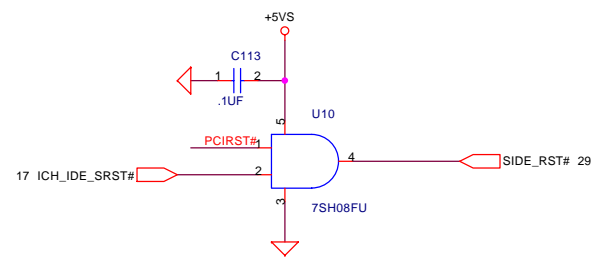
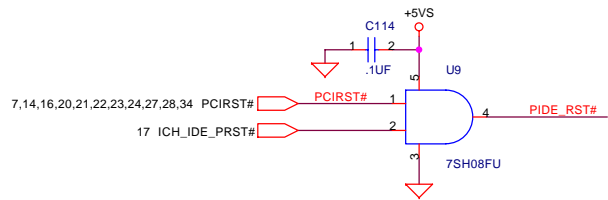
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IDE, CD-ROM Module CONN.

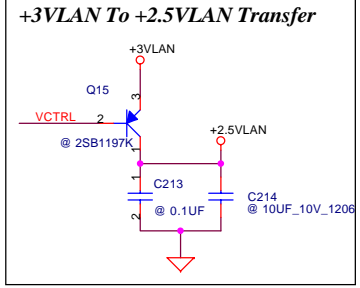
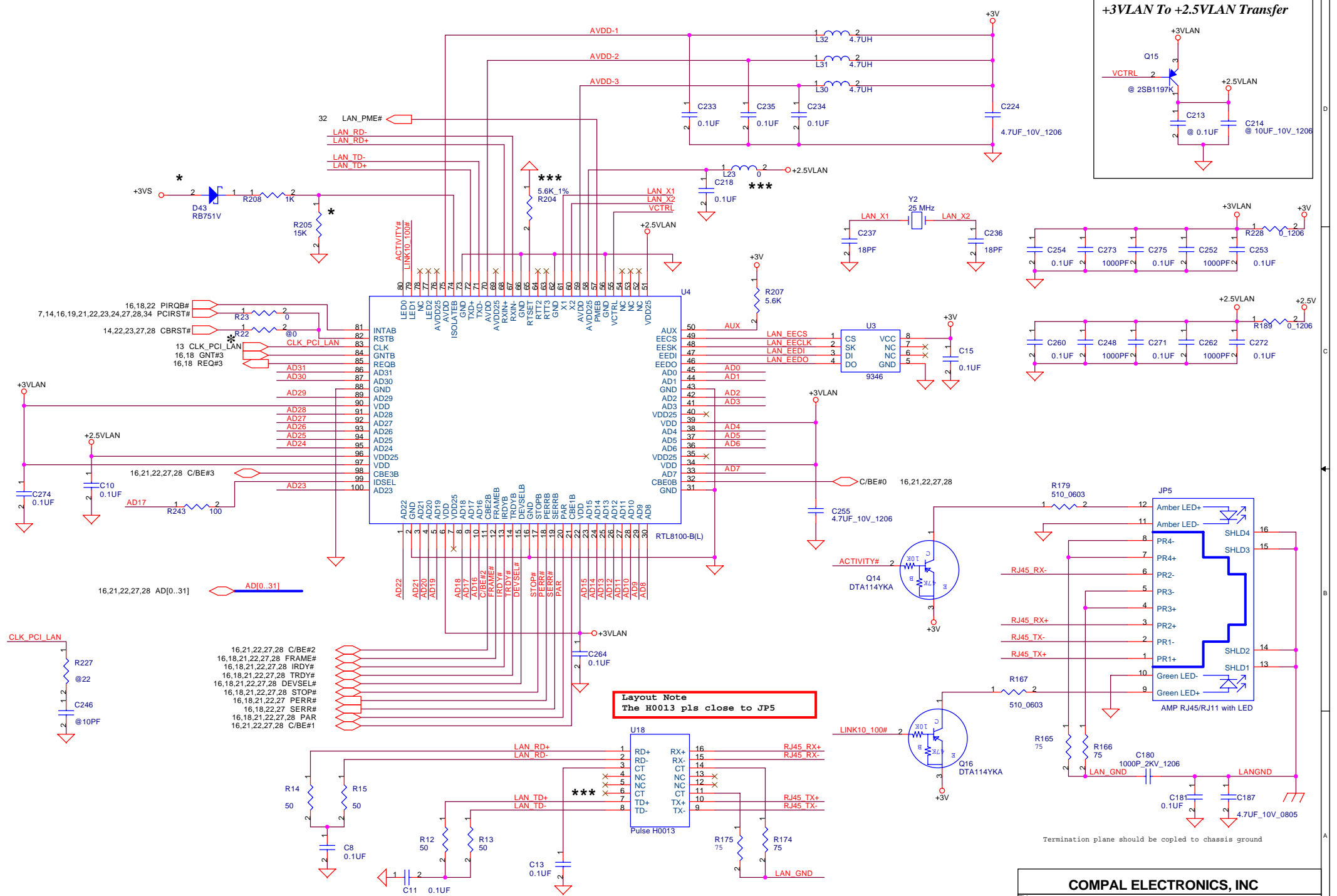


SI3456DV: N CHANNEL
 VGS: 4.5V, RDS: 65 mOHM
 Id(MAX): 5.1A
 VGS,+20V



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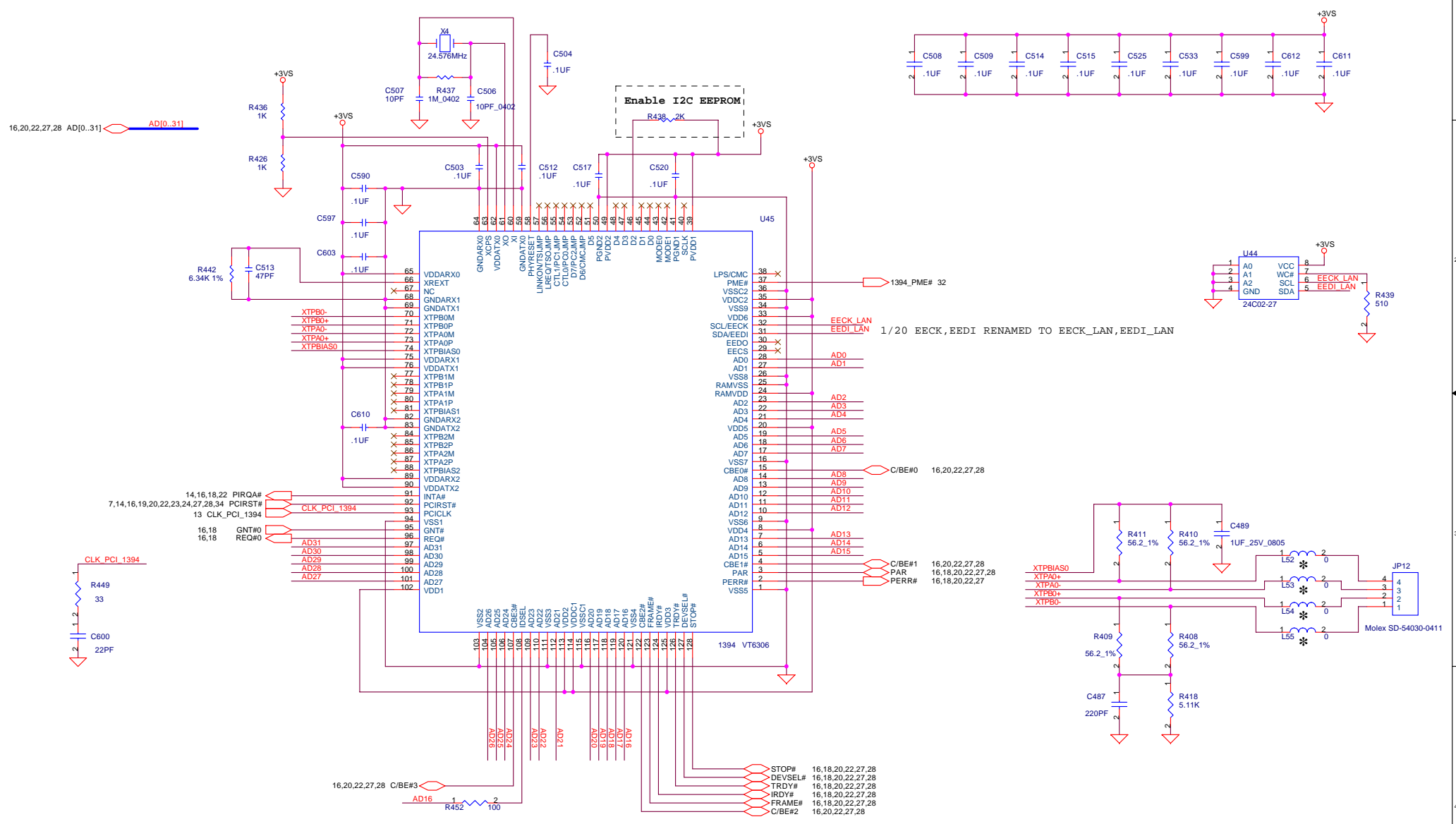


Layout Note
The H0013 pls close to JP5

Termination plane should be copled to chassis ground

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CardBus Controller OZ6933T (uBGA)

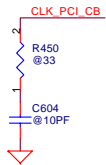
S1_IOWR# S1_IOWR# 23
S1_IORD# S1_IORD# 23
S1_OE# S1_OE# 23
S1_CE2# S1_CE2# 23

16,20,21,27,28 AD[0..31]

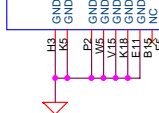
16,20,21,27,28 C/BE#3
16,20,21,27,28 C/BE#2
16,20,21,27,28 C/BE#1
16,20,21,27,28 C/BE#0

13 CLK_PCI_CB
16,18,20,21,27,28 DEVSEL#
16,18,20,21,27,28 FRAME#
16,18,20,21,27,28 IRDY#
16,18,20,21,27,28 TRDY#
16,18,20,21,27,28 STOP#
16,18,20,21,27,28 PAR#
16,18,20,21,27 PERR#
16,18,20,27 SERR#
16,18 REQ#2
16,18 GNT#2
14,16,18,21 PIRQA#
16,18,20 PIRQB#
16,18 PLOCK#
7,14,16,19,20,21,23,24,27,28,34 PCIRST#

32 PCM_PME#
16,18,24,27,28,32 PM_CLKRUN#
28 PCM_RI#
31 PCM_SPK#
33 PCM1_LED
33 PCM2_LED
16,18,24,32 INT_SERIRQ



CardBus-OZ6933T-1

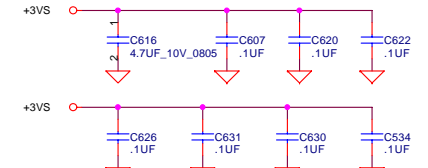
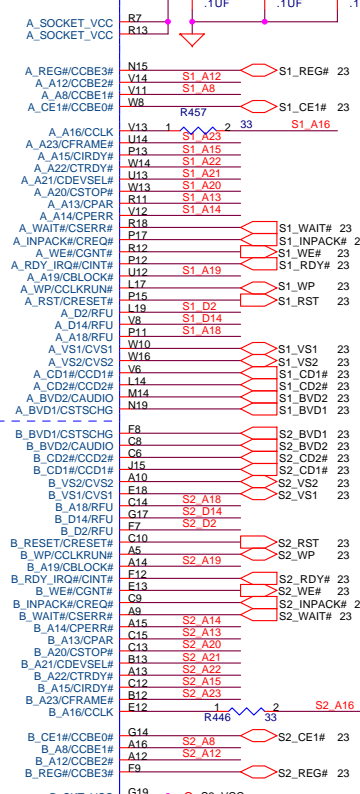
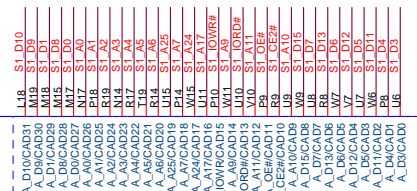


O₂ MICRO
CARDBUS CONTROLLER
OZ6933 209PIN CSP

PCI

Slot
A

Slot
B



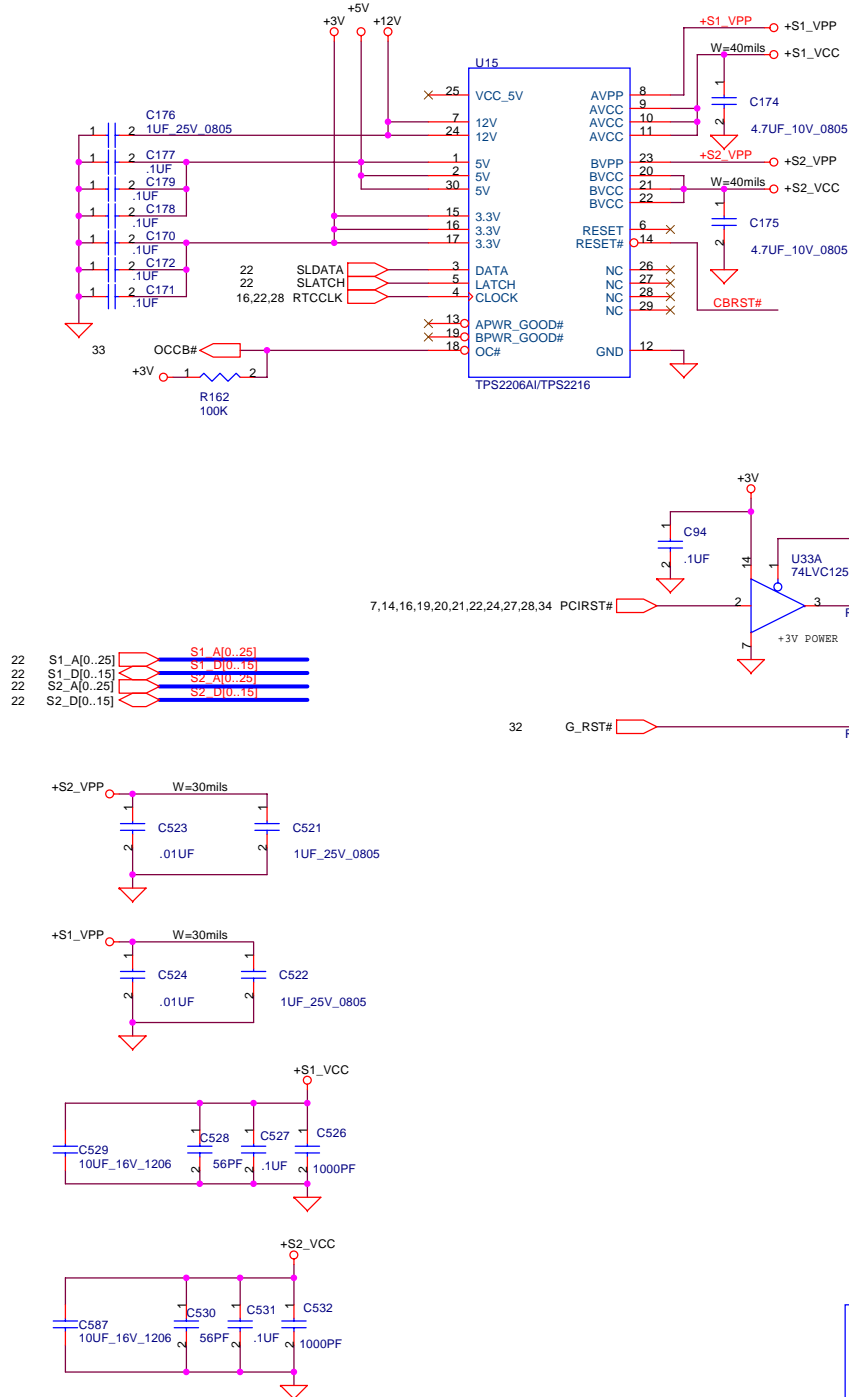
S1_A[0..25] S1_A[0..25] 23
S1_D[0..15] S1_D[0..15] 23

S2_A[0..25] S2_A[0..25] 23
S2_D[0..15] S2_D[0..15] 23

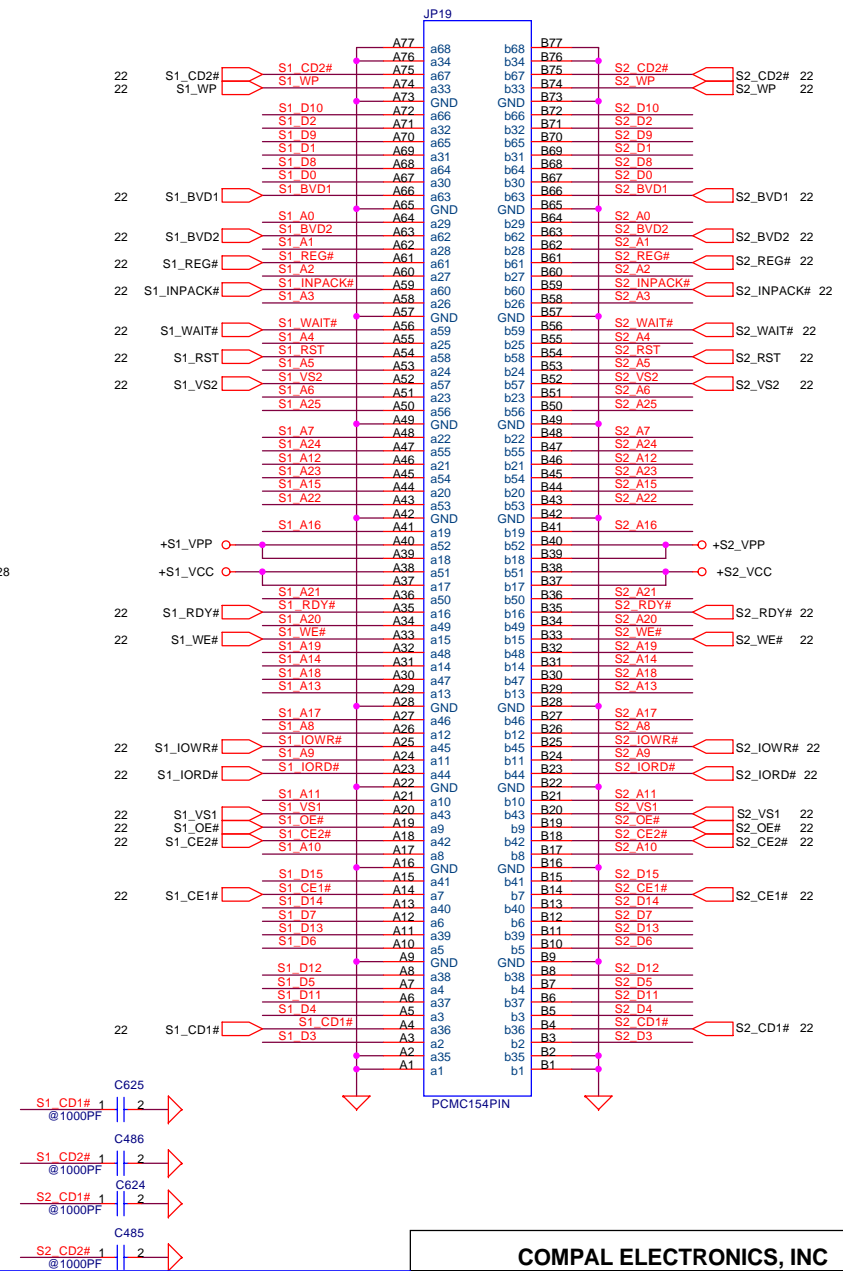
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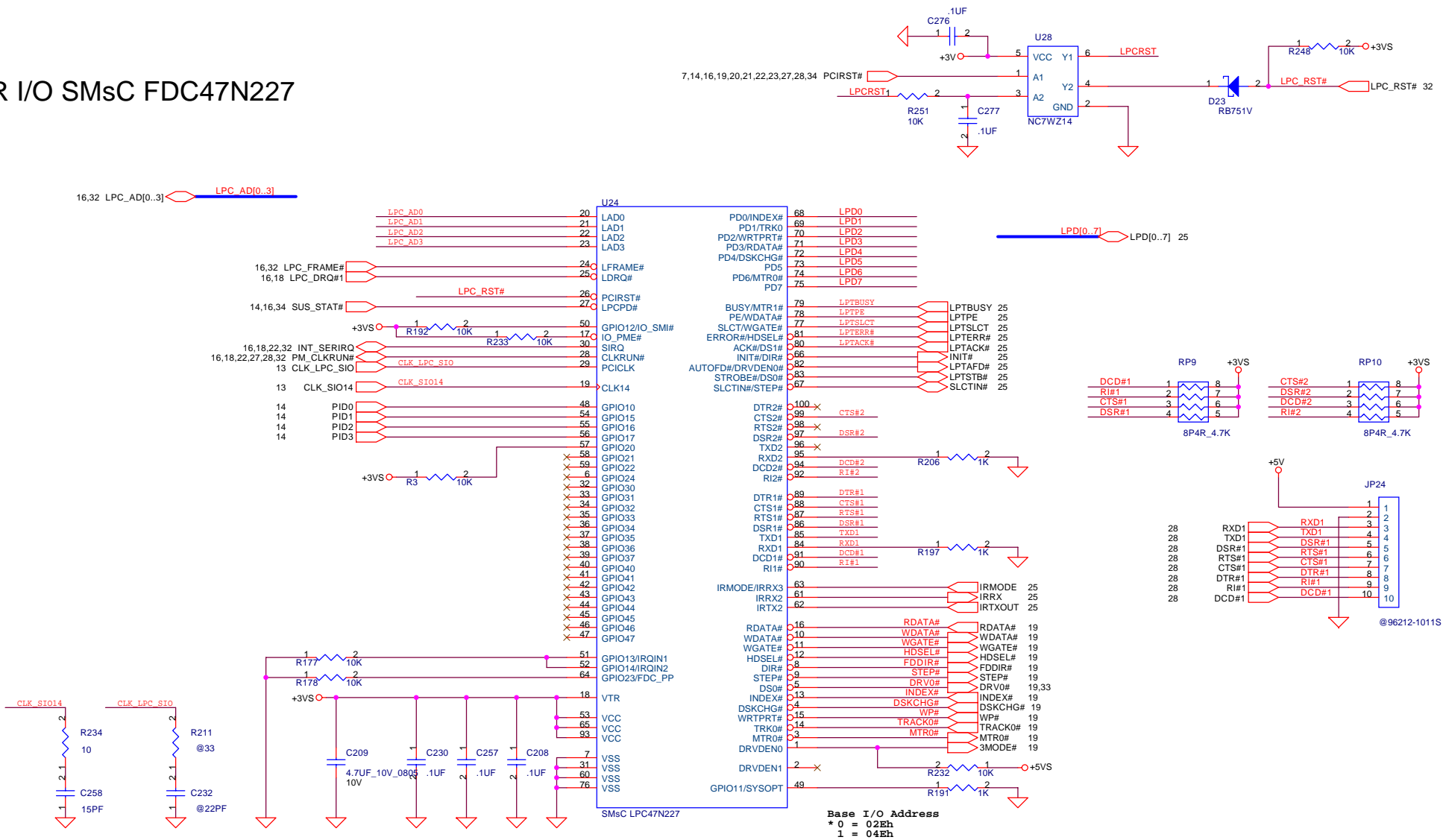
PCMCIA POWER CTRL.



CARDBUS SOCKET



SUPER I/O SMC FDC47N227



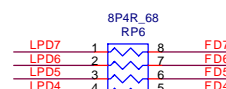
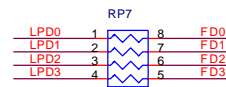
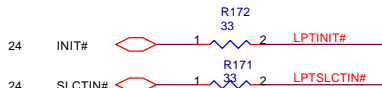
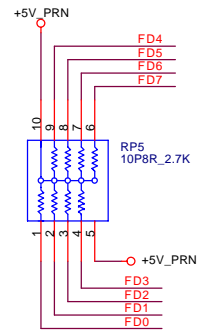
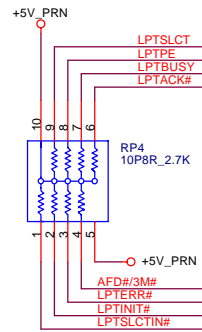
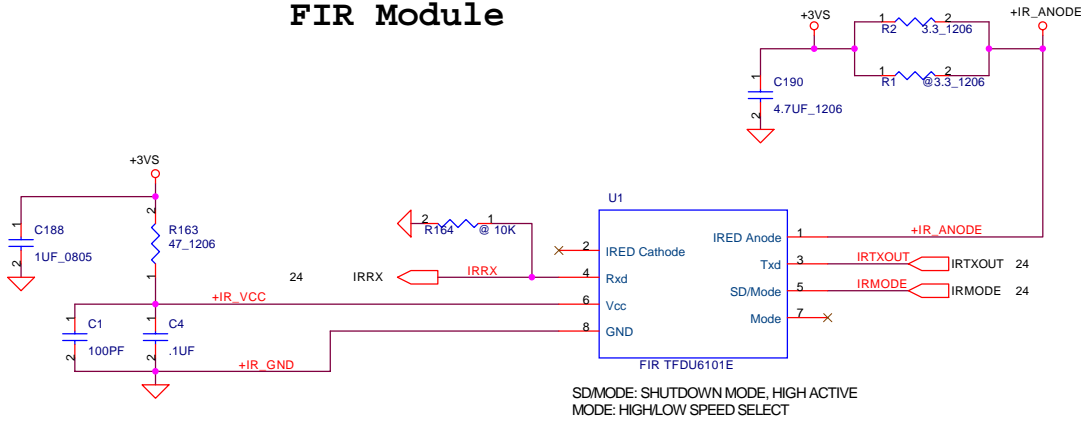
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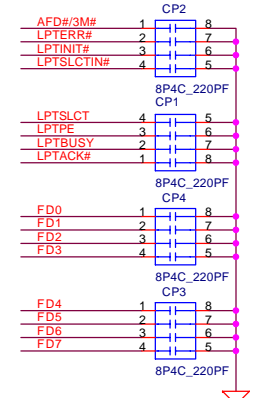
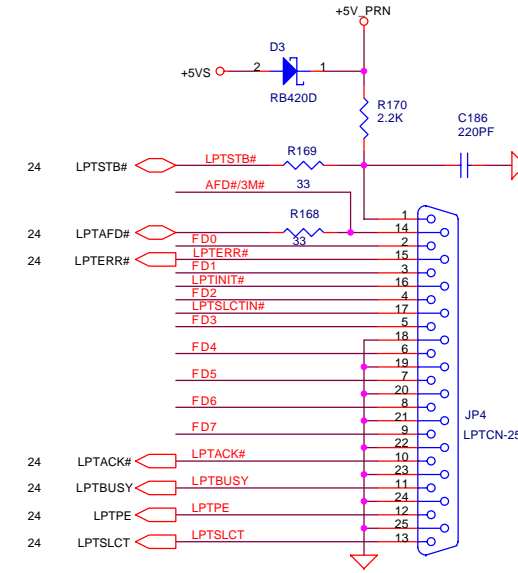
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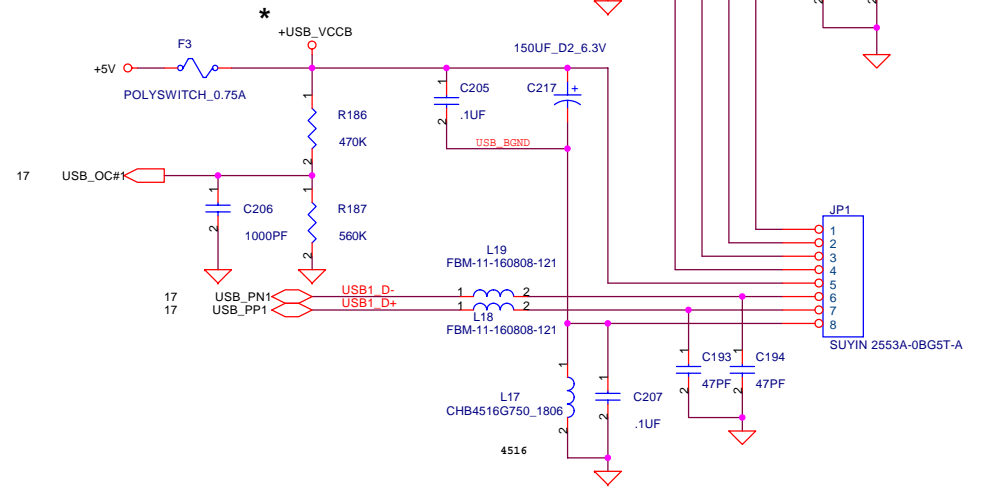
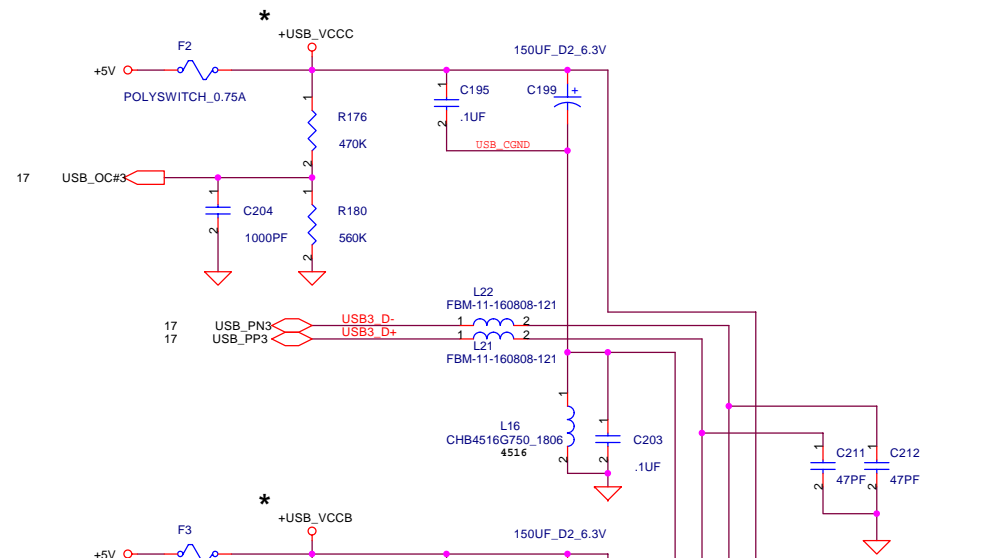
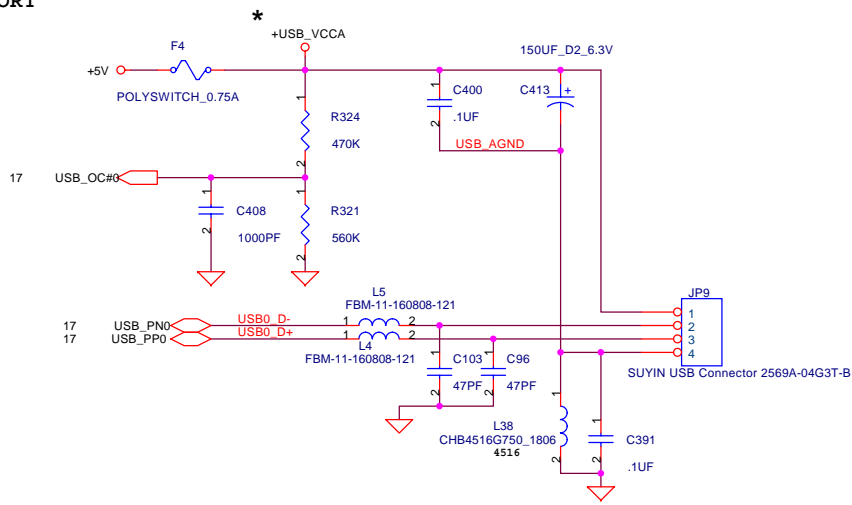
FIR Module



PARALLEL PORT



USB PORT

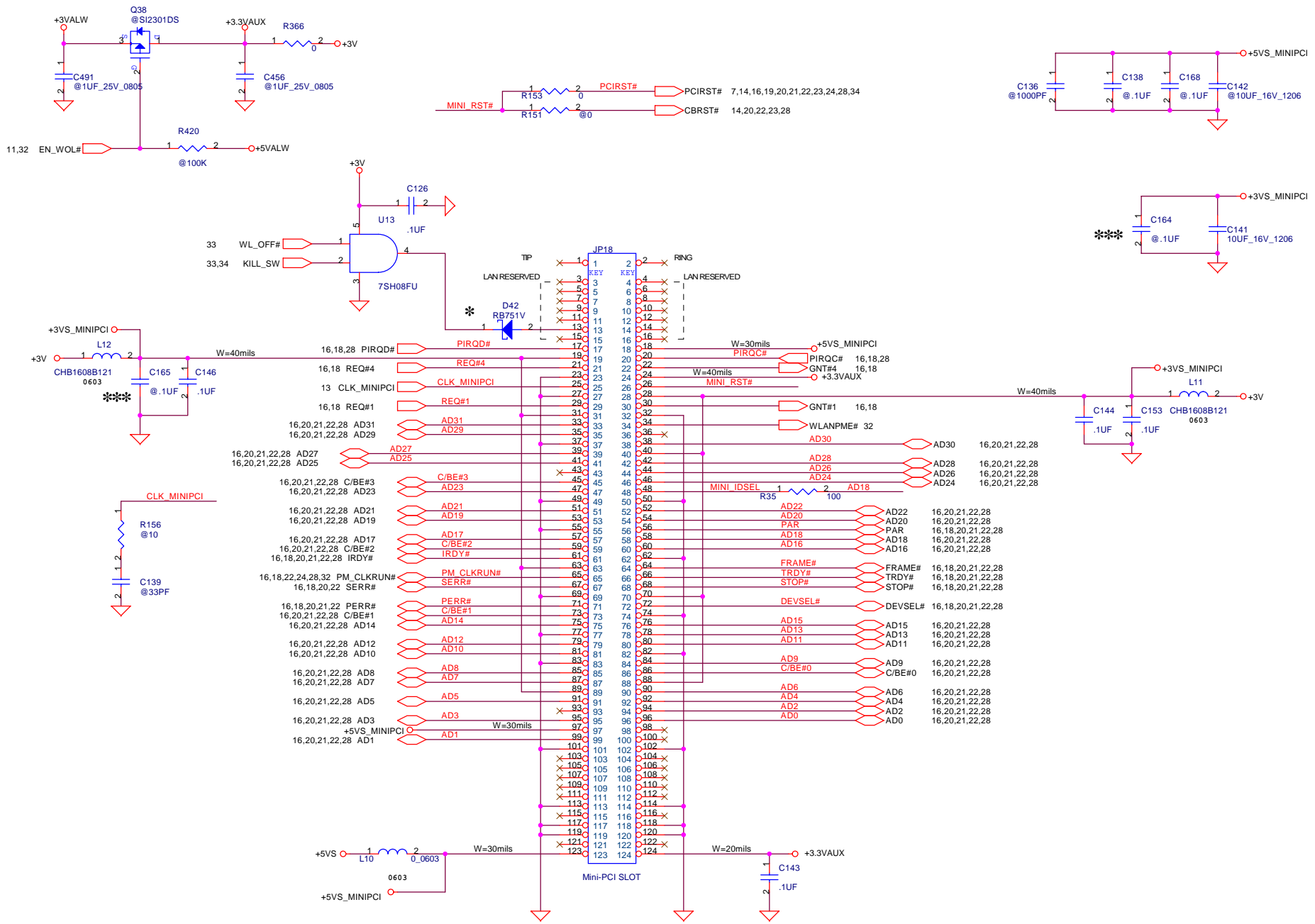


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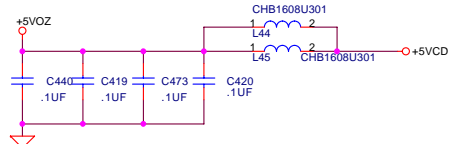
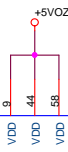
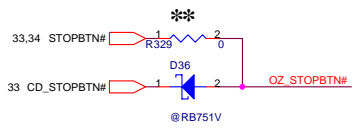
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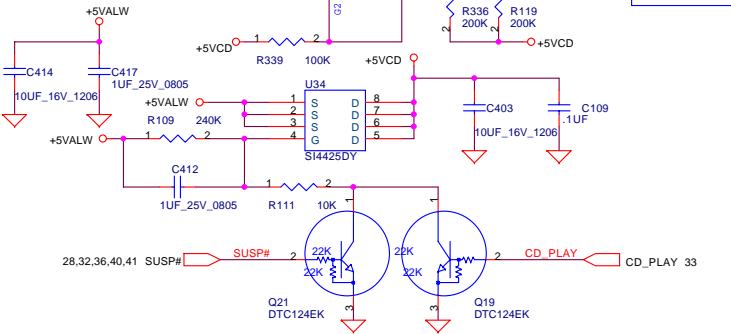
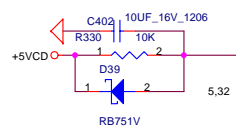
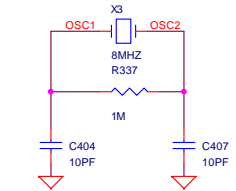
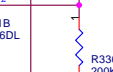
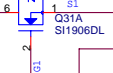
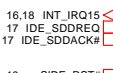
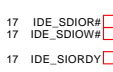
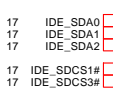
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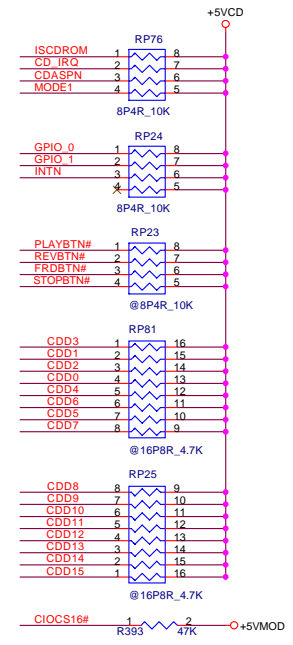
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IDE_SDD0	76	HDD0	CDD0	77	CDD0
IDE_SDD1	78	HDD1	CDD1	79	CDD1
IDE_SDD2	81	HDD2	CDD2	82	CDD2
IDE_SDD3	83	HDD3	CDD3	84	CDD3
IDE_SDD4	86	HDD4	CDD4	87	CDD4
IDE_SDD5	90	HDD5	CDD5	91	CDD5
IDE_SDD6	95	HDD6	CDD6	96	CDD6
IDE_SDD7	97	HDD7	CDD7	98	CDD7
IDE_SDD8	2	HDD8	CDD8	1	CDD8
IDE_SDD9	4	HDD9	CDD9	3	CDD9
IDE_SDD10	4	HDD9	CDD9	7	CDD10
IDE_SDD11	11	HDD10	CDD10	10	CDD11
IDE_SDD12	15	HDD12	CDD12	14	CDD12
IDE_SDD13	18	HDD13	CDD13	17	CDD13
IDE_SDD14	20	HDD14	CDD14	19	CDD14
IDE_SDD15	22	HDD15	CDD15	21	CDD15

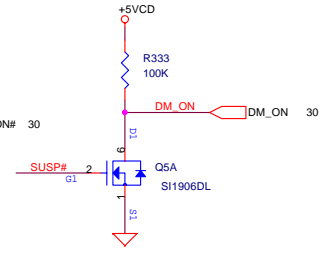
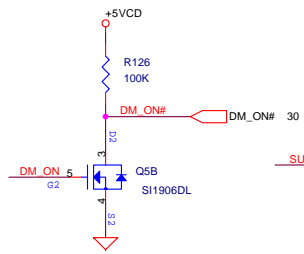


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CDA0	69	CD_SBA0	19	CD_SBA0	19
CDA1	71	CD_SBA1	19	CD_SBA1	19
CDA2	67	CD_SBA2	19	CD_SBA2	19
CCS0	64	CD_SCS1#	19	CD_SCS1#	19
CCS1	62	CD_SCS3#	19	CD_SCS3#	19
CDIOR#	100	CD_SIOR#	19	CD_SIOR#	19
CDIOW#	5	CD_SIOW#	19	CD_SIOW#	19
CIOCS16#	73	CD_SIOW#	19	CD_SIOW#	19
CIORDY	94	CD_SIOR#	19	CD_SIOR#	19
CHINTRQ	75	CD_IRO	19	CD_IRO	19
CDMARG	13	CD_DREQ	19	CD_DREQ	19
CHDMACK#	89	CD_DACK#	19	CD_DACK#	19
CRESET#	23	CD_RSTDRV#	19	CD_RSTDRV#	19
CDASPN	60	CD_RSTDRV#	19	CD_RSTDRV#	19
SSYNC	47				
SBIT_CLK	52				
SDATA_OUT	54				
SDATA_IN	49				
SACRSTN	45				
PWR_CTL	51				
ISCDROM	80				
GPIO1[VOL_UP	39				
GPIO0[VOL_DN	40				
MODE0	56				
MODE1	57				
PAVMODE	38				
CSN	41				
INCIN	42				
UDN	43				



Select OZ165 / OZ168	
STUFF	CHIP
R399, R249	OZ165
R400	OZ168

Select SM BUS ADDRESS	
STUFF	SMBus ID
R331	B4h
R332	34h



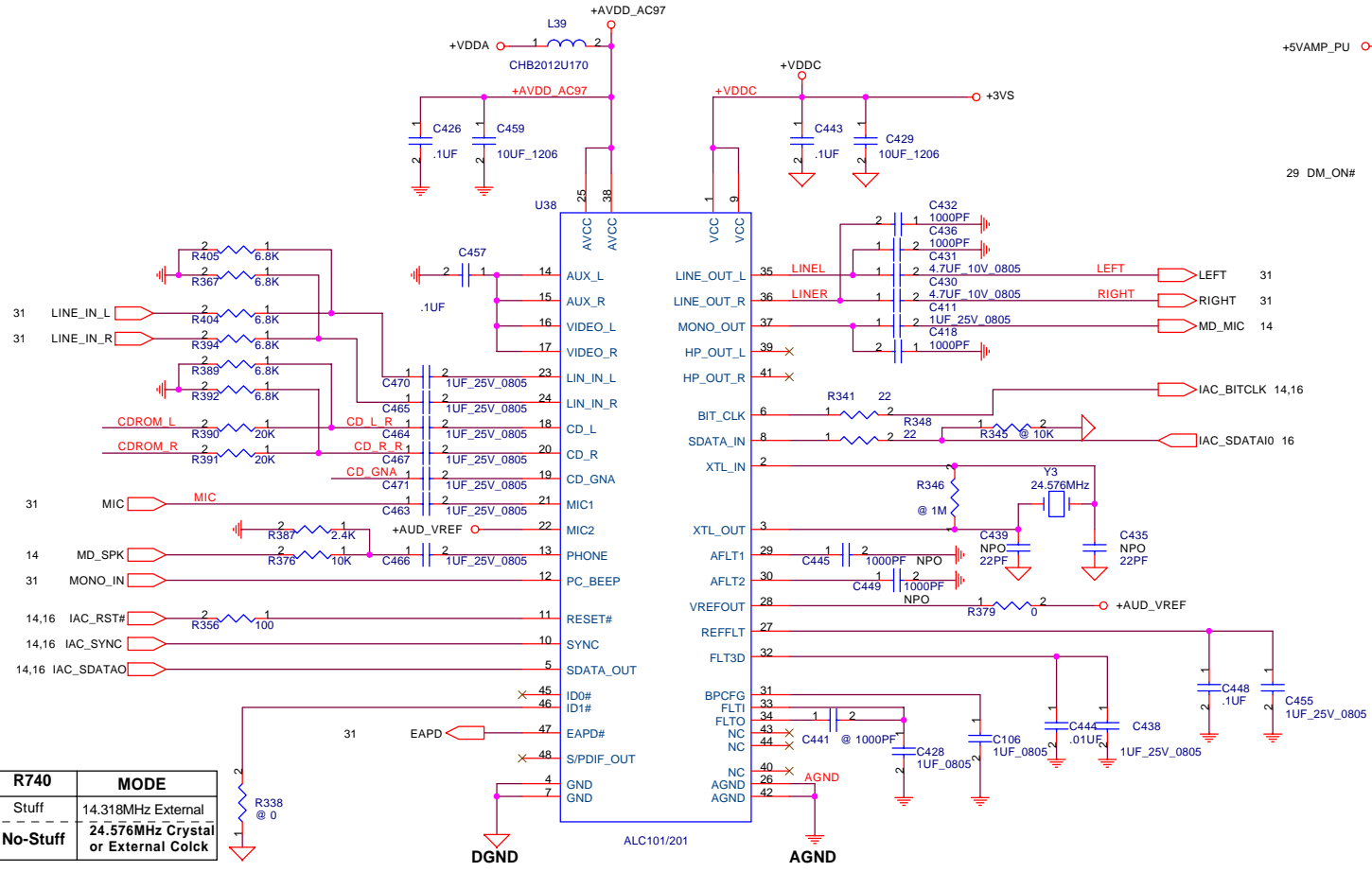
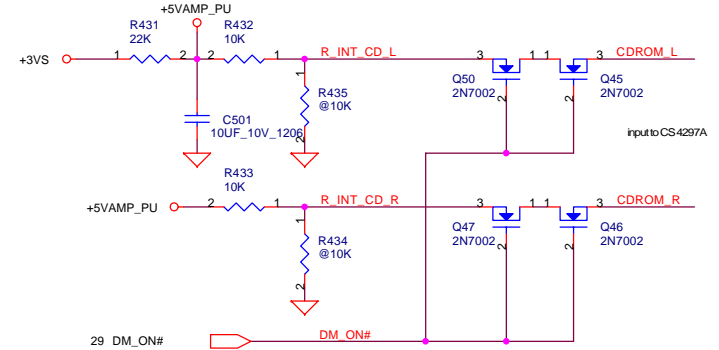
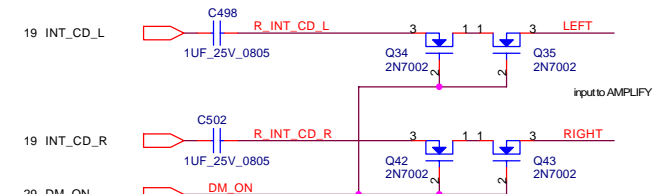
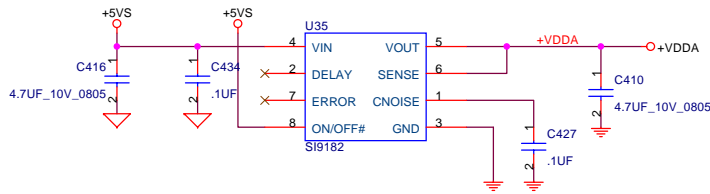
COMPAL ELECTRONICS, INC

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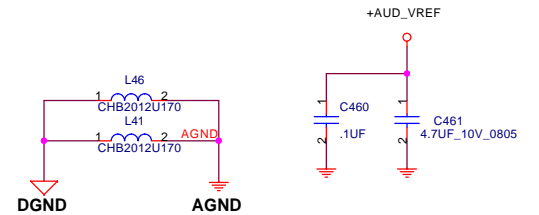
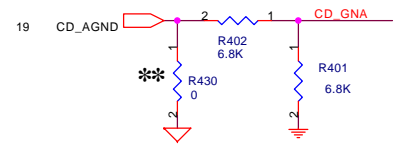
Date: 星期四, 三月 18, 2004 Sheet 29 of 83

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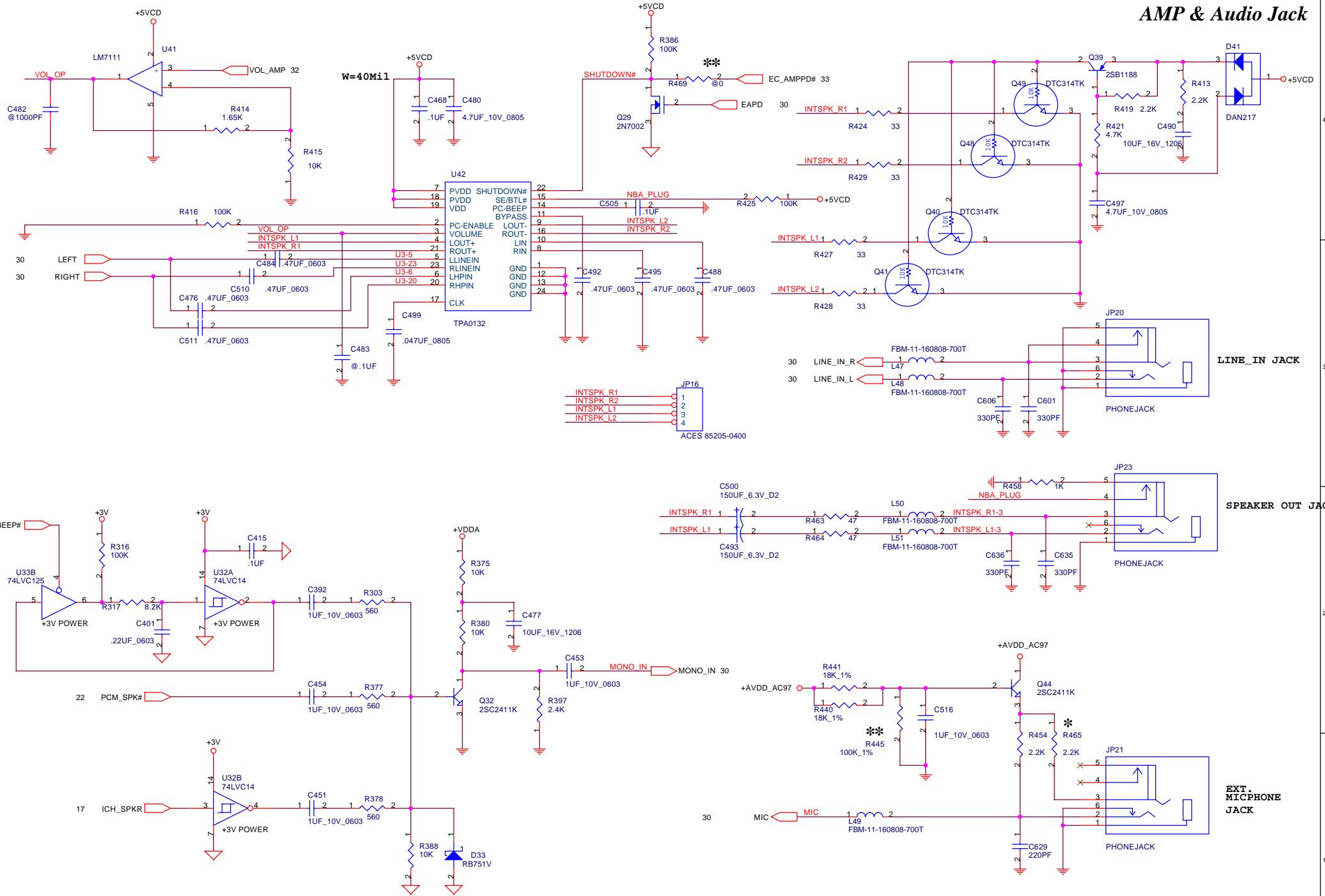
R740	MODE
Stuff	14.318MHz External
No-Stuff	24.576MHz Crystal or External Colck



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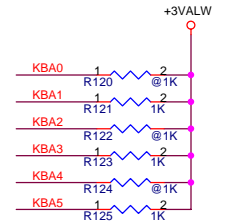
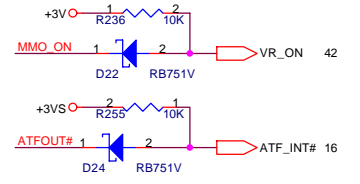
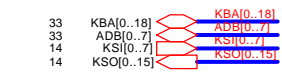
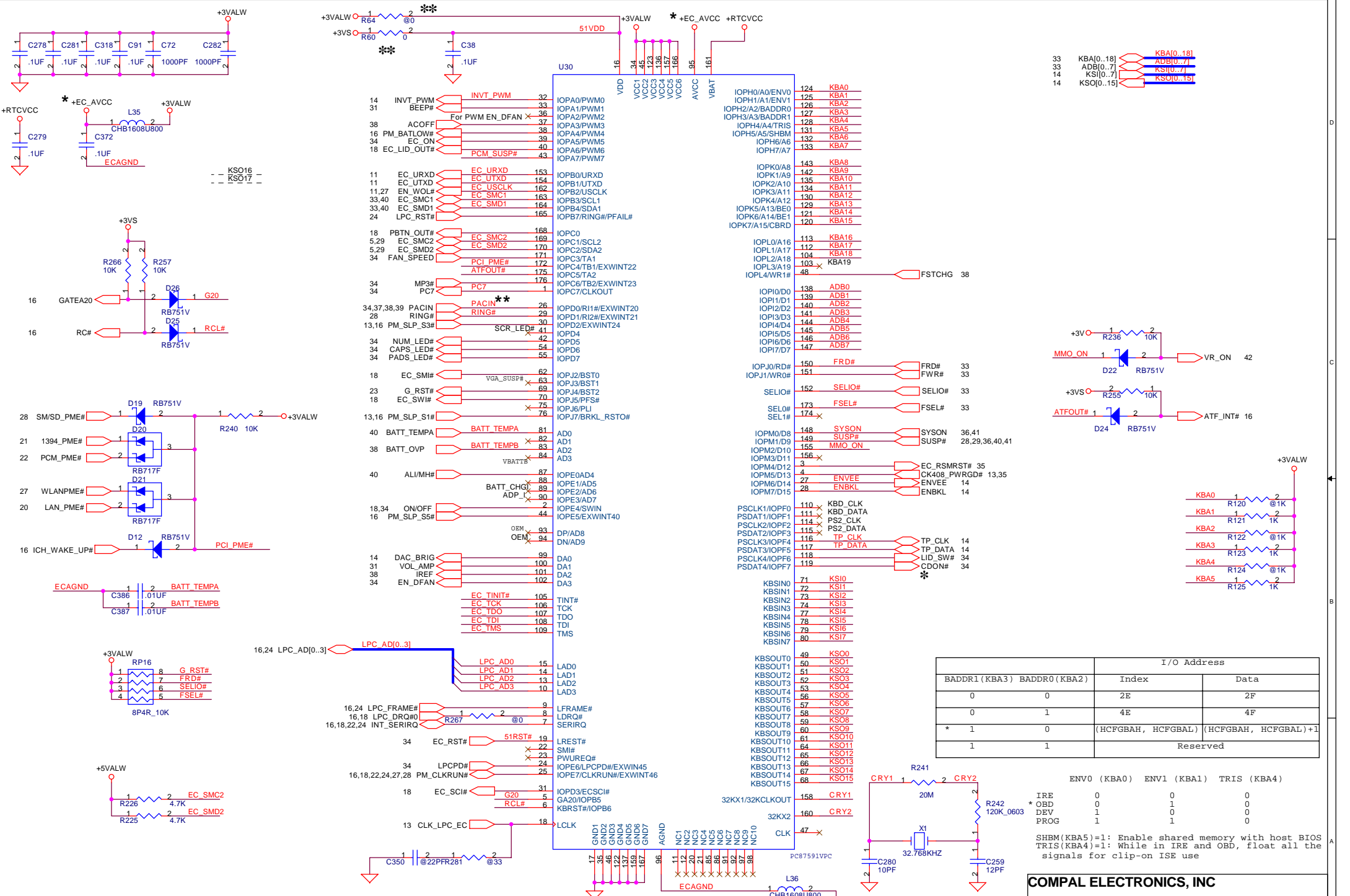
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Compal Electronics, Inc.			
SCHEMATIC, M/BLA-1331			
Size	Document Number	Rev	
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Date:	星期四, 三月 18, 2004	Sheet	30 of 83

AMP & Audio Jack



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SCHEMATIC, M/BLA-1331		
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I/O Address			
BADDR1 (KBA3)	BADDR0 (KBA2)	Index	Data
0	0	2E	2F
0	1	4E	4F
* 1	0	(HCFGBAH, HCFGBAL)	(HCFGBAH, HCFGBAL)+1
1	1		Reserved

	ENVO (KBA0)	ENV1 (KBA1)	TRIS (KBA4)
IRE	0	0	0
* OBD	0	1	0
DEV	1	0	0
PROG	1	1	0

SHBM(KBA5)=1: Enable shared memory with host BIOS
TRIS(KBA4)=1: While in IRE and OBD, float all the signals for clip-on ISE use

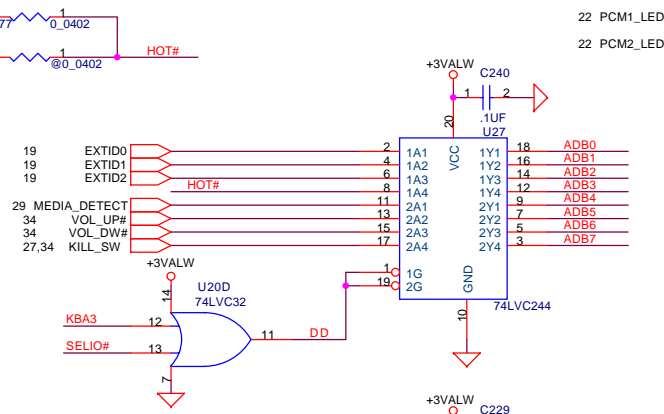
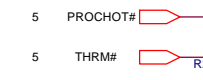
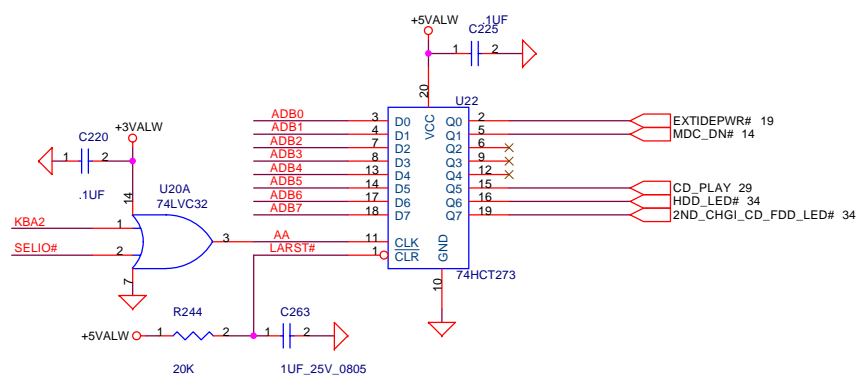
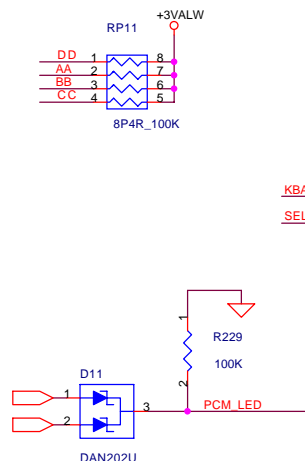
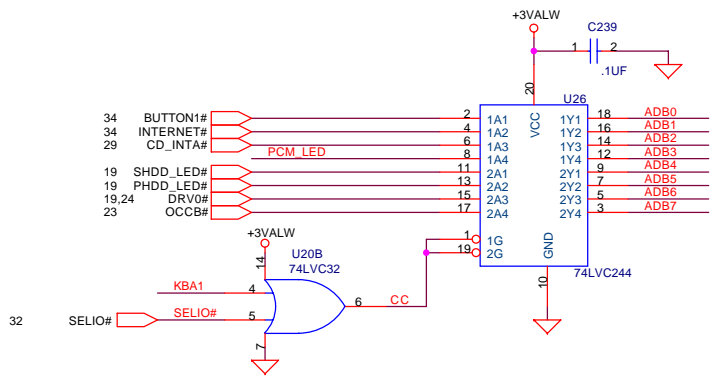
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Size B	Document Number 401207	Rev 2A
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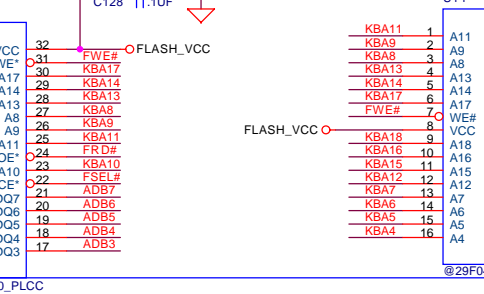
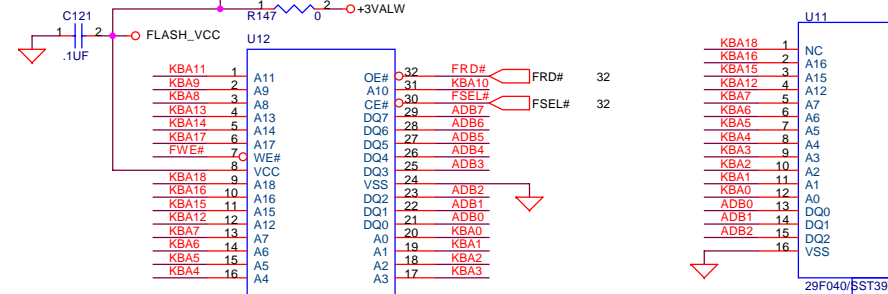
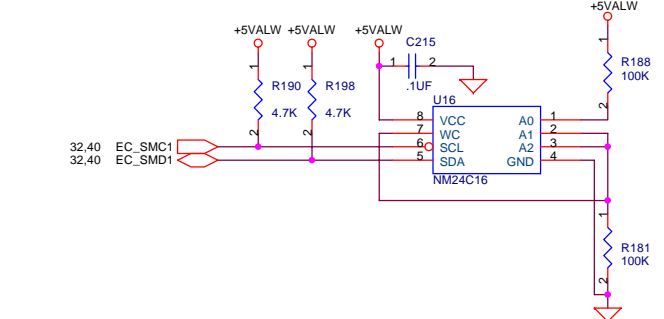
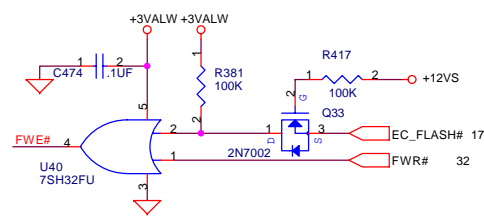
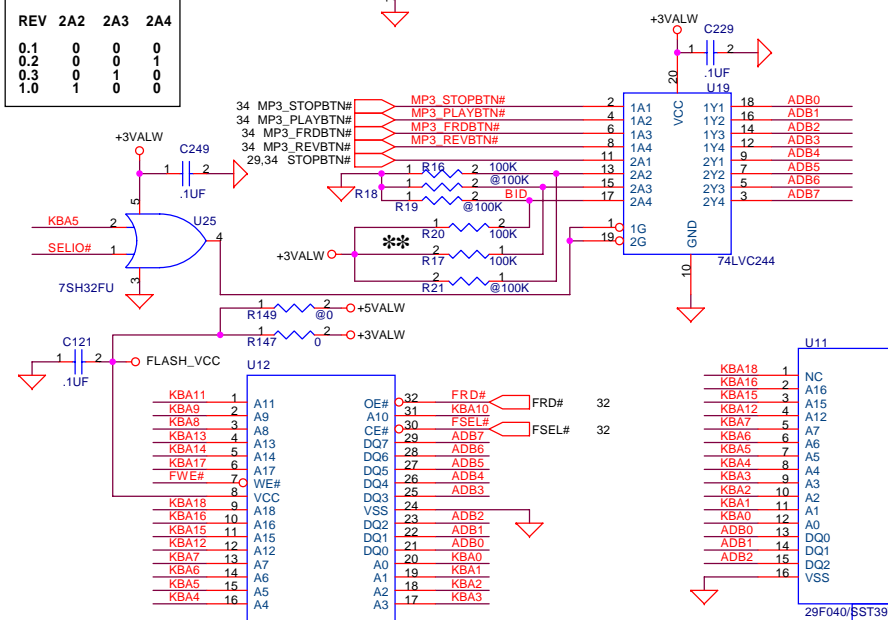
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BOARD ID

REV	2A2	2A3	2A4
0.1	0	0	0
0.2	0	0	1
0.3	0	1	0
1.0	1	0	0

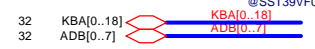


COMPAL ELECTRONICS, INC

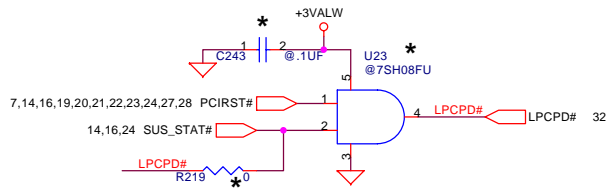
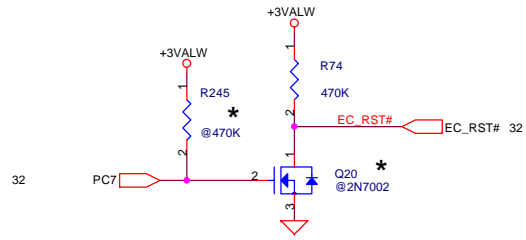
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Size B Document Number: **401207**

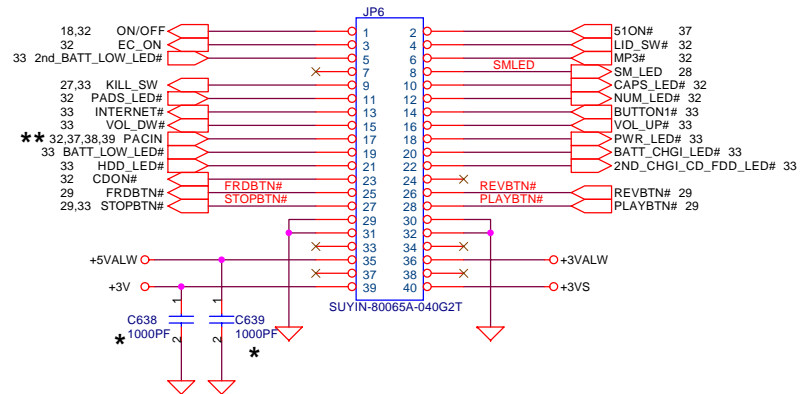
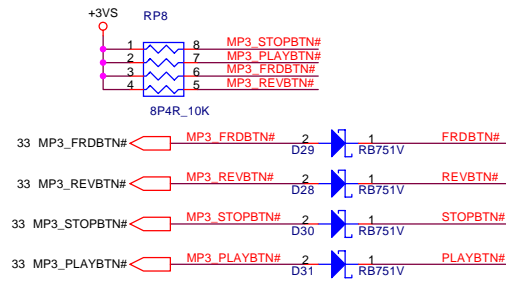
Date: 星期四, 三月 18, 2004 Sheet 33 of 83



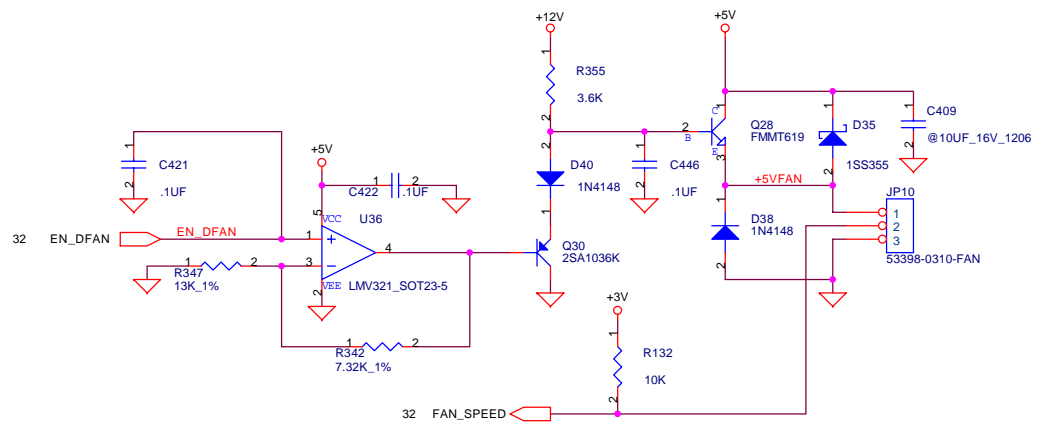
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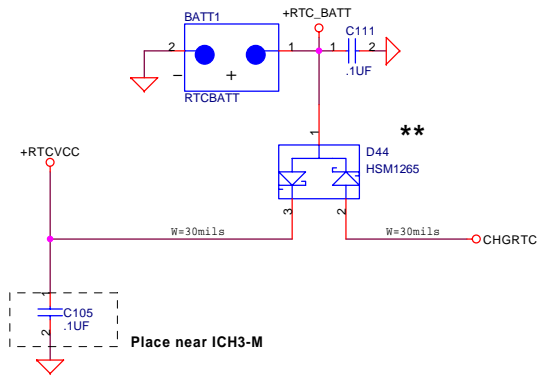
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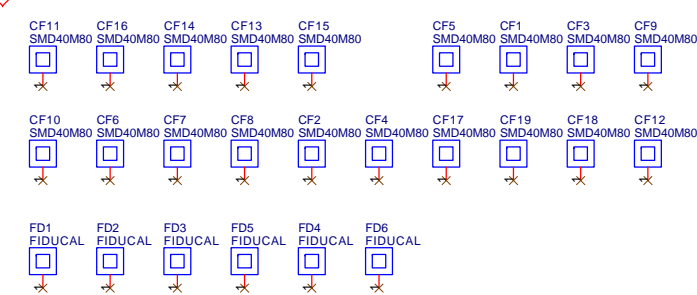
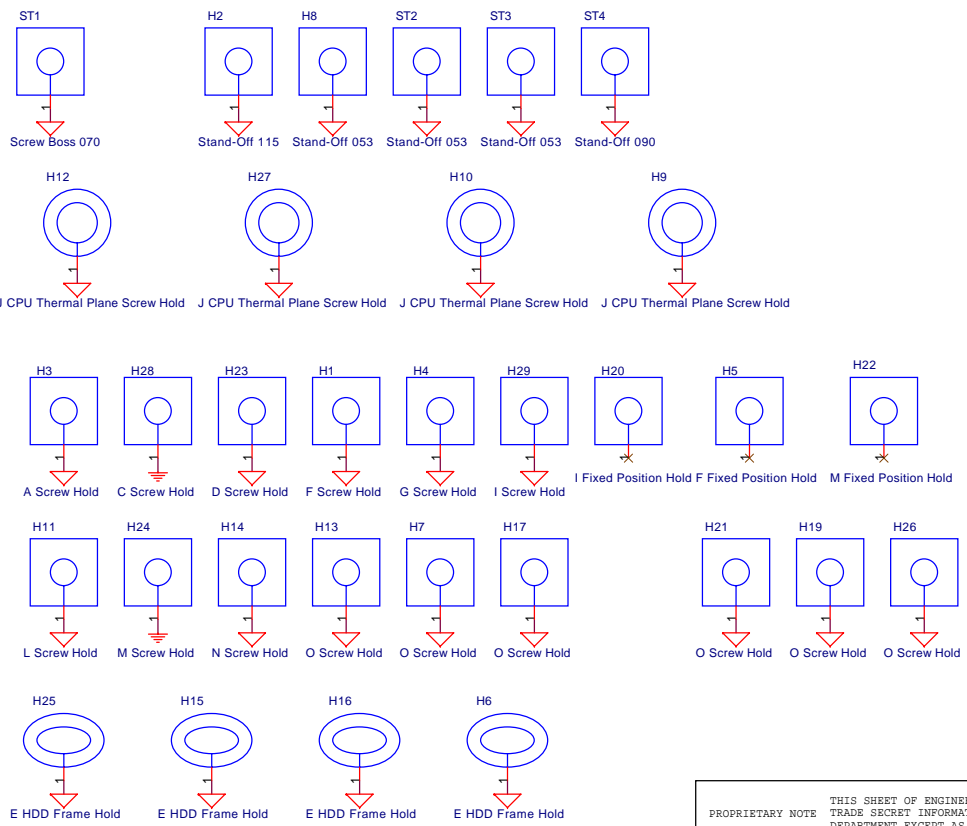
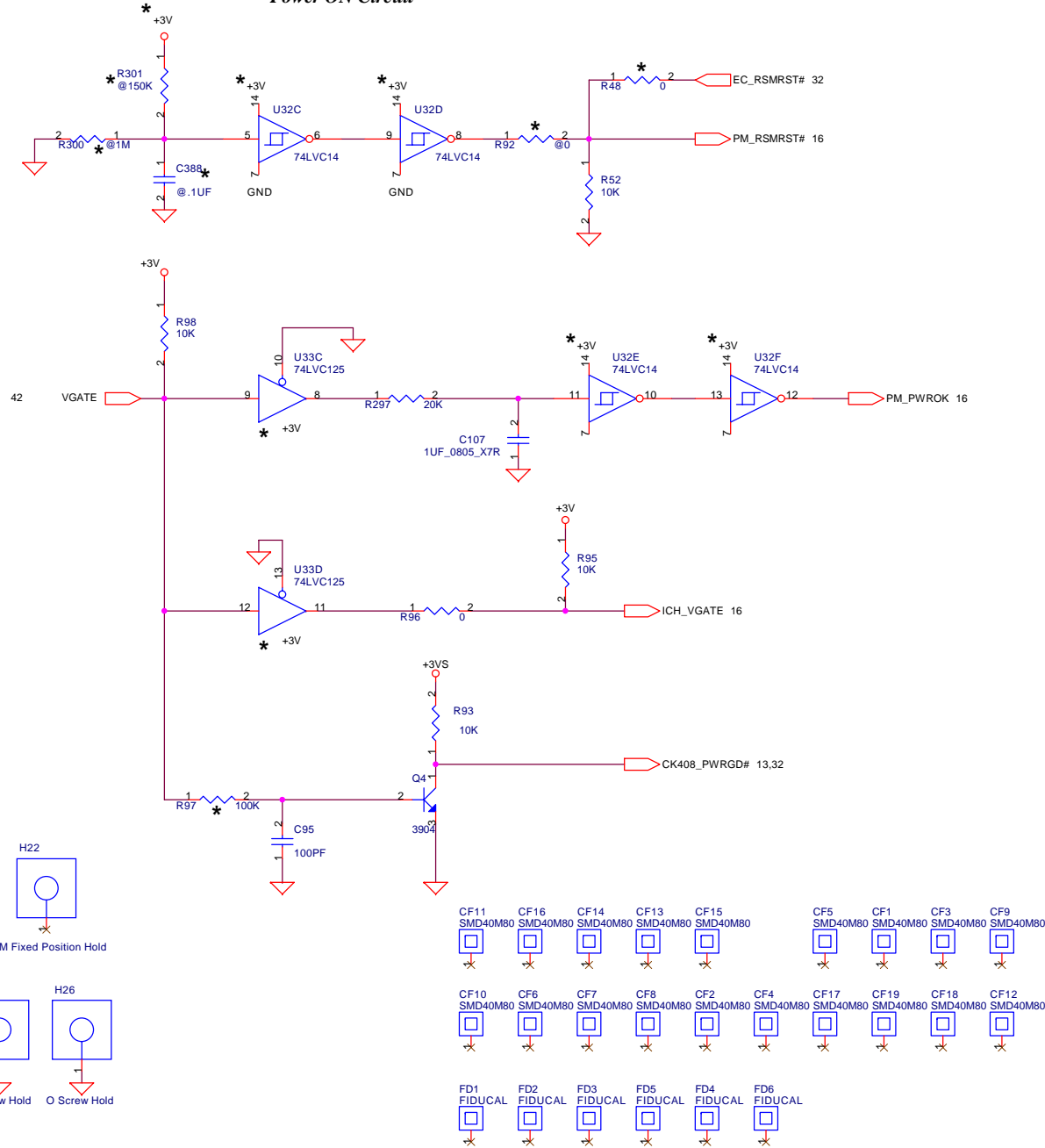
Size B Document Number 401207 Rev 2A

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RTC Batt. Connector



Power ON Circuit



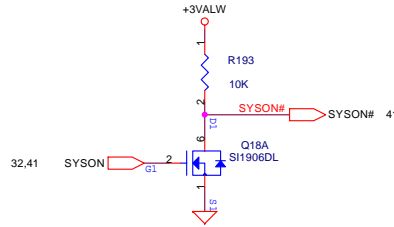
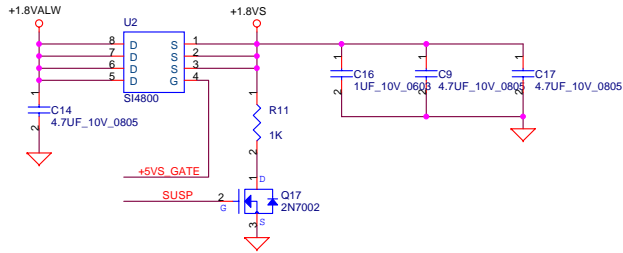
COMPAL ELECTRONICS, INC

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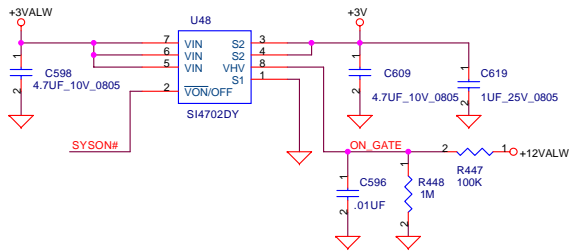
Size	Document Number	Rev
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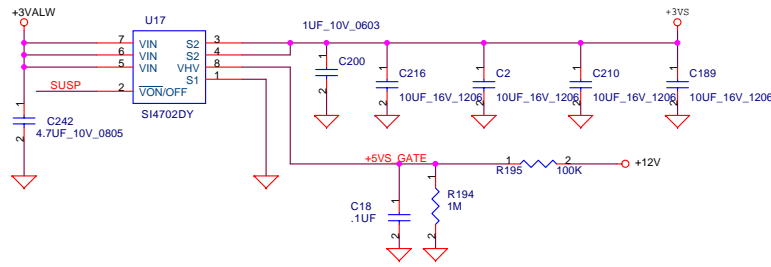
+1.8VALW To +1.8VS Transfer



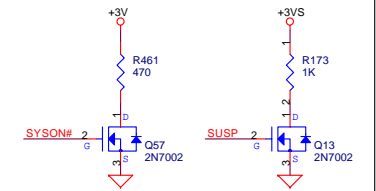
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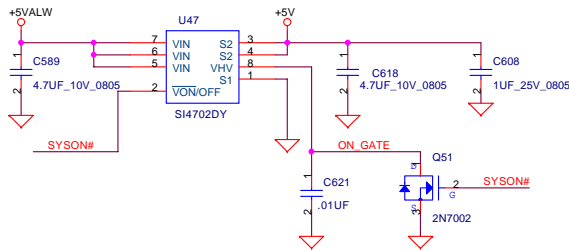
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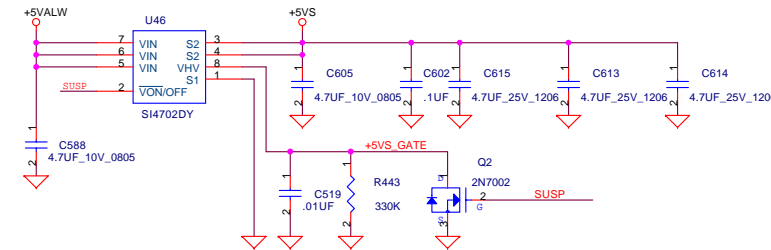
+3V & +3VS Discharge



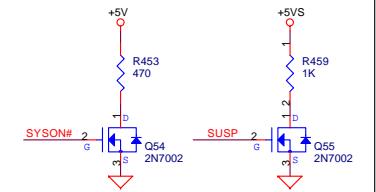
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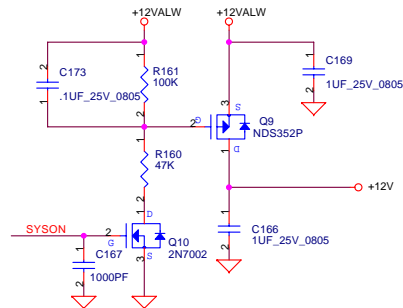
+5VALW To +5VS Transfer



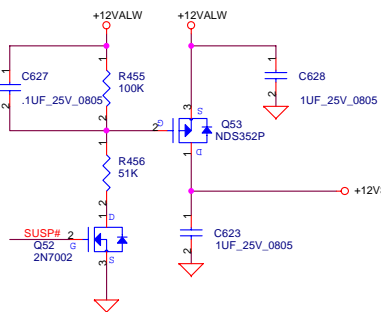
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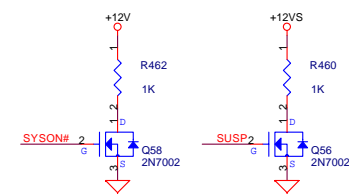
+12VALW To +12V Transfer



+12VALW To +12VS Transfer



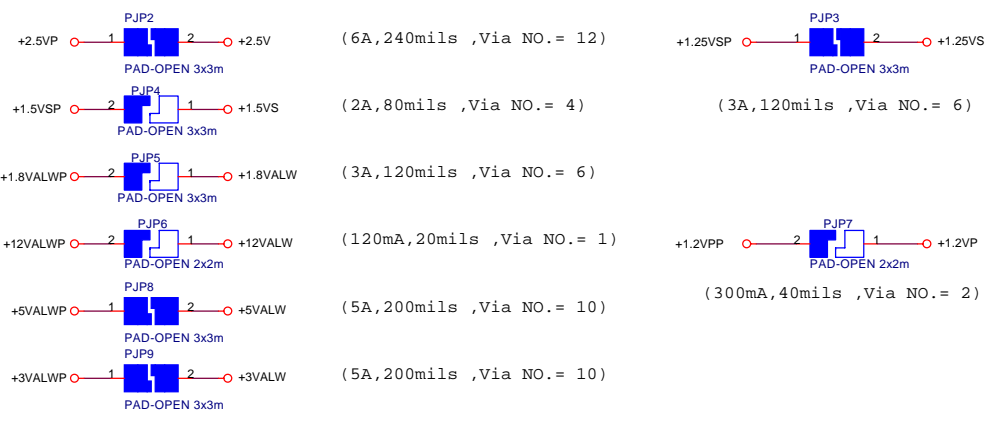
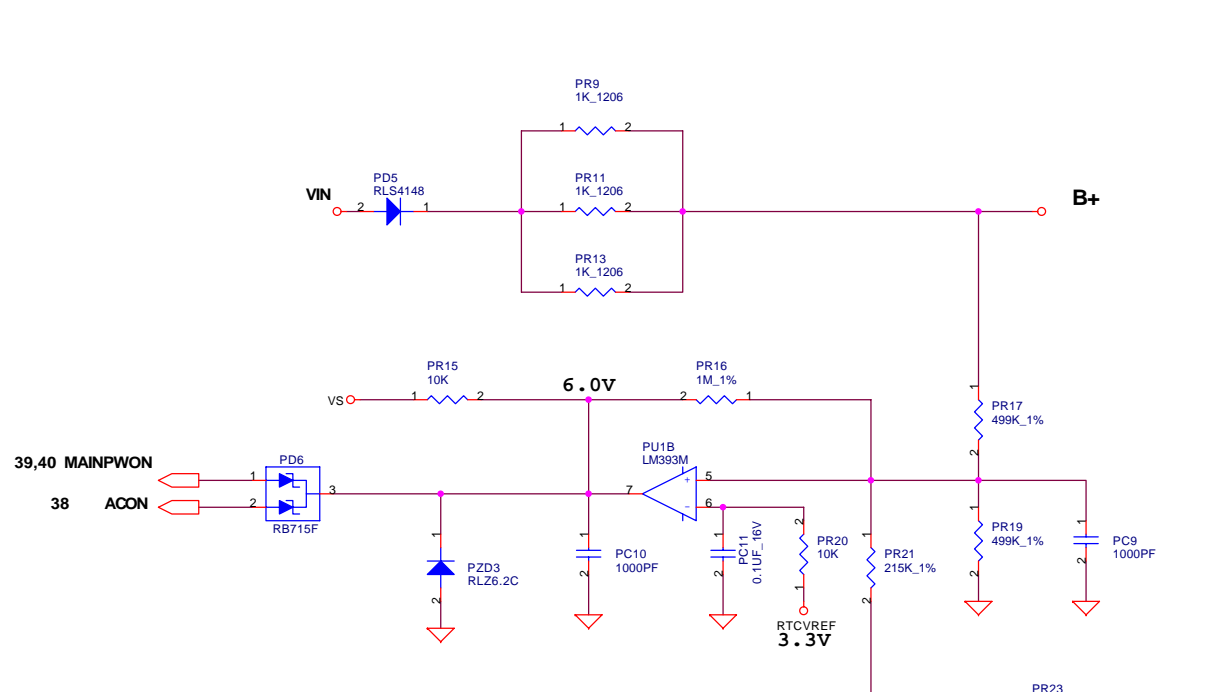
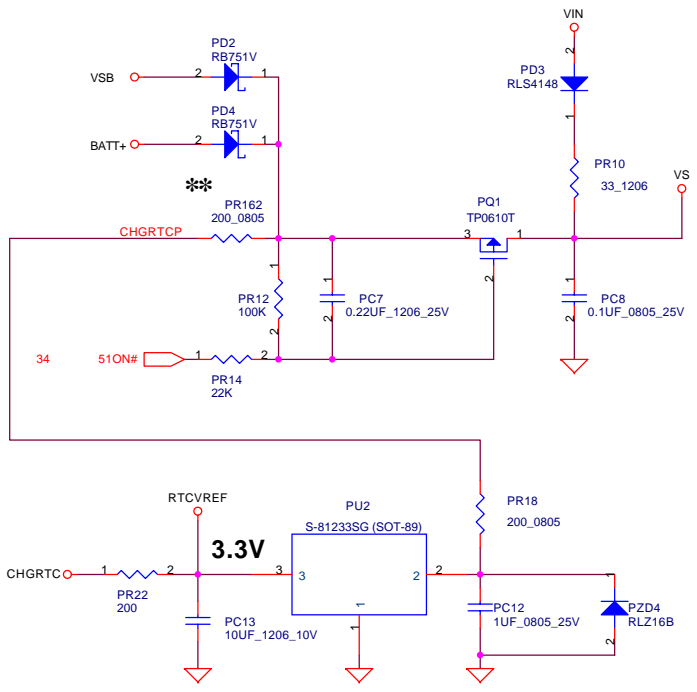
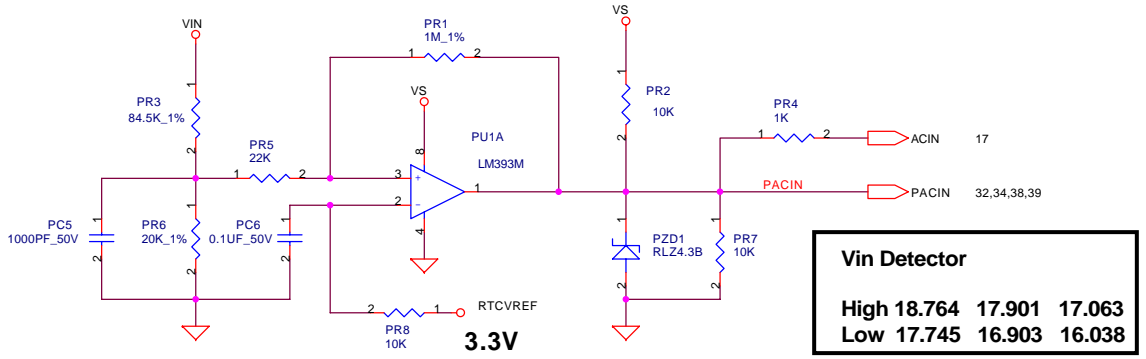
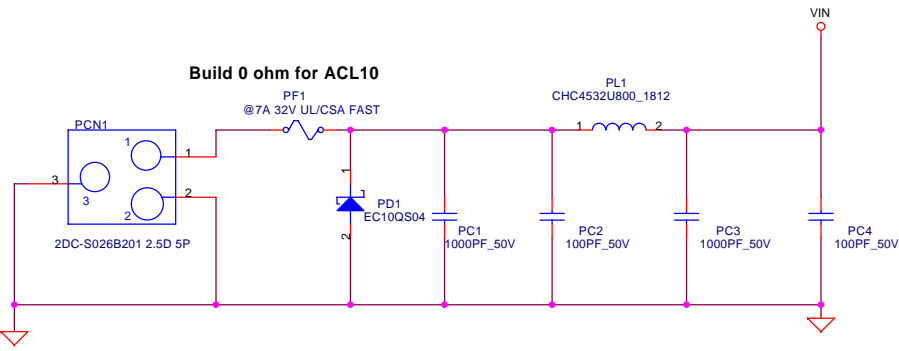
+12V & +12VS Discharge



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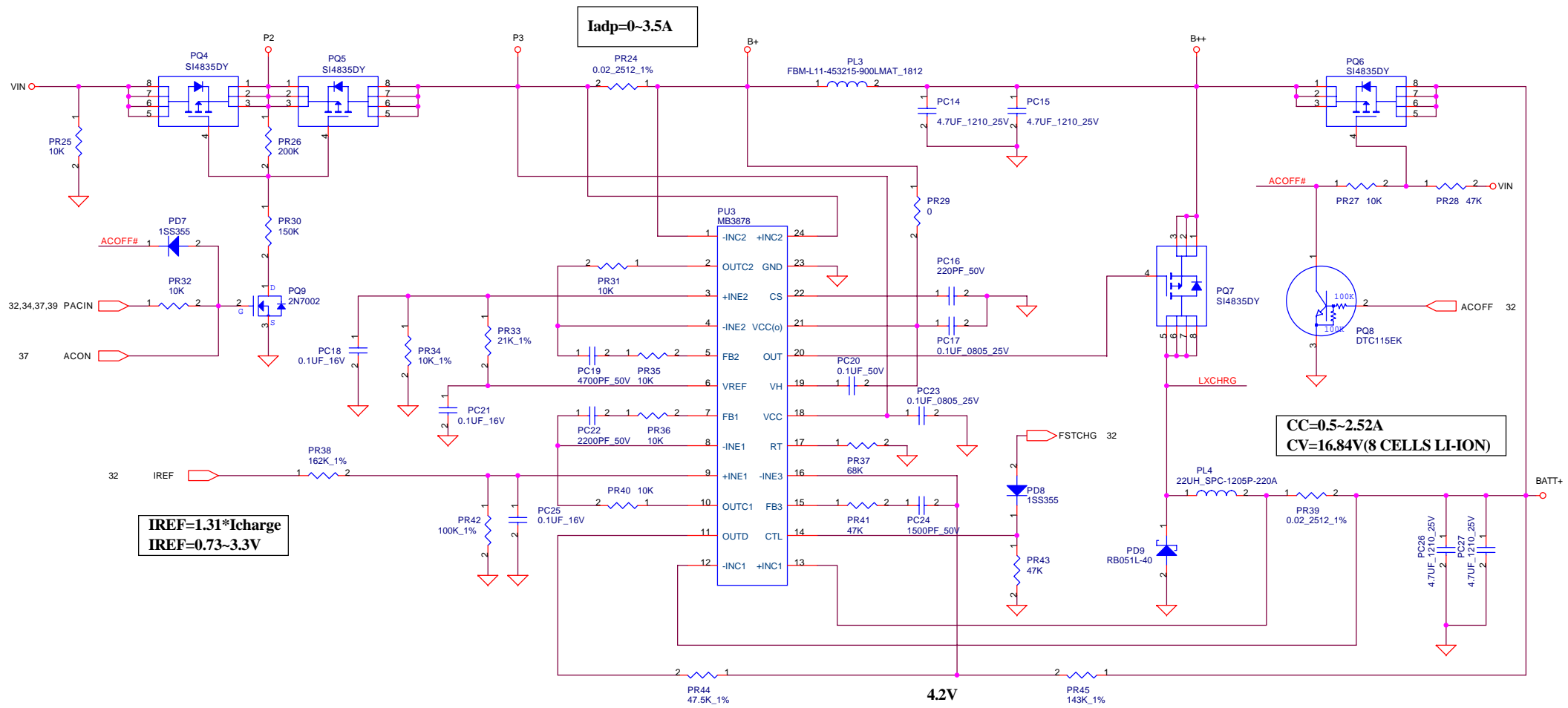
Title		
SCHEMATIC, M/B LA-1331		
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Precharge detector		
	15.34	15.90 16.48
	13.13	13.71 14.20

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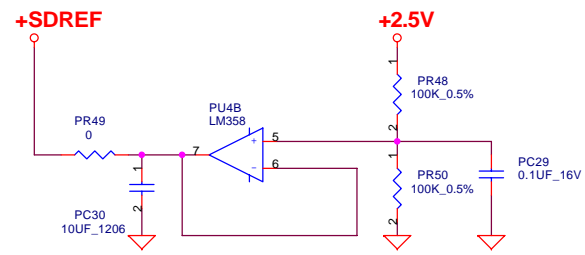
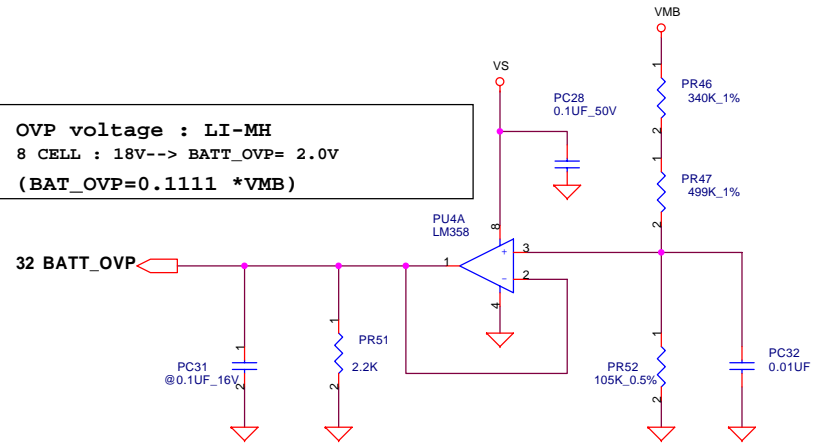


I_{adp}=0~3.5A

CC=0.5~2.52A
CV=16.84V(8 CELLS LI-ION)

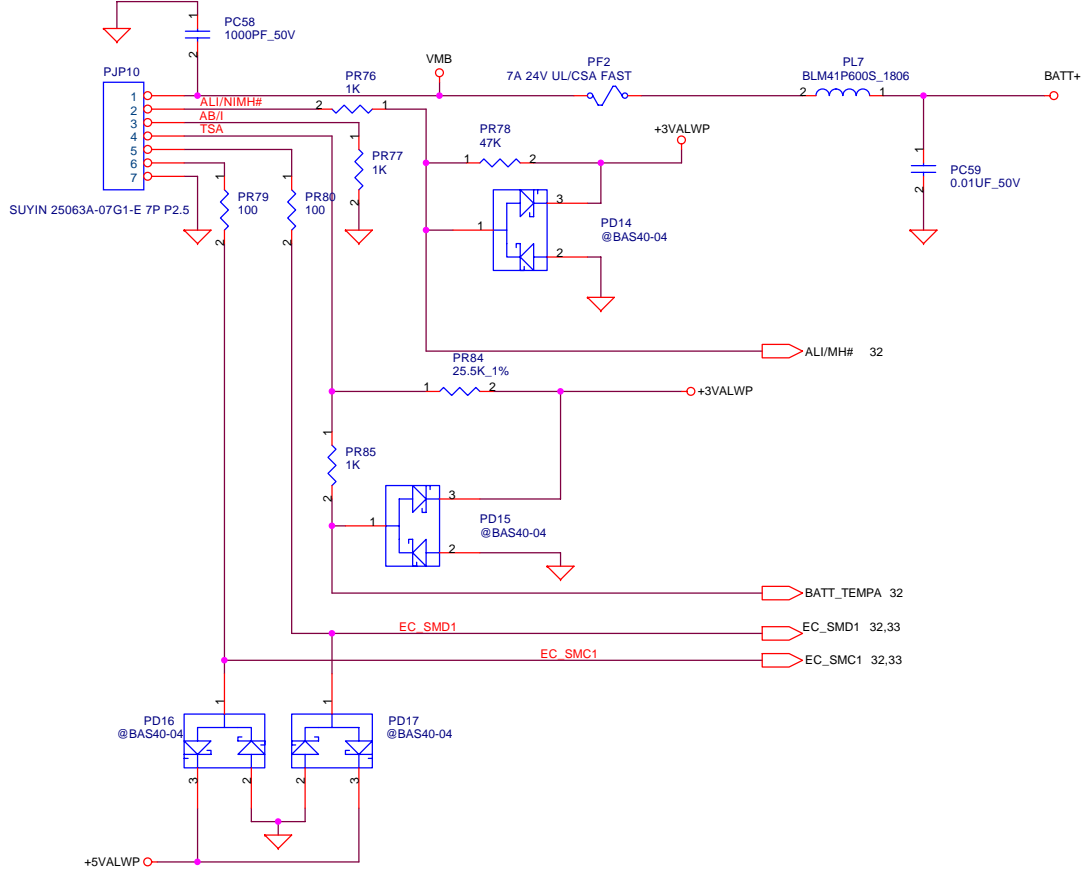
I_{REF}=1.31*I_{charge}
I_{REF}=0.73~3.3V

OVP voltage : LI-MH
8 CELL : 18V--> BATT_OVP= 2.0V
(BAT_OVP=0.1111 *V_{MB})

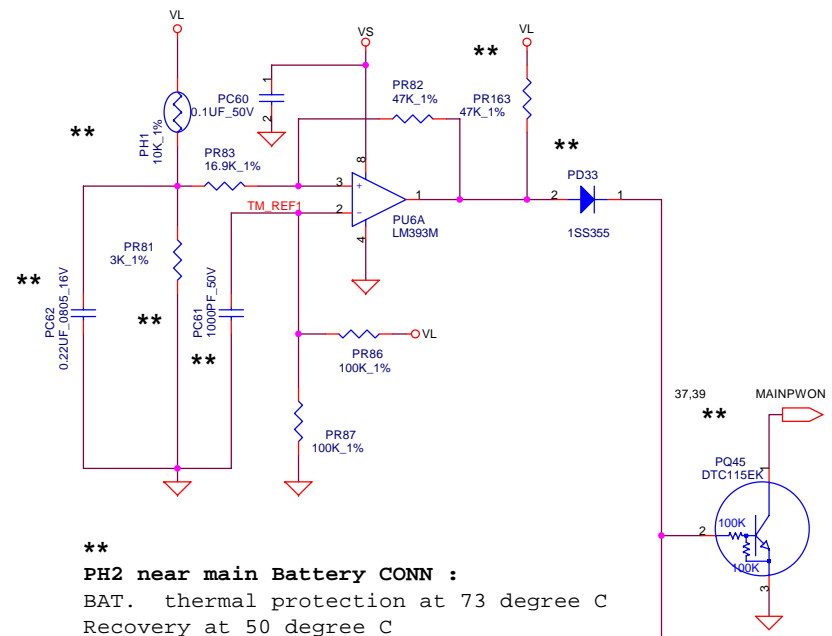


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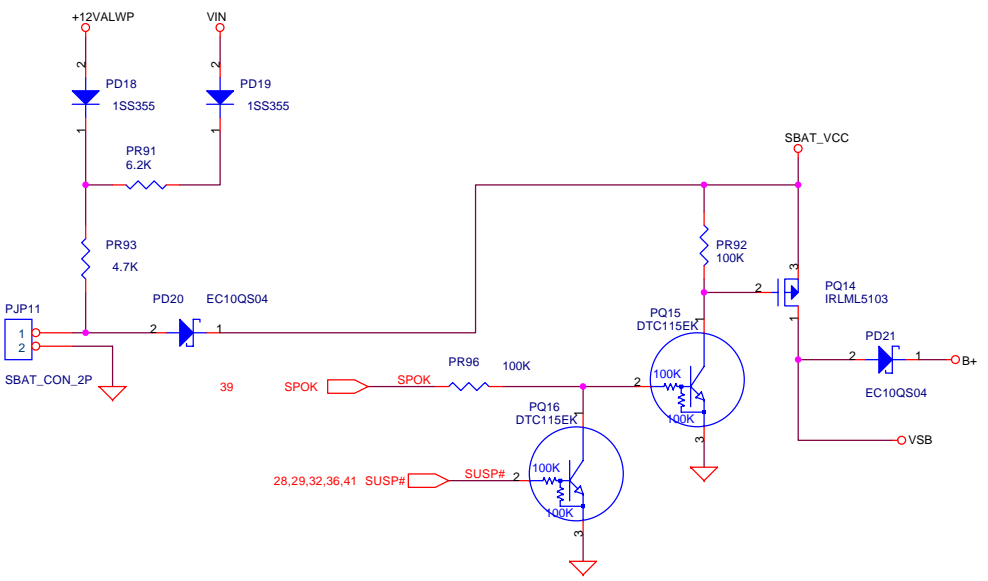
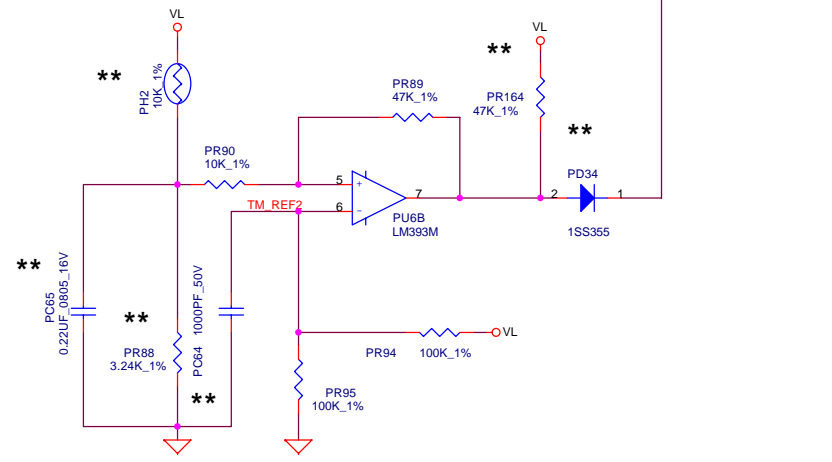
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Title	SCHEMATIC, M/B LA-1331		
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**
PH1 under CPU botten side :
 CPU thermal protection at 87 degree C
 Recovery at 48 degree C

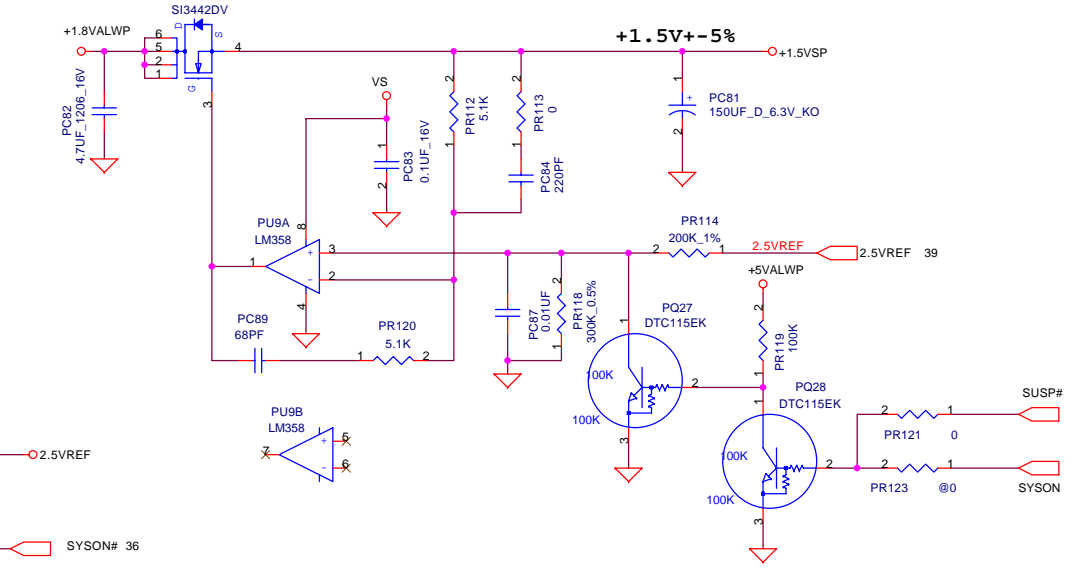
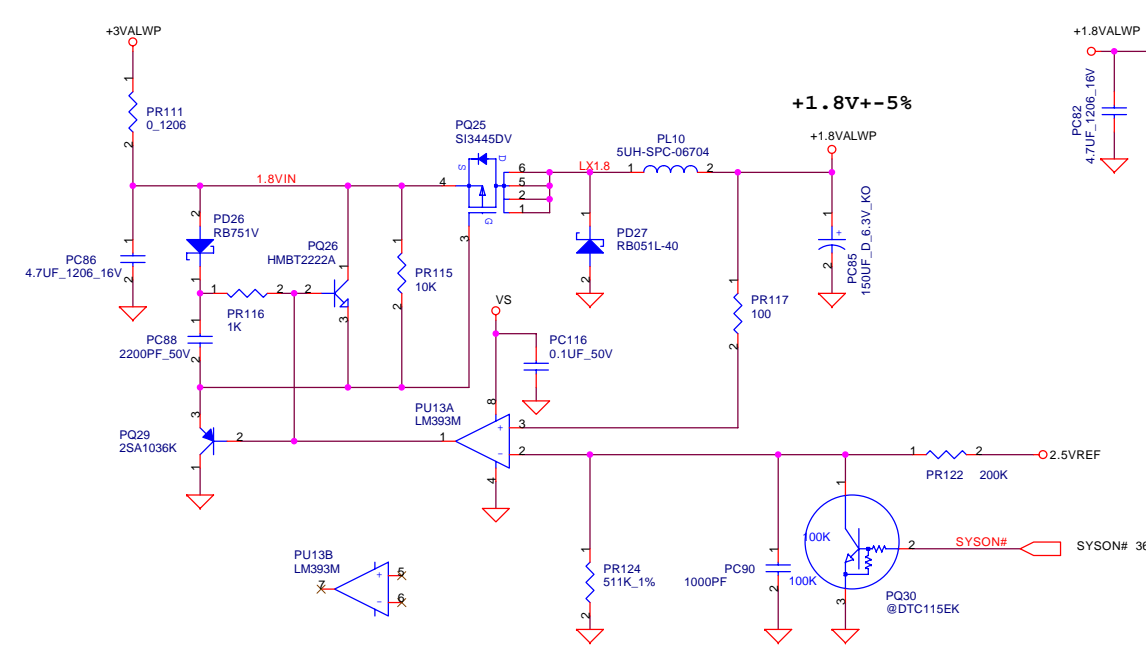
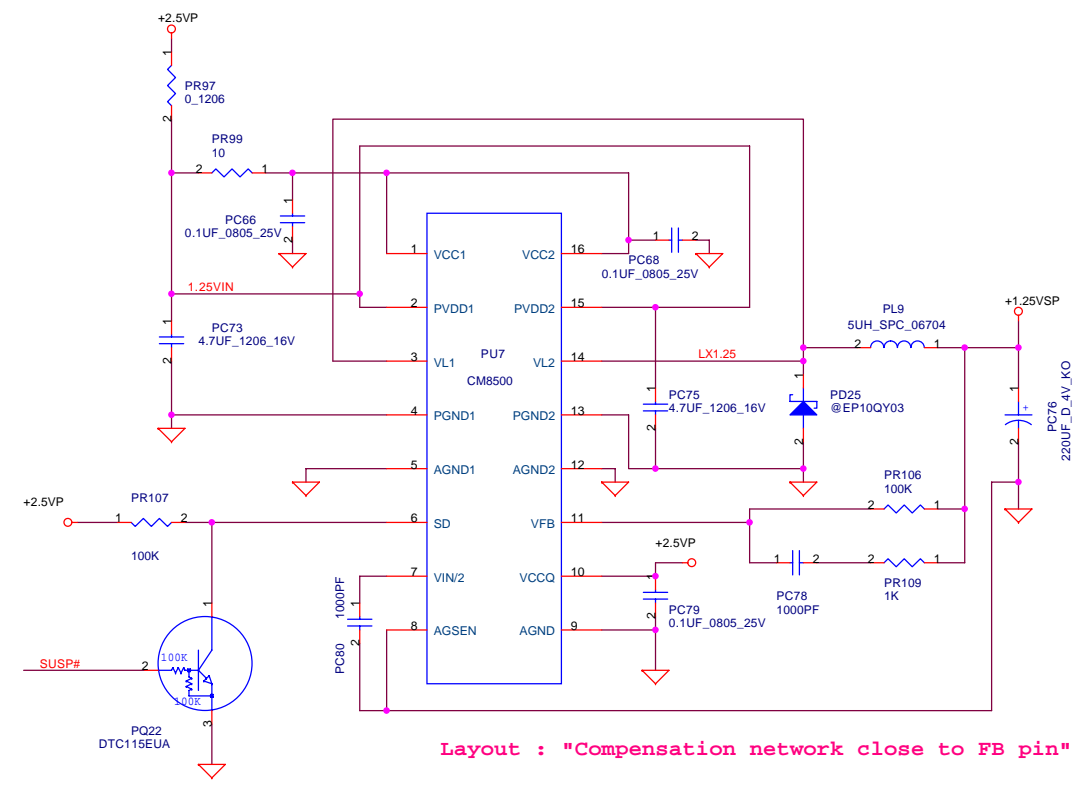
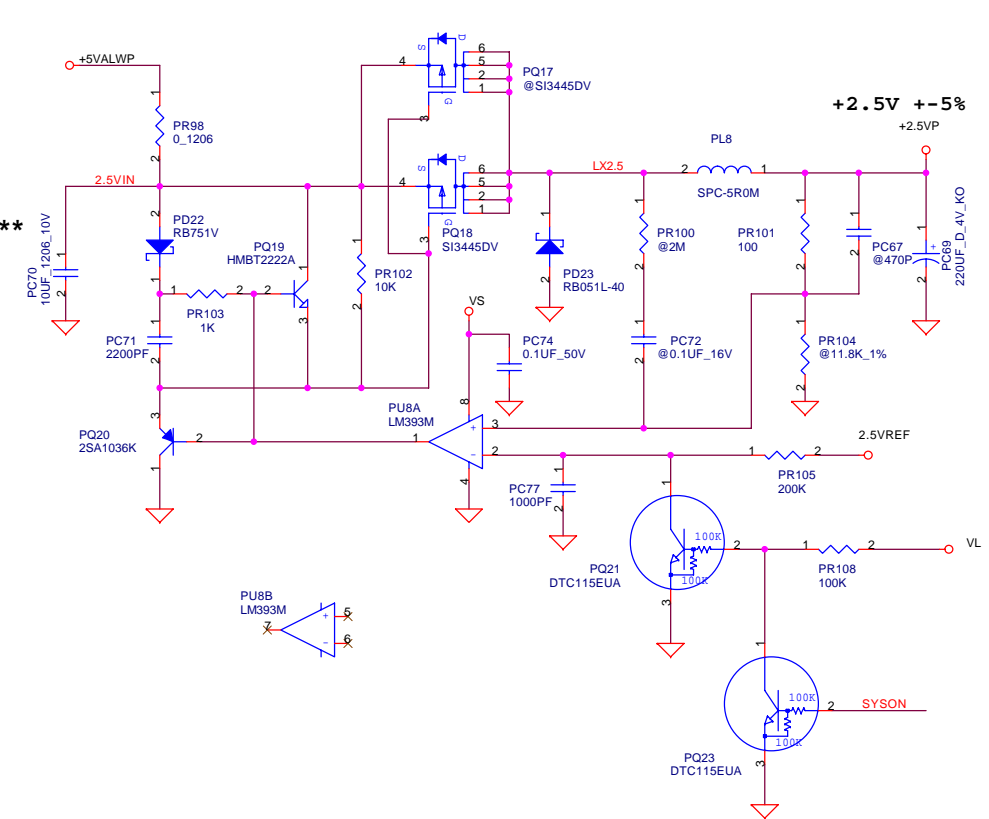


**
PH2 near main Battery CONN :
 BAT. thermal protection at 73 degree C
 Recovery at 50 degree C



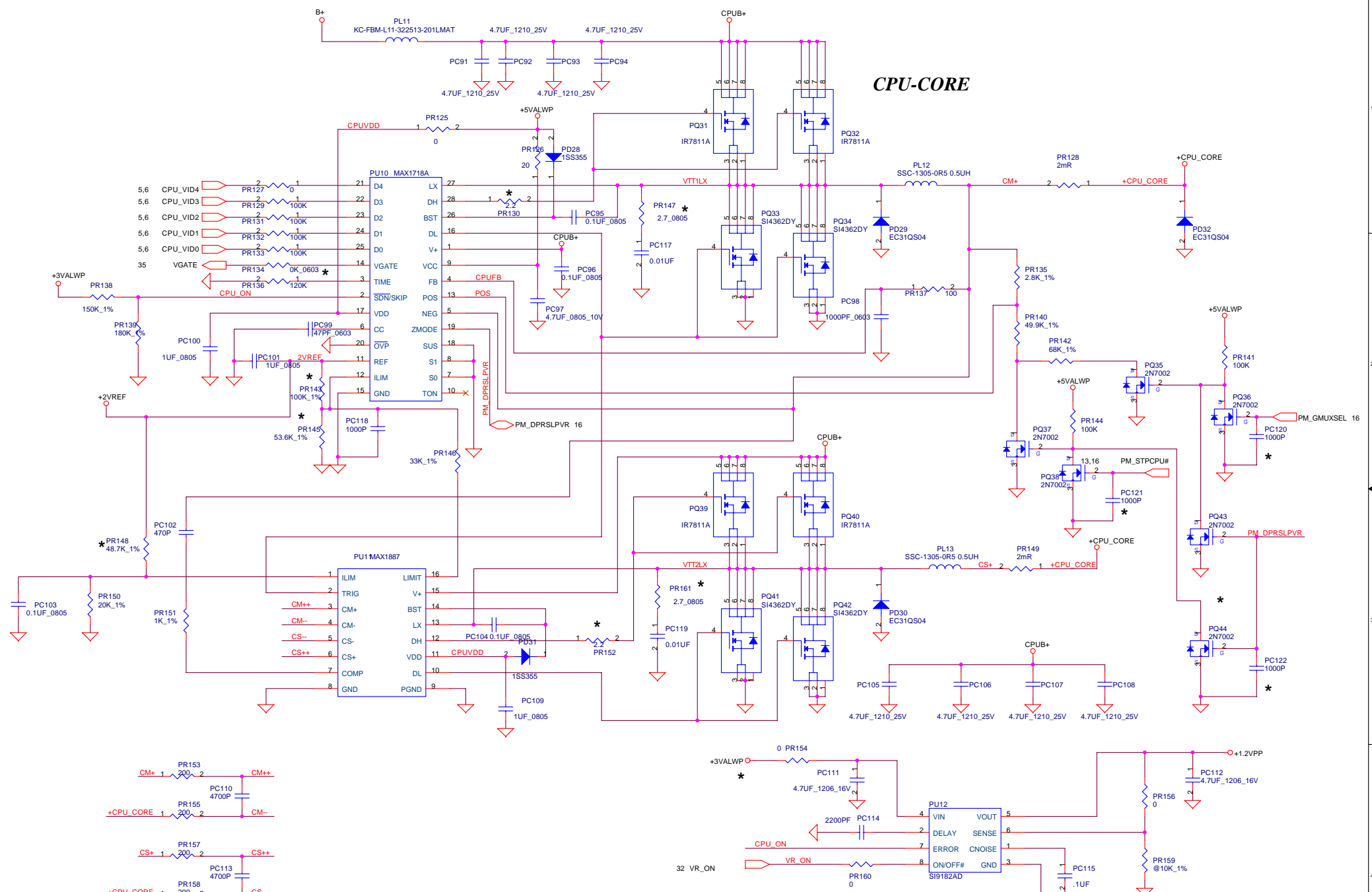
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CPU-CORE

	GMUXSEL	CPUSTP#	DPRSPLVR	VCORE'	Offset	VCORE
PM	1	1	0	1.30V	0%	1.30V
PM D-S	1	0	0	4.62%	1.239V	
BM	0	1	0	1.20V	2.0%	1.176V
BM D-S	0	0	0	4.62%	1.144V	
Deeper	X	0	1	1.0V	0%	1.0V

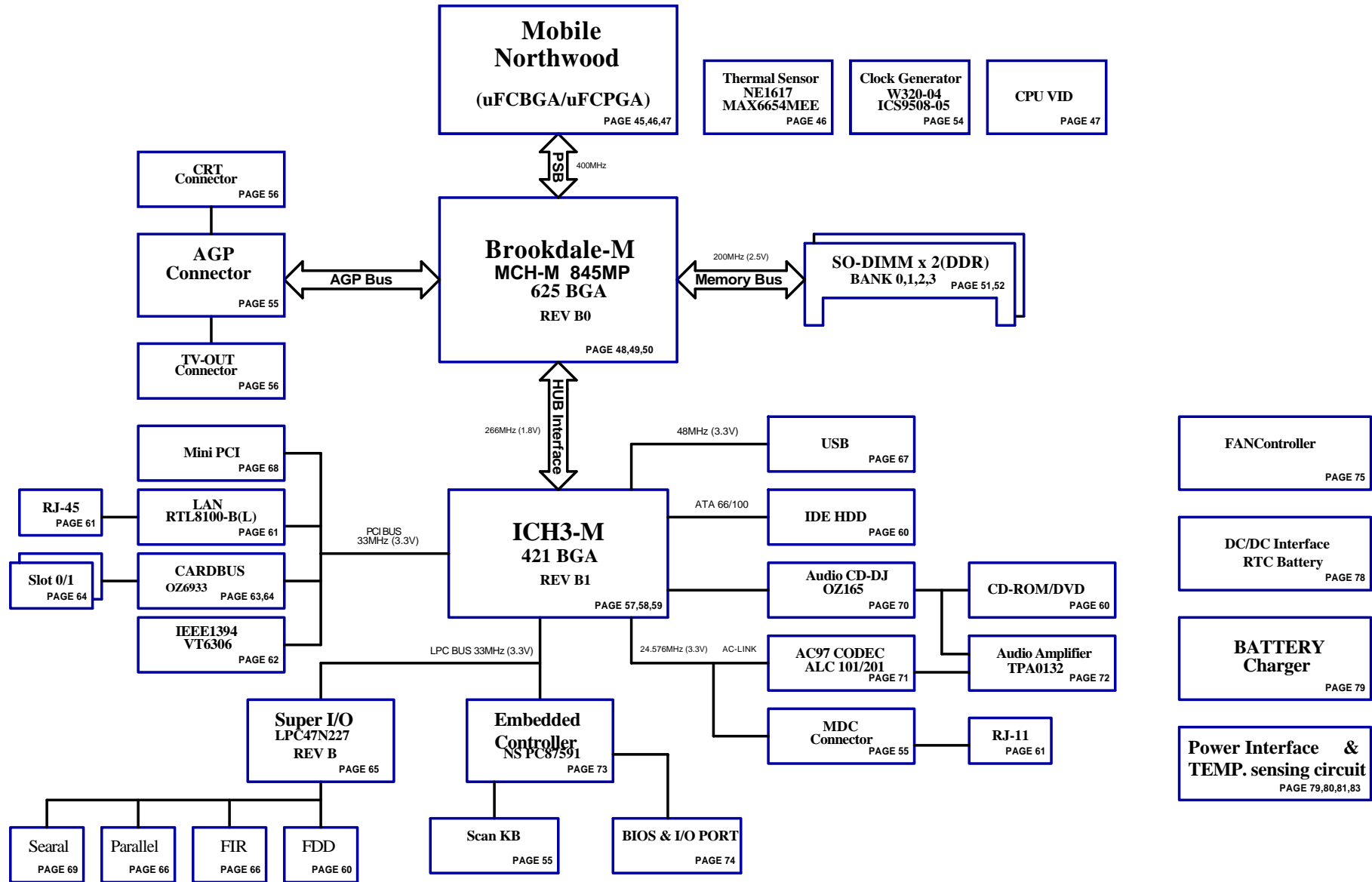
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ACL10 LA-1331 BLOCK DIAGRAM



Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	NA	NA	NA
B+	AC or battery power rail for power circuit.	NA	NA	NA
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
1.2VP	1.2VP switched power rail for CPU VID	ON	OFF	OFF
+1.25VS	1.25VS power rail	ON	OFF	OFF
+1.5VS	AGP 4X	ON	OFF	OFF
+1.8VALW	1.8V always power rail	ON	ON	ON*
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5V	2.5V power rail	ON	ON	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5V	5V power rail	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
+12V	12V power rail	ON	ON	OFF
+12VS	12V switched power rail	ON	OFF	OFF
RTCVCC	RTC power	ON	ON	ON
+SDREF	+SDREF power	ON	ON	OFF

Note : "ON*" means that this power plane is "ON" only with AC power available, otherwise it is "OFF".

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
IEEE 1394	AD16	0	PIRQA
Mini-PCI	AD18	1/4	PIRQC/PIRQD
CardBus	AD20	2	PIRQA/PIRQB
LAN	AD17	3	PIRQB
SM	AD22	-	PIRQC/PIRQD

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011Xb	MAX6654MEE	1001 110Xb
EEPROM(24C16/02)	1010 000Xb	OZ165	1011 0100b (B4h)
(24C04)	1011 000Xb	Smart Battery	0001 011Xb
		Docking	0011 011Xb
		DOT Board	XXXX XXXXb

EC SM Bus2 address

ICH3-M SM Bus address

Device	Address
Clock Generator W320-04 / ICS9508-05	1101 0000

DDR SODIMM SM Bus address

DDR SLOT	SA2	SA1	SA0
DDR SODIMM0 (REVERSE)	0	0	0
DDR SODIMM1 (NORMAL)	0	0	1

PIR

REV 0.1

Date	Page	Description
2001/12/29	7	Change R212,R214 & R213 to 8.2K ohm for Intel recommend
2001/12/29	14	Stuff R361=22 Ohm and no-stuff R360 for Data-IN1 of MDC module.
2001/12/29	15	Change L28 & L29 to 0 Ohm for EMI issue.
2001/12/29	16	Change R39 power-plane to +3VALW for Resume-well Power-plane(+3VALW)
2001/12/29	17	DEL C73, C87, C371 for EMI issue.
2001/12/29	17	Change L37 power-plane to +1.8VS for Intel recommend.
2001/12/29	17	Change R279 power-plane to +3VS for Intel recommend.
2001/12/29	17	Change U29 pinV22,U18 & P14 power-plane to +CPU_CORE for Intel recommend.
2001/12/29	17	Change R284 power-plane to +3VALW for Intel recommend.
2001/12/29	18	Change "SMB_ALERT#" power-plane to +3VALW for "RESUME-WELL" power-plane(+3VALW).
2001/12/29	18	Exchang D13,D14,D16,D17,D18 and R28,R34,R30,R29 to RP135,R466,R468 for cost-down.
2001/12/29	20	Add D43 for leakage.
2001/12/29	21	Exchang L42 to L52,L53, L54, L55 for ME limitation.
2001/12/29	27	Add D42 for leakage.
2001/12/29	31	Add R465 for PC99 Spec.
2001/12/29	34	Add C368, C369 for EMI solution.
2001/12/29	35	EC control "EC_RSMRST#". ->DEL R92, Stuff R48.
2001/12/29	35	Change R97 to 100K for "VGATE" of Max1718A issue.-> Change PR134= 0 Ohm.
2002/01/07	39	Change PR68 from 10k_1% to 10.5k_1%.(increase 5valwp to 5.125v).
2002/01/07	40	Change PR81 from 2.15k_1% to 1.87k_1%.(CPU thermal OTP from 83+-3C to 85+-3C).
2002/01/07	42	Add PR147, PR161 to 2.7_0805. for EMI requirement.
2002/01/07	42	Add PC120, PC121, PC122 to 1000pf. for ESD.
2002/01/07	42	Add PQ44 to 2N7002 for CPU SPEED STEP.
2002/01/07	42	Change PR130, PR152 from 0 to 2.2. for EMI requirement.
2002/01/07	42	Change PR143 from 53.6k_1% to 100k_1%. for CPU OCP.
2002/01/07	42	Change PR145 from 100k_1% to 53.6k_1%. for CPU OCP.
2002/01/07	42	Change PR148 from 30k_1% to 48.7k_1%. for CPU OCP.
2002/01/07	42	Change PU12 VIN from +2.5VP to +3VALWP.

REV 0.2

Date	Page	Description
2002/01/11	40	Change PH1 and PH2 design by high active for AC-IN issue.

REV 0.3

Date	Page	Description
None		

REV 1.0

Date	Page
None	

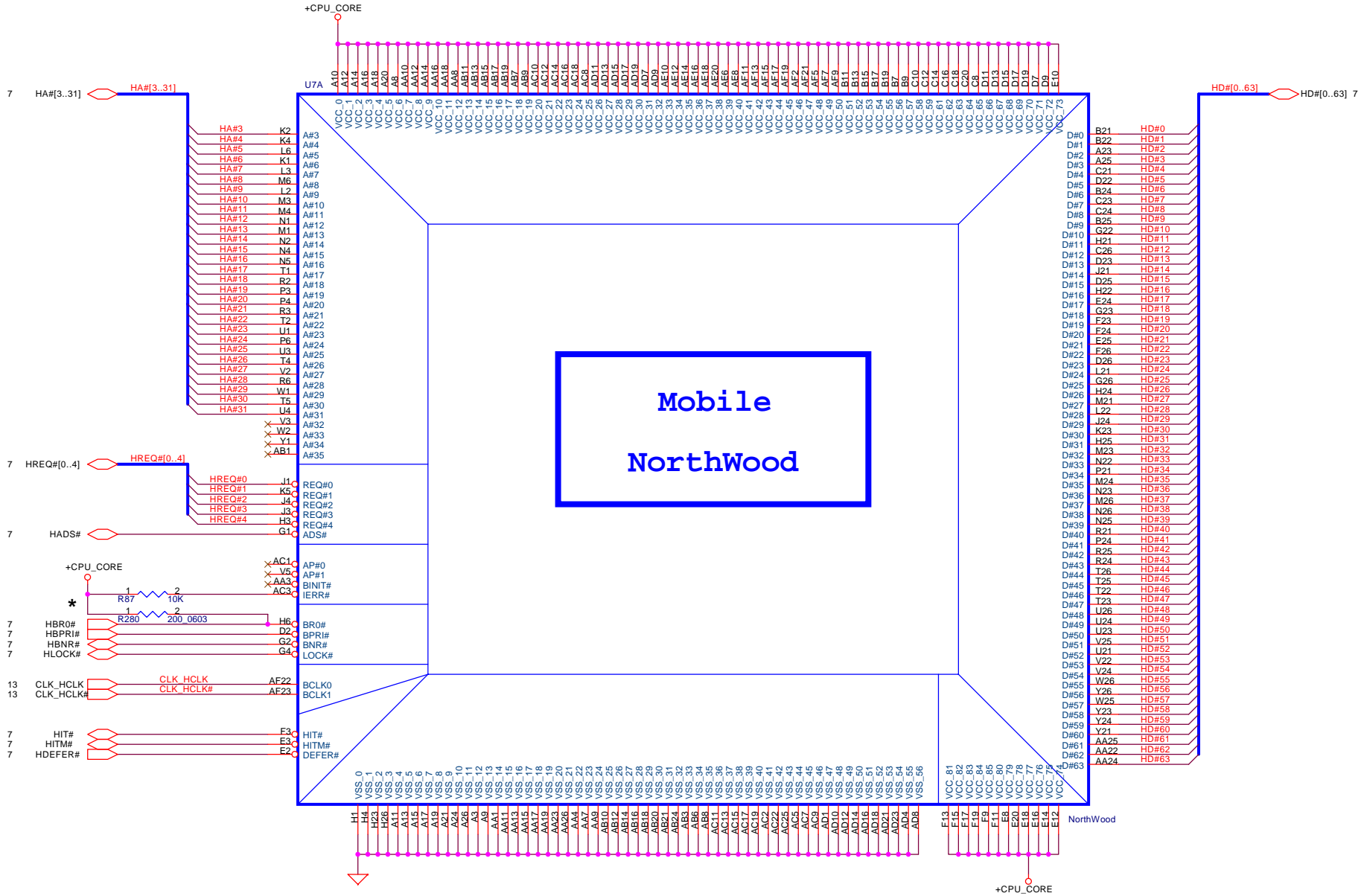
REV 2.0

Date	Page	Description
2002/04/10	20	GCR: (For LAN Issue) <1>-Isolation U18 pin6 for Realtek application notice. <2>-Change R204 from 5.9K+-1% to 5.6K +-1%. <3>-Change L23 from 4.7UH to 0 ohm.

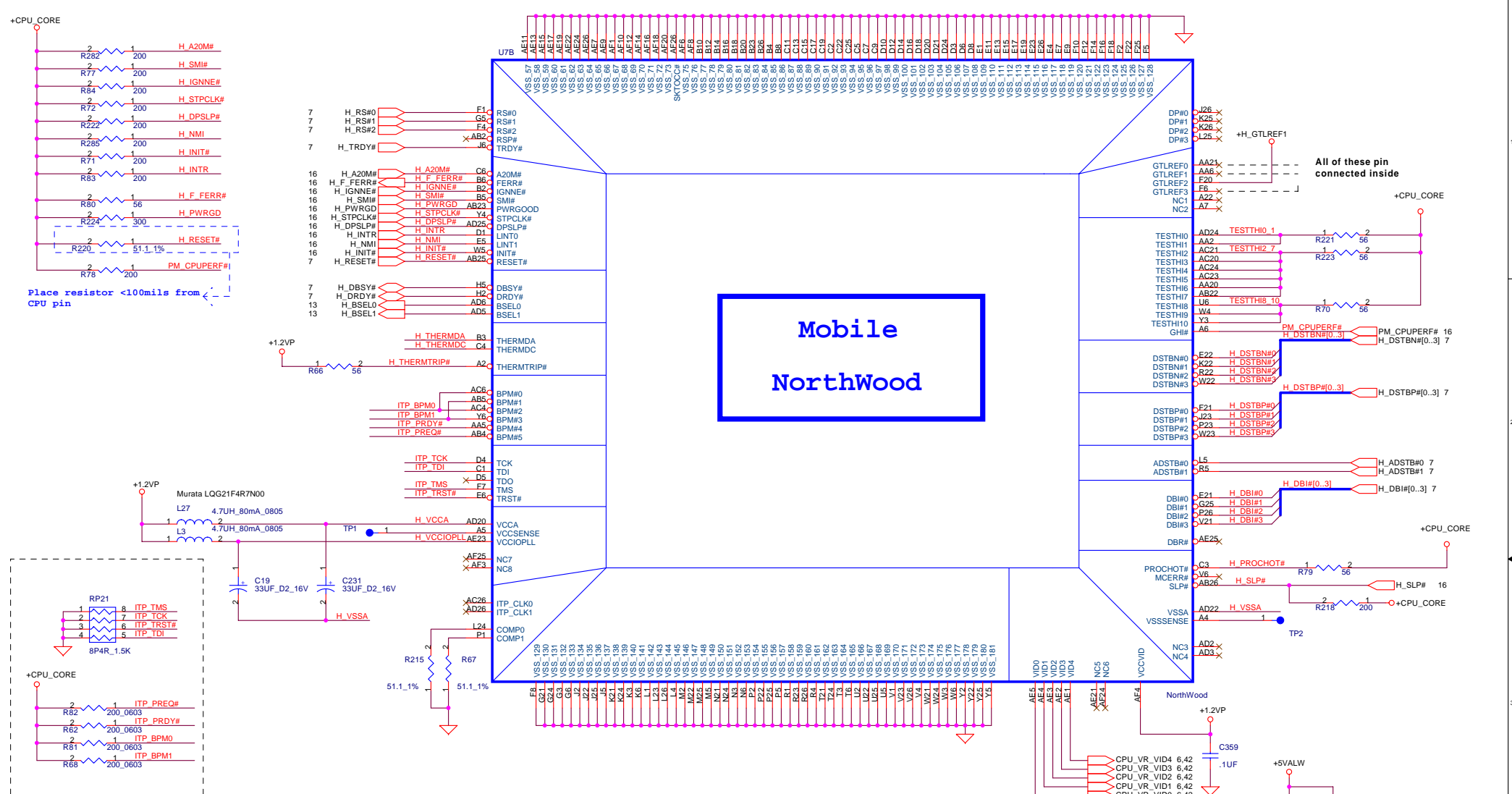
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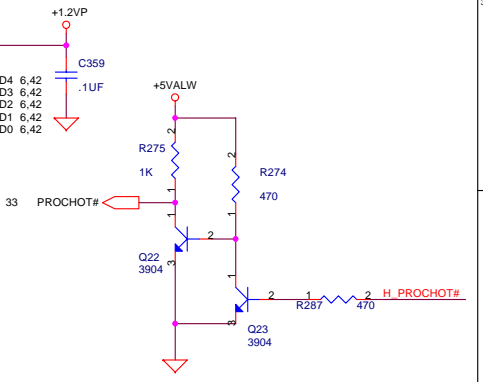
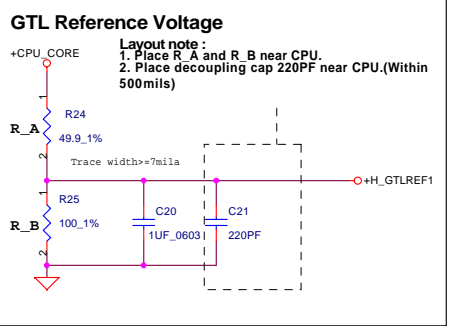
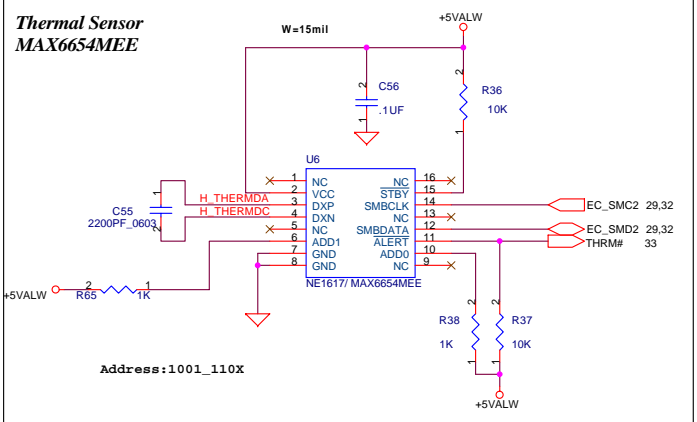
Mobile NorthWood



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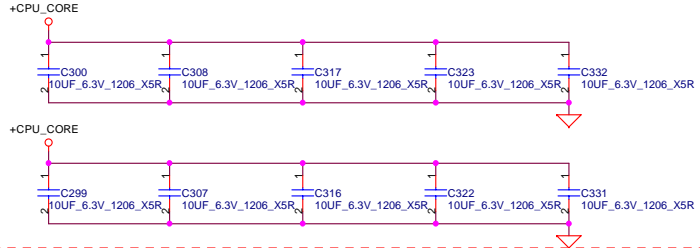
Mobile NorthWood



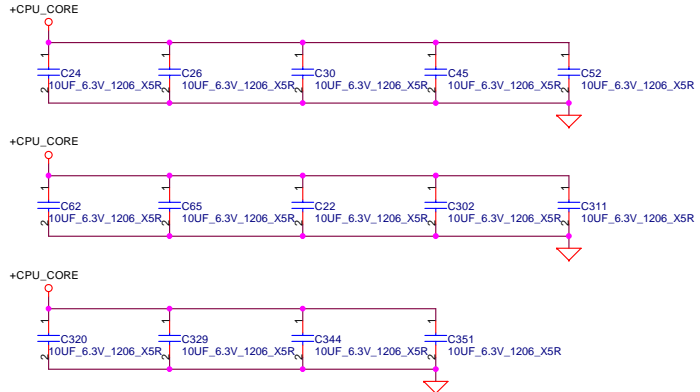
Layout note :

Place close to CPU. Use 2-3 vias per PAD.
Place 22uF caps underneath balls on solder side.
Place 10uF caps on the peripheral near balls.
Use 2-3 vias per PAD.

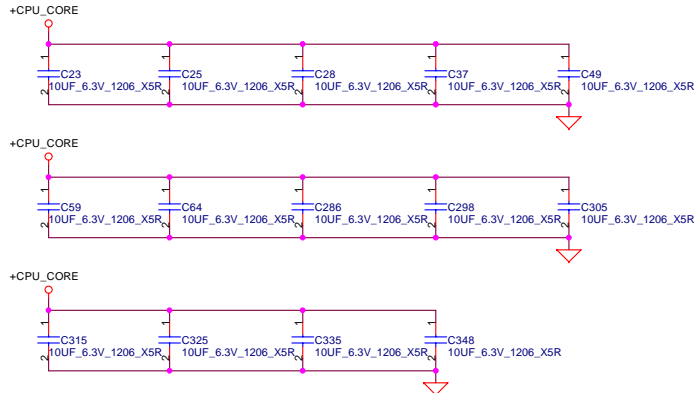
Please place these cap in the socket cavity area



Please place these cap on the socket north side



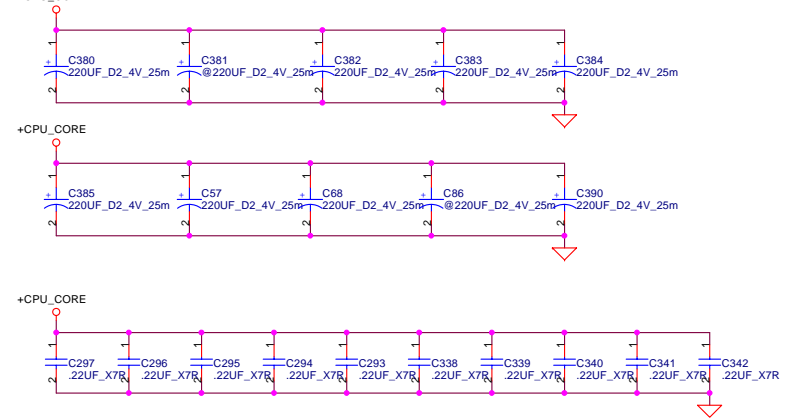
Please place these cap on the socket south side



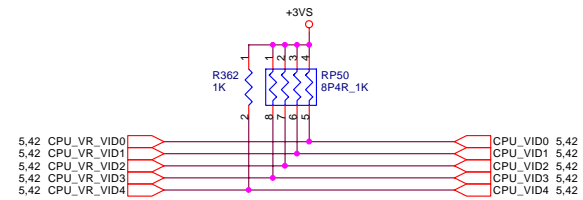
Layout note :

Place close to CPU power and ground pin as possible (<1inch)

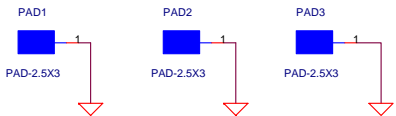
Used ESR 25m ohm cap total ESR=2.5m ohm



CPU Voltage ID

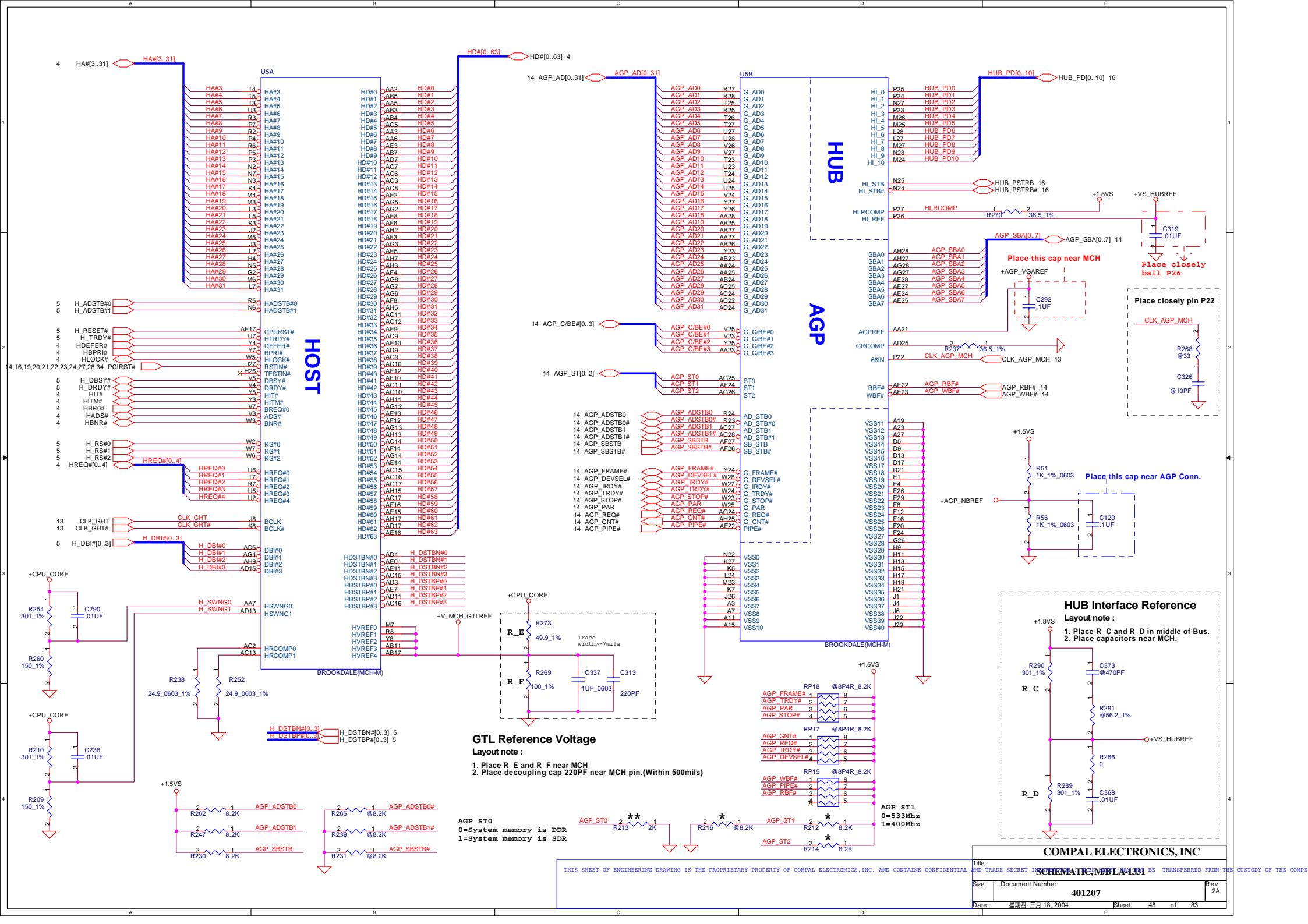


EMI Clip PAD for CPU



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HOST

HUB

AGP

GTL Reference Voltage

- Layout note :
1. Place R_E and R_F near MCH
 2. Place decoupling cap 220PF near MCH pin.(Within 500mils)

AGP_ST0
 0=System memory is DDR
 1=System memory is SDR

HUB Interface Reference

- Layout note :
1. Place R_C and R_D in middle of Bus.
 2. Place capacitors near MCH.

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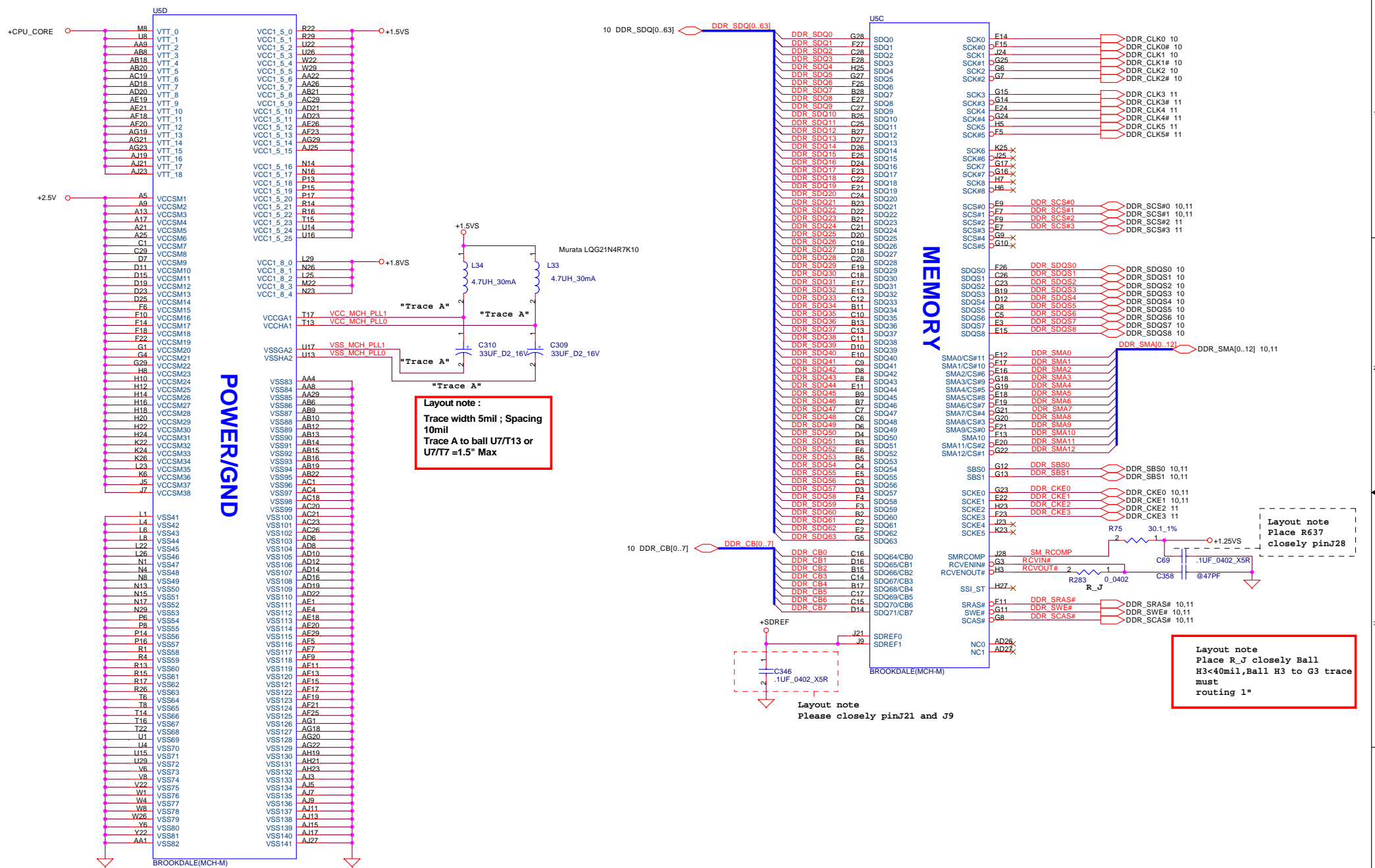
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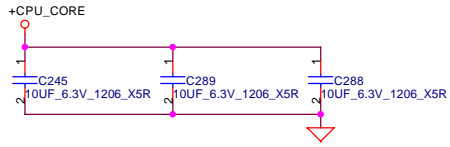
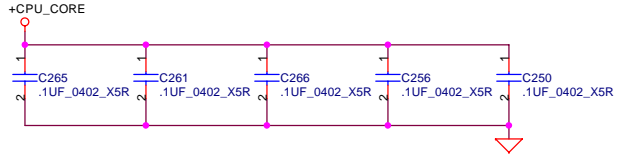
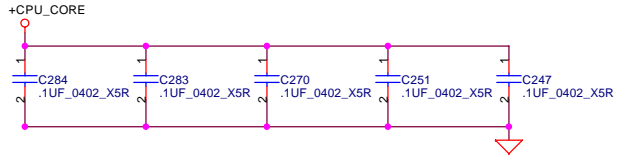
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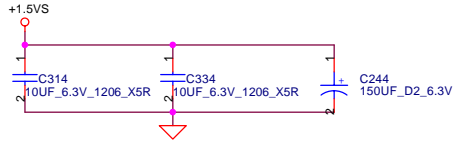
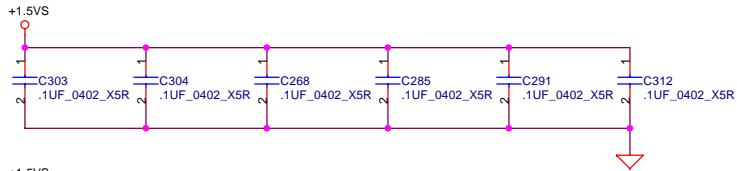
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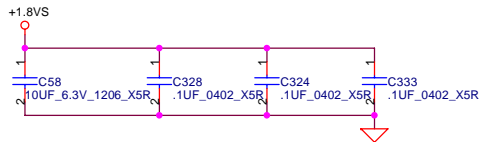
Layout note : Processor system bus
 Distribute as close as possible
 to MCH Processor Quadrant.(between VTTF5B and VSS pin)



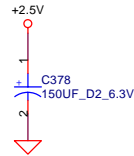
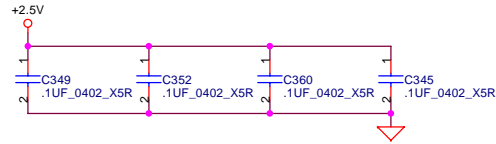
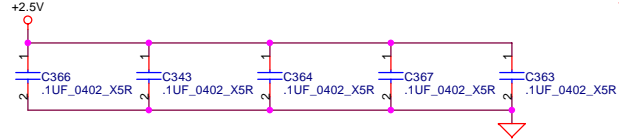
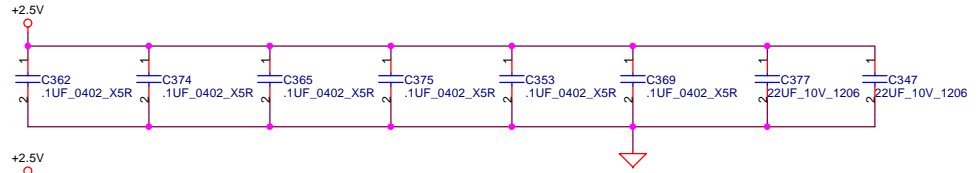
Layout note : AGP/CORE
 Distribute as close as possible
 to MCH Processor Quadrant.(between VCCAGP/VCCCORE
 and VSS pin)



Layout note : Hub-Link
 Distribute as close as possible
 to MCH Processor Quadrant.(between VCCHL and VSS pin)

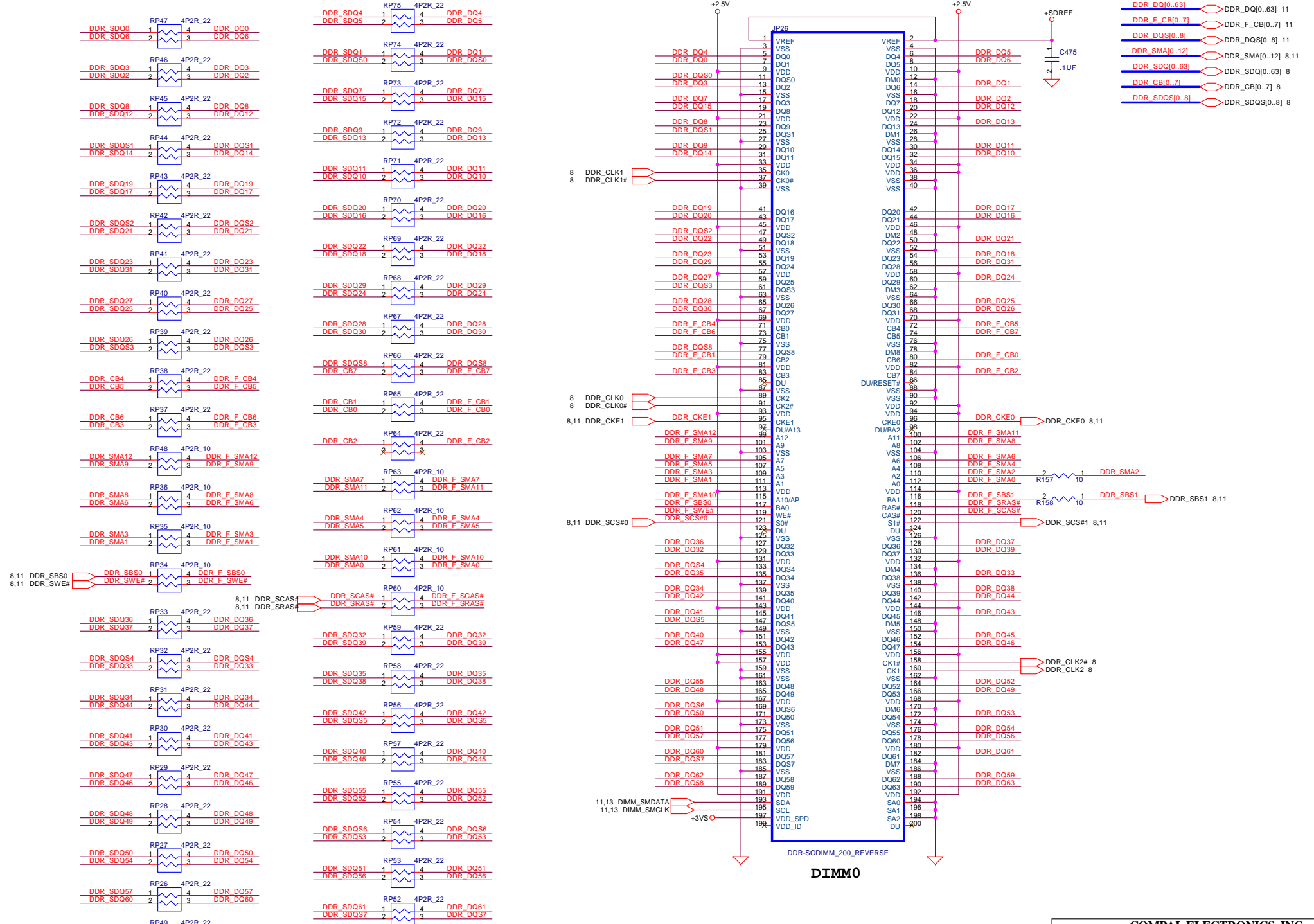


Layout note : DDR Memory interface
 Distribute as close as possible
 to MCH Processor Quadrant.(between VCCSM and VSS pin)



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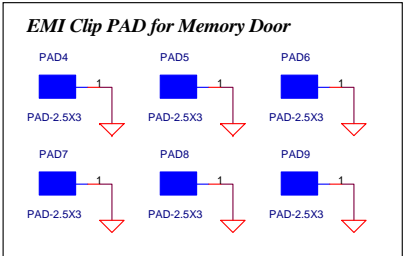
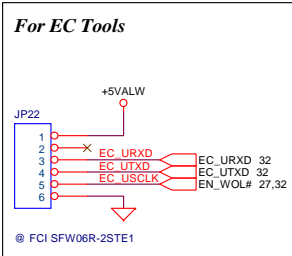
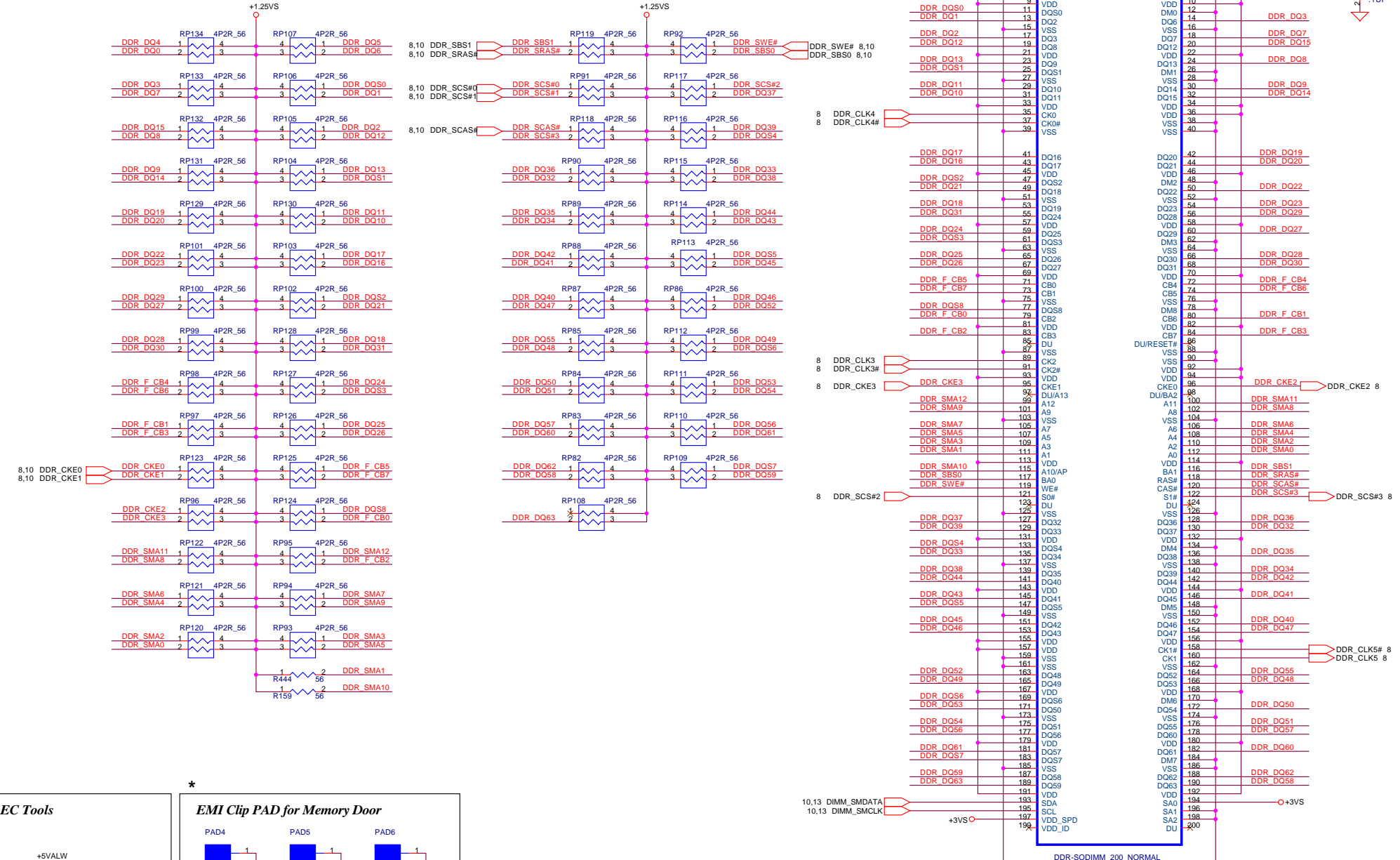


- DDR_DQ[0..63] 11
- DDR_F_CBI[0..7] 11
- DDR_DS[0..8] 11
- DDR_SMA[0..12] 8,11
- DDR_SDQ[0..63] 8
- DDR_CBI[0..7] 8
- DDR_SDQS[0..8] 8

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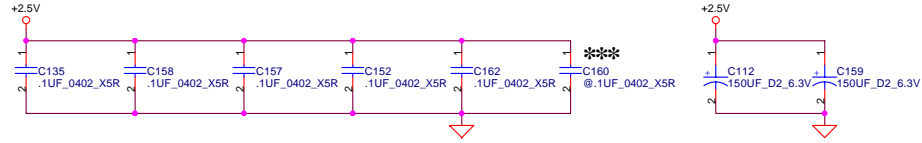
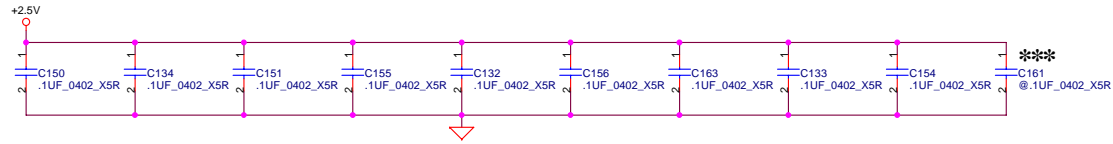
10 DDR_F_CB[0..7] \Rightarrow DDR_F_CB[0..7]
 10 DDR_DQS[0..8] \Rightarrow DDR_DQS[0..8]
 10 DDR_DQ[0..63] \Rightarrow DDR_DQ[0..63]
 8,10 DDR_SMA[0..12] \Rightarrow DDR_SMA[0..12]



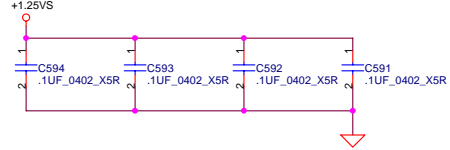
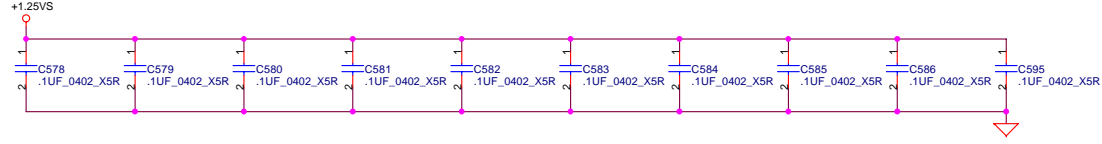
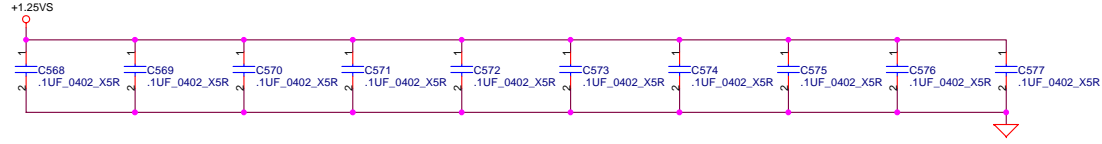
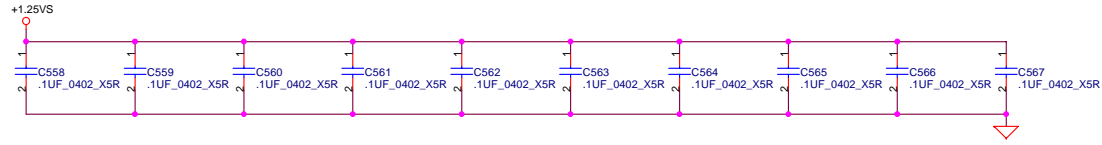
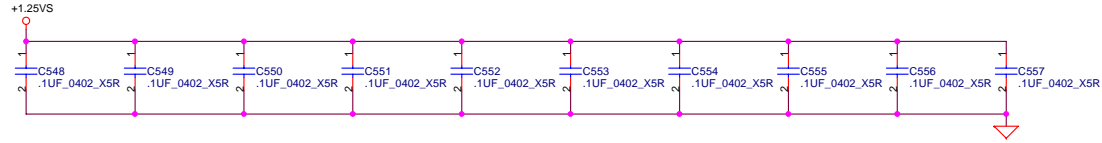
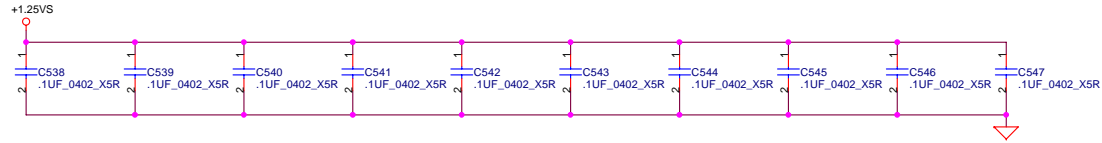
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Layout note :
Distribute as close as possible to DDR-SODIMM.



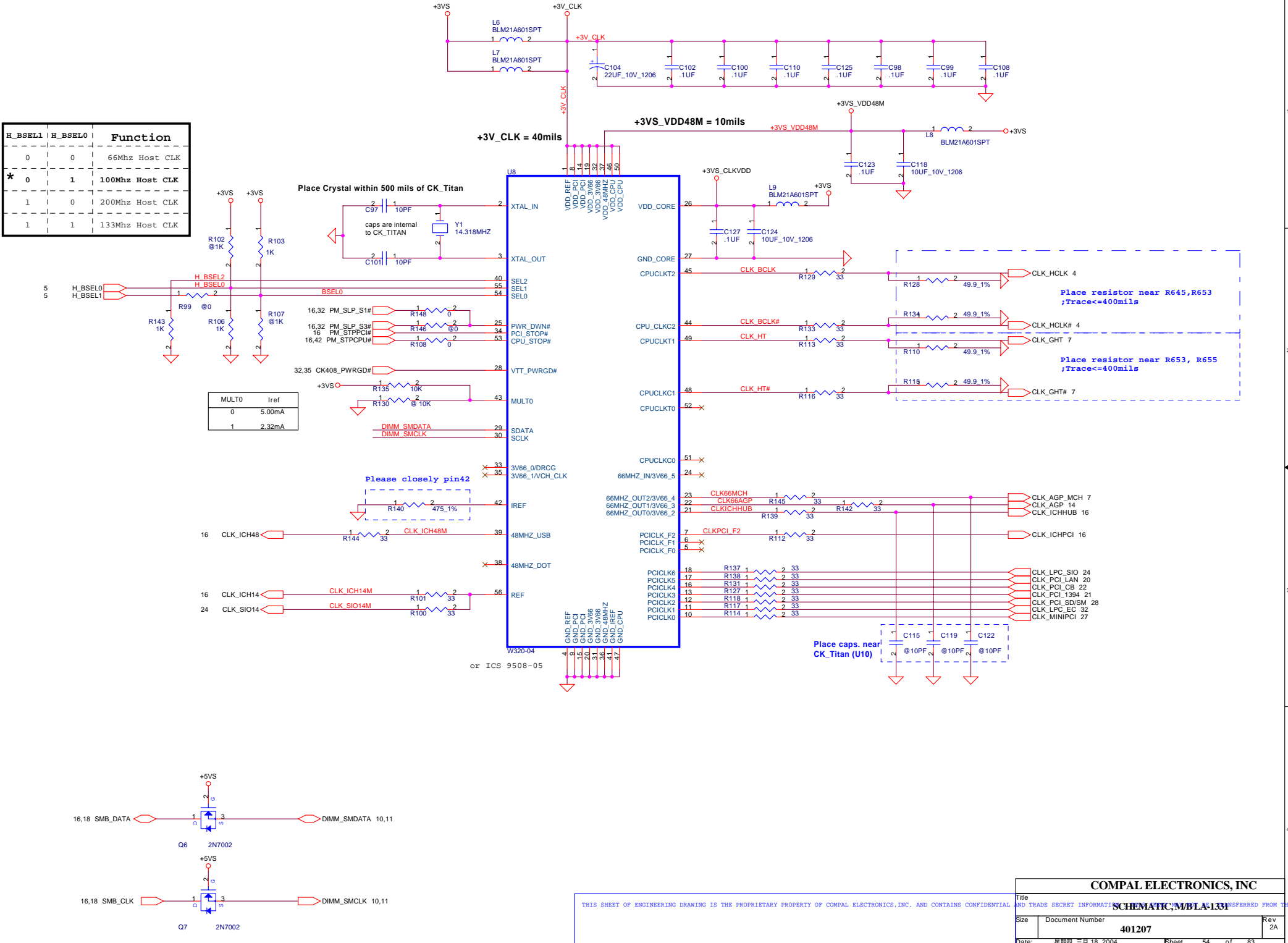
Layout note :
Place one cap close to every 2 pull up resistors termination to +1.25V



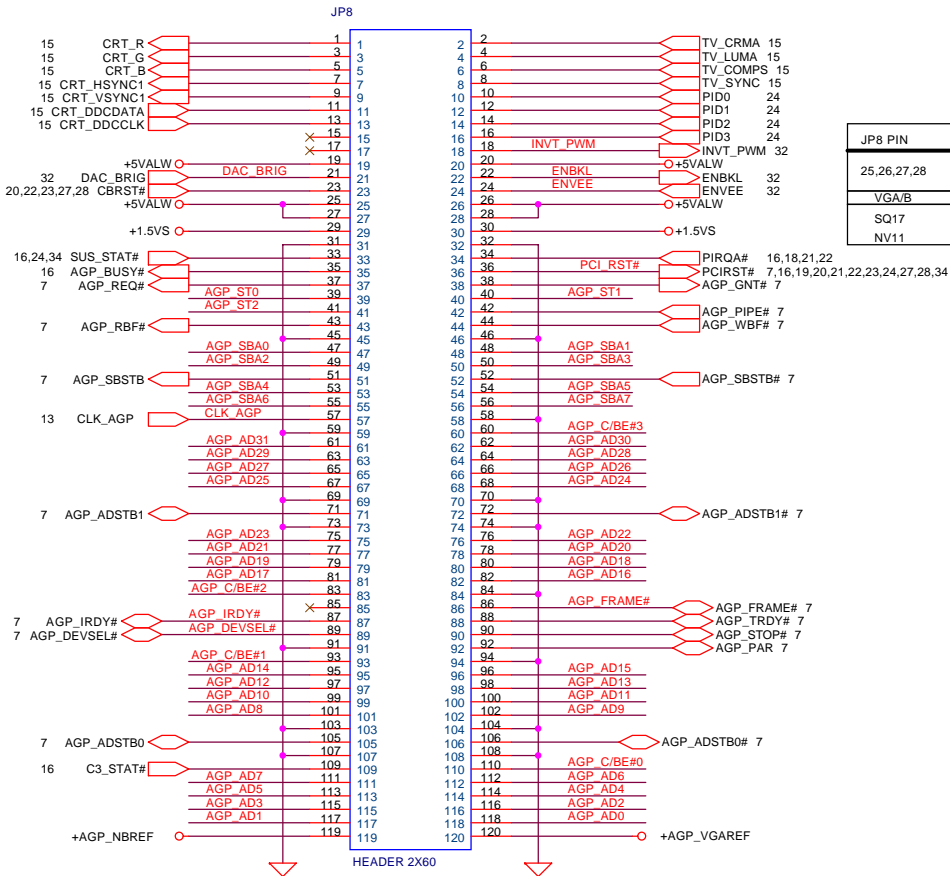
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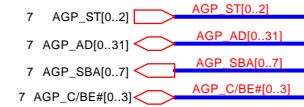
H_BSEL1	H_BSEL0	Function
0	0	66Mhz Host CLK
* 0	1	100Mhz Host CLK
1	0	200Mhz Host CLK
1	1	133Mhz Host CLK



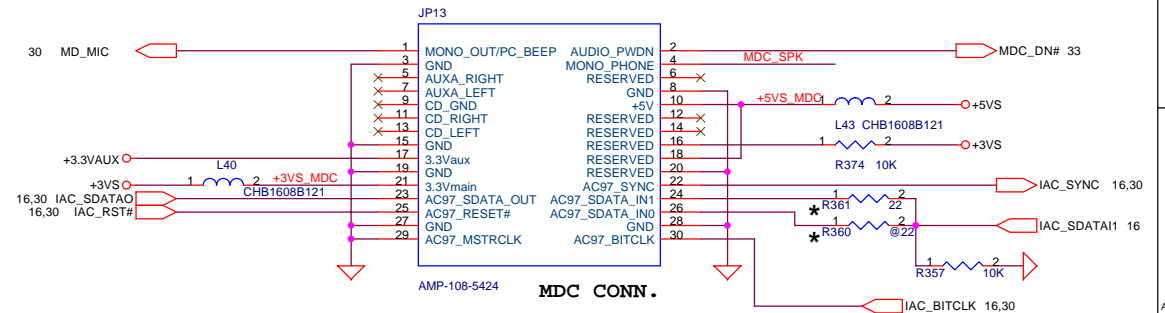
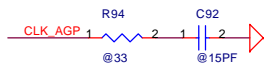
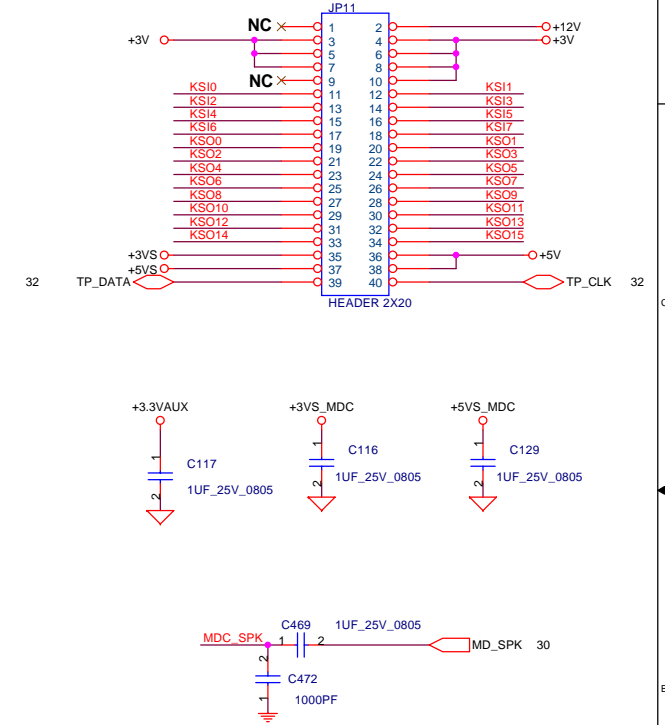
AGP CONN.



JP8 PIN	ACL10	ATL02/ACL00
25,26,27,28	+5VALW	+1.5V
VGA/B		
SQ17	V	X
NV11	V	V



Int. Keyboard CONN.

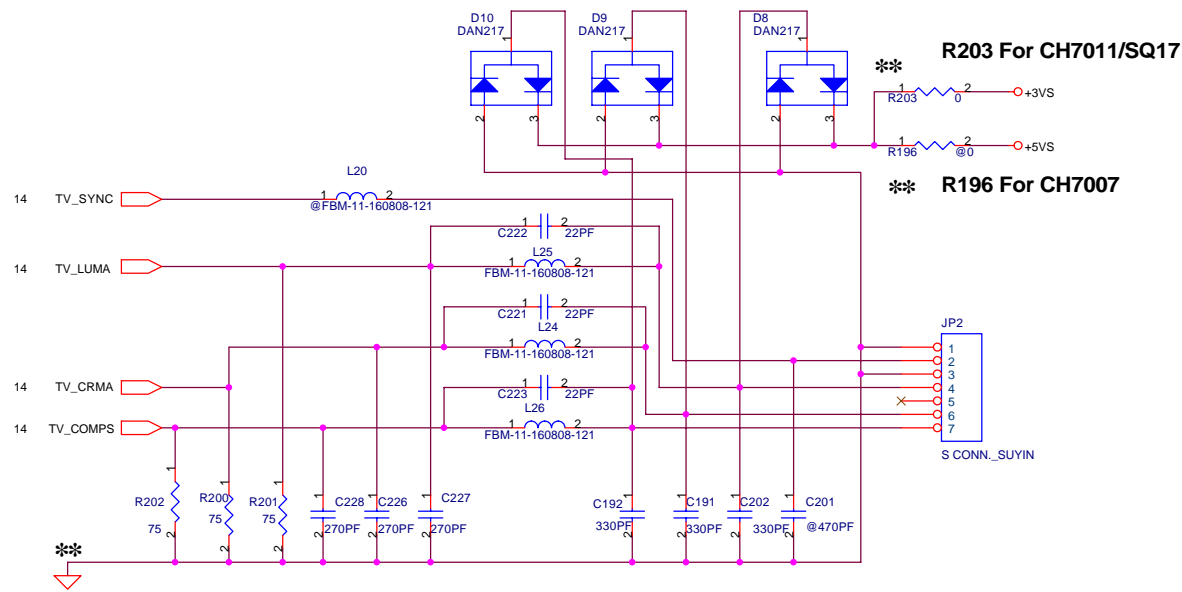


COMPAL ELECTRONICS, INC

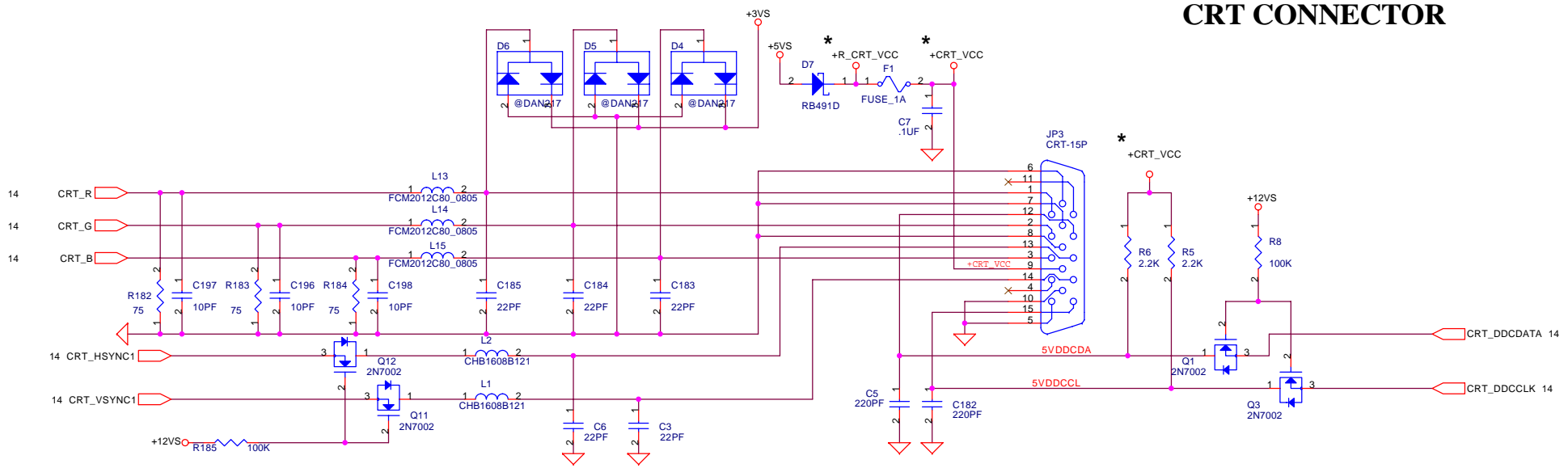
SCHEMATIC, M/B LA-1331

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TV_OUT CONNECTOR



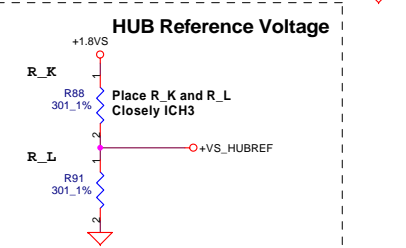
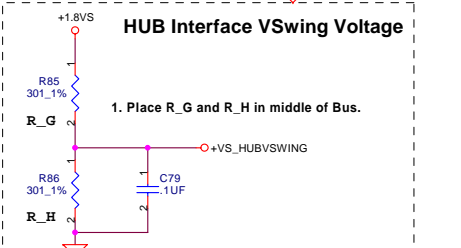
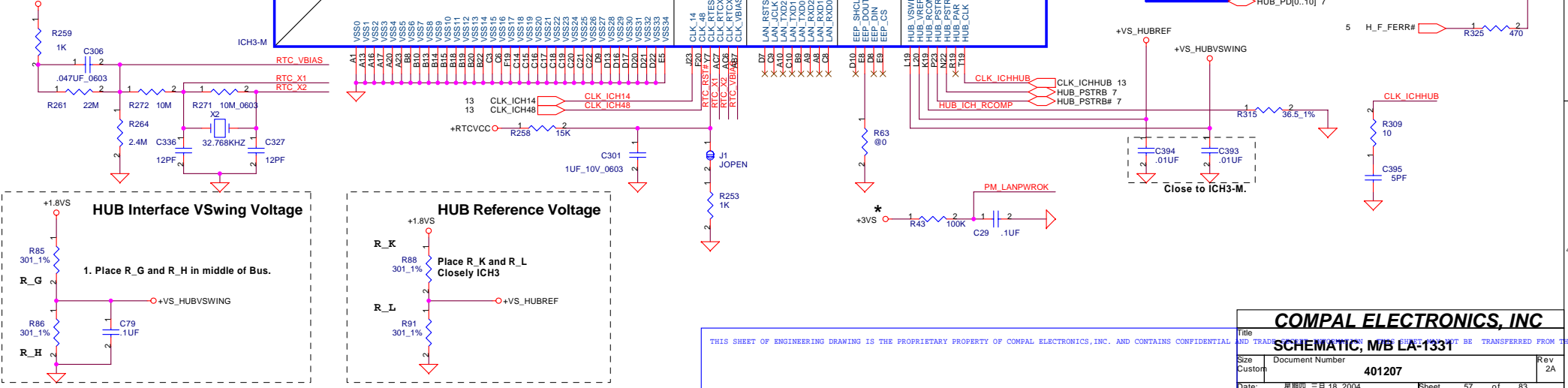
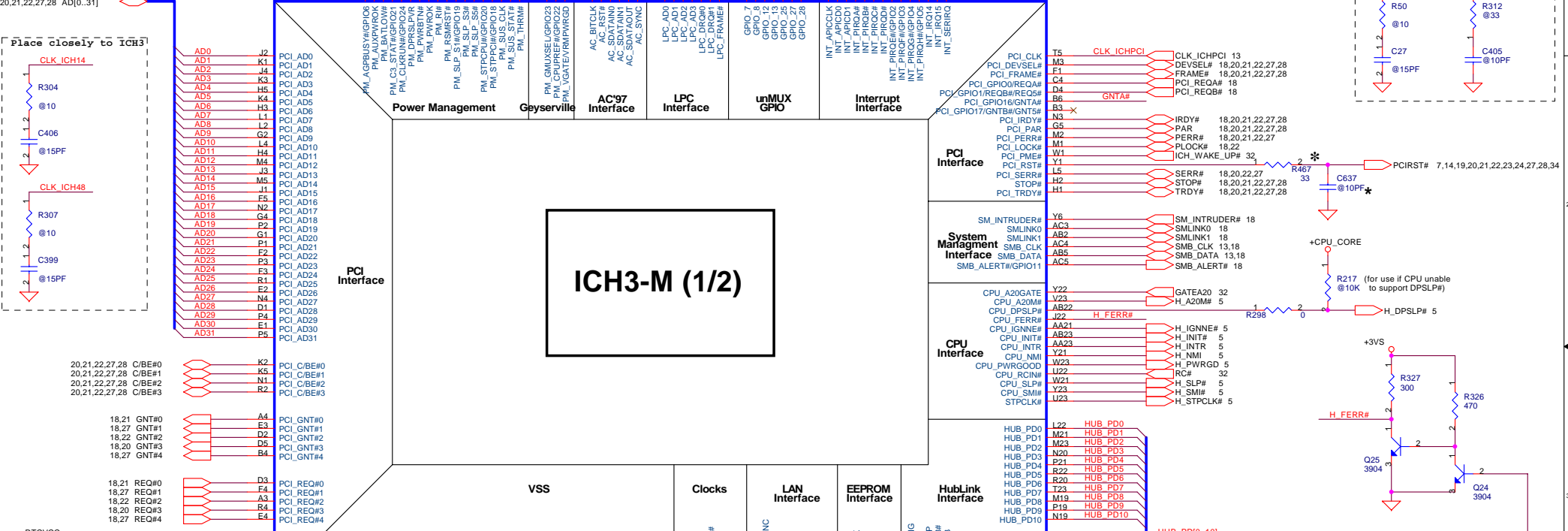
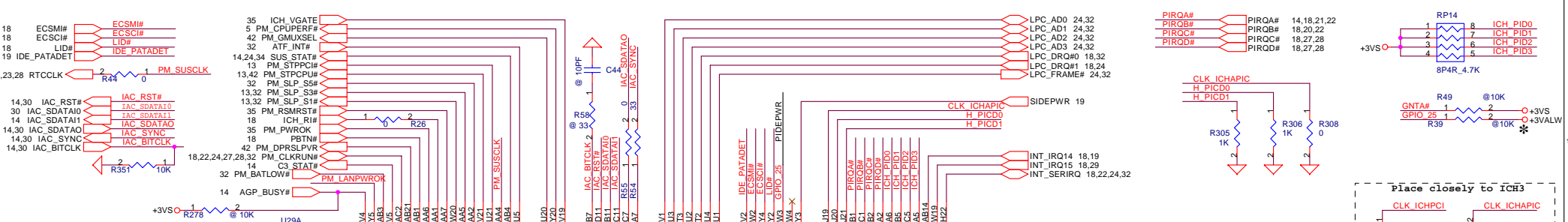
CRT CONNECTOR

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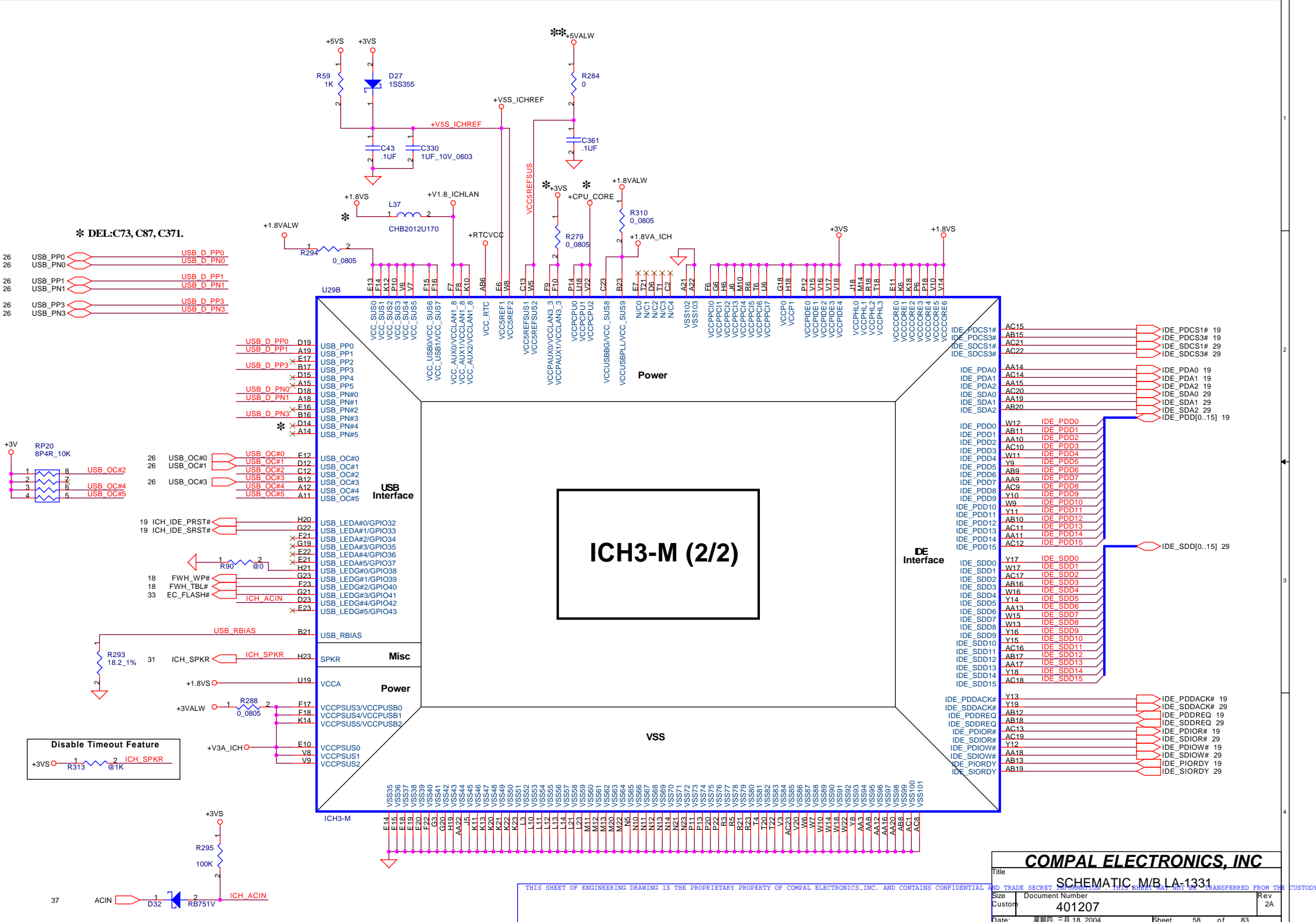
COMPAL ELECTRONICS, INC

Title: **SCHEMATIC, M/B LA-1331**

Size: Custom Document Number: **401207** Rev: 2A

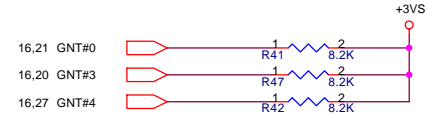
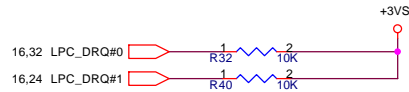
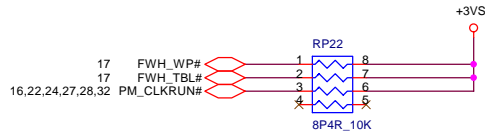
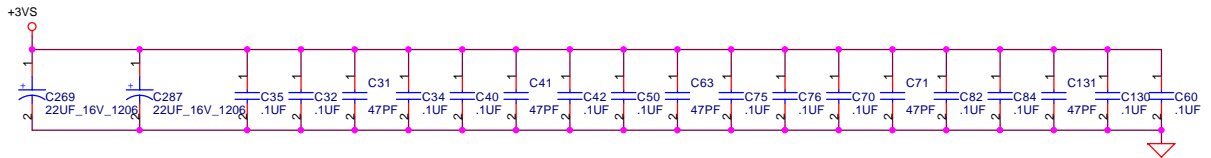
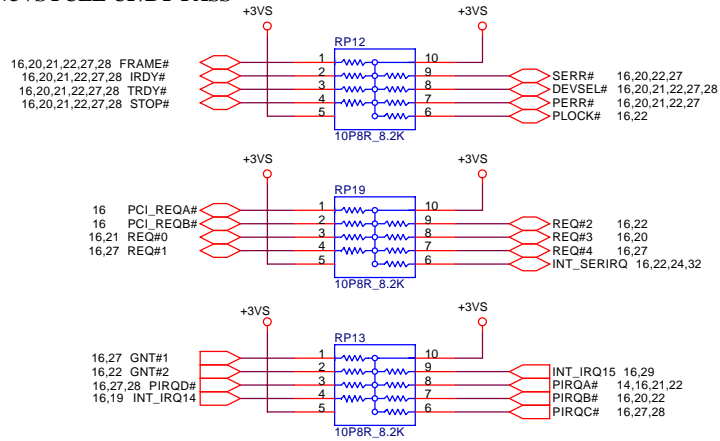
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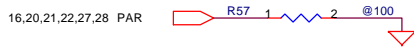
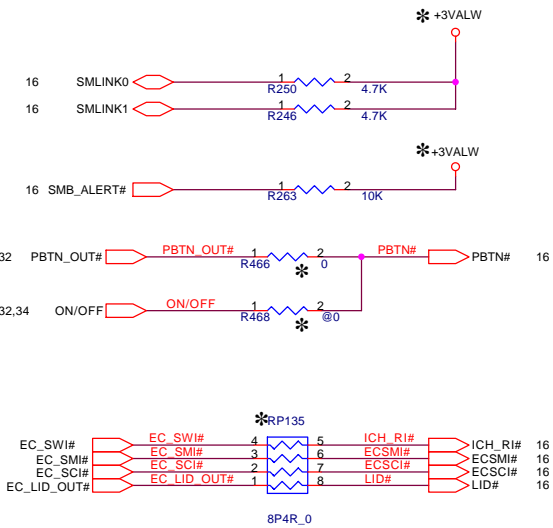


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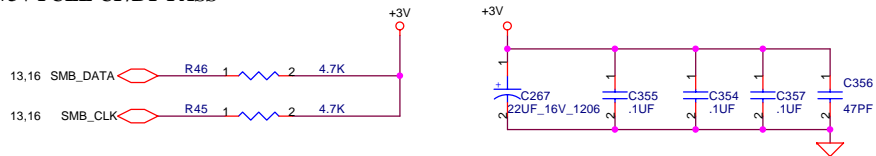
+3VS PULL-UP/BY-PASS



+3VALW PULL-UP



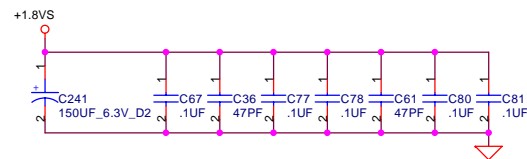
+3V PULL-UP/BY-PASS



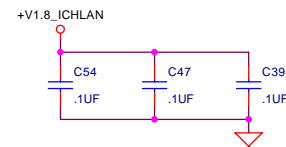
+RTCVCC PULL-UP



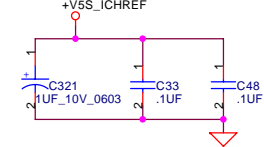
+1.8SV BY-PASS



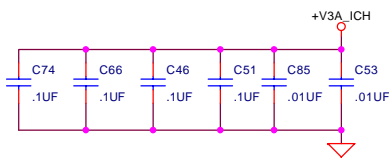
+V1.8S_ICHLAN BY-PASS



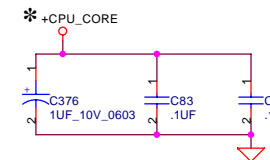
+V5S_ICHREF BY-PASS



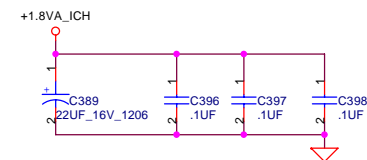
+V3A_ICH BY-PASS



+CPU_CORE BY-PASS



+1.8VA_ICH BY-PASS

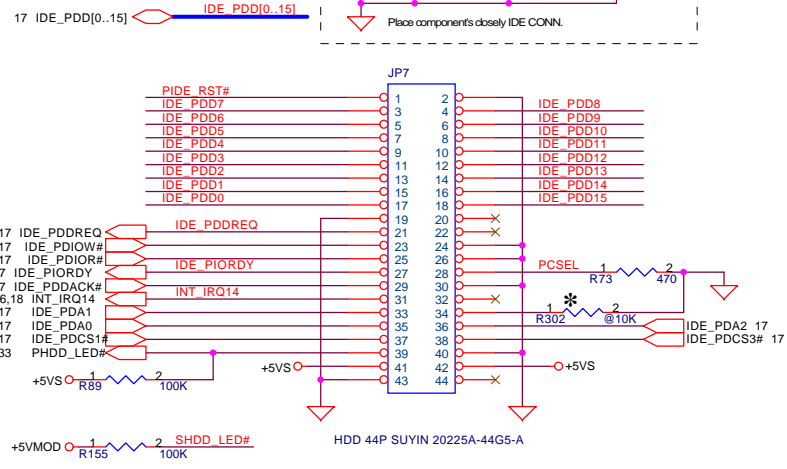
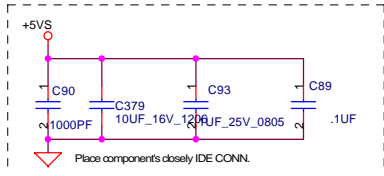


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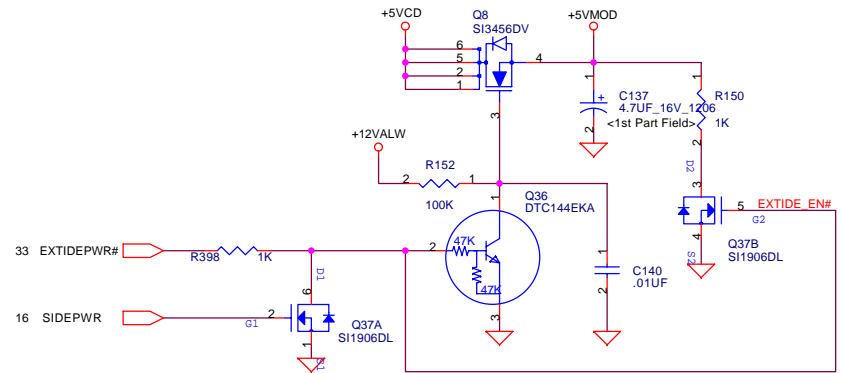
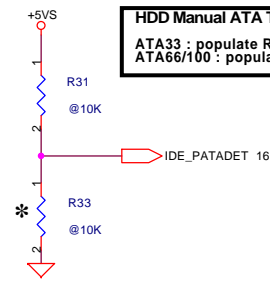
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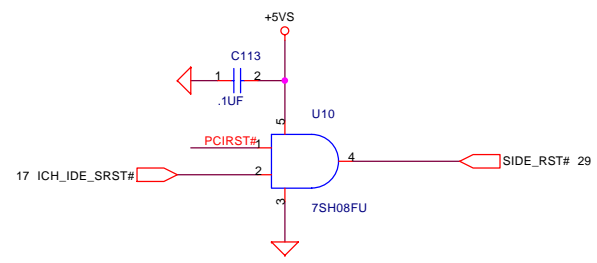
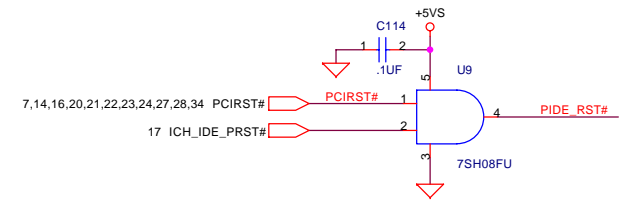
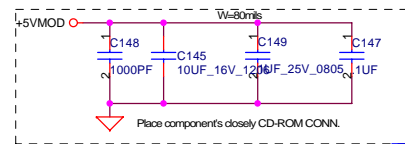
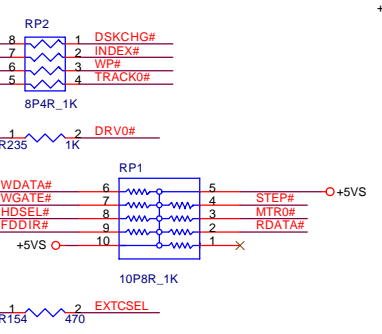
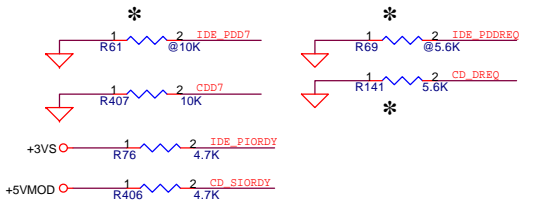
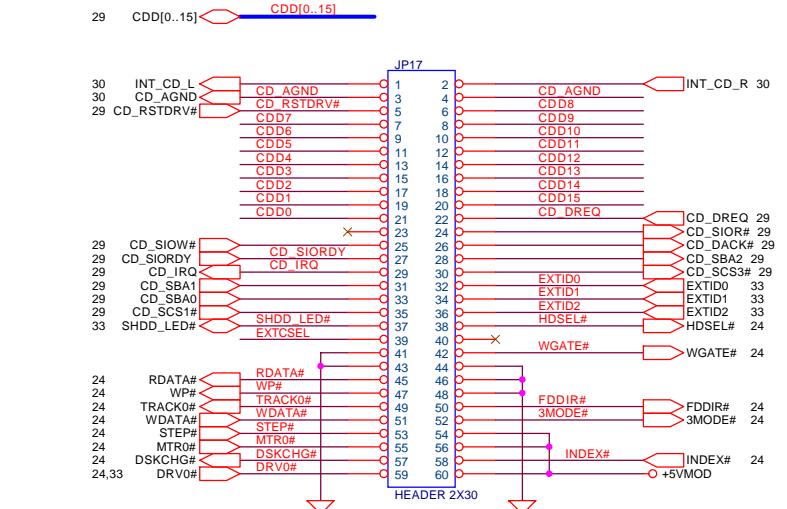
IDE, CD-ROM Module CONN.



HDD Manual ATA Type Selection:
 ATA33 : populate R31, de-populate R33.
 ATA66/100 : populate R33, de-populate R31.



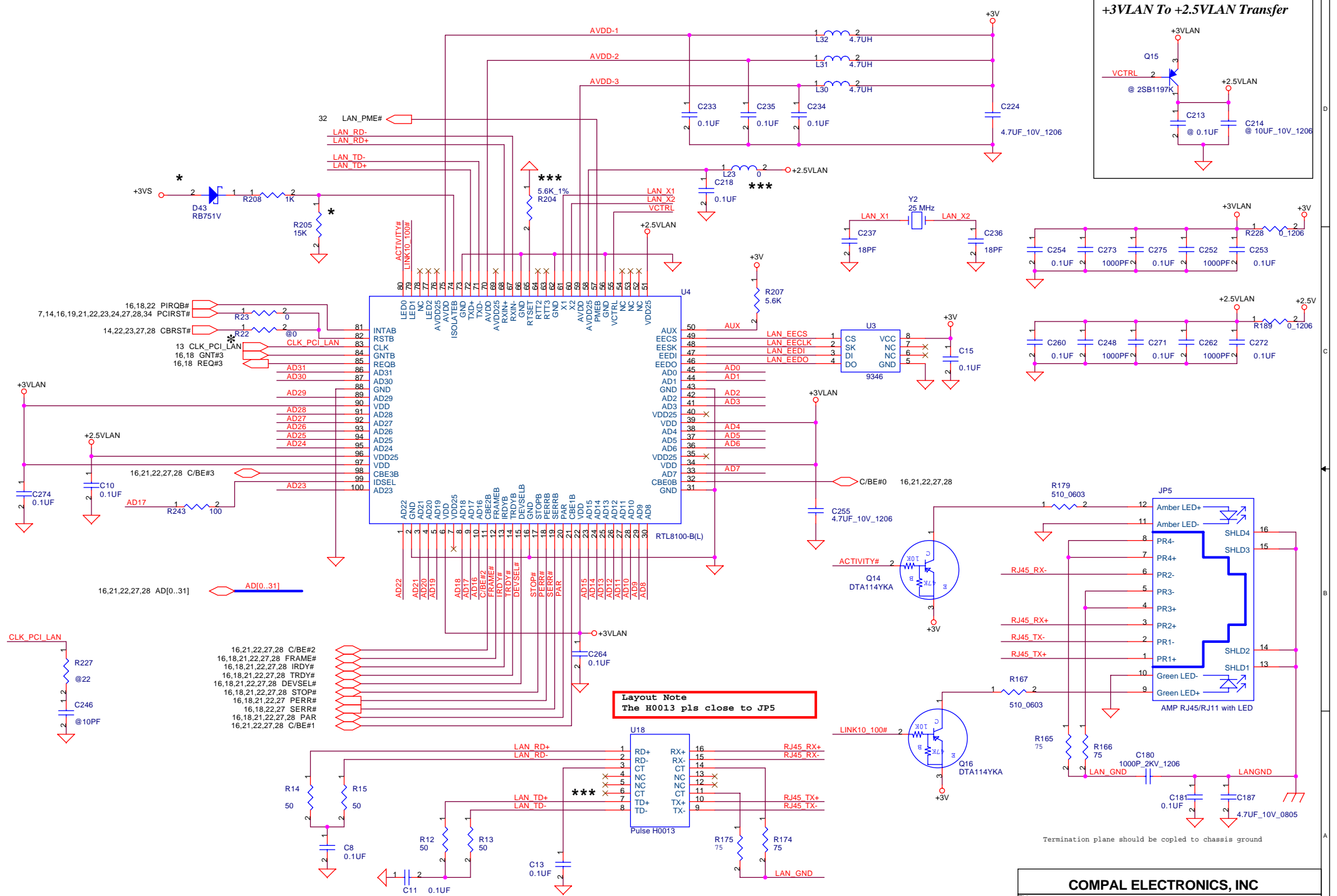
SI3456DV: N CHANNEL
 VGS: 4.5V, RDS: 65 mOHM
 Id(MAX): 5.1A
 VGS,+20V



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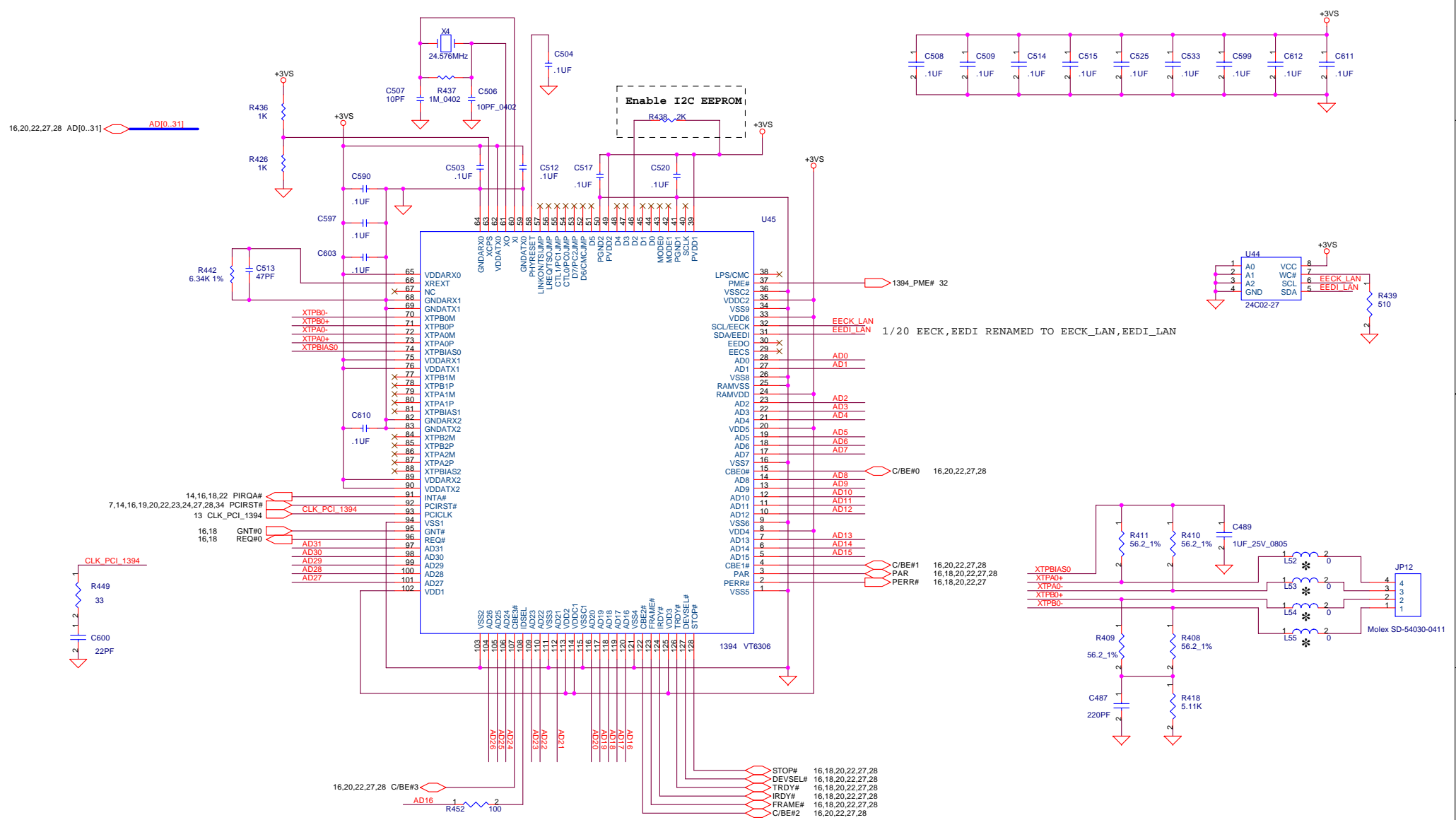
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Layout Note
The H0013 pls close to JP5

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@X3

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CardBus Controller OZ6933T (uBGA)

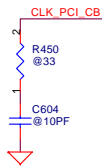
S1_IOWR# S1_IOWR# 23
S1_IORD# S1_IORD# 23
S1_OE# S1_OE# 23
S1_CE2# S1_CE2# 23

16,20,21,27,28 AD[0..31]

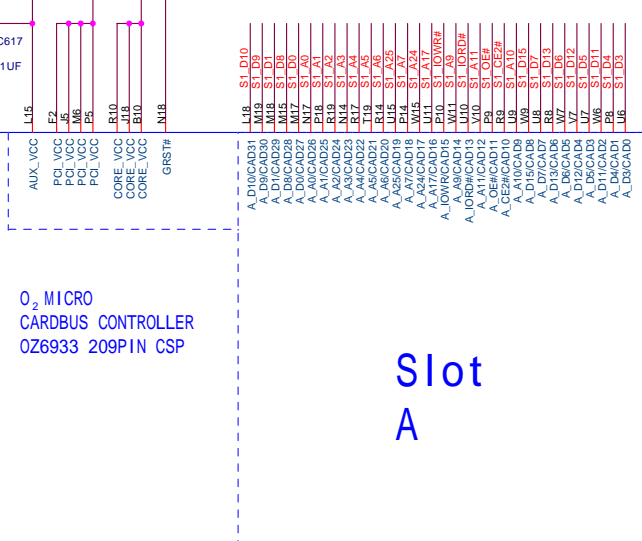
16,20,21,27,28 C/BE#3
16,20,21,27,28 C/BE#2
16,20,21,27,28 C/BE#1
16,20,21,27,28 C/BE#0

13 CLK_PCI_CB
16,18,20,21,27,28 DEVSEL#
16,18,20,21,27,28 FRAME#
16,18,20,21,27,28 IRDY#
16,18,20,21,27,28 TRDY#
16,18,20,21,27,28 STOP#
16,18,20,21,27,28 PAR
16,18,20,21,27 PERR#
16,18,20,27 SERR#
16,18 REQ#2
16,18 GNT#2
14,16,18,21 PIRQA#
16,18,20 PIRQB#
16,18 PLOCK#
7,14,16,19,20,21,23,24,27,28,34 PCIRST#

32 PCM_PME#
16,18,24,27,28,32 PM_CLKRUN#
28 PCM_RI#
31 PCM_SPK#
33 PCM1_LED
33 PCM2_LED
16,18,24,32 INT_SERIRQ



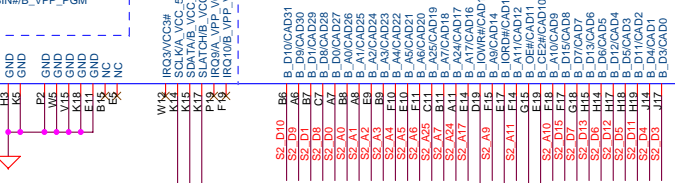
CardBus-OZ6933T-1



PCI

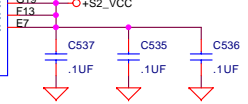
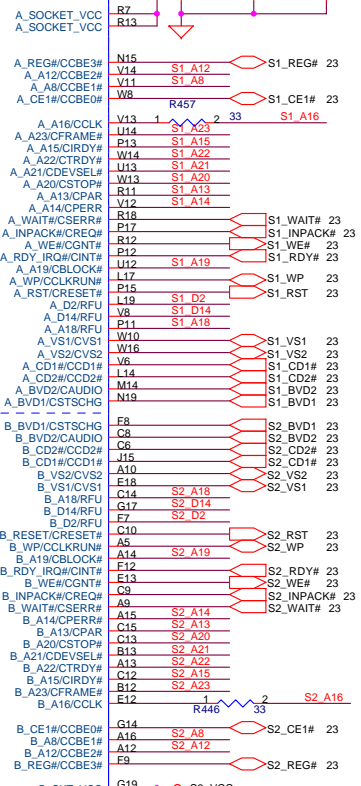
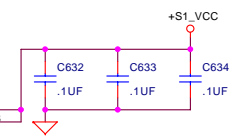
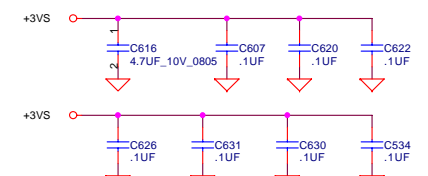
Slot
A

Slot
B



SLATCH 23
SLDATA 23
RTCLK 16,23,28

S2_CE2# S2_CE2# 23
S2_OE# S2_OE# 23
S2_IORD# S2_IORD# 23
S2_IOWR# S2_IOWR# 23



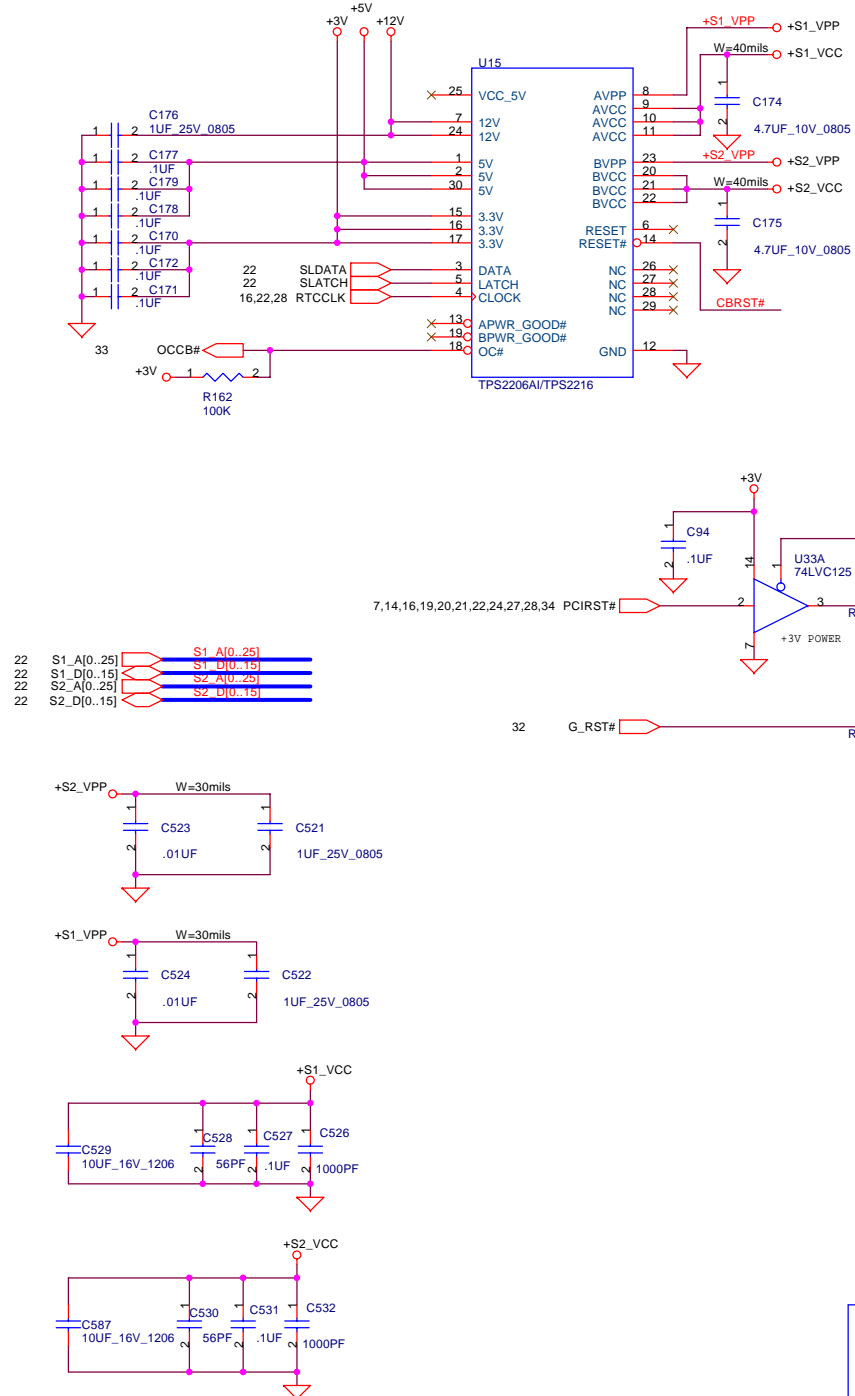
S1_A[0..25] S1_A[0..25] 23
S1_D[0..15] S1_D[0..15] 23

S2_A[0..25] S2_A[0..25] 23
S2_D[0..15] S2_D[0..15] 23

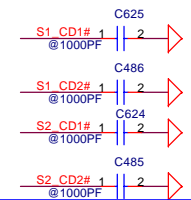
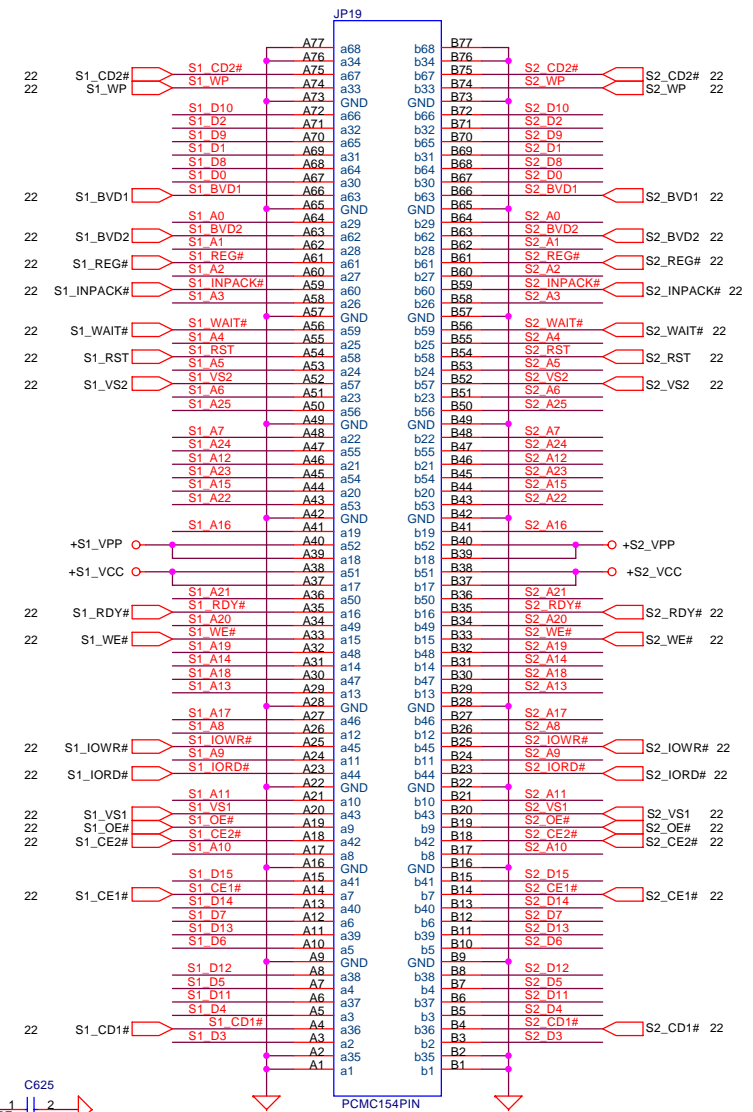
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PCMCIA POWER CTRL.



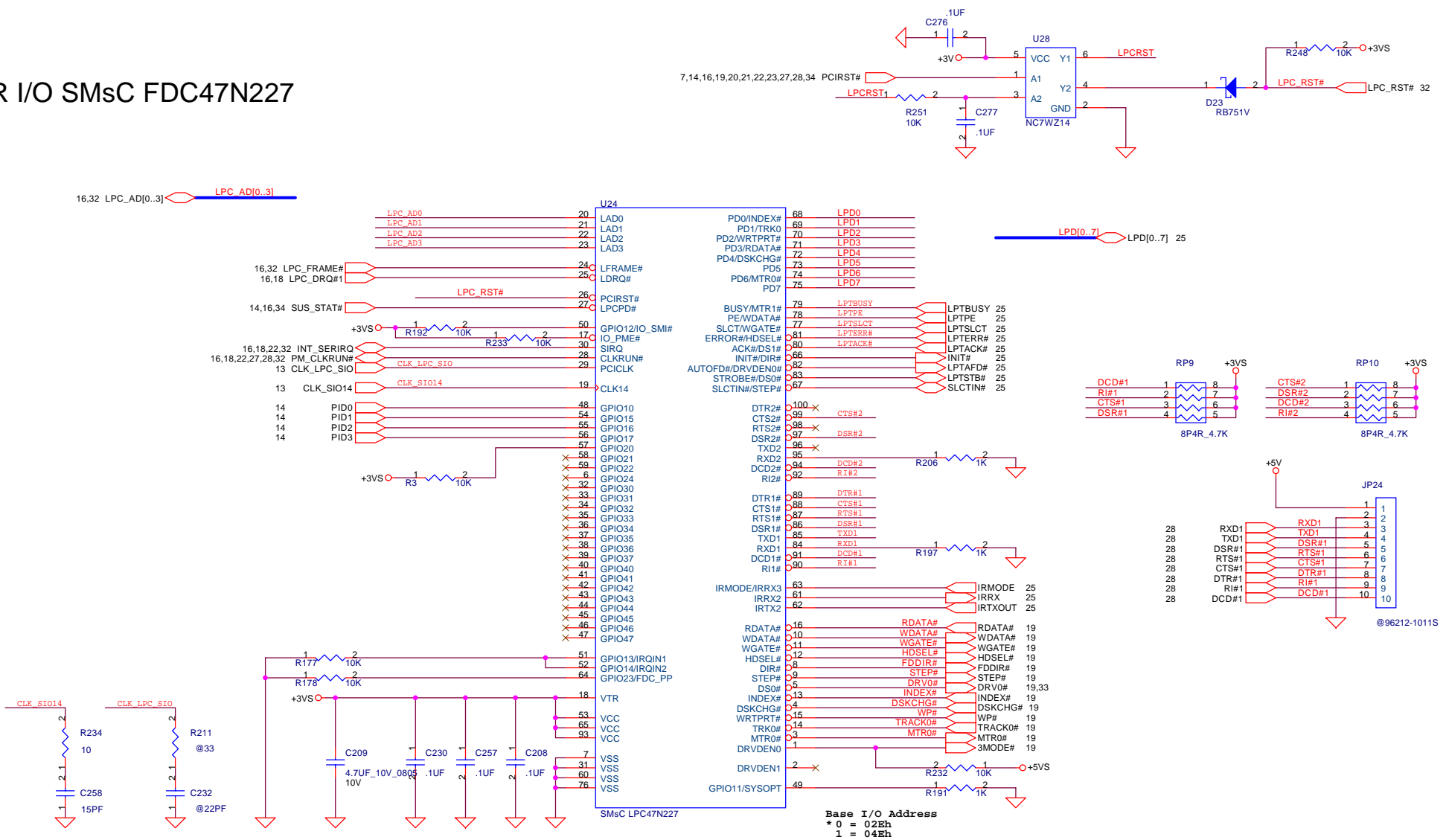
CARDBUS SOCKET



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SUPER I/O SMsC FDC47N227



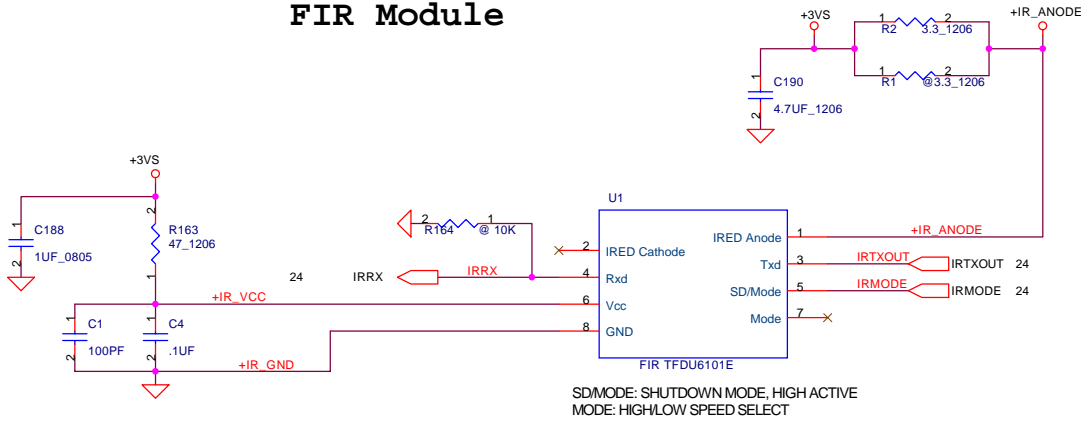
COMPAL ELECTRONICS, INC

SCHMATIC, M/B LA-1331

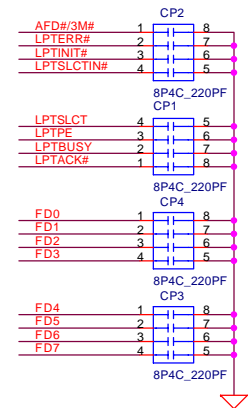
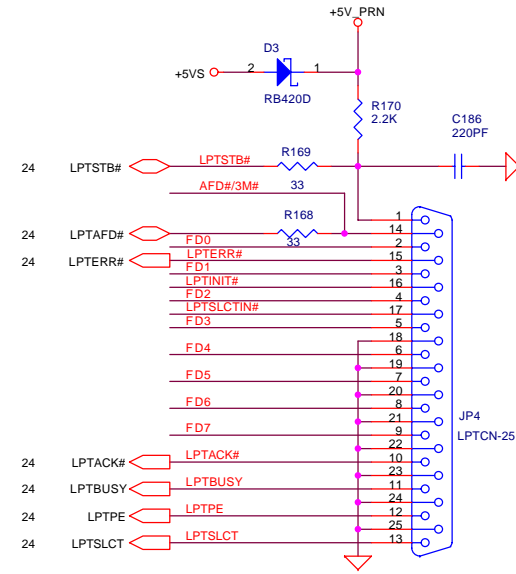
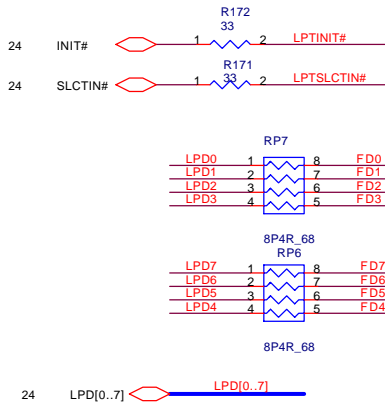
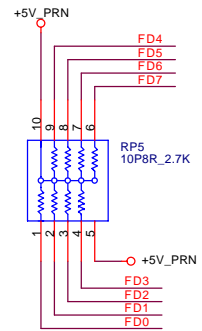
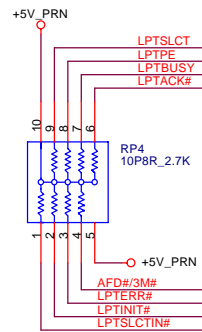
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FIR Module



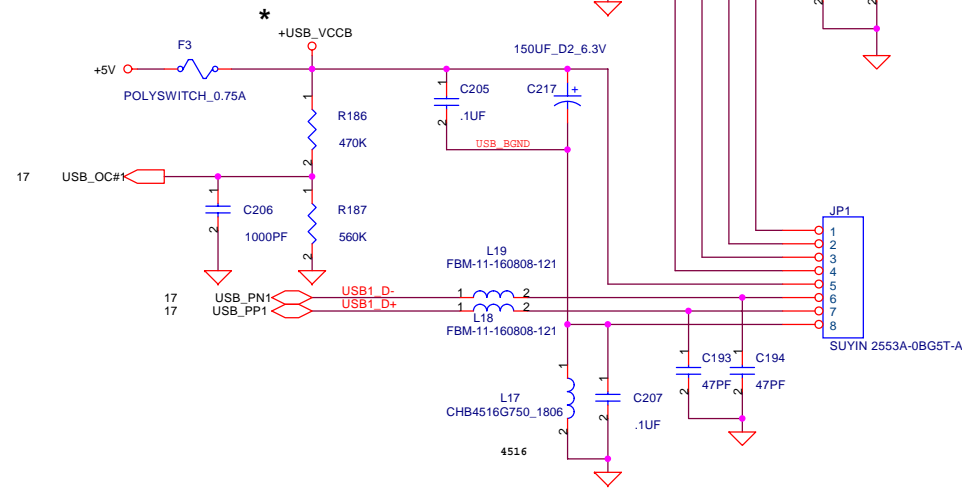
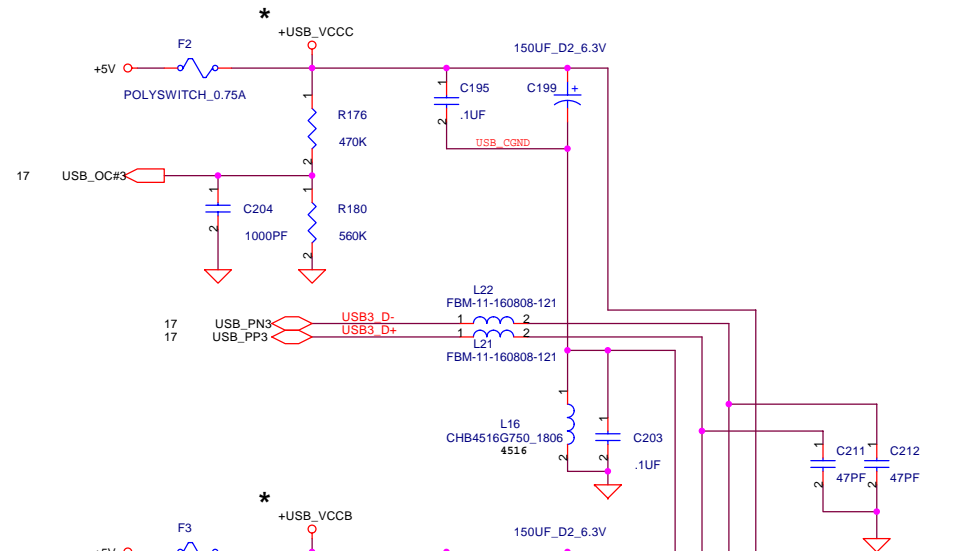
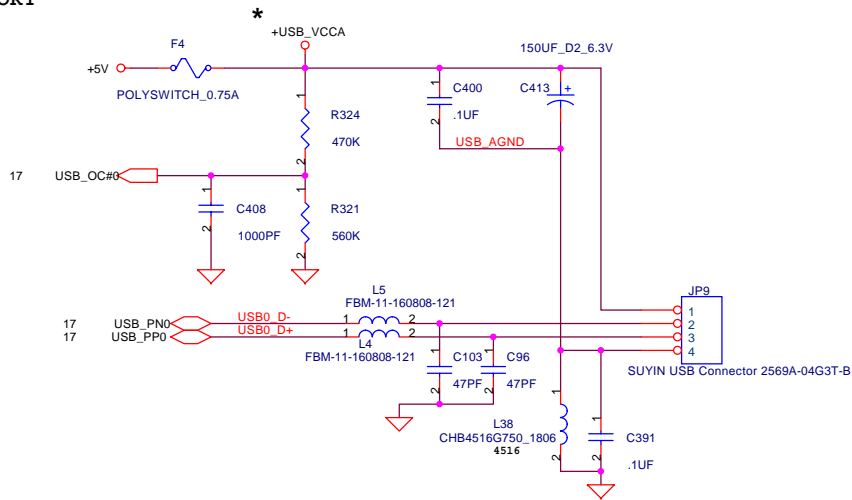
PARALLEL PORT



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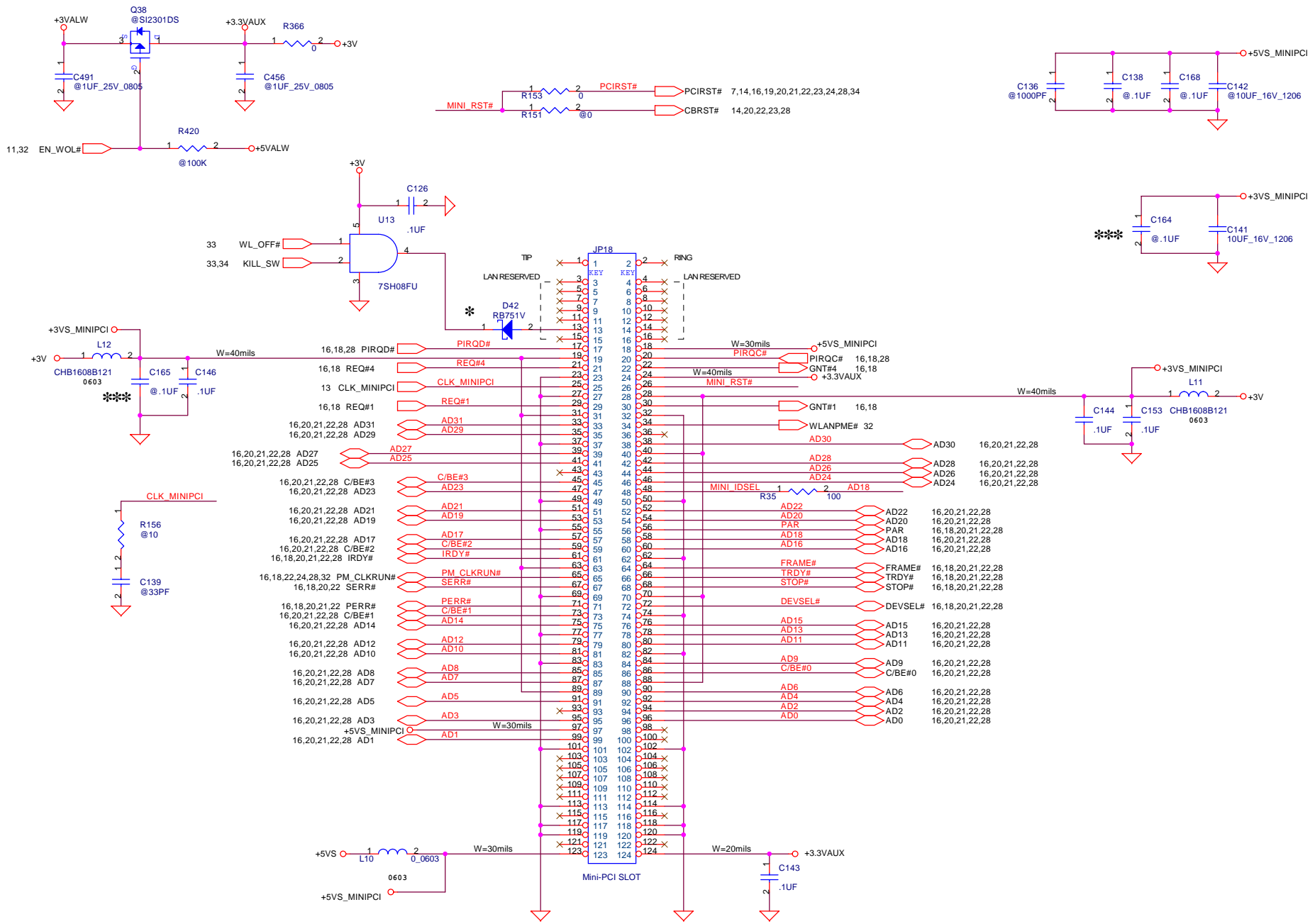
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USB PORT



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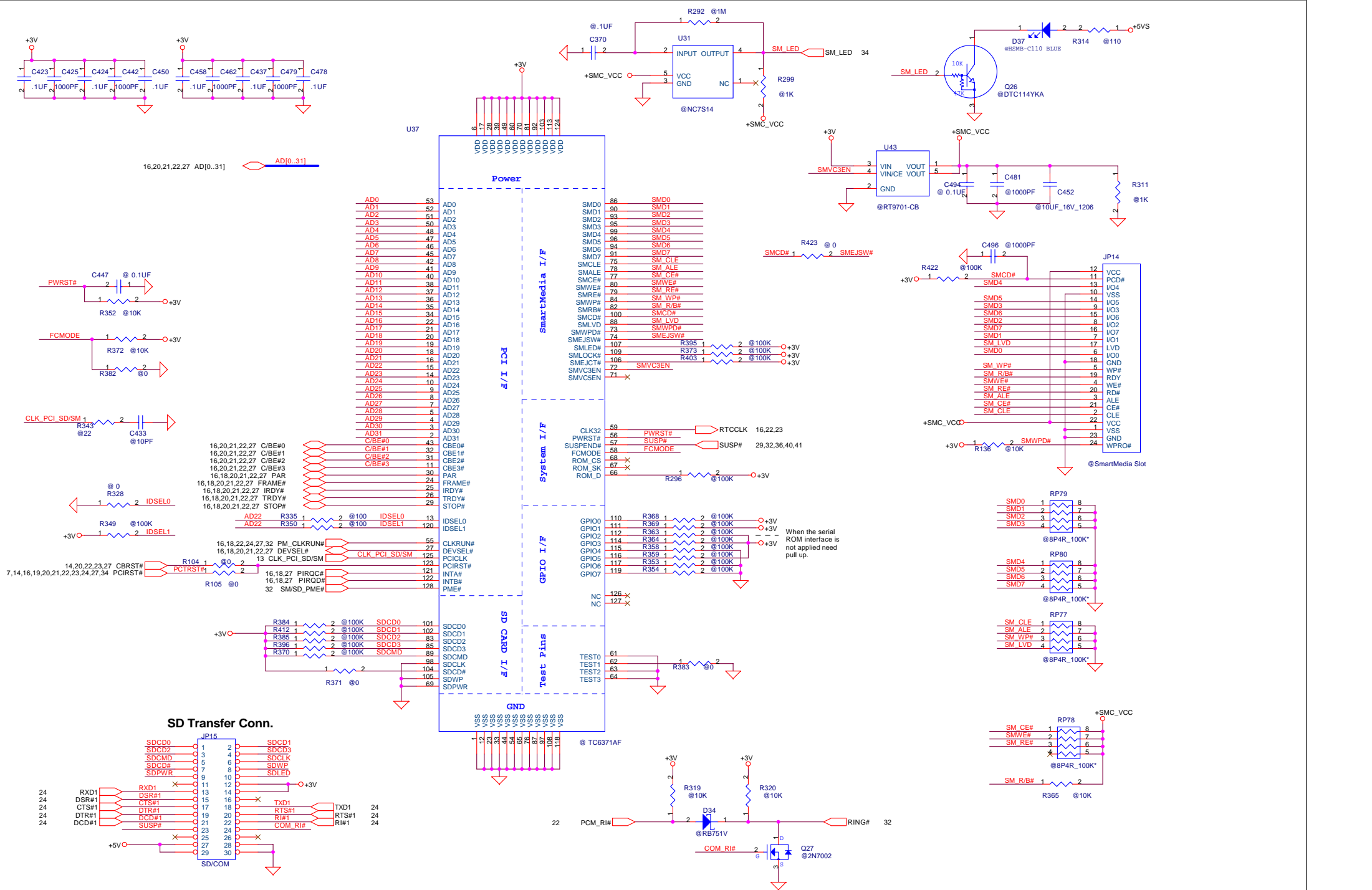


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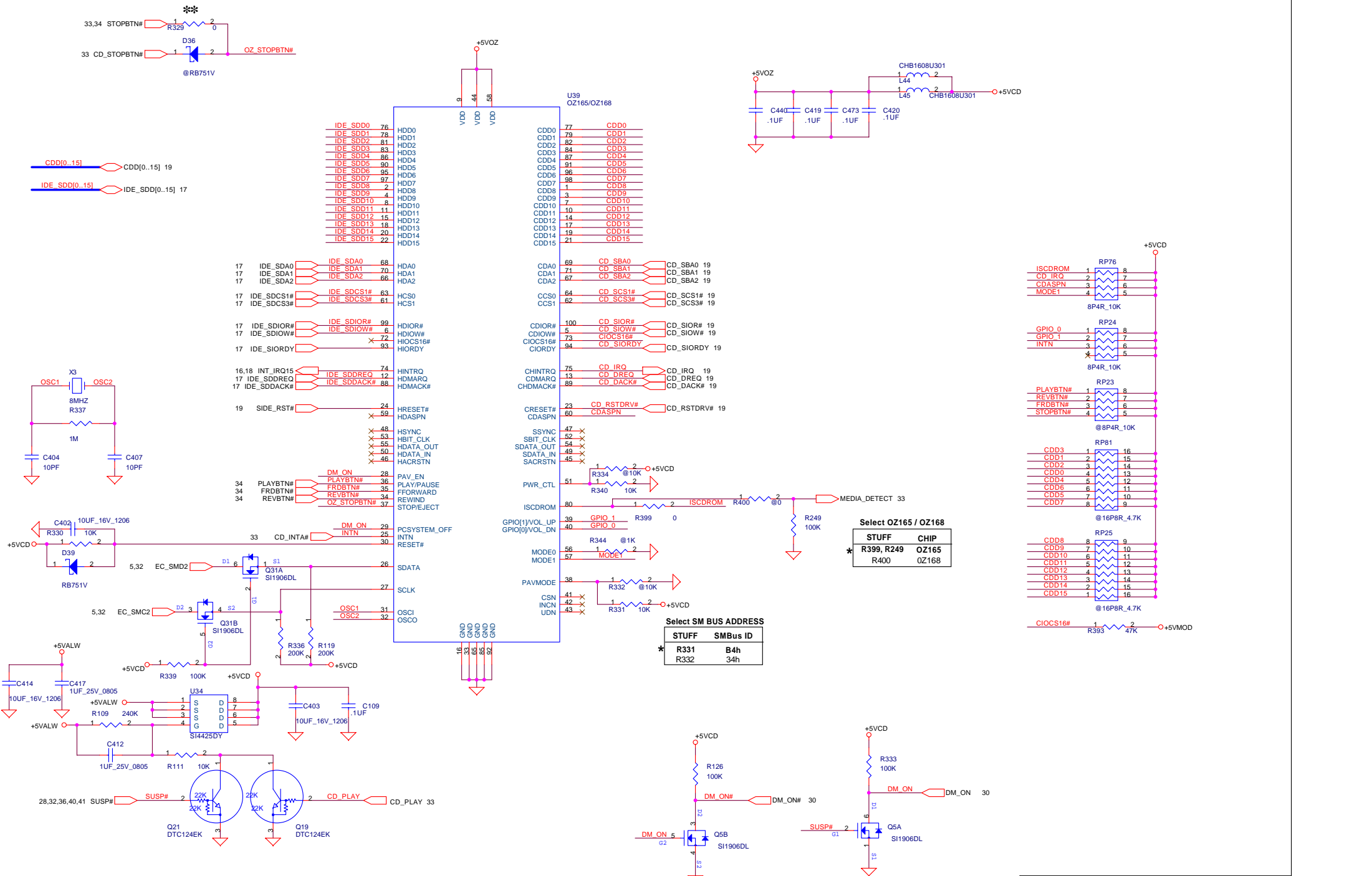
COMPAL ELECTRONICS, INC

SCHEMATIC, M/B LA-1331

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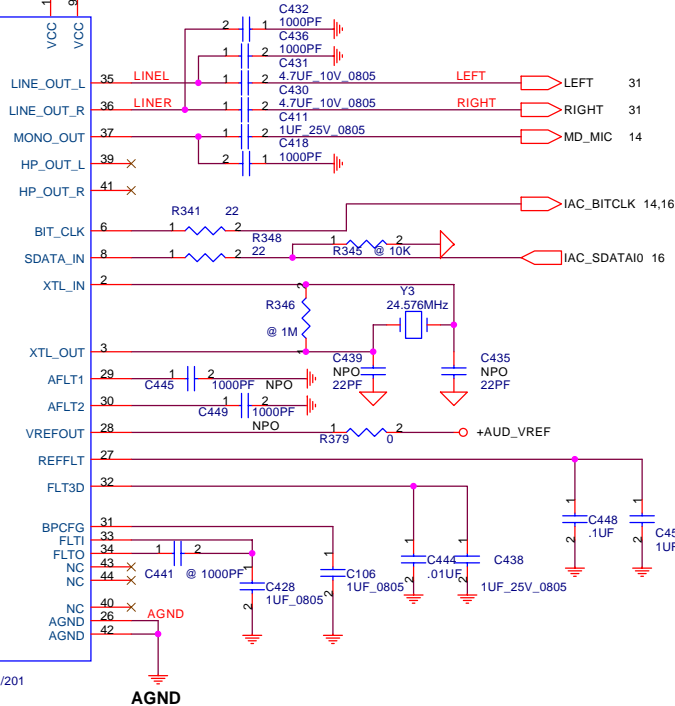
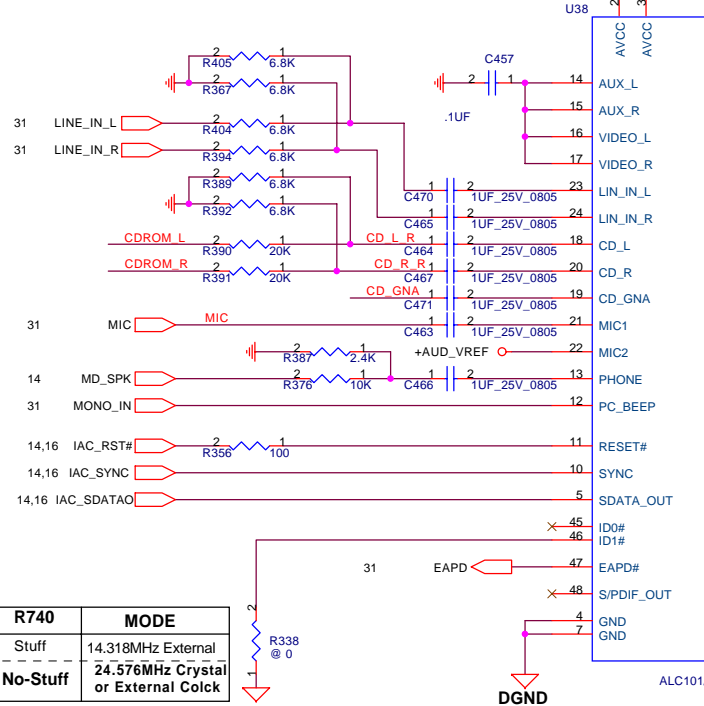
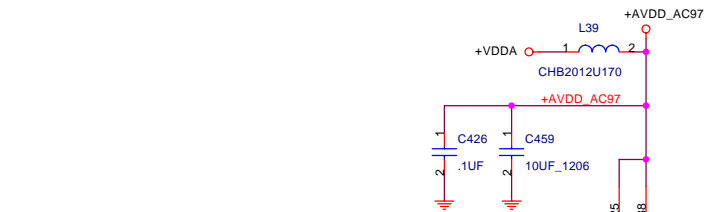
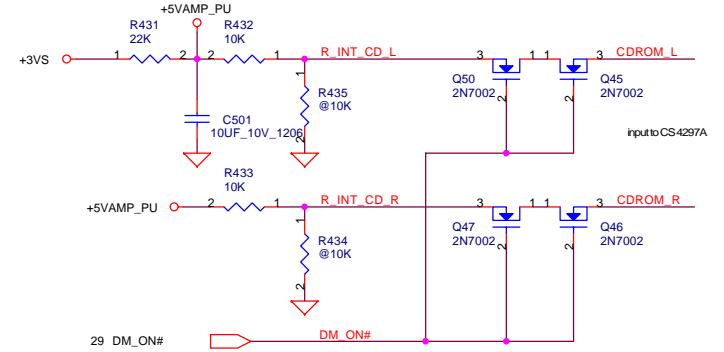
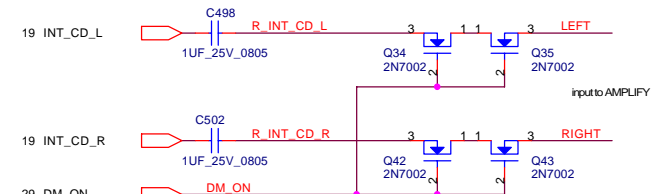
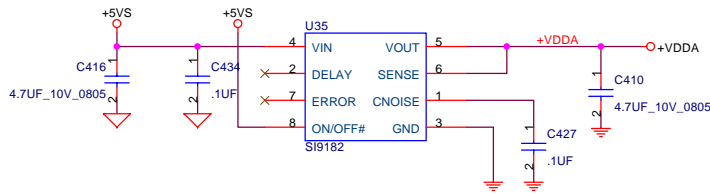


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IDE_SDD2	81	HDD2	IDE_SDD2	81	CDD2
IDE_SDD3	83	HDD3	IDE_SDD3	83	CDD3
IDE_SDD4	86	HDD4	IDE_SDD4	86	CDD4
IDE_SDD5	90	HDD5	IDE_SDD5	90	CDD5
IDE_SDD6	95	HDD6	IDE_SDD6	95	CDD6
IDE_SDD7	97	HDD7	IDE_SDD7	97	CDD7
IDE_SDD8	2	HDD8	IDE_SDD8	2	CDD8
IDE_SDD9	4	HDD9	IDE_SDD9	4	CDD9
IDE_SDD10	4	HDD9	IDE_SDD10	4	CDD10
IDE_SDD11	11	HDD10	IDE_SDD11	11	CDD11
IDE_SDD12	15	HDD12	IDE_SDD12	15	CDD12
IDE_SDD13	18	HDD13	IDE_SDD13	18	CDD13
IDE_SDD14	20	HDD14	IDE_SDD14	20	CDD14
IDE_SDD15	22	HDD15	IDE_SDD15	22	CDD15
IDE_SDA0	68	HDA0	IDE_SDA0	68	CDA0
IDE_SDA1	70	HDA1	IDE_SDA1	70	CDA1
IDE_SDA2	66	HDA2	IDE_SDA2	66	CDA2
IDE_SDCS1#	63	HCS0	IDE_SDCS1#	63	CCS0
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IDE_SDIOR#	99	HDIOR#	IDE_SDIOR#	99	CDIOR#
IDE_SDIOW#	6	HDIOW#	IDE_SDIOW#	6	CDIOW#
IDE_SDIORDY	93	HIOCS16#	IDE_SDIORDY	93	CIOWCS16#
IDE_SDIORDY	93	HIORDY	IDE_SDIORDY	93	CIORDY
IDE_SDDRQ	74	HINTRQ	IDE_SDDRQ	74	CDIRO
IDE_SDDREQ	12	HDMARQ	IDE_SDDREQ	12	CD_DREQ
IDE_SDDACK#	88	HDMACK#	IDE_SDDACK#	88	CD_DACK#
SIDE_RST#	24	HRESET#	SIDE_RST#	24	CD_RSTDRV#
	59	HDASPEN		59	CDASPEN
	48	HSYNC		48	SSYNC
	53	HBIT_CLK		53	SBIT_CLK
	55	HDATA_OUT		55	S_DATA_OUT
	50	HDATA_IN		50	S_DATA_IN
	46	HACRSTN		46	SACRSTN
PLAYBTN#	28	PAV_EN	PLAYBTN#	28	PAVMODE
FRDBTN#	35	PLAY/PAUSE	FRDBTN#	35	MODE0
REVBTN#	34	FFORWARD	REVBTN#	34	MODE1
REVBTN#	34	REWIND	REVBTN#	34	MODE1
OZ_STOPBTN#	37	STOP/EJECT	OZ_STOPBTN#	37	MODE1
DM_ON	29	PCSYSTEM_OFF	DM_ON	29	DM_ON#
INTN	25	RESET#	INTN	25	DM_ON#
	30	RESET#		30	DM_ON#
EC_SMD2	26	SDATA	EC_SMD2	26	DM_ON#
	27	SCLK		27	DM_ON#
EC_SMC2	3	OSCI	EC_SMC2	3	DM_ON#
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EC_SMC2	3		EC_SMC2	3	

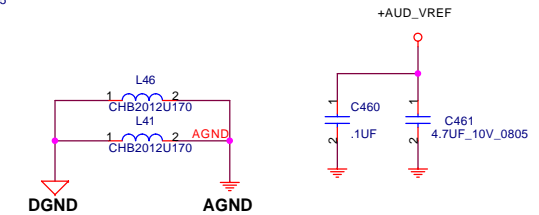
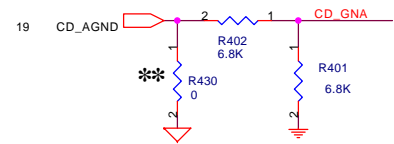
Select OZ165 / OZ168	
STUFF	CHIP
R399, R249	OZ165
R400	OZ168

Select SM BUS ADDRESS	
STUFF	SMBus ID
R331	B4h
R332	34h

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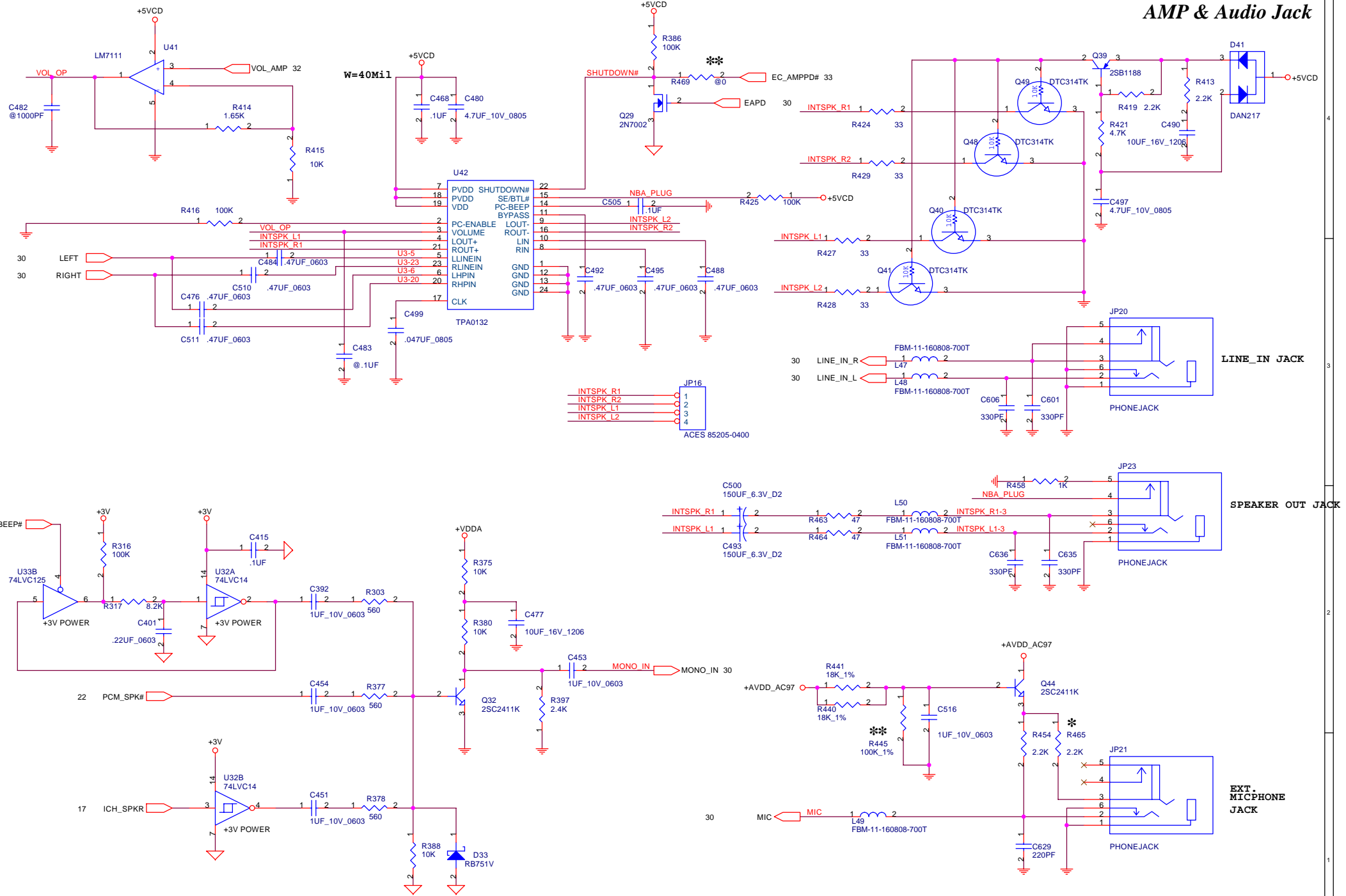
R740	MODE
Stuff	14.318MHz External
No-Stuff	24.576MHz Crystal or External Colck



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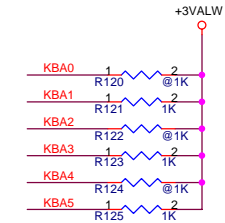
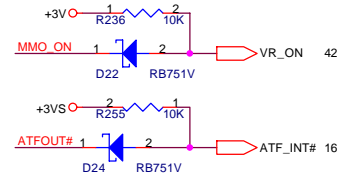
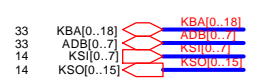
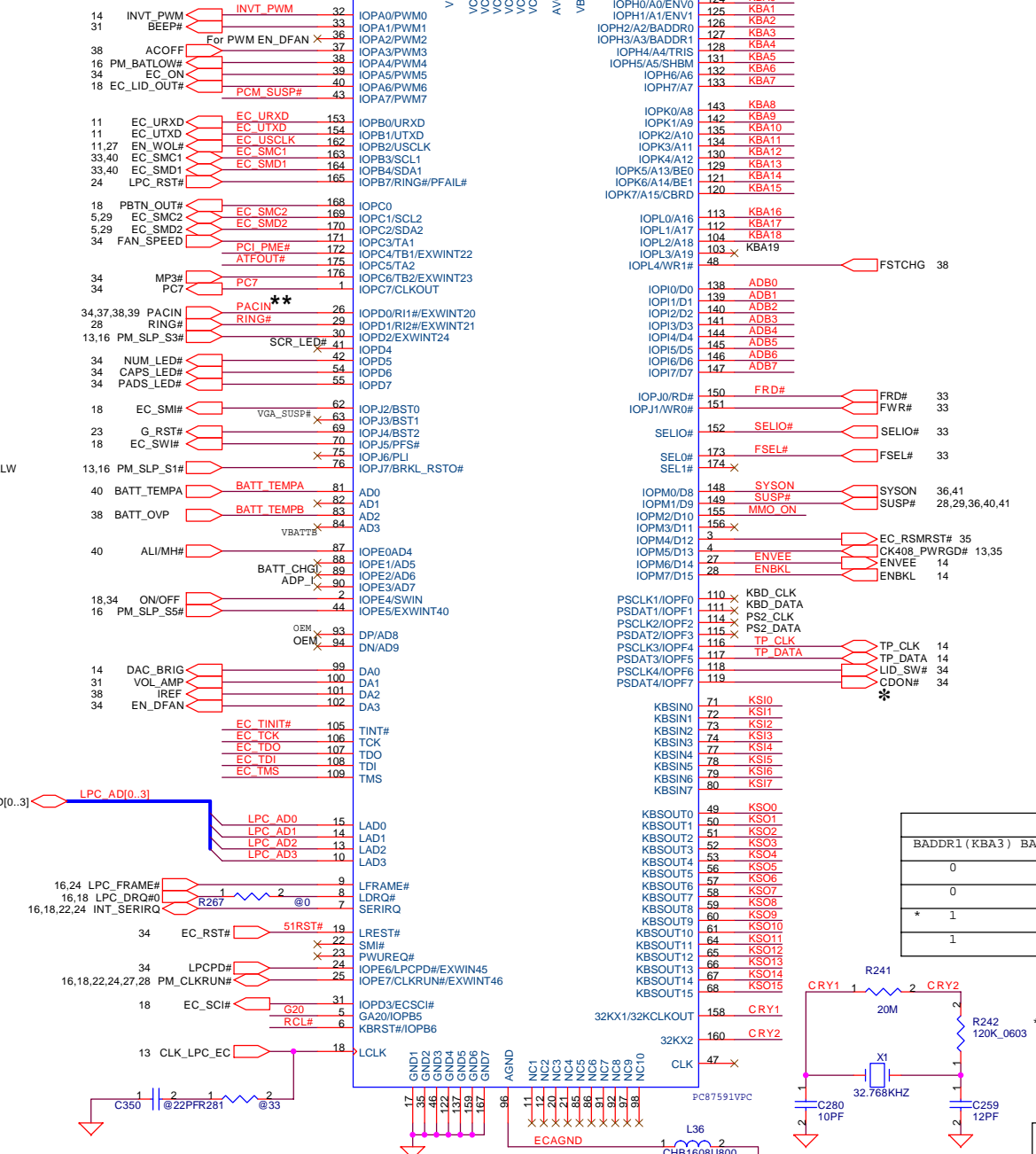
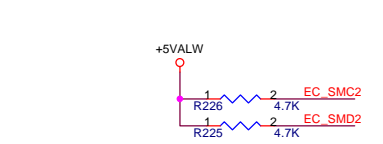
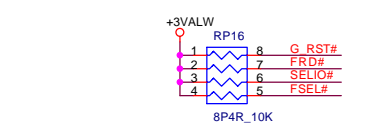
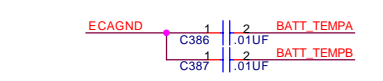
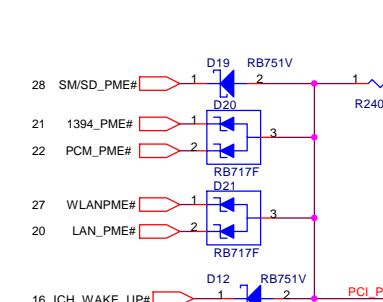
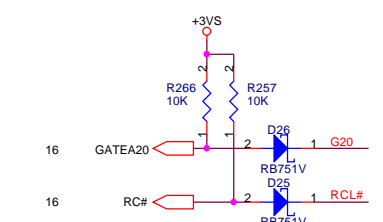
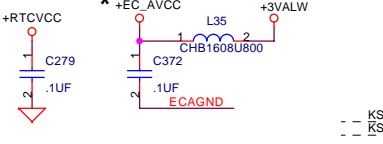
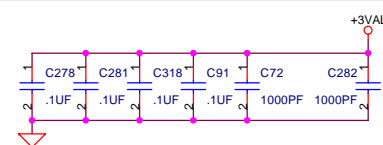
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Compal Electronics, Inc.			
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AMP & Audio Jack



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		I/O Address	
BADDR1(KBA3)	BADDR0(KBA2)	Index	Data
0	0	2E	2F
0	1	4E	4F
* 1	0	(HCFGBAH, HCFGBAL)	(HCFGBAH, HCFGBAL)+1
1	1	Reserved	

	ENVO (KBA0)	ENV1 (KBA1)	TRIS (KBA4)
IRE	0	0	0
* OBD	0	1	0
DEV	1	0	0
PROG	1	1	0

SHBM(KBA5)=1: Enable shared memory with host BIOS
 TRIS(KBA4)=1: While in IRE and OBD, float all the signals for clip-on ISE use

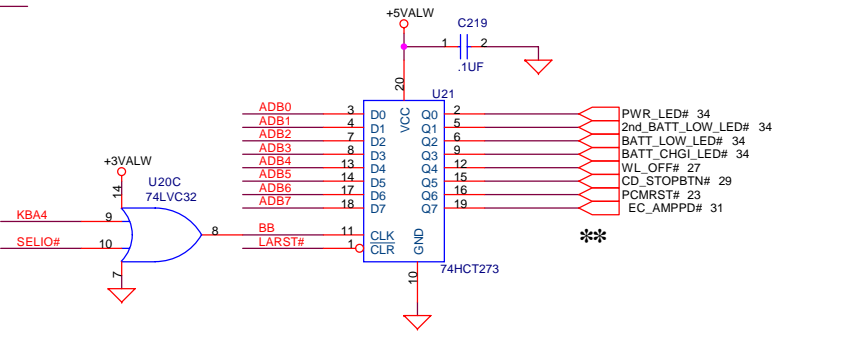
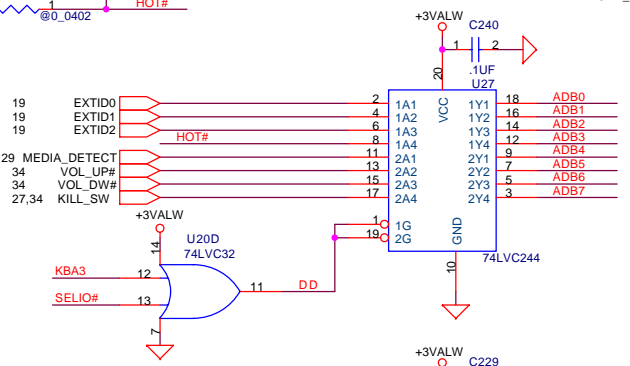
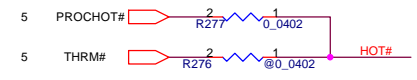
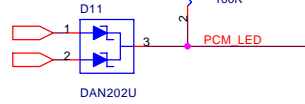
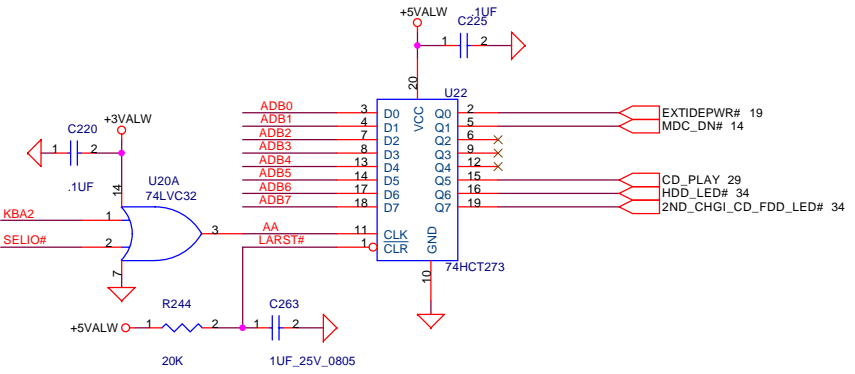
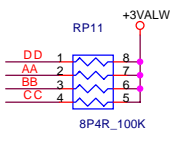
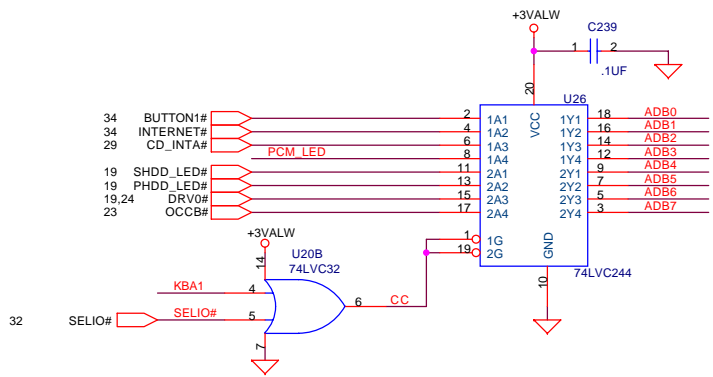
COMPAL ELECTRONICS, INC

SCHEMATIC, M/B LA-1331

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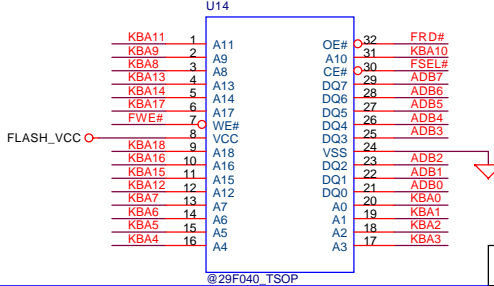
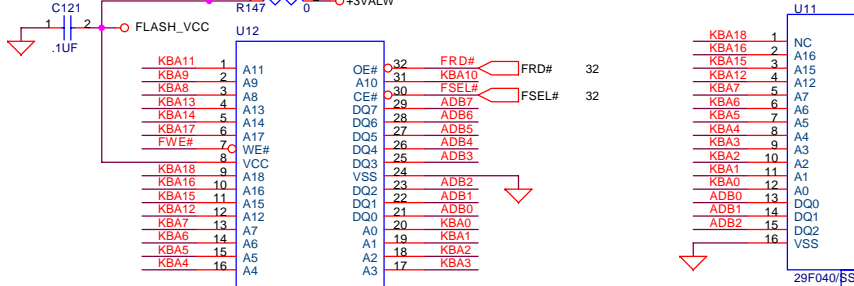
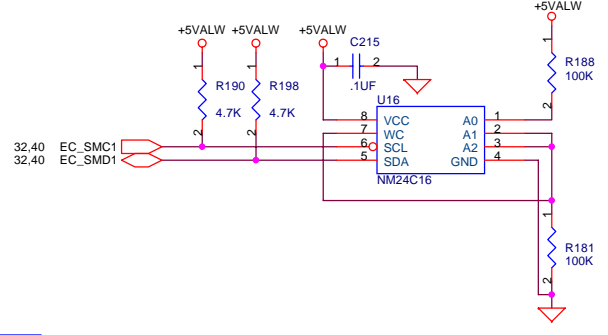
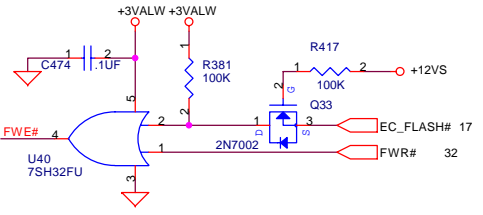
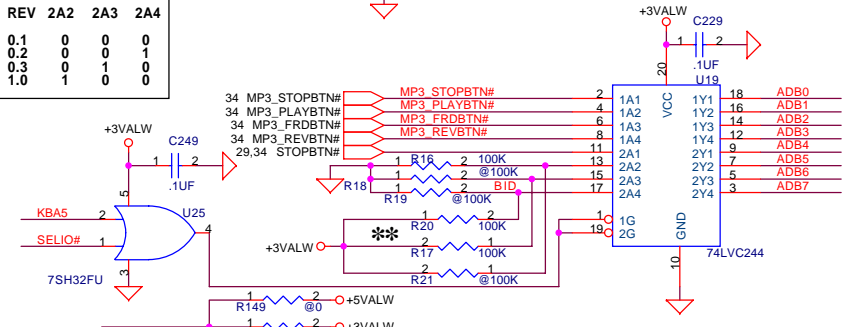
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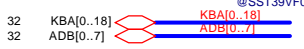


BOARD ID

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0.2	0	0	1
0.3	0	1	0
1.0	1	0	0

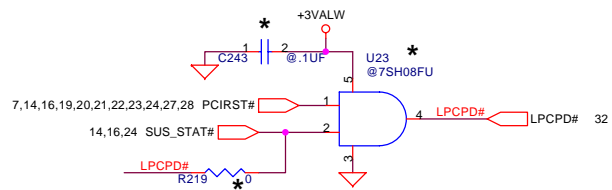
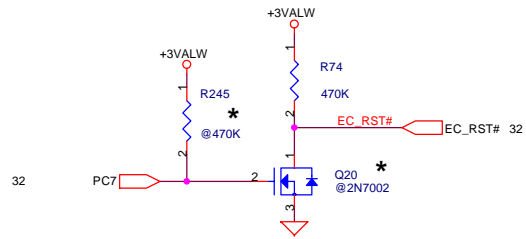


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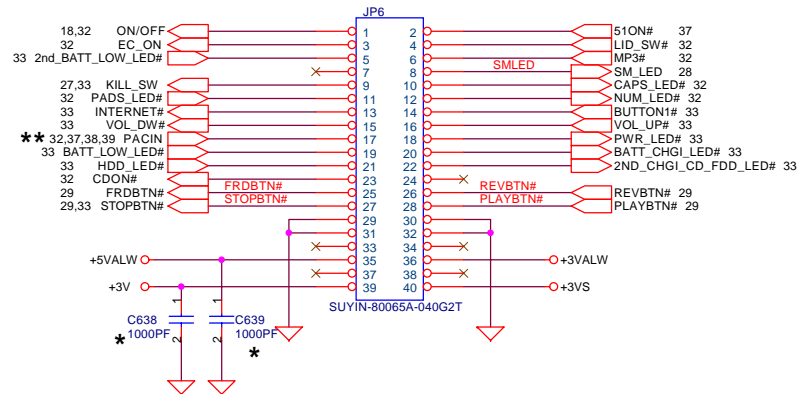
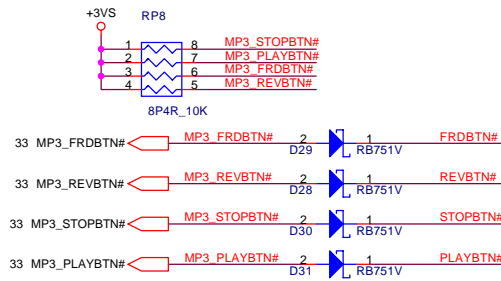


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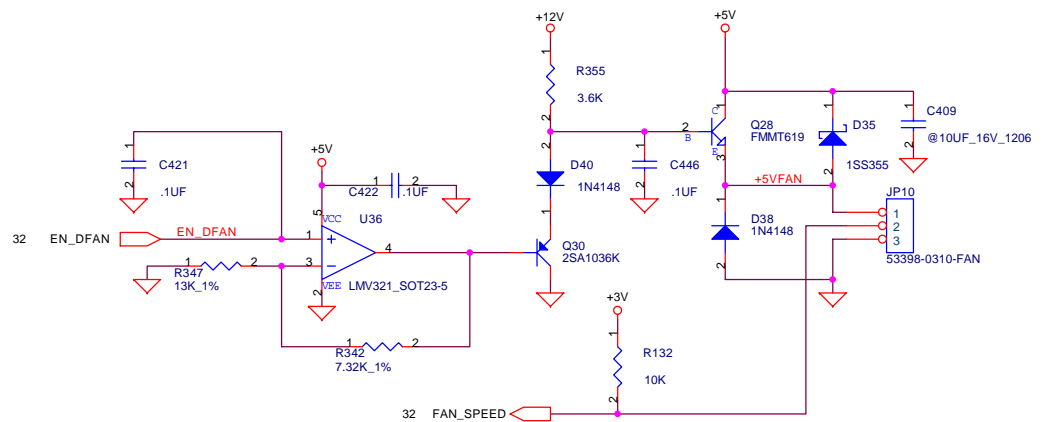
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FAN CONN.



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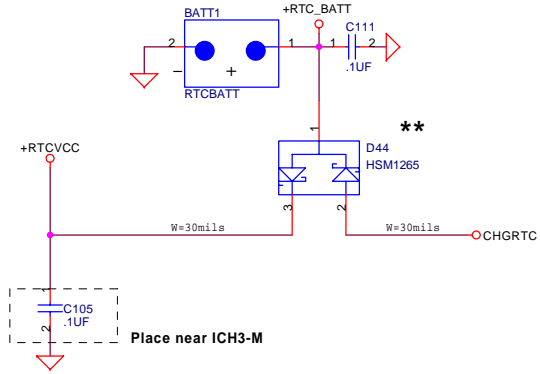
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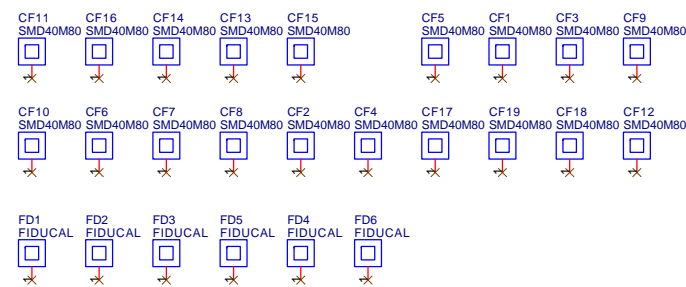
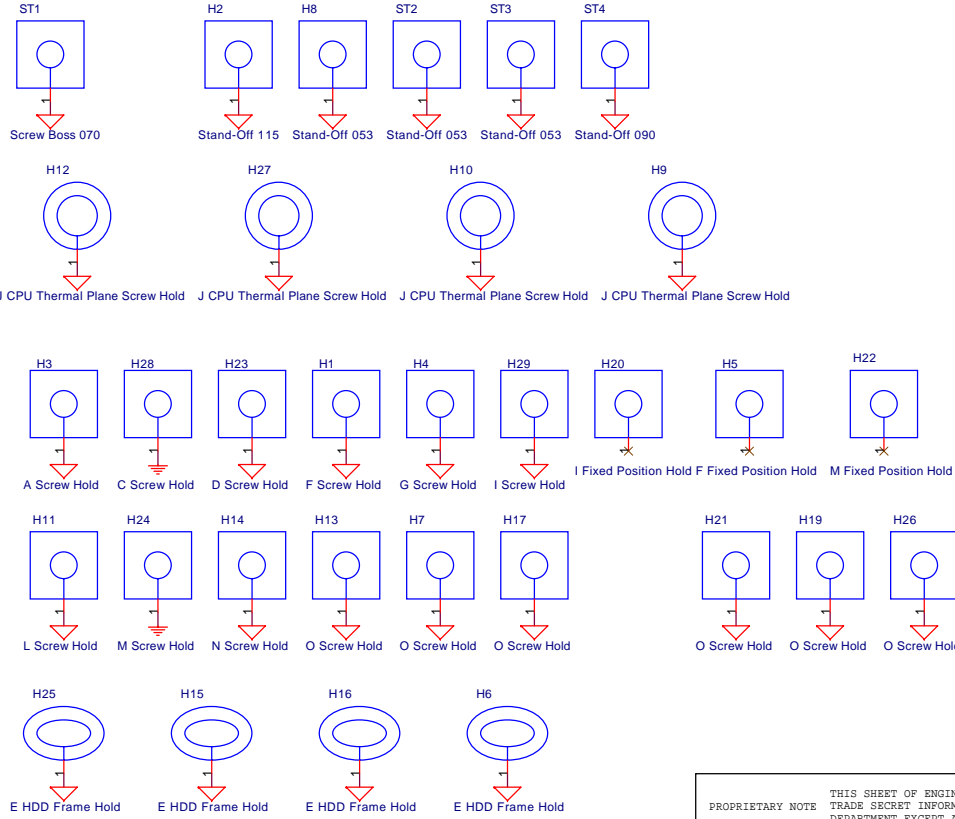
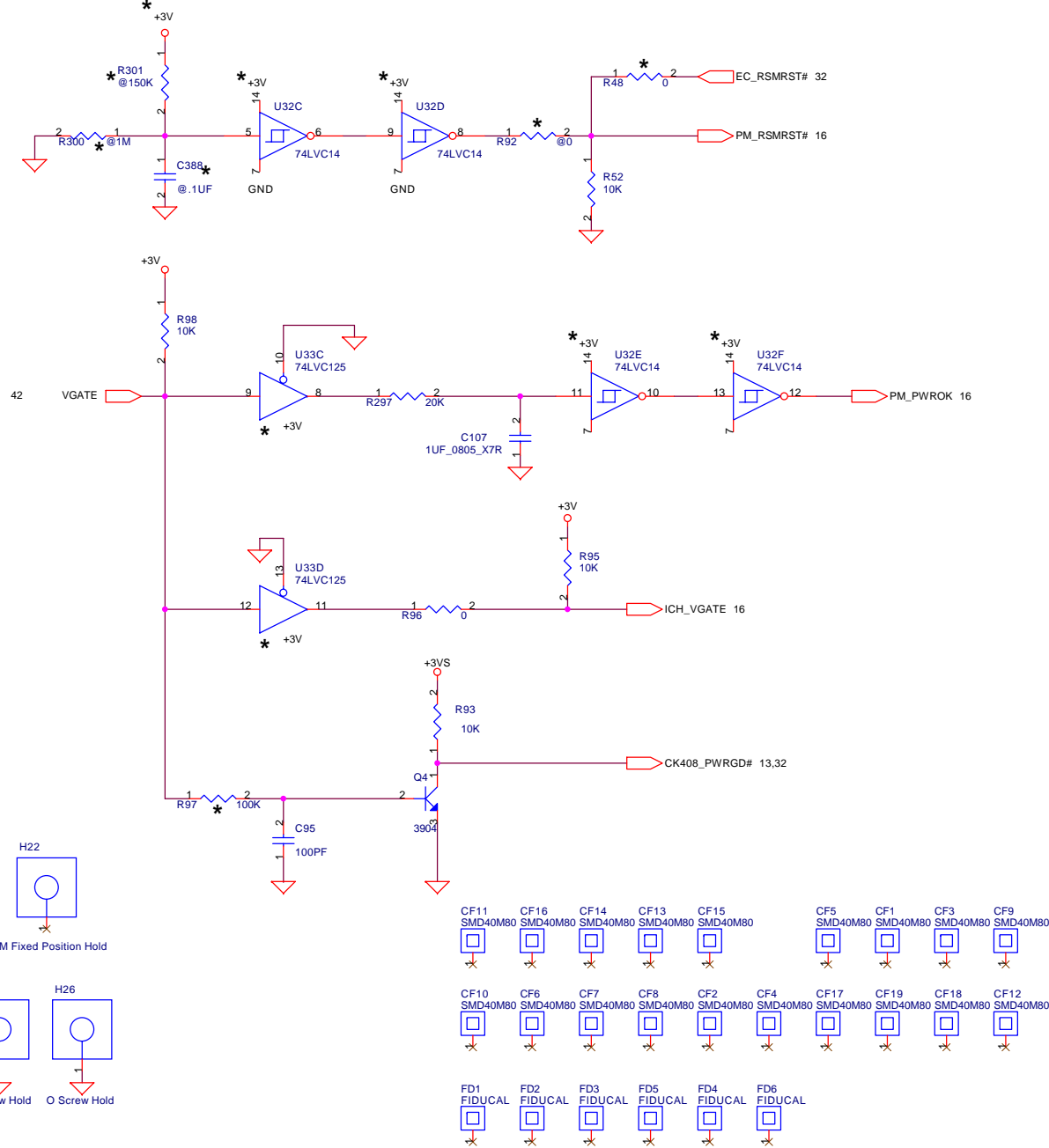
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RTC Batt. Connector



Power ON Circuit

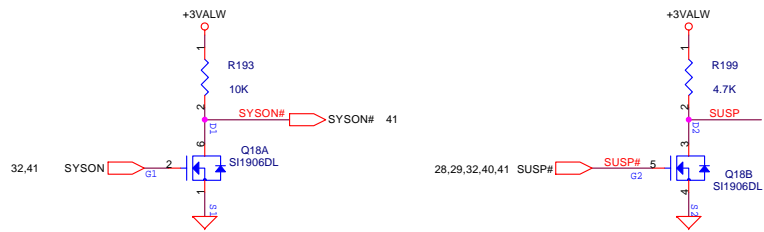
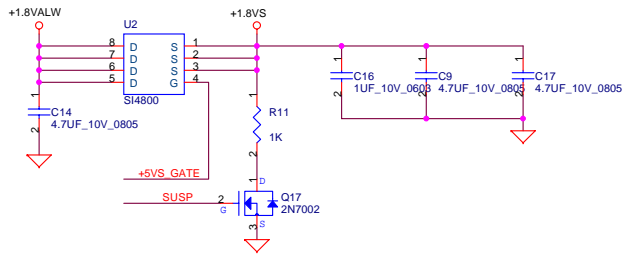


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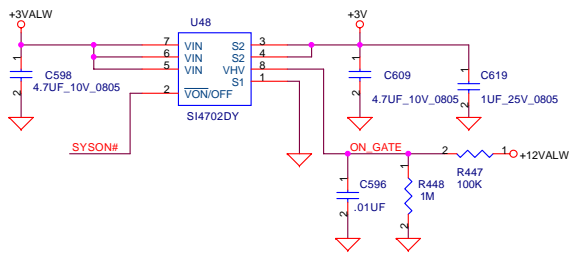
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Size	Document Number				Rev
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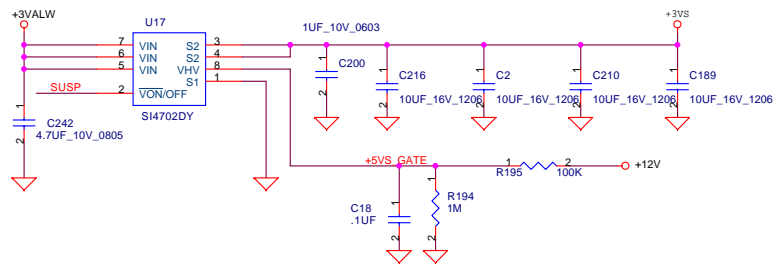
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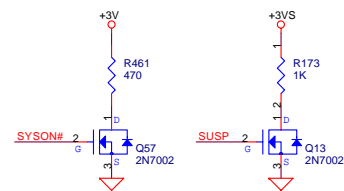
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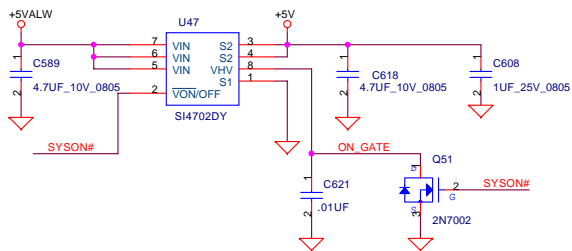
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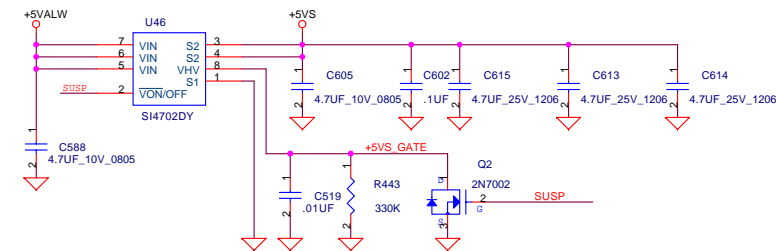
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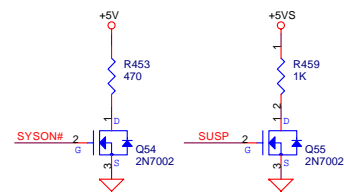
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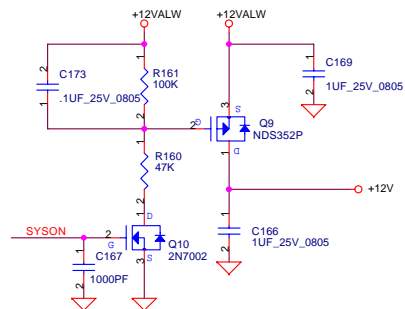
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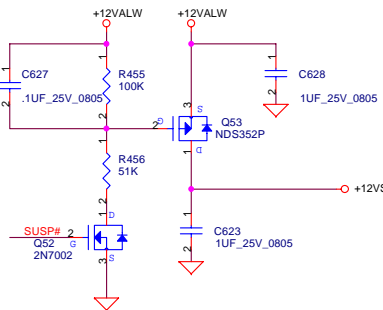
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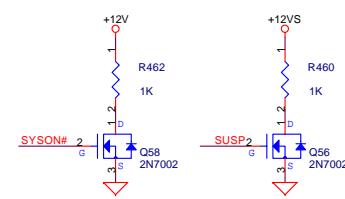
+12VALW To +12V Transfer



+12VALW To +12VS Transfer

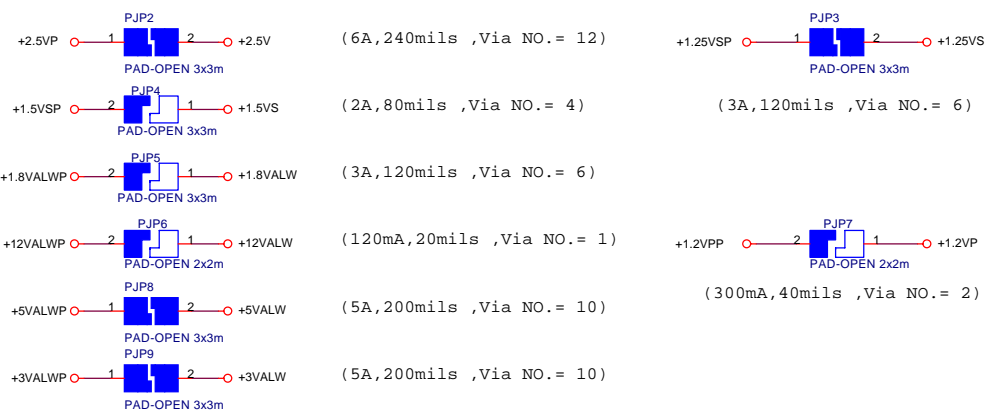
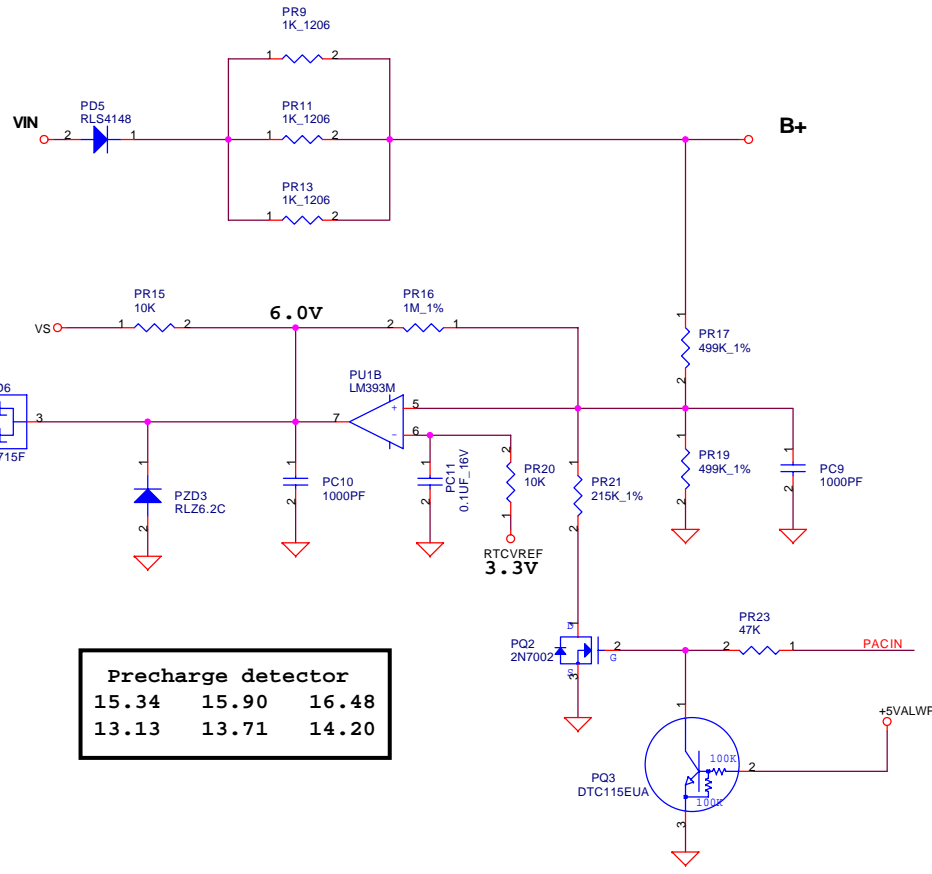
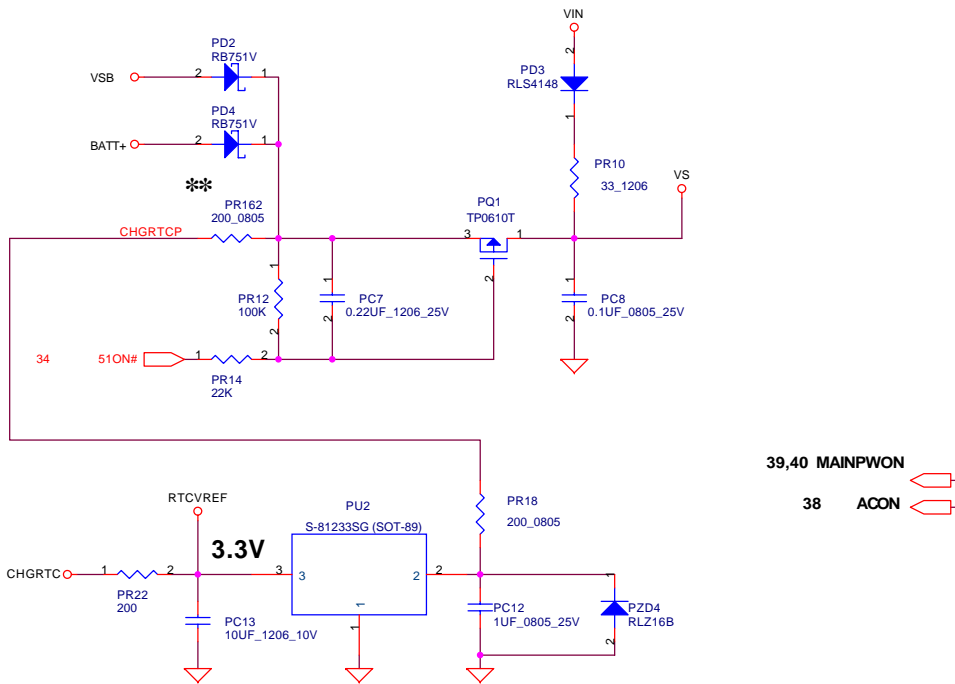
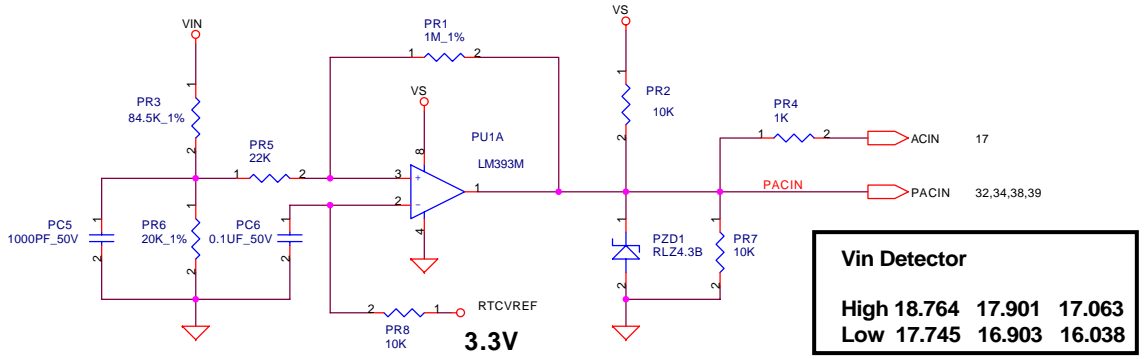
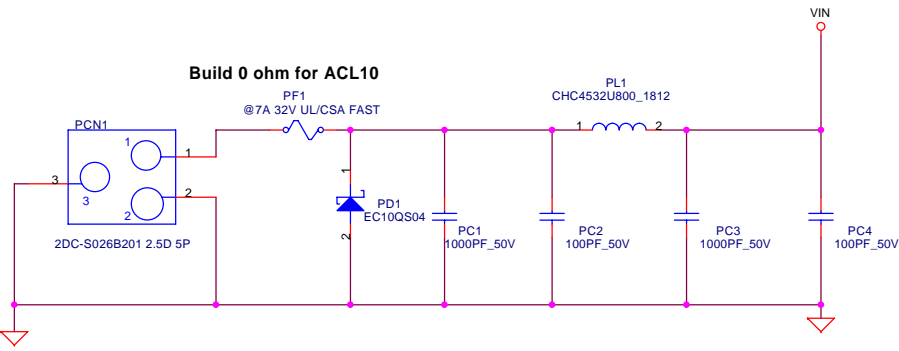


+12V & +12VS Discharge

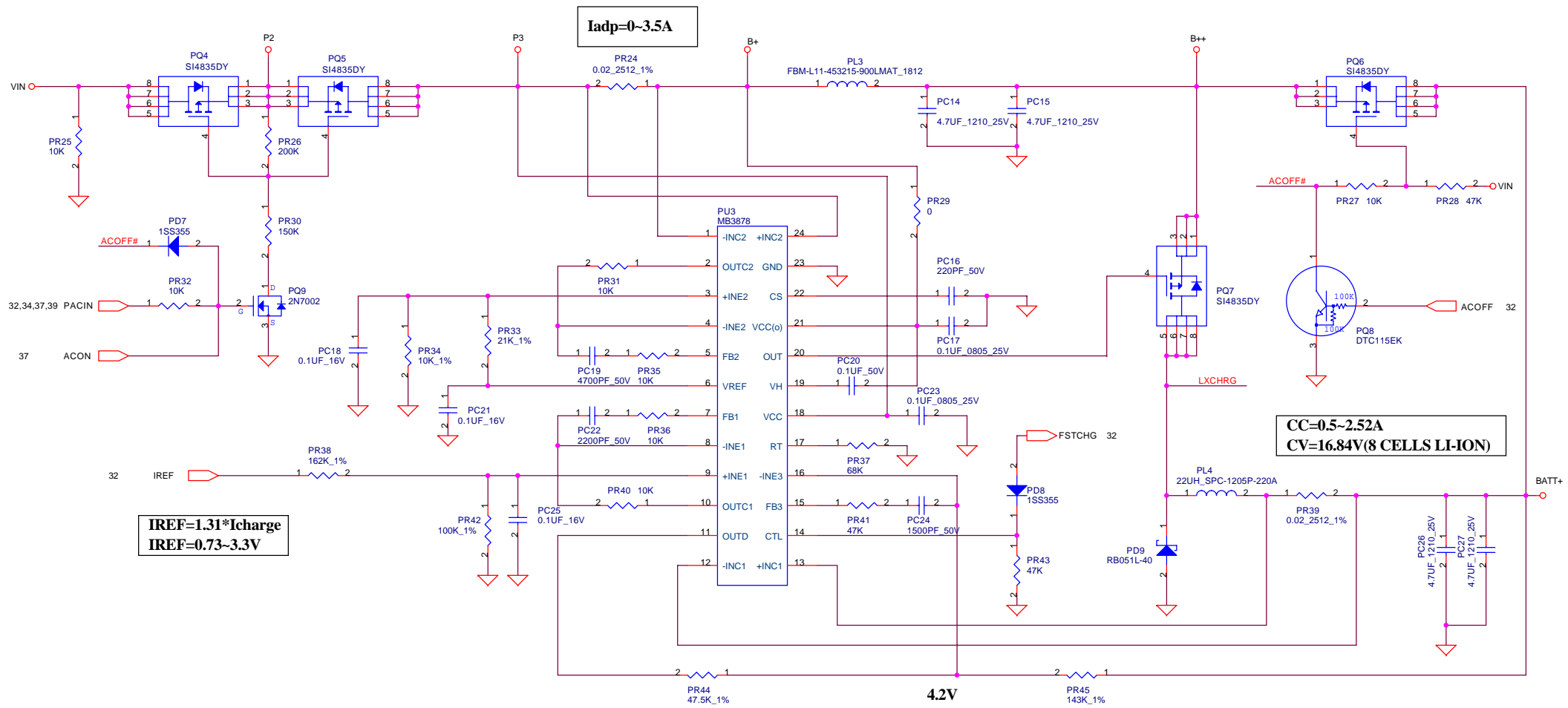


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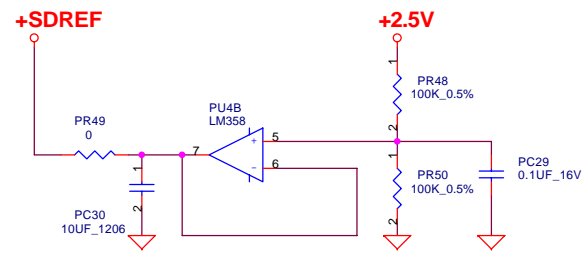
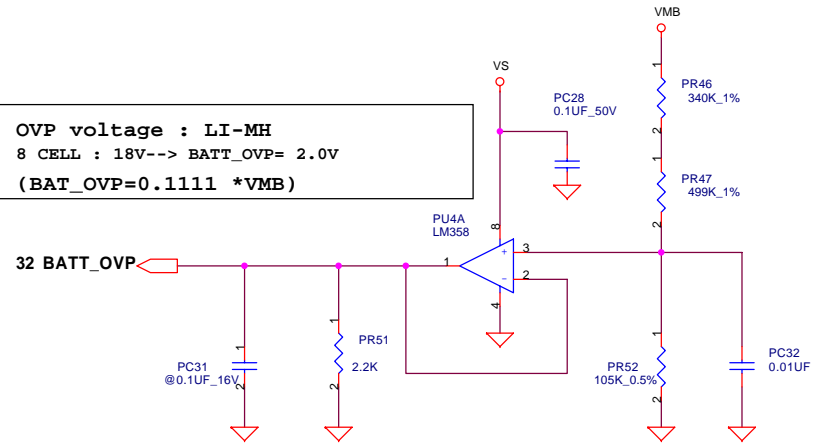


Iadp=0-3.5A

**CC=0.5-2.52A
CV=16.84V(8 CELLS LI-ION)**

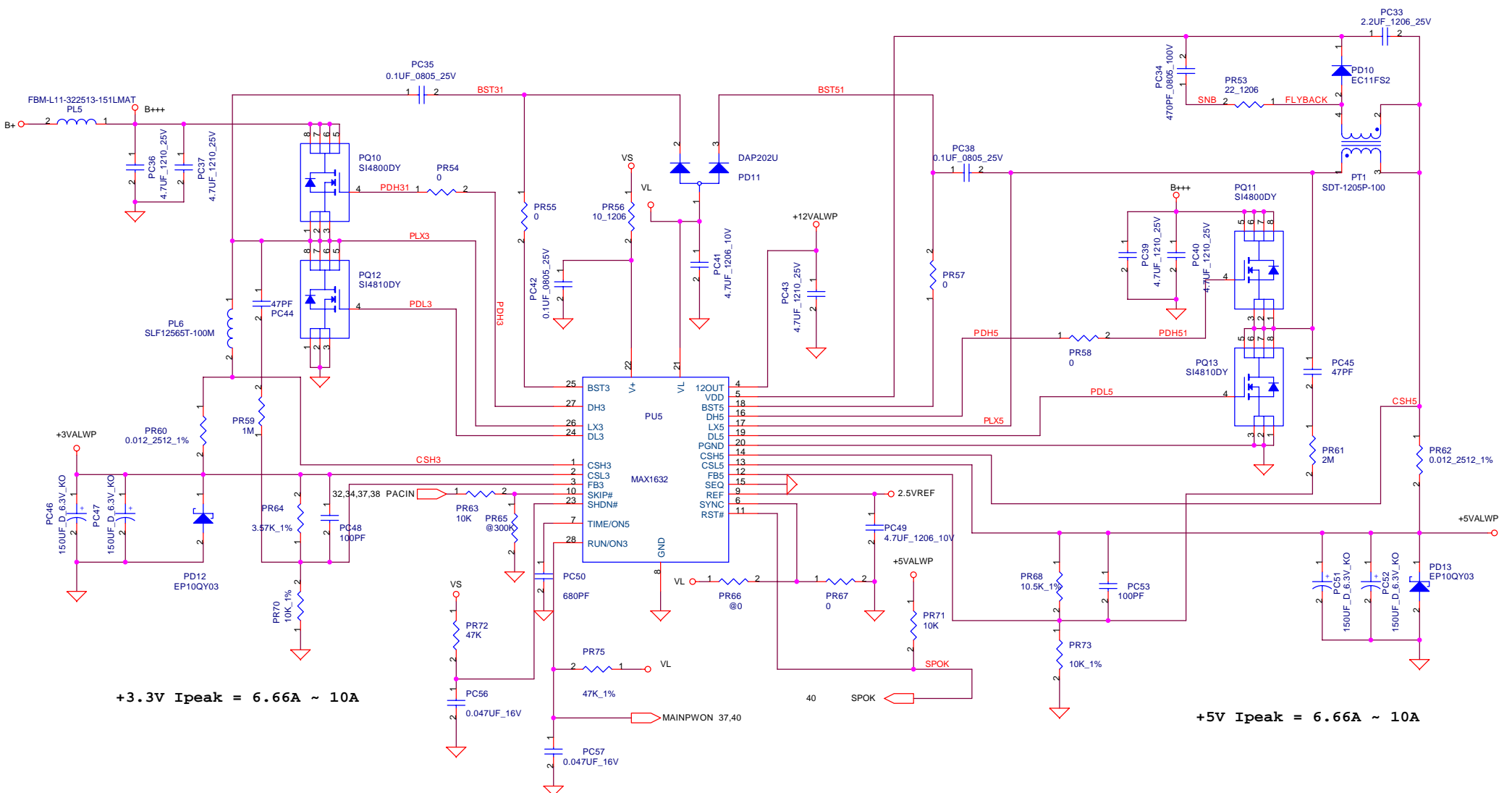
**IREF=1.31*Icharge
IREF=0.73~3.3V**

**OVP voltage : LI-MH
8 CELL : 18V--> BATT_OVP= 2.0V
(BAT_OVP=0.1111 *VMB)**



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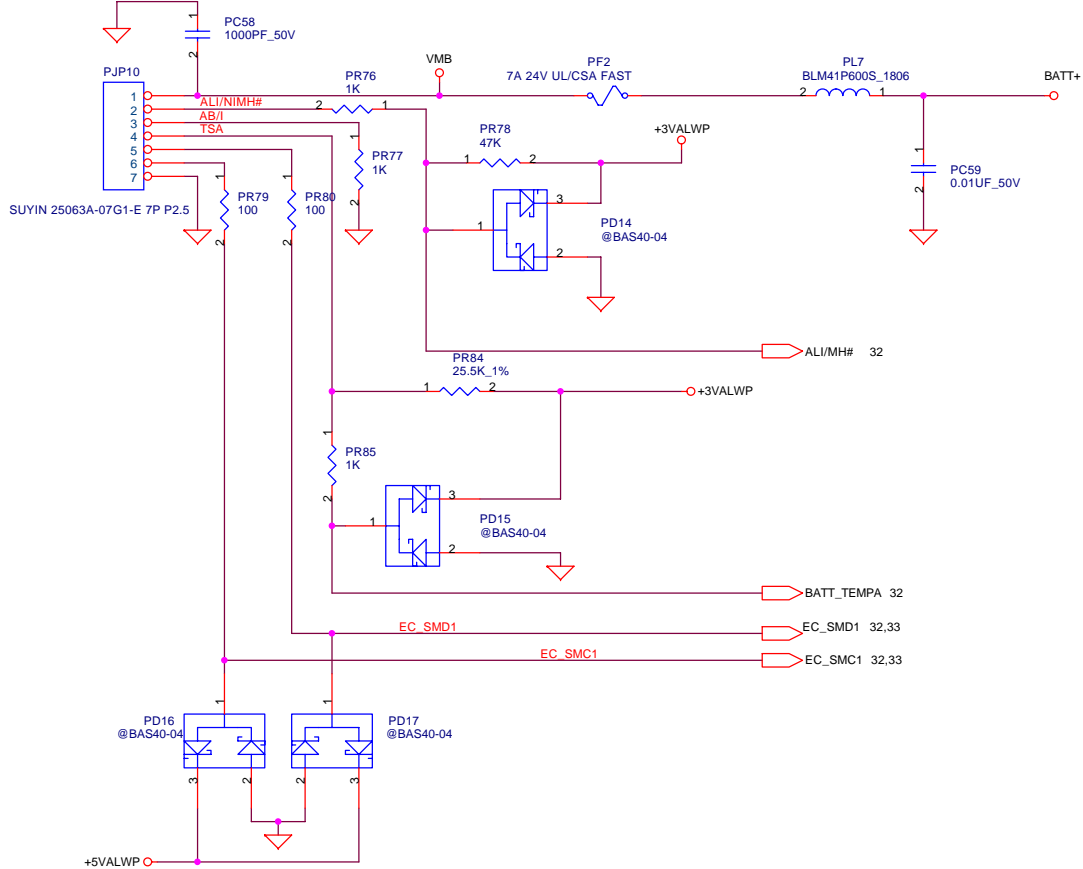


+3.3V Ipeak = 6.66A ~ 10A

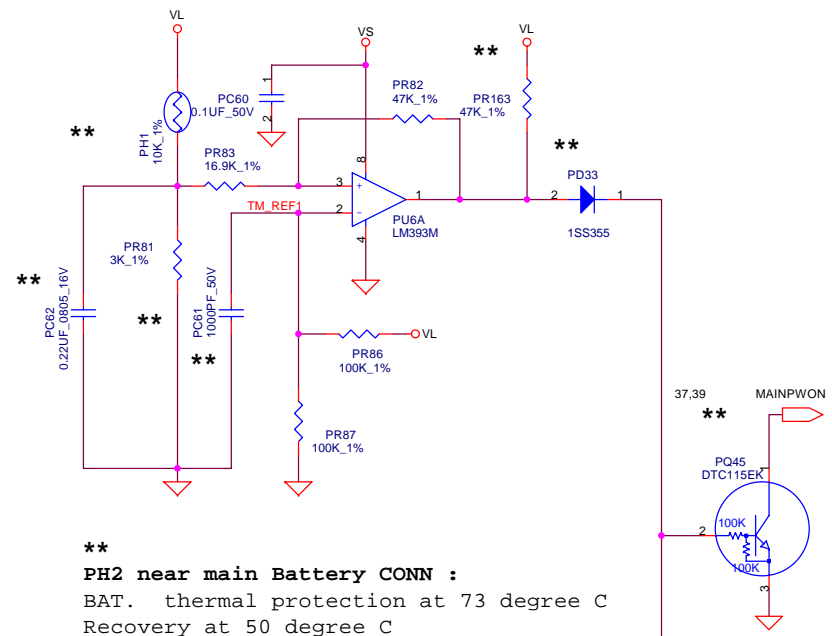
+5V Ipeak = 6.66A ~ 10A

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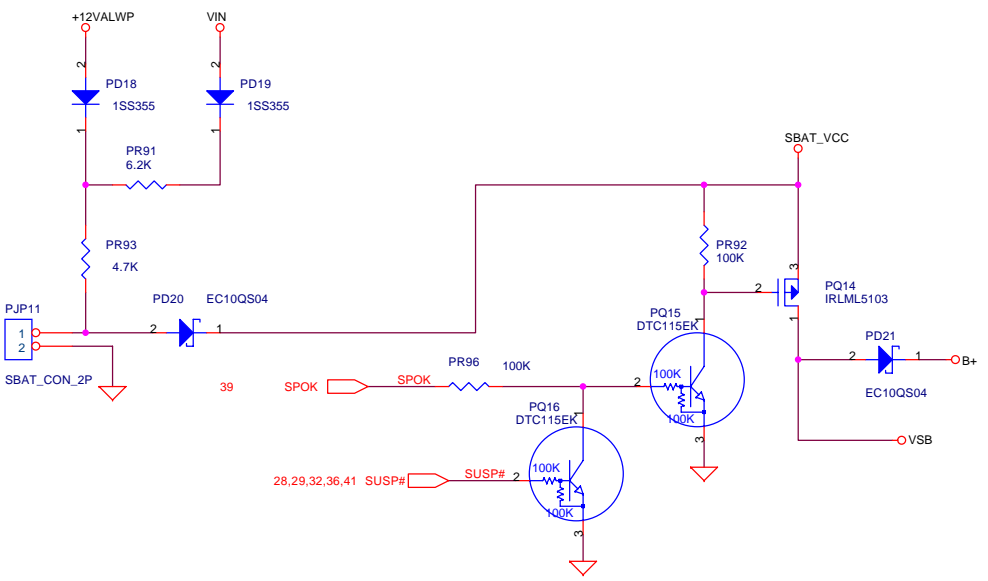
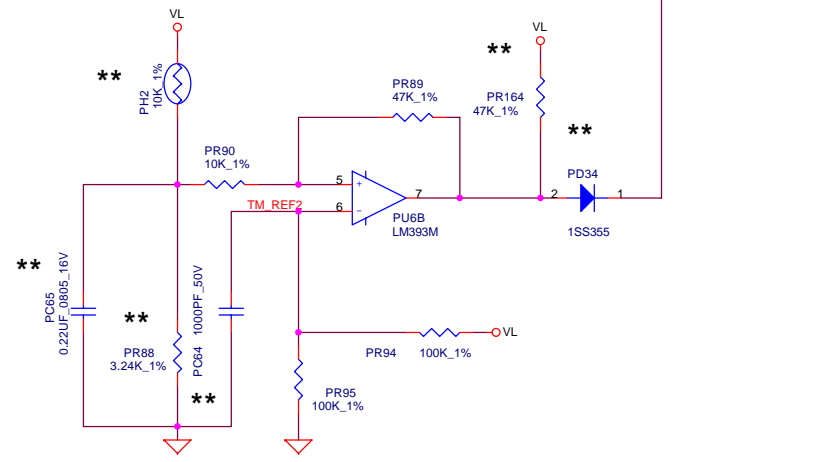
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**
PH1 under CPU botten side :
 CPU thermal protection at 87 degree C
 Recovery at 48 degree C

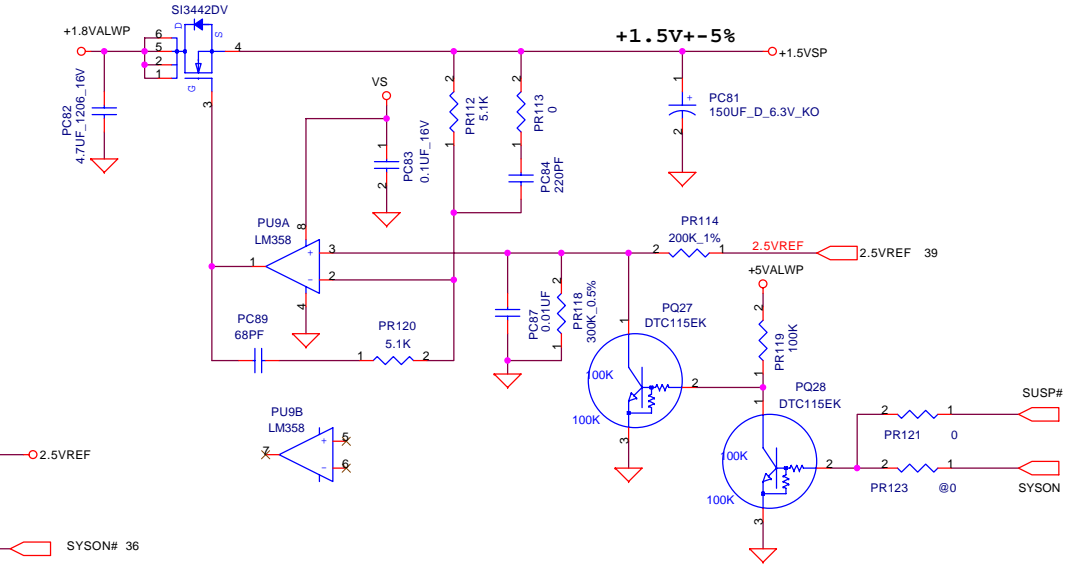
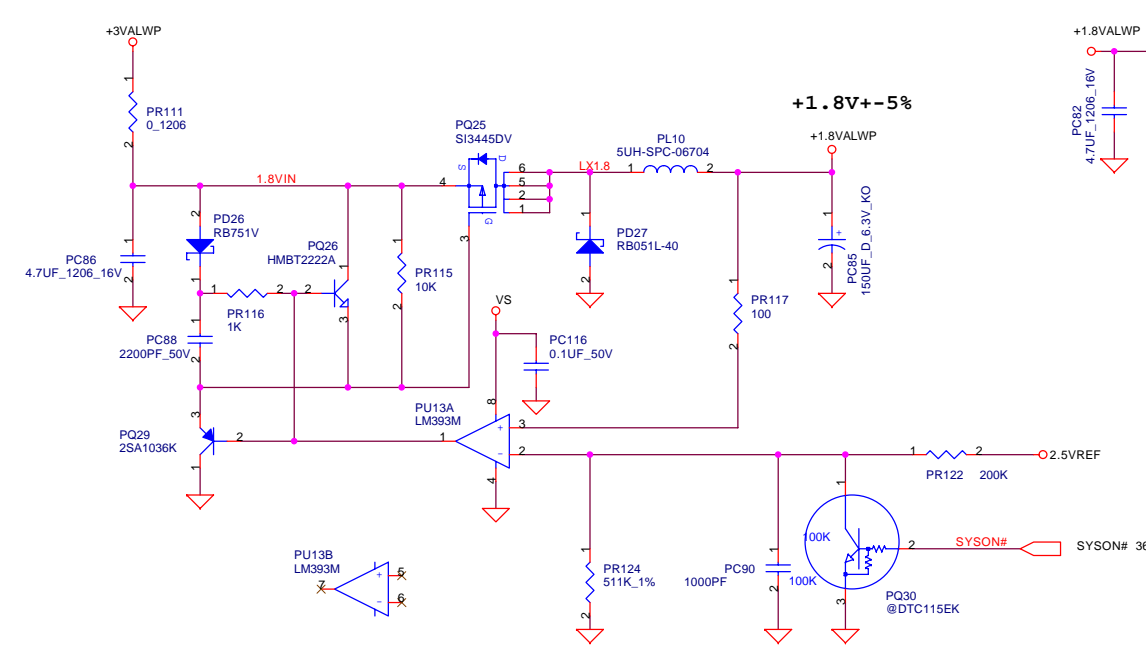
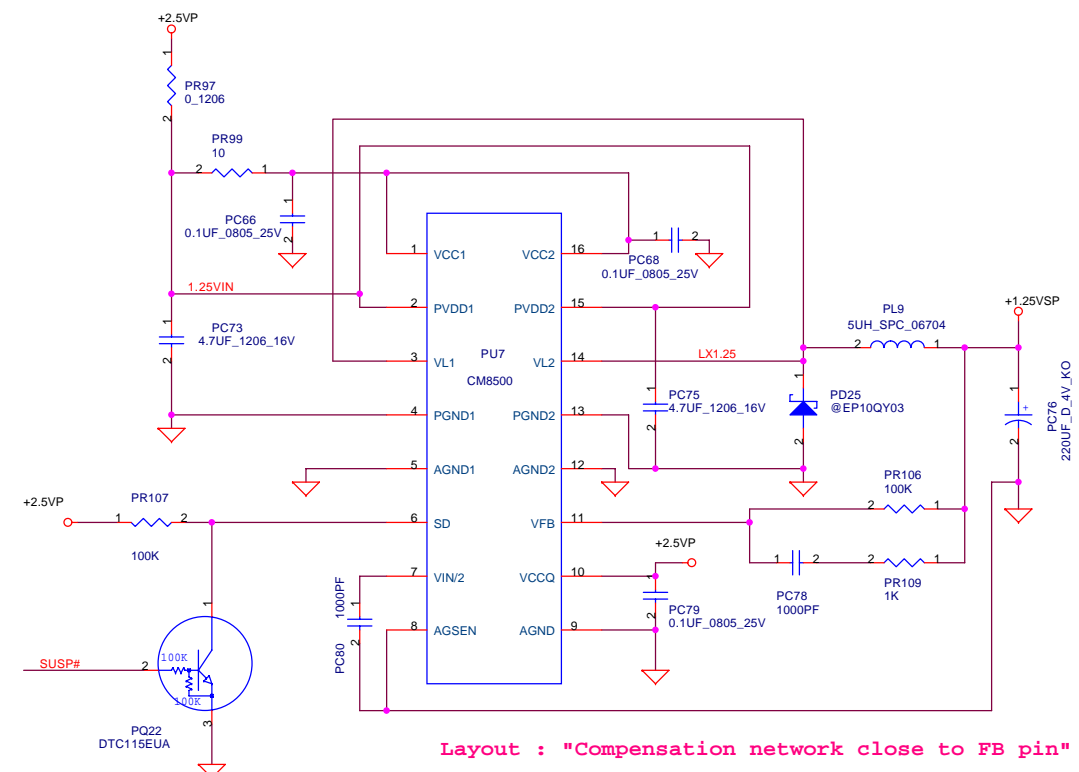
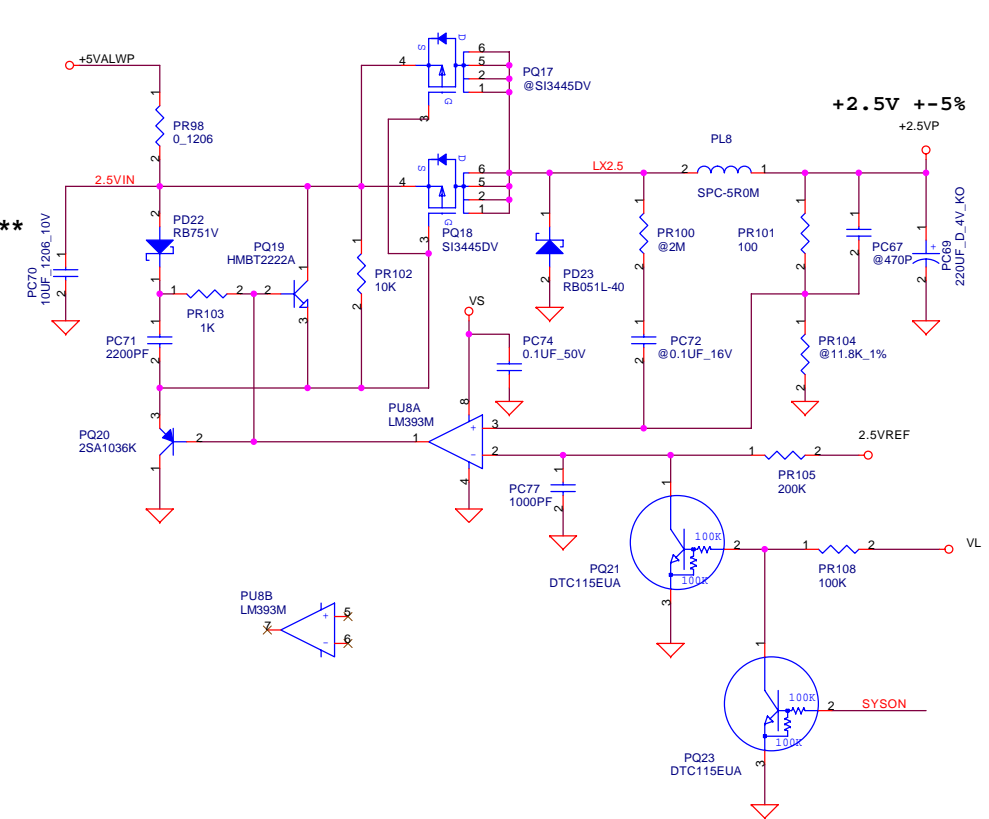


**
PH2 near main Battery CONN :
 BAT. thermal protection at 73 degree C
 Recovery at 50 degree C



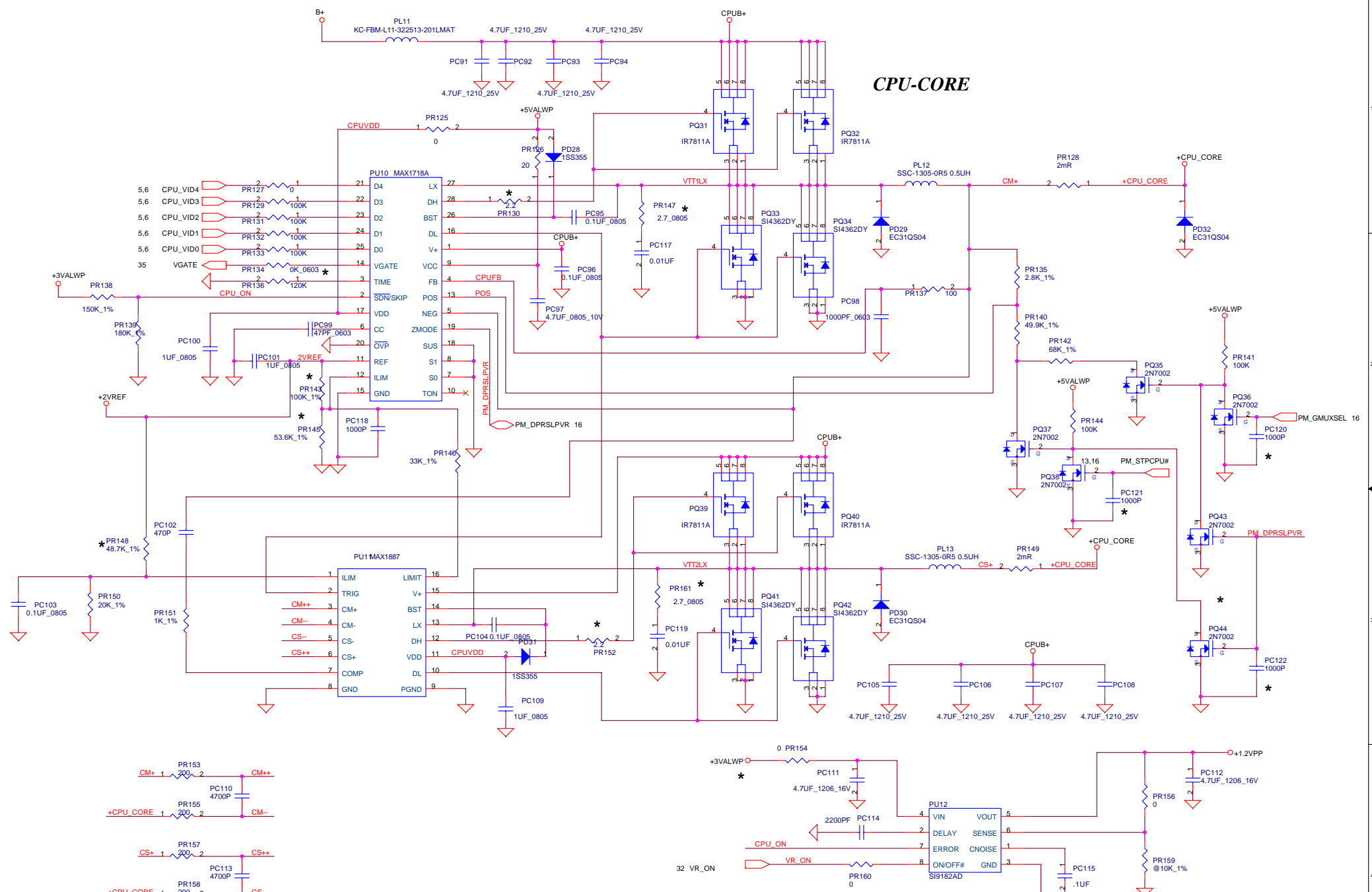
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	GMUXSEL	CPUSTP#	DPRSPLVPR	VCORE'	Offset	VCORE
PM	1	1	0	1.30V	0%	1.30V
PM D-S	1	0	0	4.62%	1.239V	
BM	0	1	0	1.20V	2.0%	1.176V
BM D-S	0	0	0	4.62%	1.144V	
Deeper	X	0	1	1.0V	0%	1.0V

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