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# HAINAN2

CPU : Intel Merom  
Chip Set : RS600M & SB600  
Remarks : Mobility Platform

Model Name : HAINAN2  
PBA Name : MAIN  
PCB Code : BA41-XXXXXA  
Dev. Step : PR  
Revision : 1.0  
T.R. Date : 2006.11.16

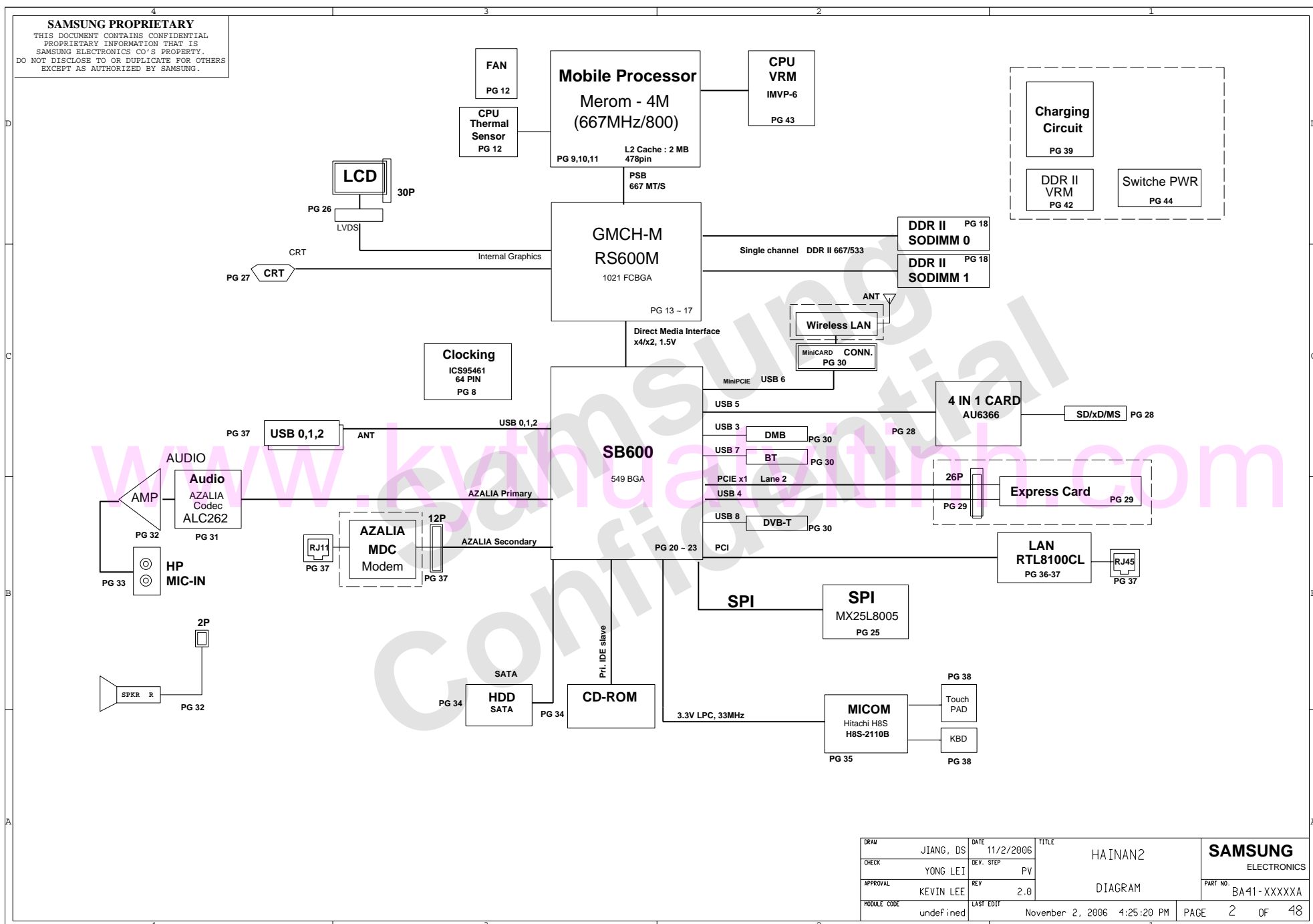
DRAW	CHECK	APPROVAL

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DRAW	JIANG, DS	DATE	11/2/2006	TITLE	HAINAN2	SAMSUNG ELECTRONICS
CHECK	YONG LEI	DEV. STEP	PV			
APPROVAL	KEVIN LEE	REV	2.0	COVER		PART NO. BA41-XXXXXA
MODULE CODE	undefined	LAST EDIT	November 2, 2006 4:25:20 PM	PAGE	1	OF 48

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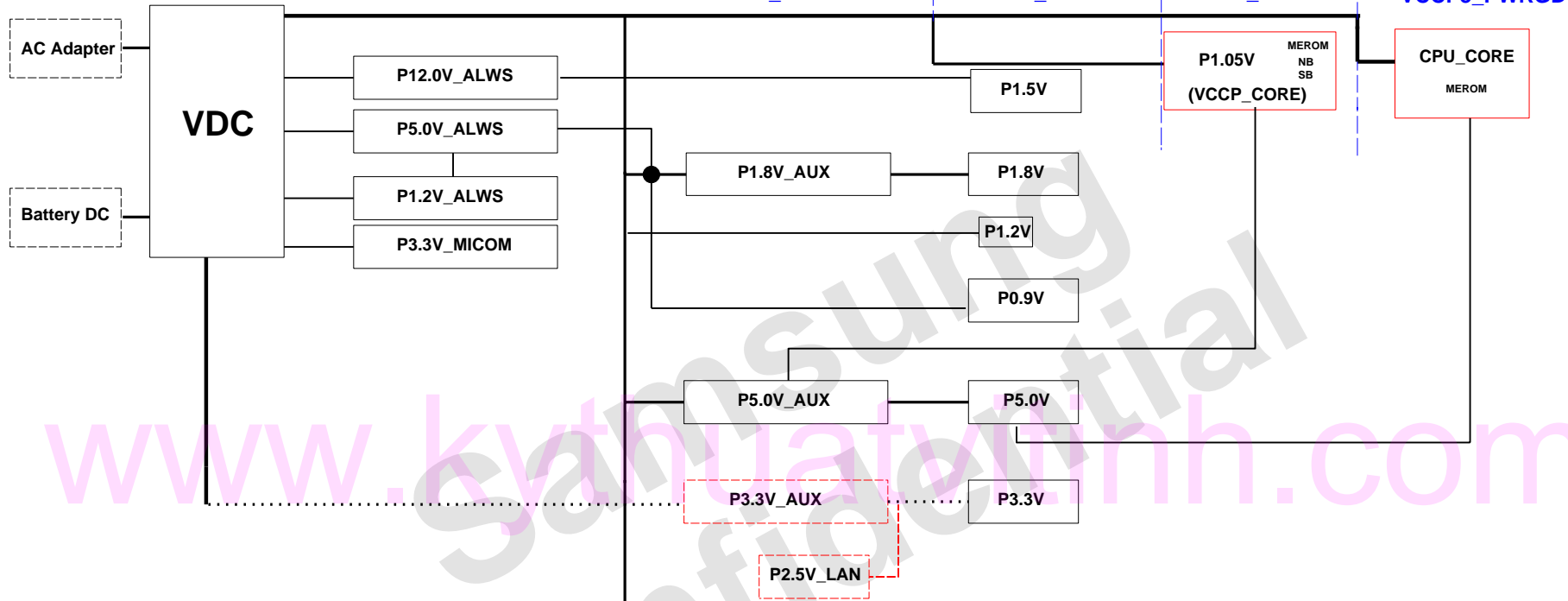


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CHECK	YONG LEI	DEV. STEP	PV			
APPROVAL	KEVIN LEE	REV	2.0			PART NO. BA41-XXXXXA
MODULE CODE	undef ined	LAST EDIT	November 2, 2006 4:25:20 PM	PAGE	2	OF 48

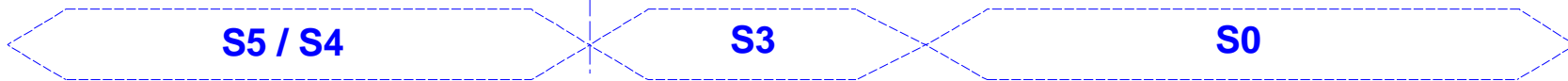
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# Power Diagram

KBC3\_SUSPWRON | KBC3\_PWRON | KBC3\_VRON | VCCP3\_PWRGD



Rail State	+V*Always	+V*AUX	+V	SUSPWR	PWRON	VRON
Full On	ON	ON	ON	H	H	H
S3	ON	ON	OFF	H	L	L
S4	ON	ON	OFF	H	L	L
S5	ON	OFF	OFF	L	L	L



DRAW	JIANG, DS	DATE	11/2/2006	TITLE	HAINAN2	SAMSUNG ELECTRONICS
CHECK	YONG LEI	DEV. STEP	PV			
APPROVAL	KEVIN LEE	REV	2.0		POWER DIAGRAM	PART NO. BA41-XXXXXA
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# POWER SEQUENCE

VDC  
ADT3\_SEL  
P3.3V\_MICOM  
KBC3\_RST\*  
P5.0V\_ALWS  
P1.2V\_ALWS  
PRTC\_BAT

KBC3\_PWRSW\*

KBC3\_SUSPWRON

P5V\_AUX/P3.3V\_AUX/P1.8V\_AUX/1.2V\_AUX

KBC3\_RSMRST\*

MEM1\_VREF

KBC3\_PWRBTN\*

CHP3\_SLPS5\*

CHP3\_SLPS3\*

KBC3\_PWRON

KBC3\_CLKPWRGD#

P5.0V

PWRON

P1.8V/P1.5V/P0.9V/P1.2V

KBC3\_RUNSCI#

KBC3\_VRON

VCCP\_CORE

VCCP3\_PWRGD

CPU\_CORE

VRM3\_CPU\_PWRGD

KBC3\_NBPWRGD

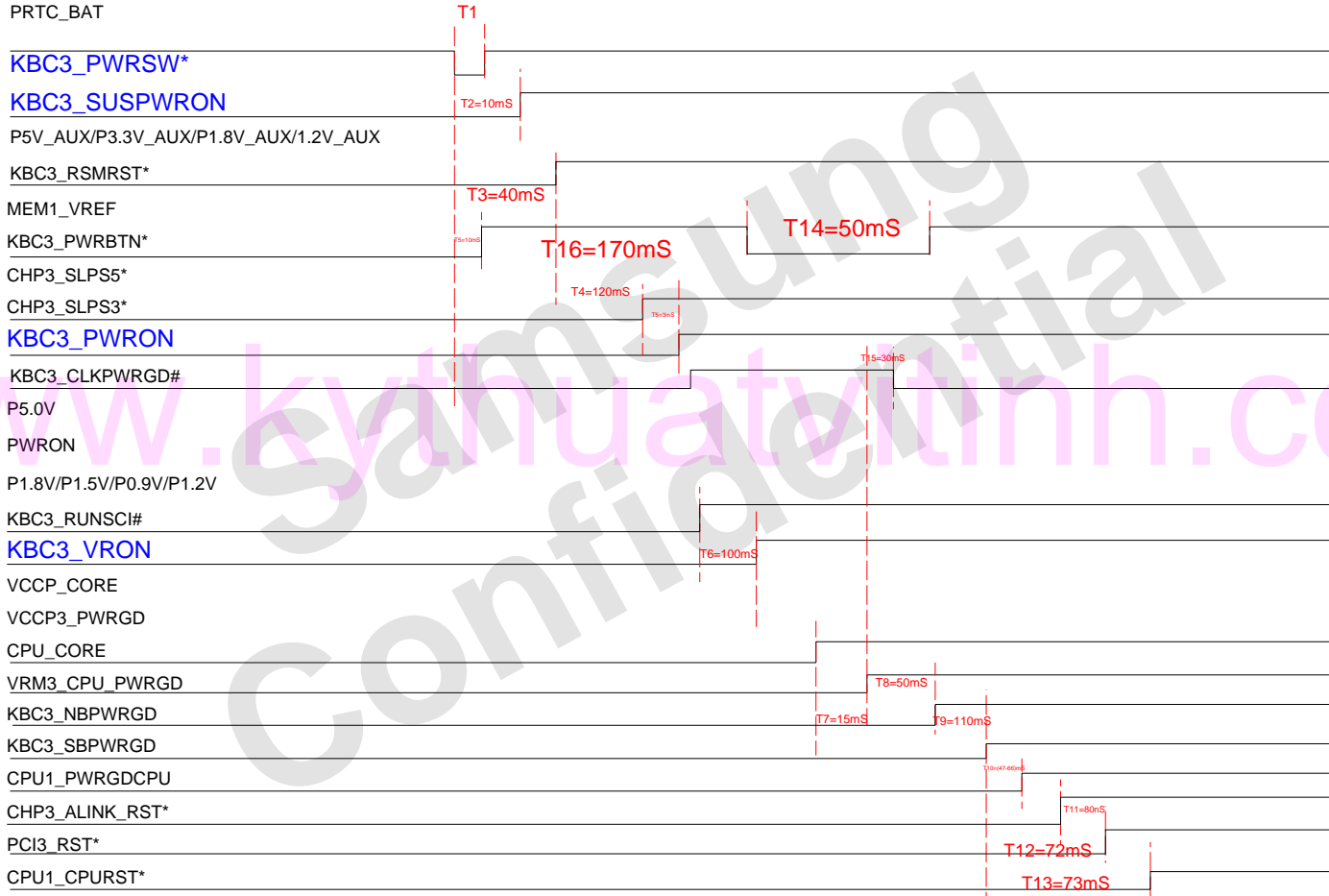
KBC3\_SBPWRGD

CPU1\_PWRGDPCPU

CHP3\_ALINK\_RST\*

PCI3\_RST\*

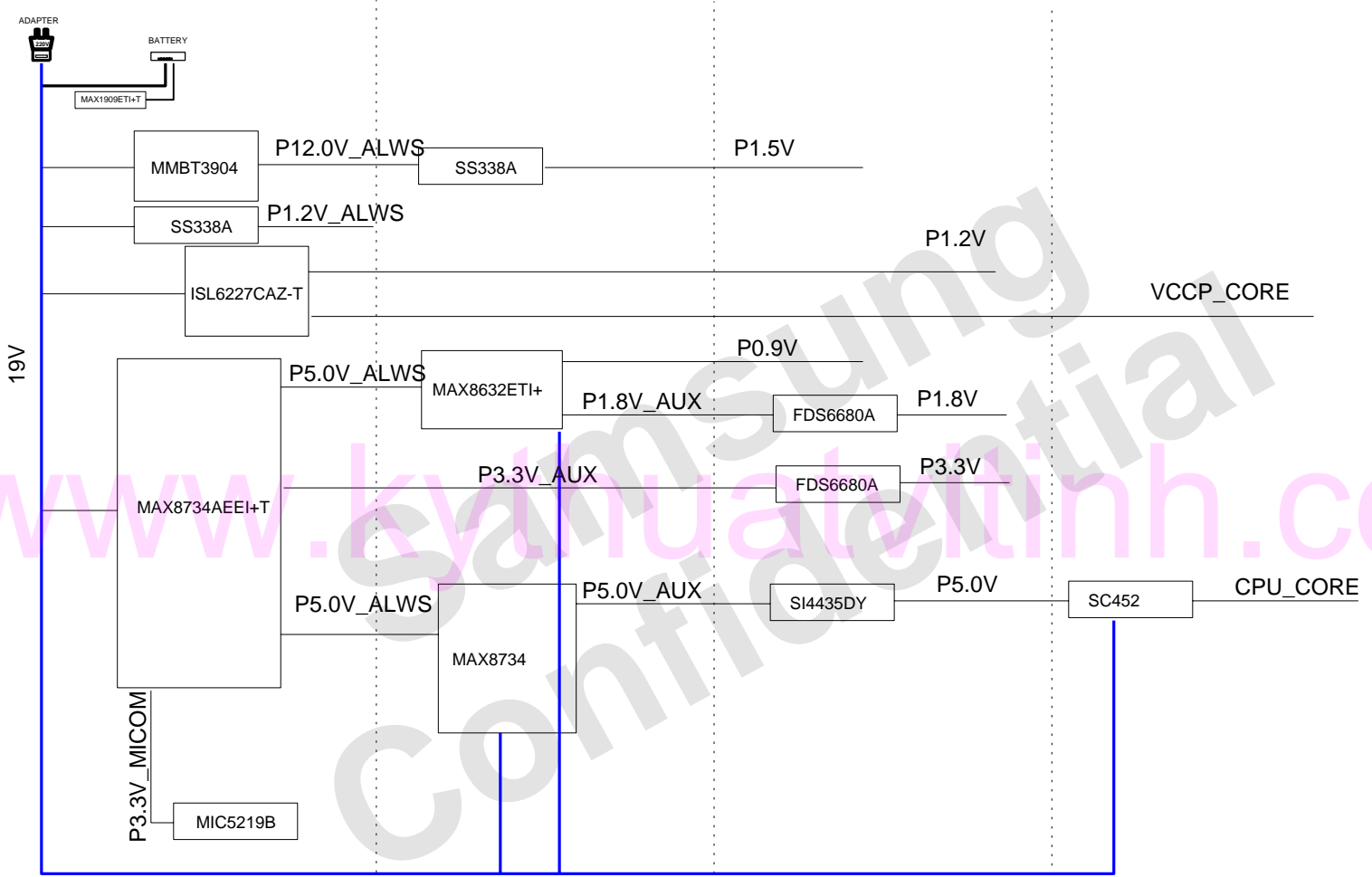
CPU1\_CPURST\*



DRAW	JIANG, DS	DATE	11/2/2006	TITLE	HAINAN2	SAMSUNG ELECTRONICS
CHECK	YONG LEI	DEV. STEP	PV			
APPROVAL	KEVIN LEE	REV	2.0	POWER SEQUENCE		PART NO. BA41-XXXXXA
MODULE CODE	undef ined	LAST EDIT	November 2, 2006 4:25:20 PM	PAGE	4	OF 48

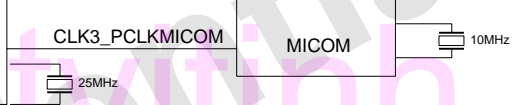
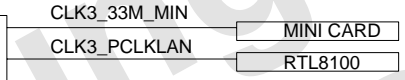
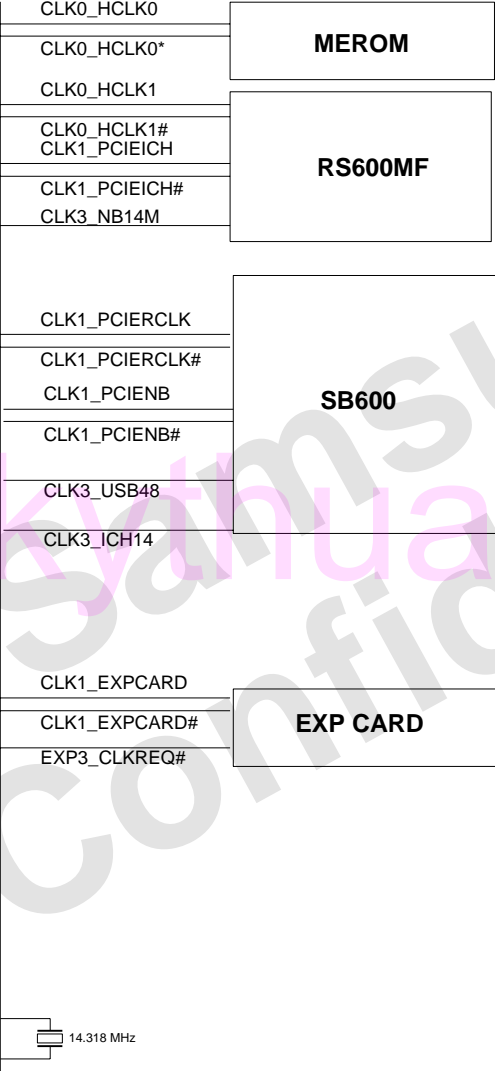
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# POWER RAILS ANALYSIS



DRAW	JIANG, DS	DATE	11/2/2006	TITLE	HAINAN2	<b>SAMSUNG</b> ELECTRONICS
CHECK	YONG LEI	DEV. STEP	PV			
APPROVAL	KEVIN LEE	REV	2.0		POWER BLOCK	PART NO. BA41-XXXXXA
MODULE CODE	undef ined	LAST EDIT	November 2, 2006 4:25:20 PM	PAGE	5	OF 48

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DRAW	JIANG, DS	DATE	11/2/2006	TITLE	HAINAN2	<b>SAMSUNG</b> ELECTRONICS
CHECK	YONG LEI	DEV. STEP	PV	CLOCK DIAGRAM		
APPROVAL	KEVIN LEE	REV	2.0	PART NO. BA41-XXXXXA		PAGE 6 OF 48
MODULE CODE	undefined	LAST EDIT	November 2, 2006 4:25:20 PM			

# SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

## PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
LAN	AD21	1	G
USB	AD30(internal)	-	-
Hub to PCI	AD31(internal)	-	-
LPC bridge/IDE/AC97/SMBUS	AD31(internal)	-	-
Internal MAC	AD31(internal)	-	-
AC Link	-	-	-

## Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	SB600	Real Time Clock
Crystal	10MHz	MICOM	HS64FZ110B
Crystal	14.318MHz	CLOCK-Generator	ICS95481
Crystal	12MHz	AUG366	4 IN 1 CARD
Crystal	25MHz	LAN	LOM

## Voltage Rails

CPU_CORE	CPU	CPU RS600 SB600
VCCP_CORE	CPU	RS600 SB600
P1.2V	RS600	SB600
P1.5V	CPU	EXPCARD
P1.8V	RS600	
P0.9V	DDR2	
P5.0V	FAN	THERMAL CRT SB600 AU6366 MINIPCI ALC262 HDD ODD MICOM USB TOUCH-PAD CPU_CORE
P3.3V	SYSTEM	POWER
P2.5V_LAN	RTL8100	
P1.8V_AUX	DDR2	P1.8V RS600
P5.0V_AUX	THERMAL	LCD P1.2V P5.0V
P3.3V_AUX	MDC	MICOM MINIPCI EXP-CARD SB600 THERMAL
P12.0V_ALWS	P1.5V	P3.3V P1.8V
P5.0V_ALWS	P3.3V	DDR2-PWR
P3.3V_MICOM	THERMAL	SB600 MICOM LED P1.8V_ALWS
P1.2V_ALWS	SB600	P1.2V
VDC	Primary DC system power supply (7 to 21V)	

## CPU Core Voltage Table IMVP-6

Active Mode		Active/Deeper Sleep Dual Mode Region		Deeper Sleep/Extended Deeper Sleep Dual Mode Region	
VID(6:0)	Voltage	VID(6:0)	Voltage	VID(6:0)	Voltage
0 0 0 0 0 0 0	1.5000 V	0 1 0 1 0 0 0	1.0000 V	1 0 1 0 0 0 1	0.4875 V
0 0 0 0 0 0 0	1.4875 V	0 1 0 1 0 0 0	0.9875 V	1 0 1 0 0 0 1	0.4750 V
0 0 0 0 0 0 1	1.4750 V	0 1 0 1 0 0 1	0.9750 V	1 0 1 0 0 0 1	0.4625 V
0 0 0 0 0 1 1	1.4625 V	0 1 0 1 0 1 0	0.9625 V	1 0 1 0 1 0 0	0.4500 V
0 0 0 0 1 0 0	1.4500 V	0 1 0 1 1 0 0	0.9500 V	1 0 1 0 1 0 0	0.4375 V
0 0 0 1 0 0 0	1.4375 V	0 1 0 1 1 0 1	0.9375 V	1 0 1 0 1 0 0	0.4250 V
0 0 0 1 0 1 0	1.4250 V	0 1 0 1 1 1 0	0.9250 V	1 0 1 0 1 1 1	0.4125 V
0 0 0 1 1 0 0	1.4125 V	0 1 0 1 1 1 1	0.9125 V	1 0 1 1 0 0 0	0.4000 V
0 0 0 1 1 0 0	1.4000 V	0 1 1 0 0 0 0	0.9000 V	1 0 1 1 0 0 1	0.3875 V
0 0 0 1 1 0 1	1.3875 V	0 1 1 0 0 0 1	0.8875 V	1 0 1 1 0 1 0	0.3750 V
0 0 0 1 1 0 1	1.3750 V	0 1 1 0 0 1 0	0.8750 V	1 0 1 1 0 1 1	0.3625 V
0 0 0 1 1 0 1	1.3625 V	0 1 1 0 0 1 1	0.8625 V	1 0 1 1 1 0 0	0.3500 V
0 0 0 1 1 0 1	1.3500 V	0 1 1 0 1 0 0	0.8500 V	1 0 1 1 1 0 1	0.3375 V
0 0 0 1 1 0 1	1.3375 V	0 1 1 0 1 0 1	0.8375 V	1 0 1 1 1 1 0	0.3250 V
0 0 0 1 1 1 0	1.3250 V	0 1 1 1 0 0 0	0.8250 V	1 0 1 1 1 1 1	0.3125 V
0 0 0 1 1 1 1	1.3125 V	0 1 1 1 0 0 1	0.8125 V	1 1 0 0 0 0 0	0.3000 V
0 0 1 0 0 0 0	1.3000 V	0 1 1 1 0 0 1	0.8000 V	1 1 0 0 0 0 1	0.2875 V
0 0 1 0 0 0 1	1.2875 V	0 1 1 1 0 1 0	0.7875 V	1 1 0 0 0 1 0	0.2750 V
0 0 1 0 0 1 0	1.2750 V	0 1 1 1 0 1 1	0.7750 V	1 1 0 0 1 0 0	0.2625 V
0 0 1 0 0 1 1	1.2625 V	0 1 1 1 1 0 0	0.7625 V	1 1 0 0 1 0 1	0.2500 V
0 0 1 0 1 0 0	1.2500 V	0 1 1 1 1 0 1	0.7500 V	1 1 0 0 1 0 1	0.2375 V
0 0 1 0 1 0 1	1.2375 V	0 1 1 1 1 1 0	0.7375 V	1 1 0 0 1 1 0	0.2250 V
0 0 1 0 1 1 0	1.2250 V	0 1 1 1 1 1 1	0.7250 V	1 1 0 0 1 1 1	0.2125 V
0 0 1 1 0 0 0	1.2125 V	0 1 1 1 1 1 1	0.7125 V	1 1 0 1 0 0 0	0.2000 V
0 0 1 1 0 0 0	1.2000 V	1 0 0 0 0 0 0	0.7000 V	1 1 0 1 0 0 1	0.1875 V
0 0 1 1 0 0 1	1.1875 V	1 0 0 0 0 0 1	0.6875 V	1 1 0 1 0 1 0	0.1750 V
0 0 1 1 0 1 0	1.1750 V	1 0 0 0 0 1 0	0.6750 V	1 1 0 1 0 1 1	0.1625 V
0 0 1 1 0 1 1	1.1625 V	1 0 0 0 0 1 1	0.6625 V	1 1 0 1 0 1 1	0.1500 V
0 0 1 1 0 1 0	1.1500 V	1 0 0 0 1 0 0	0.6500 V	1 1 0 1 0 1 0	0.1375 V
0 0 1 1 0 1 1	1.1375 V	1 0 0 0 1 0 1	0.6375 V	1 1 0 1 1 1 0	0.1250 V
0 0 1 1 1 1 0	1.1250 V	1 0 0 0 1 1 0	0.6250 V	1 1 0 1 1 1 1	0.1125 V
0 0 1 1 1 1 1	1.1125 V	1 0 0 0 1 1 1	0.6125 V	1 1 1 0 0 0 0	0.1000 V
0 1 0 0 0 0 0	1.1000 V	1 0 0 1 0 0 0	0.6000 V	1 1 1 0 0 0 1	0.0875 V
0 1 0 0 0 0 1	1.0875 V	1 0 0 1 0 0 1	0.5875 V	1 1 1 0 0 1 0	0.0750 V
0 1 0 0 0 1 0	1.0750 V	1 0 0 1 0 1 0	0.5750 V	1 1 1 0 0 1 1	0.0625 V
0 1 0 0 1 0 1	1.0625 V	1 0 0 1 1 0 1	0.5625 V	1 1 1 0 1 0 0	0.0500 V
0 1 0 0 1 1 0	1.0500 V	1 0 0 1 1 1 0	0.5500 V	1 1 1 0 1 0 1	0.0375 V
0 1 0 0 1 1 0	1.0375 V	1 0 0 1 1 1 1	0.5375 V	1 1 1 0 1 1 0	0.0250 V
0 1 0 0 1 1 1	1.0250 V	1 0 0 1 1 1 1	0.5250 V	1 1 1 0 1 1 1	0.0125 V
0 1 0 0 1 1 1	1.0125 V	1 0 0 1 1 1 1	0.5125 V	1 1 1 1 0 0 0	0.0000 V
		1 0 1 0 0 0 0	0.5000 V	1 1 1 1 0 0 1	0.0000 V
				1 1 1 1 0 1 0	0.0000 V
				1 1 1 1 0 1 1	0.0000 V
				1 1 1 1 1 0 0	0.0000 V
				1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0	0.0000 V
				1 1 1 1 1 1 1	0.0000 V
				1 1 1 1 1 1 1	0.0000 V
				1 1 1 1 1 1 1	0.0000 V

Active: DPRSLPVR 0, DPRSTP\* 1, PSI2\* 0 or 1  
 Deeper Slip: DPRSLPVR 1, DPRSTP\* 0, PSI2\* 0 or 1

\*\*11111111\*: 0V power good asserted.

## I C / SMB Address

Devices	Address	Hex	Bus
SB600	Master	-	SMBUS Master
EM6CN300(CPU Thermal Sensor)	1001 110X	9Ch	Thermal Sensor
SODIMM0	1010 0000	A0h	-
SODIMM1	1010 001X	A2h	-
ICS95411 (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable

## USB PORT Assign

PORT NUMBER	ASSIGNED TO
0	SYSTEM PORT A
1,2	SYSTEM PORT B
3	DMB
4	EXPRESS CARD
5	4 IN 1 CARD
6,8	MINI PCIE
7	BT

## System Power States

CHP3\_SLPS1\* S1, **Powered-On-Suspend(POS)** : In this state, all clocks(except the 32.768KHz clock) are stopped. The system context is maintained in system DRAM. Power is maintained to PCI, the CPU, memory controller, memory, and all other critical subsystems. Memory is retained, and refreshes continue. All clocks stop except RTC clock. Note that this state does not preclude power being removed from non-essential devices, such as disk drives. During this state, CPU can be selected for either Deep Sleep or Deeper Sleep.

CHP3\_SLPS3\* S3, **Suspend-To-RAM(STR)** : The system context is maintained in system DRAM, but power is shut off to non-critical circuits. In Deeper Sleep, CPU voltage reduced in this state to reduce the leakage power.

CHP3\_SLPS4\* S4, **Suspend-To-Disk(STD)** : The Context of the system is maintained on the disk. All power is then shut off to the system except for the logic required to resume. Externally appears same as S5, but may have different wake events.

CHP3\_SLPS5\* S5, **Soft Off(SOFF)** : System context is not maintained. All power is shut off except for the logic required to restart. A full boot is required when waking.

\*Yonah Processor (2.33 GHz / 800 MHz : TBD)

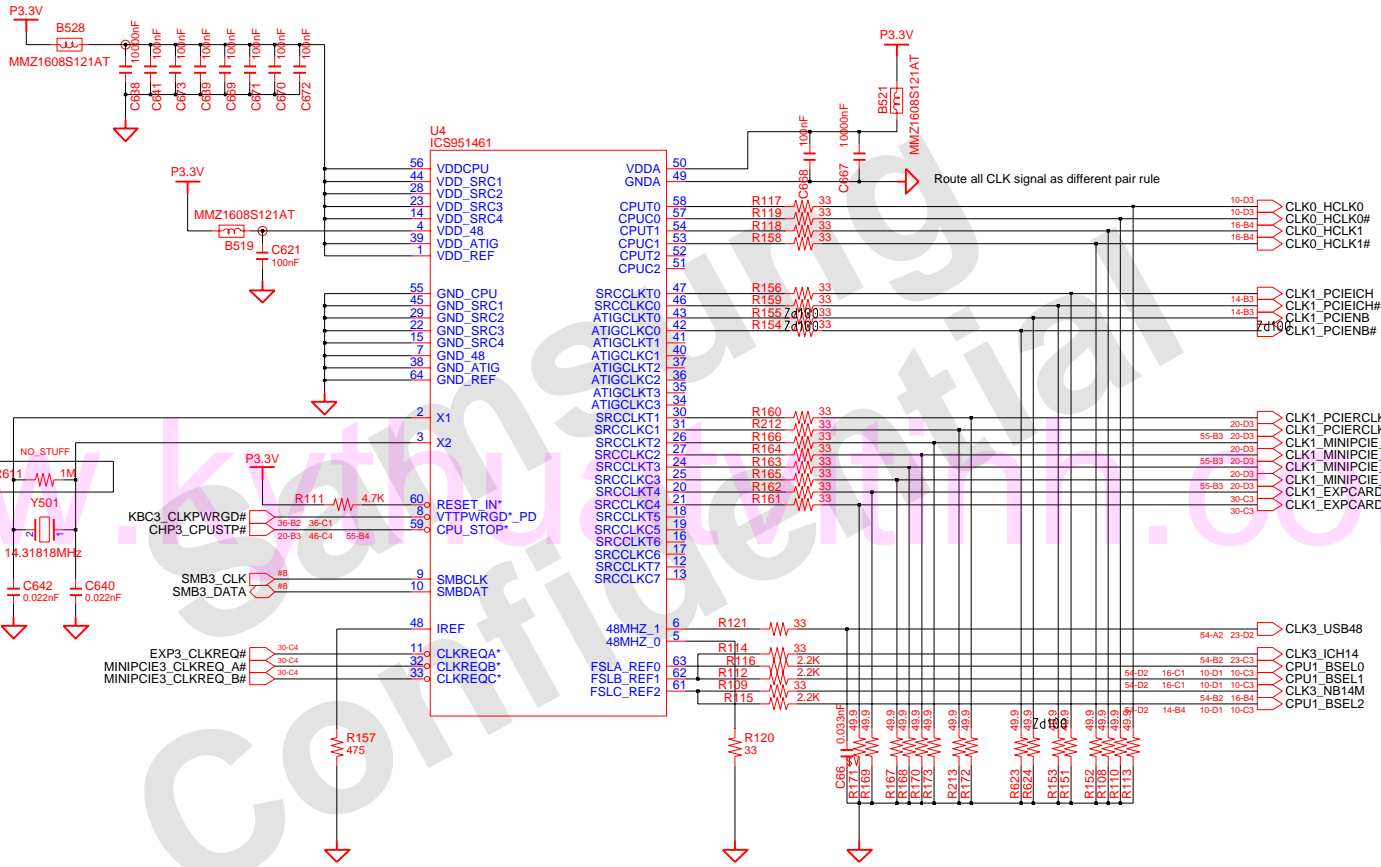
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CHECK	YONG LEI	DEV. STEP	PV			
APPROVAL	KEVIN LEE	REV	2.0		ANNOTATIONS	PART NO. BA41-XXXXXA
MODULE CODE	undef ined	LAST EDIT	November 2, 2006 4:25:20 PM	PAGE	7	OF 48

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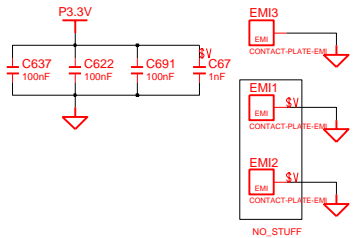
CPU	FSA	FSB	FSC	HOST CLK
	BSEL0	BSEL1	BSEL2	
	0	0	0	266 MHz
	0	0	1	333 MHz
	0	1	0	200 MHz
	0	1	1	400 MHz
	1	0	0	133 MHz
	1	0	1	100 MHz
	1	1	0	166 MHz
	1	1	1	RSVD

Pt decoupling CAPS close to ICS951461 power pin



Route all CLK signal as different pair rule

Place all te series termination resistor as clos as ICS951461 as possible

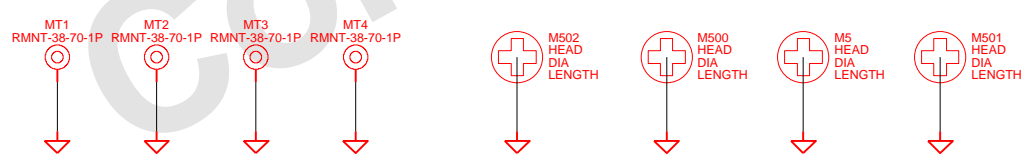
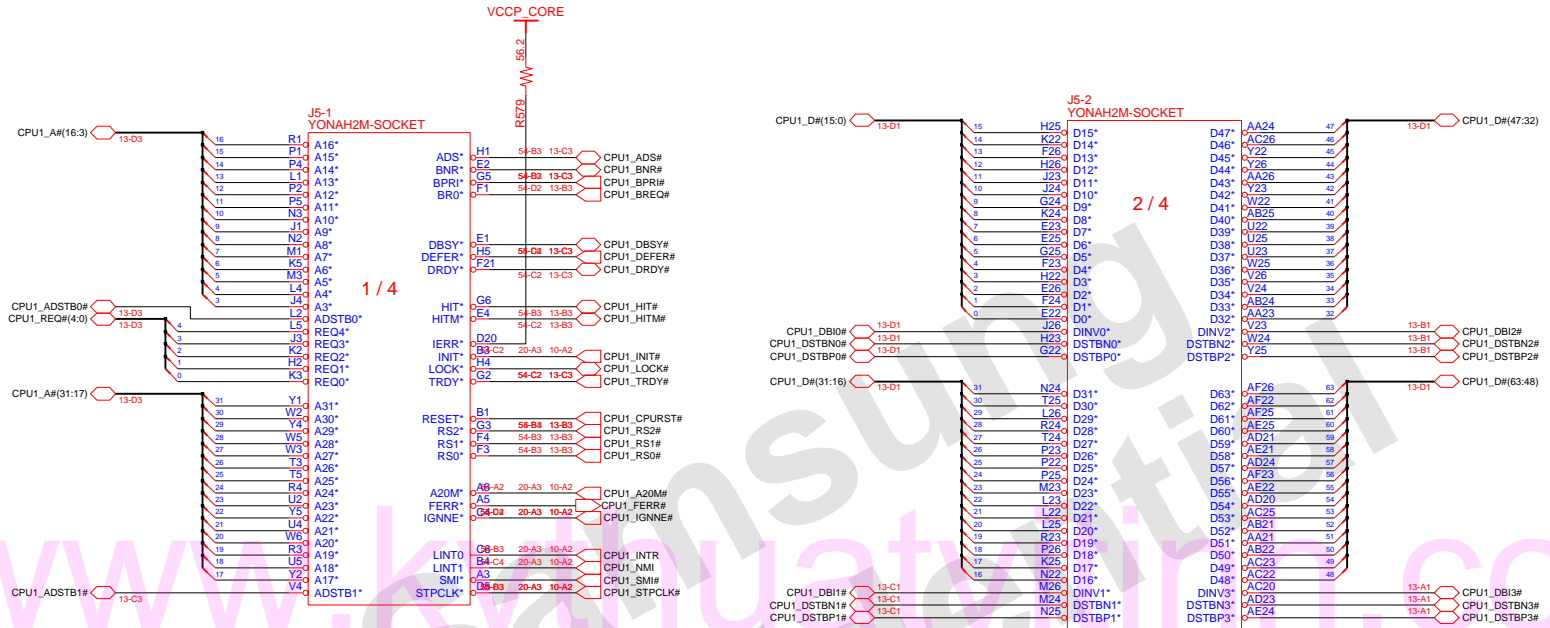


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APPROVAL	KEVIN LEE	REV	2.0		BA41-XXXXXA	
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APPROVAL	KEVIN LEE	REV	2.0		MEROM(1/3)	PART NO. BA41-XXXXXA
MODULE CODE	undef ined	LAST EDIT	November 2, 2006 4:25:20 PM	PAGE	9	OF 48

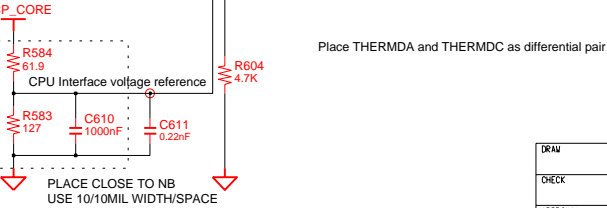
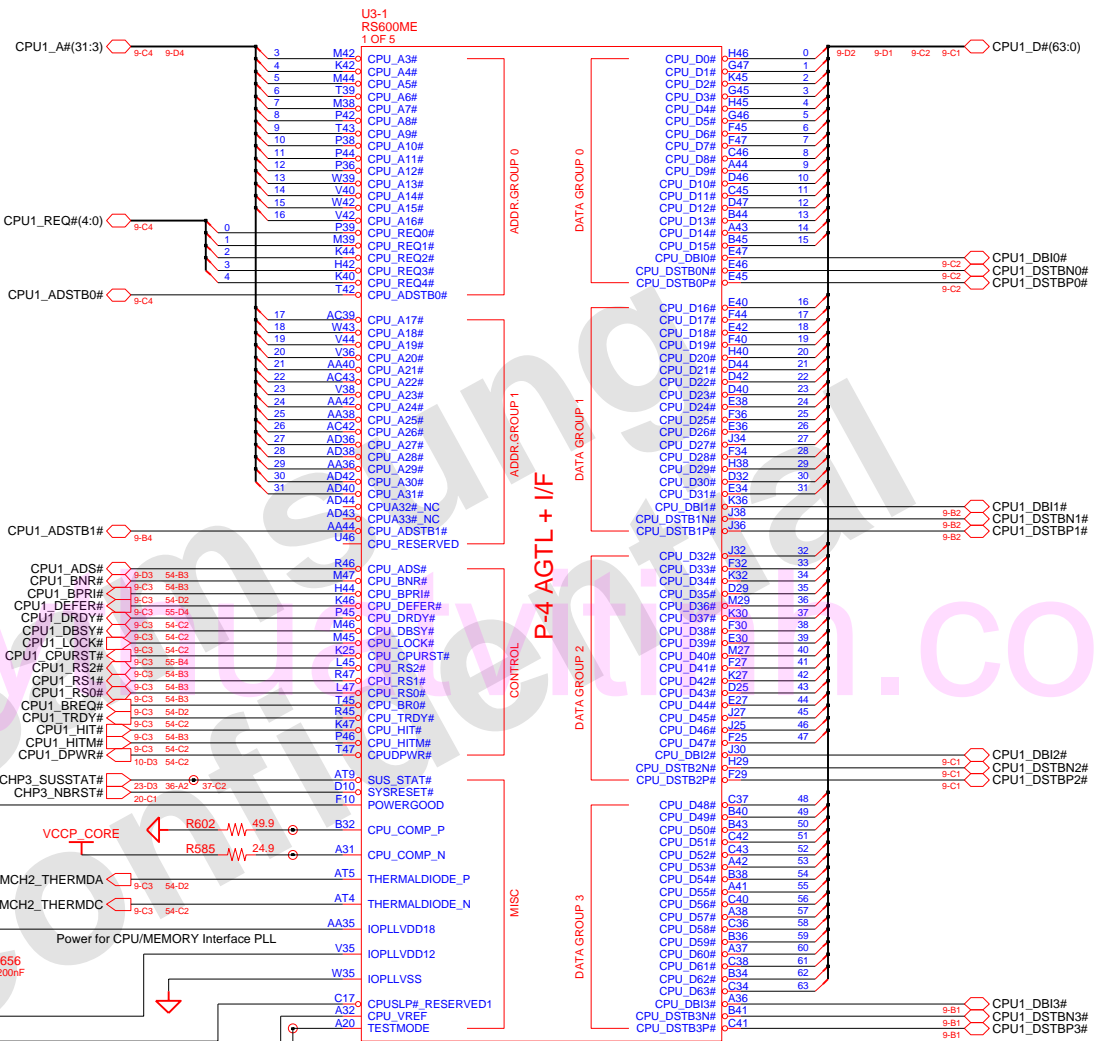
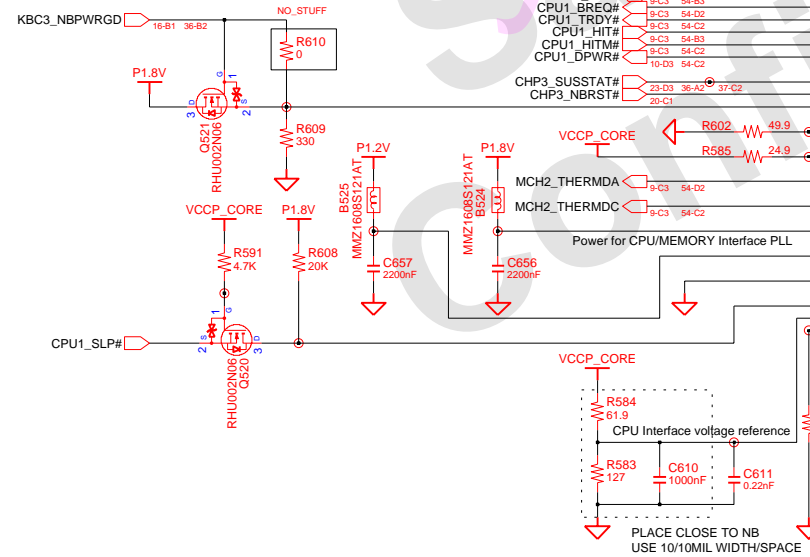
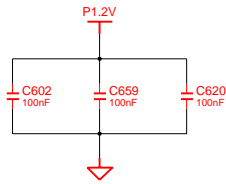






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CHECK	YONG LEI	DEV. STEP	PV		HAINAN2	
APPROVAL	KEVIN LEE	REV	2.0		RS600 (1/5)	PART NO. BA41-XXXXXA
MODULE CODE		LAST EDIT	November 2, 2006 4:25:20 PM	PAGE	13	OF 48

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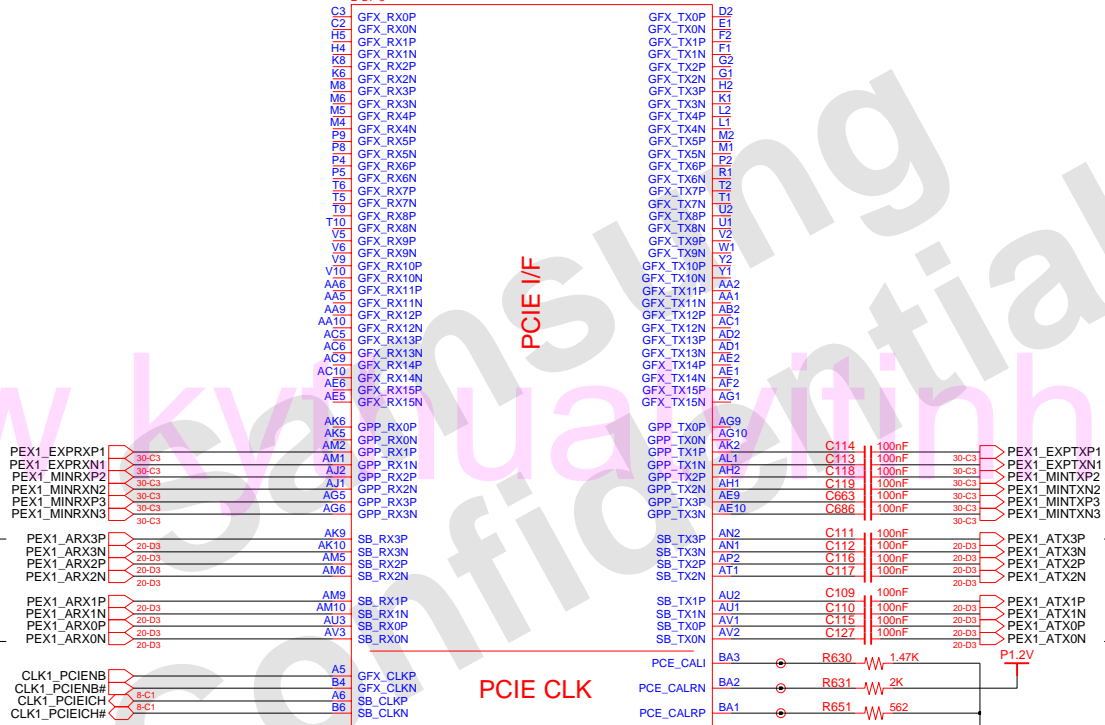
4

3

2

1

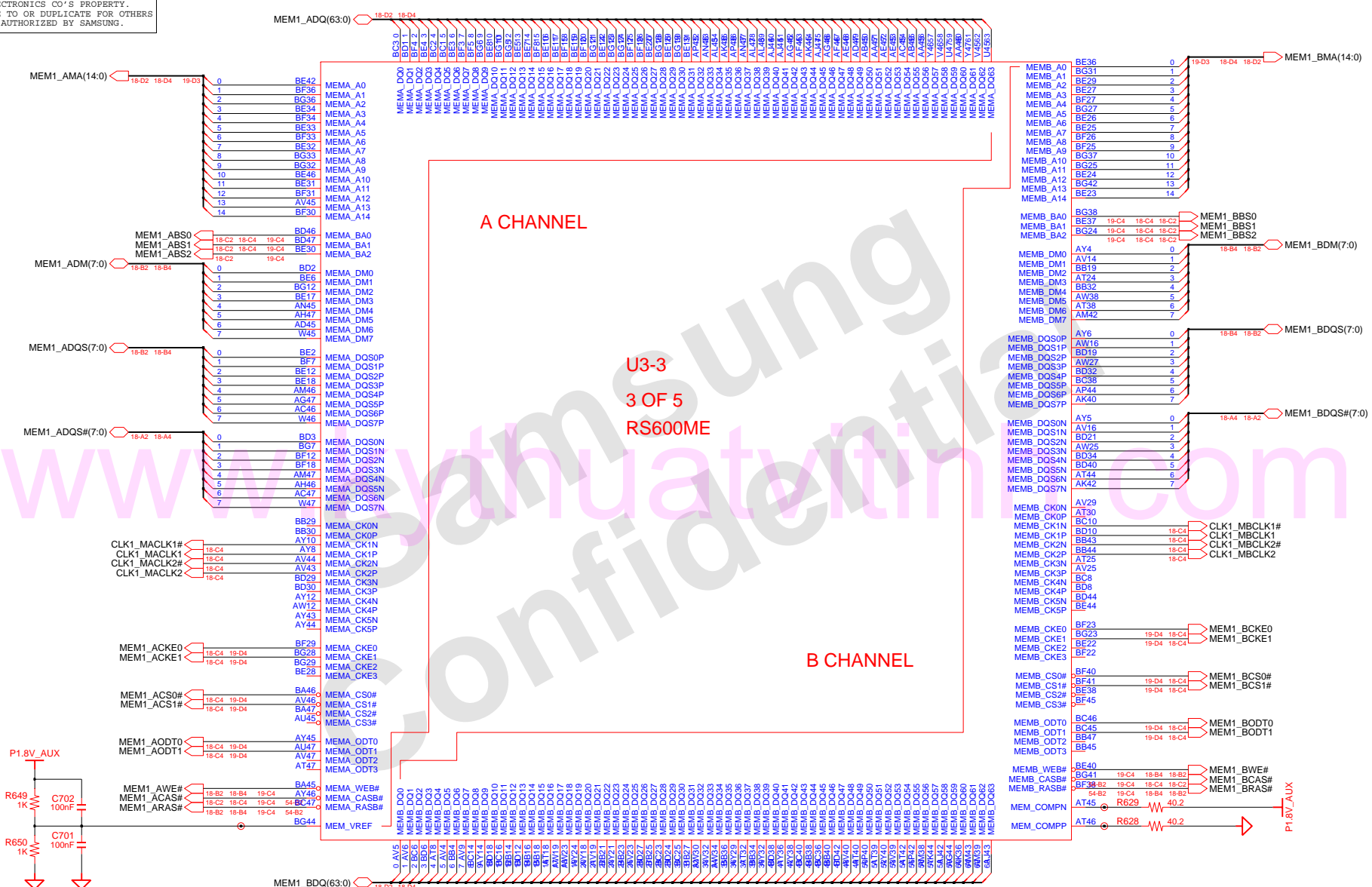
U3-2  
RS600ME  
2 OF 5



DRAW	JIANG, DS	DATE	11/2/2006	TITLE	HAINAN2 HAINAN2 RS600 (2/5)	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-XXXXXA
CHECK	YONG LEI	DEV. STEP	PV			
APPROVAL	KEVIN LEE	REV	2.0			
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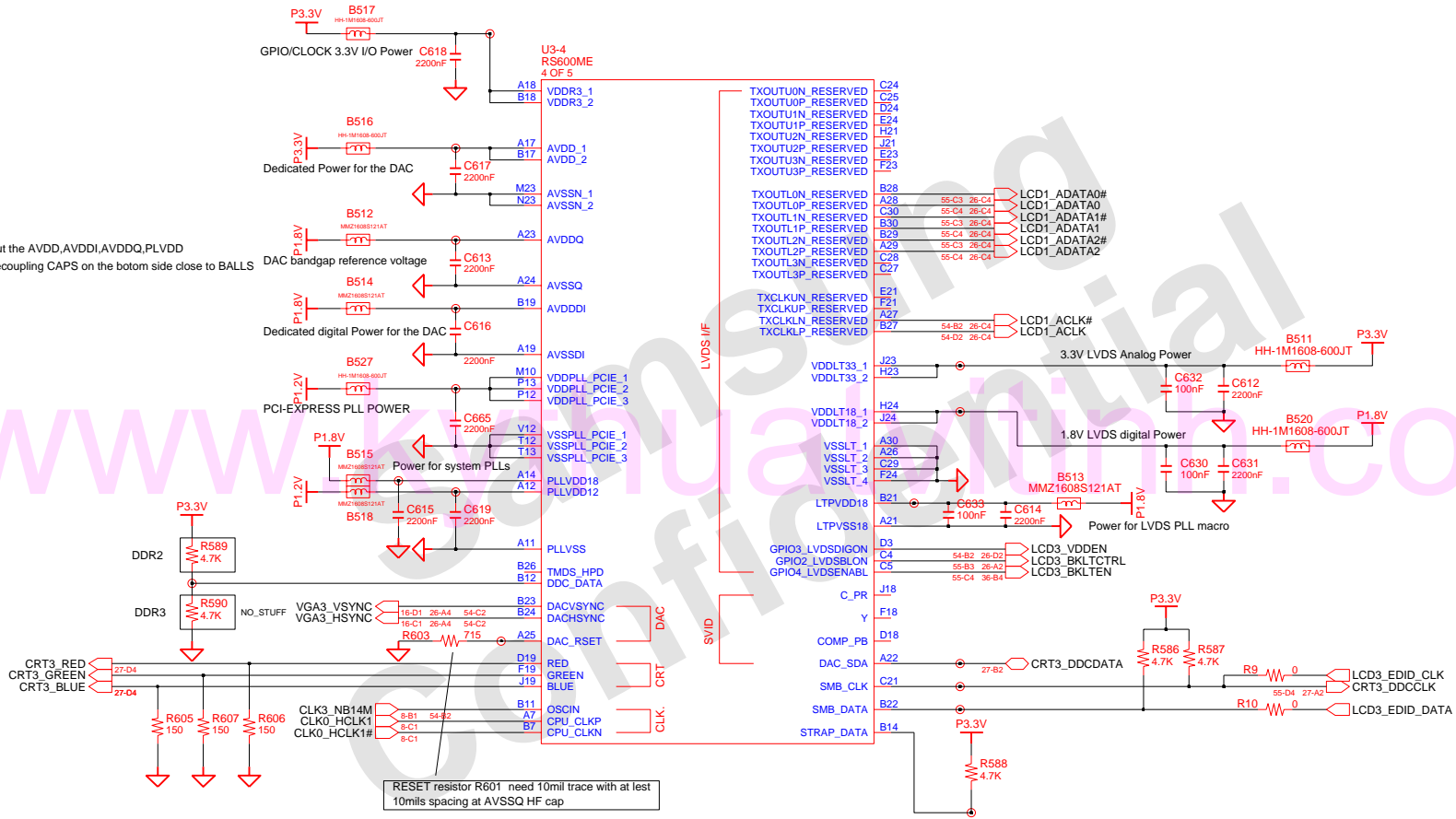


DRAW	JIANG, DS	DATE	11/2/2006	TITLE	HAINAN2	<b>SAMSUNG</b> ELECTRONICS
CHECK	YONG LEI	DEV. STEP	PV	HAINAN2	PART NO.	
APPROVAL	KEVIN LEE	REV	2.0	RS600 (3/5)	BA41-XXXXXA	
MODULE CODE		LAST EDIT	November 2, 2006 4:25:20 PM	PAGE	15	OF 48

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Put the AVDD, AVDDI, AVDDQ, PLVDD decoupling CAPS on the bottom side close to BALLS

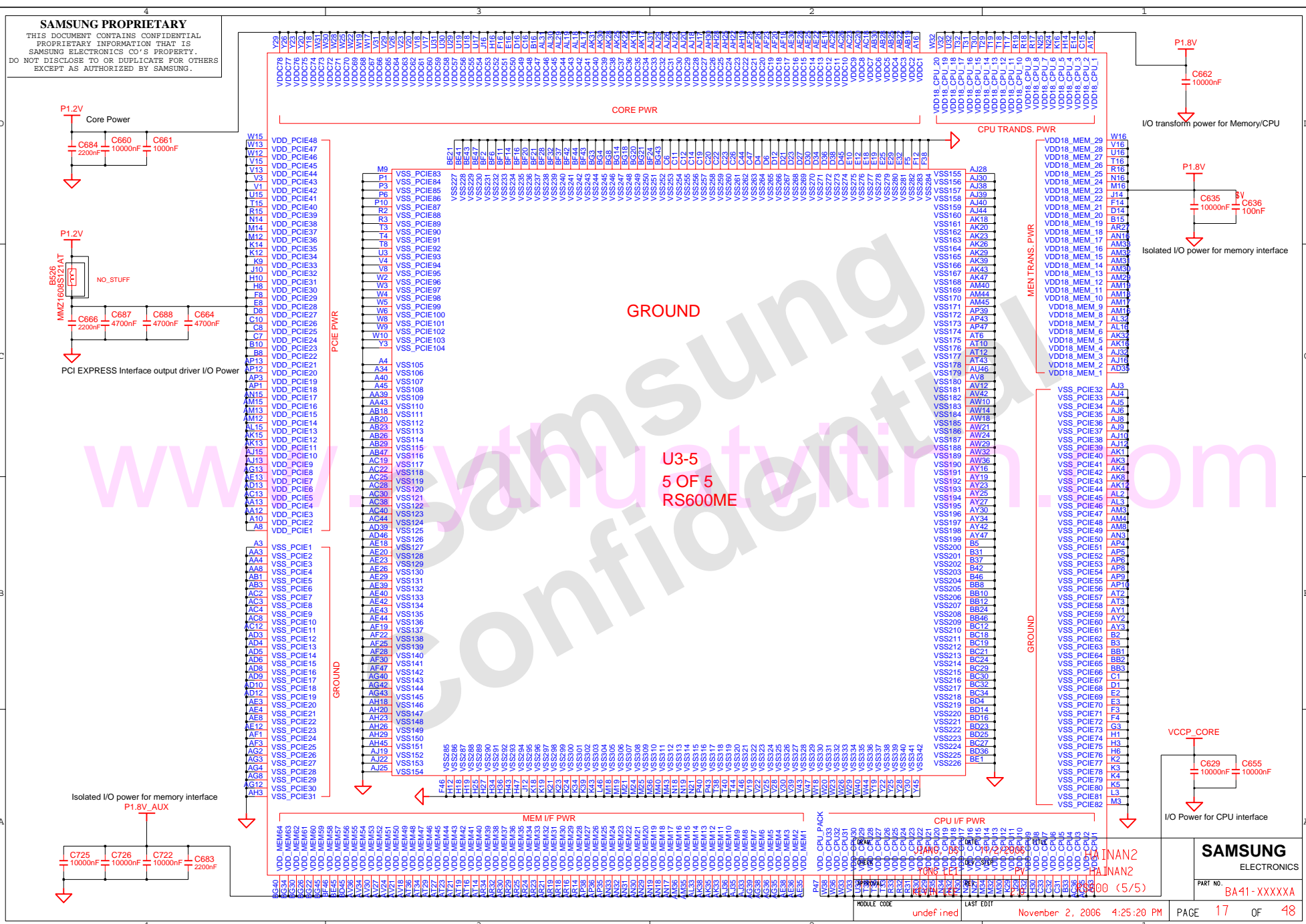


DRAW	JIANG, DS	DATE	11/2/2006	TITLE	HAINAN2	SAMSUNG ELECTRONICS
CHECK	YONG LEI	DEV. STEP	PV	HAINAN2	PART NO.	
APPROVAL	KEVIN LEE	REV	2.0	RS600 (4/5)	BA41-XXXXXA	
MODULE CODE		LAST EDIT	November 2, 2006 4:25:20 PM	PAGE	16	OF 48



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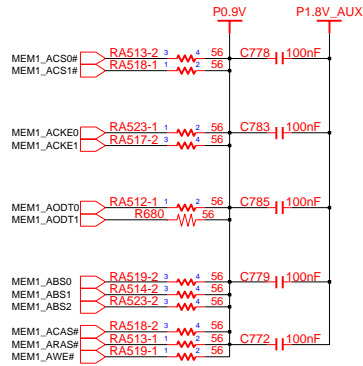
**SAMSUNG**  
ELECTRONICS  
PART NO. BA41-XXXXXA  
REV. 0000 (5/5)



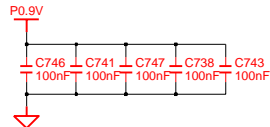
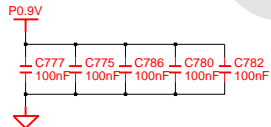
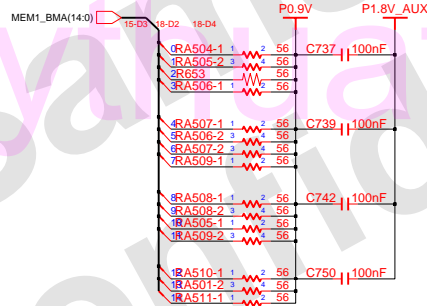
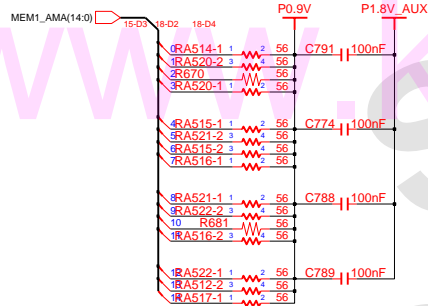
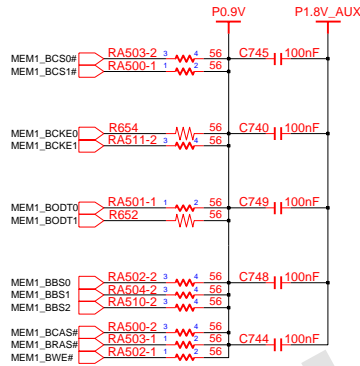
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**Channel 1**

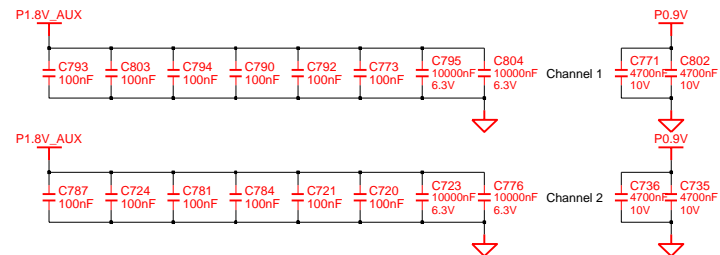
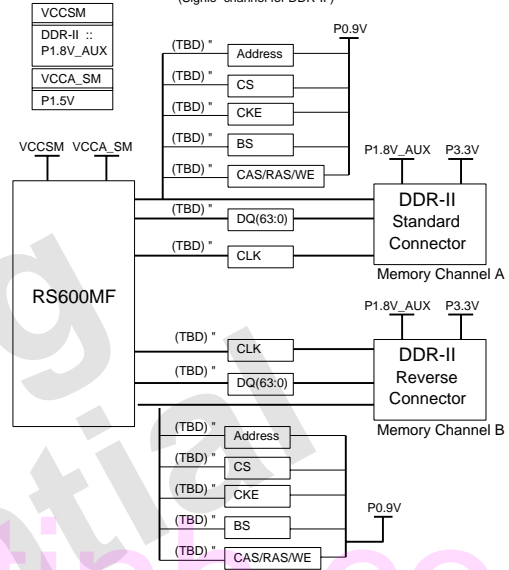


**Channel 2**



**Memory Topology**

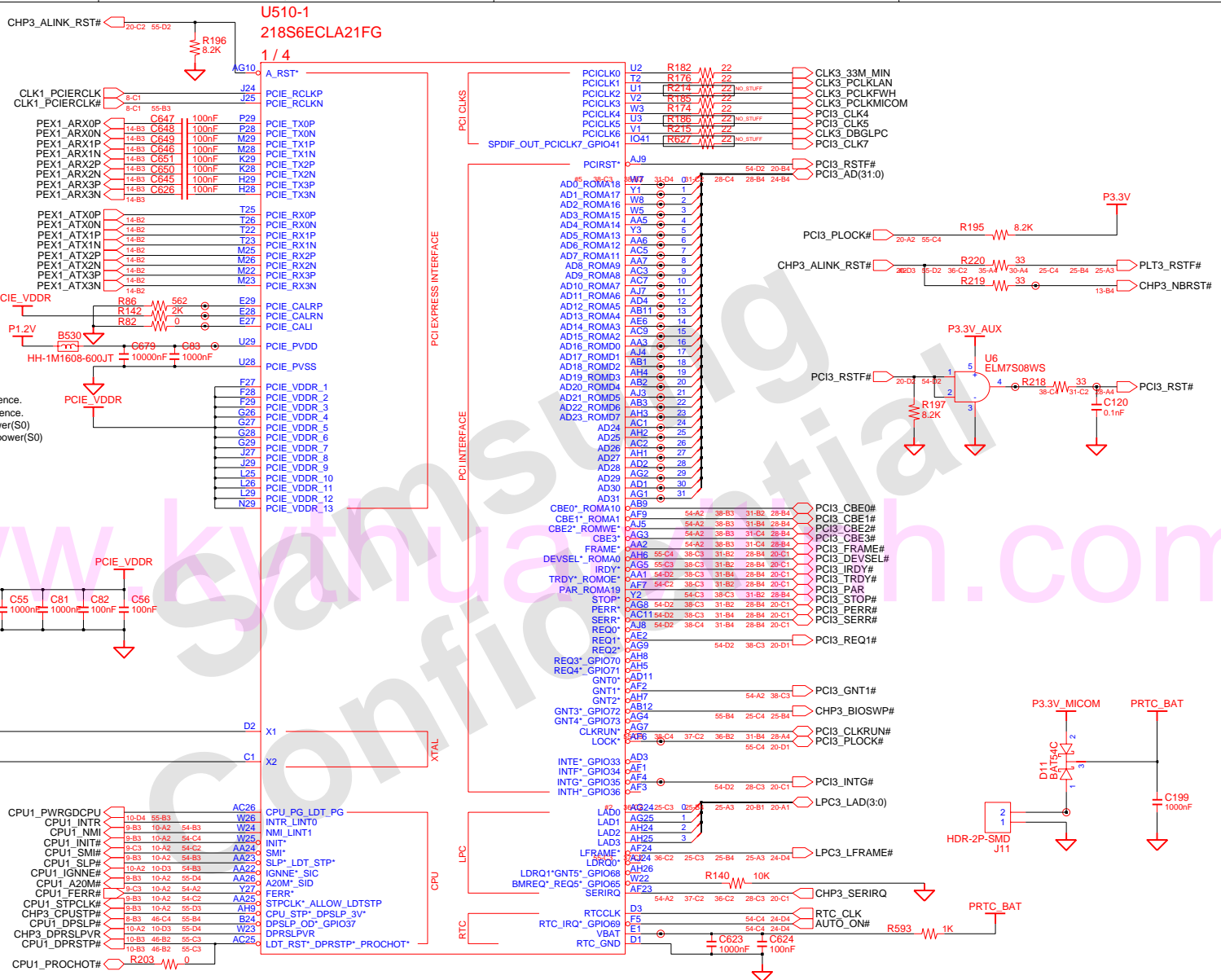
(Single channel for DDR-II)



DRAW	JIANG, DS	DATE	11/2/2006	TITLE	HAINAN2	<b>SAMSUNG</b> ELECTRONICS
CHECK	YONG LEI	DEV. STEP	PV	DDR2 TERMINATION		
APPROVAL	KEVIN LEE	REV	2.0	PART NO. BA41-XXXXXA		
MODULE CODE	undef ined	LAST EDIT	November 2, 2006 4:25:20 PM	PAGE	19	OF 48

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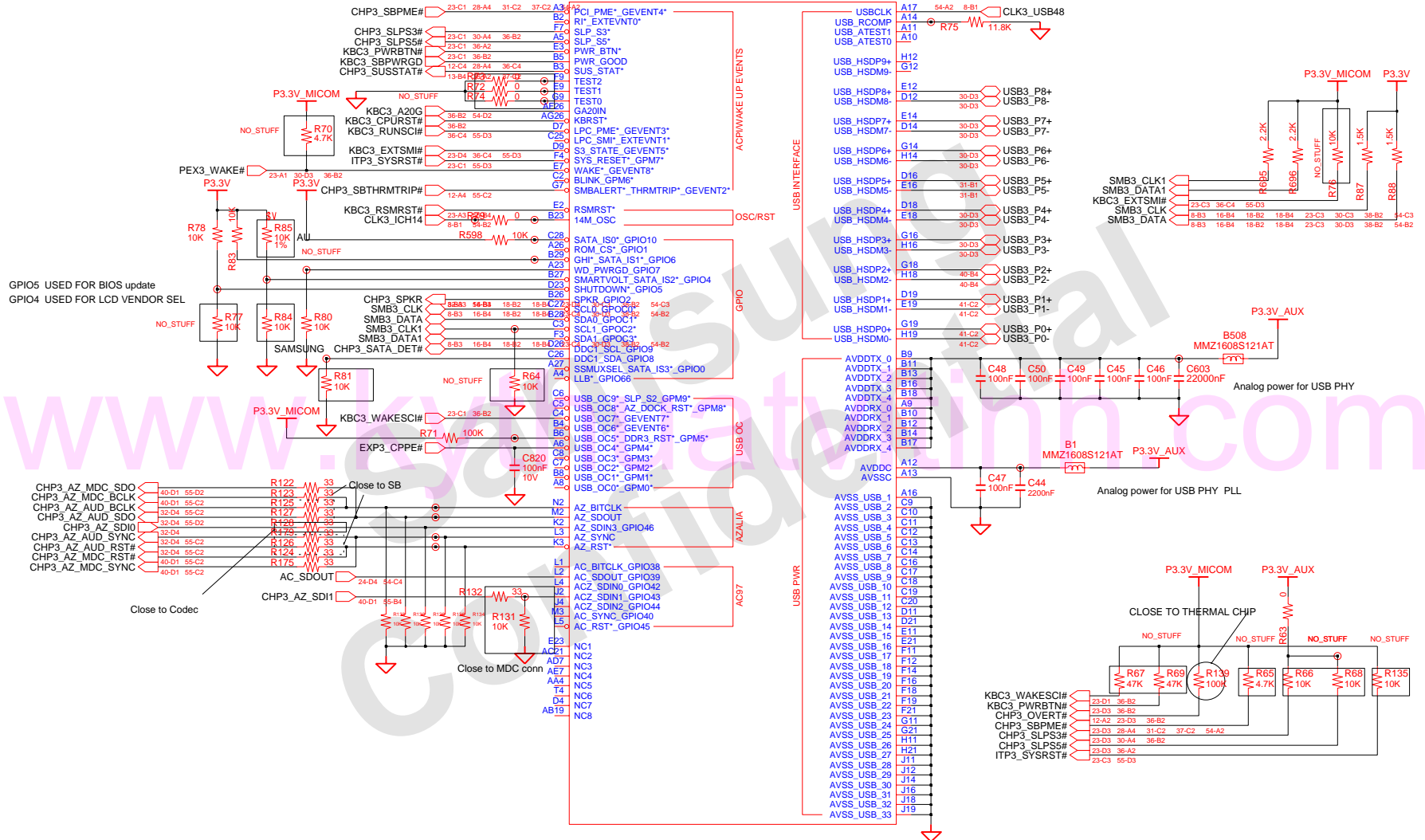
PCIE\_CALRP is TX termination reference.  
 PCIE\_CALRN is RX termination reference.  
 PCIE\_PVDD is Alink-EXP II PLL power(S0)  
 PCIE\_VDDR is Alink-EXP II analog power(S0)

DRAW	JIANG_DS	DATE	11/2/2006	TITLE	HAINAN2	<b>SAMSUNG</b> ELECTRONICS
CHECK	YONG LEI	DEV. STEP	PV			
APPROVAL	KEVIN LEE	REV	2.0		SB600(1/4)	PART NO. BA41-XXXXXA
MODULE CODE	undef ined	LAST EDIT	November 2, 2006 4:25:20 PM	PAGE	20	OF 48

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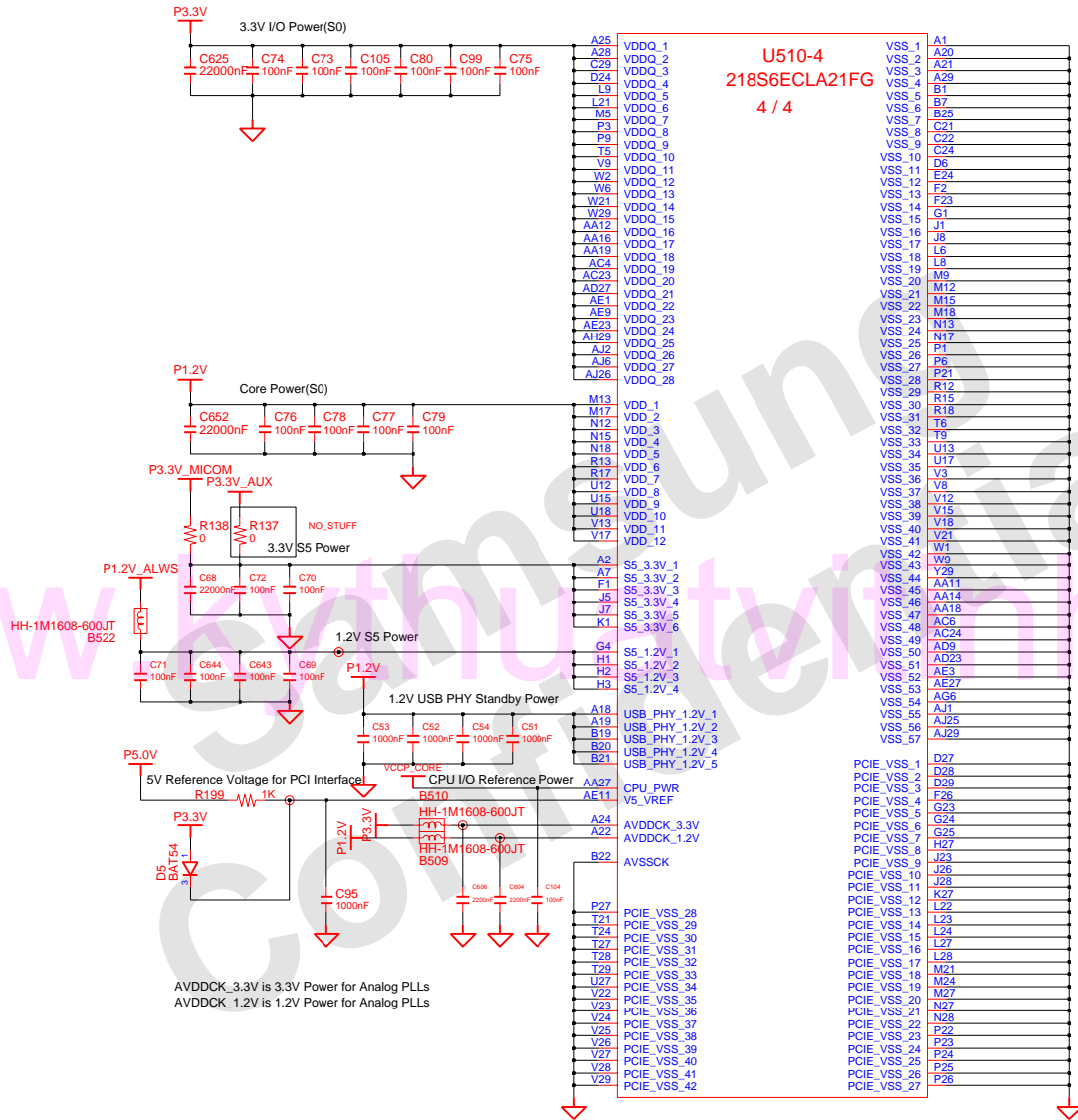
**U510-2  
218S6ECLA21FG  
2 / 4**





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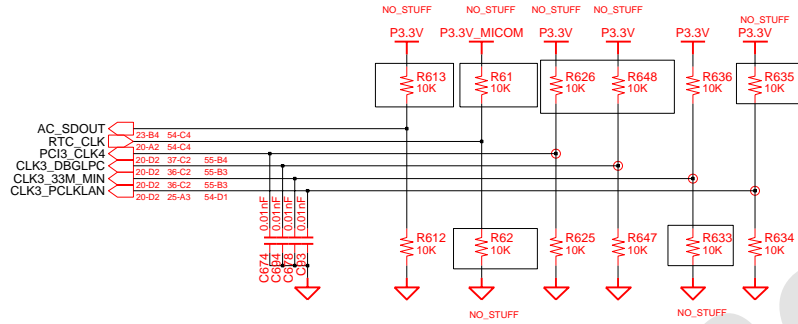


DRAW	JIANG, DS	DATE	11/2/2006	TITLE	HAINAN2	<b>SAMSUNG</b> ELECTRONICS
CHECK	YONG LEI	DEV. STEP	PV			
APPROVAL	KEVIN LEE	REV	2.0		SB600(4/4)	PART NO. BA41-XXXXXA
MODULE CODE	undef ined	LAST EDIT	November 2, 2006 4:25:20 PM	PAGE	23	OF 48

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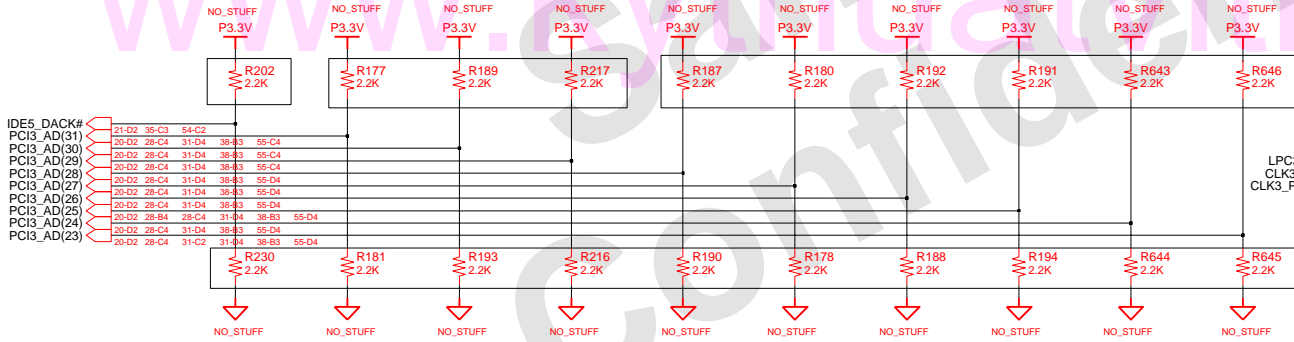
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**REQUIRED SYSTEM STRAPS**



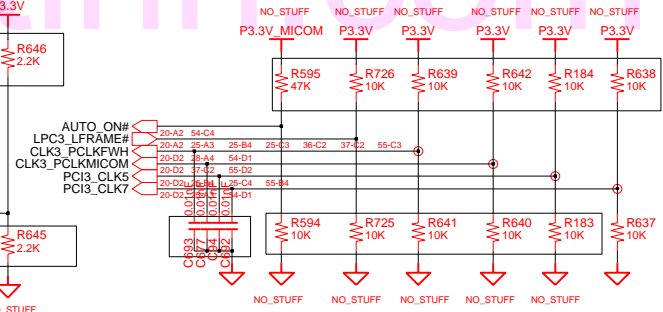
	AC_SDOUT	RTC_CLK	PCI3_CLK4	CLK3_DBG LPC	CLK3_33M_MIN, CLK3_PCLKLAN
STRAP HIGH	USE DEBUG STRAPS	INTERNAL RTC	USE INT PLL 48	CPU I/F = K8	ROM TYPE H.H = PCI ROM H.L = SPI ROM L.H = LPC ROM L.L = FWH ROM
STRAP LOW	IGNORE DEBUG STRAPS	EXRERNAL RTC	USE EXT 48MHZ	CPU I/F = P4	

**DEBUG STRAPS**



	IDE5_DACK*	PCI3_AD(31)	PCI3_AD(30)	PCI3_AD(29)	PCI3_AD(28)	PCI3_AD(27)	PCI3_AD(26)	PCI3_AD(25)	PCI3_AD(24)	PCI3_AD(23)
STRAP HIGH	RESERVED	RESERVED	RESERVED	RESERVED	USE LONG RESET	USE PCI PLL	USE ACPI BCLK	USE IDE PLL	USE DEFAULT PCIE STRAPS	BOOTF ALL TIMER DISABLED
STRAP LOW					USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	BYPASS EEPROM PCIE STRAPS	BOOTF ALL TIMER ENABLED

**RESERVED PORT DEBUG**

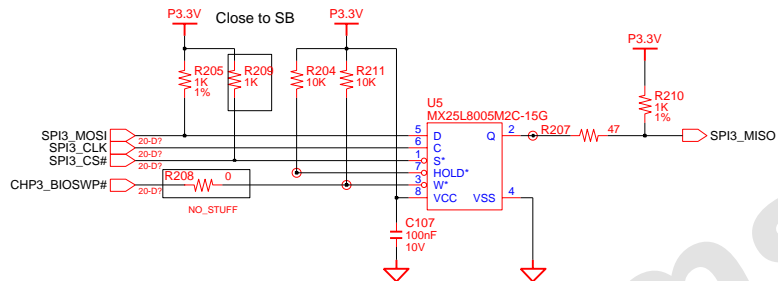


DRAW	JIANG, DS	DATE	11/2/2006	TITLE	HAINAN2	<b>SAMSUNG</b> ELECTRONICS
CHECK	YONG LEI	DEV. STEP	PV			
APPROVAL	KEVIN LEE	REV	2.0		SB600 STRAPS	PART NO. BA41-XXXXXA
MODULE CODE	undef ined	LAST EDIT	November 2, 2006 4:25:20 PM	PAGE	24	OF 48

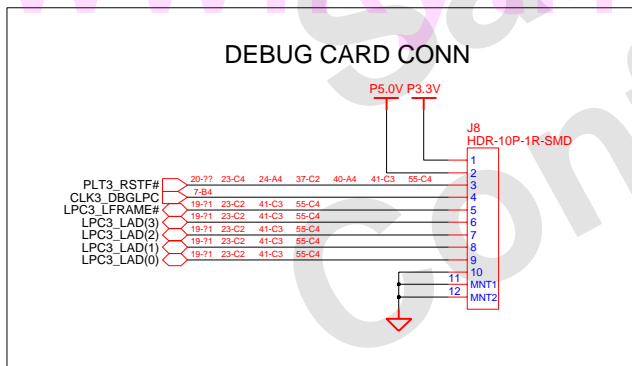


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**DEBUG CARD CONN**

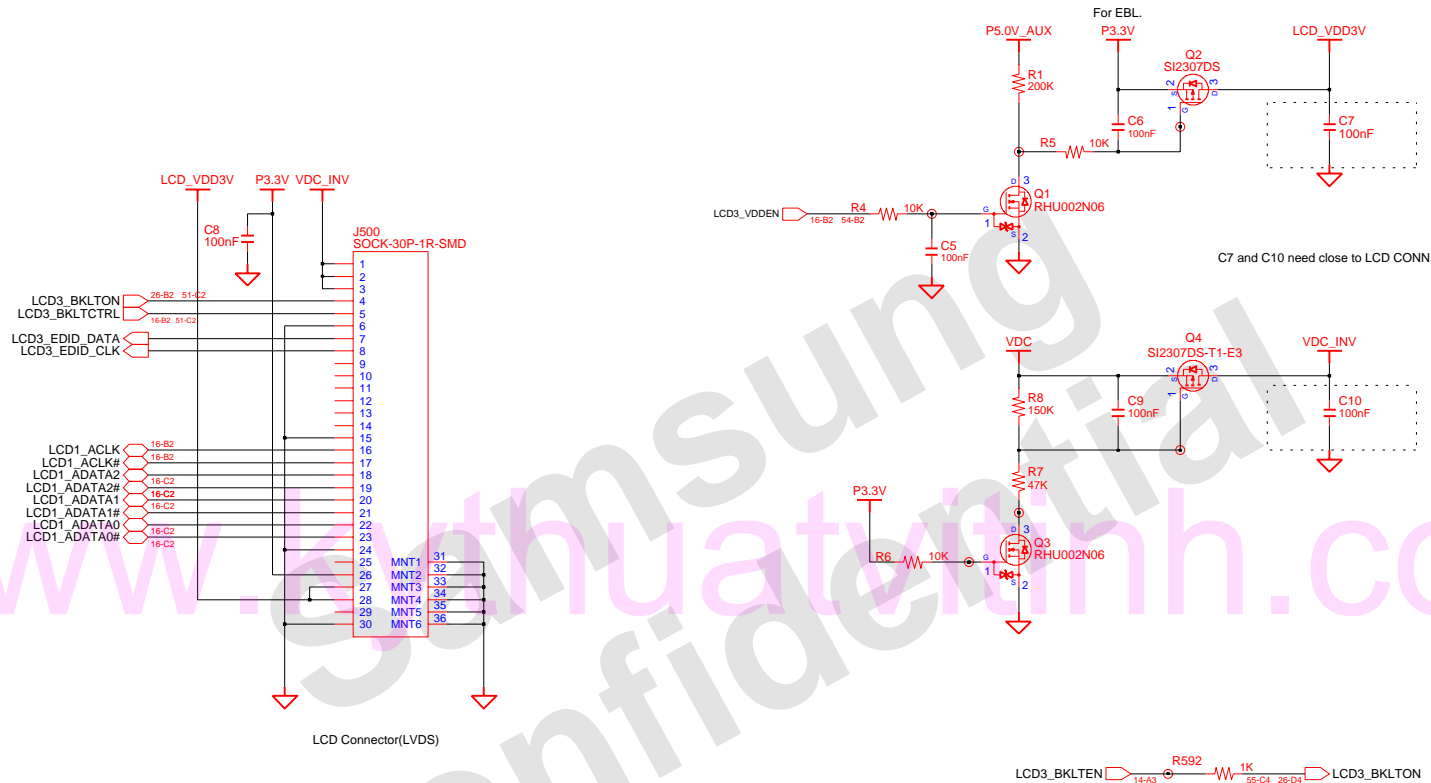


- |   |                                    |
|---|------------------------------------|
| 02 VERIFY REAL MODE                             | 66 CONFIGURE ADVANCE CACHE REG.    |
| 03 DISABLE NMI                                  | 6A DISPLAY EXTERNAL CACHE SIZE     |
| 04 GET CPU TYPE                                 | 6C DISPLAY SHADOW MESSAGE          |
| 06 INIT. SYSTEM H/W                             | 6E DISPLAY NON-DISPOSABLE SEGMENT  |
| 08 INIT. CHIPSET REG.                           | 70 DISPLAY ERROR MESSAGE           |
| 09 SET IN POST FLAG                             | 72 CHECK FOR CONFIGURATION ERROR   |
| 0A INIT CPU.REG                                 | 74 TEST REAL-TIME CLOCK            |
| 0B CPU CACHE ON                                 | 76 CHECK FOR KEYBOARD ERROR        |
| 0C INIT.CACHE TO POST                           | 7C SETUP HARDWARE INTERRUPT VECTOR |
| 0E INIT. I/O VALUE                              | 7E TEST COPROCESSER IF PRESENT     |
| 0F ENABLE THE L-BUS IDE                         | 80 DISABLE ON-BOARD I/O PORT       |
| 10 INIT. POWER MANAGER                          | 82 DETECT AND INSTALL EXT.RS232C   |
| 11 LOAD ALTERNATE REG.                          | 84 DETECT AND INSTALL EXT.PARALLEL |
| 13 PCI BUS MASTER RESET WITH INITIAL POST VALUE | 86 RE-INIT. ON-BOARD I/O PORT      |
| 14 INIT. KEYBOARD CONTROLLER                    | 88 INIT. BIOS DATA ROM             |
| 16 CHECK CHECKSUM                               | 8A INIT.EXTENDED BIOS DATA AREA    |
| 18 8254 TIMER INIT.                             | 8C INIT. FDD CONTROLLER            |
| 1A 8237 DMA CONTROLLER INIT.                    | 9A SHADOW OPTION ROMS              |
| 1C RESET INTERRUPT CONTROLLER                   | 9C SETUP POWER MANAGEMENT          |
| 20 TEST DRAM REFRESH                            | 9E ENABLE H/W INTERRUPT            |
| 22 TEST 8742 KEYBOARD CONTROLLER                | A0 SET TIME OF DAY                 |
| 24 SET ES SEGMENT REG. TO 4GB                   | A4 INIT. TYPOMATIC RATE            |
| 26 ENABLE A20                                   | A8 ERASE F2 PROMPT                 |
| 28 AUTO SIZING DRAM                             | AA SCAN FOR F2 KEY STROKE          |
| 32 COMPUTE THE CPU SPEED                        | AC ENTER SETUP                     |
| 34 TESET CMOS RAM                               | AE CLEAR IN POST FLAG              |
| 38 SHADOW SYSTEM BIOS ROM                       | B0 CHECK FOR ERRORS                |
| 3A AUTO SIZING CACHE                            | B2 POST DONE-PREPARE TO BOOT O/S   |
| 3C CONFIGURE ADVANCED CHIPSET REG.              | B4 ONE BEEP                        |
| 3D LOAD ALTER REG. WITH CMOS VALUE              | B6 CHECK PASSWORD (OPTION)         |
| 42 INIT. INTERRUPT VECTOR                       | B7 ACPI INIT                       |
| 44 INIT. BIOS INTERRUPT                         | BA DMI INIT                        |
| 46 CHECK ROM COPYRIGHT NOTICE                   | BE CLEAR SCREEN                    |
| 47 INIT. I20 SUPPORT IF INSTALLED               | C0 TRY BOOT WITH INT19             |
| 48 CHECK VIDEO CONFIGURE AGAINST CMOS           | D0 INTERRUPT HANDLER ERROR         |
| 49 INIT. PCI BUS AND DEVICE                     | D2 UNKNOWN INTERRUPT ERROR         |
| 4A INIT. ALL VIDEO BIOS ROM                     | D4 PENDING INTERRUPT ERROR         |
| 4C SHADOW VIDEO BIOS ROM                        | D6 SHUTDOWN 5                      |
| 50 DISPLAY CPU TYPE AND SPEED                   | D8 SHUTDOWN ERROR                  |
| 52 TEST KEYBOARD                                | DA EXTENDED BLOCK MOVE             |
| 54 SET KEYCLICK IF ENABLED                      | DC SHUTDOWN 10                     |
| 56 ENABLE KEYBOARD                              | DD ENABLE NMI                      |
| 58 TEST FOR UNEXPECTED INTERRUPTS               | DE INIT. HDD CONTROLLER            |
| 5A DISPLAY " PRESS ..... SETUP"                 | DF INIT. LOCAL BUS HDD CONTROLLER  |
| 5C TEST RAM BETWEEN 512K AND 640K               | E0 JUMP TO USER PATCH 2            |
| 60 TEST EXTENDED MEMORY                         | E2 DISABLE A20 ADDRESS LINE        |
| 62 TEST EXTENDED MEMORY ADDRESS LINE            | E4 CLEAR HUGE ES SEGMENT REG.      |
| 64 JUMP TO USER PATCH 1                         | E6 SEARCH FOR OPTION ROMS          |

DRAW	JIANG, DS	DATE	11/2/2006	TITLE	HAINAN2	<b>SAMSUNG</b> ELECTRONICS
CHECK	YONG LEI	DEV. STEP	PV			
APPROVAL	KEVIN LEE	REV	2.0		FWH	PART NO. BA41-XXXXXA
MODULE CODE	undef ined	LAST EDIT	November 2, 2006 4:25:20 PM	PAGE	25	OF 48

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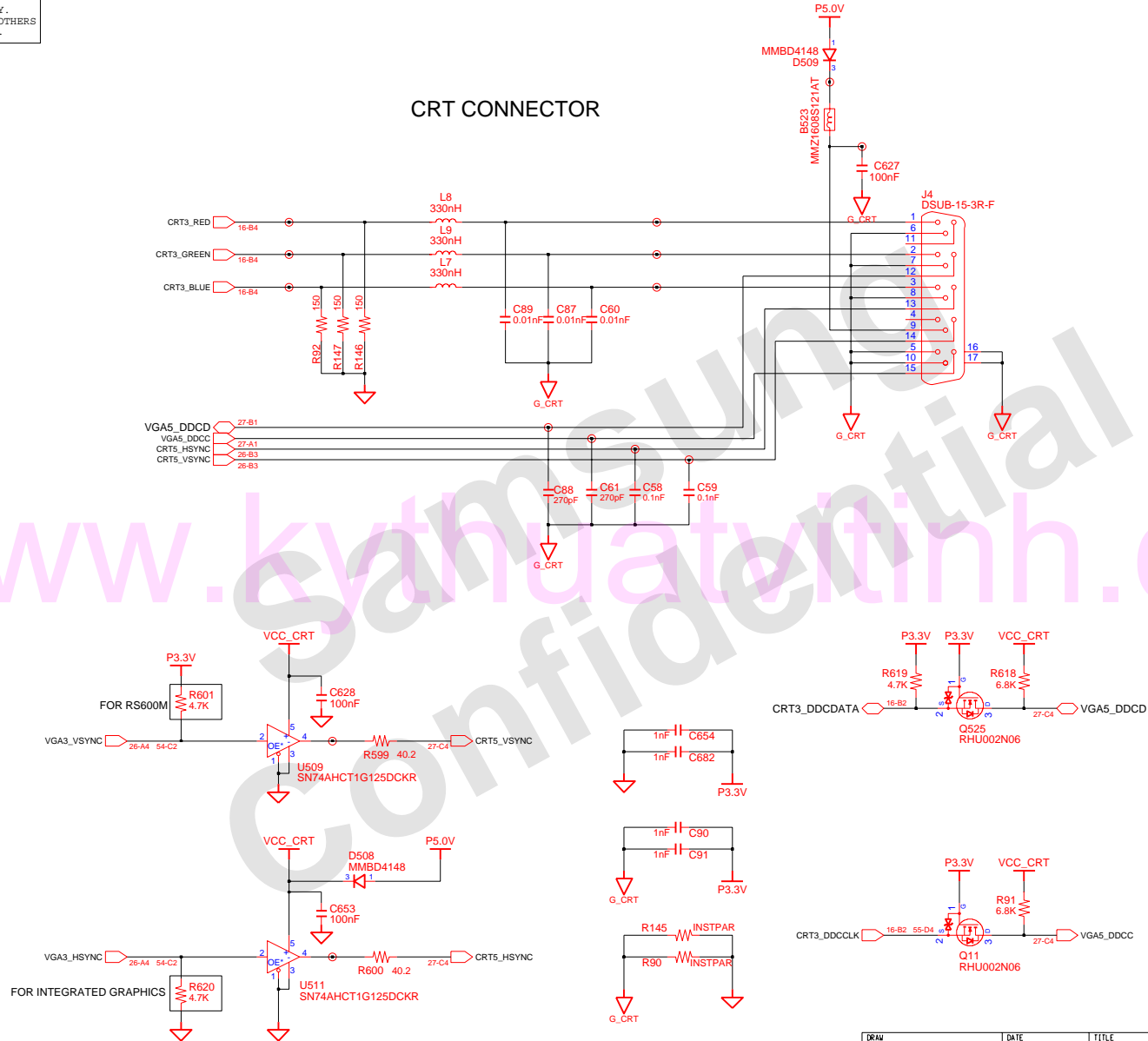


DRAW	JIANG, DS	DATE	11/2/2006	TITLE	HAINAN2	<b>SAMSUNG</b> ELECTRONICS
CHECK	YONG LEI	DEV. STEP	PV			
APPROVAL	KEVIN LEE	REV	2.0		LCD	PART NO. BA41-XXXXXA
MODULE CODE	undef ined	LAST EDIT	November 2, 2006 4:25:20 PM	PAGE	26	OF 48

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**CRT CONNECTOR**

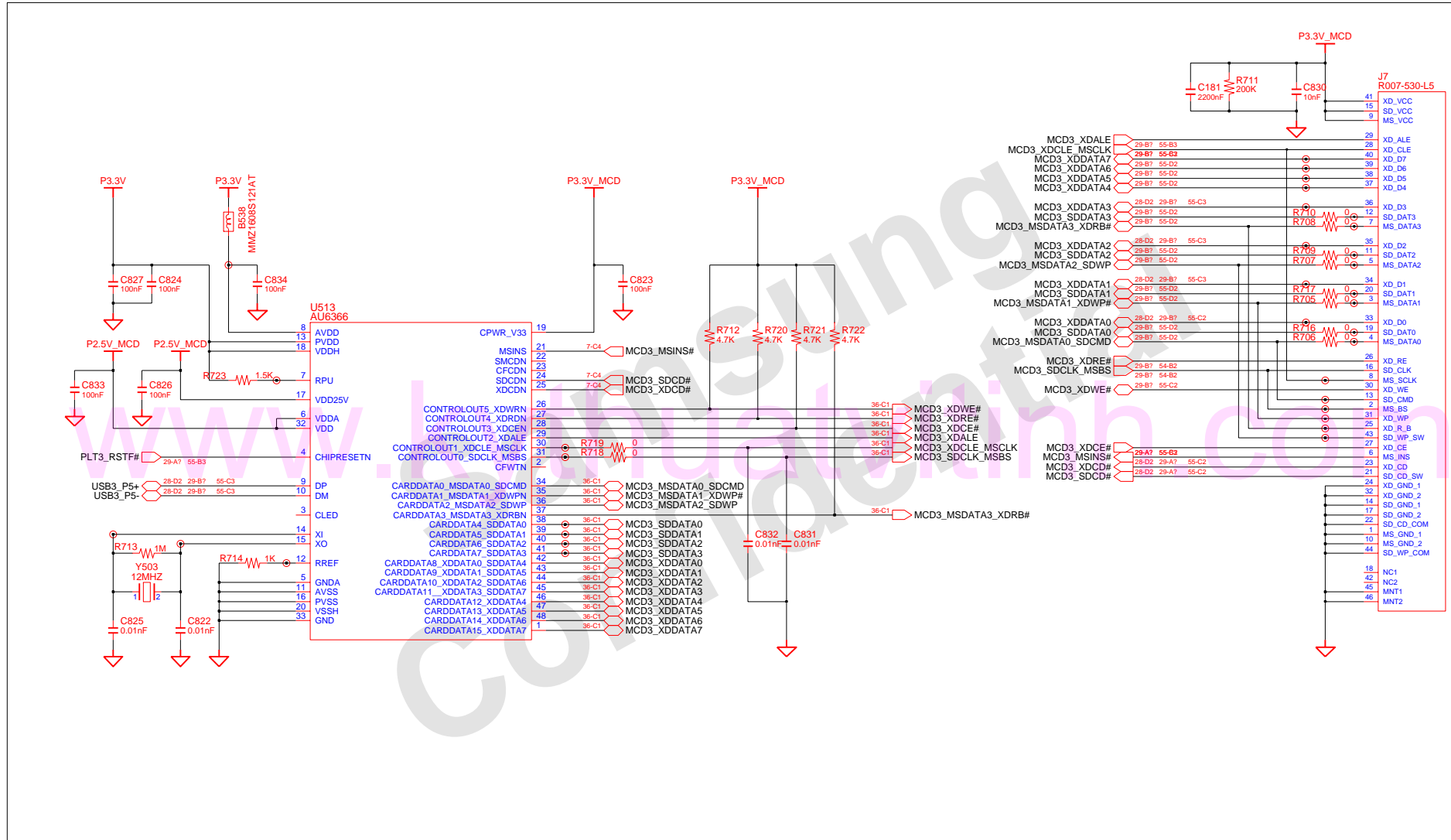


DRAW	JIANG, DS	DATE	11/2/2006	TITLE	HAINAN2	<b>SAMSUNG</b> ELECTRONICS
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APPROVAL	KEVIN LEE	REV	2.0		CRT	PART NO. BA41-XXXXXA
MODULE CODE	undef ined	LAST EDIT	November 2, 2006 4:25:20 PM	PAGE	27	OF 48

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**4 IN 1 CARD**

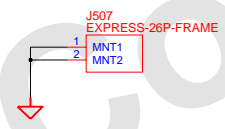
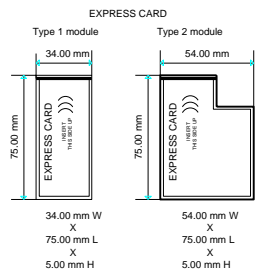
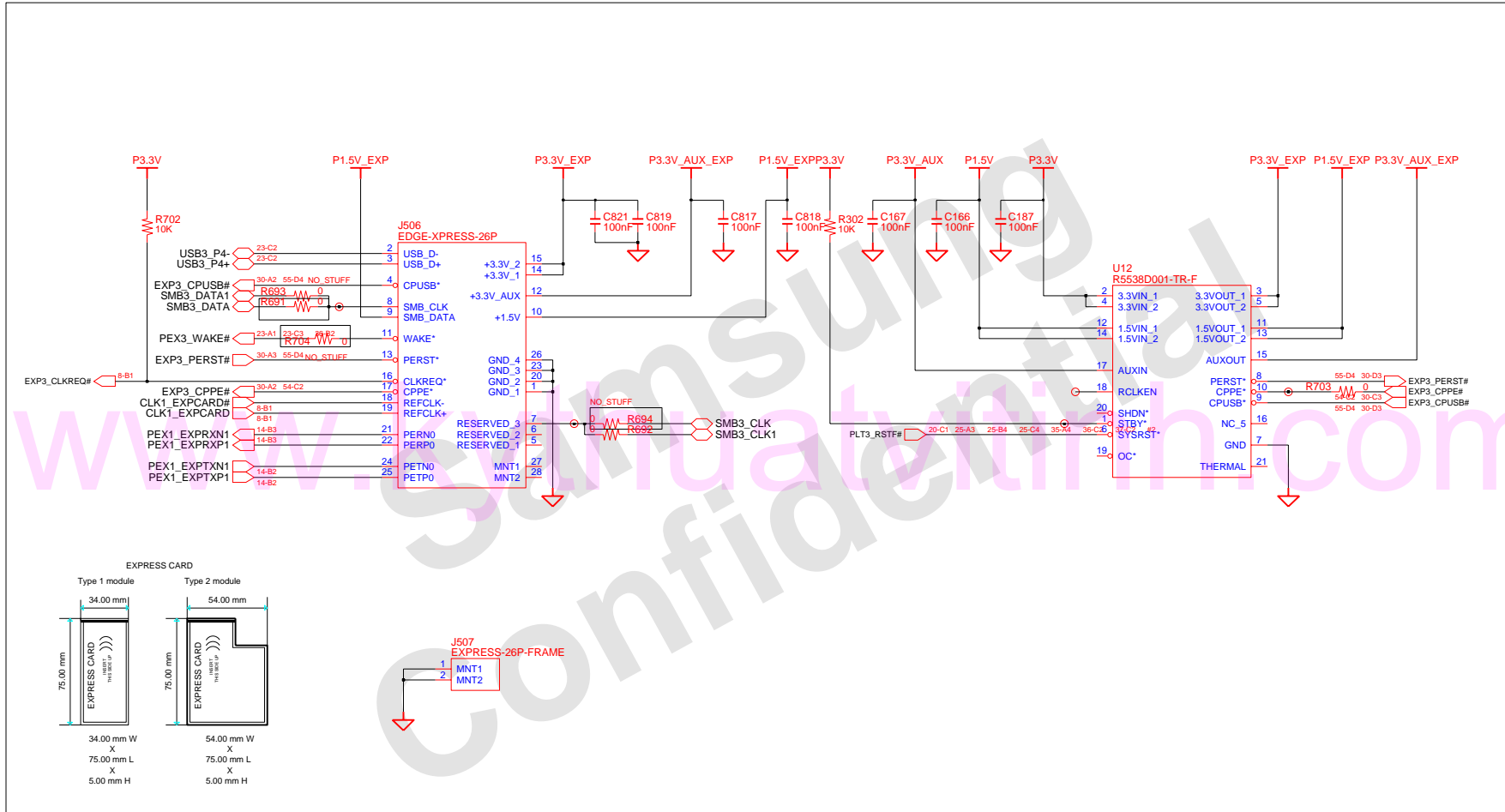


DRAW	JIANG, DS	DATE	11/2/2006	TITLE	HAINAN2	<b>SAMSUNG</b> ELECTRONICS
CHECK	YONG LEI	DEV. STEP	PV			
APPROVAL	KEVIN LEE	REV	2.0		4 IN 1 CARD	PART NO. BA41-XXXXXA
MODULE CODE	undef ined	LAST EDIT	November 2, 2006 4:25:20 PM	PAGE	28	OF 48

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**EXPCARD**



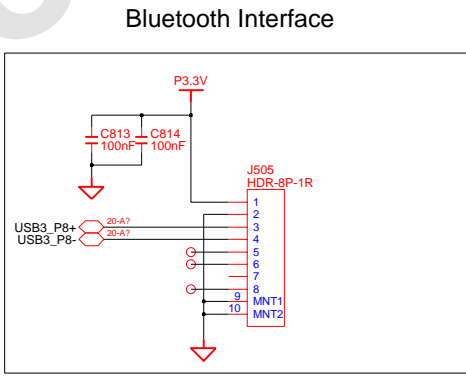
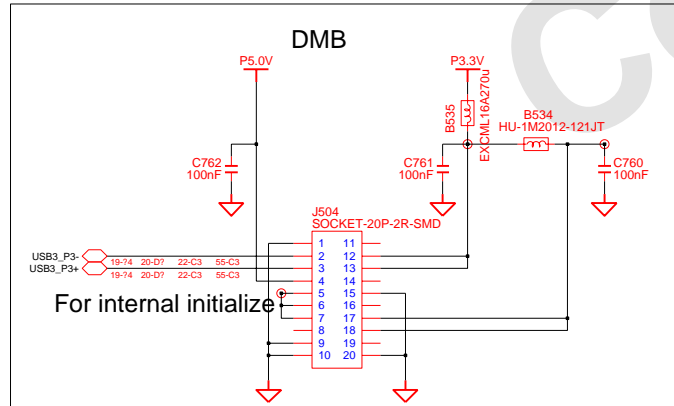
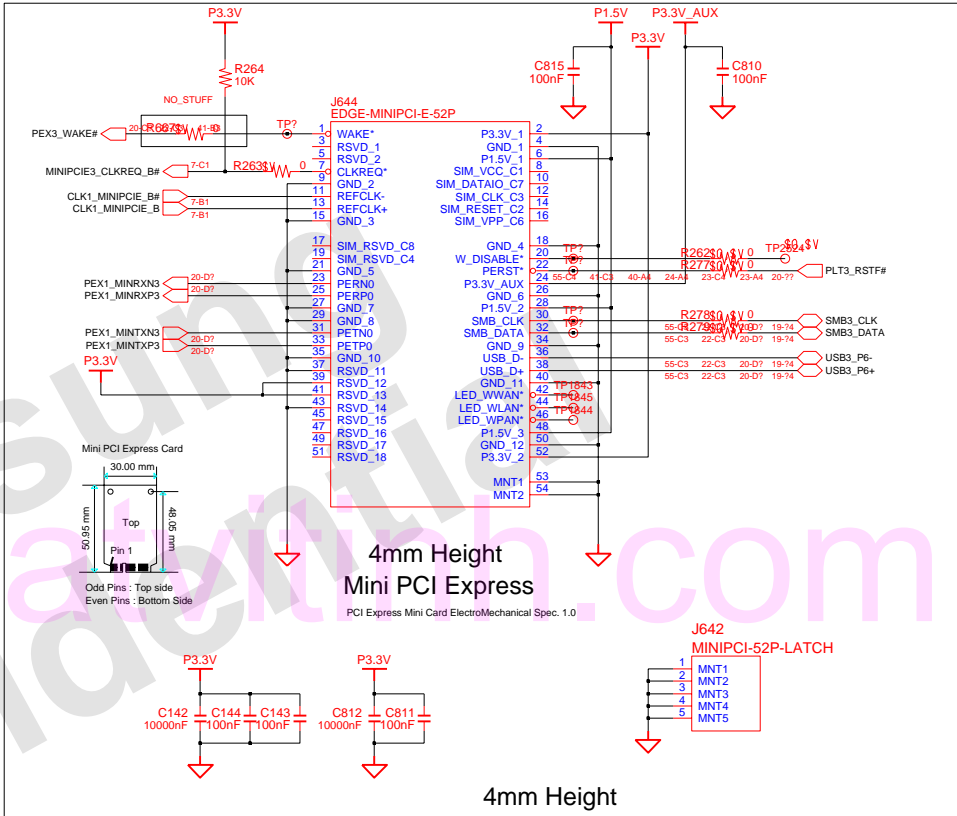
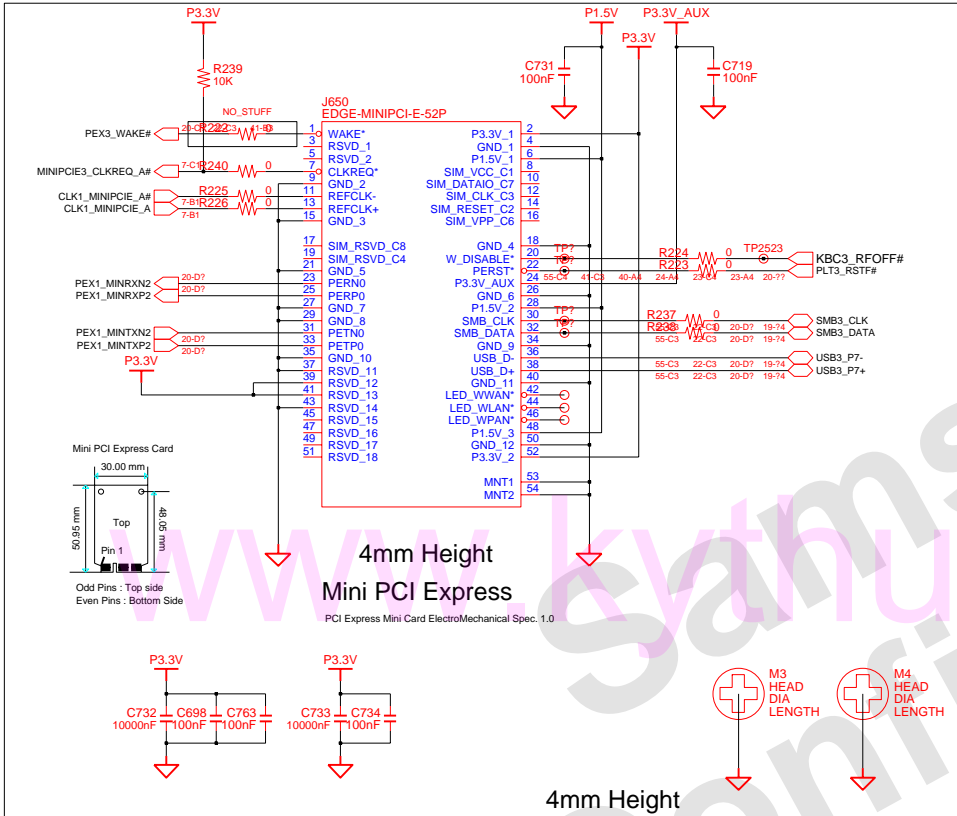
DRAW	JIANG, DS	DATE	11/2/2006	TITLE	HAINAN2	<b>SAMSUNG</b> ELECTRONICS
CHECK	YONG LEI	DEV. STEP	PV			
APPROVAL	KEVIN LEE	REV	2.0		EXPRESS CARD	PART NO. BA41-XXXXXA
MODULE CODE	undef ined	LAST EDIT	November 2, 2006 4:25:20 PM	PAGE	29	OF 48

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**MINICARD**

**DVB-T**



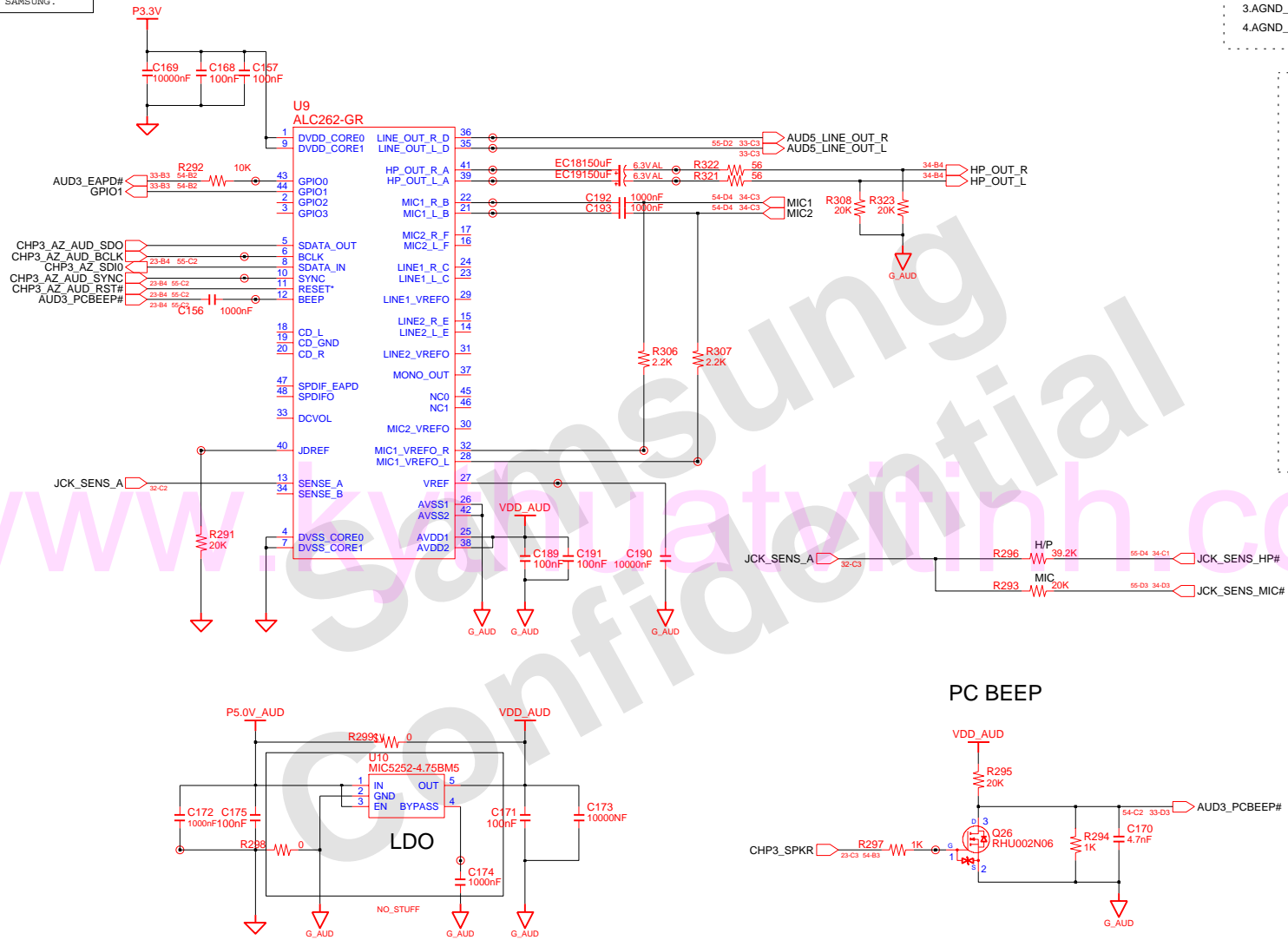
DRAW	JIANG, DS	DATE	11/2/2006	TITLE	HAINAN2 HAINAN2 MINI CARD	<b>SAMSUNG</b> ELECTRONICS
CHECK	YONG LEI	DEV. STEP	PV		PART NO.	
APPROVAL	KEVIN LEE	REV	2.0		BA41-XXXXXA	
MODULE CODE	undef ined	LAST EDIT	November 2, 2006 4:25:20 PM	PAGE	30	OF 48

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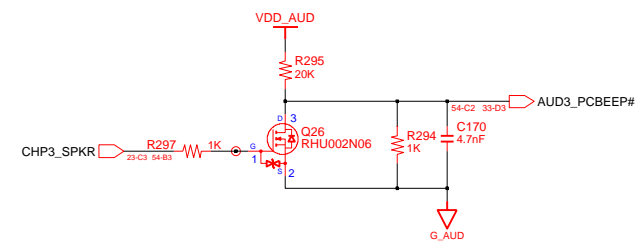
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- 1.AGND\_AUD IS AUDIO GROUND
- 2. GND IS DIGITAL GROUND
- 3.AGND\_MIC IS MIC GROUND
- 4.AGND\_CHS IS CHASSIS GROUND

ALL TYPE IS 1608



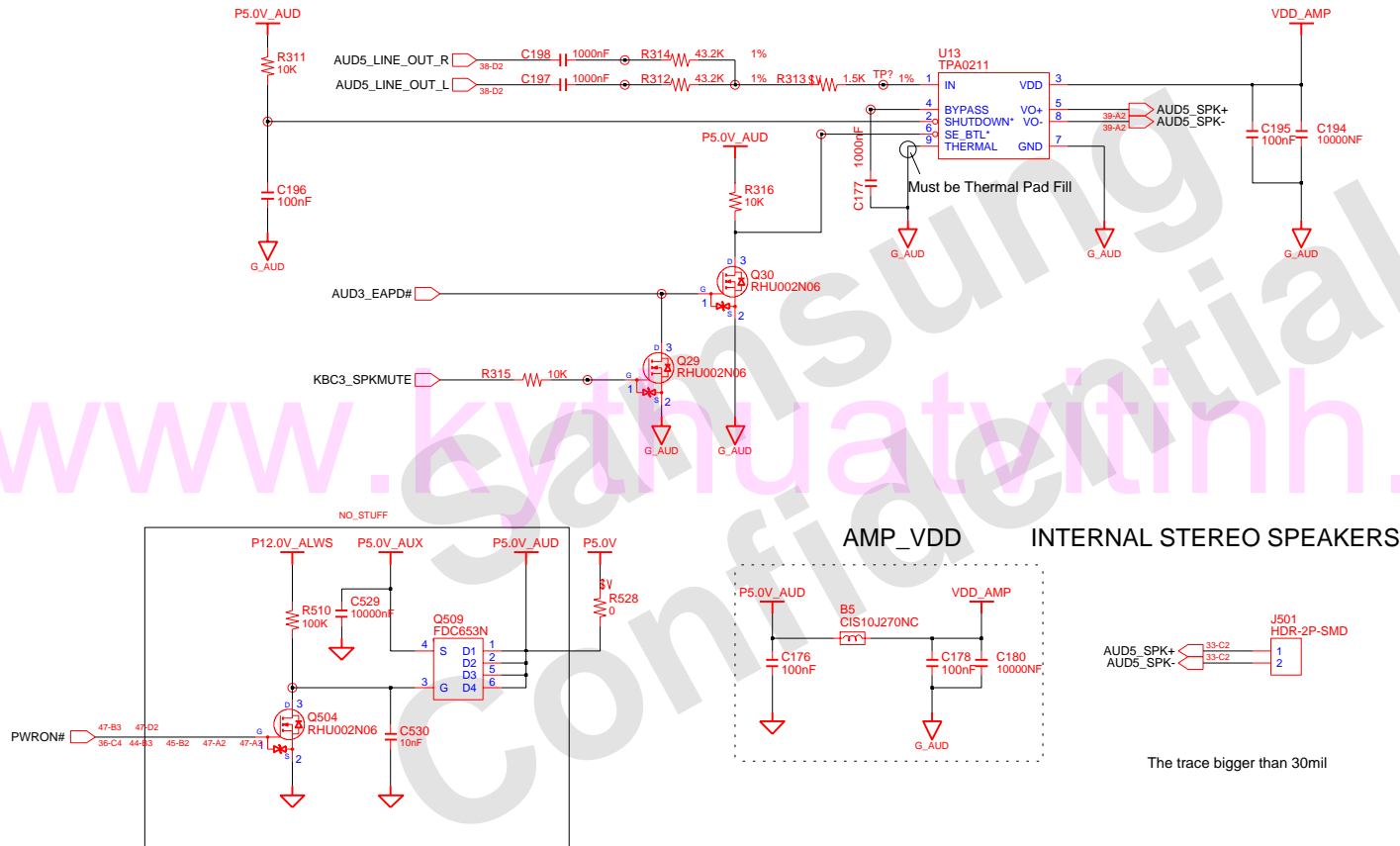
**PC BEEP**



DRAW	JIANG, DS	DATE	11/2/2006	TITLE	HAINAN2	<b>SAMSUNG</b> ELECTRONICS
CHECK	YONG LEI	DEV. STEP	PV			
APPROVAL	KEVIN LEE	REV	2.0		AUDIO(1/3)	PART NO. BA41-XXXXXA
MODULE CODE	undef ined	LAST EDIT	November 2, 2006 4:25:20 PM	PAGE	31	OF 48

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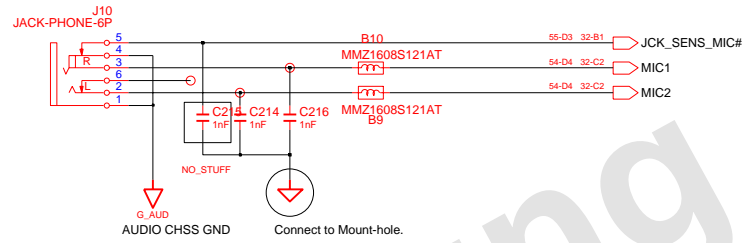
DRAW	JIANG, DS	DATE	11/2/2006	TITLE	HAINAN2	<b>SAMSUNG</b> ELECTRONICS
CHECK	YONG LEI	DEV. STEP	PV			
APPROVAL	KEVIN LEE	REV	2.0		AUDIO<2/3>	PART NO. BA41-XXXXXA
MODULE CODE	undef ined	LAST EDIT	November 2, 2006 4:25:20 PM	PAGE	32	OF 48



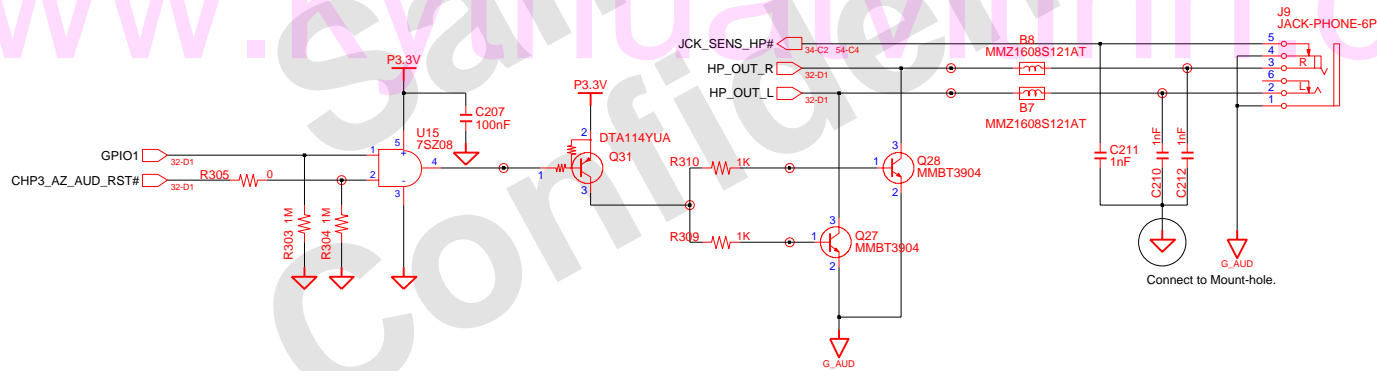
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**MIC JACK**



**HEADPHONE**



The traces led to Audio Jacks have the width over 10mil

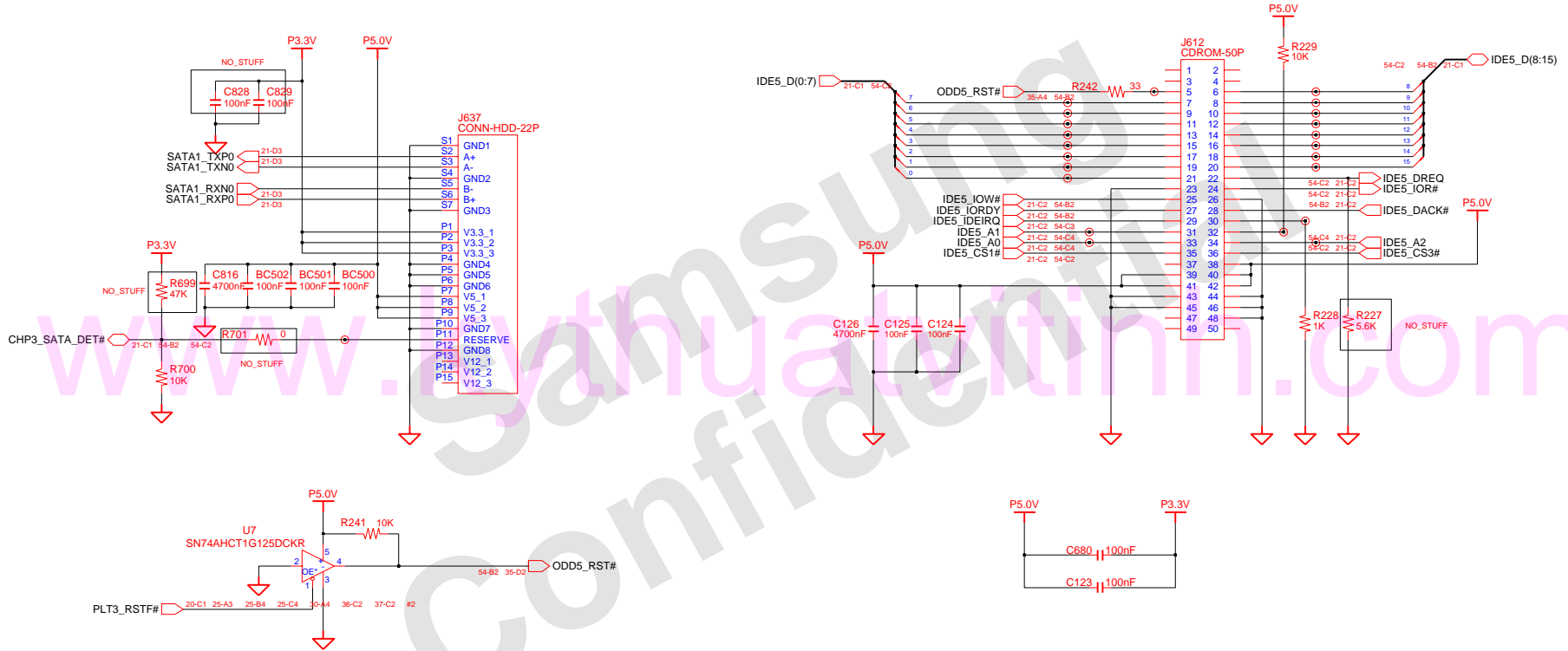
DRAW	JIANG, DS	DATE	11/2/2006	TITLE	HAINAN2	<b>SAMSUNG</b> ELECTRONICS
CHECK	YONG LEI	DEV. STEP	PV			
APPROVAL	KEVIN LEE	REV	2.0		AUDIO(3/3)	PART NO. BA41-XXXXXA
MODULE CODE	undef ined	LAST EDIT	November 2, 2006 4:25:20 PM	PAGE	33	OF 48

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**Main to HDD**

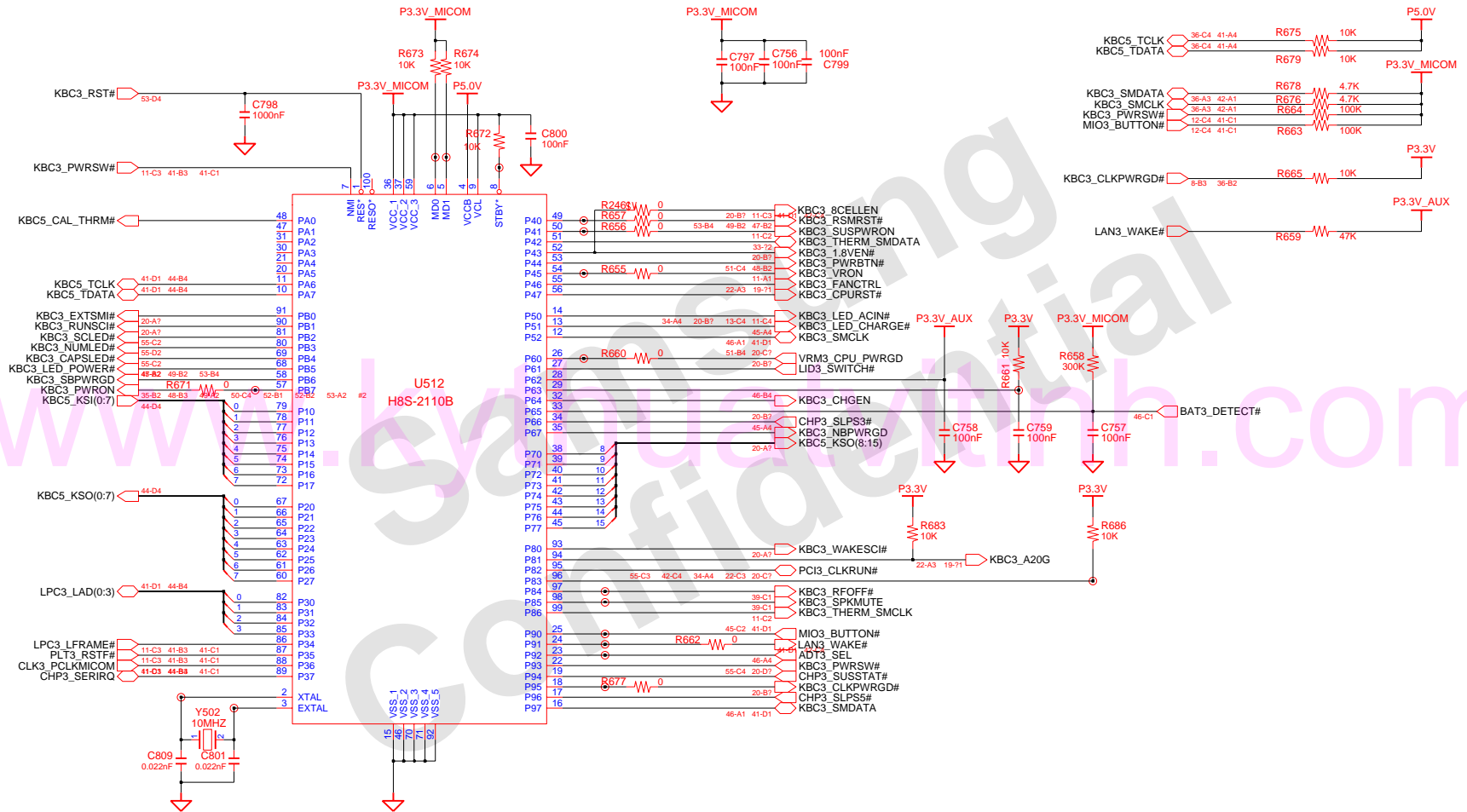
**Main to ODD**



DRAW	JIANG, DS	DATE	11/2/2006	TITLE	HAINAN2	<b>SAMSUNG</b> ELECTRONICS
CHECK	YONG LEI	DEV. STEP	PV			
APPROVAL	KEVIN LEE	REV	2.0		HDD & ODD	PART NO. BA41-XXXXXA
MODULE CODE	undef ined	LAST EDIT	November 2, 2006 4:25:20 PM	PAGE	34	OF 48

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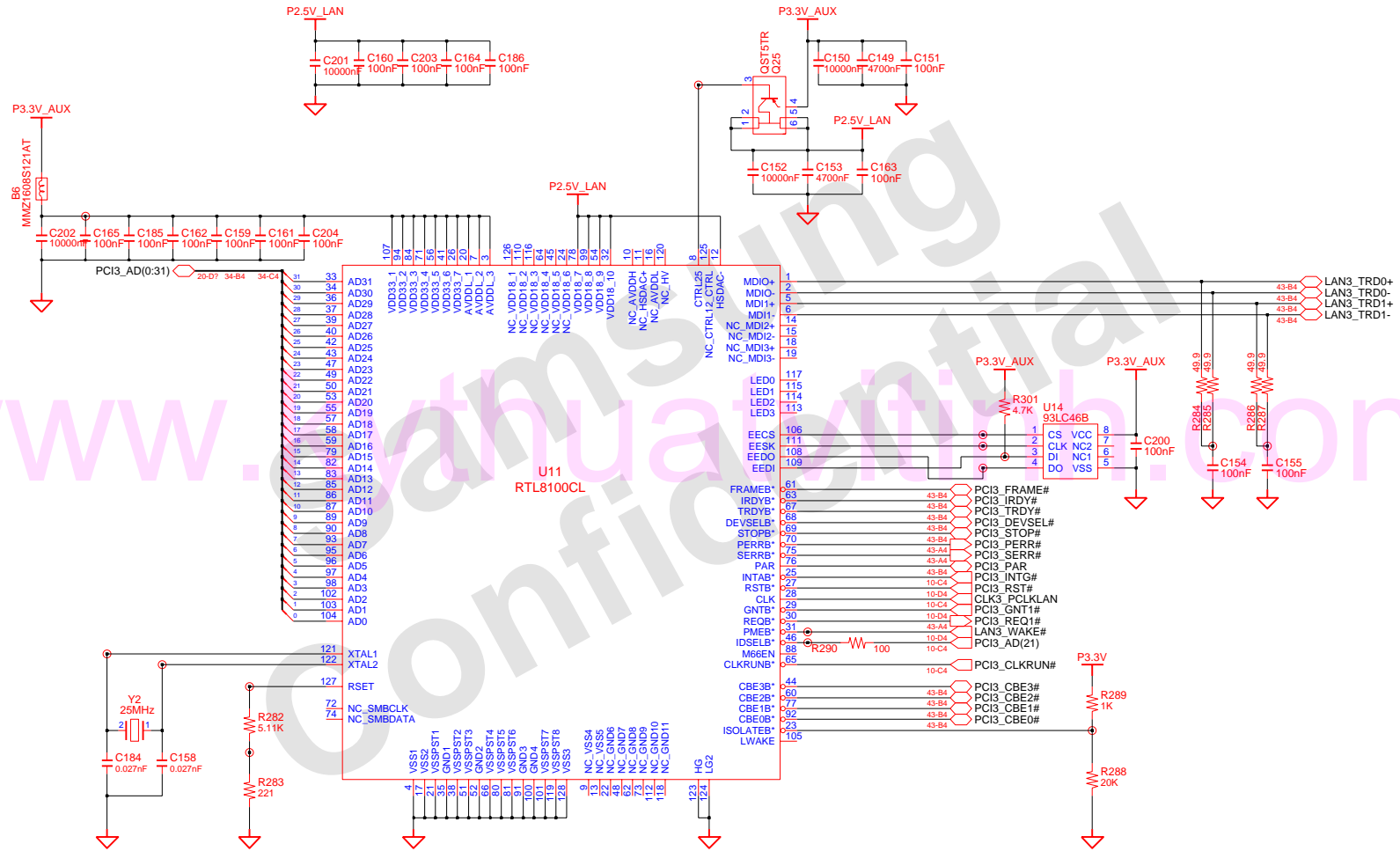
TP FOR UPDATE MICOM:  
P84=>TXD;P85=>RXD  
MD0 and MD1 =>GND  
P90,P91,P92=>VCC

DRAW	JIANG, DS	DATE	11/2/2006	TITLE	HAINAN2	SAMSUNG ELECTRONICS
CHECK	YONG LEI	DEV. STEP	PV			
APPROVAL	KEVIN LEE	REV	2.0		MICOM	PART NO. BA41-XXXXXA
MODULE CODE	undef ined	LAST EDIT	November 2, 2006 4:25:20 PM	PAGE	35	OF 48

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# LAN Controller (Only 10/100M)

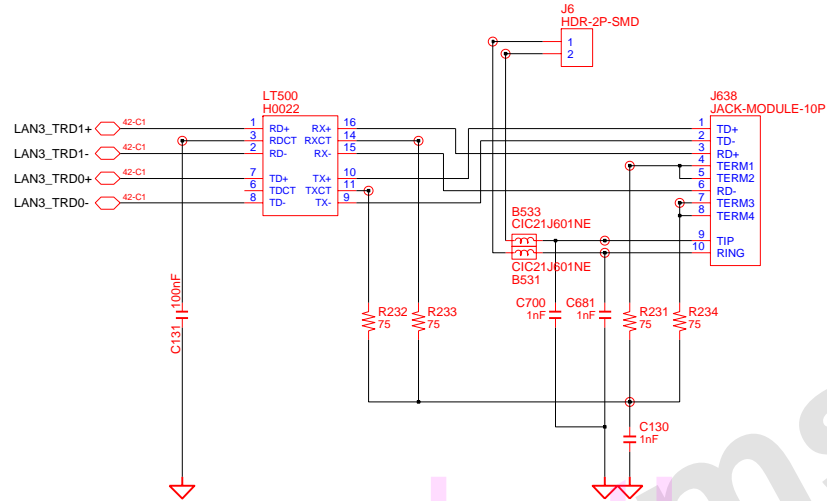


DRAW	JIANG, DS	DATE	11/2/2006	TITLE	HAINAN2	<b>SAMSUNG</b> ELECTRONICS
CHECK	YONG LEI	DEV. STEP	PV			
APPROVAL	KEVIN LEE	REV	2.0		LAN	PART NO. BA41-XXXXXA
MODULE CODE	undef ined	LAST EDIT	November 2, 2006 4:25:20 PM	PAGE	36	OF 48

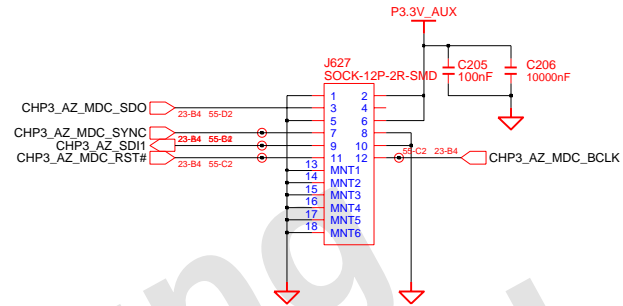
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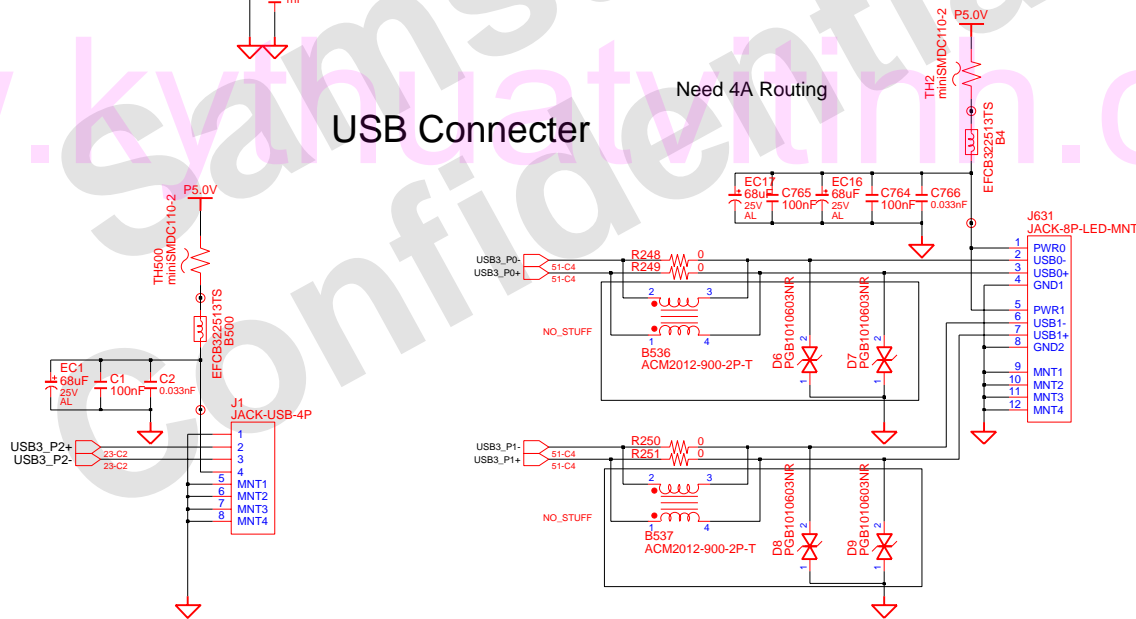
**LAN Connector**



**MDC Connector**



**USB Connector**

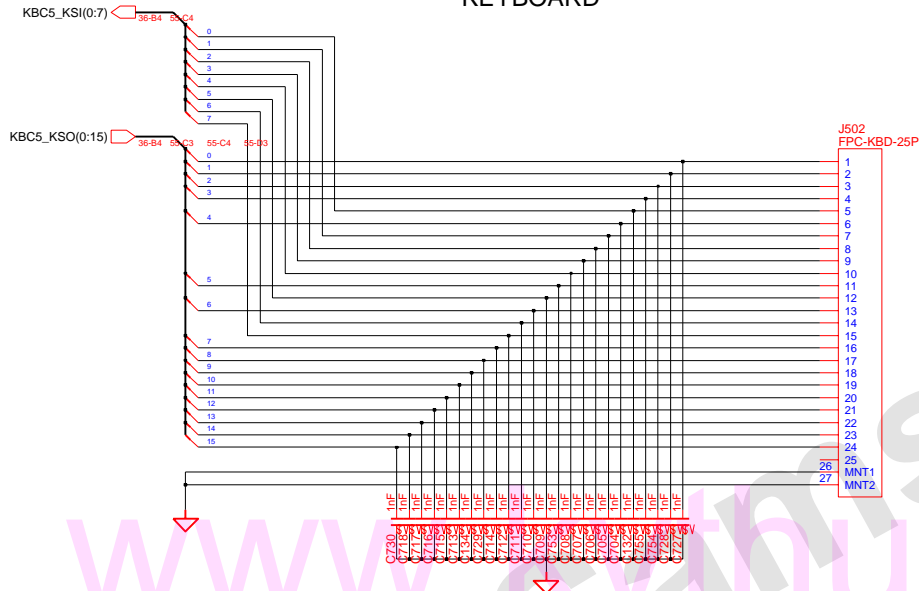


DRAW	JIANG, DS	DATE	11/2/2006	TITLE	HAINAN2	<b>SAMSUNG</b> ELECTRONICS
CHECK	YONG LEI	DEV. STEP	PV			
APPROVAL	KEVIN LEE	REV	2.0		LAN & MDC CONN	PART NO. BA41-XXXXXA
MODULE CODE	undef ined	LAST EDIT	November 2, 2006 4:25:20 PM	PAGE	37	OF 48

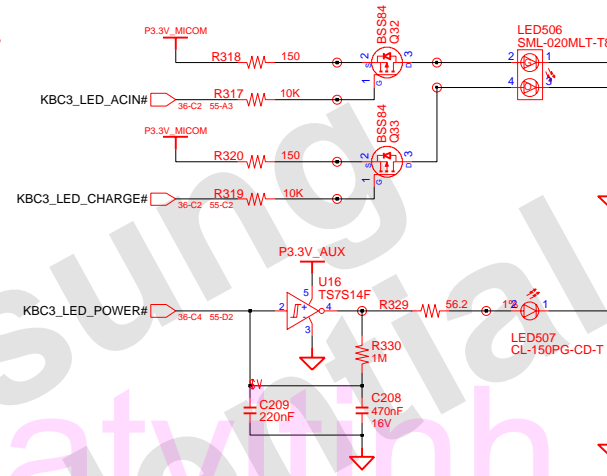
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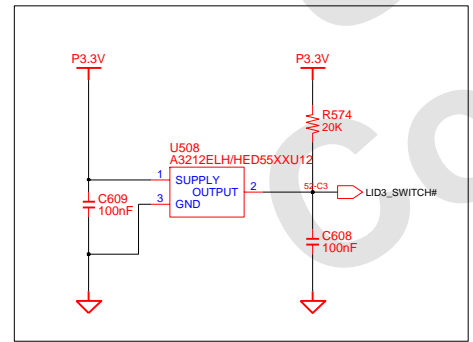
**KEYBOARD**



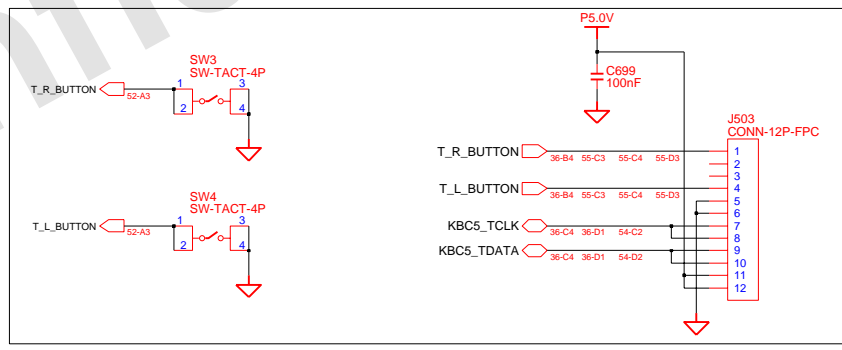
**ADAPTERIN/CHARGING LED**



**LID SWITCH**



**TOUCHPAD**

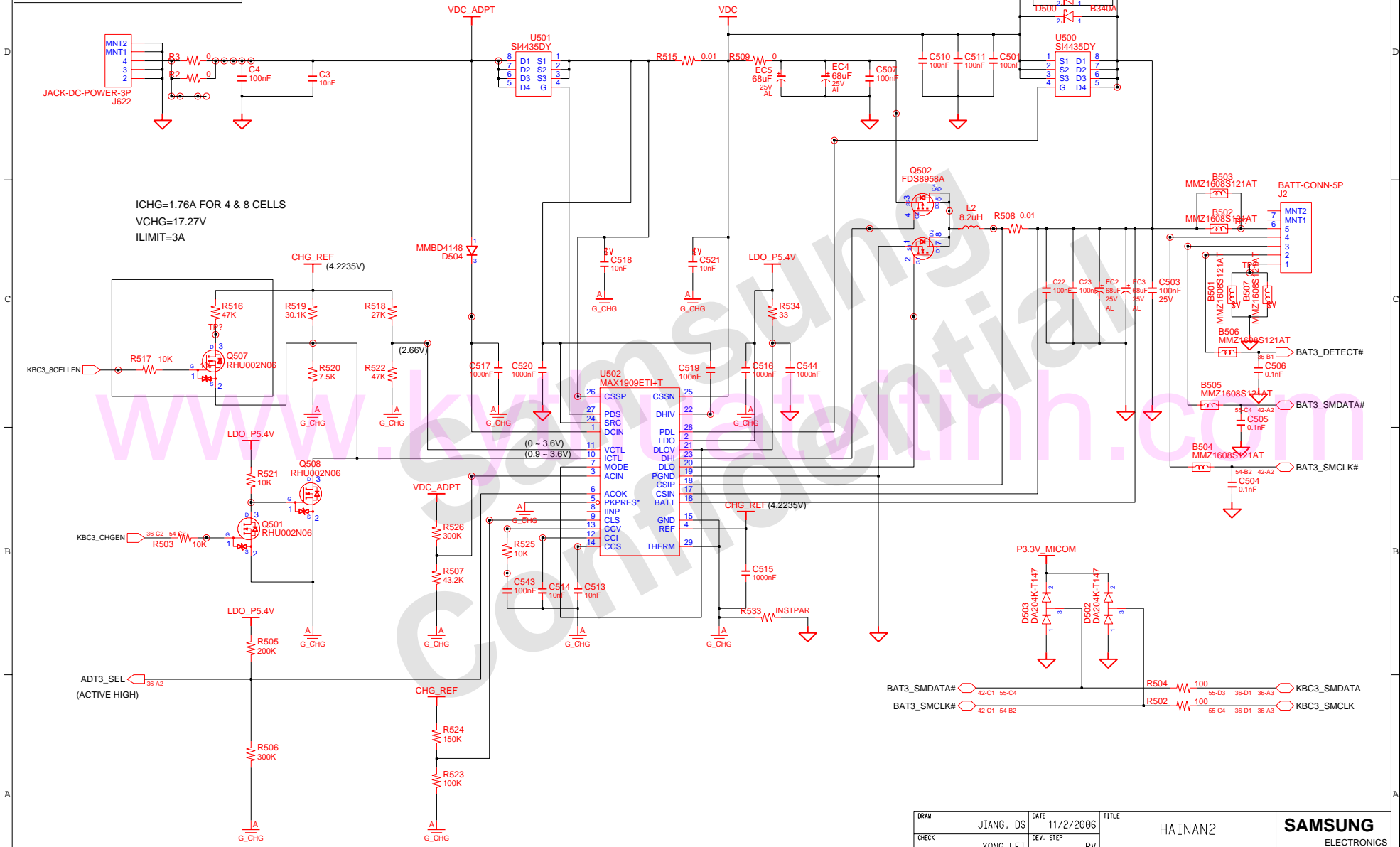


DRAW	JIANG, DS	DATE	11/2/2006	TITLE	HAINAN2	SAMSUNG ELECTRONICS
CHECK	YONG LEI	DEV. STEP	PV	BOARD CONN	PART NO.	
APPROVAL	KEVIN LEE	REV	2.0		BA41-XXXXXA	
MODULE CODE	undef ined	LAST EDIT	November 2, 2006 4:25:20 PM	PAGE	38	OF 48

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# CHARGER & POWER MANAGEMENT

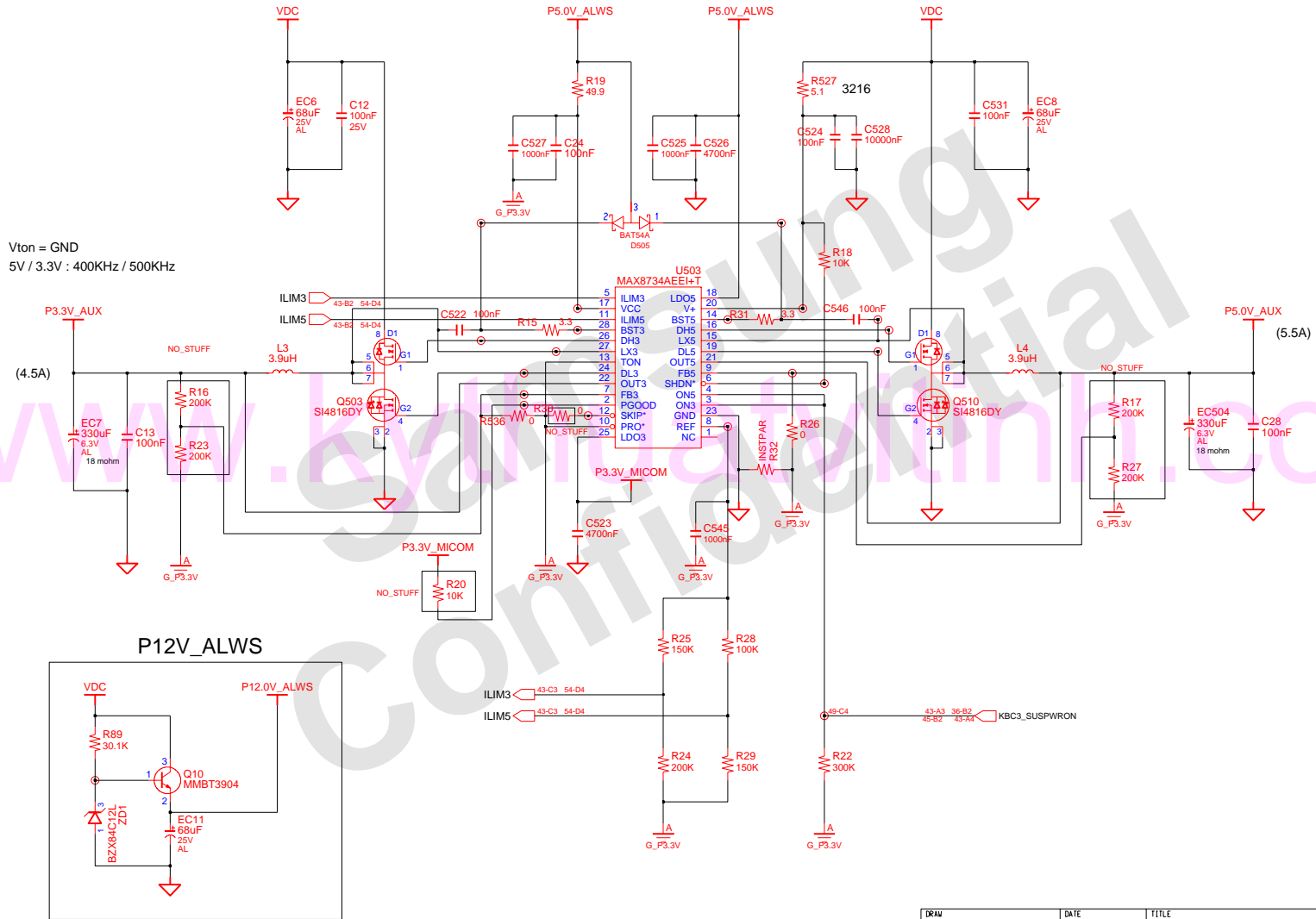


DRAW	JIANG, DS	DATE	11/2/2006	TITLE	HAINAN2	SAMSUNG ELECTRONICS
CHECK	YONG LEI	DEV. STEP	PV	CHARGE	PART NO.	
APPROVAL	KEVIN LEE	REV	2.0		BA41-XXXXXA	
MODULE CODE	undef ined	LAST EDIT	November 2, 2006 4:25:20 PM	PAGE	39	OF 48

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# P3.3V\_AUX & P5V\_AUX



V<sub>ton</sub> = GND  
 5V / 3.3V : 400KHz / 500KHz

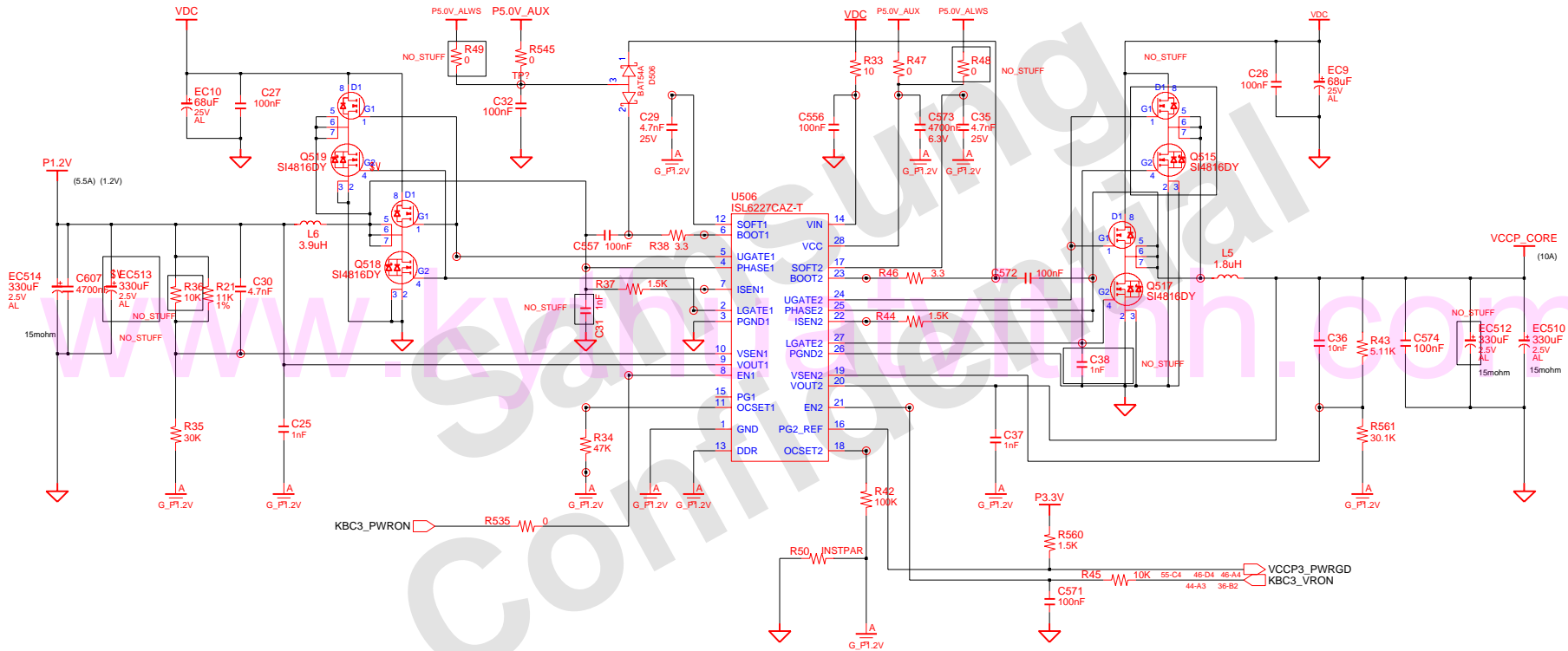
DRAW	JIANG, DS	DATE	11/2/2006	TITLE	HAINAN2	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-XXXXXA
CHECK	YONG LEI	DEV. STEP	PV	P3.3V_AUX & P5V_AUX		
APPROVAL	KEVIN LEE	REV	2.0	November 2, 2006 4:25:20 PM		PAGE 40 OF 48
MODULE CODE	undef:ind	LAST EDIT				



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# P1.2V & VCCP\_CORE(1.05V)



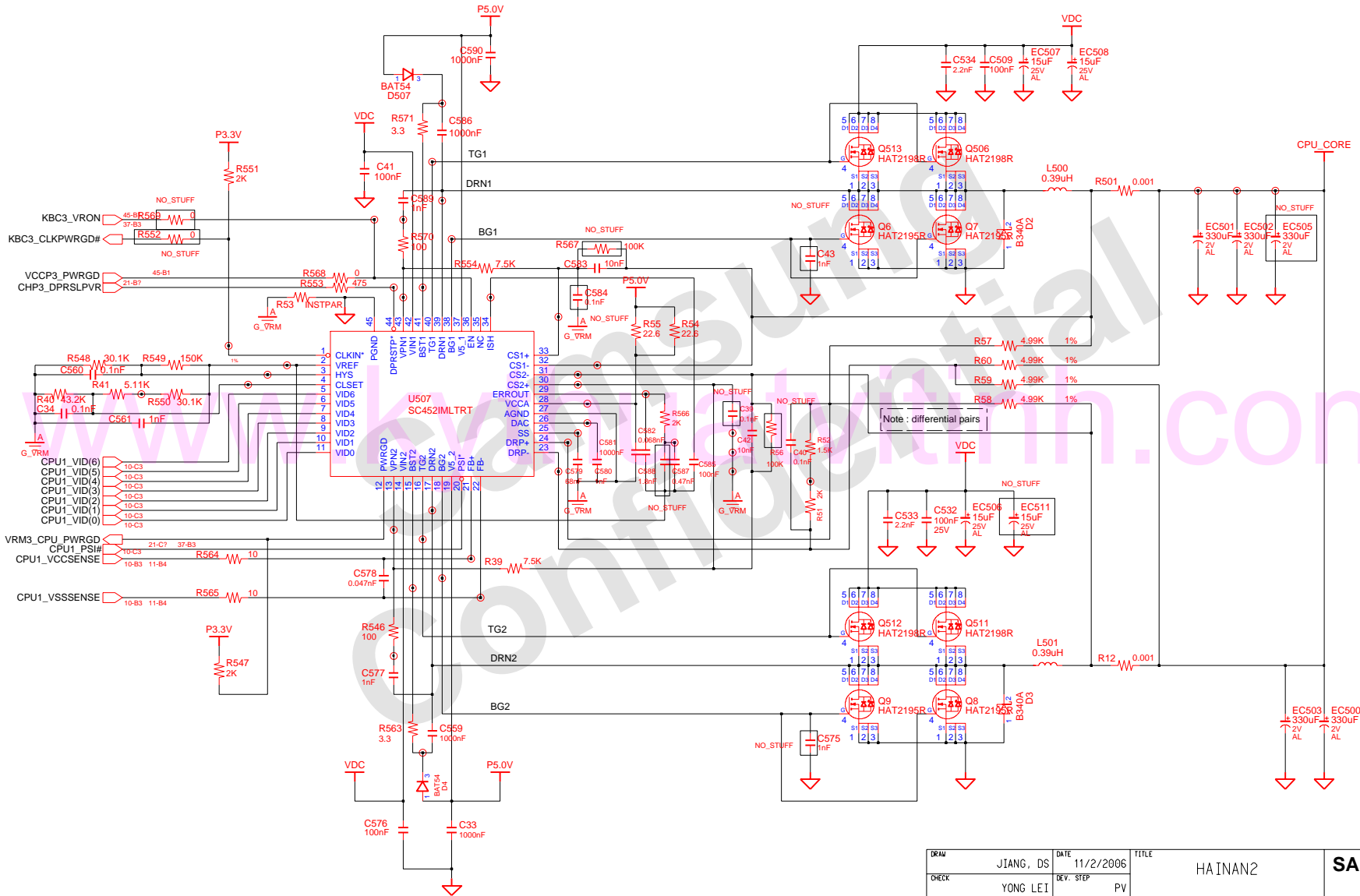
DRAW	JIANG, DS	DATE	11/2/2006	TITLE	HAINAN2	<b>SAMSUNG</b> ELECTRONICS
CHECK	YONG LEI	DEV. STEP	PV			
APPROVAL	KEVIN LEE	REV	2.0		P1.2V & VCCP	PART NO. BA41-XXXXXA
MODULE CODE	undef:ind	LAST EDIT	November 2, 2006 4:25:20 PM	PAGE	41	OF 48



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# CPU VRM [SEMTECH]

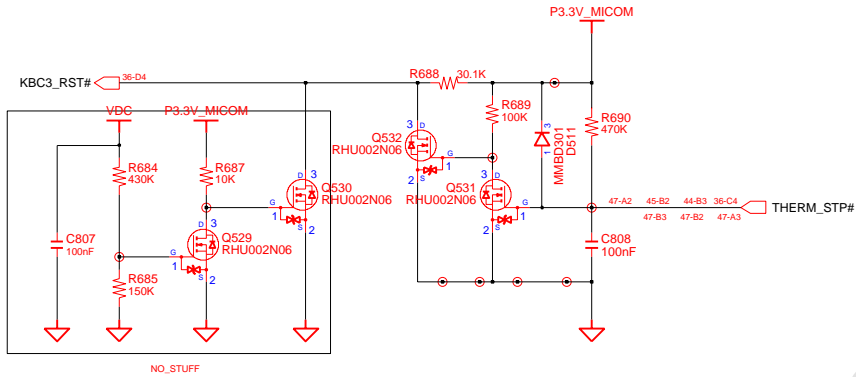


DRAM	JIANG, DS	DATE	11/2/2006	TITLE	HAINAN2	<b>SAMSUNG</b> ELECTRONICS
CHECK	YONG LEI	DEV. STEP	PV			
APPROVAL	KEVIN LEE	REV	2.0		CPU VRM	PART NO.
MODULE CODE	undefined	LAST EDIT	November 2, 2006 4:25:20 PM			BA41-XXXXXA
					PAGE	43 OF 48

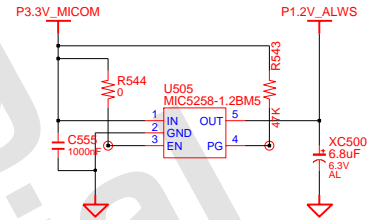
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**MICOM RESET**

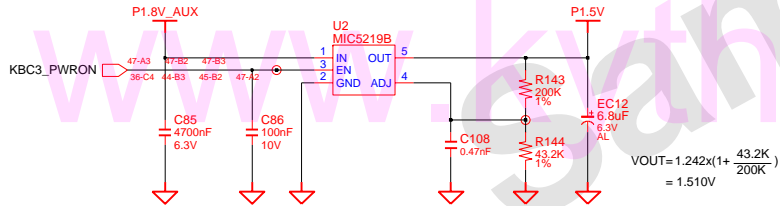


**Switched Power On (P3.3V & 1.8V&1.2V\_ALWS)**

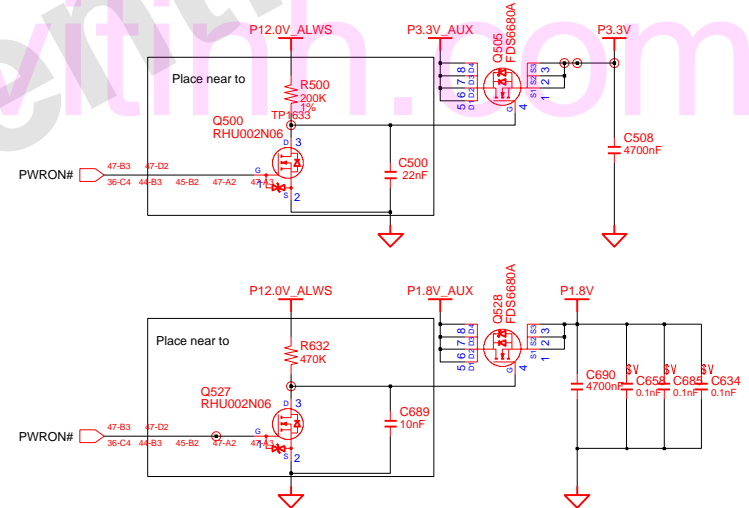
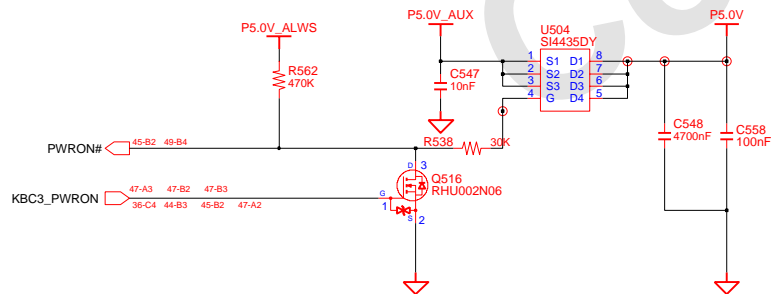


**P1.5V POWER**

(EBL)  
(AVE MAX : 2A)



**Switched Power On (P5V)**

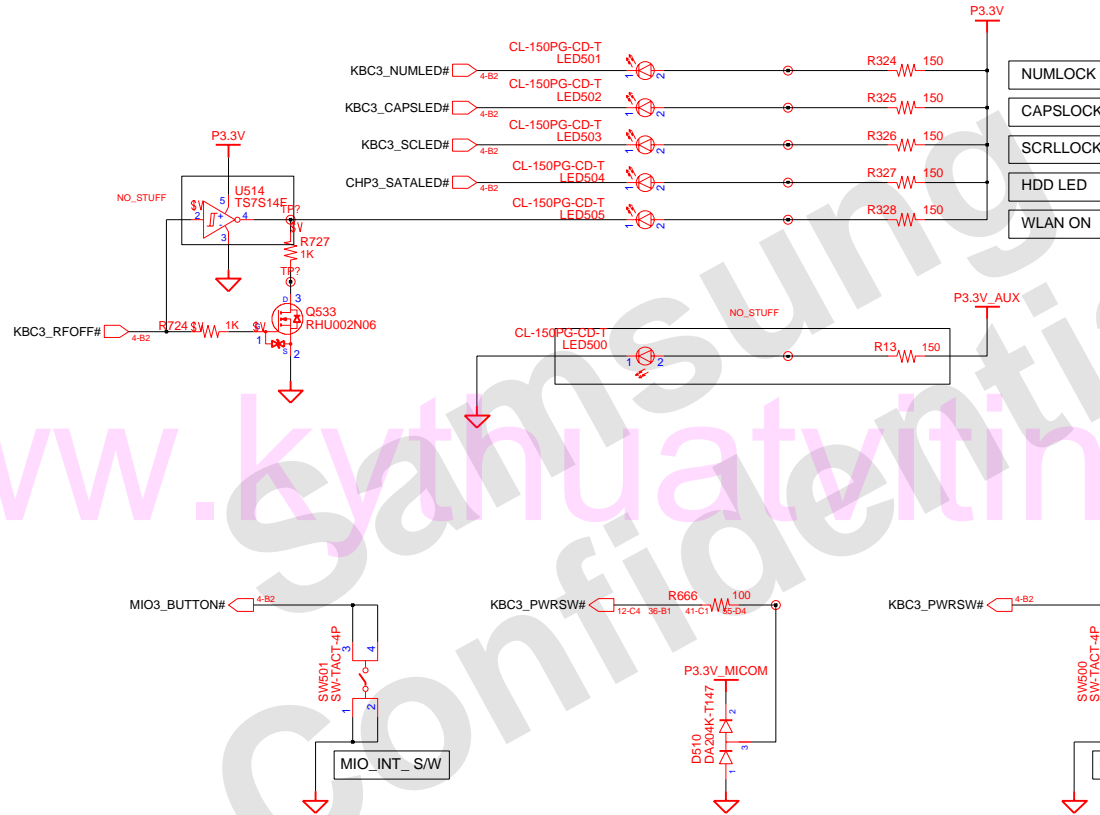


DRAW	JIANG, DS	DATE	11/2/2006	TITLE	HAINAN2	<b>SAMSUNG</b> ELECTRONICS
CHECK	YONG LEI	DEV. STEP	PV	SWITCH POWER	PART NO.	
APPROVAL	KEVIN LEE	REV	2.0		BA41-XXXXXA	
MODULE CODE	undef ined	LAST EDIT	November 2, 2006 4:25:20 PM	PAGE	44	OF 48

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**LED  
0801-002195**

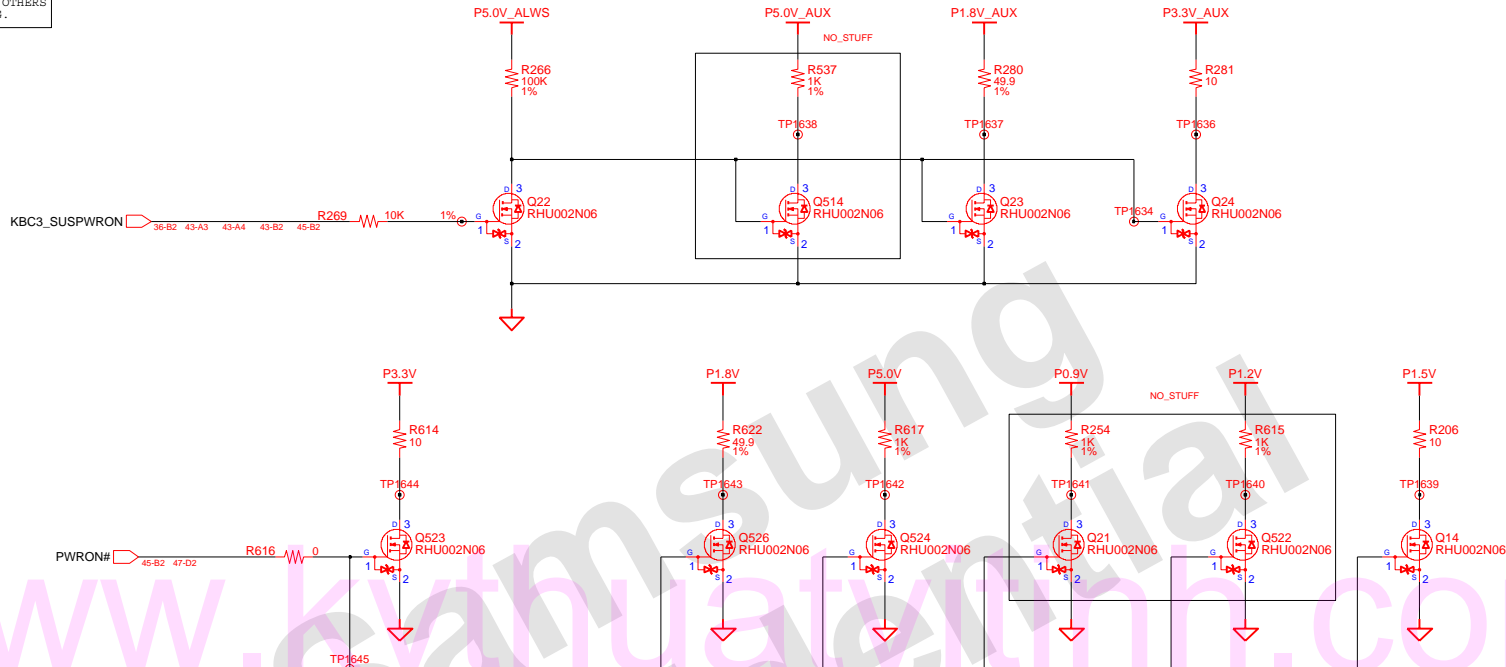


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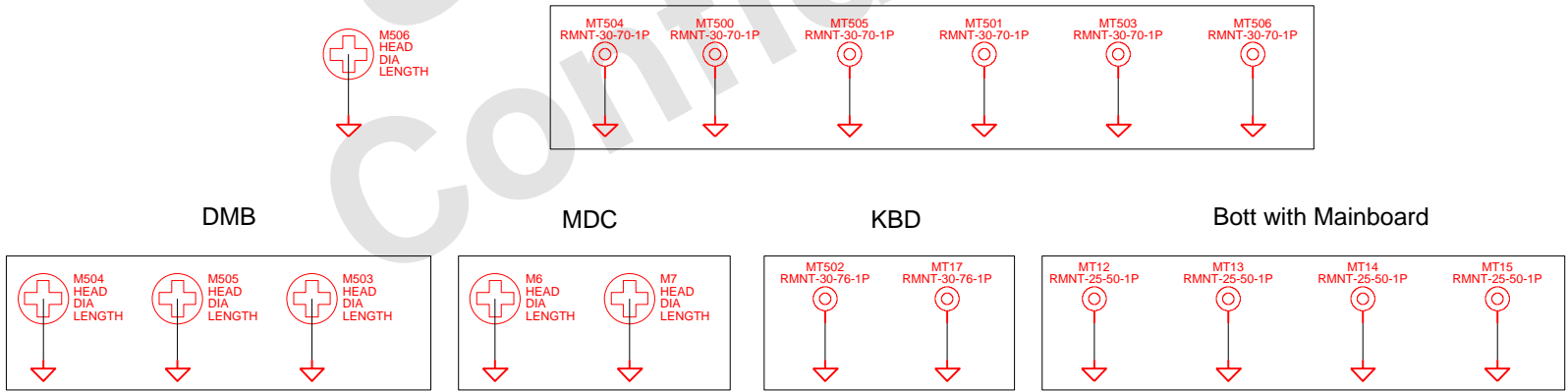
DRAW	JIANG, DS	DATE	11/2/2006	TITLE	HAINAN2 POWER SWITCH	<b>SAMSUNG</b> ELECTRONICS
CHECK	YONG LEI	DEV. STEP	PV			
APPROVAL	KEVIN LEE	REV	2.0			PART NO. BA41-XXXXXA
MODULE CODE	undef ined	LAST EDIT	November 2, 2006 4:25:20 PM	PAGE	45	OF 48

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**BT System**



DRAW	JIANG, DS	DATE	11/2/2006	TITLE	HAINAN2	<b>SAMSUNG</b> ELECTRONICS
CHECK	YONG LEI	DEV. STEP	PV	POWER STRAPS		
APPROVAL	KEVIN LEE	REV	2.0			PART NO. BA41-XXXXXA
MODULE CODE	undef ined	LAST EDIT	November 2, 2006 4:25:20 PM	PAGE	46	OF 48

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TP2027 OMC1  
 TP2028 OMC2  
 TP2029 GPIO1  
 TP2030 ILIM3  
 TP2031 ILIM5

TP2020 CPU1\_TDI  
 TP2021 CPU1\_TMS  
 TP2022 PCI3\_PAR  
 TP2023 SATA1\_X1  
 TP2024 SMB3\_CLK  
 TP2025 SPI3\_CLK  
 TP2026 SPI3\_CS#

TP1968 CPU1\_A20M#  
 TP1971 CPU1\_BSEL0  
 TP1972 CPU1\_BSEL1  
 TP1973 CPU1\_BSEL2

TP1939 PCI3\_CBE0#  
 TP1940 PCI3\_CBE1#  
 TP1941 PCI3\_CBE2#  
 TP1942 PCI3\_CBE3#  
 TP1943 PCI3\_GNT1#

TP1945 PCI3\_IRDY#  
 TP1946 PCI3\_PERR#  
 TP1947 PCI3\_REO1#  
 TP1914 PCI3\_RSTF#  
 TP1915 PCI3\_SERR#  
 TP1916 PCI3\_STOP#  
 TP1917 PCI3\_TRDY#

TP1888 KBC5\_KSO(0)  
 TP1889 KBC5\_KSO(1)  
 TP1890 KBC5\_KSO(2)  
 TP1891 KBC5\_KSO(3)  
 TP1892 KBC5\_KSO(4)  
 TP1893 KBC5\_KSO(5)  
 TP1894 KBC5\_KSO(6)  
 TP1895 KBC5\_KSO(7)  
 TP1896 KBC5\_KSO(8)  
 TP1897 KBC5\_KSO(9)

TP1898 LCD3\_BKLTON  
 TP1899 LPC3\_LAD(0)  
 TP1900 LPC3\_LAD(1)  
 TP1869 LPC3\_LAD(2)  
 TP1870 LPC3\_LAD(3)  
 TP1871 MCD3\_MSIN#

TP2002 CHP3\_SPKR

TP1977 CPU1\_FERR#

TP2006 CPU1\_INTR  
 TP2007 CPU1\_PSI#

TP1979 CPU1\_INTR#

TP1950 CPU1\_TRST#  
 TP1951 EXP3\_CPPE#

TP2011 CPU1\_SLP#  
 TP2012 CPU1\_SMI#  
 TP2013 IDE5\_CS1#  
 TP2014 IDE5\_CS3#

TP1918 PEX3\_WAKE#  
 TP1919 PFLT3\_RSTF#

TP1952 IDE5\_DACK#  
 TP1953 IDE5\_IORDY#  
 TP1954 JCK\_SENS\_A  
 TP1955 KBC3\_CHGEN  
 TP1956 KBC3\_SMLCLK  
 TP1957 KBC5\_TDATA

TP1920 OT\_L\_BUTTON  
 TP1921 OT\_R\_BUTTON  
 TP1922 VGA3\_HSYNC  
 TP1923 VGA3\_VSYNC  
 TP1924 DBA3\_SMLCLK#  
 TP1925 CHP3\_OVERT#  
 TP1910 CHP3\_SBPME#  
 TP1911 CHP3\_SERIRQ  
 TP1912 CHP3\_SLPS3#  
 TP1913 CHP3\_SLPS5#

TP1980 IDE5\_DREQ  
 TP1981 IDE5\_IOR#  
 TP1982 IDE5\_IOW#  
 TP1983 KBC3\_A20G  
 TP1984 KBC3\_RST#  
 TP1985 KBC3\_VRON  
 TP1986 KBC5\_TCLK

TP1958 LCD3\_VDEN  
 TP1959 MCD3\_SDCE#  
 TP1960 MCD3\_XDALE  
 TP1961 MCD3\_XDCD#  
 TP1962 MCD3\_XDCE#  
 TP1963 MCD3\_XDRE#  
 TP1964 MCD3\_XDWE#

TP1902 CPU1\_DPSLP#  
 TP1903 CPU1\_IGNNE#  
 TP1904 CPU1\_VID(0)  
 TP1905 CPU1\_VID(1)  
 TP1906 CPU1\_VID(2)  
 TP1907 CPU1\_VID(3)  
 TP1908 CPU1\_VID(4)  
 TP1909 CPU1\_VID(5)  
 TP1872 CPU1\_VID(6)  
 TP1873 EXP3\_PLUS#  
 TP1874 EXP3\_PERST#  
 TP1875 IDE5\_IDEIRQ  
 TP1876 KBC3\_18VEN#  
 TP1877 KBC3\_PWRSW#  
 TP1878 KBC3\_SCLEW#  
 TP1879 KBC3\_SMDATA  
 TP1880 KBC5\_KSI(0)  
 TP1881 KBC5\_KSI(1)  
 TP1882 KBC5\_KSI(2)  
 TP1883 KBC5\_KSI(3)  
 TP1884 KBC5\_KSI(4)  
 TP1885 KBC5\_KSI(5)  
 TP1886 KBC5\_KSI(6)  
 TP1887 KBC5\_KSI(7)

TP1996 ODD5\_RST#

TP1997 SMB3\_DATA  
 TP1998 SPI3\_MISO  
 TP1999 SPI3\_MOSI  
 TP2000 AUD3\_EAPD#

TP2015 RTC\_CLK  
 TP2016 AC\_SDOUT  
 TP2017 AUTO\_ON#  
 TP2018 CPU1\_NMI  
 TP2019 CPU1\_TCK

TP2001 CLK3\_NB14M



DRAW	JIANG, DS	DATE	11/2/2006	TITLE	HAINAN2	<b>SAMSUNG</b> ELECTRONICS
CHECK	YONG LEI	DEV. STEP	PV			
APPROVAL	KEVIN LEE	REV	2.0		TP	PART NO. BA41-XXXXXA
MODULE CODE		LAST EDIT	November 2, 2006 4:25:20 PM	PAGE	47	OF 48

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- TP2195 ○ CHP3\_DPRSPLVR
- TP2196 ○ CHP3\_SATALED#
- TP2197 ○ CPU1\_PROCHOT#
- TP2198 ○ CPU1\_PWRGDCPU
- TP2199 ○ CPU1\_VCCSENSE
- TP2200 ○ CPU1\_VSSSENSE
- TP2201 ○ JCK\_SENS\_MCHP
- TP2202 ○ KBC3\_CAPSLED#
- TP2203 ○ KBC3\_WAKESCI#
- TP2204 ○ LCD3\_BKLTCTRL
- TP2205 ○ LCD3\_EDID\_CLK
- TP2126 ○ G\_CRT
- TP2127 ○ G\_CRT
- TP2128 ○ G\_DDR
- TP2129 ○ G\_DDR
- TP2130 ○ G\_DDR
- TP2131 ○ G\_DDR
- TP2132 ○ G\_P3.3V
- TP2133 ○ G\_P3.3V
- TP2134 ○ G\_P3.3V
- TP2135 ○ G\_P3.3V
- TP2136 ○ LCD\_VDD3V
- TP2137 ○ LCD\_VDD3V
- TP2078 ○ P5.0V\_AUX
- TP2079 ○ P5.0V\_AUX
- TP2080 ○ PCIE\_VDDR
- TP2085 ○ P1.2V\_ALWS
- TP2086 ○ P1.2V\_ALWS
- TP2088 ○ P5.0V\_ALWS
- TP2089 ○ P5.0V\_ALWS
- TP2090 ○ P5.0V\_ALWS
- TP2091 ○ P5.0V\_ALWS
- TP2092 ○ P12.0V\_ALWS
- TP2093 ○ P12.0V\_ALWS
- TP2032 ○ P12.0V\_ALWS
- TP2033 ○ P12.0V\_ALWS
- TP2035 ○ P3.3V\_AUX\_EXP
- TP2037 ○ P3.3V\_AUX\_EXP
- TP2038 ○ VDC
- TP2039 ○ VDC
- TP2040 ○ VDC
- TP2041 ○ VDC
- TP2045 ○ VCC\_CRT
- TP2046 ○ VDC\_INV
- TP2047 ○ VDC\_INV
- TP2050 ○ VDD\_AMP
- TP2051 ○ VDD\_AMP
- TP2052 ○ VDD\_AMP
- TP2053 ○ VDD\_AMP
- TP2054 ○ VDD\_AUID
- TP2055 ○ VDD\_AUID
- TP2056 ○ VDD\_AUID
- TP2057 ○ VDD\_AUID
- TP2058 ○ VCCP\_CORE
- TP2059 ○ VCCP\_CORE
- TP2060 ○ VCCP\_CORE
- TP2061 ○ VCCP\_CORE
- TP2142 ○ LDO\_P5.4V
- TP2143 ○ LDO\_P5.4V
- TP2146 ○ MEM1\_VREF
- TP2147 ○ MEM1\_VREF
- TP2148 ○ P0.9V
- TP2149 ○ P0.9V
- TP2150 ○ P0.9V
- TP2151 ○ P0.9V
- TP2152 ○ P1.2V
- TP2153 ○ P1.2V
- TP2154 ○ P1.2V
- TP2155 ○ P1.2V
- TP2156 ○ P1.5V
- TP2157 ○ P1.5V
- TP2094 ○ P1.5V
- TP2095 ○ P1.5V
- TP2096 ○ P1.8V
- TP2097 ○ P1.8V
- TP2098 ○ P1.8V
- TP2099 ○ P1.8V
- TP2181 ○ CPU1\_THRMTRIP#
- TP2182 ○ KBC3\_CLKPWRGD#
- TP2183 ○ KBC3\_LED\_ACIN#
- TP2184 ○ KBC5\_CAL\_THRM#
- TP2185 ○ LCD3\_EDID\_DATA
- TP2186 ○ VRM3\_CPU\_PWRGD
- TP2103 ○ PRTC\_BAT
- TP2109 ○ P1.5V\_EXP
- TP2110 ○ P1.5V\_EXP
- TP2111 ○ P1.5V\_EXP
- TP2112 ○ P1.8V\_AUX
- TP2113 ○ P1.8V\_AUX
- TP2114 ○ P1.8V\_AUX
- TP2115 ○ P1.8V\_AUX
- TP2116 ○ P2.5V\_LAN
- TP2117 ○ P2.5V\_LAN
- TP2118 ○ P2.5V\_LAN
- TP2119 ○ P2.5V\_LAN
- TP2162 ○ KBC3\_LED\_CHARGE#
- TP2163 ○ KBC3\_THERM\_SMCLK
- TP2164 ○ KBC3\_THERM\_SMDATA
- TP2165 ○ MINIPCI3\_CLKREQ\_B#
- TP2123 ○ P2.5V\_MCD
- TP2124 ○ P3.3V\_AUX
- TP2125 ○ P3.3V\_AUX
- TP2062 ○ P3.3V\_AUX
- TP2063 ○ P3.3V\_AUX
- TP2065 ○ P3.3V\_EXP
- TP2066 ○ P3.3V\_EXP
- TP2168 ○ CHG\_REF
- TP2170 ○ G\_AUD
- TP2171 ○ G\_AUD
- TP2172 ○ G\_AUD
- TP2173 ○ G\_AUD
- TP2174 ○ G\_CHG
- TP2175 ○ G\_CHG
- TP2176 ○ G\_CHG
- TP2177 ○ G\_CHG
- TP2178 ○ G\_CRT
- TP2179 ○ G\_CRT
- TP2068 ○ P3.3V\_MCD
- TP2069 ○ P3.3V\_MCD
- TP2070 ○ P3.3V\_MCD
- TP2071 ○ P3.3V\_MCD
- TP2072 ○ P5.0V\_AUD
- TP2073 ○ P5.0V\_AUD
- TP2074 ○ P5.0V\_AUD
- TP2075 ○ P5.0V\_AUD
- TP2076 ○ P5.0V\_AUD
- TP2077 ○ P5.0V\_AUD

- TP2233 ○ PCI3\_FRAME#
- TP2235 ○ VCCP3\_PWRGD
- TP2236 ○ AUD3\_PCBEEP#
- TP2237 ○ BAT3\_DETECT#
- TP2238 ○ BAT3\_SMDATA#
- TP2239 ○ CHP3\_AZ\_SDI0
- TP2240 ○ CHP3\_BIOSWP#
- TP2241 ○ CHP3\_CPUSTP#

- TP2180 ○ CHP3\_SATA\_DET#
- TP2181 ○ CPU1\_THRMTRIP#
- TP2182 ○ KBC3\_CLKPWRGD#
- TP2183 ○ KBC3\_LED\_ACIN#
- TP2184 ○ KBC5\_CAL\_THRM#
- TP2185 ○ LCD3\_EDID\_DATA
- TP2186 ○ VRM3\_CPU\_PWRGD

- TP2187 ○ CHP3\_ALINK\_RST#
- TP2188 ○ CHP3\_AZ\_AUD\_SDI0
- TP2189 ○ CHP3\_AZ\_MDC\_SDI0

- TP2192 ○ KBC3\_LED\_POWER#

- TP2158 ○ CHP3\_AZ\_AUD\_RST#

- TP2159 ○ CHP3\_SBTHRMTRIP#

- TP2162 ○ KBC3\_LED\_CHARGE#
- TP2163 ○ KBC3\_THERM\_SMCLK

- TP2164 ○ KBC3\_THERM\_SMDATA
- TP2165 ○ MINIPCI3\_CLKREQ\_B#

- TP2193 ○ PCI3\_CLKRUN#
- TP2194 ○ PCI3\_DEVSEL#

- TP2223 ○ CPU1\_STPCLK#

- TP2224 ○ EXP3\_CLKREQ#
- TP2225 ○ ITP3\_SYSRST#
- TP2226 ○ JCK\_SENS\_HP#
- TP2227 ○ KBC3\_CPURST#
- TP2228 ○ KBC3\_EXTSMI#
- TP2229 ○ KBC3\_FANCTRL
- TP2230 ○ KBC3\_NBPWRGD
- TP2231 ○ KBC3\_NUMLED#
- TP2232 ○ KBC3\_PWRBTN#
- TP2207 ○ KBC3\_RSMRST#
- TP2208 ○ KBC3\_RUNSC#
- TP2209 ○ KBC3\_SBPWRGD
- TP2210 ○ KBC5\_KSO(10)
- TP2211 ○ KBC5\_KSO(11)
- TP2212 ○ KBC5\_KSO(12)
- TP2213 ○ KBC5\_KSO(13)
- TP2214 ○ KBC5\_KSO(14)
- TP2215 ○ KBC5\_KSO(15)

- TP2216 ○ LID3\_SWITCH#
- TP2217 ○ LPC3\_LFRAME#

PCB REVISION CONTROL ( ICT )					
NO	CONNECTION	DATE(Y/M/D)	REVISION	STEP	
1	N.C.				
2	1-2				
3	2-3				
4	3-1				
5	1-2-3				
6	N.C.				
7	1-2				
8	2-3				
9	3-1				
10	1-2-3				

REV500  
 1 ○  
 2 ○ ○3

DRAW	JIANG, DS	DATE	11/2/2006	TITLE	HAINAN2	SAMSUNG ELECTRONICS
CHECK	YONG LEI	DEV. STEP	PV			
APPROVAL	KEVIN LEE	REV	2.0		TP	PART NO. BA41-XXXXXA
MODULE CODE		LAST EDIT	November 2, 2006 4:25:20 PM	PAGE	48	OF 48