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HAINAN3_EXT

CPU : Intel Santarosa Merom
 Chip Set : RS600&SB600&M64S
 Remarks : Mobility Platform

Model Name : HAINAN3_EXT
 PBA Name : MAIN
 PCB Code : BA41-00809A GCE
 BA41-00810A NANYA
 Dev. Step : MP1.1
 Revision : 1.0
 T.R. Date : 2007.09.08

DRAW	CHECK	APPROVAL
ELLEN ZHANG	ROKY ZHENG	KEVIN LEE

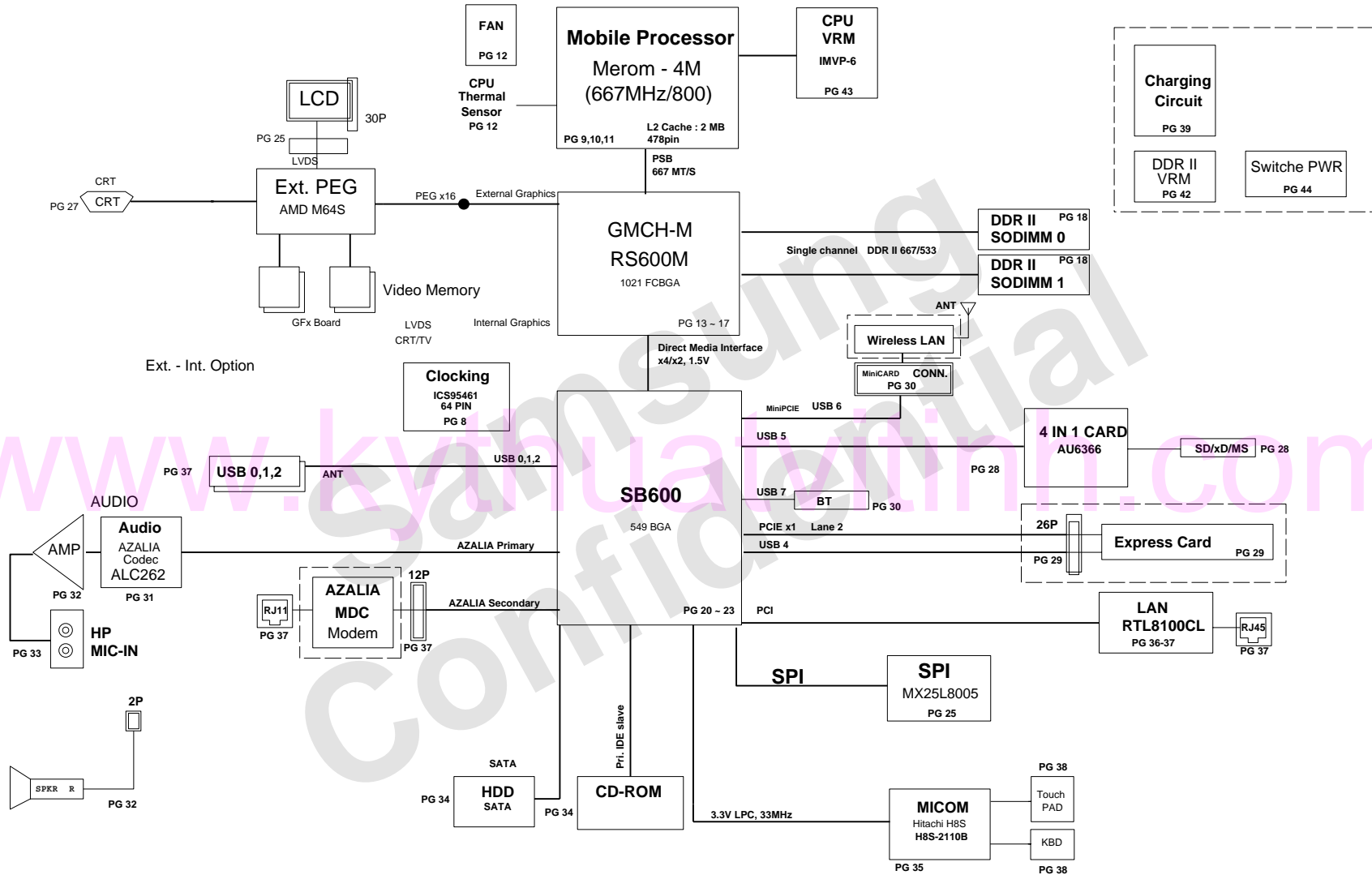
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DRAW	ELLEN ZHANG	DATE	9/8/2007	TITLE	HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK	ROKY ZHENG	DEV. STEP	MP1.1	COVER	PART NO.	
APPROVAL	KEVIN LEE	REV	1.0		BA41-00809/810A	
MODULE CODE	undefined	LAST EDIT	September 8, 2007 12:02:16 PM	PAGE	1	OF 53

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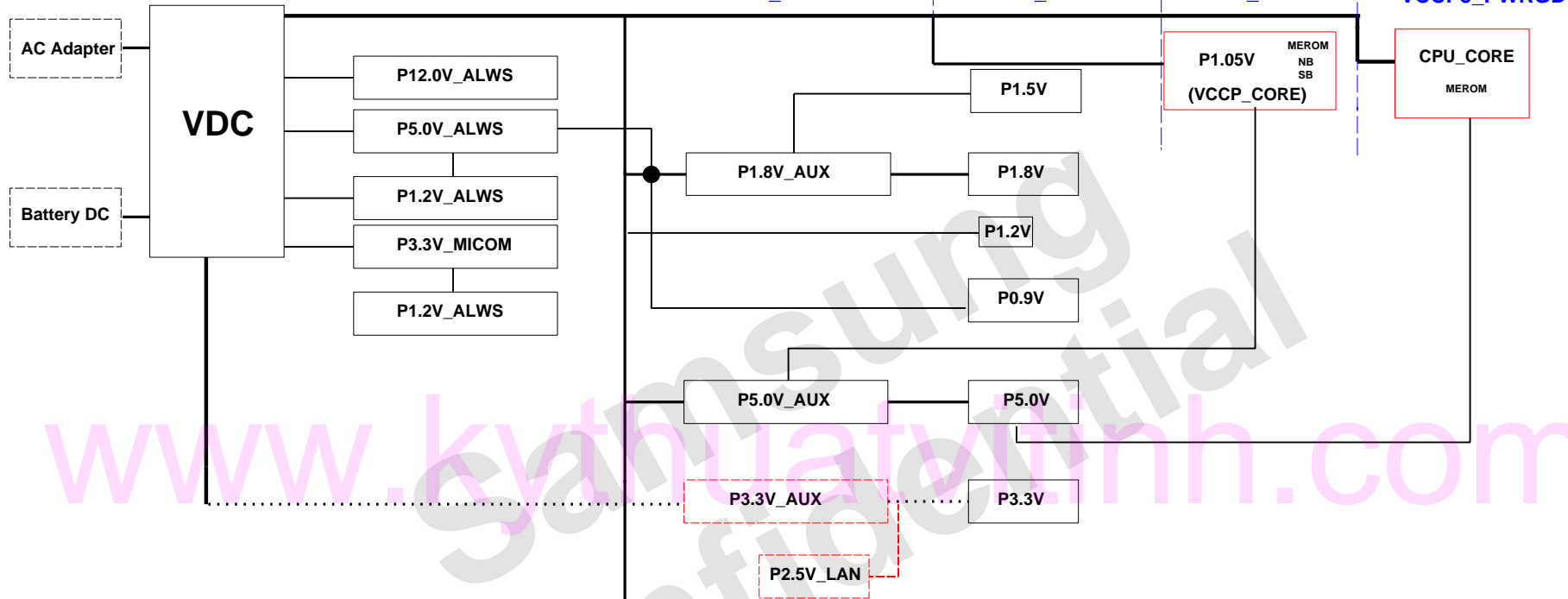


DRAW	ELLEN ZHANG	DATE	9/8/2007	TITLE	HAINAN3_EXT DIAGRAM	SAMSUNG ELECTRONICS
CHECK	ROKY ZHENG	DEV. STEP	MP1.1			
APPROVAL	KEVIN LEE	REV	1.0			PART NO. BA41-00809/810A
MODULE CODE	undef ined	LAST EDIT	September 8, 2007 12:02:16 PM	PAGE	2	OF 53

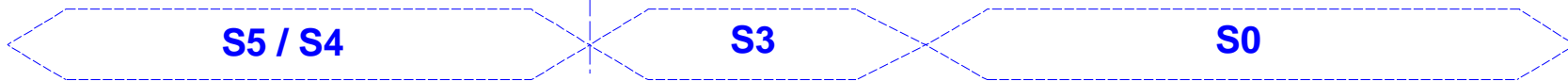
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Power Diagram

KBC3_SUSPWRON | KBC3_PWRON | KBC3_VRON | VCCP3_PWRGD



Rail State	+V*Always	+V*AUX	+V	SUSPWR	PWRON	VRON
Full On	ON	ON	ON	H	H	H
S3	ON	ON	OFF	H	L	L
S4	ON	ON	OFF	H	L	L
S5	ON	OFF	OFF	L	L	L



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CHECK	ROKY ZHENG	DEV. STEP	MP1.1			
APPROVAL	KEVIN LEE	REV	1.0		POWER DIAGRAM	PART NO. BA41-00809/810A
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POWER SEQUENCE

VDC
ADT3_SEL
P3.3V_MICOM
KBC3_RST*
P5.0V_ALWS
P1.2V_ALWS
PRTC_BAT

KBC3_PWRSW*

KBC3_SUSPWRON

P5V_AUX/P3.3V_AUX/P1.8V_AUX/1.2V_AUX

KBC3_RSMRST*

MEM1_VREF

KBC3_PWRBTN*

CHP3_SLPS5*

CHP3_SLPS3*

KBC3_PWRON

KBC3_CLKPWRGD#

P5.0V

PWRON

P1.8V/P1.5V/P0.9V/P1.2V

KBC3_RUNSCI#

KBC3_VRON

VCCP_CORE

VCCP3_PWRGD

CPU_CORE

VRM3_CPU_PWRGD

KBC3_NBPWRGD

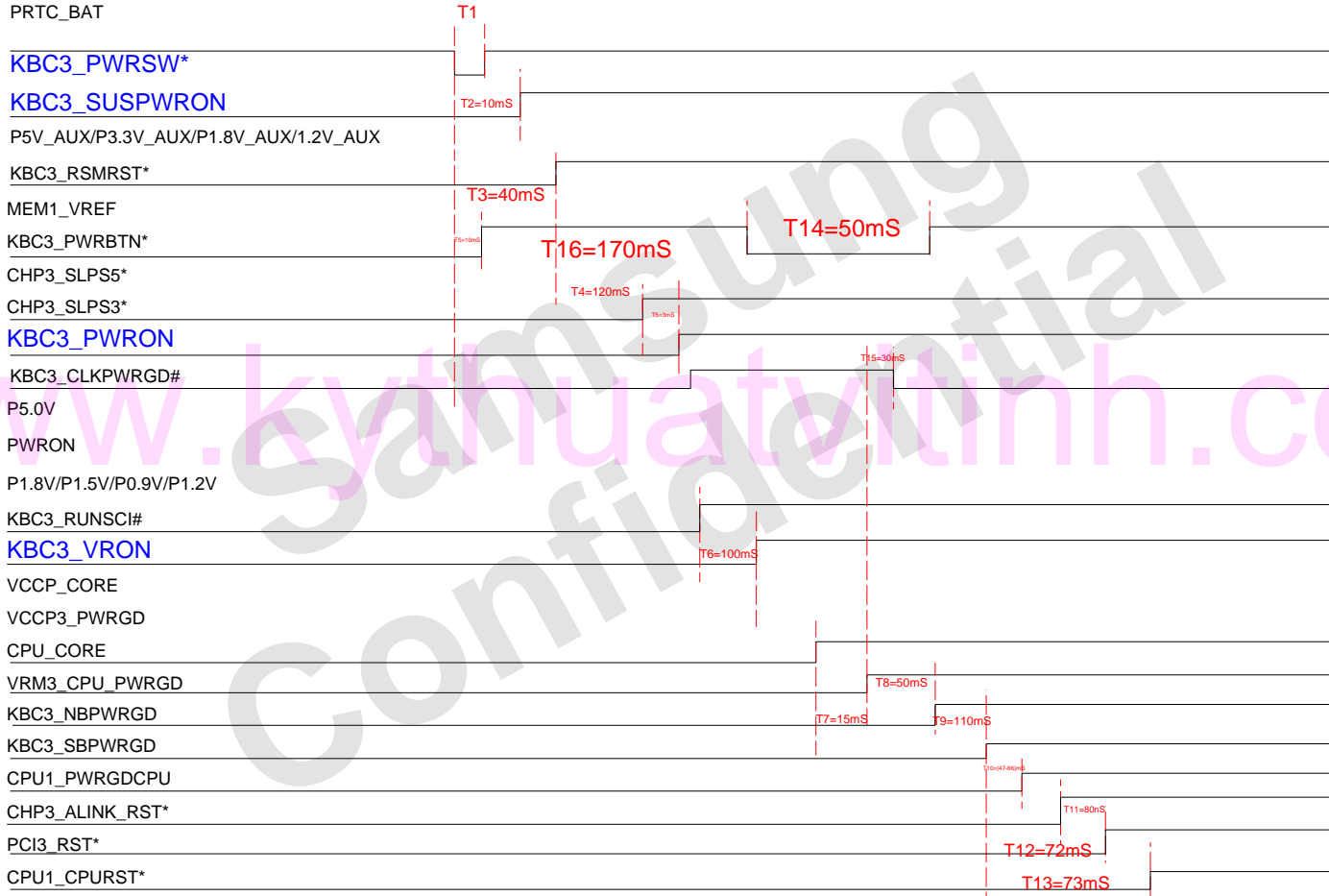
KBC3_SBPWRGD

CPU1_PWRGDPCPU

CHP3_ALINK_RST*

PCI3_RST*

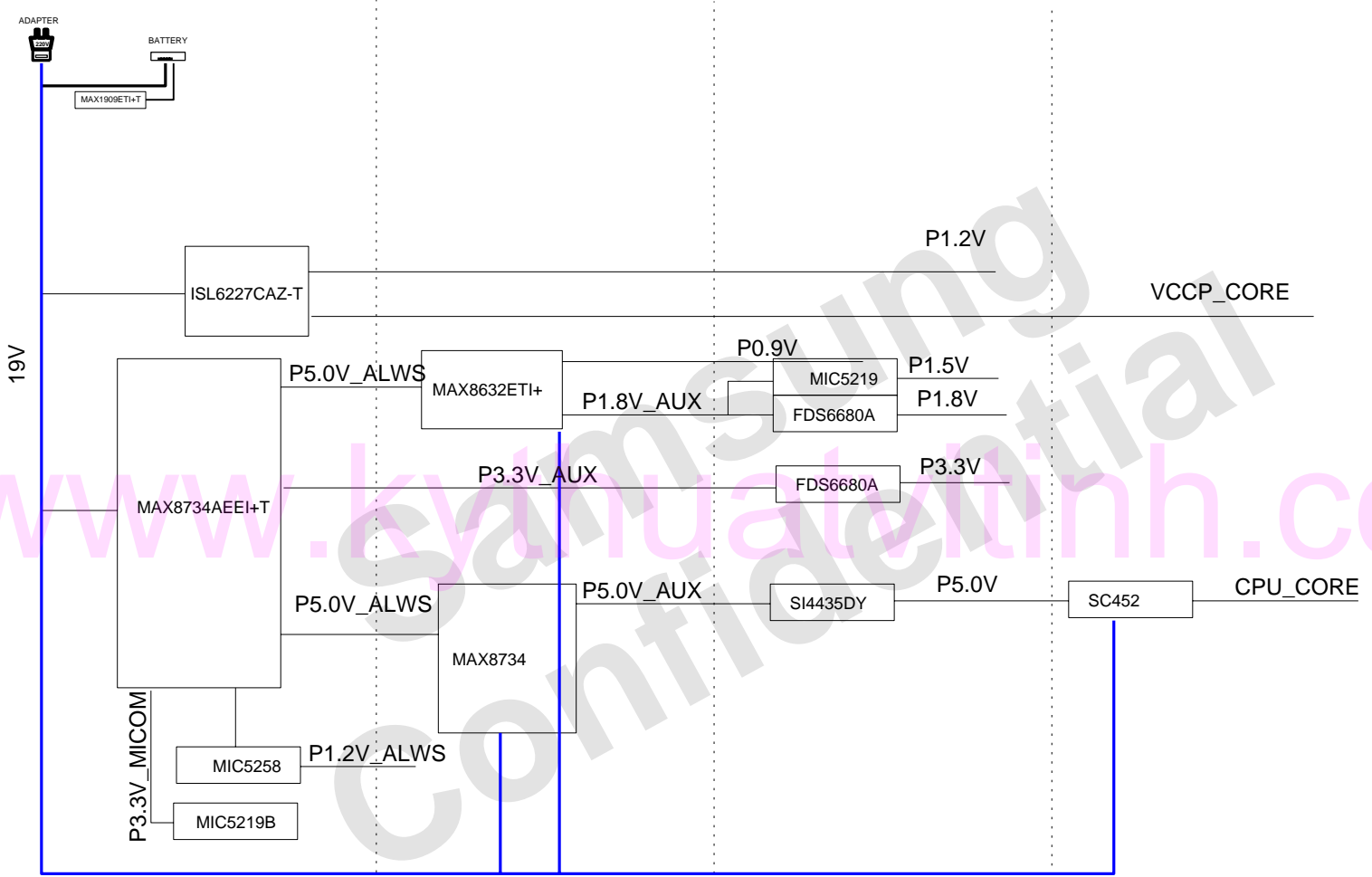
CPU1_CPURST*



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APPROVAL	KEVIN LEE	REV	1.0		POWER SEQUENCE	PART NO. BA41-00809/810A
MODULE CODE	undef ined	LAST EDIT	September 8, 2007 12:02:16 PM	PAGE	4	OF 53

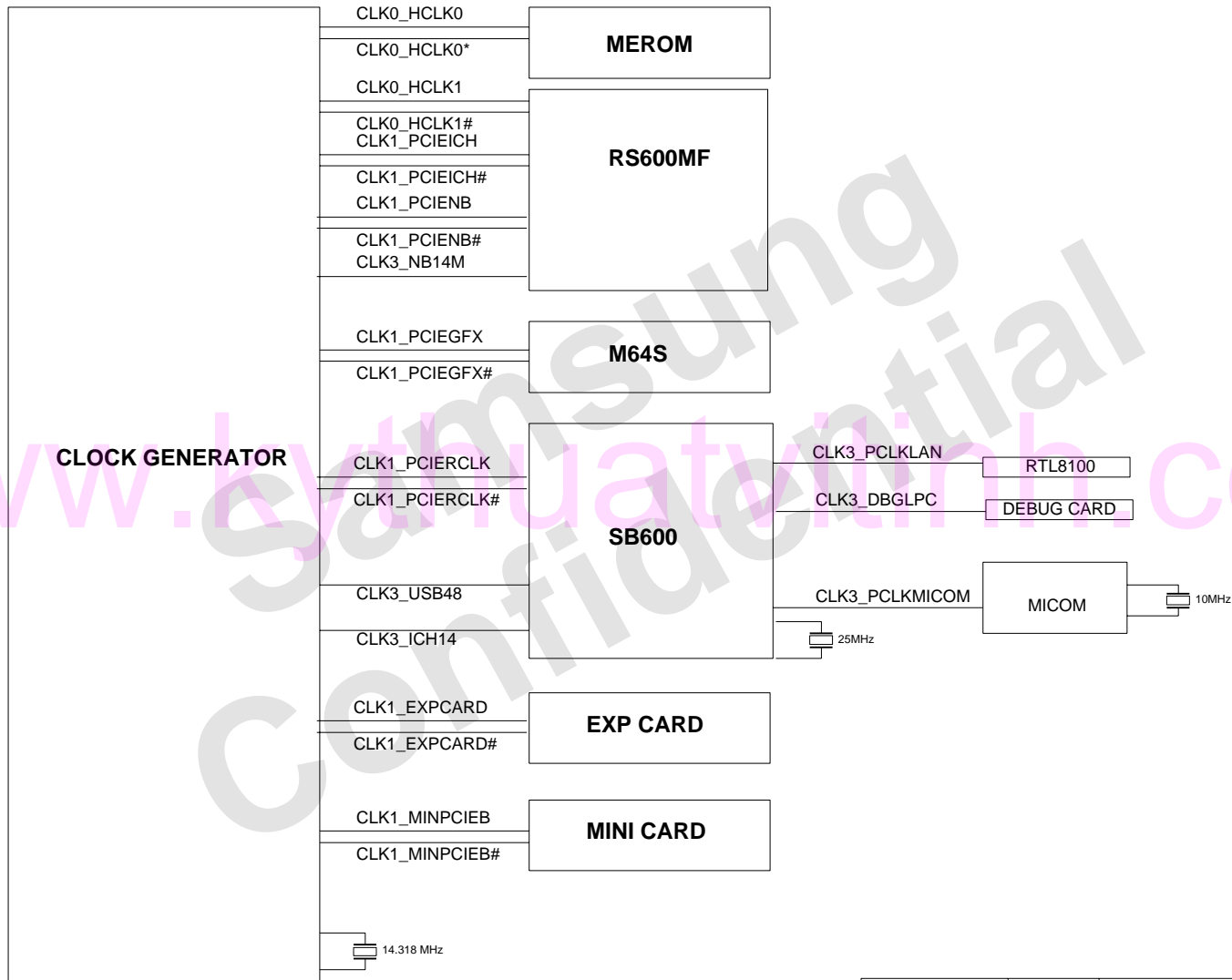
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POWER RAILS ANALYSIS



DRAW	ELLEN ZHANG	DATE	9/8/2007	TITLE	HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK	ROKY ZHENG	DEV. STEP	MP1.1			
APPROVAL	KEVIN LEE	REV	1.0	POWER BLOCK	PART NO.	BA41-00809/810A
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DRAW	ELLEN ZHANG	DATE	9/8/2007	TITLE	HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK	ROKY ZHENG	DEV. STEP	MP1.1			
APPROVAL	KEVIN LEE	REV	1.0		CLOCK DIAGRAM	PART NO. BA41-00809/810A
MODULE CODE	undefined	LAST EDIT	September 8, 2007 12:02:16 PM	PAGE	6	OF 53

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SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
LAN	AD21	1	G
USB	AD30(internal)	-	-
Hub to PCI	AD31(internal)	-	-
LPC bridge/IDE/AC97/SMBUS	AD31(internal)	-	-
Internal MAC	AD31(internal)	-	-
AC Link	-	-	-

Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	SB600	Real Time Clock
Crystal	10MHz	MICOM	HS64FZ110B
Crystal	14.318MHz	CLOCK-Generator	ICS95481
Crystal	12MHz	AU6366	4 IN 1 CARD
Crystal	25MHz	LAN	LOM

Voltage Rails

CPU_CORE	CPU	CPU RS600 SB600
VCCP_CORE	CPU	RS600 SB600
P1.2V		
P1.5V	CPU EXPCARD	
P1.8V	RS600	
P0.9V	DDR2	
P5.0V	FAN THERMAL CRT SB600 AU6366 MINIPCI ALC262 HDD ODD MICOM USB TOUCH-PAD CPU_CORE	
P3.3V	SYSTEM POWER	
P2.5V_LAN	RTL8100	
P1.8V_AUX	DDR2 P1.8V RS600	
P5.0V_AUX	THERMAL LCD P1.2V P5.0V	
P3.3V_AUX	MDC MICOM MINIPCI EXP-CARD SB600 THERMAL	
P12.0V_ALWS	P1.5V P3.3V P1.8V	
P5.0V_ALWS	P3.3V DDR2-PWR	
P3.3V_MICOM	THERMAL SB600 MICOM LED P1.8V_ALWS	
P1.2V_ALWS	SB600,P1.2V	
VDC	Primary DC system power supply (7 to 21V)	

CPU Core Voltage Table IMVP-6

Active Mode		Active/Deeper Sleep Dual Mode Region		Deeper Sleep/Extended Deeper Sleep Dual Mode Region	
VID(6:0)	Voltage	VID(6:0)	Voltage	VID(6:0)	Voltage
0 0 0 0 0 0 0	1.5000 V	0 1 0 1 0 0 0	1.0000 V	1 0 1 0 0 0 1	0.4875 V
0 0 0 0 0 0 0	1.4875 V	0 1 0 1 0 0 0	0.9875 V	1 0 1 0 0 0 1	0.4750 V
0 0 0 0 0 0 1	1.4750 V	0 1 0 1 0 0 1	0.9750 V	1 0 1 0 0 0 1	0.4625 V
0 0 0 0 0 1 1	1.4625 V	0 1 0 1 0 0 1	0.9625 V	1 0 1 0 0 1 0	0.4500 V
0 0 0 0 1 0 0	1.4500 V	0 1 0 1 0 0 0	0.9500 V	1 0 1 0 1 0 1	0.4375 V
0 0 0 0 1 0 1	1.4375 V	0 1 0 1 0 0 1	0.9375 V	1 0 1 0 1 0 0	0.4250 V
0 0 0 0 1 1 0	1.4250 V	0 1 0 1 0 1 0	0.9250 V	1 0 1 0 1 1 1	0.4125 V
0 0 0 0 1 1 1	1.4125 V	0 1 0 1 0 1 1	0.9125 V	1 0 1 1 0 0 0	0.4000 V
0 0 0 1 0 0 0	1.4000 V	0 1 1 0 0 0 0	0.9000 V	1 0 1 1 0 0 1	0.3875 V
0 0 0 1 0 0 1	1.3875 V	0 1 1 0 0 0 1	0.8875 V	1 0 1 1 0 1 0	0.3750 V
0 0 0 1 0 1 0	1.3750 V	0 1 1 0 0 1 0	0.8750 V	1 0 1 1 0 1 1	0.3625 V
0 0 0 1 0 1 1	1.3625 V	0 1 1 0 0 1 1	0.8625 V	1 0 1 1 1 0 0	0.3500 V
0 0 0 1 1 0 0	1.3500 V	0 1 1 0 1 0 0	0.8500 V	1 0 1 1 1 0 1	0.3375 V
0 0 0 1 1 0 1	1.3375 V	0 1 1 0 1 0 1	0.8375 V	1 0 1 1 1 1 0	0.3250 V
0 0 0 1 1 1 0	1.3250 V	0 1 1 0 1 1 0	0.8250 V	1 0 1 1 1 1 1	0.3125 V
0 0 0 1 1 1 1	1.3125 V	0 1 1 0 1 1 1	0.8125 V	1 1 0 0 0 0 0	0.3000 V
0 0 1 0 0 0 0	1.3000 V	0 1 1 1 0 0 0	0.8000 V	1 1 0 0 0 0 1	0.2875 V
0 0 1 0 0 0 1	1.2875 V	0 1 1 1 0 0 1	0.7875 V	1 1 0 0 0 1 0	0.2750 V
0 0 1 0 0 1 0	1.2750 V	0 1 1 1 0 1 0	0.7750 V	1 1 0 0 1 0 1	0.2625 V
0 0 1 0 0 1 1	1.2625 V	0 1 1 1 0 1 1	0.7625 V	1 1 0 0 1 1 0	0.2500 V
0 0 1 0 1 0 0	1.2500 V	0 1 1 1 1 0 0	0.7500 V	1 1 0 0 1 1 1	0.2375 V
0 0 1 0 1 0 1	1.2375 V	0 1 1 1 1 0 1	0.7375 V	1 1 0 0 1 1 0	0.2250 V
0 0 1 0 1 1 0	1.2250 V	0 1 1 1 1 1 0	0.7250 V	1 1 0 0 1 1 1	0.2125 V
0 0 1 0 1 1 1	1.2125 V	0 1 1 1 1 1 1	0.7125 V	1 1 0 1 0 0 0	0.2000 V
0 0 1 1 0 0 0	1.2000 V	1 0 0 0 0 0 0	0.7000 V	1 1 0 1 0 0 1	0.1875 V
0 0 1 1 0 0 1	1.1875 V	1 0 0 0 0 0 1	0.6875 V	1 1 0 1 0 1 0	0.1750 V
0 0 1 1 0 1 0	1.1750 V	1 0 0 0 0 1 0	0.6750 V	1 1 0 1 0 1 1	0.1625 V
0 0 1 1 0 1 1	1.1625 V	1 0 0 0 0 1 1	0.6625 V	1 1 0 1 1 0 0	0.1500 V
0 0 1 1 1 0 0	1.1500 V	1 0 0 0 1 0 0	0.6500 V	1 1 0 1 1 0 1	0.1375 V
0 0 1 1 1 0 1	1.1375 V	1 0 0 0 1 0 1	0.6375 V	1 1 0 1 1 1 0	0.1250 V
0 0 1 1 1 1 0	1.1250 V	1 0 0 0 1 1 0	0.6250 V	1 1 0 1 1 1 1	0.1125 V
0 0 1 1 1 1 1	1.1125 V	1 0 0 0 1 1 1	0.6125 V	1 1 1 0 0 0 0	0.1000 V
0 1 0 0 0 0 0	1.1000 V	1 0 0 0 1 0 0	0.6000 V	1 1 1 0 0 0 1	0.0875 V
0 1 0 0 0 0 1	1.0875 V	1 0 0 0 1 0 1	0.5875 V	1 1 1 0 0 1 0	0.0750 V
0 1 0 0 0 1 0	1.0750 V	1 0 0 0 1 0 0	0.5750 V	1 1 1 0 0 1 1	0.0625 V
0 1 0 0 0 1 1	1.0625 V	1 0 0 0 1 0 1	0.5625 V	1 1 1 0 1 0 0	0.0500 V
0 1 0 0 1 0 0	1.0500 V	1 0 0 0 1 1 0	0.5500 V	1 1 1 0 1 0 1	0.0375 V
0 1 0 0 1 0 1	1.0375 V	1 0 0 0 1 1 0	0.5375 V	1 1 1 0 1 1 0	0.0250 V
0 1 0 0 1 1 0	1.0250 V	1 0 0 0 1 1 1	0.5250 V	1 1 1 0 1 1 1	0.0125 V
0 1 0 0 1 1 1	1.0125 V	1 0 0 0 1 1 1	0.5125 V	1 1 1 1 0 0 0	0.0000 V
		1 0 0 1 0 0 0	0.5000 V	1 1 1 1 0 0 1	0.0000 V
				1 1 1 1 0 1 0	0.0000 V
				1 1 1 1 0 1 1	0.0000 V
				1 1 1 1 1 0 0	0.0000 V
				1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0	0.0000 V
				1 1 1 1 1 1 1	0.0000 V
				1 1 1 1 1 1 1	0.0000 V

I C / SMB Address

Devices	Address	Hex	Bus
SB600	Master	-	SMBUS Master
EMCN300(CPU Thermal Sensor)	1001 110X	9Ch	Thermal Sensor
SODIMM0	1010 0000	A0h	-
SODIMM1	1010 001X	A2h	-
ICS95411 (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable

USB PORT Assign

PORT NUMBER	ASSIGNED TO
0,1	SYSTEM PORT A
2	SYSTEM PORT B
4	EXPRESS CARD
5	4 IN 1 CARD
6	MINI CARD
8	BT

System Power States

CHP3_SLPS1* S1, Powered-On-Suspend(POS) : In this state, all clocks(except the 32.768KHz clock) are stopped. The system context is maintained in system DRAM. Power is maintained to PCI, the CPU, memory controller, memory, and all other critical subsystems. Memory is retained, and refreshes continue. All clocks stop except RTC clock. Note that this state does not preclude power being removed from non-essential devices, such as disk drives. During this state, CPU can be selected for either Deep Sleep or Deeper Sleep.

CHP3_SLPS3* S3, Suspend-To-RAM(STR) : The system context is maintained in system DRAM, but power is shut off to non-critical circuits. In Deeper Sleep, CPU voltage reduced in this state to reduce the leakage power.

CHP3_SLPS4* S4, Suspend-To-Disk(STD) : The Context of the system is maintained on the disk. All power is then shut off to the system except for the logic required to resume. Externally appears same as S5, but may have different wake events.

CHP3_SLPS5* S5, Soft Off(SOFF) : System context is not maintained. All power is shut off except for the logic required to restart. A full boot is required when waking.

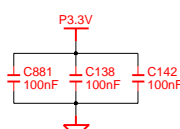
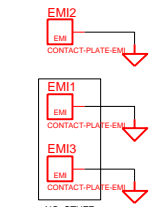
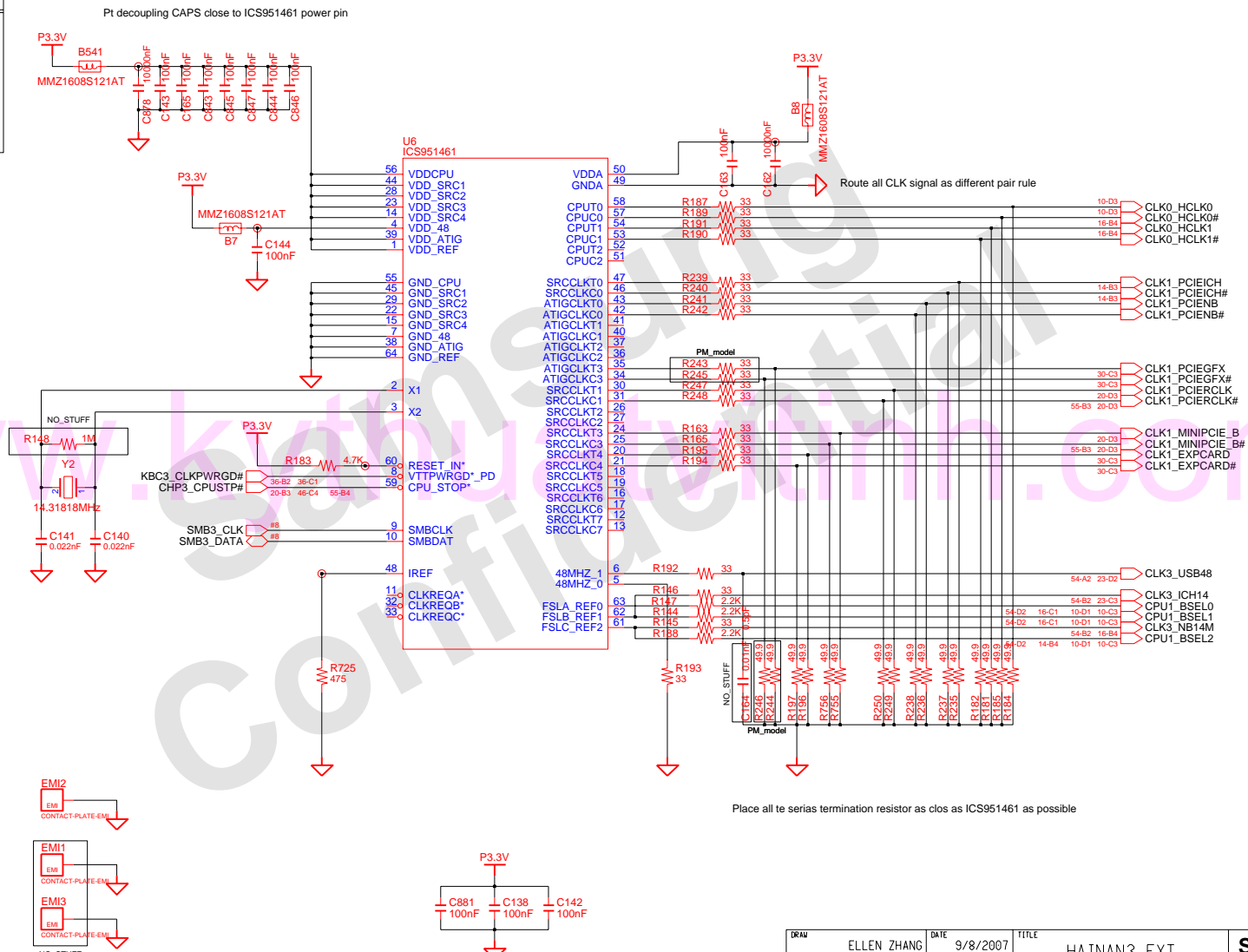
*Yonah Processor (2.33 GHz / 800 MHz : TBD)

DRAW	ELLEN ZHANG	DATE	9/8/2007	TITLE	HAINAN3_EXT	SAMSUNG ELECTRONICS PART NO. BA41-00809/810A
CHECK	ROKY ZHENG	DEV. STEP	MP1.1			
APPROVAL	KEVIN LEE	REV	1.0	ANNOTATIONS		
MODULE CODE	undef ined	LAST EDIT	September 8, 2007 12:02:16 PM	PAGE	7 OF 53	

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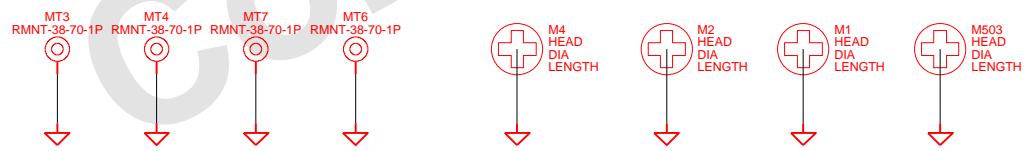
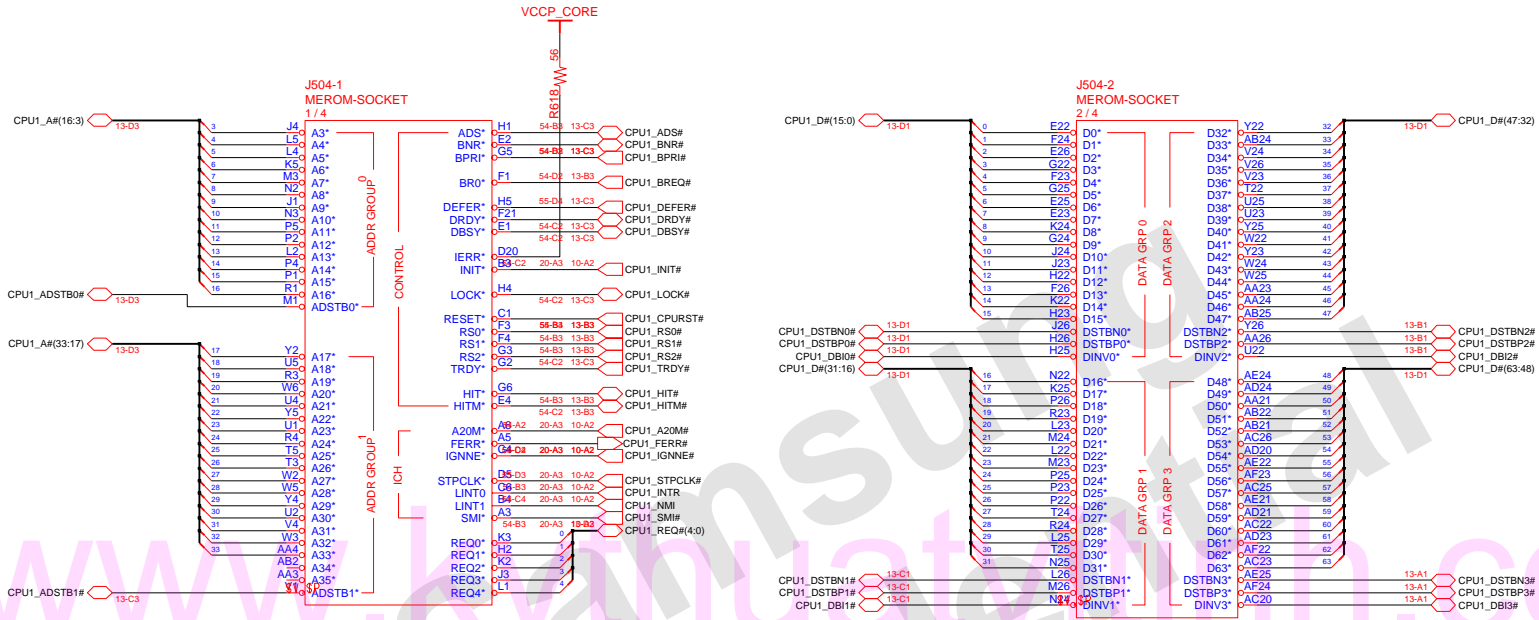
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CPU	FSA	FSB	FSC	HOST CLK
	BSEL0	BSEL1	BSEL2	
	0	0	0	266 MHz
	0	0	1	333 MHz
	0	1	0	200 MHz
	0	1	1	400 MHz
	1	0	0	133 MHz
	1	0	1	100 MHz
	1	1	0	166 MHz
	1	1	1	RSVD



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APPROVAL	KEVIN LEE	REV	1.0	MEROM(1/3)		PART NO. BA41-00809/810A
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CPU Core Voltage Table IMVP-6

Active Mode		Active/Deeper Sleep Dual Mode Region		Deeper Sleep/Extended Deeper Sleep Dual Mode Region	
VID(6:0)	Voltage	VID(6:0)	Voltage	VID(6:0)	Voltage
0 0 0 0 0 0 0	1.5000 V	0 1 0 1 0 0 0	1.0000 V	1 0 1 0 0 0 1	0.4875 V
0 0 0 0 0 0 1	1.4875 V	0 1 0 1 0 0 1	0.9875 V	1 0 1 0 0 1 0	0.4750 V
0 0 0 0 0 1 0	1.4750 V	0 1 0 1 0 1 0	0.9750 V	1 0 1 0 0 1 1	0.4625 V
0 0 0 0 0 1 1	1.4625 V	0 1 0 1 1 0 0	0.9625 V	1 0 1 0 1 0 0	0.4500 V
0 0 0 0 1 0 0	1.4500 V	0 1 0 1 1 0 1	0.9500 V	1 0 1 0 1 0 1	0.4375 V
0 0 0 0 1 0 1	1.4375 V	0 1 0 1 1 1 0	0.9375 V	1 0 1 0 1 1 0	0.4250 V
0 0 0 0 1 1 0	1.4250 V	0 1 0 1 1 1 1	0.9250 V	1 0 1 1 0 0 0	0.4125 V
0 0 0 0 1 1 1	1.4125 V	0 1 1 0 0 0 0	0.9125 V	1 0 1 1 0 0 1	0.4000 V
0 0 0 1 0 0 0	1.4000 V	0 1 1 0 0 0 1	0.9000 V	1 0 1 1 0 0 1	0.3875 V
0 0 0 1 0 0 1	1.3875 V	0 1 1 0 0 1 0	0.8875 V	1 0 1 1 0 1 0	0.3750 V
0 0 0 1 0 1 0	1.3750 V	0 1 1 0 0 1 1	0.8750 V	1 0 1 1 0 1 1	0.3625 V
0 0 0 1 0 1 1	1.3625 V	0 1 1 0 1 0 0	0.8625 V	1 0 1 1 1 0 0	0.3500 V
0 0 0 1 1 0 0	1.3500 V	0 1 1 0 1 0 1	0.8500 V	1 0 1 1 1 0 1	0.3375 V
0 0 0 1 1 0 1	1.3375 V	0 1 1 0 1 1 0	0.8375 V	1 0 1 1 1 1 0	0.3250 V
0 0 0 1 1 1 0	1.3250 V	0 1 1 1 0 0 0	0.8250 V	1 0 1 1 1 1 1	0.3125 V
0 0 0 1 1 1 1	1.3125 V	0 1 1 1 0 0 1	0.8125 V	1 1 0 0 0 0 0	0.3000 V
0 0 1 0 0 0 0	1.3000 V	0 1 1 1 0 0 1	0.8000 V	1 1 0 0 0 0 1	0.2875 V
0 0 1 0 0 0 1	1.2875 V	0 1 1 1 0 1 0	0.7875 V	1 1 0 0 0 1 0	0.2750 V
0 0 1 0 0 1 0	1.2750 V	0 1 1 1 0 1 1	0.7750 V	1 1 0 0 0 1 1	0.2625 V
0 0 1 0 0 1 1	1.2625 V	0 1 1 1 1 0 0	0.7625 V	1 1 0 0 1 0 0	0.2500 V
0 0 1 0 1 0 0	1.2500 V	0 1 1 1 1 0 1	0.7500 V	1 1 0 0 1 0 1	0.2375 V
0 0 1 0 1 0 1	1.2375 V	0 1 1 1 1 1 0	0.7375 V	1 1 0 0 1 1 0	0.2250 V
0 0 1 0 1 1 0	1.2250 V	0 1 1 1 1 1 1	0.7250 V	1 1 0 0 1 1 1	0.2125 V
0 0 1 1 0 0 0	1.2125 V	0 1 1 1 1 1 1	0.7125 V	1 1 0 1 0 0 0	0.2000 V
0 0 1 1 0 0 1	1.2000 V	1 0 0 0 0 0 0	0.7000 V	1 1 0 1 0 0 1	0.1875 V
0 0 1 1 0 1 0	1.1875 V	1 0 0 0 0 0 1	0.6875 V	1 1 0 1 0 1 0	0.1750 V
0 0 1 1 0 1 1	1.1750 V	1 0 0 0 0 1 0	0.6750 V	1 1 0 1 0 1 1	0.1625 V
0 0 1 1 1 0 0	1.1625 V	1 0 0 0 1 0 0	0.6625 V	1 1 0 1 1 0 0	0.1500 V
0 0 1 1 1 0 1	1.1500 V	1 0 0 0 1 0 1	0.6500 V	1 1 0 1 1 0 1	0.1375 V
0 0 1 1 1 1 0	1.1375 V	1 0 0 0 1 1 0	0.6375 V	1 1 0 1 1 1 0	0.1250 V
0 0 1 1 1 1 1	1.1250 V	1 0 0 0 1 1 1	0.6250 V	1 1 0 1 1 1 1	0.1125 V
0 0 1 0 0 0 0	1.1125 V	1 0 0 0 1 1 1	0.6125 V	1 1 1 0 0 0 0	0.1000 V
0 1 0 0 0 0 0	1.1000 V	1 0 0 1 0 0 0	0.6000 V	1 1 1 0 0 0 1	0.0875 V
0 1 0 0 0 0 1	1.0875 V	1 0 0 1 0 0 1	0.5875 V	1 1 1 0 0 1 0	0.0750 V
0 1 0 0 0 1 0	1.0750 V	1 0 0 1 0 1 0	0.5750 V	1 1 1 0 0 1 1	0.0625 V
0 1 0 0 0 1 1	1.0625 V	1 0 0 1 0 1 1	0.5625 V	1 1 1 0 1 0 0	0.0500 V
0 1 0 0 1 0 0	1.0500 V	1 0 0 1 0 1 1	0.5500 V	1 1 1 0 1 0 1	0.0375 V
0 1 0 0 1 0 1	1.0375 V	1 0 0 1 1 0 0	0.5375 V	1 1 1 0 1 0 1	0.0250 V
0 1 0 0 1 1 0	1.0250 V	1 0 0 1 1 1 0	0.5250 V	1 1 1 0 1 1 0	0.0125 V
0 1 0 0 1 1 1	1.0125 V	1 0 0 1 1 1 1	0.5125 V	1 1 1 0 1 1 1	0.0000 V
		1 0 1 0 0 0 0	0.5000 V	1 1 1 1 0 0 0	0.0000 V
		1 1 1 1 0 0 0	0.5000 V	1 1 1 1 0 0 1	0.0000 V
		1 1 1 1 0 0 1	0.5000 V	1 1 1 1 0 1 0	0.0000 V
		1 1 1 1 0 1 0	0.5000 V	1 1 1 1 0 1 1	0.0000 V
		1 1 1 1 1 0 0	0.5000 V	1 1 1 1 1 0 1	0.0000 V
		1 1 1 1 1 0 1	0.5000 V	1 1 1 1 1 1 0	0.0000 V
		1 1 1 1 1 1 0	0.5000 V	1 1 1 1 1 1 1	0.0000 V
		1 1 1 1 1 1 1	0.5000 V		

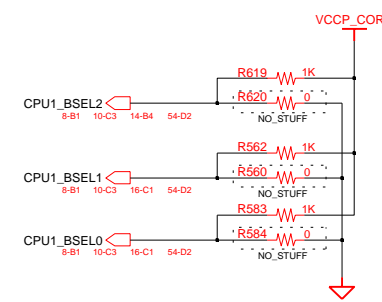
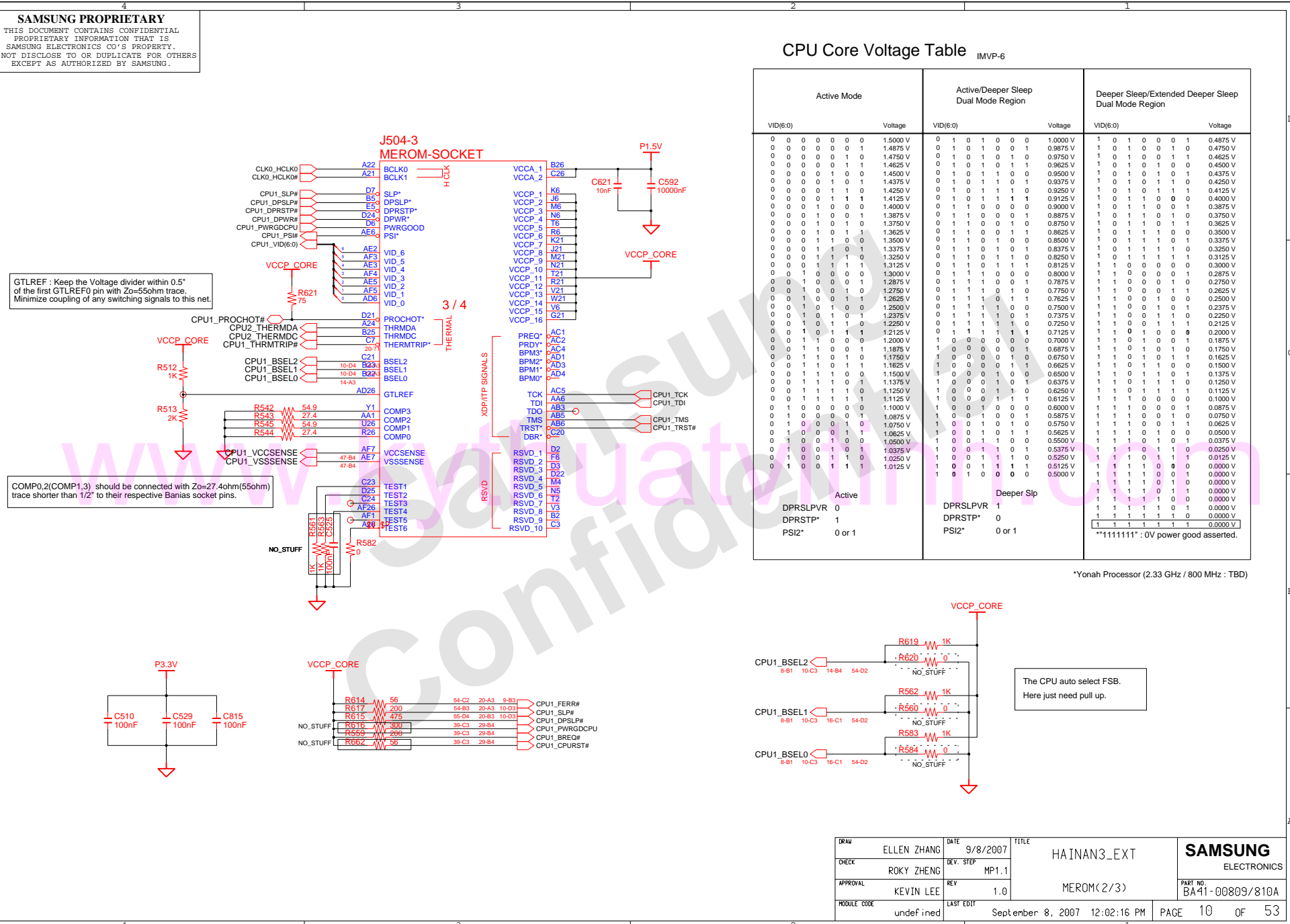
11111111 : 0V power good asserted.

*Yonah Processor (2.33 GHz / 800 MHz : TBD)

GTLREF : Keep the Voltage divider within 0.5" of the first GTLREF0 pin with Zo=55ohm trace. Minimize coupling of any switching signals to this net.

COMP0,2(COMP1,3) should be connected with Zo=27.4ohm(55ohm) trace shorter than 1/2" to their respective Banias socket pins.

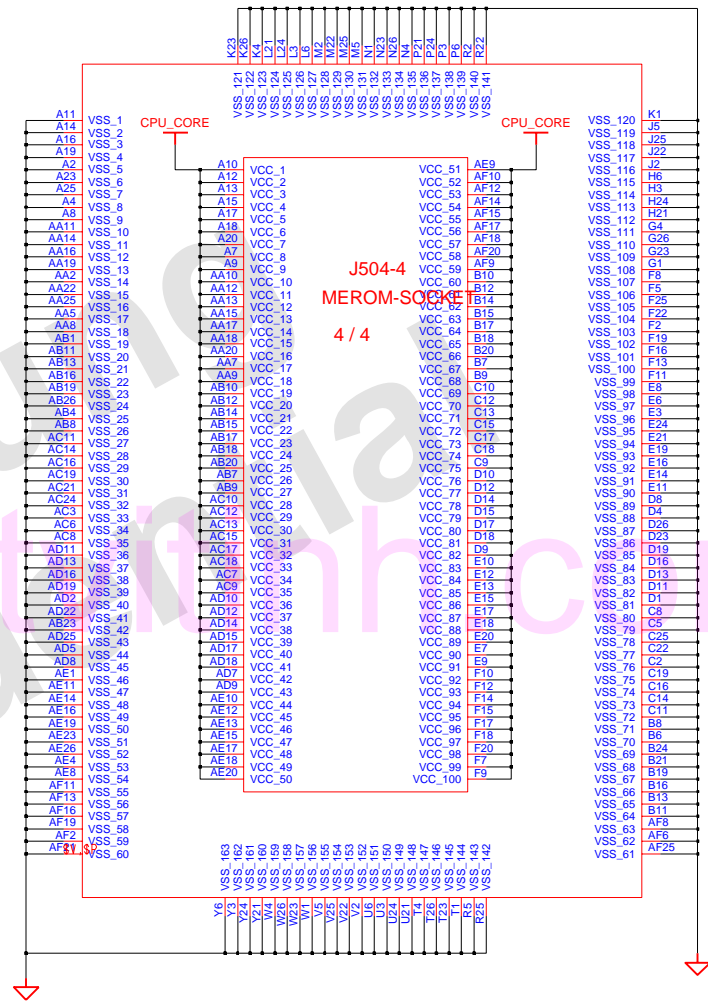
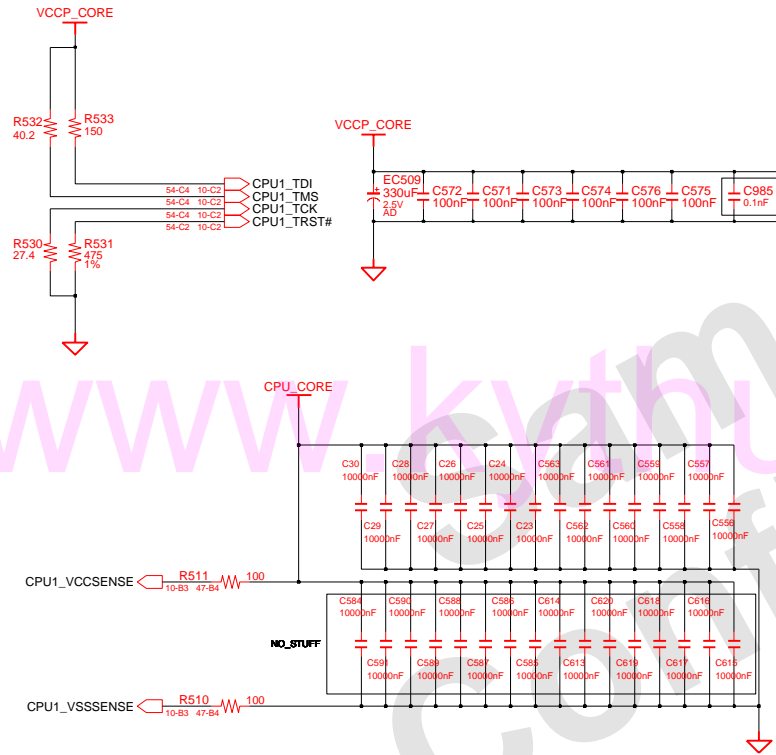
The CPU auto select FSB. Here just need pull up.



DRAW	ELLEN ZHANG	DATE	9/8/2007	TITLE	HAINAN3_EXT	SAMSUNG ELECTRONICS PART NO. BA41-00809/810A
CHECK	ROKY ZHENG	DEV. STEP	MP1.1			
APPROVAL	KEVIN LEE	REV	1.0	MEROM(2/3)		
MODULE CODE	undef ined	LAST EDIT	September 8, 2007 12:02:16 PM	PAGE	10 OF 53	

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DRAW	ELLEN ZHANG	DATE	9/8/2007	TITLE	HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK	ROKY ZHENG	DEV. STEP	MP1.1			
APPROVAL	KEVIN LEE	REV	1.0		MEROM(3/3)	PART NO. BA41-00809/810A
MODULE CODE	undef ined	LAST EDIT	September 8, 2007 12:02:16 PM	PAGE	11	OF 53

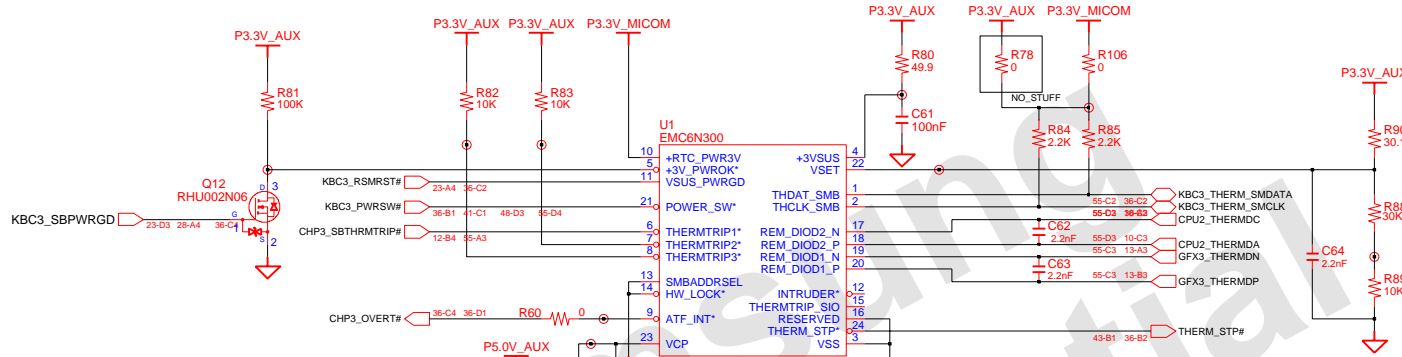
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CPU / RS600 Thermal Sensor

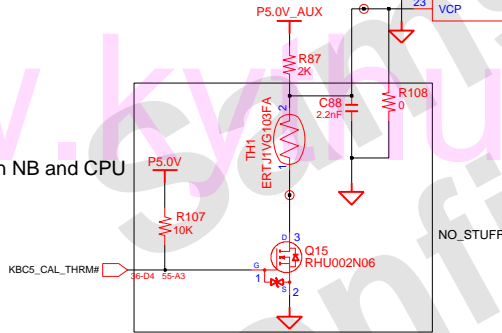
Refer To Thermal Sensor Layout Guidelines.

- Place the Thermal Sensor close to a remote diode.
- Keep traces away from high voltage (+12V bus)
- Keep traces away from fast data buses and CRT signal.
- Use recommended trace widths and spacings (10mil)
- Place a ground plane under the traces.
- Use guard traces flanking DXP and DXN and connecting to GND



PLACE THIS AT THE OPPOSITE SIDE OF CPU

Place between NB and CPU



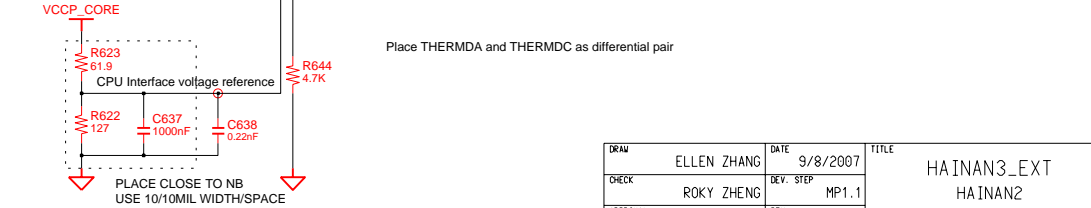
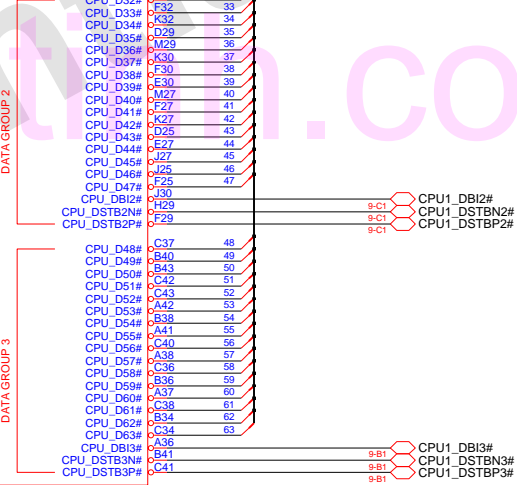
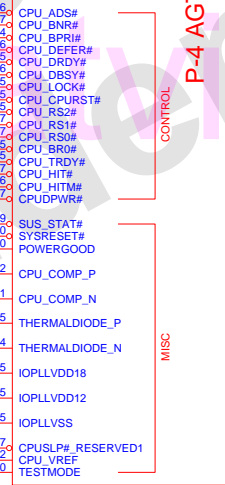
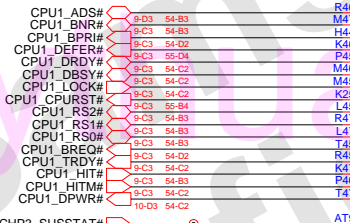
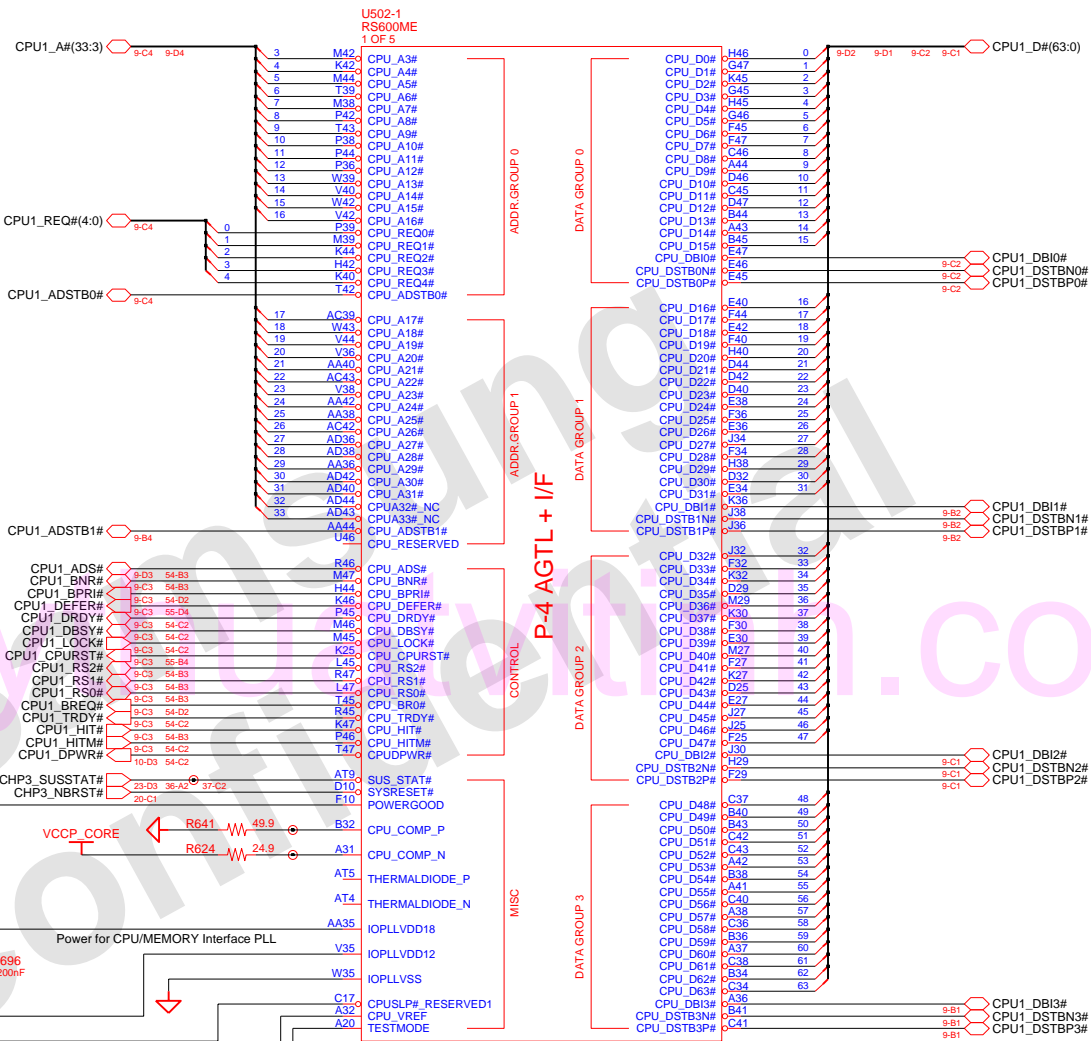
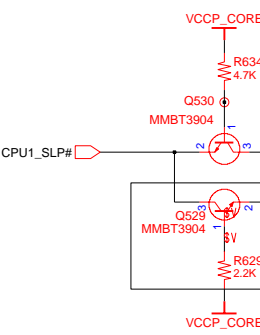
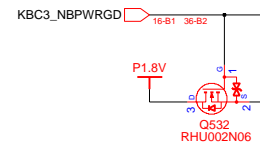
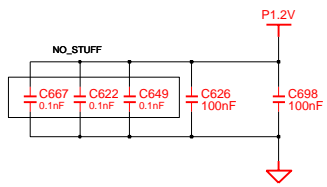
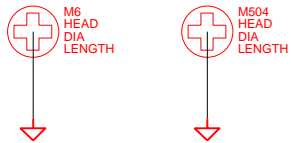
FAN Control Logic



DRAW	ELLEN ZHANG	DATE	9/8/2007	TITLE	HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK	ROKY ZHENG	DEV. STEP	MP1.1			
APPROVAL	KEVIN LEE	REV	1.0	THERMAL & FAN		PART NO. BA41-00809/810A
MODULE CODE	undef ined	LAST EDIT	September 8, 2007 12:02:16 PM			PAGE 12 OF 53

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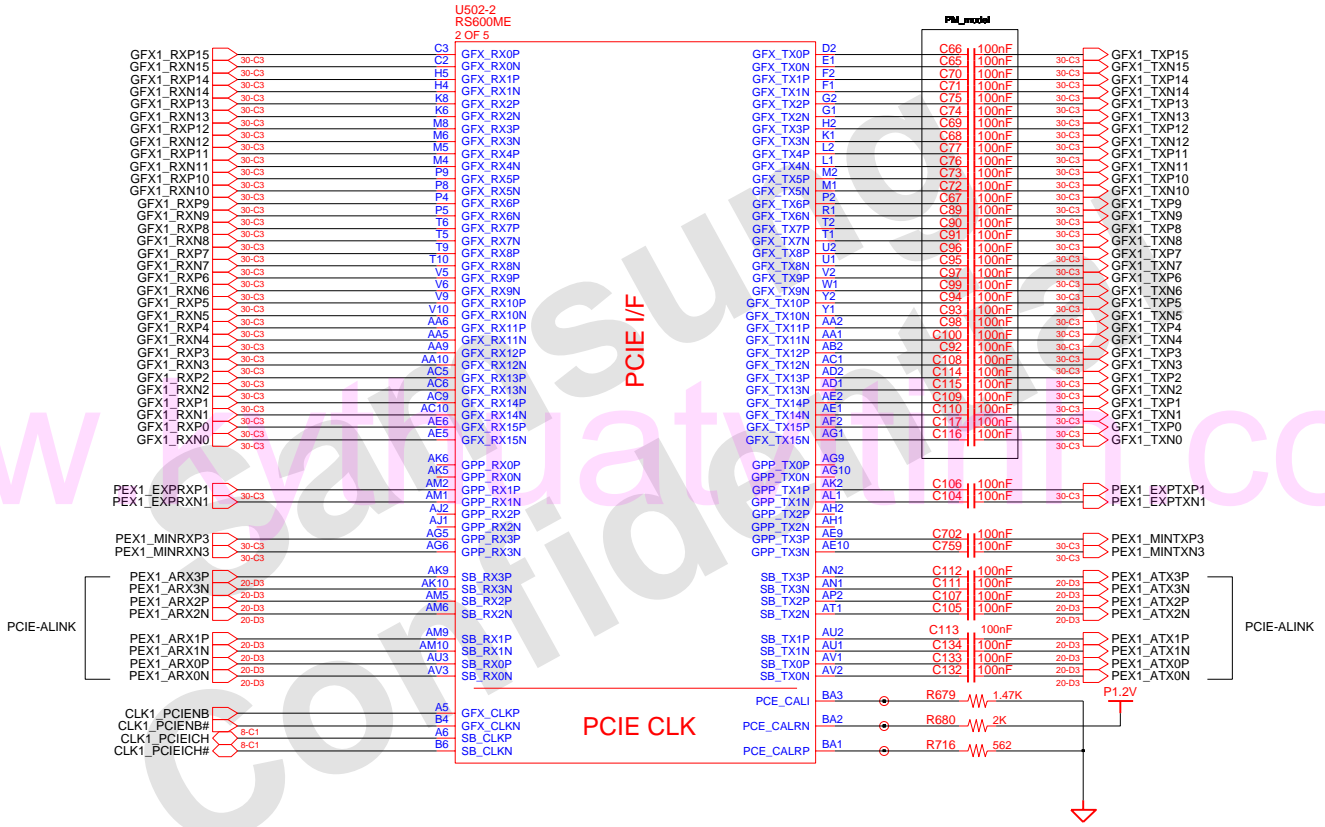
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DRAW	ELLEN ZHANG	DATE	9/8/2007	TITLE	HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK	ROKY ZHENG	DEV. STEP	MP1.1	HAINAN2	PART NO.	
APPROVAL	KEVIN LEE	REV	1.0	RS600 (1/5)	BA41-00809/810A	
MODULE CODE		LAST EDIT	September 8, 2007 12:02:16 PM	PAGE	13	OF 53

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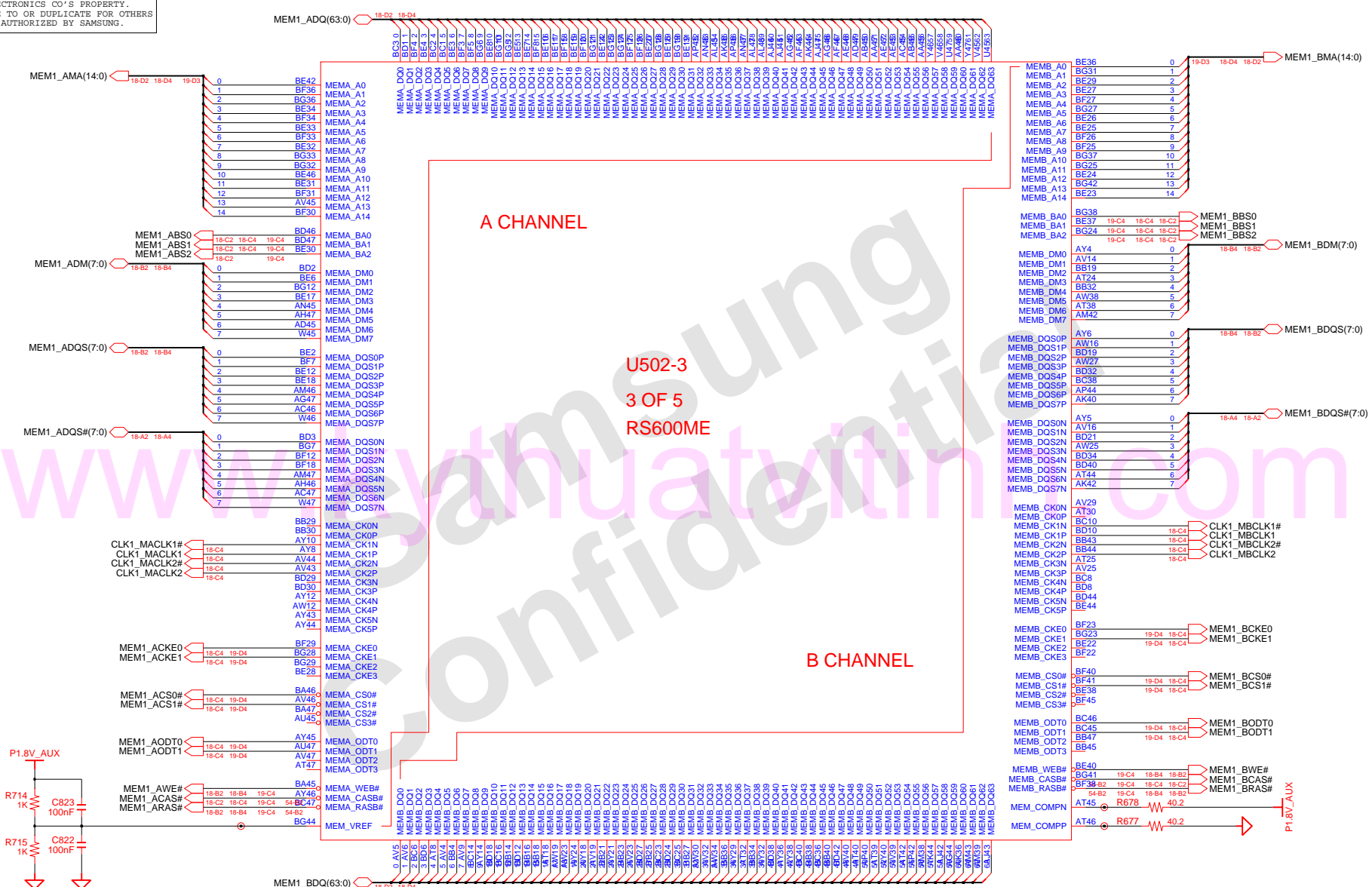
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DRAW	ELLEN ZHANG	DATE	9/8/2007	TITLE	HAINAN3_EXT HAINAN2 RS600 (2/5)	SAMSUNG ELECTRONICS PART NO. BA41-00809/810A
CHECK	ROKY ZHENG	DEV. STEP	MP1.1			
APPROVAL	KEVIN LEE	REV	1.0			
MODULE CODE		LAST EDIT	September 8, 2007 12:02:16 PM	PAGE	14 OF 53	

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A CHANNEL

B CHANNEL

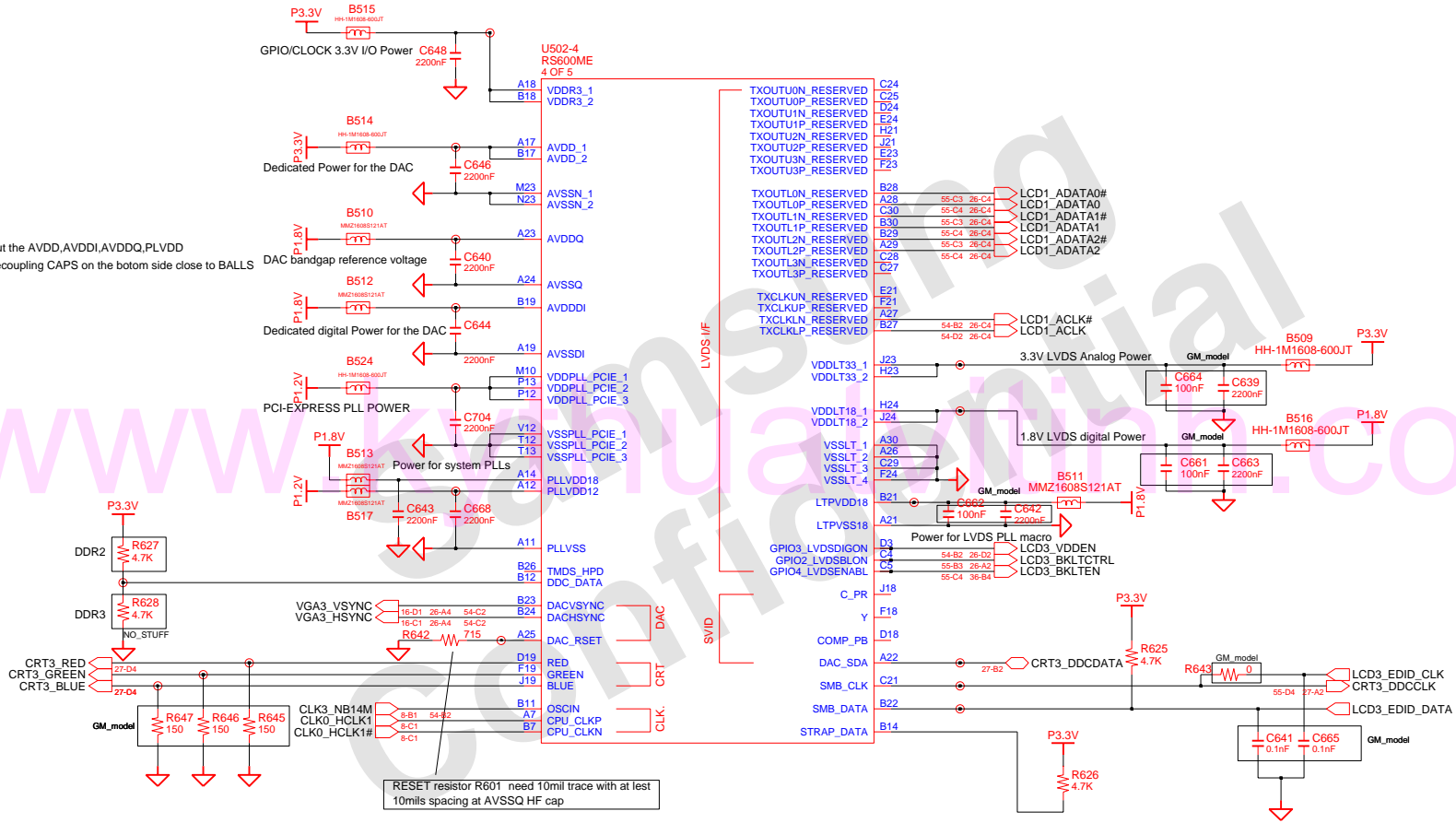
U502-3
3 OF 5
RS600ME

DRAW	ELLEN ZHANG	DATE	9/8/2007	TITLE	HAINAN3_EXT	SAMSUNG ELECTRONICS PART NO. BA41-00809/810A
CHECK	ROKY ZHENG	DEV. STEP	MP1.1		HAINAN2	
APPROVAL	KEVIN LEE	REV	1.0		RS600 (3/5)	
MODULE CODE		LAST EDIT	September 8, 2007 12:02:16 PM	PAGE	15	OF 53

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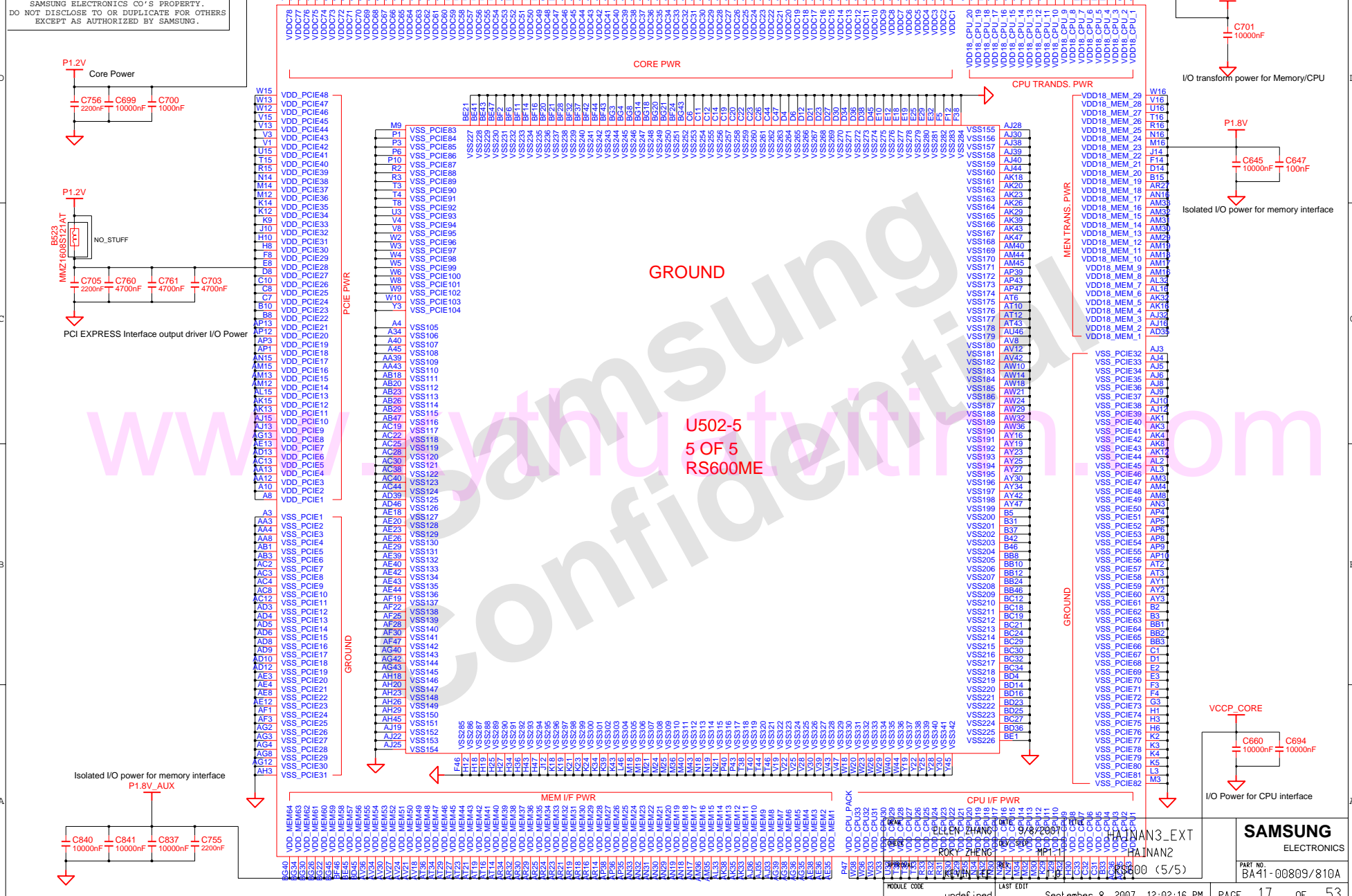
Put the AVDD, AVDDI, AVDDQ, PLVDD decoupling CAPS on the bottom side close to BALLS



DRAW	ELLEN ZHANG	DATE	9/8/2007	TITLE	HAINAN3_EXT	SAMSUNG ELECTRONICS PART NO. BA41-00809/810A
CHECK	ROKY ZHENG	DEV. STEP	MP1.1		HAINAN2	
APPROVAL	KEVIN LEE	REV	1.0		RS600 (4/5)	
MODULE CODE		LAST EDIT	September 8, 2007 12:02:16 PM		PAGE 16 OF 53	

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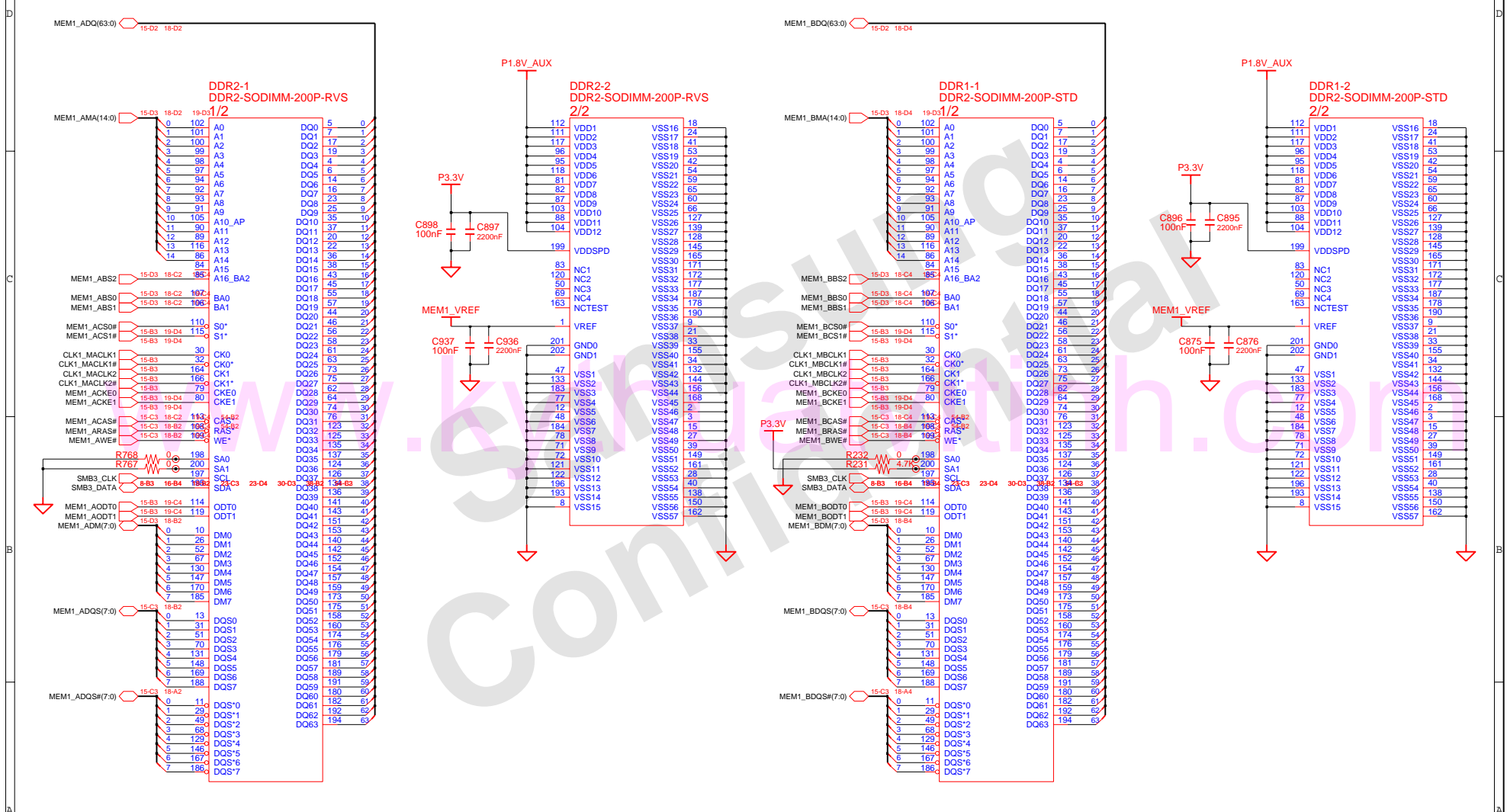


SAMSUNG
ELECTRONICS

PART NO.
BA41-00809/810A

REV. 1.1
KPS800 (5/5)

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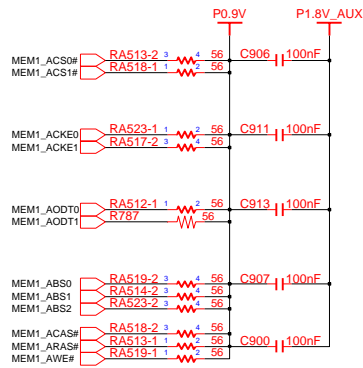


DRAW	ELLEN ZHANG	DATE	9/8/2007	TITLE	HAINAN3_EXT	SAMSUNG ELECTRONICS PART NO. BA41-00809/810A
CHECK	ROKY ZHENG	DEV. STEP	MP1.1			
APPROVAL	KEVIN LEE	REV	1.0		MEMORY SODIMM	
MODULE CODE	undef:ined	LAST EDIT	September 8, 2007 12:02:16 PM	PAGE	18	OF 53

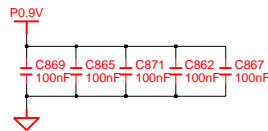
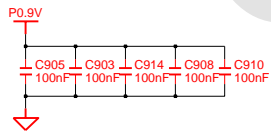
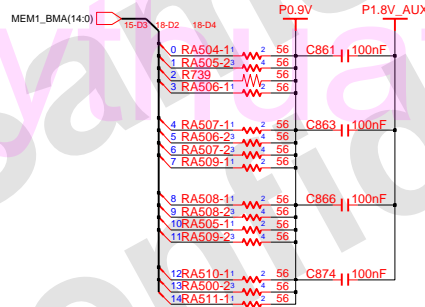
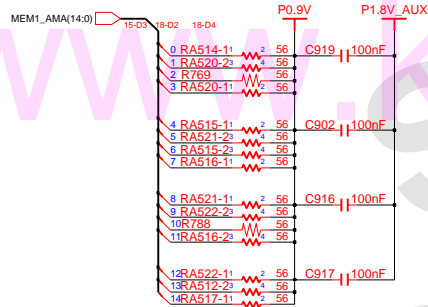
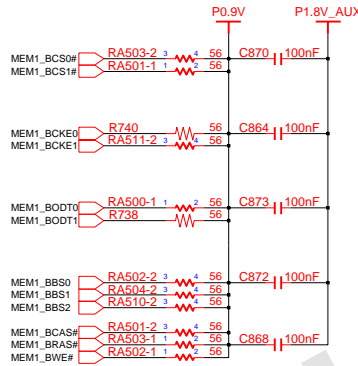
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Channel 1

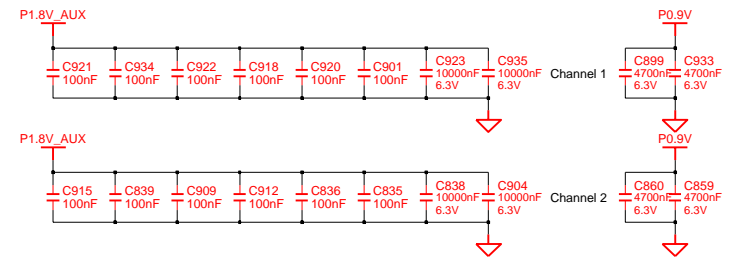
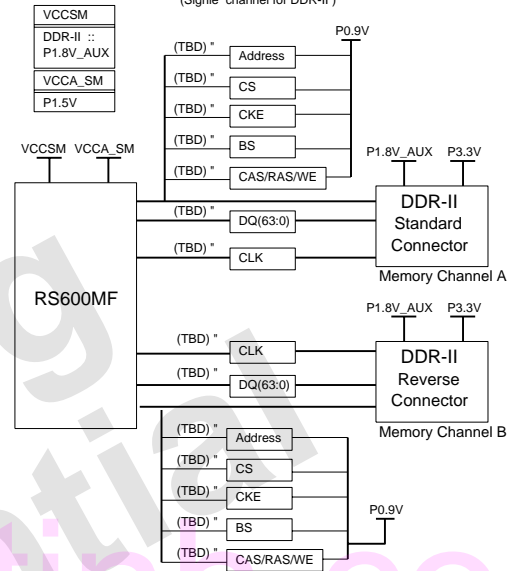


Channel 2



Memory Topology

(Single channel for DDR-II)

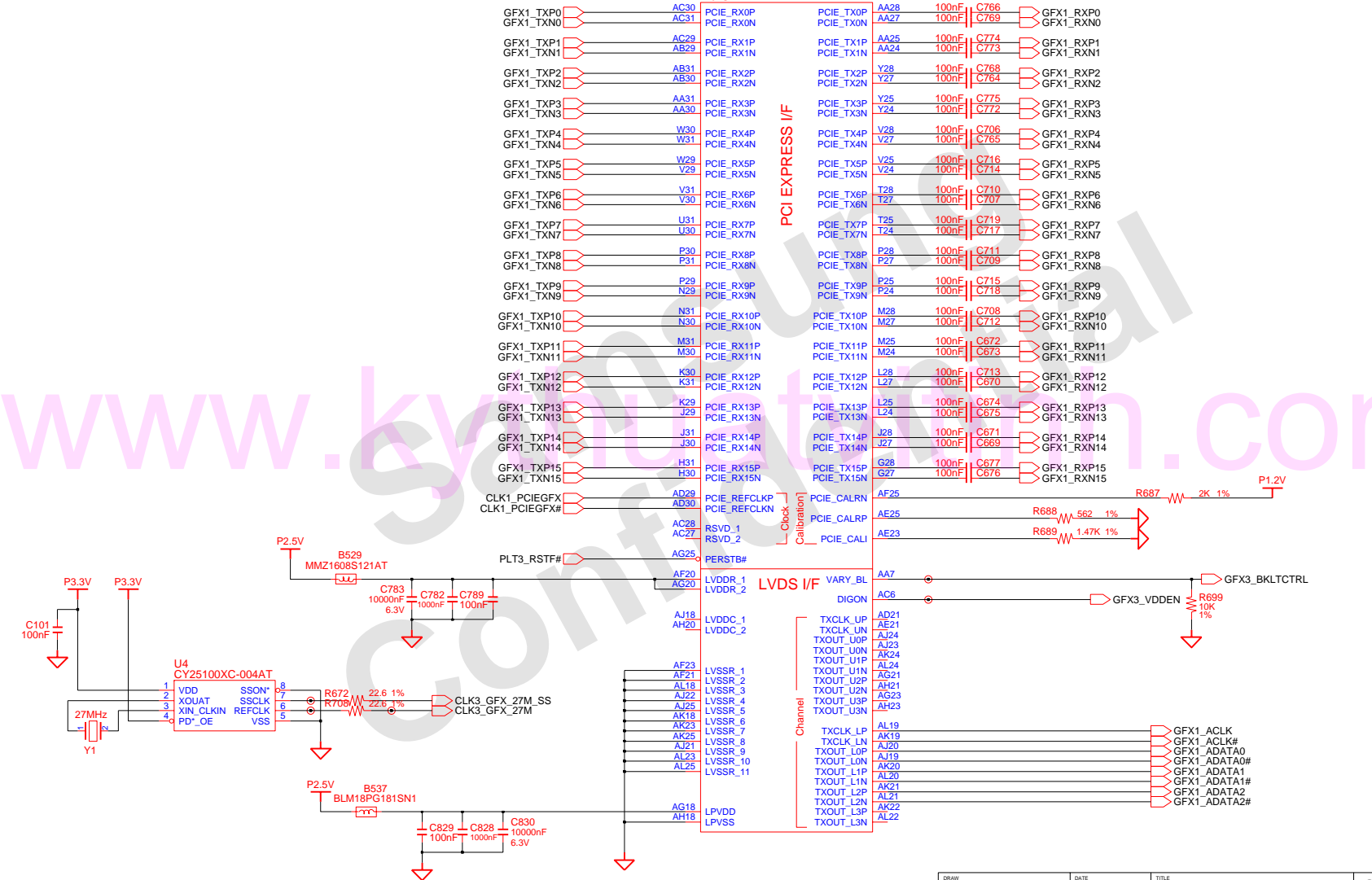


DRAW	ELLEN ZHANG	DATE	9/8/2007	TITLE	HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK	ROKY ZHENG	DEV. STEP	MP1.1			
APPROVAL	KEVIN LEE	REV	1.0		DDR2 TERMINATION	PART NO. BA41-00809/810A
MODULE CODE	undef ined	LAST EDIT	September 8, 2007 12:02:16 PM	PAGE	19	OF 53

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U3-1
216PWAACA13FG
 1 / 5

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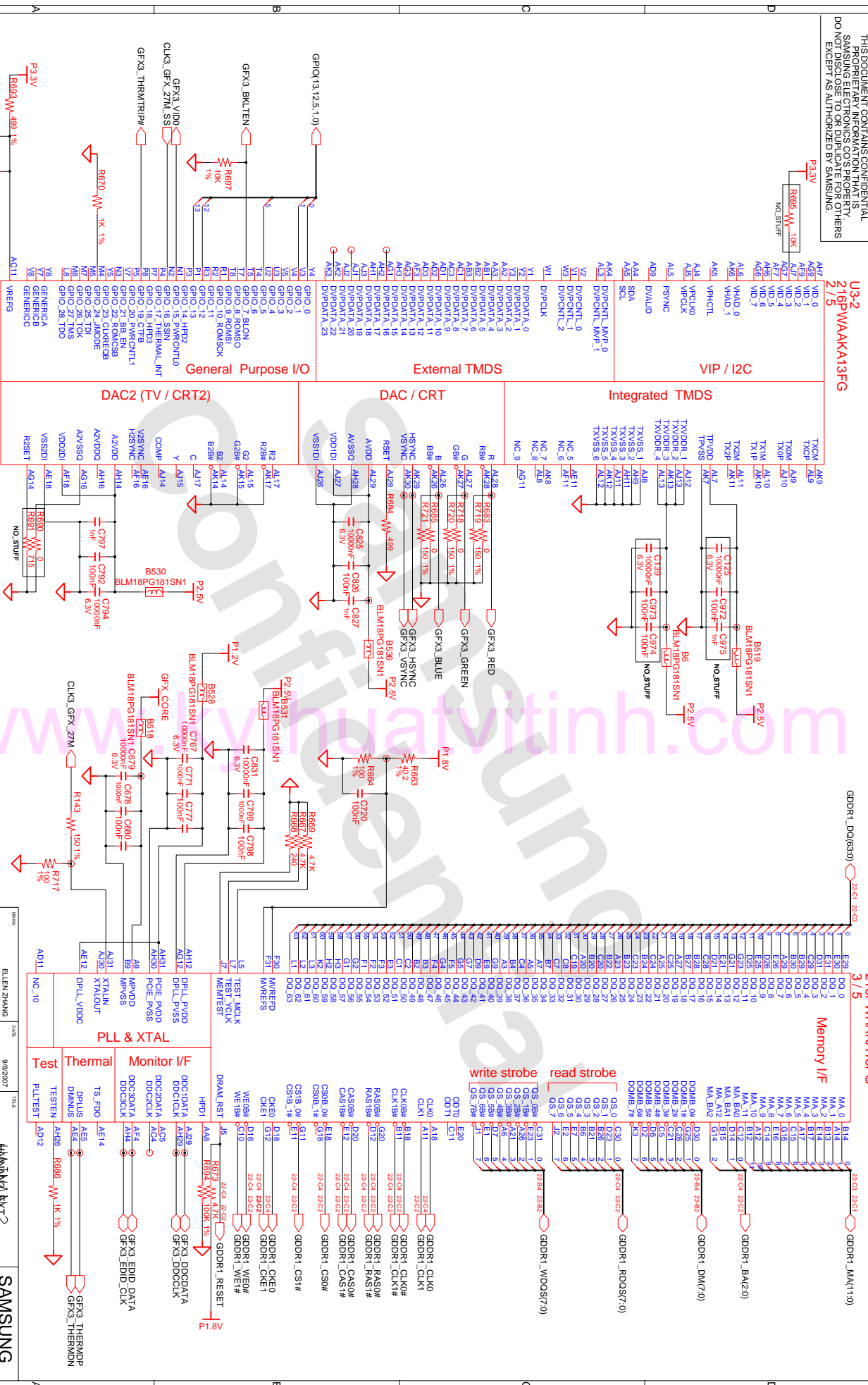


DRAW	ELLEN ZHANG	DATE	9/8/2007	TITLE	HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK	ROKY ZHENG	DEV STEP	MP1.1	MAIN		
APPROVAL	KEVIN LEE	REV	1.0	GFX (1)		PART NO. BA41-00809/810A
MODULE CODE		LAST EDIT			September 8, 2007 12:02:16 PM	PAGE 20 OF 53

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U3-2
216PWAKA13FG
 2 / 5

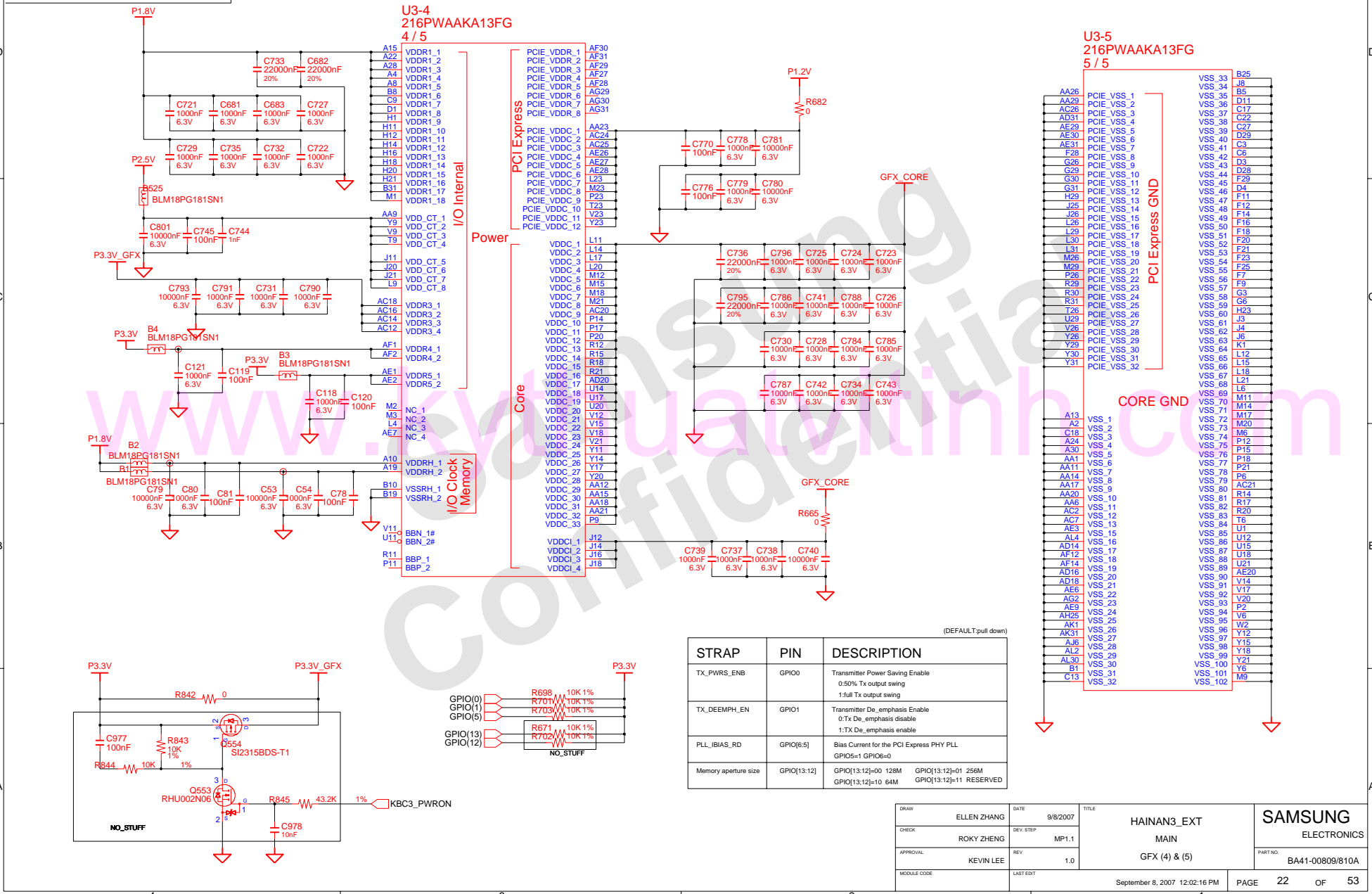
U3-3
216PWAKA13FG
 3 / 5



www.vietatvintinh.com

DESIGNER	ELEN ZHANG	DATE	9/8/2007	TIME	
CHECKER	ROKY ZHENG	ENC. STEP	MPI. 1		
APPROVAL	KEVIN LEE	REV.	1.0		
MODULE CODE		LAYER EDIT			
HAMMANN EXT 2		SAMSUNG		ELECTRONICS	
MAIN		BA41-00809/10A		PAGE 21 OF 53	
GFX (2/8/3)		September 8, 2007 12:02:16 PM		D:\mwan\mwan\exam\GHR_EXT_MPI.1_0907	

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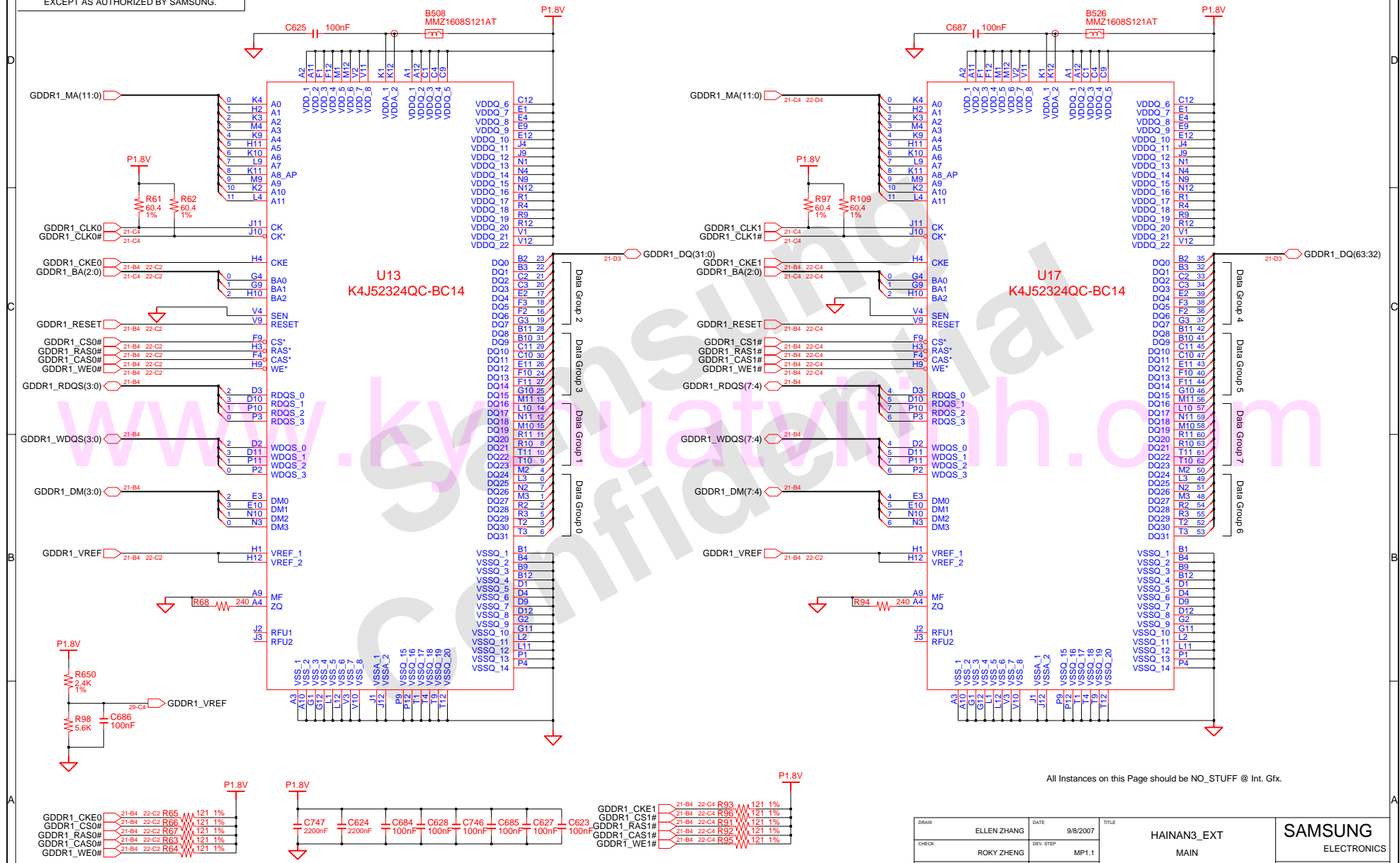


(DEFAULT:pull down)

STRAP	PIN	DESCRIPTION
TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0:50% Tx output swing 1:full Tx output swing
TX_DEEMPH_EN	GPIO1	Transmitter De-emphasis Enable 0:Tx De-emphasis disable 1:Tx De-emphasis enable
PLL_IBIAS_RD	GPIO[6:5]	Bias Current for the PCI Express PHY PLL GPIO[5]=1 GPIO[6]=0
Memory aperture size	GPIO[13:12]	GPIO[13:12]=00 128M GPIO[13:12]=01 256M GPIO[13:12]=10 64M GPIO[13:12]=11 RESERVED

DRAW	ELLEN ZHANG	DATE	9/8/2007	TITLE	HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK	ROKY ZHENG	DEV_STEP	MP1.1		MAIN	
APPROVAL	KEVIN LEE	REV	1.0		GFX (4) & (5)	PART NO. BA41-00809/810A
MODULE CODE		LAST EDIT			September 8, 2007 12:02:16 PM	PAGE 22 OF 53

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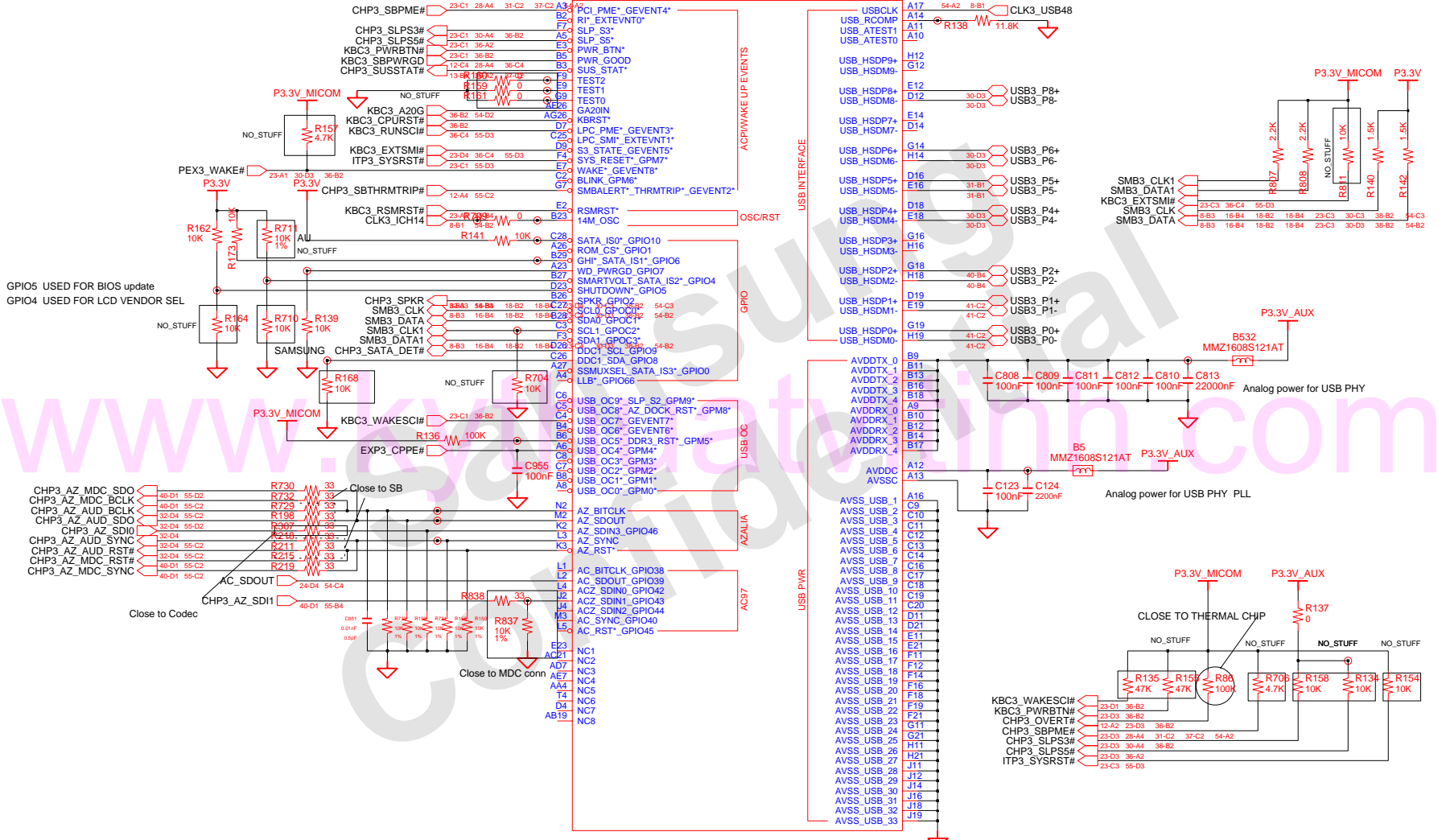
All Instances on this Page should be NO_STUFF @ Int. Gfx.

DRAW	ELLEN ZHANG	DATE	9/8/2007	TITLE	HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK	ROKY ZHENG	DEV. STEP	MP1.1	MAIN		
APPROVAL	KEVIN LEE	REV	1.0	GFX MEMORY		PART NO. BA41-00809/810A
MODULE CODE		LAST EDIT		September 8, 2007 12:02:16 PM	PAGE	23 OF 53

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**U19-2
218S6ECLA21FG
2 / 4**

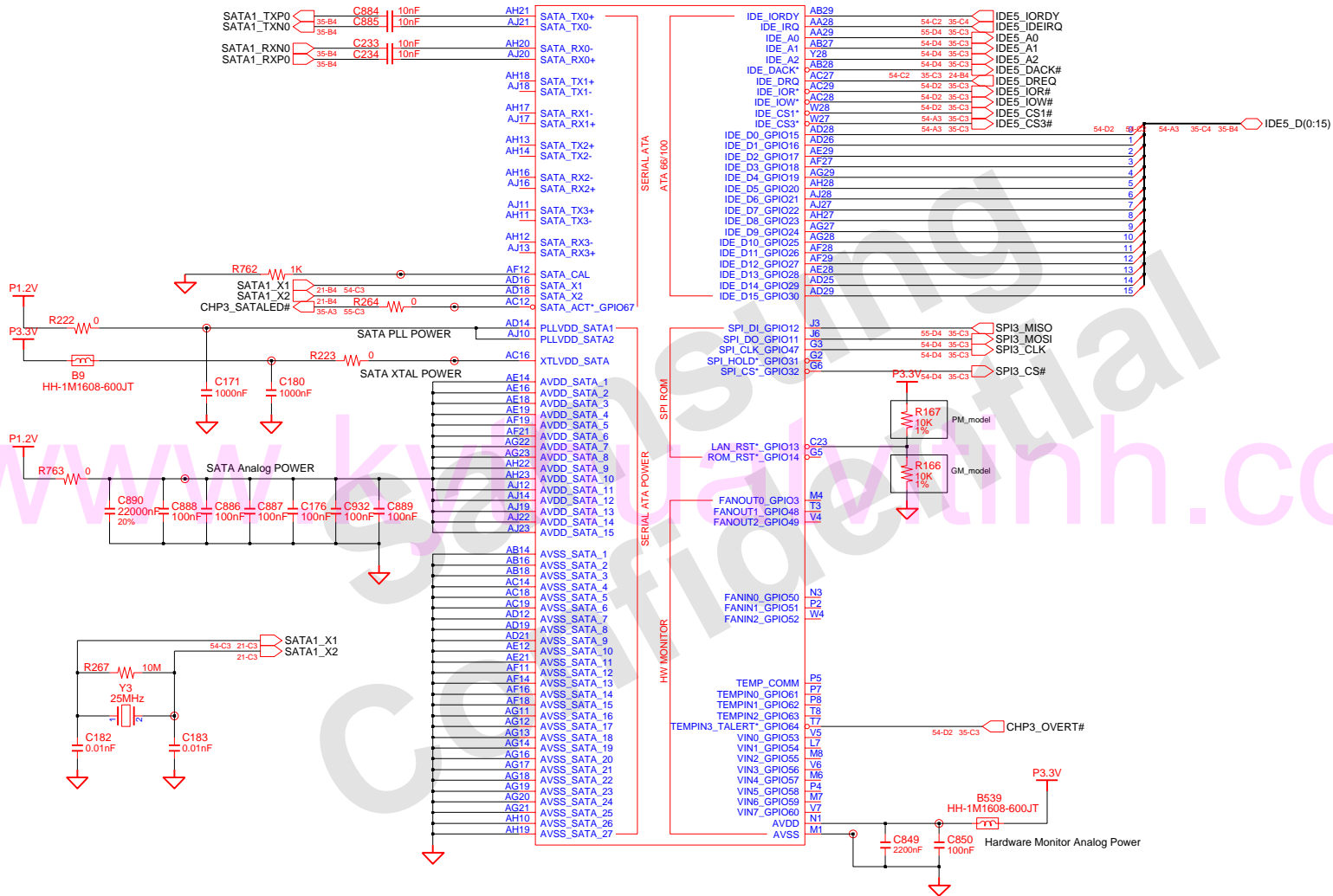


DRAW	ELLEN ZHANG	DATE	9/8/2007	TITLE	HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK	ROKY ZHENG	DEV. STEP	MP1.1			
APPROVAL	KEVIN LEE	REV	1.0		SB600(2/4)	PART NO. BA41-00809/810A
MODULE CODE	undef ined	LAST EDIT	September 8, 2007 12:02:16 PM	PAGE	25	OF 53

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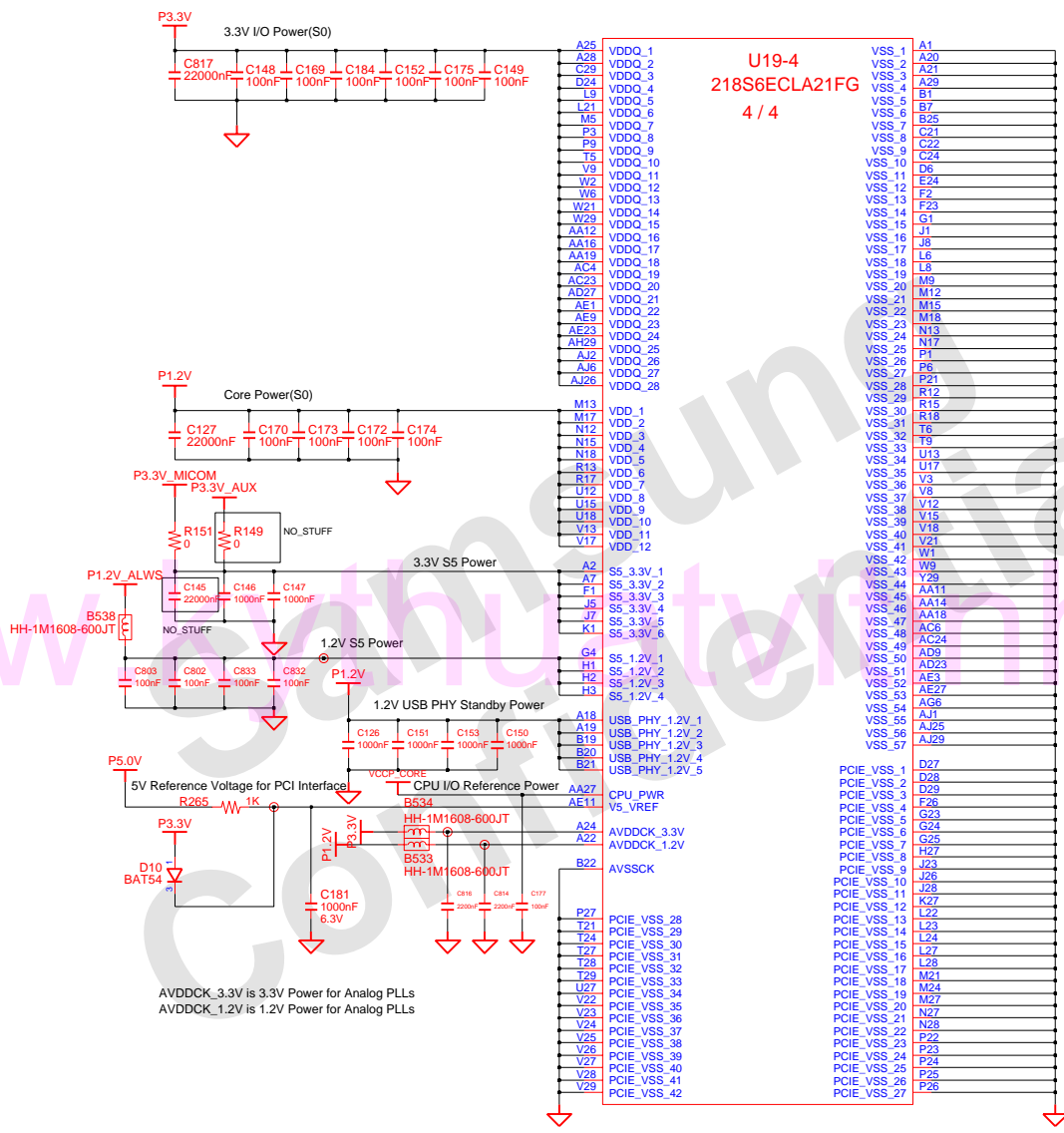
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U19-3
218S6ECLA21FG
3 / 4



DRAW	ELLEN ZHANG	DATE	9/8/2007	TITLE	HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK	ROKY ZHENG	DEV. STEP	MP1.1			
APPROVAL	KEVIN LEE	REV	1.0		SB600(3/4)	PART NO. BA41-00809/810A
MODULE CODE	undef ined	LAST EDIT	September 8, 2007 12:02:16 PM	PAGE	26	OF 53

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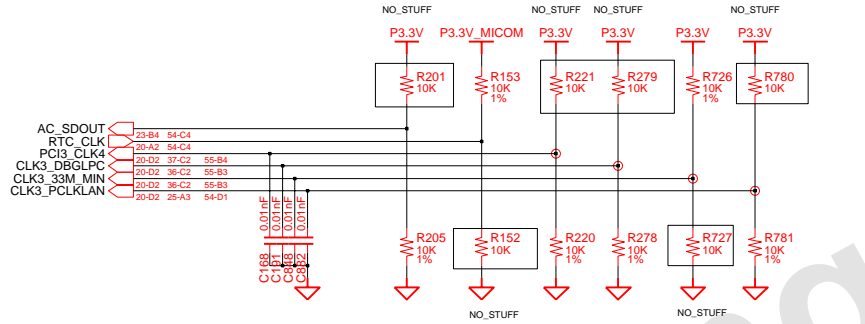


DRAW	ELLEN ZHANG	DATE	9/8/2007	TITLE	HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK	ROKY ZHENG	DEV. STEP	MP1.1			
APPROVAL	KEVIN LEE	REV	1.0		SB600(4/4)	PART NO. BA41-00809/810A
MODULE CODE	undef ined	LAST EDIT	September 8, 2007 12:02:16 PM	PAGE	27	OF 53

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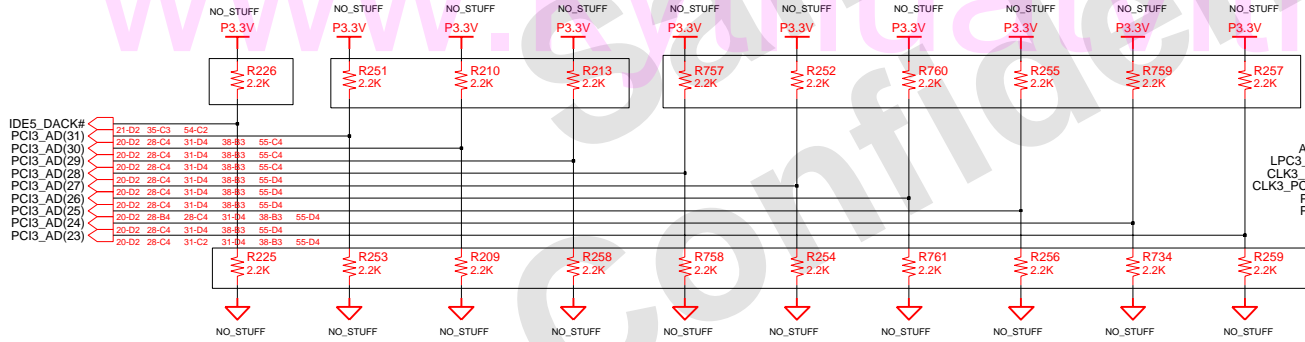
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REQUIRED SYSTEM STRAPS



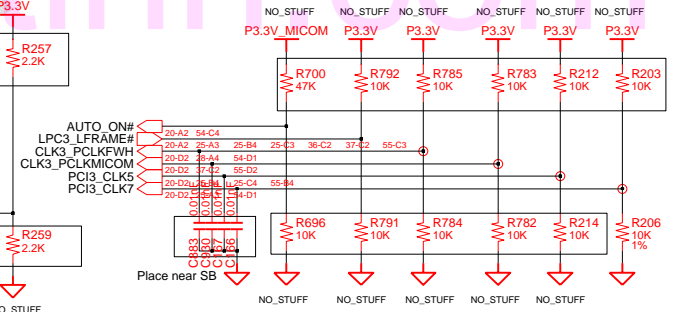
	AC_SDOUT	RTC_CLK	PCI3_CLK4	CLK3_DBG LPC	CLK3_33M_MIN, CLK3_PCLKLAN
STRAP HIGH	USE DEBUG STRAPS	INTERNAL RTC	USE INT PLL 48	CPU I/F = K8	ROM TYPE H.H = PCI ROM H.L = SPI ROM L.H = LPC ROM L.L = FWH ROM
STRAP LOW	IGNORE DEBUG STRAPS	EXRERNAL RTC	USE EXT 48MHZ	CPU I/F = P4	
	DEFAULT	DEFAULT	DEFAULT	DEFAULT	

DEBUG STRAPS



	IDE5_DACK*	PCI3_AD(31)	PCI3_AD(30)	PCI3_AD(29)	PCI3_AD(28)	PCI3_AD(27)	PCI3_AD(26)	PCI3_AD(25)	PCI3_AD(24)	PCI3_AD(23)
STRAP HIGH	RESERVED	RESERVED	RESERVED	RESERVED	USE LONG RESET	USE PCI PLL	USE ACPI BCLK	USE IDE PLL	USE DEFAULT PCIE STRAPS	BOOTF ALL TIMER DISABLED
STRAP LOW					USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	BYPASS EEPROM PCIE STRAPS	BOOTF ALL TIMER ENABLED

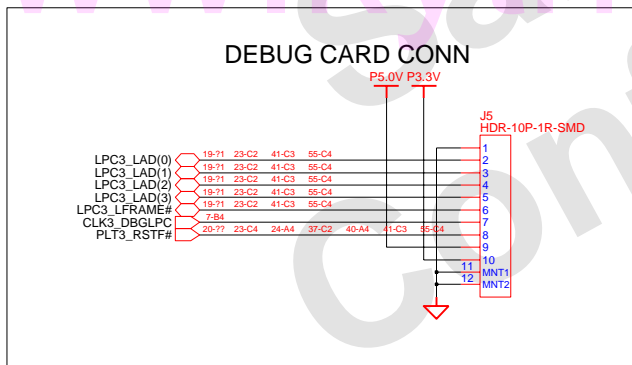
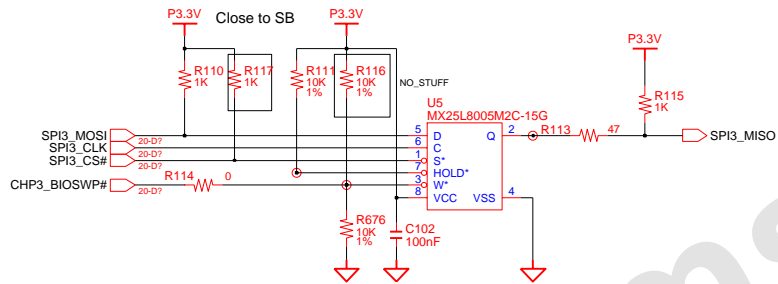
RESERVED PORT DEBUG



DRAW	ELLEN ZHANG	DATE	9/8/2007	TITLE	HAINAN3_EXT	SAMSUNG ELECTRONICS PART NO. BA41-00809/810A
CHECK	ROKY ZHENG	DEV. STEP	MP1.1			
APPROVAL	KEVIN LEE	REV	1.0	SB600 STRAPS		
MODULE CODE	undef ined	LAST EDIT	September 8, 2007 12:02:16 PM	PAGE	28 OF 53	

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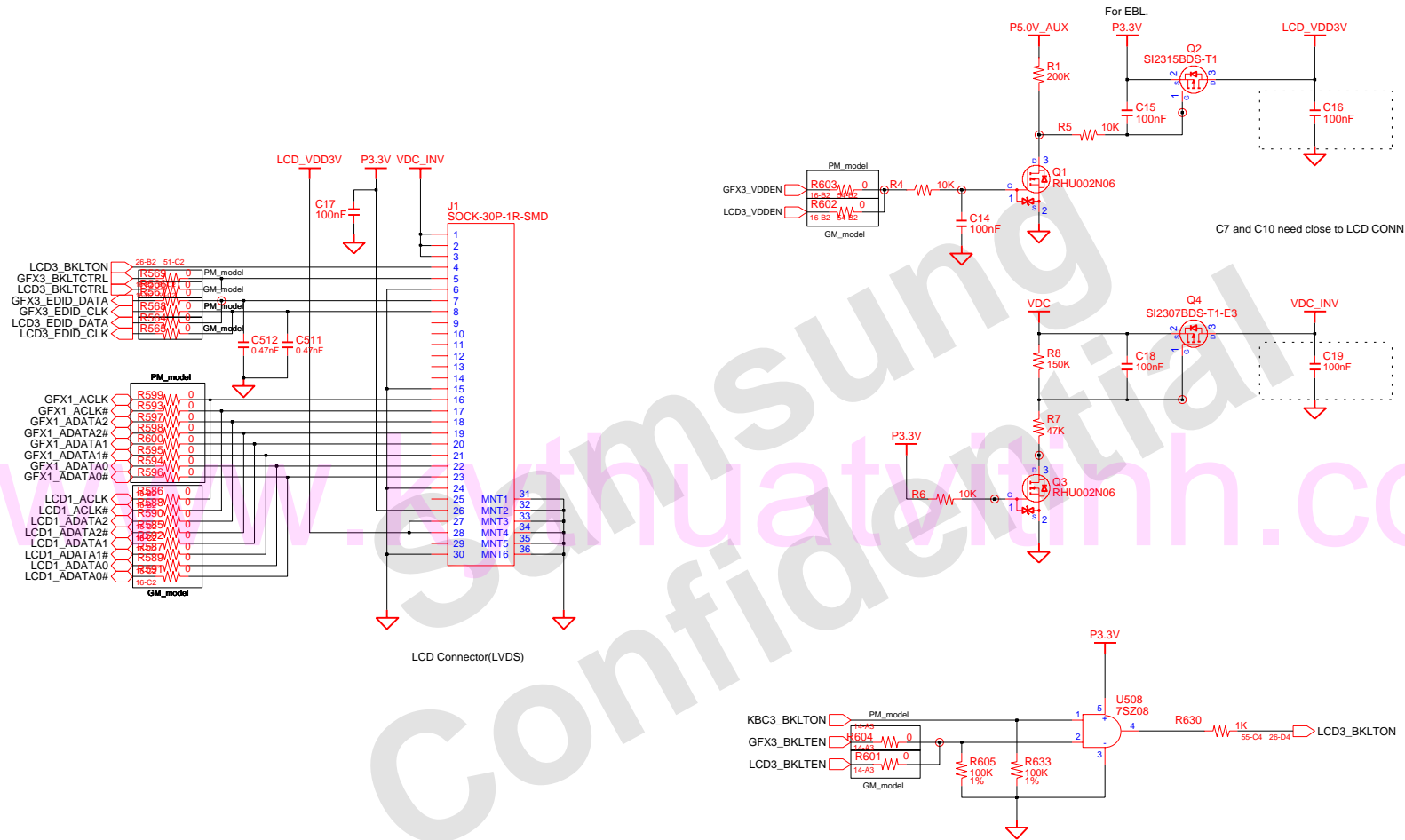


- | | |
|---|------------------------------------|
| 02 VERIFY REAL MODE | 66 CONFIGURE ADVANCE CACHE REG. |
| 03 DISABLE NMI | 6A DISPLAY EXTERNAL CACHE SIZE |
| 04 GET CPU TYPE | 6C DISPLAY SHADOW MESSAGE |
| 06 INIT. SYSTEM H/W | 6E DISPLAY NON-DISPOSABLE SEGMENT |
| 08 INIT. CHIPSET REG. | 70 DISPLAY ERROR MESSAGE |
| 09 SET IN POST FLAG | 72 CHECK FOR CONFIGURATION ERROR |
| 0A INIT CPU.REG | 74 TEST REAL-TIME CLOCK |
| 0B CPU CACHE ON | 76 CHECK FOR KEYBOARD ERROR |
| 0C INIT.CACHE TO POST | 7C SETUP HARDWARE INTERRUPT VECTOR |
| 0E INIT. I/O VALUE | 7E TEST COPROCESSER IF PRESENT |
| 0F ENABLE THE L-BUS IDE | 80 DISABLE ON-BOARD I/O PORT |
| 10 INIT. POWER MANAGER | 82 DETECT AND INSTALL EXT.RS232C |
| 11 LOAD ALTERNATE REG. | 84 DETECT AND INSTALL EXT.PARALLEL |
| 13 PCI BUS MASTER RESET WITH INITIAL POST VALUE | 86 RE-INIT. ON-BOARD I/O PORT |
| 14 INIT. KEYBOARD CONTROLLER | 88 INIT. BIOS DATA ROM |
| 16 CHECK CHECKSUM | 8A INIT.EXTENDED BIOS DATA AREA |
| 18 8254 TIMER INIT. | 8C INIT. FDD CONTROLLER |
| 1A 8237 DMA CONTROLLER INIT. | 9A SHADOW OPTION ROMS |
| 1C RESET INTERRUPT CONTROLLER | 9C SETUP POWER MANAGEMENT |
| 20 TEST DRAM REFRESH | 9E ENABLE H/W INTERRUPT |
| 22 TEST 8742 KEYBOARD CONTROLLER | A0 SET TIME OF DAY |
| 24 SET ES SEGMENT REG. TO 4GB | A4 INIT. TYPOMATIC RATE |
| 26 ENABLE A20 | A8 ERASE F2 PROMPT |
| 28 AUTO SIZING DRAM | AA SCAN FOR F2 KEY STROKE |
| 32 COMPUTE THE CPU SPEED | AC ENTER SETUP |
| 34 TESET CMOS RAM | AE CLEAR IN POST FLAG |
| 38 SHADOW SYSTEM BIOS ROM | B0 CHECK FOR ERRORS |
| 3A AUTO SIZING CACHE | B2 POST DONE-PREPARE TO BOOT O/S |
| 3C CONFIGURE ADVANCED CHIPSET REG. | B4 ONE BEEP |
| 3D LOAD ALTER REG. WITH CMOS VALUE | B6 CHECK PASSWORD (OPTION) |
| 42 INIT. INTERRUPT VECTOR | B7 ACPI INIT |
| 44 INIT. BIOS INTERRUPT | BA DMI INIT |
| 46 CHECK ROM COPYRIGHT NOTICE | BE CLEAR SCREEN |
| 47 INIT. I20 SUPPORT IF INSTALLED | C0 TRY BOOT WITH INT19 |
| 48 CHECK VIDEO CONFIGURE AGAINST CMOS | D0 INTERRUPT HANDLER ERROR |
| 49 INIT. PCI BUS AND DEVICE | D2 UNKNOWN INTERRUPT ERROR |
| 4A INIT. ALL VIDEO BIOS ROM | D4 PENDING INTERRUPT ERROR |
| 4C SHADOW VIDEO BIOS ROM | D6 SHUTDOWN 5 |
| 50 DISPLAY CPU TYPE AND SPEED | D8 SHUTDOWN ERROR |
| 52 TEST KEYBOARD | DA EXTENDED BLOCK MOVE |
| 54 SET KEYCLICK IF ENABLED | DC SHUTDOWN 10 |
| 56 ENABLE KEYBOARD | 89 ENABLE NMI |
| 58 TEST FOR UNEXPECTED INTERRUPTS | 90 INIT. HDD CONTROLLER |
| 5A DISPLAY " PRESS SETUP" | 91 INIT. LOCAL BUS HDD CONTROLLER |
| 5C TEST RAM BETWEEN 512K AND 640K | 92 JUMP TO USER PATCH 2 |
| 60 TEST EXTENDED MEMORY | 94 DISABLE A20 ADDRESS LINE |
| 62 TEST EXTENDED MEMORY ADDRESS LINE | 96 CLEAR HUGE ES SEGMENT REG. |
| 64 JUMP TO USER PATCH 1 | 98 SEARCH FOR OPTION ROMS |

DRAW	ELLEN ZHANG	DATE	9/8/2007	TITLE	HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK	ROKY ZHENG	DEV. STEP	MP1.1			
APPROVAL	KEVIN LEE	REV	1.0		FWH	PART NO. BA41-00809/810A
MODULE CODE	undef ined	LAST EDIT	September 8, 2007 12:02:16 PM	PAGE	29	OF 53

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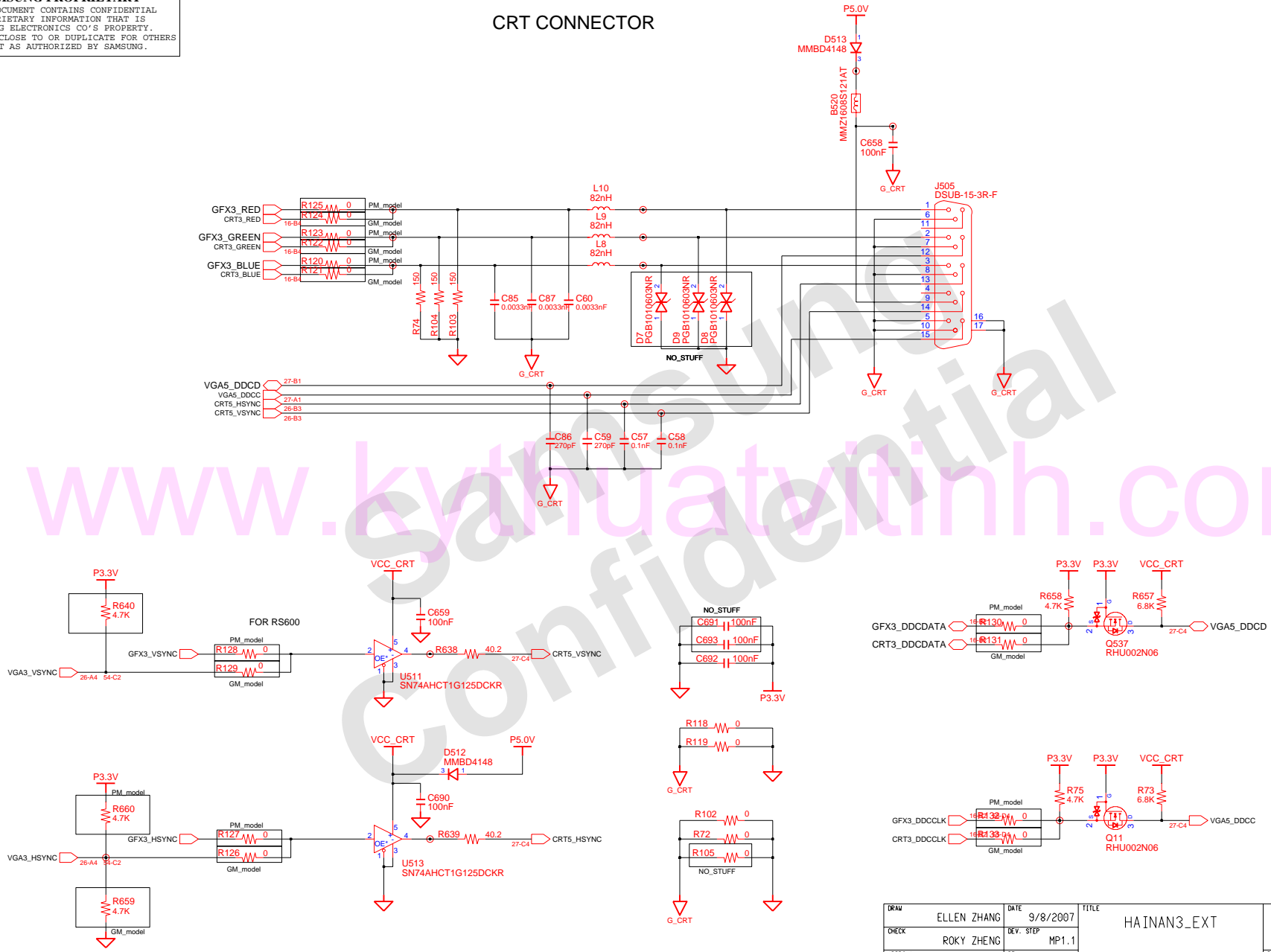
C7 and C10 need close to LCD CONN

DRAW	ELLEN ZHANG	DATE	9/8/2007	TITLE	HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK	ROKY ZHENG	DEV. STEP	MP1.1			
APPROVAL	KEVIN LEE	REV	1.0		LCD	PART NO. BA41-00809/810A
MODULE CODE	undef ined	LAST EDIT	September 8, 2007 12:02:16 PM	PAGE	30	OF 53

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CRT CONNECTOR

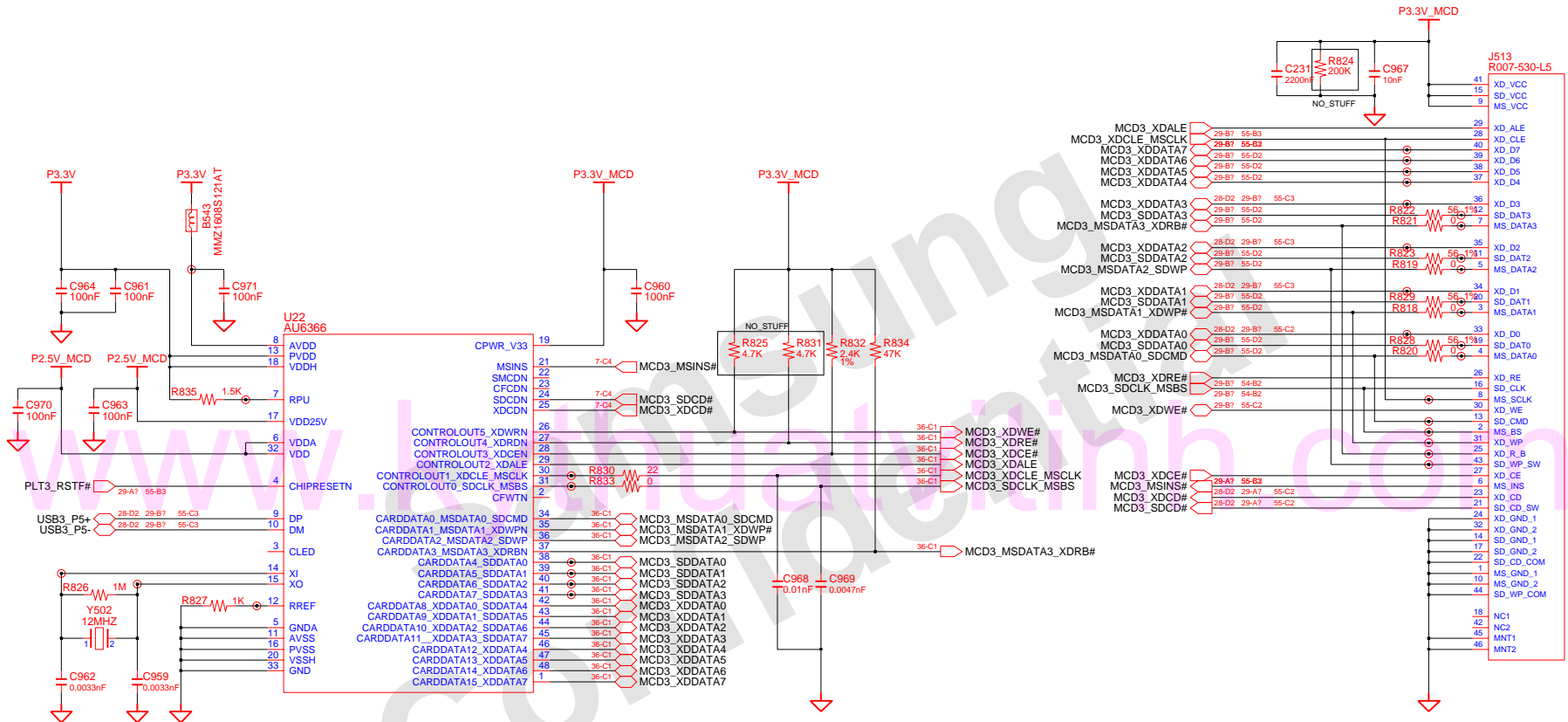


DRAW	ELLEN ZHANG	DATE	9/8/2007	TITLE	HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK	ROKY ZHENG	DEV. STEP	MP1.1			
APPROVAL	KEVIN LEE	REV	1.0		CRT	PART NO. BA41-00809/810A
MODULE CODE	undef:ined	LAST EDIT	September 8, 2007 12:02:16 PM	PAGE	31	OF 53

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4 IN 1 CARD

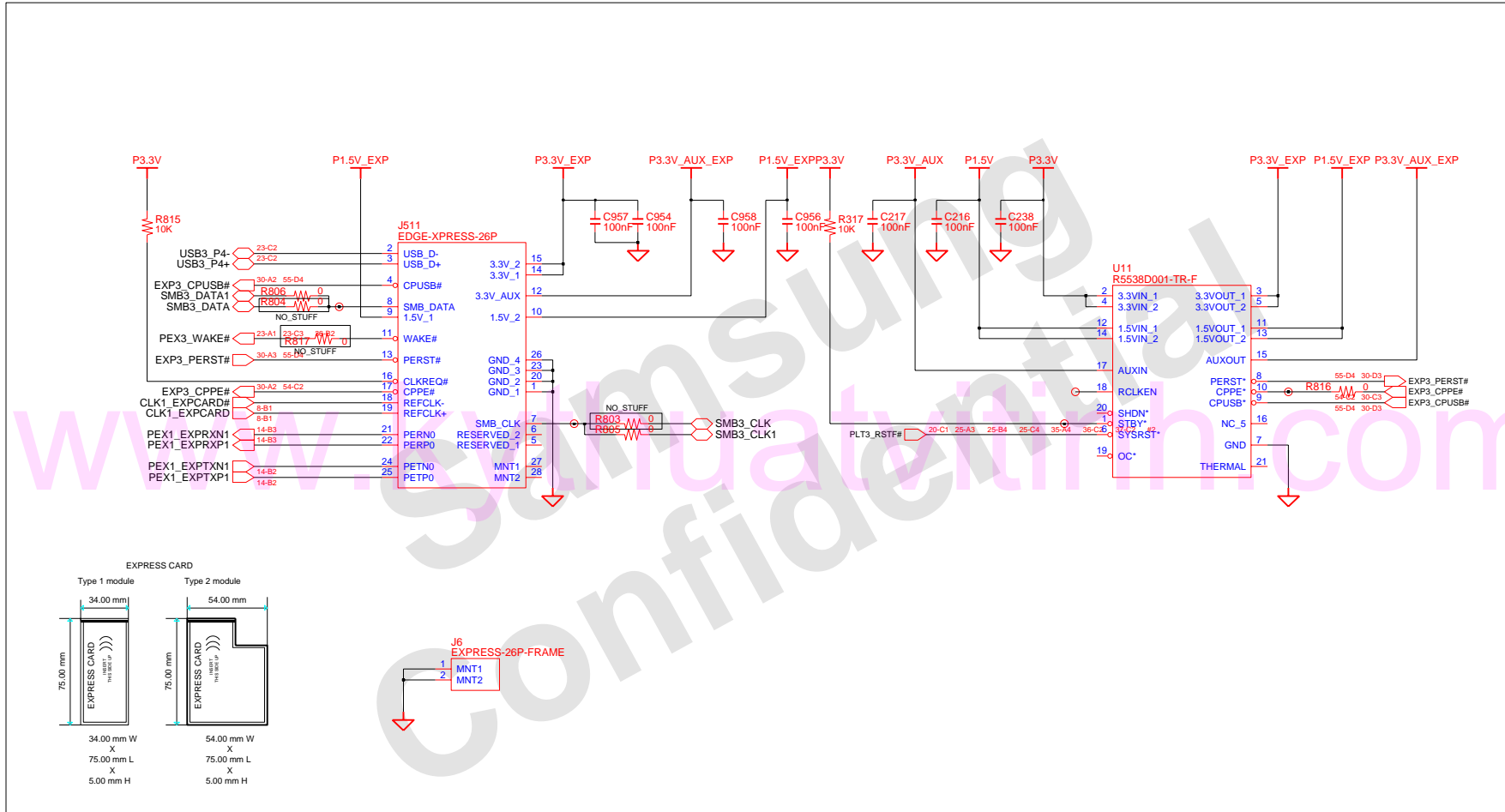


DRAW	ELLEN ZHANG	DATE	9/8/2007	TITLE	HAINAN3_EXT	SAMSUNG ELECTRONICS PART NO. BA41-00809/810A
CHECK	ROKY ZHENG	DEV. STEP	MP1.1	4 IN 1 CARD		
APPROVAL	KEVIN LEE	REV	1.0	September 8, 2007 12:02:16 PM		PAGE 32 OF 53
MODULE CODE	undef ined	LAST EDIT				

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EXPCARD

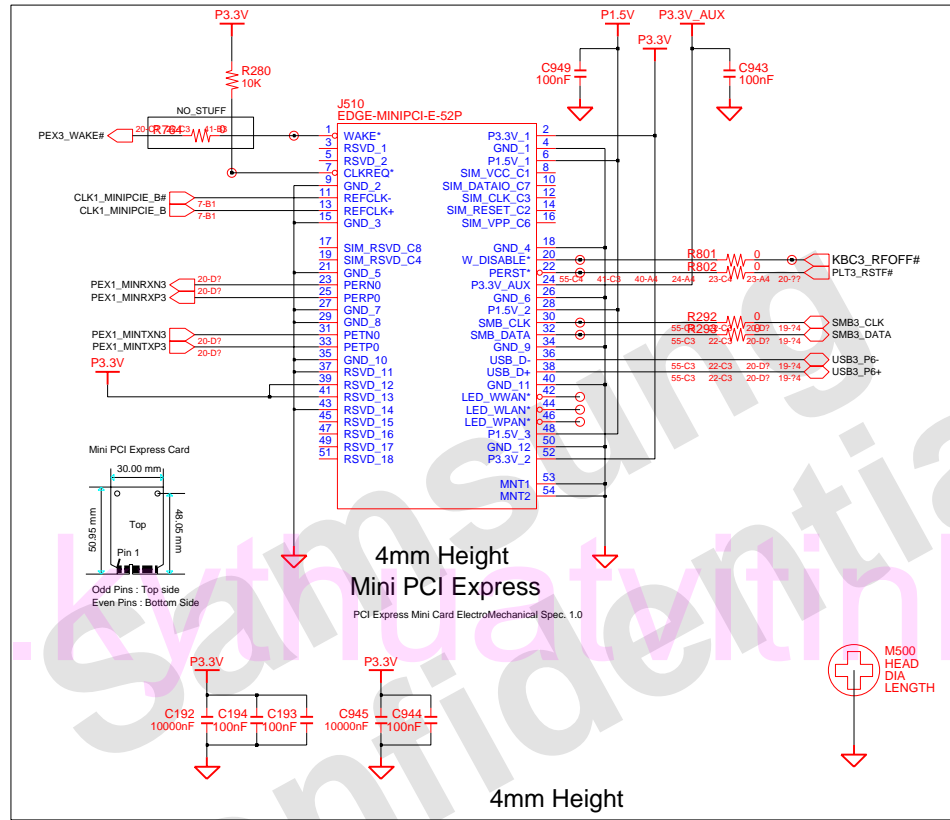


DRAW	ELLEN ZHANG	DATE	9/8/2007	TITLE	HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK	ROKY ZHENG	DEV. STEP	MP1.1			
APPROVAL	KEVIN LEE	REV	1.0		EXPRESS CARD	PART NO. BA41-00809/810A
MODULE CODE	undef ined	LAST EDIT	September 8, 2007 12:02:16 PM	PAGE	33	OF 53

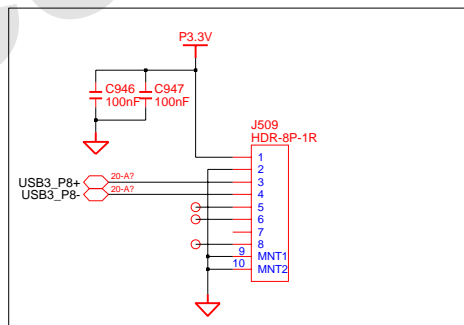
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MINI CARD



Bluetooth Interface



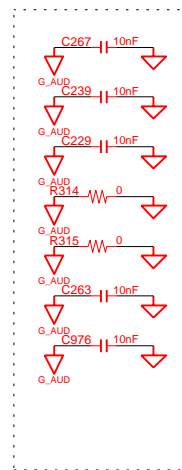
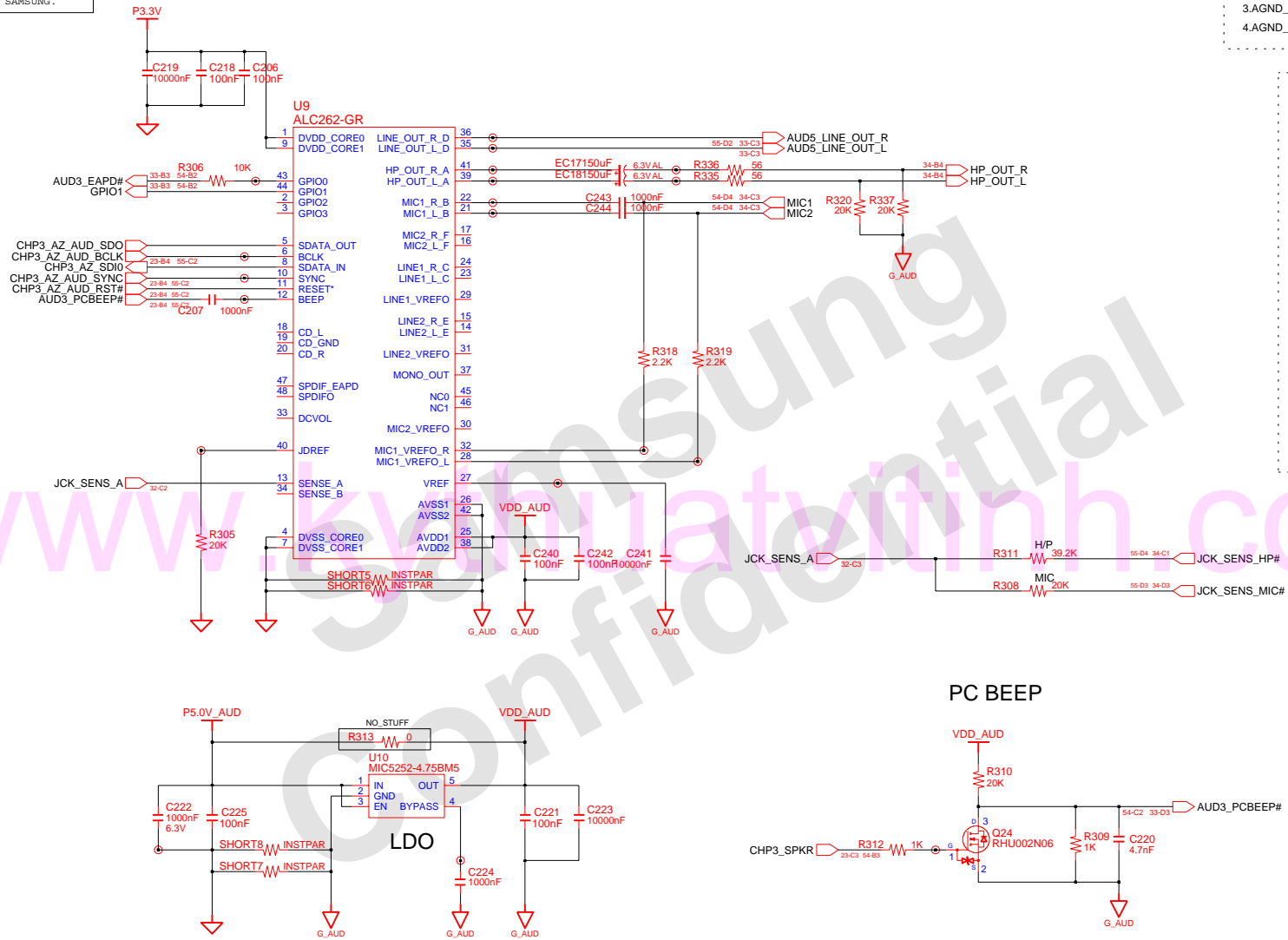
DRAW	ELLEN ZHANG	DATE	9/8/2007	TITLE	HAINAN3_EXT HAINAN2 MINI CARD	SAMSUNG ELECTRONICS
CHECK	ROKY ZHENG	DEV. STEP	MP1.1			
APPROVAL	KEVIN LEE	REV	1.0			PART NO. BA41-00809/810A
MODULE CODE	undef ined	LAST EDIT	September 8, 2007 12:02:16 PM	PAGE	34	OF 53

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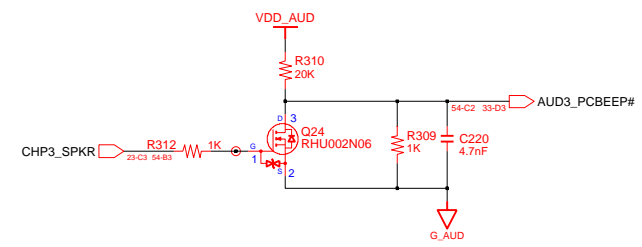
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- 1.AGND_AUD IS AUDIO GROUND
- 2. GND IS DIGITAL GROUND
- 3.AGND_MIC IS MIC GROUND
- 4.AGND_CHS IS CHASSIS GROUND

ALL TYPE IS 1608



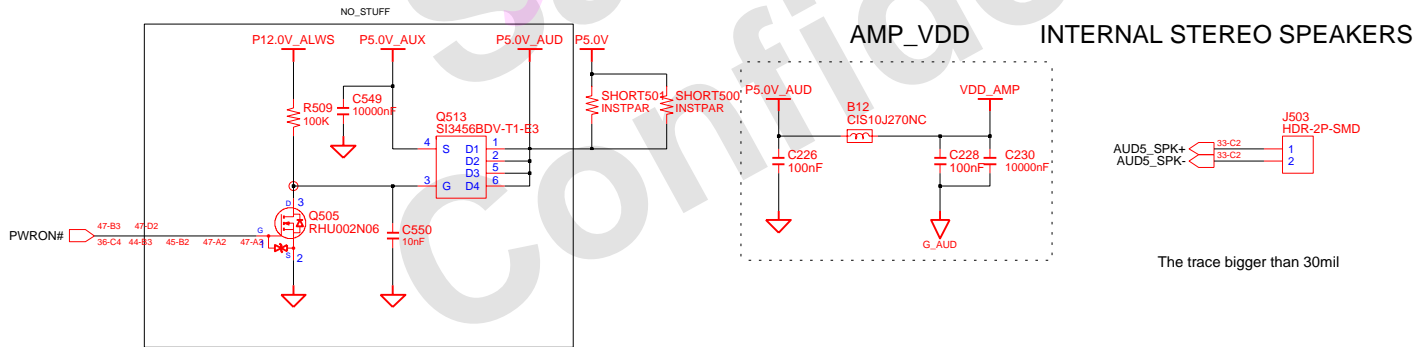
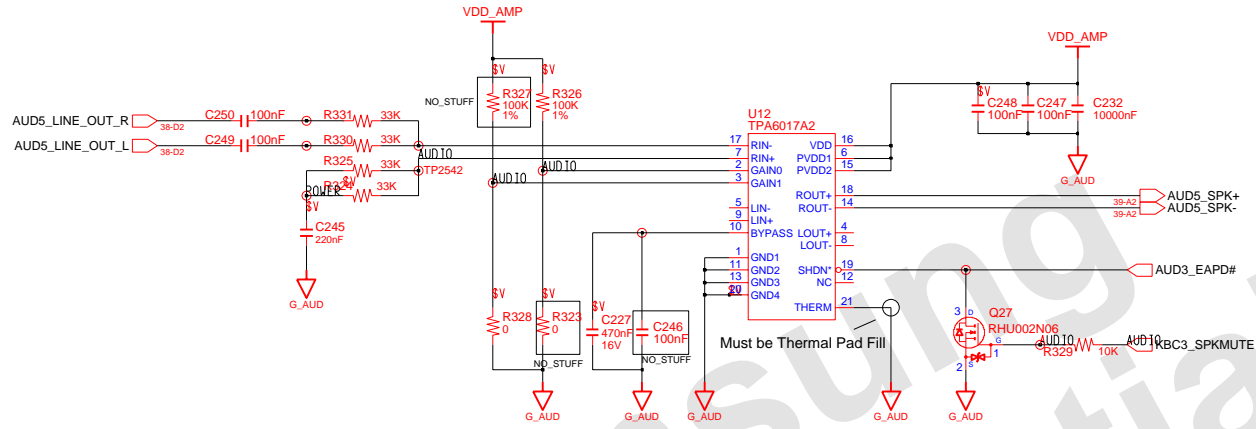
PC BEEP



DRAW	ELLEN ZHANG	DATE	9/8/2007	TITLE	HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK	ROKY ZHENG	DEV. STEP	MP1.1			
APPROVAL	KEVIN LEE	REV	1.0		AUDIO<1/3>	PART NO. BA41-00809/810A
MODULE CODE	undef ined	LAST EDIT	September 8, 2007 12:02:16 PM	PAGE	35	OF 53

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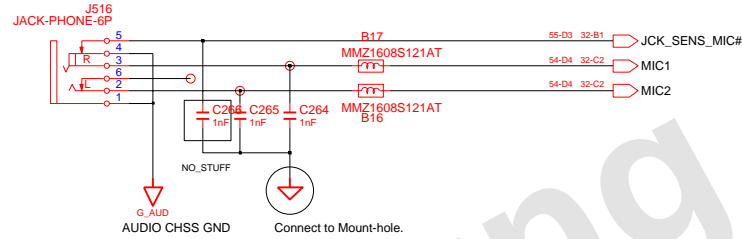
The trace bigger than 30mil

DRAW	ELLEN ZHANG	DATE	9/8/2007	TITLE	HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK	ROKY ZHENG	DEV. STEP	MP1.1			
APPROVAL	KEVIN LEE	REV	1.0		AUDIO<2/3>	PART NO. BA41-00809/810A
MODULE CODE	undefined	LAST EDIT	September 8, 2007 12:02:16 PM	PAGE	36	OF 53

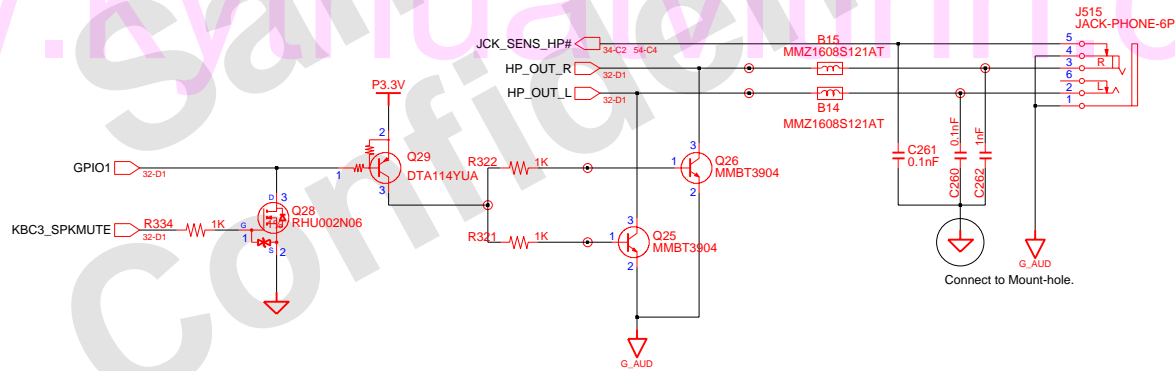
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MIC JACK



HEADPHONE



The traces led to Audio Jacks have the width over 10mil

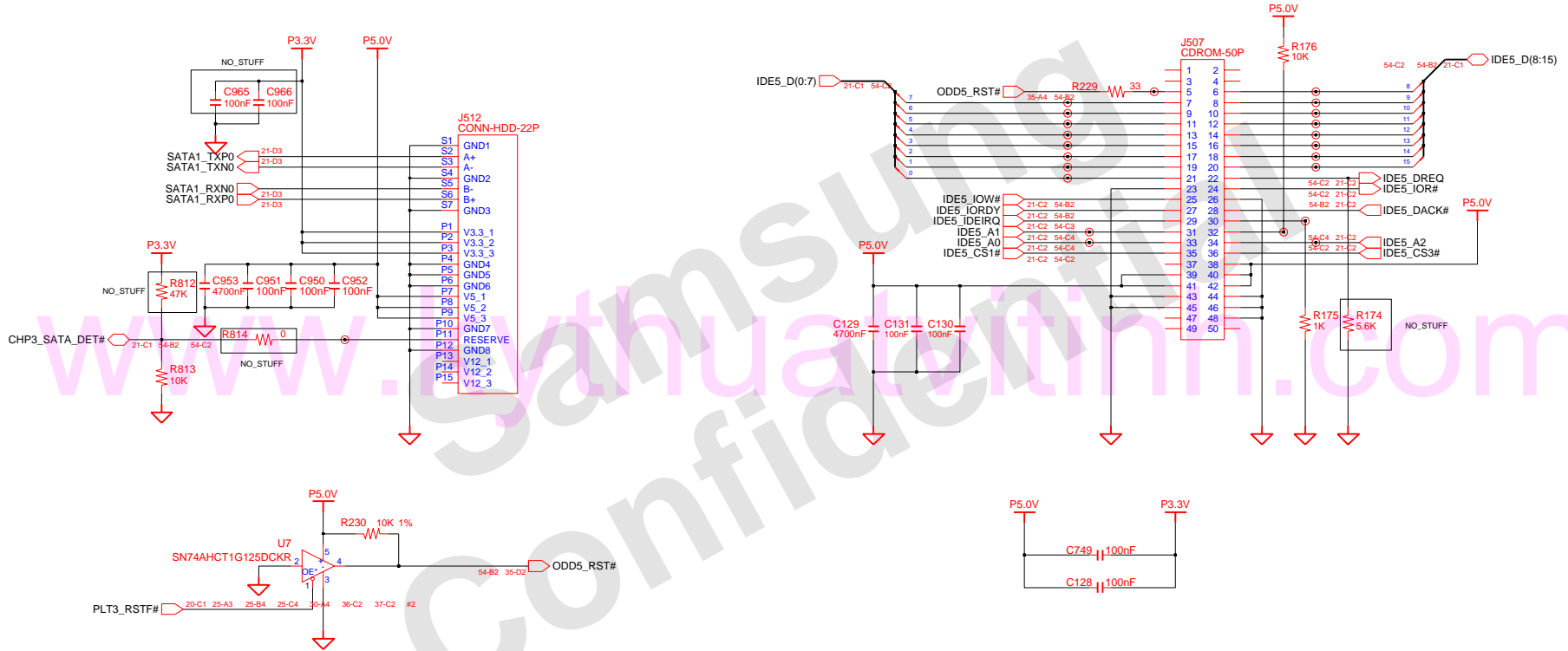
DRAW	ELLEN ZHANG	DATE	9/8/2007	TITLE	HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK	ROKY ZHENG	DEV. STEP	MP1.1			
APPROVAL	KEVIN LEE	REV	1.0		AUDIO<3/3>	PART NO. BA41-00809/810A
MODULE CODE	undef ined	LAST EDIT	September 8, 2007 12:02:16 PM	PAGE	37	OF 53

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Main to HDD

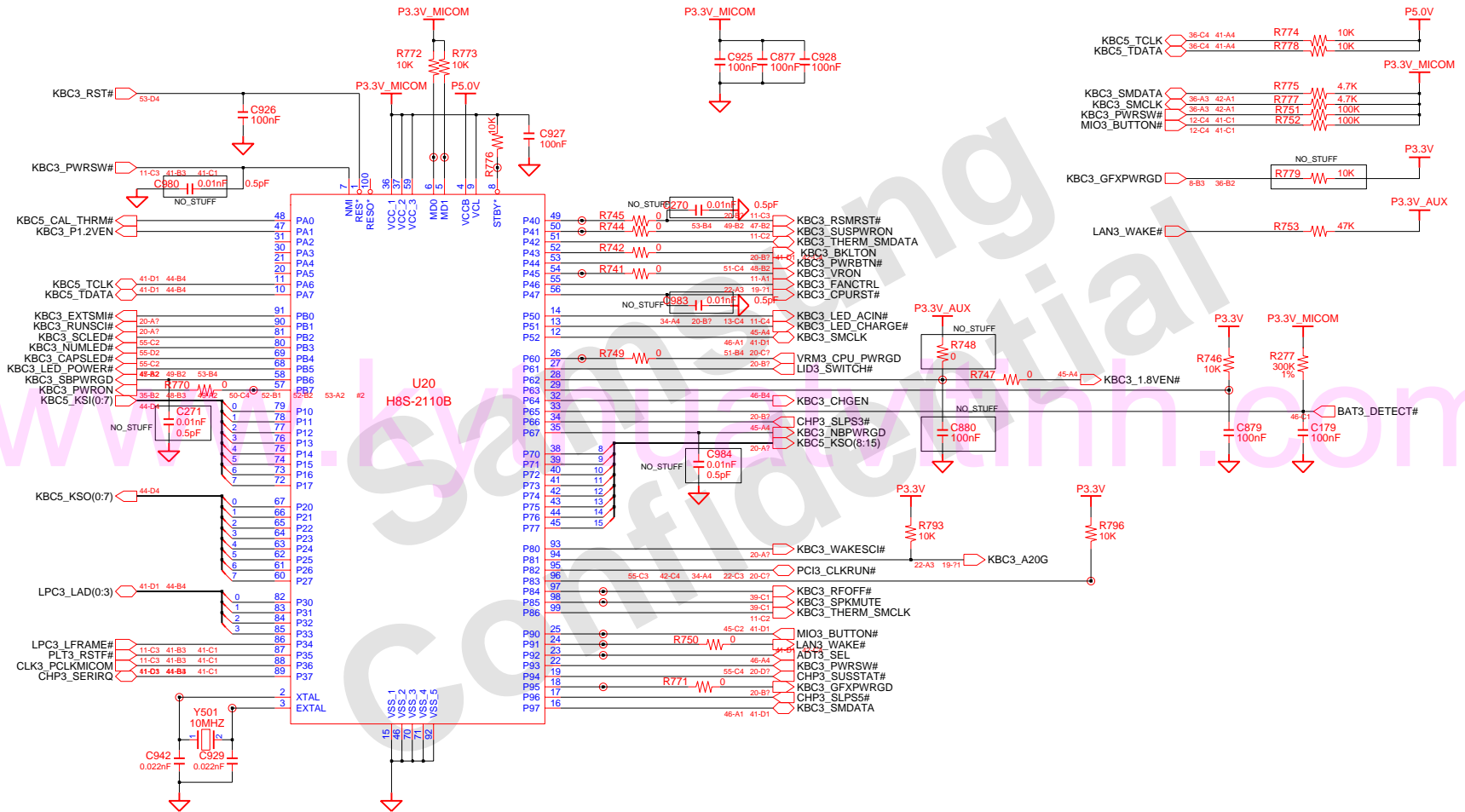
Main to ODD



DRAW	ELLEN ZHANG	DATE	9/8/2007	TITLE	HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK	ROKY ZHENG	DEV. STEP	MP1.1			
APPROVAL	KEVIN LEE	REV	1.0		HDD & ODD	PART NO. BA41-00809/810A
MODULE CODE	undef ined	LAST EDIT	September 8, 2007 12:02:16 PM	PAGE	38	OF 53

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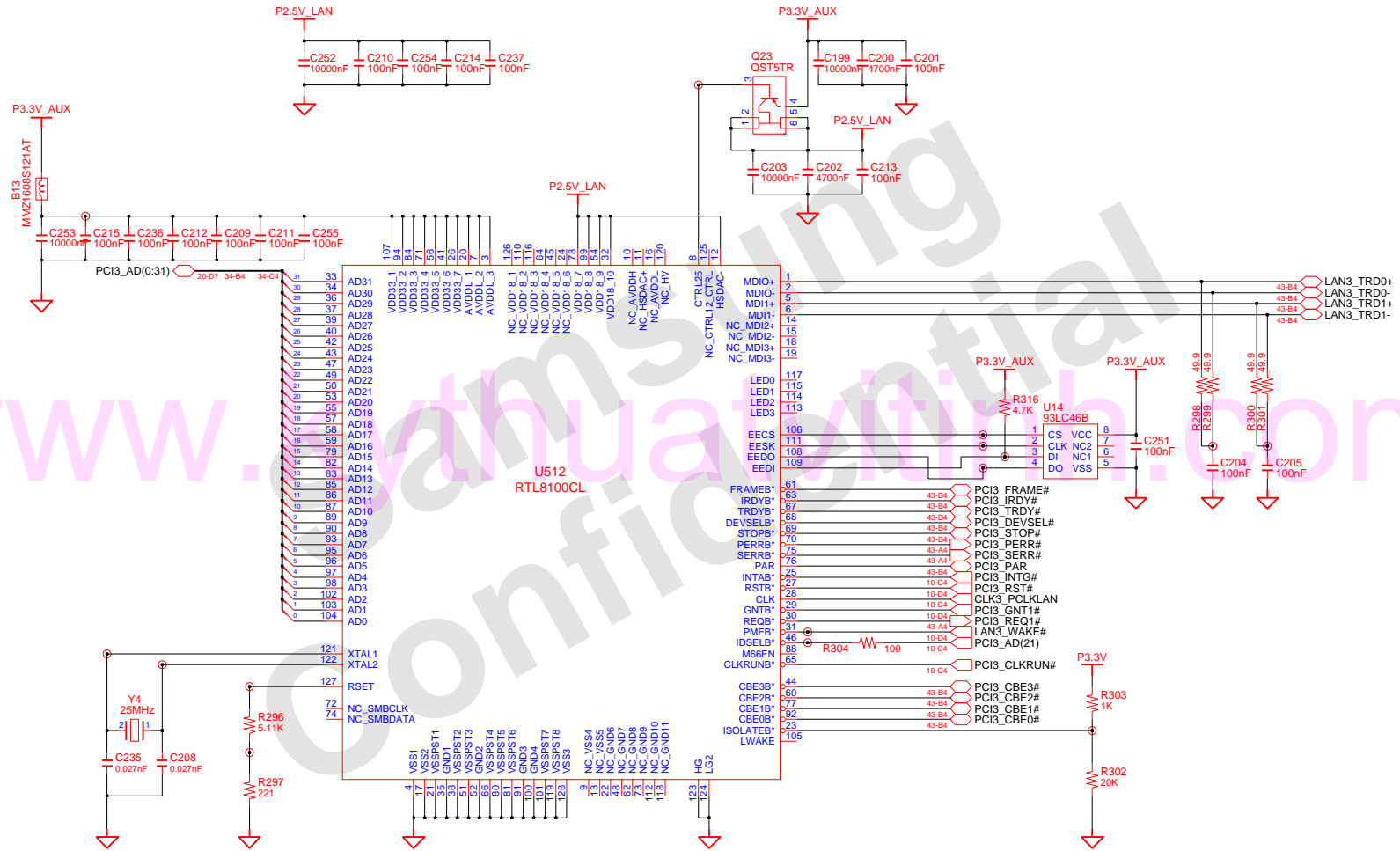
TP FOR UPDATE MICOM:
 P84=>TXD;P85=>RXD
 MD0 and MD1 =>GND
 P90,P91,P92=>VCC

DRAW	ELLEN ZHANG	DATE	9/8/2007	TITLE	HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK	ROKY ZHENG	DEV. STEP	MP1.1			
APPROVAL	KEVIN LEE	REV	1.0	MICOM		PART NO. BA41-00809/810A
MODULE CODE	undef ined	LAST EDIT	September 8, 2007 12:02:16 PM	PAGE	39	OF 53

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LAN Controller (Only 10/100M)

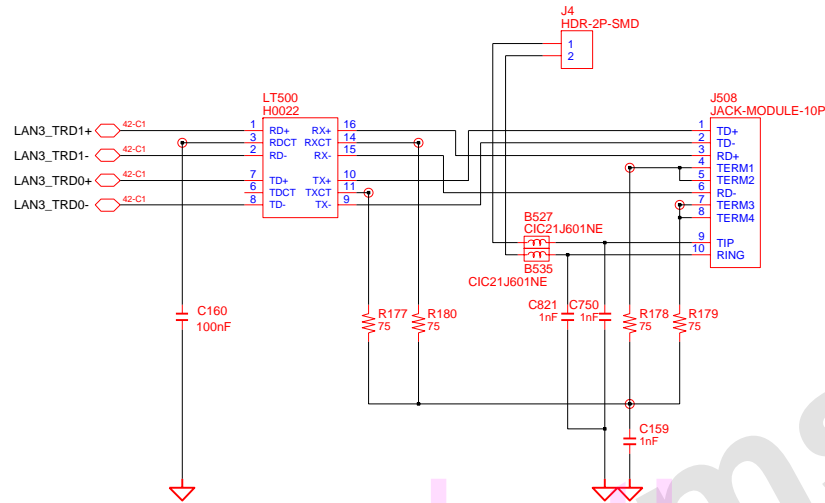


DRAW	ELLEN ZHANG	DATE	9/8/2007	TITLE	HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK	ROKY ZHENG	DEV. STEP	MP1.1			
APPROVAL	KEVIN LEE	REV	1.0		LAN	PART NO. BA41-00809/810A
MODULE CODE	undef ined	LAST EDIT	September 8, 2007 12:02:16 PM	PAGE	40	OF 53

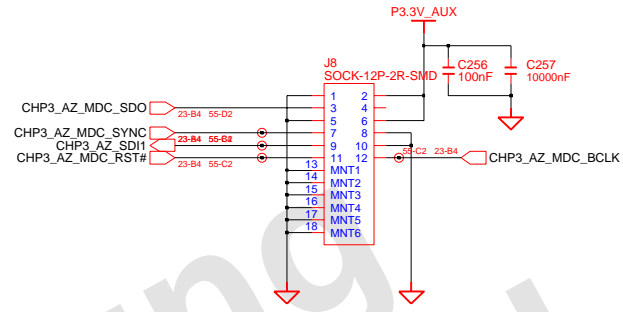
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LAN Connector

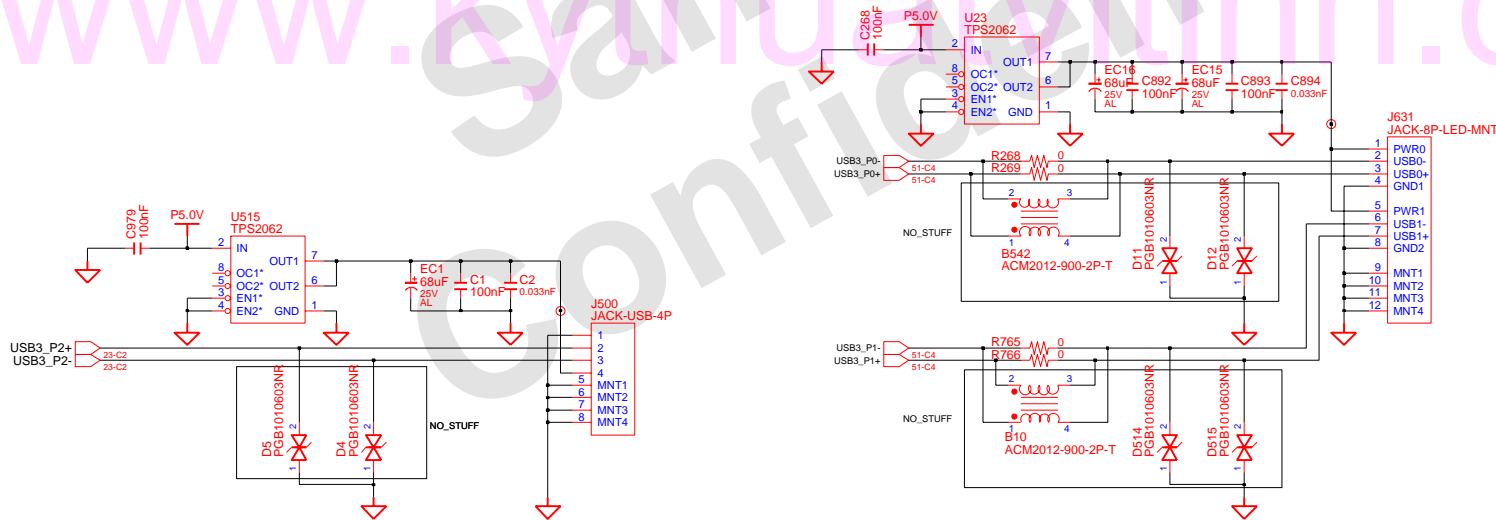


MDC Connector



USB Connector

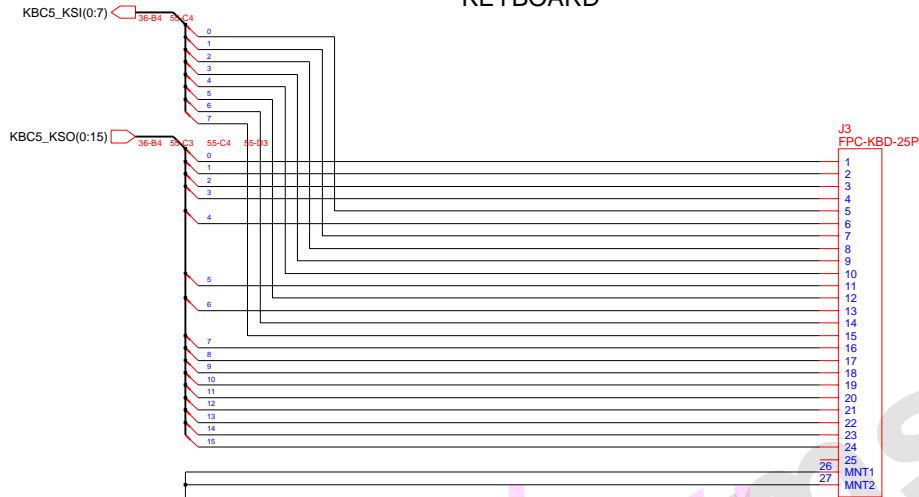
Need 4A Routing



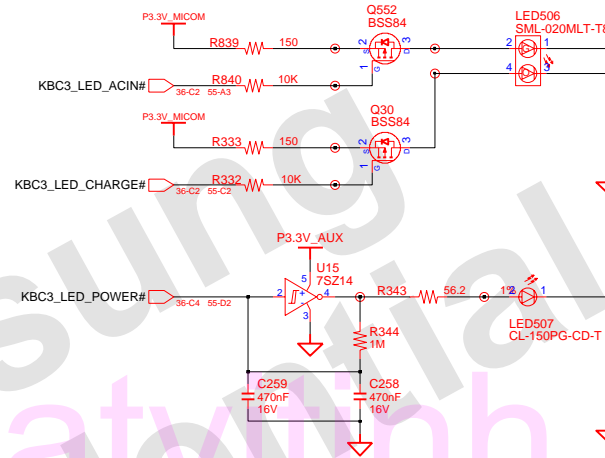
DRAW	ELLEN ZHANG	DATE	9/8/2007	TITLE	HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK	ROKY ZHENG	DEV. STEP	MP1.1			
APPROVAL	KEVIN LEE	REV	1.0	LAN & MDC & USB		PART NO. BA41-00809/810A
MODULE CODE	undef ined	LAST EDIT	September 8, 2007 12:02:16 PM	PAGE	41	OF 53

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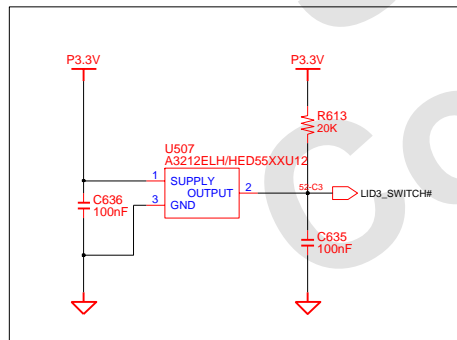
KEYBOARD



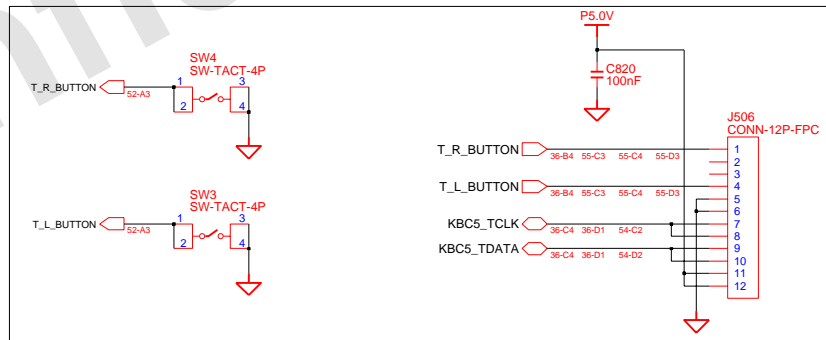
ADAPTERIN/CHARGING LED



LID SWITCH



TOUCHPAD

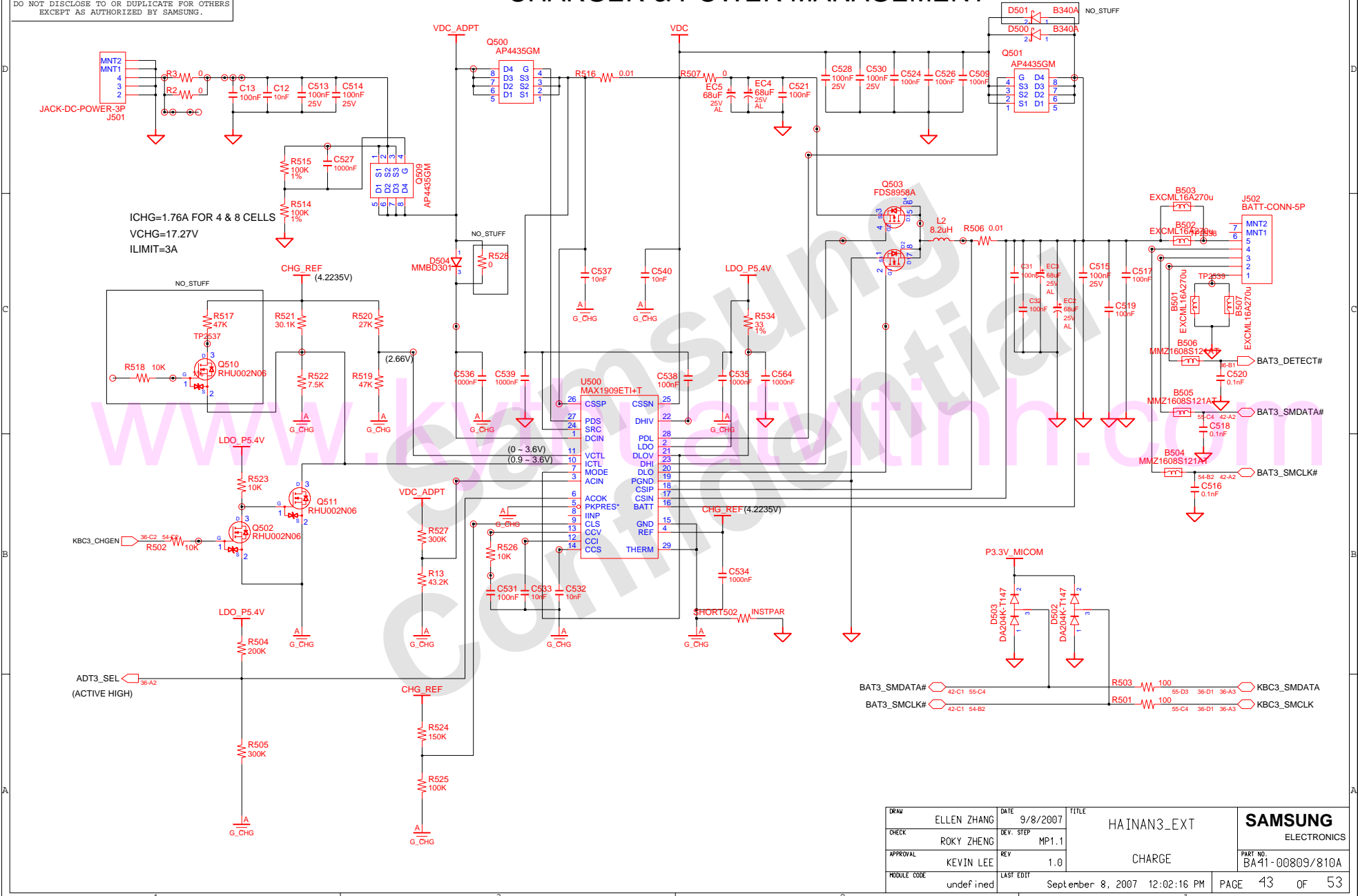


DRAW	ELLEN ZHANG	DATE	9/8/2007	TITLE	HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK	ROKY ZHENG	DEV. STEP	MP1.1	BOARD CONN		
APPROVAL	KEVIN LEE	REV	1.0			PART NO. BA41-00809/810A
MODULE CODE	undef ined	LAST EDIT	September 8, 2007 12:02:16 PM	PAGE	42	OF 53

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CHARGER & POWER MANAGEMENT



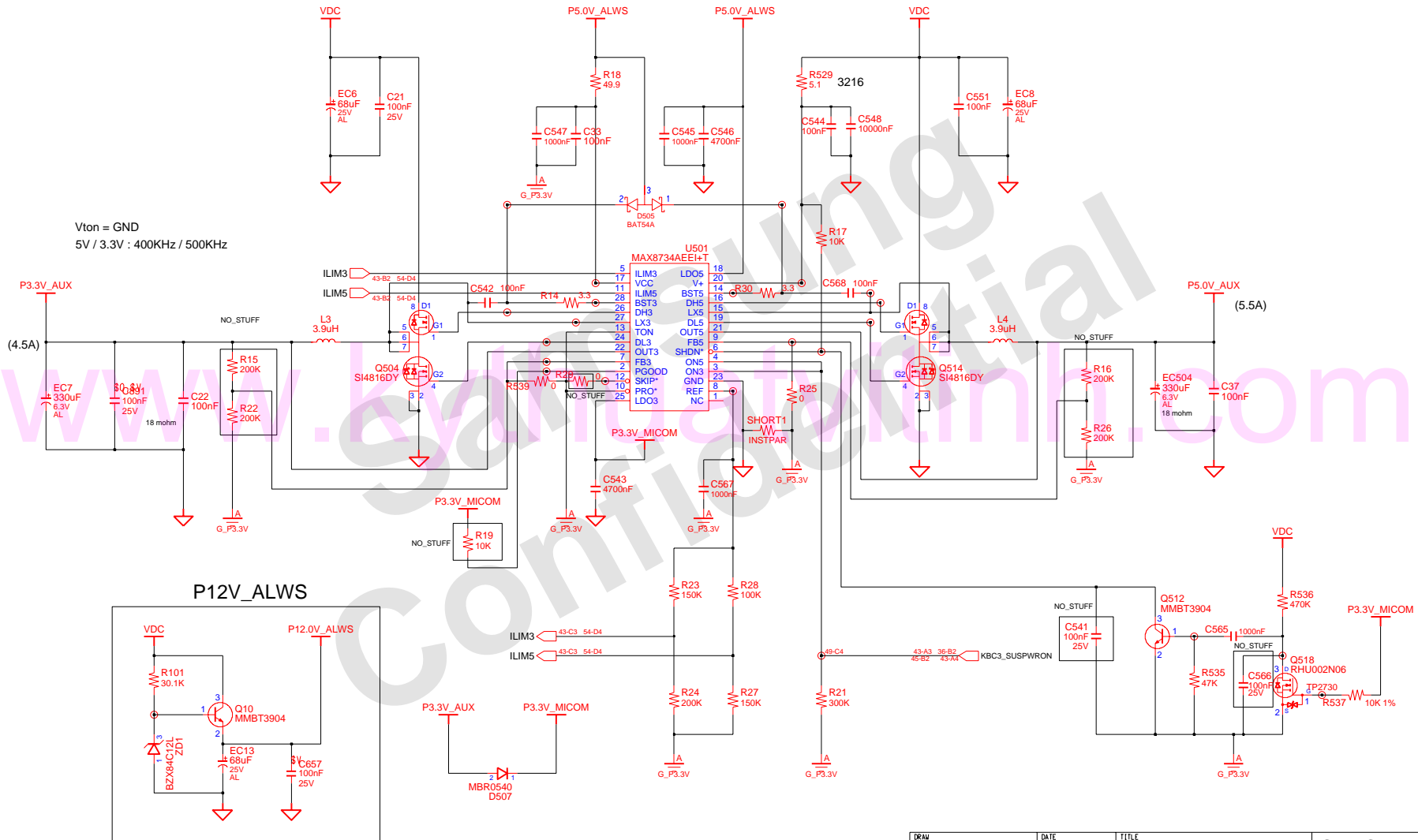
DRAW	ELLEN ZHANG	DATE	9/8/2007	TITLE	HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK	ROKY ZHENG	DEV. STEP	MP1.1			
APPROVAL	KEVIN LEE	REV	1.0		CHARGE	PART NO. BA41-00809/810A
MODULE CODE	undef ined	LAST EDIT	September 8, 2007 12:02:16 PM	PAGE	43	OF 53

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P3.3V_AUX & P5V_AUX

V_{ton} = GND
5V / 3.3V : 400KHz / 500KHz

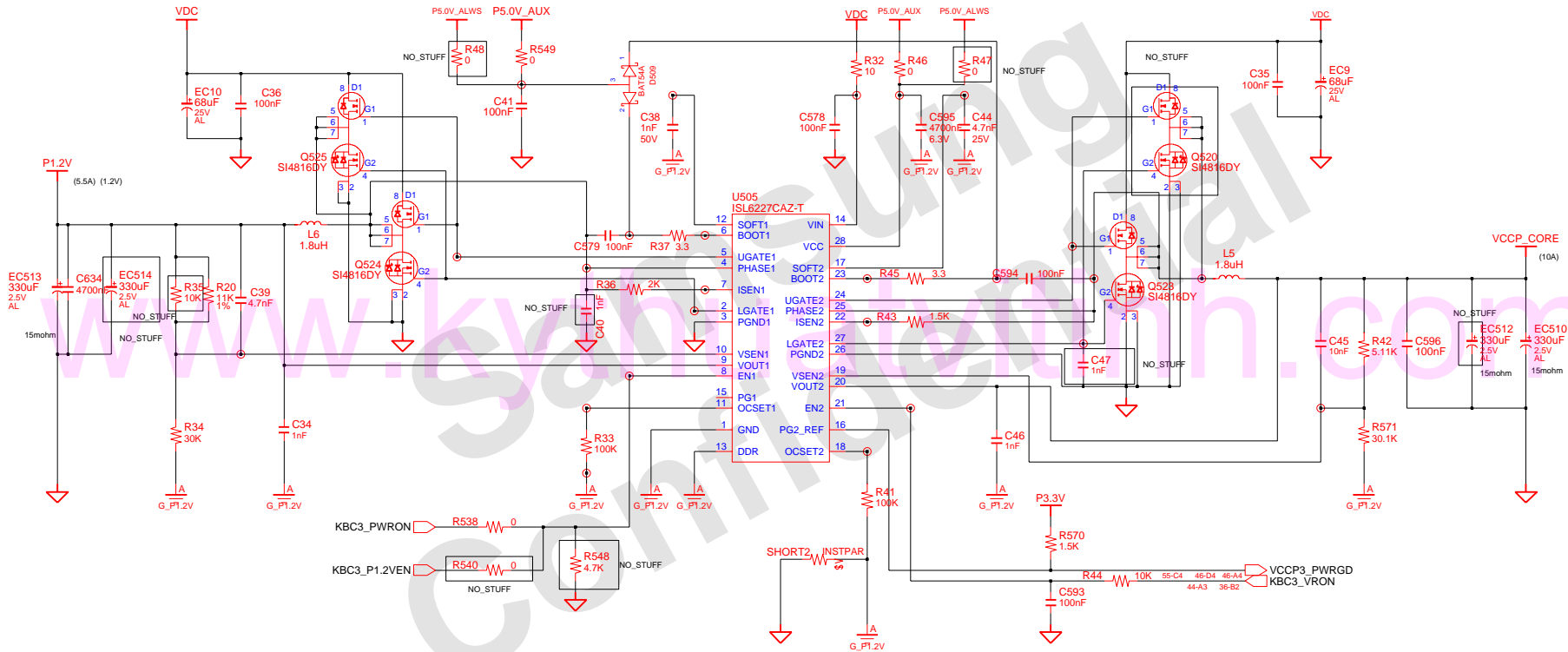


DRAW	ELLEN ZHANG	DATE	9/8/2007	TITLE	HAINAN3_EXT	SAMSUNG ELECTRONICS PART NO. BA41-00809/810A
CHECK	ROKY ZHENG	DEV. STEP	MP1.1			
APPROVAL	KEVIN LEE	REV	1.0		P3.3V_AUX & P5V_AUX	
MODULE CODE	undef ined	LAST EDIT	September 8, 2007 12:02:16 PM	PAGE	44	OF 53

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P1.2V & VCCP_CORE(1.05V)

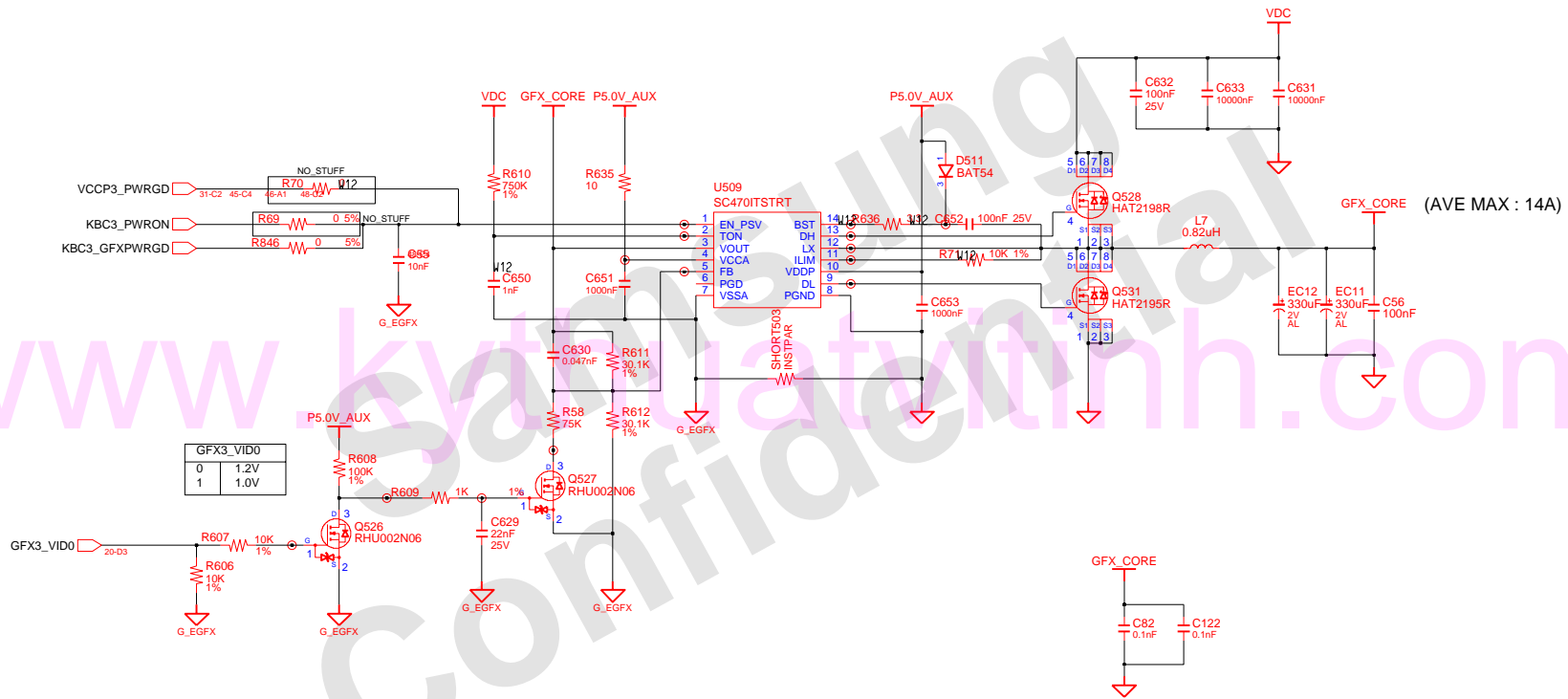


DRAW	ELLEN ZHANG	DATE	9/8/2007	TITLE	HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK	ROKY ZHENG	DEV. STEP	MP1.1			
APPROVAL	KEVIN LEE	REV	1.0		P1.2V & VCCP	PART NO. BA41-00809/810A
MODULE CODE	undef ined	LAST EDIT	September 8, 2007 12:02:16 PM	PAGE	45	OF 53

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Graphic Core Power

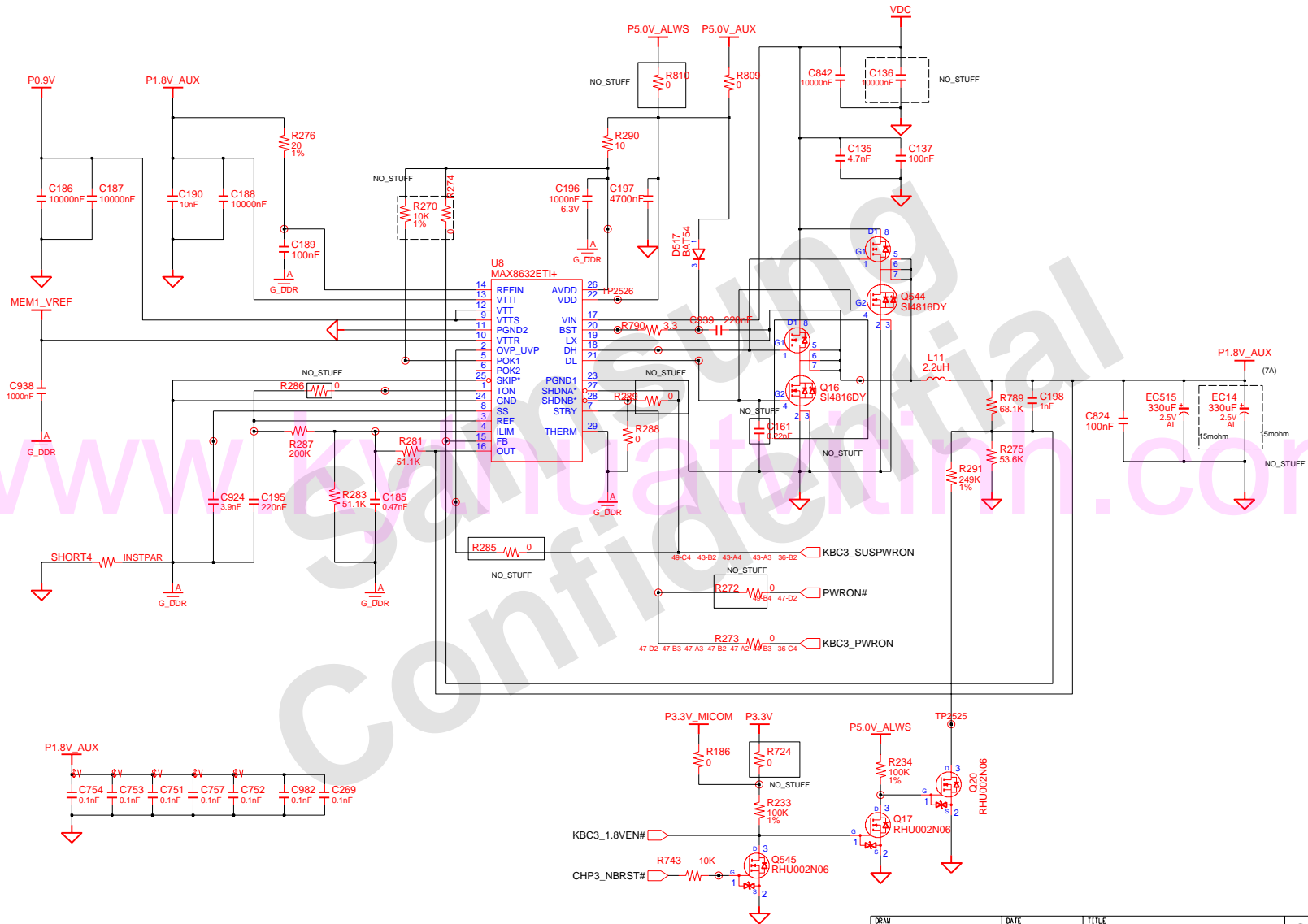


DRAW	ELLEN ZHANG	DATE	9/8/2007	TITLE	HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK	ROKY ZHENG	DEV. STEP	MP1.1		MAIN	
APPROVAL	KEVIN LEE	REV	1.0		GFX_CORE	PART NO. BA41-00809/810A
MODULE CODE		LAST EDIT	September 8, 2007 12:02:16 PM	PAGE	46	OF 53

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DDR2 Power

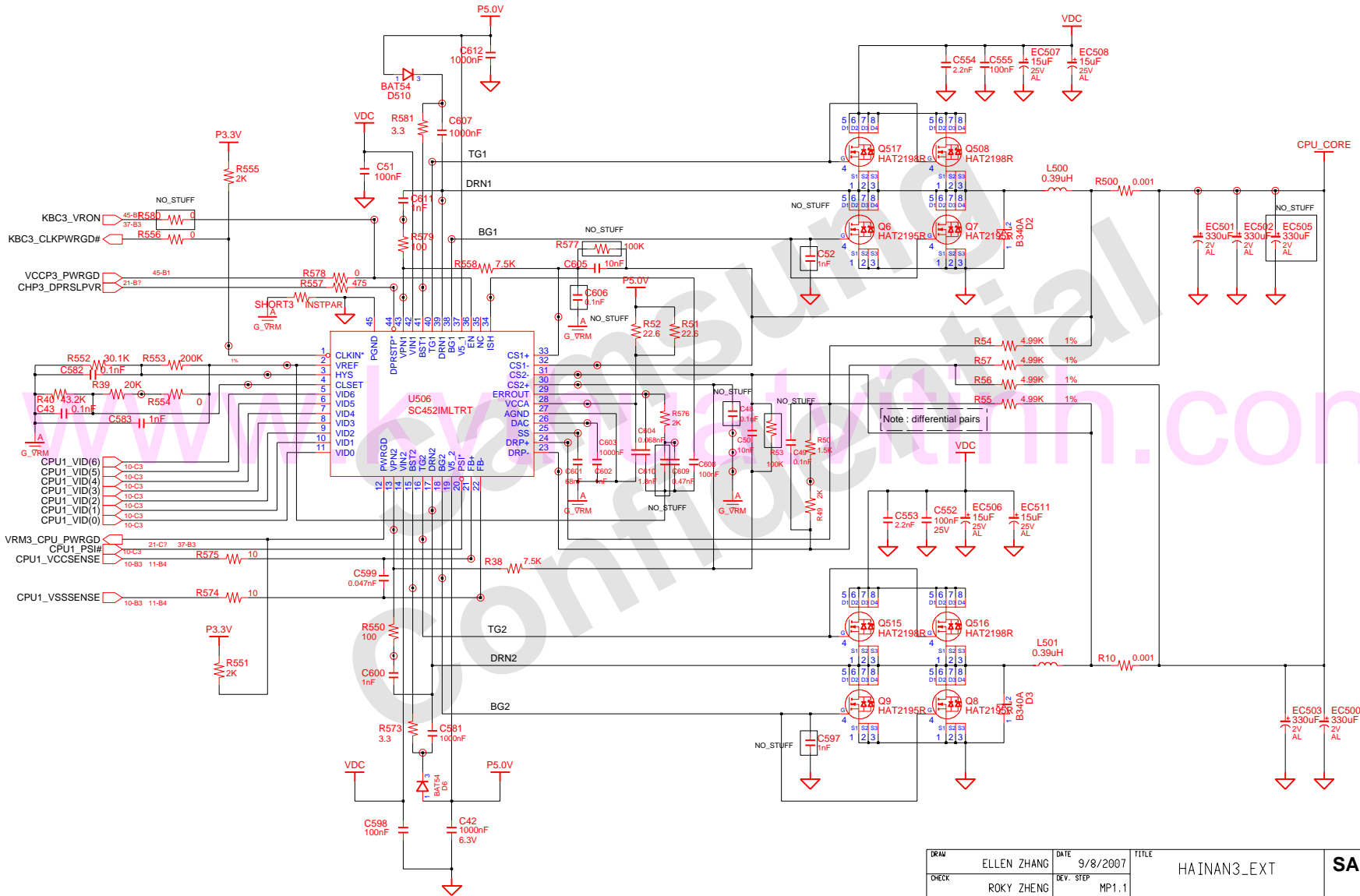


DRAW	ELLEN ZHANG	DATE	9/8/2007	TITLE	HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK	ROKY ZHENG	DEV. STEP	MP1.1			
APPROVAL	KEVIN LEE	REV	1.0		DDR2 POWER	PART NO. BA41-00809/810A
MODULE CODE	undef ined	LAST EDIT	September 8, 2007 12:02:16 PM	PAGE	47	OF 53

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CPU VRM [SEMTECH]

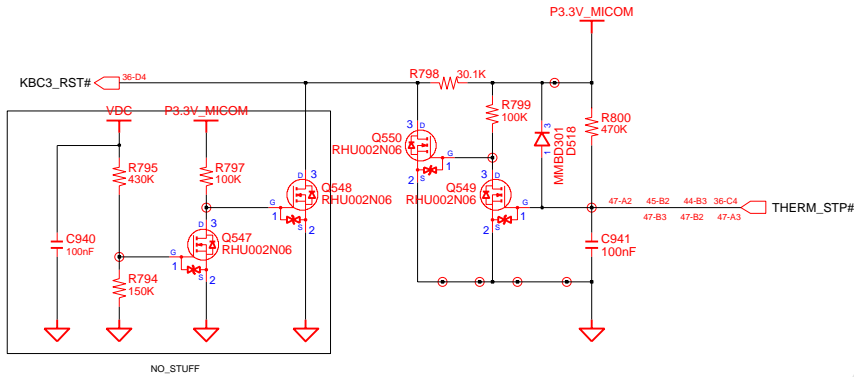


DRAM	ELLEN ZHANG	DATE	9/8/2007	TITLE	HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK	ROKY ZHENG	DEV. STEP	MP1.1			PART NO. BA41-00809/810A
APPROVAL	KEVIN LEE	REV	1.0		CPU VRM	
MODULE CODE	undefined	LAST EDIT	September 8, 2007 12:02:16 PM			PAGE 48 OF 53

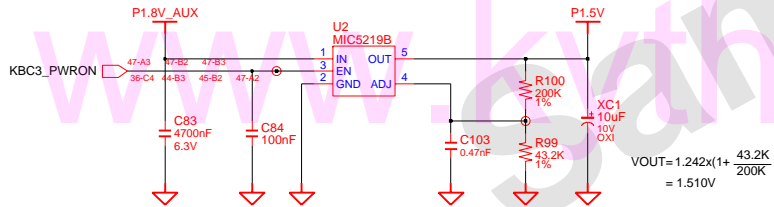
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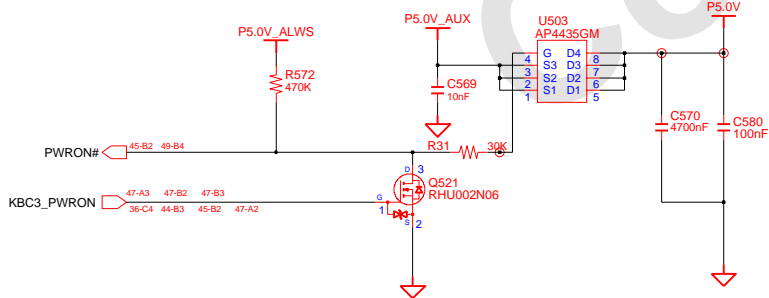
MICOM RESET



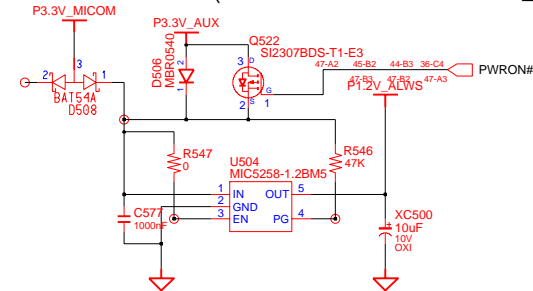
P1.5V POWER



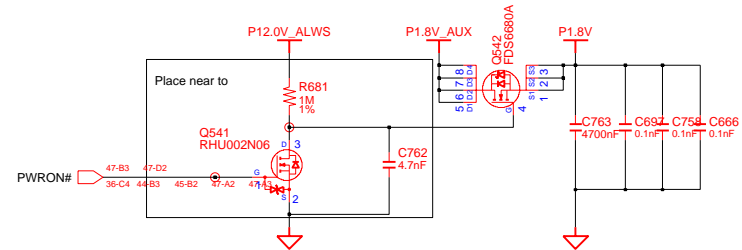
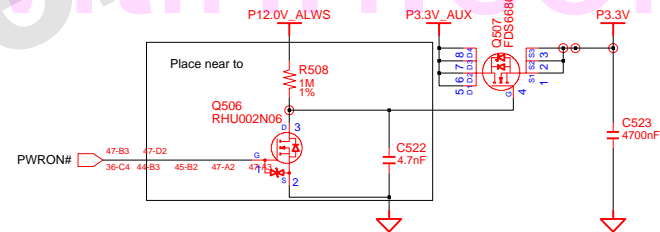
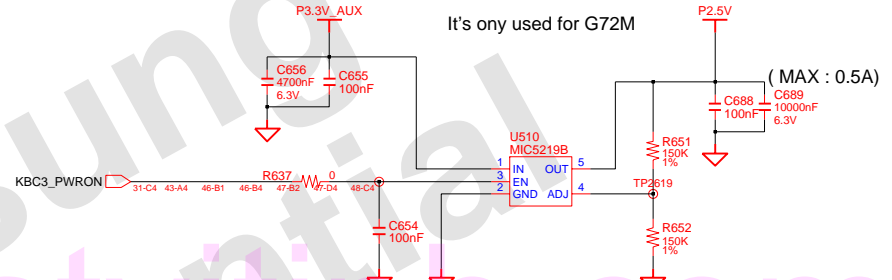
Switched Power On (P5V)



Switched Power On (P3.3V & P2.5V & 1.8V & 1.2V_ALWS)



It's only used for G72M

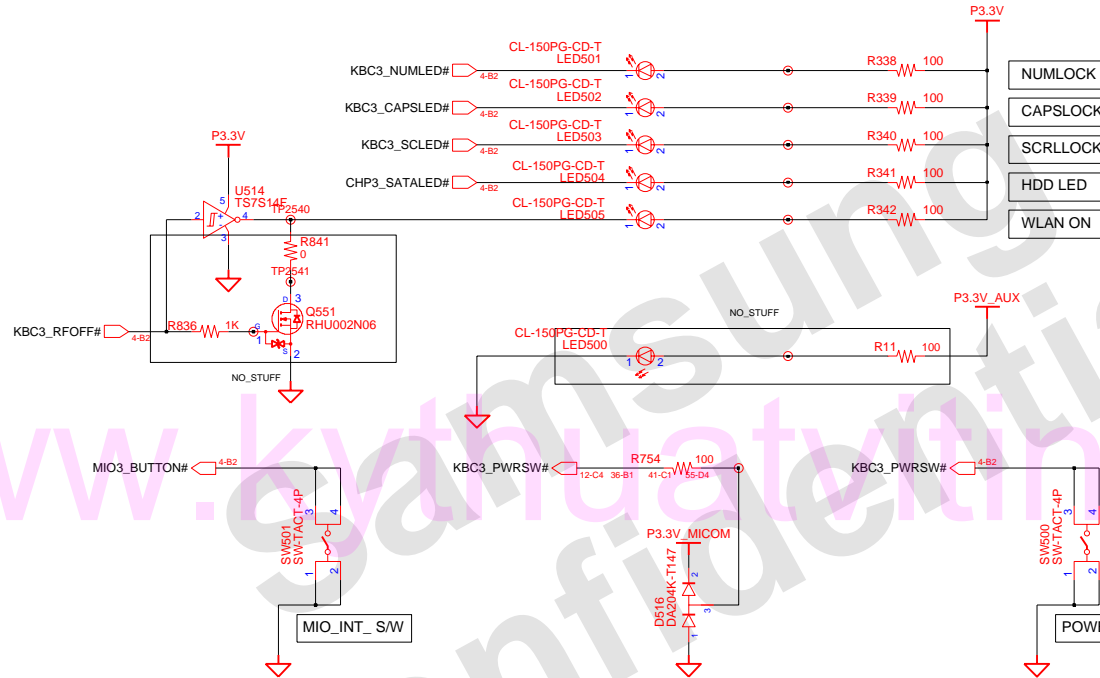


DRAW	ELLEN ZHANG	DATE	9/8/2007	TITLE	HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK	ROKY ZHENG	DEV. STEP	MP1.1			
APPROVAL	KEVIN LEE	REV	1.0		SWITCH POWER	PART NO. BA41-00809/810A
MODULE CODE	undef ined	LAST EDIT	September 8, 2007 12:02:16 PM			PAGE 49 OF 53

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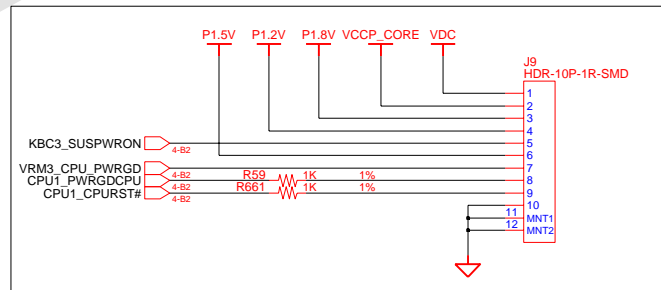
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**LED
0801-002195**



TP	Value	TP	Value
TP2543	C507 0.1nF	TP2544	C508 0.1nF
TP2544	C501 0.01nF 0.5pF	TP2546	C502 0.01nF 0.5pF
TP2545	C502 0.018nF	TP2547	C503 0.022nF
TP2546	C503 0.022nF	TP2548	C504 0.027nF
TP2547	C504 0.027nF	TP2549	C505 0.033nF
TP2548	C505 0.033nF	TP2550	C506 0.047nF
TP2549	C506 0.047nF	TP2551	C507 0.068nF
TP2550	C508 0.068nF	TP2552	C509 0.0033nF
TP2551	C509 0.0033nF	TP2553	C500 0.0033nF

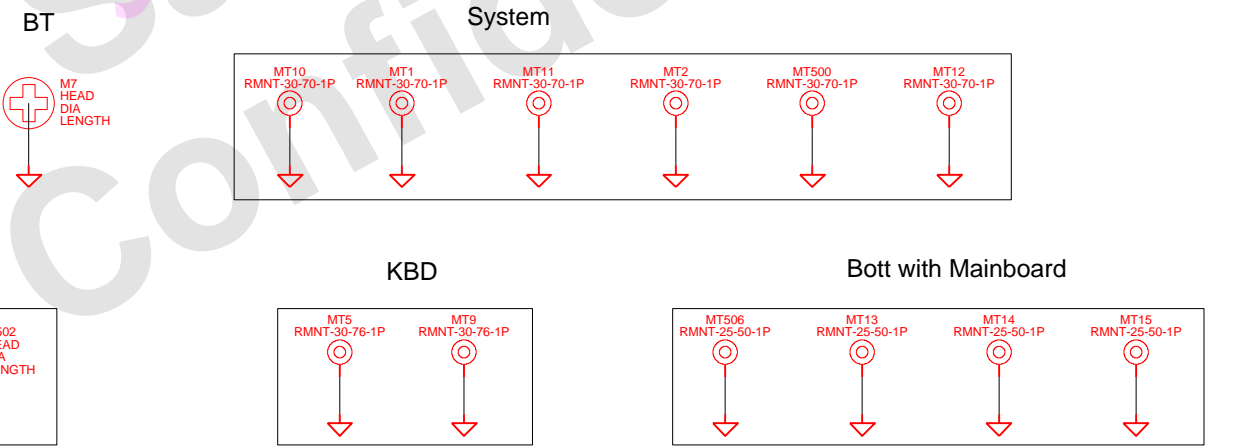
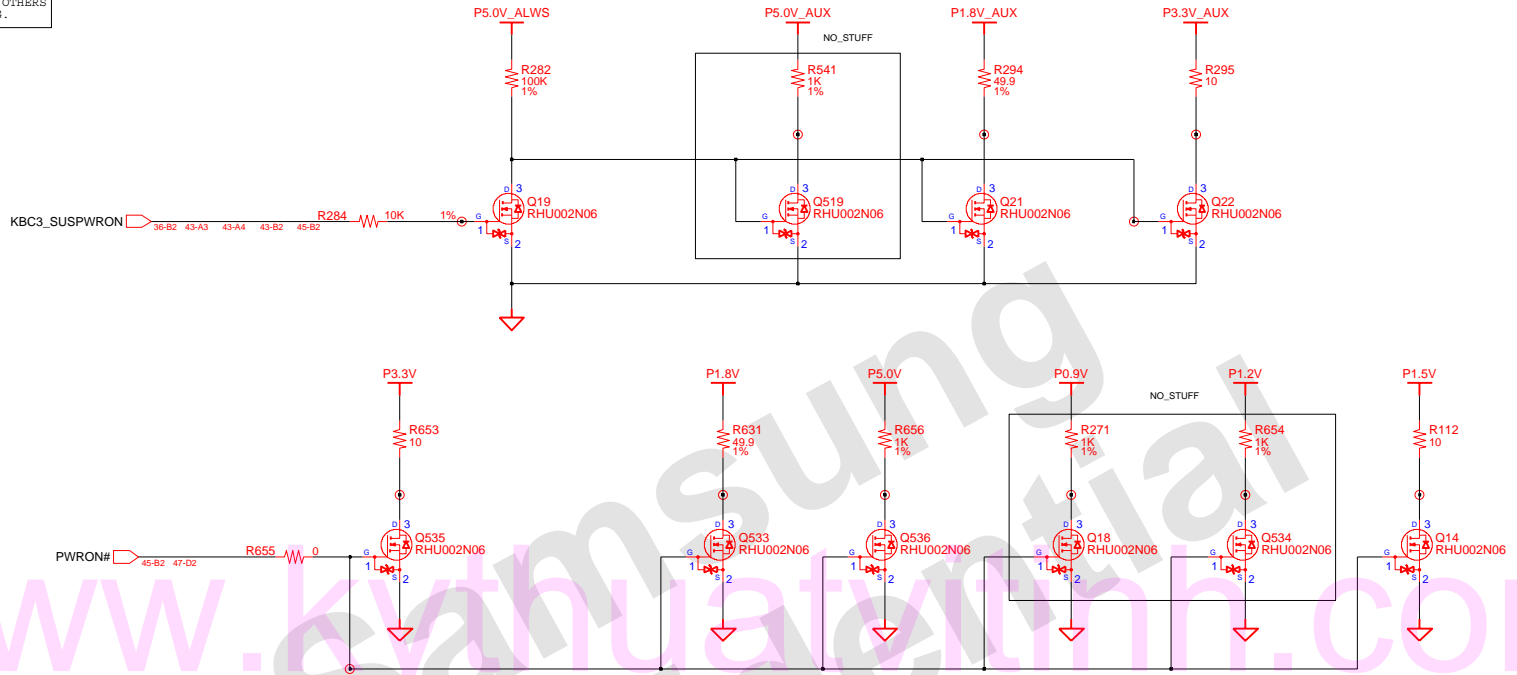
ICT



ICT/JIG

DRAW	ELLEN ZHANG	DATE	9/8/2007	TITLE	HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK	ROKY ZHENG	DEV. STEP	MP1.1			
APPROVAL	KEVIN LEE	REV	1.0		POWER SWITCH	
MODULE CODE	undef ined	LAST EDIT	September 8, 2007 12:02:16 PM	PAGE	50	OF 53

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DRAW	ELLEN ZHANG	DATE	9/8/2007	TITLE	HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK	ROKY ZHENG	DEV. STEP	MP1.1			
APPROVAL	KEVIN LEE	REV	1.0		POWER STRAPS	PART NO. BA41-00809/810A
MODULE CODE	undef ined	LAST EDIT	September 8, 2007 12:02:16 PM	PAGE	51	OF 53

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TP2027 OMC1
 TP2028 OMC2
 TP2029 GPI01
 TP2030 ILIM3
 TP2031 ILIM5

TP2637 OSMB3_DATA1

TP2638 OVG3_HS_SYNC
 TP2639 OVG3_VS_SYNC
 TP2640 CGFX_CORE
 TP2641 CGFX_CORE
 TP2642 CGFX_CORE
 TP2643 CGFX_CORE
 TP2644 CG_E_GFX
 TP2645 CG_E_GFX
 TP2646 CG_E_GFX
 TP2647 CG_E_GFX
 TP2648 OP2_5V
 TP2649 OP2_5V
 TP2650 OP2_5V
 TP2651 OP2_5V

TP2020 CPU1_TDI
 TP2021 CPU1_TMS
 TP2022 PCI3_PAR
 TP2023 SATA1_X1
 TP2024 SMB3_CLK
 TP2025 SPI3_CLK
 TP2026 SPI3_CS#

TP1968 CPU1_A20M#
 TP1971 CPU1_BSEL0
 TP1972 CPU1_BSEL1
 TP1973 CPU1_BSEL2

TP1939 PCI3_CBE0#
 TP1940 PCI3_CBE1#
 TP1941 PCI3_CBE2#
 TP1942 PCI3_CBE3#
 TP1943 PCI3_GNT1#

TP1945 PCI3_IRDY#
 TP1946 PCI3_PERR#
 TP1947 PCI3_REO1#
 TP1948 PCI3_RSTF#
 TP1949 PCI3_SERR#
 TP1950 PCI3_STOP#
 TP1951 PCI3_TRDY#

TP1888 KBC5_KSO(0)
 TP1889 KBC5_KSO(1)
 TP1890 KBC5_KSO(2)
 TP1891 KBC5_KSO(3)
 TP1892 KBC5_KSO(4)
 TP1893 KBC5_KSO(5)
 TP1894 KBC5_KSO(6)
 TP1895 KBC5_KSO(7)
 TP1896 KBC5_KSO(8)
 TP1897 KBC5_KSO(9)

TP1898 LCD3_BKLTON
 TP1899 LPC3_LAD(0)
 TP1900 LPC3_LAD(1)
 TP1869 LPC3_LAD(2)
 TP1870 LPC3_LAD(3)
 TP1871 MCD3_MSIN#

TP2002 CHP3_SPKR

TP1977 CPU1_FERR#

TP1979 CPU1_INTR#

TP1950 CPU1_TRST#
 TP1951 EXP3_CPPE#

TP2006 CPU1_INTR
 TP2007 CPU1_PSI#

TP2011 CPU1_SLP#
 TP2012 CPU1_SMI#
 TP2013 IDE5_CS1#
 TP2014 IDE5_CS3#

TP1918 PEX3_WAKE#
 TP1919 OPLT3_RSTF#

TP1952 IDE5_DACK#
 TP1953 IDE5_IORDY#
 TP1954 JCK_SENS_A
 TP1955 KBC3_CHGEN
 TP1956 KBC3_SMLCLK
 TP1957 KBC3_TDATA

TP1920 OT_L_BUTTON
 TP1921 OT_R_BUTTON

TP1924 OBT3_SMLCLK#
 TP1925 CHP3_OVERT#
 TP1910 CHP3_SBPME#
 TP1911 CHP3_SERIRQ
 TP1912 CHP3_SLPS#
 TP1913 CHP3_SLPS5#

TP2621 MEM1_BRAS#
 TP2622 MEM1_BWE#

TP1980 IDE5_DREQ
 TP1981 IDE5_IOR#
 TP1982 IDE5_IOW#
 TP1983 KBC3_A20#
 TP1984 KBC3_RST#
 TP1985 KBC3_VRON
 TP1986 KBC5_TCLK

TP1959 MCD3_SDCD#
 TP1960 MCD3_XDALE
 TP1961 MCD3_XDCD#
 TP1962 MCD3_XDCE#
 TP1963 MCD3_XDRE#
 TP1964 MCD3_XDWE#

TP1902 CPU1_DPSLP#
 TP1903 CPU1_IGNNE#
 TP1904 CPU1_VID(0)
 TP1905 CPU1_VID(1)
 TP1906 CPU1_VID(2)
 TP1907 CPU1_VID(3)
 TP1908 CPU1_VID(4)
 TP1909 CPU1_VID(5)
 TP1872 CPU1_VID(6)
 TP1873 EXP3_PLUS#
 TP1874 EXP3_PERST#
 TP1875 IDE5_IDEIRQ
 TP1876 KBC3_18VEN#
 TP1877 KBC3_PWR5W#
 TP1878 KBC3_SCLE#
 TP1879 KBC3_SMDATA
 TP1880 KBC5_KSI(0)
 TP1881 KBC5_KSI(1)
 TP1882 KBC5_KSI(2)
 TP1883 KBC5_KSI(3)
 TP1884 KBC5_KSI(4)
 TP1885 KBC5_KSI(5)
 TP1886 KBC5_KSI(6)
 TP1887 KBC5_KSI(7)

TP2633 LCD3_BKLT_CTRL
 TP2634 LCD3_BKLTEN
 TP2635 LCD3_EDIO_CLK
 TP2636 LCD3_VDDEN

TP2623 CGFX3_BKLTEN
 TP2624 CGFX3_THRINTRIP#
 TP2625 CGFX3_VID0

TP1996 ODD5_RST#

TP2629 GPI0(13)
 TP2630 GPI0(5)
 TP2631 KBC3_BKLTON
 TP2632 KBC3_P1_2VEN

TP1997 SMB3_DATA
 TP1998 SPI3_MISO
 TP1999 SPI3_MOSI
 TP2000 AUD3_EAPD#

TP2015 RTC_CLK
 TP2016 AC_SDOUT
 TP2017 AUTO_ON#
 TP2018 CPU1_NMI
 TP2019 CPU1_TCK

TP2001 CLK3_NB14M

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DRAW	ELLEN ZHANG	DATE	9/8/2007	TITLE	HAINAN3_EXT	SAMSUNG ELECTRONICS
CHECK	ROKY ZHENG	DEV. STEP	MP1.1			
APPROVAL	KEVIN LEE	REV	1.0		TP	PART NO. BA41-00809/810A
MODULE CODE		LAST EDIT	September 8, 2007 12:02:16 PM	PAGE	52	OF 53

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TP2195 ○ CHP3_DPRSPLVR
TP2196 ○ CHP3_SATALED#

TP2197 ○ CPU1_PROCHOT#
TP2198 ○ CPU1_PWRGDCPU
TP2199 ○ CPU1_VCCSENSE
TP2200 ○ CPU1_VSSSENSE
TP2201 ○ JCK_SENS_MCHP
TP2202 ○ KBC3_CAPSLED#
TP2203 ○ KBC3_WAKESCIF#

TP2126 ○ G_CRT
TP2127 ○ G_CRT
TP2128 ○ G_DDR
TP2129 ○ G_DDR
TP2130 ○ G_DDR
TP2131 ○ G_DDR
TP2132 ○ G_P3.3V
TP2133 ○ G_P3.3V
TP2134 ○ G_P3.3V
TP2135 ○ G_P3.3V
TP2136 ○ LCD_VDD3V
TP2137 ○ LCD_VDD3V

TP2078 ○ P5.0V_AUX
TP2079 ○ P5.0V_AUX
TP2080 ○ PCIE_VDDR

TP2085 ○ P1.2V_ALWS
TP2086 ○ P1.2V_ALWS

TP2088 ○ P5.0V_ALWS
TP2089 ○ P5.0V_ALWS
TP2090 ○ P5.0V_ALWS
TP2091 ○ P5.0V_ALWS
TP2092 ○ P12.0V_ALWS
TP2093 ○ P12.0V_ALWS
TP2094 ○ P12.0V_ALWS
TP2095 ○ P12.0V_ALWS
TP2096 ○ P12.0V_ALWS
TP2097 ○ P12.0V_ALWS
TP2098 ○ P12.0V_ALWS
TP2099 ○ P12.0V_ALWS

TP2233 ○ PCI3_FRAME#

TP2235 ○ VCCP3_PWRGD
TP2236 ○ AUD3_PCBEEP#
TP2237 ○ BAT3_DETECT#
TP2238 ○ BAT3_SMDATA#
TP2239 ○ CHP3_AZ_SDI0
TP2240 ○ CHP3_BIOSWP#
TP2241 ○ CHP3_CPUSTP#

TP2142 ○ LDO_P5.4V
TP2143 ○ LDO_P5.4V

TP2146 ○ MEM1_VREF
TP2147 ○ MEM1_VREF

TP2148 ○ P0.9V
TP2149 ○ P0.9V
TP2150 ○ P0.9V
TP2151 ○ P0.9V
TP2152 ○ P1.2V
TP2153 ○ P1.2V
TP2154 ○ P1.2V

TP2035 ○ P3.3V_AUX_EXP
TP2037 ○ P3.3V_AUX_EXP
TP2038 ○ VDC
TP2039 ○ VDC
TP2040 ○ VDC
TP2041 ○ VDC

TP2045 ○ VCC_CRT
TP2046 ○ VDC_INV
TP2047 ○ VDC_INV

TP2180 ○ CHP3_SATA_DET#

TP2181 ○ CPU1_THRMTRIP#
TP2182 ○ KBC3_CLKPWRGD#
TP2183 ○ KBC3_LED_ACIN#
TP2184 ○ KBC3_CAL_THRM#

TP2186 ○ VRM3_CPU_PWRGD

TP2187 ○ CHP3_ALINK_RST#
TP2188 ○ CHP3_AZ_AUD_SDI0
TP2189 ○ CHP3_AZ_MDC_SDI0

TP2103 ○ PRTC_BAT

TP2192 ○ KBC3_LED_POWER#

TP2158 ○ CHP3_AZ_AUD_RST#

TP2159 ○ CHP3_SBTHRMTRIP#

TP2162 ○ KBC3_LED_CHARGE#
TP2163 ○ KBC3_THERM_SMCLK

TP2164 ○ KBC3_THERM_SMDATA

TP2109 ○ P1.5V_EXP
TP2110 ○ P1.5V_EXP
TP2111 ○ P1.5V_EXP
TP2112 ○ P1.8V_AUX
TP2113 ○ P1.8V_AUX
TP2114 ○ P1.8V_AUX
TP2115 ○ P1.8V_AUX
TP2116 ○ P2.5V_LAN
TP2117 ○ P2.5V_LAN
TP2118 ○ P2.5V_LAN
TP2119 ○ P2.5V_LAN

TP2656 ○ GPI0(1)

TP2660 ○ KBC3_BKLTON
TP2661 ○ KBC3_P1.2VEN

TP2123 ○ P2.5V_MCD
TP2124 ○ P3.3V_AUX
TP2125 ○ P3.3V_AUX
TP2062 ○ P3.3V_AUX
TP2063 ○ P3.3V_AUX

TP2065 ○ P3.3V_EXP
TP2066 ○ P3.3V_EXP

TP2169 ○ CHG_REF
TP2170 ○ G_AUD
TP2171 ○ G_AUD
TP2172 ○ G_AUD
TP2173 ○ G_AUD
TP2174 ○ G_CHG
TP2175 ○ G_CHG
TP2176 ○ G_CHG
TP2177 ○ G_CHG
TP2178 ○ G_CRT
TP2179 ○ G_CRT

TP2068 ○ P3.3V_MCD
TP2069 ○ P3.3V_MCD
TP2070 ○ P3.3V_MCD
TP2071 ○ P3.3V_MCD
TP2072 ○ P5.0V_AUD
TP2073 ○ P5.0V_AUD
TP2074 ○ P5.0V_AUD
TP2075 ○ P5.0V_AUD
TP2076 ○ P5.0V_AUX
TP2077 ○ P5.0V_AUX

TP2663 ○ GFX_CORE
TP2664 ○ GFX_CORE
TP2665 ○ GFX_CORE
TP2666 ○ GFX_CORE
TP2667 ○ G_EGFX
TP2668 ○ G_EGFX
TP2669 ○ G_EGFX
TP2670 ○ G_EGFX
TP2671 ○ P2.5V
TP2672 ○ P2.5V
TP2673 ○ P2.5V
TP2674 ○ P2.5V

TP2193 ○ PCI3_CLKRUN#
TP2194 ○ PCI3_DEVSEL#

TP2223 ○ CPU1_STPCLK#

TP2225 ○ ITP3_SYSRST#
TP2226 ○ JCK_SENS_HP#
TP2227 ○ KBC3_CPURST#
TP2228 ○ KBC3_EXTSMI#
TP2229 ○ KBC3_FANCTRL
TP2230 ○ KBC3_NBPWRGD
TP2231 ○ KBC3_NUMLED#
TP2232 ○ KBC3_PWRBTN#
TP2207 ○ KBC3_RSMRST#
TP2208 ○ KBC3_RUNSCIF#
TP2209 ○ KBC3_SBPWRGD
TP2210 ○ KBC5_KSO(10)
TP2211 ○ KBC5_KSO(11)
TP2212 ○ KBC5_KSO(12)
TP2213 ○ KBC5_KSO(13)
TP2214 ○ KBC5_KSO(14)
TP2215 ○ KBC5_KSO(15)

TP2216 ○ LID3_SWITCH#
TP2217 ○ LPC3_LFRAME#



PCB REVISION CONTROL (ICT)					
NO	CONNECTION	DATE(Y/M/D)	REVISION	STEP	
1	N.C.				
2	1-2				
3	2-3				
4	3-1				
5	1-2-3				
6	N.C.				
7	1-2				
8	2-3				
9	3-1				
10	1-2-3				

REV500
1 ○
2 ○ ○3

DRAW	ELLEN ZHANG	DATE	9/8/2007	TITLE	HAINAN3_EXT	SAMSUNG ELECTRONICS PART NO. BA41-00809/810A
CHECK	ROKY ZHENG	DEV. STEP	MP1.1		TP	
APPROVAL	KEVIN LEE	REV	1.0			
MODULE CODE		LAST EDIT	September 8, 2007 12:02:16 PM	PAGE	53	OF 53