

CICHLID

CPU : BANIAS/DOTHAN
 Chip Set : MCH-M ODEM+
 Remarks : TEMP

Model Name : CICHLID MAIN
 PBA Name : BA92-02649A
 PCB Code : BA41-00392A
 Dev. Step : MP
 Revision : 1.0

DRAW	CHECK	APPROVAL

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DRAW	RYAN, PARK	DATE	3/30/2004	TITLE	CICHLID	SAMSUNG ELECTRONICS
CHECK	H.S, OH	DEV. STEP	MP	COVER	PART NO.	
APPROVAL	H.S, KIM	REV	1.0	March, 30, 2004 10:12:30 AM	PAGE	1 OF 41
MODULE CODE		LAST EDIT				

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
Cardbus	AD19	0	A,B,C
LAN	AD21	3	D
MiniPCI SLOT1	AD23	2	E,F
USB	AD29(internal)	-	USB2.0 #0 : A USB2.0 #1 : D USB2.0 #2 : C
Hub to PCI	AD30(internal)	-	-
LPC bridge/IDE/AC97/SMBUS	AD31(internal)	-	B
AGP	AD17(internal)	-	A,B
Internal MAC	AD24(internal)	-	E
AC Link	-	-	B
PCI SLOT	AD20	-	A,B,C,D

Voltage Rails

VDC	Primary DC system power supply (7 to 21V)
VCC_CORE	Core voltage for BANIAS CPU (1.356 - 0.844V)
VCCP	BANIAS/ODEM Processor System Bus(PSB) Termination (1.05V)
VCC_MCH	MCH-M Core Voltage (1.2V)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.5V_AUX	1.5V power rail (off in S4-S5)
P1.8V	1.8V switched power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail(off in S4-S5)
P2.5V	2.5V switched power rail (off in S3-S5)
P2.5V_AUX	2.5V power rail (off in S4-S5)
P1.25V_AUX	1.25V power rail (off in S4-S5)
MICOM_P3V	3.3V always on power rail for MICOM
P3.3V	3.3V switched power rail (off in S3-S5)
P3.3V_AUX	3.3V power rail (off in S4-S5)
P3.3V_ALWAYS	3.3V always on Power Rail
P5V	5.0V switched power rail (off in S3-S5)
P5V_ALWAYS	5.0V always on power
P12V	12.0V switched power rail (off in S3-S5)

CPU Core Voltage Table

VID5	VID4	VID3	VID2	VID1	VID0	Voltage	VID5	VID4	VID3	VID2	VID1	VID0	Voltage
0	0	0	0	0	0	1.708 V	1	0	0	0	0	0	1.196 V
0	0	0	0	0	1	1.692 V	1	0	0	0	0	1	1.180 V
0	0	0	0	1	0	1.676 V	1	0	0	0	1	0	1.164 V
0	0	0	0	1	1	1.660 V	1	0	0	0	1	1	1.148 V
0	0	0	1	0	0	1.644 V	1	0	0	1	0	0	1.132 V
0	0	0	1	0	1	1.628 V	1	0	0	1	0	1	1.116 V
0	0	0	1	1	0	1.612 V	1	0	0	1	1	0	1.100 V
0	0	1	0	0	0	1.596 V	1	0	1	0	0	0	1.084 V
0	0	1	0	0	1	1.580 V	1	0	1	0	0	1	1.068 V
0	0	1	0	1	0	1.564 V	1	0	1	0	1	0	1.052 V
0	0	1	0	1	1	1.548 V	1	0	1	0	1	1	1.036 V
0	0	1	1	0	0	1.532 V	1	0	1	0	1	1	1.020 V
0	0	1	1	0	1	1.516 V	1	0	1	1	0	0	1.004 V
0	0	1	1	1	0	1.500 V	1	0	1	1	0	1	0.988 V
0	0	1	1	1	1	1.484 V	1	0	1	1	1	0	0.972 V
0	0	1	1	1	1	1.468 V	1	0	1	1	1	1	0.956 V
0	1	0	0	0	0	1.452 V	1	1	0	0	0	0	0.940 V
0	1	0	0	0	1	1.436 V	1	1	0	0	0	1	0.924 V
0	1	0	0	1	0	1.420 V	1	1	0	0	1	0	0.908 V
0	1	0	0	1	1	1.404 V	1	1	0	0	1	1	0.892 V
0	1	0	1	0	0	1.388 V	1	1	0	1	0	0	0.876 V
0	1	0	1	0	1	1.372 V	1	1	0	1	0	1	0.860 V
0	1	0	1	1	0	1.356 V	1	1	0	1	1	0	0.844 V
0	1	0	1	1	1	1.340 V	1	1	0	1	1	1	0.828 V
0	1	0	1	1	1	1.324 V	1	1	0	1	1	1	0.812 V
0	1	0	1	1	1	1.308 V	1	1	0	1	1	1	0.796 V
0	1	0	1	1	1	1.292 V	1	1	0	1	1	1	0.780 V
0	1	0	1	1	1	1.276 V	1	1	0	1	1	1	0.764 V
0	1	0	1	1	1	1.260 V	1	1	0	1	1	1	0.748 V
0	1	0	1	1	1	1.244 V	1	1	0	1	1	1	0.732 V
0	1	0	1	1	1	1.228 V	1	1	0	1	1	1	0.716 V
0	1	0	1	1	1	1.212 V	1	1	0	1	1	1	0.700 V

Highest Freq. L - - - - - Lowest Freq.

- - - - - Deeper Sleep

I C / SMB Address

Devices	Address	Hex	Bus
ICH4	-	-	-
ADM1032(CPU Thermal Sensor)	1001 110X	9Ch	SMBUS Master
SODIMM0	1010 0000	A0h	Thermal Sensor
SODIMM1	1010 001X	A2h	-
CK-408 (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable

USB PORT Assign

PORT NUMBER	ASSIGNED TO
0	SYSTEM PORT A
1	SYSTEM PORT B
2	SYSTEM PORT C
3	FINGER PRINT
4	BLUETOOTH

System Power States

- CHP3_SLPS1* S1, Power-On-Suspend(POS) : In this state, all clocks(except the 32.768KHz clock) are stopped. The system context is maintained in system DRAM. Power is maintained to PCI, the CPU, memory controller, memory, and all other critical subsystems. Note that this state does not preclude power being removed from non-essential devices, such as disk drives. During this state, CPU can be selected for either Deep Sleep or Deeper Sleep.
- CHP3_SLPS3* S3, Suspend-To-RAM(STR) : The system context is maintained in system DRAM, but power is shut off to non-critical circuits. Memory is retained, and refreshes continue. All clocks stop except RTC clock.
- CHP3_SLPS4* S4, Suspend-To-Disk(STD) : The Context of the system is maintained on the disk. All power is then shut off to the system except for the logic required to resume. Externally appears same as S5, but may have different wake events.
- CHP3_SLPS5* S5, Soft Off(SOFF) : System context is not maintained. All power is shut off except for the logic required to restart. A full boot is required when waking.

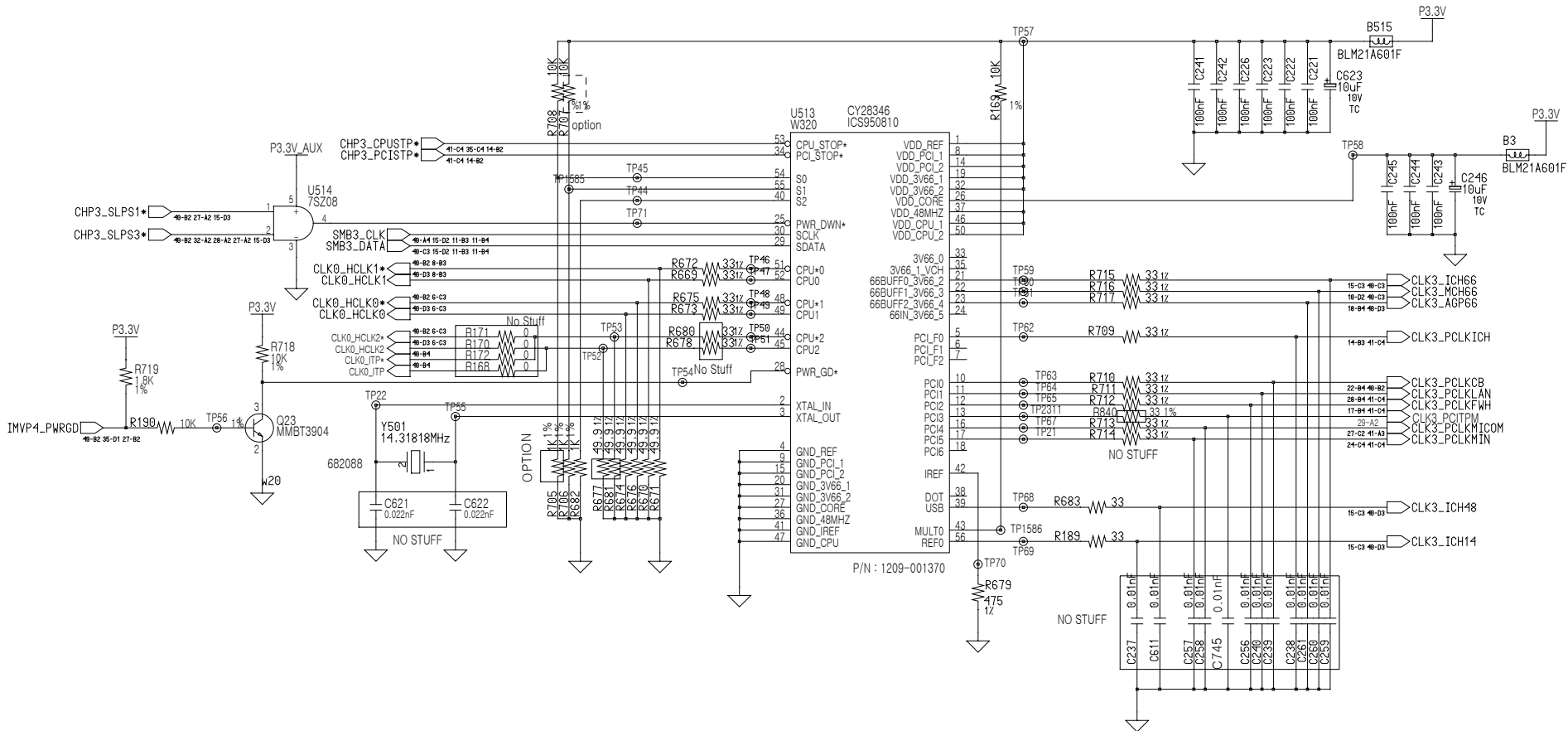
REVISION HISTORY

See rev notes in the changes file for more information.

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APPROVAL	H.S, KIM	REV	1.0	BOARD INFORMATION	PART NO.	BA41-00392A
MODULE CODE		LAST EDIT	March, 30, 2004 10:13:36 AM	PAGE	3	OF 41

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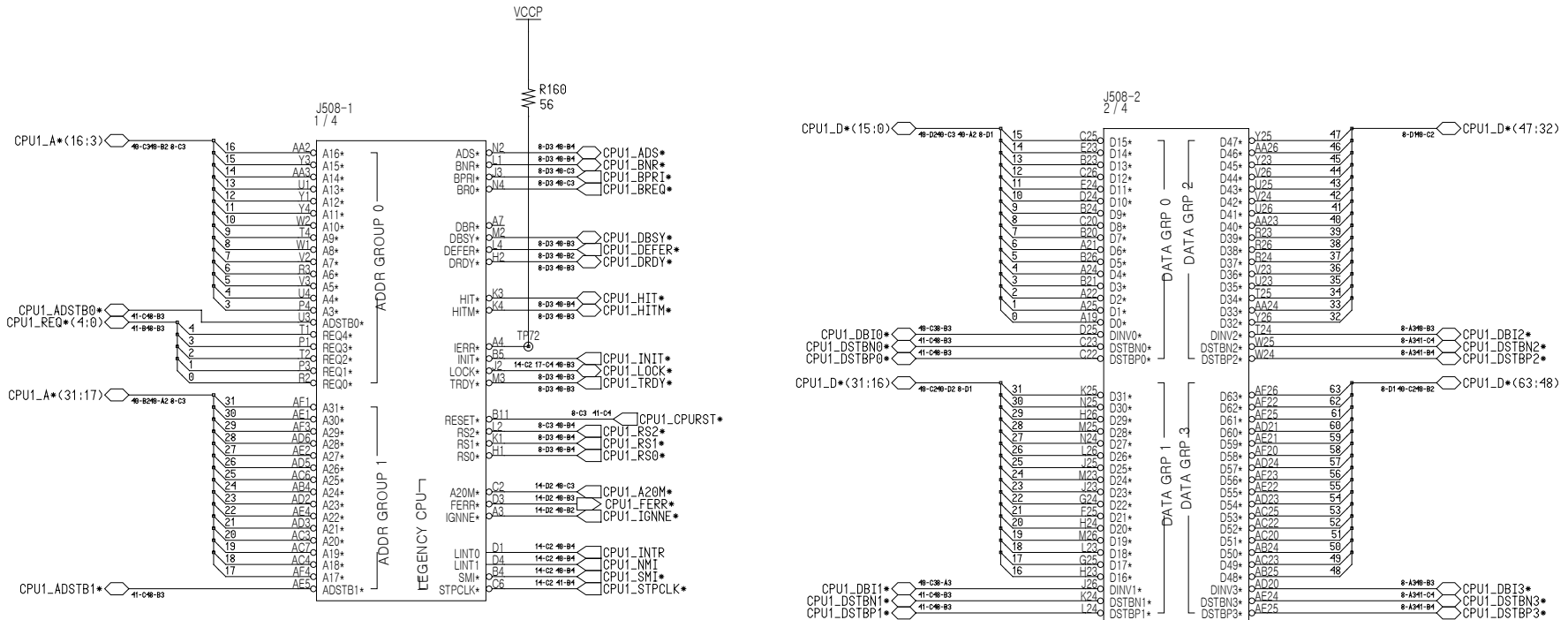


SEL1	SEL0	HOST CLK
0	0	66MHz
0	1	100MHz
1	0	200MHz
1	1	133MHz

DRAW	RYAN, PARK	DATE	3/30/2004	TITLE	CICHL ID CLOCK GENERATOR	SAMSUNG ELECTRONICS PART NO. BA41-00392A
CHECK	H.S, OH	DEV. STEP	MP			
APPROVAL	H.S, KIM	REV	1.0			
MODULE CODE		LAST EDIT				
				March, 30, 2004 10:14:03 AM	PAGE	4 OF 41

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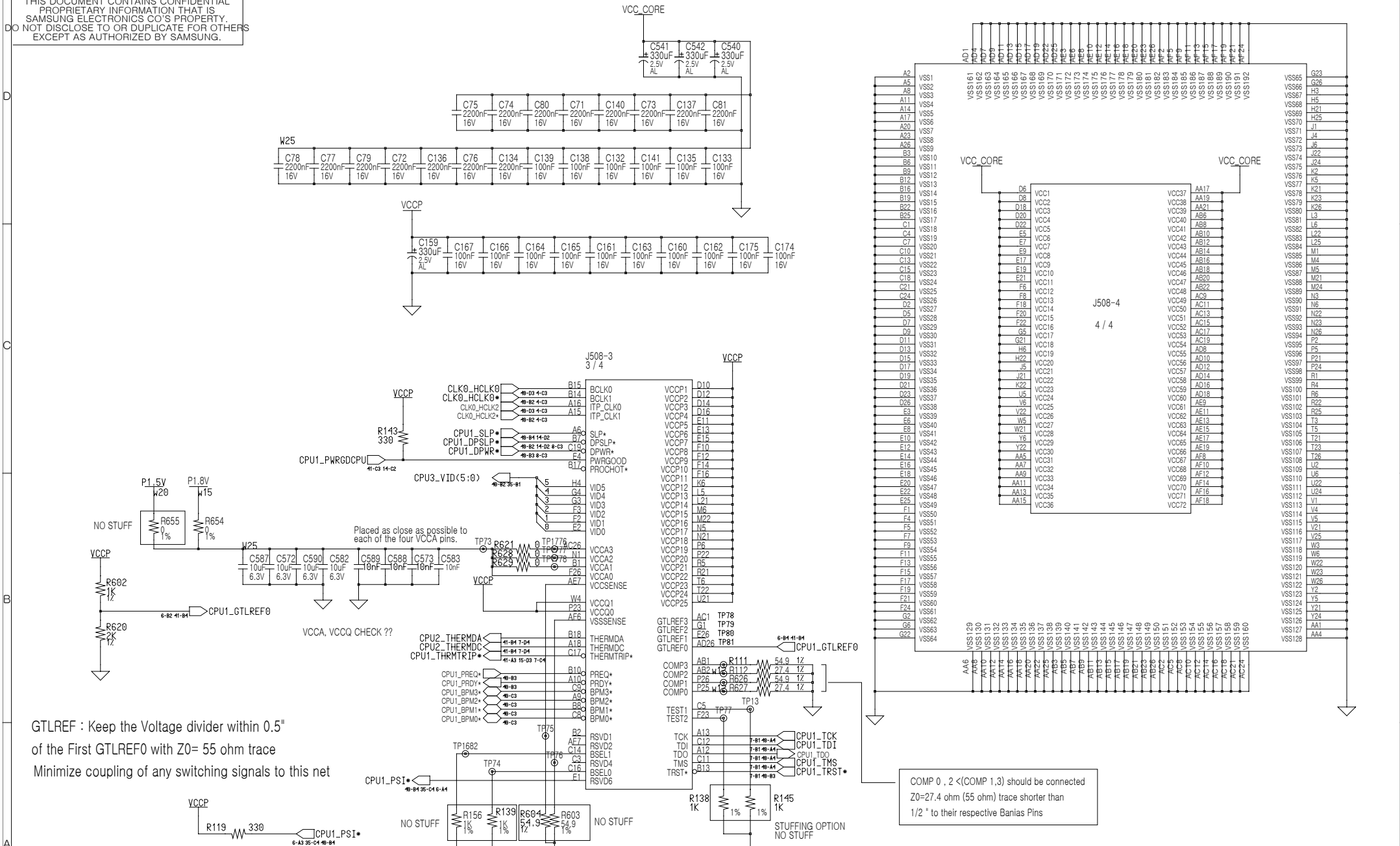
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CHECK	H.S, OH	DEV. STEP	MP			
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MODULE CODE		LAST EDIT		March, 30, 2004 10:14:26 AM	PAGE	5 OF 41

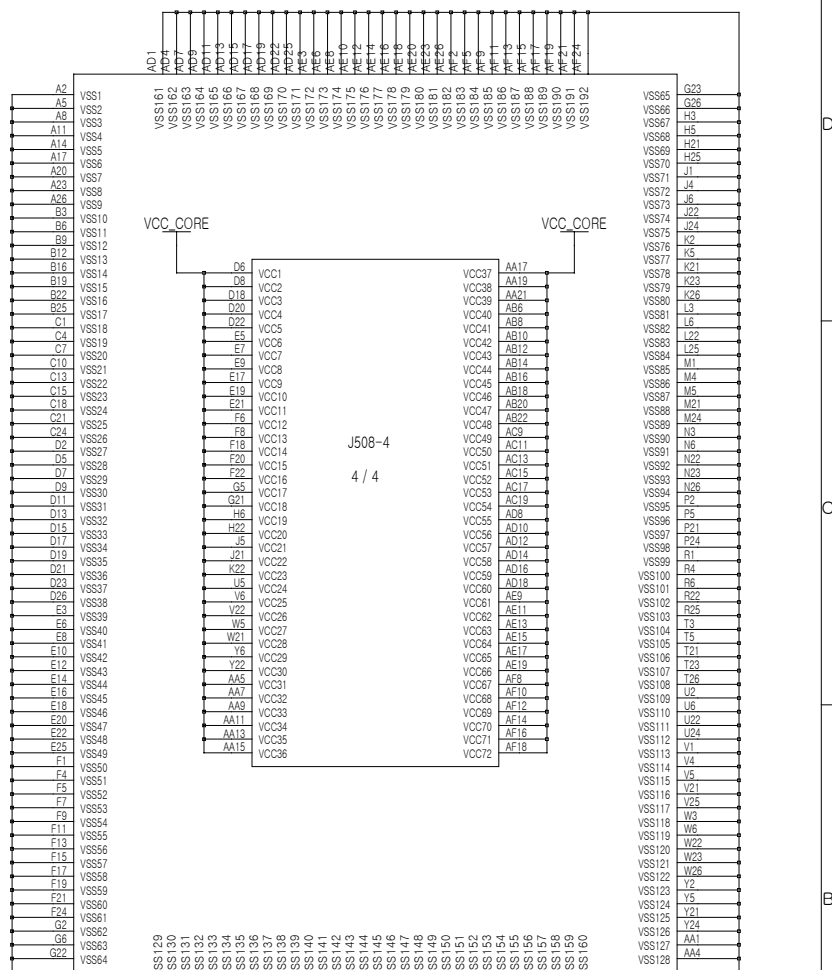
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GTLREF : Keep the Voltage divider within 0.5" of the First GTLREF0 with Z0= 55 ohm trace Minimize coupling of any switching signals to this net

COMP 0 , 2 <(COMP 1,3) should be connected Z0=27.4 ohm (55 ohm) trace shorter than 1/2 " to their respective Banias Pins

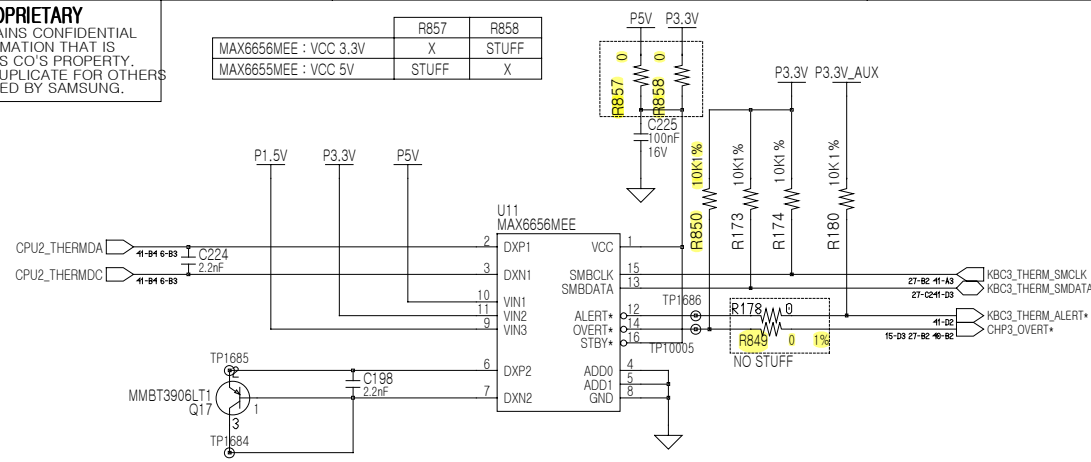


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CHECK	H.S, OH	DEV. STEP	MP			
APPROVAL	H.S, KIM	REV	1.0		BANIAS CPU (2/2)	
MODULE CODE		LAST EDIT				

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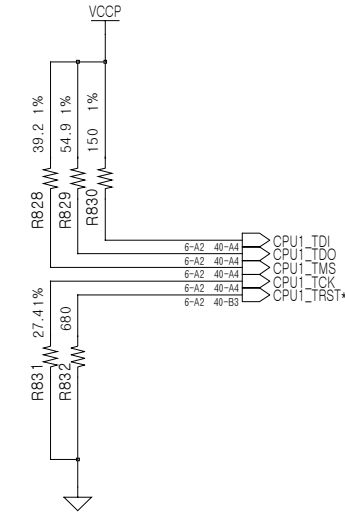
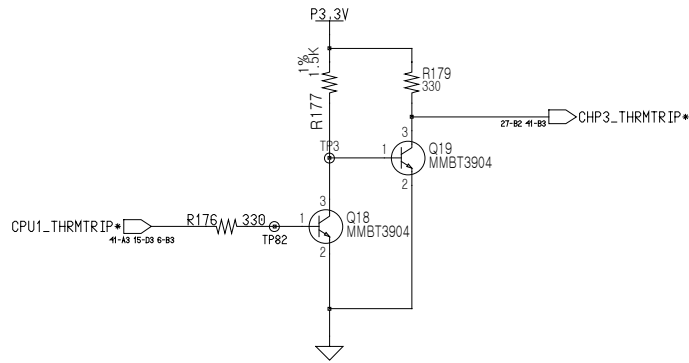
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	R857	R858
MAX6656MEE : VCC 3.3V	X	STUFF
MAX6656MEE : VCC 5V	STUFF	X



Refer To Thermal Sensor Layout Guidelines.

- Place the Thermal Sensor close to a remote diode.
- Keep traces away from high voltage (+12V bus)
- Keep traces away from fast data buses and CRT signal.
- Use recommended trace widths and spacings (10mil)
- Place a ground plane under the traces.
- Use guard traces flanking DXP and DXN and connecting to GND



CPU Core Voltage Table

VID5	VID4	VID3	VID2	VID1	VID0	Voltage	VID5	VID4	VID3	VID2	VID1	VID0	Voltage
0	0	0	0	0	0	1.708 V	1	0	0	0	0	0	1.196 V
0	0	0	0	1	0	1.692 V	1	0	0	0	0	1	1.180 V
0	0	0	0	1	1	1.676 V	1	0	0	0	0	1	1.164 V
0	0	0	0	1	1	1.660 V	1	0	0	0	0	1	1.148 V
0	0	0	1	0	0	1.644 V	1	0	0	0	1	0	1.132 V
0	0	0	1	0	1	1.628 V	1	0	0	0	1	0	1.116 V
0	0	0	1	1	0	1.612 V	1	0	0	0	1	0	1.100 V
0	0	0	1	1	1	1.596 V	1	0	0	0	1	1	1.084 V
0	0	0	1	0	0	1.580 V	1	0	0	0	0	0	1.068 V
0	0	0	1	0	1	1.564 V	1	0	0	0	0	1	1.052 V
0	0	0	1	1	0	1.548 V	1	0	0	0	1	0	1.036 V
0	0	0	1	1	1	1.532 V	1	0	0	0	1	1	1.020 V
0	0	0	1	1	0	1.516 V	1	0	0	0	1	0	1.004 V
0	0	0	1	1	1	1.500 V	1	0	0	0	1	0	0.988 V
0	0	0	1	1	0	1.484 V	1	0	0	0	1	1	0.972 V
0	0	0	1	1	1	1.468 V	1	0	0	0	1	1	0.956 V
0	0	1	0	0	0	1.452 V	1	0	0	0	0	0	0.940 V
0	0	1	0	0	1	1.436 V	1	0	0	0	0	1	0.924 V
0	0	1	0	0	1	1.420 V	1	0	0	0	0	1	0.908 V
0	0	1	0	1	0	1.404 V	1	0	0	0	1	0	0.892 V
0	0	1	0	1	1	1.388 V	1	0	0	0	1	0	0.876 V
0	0	1	0	1	0	1.372 V	1	0	0	0	1	1	0.860 V
0	0	1	0	1	1	1.356 V	1	0	0	0	1	1	0.844 V
0	0	1	0	1	1	1.340 V	1	0	0	0	1	1	0.828 V
0	0	1	0	0	0	1.324 V	1	0	0	0	0	0	0.812 V
0	0	1	0	0	1	1.308 V	1	0	0	0	0	1	0.796 V
0	0	1	1	0	0	1.292 V	1	0	0	0	0	0	0.780 V
0	0	1	1	0	1	1.276 V	1	0	0	0	0	1	0.764 V
0	0	1	1	1	0	1.260 V	1	0	0	0	0	1	0.748 V
0	0	1	1	1	0	1.244 V	1	0	0	0	0	1	0.732 V
0	0	1	1	1	1	1.228 V	1	0	0	0	0	1	0.716 V
0	1	1	1	1	1	1.212 V	1	1	1	1	1	1	0.700 V

Lowest Freq. (VID5=1, VID4=0, VID3=0, VID2=0, VID1=0, VID0=0) Voltage: 0.844 V

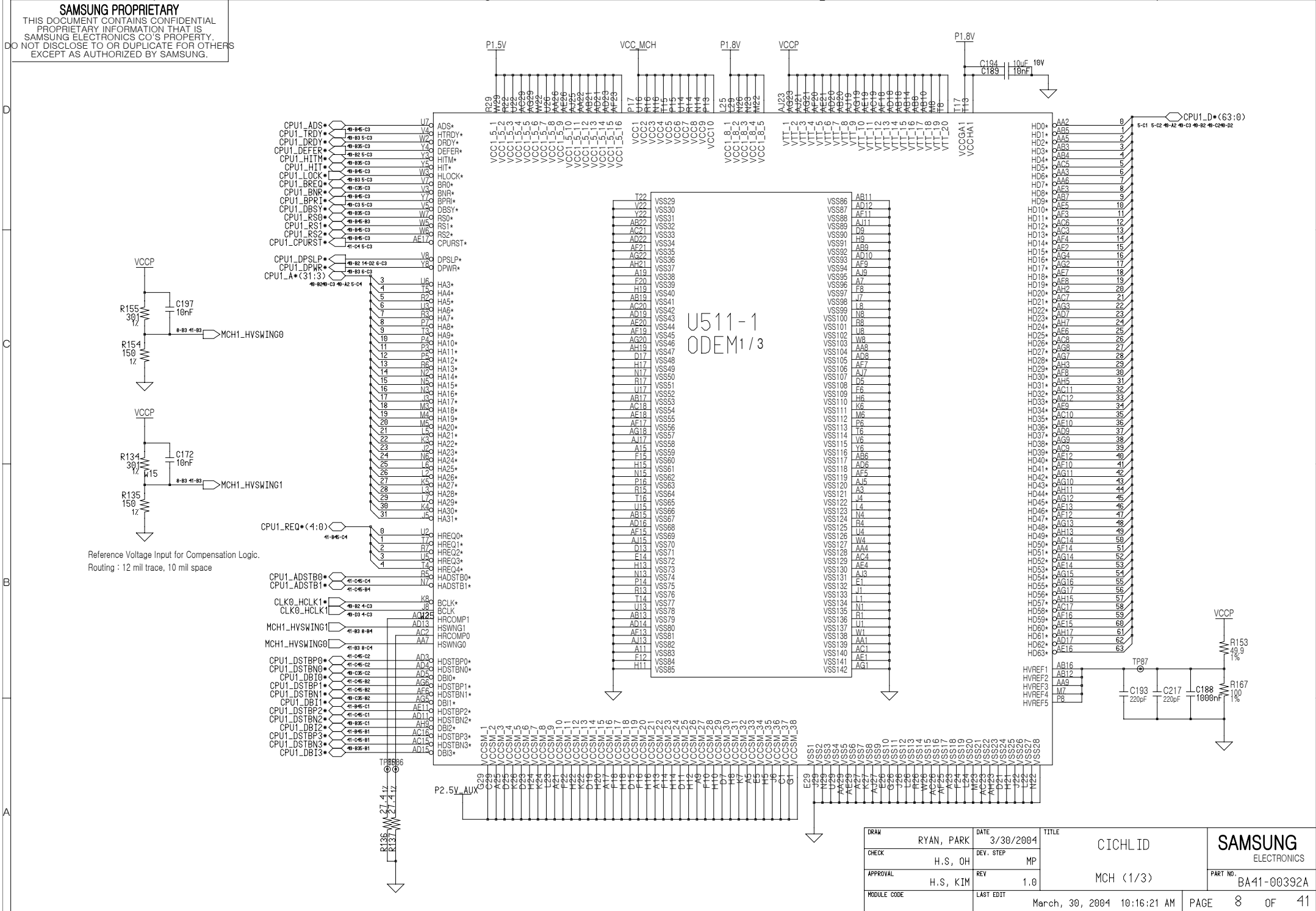
Deeper Sleep (VID5=1, VID4=0, VID3=0, VID2=0, VID1=0, VID0=1) Voltage: 0.748 V

DRAW	KI. IM	DATE	4/7/2003	TITLE	AQUILA W MAIN	SAMSUNG ELECTRONICS
CHECK	KK.BIN	DEV. STEP	DV	THERMAL SENSOR & VID		
APPROVAL	DW.KIM	REV	1.0	PART NO. BA41-#####		
MODULE CODE	LAST EDIT		April 7, 2003 8:36:31 AM		PAGE	7 OF 42

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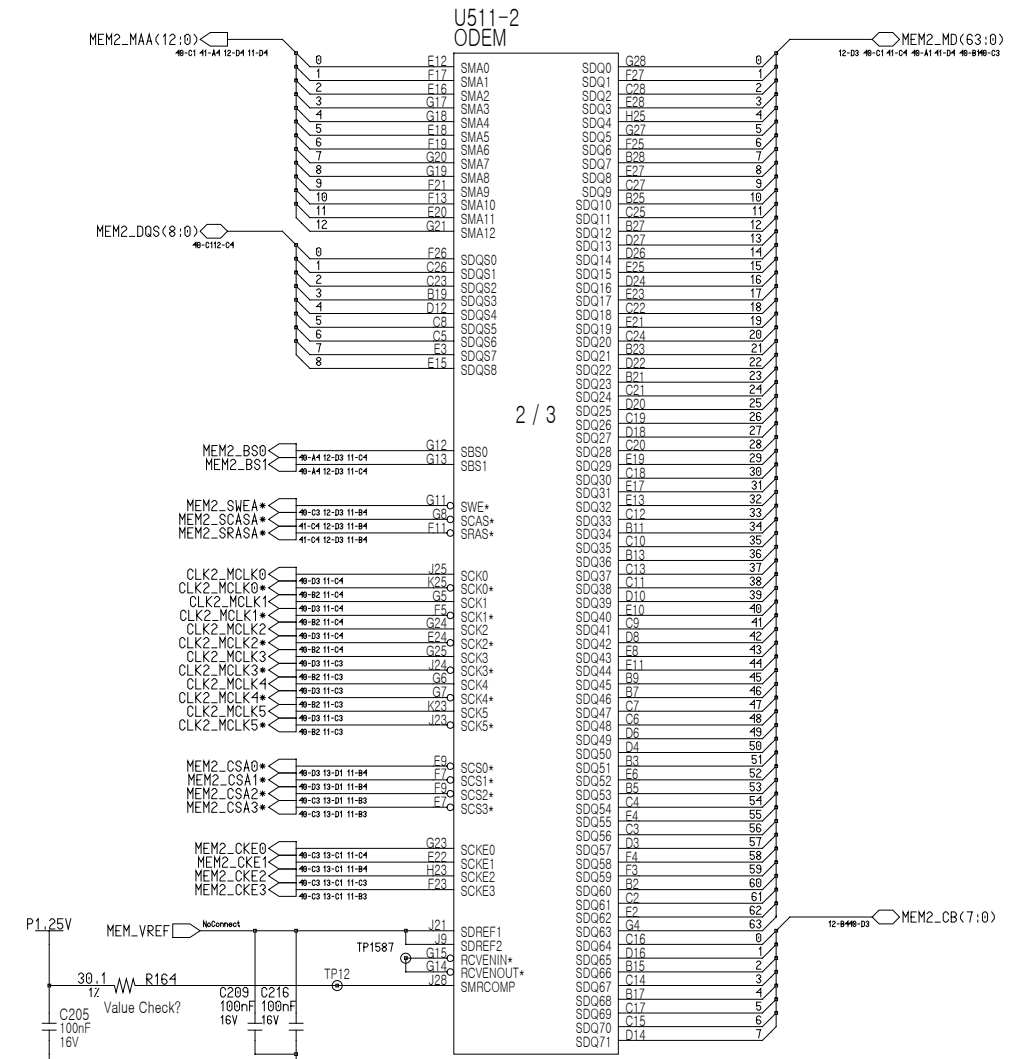


Reference Voltage Input for Compensation Logic.
Routing : 12 mil trace, 10 mil space

DRAW	RYAN, PARK	DATE	3/30/2004	TITLE	CICHL ID MCH (1/3)	
CHECK	H.S, OH	DEV. STEP	MP	PART NO.		
APPROVAL	H.S, KIM	REV	1.0	BA41-00392A		
MODULE CODE		LAST EDIT				
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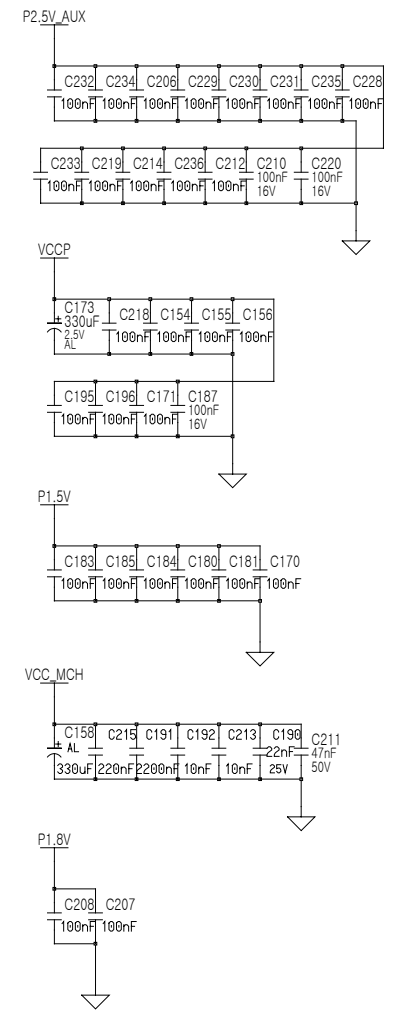
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Place the R,C within 1" of the MCH-M.

- DDR Clocks Routing
- > SCK/SCK#[0] = SCK/SCK#[1] = SCK/SCK#[2]
 - > SCK/SCK#[3] = SCK/SCK#[4] = SCK/SCK#[5]
 - > Differential clock length must be 1~2" longer than Strobe signals.
 - > Differential clock length must be 1~3" longer than Control and Command signals.

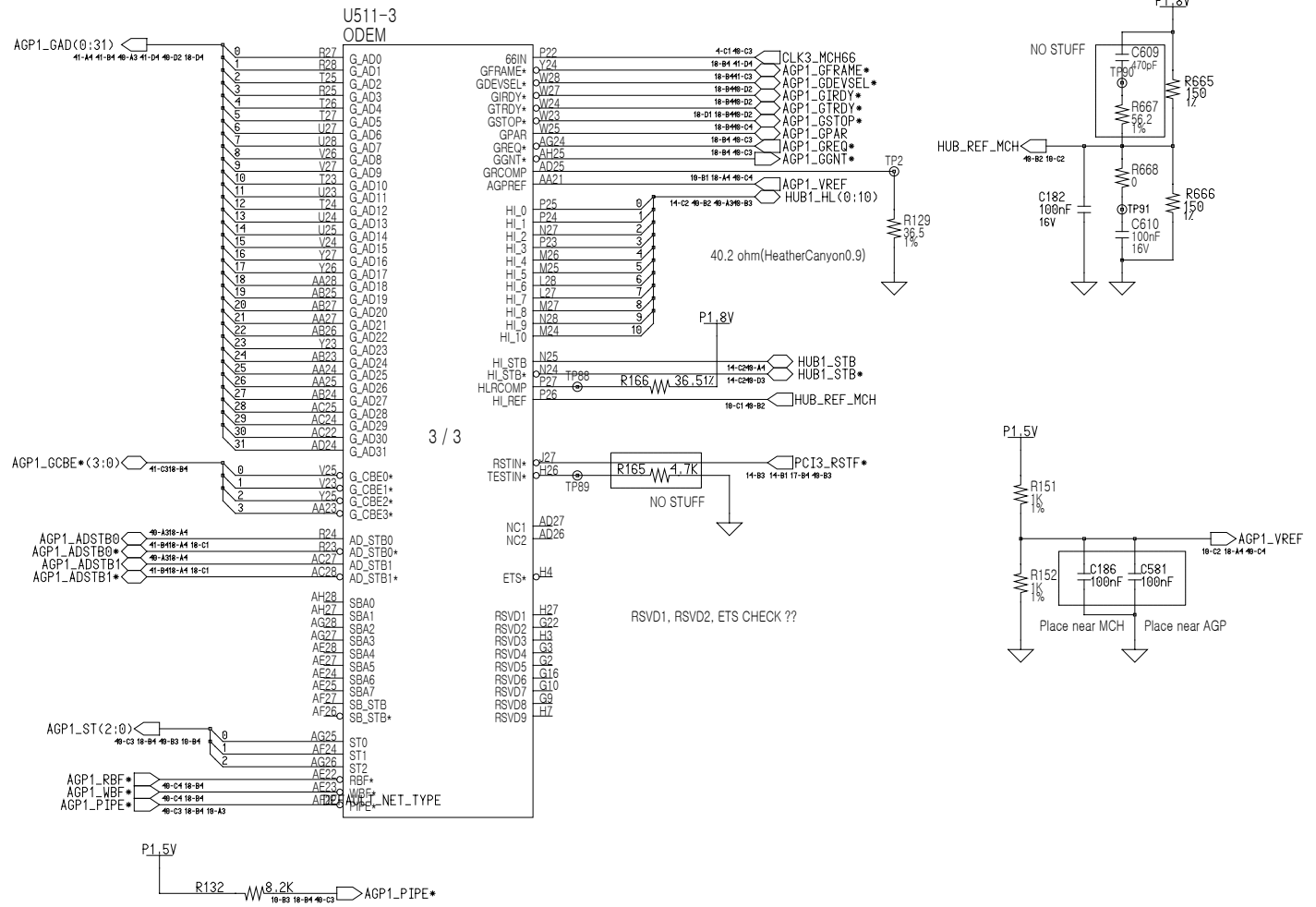
- DDR Feedback Routing
- MCH signal ball to signal Via = Max 40 mil
 - MCH output signal via to input signal via = 95mil ~ 105 mil
 - RCVEN Signal must be routed on the same layer as the memory clocks.



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APPROVAL	H.S, KIM	REV	1.0	MCH (2/3)	PART NO.	BA41-00392A
MODULE CODE		LAST EDIT		March, 30, 2004 10:18:51 AM	PAGE	9 OF 41

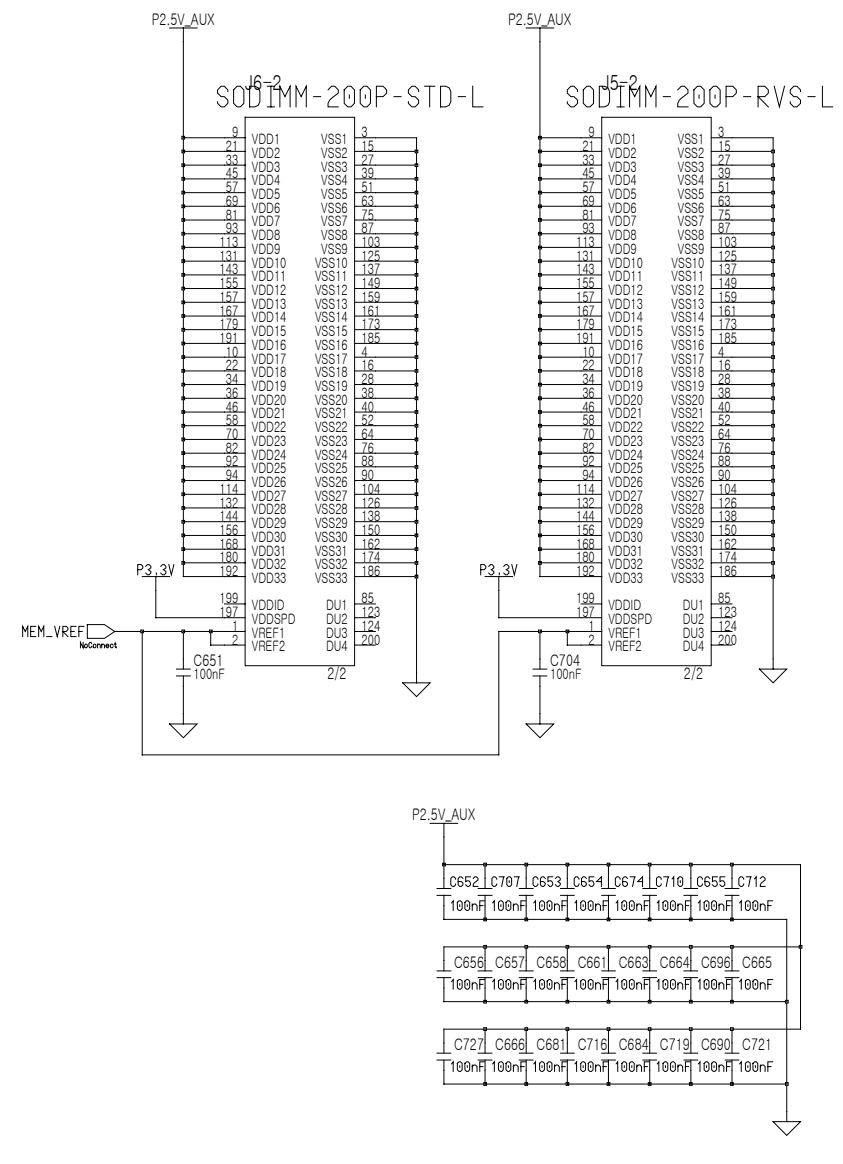
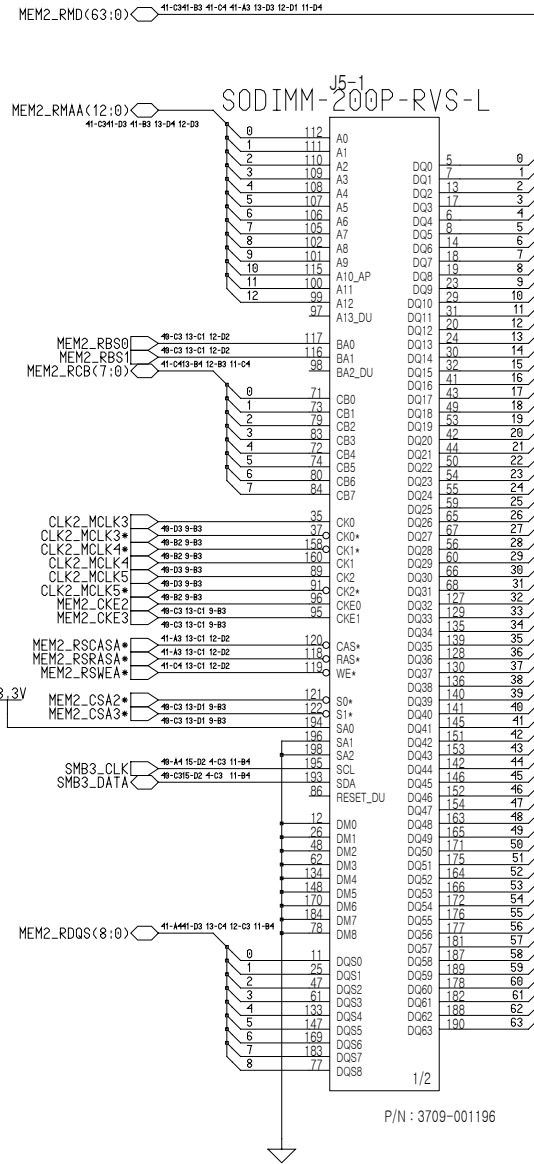
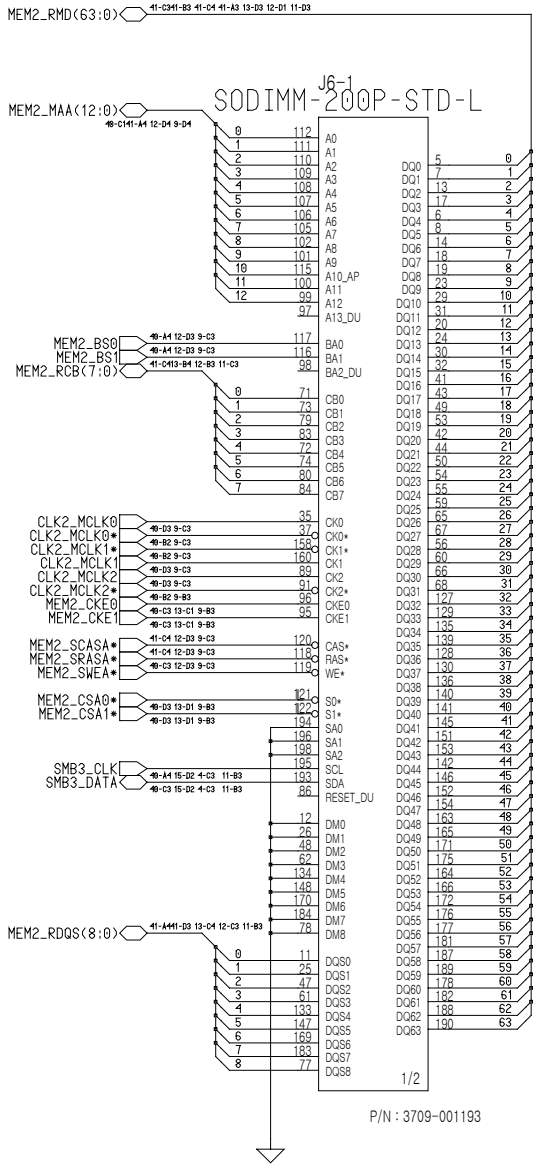
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ST1	ST2	MCH Strap
X	1	DDR
0	X	TEST
1	X	400 MHz

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APPROVAL	H.S, KIM	REV	1.0		MCH (3/3)	PART NO. BA41-00392A
MODULE CODE		LAST EDIT		March, 30, 2004 10:19:07 AM	PAGE 10 OF 41	

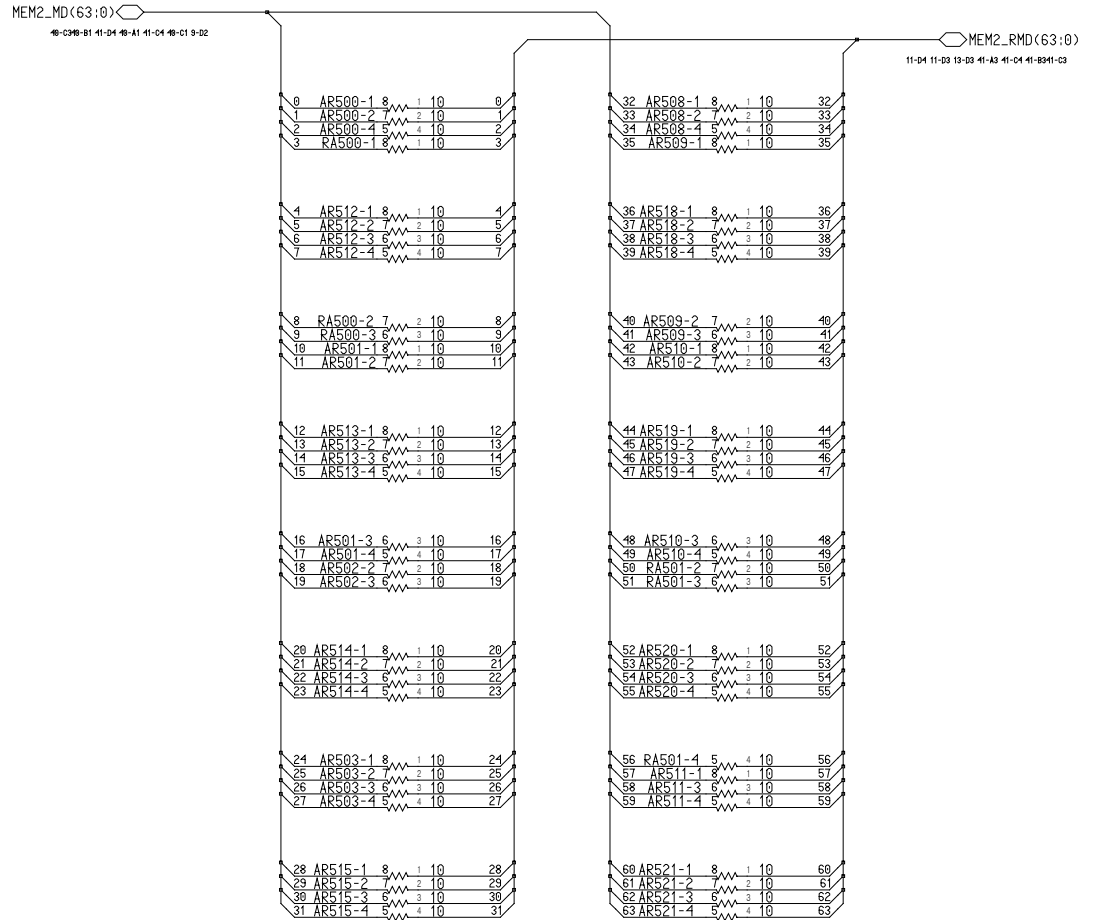
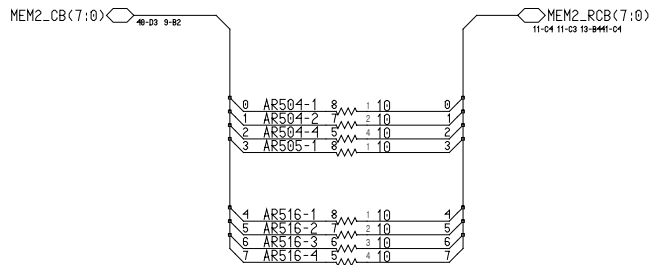
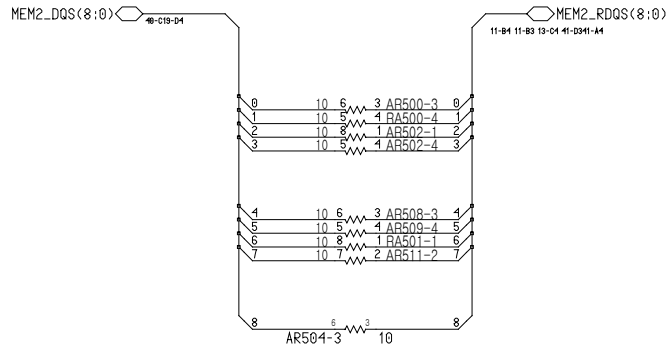
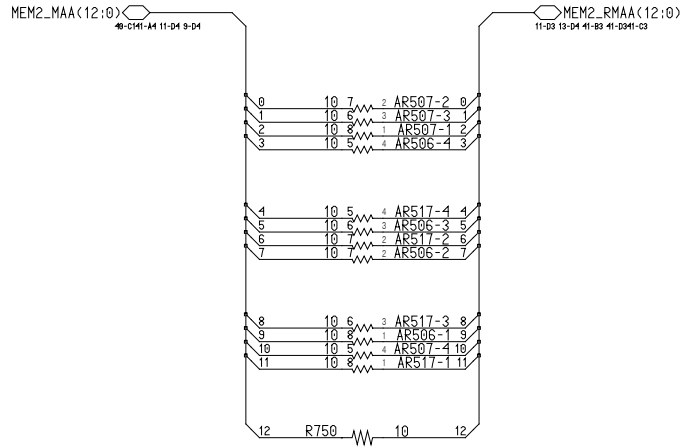
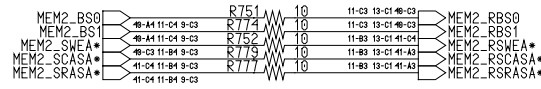


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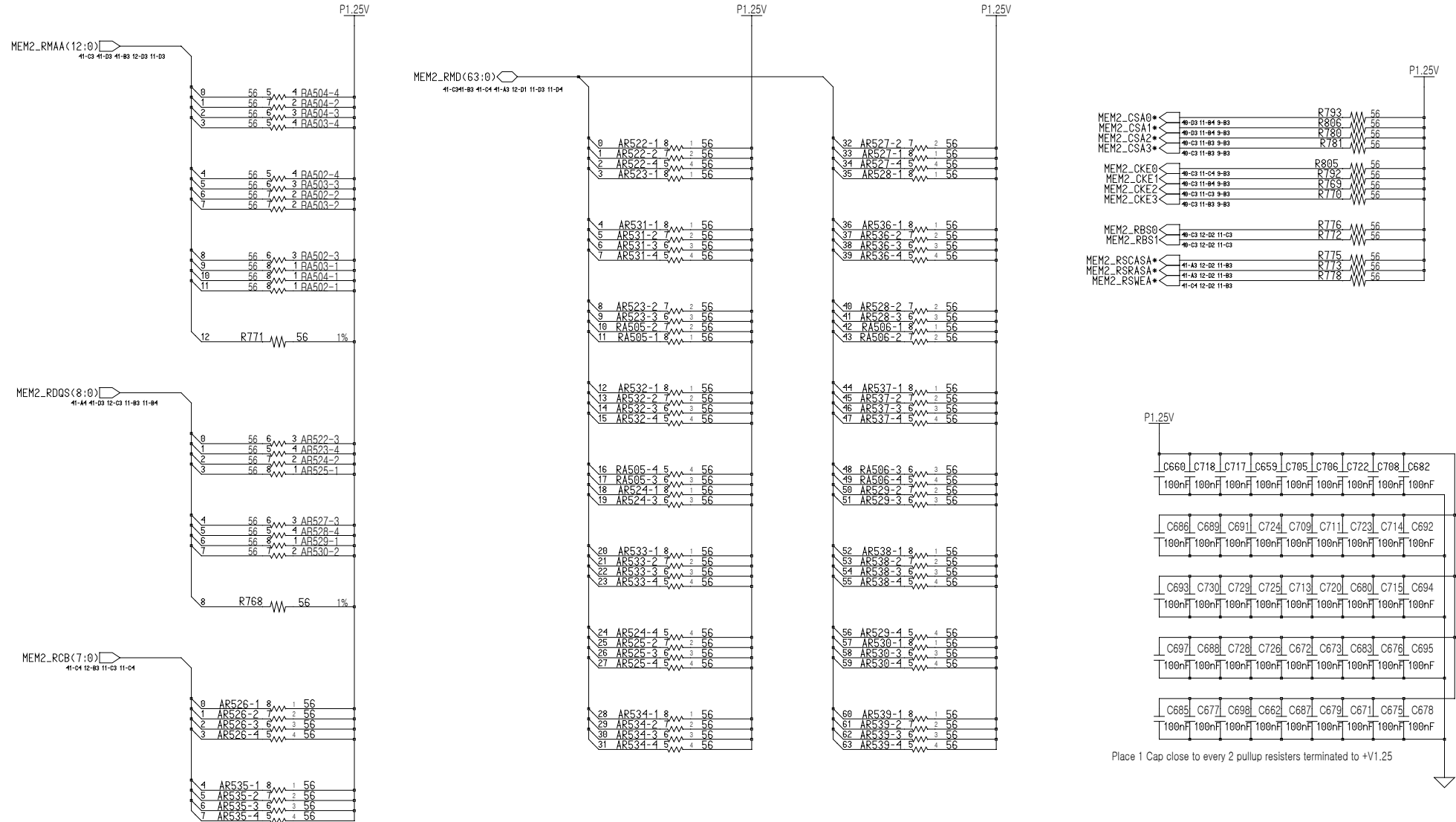
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DRAW	RYAN, PARK	DATE	3/30/2004	TITLE	CICHLID	SAMSUNG ELECTRONICS
CHECK	H.S, OH	DEV. STEP	MP			
APPROVAL	H.S, KIM	REV	1.0	DDR S-TERMINATION	PART NO.	BA41-00392A
MODULE CODE		LAST EDIT		March, 30, 2004 10:21:51 AM	PAGE	12 OF 41

SAMSUNG PROPRIETARY

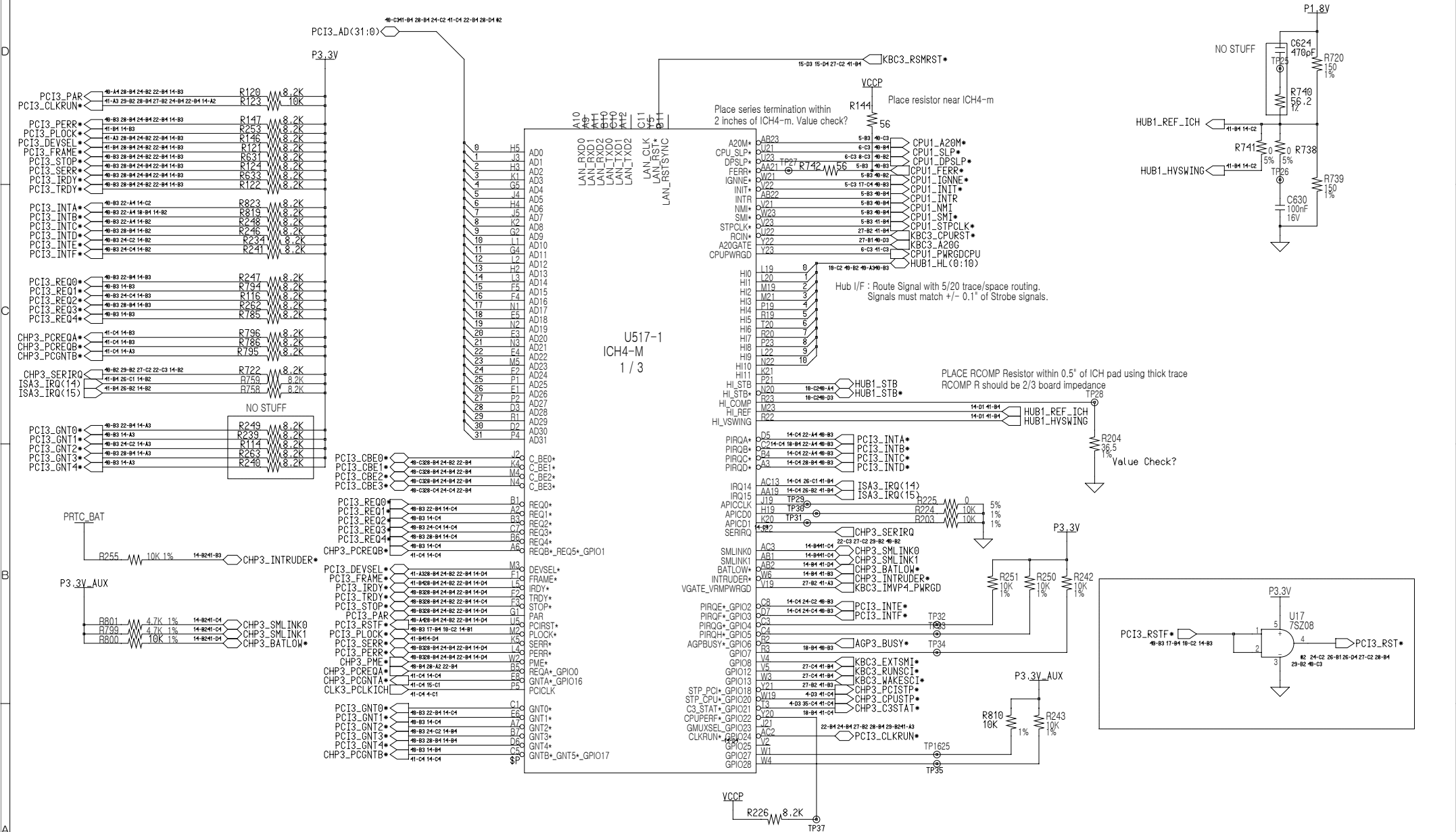
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DRAW	RYAN, PARK	DATE	3/30/2004	TITLE	CICHL ID	SAMSUNG ELECTRONICS
CHECK	H.S, OH	DEV. STEP	MP			
APPROVAL	H.S, KIM	REV	1.0	DDR P-TERMINATION	PART NO.	BA41-00392A
MODULE CODE		LAST EDIT		March, 30, 2004 10:23:05 AM	PAGE	13 OF 41

SAMSUNG PROPRIETARY

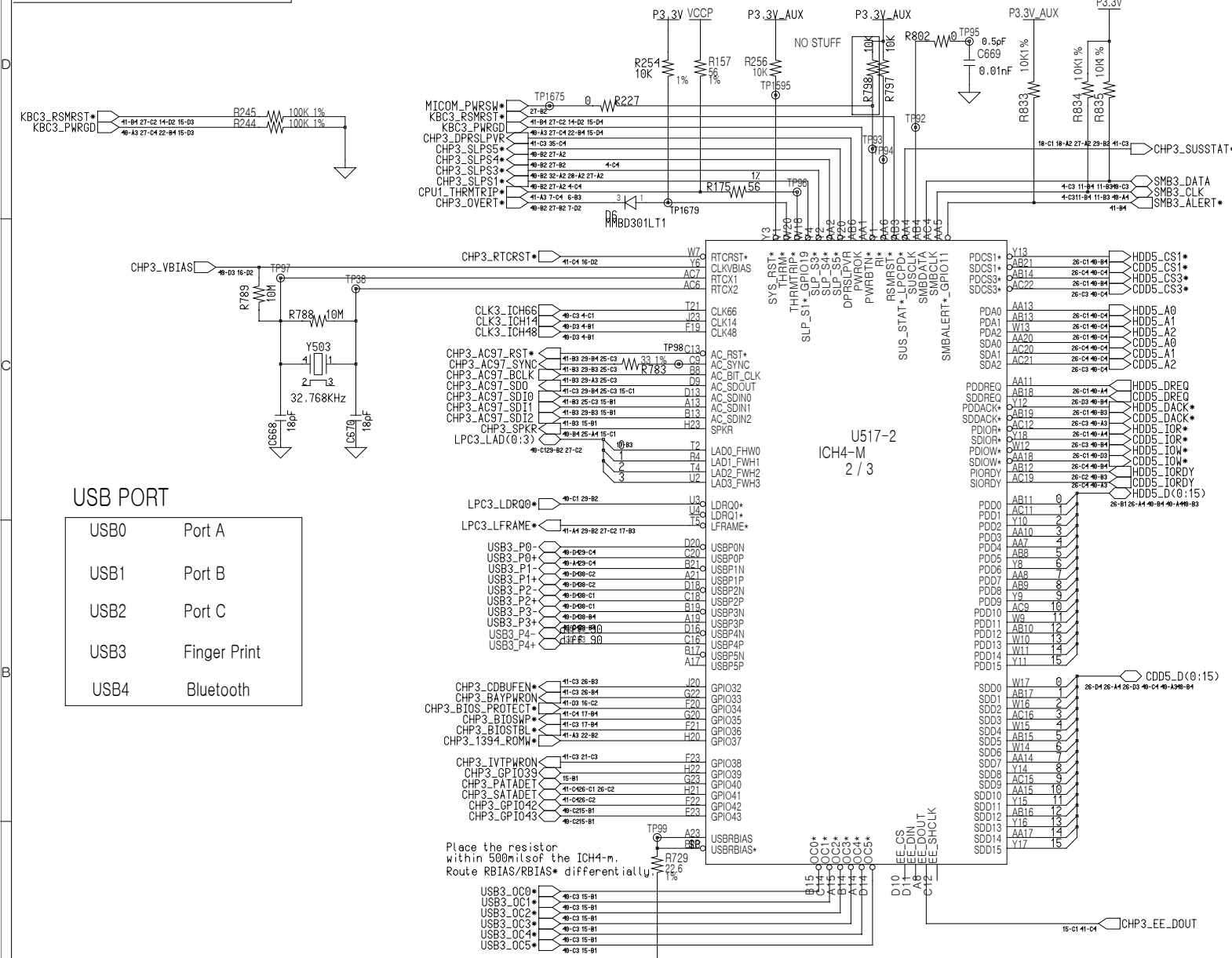
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DRAW	RYAN, PARK	DATE	3/30/2004	TITLE	ICHL ID	SAMSUNG ELECTRONICS
CHECK	H.S, OH	DEV. STEP	MP			
APPROVAL	H.S, KIM	REV	1.0		ICHL-M (1/3)	PART NO. BA41-00392A
MODULE CODE		LAST EDIT			March, 30, 2004 10:23:29 AM	PAGE 14 OF 41

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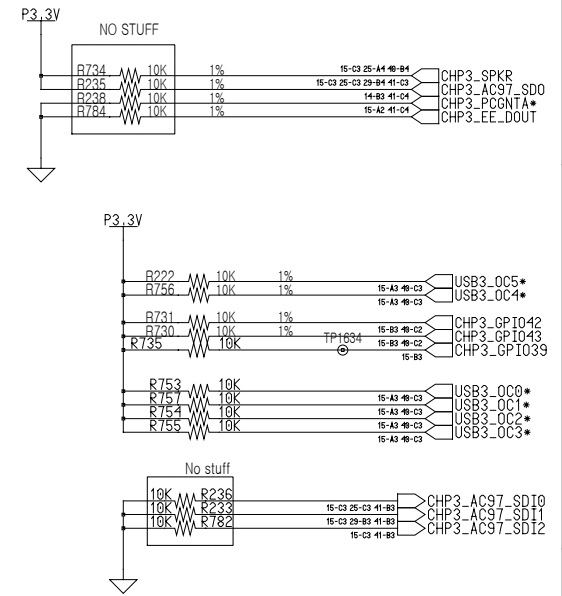
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ICH4-m Strapping Options

	Function	Default
ICH_SPKR	No Reboot	No Stuff
AC97_SDOUT	Safe Mode	No Stuff
PC/PCI GNTA*	A16 swap override	No Stuff
ECP_DOUT	Reserved	No Stuff

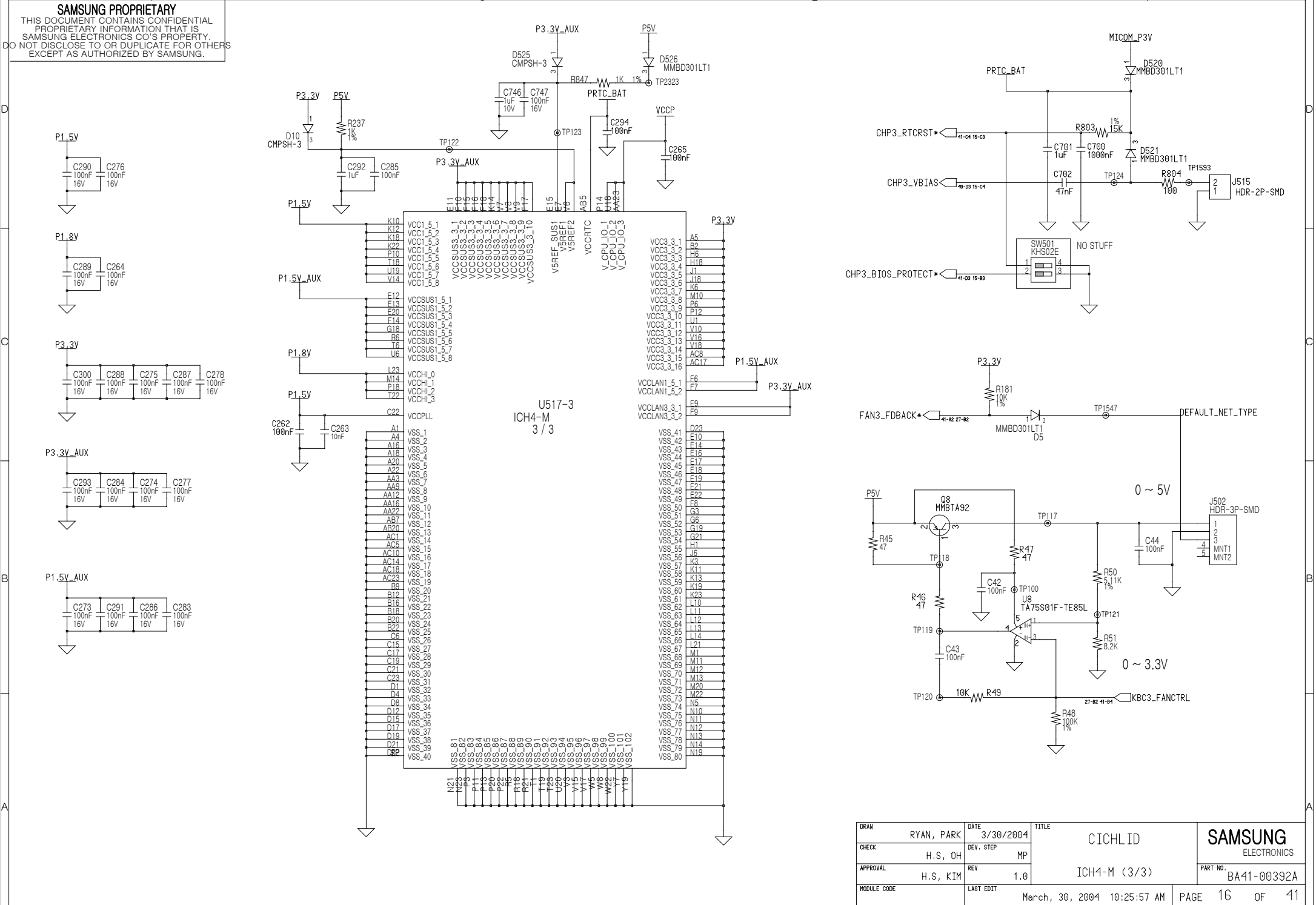
Primary CODEC : AUDIO
Secondary CODEC : MODEM



DRAW	RYAN, PARK	DATE	3/30/2004	TITLE	CICHL ID	SAMSUNG ELECTRONICS	
CHECK	H.S, OH	DEV. STEP	MP				
APPROVAL	H.S, KIM	REV	1.0		ICH4-M (2/3)	PART NO.	
MODULE CODE		LAST EDIT		March, 30, 2004 10:25:28 AM		BA41-00392A	
						PAGE	15 OF 41

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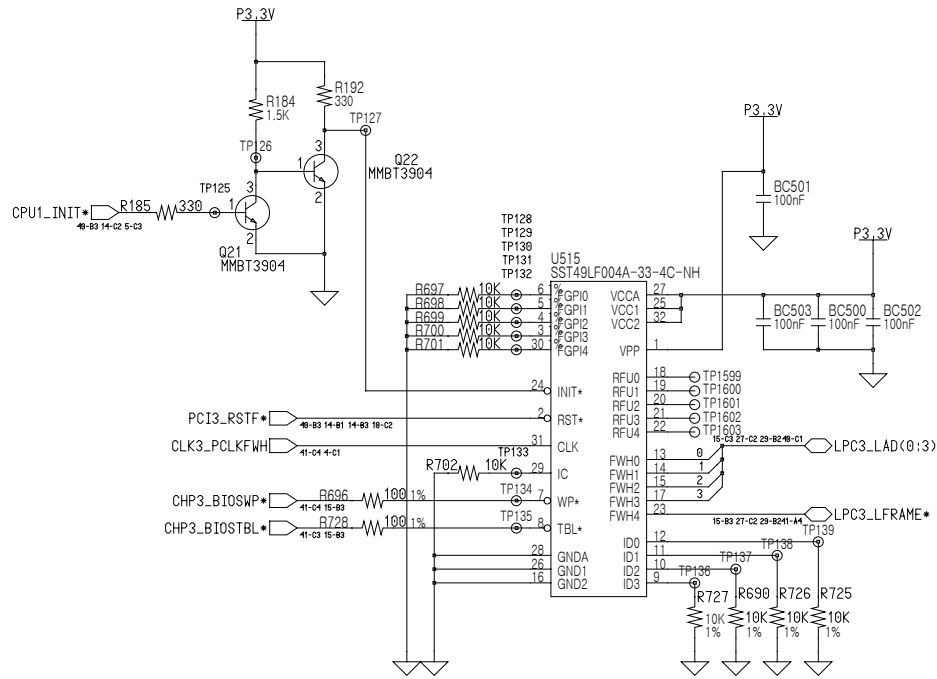
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DRAW	RYAN, PARK	DATE	3/30/2004	TITLE	ICHL ID	SAMSUNG ELECTRONICS
CHECK	H.S, OH	DEV. STEP	MP			
APPROVAL	H.S, KIM	REV	1.0		ICHL-M (3/3)	PART NO. BA41-00392A
MODULE CODE		LAST EDIT		March, 30, 2004 10:25:57 AM	PAGE 16	OF 41

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```

02 VERIFY REAL MODE
03 DISABLE NMI
04 GET CPU TYPE
06 INIT, SYSTEM H/W
08 INIT, CHIPSET REG.
09 SET IN POST FLAG
0A INIT CPU.REG
0B CPU CACHE ON
0C INIT.CACHE TO POST
0E INIT, I/O VALUE
0F ENABLE THE L-BUS IDE
10 INIT, POWER MANAGER
11 LOAD ALTERNATE REG.
13 PCI BUS MASTER RESET WITH INITIAL POST VALUE
14 INIT, KEYBOARD CONTROLLER
16 CHECK CHECKSUM
18 8254 TIMER INIT.
1A 8237 DMA CONTROLLER INIT.
1C RESET INTERRUPT CONTROLLER
20 TEST DRAM REFRESH
22 TEST 8742 KEYBOARD CONTROLLER
24 SET ES SEGMENT REG. TO 4GB
26 ENABLE A20
28 AUTO SIZING DRAM
32 COMPUTE THE CPU SPEED
34 TESET CMOS RAM
38 SHADOW SYSTEM BIOS ROM
3A AUTO SIZING CACHE
3C CONFIGURE ADVANCED CHIPSET REG.
3D LOAD ALTER REG. WITH CMOS VALUE
42 INIT, INTERRUPT VECTOR
44 INIT, BIOS INTERRUPT
46 CHECK ROM COPYRIGHT NOTICE
47 INIT, I20 SUPPORT IF INSTALLED
48 CHECK VIDEO CONFIGURE AGAINST CMOS
49 INIT, PCI BUS AND DEVICE
4A INIT, ALL VIDEO BIOS ROM
4C SHADOW VIDEO BIOS ROM
50 DISPLAY CPU TYPE AND SPEED
52 TEST KEYBOARD
54 SET KEYCLICK IF ENABLED
56 ENABLE KEYBOARD
58 TEST FOR UNEXPECTED INTERRUPTS
5A DISPLAY " PRESS ..... SETUP"
5C TEST RAM BETWEEN 512K AND 640K
60 TEST EXTENDED MEMORY
62 TEST EXTENDED MEMORY ADDRESS LINE
64 JUMP TO USER PATCH 1
    
```

```

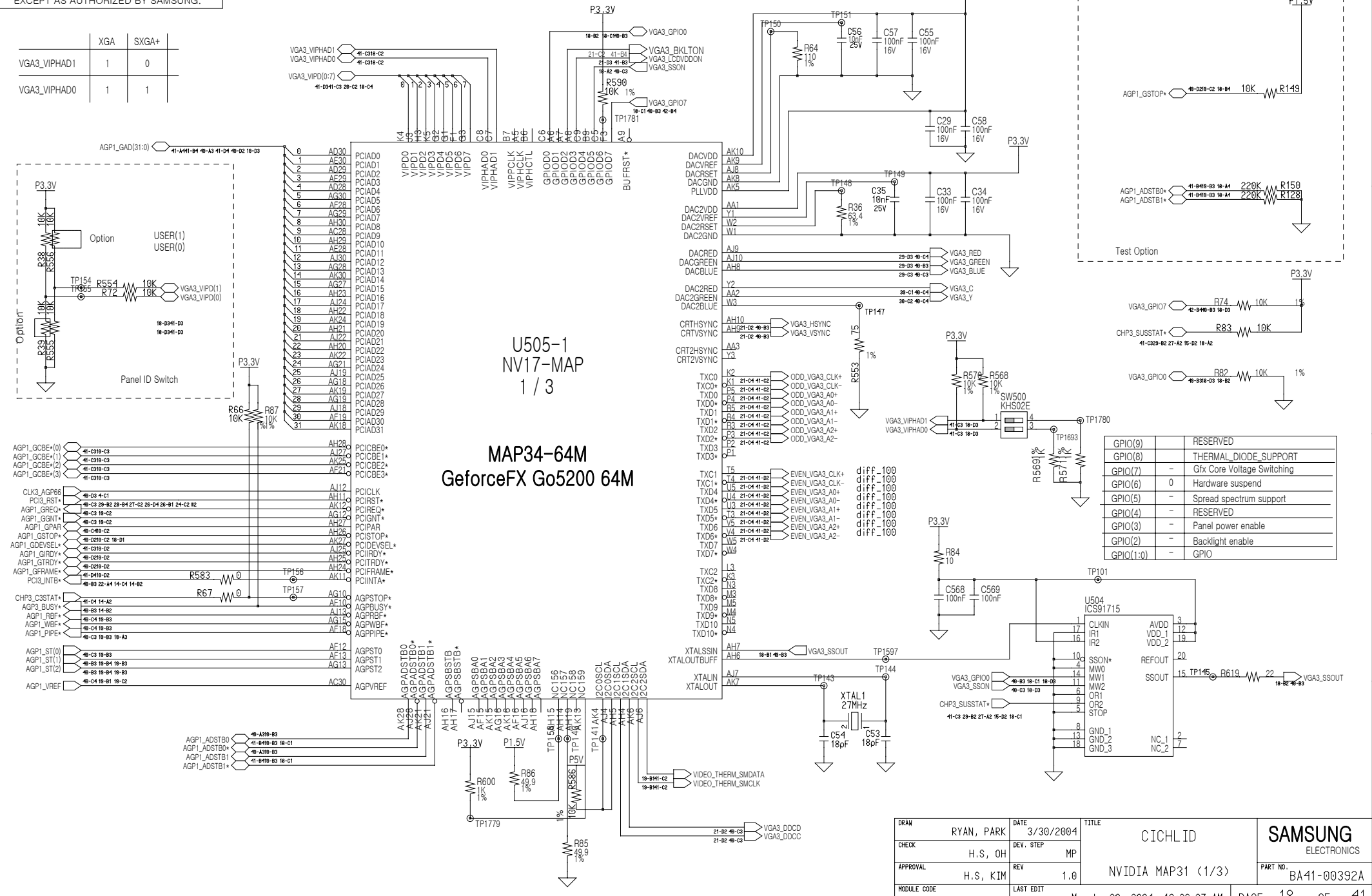
66 CONFIGURE ADVANCE CACHE REG.
6A DISPLAY EXTERNAL CACHE SIZE
6C DISPLAY SHADOW MESSAGE
6E DISPLAY NON-DISPOSABLE SEGMENT
70 DISPLAY ERROR MESSAGE
72 CHECK FOR CONFIGURATION ERROR
74 TEST REAL-TIME CLOCK
76 CHECK FOR KEYBOARD EERROR
7C SETUP HARDWARE INTERRUPT VECTOR
7E TEST COPROCESSER IF PRESENT
80 DISABLE ON-BOARD I/O PORT
82 DETECT AND INSTALL EXT.RS232C
84 DETECT AND INSTALL EXT.PARALLEL RE-INIT, ON-BOARD I/O PORT
86 INIT, BIOS DATA ROM
8A INIT.EXTENDED BIOS DATA AREA
8C INIT, FDD CONTROLLER
9A SHADOW OPTION ROMS
9C SETUP POWER MANAGEMENT
9E ENABLE H/W INTERRUPT
A0 SET TIME OF DAY
A4 INIT, TYPOMATIC RATE
A8 ERASE F2 PROMPT
AA SCAN FOR F2 KEY STROKE
AC ENTER SETUP
AE CLEAR IN POST FLAG
B0 CHECK FOR ERRORS
B2 POST DONE-PREPARE TO BOOT O/S
B4 ONE BEEP
B6 CHECK PASSWORD (OPTION)
B7 ACPI INIT
BA DMI INIT
BE CLEAR SCREEN
C0 TRY BOOT WITH INT19
D0 INTERRUPT HANDLER ERROR
D2 UNKNOWN INTERRUPT ERROR
D4 PENDING INTERRUPT ERROR
D6 SHUTDOWN 5
D8 SHUTDOWN ERROR
DA EXTENDED BLOCK MOVE
DC SHUTDOWN 10
89 ENABLE NMI
90 INIT, HDD CONTROLLER
91 INIT, LOCAL BUS HDD CONTROLLER
92 JUMP TO USER PATCH 2
94 DISABLE A20 ADDRESS LINE
96 CLEAR HUGE ES SEGMENT REG.
98 SEARCH FOR OPTION ROMS
    
```

DRAW	RYAN, PARK	DATE	3/30/2004	TITLE	CICHL ID	SAMSUNG ELECTRONICS
CHECK	H.S, OH	DEV. STEP	MP			
APPROVAL	H.S, KIM	REV	1.0	FIRMWARE HUB	PART NO.	BA41-00392A
MODULE CODE		LAST EDIT	March, 30, 2004 10:26:13 AM	PAGE	17	OF 41

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	XGA	SXGA+
VGA3_VIPHAD1	1	0
VGA3_VIPHAD0	1	1



**U505-1
NV17-MAP
1 / 3**

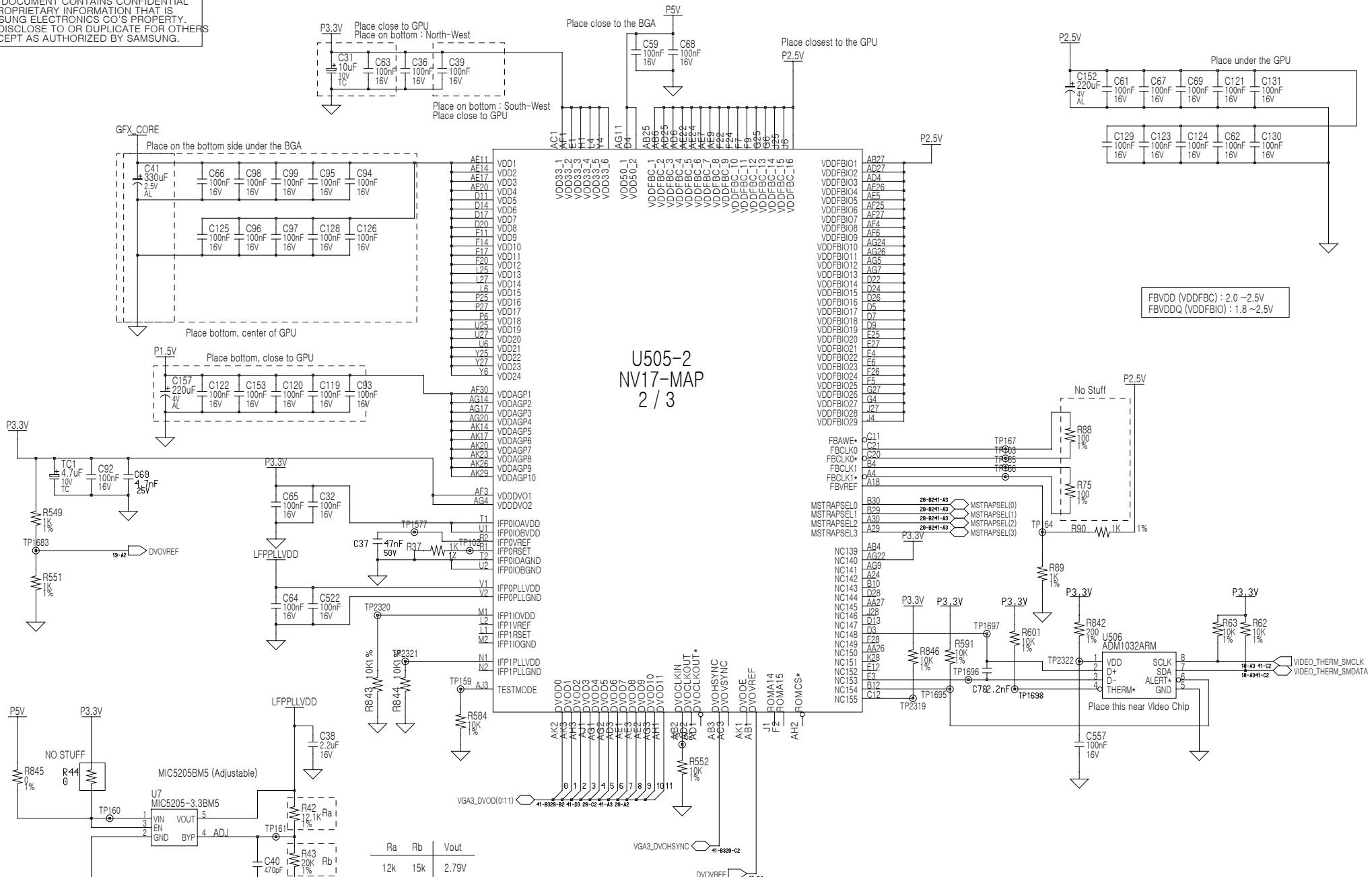
**MAP34-64M
GeForceFX Go5200 64M**

GPIO(9)	RESERVED
GPIO(8)	THERMAL_DIODE_SUPPORT
GPIO(7)	Glx Core Voltage Switching
GPIO(6)	0 Hardware suspend
GPIO(5)	Spread spectrum support
GPIO(4)	RESERVED
GPIO(3)	Panel power enable
GPIO(2)	Backlight enable
GPIO(1:0)	GPIO

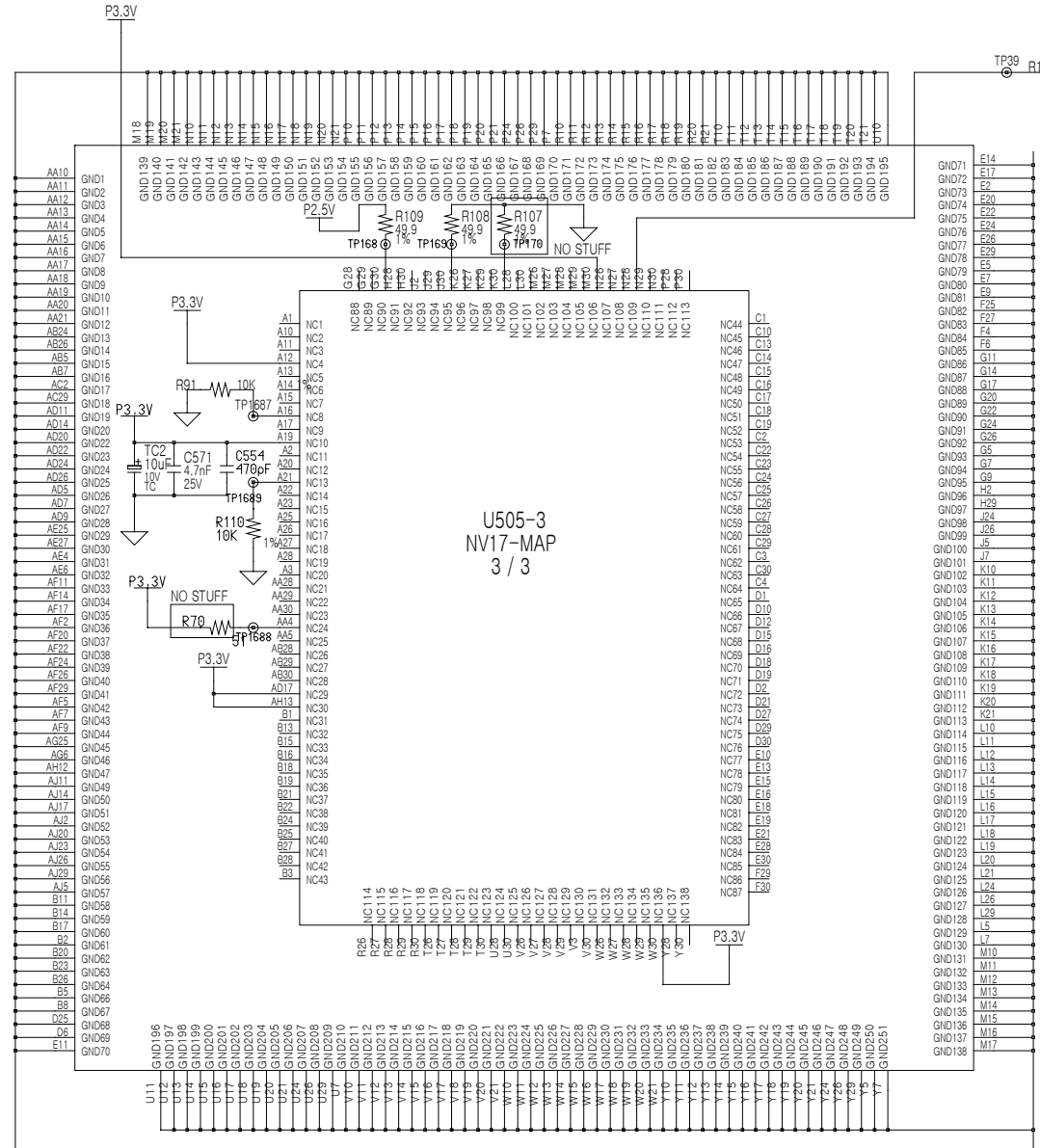
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CHECK	H.S, OH	DEV. STEP	MP			
APPROVAL	H.S, KIM	REV	1.0		NVIDIA MAP31 (1/3)	PART NO. BA41-00392A
MODULE CODE		LAST EDIT			March, 30, 2004 10:26:37 AM	PAGE 18 OF 41

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Strapping Option

Table with 3 columns: Strapping Register, Value, and Description. Rows include VIPD(2):DVOD(10), DVOD(11), HSYNC,VIPD, VIPD(7), DVOD[9], DVOD[8:7], VIPD(6):DVOD(6), DVOD[5:2], DVOD(1), and DVOD(0).

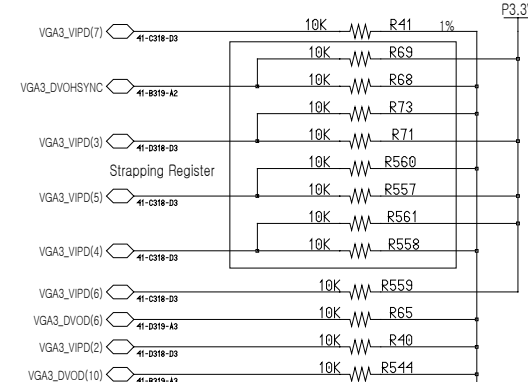
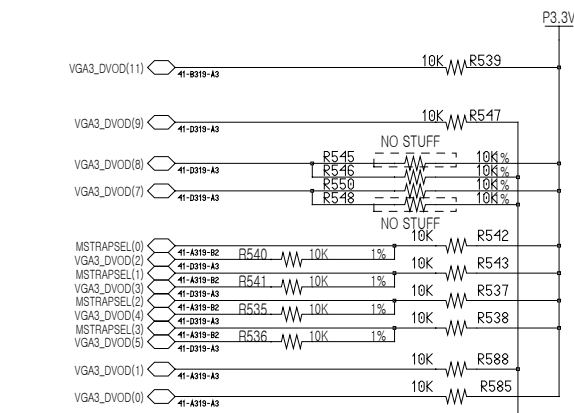


Table with 4 columns: Register Name, 32MB, 64MB, and MAP34. Rows include VGA3_DVOHSYNC, VGA3_VIPD(3), VGA3_VIPD(5), and VGA3_VIPD(4).

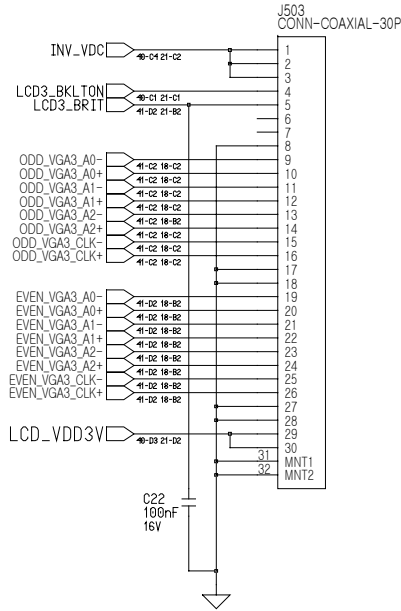


Revision table with columns: DRAW, CHECK, APPROVAL, MODULE CODE, DATE, DEV. STEP, REV, LAST EDIT, TITLE, CICHL ID, SAMSUNG ELECTRONICS, PART NO., and page information (PAGE 20 OF 41).

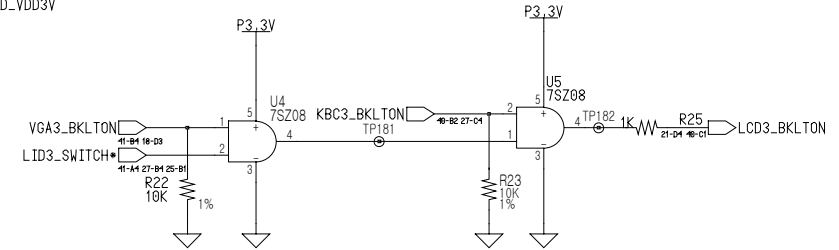
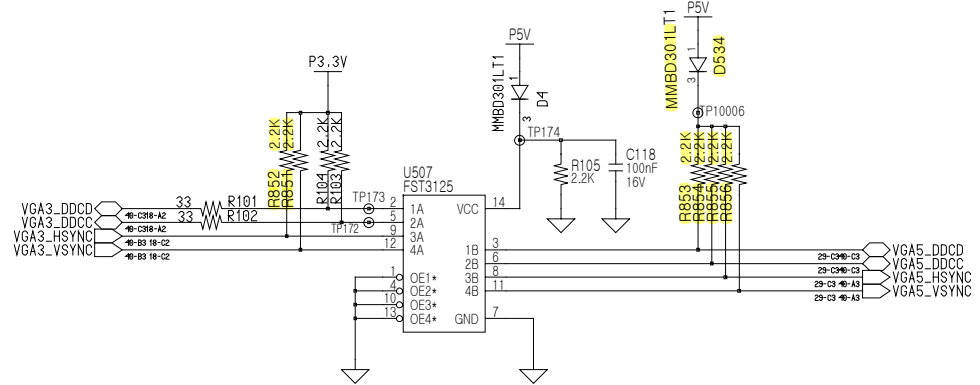
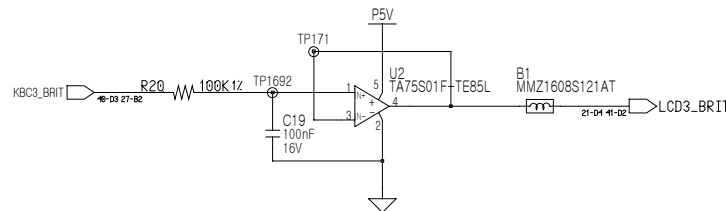
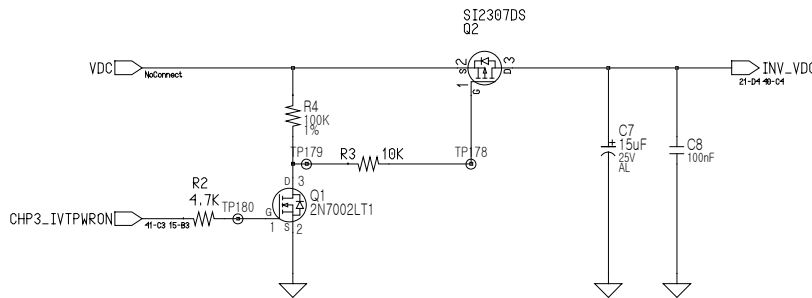
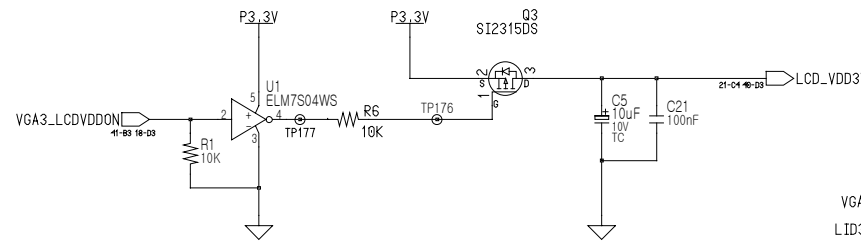
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LCD CONNECTOR



	XGA	SXGA+
VGA3_VIPHAD1	1	0
VGA3_VIPHAD0	1	1

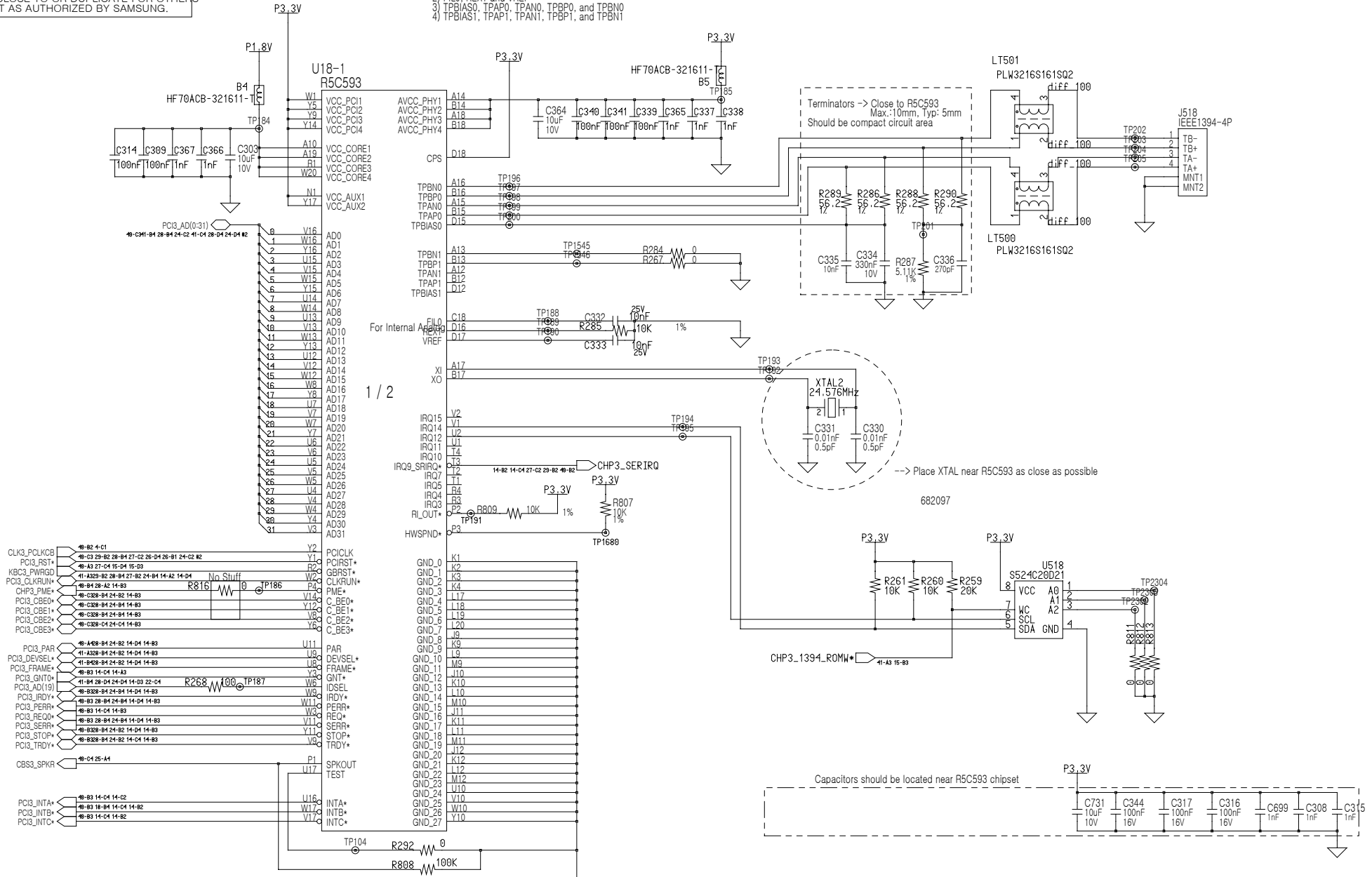


DRAW	KI. IM	DATE	4/7/2003	TITLE	AQUILA W MAIN LCD_CONNECTOR	SAMSUNG ELECTRONICS
CHECK	KK.BIN	DEV. STEP	DV	PART NO.		
APPROVAL	DW.KIM	REV	1.0	BA41-#####		
MODULE CODE		LAST EDIT				

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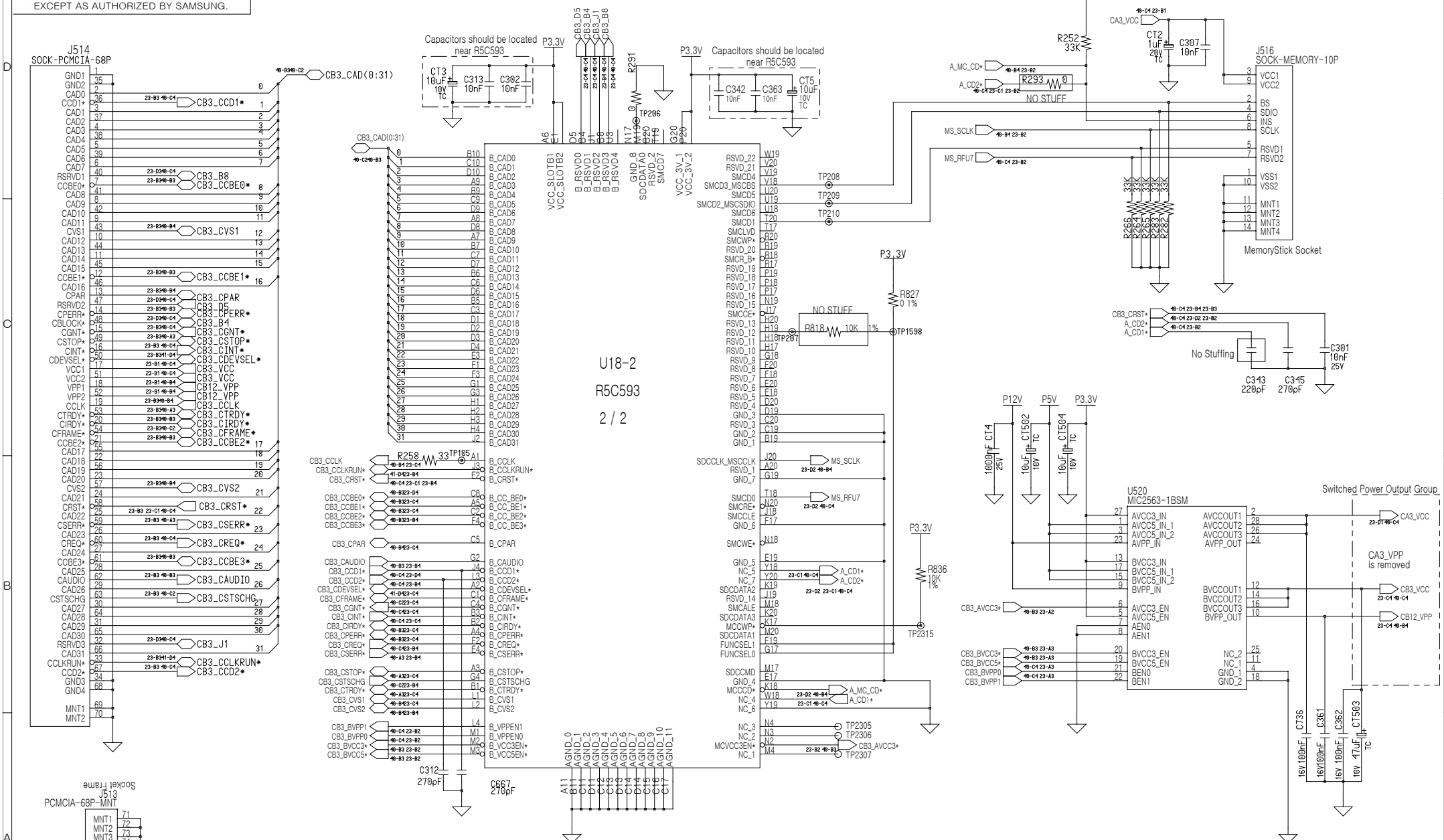
- * GUARD GROUND *
- Apply Guard Grounding to Following Signals
- 1) Xtal for X1/X0 (Y1 24.576MHz) and its capacitors
- 2) FILO, REXT and VREF
- 3) TPBIAS0, TPAP0, TPAN0, TPBP0, and TPBN0
- 4) TPBIAS1, TPAP1, TPAN1, TPBP1, and TPBN1



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CARDBUS SOCKET CONNECTOR



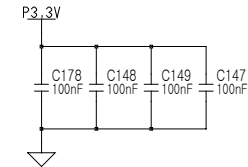
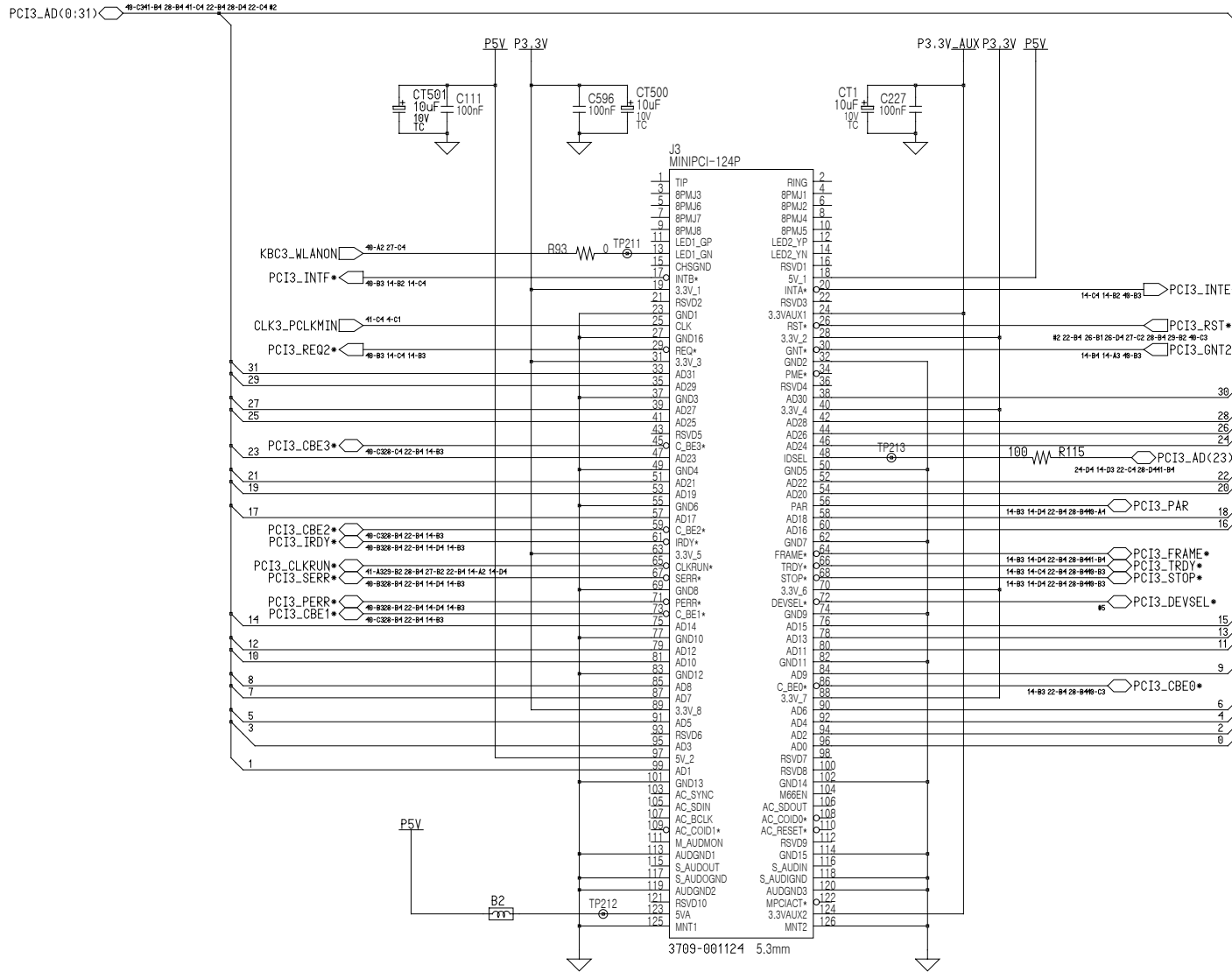
U18-2
R5C593
2 / 2

DRAW	RYAN, PARK	DATE	3/30/2004	TITLE	CICHL ID	SAMSUNG ELECTRONICS
CHECK	H.S, OH	DEV. STEP	MP			
APPROVAL	H.S, KIM	REV	1.0		CARDBUS SOCKET	PART NO. BA41-00392A
MODULE CODE		LAST EDIT	March, 30, 2004 10:29:38 AM	PAGE	23	OF 41

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MINIPCI



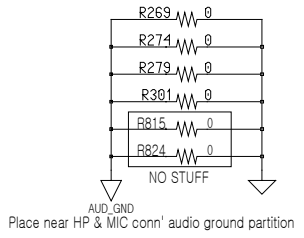
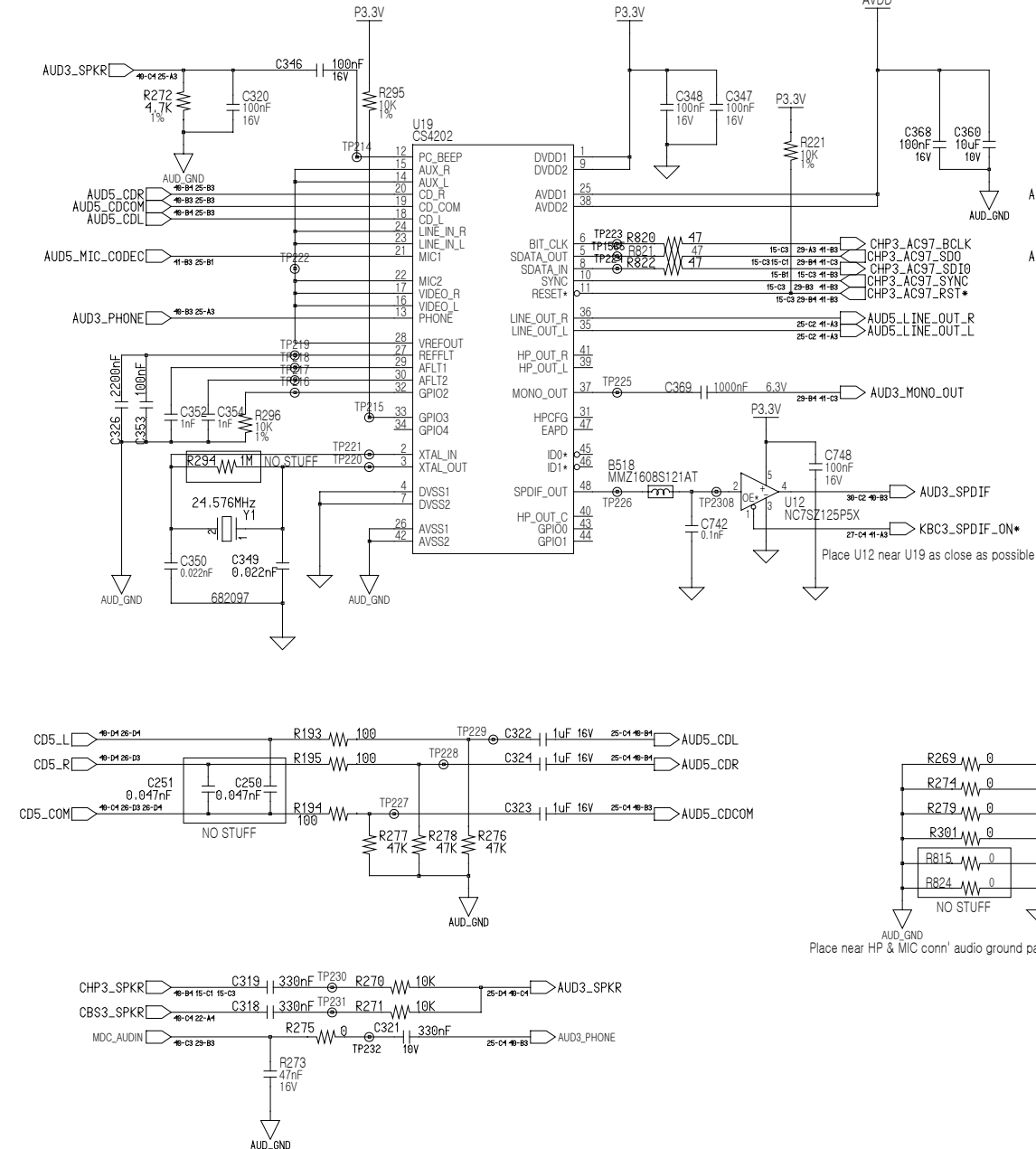
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CHECK	H.S, OH	DEV. STEP	MP			
APPROVAL	H.S, KIM	REV	1.0	MINI PCI	PART NO.	BA41-00392A
MODULE CODE		LAST EDIT		March, 30, 2004 10:29:54 AM	PAGE	24 OF 41

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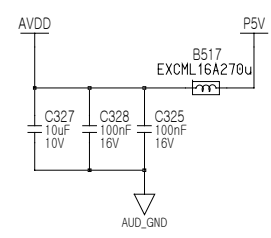
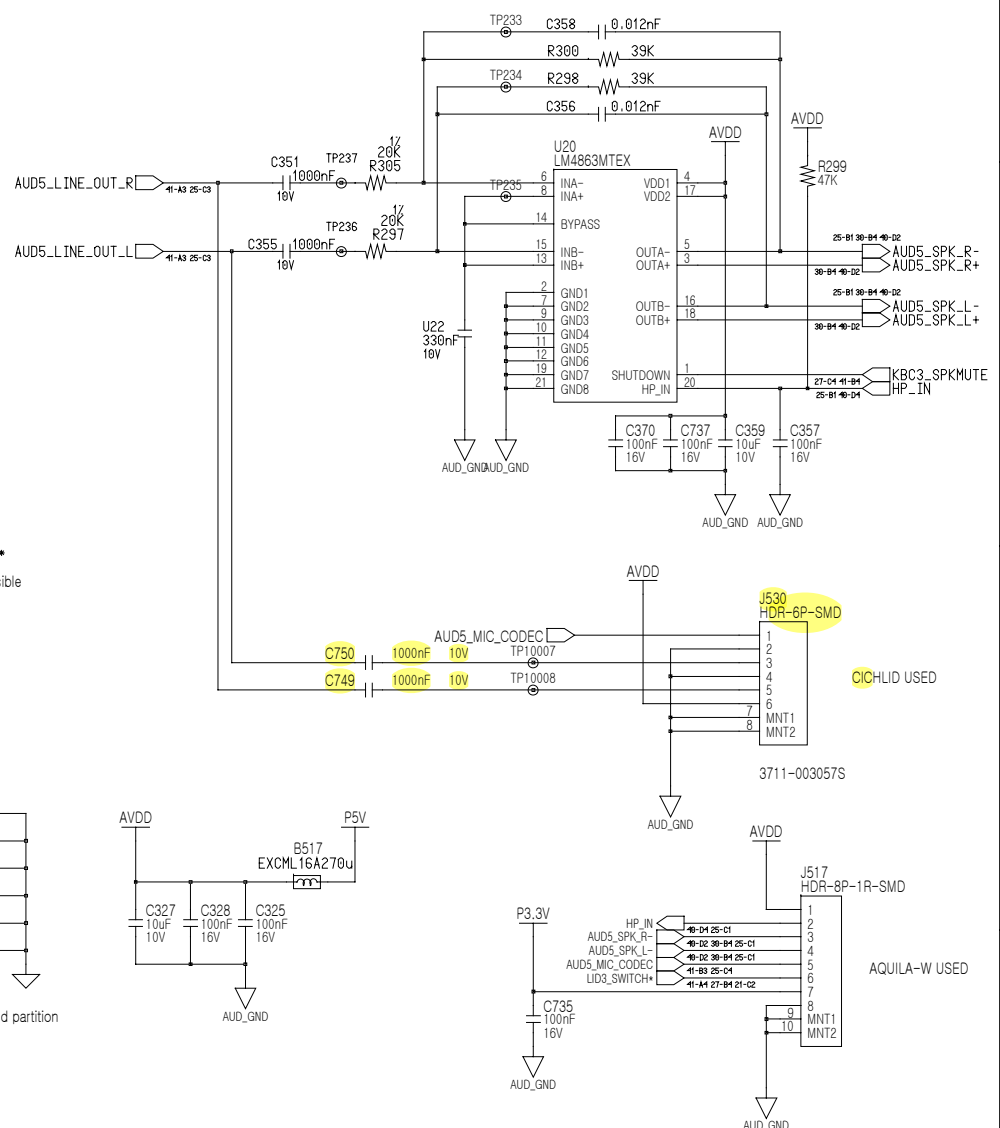
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AC97 Audio Codec

Place each caps near the pin of CS4299



Audio AMP

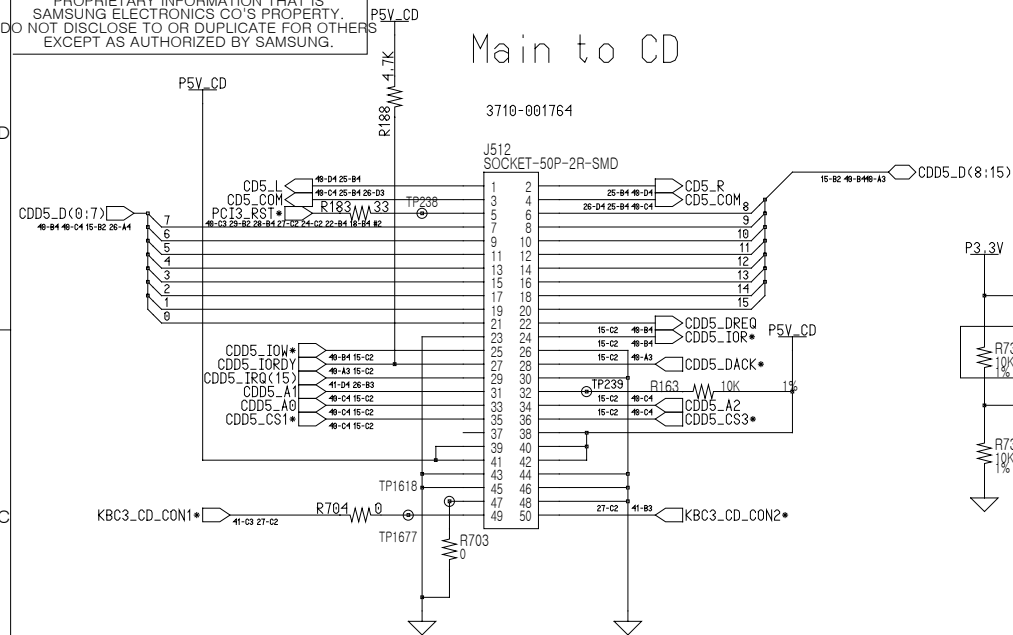


DRAW	KI. IM	DATE	4/7/2003	TITLE	AQUILA W MAIN	SAMSUNG ELECTRONICS PART NO. BA41-#####
CHECK	KK.BIN	DEV. STEP	DV	AUDIO CODEC & AMP		
APPROVAL	DW.KIM	REV	1.0	April 7, 2003 8:36:31 AM		
MODULE CODE		LAST EDIT		PAGE	25 OF 42	

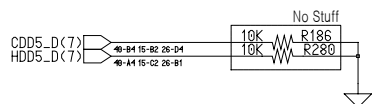
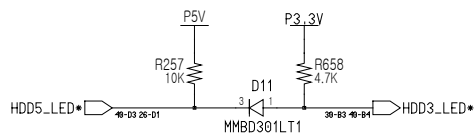
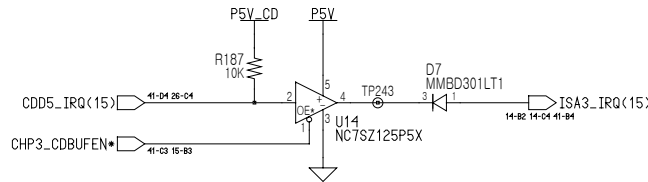
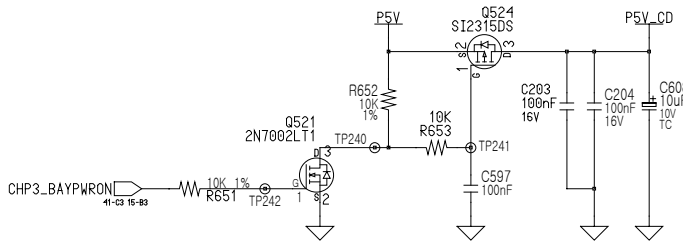
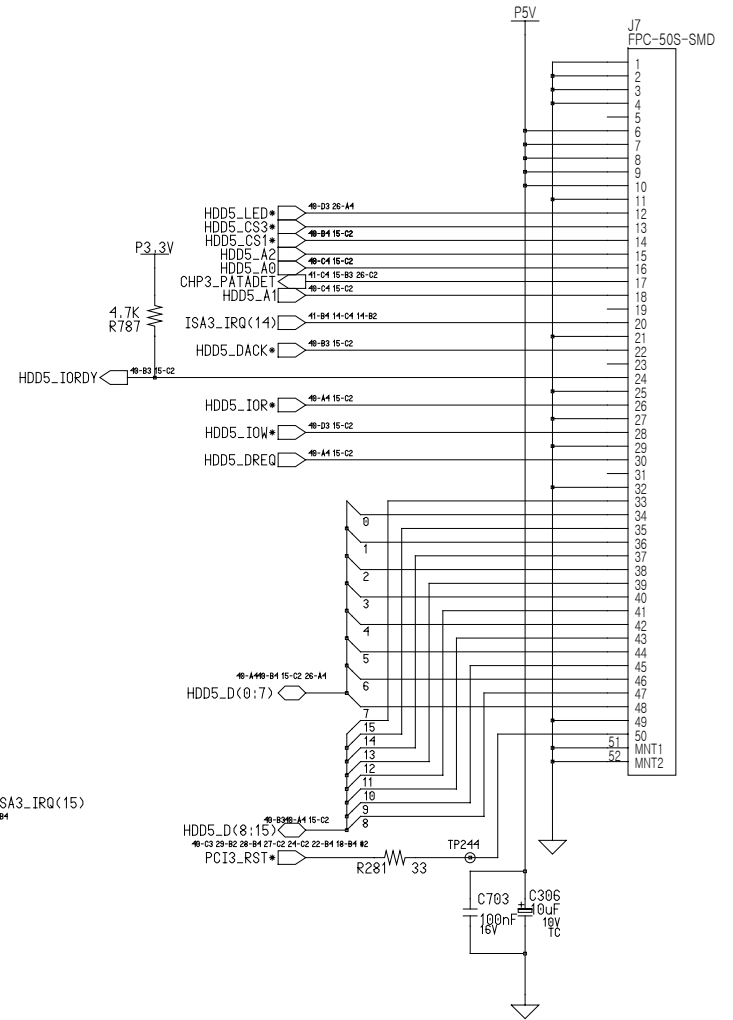
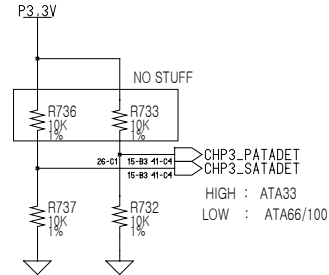
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Main to CD



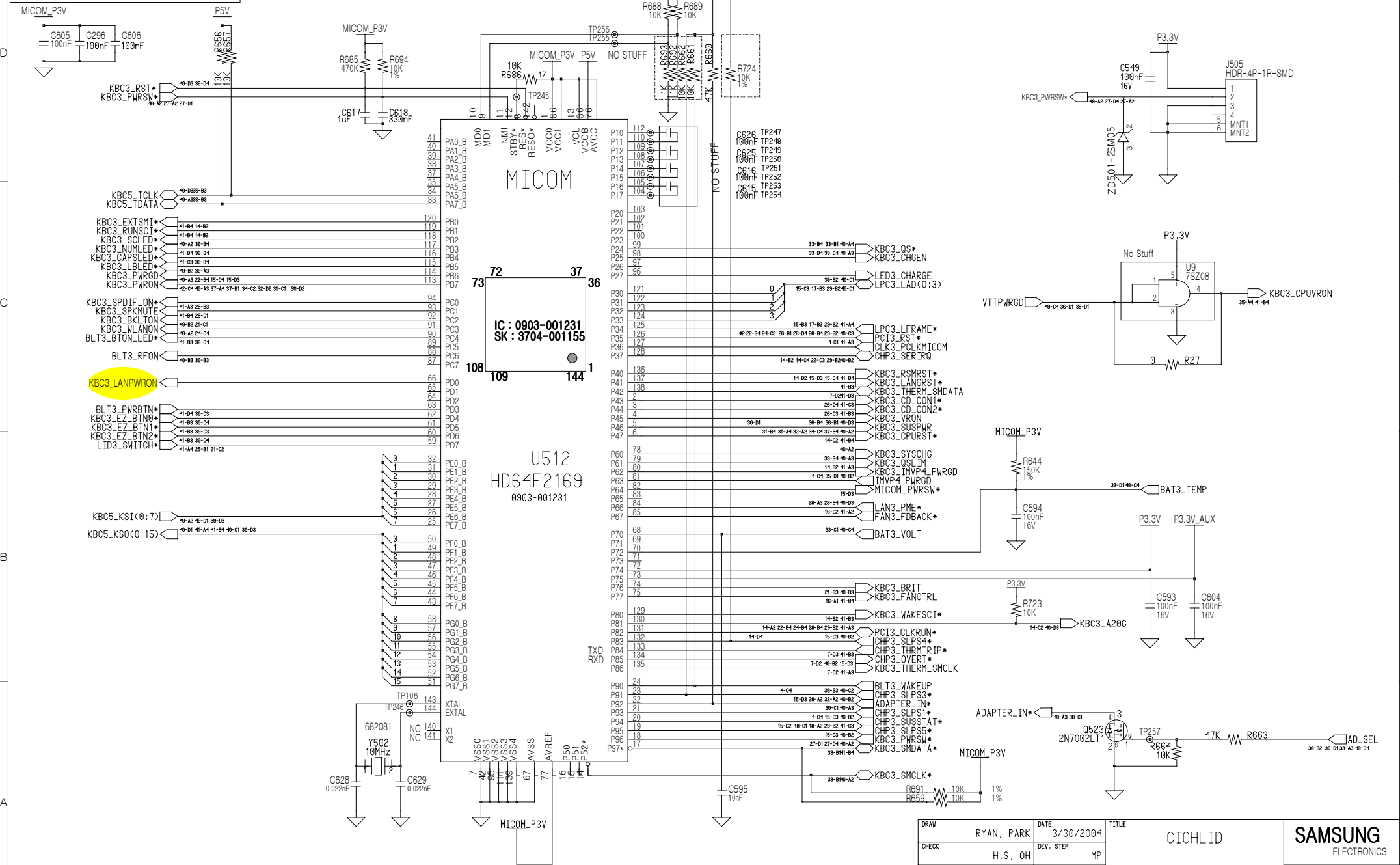
Main to HDD



DRAW	RYAN, PARK	DATE	3/30/2004	TITLE	CICHL ID	SAMSUNG ELECTRONICS
CHECK	H.S, OH	DEV. STEP	MP			
APPROVAL	H.S, KIM	REV	1.0		BAY CONNECTOR	PART NO. BA41-00392A
MODULE CODE		LAST EDIT		March, 30, 2004 10:53:09 AM	PAGE 26	OF 41

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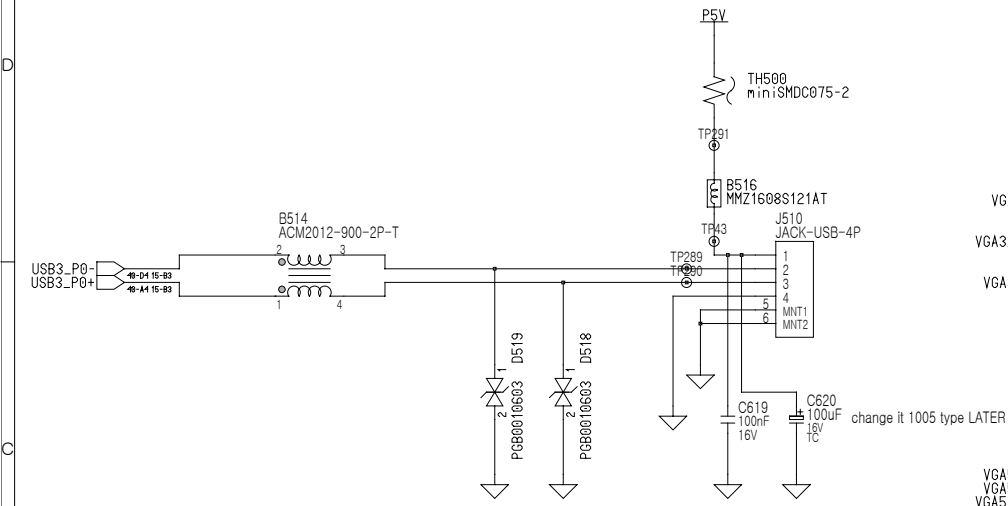
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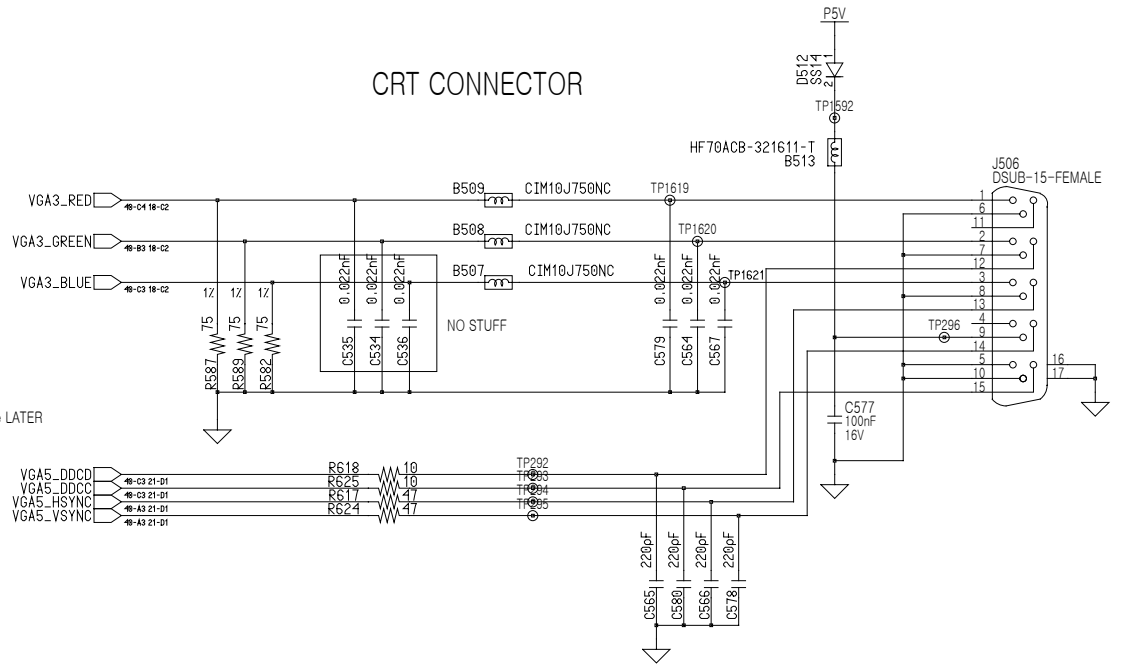
DRAW	RYAN, PARK	DATE	3/30/2004	TITLE	CICHL ID	SAMSUNG ELECTRONICS PART NO. BA41-00392A
CHECK	H.S, OH	DEV. STEP	MP			
APPROVAL	H.S, KIM	REV	1.0			
MODULE CODE		LAST EDIT				
				March, 30, 2004 10:53:25 AM	PAGE 27 OF 41	

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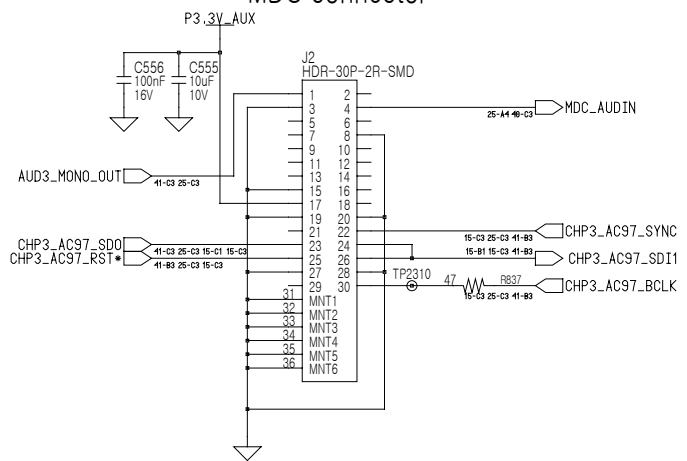
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CRT CONNECTOR

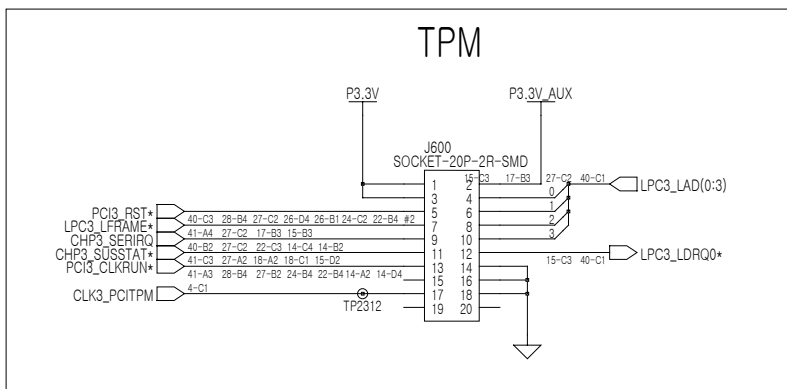


MDC connector



NO STUFF

TPM



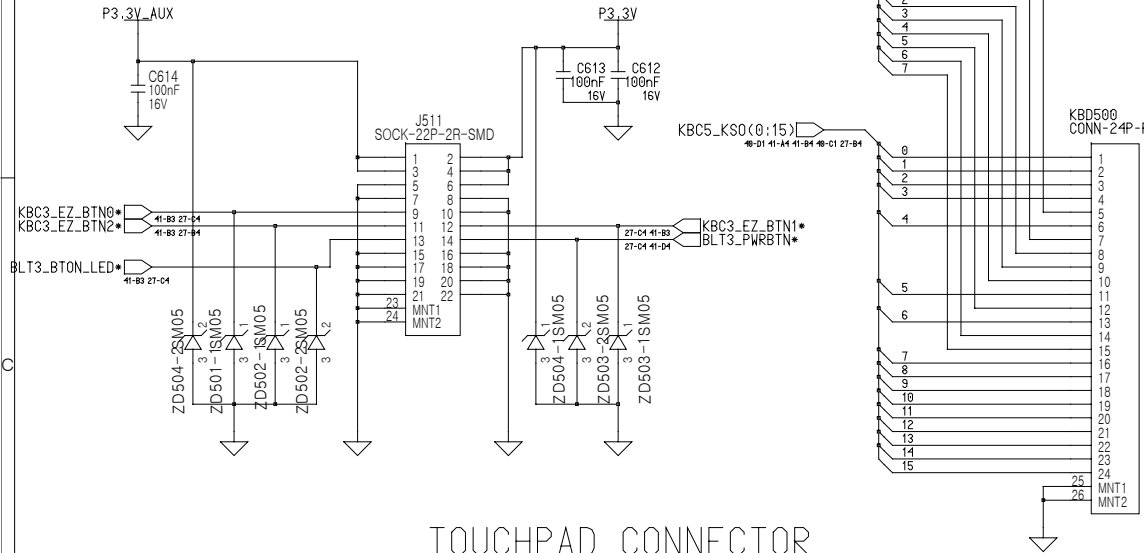
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CHECK	H.S, OH	DEV. STEP	MP	USB CONNECTOR		
APPROVAL	H.S, KIM	REV	1.0		PART NO.	BA41-00392A
MODULE CODE		LAST EDIT	March, 30, 2004 10:54:11 AM	PAGE	29	OF 41

SAMSUNG PROPRIETARY

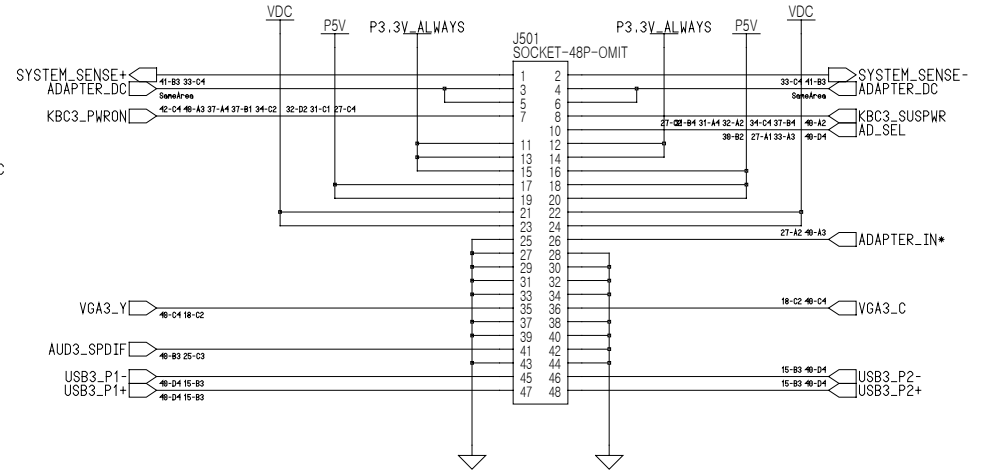
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KEYBOARD

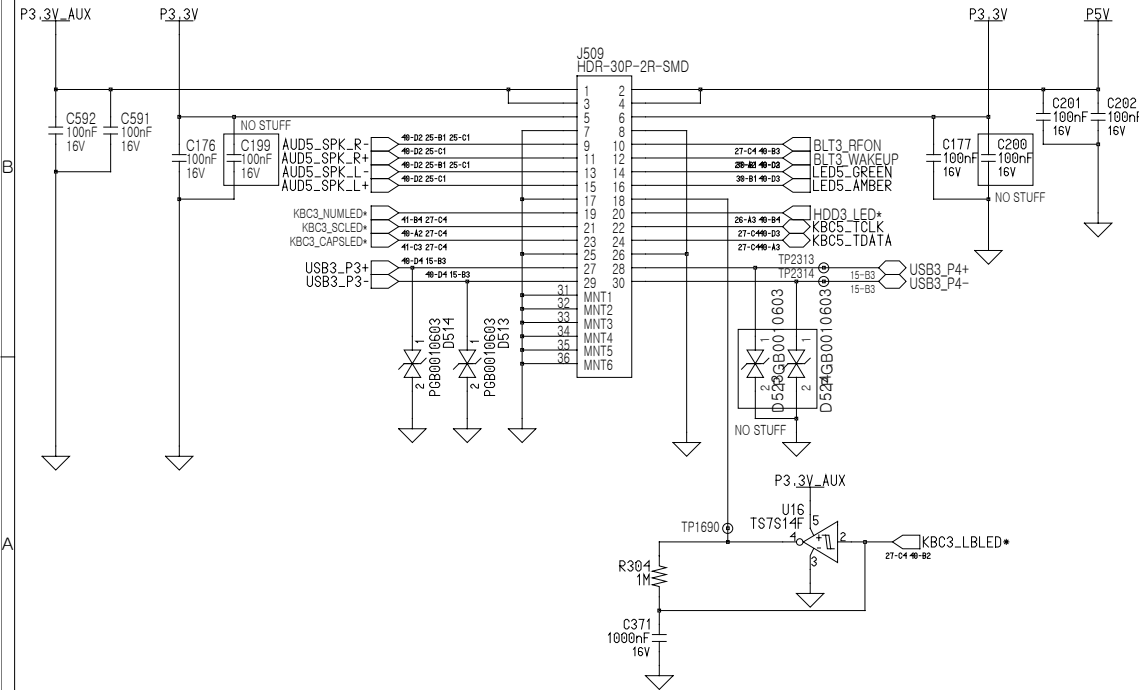
MAIN TO ON-TOP



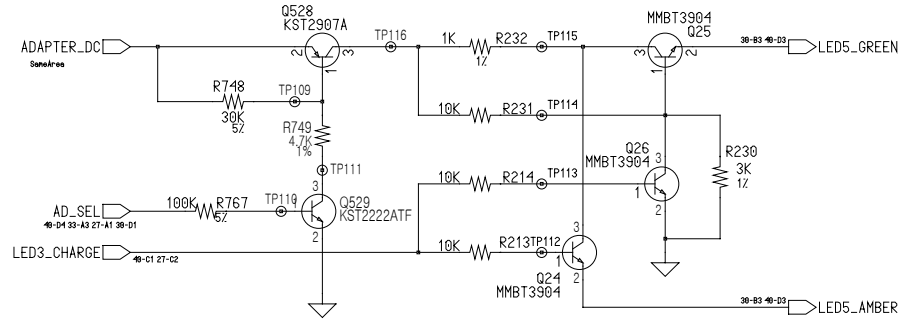
Main to DC/DC BOARD



TOUCHPAD CONNECTOR



ADAPTERIN/CHARGING LED

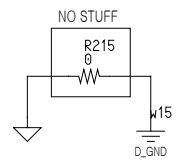
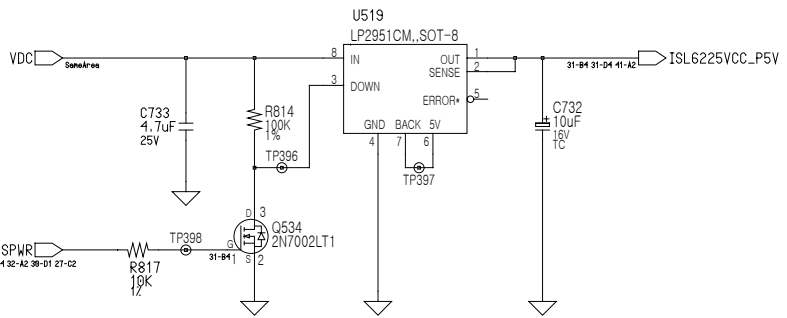
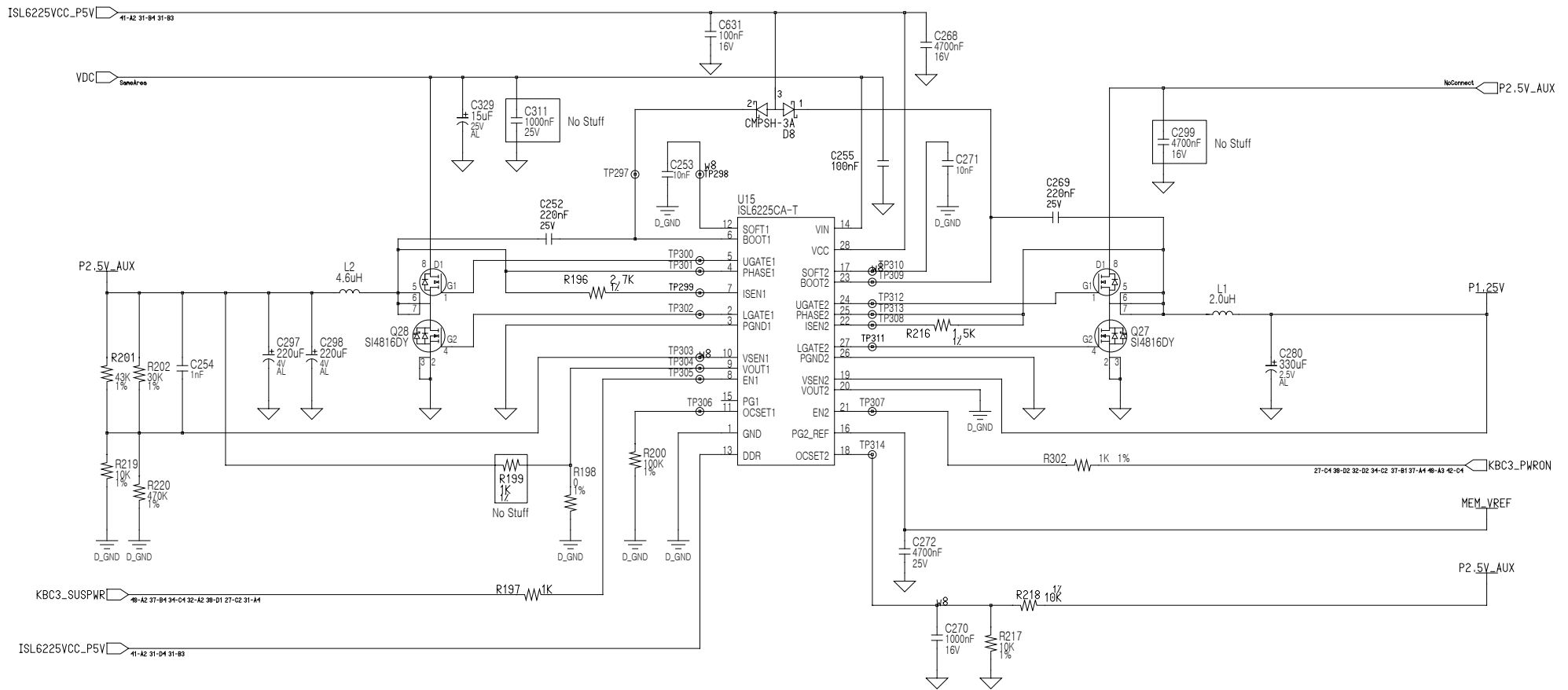


DRAW	RYAN, PARK	DATE	3/30/2004	TITLE	CICHLID	SAMSUNG ELECTRONICS
CHECK	H.S, OH	DEV. STEP	MP			
APPROVAL	H.S, KIM	REV	1.0	B'D TO B'D CONNECTOR		PART NO. BA41-00392A
MODULE CODE		LAST EDIT		March, 30, 2004 10:54:33 AM		PAGE 30 OF 41

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Main DDR Power

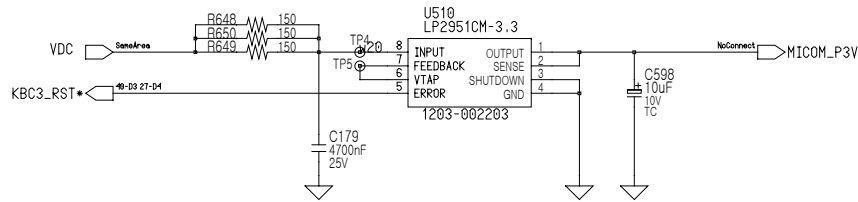


DRAW	RYAN, PARK	DATE	3/30/2004	TITLE	CICHLID	SAMSUNG ELECTRONICS
CHECK	H.S, OH	DEV. STEP	MP			
APPROVAL	H.S, KIM	REV	1.0	DDR & GRAPHIC POWER	PART NO.	BA41-00392A
MODULE CODE		LAST EDIT	March, 30, 2004 10:55:56 AM	PAGE	31	OF 41

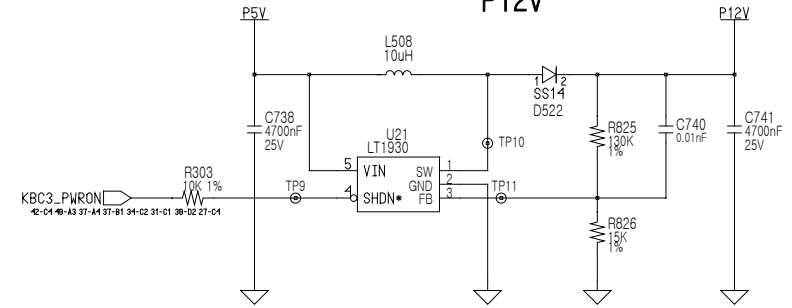
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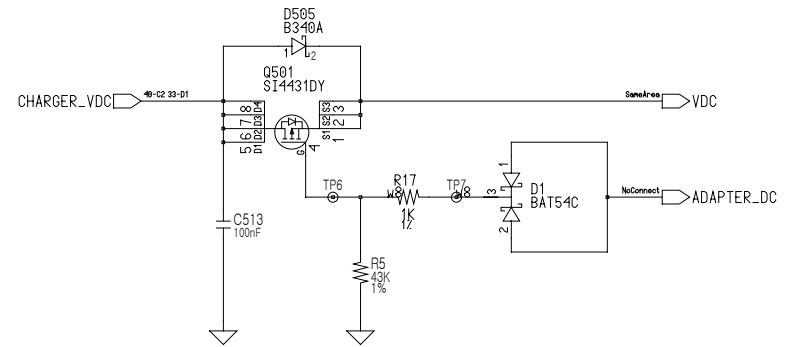
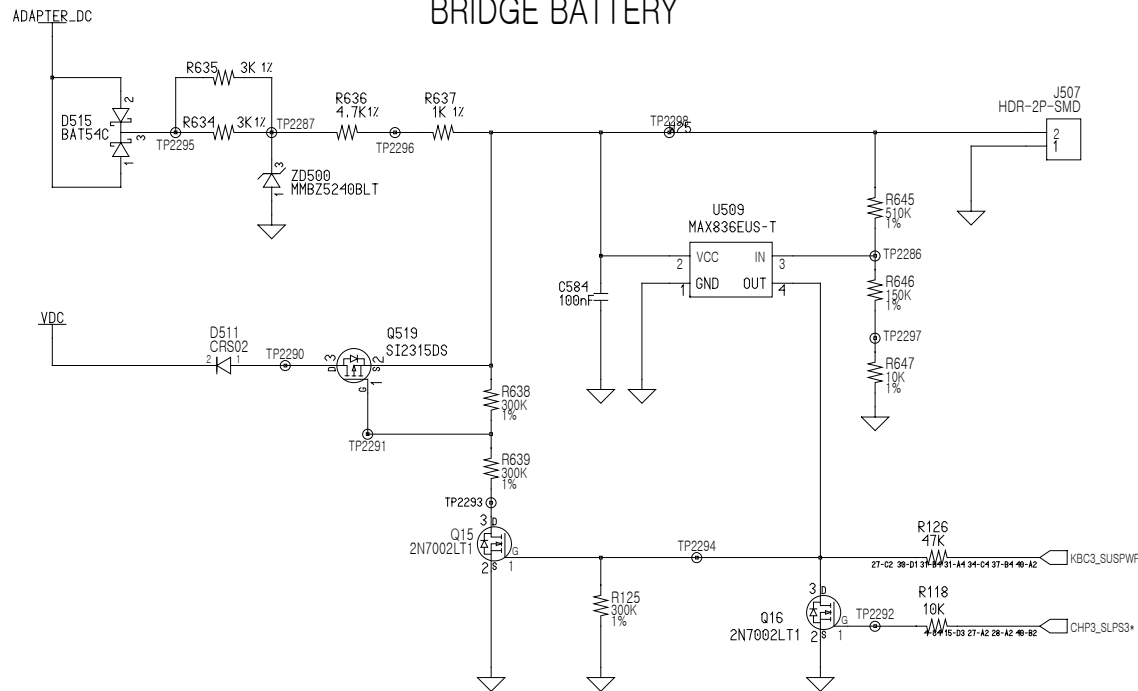
MICOM_P3V Power



P12V



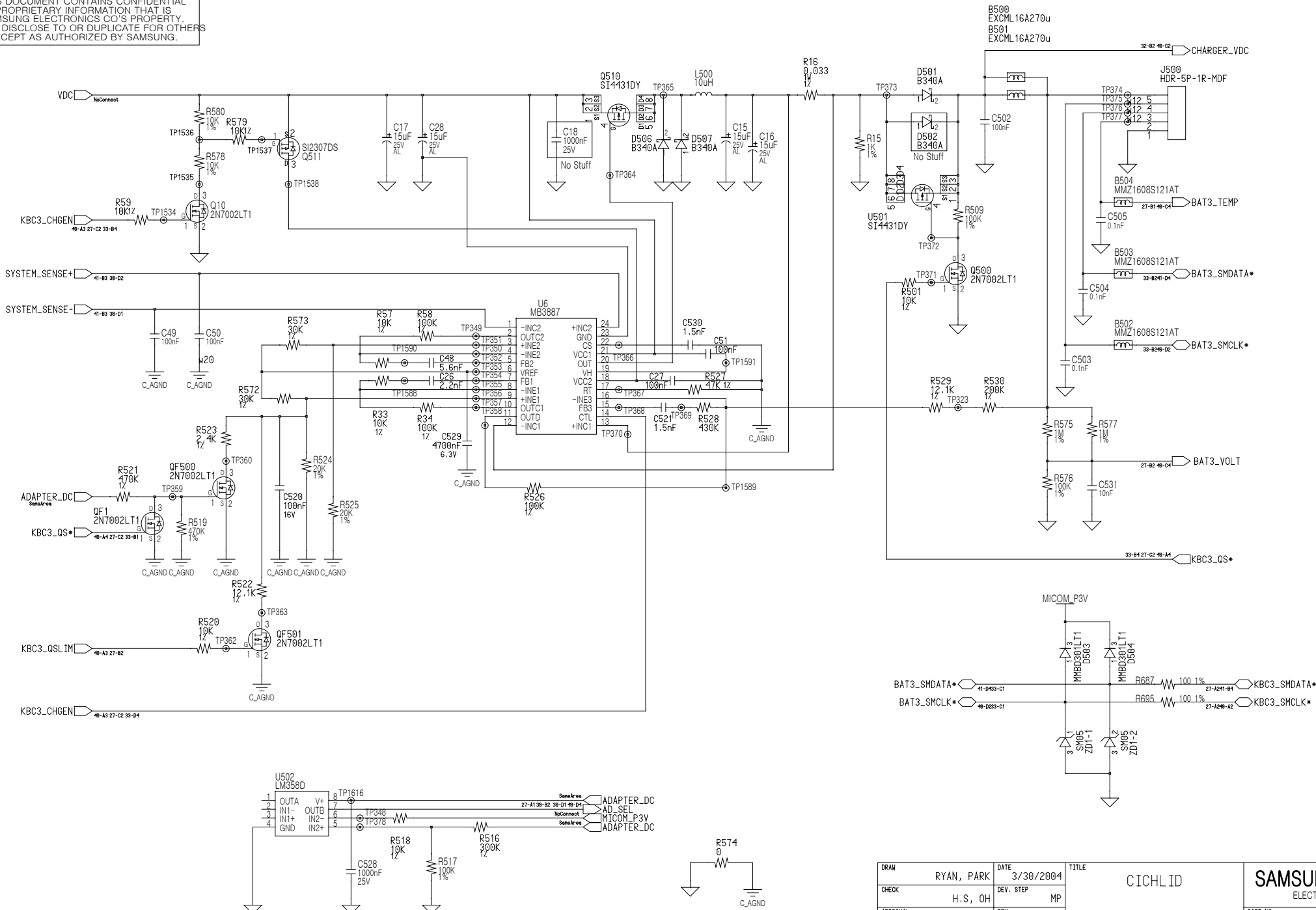
BRIDGE BATTERY



DRAW	RYAN, PARK	DATE	3/30/2004	TITLE	CICHLID	SAMSUNG ELECTRONICS
CHECK	H.S, OH	DEV. STEP	MP			
APPROVAL	H.S, KIM	REV	1.0	MICOM & P12V & BBVL POWER	PART NO.	BA41-00392A
MODULE CODE		LAST EDIT	March, 30, 2004 10:56:31 AM	PAGE	32	OF 41

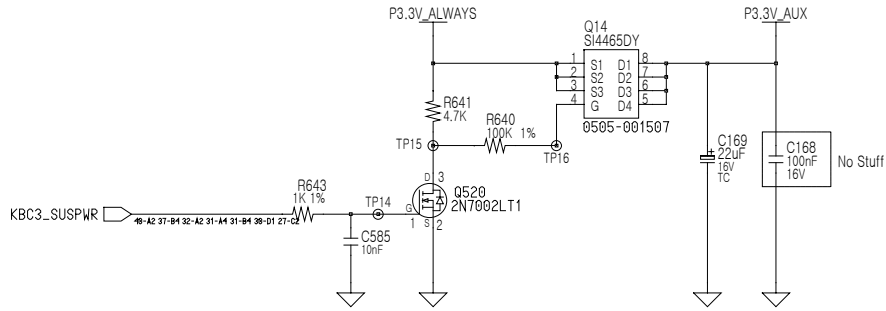
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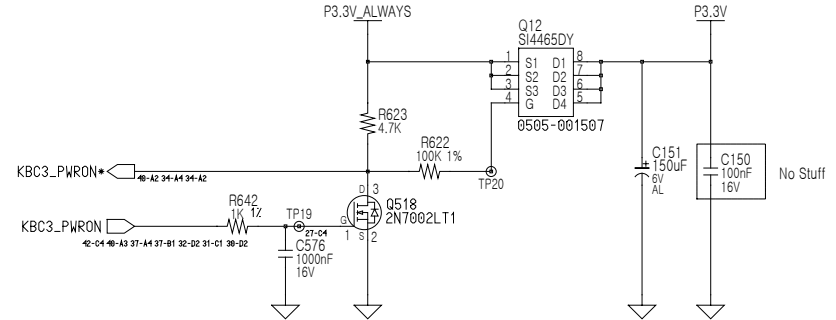


DRAW	RYAN, PARK	DATE	3/30/2004	TITLE	CICHL ID	SAMSUNG ELECTRONICS
CHECK	H.S, OH	DEV. STEP	MP			
APPROVAL	H.S, KIM	REV	1.0		CHARGER	PART NO. BA41-00392A
MODULE CODE		LAST EDIT	March, 30, 2004 10:56:47 AM		PAGE	33 OF 41

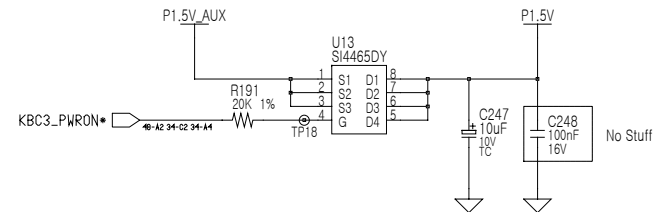
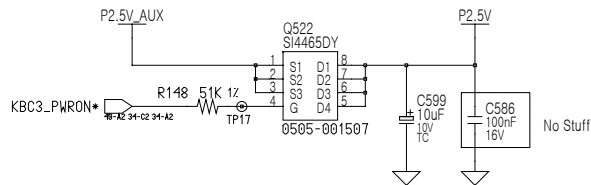
Switched Power On (P3.3V_AUX)



Switched Power On (P3.3V)



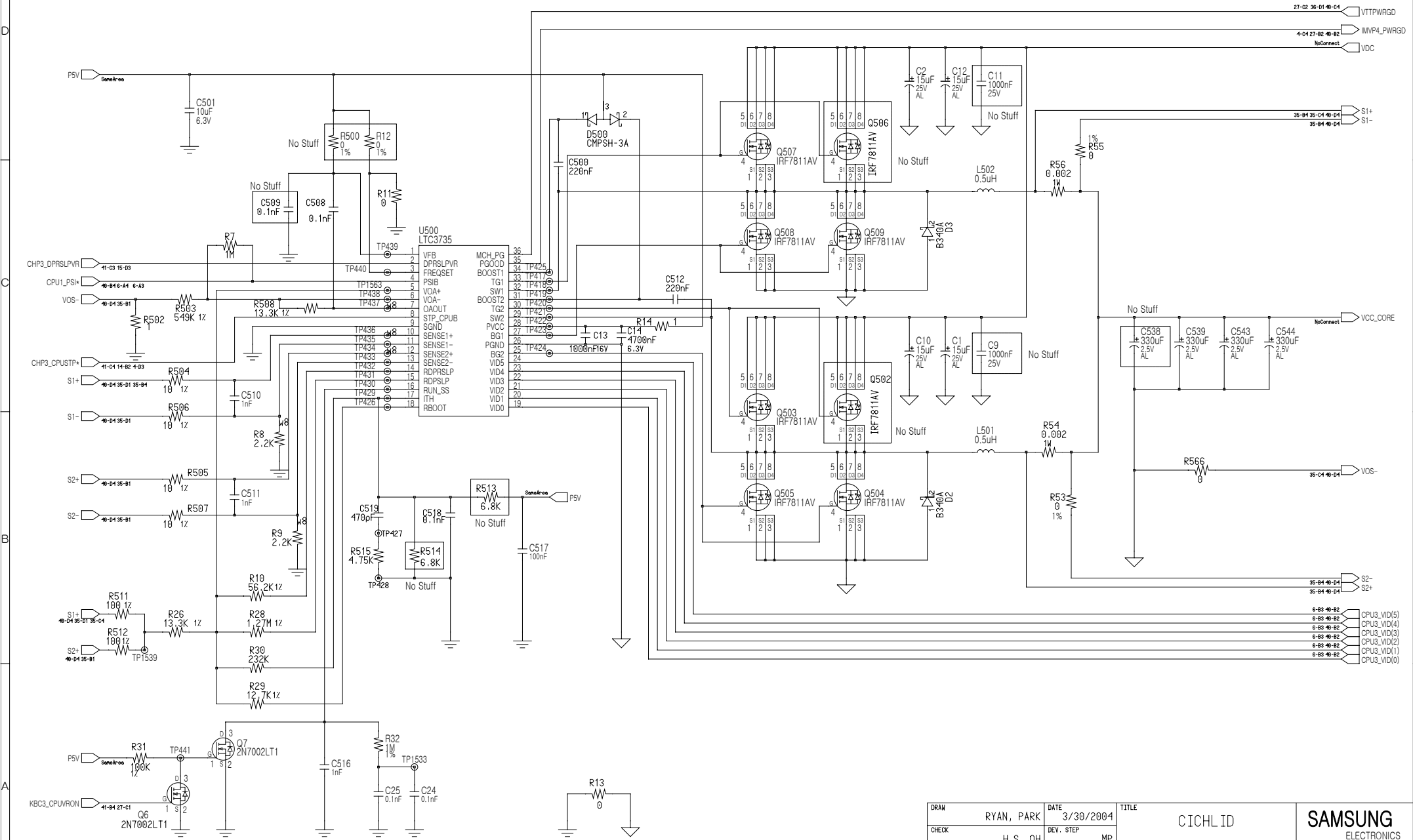
Switched Power On (P2.5V, P1.5V)



DRAW	RYAN, PARK	DATE	3/30/2004	TITLE	CICHLID	SAMSUNG ELECTRONICS
CHECK	H.S., OH	DEV. STEP	MP			
APPROVAL	H.S., KIM	REV	1.0	P3.3 & P2.5 & P1.5 POWER		PART NO.
MODULE CODE		LAST EDIT	March, 30, 2004 10:57:13 AM	PAGE	34	OF 41

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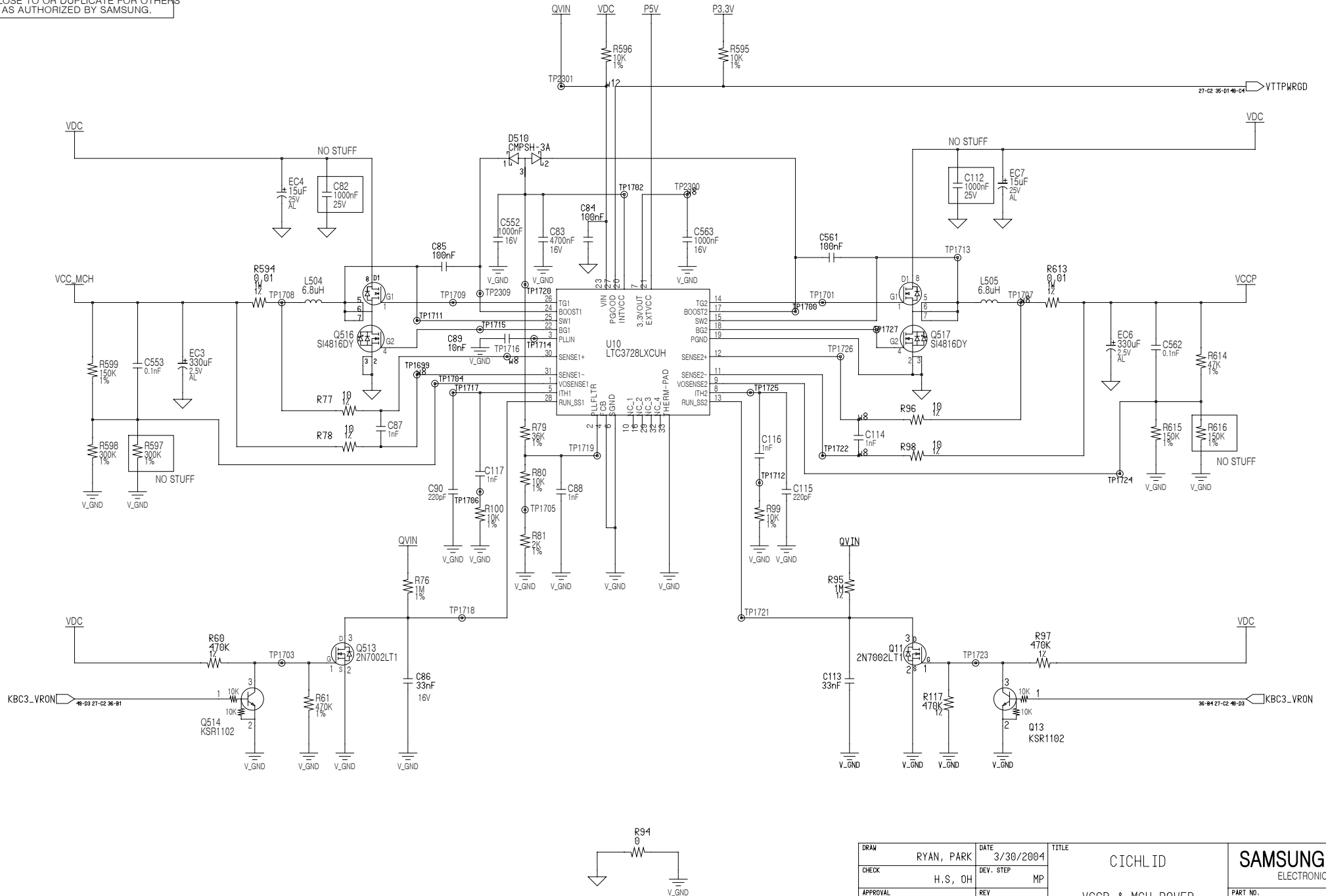
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DRAW	RYAN, PARK	DATE	3/30/2004	TITLE	CICHL ID	SAMSUNG ELECTRONICS
CHECK	H.S, OH	DEV. STEP	MP			
APPROVAL	H.S, KIM	REV	1.0		CPU POWER	PART NO. BA41-00392A
MODULE CODE		LAST EDIT		March, 30, 2004 10:57:28 AM	PAGE	35 OF 41

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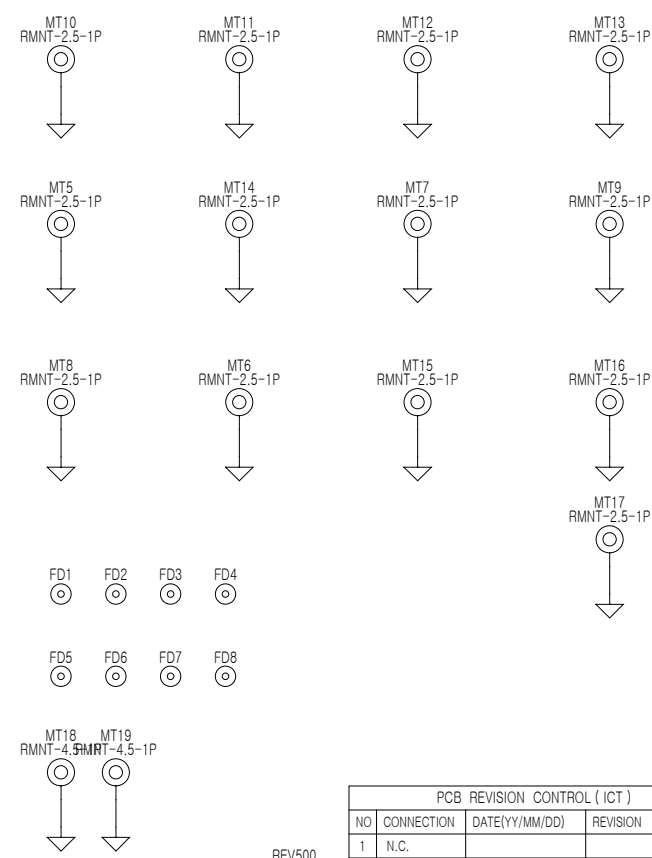
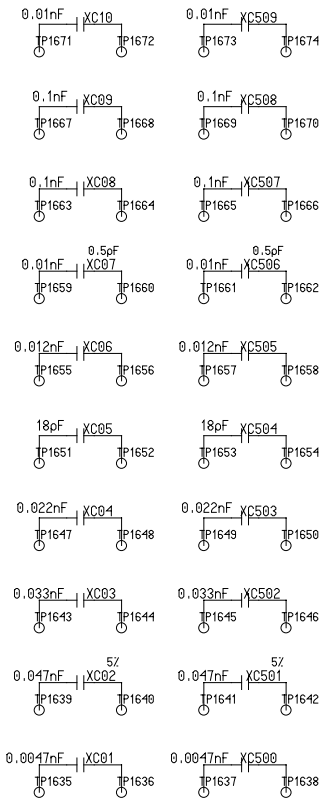
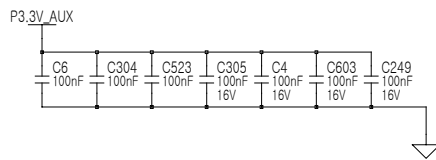
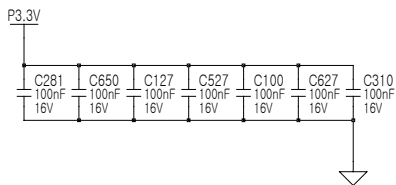
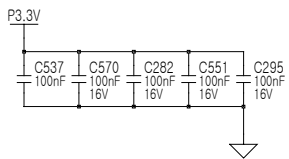
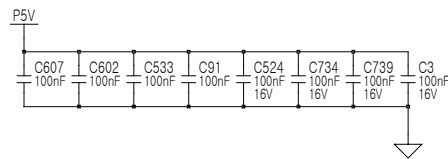
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DRAW	RYAN, PARK	DATE	3/30/2004	TITLE	CICHL ID	SAMSUNG ELECTRONICS
CHECK	H.S, OH	DEV. STEP	MP			
APPROVAL	H.S, KIM	REV	1.0		VCCP & MCH POWER	PART NO. BA41-00392A
MODULE CODE		LAST EDIT			March, 30, 2004 10:57:47 AM	PAGE 36 OF 41

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REV500
1
2

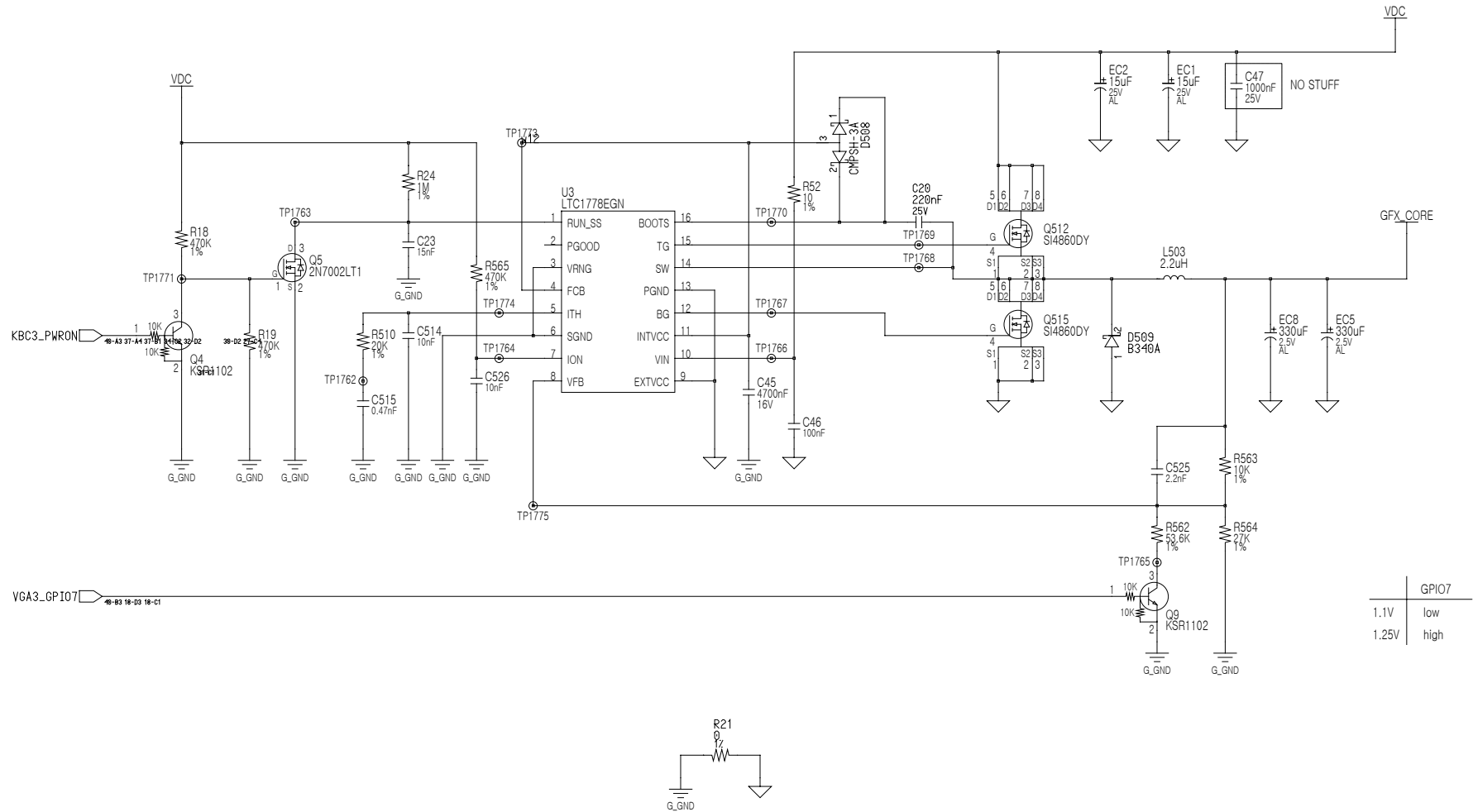
PCB REVISION CONTROL (ICT)				
NO	CONNECTION	DATE(Y/M/DD)	REVISION	STEP
1	N.C.			
2	1-2			
3	2-3			
4	3-1			
5	1-2-3			
6	N.C.			
7	1-2			
8	2-3			
9	3-1			
10	1-2-3			

DRAW	RYAN, PARK	DATE	3/30/2004	TITLE	CICHLID	SAMSUNG ELECTRONICS
CHECK	H.S, OH	DEV. STEP	MP			
APPROVAL	H.S, KIM	REV	1.0	MOUNT HOLE & REV.		PART NO.
MODULE CODE		LAST EDIT	March, 30, 2004 10:58:37 AM	PAGE	38	OF
					41	

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Graphic Core Power



GPIO7	
1.1V	low
1.25V	high

DRAW	RYAN, PARK	DATE	3/30/2004	TITLE	CICHLID	SAMSUNG ELECTRONICS
CHECK	H.S., OH	DEV. STEP	MP			
APPROVAL	H.S., KIM	REV	1.0		GRAPHIC POWER	PART NO. BA41-00392A
MODULE CODE		LAST EDIT		March, 30, 2004 11:43:13 AM	PAGE 39	OF 41

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 TP1468OEM2_SRASA*
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 TP1462OCHP3_BIOSWP*
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 TP1464OCHP3_CPUISTP*
 TP1465OCHP3_FF_DOUT
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 TP1479OCLK3_PCLKMIN
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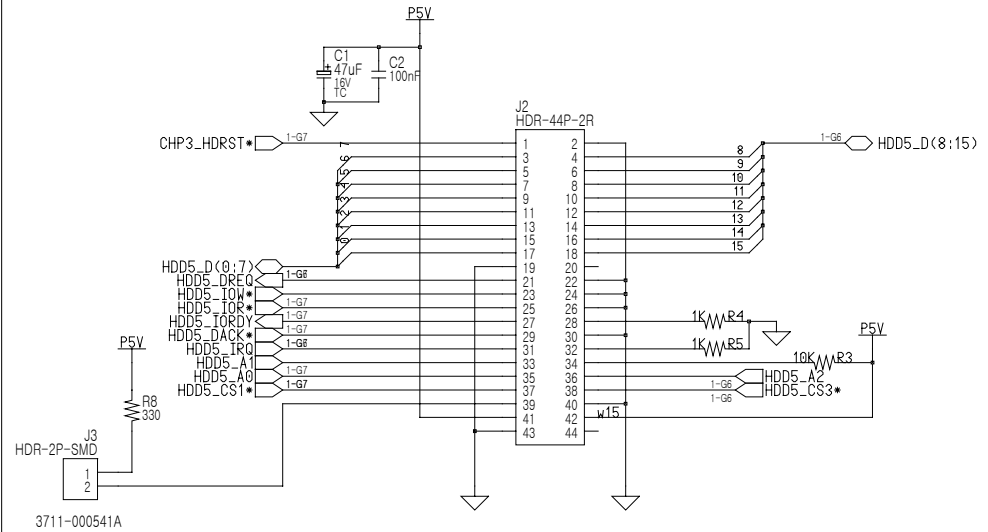
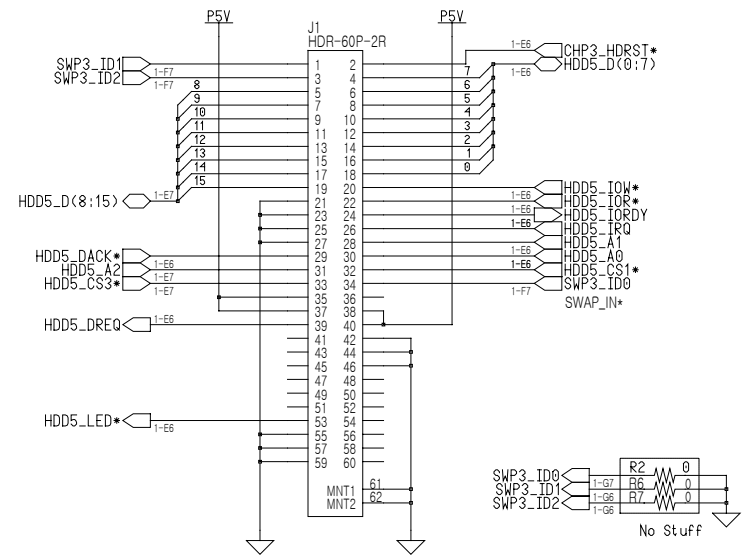
2ndHDD-I/F BOARD

CPU : BANIAS
 Chip Set : ODEM+
 Remarks : 2ndHDD

Model Name : CICHOLID
 PBA Name : 2nd HDD Interface
 A'ssy Code : BA59-01330A
 Dev. Step : MP
 Revision : 1.0
 T.R. Date : 2004. 1. 17

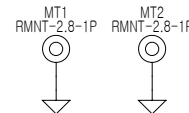
DRAW	CHECK	APPROVAL

Owner : Signature : X



SWAPBAY ID

Devices	SWAP_IN*
CD-ROM	0
2nd HDD	1 (No Connect)



DRAM	RYAN, PARK	DATE	12/11/2003	TITLE	CICHLID	SAMSUNG
CHECK	OH, H.S	DEV. STEP	DV	2ND HDD I/F B'D		ELECTRONICS
APPROVAL	LEE, KEVIN	REV	1.0	2ND HDD I/F B'D		PART NO. BA41-XXXXXX
MODULE CODE	LAST EDIT		December, 11, 2003 5:35:29 PM		PAGE	1 OF 1

CICHLID

CPU : BANIAS/DOTHAN
 Chip Set : ODEM+
 Remarks :

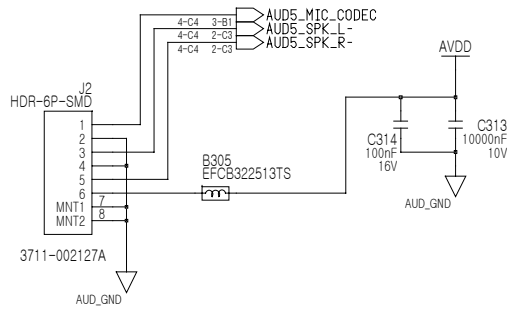
Model Name : AUDIO Board
 PBA Name :
 PCB Code : BA59-01332A
 Dev. Step : MP
 Revision : 1.3
 T.R. Date : 05/07/2004

DRAW	CHECK	APPROVAL

DRAW	PARK, RYAN	DATE	3/22/2004	TITLE	CICHLID AUDIO BOARD	SAMSUNG ELECTRONICS <small>PART NO.</small> BA59-01332A
CHECK	OH, H.S	DEV. STEP	MP			
APPROVAL	LEE, KEVIN	REV	1.1			
MODULE CODE		LAST EDIT	March 22, 2004 7:52:12 PM	PAGE	1	OF 4

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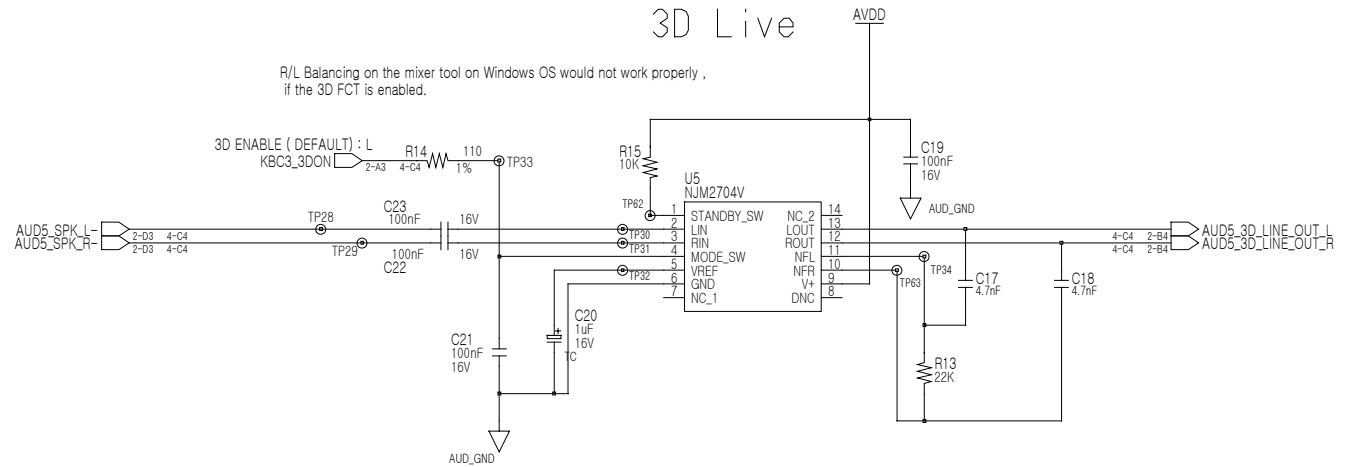
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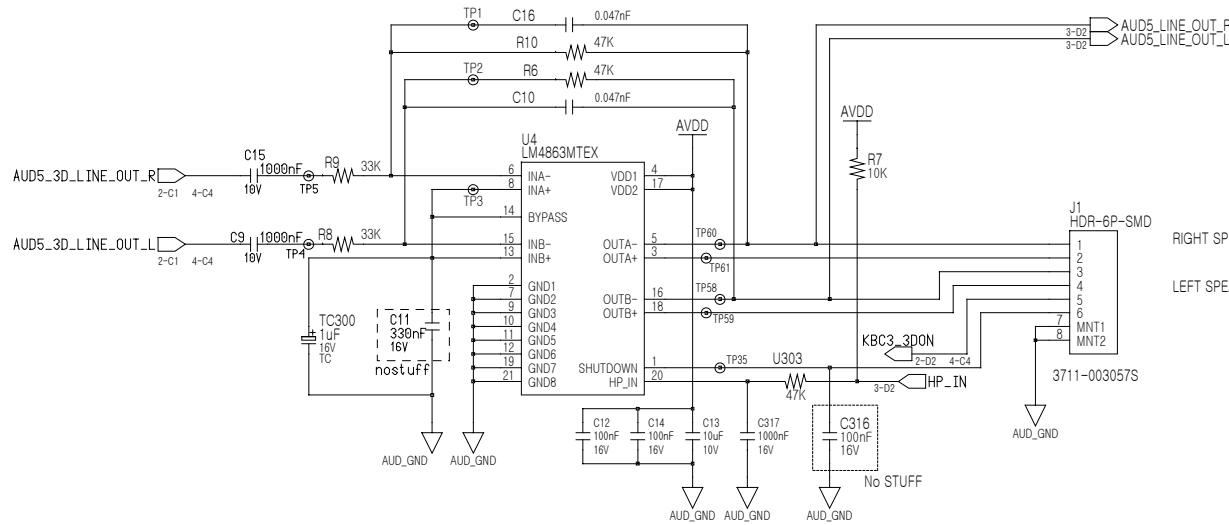
The Ground 'Line between MIC_CODEC and SPK_L-' of the 'Audio BD to Main BD Cable' must be shielded.

3D Live

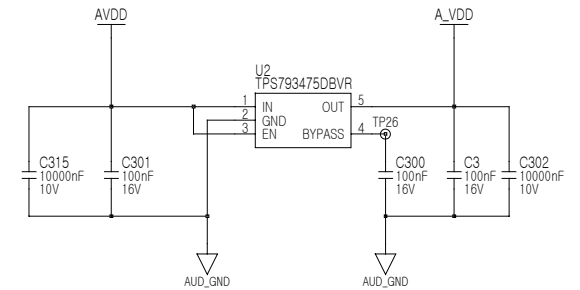
R/L Balancing on the mixer tool on Windows OS would not work properly, if the 3D FCT is enabled.



Audio AMP



Enough Thermal Ground Area Should be Guaranteed for spreading intense heat of LM4863.



RIGHT SPEAKER
LEFT SPEAKER

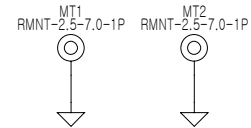
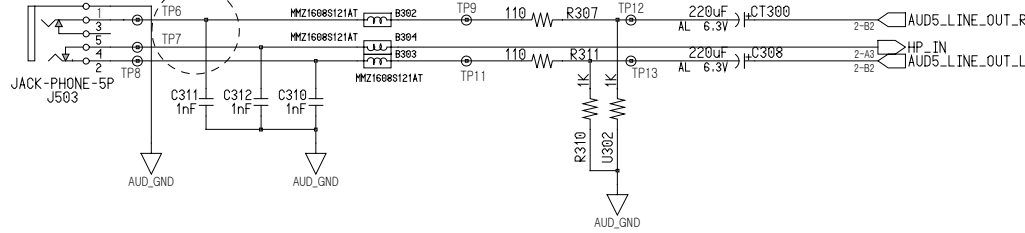
DRAW	PARK, RYAN	DATE	3/22/2004	TITLE	CICHLID AUDIO BOARD UNDEFINED	SAMSUNG ELECTRONICS PART NO. BA59-01332A
CHECK	OH, H.S	DEV. STEP	MP			
APPROVAL	LEE, KEVIN	REV	1.1			
MODULE CODE		LAST EDIT	March 22, 2004 7:52:12 PM	PAGE 2 OF		

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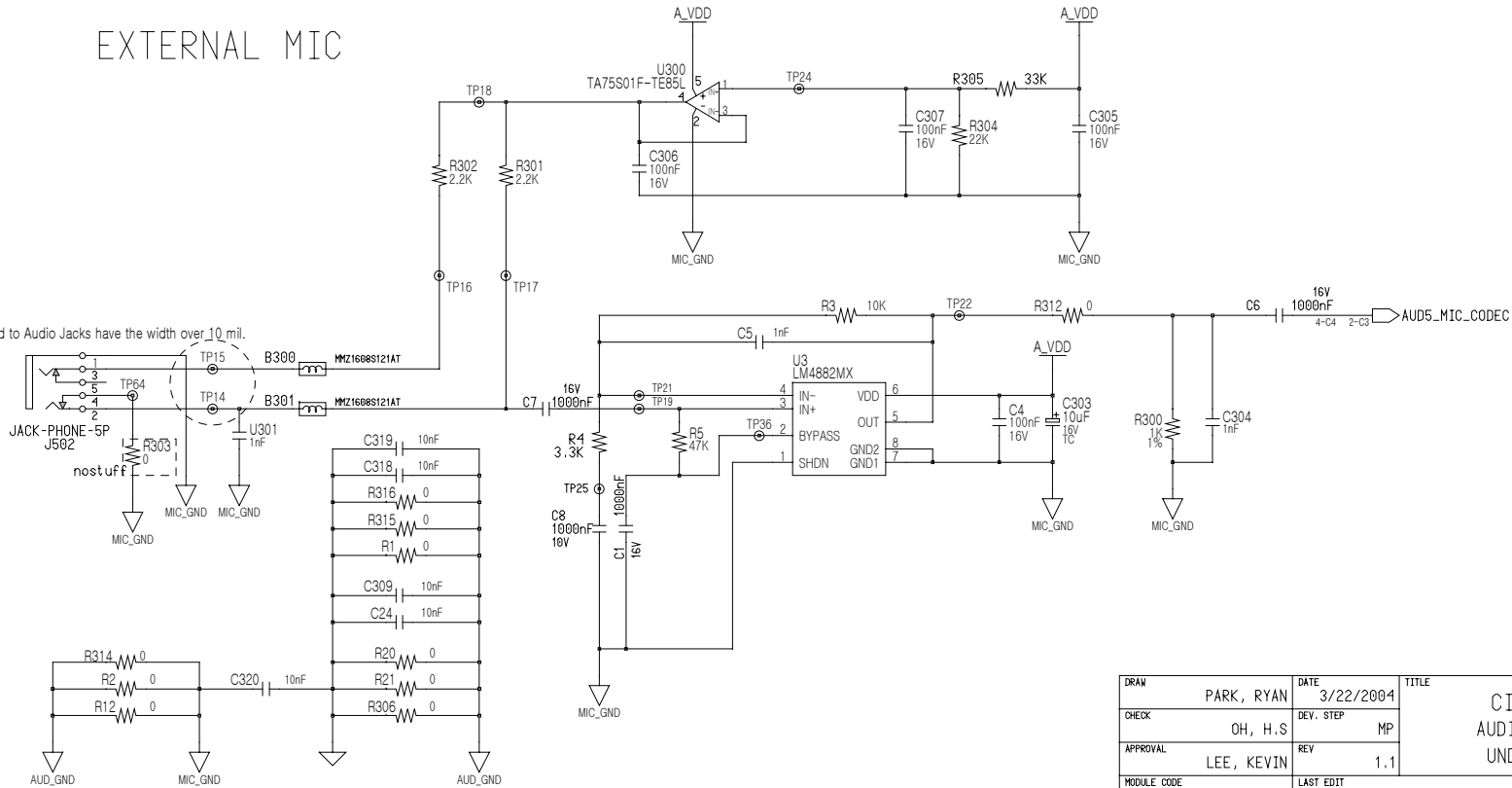
HEADPHONE

Make sure that the traces led to Audio Jacks have the width over 10 mil.



EXTERNAL MIC

Make sure that the traces led to Audio Jacks have the width over 10 mil.



DRAW	PARK, RYAN	DATE	3/22/2004	TITLE	CICHLID AUDIO BOARD UNDEFINED SAMSUNG ELECTRONICS PART NO. BA59-01332A
CHECK	OH, H.S	DEV. STEP	MP		
APPROVAL	LEE, KEVIN	REV	1.1		
MODULE CODE		LAST EDIT			
				March 22, 2004 7:52:12 PM	PAGE 3 OF 4

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TP37OKBC3_3D0N
 TP38OAU5_SPK_L-
 TP39OAU5_SPK_R-
 TP40OAU5_MIC.CODEC

TP41OAU5_3D_LINE_OUT_L
 TP42OAU5_3D_LINE_OUT_R

TP55OAVDD
 TP54OA_VDD

TP43OAU_GND

TP51OMIC_GND

DRAW	PARK, RYAN	DATE	3/22/2004	TITLE	CICHLID AUDIO BOARD UNDEFINED	SAMSUNG ELECTRONICS
CHECK	OH, H.S	DEV. STEP	MP			
APPROVAL	LEE, KEVIN	REV	1.1			
MODULE CODE		LAST EDIT	March 22, 2004 7:52:12 PM	PAGE	4	OF 4
					PART NO.	BA59-01332A

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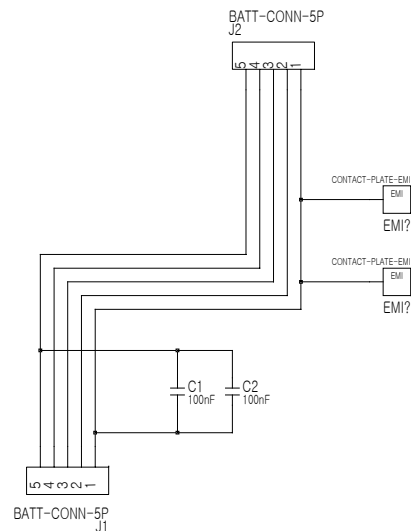
CICHLID

CPU : BANIAS / DOTHAN
 Chip Set : ODEM+
 Remarks :

Model Name : BATTERY BR. BOARD
 PBA Name :
 PCB Code : BA59-01331A
 Dev. Step : MP
 Revision : 1.2
 T.R. Date : 2004.04.01

DRAW	CHECK	APPROVAL

To BATTERY



To MAIN

NET LIST NAME

- #1 GND
- #2 BAT3_TEMP
- #3 BAT3_SMDATA*
- #4 BAT3_SMCLK*
- #5 VDC

DRAW	PARK, RYAN	DATE	12/5/2003	TITLE	CICHLID BATTERY BRIDGE BOARD	SAMSUNG ELECTRONICS
CHECK	OH, H.S	DEV. STEP	DV			
APPROVAL	LEE, KEVIN	REV	1.0			PART NO. BA41-
MODULE CODE		LAST EDIT		December, 5, 2003 6:00:28 PM	PAGE	1 OF 1

4
3
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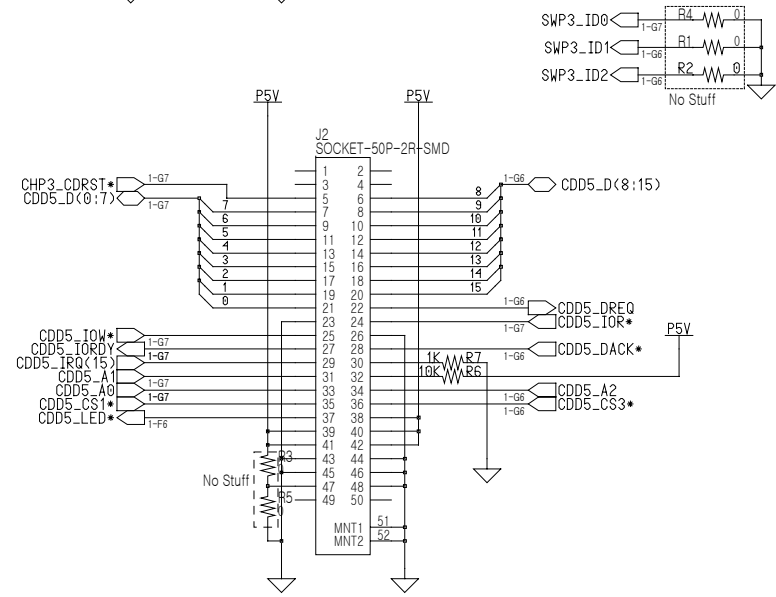
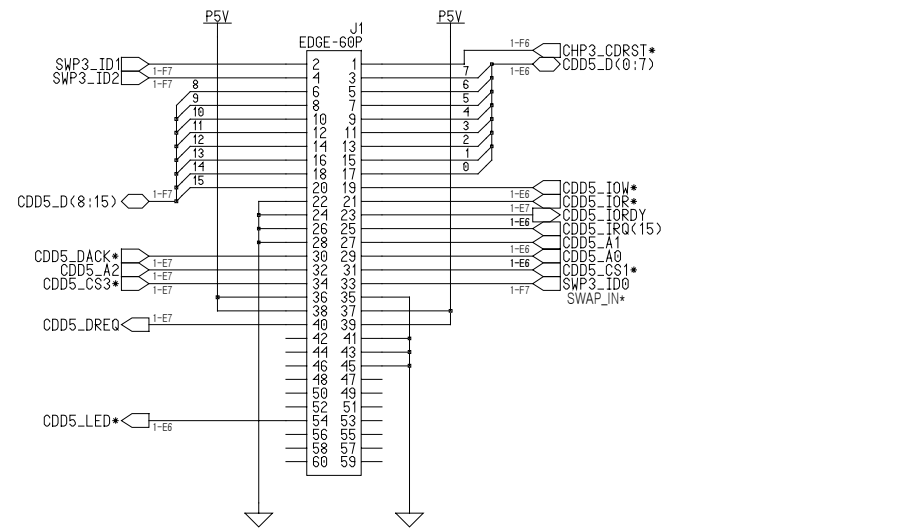
CD-I/F BOARD

CPU : BANIAS/DOTHAN
Chip Set : ODEM+
Remarks : CD/COMBO/DVD-MULTI

Model Name : CICHOLID
PBA Name : CD Interface
A'ssy Code : BA59-01333A
Dev. Step : MP
Revision : 1.1
T.R. Date : 2004.05.06

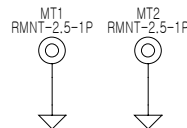
DRAW	CHECK	APPROVAL

Owner : Signature : X



SWAPBAY ID

Devices	SWAP_IN*
CD-ROM	0
2nd HDD	1



DRAW	PARK, RYAN	DATE	12/4/2003	TITLE	CICHOLID CD I/F B'D	SAMSUNG ELECTRONICS
CHECK	OH, H.S	DEV. STEP	DV	CD I/F B'D	PART NO.	
APPROVAL	LEE, KEVIN	REV	1.0		BA41-XXXXXX	
MODULE CODE		LAST EDIT		December, 4, 2003 2:55:12 PM	PAGE	1 OF 1

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ONTOP BOARD

CPU : BANIAS/DOTHAN
Chip Set : ODEM+
Remarks : EASY BUTTON BOARD

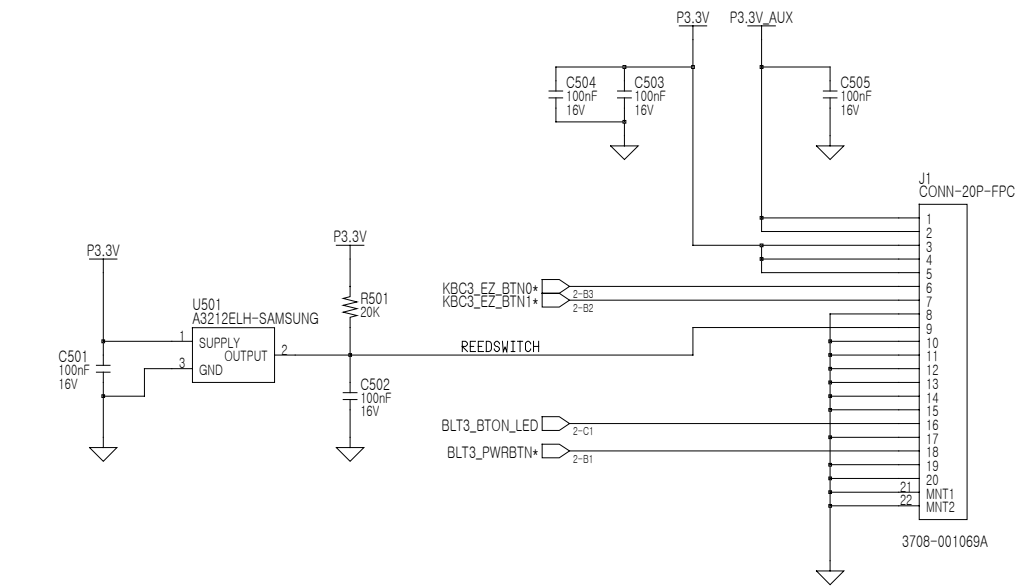
Model Name : ONTOP BOARD
PBA Name :
PCB Code : BA59-01334A
Dev. Step : MP
Revision : 1.0
T.R. Date : 2004.01.28

DRAW	CHECK	APPROVAL

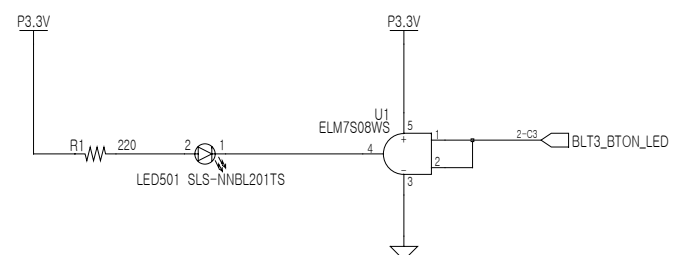
DRAW	PARK, RYAN	DATE	12/3/2003	TITLE	CICHL ID ONTOP BOARD	SAMSUNG ELECTRONICS
CHECK	OH, H.S	DEV. STEP	DV			
APPROVAL	LEE, KEVIN	REV	1.0	PART NO. BA41-		
MODULE CODE	LAST EDIT			January, 28, 2004 2:12:38 PM	PAGE	1 OF 2

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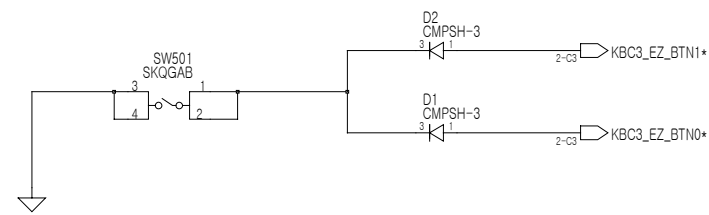
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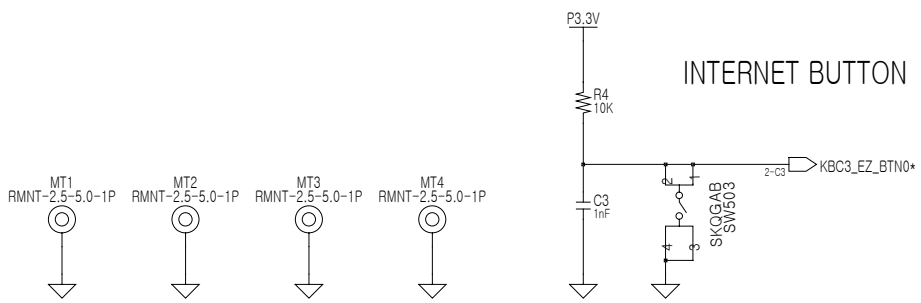
BLUETOOTH BUTTON LED



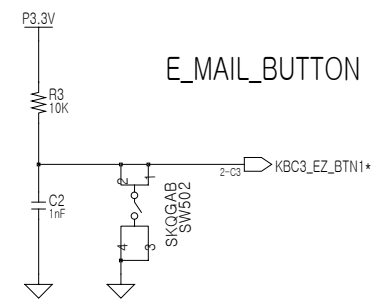
USER BUTTON



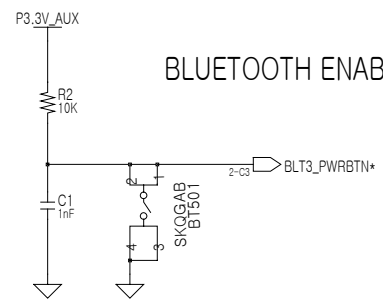
INTERNET BUTTON



E_MAIL_BUTTON



BLUETOOTH ENABLE BUTTON



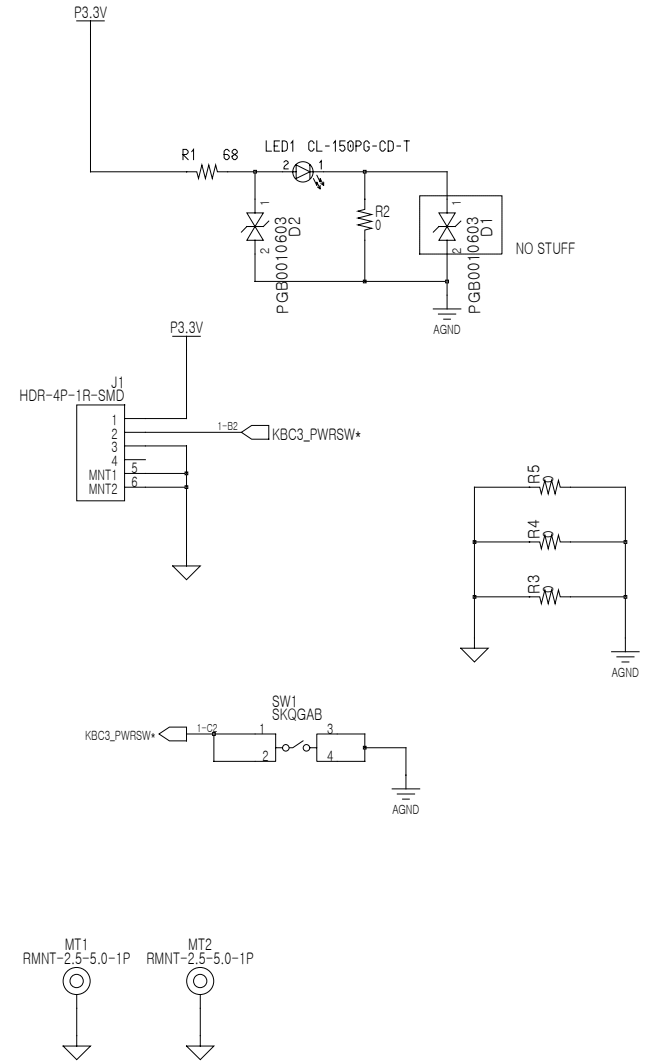
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CHECK	OH, H.S	DEV. STEP	DV			
APPROVAL	LEE, KEVIN	REV	1.0			
MODULE CODE		LAST EDIT	December, 3, 2003 2:13:08 PM	PAGE	2 OF 2	

POWER SW BOARD

CPU : BANIAS/DOTHAN
 Chip Set : ODEM+
 Remarks :

Model Name : Power SW Board
 PBA Name :
 PCB Code : BA59-01336A
 Dev. Step : MP
 Revision : 1.0
 T.R. Date : 2004.01.28

DRAW	CHECK	APPROVAL



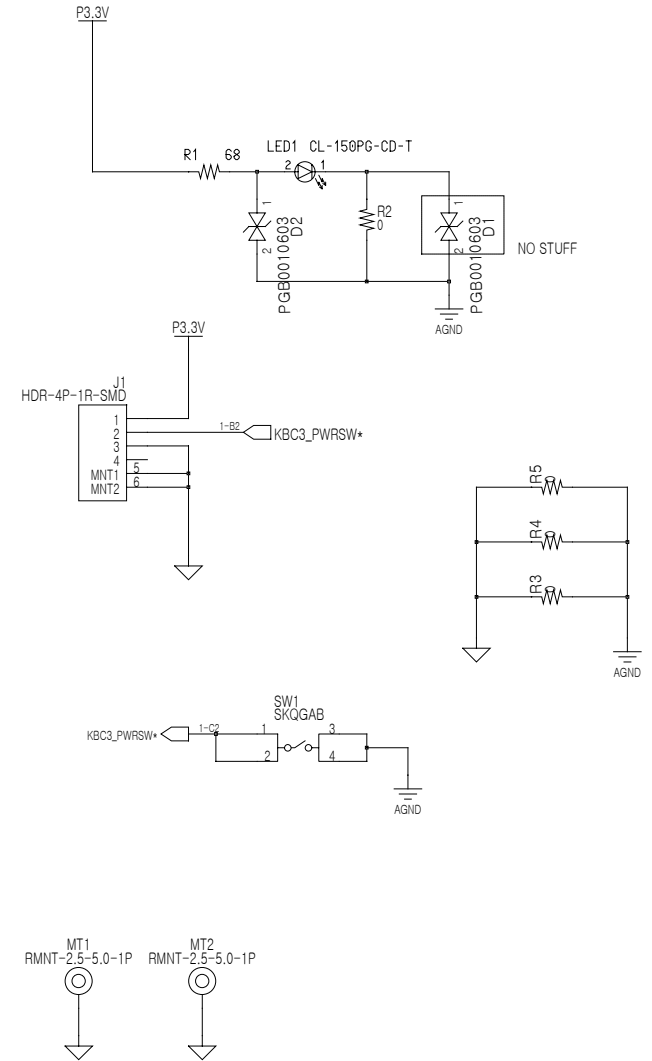
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CHECK	OH, H.S	DEV. STEP	DV			
APPROVAL	LEE, KEVIN	REV	1.0			PART NO. BA41-undef ined
MODULE CODE		LAST EDIT	December, 4, 2003 11:57:34 AM	PAGE	1	OF 1

POWER SW BOARD

CPU : BANIAS/DOTHAN
 Chip Set : ODEM+
 Remarks :

Model Name : Power SW Board
 PBA Name :
 PCB Code : BA59-01336A
 Dev. Step : MP
 Revision : 1.0
 T.R. Date : 2004.01.28

DRAW	CHECK	APPROVAL



DRAW	PARK, RYAN	DATE	12/4/2003	TITLE	CICHL ID POWER BOARD POWER BOARD	SAMSUNG ELECTRONICS PART NO. BA41-undef ined
CHECK	OH, H.S	DEV. STEP	DV			
APPROVAL	LEE, KEVIN	REV	1.0			
MODULE CODE		LAST EDIT	December, 4, 2003 11:57:34 AM	PAGE	1 OF	1

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SWAPBAY BR. BOARD

CPU : BANIAS/DOTHAN

Chip Set : ODEM+

Remarks :

Model Name : SWAPBAY BR. BOARD

PBA Name :

PCB Code : BA59-01335A

Dev. Step : MP

Revision : 1.2

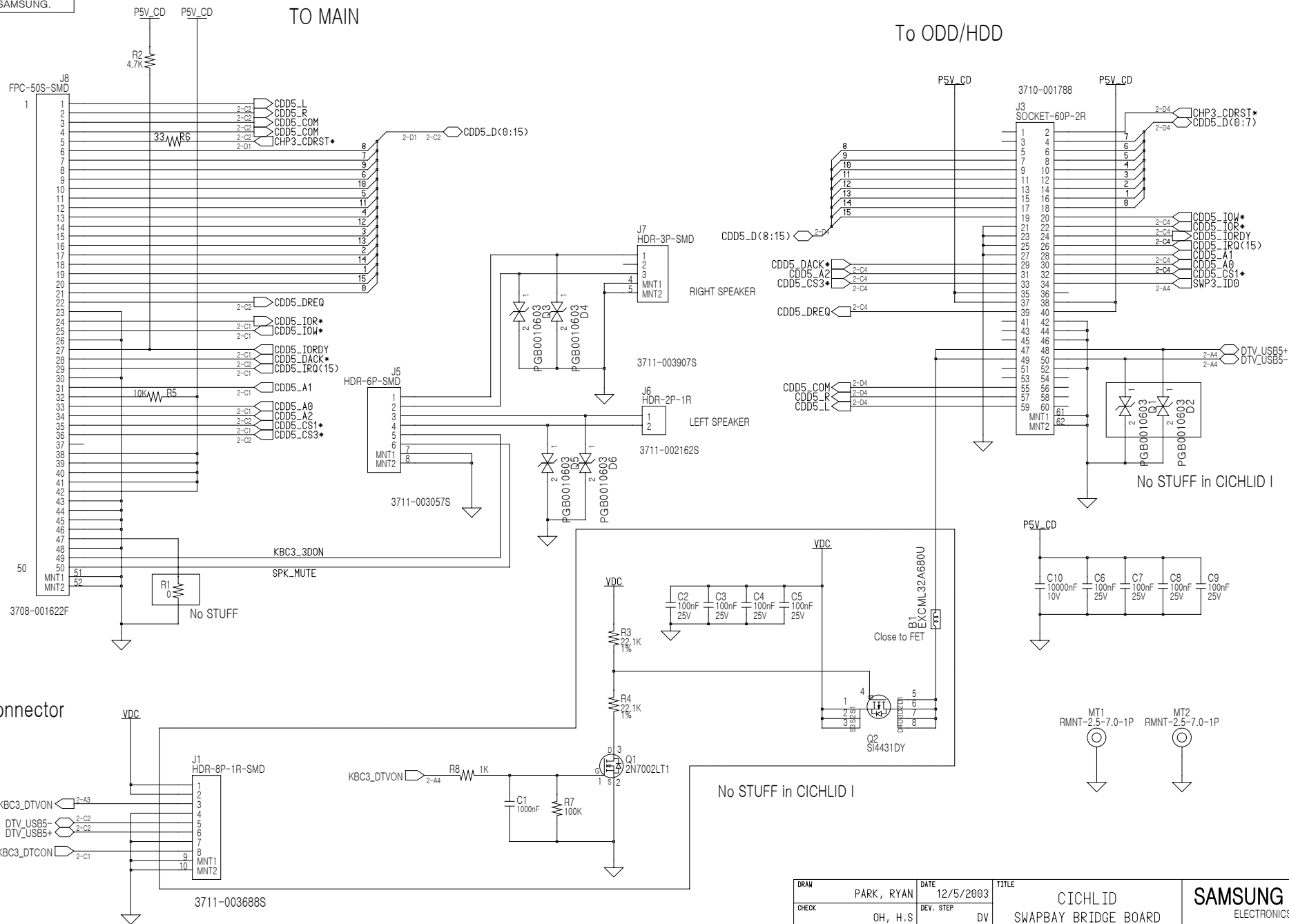
T.R. Date : 2004.04.01

DRAW	CHECK	APPROVAL

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CHECK	OH, H.S	DEV. STEP	DV			
APPROVAL	LEE, KEVIN	REV	1.0	PART NO.		BA41-
MODULE CODE	LAST EDIT			December, 5, 2003 9:40:29 AM	PAGE	1 OF 2

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DRAW	PARK, RYAN	DATE	12/5/2003	TITLE	CICHlid	SAMSUNG ELECTRONICS
CHECK	OH, H.S	DEV. STEP	DV	SWAPBAY BRIDGE BOARD	UNDEF INED	
APPROVAL	LEE, KEVIN	REV	1.0			PART NO. BA41-undef ined
MODULE CODE		LAST EDIT		December, 5, 2003 9:40:50 AM	PAGE	2 OF 2

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TP19ONS4406
TP20ONS4407
TP21ONS4408
TP22OCDD5_L
TP23OCDD5_R
TP24ONS4411
TP25ONS4412
TP26ONS4413
TP27ONS4414
TP28ONS4415
TP29ONS4416
TP30ONS4417
TP31ONS4418
TP32ONS4419
TP33OCDD5_A0
TP34OCDD5_A1
TP35OCDD5_A2
TP36OCDD5_COM
TP37OSPK_MUTE
TP38OCDD5_CS1*
TP39OCDD5_CS3*
TP40OCDD5_D(0)
TP41OCDD5_D(1)
TP42OCDD5_D(2)
TP43OCDD5_D(3)
TP44OCDD5_D(4)
TP45OCDD5_D(5)
TP46OCDD5_D(6)
TP47OCDD5_D(7)
TP48OCDD5_D(8)
TP49OCDD5_D(9)
TP50OCDD5_DREQ
TP3OCDD5_IOR*
TP4OCDD5_IOW*
TP5ODTV_USB5+
TP6ODTV_USB5-
TP7OKBC3_3D0N
TP8OCDD5_D(10)
TP9OCDD5_D(11)
TP10OCDD5_D(12)
TP11OCDD5_D(13)
TP12OCDD5_D(14)
TP13OCDD5_D(15)
TP14OCDD5_DACK*
TP15OCDD5_IORDY
TP16OKBC3_DTVON
TP17OCHP3_CDRST*
TP18OCDD5_IRQ(15)
TP1OP5V_CD
TP2OVDC

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CICHLID

CPU : BANIAS/DOTHAN

Chip Set : ODEM+

Remarks :

Model Name : TOUCHPAD I/F BOARD

PBA Name :

PCB Code : BA59-01329A

Dev. Step : MP

Revision : 1.0

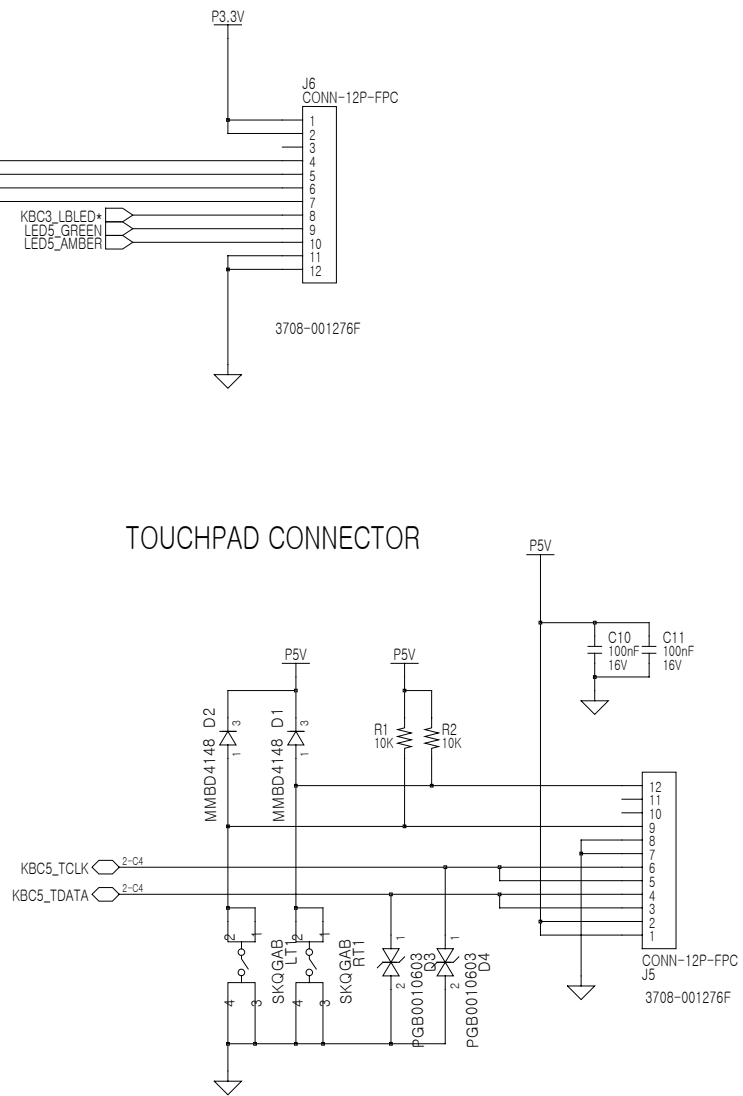
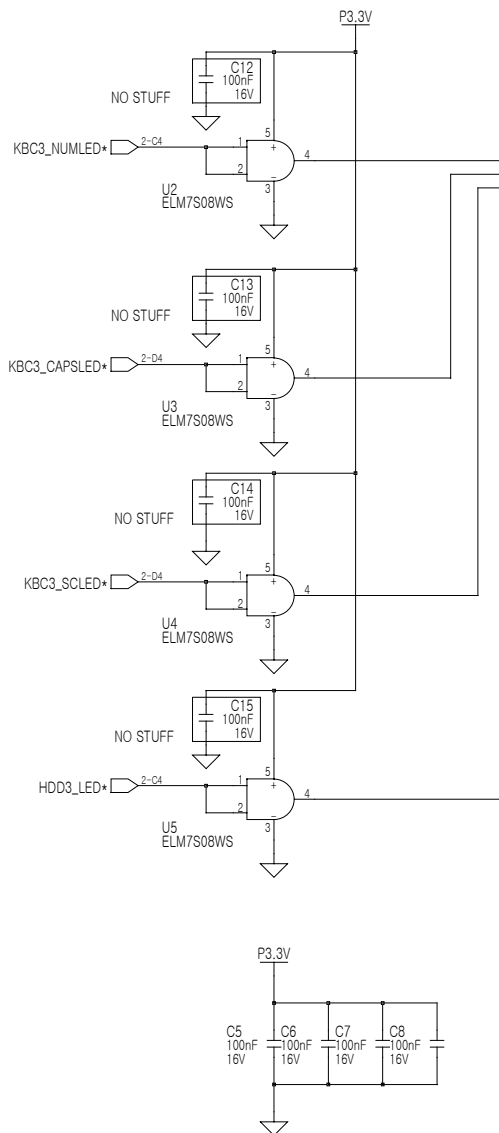
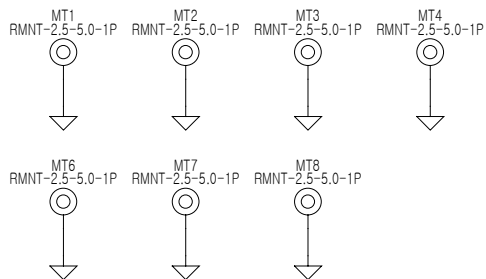
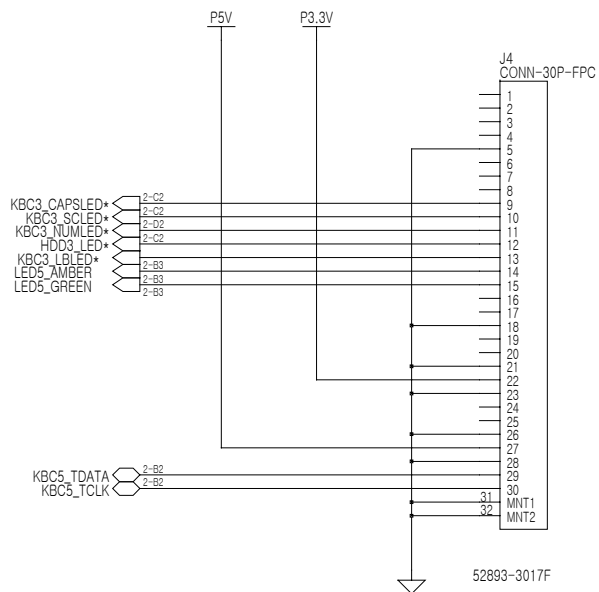
T.R. Date : 2004. 2. 28

DRAW	CHECK	APPROVAL

DRAW	PARK, RYAN	DATE	12/2/2003	TITLE	CICHLID TOUCHPAD I/F BOARD	SAMSUNG ELECTRONICS
CHECK	OH, H.S	DEV. STEP	DV	PART NO.		
APPROVAL	LEE, KEVIN	REV	1.0	December, 2, 2003 1:43:54 PM		PAGE 1 OF 2
MODULE CODE		LAST EDIT				

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DRAW	PARK, RYAN	DATE	12/2/2003	TITLE	CICHlid TOUCHPAD I/F BOARD UNDEFINED			SAMSUNG ELECTRONICS																	
CHECK	OH, H.S	DEV. STEP	DV	PART NO.					BA41-undef ined																
APPROVAL	LEE, KEVIN	REV	1.0																						
MODULE CODE		LAST EDIT	December, 2, 2003 1:44:53 PM	PAGE		2 OF 2																			