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HABANA-C

CPU : Intel Dothan -2M
 Chip Set : RC410MD & SB450
 Remarks : Mobility Platform

Model Name : HABANA-C
 PBA Name : MAIN
 PCB Code : BA41-00615A
 Dev. Step : PRR
 Revision : 1.0
 T.R. Date : 2005.12.26

DRAW	CHECK	APPROVAL
DS.JIANG	DJ.XU	KEVINLEE

Owner : *SESC R & D*

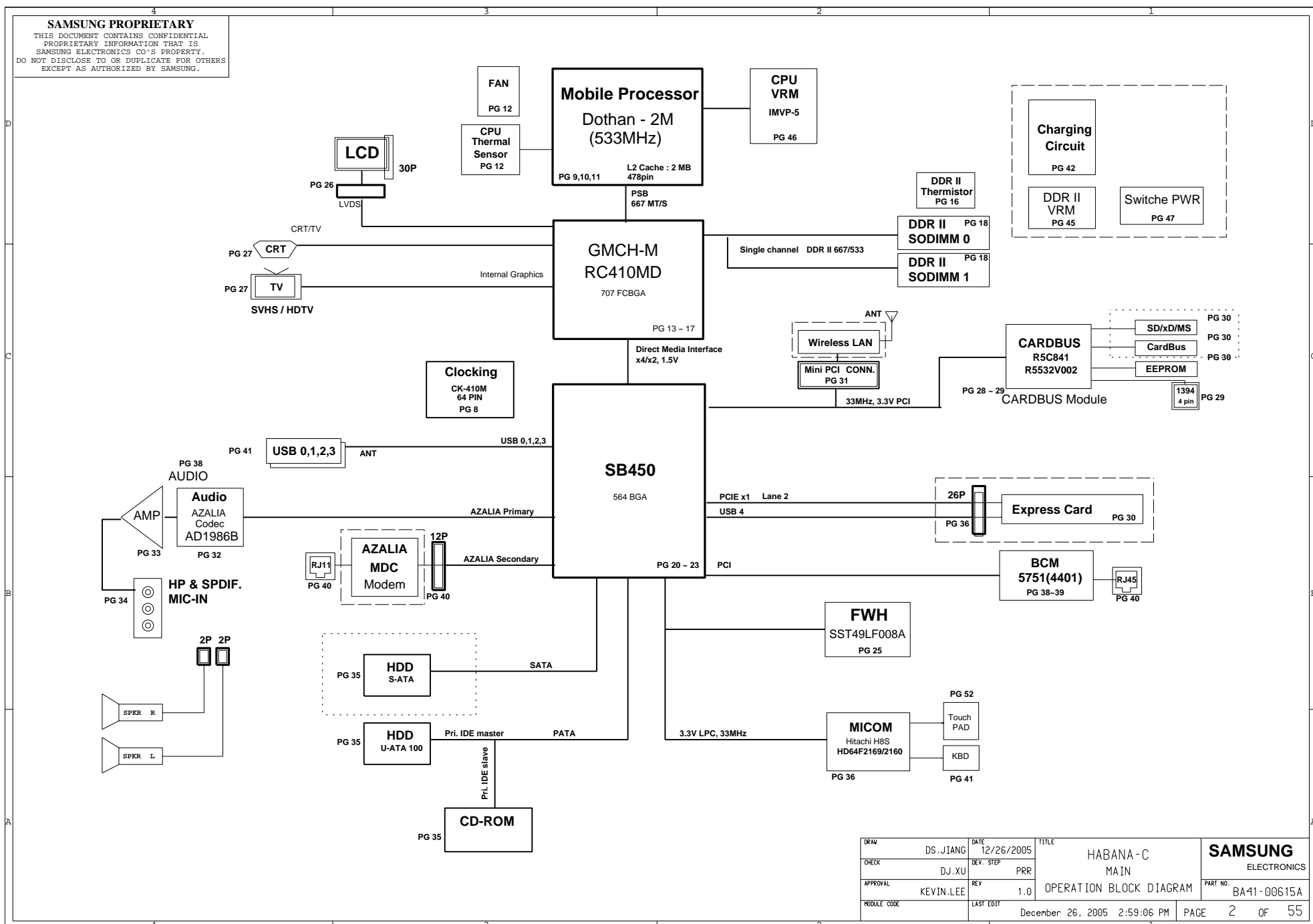
Signature :

Table of Contents

Sheet 1. COVER
 Sheet 2 - 7. DIAGRAM (Block/Power) & ANNOTATIONS
 Sheet 8. CLOCK GENERATOR
 Sheet 9 - 11. DOTHAN
 Sheet 12. THERMAL SENSOR / FAN CONTROL
 Sheet 13 - 17. RC410MD
 Sheet18. DDR II SODIMM
 Sheet19. DDR TERMINATION
 Sheet20 - 23. SB450
 Sheet24. SB450 STRAPS
 Sheet25. FWH
 Sheet26. LCD
 Sheet27. CRT AND TV CONN
 Sheet28-29. CARDBUS
 Sheet30. EXPRESS CARD
 Sheet31. MINIPC1
 Sheet32-34. AUDIO
 Sheet35. HDD AND ODD
 Sheet36. MICOM
 Sheet37. S I/O
 Sheet38-39. LAN
 Sheet40. LAN AND MDC CONN
 Sheet41. BOARD CONN
 Sheet42. CHARGE
 Sheet43. P3.3V_AUX AND P5V_AUX
 Sheet44. P1.2V AND VCCP
 Sheet45. DDR2 POWER
 Sheet46. CPU VRM
 Sheet47. SWITCH POWER
 Sheet48. P1.8V_ALW
 Sheet49. POWER STRAPS
 Sheet50. 1394 BOARD
 Sheet51. USB BOARD
 Sheet52. TOUCH PAD BOARD
 Sheet53-55. TP

DRAW	DS.JIANG	DATE	12/26/2005	TITLE	HABANA-C	SAMSUNG ELECTRONICS
CHECK	DJ.XU	DEV. STEP	PRR	COVER	PART NO.	
APPROVAL	KEVIN.LEE	REV	1.0		BA41-00615A	
MODULE CODE		LAST EDIT	December 26, 2005 2:59:06 PM	PAGE	1	OF 55

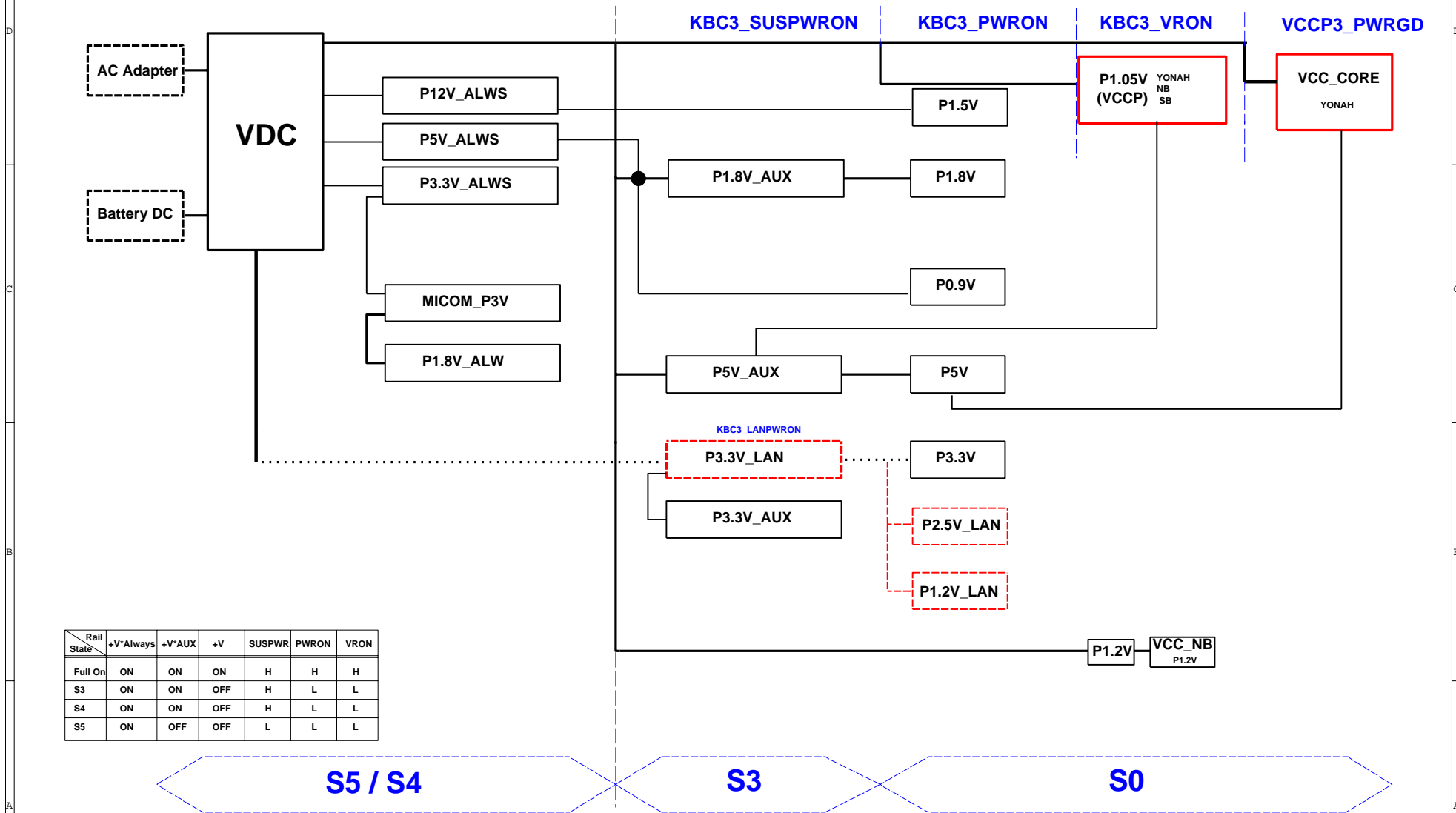
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APPROVAL	KEVIN.LEE	REV	1.0			
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Power Diagram

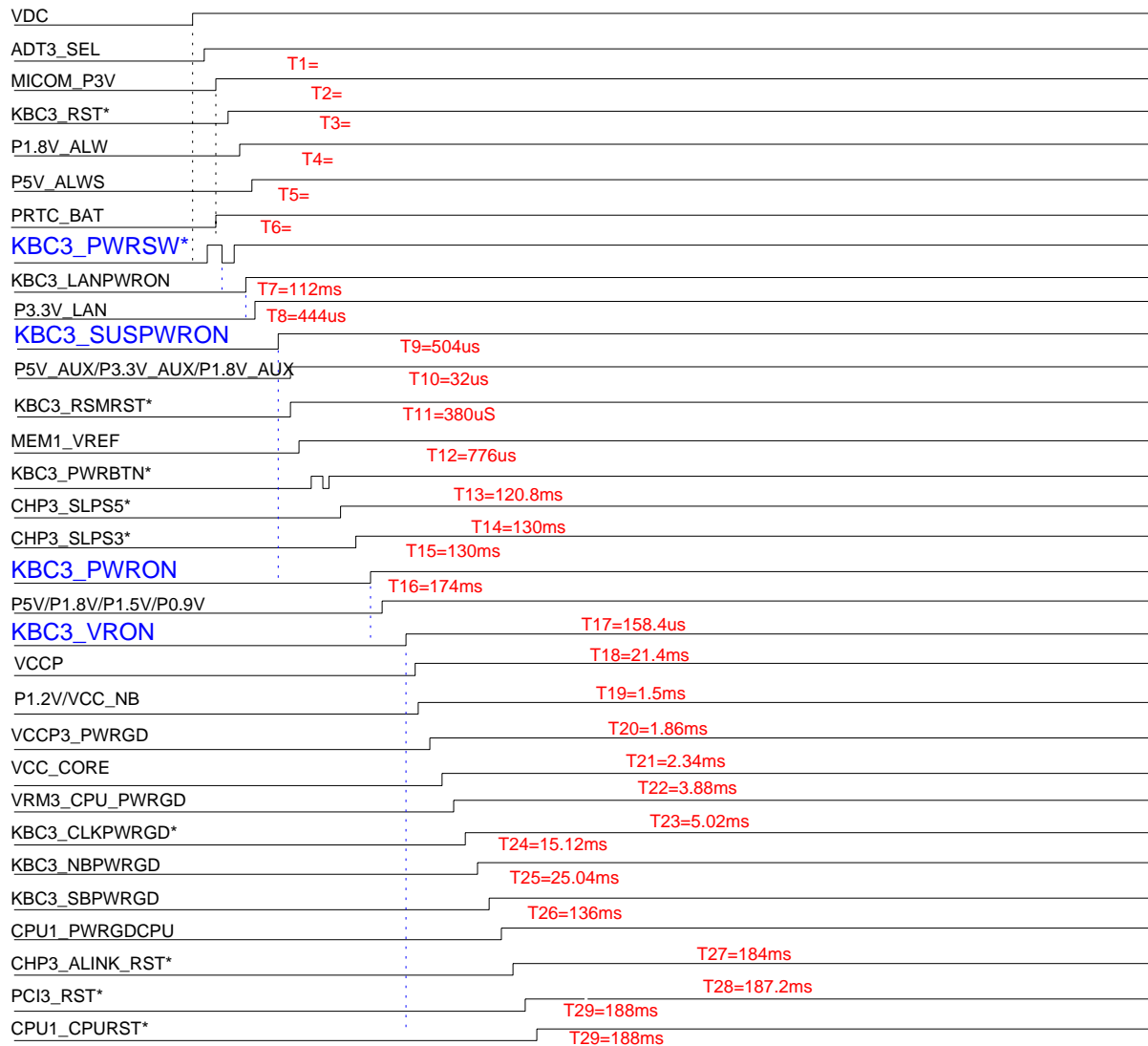


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CHECK	DJ.XU	DEV. STEP	PRR			
APPROVAL	KEVIN.LEE	REV	1.0			
MODULE CODE		LAST EDIT	December 26, 2005 2:59:06 PM	PAGE	3 OF 55	

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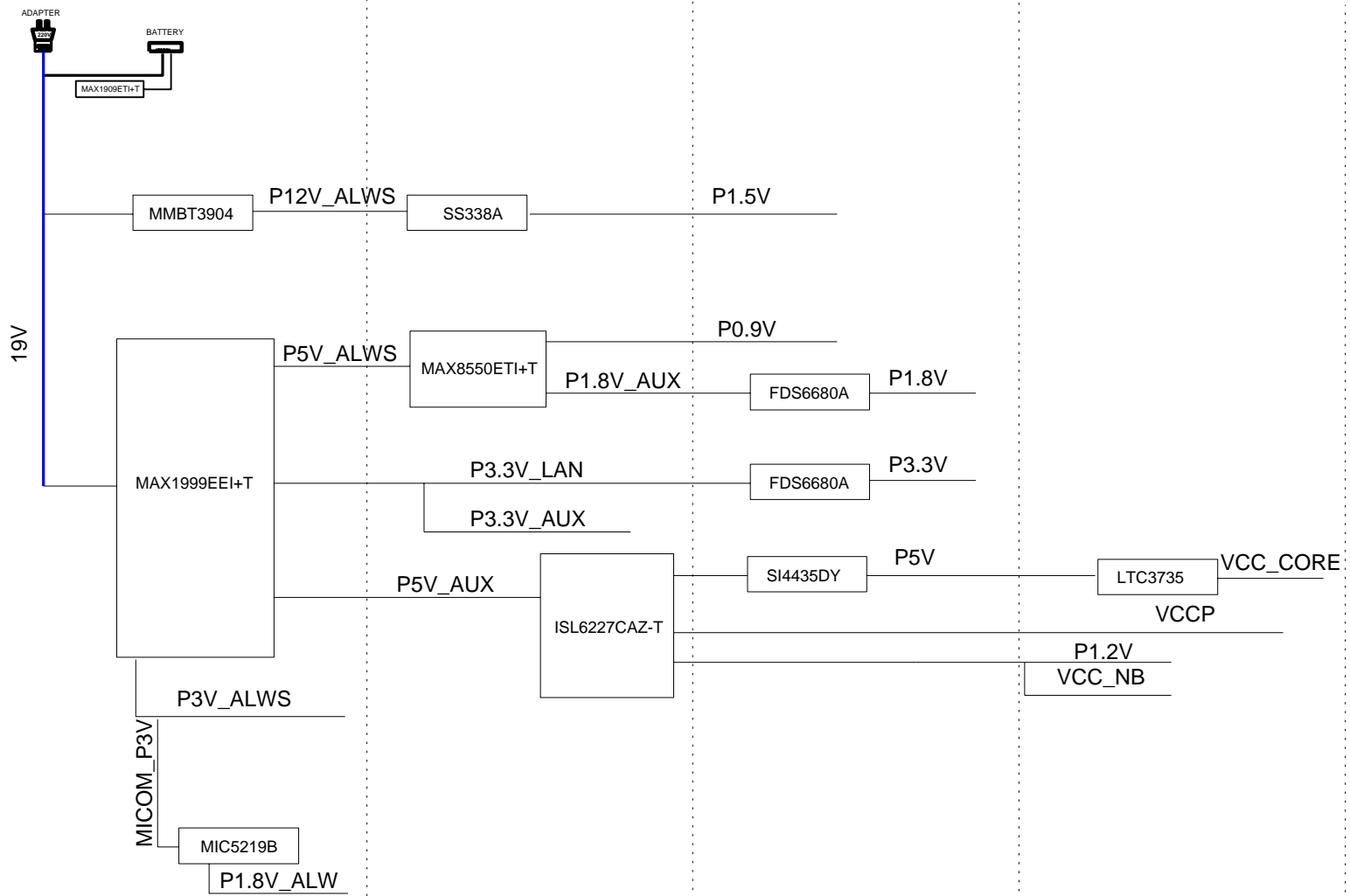
POWER SEQUENCE



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CHECK	DJ.XU	DEV. STEP	PRR			
APPROVAL	KEVIN.LEE	REV	1.0	POWER SEQUENCE		PART NO. BA41-00615A
MODULE CODE		LAST EDIT	December 26, 2005 2:59:06 PM	PAGE	4	OF 55

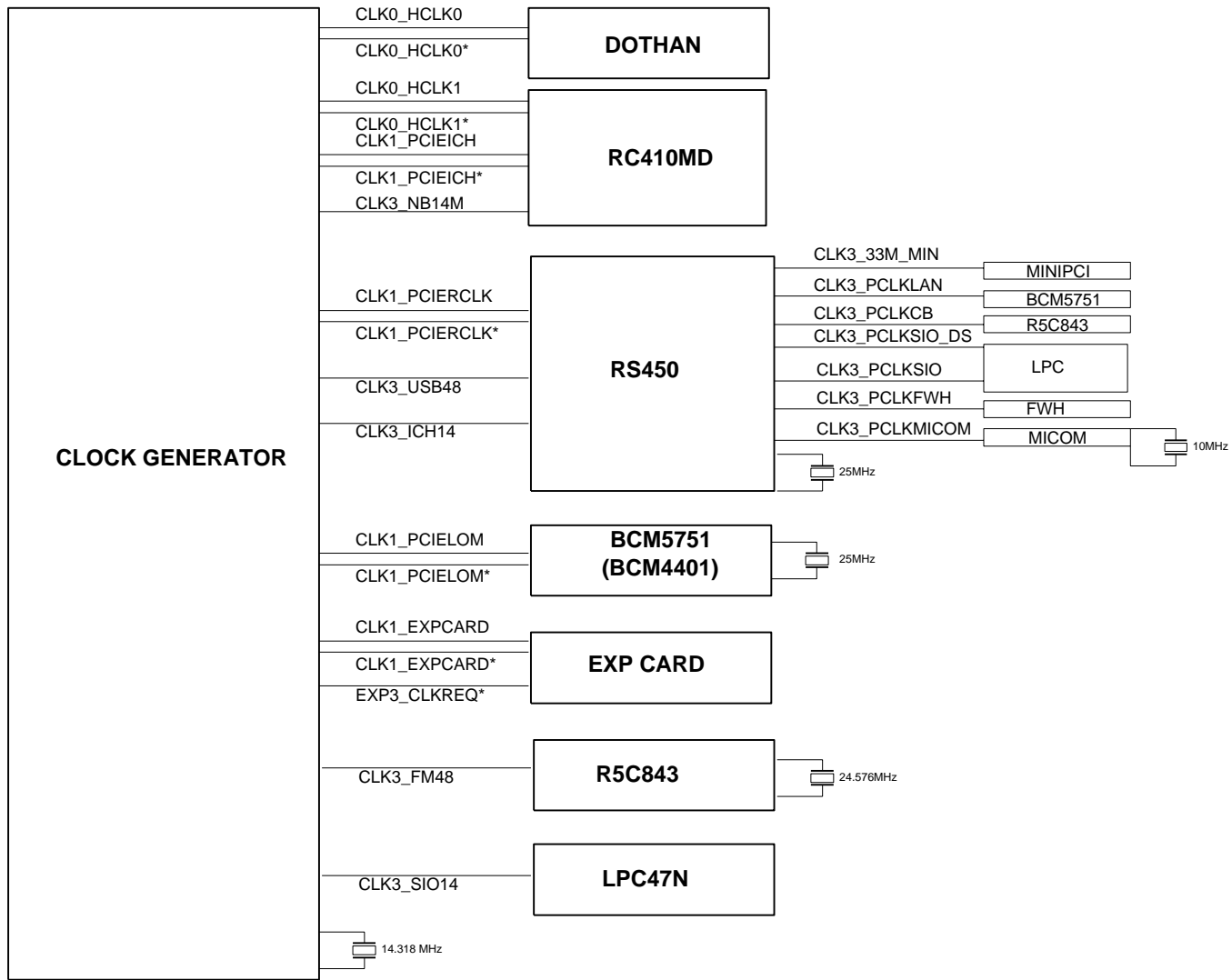
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POWER RAILS ANALYSIS



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MODULE CODE		LAST EDIT	December 26, 2005 2:59:06 PM	PAGE	5	OF 55

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MODULE CODE		LAST EDIT	December 26, 2005 2:59:06 PM				

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SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
Cardbus	AD24	0	E,F,G
LAN	AD21	1	C
MINIPCI	AD23	2	A,B
USB	AD30(internal)	-	-
Hub to PCI	AD31(internal)	-	-
LPC bridge/IDE/AC97/SMBUS	AD31(internal)	-	--
Internal MAC	AD31(internal)	-	-
AC Link	-	-	-

Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	SB450	Real Time Clock
Crystal	10MHz	MICOM	HD64F2169/2160
Crystal	14.318MHz	CLOCK-Generator	CK-410M
Crystal	24.576MHz	LAN	Cardbus Controller
Crystal	25MHz	LAN	1394 LOM

Voltage Rails

VCC_CORE	CPU
VCCP	CPU RC410MD SB450
VCC_NB	RC410MD
P1.2V	RC410MD VCC_NB
P1.5V	CPU EXPCARD
P1.8V	RC410MD SB450 R5C843
P0.9V	DDR2
P5V	FAN THERMAL CRT SB450 R5C483 MINIPCI AD1986B HDD ODD MICOM USB TOUCH-PAD VCC_CORE
P3.3V	SYSTEM POWER
P2.5V_LAN	BCM5751
P1.2V_LAN	BCM5751
P1.8V_AUX	DDR2 P1.8V RC410MD
P5V_AUX	THERMAL LCD P1.2V P5V
P3.3V_LAN	LCD BCM5751 P3.3V
P3.3V_AUX	MDC MICOM MINIPCI EXP-CARD SB450 THERMAL
P12V_ALWS	VCC_NB P1.5V P3.3V P1.8V
P5V_ALWS	P3.3V DDR2-PWR
P3.3V_ALWS	MICOM_P3V
MICOM_P3V	THERMAL SB450 MICOM LED P1.8V_ALWS
P1.8V_ALW	SB450
VDC	Primary DC system power supply (7 to 21V)

CPU Core Voltage Table

VID(5:0)	Voltage	VID(5:0)	Voltage
0 0 0 0 0 0	1.708 V	1 0 0 0 0 0	1.196 V
0 0 0 0 0 1	1.692 V	1 0 0 0 0 1	1.180 V
0 0 0 0 1 0	1.676 V	1 0 0 0 1 0	1.164 V
0 0 0 0 1 1	1.660 V	1 0 0 0 1 1	1.148 V
0 0 0 1 0 0	1.644 V	1 0 0 1 0 0	1.132 V
0 0 0 1 0 1	1.628 V	1 0 0 1 0 1	1.116 V
0 0 0 1 1 0	1.612 V	1 0 0 1 1 0	1.100 V
0 0 0 1 1 1	1.596 V	1 0 0 1 1 1	1.084 V
0 0 1 0 0 0	1.580 V	1 0 1 0 0 0	1.068 V
0 0 1 0 0 1	1.564 V	1 0 1 0 0 1	1.052 V
0 0 1 0 1 0	1.548 V	1 0 1 0 1 0	1.036 V
0 0 1 0 1 1	1.532 V	1 0 1 0 1 1	1.020 V
0 0 1 1 0 0	1.516 V	1 0 1 1 0 0	1.004 V
0 0 1 1 0 1	1.500 V	1 0 1 1 0 1	0.988 V
0 0 1 1 1 0	1.484 V	1 0 1 1 1 0	0.972 V
0 0 1 1 1 1	1.468 V	1 0 1 1 1 1	0.956 V
0 1 0 0 0 0	1.452 V	1 1 0 0 0 0	0.940 V
0 1 0 0 0 1	1.436 V	1 1 0 0 0 1	0.924 V
0 1 0 0 1 0	1.420 V	1 1 0 0 1 0	0.908 V
0 1 0 0 1 1	1.404 V	1 1 0 0 1 1	0.892 V
0 1 0 1 0 0	1.388 V	1 1 0 1 0 0	0.876 V
0 1 0 1 0 1	1.372 V	1 1 0 1 0 1	0.860 V
0 1 0 1 1 0	1.356 V	1 1 0 1 1 0	0.844 V
0 1 0 1 1 1	1.340 V	1 1 0 1 1 1	0.828 V
0 1 1 0 0 0	1.324 V	1 1 1 0 0 0	0.812 V
0 1 1 0 0 1	1.308 V	1 1 1 0 0 1	0.796 V
0 1 1 0 1 0	1.292 V	1 1 1 0 1 0	0.780 V
0 1 1 0 1 1	1.276 V	1 1 1 0 1 1	0.764 V
0 1 1 1 0 0	1.260 V	1 1 1 1 0 0	0.748 V
0 1 1 1 0 1	1.244 V	1 1 1 1 0 1	0.732 V
0 1 1 1 1 0	1.228 V	1 1 1 1 1 0	0.716 V
0 1 1 1 1 1	1.212 V	1 1 1 1 1 1	0.700 V

HFM Voltage
770:1.26V->1.372V
730,740,750,760:1.26->1.356V

IC / SMB Address

Devices	Address	Hex	Bus
SB450	Master	-	SMBUS Master
EMCN300(CPU Thermal Sensor)	1001 110X	9Ch	Thermal Sensor
SODIMM0	1010 0000	A0h	-
SODIMM1	1010 001X	A2h	-
CK-408 (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable

USB PORT Assign

PORT NUMBER	ASSIGNED TO
0	SYSTEM PORT A
1,2	SYSTEM PORT B
3	SYSTEM PORT C
4	EXPRESS CARD

System Power States

- CHP3_SLPS1* S1, Powered-On-Suspend(POS) : In this state, all clocks(except the 32.768KHz clock) are stopped. The system context is maintained in system DRAM. Power is maintained to PCI, the CPU, memory controller, memory, and all other critical subsystems. Note that this state does not preclude power being removed from non-essential devices, such as disk drives. During this state, CPU can be selected for either Deep Sleep or Deeper Sleep.
- CHP3_SLPS3* S3, Suspend-To-RAM(STR) : The system context is maintained in system DRAM, but power is shut off to non-critical circuits. Memory is retained, and refreshes continue. All clocks stop except RTC clock.
- CHP3_SLPS4* S4, Suspend-To-Disk(STD) : The Context of the system is maintained on the disk. All power is then shut off to the system except for the logic required to resume. Externally appears same as S5, but may have different wake events.
- CHP3_SLPS5* S5, Soft Off(SOFF) : System context is not maintained. All power is shut off except for the logic required to restart. A full boot is required when waking.

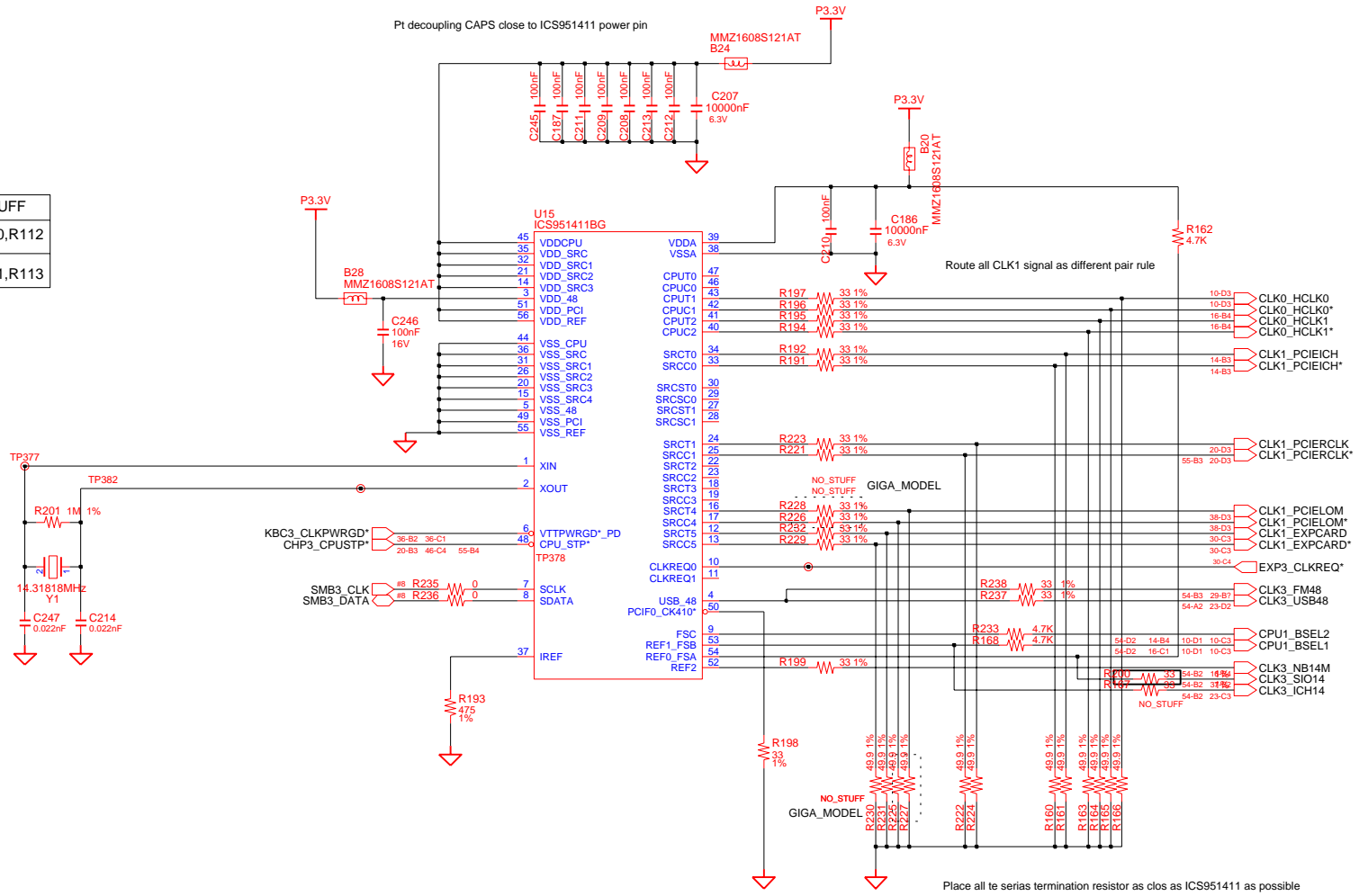
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CHECK	DJ.XU	DEV. STEP	PRR	PART NO.		
APPROVAL	KEVIN.LEE	REV	1.0	December 26, 2005 2:59:06 PM	PAGE	7 OF 55
MODULE CODE		LAST EDIT				

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CPU			HOST CLK
FSA	FSB	FSC	
BSEL0	BSEL1	BSEL2	
0	0	0	266 MHz
0	0	1	333 MHz
0	1	0	200 MHz
0	1	1	400 MHz
1	0	0	133 MHz
1	0	1	100 MHz
1	1	0	166 MHz
1	1	1	RSVD

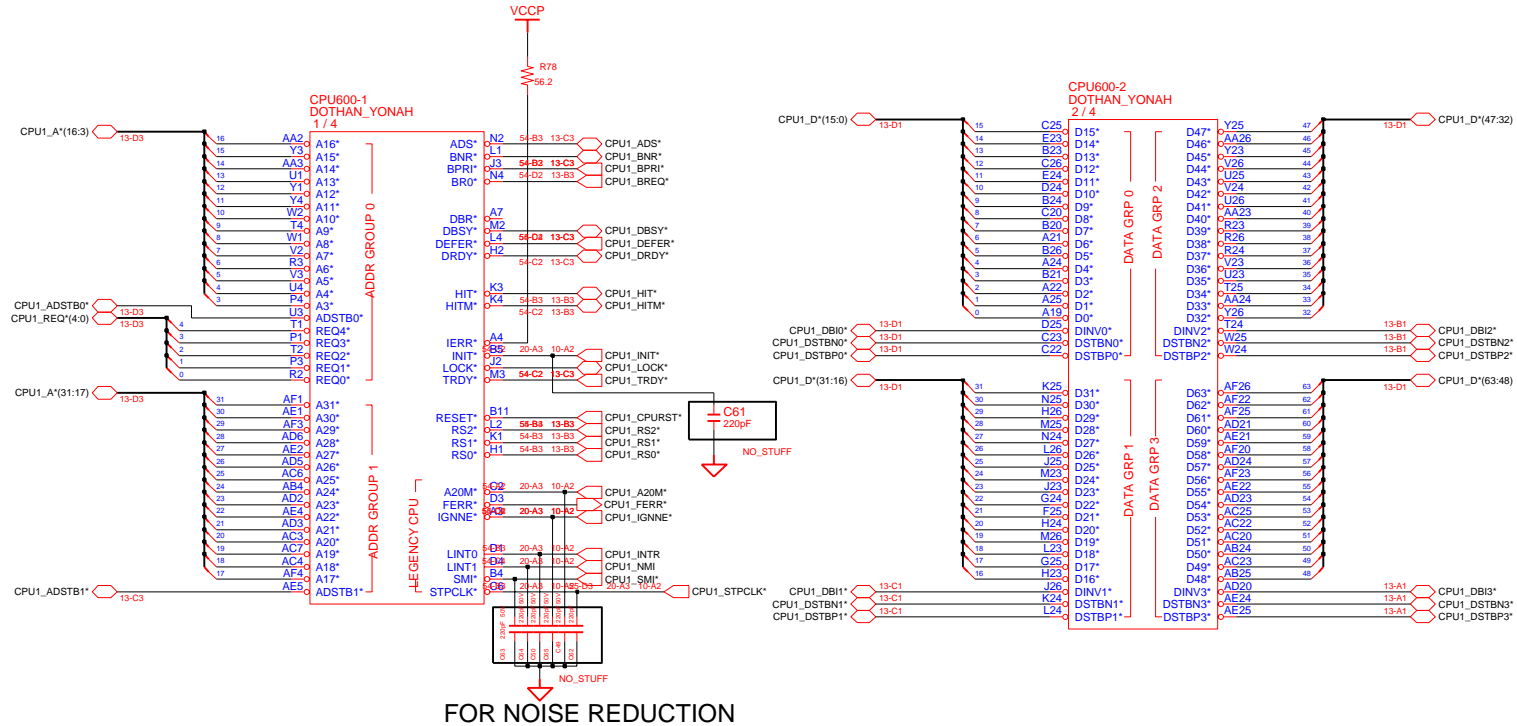
FSB	STUFF	NO STUFF
400MHz	R119,R141,R113	R121,R140,R112
533MHz	R119,R140,R112	R121,R141,R113



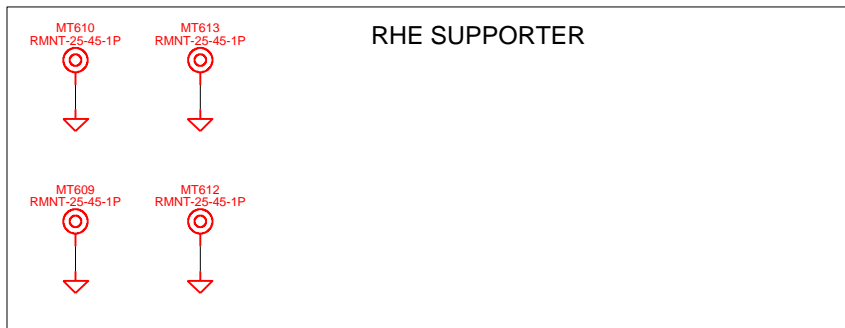
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APPROVAL	KEVIN.LEE	REV	1.0			
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**NOTE

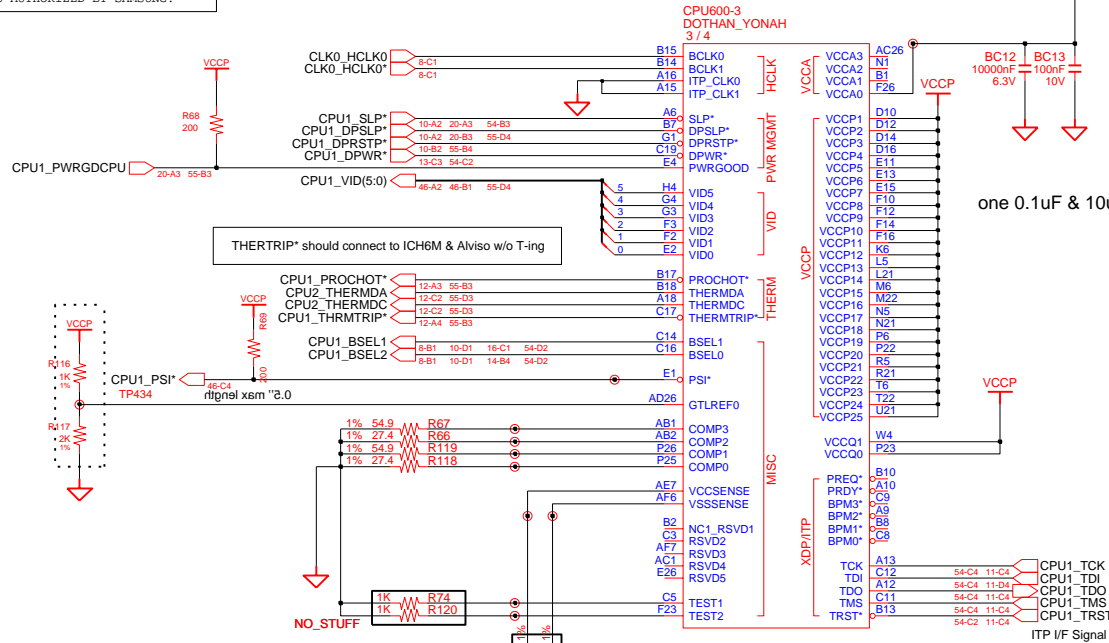


RHE SUPPORTER

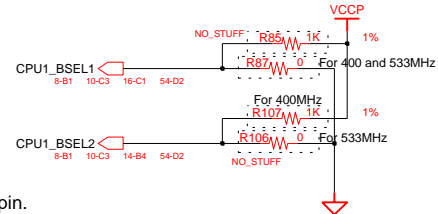
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CHECK	DJ.XU	DEV. STEP	PRR			
APPROVAL	KEVIN.LEE	REV	1.0			
MODULE CODE		LAST EDIT	December 26, 2005 2:59:06 PM	PAGE	9 OF 55	

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one 0.1uF & 10uF cap for each VCCA pin.



GTLREF : Keep the Voltage divider within 0.5" of the First GTLREF0 with Z0= 55 ohm trace
Minimize coupling of any switching signals to this net

COMP 0, 2 <(COMP 1,3) should be connected
Z0=27.4 ohm (55 ohm) trace shorter than
1/2" to their respective Banias Pins

CPU Core Voltage Table

VID(5:0)	Voltage	VID(5:0)	Voltage
0 0 0 0 0	1.708 V	1 0 0 0 0	1.196 V
0 0 0 0 1	1.692 V	1 0 0 0 1	1.180 V
0 0 0 1 0	1.676 V	1 0 0 1 0	1.164 V
0 0 0 1 1	1.660 V	1 0 0 1 1	1.148 V
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0 1 0 0 0	1.324 V	1 1 0 0 0	0.812 V
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0 1 0 1 0	1.292 V	1 1 0 1 0	0.780 V
0 1 0 1 1	1.276 V	1 1 0 1 1	0.764 V
0 1 1 0 0	1.260 V	1 1 1 0 0	0.748 V
0 1 1 0 1	1.244 V	1 1 1 0 1	0.732 V
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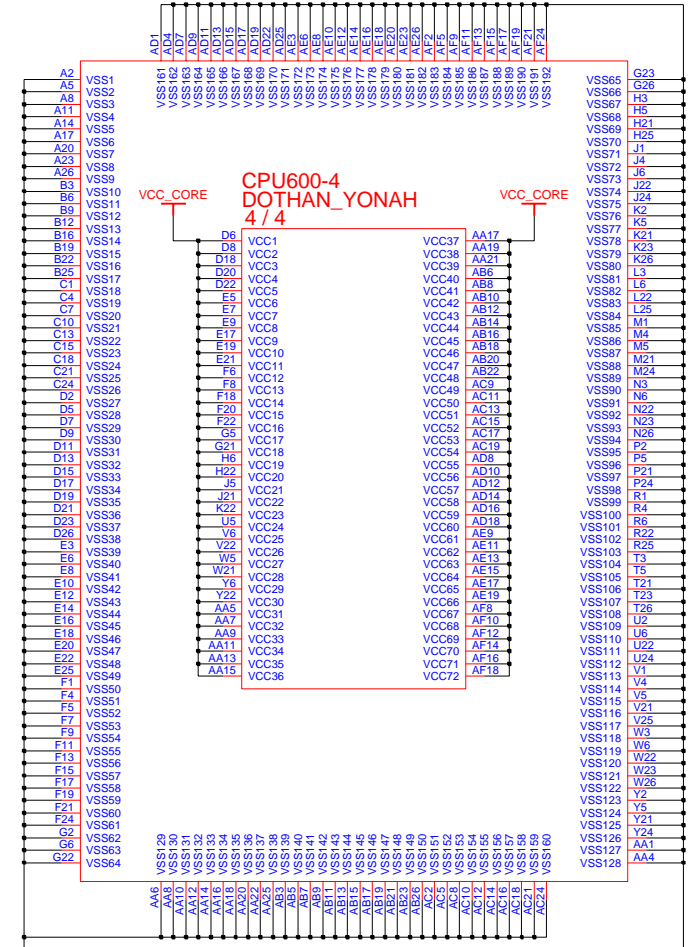
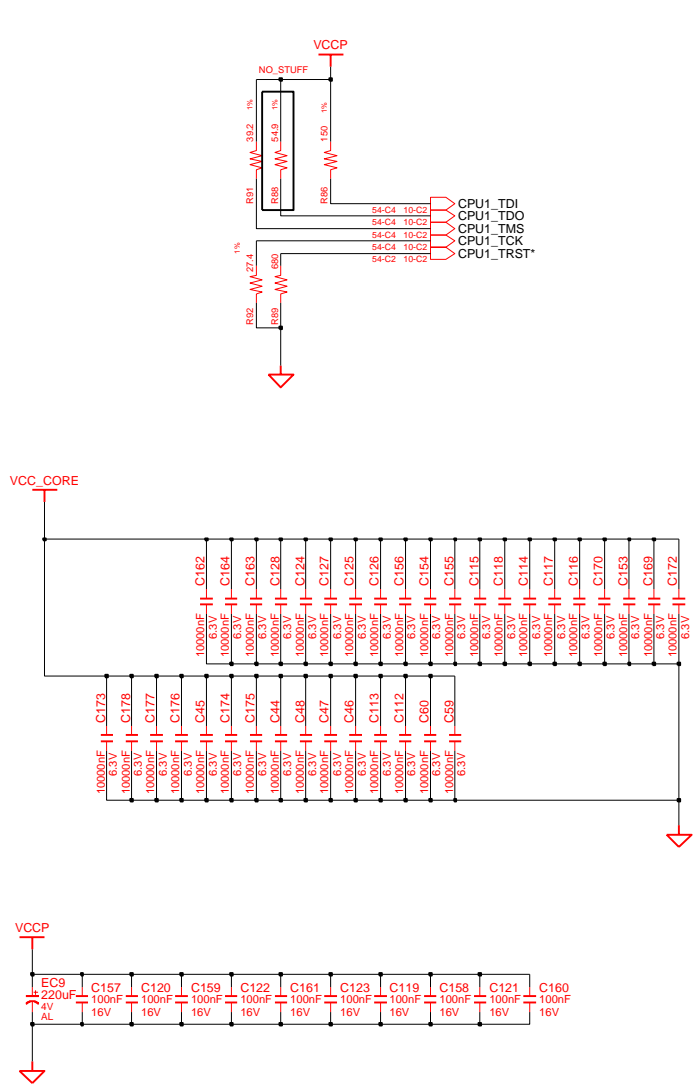
Std Voltage Dothan with 533MHz FSB updates
VCC(High Frequency Mode) = 1.26 V - 1.356 V(VID values)
TDP(High Frequency Mode) = 27W (no charge)
VCC(Lowest Frequency Mode) = 1.052V(VID value)
TDP(Lowest Frequency Mode) = 13.8W

GND test points within 100mil of the VCC/VSS sense at the end of the line
Route the VCC/VSS sense as a Z0=55ohm trace with equal length
Observe 3:1 spacing b/w VCC/VSS sense lines and 25mil away (preferred 50mil) from any other signal. And GND Via 100mil away from each of the VCC/VSS test point vias

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APPROVAL	KEVIN.LEE	REV	1.0	PAGE	10	PART NO. BA41-00615A
MODULE CODE		LAST EDIT	December 26, 2005 2:59:06 PM	PAGE	10	OF 55

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CHECK	DJ.XU	DEV. STEP	PRR	MAIN		
APPROVAL	KEVIN.LEE	REV	1.0	YONAH CPU(3/3)		
MODULE CODE		LAST EDIT	December 26, 2005 2:59:06 PM	PAGE	11 OF 55	

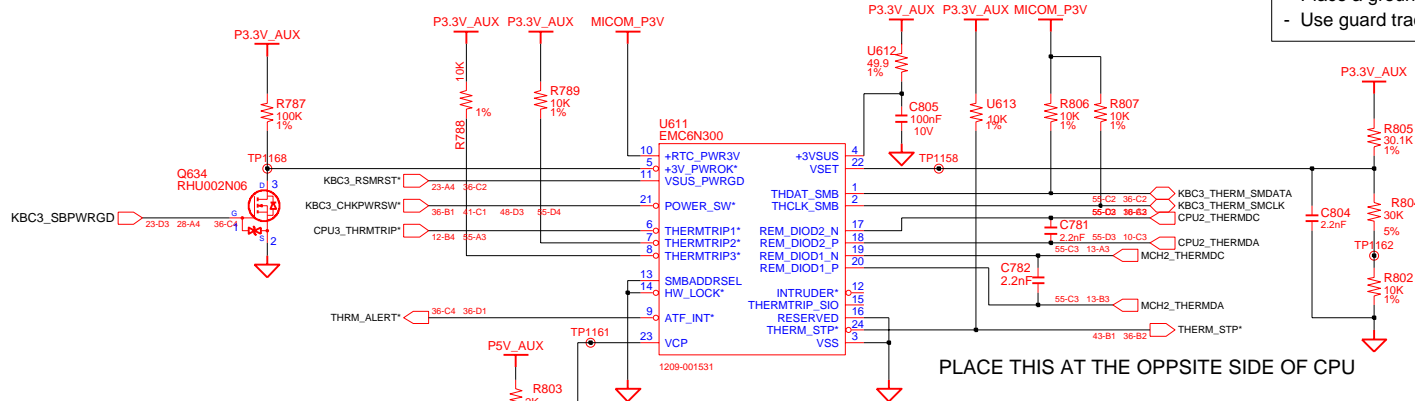
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CPU / DDR2 Thermal Sensor

Refer To Thermal Sensor Layout Guidelines.

- Place the Thermal Sensor close to a remote diode.
- Keep traces away from high voltage (+12V bus)
- Keep traces away from fast data buses and CRT signal.
- Use recommended trace widths and spacings (10mil)
- Place a ground plane under the traces.
- Use guard traces flanking DXP and DXN and connecting to GND



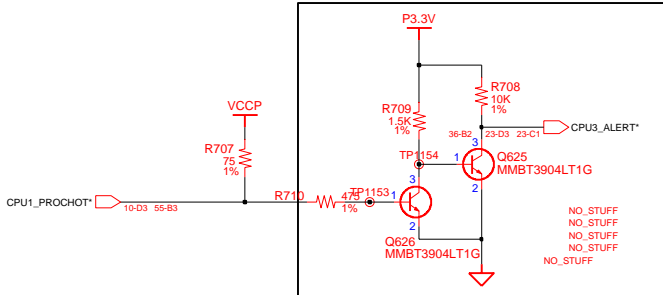
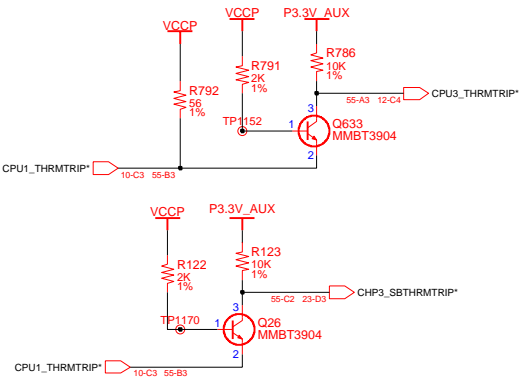
PLACE NEAR TO DDR2 SODIMM

PLACE THIS AT THE OPPSITE SIDE OF CPU

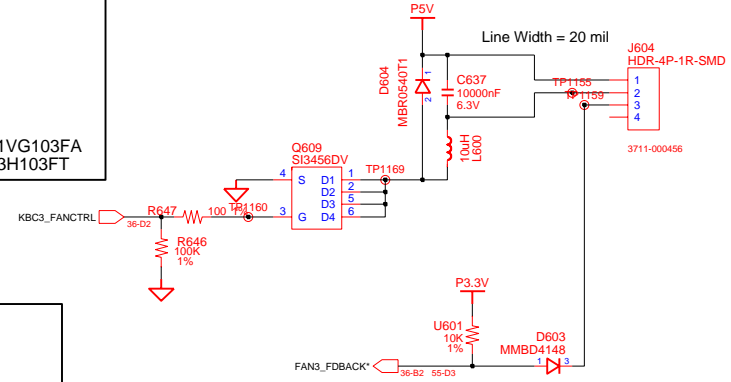
$V_{set} = (T_p - 75) / 16$ Where $T_p = 75$ to 106 degree C
 Set Trip point = 105 degree C
 $V_{set} = (105 - 75) / 16 = 1.875V$
 Guardian Temp-tolerance = ± 3 degree C

TH1:
 Panasonic 1% 0603 10K ohm @ 25 degree C.P/N: ERTJ1VG103FA
 Mitsubishi 1% 0603 10K ohm @ 25 degree C.P/N: TH11-3H103FT

$VCP \text{ voltage} = 5V * TH1 / (TH1 + 2.21K)$
 When TH1 is 10Kohm, VCP is 4.1V.
 If TH1 is 1Kohm, VCP is 1.56V.



FAN Control Logic

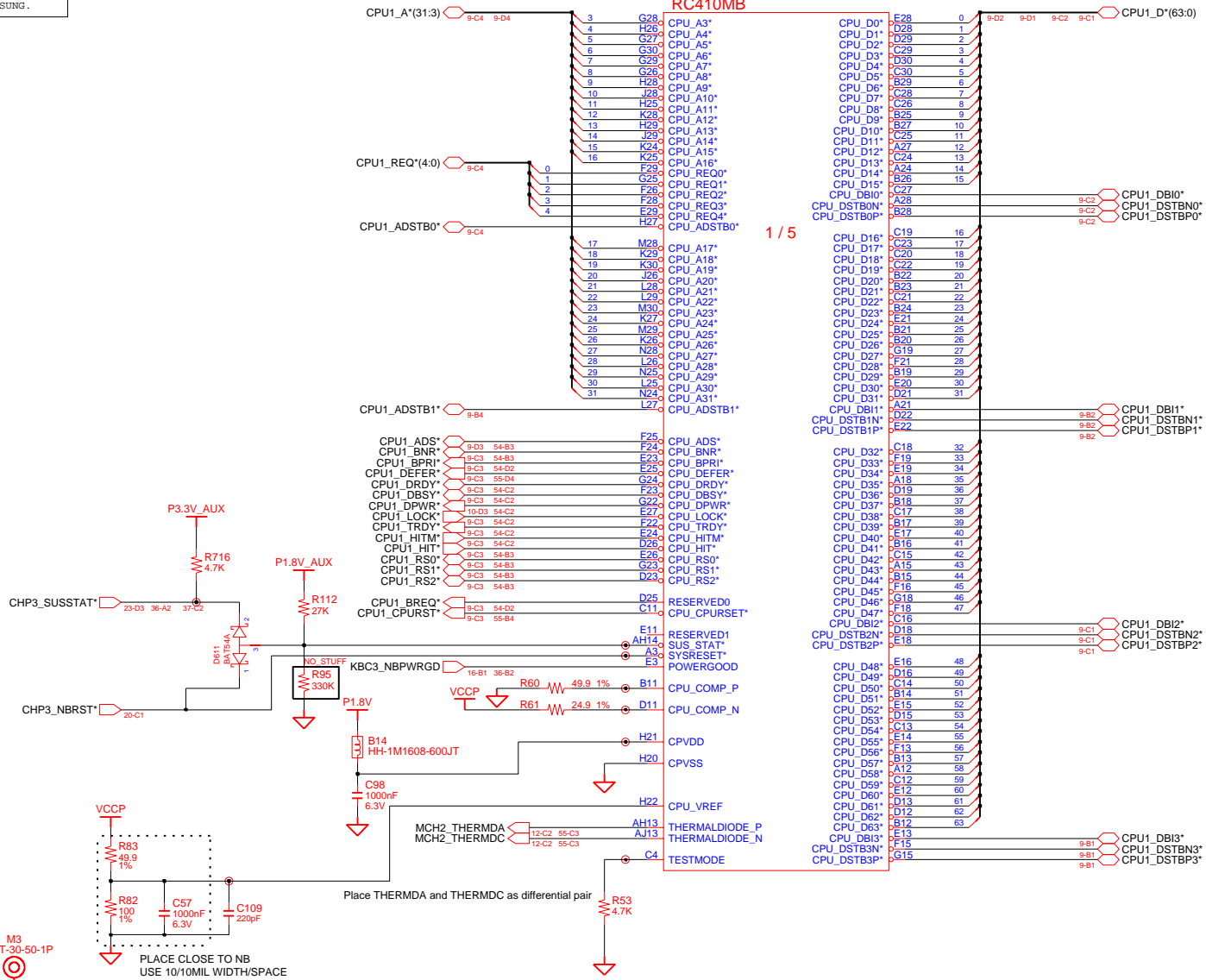


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CHECK	DJ.XU	DEV. STEP	PRR	MAIN		
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MODULE CODE		LAST EDIT	December 26, 2005 2:59:06 PM		PAGE	12 OF 55

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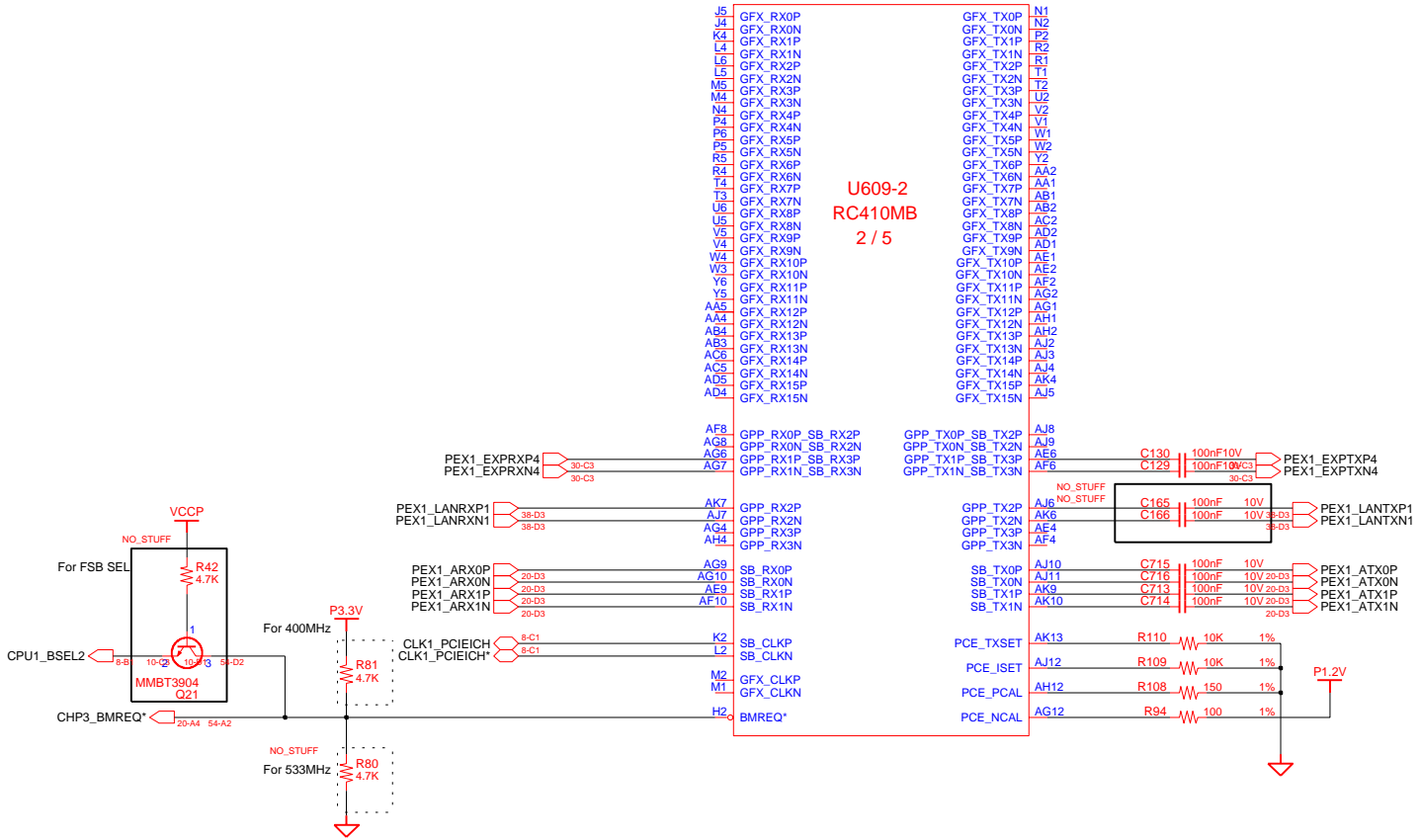
**U609-1
RC410MB**



DRAW	DS.JIANG	DATE	12/26/2005	TITLE	HABANA-C MAIN RC410MD(1/5)	SAMSUNG ELECTRONICS PART NO. BA41-00615A
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MODULE CODE		LAST EDIT	December 26, 2005 2:59:06 PM	PAGE	13 OF 55	

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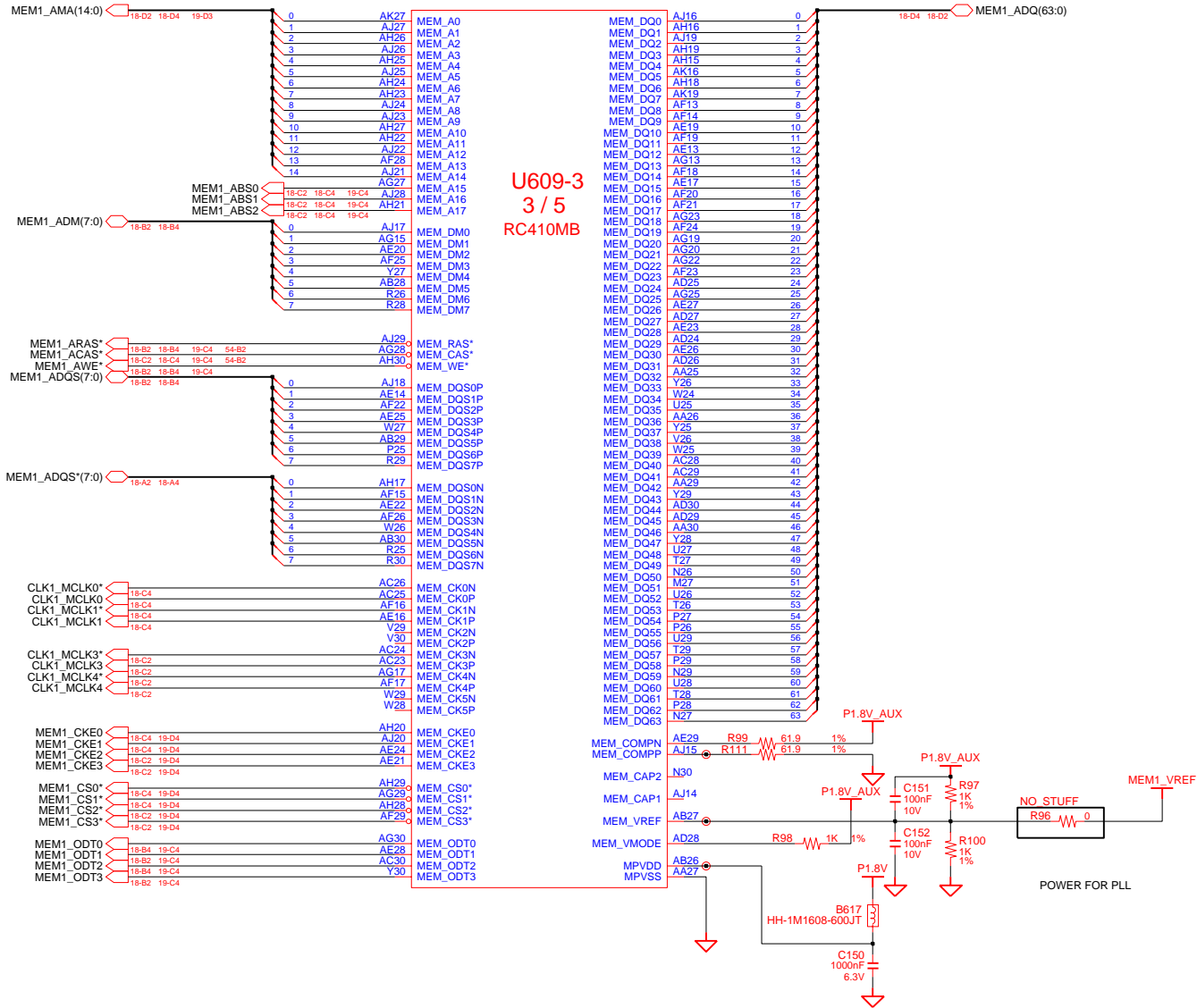
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DRAW	DS.JIANG	DATE	12/26/2005	TITLE	HABANA-C MAIN RC410MD(2/5)	SAMSUNG ELECTRONICS PART NO. BA41-00615A
CHECK	DJ.XU	DEV. STEP	PRR			
APPROVAL	KEVIN.LEE	REV	1.0			
MODULE CODE		LAST EDIT				
				December 26, 2005 2:59:06 PM	PAGE	14 OF 55

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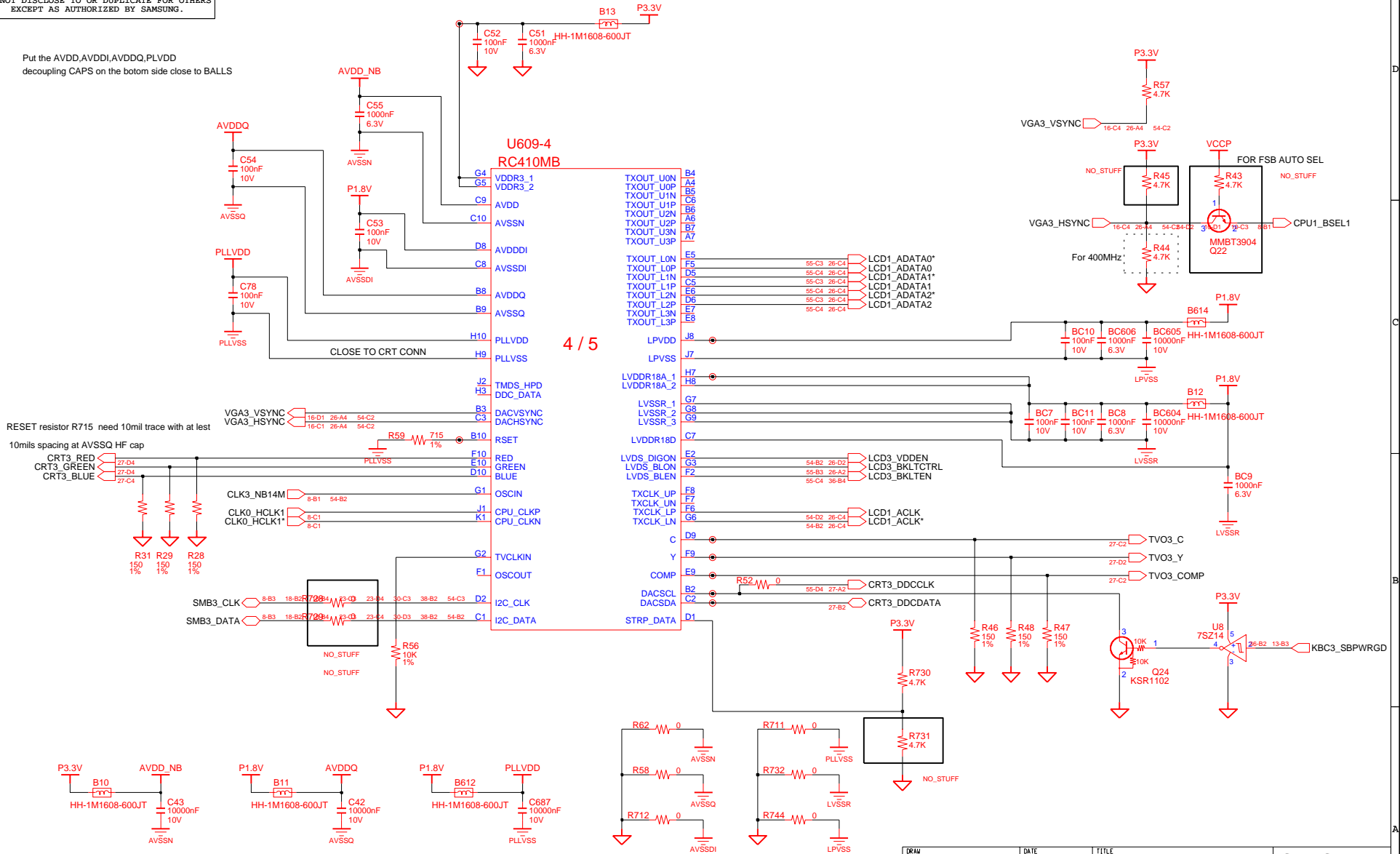


DRAW	DS.JIANG	DATE	12/26/2005	TITLE	HABANA-C MAIN RC410MD(3/5)	SAMSUNG ELECTRONICS PART NO. BA41-00615A
CHECK	DJ.XU	DEV. STEP	PRR	REV	1.0	
APPROVAL	KEVIN.LEE	LAST EDIT	December 26, 2005 2:59:06 PM	PAGE	15	OF 55

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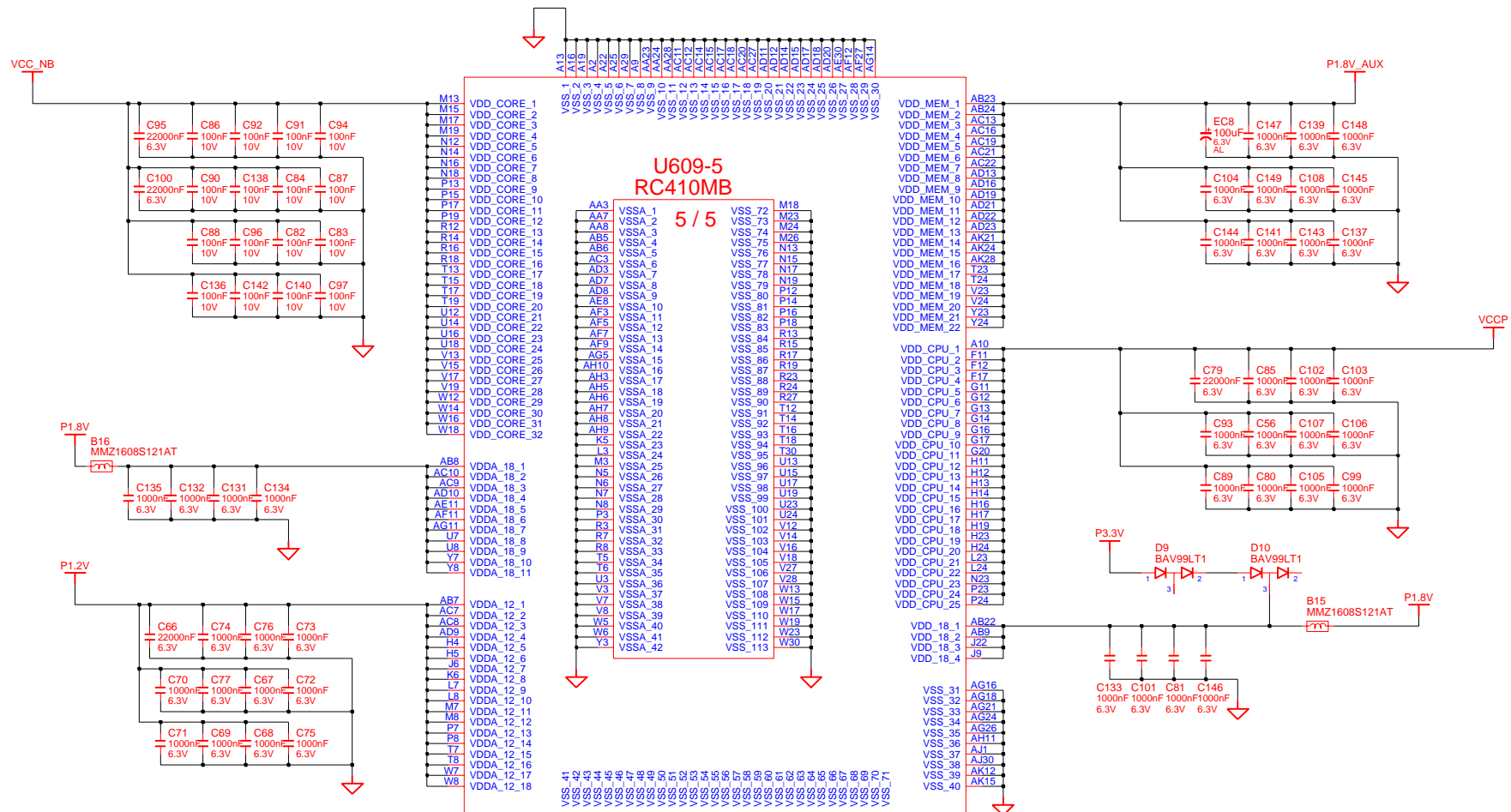
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Put the AVDD,AVDDI,AVDDQ,PLVDD decoupling CAPS on the bottom side close to BALLS



DRAW	DS.JIANG	DATE	12/26/2005	TITLE	HABANA-C	SAMSUNG ELECTRONICS
CHECK	DJ.XU	DEV. STEP	PRR	MAIN		
APPROVAL	KEVIN.LEE	REV	1.0	RC410MD(4/5)		PART NO. BA41-00615A
MODULE CODE		LAST EDIT	December 26, 2005 2:59:06 PM	PAGE	16	OF 55

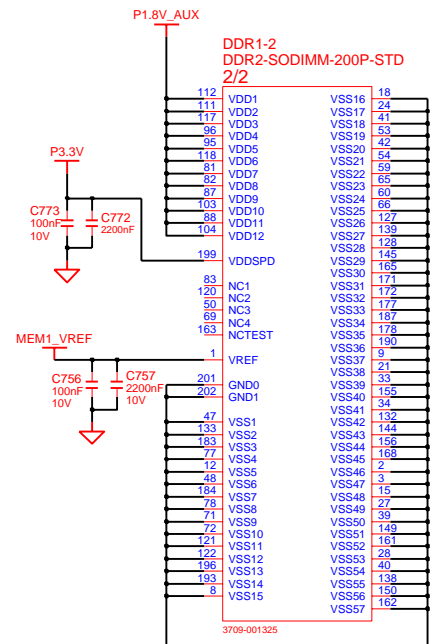
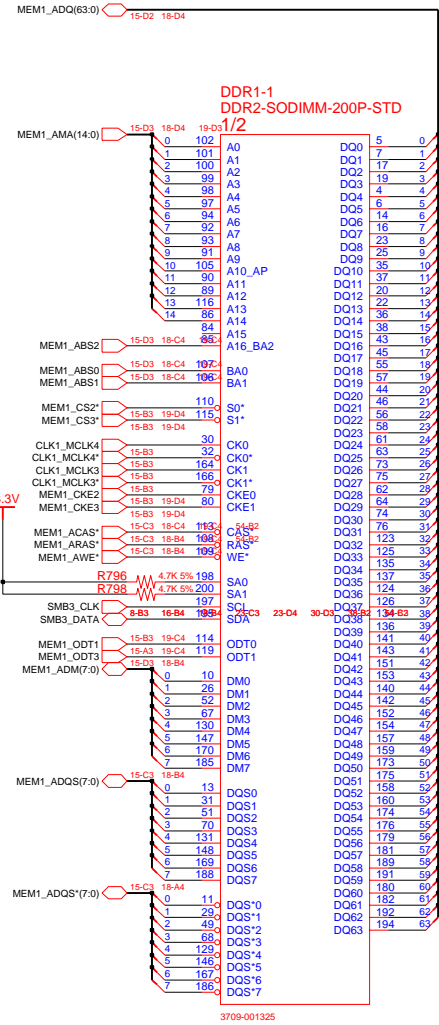
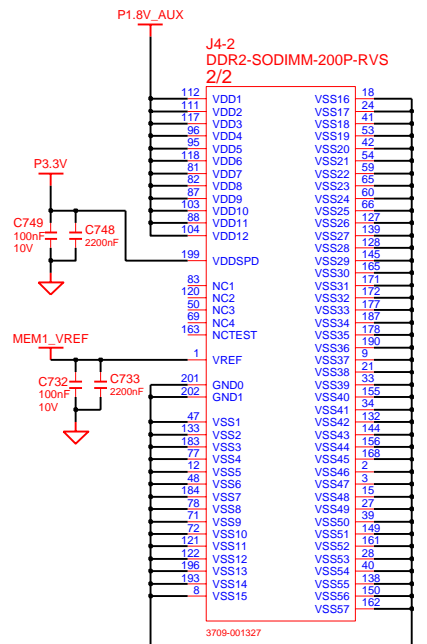
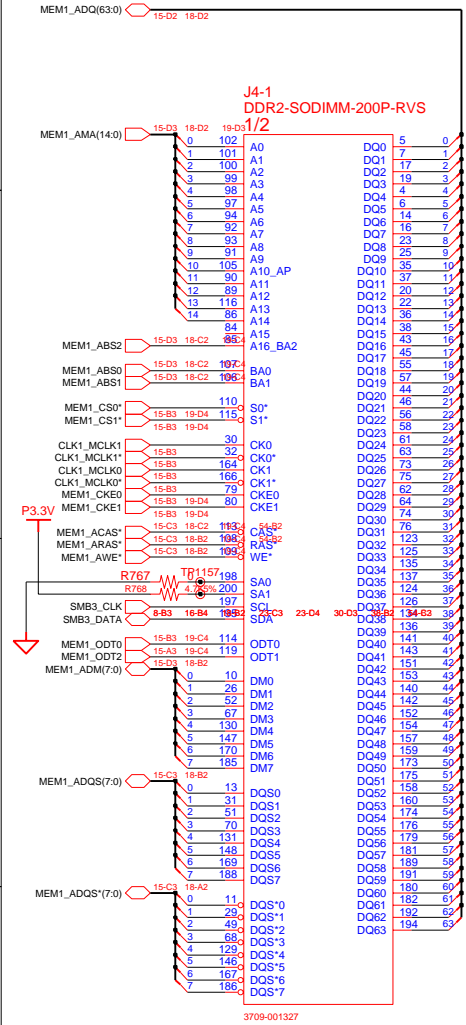
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CHECK	DJ.XU	DEV. STEP	PRR		PART NO.	
APPROVAL	KEVIN.LEE	REV	1.0			
MODULE CODE		LAST EDIT	December 26, 2005 2:59:06 PM	PAGE	17	OF 55

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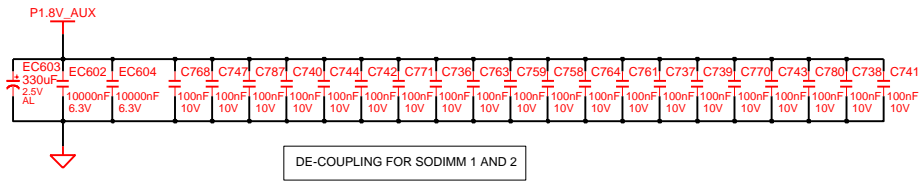
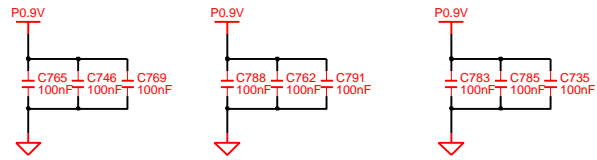
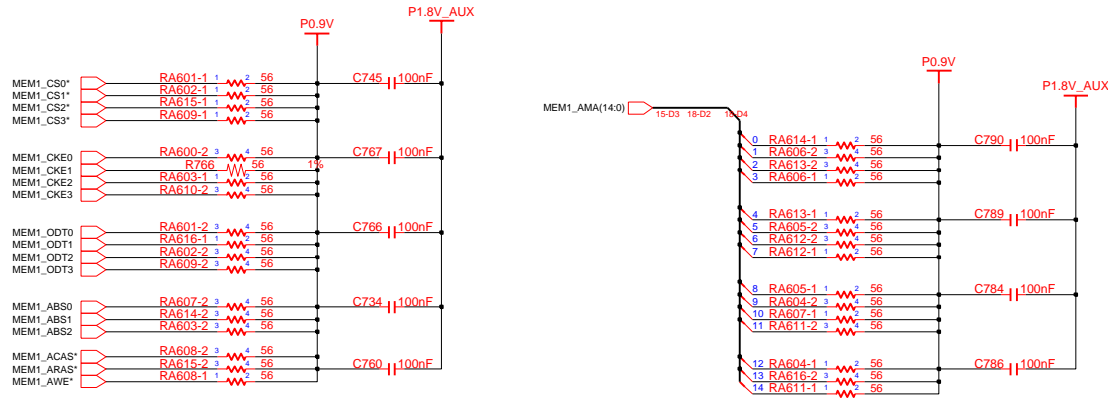
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CHECK	DJ.XU	DEV. STEP	PRR	MAIN		
APPROVAL	KEVIN.LEE	REV	1.0	DDR2 - SODIMM	PART NO.	BA41-00615A
MODULE CODE		LAST EDIT	December 26, 2005 2:59:06 PM	PAGE	18	OF 55

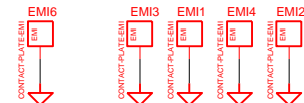
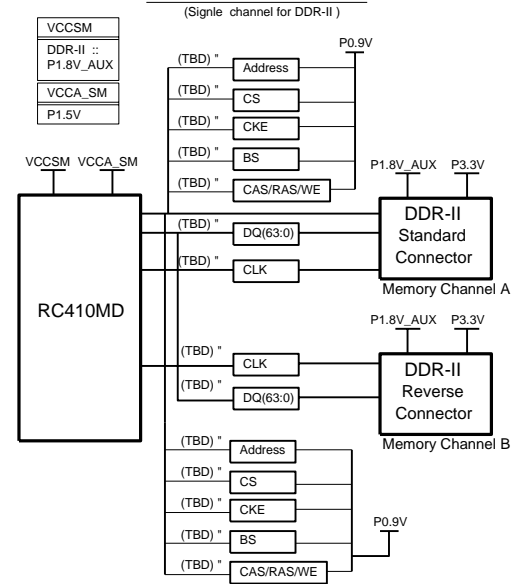
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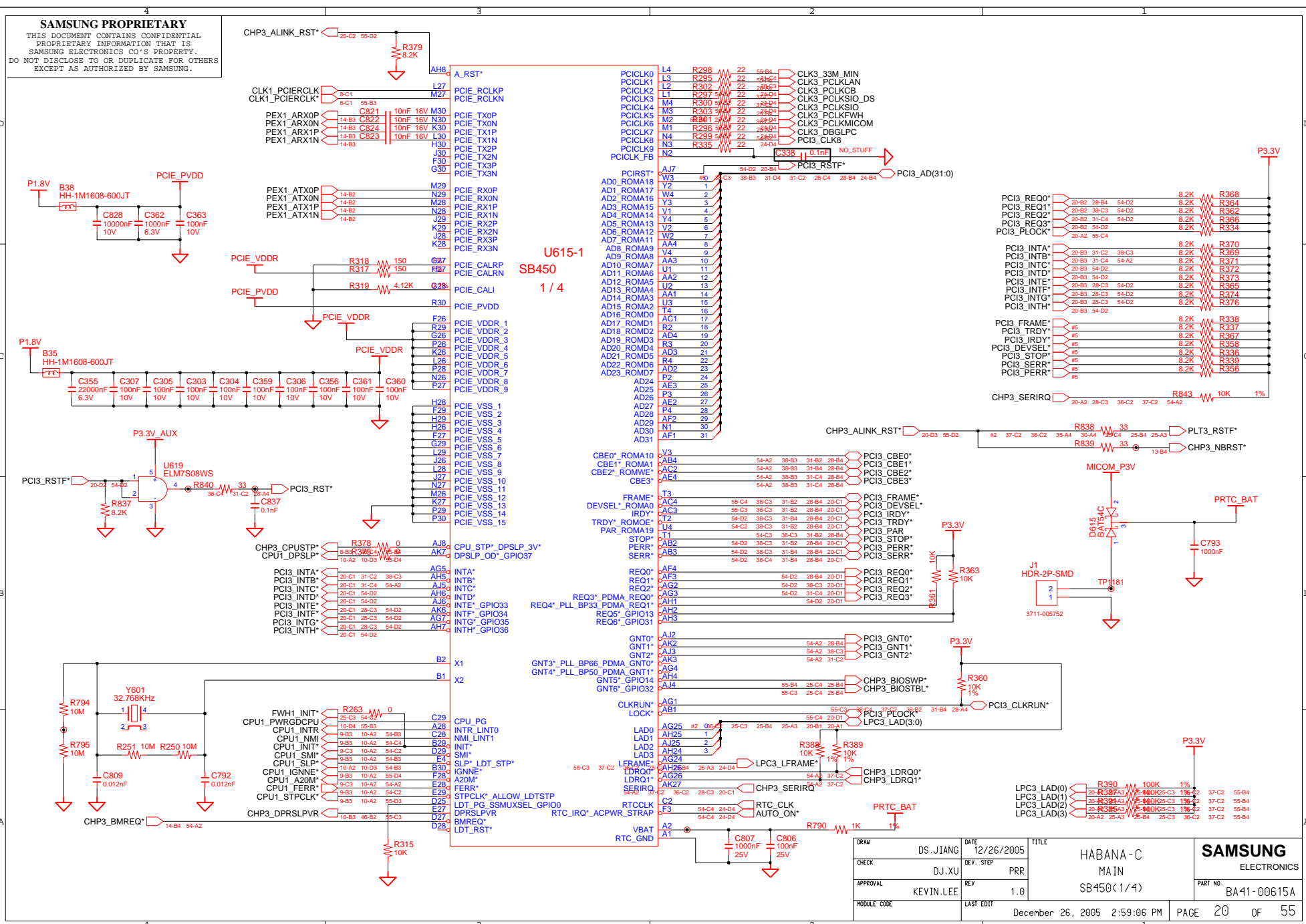


DE-COUPLING FOR SODIMM 1 AND 2

Memory Topology



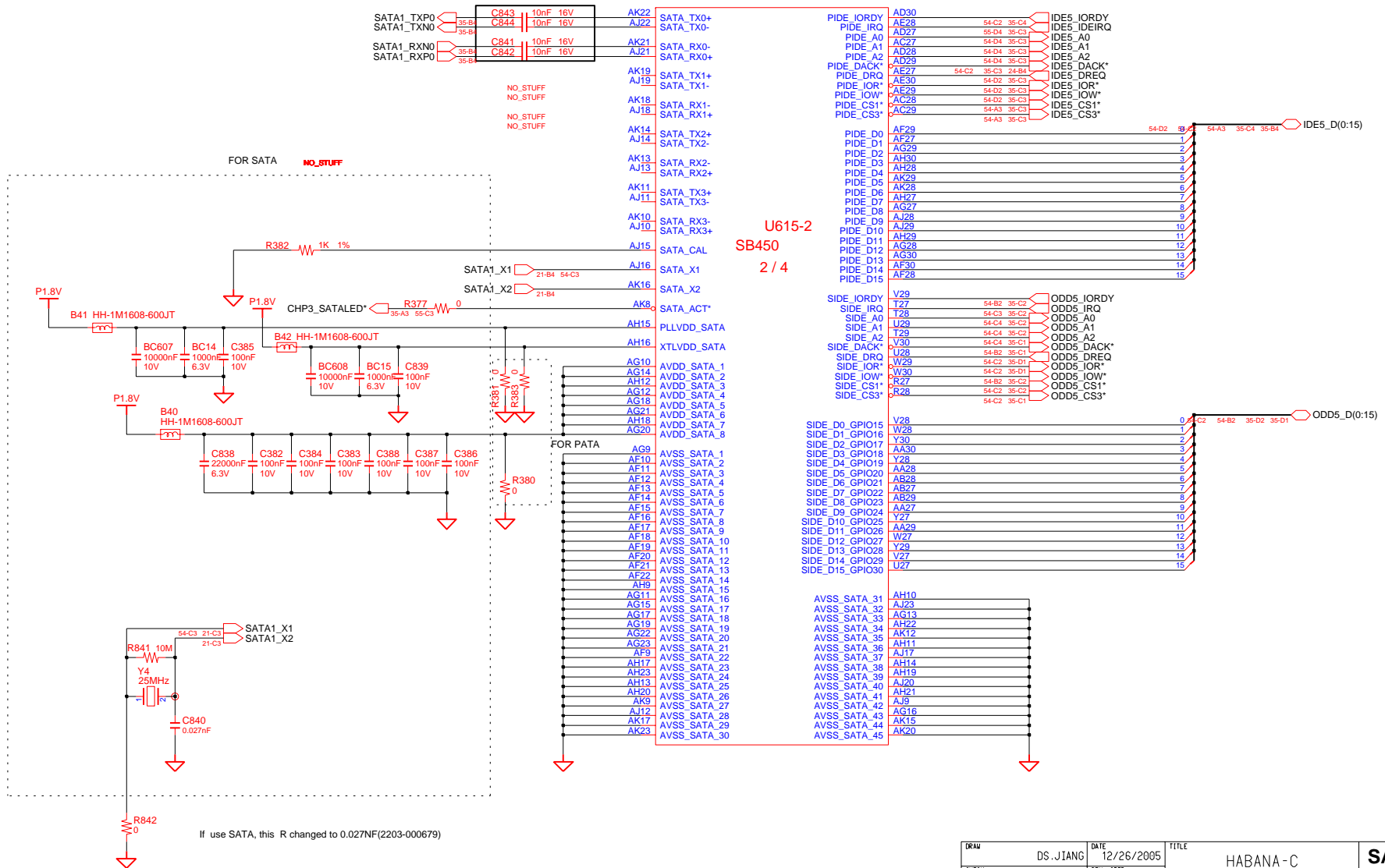
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CHECK	DJ.XU	DEV. STEP	PRR			
APPROVAL	KEVIN.LEE	REV	1.0			
MODULE CODE		LAST EDIT	December 26, 2005 2:59:06 PM	PAGE 19 OF 55		



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DRAW	DS.JIANG	DATE	12/26/2005	TITLE	HABANA-C MAIN	SAMSUNG ELECTRONICS	
CHECK	DJ.XU	DEV. STEP	PRR	REV	SB450(1/4)		PART NO. BA41-00615A
APPROVAL	KEVIN.LEE	REV	1.0	LAST EDIT	December 26, 2005 2:59:06 PM		PAGE 20 OF 55

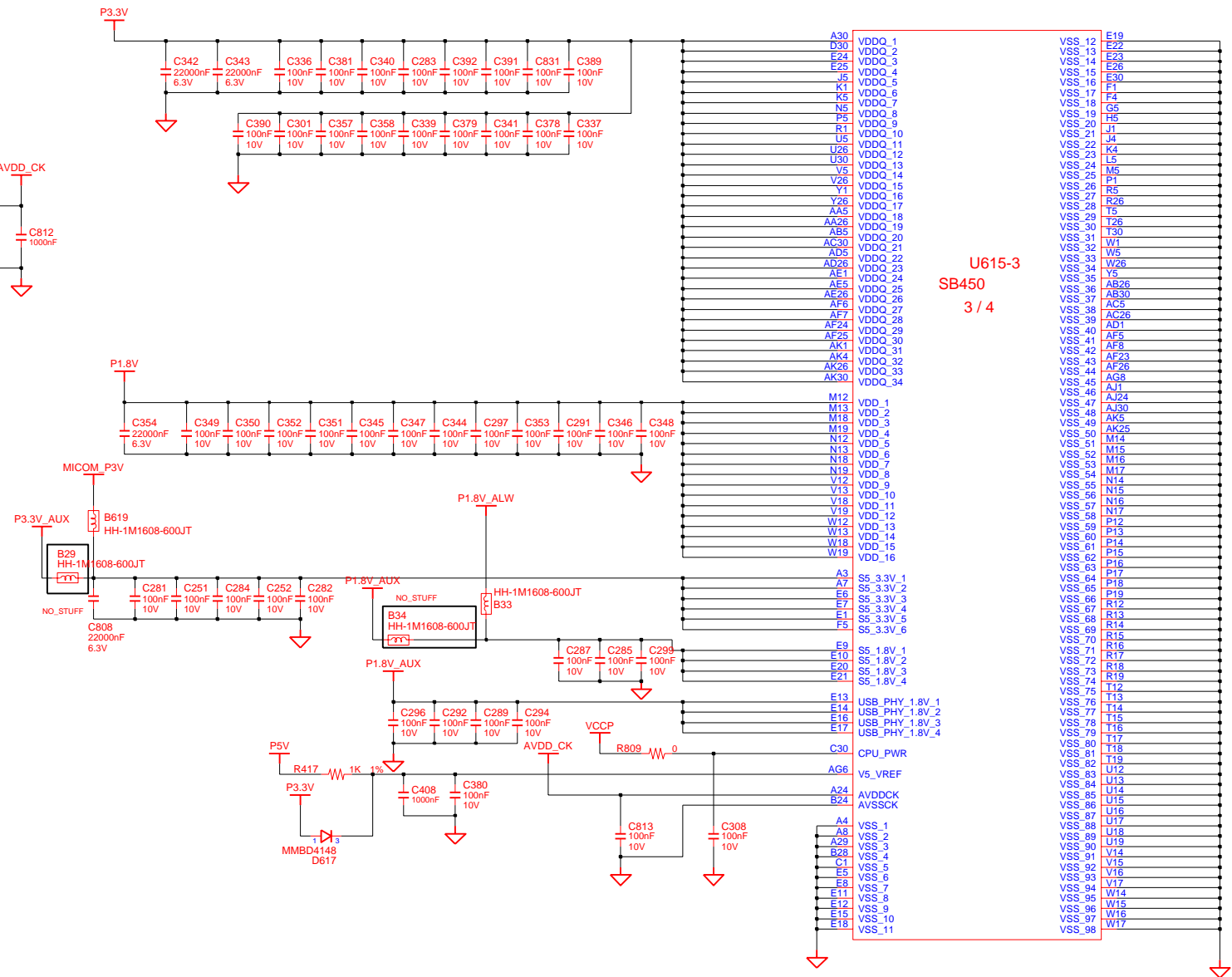
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DRAW	DS.JIANG	DATE	12/26/2005	TITLE	HABANA-C POWER SB450(2/4)	SAMSUNG ELECTRONICS PART NO. BA41-00615A
CHECK	DJ.XU	DEV. STEP	PRR			
APPROVAL	KEVIN.LEE	REV	1.0			
MODULE CODE		LAST EDIT				
			December 26, 2005 2:59:06 PM	PAGE	21	OF 55

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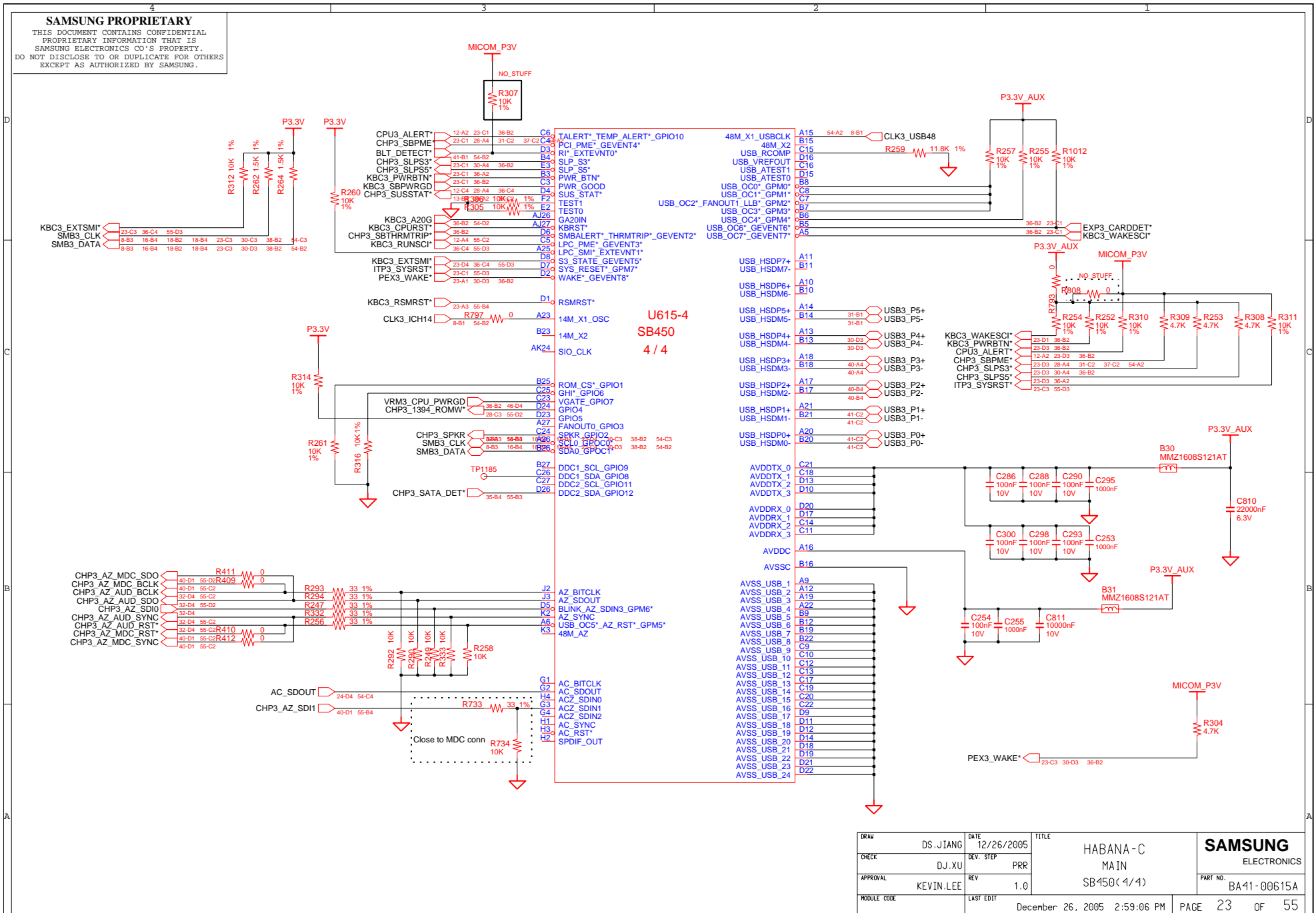


U615-3
SB450
3/4

DRAW	DS.JIANG	DATE	12/26/2005	TITLE	HABANA-C MAIN SB450(3/4)	SAMSUNG ELECTRONICS PART NO. BA41-00615A
CHECK	DJ.XU	DEV. STEP	PRR			
APPROVAL	KEVIN.LEE	REV	1.0			
MODULE CODE		LAST EDIT				
December 26, 2005 2:59:06 PM					PAGE	22 OF 55

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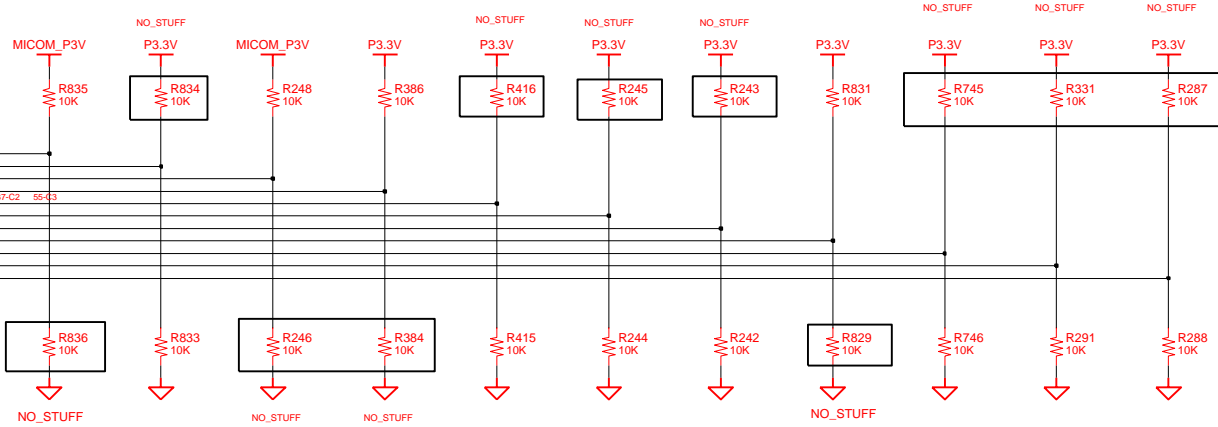
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CHECK	DJ.XU	DEV. STEP	PRR			
APPROVAL	KEVIN.LEE	REV	1.0			
MODULE CODE		LAST EDIT	December 26, 2005 2:59:06 PM	PAGE	23 OF 55	

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REQUIRED SYSTE STRAPS

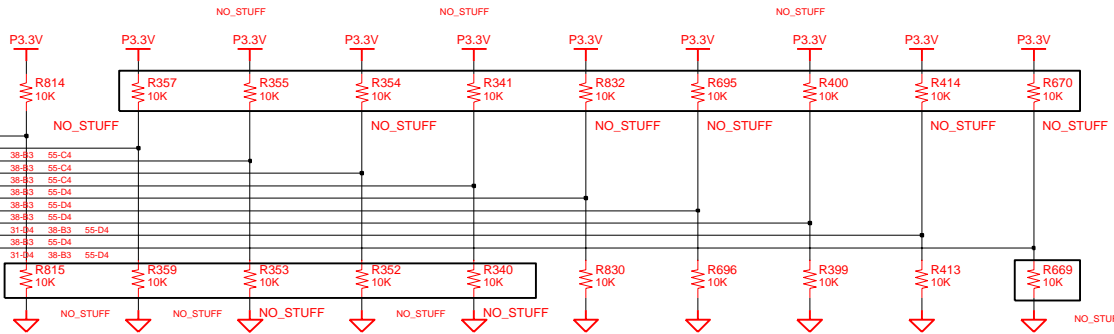
- AUTO_ON* 20-A2 54-C4
- AC_SDOUT 23-B4 54-C4
- RTC_CLK 20-A2 54-C4
- LPC3_LFRAME* 20-A2 25-A3 25-B4 25-C3 36-C2 37-C2 55-43
- CLK3_PCLKCB 20-D2 29-A4 54-D1
- CLK3_PCLKSIO_DS 20-D2 37-C2 55-D2
- CLK3_PCLKSIO 20-D2 37-C2 55-B4
- CLK3_PCLKFWH 20-D2 25-B4 25-C4 55-B4
- CLK3_PCLKMICOM 20-D2 36-C2 55-B3
- CLK3_DBGLPC 20-D2 25-A3 54-D1
- PCI3_CLK8 20-D2 54-B2



	AUTO_ON	AC_SDOUT	RTC_CLK	LPC3_FRAME	PCI3_CLK2	PCI3_CLK3	PCI3_CLK4	PCI3_CLK5	PCI3_CLK6	PCI3_CLK7, PCI3_CLK8
STRAP HIGH	MANUAL PWR ON	USE DEBUG STRAPS	INTERNAL RTC	Enable thermtrip* on power up	48MHZ OSC MODE	USB PHY PWRDOWN DISABLE	USE USB PLL	PCI-E lane auto detect	CPU I/F = KB	ROM TYPE H.H = PCI ROM L.L = LPCROM I LPC ADDRESS MAPPED BELOW 1 M LPC ADDRESS MAPPED TO TOP 4G L.H = LPC ROM II L.L = FWH ROM
STRAP LOW	AUTO PWR ON	IGNORE DEBUG STRAPS	EXRERNAL RTC	Disable thermtrip* on power up	48MHZ XTAL MODE	USB PHY PWRDOWN ENABLE	BYPASS USB PLL	Force PCI-E to lane2	CPU I/F = P4	

DEBUS STRAPS

- IDE5_DACK* 21-D2 35-C3 54-C2
- PCI3_AD(31) 20-D2 28-C4 31-D4 38-43 55-C4
- PCI3_AD(30) 20-D2 28-C4 31-D4 38-43 55-C4
- PCI3_AD(29) 20-D2 28-C4 31-D4 38-43 55-C4
- PCI3_AD(28) 20-D2 28-C4 31-D4 38-43 55-C4
- PCI3_AD(27) 20-D2 28-C4 31-D4 38-43 55-D4
- PCI3_AD(26) 20-D2 28-C4 31-D4 38-43 55-D4
- PCI3_AD(25) 20-D2 28-C4 31-D4 38-43 55-D4
- PCI3_AD(24) 20-D2 28-B4 28-C4 31-D4 38-83 55-D4
- PCI3_AD(23) 20-D2 28-C4 31-D4 38-43 55-D4

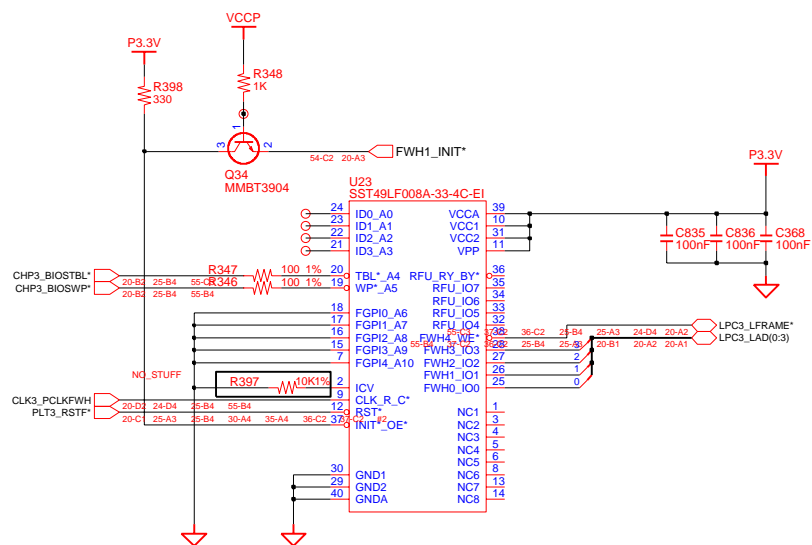


	IDE5_DACK*	PCI3_AD(31)	PCI3_AD(30)	PCI3_AD(29)	PCI3_AD(28)	PCI3_AD(27)	PCI3_AD(26)	PCI3_AD(25)	PCI3_AD(24)	PCI3_AD(23)
STRAP HIGH	USE LONG RESET	RESERVED	RESERVED	RESERVED	RESERVED	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	BYPASS EEPROM PCIE STRAPS	RESERVED
STRAP LOW	USE SHORT RESET					USE PCI PLL	USE ACPI BCLK	USE IDE PLL	USE DEFAULT PCIE STRAPS	

DRAW	DS.JIANG	DATE	12/26/2005	TITLE	HABANA-C STRAPS	SAMSUNG ELECTRONICS PART NO. BA41-00615A
CHECK	DJ.XU	DEV. STEP	PRR			
APPROVAL	KEVIN.LEE	REV	1.0			
MODULE CODE		LAST EDIT	December 26, 2005 2:59:06 PM			
PAGE 24 OF 55						

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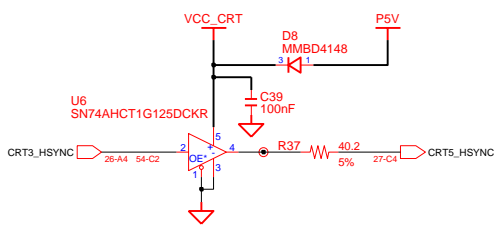
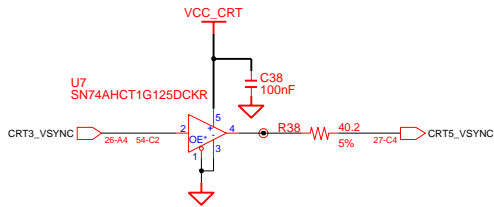
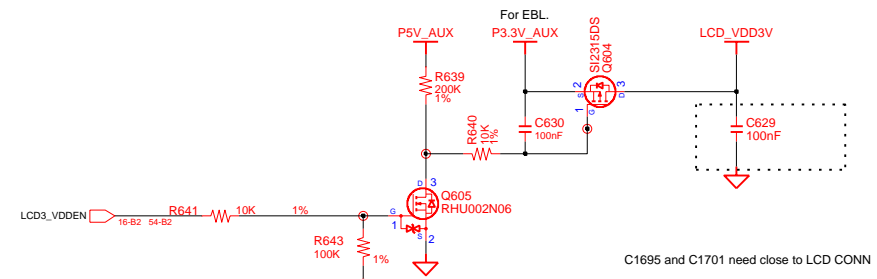
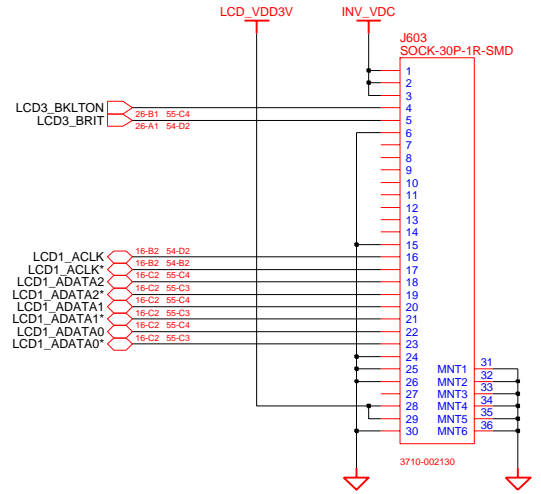


02	VERIFY REAL MODE	66	CONFIGURE ADVANCE CACHE REG.
03	DISABLE NMI	6A	DISPLAY EXTERNAL CACHE SIZE
04	GET CPU TYPE	6C	DISPLAY SHADOW MESSAGE
06	INIT. SYSTEM H/W	6E	DISPLAY NON-DISPOSABLE SEGMENT
08	INIT. CHIPSET REG.	70	DISPLAY ERROR MESSAGE
09	SET IN POST FLAG	72	CHECK FOR CONFIGURATION ERROR
0A	INIT CPU.REG	74	TEST REAL-TIME CLOCK
0B	CPU CACHE ON	76	CHECK FOR KEYBOARD ERROR
0C	INIT.CACHE TO POST	7C	SETUP HARDWARE INTERRUPT VECTOR
0E	INIT. I/O VALUE	7E	TEST COPROCESSER IF PRESENT
0F	ENABLE THE L-BUS IDE	80	DISABLE ON-BOARD I/O PORT
10	INIT. POWER MANAGER	82	DETECT AND INSTALL EXT.RS232C
11	LOAD ALTERNATE REG.	84	DETECT AND INSTALL EXT.PARALLEL
13	PCI BUS MASTER RESET WITH INITIAL POST VALUE	86	RE-INIT. ON-BOARD I/O PORT
14	INIT. KEYBOARD CONTROLLER	88	INIT. BIOS DATA ROM
16	CHECK CHECKSUM	8A	INIT.EXTENDED BIOS DATA AREA
18	8254 TIMER INIT.	8C	INIT. FDD CONTROLLER
1A	8237 DMA CONTROLLER INIT.	9A	SHADOW OPTION ROMS
1C	RESET INTERRUPT CONTROLLER	9C	SETUP POWER MANAGEMENT
20	TEST DRAM REFRESH	9E	ENABLE H/W INTERRUPT
22	TEST 8742 KEYBOARD CONTROLLER	A0	SET TIME OF DAY
24	SET ES SEGMENT REG. TO 4GB	A4	INIT. TYPOMATIC RATE
26	ENABLE A20	A8	ERASE F2 PROMPT
28	AUTO SIZING DRAM	AA	SCAN FOR F2 KEY STROKE
32	COMPUTE THE CPU SPEED	AC	ENTER SETUP
34	TESET CMOS RAM	AE	CLEAR IN POST FLAG
38	SHADOW SYSTEM BIOS ROM	B0	CHECK FOR ERRORS
3A	AUTO SIZING CACHE	B2	POST DONE-PREPARE TO BOOT O/S
3C	CONFIGURE ADVANCED CHIPSET REG.	B4	ONE BEEP
3D	LOAD ALTER REG. WITH CMOS VALUE	B6	CHECK PASSWORD (OPTION)
42	INIT. INTERRUPT VECTOR	B7	ACPI INIT
44	INIT. BIOS INTERRUPT	BA	DMI INIT
46	CHECK ROM COPYRIGHT NOTICE	BE	CLEAR SCREEN
47	INIT. I20 SUPPORT IF INSTALLED	C0	TRY BOOT WITH INT19
48	CHECK VIDEO CONFIGURE AGAINST CMOS	D0	INTERRUPT HANDLER ERROR
49	INIT. PCI BUS AND DEVICE	D2	UNKNOWN INTERRUPT ERROR
4A	INIT. ALL VIDEO BIOS ROM	D4	PENDING INTERRUPT ERROR
4C	SHADOW VIDEO BIOS ROM	D6	SHUTDOWN 5
50	DISPLAY CPU TYPE AND SPEED	D8	SHUTDOWN ERROR
52	TEST KEYBOARD	DA	EXTENDED BLOCK MOVE
54	SET KEYCLICK IF ENABLED	DC	SHUTDOWN 10
56	ENABLE KEYBOARD	89	ENABLE NMI
58	TEST FOR UNEXPECTED INTERRUPTS	90	INIT. HDD CONTROLLER
5A	DISPLAY " PRESS SETUP"	91	INIT. LOCAL BUS HDD CONTROLLER
5C	TEST RAM BETWEEN 512K AND 640K	92	JUMP TO USER PATCH 2
60	TEST EXTENDED MEMORY	94	DISABLE A20 ADDRESS LINE
62	TEST EXTENDED MEMORY ADDRESS LINE	96	CLEAR HUGE ES SEGMENT REG.
64	JUMP TO USER PATCH 1	98	SEARCH FOR OPTION ROMS

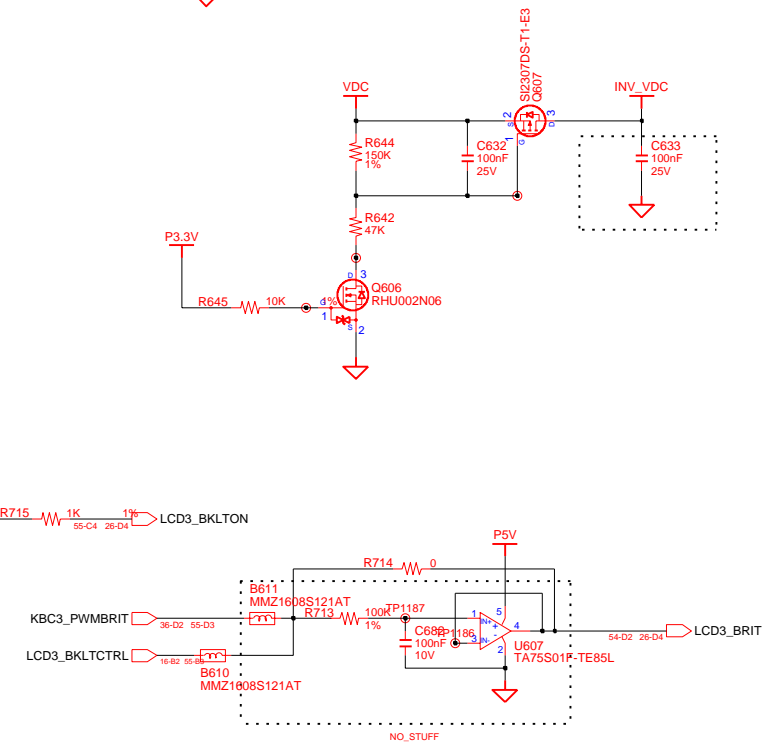
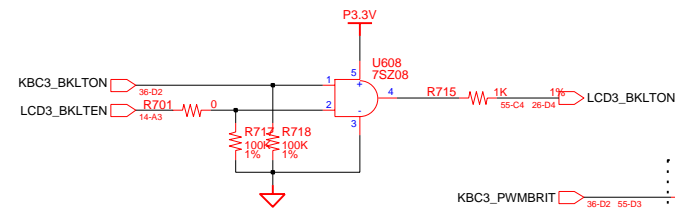
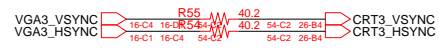
DRAW	DS.JIANG	DATE	12/26/2005	TITLE	HABANA-C	SAMSUNG ELECTRONICS
CHECK	DJ.XU	DEV. STEP	PRR		MAIN	
APPROVAL	KEVIN.LEE	REV	1.0		FIRMWARE HUB	PART NO. BA41-00615A
MODULE CODE		LAST EDIT	December 26, 2005 2:59:06 PM	PAGE	25	OF 55

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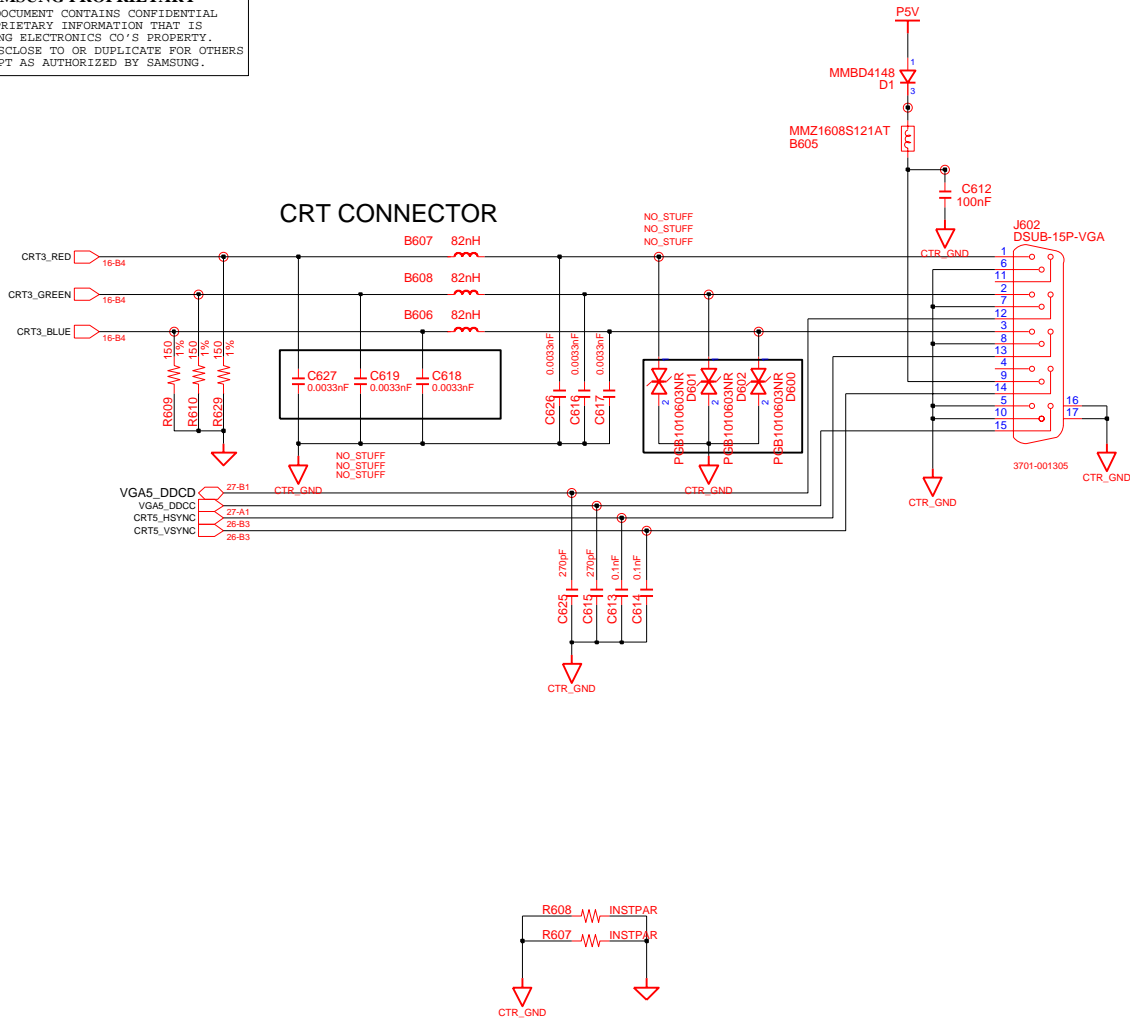
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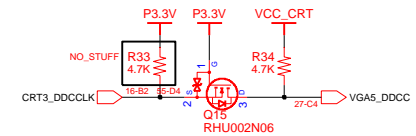
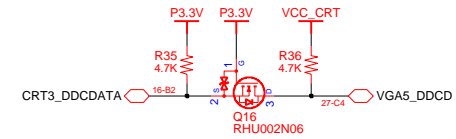
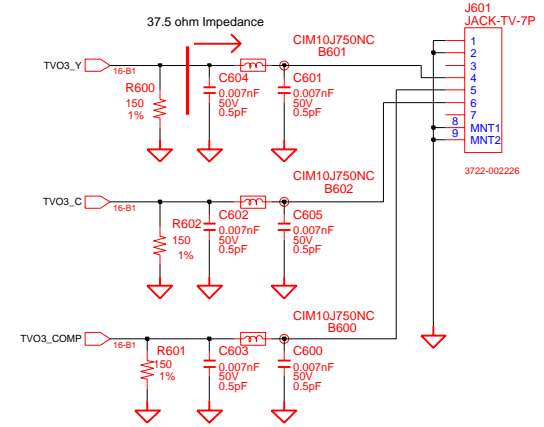
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CHECK	DJ.XU	DEV. STEP	PRR	LCD Connector & SPREAD SPECTRUM		
APPROVAL	KEVIN.LEE	REV	1.0			PART NO. BA41-00615A
MODULE CODE		LAST EDIT	December 26, 2005 2:59:06 PM	PAGE	26	OF 55

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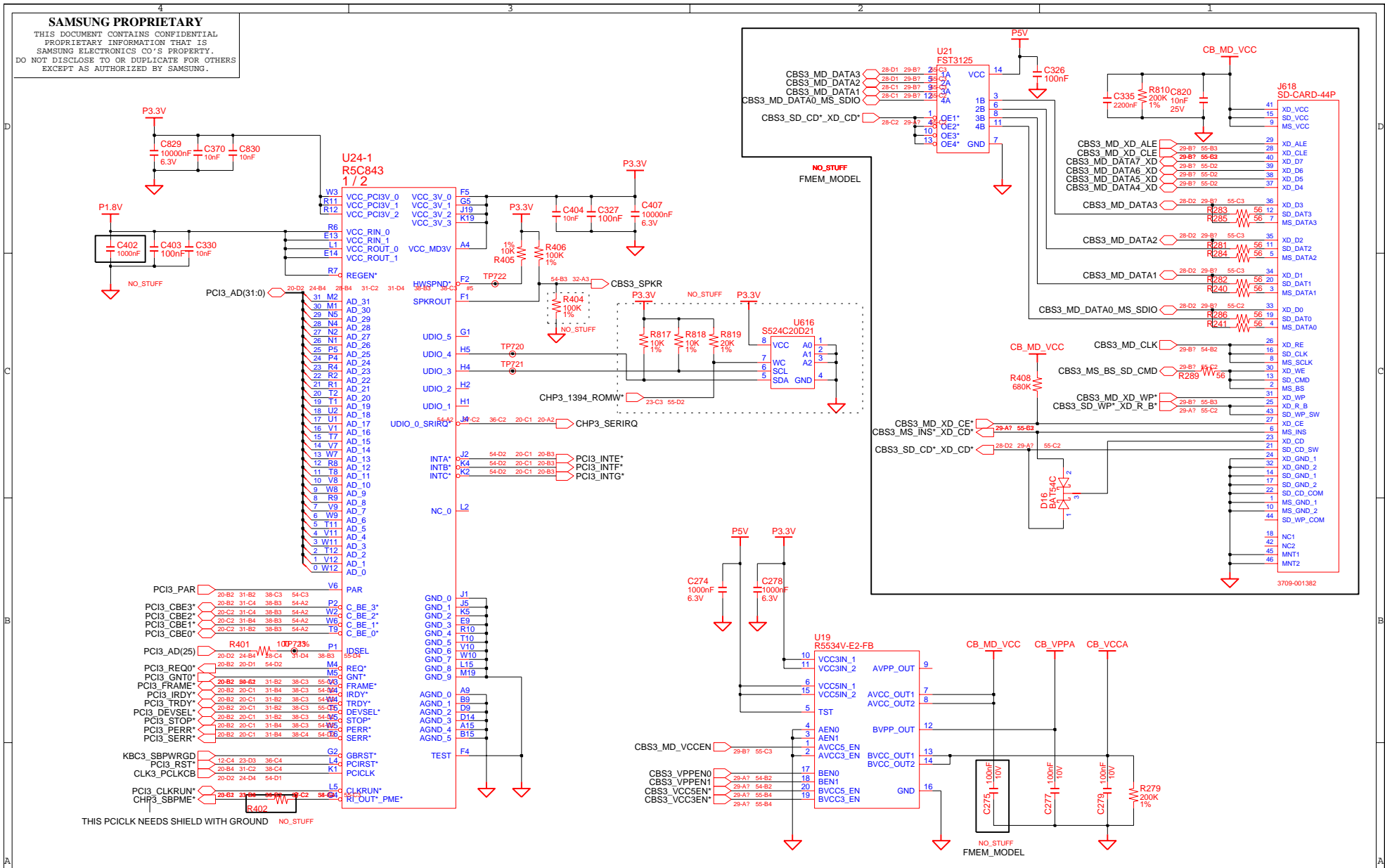
TV-OUT(S-VHS,COMPONENT)



DRAW	DS.JIANG	DATE	12/26/2005	TITLE	HABANA-C	SAMSUNG ELECTRONICS
CHECK	DJ.XU	DEV. STEP	PRR			
APPROVAL	KEVIN.LEE	REV	1.0		CRT AND TV-OUT	PART NO. BA41-00615A
MODULE CODE		LAST EDIT	December 26, 2005 2:59:06 PM	PAGE	27	OF 55

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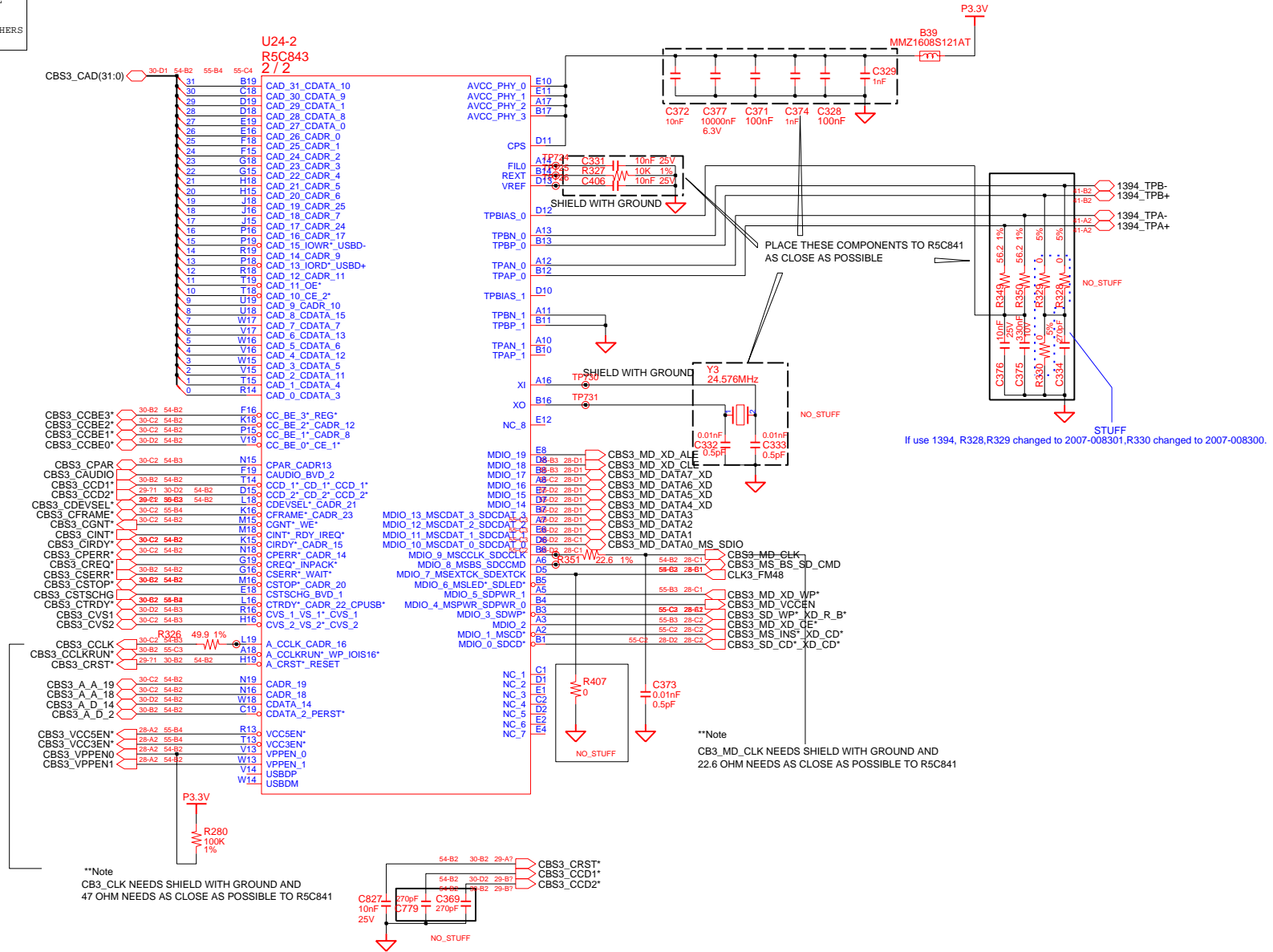
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DRAW	DS.JIANG	DATE	12/26/2005	TITLE	HABANA-C MAIN	SAMSUNG ELECTRONICS
CHECK	DJ.XU	DEV. STEP	PRR	REV	CARDBUS / 1394	
APPROVAL	KEVIN.LEE	REV	1.0	LAST EDIT	December 26, 2005 2:59:06 PM	PART NO. BA41-00615A
MODULE CODE					December 26, 2005 2:59:06 PM	PAGE 28 OF 55

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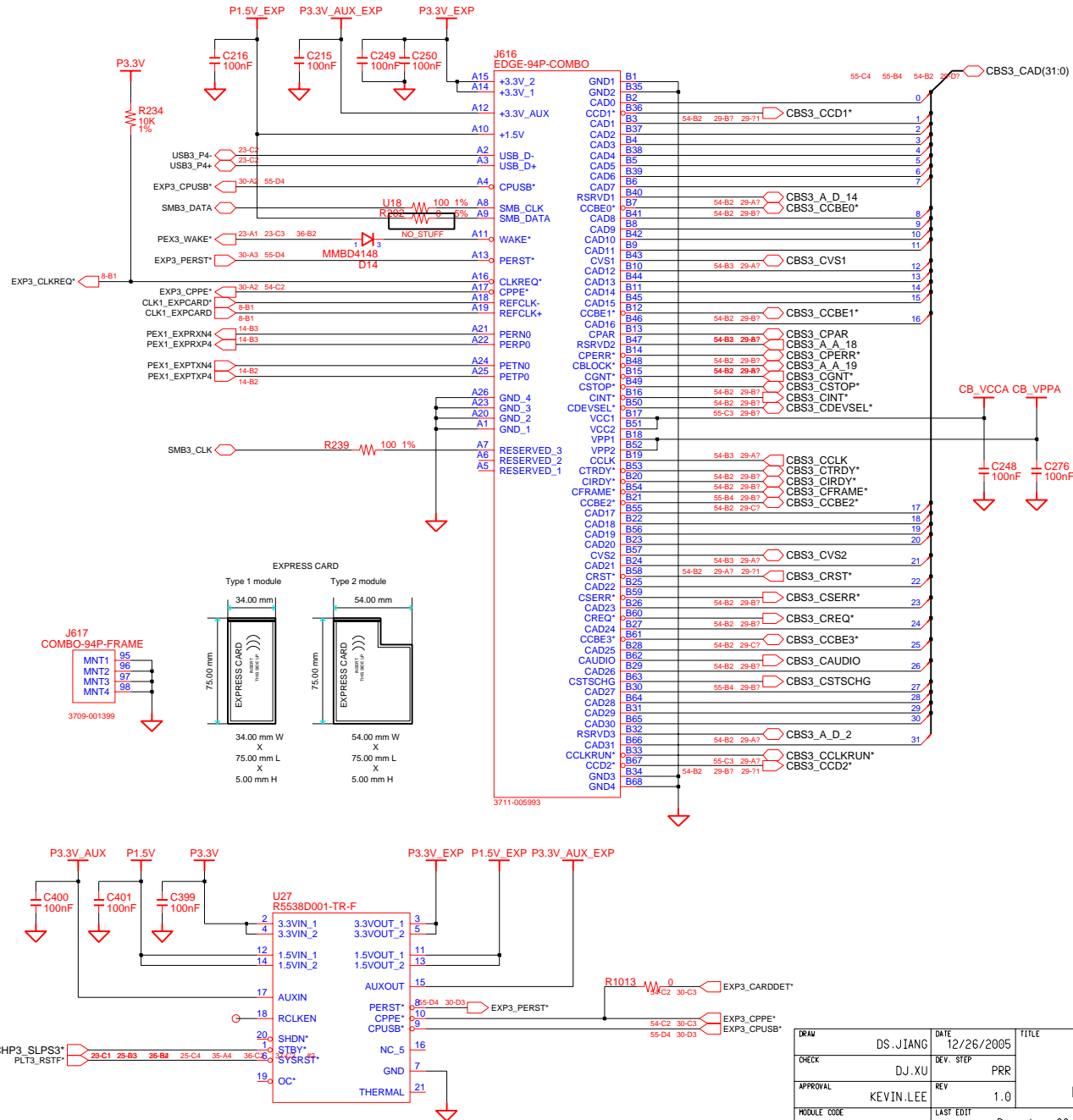
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DRAW	DS.JIANG	DATE	12/26/2005	TITLE	HABANA-C POWER CARD BUSS(2/2)	SAMSUNG ELECTRONICS PART NO. BA41-00615A
CHECK	DJ.XU	DEV. STEP	PRR			
APPROVAL	KEVIN.LEE	REV	1.0			
MODULE CODE		LAST EDIT	December 26, 2005 2:59:06 PM	PAGE	29 OF 55	

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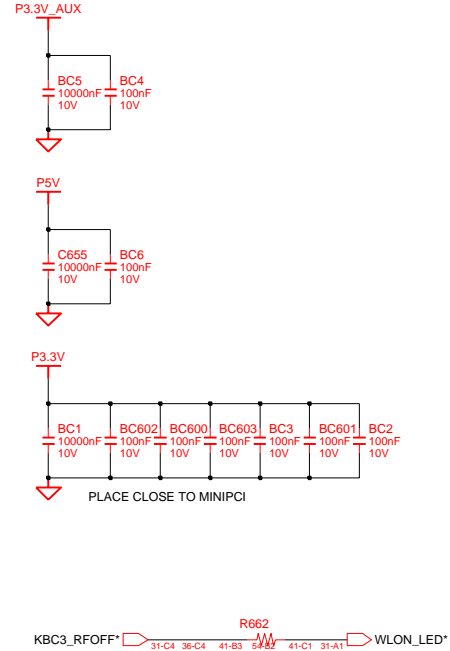
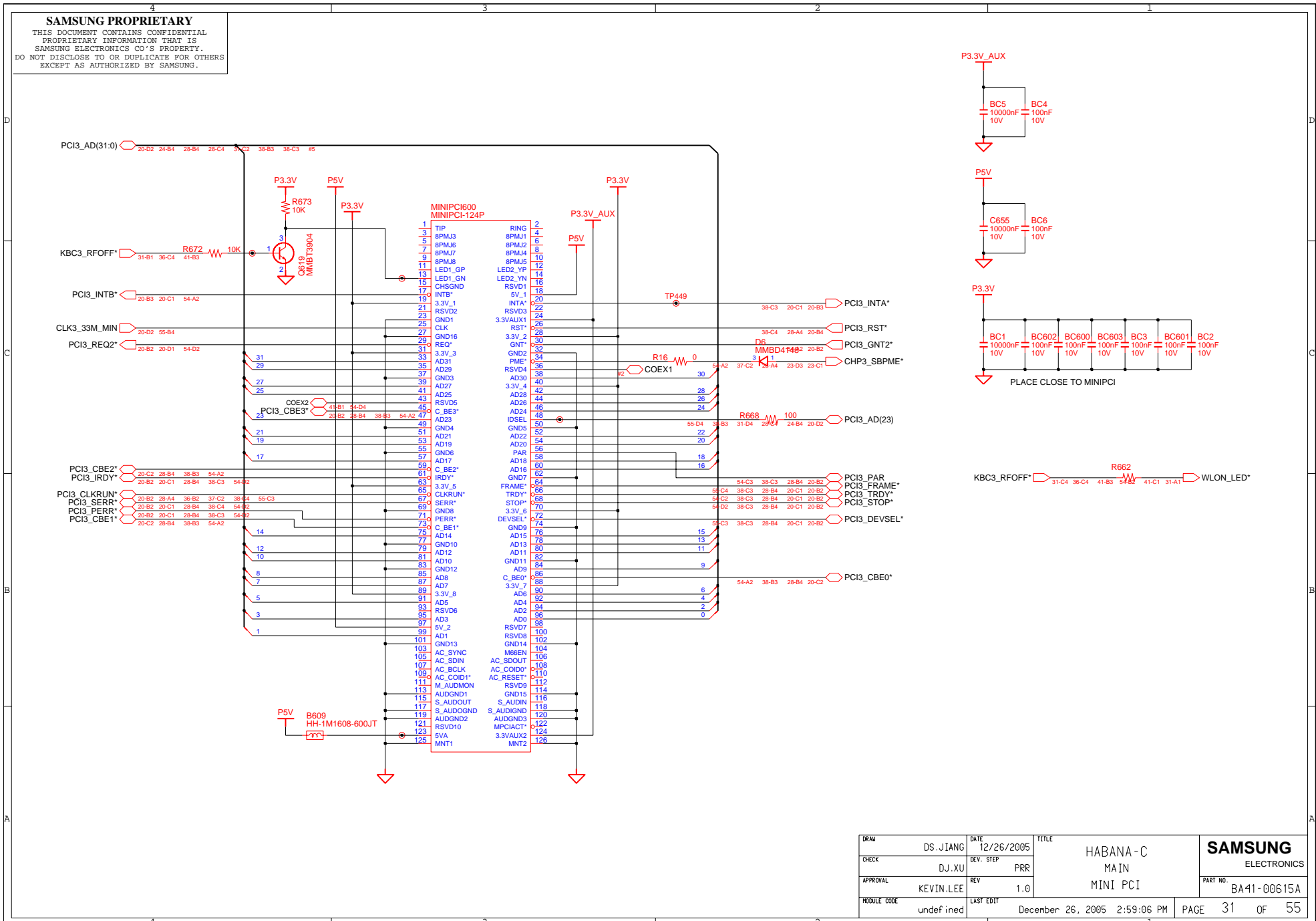
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DRAW	DS.JIANG	DATE	12/26/2005	TITLE	HABANA-C	SAMSUNG ELECTRONICS
CHECK	DJ.XU	DEV. STEP	PRR	REV	EXPRESS CARD	
APPROVAL	KEVIN.LEE	REV	1.0	LAST EDIT	December 26, 2005 2:59:06 PM	PAGE 30 OF 55

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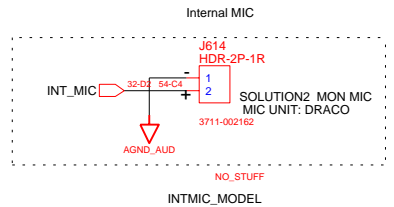
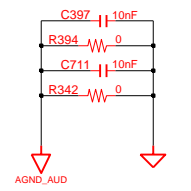
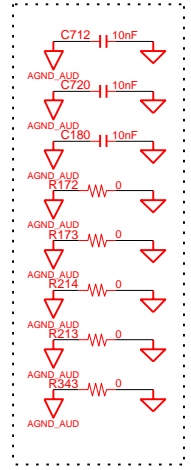
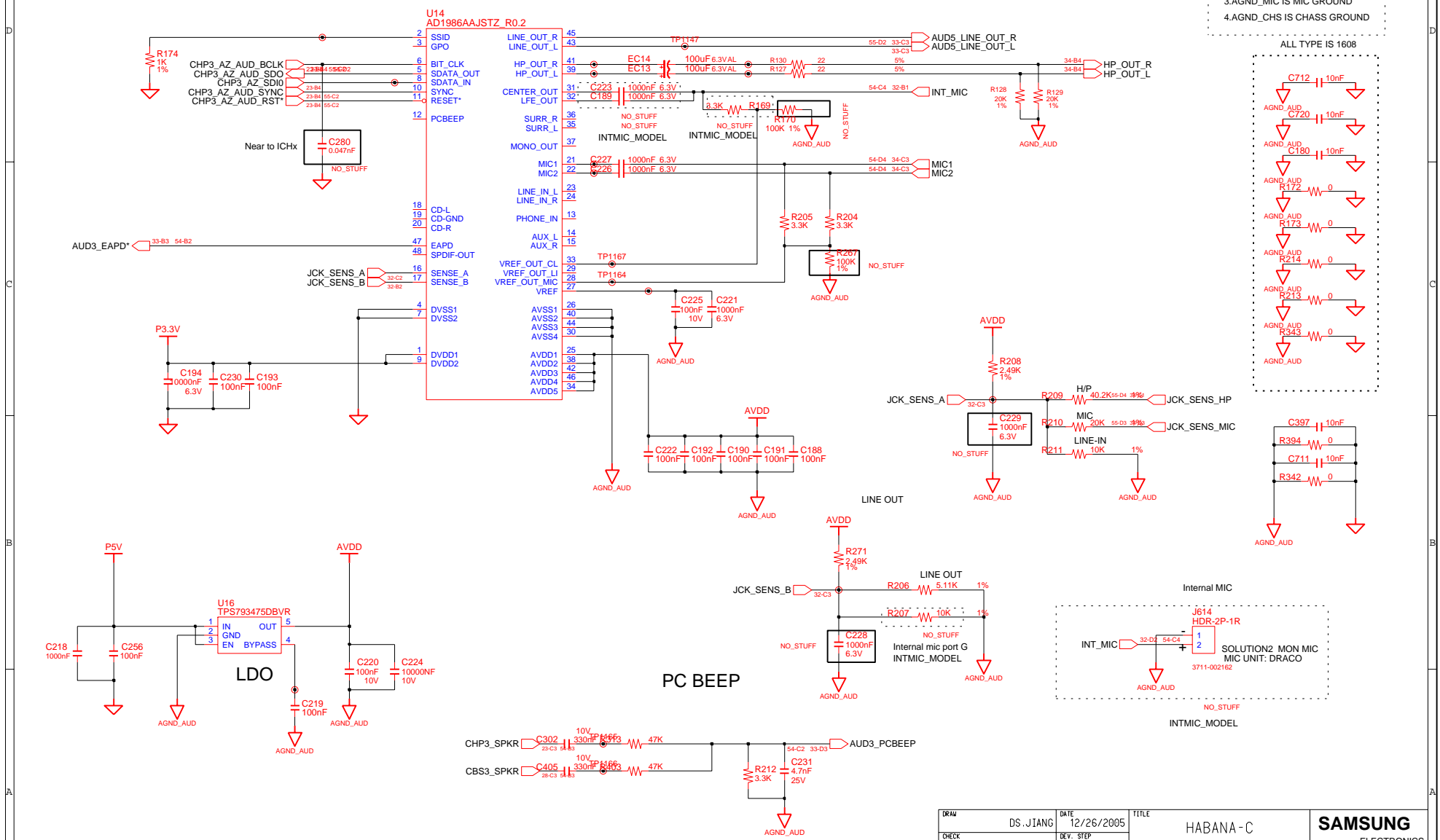
DRAW	DS.JIANG	DATE	12/26/2005	TITLE	HABANA-C MAIN MINI PCI	SAMSUNG ELECTRONICS
CHECK	DJ.XU	DEV. STEP	PRR			
APPROVAL	KEVIN.LEE	REV	1.0			
MODULE CODE	undef:ined	LAST EDIT	December 26, 2005 2:59:06 PM	PAGE 31 OF 55		

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- 1. AGND_AUD IS AUDIO GROUND
- 2. GND IS DIGITAL GROUND
- 3. AGND_MIC IS MIC GROUND
- 4. AGND_CHS IS CHASSIS GROUND

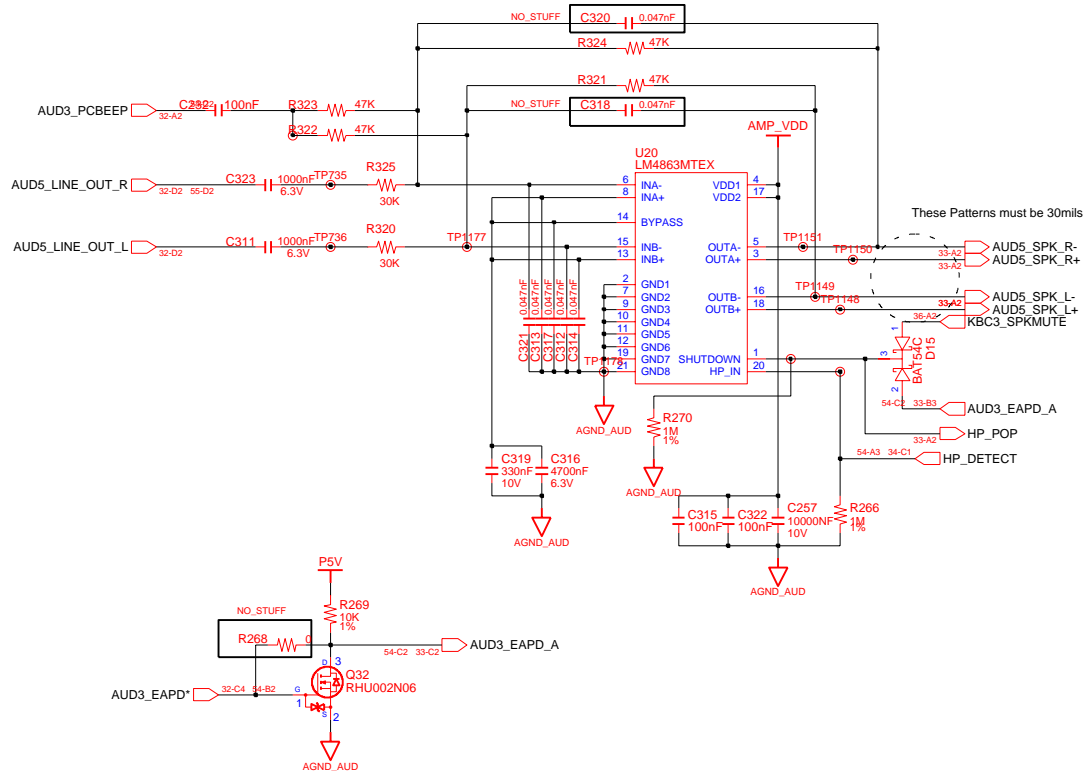
ALL TYPE IS 1608



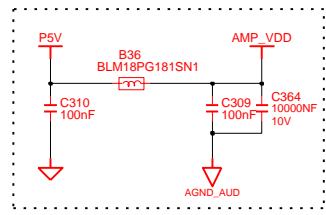
DRAW	DS.JIANG	DATE	12/26/2005	TITLE	HABANA-C	SAMSUNG ELECTRONICS
CHECK	DJ.XU	DEV. STEP	PRR	MAIN		
APPROVAL	KEVIN.LEE	REV	1.0	AUDIO CODEC		PART NO. BA41-00615A
MODULE CODE	undefined	LAST EDIT	December 26, 2005 2:59:06 PM		PAGE	32 OF 55

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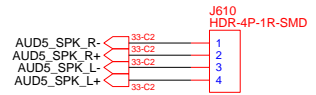
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AMP_VDD



INTERNAL STEREO SPEAKERS



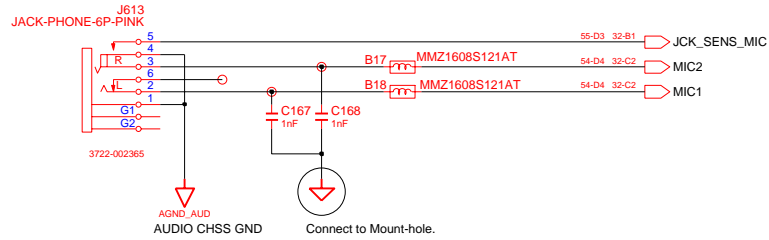
Should be written sign "L", "R" on the PCB

DRAW	DS.JIANG	DATE	12/26/2005	TITLE	HABANA-C MAIN LIMITER & AMP	SAMSUNG ELECTRONICS
CHECK	DJ.XU	DEV. STEP	PRR			
APPROVAL	KEVIN.LEE	REV	1.0			
MODULE CODE	undef:ined	LAST EDIT	December 26, 2005 2:59:06 PM	PAGE 33 OF 55		
					PART NO.	BA41-00615A

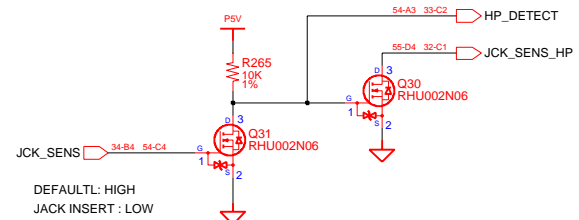
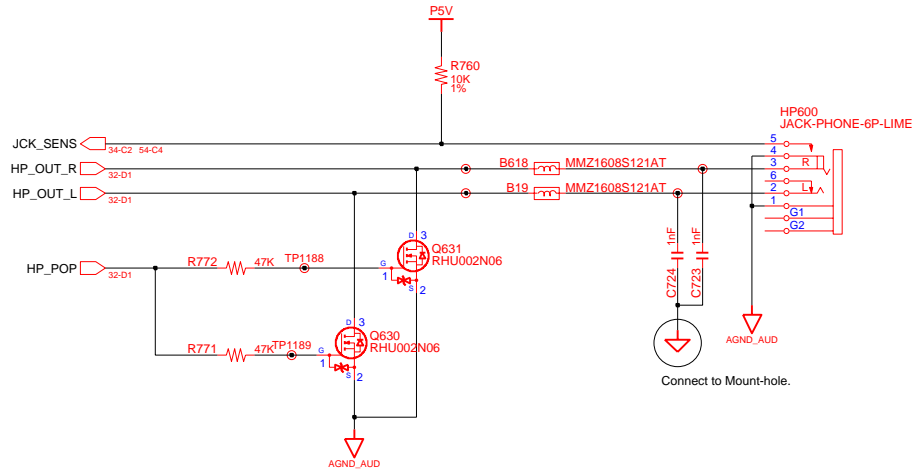
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MIC JACK



HEADPHONE



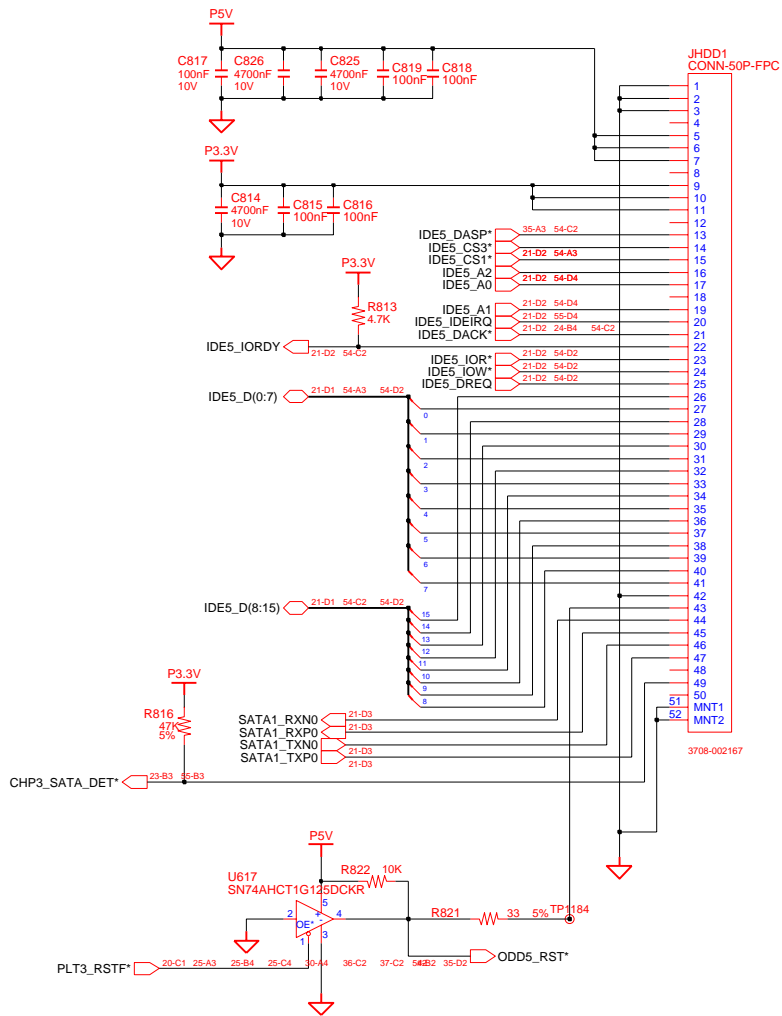
The traces led to Audio Jacks have the width over 10mil

DRAW	DS.JIANG	DATE	12/26/2005	TITLE	HABANA-C MAIN UPPER & AUDIO CONN	SAMSUNG ELECTRONICS PART NO. BA41-00615A
CHECK	DJ.XU	DEV. STEP	PRR			
APPROVAL	KEVIN.LEE	REV	1.0			
MODULE CODE	undefined	LAST EDIT	December 26, 2005 2:59:06 PM	PAGE 34 OF 55		

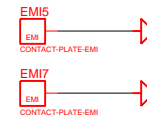
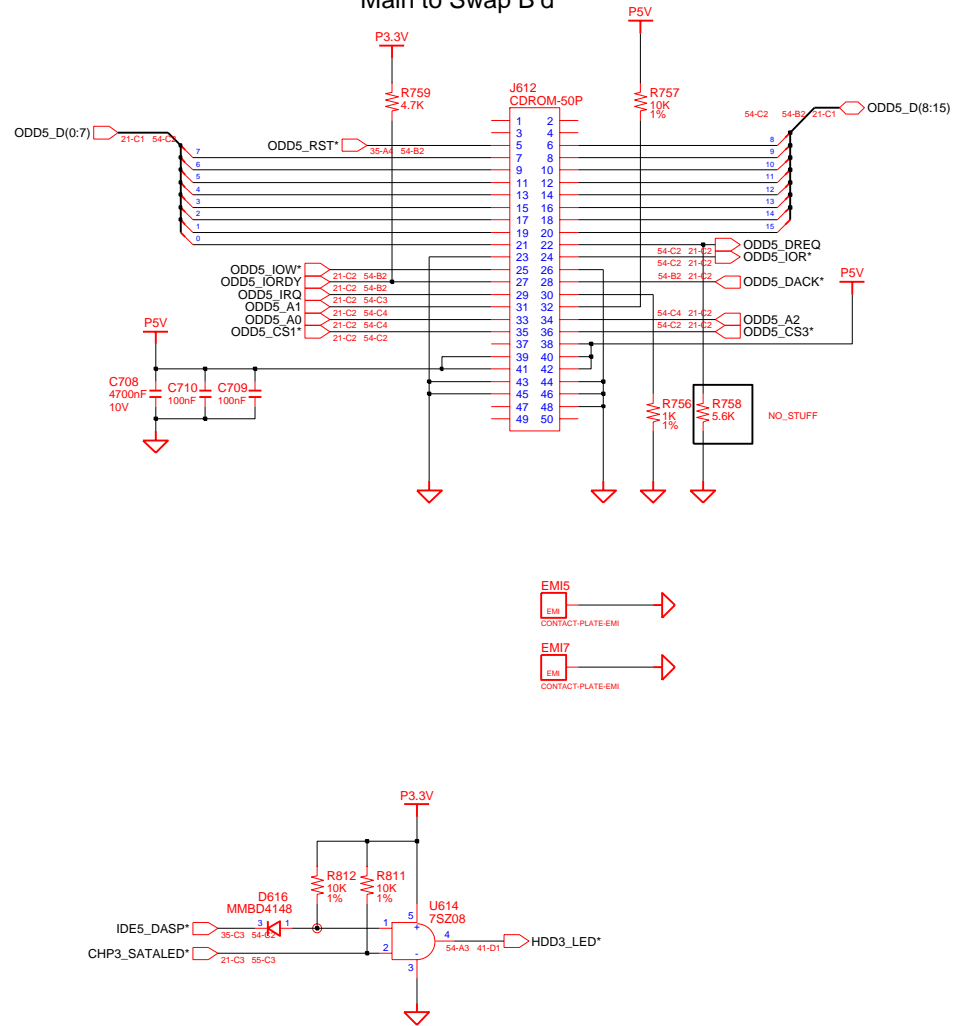
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Main to HDD



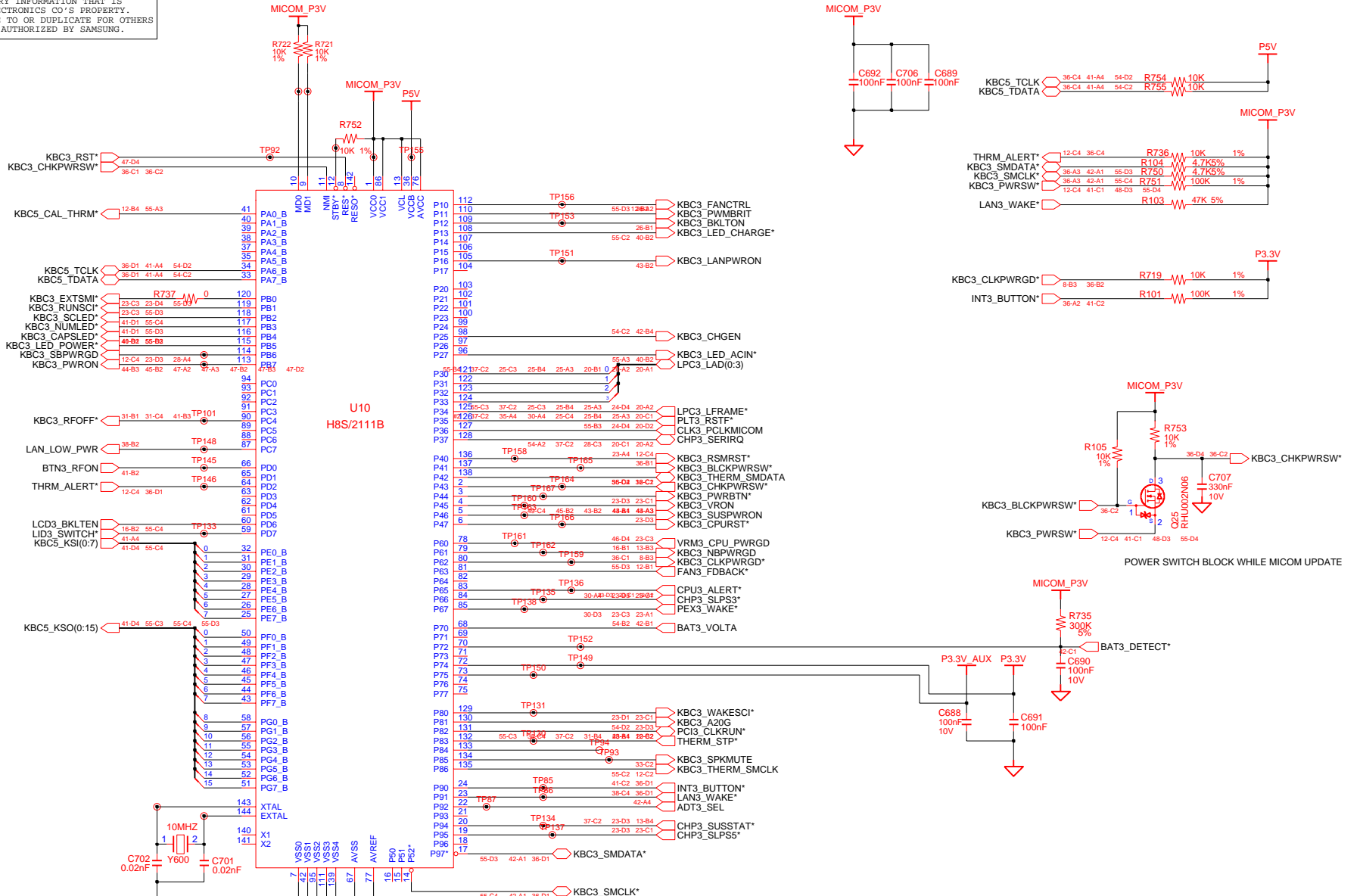
Main to Swap B'd



DRAW	DS.JIANG	DATE	12/26/2005	TITLE	HABANA-C POWER HDD & ODD	SAMSUNG ELECTRONICS PART NO. BA41-00615A
CHECK	DJ.XU	DEV. STEP	PRR			
APPROVAL	KEVIN.LEE	REV	1.0			
MODULE CODE	undefined	LAST EDIT	December 26, 2005 2:59:06 PM	PAGE	35 OF 55	

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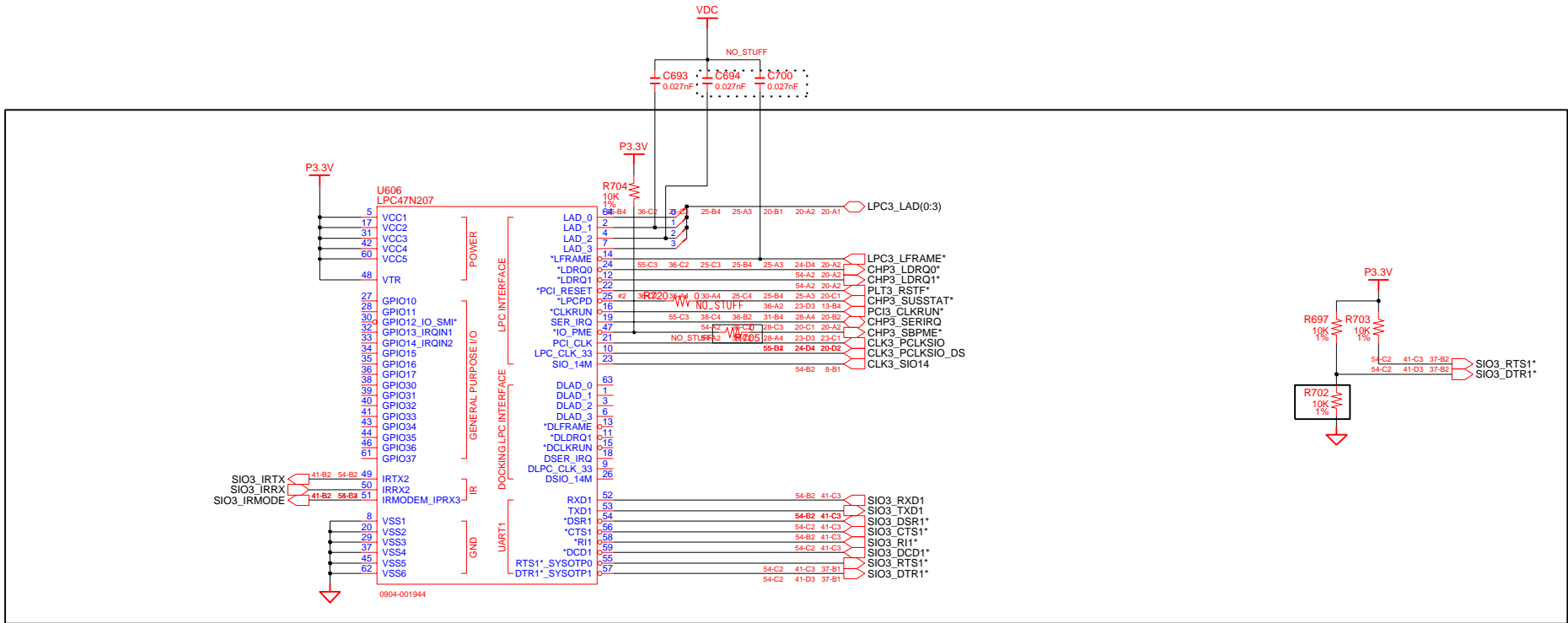
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DRAW	DS.JIANG	DATE	12/26/2005	TITLE	HABANA-C POWER MICOM	SAMSUNG ELECTRONICS PART NO. BA41-00615A
CHECK	DJ.XU	DEV. STEP	PRR			
APPROVAL	KEVIN.LEE	REV	1.0			
MODULE CODE	undefined	LAST EDIT	December 26, 2005 2:59:06 PM	PAGE	36 OF 55	

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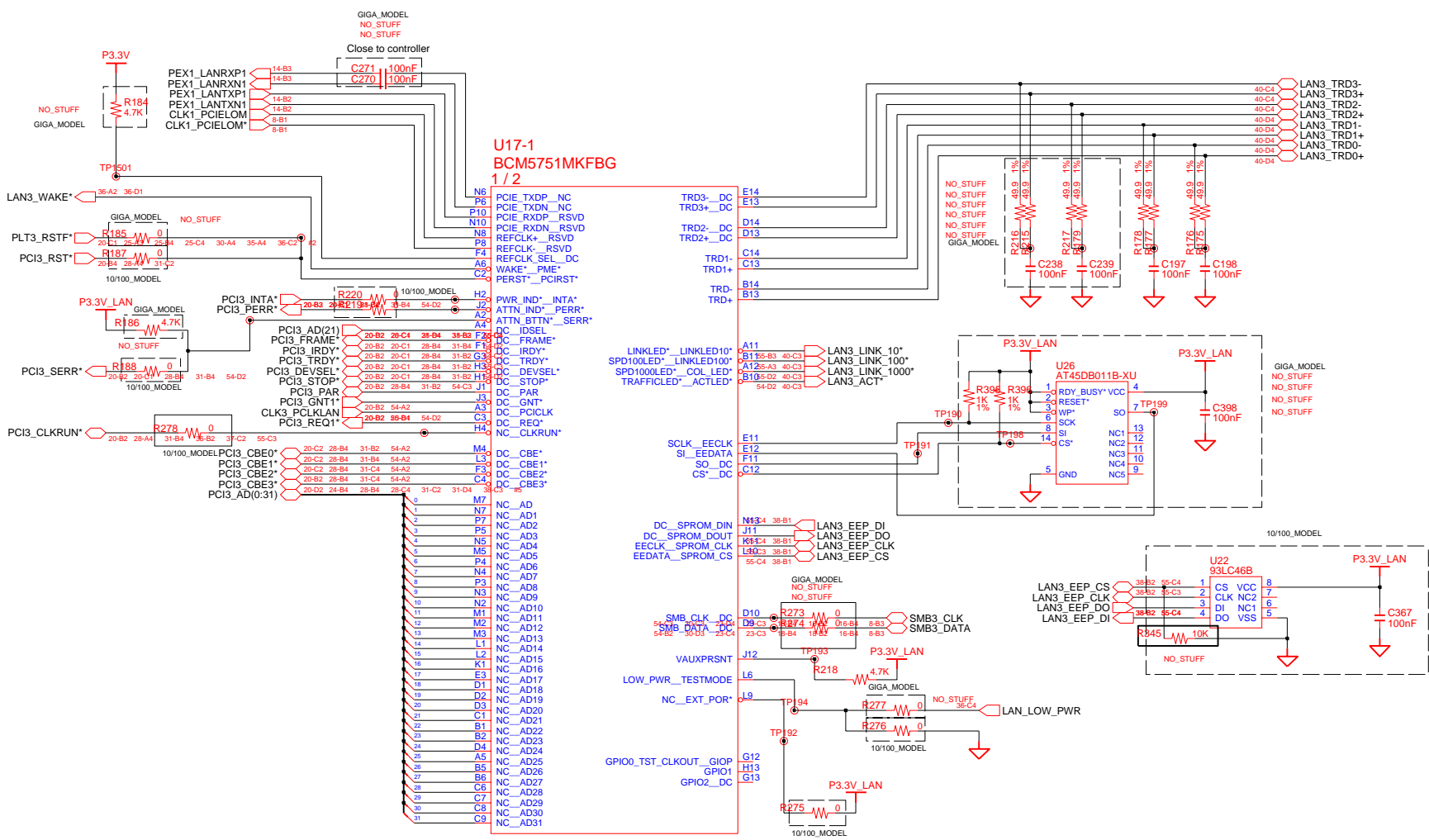


NO_STUFF

DRAW	DS.JIANG	DATE	12/26/2005	TITLE	HABANA-C MAIN LPC	SAMSUNG ELECTRONICS
CHECK	DJ.XU	DEV. STEP	PRR			
APPROVAL	KEVIN.LEE	REV	1.0			
MODULE CODE	undefined	LAST EDIT	December 26, 2005 2:59:06 PM	PAGE 37 OF 55		
					PART NO.	BA41-00615A

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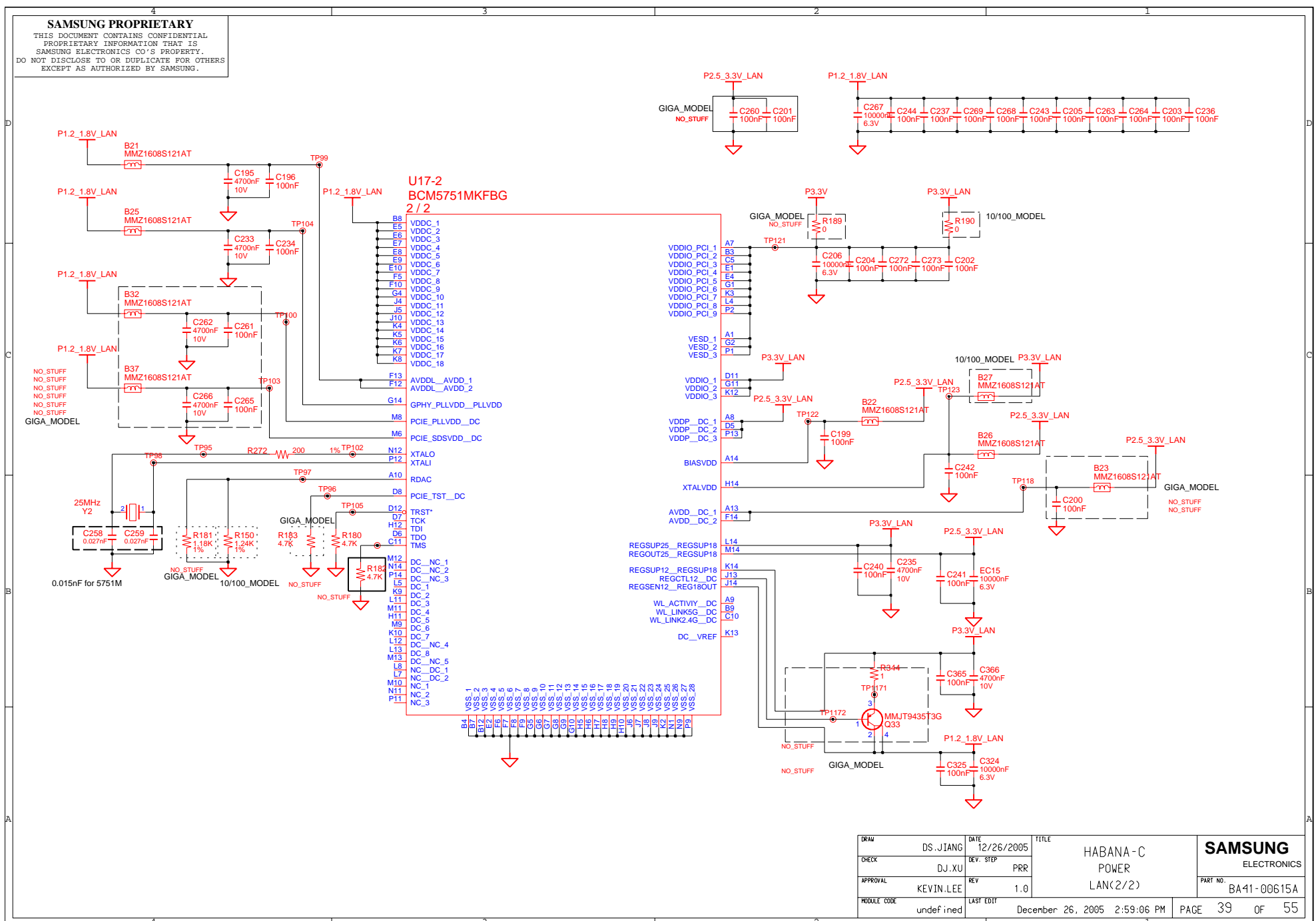


BCM4401E pin to pin

DRAW	DS.JIANG	DATE	12/26/2005	TITLE	HABANA-C	SAMSUNG ELECTRONICS
CHECK	DJ.XU	DEV. STEP	PRR	MAIN	LAN	
APPROVAL	KEVIN.LEE	REV	1.0			PART NO. BA41-00615A
MODULE CODE	undef:ind	LAST EDIT	December 26, 2005 2:59:06 PM			PAGE 38 OF 55

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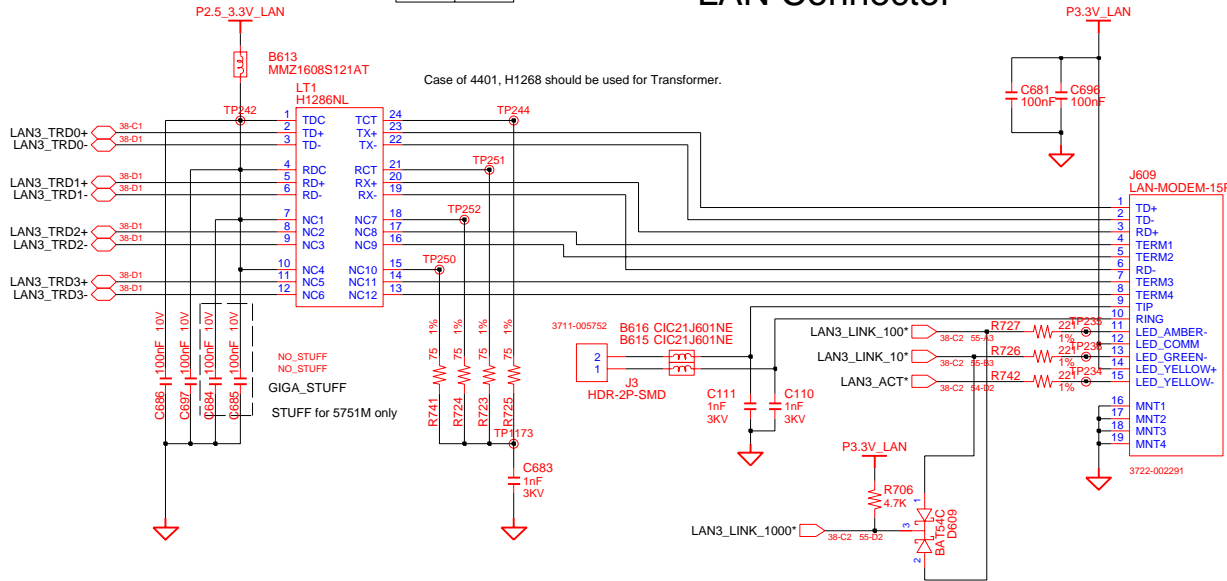
DRAW	DS.JIANG	DATE	12/26/2005	TITLE	HABANA-C POWER LAN(2/2)	SAMSUNG ELECTRONICS PART NO. BA41-00615A
CHECK	DJ.XU	DEV. STEP	PRR			
APPROVAL	KEVIN.LEE	REV	1.0			
MODULE CODE	undefined	LAST EDIT	December 26, 2005 2:59:06 PM	PAGE	39	OF 55

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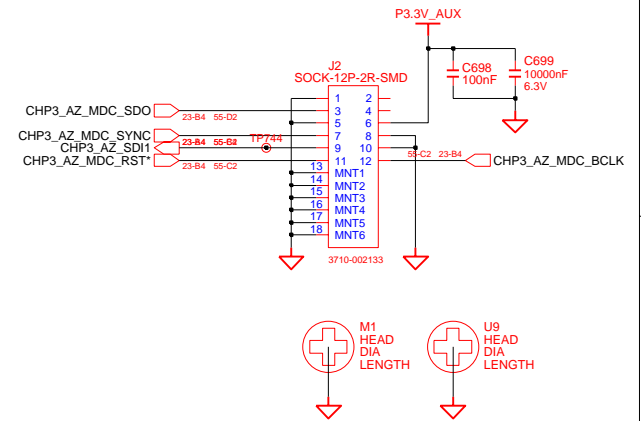
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4401E	5751
H1286	H5015

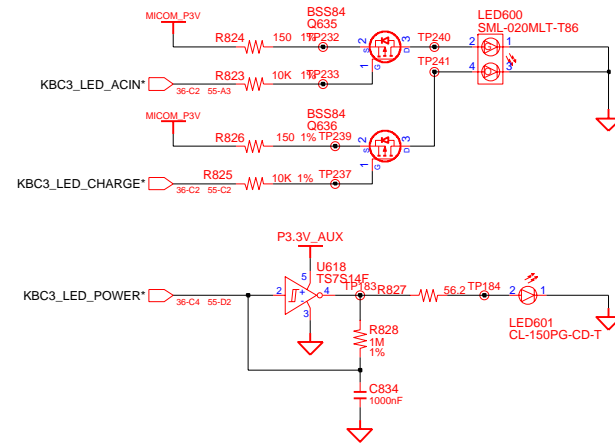
LAN Connector



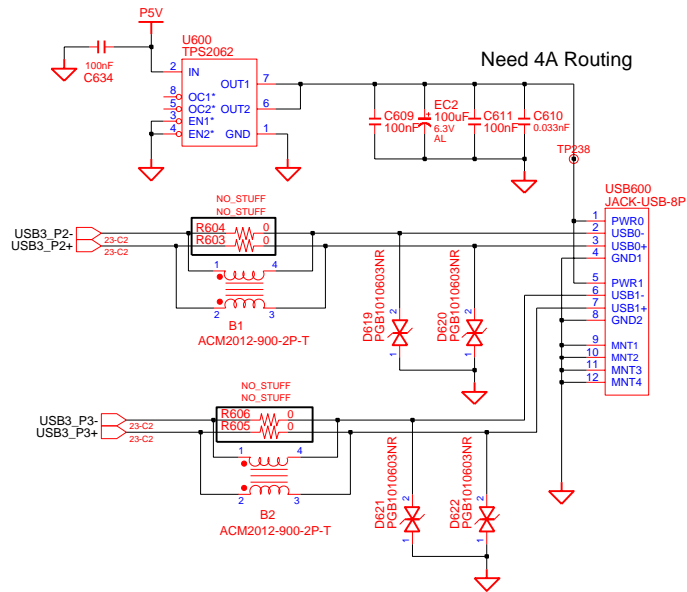
MDC Connector



ADAPTERIN/CHARGING LED

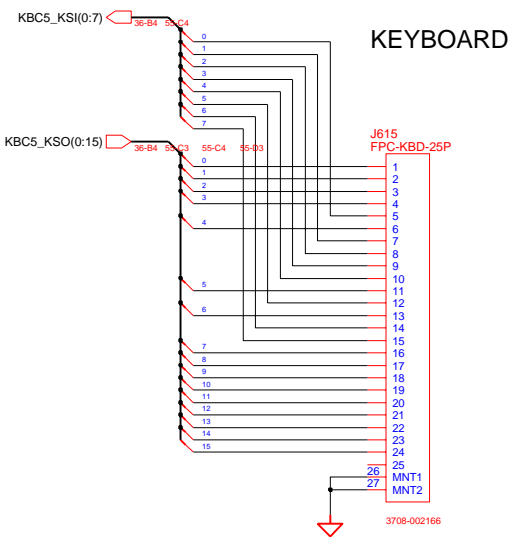


Need 4A Routing

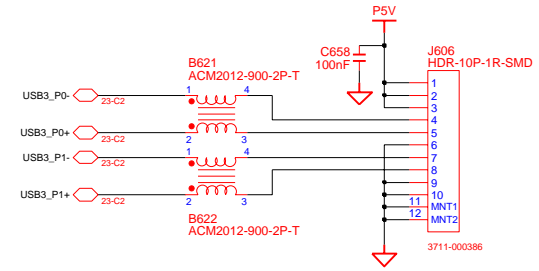
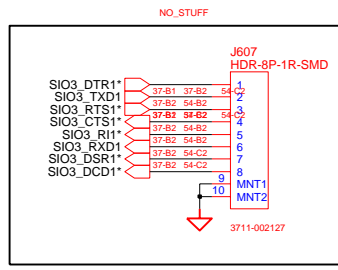


DRAW	DS.JIANG	DATE	12/26/2005	TITLE	HABANA-C MAIN	SAMSUNG ELECTRONICS
CHECK	DJ.XU	DEV. STEP	PRR	REV	1.0	
APPROVAL	KEVIN.LEE	LAST EDIT	December 26, 2005 2:59:06 PM	PAGE	40	OF 55

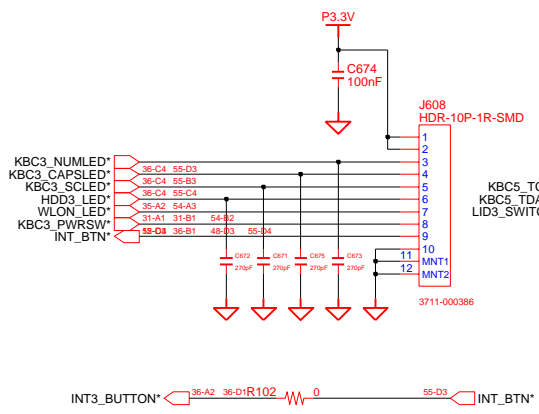
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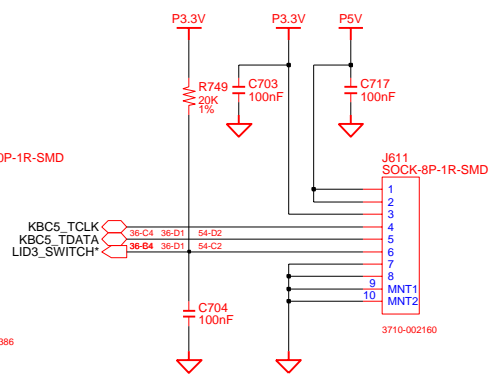
USB_SIO BOARD



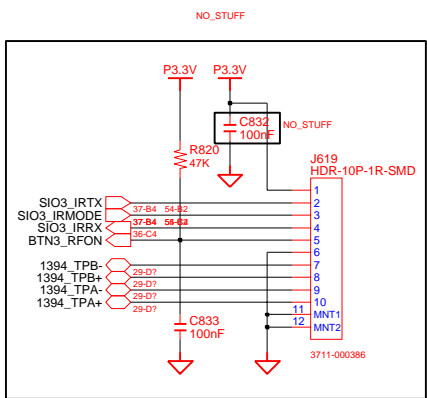
LED BOARD



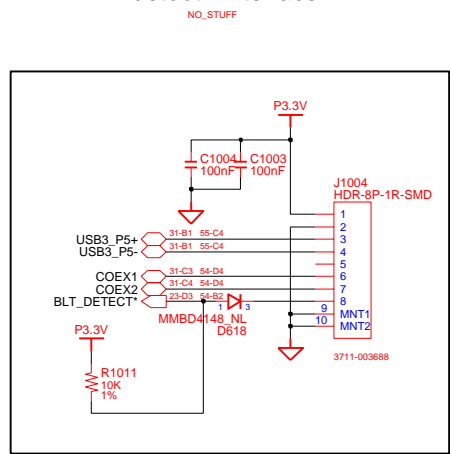
TOUCHPAD



1394_IR BOARD



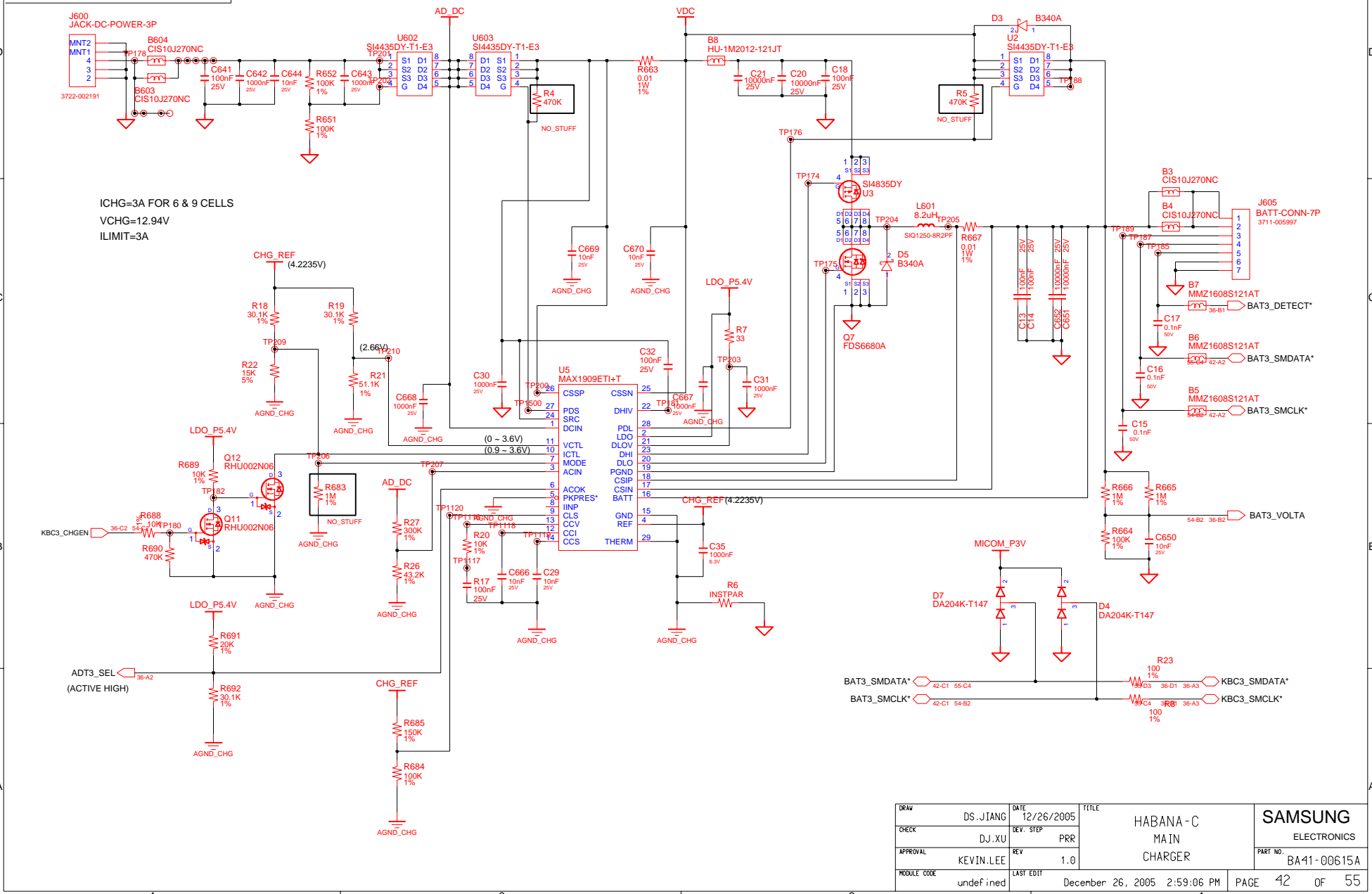
Bluetooth Interface



DRAW	DS.JIANG	DATE	12/26/2005	TITLE	HABANA-C	SAMSUNG ELECTRONICS
CHECK	DJ.XU	DEV. STEP	PRR	MAIN		
APPROVAL	KEVIN.LEE	REV	1.0	B'D TO B'D CONNECTOR	PART NO.	BA41-00615A
MODULE CODE	undefined	LAST EDIT	December 26, 2005 2:59:06 PM	PAGE	41	OF 55

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CHARGER & POWER MANAGEMENT

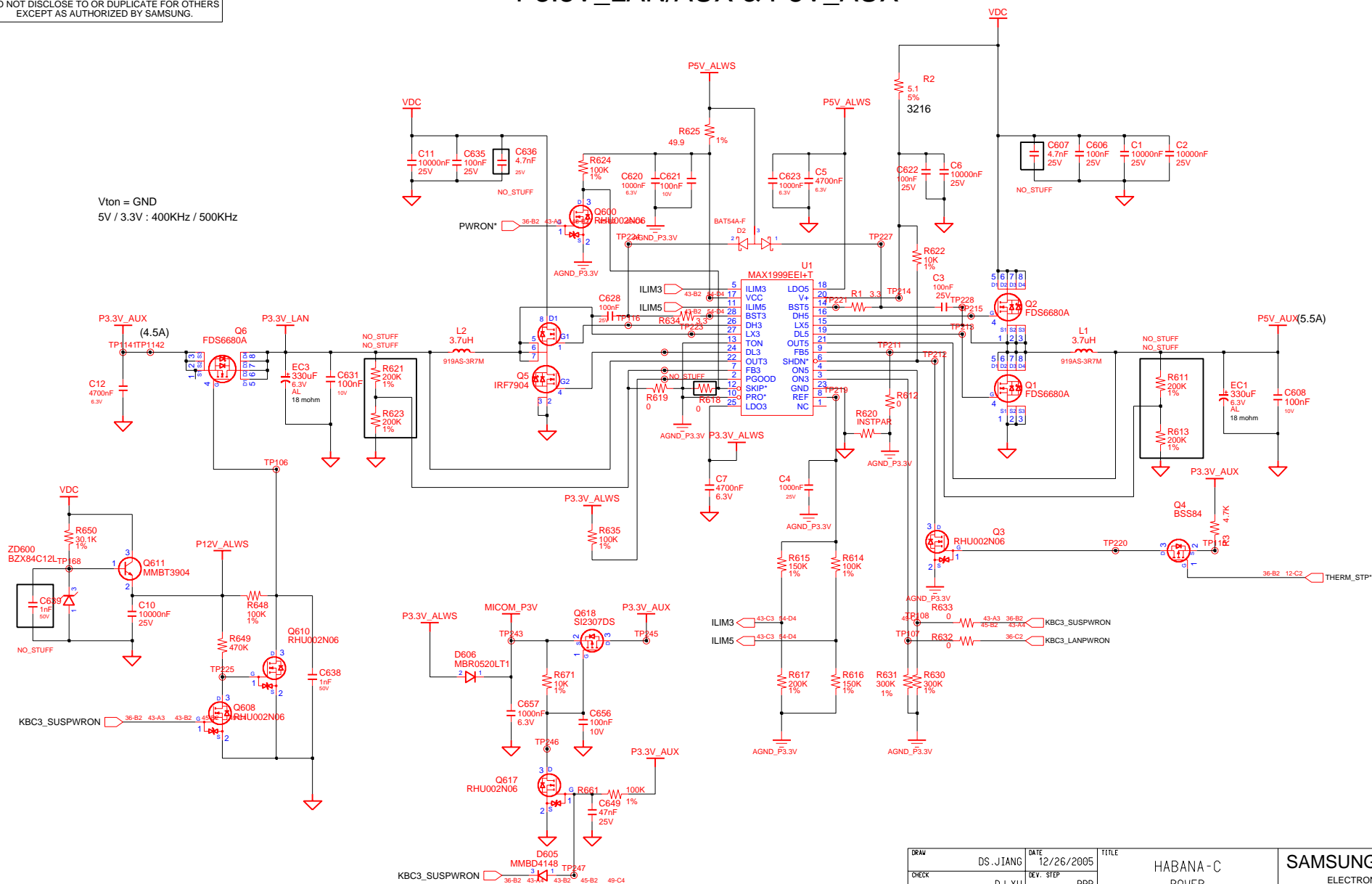


DRAW	DS.JIANG	DATE	12/26/2005	TITLE	HABANA-C MAIN CHARGER	SAMSUNG ELECTRONICS PART NO. BA11-00615A
CHECK	DJ.XU	DEV. STEP	PRR			
APPROVAL	KEVIN.LEE	REV	1.0			
MODULE CODE	undef ined	LAST EDIT	December 26, 2005 2:59:06 PM	PAGE	42 OF 55	

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P3.3V_LAN/AUX & P5V_AUX

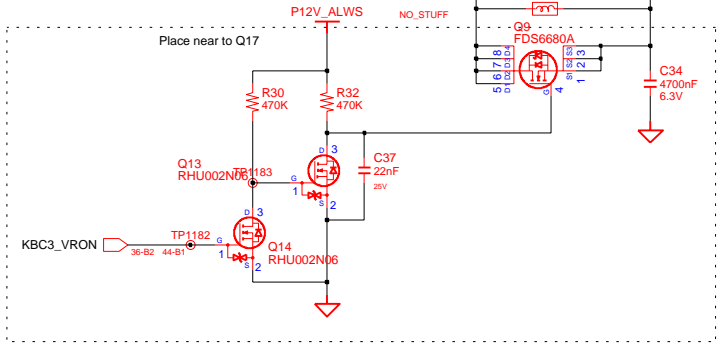
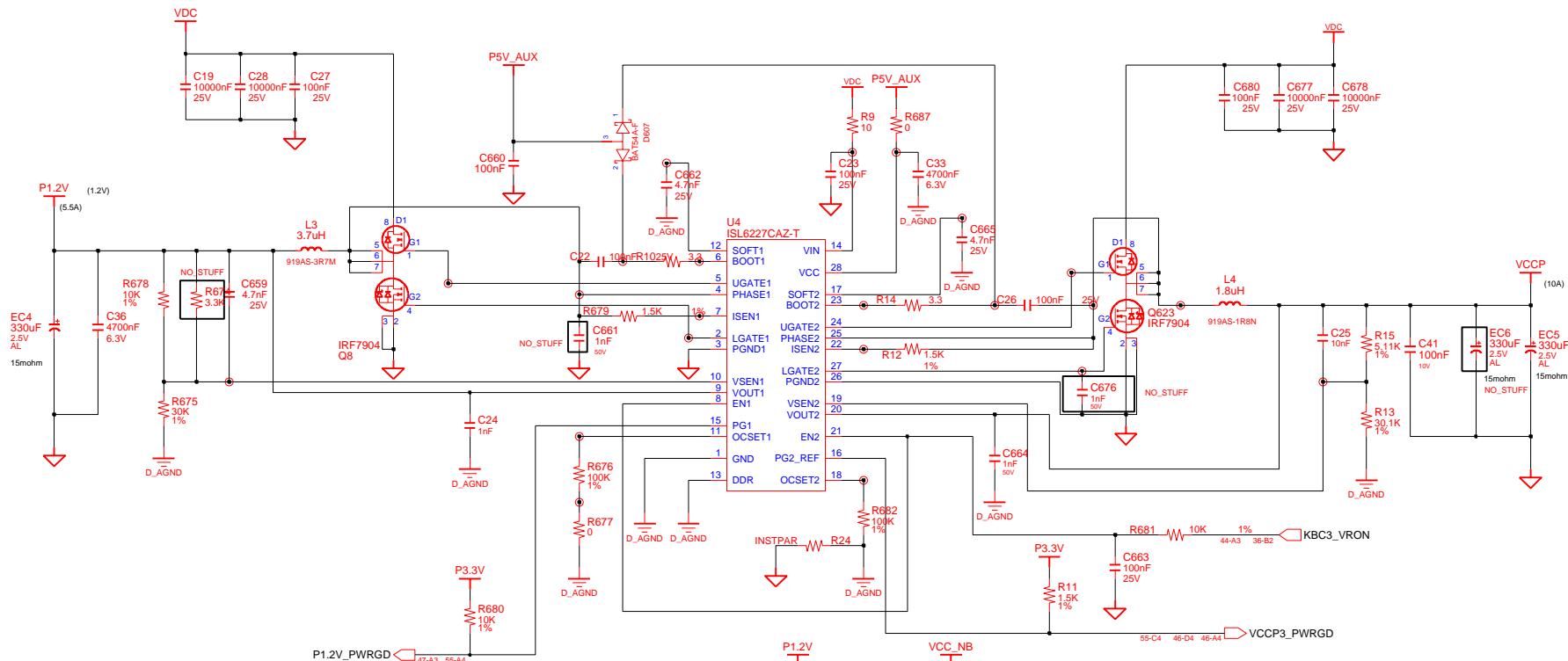
V_{ton} = GND
 5V / 3.3V : 400KHz / 500KHz



DRAW	DS.JIANG	DATE	12/26/2005	TITLE	HABANA-C POWER	SAMSUNG ELECTRONICS
CHECK	DJ.XU	DEV. STEP	PRR	REV	1.0	
APPROVAL	KEVIN.LEE	REV	1.0	LAST EDIT	December 26, 2005 2:59:06 PM	PART NO. BA11-00615A
MODULE CODE	undef ined	LAST EDIT	December 26, 2005 2:59:06 PM	PAGE	43	OF 55

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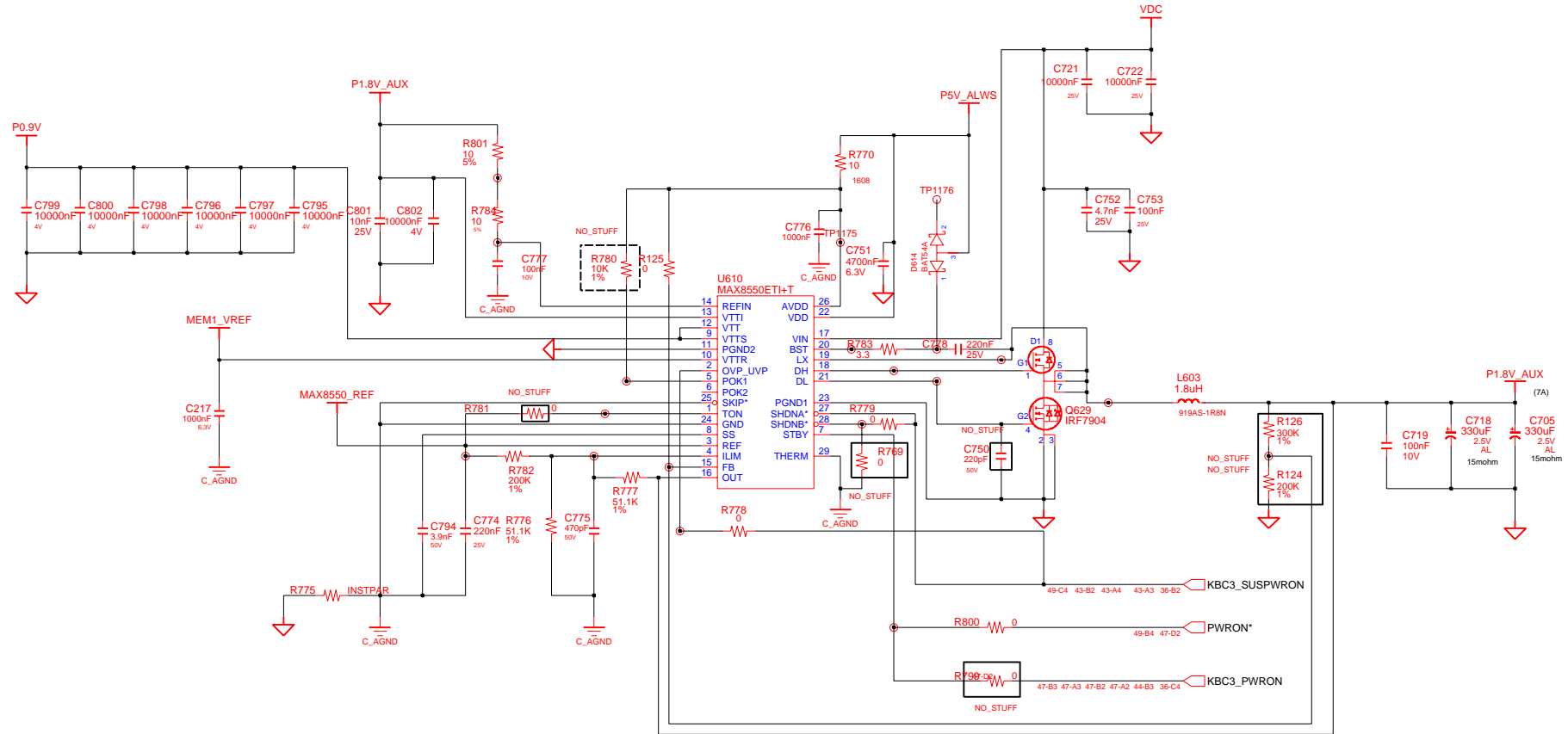
P1.2V(VCC_NB) & VCCP (1.05V)



DRAW	DS.JIANG	DATE	12/26/2005	TITLE	HABANA-C POWER P1.2V & VCCP	SAMSUNG ELECTRONICS
CHECK	DJ.XU	DEV. STEP	PRR			
APPROVAL	KEVIN.LEE	REV	1.0			PART NO. BA41-00615A
MODULE CODE	undef ined	LAST EDIT	December 26, 2005 2:59:06 PM	PAGE	44	OF 55

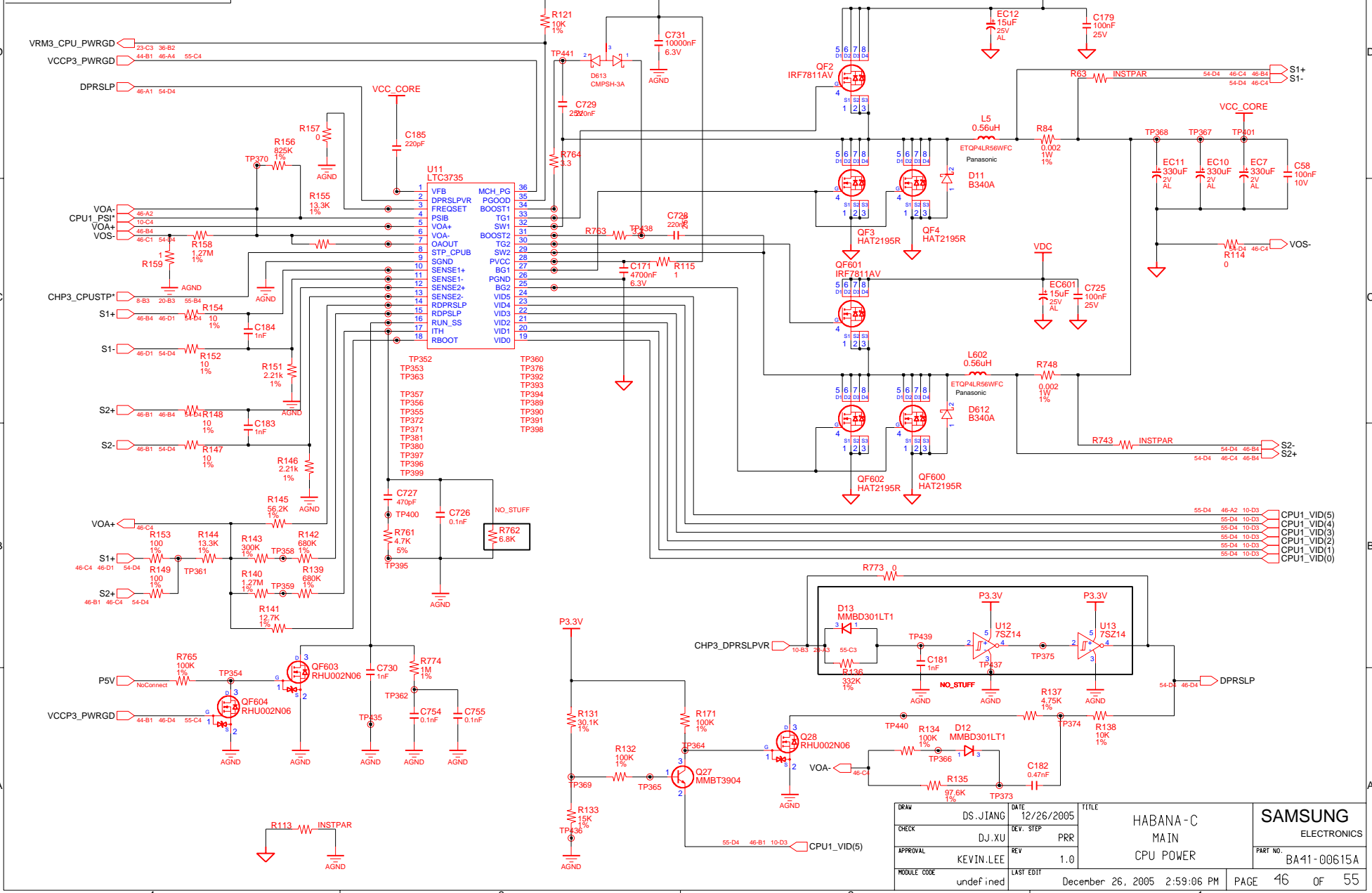
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DDR2 Power



DRAW	DS.JIANG	DATE	12/26/2005	TITLE	HABANA-C MAIN DDR POWER	SAMSUNG ELECTRONICS PART NO. BA41-00615A
CHECK	DJ.XU	DEV. STEP	PRR			
APPROVAL	KEVIN.LEE	REV	1.0			
MODULE CODE	undef:ined	LAST EDIT	December 26, 2005 2:59:06 PM	PAGE 45 OF 55		

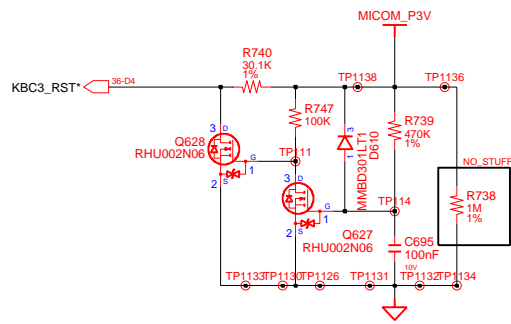
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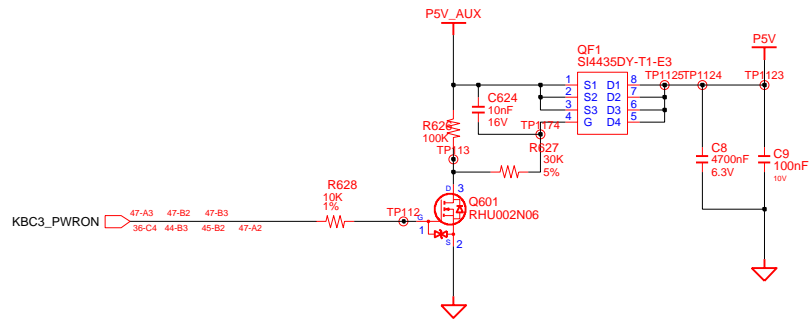
DRAW	DS.JIANG	DATE	12/26/2005	TITLE	HABANA-C MAIN CPU POWER	SAMSUNG ELECTRONICS PART NO. BA11-00615A
CHECK	DJ.XU	DEV. STEP	PRR	REV	1.0	
APPROVAL	KEVIN.LEE	LAST EDIT	December 26, 2005 2:59:06 PM	PAGE	46	OF 55

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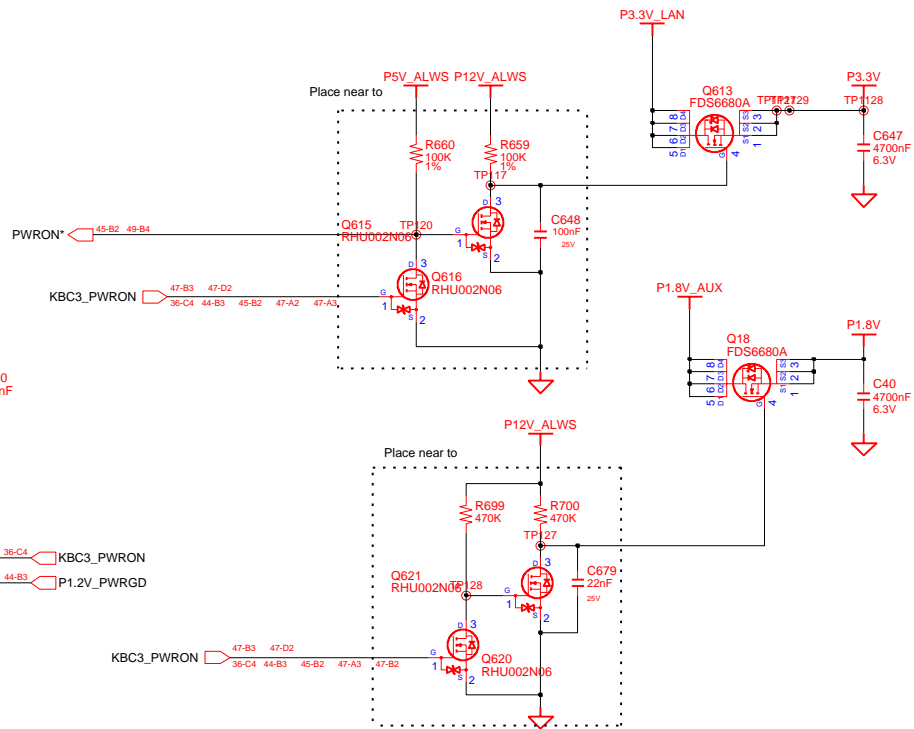
MICOM RESET



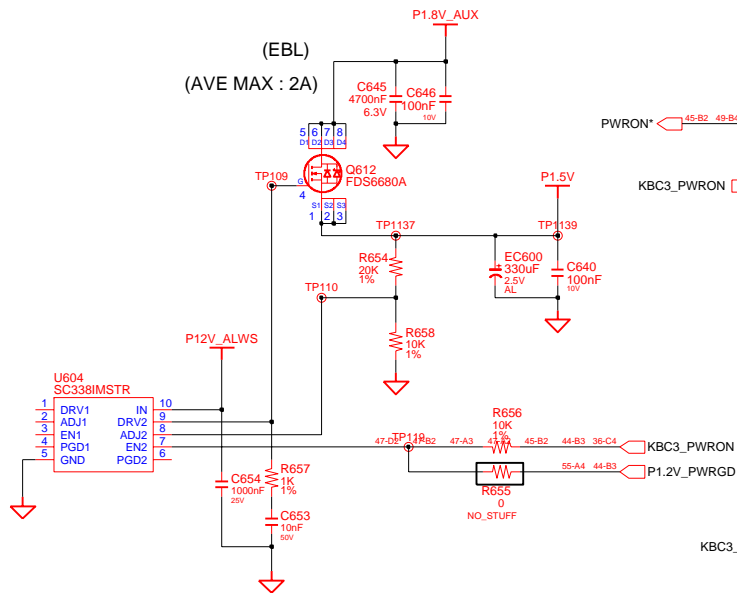
Switched Power On (P5V)



Switched Power On (P3.3V & 1.8V)

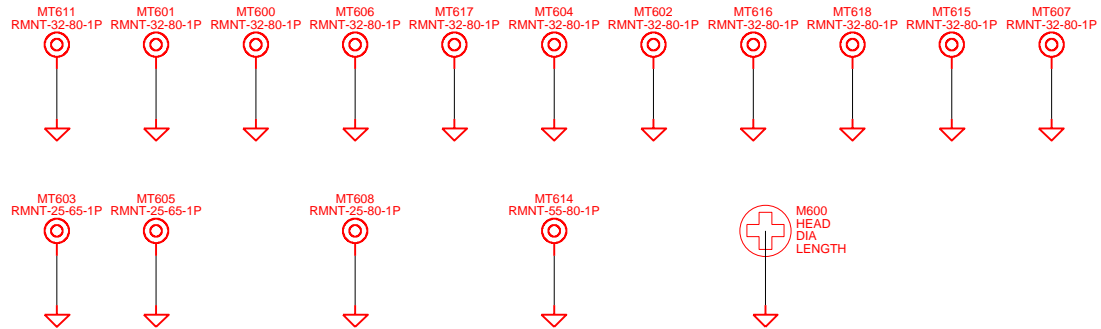
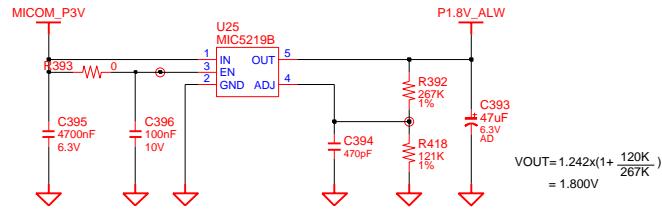
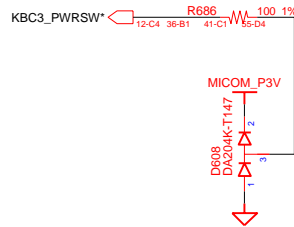


P1.5V POWER



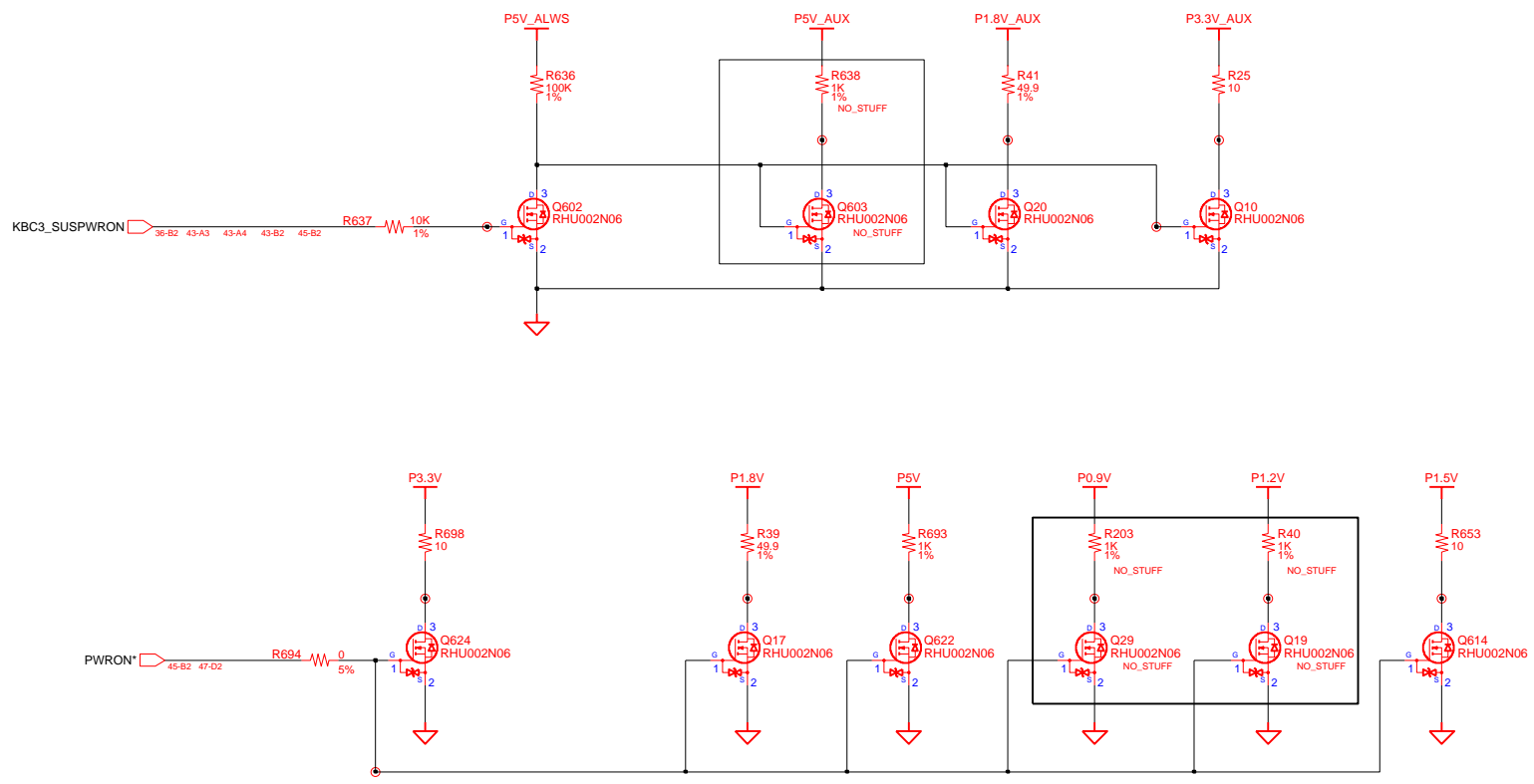
DRAW	DS.JIANG	DATE	12/26/2005	TITLE	HABANA-C MAIN MICOM & SWITCHED POWER	SAMSUNG ELECTRONICS
CHECK	DJ.XU	DEV. STEP	PRR	REV	1.0	
APPROVAL	KEVIN.LEE	LAST EDIT	December 26, 2005 2:59:06 PM	PAGE	47	OF 55
MODULE CODE	undefined					PART NO. BA41-00615A

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DRAW	DS.JIANG	DATE	12/26/2005	TITLE	HABANA - C	SAMSUNG ELECTRONICS
CHECK	DJ.XU	DEV. STEP	PRR			
APPROVAL	KEVIN.LEE	REV	1.0	P1.2V & P2.5V AUX POWER		PART NO. BA41-00615A
MODULE CODE	undefined	LAST EDIT	December 26, 2005 2:59:06 PM	PAGE	48	OF 55

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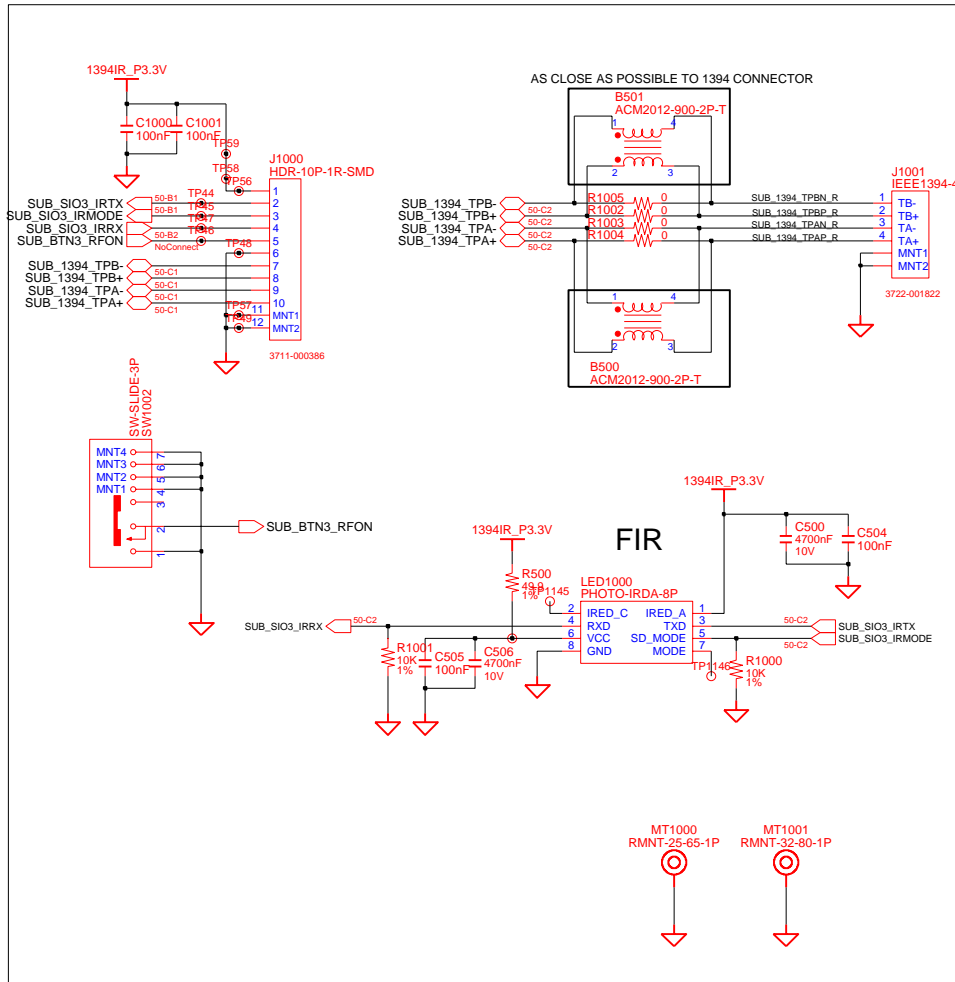
DRAW	DS.JIANG	DATE	12/26/2005	TITLE	HABANA-C MAINBD POWER ADAPT	SAMSUNG ELECTRONICS PART NO. BA41-00615A
CHECK	DJ.XU	DEV. STEP	PRR			
APPROVAL	KEVIN.LEE	REV	1.0			
MODULE CODE	undefined	LAST EDIT	December 26, 2005 2:59:06 PM	PAGE 49 OF 55		

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1394_IR BOARD

NO_STUFF

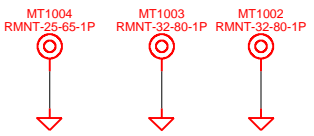
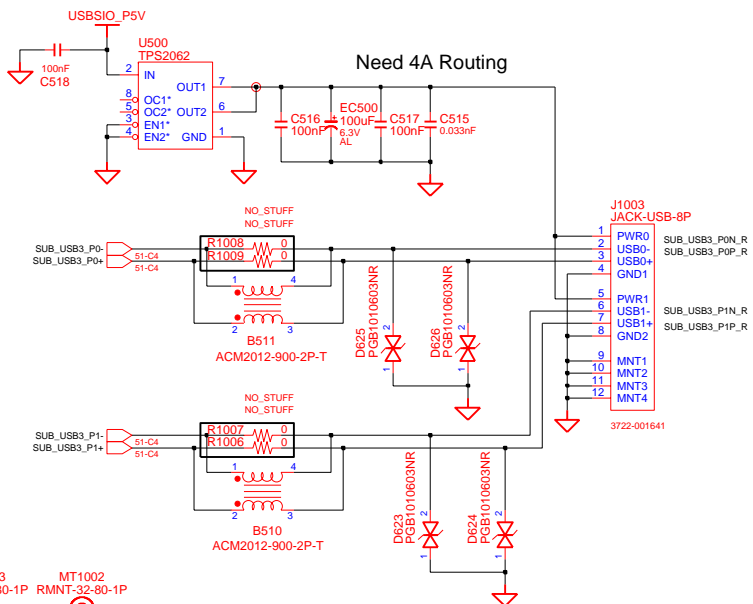
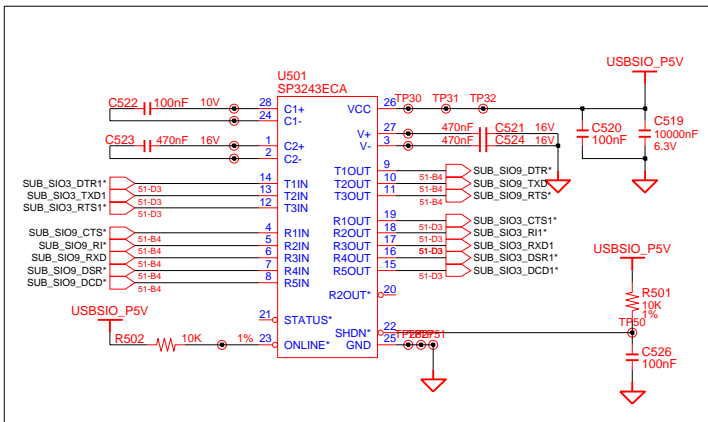
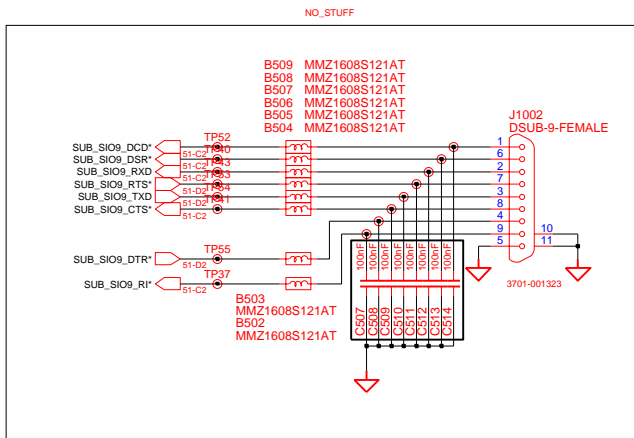
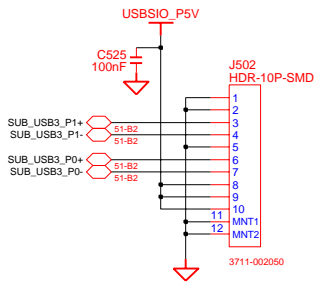
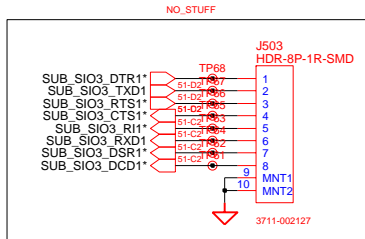


DRAW	DS.JIANG	DATE	12/26/2005	TITLE	HABANA-C MAIN 1394 BOARD	SAMSUNG ELECTRONICS PART NO. BA41-00615A
CHECK	DJ.XU	DEV. STEP	PRR			
APPROVAL	KEVIN.LEE	REV	1.0			
MODULE CODE		LAST EDIT	December 26, 2005 2:59:06 PM	PAGE 50 OF 55		

USB_SIO BOARD

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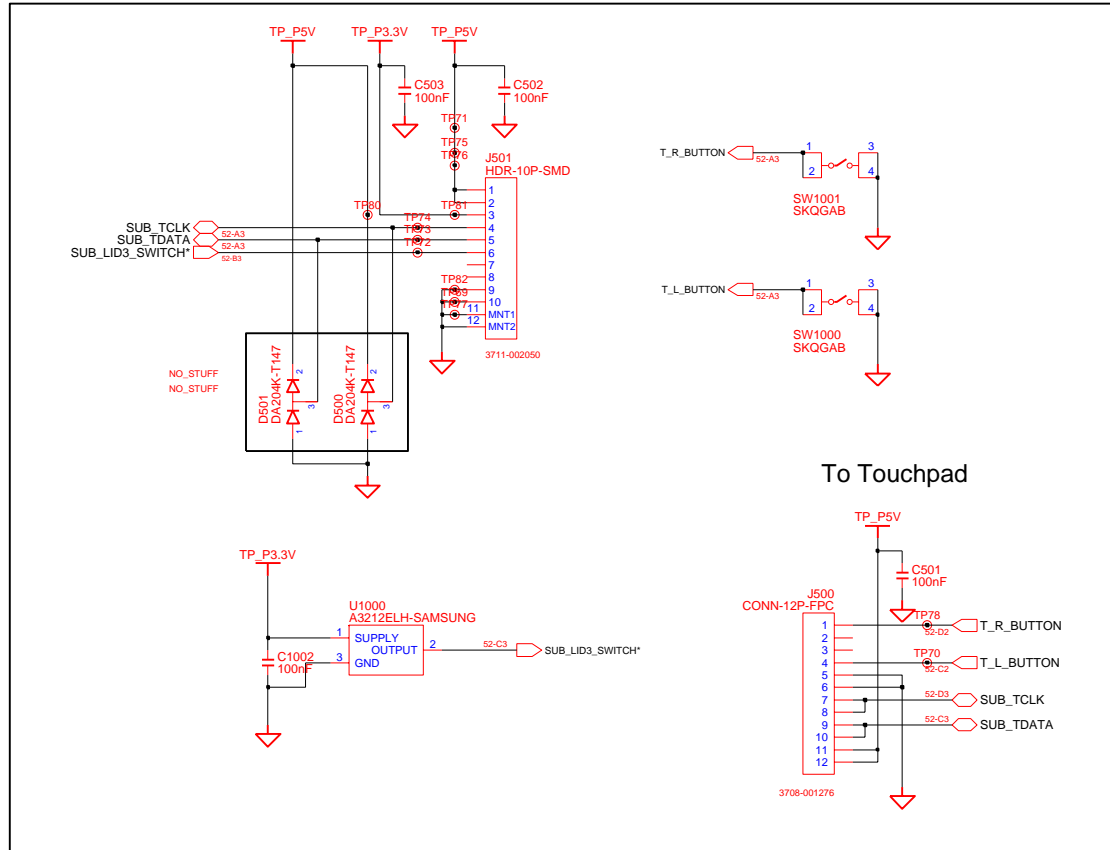


DRAW	DS.JIANG	DATE	12/26/2005	TITLE	HABANA-C POWER USB BOARD	SAMSUNG ELECTRONICS PART NO. BA41-00615A
CHECK	DJ.XU	DEV. STEP	PRR			
APPROVAL	KEVIN.LEE	REV	1.0			
MODULE CODE		LAST EDIT				
				December 26, 2005 2:59:06 PM	PAGE	51 OF 55

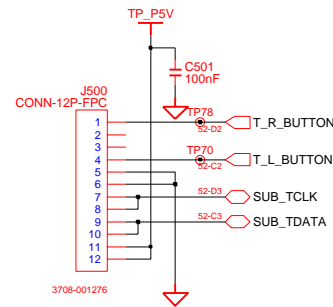
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TOUCHPAD BOARD



To Touchpad



DRAW	DS.JIANG	DATE	12/26/2005	TITLE	HABANA-C TOUCH PAD BOARD	SAMSUNG ELECTRONICS PART NO. BA41-00615A
CHECK	DJ.XU	DEV. STEP	PRR	REV		
APPROVAL	KEVIN.LEE	REV	1.0	LAST EDIT	December 26, 2005 2:59:06 PM	PAGE 52 OF 55
MODULE CODE						

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TP860CS1+
TP861CS1-
TP862CS2+
TP863CS2-
TP864CMIC1
TP865CMIC2
TP866OVOS-

TP868OILM3
TP870OILM5
TP871ODPRSLP
TP872OIDE5_A0
TP873OIDE5_A1
TP874OIDE5_A2
TP875OINI_MIC
TP876OODD5_A0
TP877OODD5_A1
TP878OODD5_A2
TP879ORIC_CLK
TP880CAC_SDOUT
TP881CAUTO_ON+
TP882OCPU1_NM1
TP883OCPU1_TCK
TP884OCPU1_TDI
TP885OCPU1_TDO
TP886OCPU1_TMS
TP887OJCK_SENS

TP856OODD5_IRQ
TP857OCPI3_PAR
TP858CSAT1_X1
TP859CSMB3_CLK

TP831OCBS3_CCLK
TP832OCBS3_CPAR
TP833OCBS3_CVS1
TP834OCBS3_CVS2
TP835OCBS3_SPKR
TP836OCHP3_SPKR

TP841OCPU1_INTR

TP845OCPU1_SLP+
TP846OCPU1_SM1+
TP847OHDD3_LED+

TP849OIDE5_CS1+
TP850OIDE5_CS3+
TP851OIDE5_D(8)
TP852OIDE5_D(1)
TP853OIDE5_D(2)
TP854OIDE5_D(3)
TP855OIDE5_D(4)

TP815OIDE5_D(5)
TP816OIDE5_D(6)
TP817OIDE5_D(7)
TP818OIDE5_D(8)
TP819OIDE5_D(9)
TP820OIDE5_DREQ
TP821OIDE5_IOR+
TP822OIDE5_IOW+
TP823OKBC3_A20G
TP824OKBC5_TCLK
TP825OLAN3_ACT+

TP827OLCD3_BRIT

TP828OODD5_CS1+
TP829OODD5_CS3+
TP830OODD5_D(0)
TP785OODD5_D(1)
TP786OODD5_D(2)
TP787OODD5_D(3)
TP788OODD5_D(4)
TP789OODD5_D(5)
TP790OODD5_D(6)
TP791OODD5_D(7)
TP792OODD5_D(8)
TP793OODD5_D(9)
TP794OODD5_DREQ
TP795OODD5_IOR+
TP796OODD5_IOW+
TP797OODD5_RST+
TP798OCPI3_CLK8
TP799OS103_IRRX
TP800OS103_IRTX
TP801OS103_R11+
TP802OS103_RXD1
TP803OS103_TXD1
TP804CSMB3_DATA
TP805OMLON_LED+
TP806OAUD3_EAPD+
TP807OBAT3_VOLTA
TP808OCBS3_A_D_2
TP809OCBS3_CCD1+
TP810OCBS3_CCD2+
TP811OCBS3_CGNT+
TP812OCBS3_CINT+
TP813OCBS3_CRE0+
TP814OCBS3_CRST+

TP776OCLK3_ICH14
TP777OCLK3_NB14M
TP778OCLK3_S1014

TP780OCPU1_A20M+

TP783OCPU1_BSEL1
TP784OCPU1_BSEL2

TP755OCPU1_FERR+
TP757OCPU1_INIT+

TP760OCPU1_TRST+
TP761OCRT3_HSYNC
TP762OCRT3_VSYNC
TP763OEXP3_CPPE+
TP764OFWH1_INIT+
TP765OIDE5_D(10)
TP766OIDE5_D(11)
TP767OIDE5_D(12)
TP768OIDE5_D(13)
TP769OIDE5_D(14)
TP770OIDE5_D(15)
TP771OIDE5_DACK+
TP772OIDE5_DASP+
TP773OIDE5_IORDY
TP774OKBC3_CHGEN
TP775CKBC5_TDATA

TP513QLCD3_VDDEN

TP516OODD5_D(10)
TP517OODD5_D(11)
TP518OODD5_D(12)
TP519OODD5_D(13)
TP520OODD5_D(14)
TP521OODD5_D(15)
TP522OODD5_DACK+
TP523OODD5_IORDY
TP524OCPI3_AD(0)
TP525OCPI3_AD(1)
TP526OCPI3_AD(2)
TP527OCPI3_AD(3)
TP528OCPI3_AD(4)
TP529OCPI3_AD(5)
TP530OCPI3_AD(6)
TP531OCPI3_AD(7)
TP532OCPI3_AD(8)
TP533OCPI3_AD(9)
TP534OCPI3_CBEO+
TP745OCPI3_CBE1+
TP746OCPI3_CBE2+
TP747OCPI3_CBE3+
TP748OCPI3_GNT0+
TP749OCPI3_GNT1+
TP750OCPI3_GNT2+
TP751OCPI3_INTB+

TP492OCPI3_INTC+
TP493OCPI3_INTD+
TP494OCPI3_INTE+
TP495OCPI3_INF+
TP496OCPI3_INTC+
TP497OCPI3_INTH+
TP498OCPI3_IORDY+
TP499OCPI3_PERR+
TP500OCPI3_RE00+
TP501OCPI3_RE01+
TP502OCPI3_RE02+
TP503OCPI3_RE03+
TP504OCPI3_RSTF+
TP505OCPI3_SERR+
TP506OCPI3_STOP+
TP507OCPI3_TRODY+

TP462CCLK3_DBGLPC

TP508OPLT3_RSTF+

TP509OS103_CTS1+
TP510OS103_DCD1+
TP511OS103_DSR1+
TP464CS103_DTR1+
TP465CS103_RTS1+

TP467OVGA3_HSYNC
TP468OVGA3_VSYNC
TP469OAUD3_EAPD_A
TP470OAUD3_PCBEF

TP471OBAT3_SMCLK+

TP473OCBS3_A_A_18
TP474OCBS3_A_A_19
TP475OCBS3_A_D_14
TP476OCBS3_CAD(0)
TP477OCBS3_CAD(1)
TP478OCBS3_CAD(2)
TP479OCBS3_CAD(3)
TP480OCBS3_CAD(4)
TP481OCBS3_CAD(5)
TP482OCBS3_CAD(6)
TP483OCBS3_CAD(7)
TP484OCBS3_CAD(8)
TP485OCBS3_CAD(9)
TP486OCBS3_CAUD10
TP487OCBS3_CCBE0+
TP488OCBS3_CCBE1+
TP489OCBS3_CCBE2+
TP490OCBS3_CCBE3+
TP491OCBS3_CTRDY+
TP492OCBS3_CPERR+
TP493OCBS3_CSERR+
TP494OCBS3_CSTOP+
TP495OCBS3_CTRDY+
TP496OCBS3_MD_CLK
TP497OCBS3_VPPEN1
TP498OCHP3_BMREQ
TP499OCHP3_LDR00+
TP500OCHP3_LDR01+
TP501OCHP3_SDRME+
TP461OCHP3_SERIRQ

DRAW	JIANG, DS	DATE	12/26/2005	TITLE	HABANA-C	SAMSUNG ELECTRONICS
CHECK	XU, DJ	DEV. STEP	PRR			
APPROVAL	LEE, KEVIN	REV	1.0	TP		PART NO. BA41-00615A
MODULE CODE	undefined	LAST EDIT	December 26, 2005 2:59:06 PM	PAGE	53	OF 55

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TP1085OCPU1_DPSLP*
 TP1086OCPU1_IGNNE*
 TP1087OCPU1_VID(0)
 TP1088OCPU1_VID(1)
 TP1089OCPU1_VID(2)
 TP1090OCPU1_VID(3)
 TP1091OCPU1_VID(4)
 TP1092OCPU1_VID(5)
 TP1093OCRT3_DDCCLK
 TP1094OEP3_CPUSB*
 TP1095OEXP3_PERST*
 TP1096OIDE5_IDEIRO
 TP1097OJCK_SEN5_HP
 TP1098OKBC3_PMS5A*
 TP1099OKBC3_SCLLED*
 TP1100OKBC3_SMLCK*
 TP1101OKBC5_KS1(0)
 TP1102OKBC5_KS1(1)
 TP1103OKBC5_KS1(2)
 TP1104OKBC5_KS1(3)
 TP1105OKBC5_KS1(4)
 TP1106OKBC5_KS1(5)
 TP1107OKBC5_KS1(6)
 TP1108OKBC5_KS0(1)
 TP1109OKBC5_KS0(0)
 TP1110OKBC5_KS0(1)
 TP1111OKBC5_KS0(2)
 TP1112OKBC5_KS0(3)
 TP1113OKBC5_KS0(4)
 TP1114OKBC5_KS0(5)
 TP1115OKBC5_KS0(6)
 TP1099OKBC5_KS0(7)
 TP1070OKBC5_KS0(8)
 TP1071OKBC5_KS0(9)
 TP1072OLAN3_EEP_CS
 TP1073OLAN3_EEP_D1
 TP1074OLAN3_EEP_D0
 TP1078OLCD3_BKL1EN
 TP1079OLCD3_BKL1ON
 TP1080OLPC3_LAD(0)
 TP1081OLPC3_LAD(1)
 TP1082OLPC3_LAD(2)
 TP1083OLPC3_LAD(3)
 TP1048OP1_2V_PWRGD
 TP1049OPC13_AD(10)
 TP1050OPC13_AD(11)
 TP1051OPC13_AD(12)
 TP1052OPC13_AD(13)

TP1053OPC13_AD(14)
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 TP1001OCBS3_CAD(31)
 TP1002OCBS3_CFRAME*
 TP1003OCBS3_CSTSCHG
 TP1004OCBS3_VCC3EN*
 TP1005OCBS3_VCC5EN*
 TP1007OCHP3_BIOSWP*
 TP1008OCHP3_CPUSIP*
 TP1010OCLK3_33M_MIN
 TP1011OCLK3_PCLKFVH
 TP1012OCLK3_PCLKLAN
 TP1013OCLK3_PCLKS10
 TP1014OCPU1_CPURST*
 TP1015OCPU1_DPRSTP*

TP975OCPU1_STPCLK*
 TP976OCPU2_THERMDA
 TP977OCPU2_THERMD
 TP978OFAN3_FDBACK*
 TP979OITP3_SYSRST*
 TP980OJCK_SEN5_MIC
 TP981OKBC3_EX15MT*
 TP982OKBC3_NUMLED*
 TP983OKBC3_PWMBRIT
 TP984OKBC3_RUNSC1*
 TP985OKBC3_SMDATA*
 TP986OKBC5_KS0(10)
 TP987OKBC5_KS0(11)
 TP988OKBC5_KS0(12)
 TP989OKBC5_KS0(13)
 TP990OKBC5_KS0(14)
 TP991OKBC5_KS0(15)
 TP992OLAN3_EEP_CLK
 TP996OLPC3_LFRAME*
 TP997OMCH2_THERMDA
 TP998OMCH2_THERMD

TP973OINT_BTN*
 TP974OPC13_CLKRUN*
 TP975OPC13_DEVSEL*

TP961OCBS3_CCLKRUN*
 TP962OCBS3_CDEVSEL*
 TP963OCBS3_MD_DATA1*
 TP964OCBS3_MD_DATA2*
 TP965OCBS3_MD_DATA3*
 TP966OCBS3_MD_VCCEN*
 TP967OCHP3_BIOS_TBL*
 TP968OCHP3_DPRSLPVR
 TP969OCHP3_SATALED*

TP970OCPU1_PROCH01*
 TP971OCPU1_PARGDCPU
 TP972OKBC3_CAPSLED*
 TP942OLAN3_LINK_10*
 TP943OLCD3_BKL1CTRL

TP945OCBS3_MD_XD_ALE
 TP946OCBS3_MD_XD_CE*
 TP947OCBS3_MD_XD_CLE
 TP948OCBS3_MD_XD_WP*
 TP949OCHP3_SATA_DET*

TP951OCLK3_PCLKK1COM
 TP952OCPU1_THRMTRIP*
 TP953OCPU3_THRMTRIP*
 TP954OKBC3_LED_ACIN*
 TP955OKBC5_CAL_THRM*
 TP956OLAN3_LINK_100*

TP914OAU5_L1NE_OUT_R
 TP915OCHP3_1394_ROM*
 TP916OCHP3_ALINK_RST*
 TP917OCHP3_AZ_AUD_SDO
 TP918OCHP3_AZ_MDC_SDO
 TP919OCLK3_PCLKS10_DS
 TP920OKBC3_LED_POWER*
 TP921OLAN3_LINK_1000*

TP922OCBS3_MD_DATA4_XD
 TP923OCBS3_MD_DATA5_XD
 TP924OCBS3_MD_DATA6_XD
 TP925OCBS3_MD_DATA7_XD
 TP926OCHP3_AZ_AUD_BCLK
 TP927OCHP3_AZ_AUD_RST*
 TP928OCHP3_AZ_AUD_SYNC
 TP929OCHP3_AZ_MDC_BCLK
 TP930OCHP3_AZ_MDC_RST*
 TP931OCHP3_AZ_MDC_SYNC
 TP932OCHP3_SBT_HRMTRIP*
 TP933OKBC3_LED_CHARGE*
 TP934OKBC3_THERM_SMLCK

TP936OKBC3_THERM_SMDATA
 TP937OCBS3_SD_CD*_XD_CD*
 TP938OCBS3_MS_INSA*_XD_CD*
 TP939OCBS3_SD_WP*_XD_R_B*
 TP940OCBS3_MD_DATA0_MS_SD10
 TP941OAVDD
 TP942OAVDD
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 TP944OAVDD
 TP945OAVDD
 TP946OAVDD
 TP947OAVDD
 TP948OAVDD
 TP949OAVDD

TP892OAVDDO
 TP896OAVSSN
 TP897OAVSSQ
 TP898OAVSSQ

TP902OAVSSDI
 TP904OAVSSDI
 TP905OAMP_VDD
 TP906OAMP_VDD
 TP907OAMP_VDD
 TP908OAMP_VDD

TP912OAVDD_CK
 TP913OAVDD_NB
 TP682OAVDD_NB

TP685OAGND_AUD
 TP686OAGND_AUD
 TP687OAGND_AUD
 TP688OAGND_AUD
 TP689OAGND_CHG
 TP690OAGND_CHG
 TP691OAGND_CHG
 TP692OAGND_CHG
 TP693OAGND_P3_3V
 TP694OAGND_P3_3V
 TP695OAGND_P3_3V
 TP696OAGND_P3_3V

TP702OC_AGND
 TP703OC_AGND
 TP704OC_AGND
 TP705OCB_VCCA
 TP707OCB_VCCA
 TP708OCB_VCCA
 TP709OCB_VPPA

TP712OCB_VPPA
 TP650OCHG_REF
 TP651OCHG_REF
 TP653OCTR_GND
 TP654OCTR_GND
 TP655OCTR_GND
 TP656OCTR_GND

TP659OCB_MD_VCC
 TP660OCB_MD_VCC
 TP661OC_AGND
 TP662OC_AGND
 TP663OC_AGND
 TP664OC_AGND

TP666OINV_VDC
 TP671OLPVSS
 TP672OLPVSS

TP676OLVSSR
 TP680OLCD_VDD3V
 TP681OLCD_P5_4V
 TP618OLCD_P5_4V

TP624OMEM1_VREF
 TP625OP0_3V
 TP626OP0_3V
 TP627OP0_3V
 TP628OP0_3V
 TP629OP1_2V
 TP630OP1_2V
 TP631OP1_2V
 TP632OP1_2V
 TP633OP1_8V
 TP634OP1_8V
 TP635OP1_8V
 TP636OP1_8V

TP589OP5V_AUX
 TP590OP5V_AUX
 TP591OP5V_AUX
 TP592OP5V_AUX
 TP593OP5V_ALWS
 TP594OP5V_ALWS
 TP595OP5V_ALWS
 TP596OP5V_ALWS

TP600OPRTC_BAT
 TP601OP1_5V_EXP
 TP603OP1_5V_EXP
 TP604OP1_5V_EXP

TP607OP1_8V_ALW
 TP608OP1_8V_ALW
 TP609OP1_8V_AUX
 TP610OP1_8V_AUX
 TP611OP1_8V_AUX
 TP612OP1_8V_AUX
 TP613OP12V_ALWS
 TP614OP12V_ALWS
 TP615OP12V_ALWS
 TP616OP12V_ALWS
 TP617OP3_3V_EXP
 TP618OP3_3V_EXP
 TP619OP3_3V_EXP
 TP620OP3_3V_EXP
 TP621OP3_3V_LAN
 TP622OP3_3V_LAN
 TP623OP3_3V_LAN

TP563OPCIE_PVDD
 TP564OPCIE_PVDD

TP568OPCIE_VDDR
 TP569OP3_3V_ALWS
 TP570OP3_3V_ALWS
 TP571OP3_3V_ALWS
 TP572OP3_3V_ALWS
 TP573OP1_2_1_8V_LAN
 TP574OP1_2_1_8V_LAN
 TP575OP1_2_1_8V_LAN
 TP576OP1_2_1_8V_LAN
 TP577OP2_5_3_3V_LAN
 TP578OP2_5_3_3V_LAN
 TP579OP2_5_3_3V_LAN
 TP580OP2_5_3_3V_LAN
 TP581OP3_3V_AUX_EXP
 TP582OP3_3V_AUX_EXP

TP538OVDC
 TP539OVDC
 TP540OVDC
 TP541OVDC
 TP542OVCCP
 TP543OVCCP
 TP544OVCCP
 TP545OVCCP
 TP546OVCC_NB
 TP547OVCC_NB
 TP548OVCC_NB
 TP549OVCC_NB

TP553OVCC_CRT

DRAW	JIANG, DS	DATE	12/26/2005	TITLE	HABANA-C	SAMSUNG ELECTRONICS
CHECK	XU, DJ	DEV. STEP	PRR			
APPROVAL	LEE, KEVIN	REV	1.0		TP	PART NO. BA41-00615A
MODULE CODE	undefined	LAST EDIT	December 26, 2005 2:59:06 PM	PAGE	54	OF 55

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REV600
 1 O
 2 O O3

PCB REVISION CONTROL (ICT)				
NO	CONNECTION	DATE(Y/M/D)	REVISION	STEP
1	N.C.			
2	1-2			
3	2-3			
4	3-1			
5	1-2-3			
6	N.C.			
7	1-2			
8	2-3			
9	3-1			
10	1-2-3			

DRAW	JIANG, DS	DATE	12/26/2005	TITLE	HABANA-C	SAMSUNG ELECTRONICS
CHECK	XU, DJ	DEV. STEP	PRR			
APPROVAL	LEE, KEVIN	REV	1.0		TP	PART NO. BA41-00615A
MODULE CODE	undefined	LAST EDIT	December 26, 2005 2:59:06 PM	PAGE	55	OF 55