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# FIRENZE-R

CPU : Yonah 667  
Chip Set : CALISTOGA & ICH7-M  
Remarks : Mobility Platform

Model Name : FIRENZE-R  
PBA Name : MAIN  
PCB Code : BA41-00655A/B  
Dev. Step : SR  
Revision : 1.0  
T.R. Date : 2006.03.09

DRAW	CHECK	APPROVAL
SON,C.W	YUN,C.Y	LIM,J.G

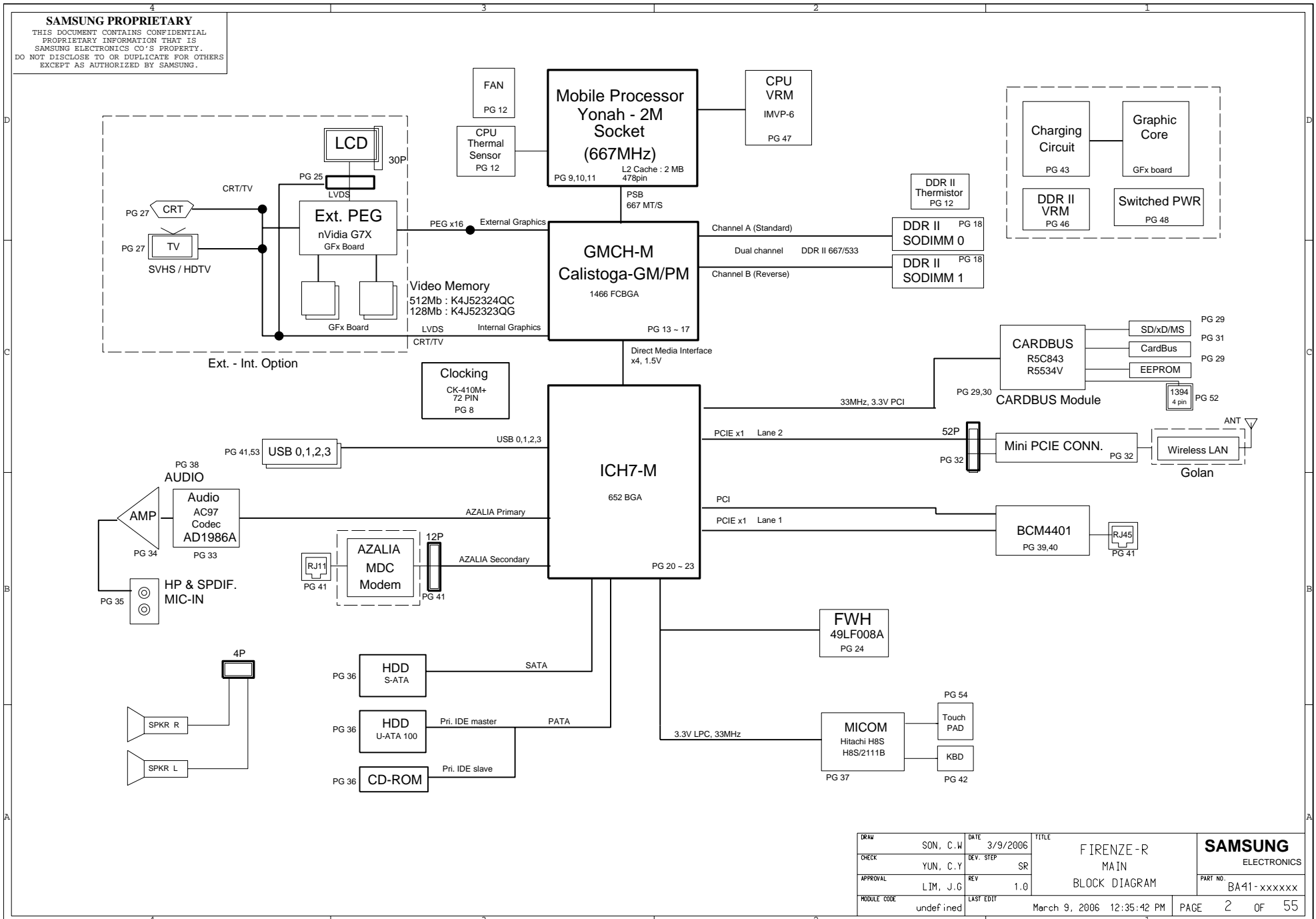
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- GRAPHIC CORE POWER
- CPU POWER
- 1.2V / 2.5V POWER
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- 5-IN-1 SUB B'D
- TPM
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DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	SR	MAIN		
APPROVAL	LIM, J.G	REV	1.0	BOARD INFORMATION	PART NO.	BA41-00655A
MODULE CODE	undef ined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	1	OF 55

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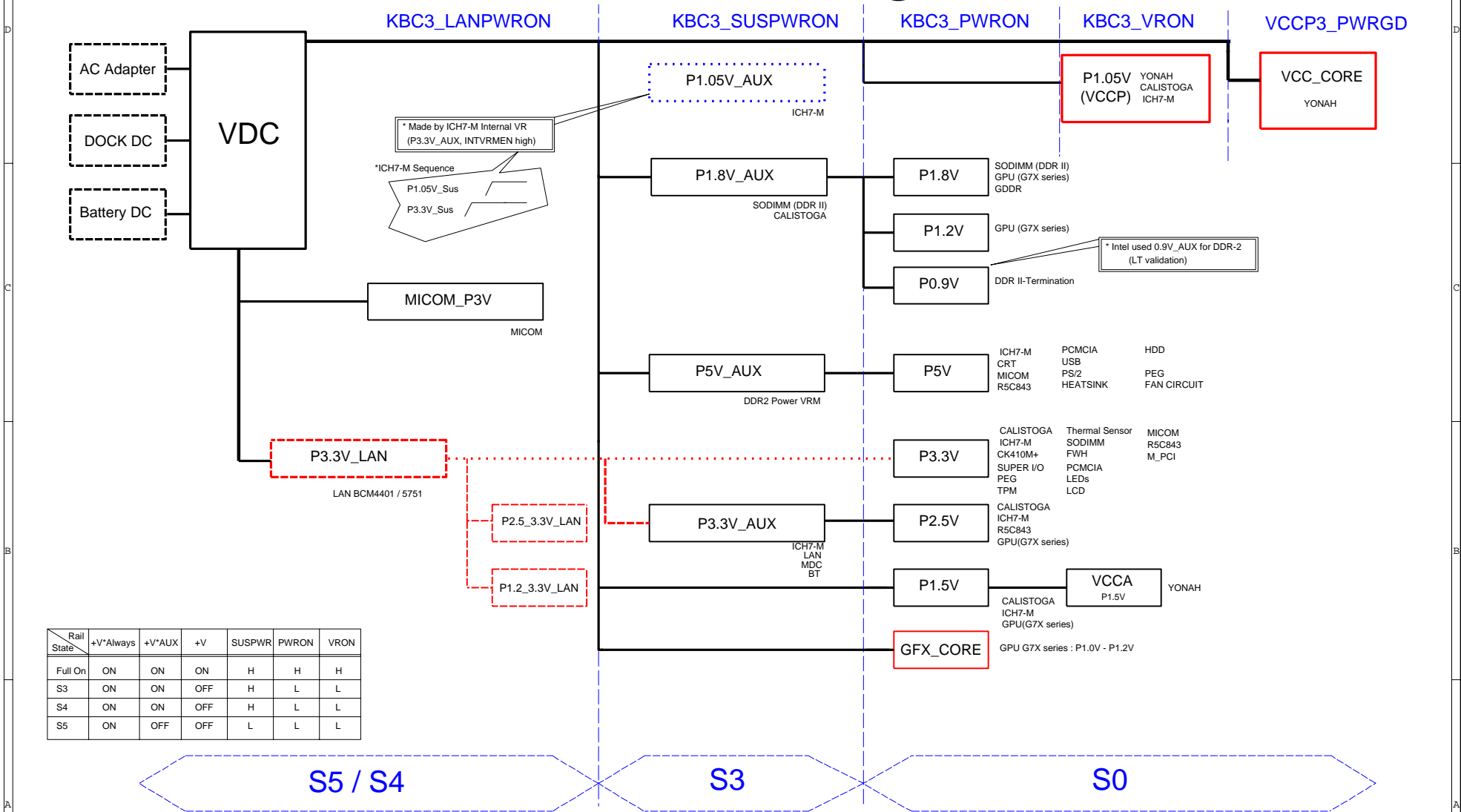


DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN BLOCK DIAGRAM	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-xxxxxx
CHECK	YUN, C.Y	DEV. STEP	SR			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undef ined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE 2 OF 55		

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# Power Diagram



DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN POWER DIAGRAM	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-xxxxxx
CHECK	YUN, C.Y	DEV. STEP	SR			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undef ined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE 3 OF 55		

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# SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

## PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
Cardbus	AD25	0	E,F,G
LAN	AD21	1	G
USB	AD29(internal)	-	USB2.0 #0 : A USB2.0 #1 : D USB2.0 #2 : C
Hub to PCI	AD30(internal)	-	B
LPC bridge/IDE/AC97/SMBUS	AD31(internal)	-	B
Internal MAC	AD24(internal)	-	E
AC Link	-	-	B

## Voltage Rails

VDC	Primary DC system power supply (7 to 21V)
VCC_CORE	Core voltage for DOTHAN (1.308~1.068V)
VCCP	YONAH/CALISTOGA Processor System Bus(PSB) Termination (1.05V) MCH-M Core Voltage
P0.9V	0.9V switched power rail (off in S3-S5)
P1.2V	1.2V switched power rail (off in S3-S5)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.8V	1.8V switched power rail (off in S3-S5)
P2.5V	2.5V switched power rail (off in S3-S5)
P3.3V	3.3V switched power rail (off in S3-S5)
P5V	5.0V switched power rail (off in S3-S5)
MEM1_VREF	0.9V power rail (off in S4-S5)
P1.8V_AUX	1.8V power rail(off in S4-S5)
P3.3V_AUX	3.3V power rail (off in S4-S5)
P5V_AUX	5.0V power rail (off in S4-S5)
MICOM_P3V	3.3V always on power rail for MICOM
P5V_ALWS	5V power rail (Always On)
P12V_ALWS	12V power rail (Always On)

## I<sup>2</sup>C / SMB Address

Devices	Address	Hex	Bus
ICH7	Master	-	SMBUS Master
SODIMM0	1010 0000	A0h	-
SODIMM1	1010 001X	A4h	-
CK-408 (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable

Devices	Address	Hex	Bus
MICOM	Master	-	SMBUS Master
EMC6N300(CPU Thermal Sensor)	0101 111X	5Eh	Thermal Sensor
BATTERY	-	-	-
GFX thermal sensor	1001 000X	90h	Thermal Sensor

## USB PORT Assign

PORT NUMBER	ASSIGNED TO
0,1	SYSTEM PORT A
2,3	SYSTEM PORT B
3	SYSTEM PORT C
4	BLUETOOTH
5	PORT REPLICATOR
6	FINGER PRINT
7	EXPRESS CARD

## System Power States

- CHP3\_SLPS1\* S1, Powered-On-Suspend(POS) : In this state, all clocks(except the 32.768KHz clock) are stopped. The system context is maintained in system DRAM. Power is maintained to PCI, the CPU, memory controller, memory, and all other critical subsystems. Note that this state does not preclude power being removed from non-essential devices, such as disk drives. During this state, CPU can be selected for either Deep Sleep or Deeper Sleep.
- In Deeper Sleep, CPU voltage reduced in this state to reduce the leakage power.
- CHP3\_SLPS3\* S3, Suspend-To-RAM(STR) : The system context is maintained in system DRAM, but power is shut off to non-critical circuits. Memory is retained, and refreshes continue. All clocks stop except RTC clock.
- CHP3\_SLPS4\* S4, Suspend-To-Disk(STD) : The Context of the system is maintained on the disk. All power is then shut off to the system except for the logic required to resume. Externally appears same as S5, but may have different wake events.
- CHP3\_SLPS5\* S5, Soft Off(SOFF) : System context is not maintained. All power is shut off except for the logic required to restart. A full boot is required when waking.

## Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	ICH7-M	Real Time Clock
Crystal	10MHz	MICOM	H8S/211B
Crystal	14.318MHz	CLOCK-Generator	CK-410M+
Crystal	24.576MHz	Cardbus Controller	1394
Crystal	25MHz	LAN	BROADCOM LAN
Crystal	24MHz	Finger Printer	AES2501A

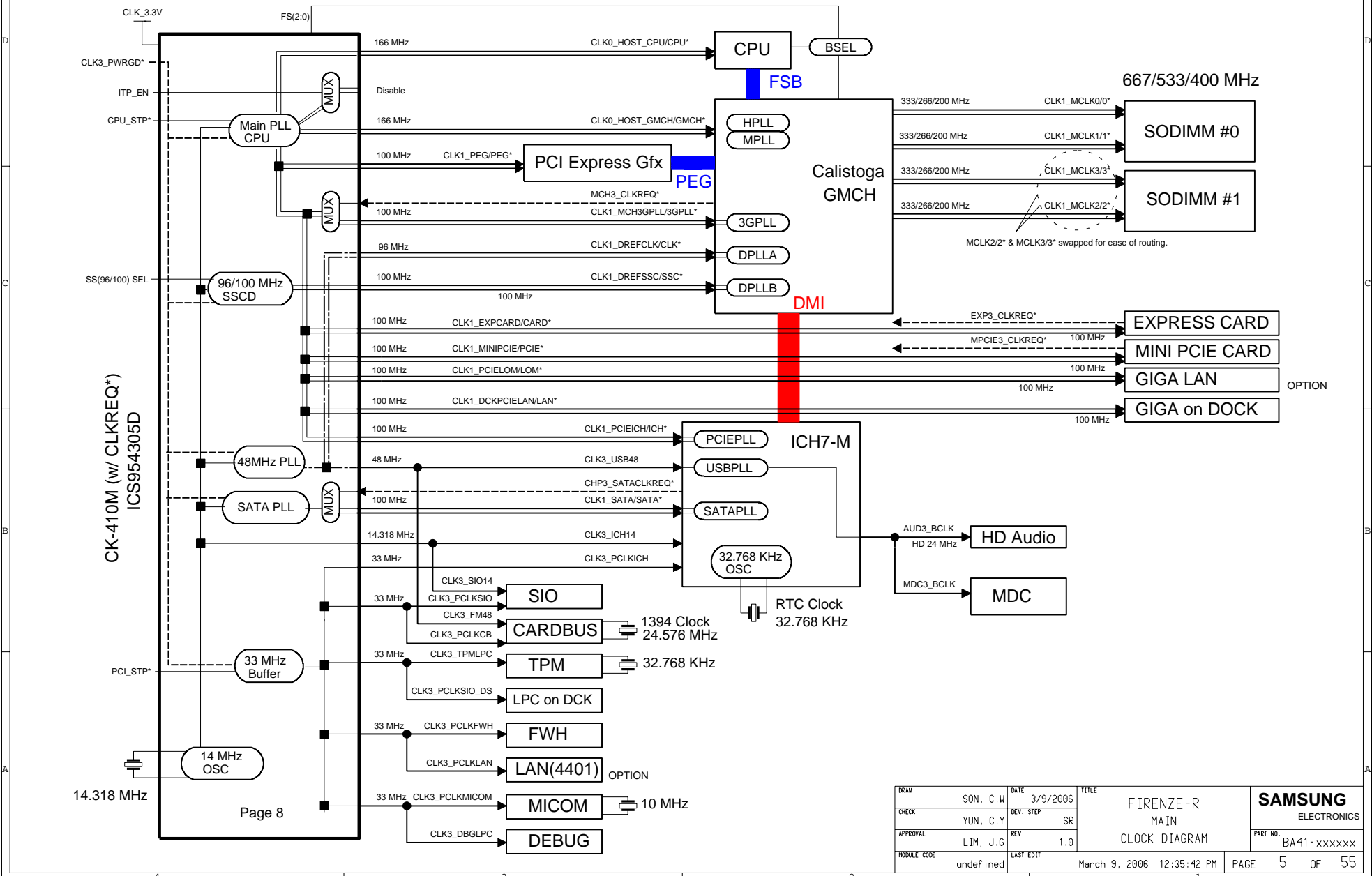
## CPU Core Voltage Table MVP-6

Active Mode		Active/Deeper Sleep Dual Mode Region		Deeper Sleep/Extended Deeper Sleep Dual Mode Region	
VID(6:0)	Voltage	VID(6:0)	Voltage	VID(6:0)	Voltage
0 0 0 0 0 0 0	1.5000 V	0 1 0 1 0 0 0	1.0000 V	1 0 1 0 0 0 1	0.4875 V
0 0 0 0 0 0 1	1.4875 V	0 1 0 1 0 0 0	0.9875 V	1 0 1 0 0 1 0	0.4750 V
0 0 0 0 0 1 0	1.4750 V	0 1 0 1 0 1 0	0.9750 V	1 0 1 0 0 1 1	0.4625 V
0 0 0 0 0 1 1	1.4625 V	0 1 0 1 1 0 1	0.9625 V	1 0 1 0 1 0 0	0.4500 V
0 0 0 0 1 0 0	1.4500 V	0 1 0 1 1 0 0	0.9500 V	1 0 1 0 1 0 1	0.4375 V
0 0 0 0 1 0 1	1.4375 V	0 1 0 1 1 0 1	0.9375 V	1 0 1 0 1 1 0	0.4250 V
0 0 0 0 1 1 0	1.4250 V	0 1 0 1 1 1 0	0.9250 V	1 0 1 0 1 1 1	0.4125 V
0 0 0 0 1 1 1	1.4125 V	0 1 0 1 1 1 1	0.9125 V	1 0 1 1 0 0 0	0.4000 V
0 0 0 1 0 0 0	1.4000 V	0 1 1 0 0 0 0	0.9000 V	1 0 1 1 0 0 1	0.3875 V
0 0 0 1 0 0 1	1.3875 V	0 1 1 0 0 0 1	0.8875 V	1 0 1 1 0 1 0	0.3750 V
0 0 0 1 0 1 0	1.3750 V	0 1 1 0 0 1 0	0.8750 V	1 0 1 1 0 1 1	0.3625 V
0 0 0 1 0 1 1	1.3625 V	0 1 1 0 1 0 1	0.8625 V	1 0 1 1 1 0 0	0.3500 V
0 0 0 1 1 0 0	1.3500 V	0 1 1 0 1 0 0	0.8500 V	1 0 1 1 1 0 1	0.3375 V
0 0 0 1 1 0 1	1.3375 V	0 1 1 0 1 0 1	0.8375 V	1 0 1 1 1 1 0	0.3250 V
0 0 0 1 1 1 0	1.3250 V	0 1 1 0 1 1 0	0.8250 V	1 0 1 1 1 1 1	0.3125 V
0 0 0 1 1 1 1	1.3125 V	0 1 1 0 1 1 1	0.8125 V	1 1 0 0 0 0 0	0.3000 V
0 0 1 0 0 0 0	1.3000 V	0 1 1 1 0 0 0	0.8000 V	1 1 0 0 0 0 1	0.2875 V
0 0 1 0 0 0 1	1.2875 V	0 1 1 1 0 0 1	0.7875 V	1 1 0 0 0 1 0	0.2750 V
0 0 1 0 0 1 0	1.2750 V	0 1 1 1 0 1 0	0.7750 V	1 1 0 0 0 1 1	0.2625 V
0 0 1 0 0 1 1	1.2625 V	0 1 1 1 0 1 1	0.7625 V	1 1 0 0 1 0 0	0.2500 V
0 0 1 0 1 0 0	1.2500 V	0 1 1 1 0 1 0	0.7500 V	1 1 0 0 1 0 1	0.2375 V
0 0 1 0 1 0 1	1.2375 V	0 1 1 1 1 0 1	0.7375 V	1 1 0 0 1 1 0	0.2250 V
0 0 1 0 1 1 0	1.2250 V	0 1 1 1 1 1 0	0.7250 V	1 1 0 0 1 1 1	0.2125 V
0 0 1 0 1 1 1	1.2125 V	0 1 1 1 1 1 1	0.7125 V	1 1 0 1 0 0 0	0.2000 V
0 0 1 1 0 0 0	1.2000 V	0 1 1 1 0 0 0	0.7000 V	1 1 0 1 0 0 1	0.1875 V
0 0 1 1 0 0 1	1.1875 V	1 0 0 0 0 0 1	0.6875 V	1 1 0 1 0 1 0	0.1750 V
0 0 1 1 0 1 0	1.1750 V	1 0 0 0 0 0 0	0.6750 V	1 1 0 1 0 1 1	0.1625 V
0 0 1 1 0 1 1	1.1625 V	1 0 0 0 0 1 1	0.6625 V	1 1 0 1 1 0 0	0.1500 V
0 0 1 1 1 0 0	1.1500 V	1 0 0 0 1 0 0	0.6500 V	1 1 0 1 1 0 1	0.1375 V
0 0 1 1 1 0 1	1.1375 V	1 0 0 0 1 0 1	0.6375 V	1 1 0 1 1 1 0	0.1250 V
0 0 1 1 1 1 0	1.1250 V	1 0 0 0 1 1 0	0.6250 V	1 1 0 1 1 1 1	0.1125 V
0 0 1 1 1 1 1	1.1125 V	1 0 0 0 1 1 1	0.6125 V	1 1 1 0 0 0 0	0.1000 V
0 1 0 0 0 0 0	1.1000 V	1 0 0 1 0 0 0	0.6000 V	1 1 1 0 0 0 1	0.0875 V
0 1 0 0 0 0 1	1.0875 V	1 0 0 1 0 0 1	0.5875 V	1 1 1 0 0 1 0	0.0750 V
0 1 0 0 0 1 0	1.0750 V	1 0 0 1 0 1 0	0.5750 V	1 1 1 0 0 1 1	0.0625 V
0 1 0 0 0 1 1	1.0625 V	1 0 0 1 0 1 1	0.5625 V	1 1 1 0 1 0 0	0.0500 V
0 1 0 0 1 0 0	1.0500 V	1 0 0 1 1 0 0	0.5500 V	1 1 1 0 1 0 1	0.0375 V
0 1 0 0 1 0 1	1.0375 V	1 0 0 1 1 0 1	0.5375 V	1 1 1 0 1 1 0	0.0250 V
0 1 0 0 1 1 0	1.0250 V	1 0 0 1 1 1 0	0.5250 V	1 1 1 1 0 0 0	0.0125 V
0 1 0 0 1 1 1	1.0125 V	1 0 0 1 1 1 1	0.5125 V	1 1 1 1 0 0 1	0.0000 V
0 1 0 1 0 0 0	1.0000 V	1 0 0 1 0 0 0	0.5000 V	1 1 1 1 0 1 0	0.0000 V
				1 1 1 1 0 1 1	0.0000 V
				1 1 1 1 1 0 0	0.0000 V
				1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0	0.0000 V
				1 1 1 1 1 1 1	0.0000 V
				1 1 1 1 1 1 1	0.0000 V

\*Yonah Processor (2.33 GHz / 800 MHz : T8D)

DRAW	SON, C.W	DATE	3/9/2006	TITLE	F I R E N Z E - R	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	SR		MAIN	
APPROVAL	LIM, J.G	REV	1.0		BOARD INFORMATION	PART NO. BA41-xxxxxx
MODULE CODE	undef ined	LAST EDIT	March 9, 2006 12:35:42 PM		PAGE	4 OF 55

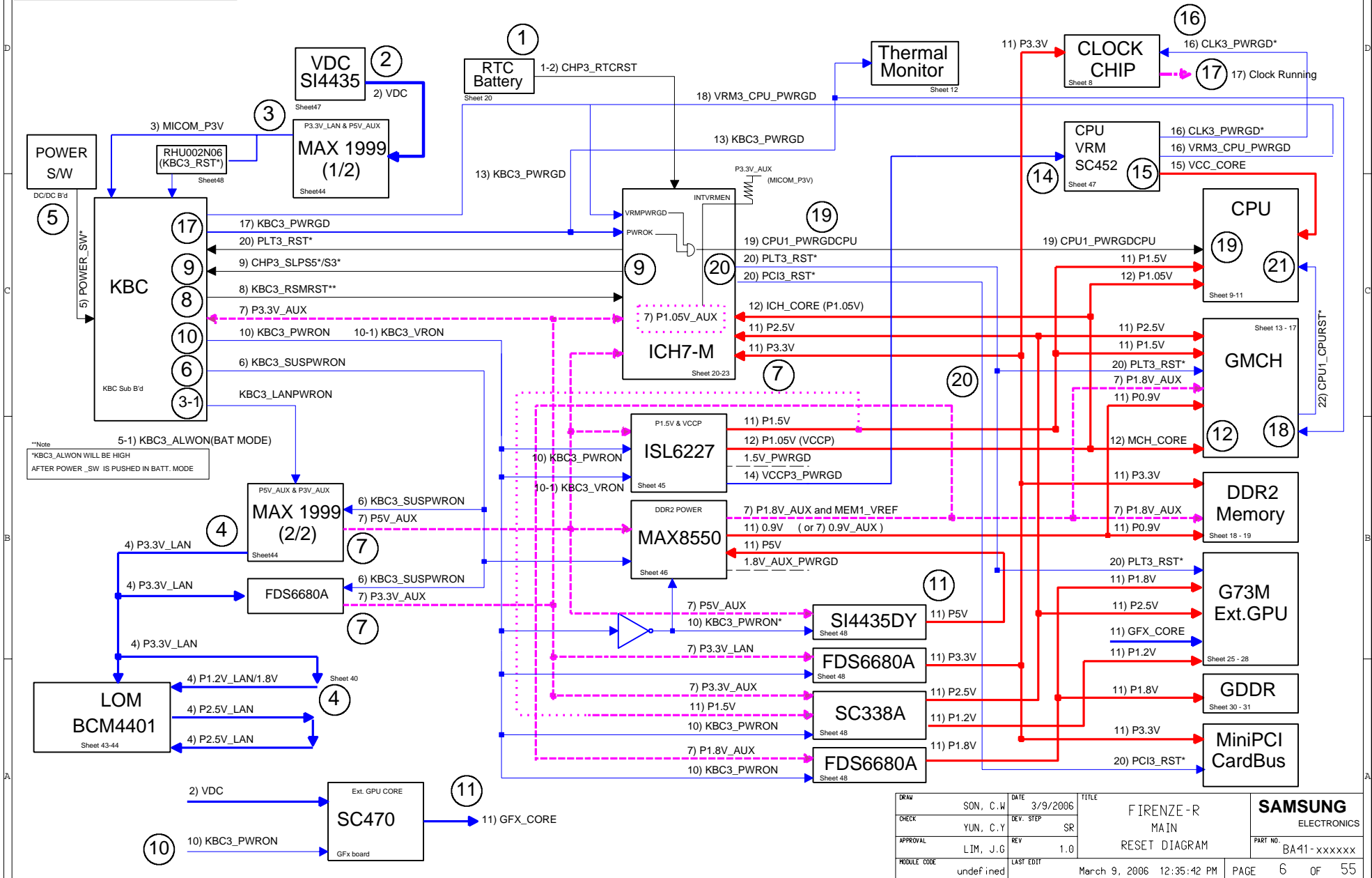
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DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN CLOCK DIAGRAM	<b>SAMSUNG</b> ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	SR		PART NO.	
APPROVAL	LIM, J.G	REV	1.0		BA41-xxxxxx	
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# RESET DIAGRAM



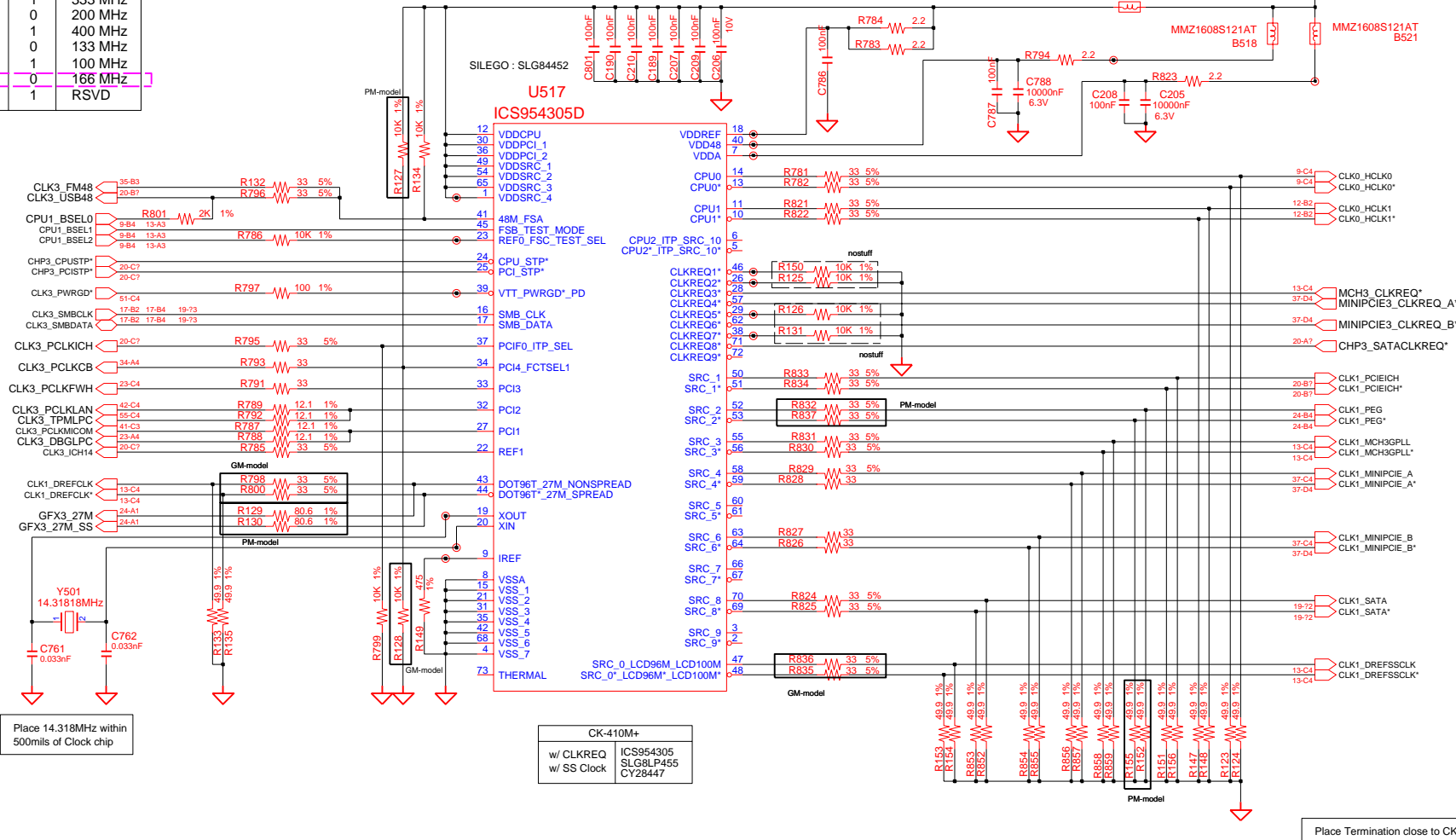
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CHECK	YUN, C.Y	DEV. STEP	SR			
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FCTSEL1(43,44,47,48)	1 : 27M & SRC0	0 : DOT96 & LCD100
ITP_EN (5,6)	1 : CPU_ITP pair	0 : SRC pair

CPU			
FSA	FSB	FSC	HOST CLK
BSEL0	BSEL1	BSEL2	
0	0	0	266 MHz
0	0	1	333 MHz
0	1	0	200 MHz
0	1	1	400 MHz
1	0	0	133 MHz
1	0	1	100 MHz
1	1	0	166 MHz
1	1	1	RSVD



Place 14.318MHz within 500mils of Clock chip

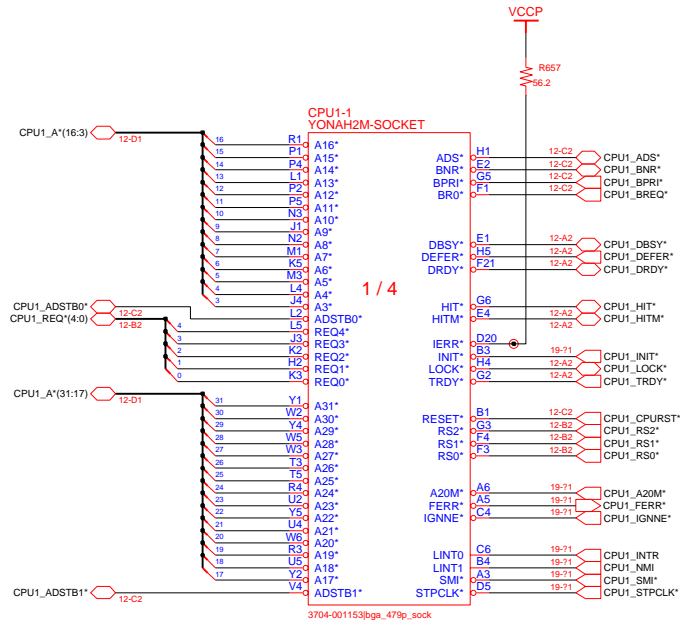
CK-410M+	
w/ CLKREQ	ICS954305
w/ SS Clock	SLG8LP455
	CY28447

Place Termination close to CK-410M

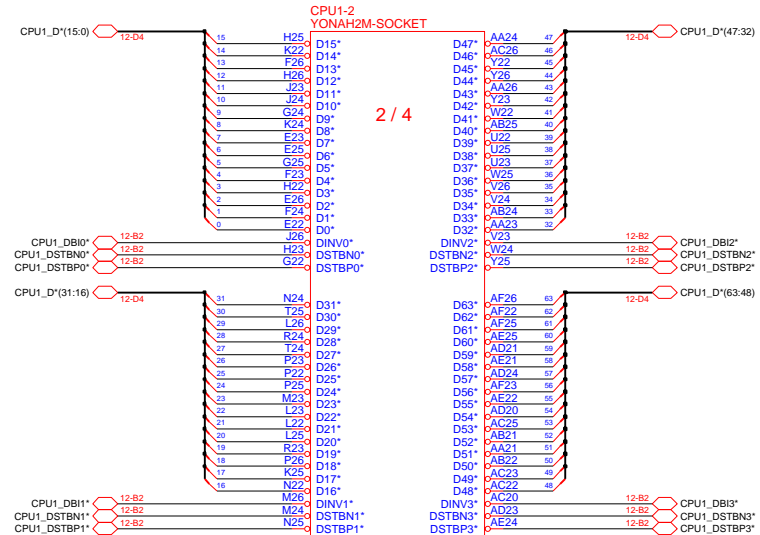
DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN CLOCK GENERATOR	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-xxxxxx
CHECK	YUN, C.Y	DEV. STEP	SR			
APPROVAL	LIM, J.G	REV	1.0			
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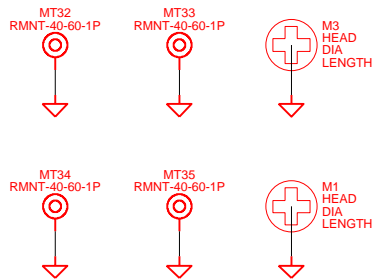
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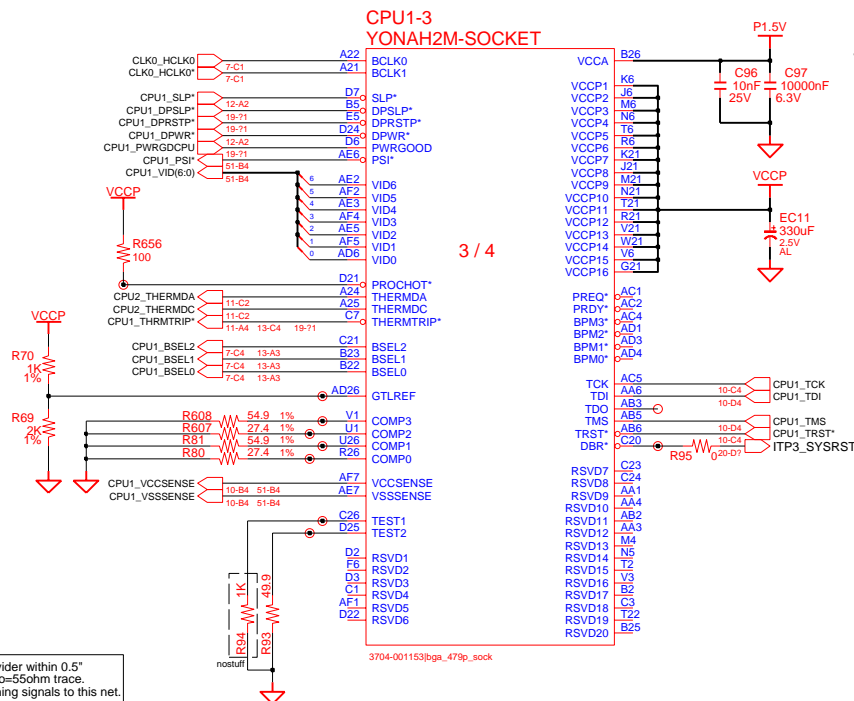


DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN CPU(1/3)	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-xxxxxx
CHECK	YUN, C.Y	DEV. STEP	SR			
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**CPU Core Voltage Table** MVP-6

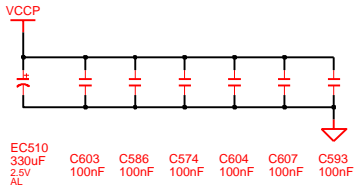
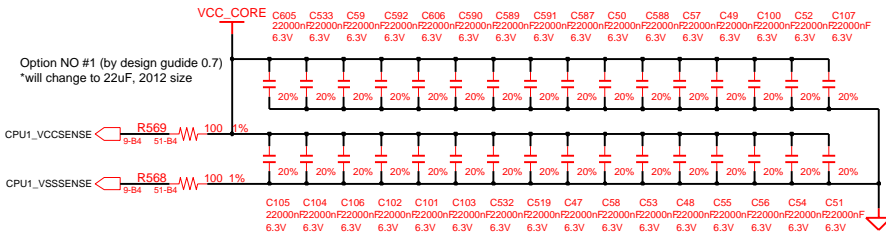
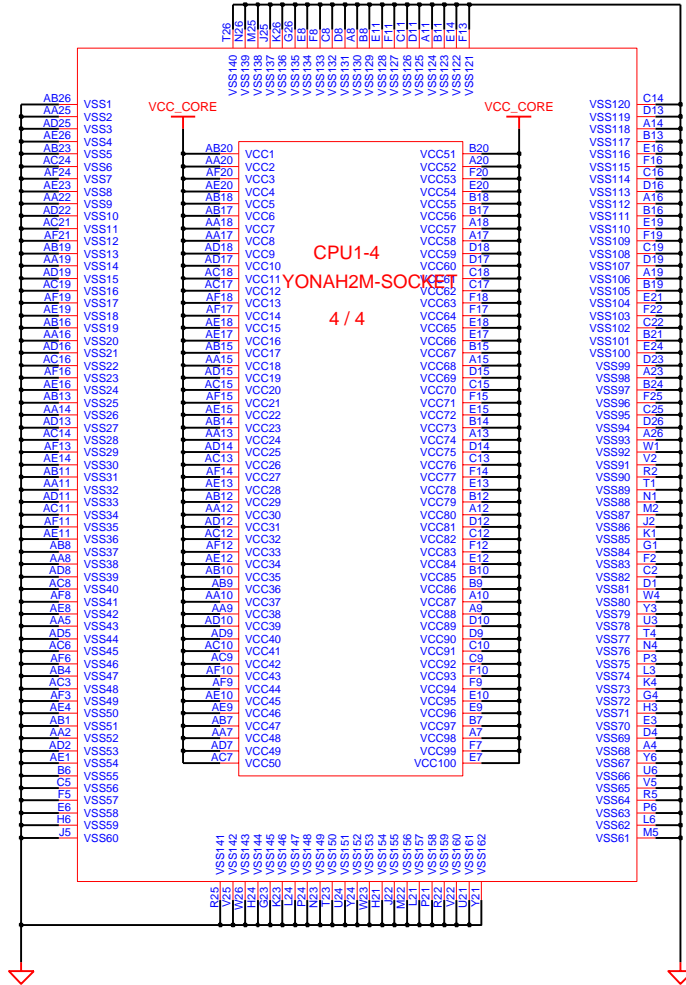
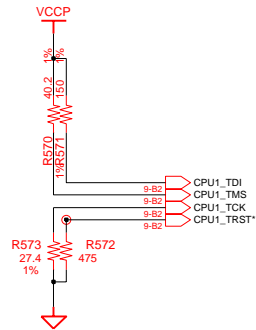
Active Mode		Active/Deeper Sleep Dual Mode Region		Deeper Sleep/Extended Deeper Sleep Dual Mode Region	
VID(6:0)	Voltage	VID(6:0)	Voltage	VID(6:0)	Voltage
0 0 0 0 0 0 0	1.5000 V	0 1 0 1 0 0 0	1.0000 V	1 0 1 0 0 0 1	0.4875 V
0 0 0 0 0 0 1	1.4875 V	0 1 0 1 0 0 1	0.9875 V	1 0 1 0 0 1 0	0.4750 V
0 0 0 0 0 1 0	1.4750 V	0 1 0 1 0 1 0	0.9750 V	1 0 1 0 0 1 1	0.4625 V
0 0 0 0 0 1 1	1.4625 V	0 1 0 1 1 0 1	0.9625 V	1 0 1 0 1 0 0	0.4500 V
0 0 0 0 1 0 0	1.4500 V	0 1 0 1 1 0 0	0.9500 V	1 0 1 0 1 0 1	0.4375 V
0 0 0 0 1 0 1	1.4375 V	0 1 0 1 1 1 0	0.9375 V	1 0 1 0 1 1 0	0.4250 V
0 0 0 0 1 1 0	1.4250 V	0 1 0 1 1 1 0	0.9250 V	1 0 1 0 1 1 1	0.4125 V
0 0 0 0 1 1 1	1.4125 V	0 1 0 1 1 1 1	0.9125 V	1 0 1 1 0 0 0	0.4000 V
0 0 0 1 0 0 0	1.4000 V	0 1 1 0 0 0 0	0.9000 V	1 0 1 1 0 0 1	0.3875 V
0 0 0 1 0 0 1	1.3875 V	0 1 1 0 0 0 1	0.8875 V	1 0 1 1 0 1 0	0.3750 V
0 0 0 1 0 1 0	1.3750 V	0 1 1 0 0 1 0	0.8750 V	1 0 1 1 0 1 1	0.3625 V
0 0 0 1 0 1 1	1.3625 V	0 1 1 0 0 1 1	0.8625 V	1 0 1 1 1 0 0	0.3500 V
0 0 0 1 1 0 0	1.3500 V	0 1 1 0 1 0 0	0.8500 V	1 0 1 1 1 0 1	0.3375 V
0 0 0 1 1 0 1	1.3375 V	0 1 1 0 1 0 1	0.8375 V	1 0 1 1 1 1 0	0.3250 V
0 0 0 1 1 1 0	1.3250 V	0 1 1 0 1 1 0	0.8250 V	1 0 1 1 1 1 1	0.3125 V
0 0 0 1 1 1 1	1.3125 V	0 1 1 1 0 1 1	0.8125 V	1 1 0 0 0 0 0	0.3000 V
0 0 1 0 0 0 0	1.3000 V	0 1 1 1 0 0 0	0.8000 V	1 1 0 0 0 0 1	0.2875 V
0 0 1 0 0 0 1	1.2875 V	0 1 1 1 0 0 1	0.7875 V	1 1 0 0 0 1 0	0.2750 V
0 0 1 0 0 1 0	1.2750 V	0 1 1 1 0 1 0	0.7750 V	1 1 0 0 0 1 1	0.2625 V
0 0 1 0 0 1 1	1.2625 V	0 1 1 1 1 0 1	0.7625 V	1 1 0 0 1 0 0	0.2500 V
0 0 1 0 1 0 0	1.2500 V	0 1 1 1 1 0 0	0.7500 V	1 1 0 0 1 0 1	0.2375 V
0 0 1 0 1 0 1	1.2375 V	0 1 1 1 1 0 1	0.7375 V	1 1 0 0 1 1 0	0.2250 V
0 0 1 0 1 1 0	1.2250 V	0 1 1 1 1 1 0	0.7250 V	1 1 0 0 1 1 1	0.2125 V
0 0 1 0 1 1 1	1.2125 V	0 1 1 1 1 1 1	0.7125 V	1 1 0 1 0 0 0	0.2000 V
0 0 1 1 0 0 0	1.2000 V	1 0 0 0 0 0 0	0.7000 V	1 1 0 1 0 0 1	0.1875 V
0 0 1 1 0 0 1	1.1875 V	1 0 0 0 0 0 1	0.6875 V	1 1 0 1 0 1 0	0.1750 V
0 0 1 1 0 1 0	1.1750 V	1 0 0 0 0 1 0	0.6750 V	1 1 0 1 0 1 1	0.1625 V
0 0 1 1 0 1 1	1.1625 V	1 0 0 0 0 1 1	0.6625 V	1 1 0 1 1 0 0	0.1500 V
0 0 1 1 1 0 0	1.1500 V	1 0 0 0 0 1 0	0.6500 V	1 1 0 1 1 0 1	0.1375 V
0 0 1 1 1 0 1	1.1375 V	1 0 0 0 0 1 1	0.6375 V	1 1 0 1 1 1 0	0.1250 V
0 0 1 1 1 1 0	1.1250 V	1 0 0 0 1 1 0	0.6250 V	1 1 0 1 1 1 1	0.1125 V
0 0 1 1 1 1 1	1.1125 V	1 0 0 0 1 1 1	0.6125 V	1 1 1 0 0 0 0	0.1000 V
0 1 0 0 0 0 0	1.1000 V	1 0 0 1 0 0 0	0.6000 V	1 1 1 0 0 0 1	0.0875 V
0 1 0 0 0 0 1	1.0875 V	1 0 0 1 0 0 1	0.5875 V	1 1 1 0 0 1 0	0.0750 V
0 1 0 0 0 1 0	1.0750 V	1 0 0 1 0 1 0	0.5750 V	1 1 1 0 0 1 1	0.0625 V
0 1 0 0 0 1 1	1.0625 V	1 0 0 1 1 0 1	0.5625 V	1 1 1 0 1 0 0	0.0500 V
0 1 0 0 1 0 0	1.0500 V	1 0 0 1 1 0 0	0.5500 V	1 1 1 0 1 0 1	0.0375 V
0 1 0 0 1 0 1	1.0375 V	1 0 0 1 1 0 1	0.5375 V	1 1 1 0 1 1 0	0.0250 V
0 1 0 0 1 1 0	1.0250 V	1 0 0 1 1 1 0	0.5250 V	1 1 1 0 1 1 1	0.0125 V
0 1 0 0 1 1 1	1.0125 V	1 0 0 1 1 1 1	0.5125 V	1 1 1 1 0 0 0	0.0000 V
		1 0 0 1 1 1 1	0.5000 V	1 1 1 1 0 0 1	0.0000 V
				1 1 1 1 0 1 0	0.0000 V
				1 1 1 1 0 1 1	0.0000 V
				1 1 1 1 1 0 0	0.0000 V
				1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0	0.0000 V
				1 1 1 1 1 1 1	0.0000 V
				***11111111** : 0V power good asserted.	

\*Yonah Processor (2.33 GHz / 800 MHz : TBD)

DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN CPU(2/3)	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-xxxxxx
CHECK	YUN, C.Y	DEV. STEP	SR			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undef ined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	9 OF 55	

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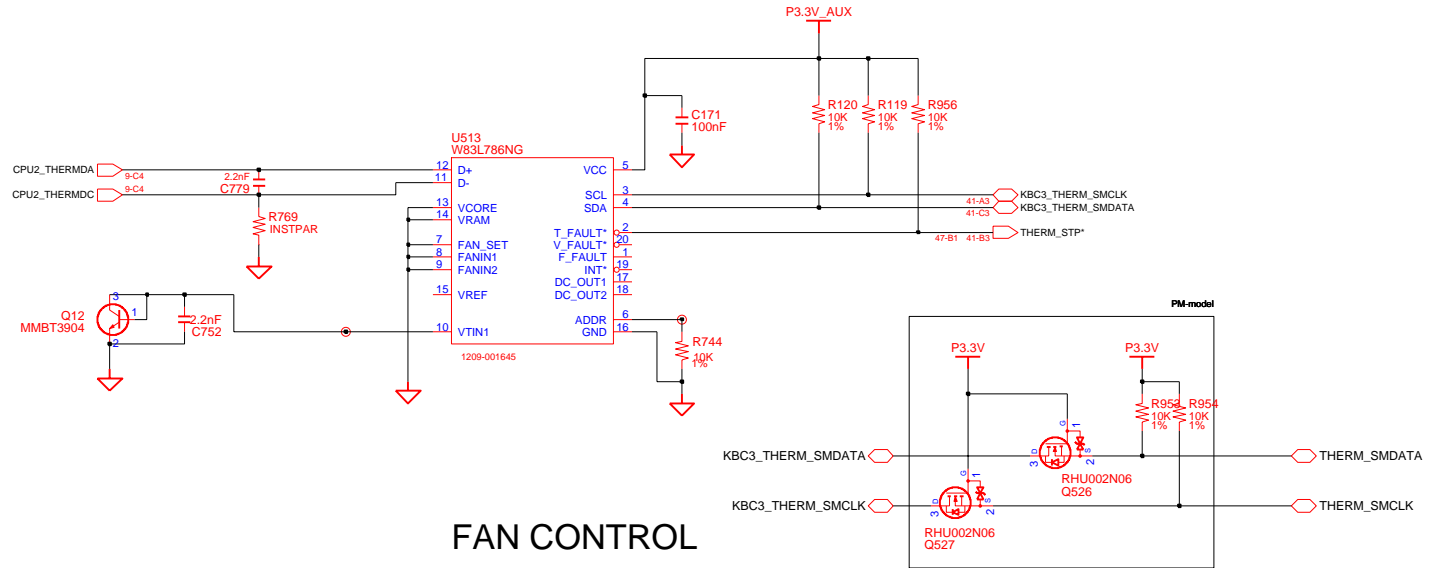


DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN CPU(3/3)	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-xxxxxx
CHECK	YUN, C.Y	DEV. STEP	SR			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undef ined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	10 OF 55	

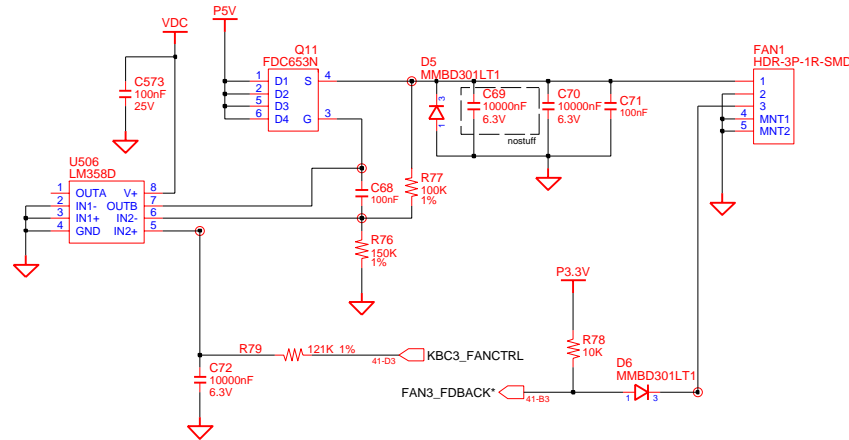
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### CPU/GFX Thermal Sensor



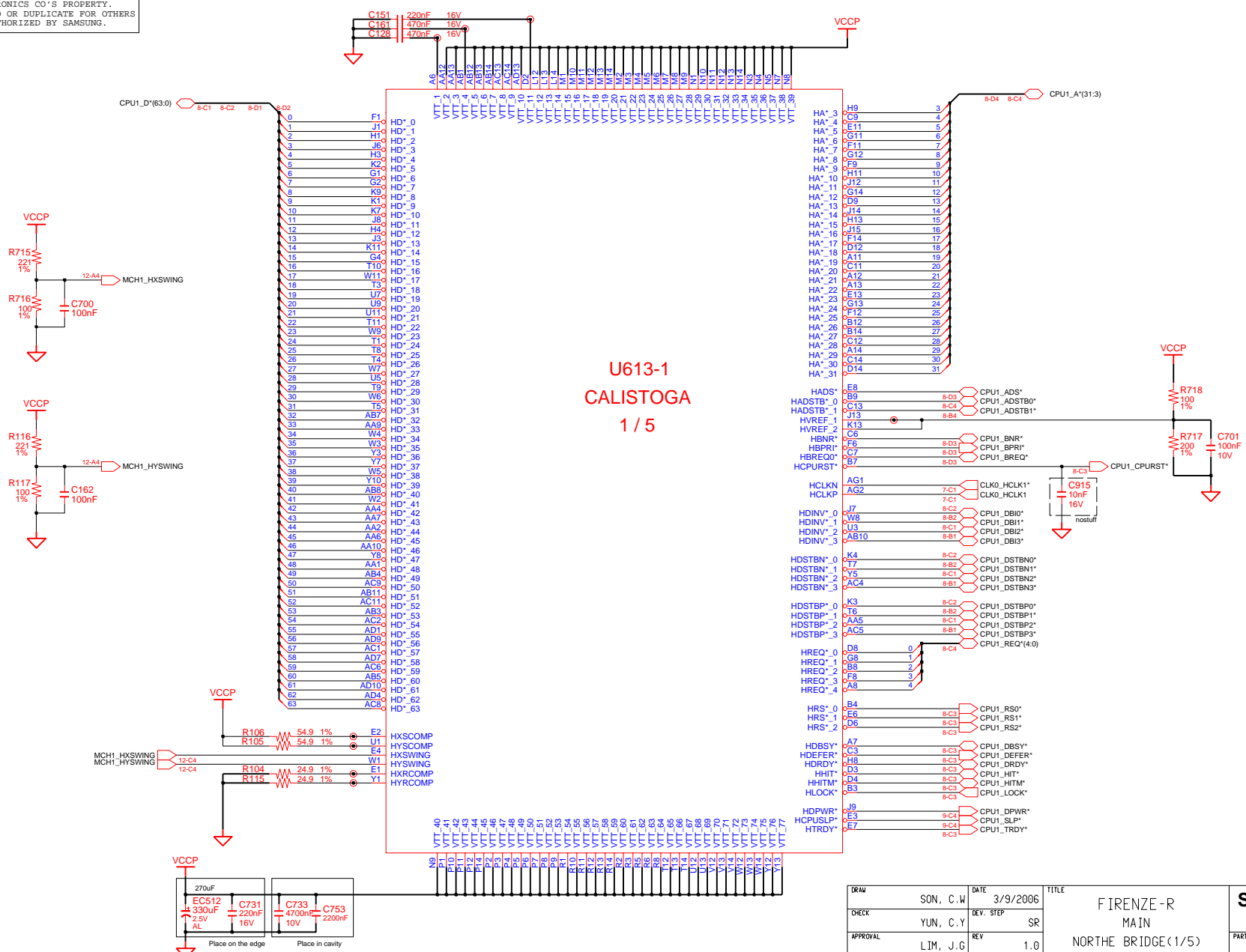
### FAN CONTROL



DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN	<b>SAMSUNG</b> ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	SR	REV	1.0	
APPROVAL	LIM, J.G	REV	1.0	THERMAL SENSOR/FAN CTRL	PART NO.	BA41-xxxxxx
MODULE CODE	undef ined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	11	OF 55

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**U613-1  
CALISTOGA  
1 / 5**

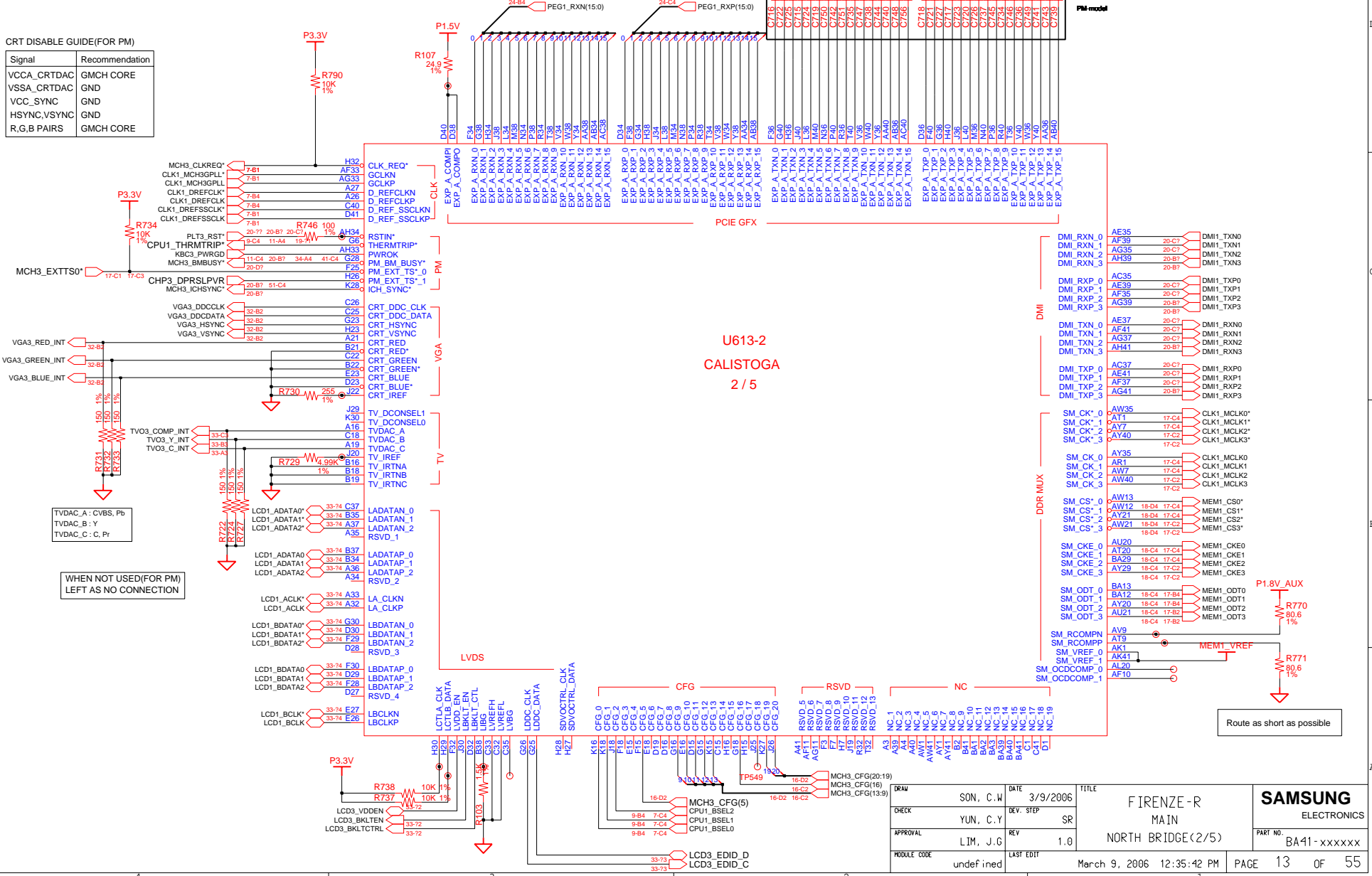
DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN	<b>SAMSUNG</b> ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	SR	NORTHE BRIDGE(1/5)		
APPROVAL	LIM, J.G	REV	1.0			PART NO. BA41-xxxxxx
MODULE CODE	undef ined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	12	OF 55

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**CRT DISABLE GUIDE(FOR PM)**

Signal	Recommendation
VCCA_CRTDAC	GMCH CORE
VSSA_CRTDAC	GND
VCC_SYNC	GND
HSYNC_VSYNC	GND
R,G,B PAIRS	GMCH CORE



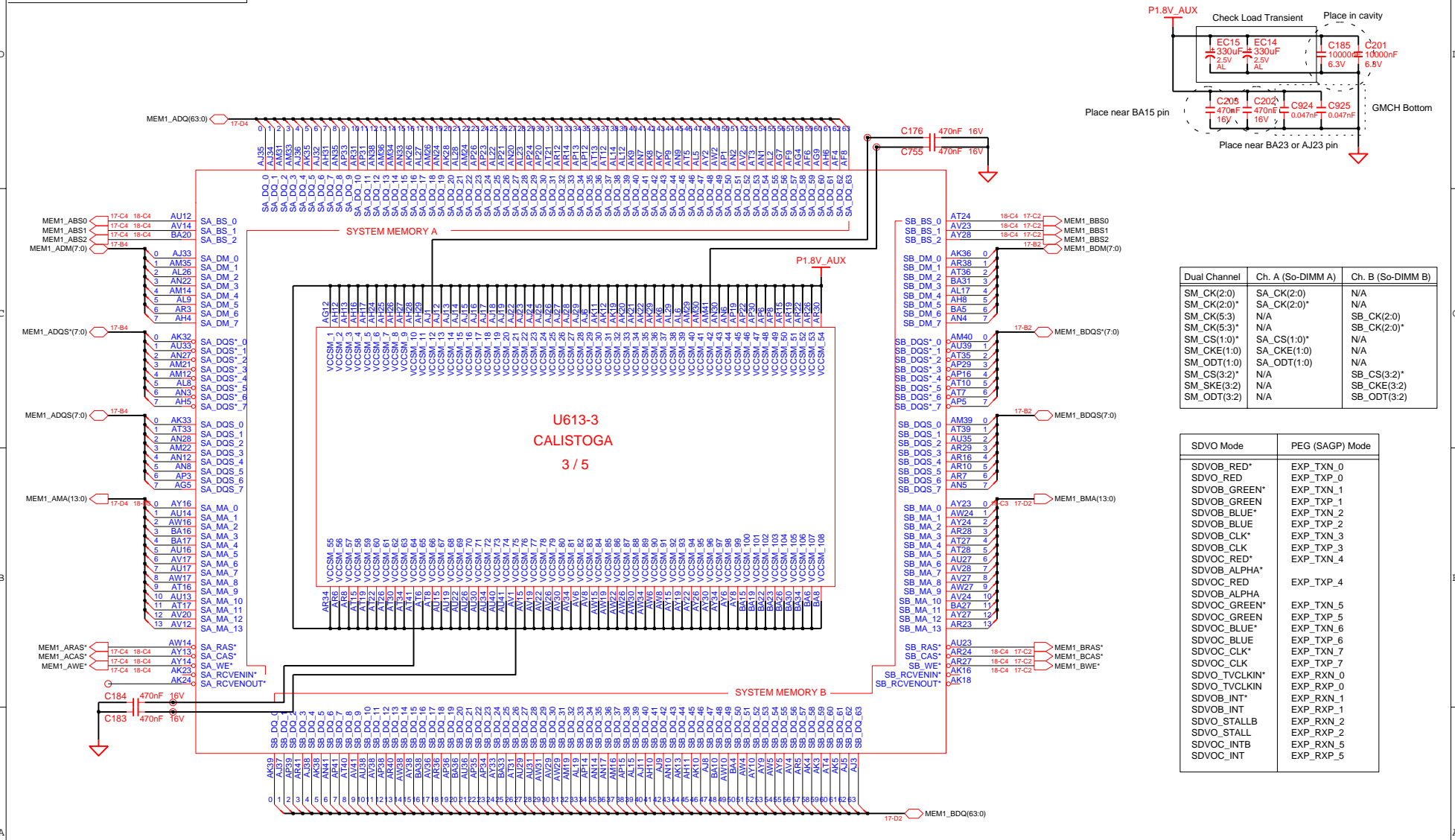
WHEN NOT USED(FOR PM)  
LEFT AS NO CONNECTION

Route as short as possible

DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE+R MAIN NORTH BRIDGE(2/5)	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-xxxxxx
CHECK	YUN, C.Y	DEV. STEP	SR			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undef ined	LAST EDIT				
		March 9, 2006 12:35:42 PM			PAGE 13 OF 55	

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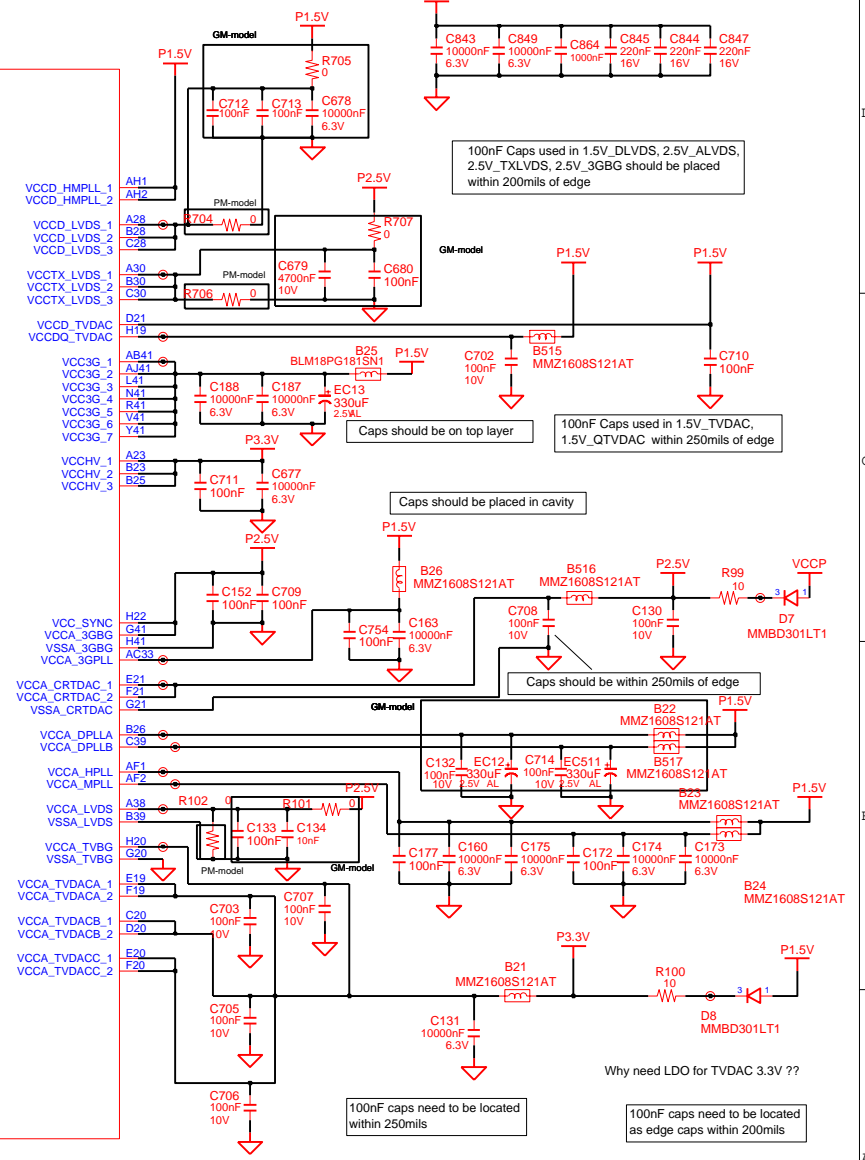
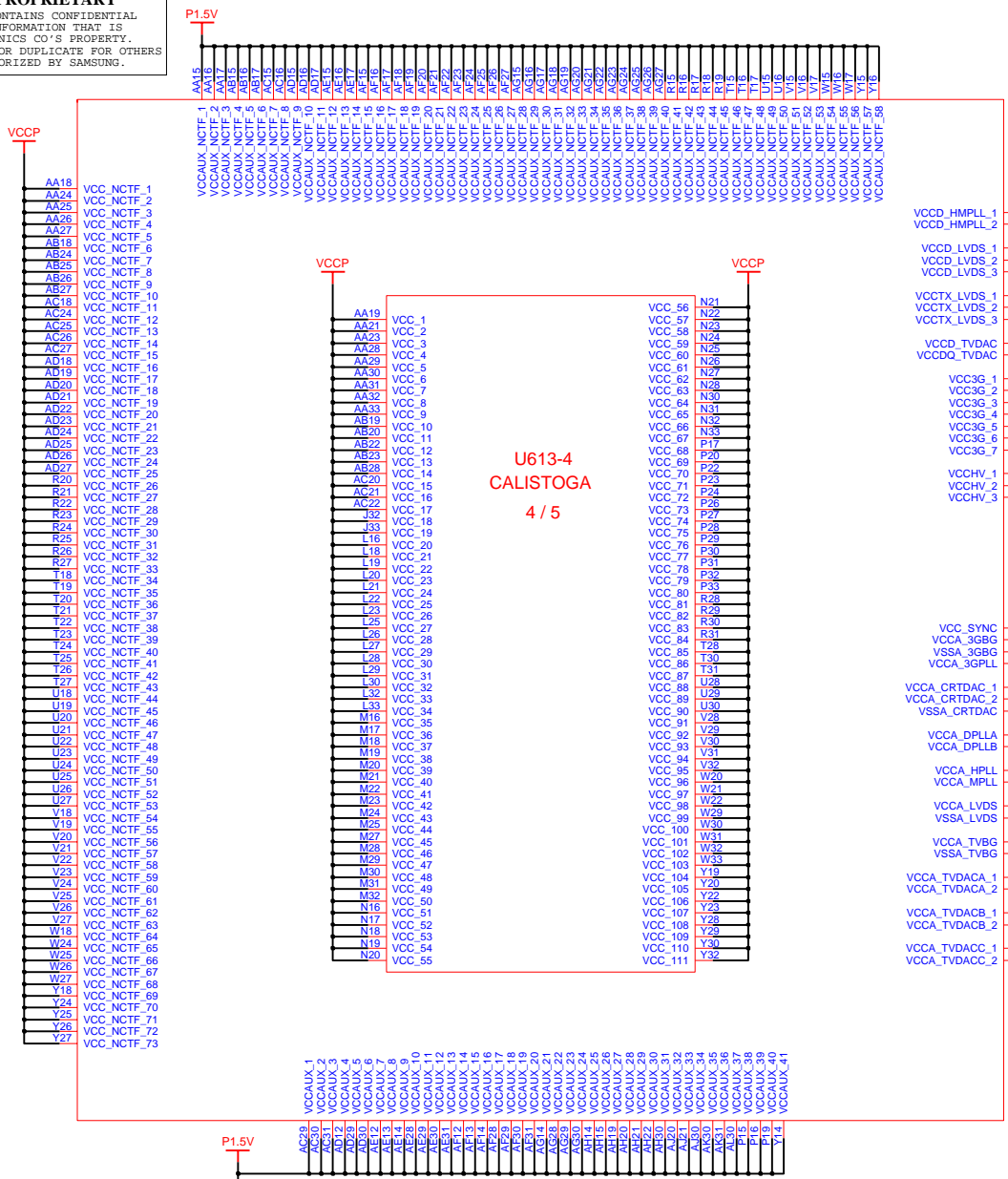


Dual Channel	Ch. A (So-DIMM A)	Ch. B (So-DIMM B)
SM_CK(2:0)	SA_CK(2:0)	N/A
SM_CK(2:0)*	SA_CK(2:0)*	N/A
SM_CK(5:3)	N/A	SB_CK(2:0)
SM_CK(5:3)*	N/A	SB_CK(2:0)*
SM_CS(1:0)	SA_CS(1:0)*	N/A
SM_CKE(1:0)	SA_CKE(1:0)	N/A
SM_ODT(1:0)	SA_ODT(1:0)	N/A
SM_CS(3:2)	N/A	SB_CS(3:2)*
SM_SKE(3:2)	N/A	SB_CKE(3:2)
SM_ODT(3:2)	N/A	SB_ODT(3:2)

SDVO Mode	PEG (SAGP) Mode
SDVOB_RED*	EXP_TXN_0
SDVO_RED	EXP_TXP_0
SDVOB_GREEN*	EXP_TXN_1
SDVOB_GREEN	EXP_TXP_1
SDVOB_BLUE*	EXP_TXN_2
SDVOB_BLUE	EXP_TXP_2
SDVOB_CLK*	EXP_TXN_3
SDVOB_CLK	EXP_TXP_3
SDVOC_RED*	EXP_TXN_4
SDVOC_ALPHA*	EXP_TXP_4
SDVOC_RED	EXP_TXN_5
SDVOC_ALPHA	EXP_TXP_5
SDVOC_GREEN*	EXP_TXN_6
SDVOC_GREEN	EXP_TXP_6
SDVOC_BLUE*	EXP_TXN_7
SDVOC_BLUE	EXP_TXP_7
SDVOC_CLK*	EXP_TXN_8
SDVOC_CLK	EXP_TXP_8
SDVO_TVCLKIN*	EXP_RXN_0
SDVO_TVCLKIN	EXP_RXP_0
SDVOB_INT*	EXP_RXN_1
SDVOB_INT	EXP_RXP_1
SDVO_STALLB	EXP_RXN_2
SDVO_STALL	EXP_RXP_2
SDVOC_INTB	EXP_RXN_5
SDVOC_INT	EXP_RXP_5

DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN NORTH BRIDGE(3/5)	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-xxxxxx
CHECK	YUN, C.Y	DEV. STEP	SR			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undef ined	LAST EDIT	March 9, 2006 12:35:42 PM			
				PAGE	14 OF 55	

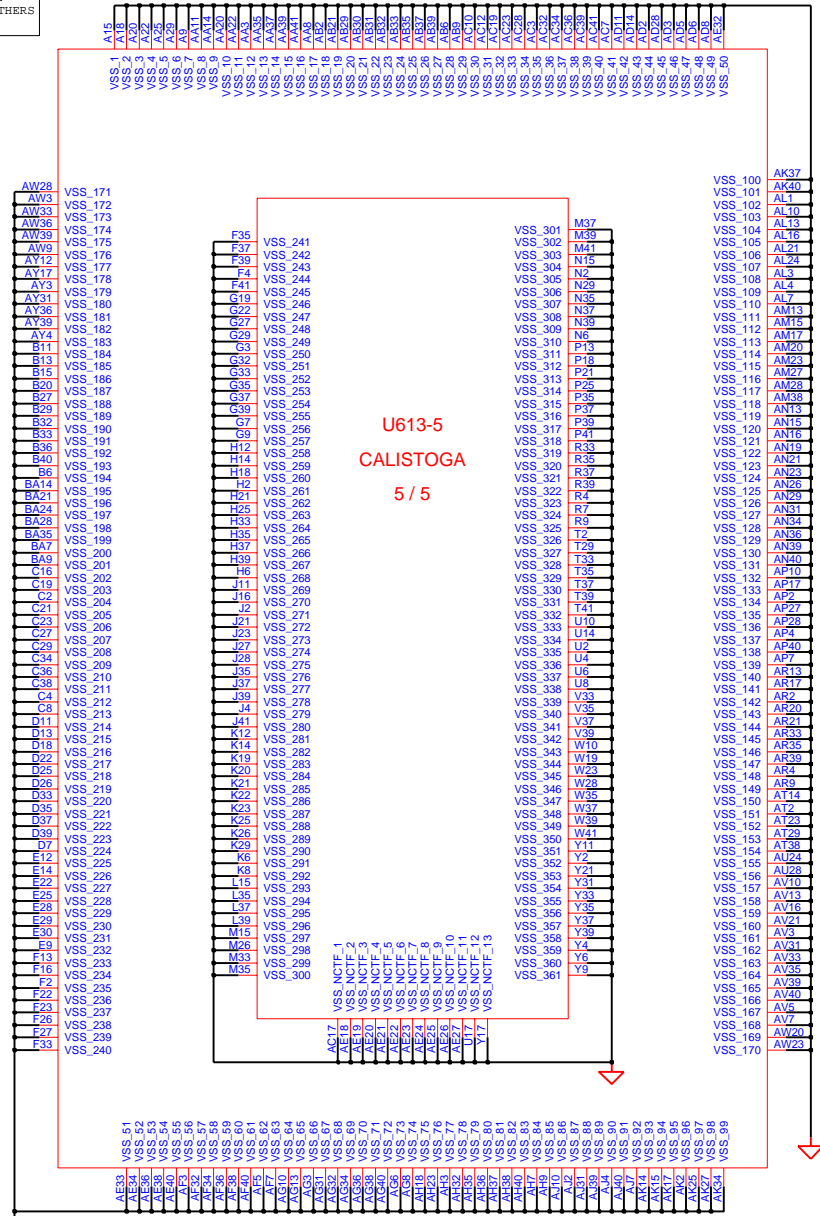
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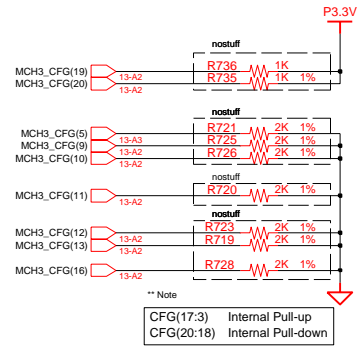
DRAW	SON, C.W.	DATE	3/9/2006	TITLE	FIRENZE -R MAIN	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-xxxxxx
CHECK	YUN, C.Y.	DEV. STEP	SR	NORTH BRIDGE (4/5)		
APPROVAL	LIM, J.G.	REV	1.0	PAGE 15 OF 55		
MODULE CODE	undef ined	LAST EDIT	March 9, 2006 12:35:42 PM			

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U613-5  
CALISTOGA  
5/5



\*\* Note \*POCAFE-10 Only (Remove in MP Model)

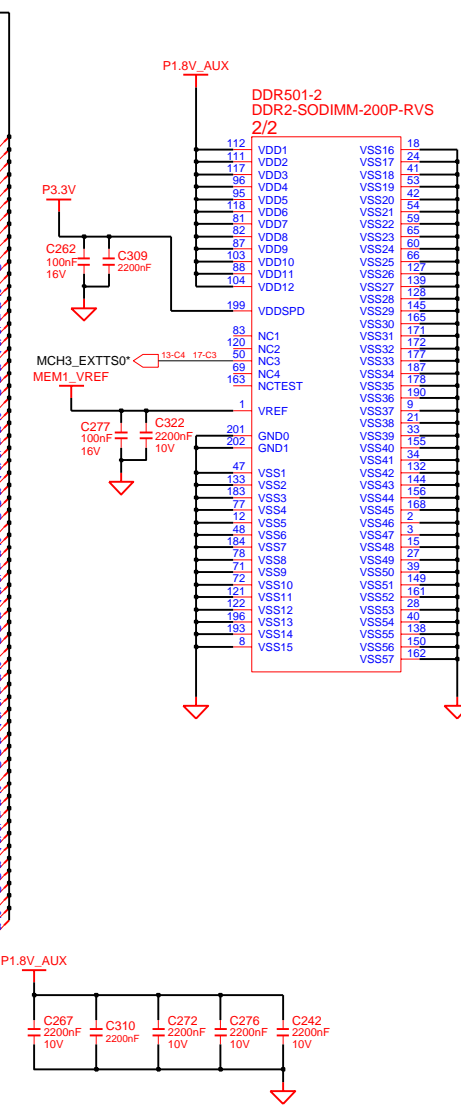
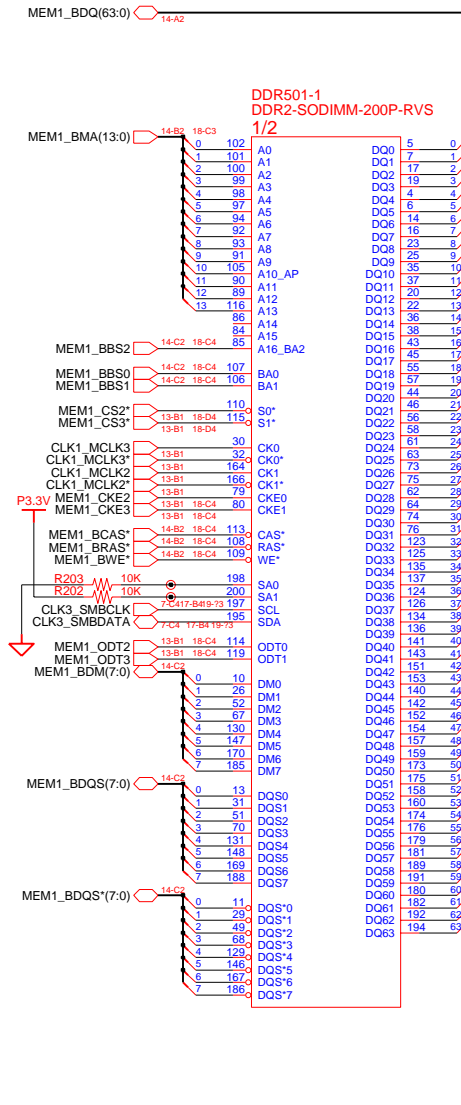
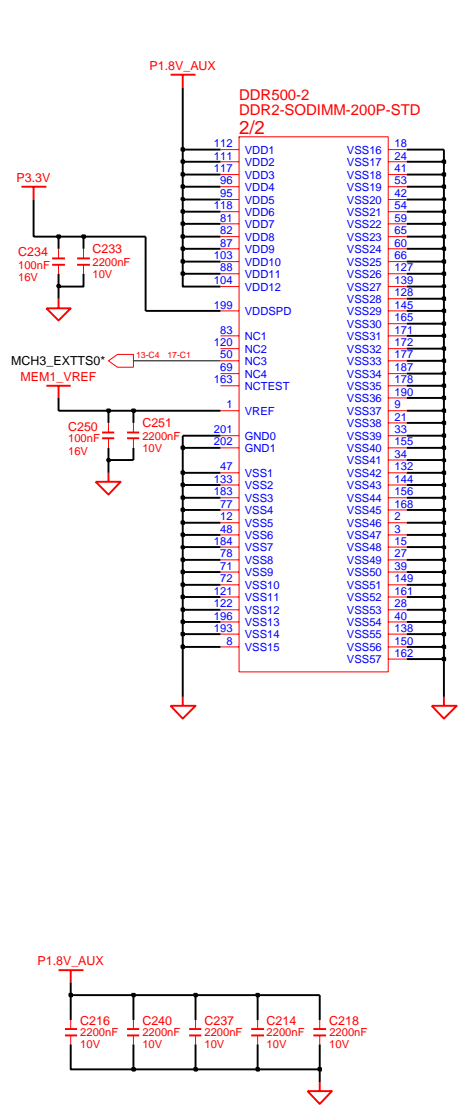
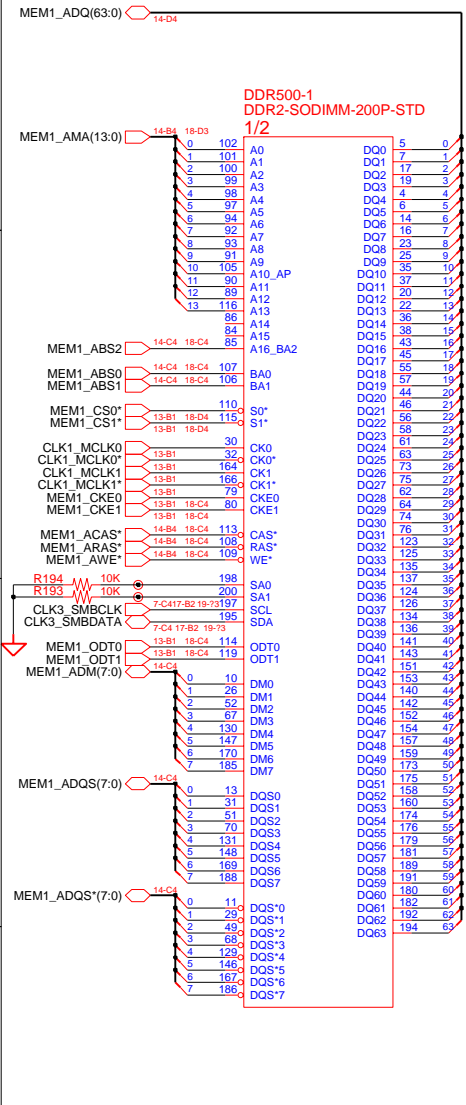
CFG#	Current Setting (def.: default Option)	
	Low	High
CFG(5)	DMix2	DMix4 (def.)
CFG(6)	Reserved	DDR-II (def.)
CFG(7)	DT/Transportable	Mobile CPU (def.)
CFG(9)	PEG Reversal	Normal
CFG(16)	Dynamic ODT	Dynamic ODT
	Disabled	Enabled (def.)
CFG(18)	VCC 1.05V (def.)	VCC 1.5V
CFG(19)	DMI Lane Normal	DMI Lane Reversal
CFG(20)	SDVO or PCIE X1 Only(def.)	SDVO and PCIE X1 Simultaneously

When CFG 13:12 are pulled down to '00', certain clocks within Calistoga will become free-running clocks. This will lead to a rise in avg. power, but eliminates any possible clock-timing marginalities involved in clock power-up/power-down. Intel strongly recommends leaving CFG 13:12 = NC (Internal PU to '11) to ensure low avg.power.

DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN NORTH BRIDGE(5/5)	<b>SAMSUNG</b> ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	SR		PART NO. BA41-xxxxxx	
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undef:ined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	16	OF 55



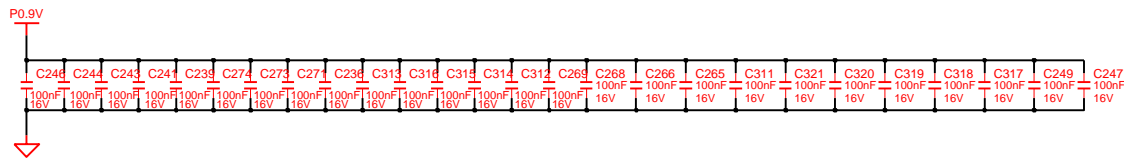
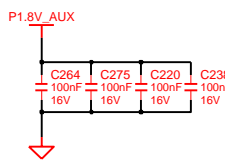
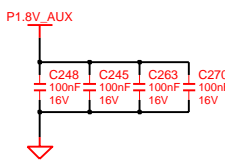
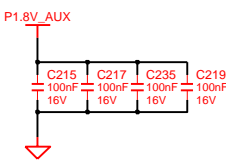
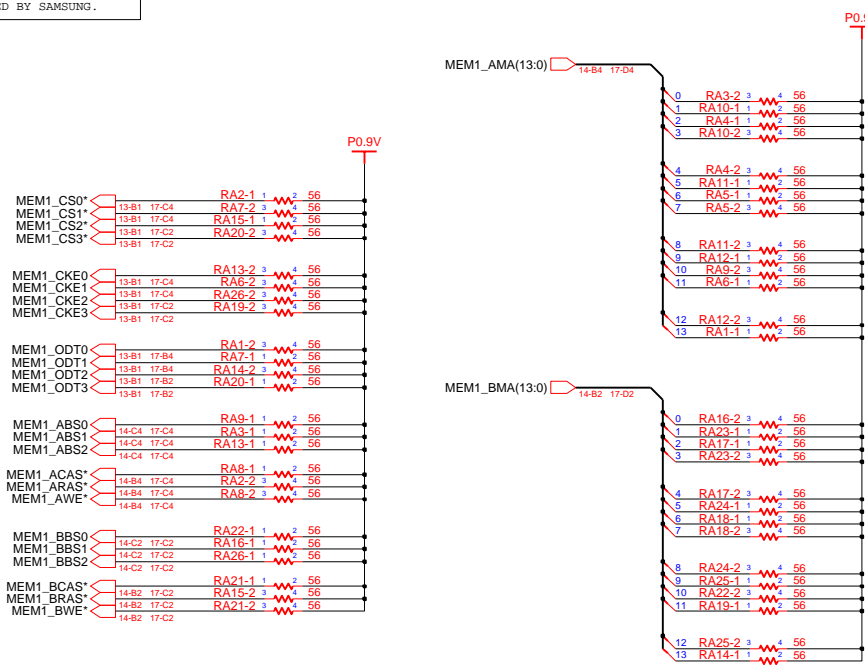
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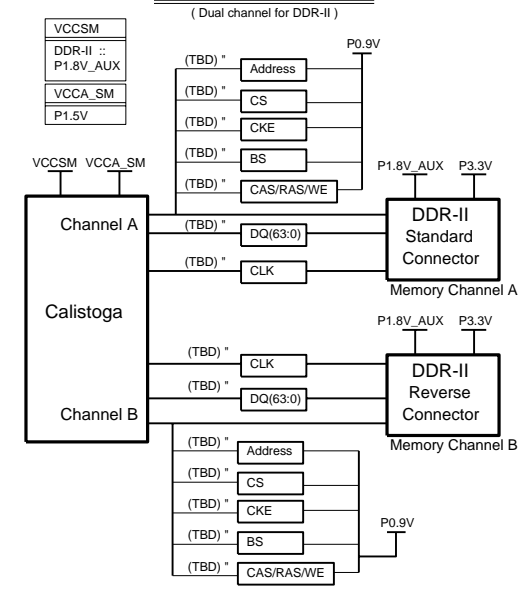
DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-xxxxxx
CHECK	YUN, C.Y	DEV. STEP	SR	MAIN		
APPROVAL	LIM, J.G	REV	1.0	DDR2-SODIMM		
MODULE CODE	undef:ined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	17 OF 55	

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**Memory Topology**



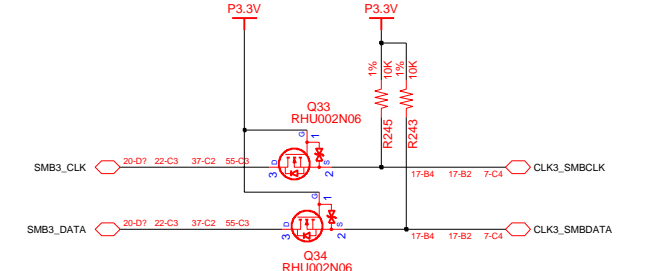
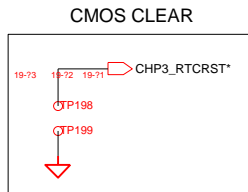
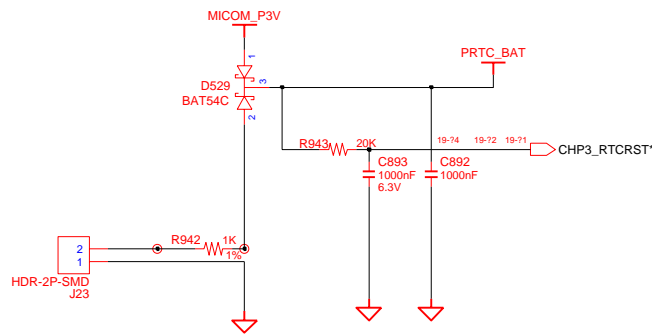
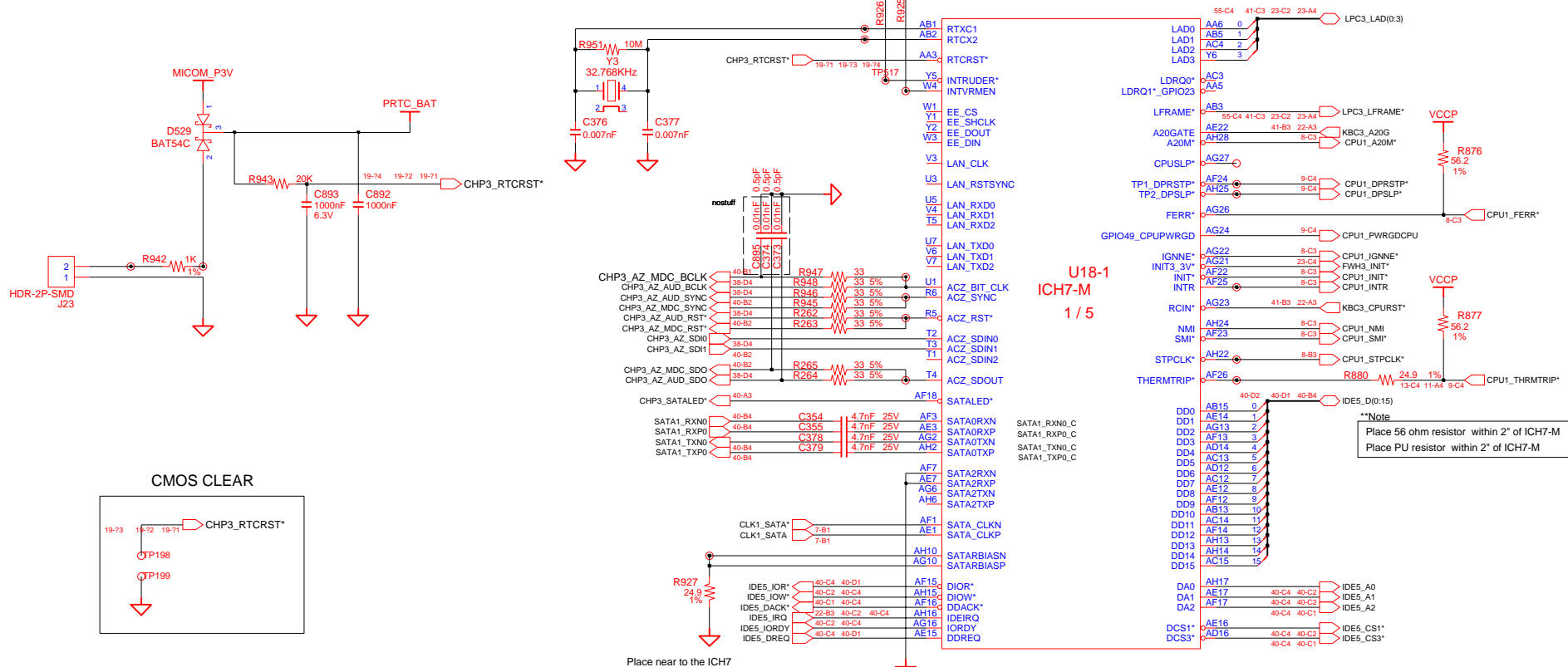
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CHECK	YUN, C.Y	DEV. STEP	SR	REV	1.0	
APPROVAL	LIM, J.G	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	18 OF 55	PART NO. BA41-xxxxxx
MODULE CODE	undef ined					

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**\*\*Note**

Internal VR Strap	
Enable	Pull up (VccSus1_05 : NC)
Disable	Pull down

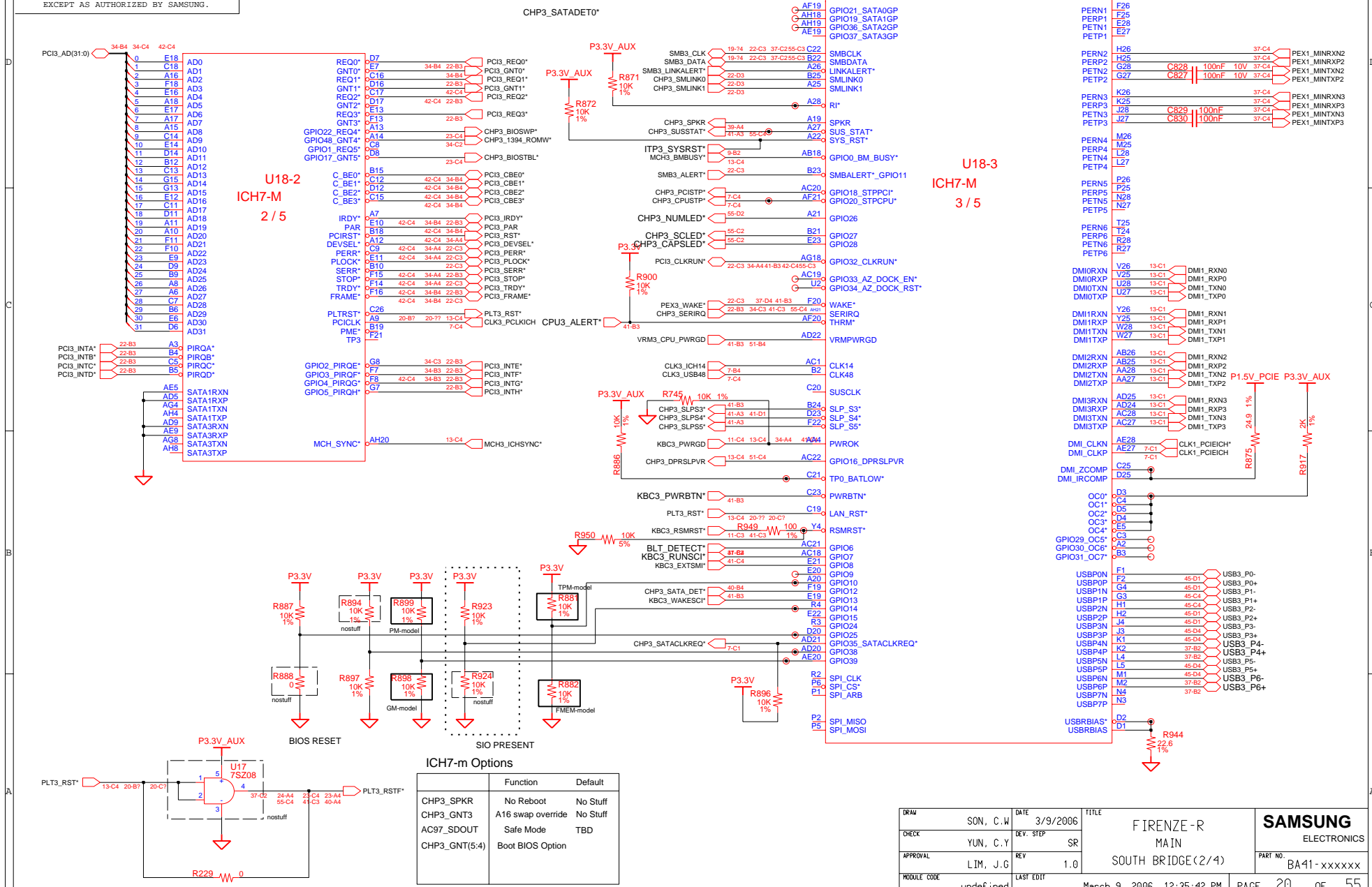


DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN SOUTH BRIDGE(1/4)	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-xxxxxx
CHECK	YUN, C.Y	DEV. STEP	SR			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undefined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	19 OF 55	

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AC caps : PCIe need to be within 250mils of the driver  
Resistor for Test : Place Stuffed Option to minimize stubs

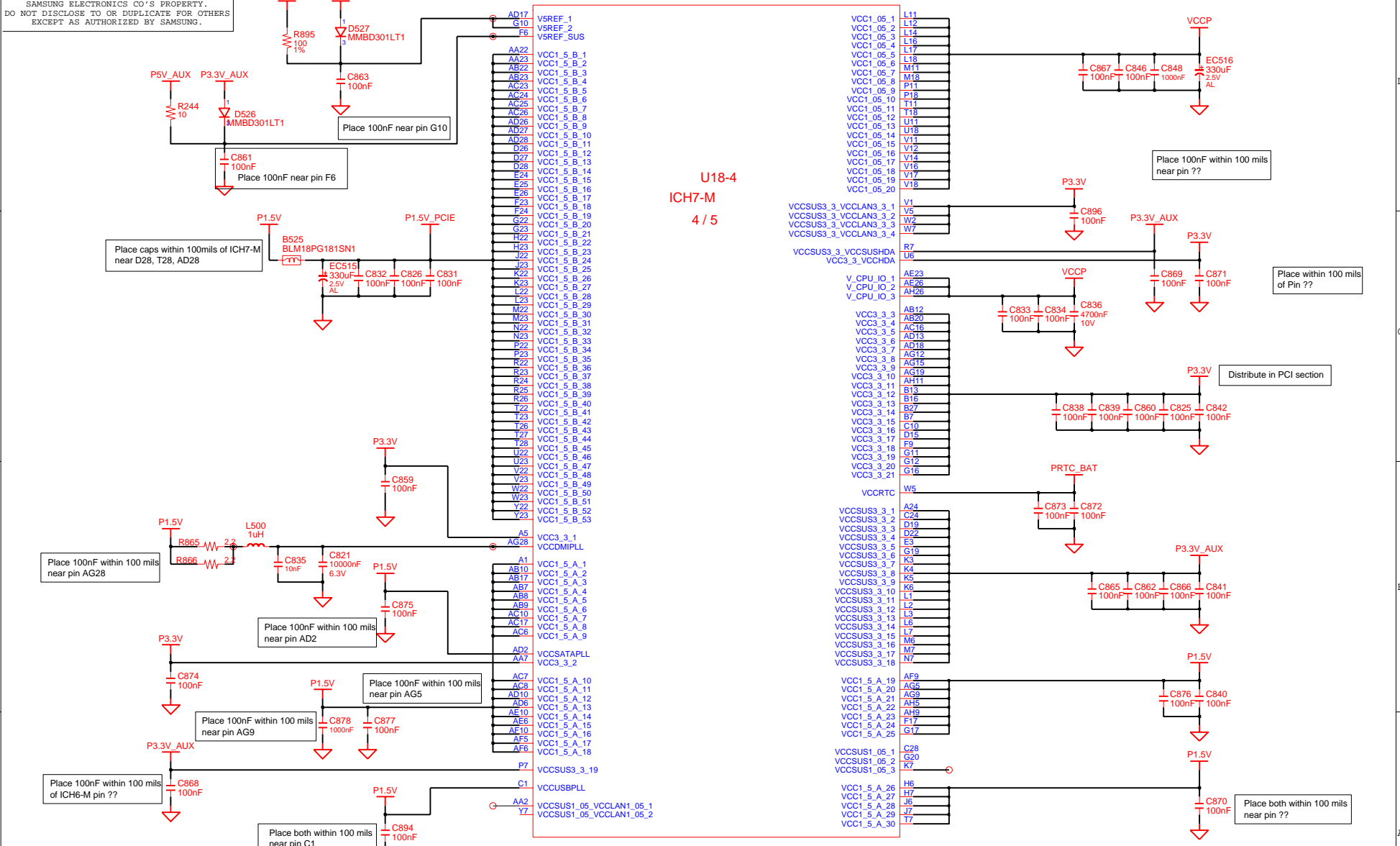


**ICH7-m Options**

Option	Function	Default
CHP3_SPKR	No Reboot	No Stuff
CHP3_GNT3	A16 swap override	No Stuff
AC97_SDOUT	Safe Mode	TBD
CHP3_GNT(5:4)	Boot BIOS Option	

DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R	<b>SAMSUNG</b> ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	SR	MAIN		
APPROVAL	LIM, J.G	REV	1.0	SOUTH BRIDGE(2/4)		PART NO. BA41-xxxxxx
MODULE CODE	undef ined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	20	OF 55

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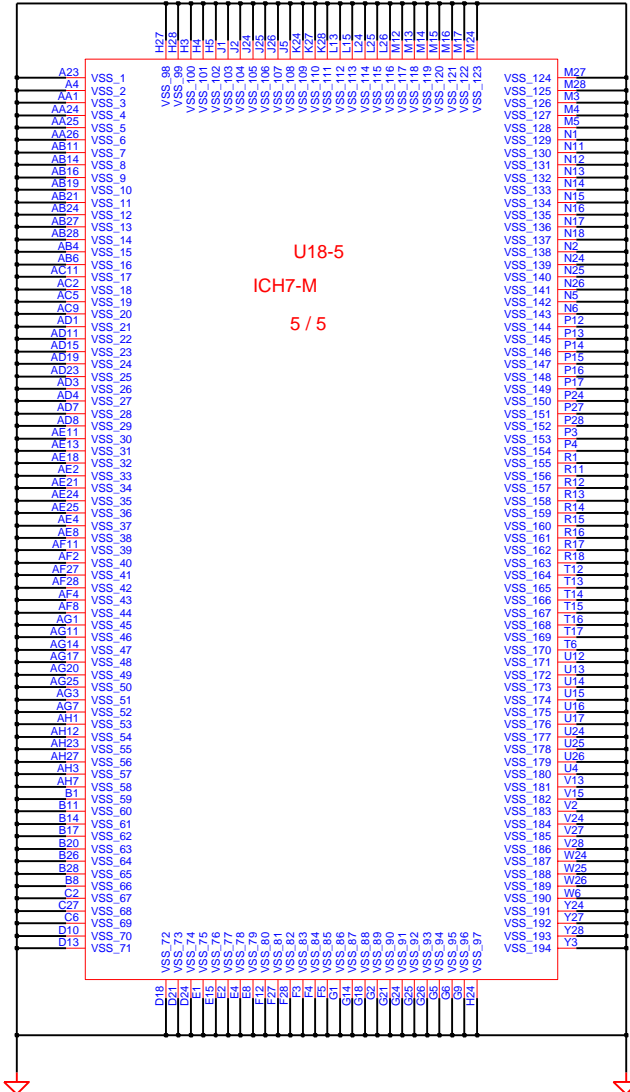
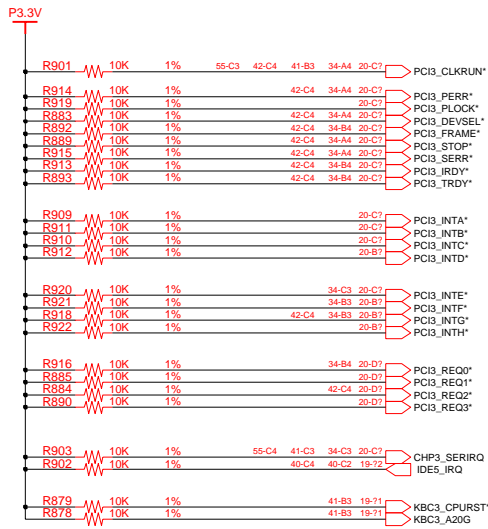
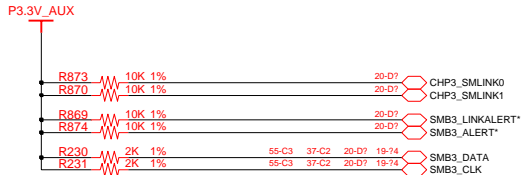


**U18-4**  
**ICH7-M**  
**4 / 5**

DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN SOUTH BRIDGE(3/4)	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-xxxxxx
CHECK	YUN, C.Y	DEV. STEP	SR			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undef ined	LAST EDIT				
		March 9, 2006	12:35:42 PM	PAGE	21 OF 55	

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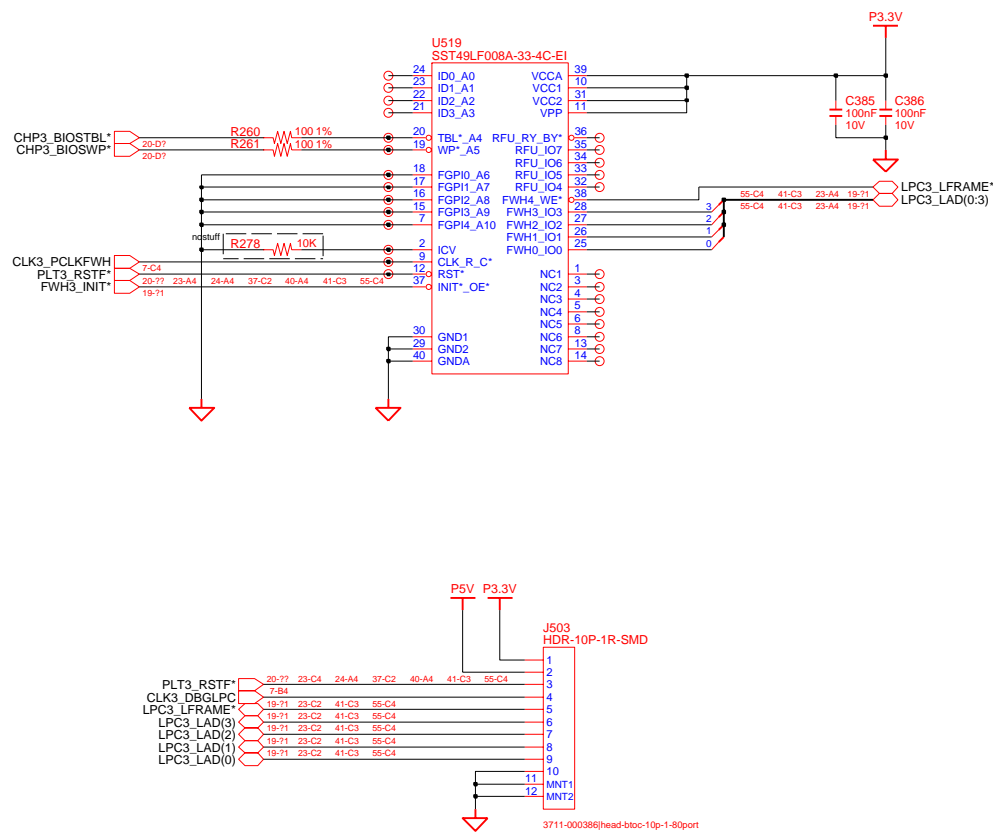
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DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	SR		MAIN	
APPROVAL	LIM, J.G	REV	1.0		SOUTH BRIDGE(4/4)	PART NO. BA41-xxxxxx
MODULE CODE	undef ined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	22	OF 55

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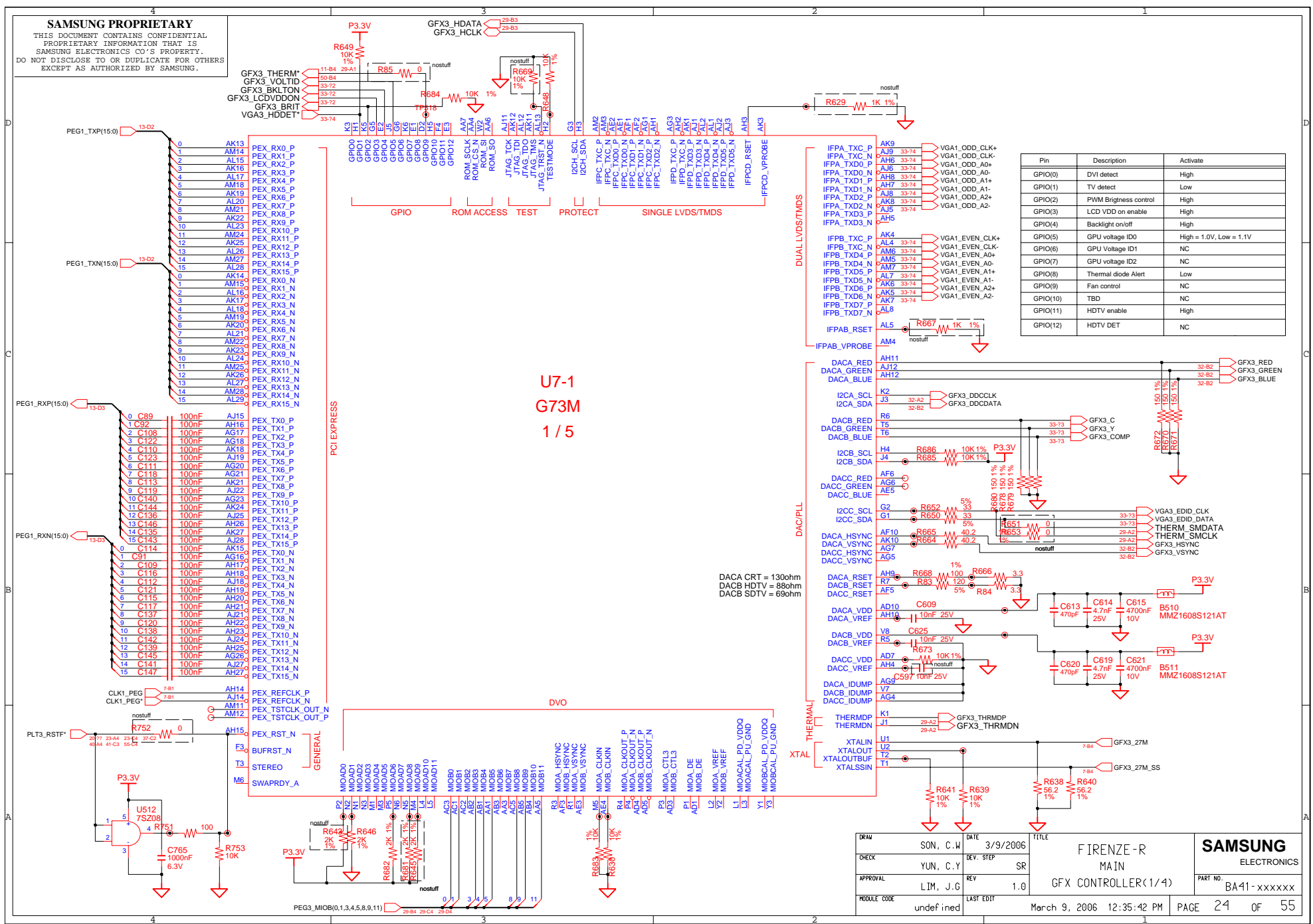
02	VERIFY REAL MODE	66	CONFIGURE ADVANCE CACHE REG.
03	DISABLE NMI	6A	DISPLAY EXTERNAL CACHE SIZE
04	GET CPU TYPE	6C	DISPLAY SHADOW MESSAGE
06	INIT. SYSTEM H/W	6E	DISPLAY NON-DISPOSABLE SEGMENT
08	INIT. CHIPSET REG.	70	DISPLAY ERROR MESSAGE
09	SET IN POST FLAG	72	CHECK FOR CONFIGURATION ERROR
0A	INIT CPU.REG	74	TEST REAL-TIME CLOCK
0B	CPU CACHE ON	76	CHECK FOR KEYBOARD ERROR
0C	INIT.CACHE TO POST	7C	SETUP HARDWARE INTERRUPT VECTOR
0E	INIT. I/O VALUE	7E	TEST COPROCESSER IF PRESENT
0F	ENABLE THE L-BUS IDE	80	DISABLE ON-BOARD I/O PORT
10	INIT. POWER MANAGER	82	DETECT AND INSTALL EXT.RS232C
11	LOAD ALTERNATE REG.	84	DETECT AND INSTALL EXT.PARALLEL
13	PCI BUS MASTER RESET WITH INITIAL POST VALUE	86	RE-INIT. ON-BOARD I/O PORT
14	INIT. KEYBOARD CONTROLLER	88	INIT. BIOS DATA ROM
16	CHECK CHECKSUM	8A	INIT.EXTENDED BIOS DATA AREA
18	8254 TIMER INIT.	8C	INIT. FDD CONTROLLER
1A	8237 DMA CONTROLLER INIT.	9A	SHADOW OPTION ROMS
1C	RESET INTERRUPT CONTROLLER	9C	SETUP POWER MANAGEMENT
20	TEST DRAM REFRESH	9E	ENABLE H/W INTERRUPT
22	TEST 8742 KEYBOARD CONTROLLER	A0	SET TIME OF DAY
24	SET ES SEGMENT REG. TO 4GB	A4	INIT. TYPEMATIC RATE
26	ENABLE A20	A8	ERASE F2 PROMPT
28	AUTO SIZING DRAM	AA	SCAN FOR F2 KEY STROKE
32	COMPUTE THE CPU SPEED	AC	ENTER SETUP
34	TESET CMOS RAM	AE	CLEAR IN POST FLAG
38	SHADOW SYSTEM BIOS ROM	B0	CHECK FOR ERRORS
3A	AUTO SIZING CACHE	B2	POST DONE-PREPARE TO BOOT O/S
3C	CONFIGURE ADVANCED CHIPSET REG.	B4	ONE BEEP
3D	LOAD ALTER REG. WITH CMOS VALUE	B6	CHECK PASSWORD (OPTION)
42	INIT. INTERRUPT VECTOR	B7	ACPI INIT
44	INIT. BIOS INTERRUPT	BA	DMI INIT
46	CHECK ROM COPYRIGHT NOTICE	BE	CLEAR SCREEN
47	INIT. I20 SUPPORT IF INSTALLED	C0	TRY BOOT WITH INT19
48	CHECK VIDEO CONFIGURE AGAINST CMOS	D0	INTERRUPT HANDLER ERROR
49	INIT. PCI BUS AND DEVICE	D2	UNKNOWN INTERRUPT ERROR
4A	INIT. ALL VIDEO BIOS ROM	D4	PENDING INTERRUPT ERROR
4C	SHADOW VIDEO BIOS ROM	D6	SHUTDOWN 5
50	DISPLAY CPU TYPE AND SPEED	D8	SHUTDOWN ERROR
52	TEST KEYBOARD	DA	EXTENDED BLOCK MOVE
54	SET KEYCLICK IF ENABLED	DC	SHUTDOWN 10
56	ENABLE KEYBOARD	89	ENABLE NMI
58	TEST FOR UNEXPECTED INTERRUPTS	90	INIT. HDD CONTROLLER
5A	DISPLAY " PRESS ..... SETUP"	91	INIT. LOCAL BUS HDD CONTROLLER
5C	TEST RAM BETWEEN 512K AND 640K	92	JUMP TO USER PATCH 2
60	TEST EXTENDED MEMORY	94	DISABLE A20 ADDRESS LINE
62	TEST EXTENDED MEMORY ADDRESS LINE	96	CLEAR HUGE ES SEGMENT REG.
64	JUMP TO USER PATCH 1	98	SEARCH FOR OPTION ROMS

DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	SR	MAIN		
APPROVAL	LIM, J.G	REV	1.0	FWH		PART NO. BA41-xxxxxx
MODULE CODE	undef ined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	23	OF 55



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Pin	Description	Activate
GPIO(0)	DVI detect	High
GPIO(1)	TV detect	Low
GPIO(2)	PWM Brightness control	High
GPIO(3)	LCD VDD on enable	High
GPIO(4)	Backlight on/off	High
GPIO(5)	GPU voltage ID0	High = 1.0V, Low = 1.1V
GPIO(6)	GPU Voltage ID1	NC
GPIO(7)	GPU voltage ID2	NC
GPIO(8)	Thermal diode Alert	Low
GPIO(9)	Fan control	NC
GPIO(10)	TBD	NC
GPIO(11)	HDTV enable	High
GPIO(12)	HDTV DET	NC

U7-1  
G73M  
1/5

DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	SR		MAIN	
APPROVAL	LIM, J.G	REV	1.0		GFX CONTROLLER(1/4)	PART NO. BA41-xxxxxx
MODULE CODE	undef ined	LAST EDIT	March 9, 2006 12:35:42 PM			PAGE 24 OF 55

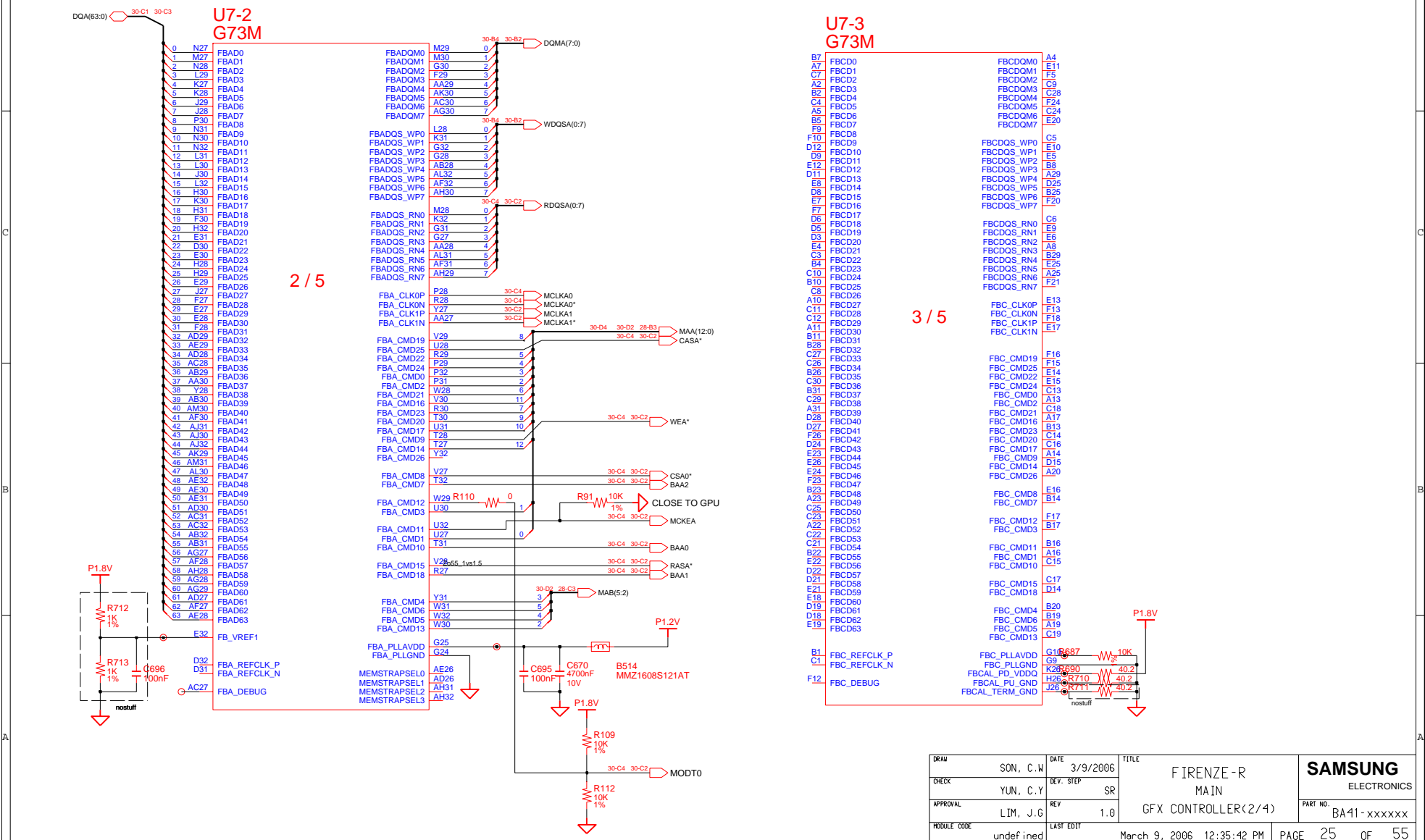


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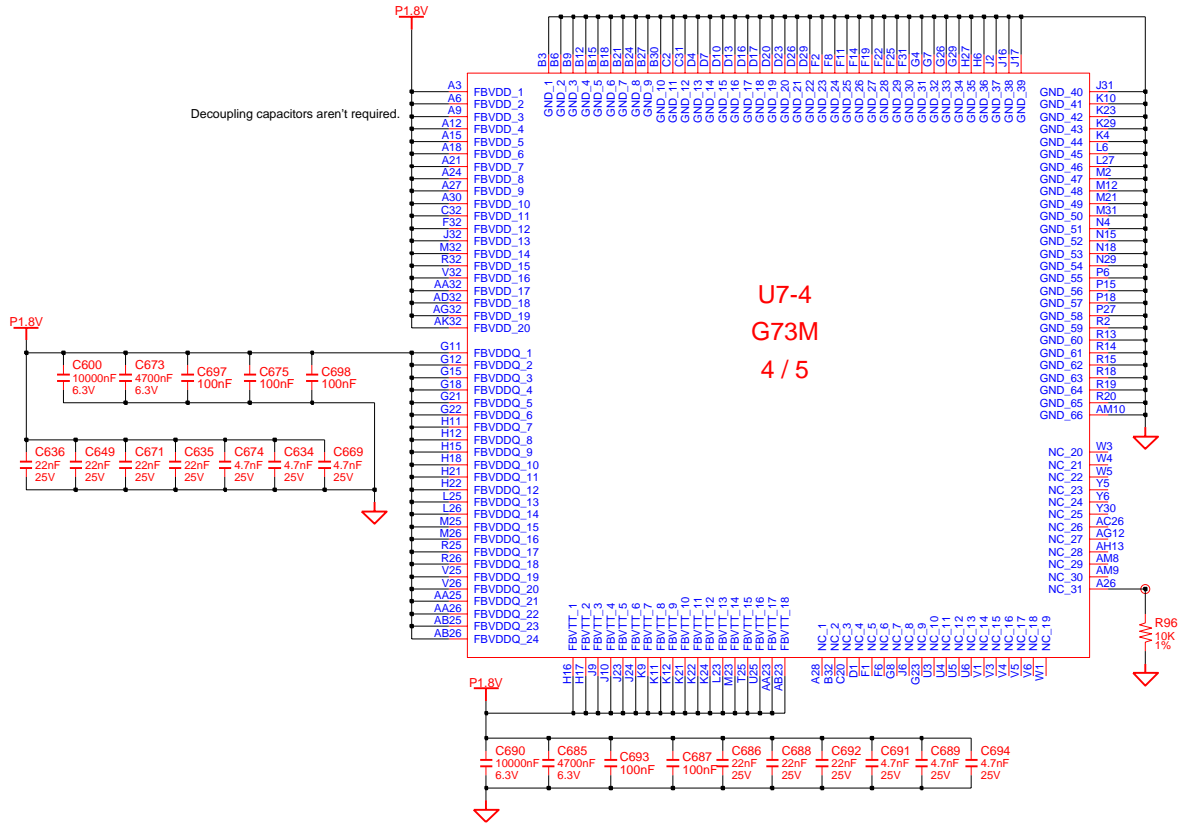
**Graphic Memory I/F  
(Using FBA Channel)**

**Graphic Memory I/F  
(Using FBC Channel)**



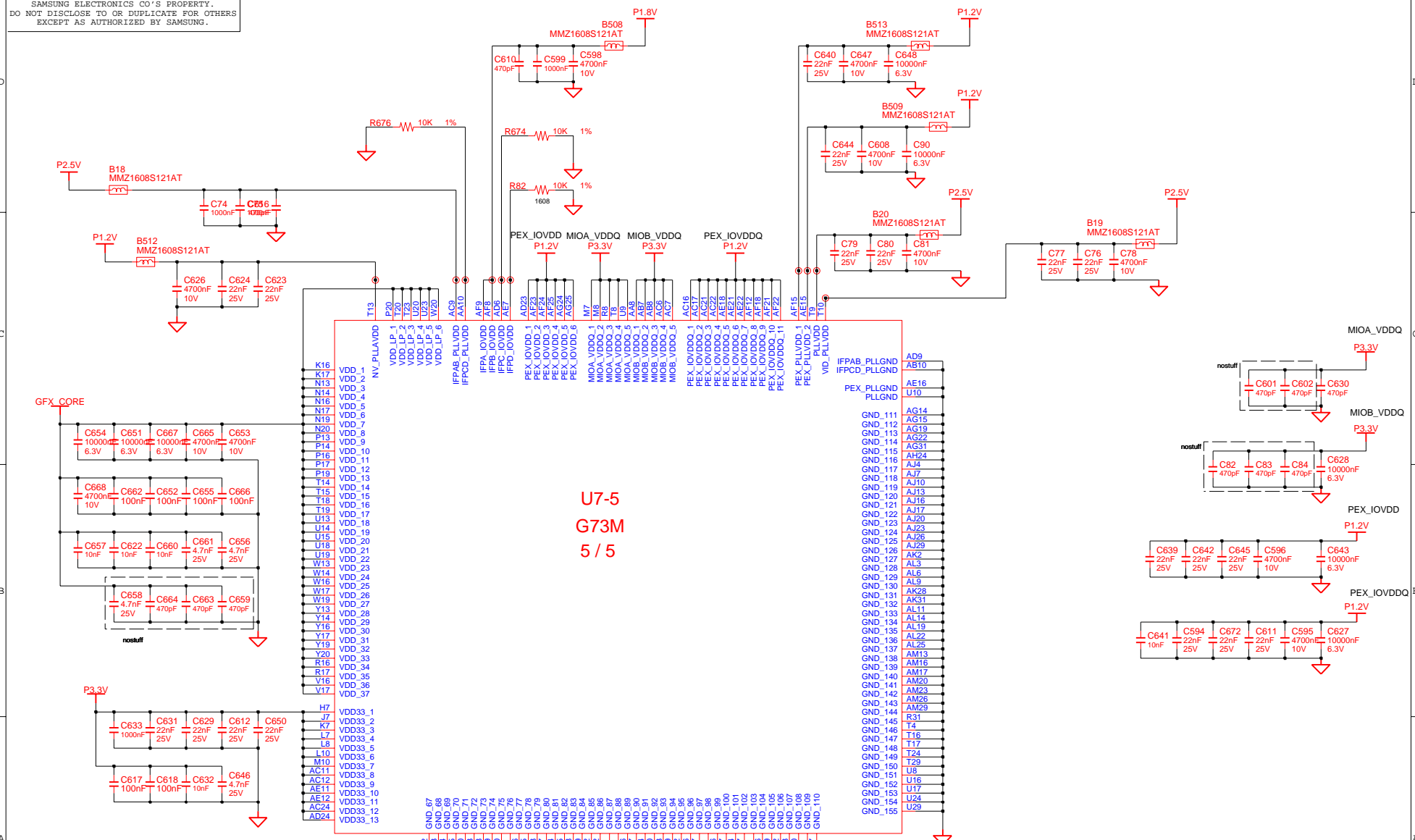
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CHECK	YUN, C.Y	DEV. STEP	SR	MAIN		
APPROVAL	LIM, J.G	REV	1.0	GFX CONTROLLER(2/4)		
MODULE CODE	undef ined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	25 OF 55	

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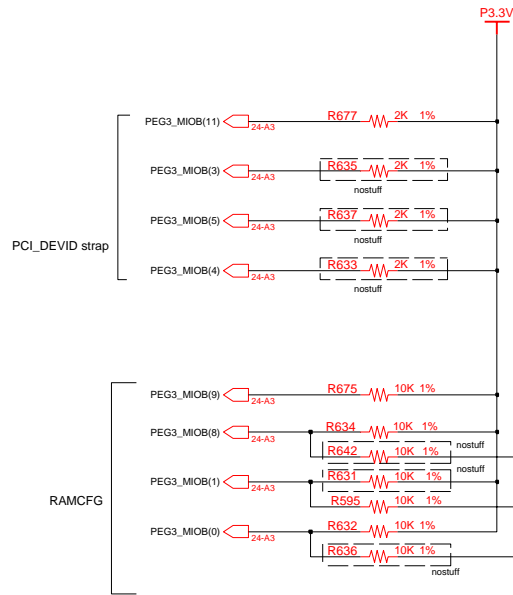
DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN	<b>SAMSUNG</b> ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	SR	GFX CONTROLLER(3/4)		
APPROVAL	LIM, J.G	REV	1.0			PART NO. BA41-xxxxxx
MODULE CODE	undef ined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	26	OF 55

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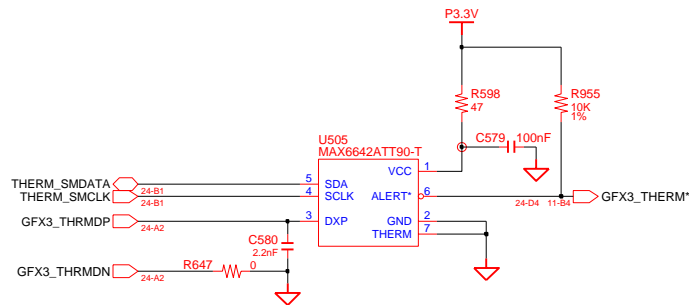
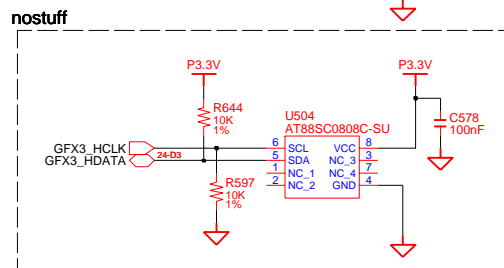


DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN GFX CONTROLLER(4/4)	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-xxxxxx
CHECK	YUN, C.Y	DEV. STEP	SR			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undef ined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	27 OF 55	

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Straps	Pin # (Rev.A02)	Descriptions
SUB_VENDOR	MIOAD(1)	0 : No BIOS 1 : Read from BIOS(Default)
RAMCFG(3:0) [9,8,1,0]	MIOB(9) MIOB(8) MIOB(1) MIOB(0)	1001 : samsung_GDDR2_256Mbit 1010 : infineon_GDDR2_256Mbit 1101 : samsung_GDDR2_512Mbit 1110 : infineon_GDDR2_512Mbit
CRYSTAL(1:0)	MIOB(2) MIOB(6)	01 : 14.318 MHz 10 : 27 MHz (Default) 11 : Unknown 00 : 13.5 MHz
TV_MODE(1:0)	MIOAD(7) MIOAD(10)	00 : SECAM 01 : NTSC (Default) 10 : PAL 11 : CRT
PCI_DEVID(3:0) [11,3,5,4]	MIOB(11) MIOB(3) MIOB(5) MIOB(4)	72M : 0X01D8 72M-V : 0X01D7 73M : 0X0398
ROM_TYPE(1:0)	MIOB(10) MIOBVSYN	No ROM (NC)
USER STRAP	MIOAD(2:5)	EDID

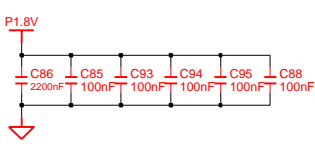
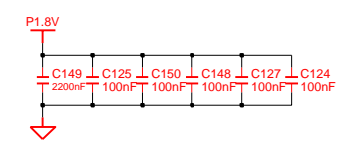
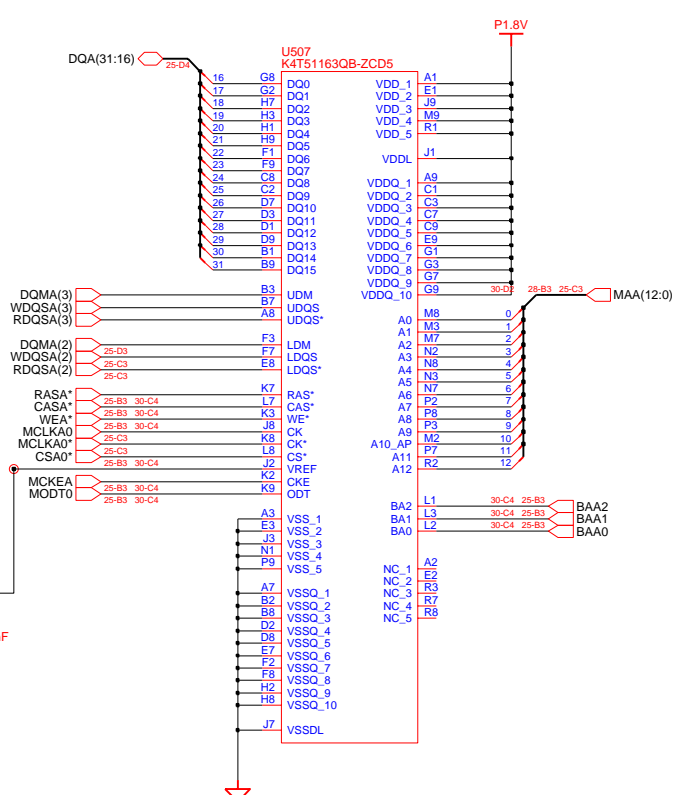
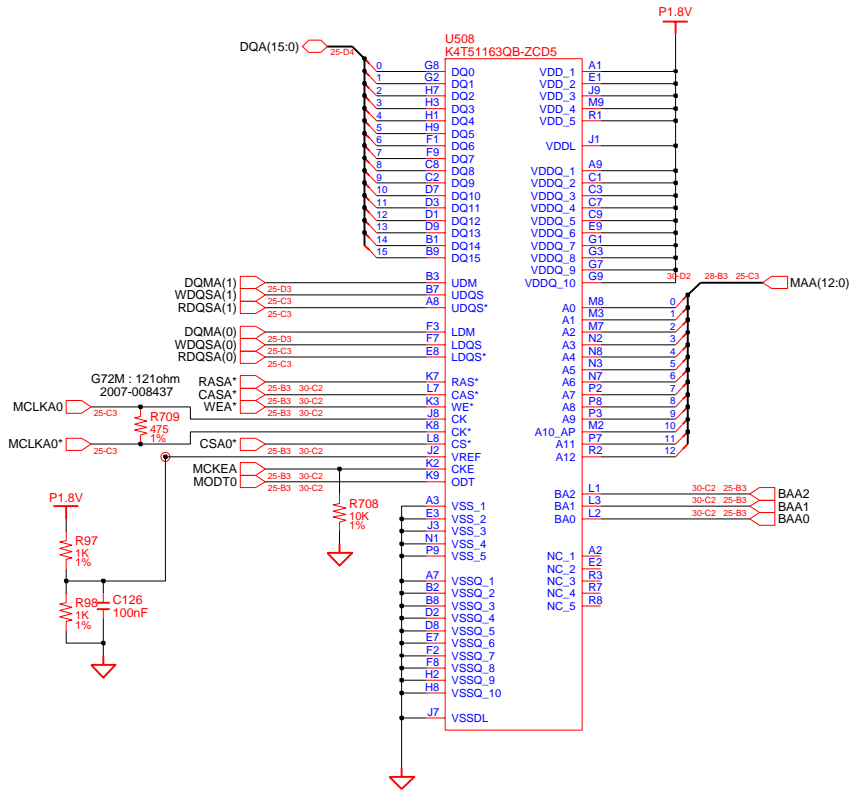


DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN GFX THERMAL SENSOR	<b>SAMSUNG</b> ELECTRONICS	
CHECK	YUN, C.Y	DEV. STEP	SR	PART NO.			BA41-xxxxxx
APPROVAL	LIM, J.G	REV	1.0	REV			
MODULE CODE	undef ined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE			28 OF 55

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**A-channel**

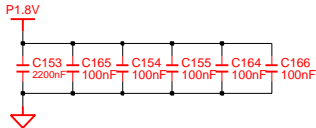
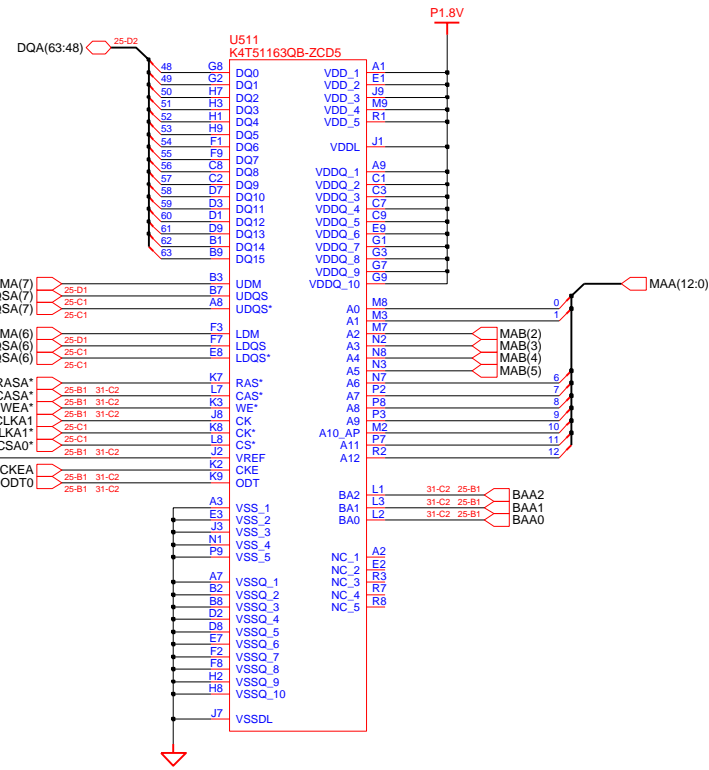
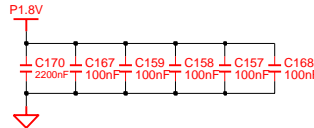
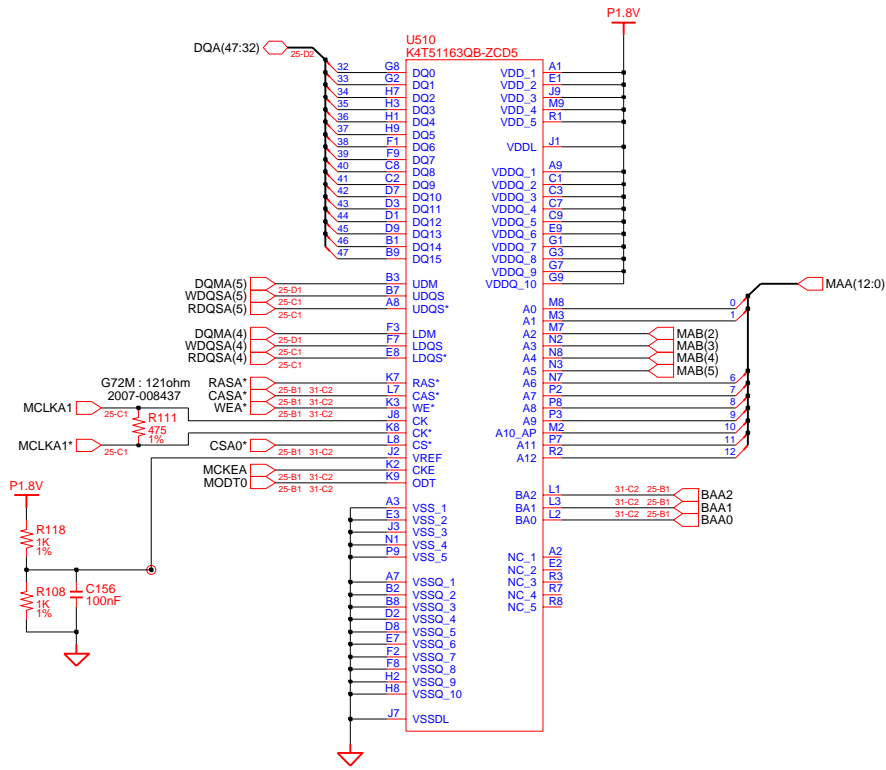


DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN GFX MEMORY(1/2)	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-xxxxxx
CHECK	YUN, C.Y	DEV. STEP	SR			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undef:ined	LAST EDIT				
				March 9, 2006 12:35:42 PM	PAGE 29 OF 55	

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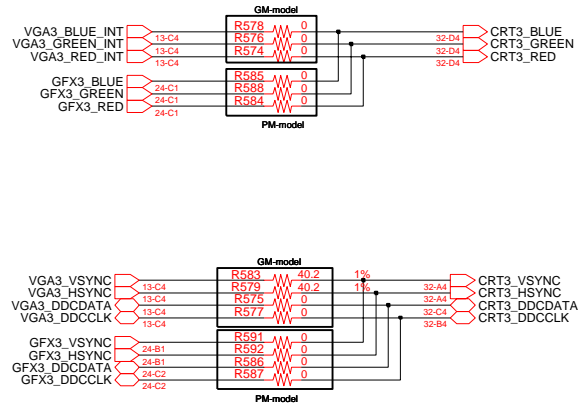
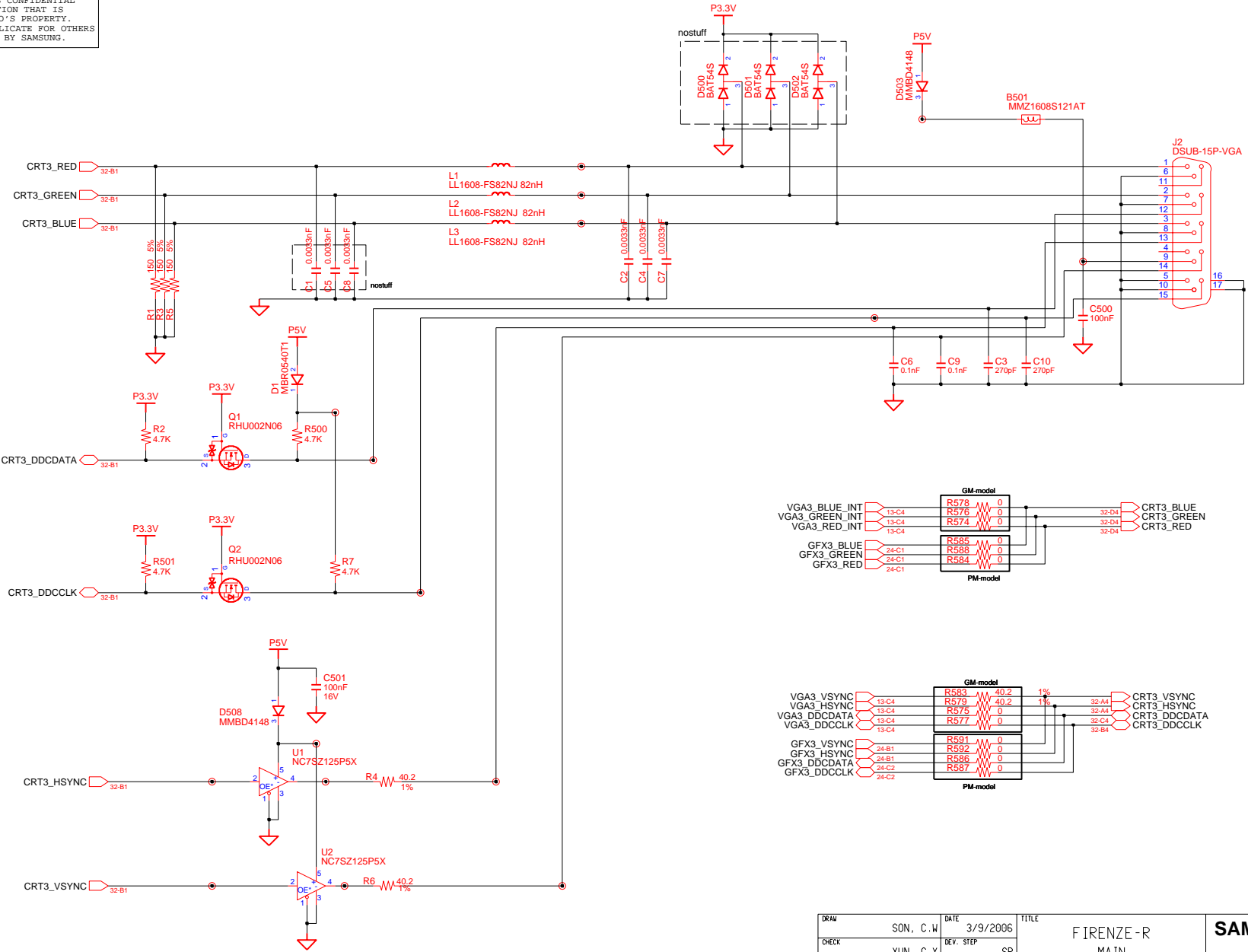
**A-channel**



DRAW	SON, C. W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN GFX MEMORY(2/2)	<b>SAMSUNG</b> ELECTRONICS PART NO. BAA1-xxxxxx
CHECK	YUN, C. Y	DEV. STEP	SR	REV	1.0	
APPROVAL	LIM, J. G	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	30	OF 55

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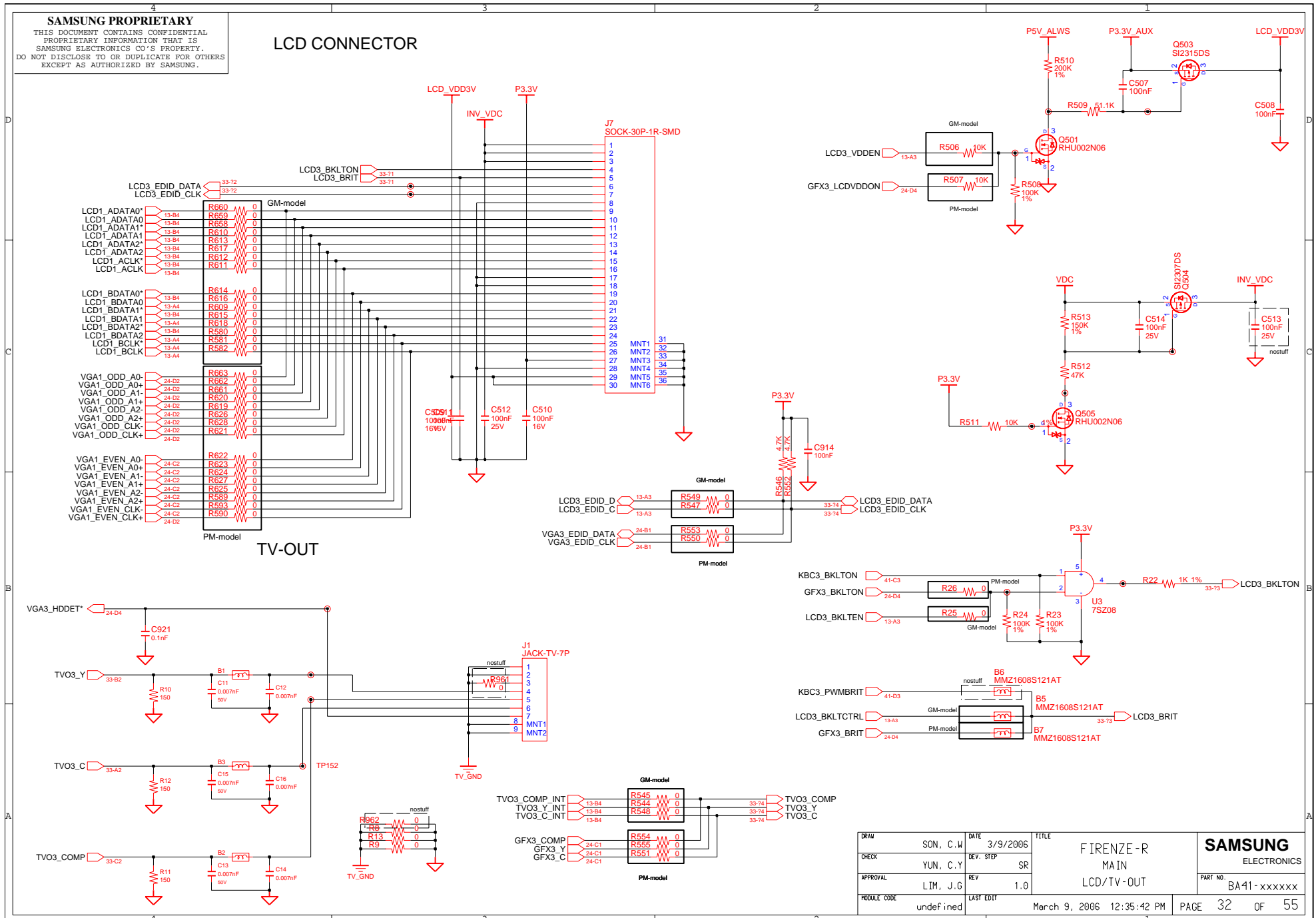


DRAW	SON, C. W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN CRT PORT	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-xxxxxx
CHECK	YUN, C. Y	DEV. STEP	SR			
APPROVAL	LIM, J. G	REV	1.0			
MODULE CODE	undef ined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	31 OF 55	

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**LCD CONNECTOR**

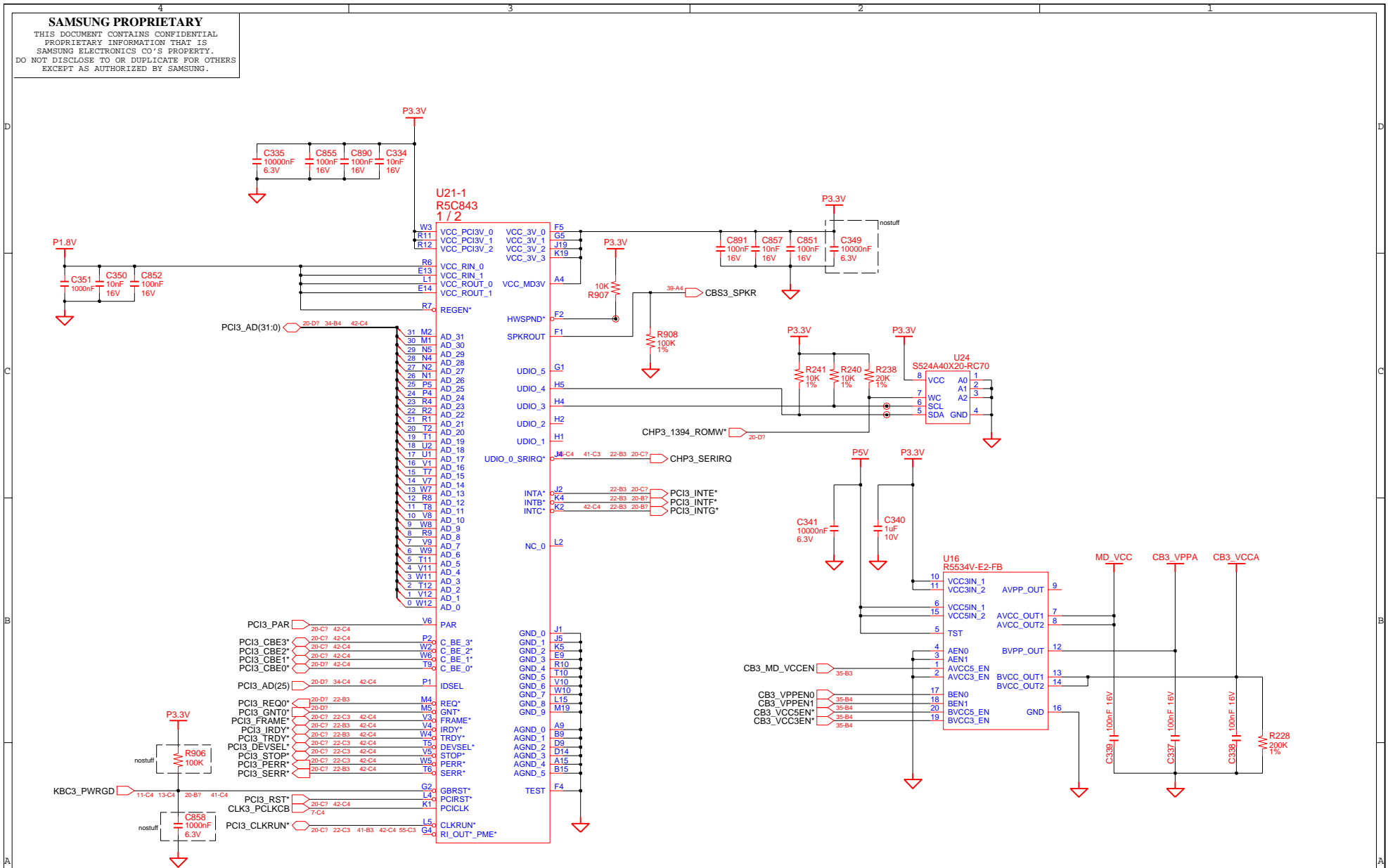


DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R	<b>SAMSUNG</b> ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	SR	MAIN		
APPROVAL	LIM, J.G	REV	1.0	LCD/TV-OUT		PART NO. BA41-xxxxxx
MODULE CODE	undef ined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	32	OF 55



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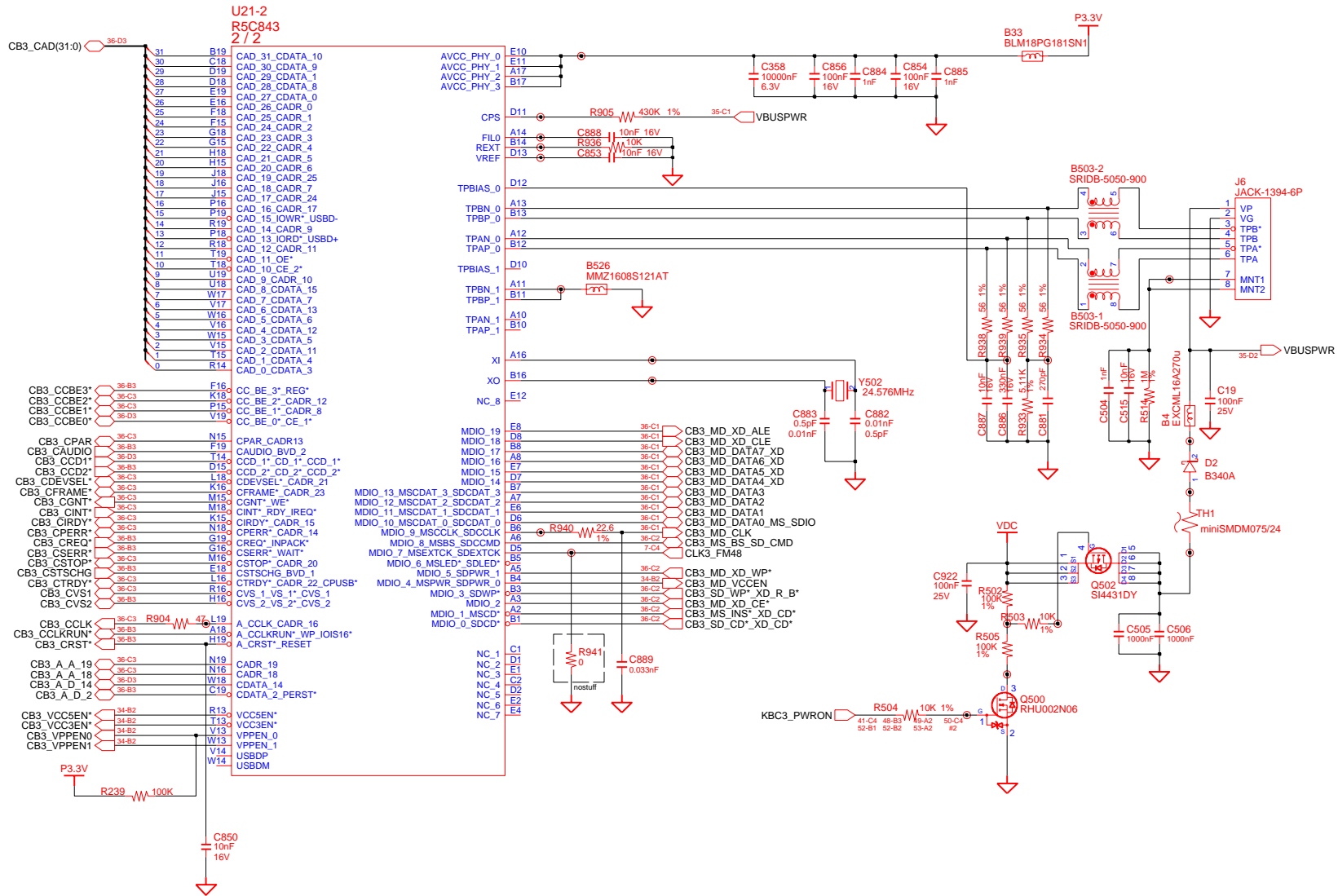
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DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN CARBUS(1/2)	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-xxxxxx
CHECK	YUN, C.Y	DEV. STEP	SR			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undef ined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	33 OF 55	

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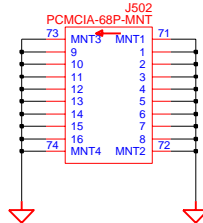
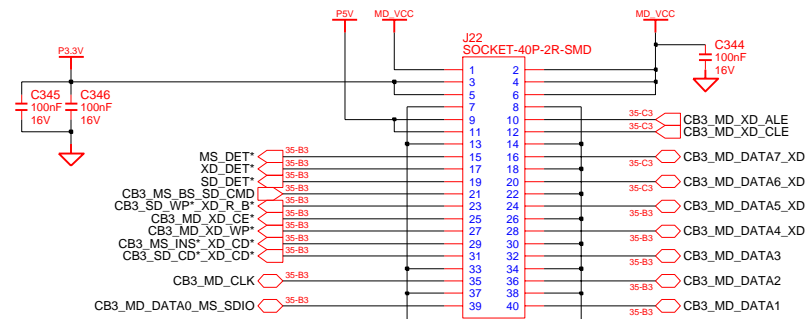
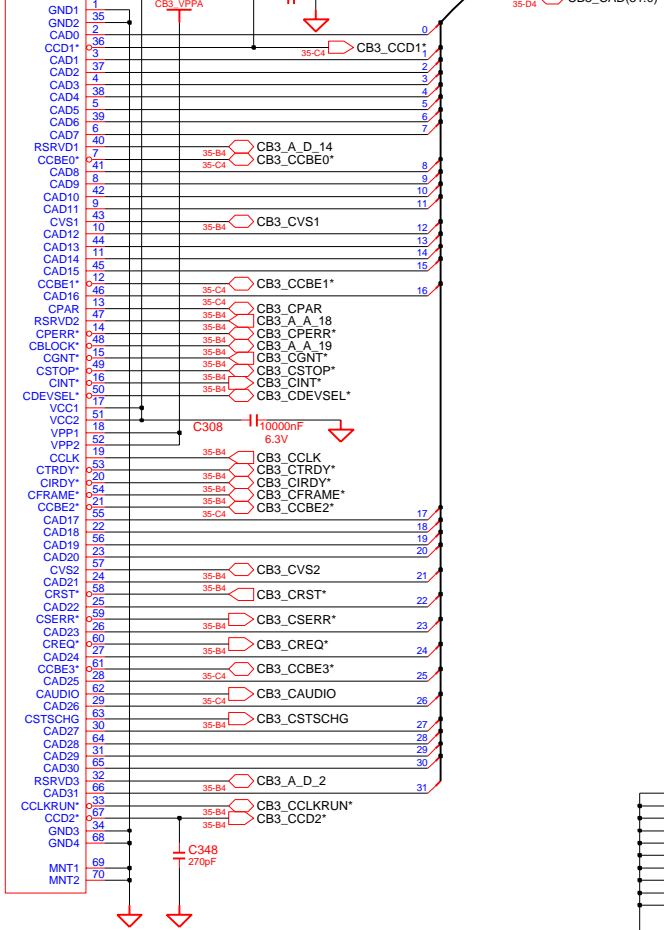


DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN CARDBUS(2/2)	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-xxxxxx
CHECK	YUN, C.Y	DEV. STEP	SR			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undef ined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	34 OF 55	

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**J501  
PCMCIA-68P-REVERSE**

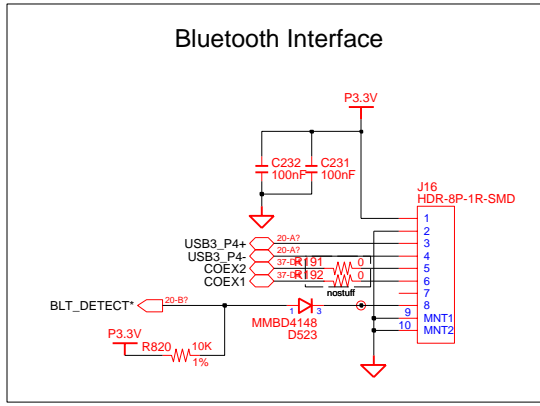
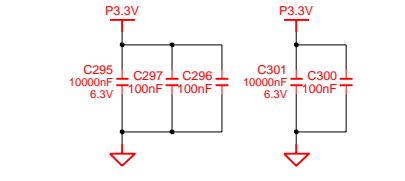
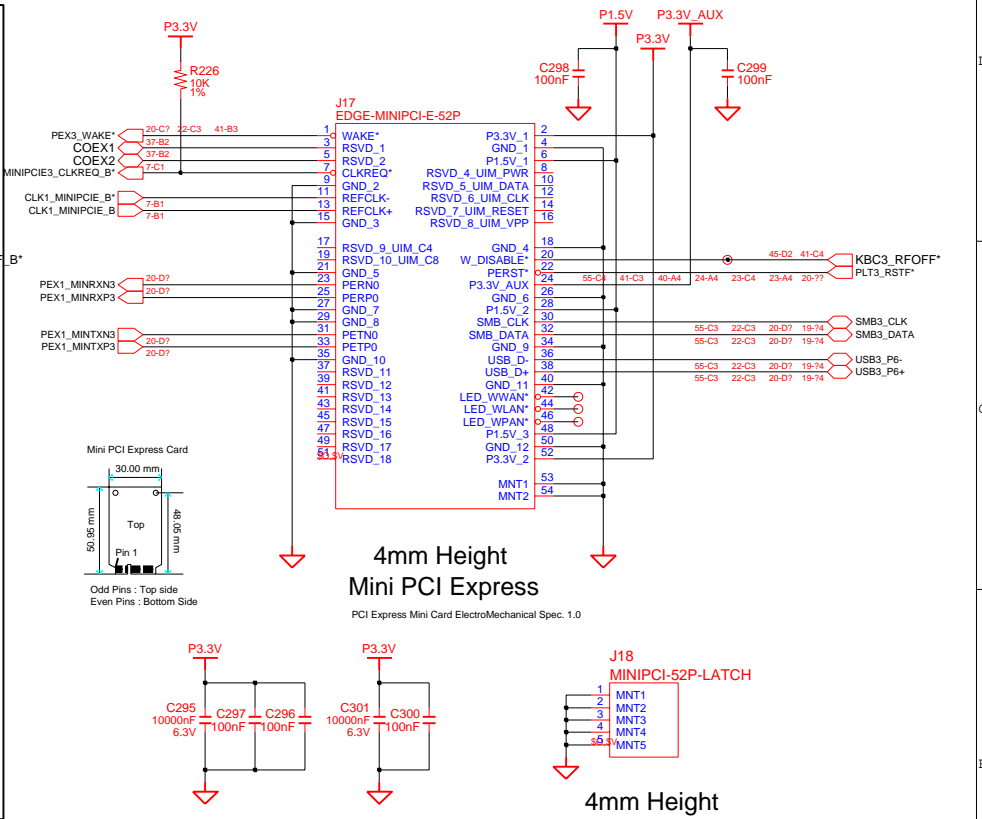
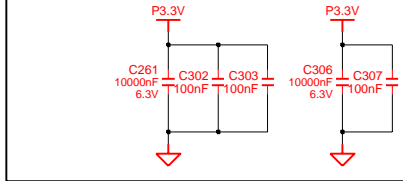
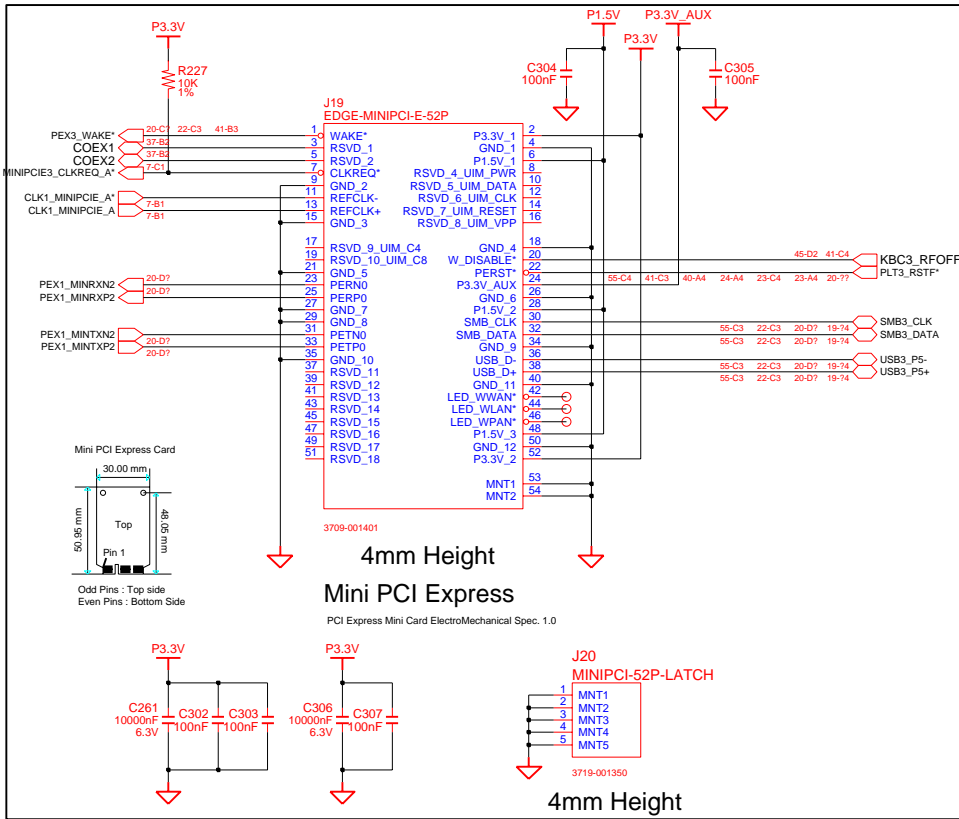


DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN	<b>SAMSUNG</b> ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	SR	REV	1.0	
APPROVAL	LIM, J.G	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	35	OF 55
MODULE CODE	undef ined					

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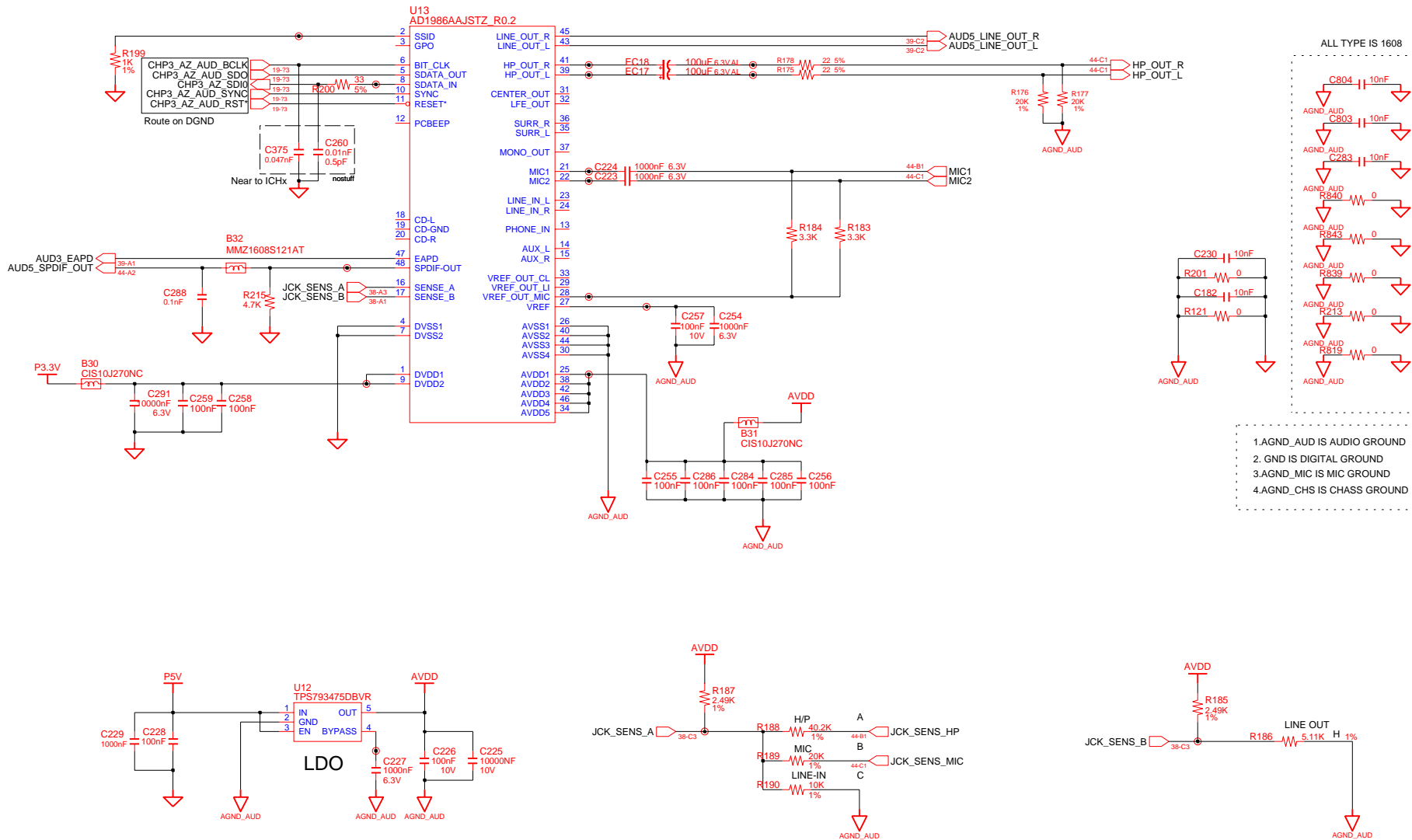
nostuff



DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN MINI CARD	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-xxxxxx
CHECK	YUN, C.Y	DEV. STEP	SR			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undef:ind	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	36	OF 55

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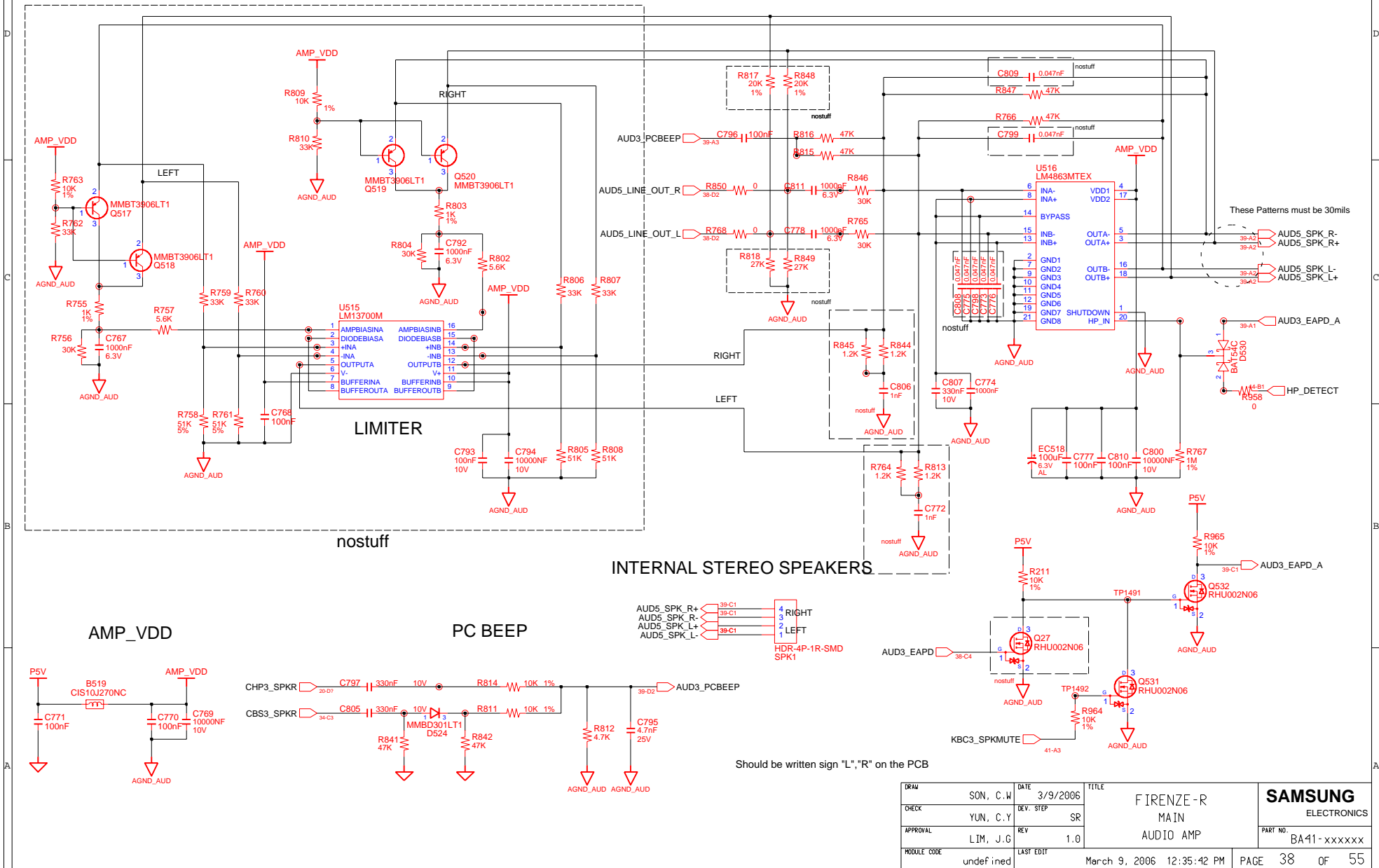


- ALL TYPE IS 1608
- AGND\_AUD C804 10nF
  - AGND\_AUD C803 10nF
  - AGND\_AUD C283 10nF
  - AGND\_AUD R640 0
  - AGND\_AUD R645 0
  - AGND\_AUD R639 0
  - AGND\_AUD R213 0
  - AGND\_AUD R819 0
  - AGND\_AUD R819 0
- 1.AGND\_AUD IS AUDIO GROUND  
 2. GND IS DIGITAL GROUND  
 3.AGND\_MIC IS MIC GROUND  
 4.AGND\_CHS IS CHASS GROUND

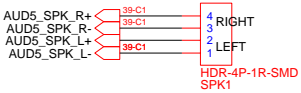
DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN AUDIO CODEC	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-xxxxxx
CHECK	YUN, C.Y	DEV. STEP	SR			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undef ined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	37 OF 55	

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**INTERNAL STEREO SPEAKERS**



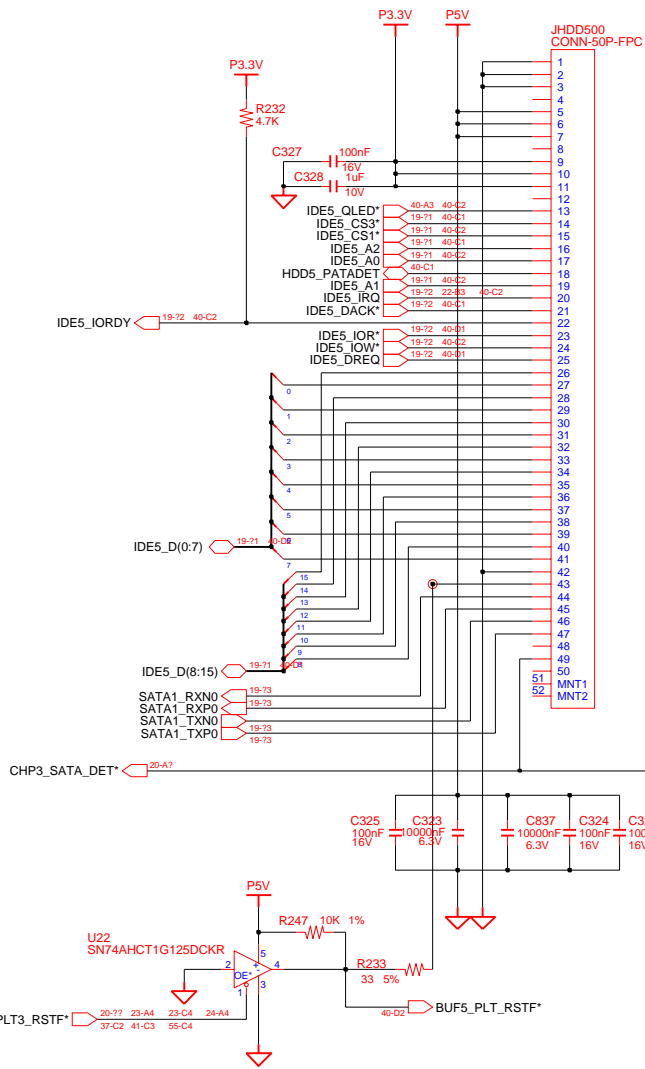
Should be written sign "L,"R on the PCB

DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN AUDIO AMP	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-xxxxxx
CHECK	YUN, C.Y	DEV. STEP	SR			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undef ined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	38 OF 55	

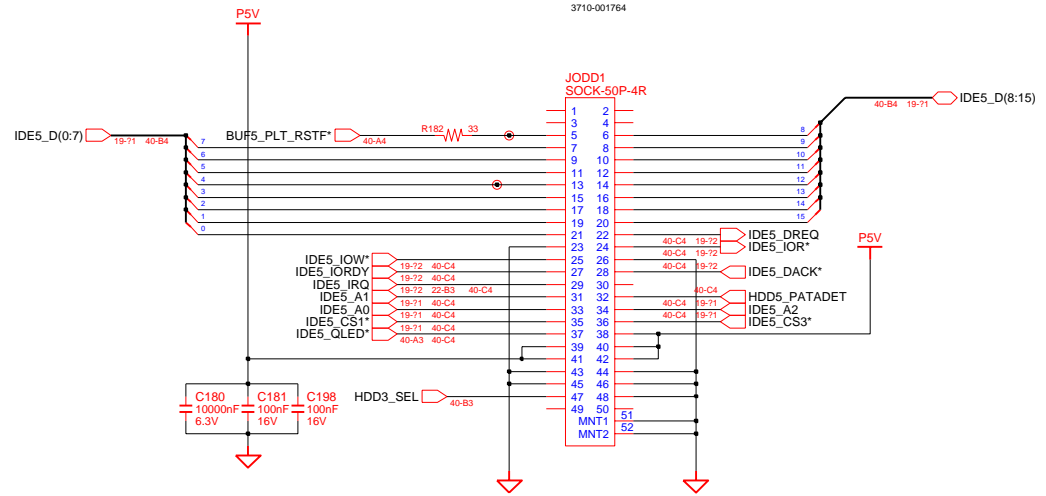
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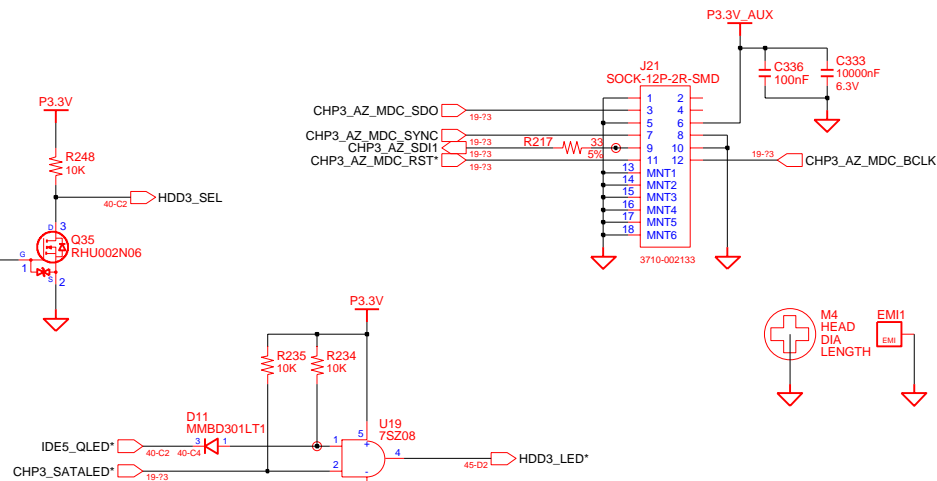
**MAIN TO HDD**



**MAIN TO ODD**



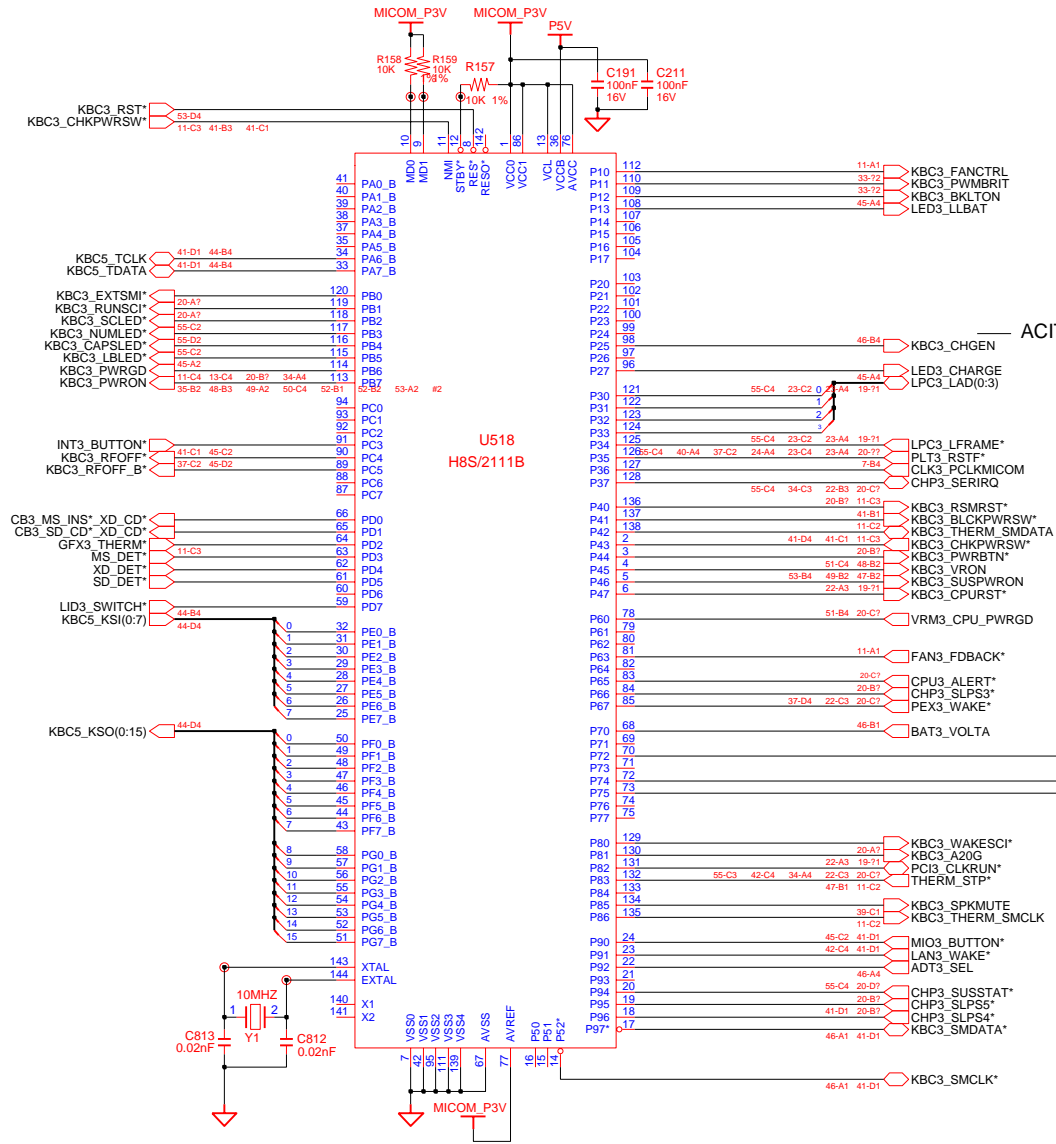
**MDC Connector**



DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN HDD/ODD/MDC CONN	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-xxxxxx
CHECK	YUN, C.Y	DEV. STEP	SR			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undef ined	LAST EDIT	March 9, 2006 12:35:42 PM			
				PAGE	39 OF 55	

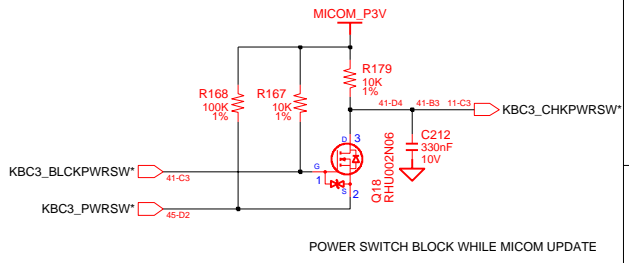
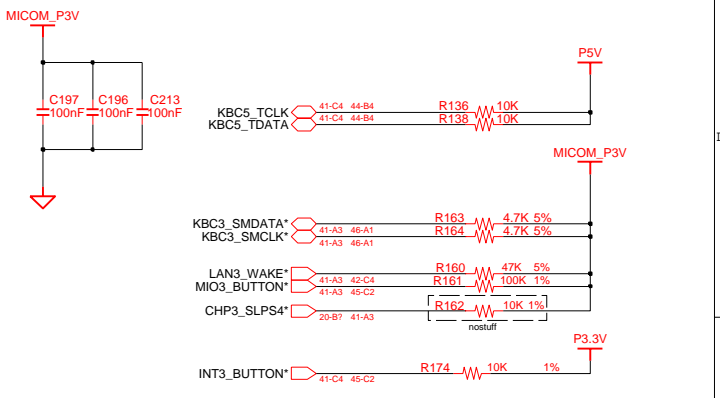
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ACTIVE HIGH

U518  
H8S/2111B



MICOM\_P3V

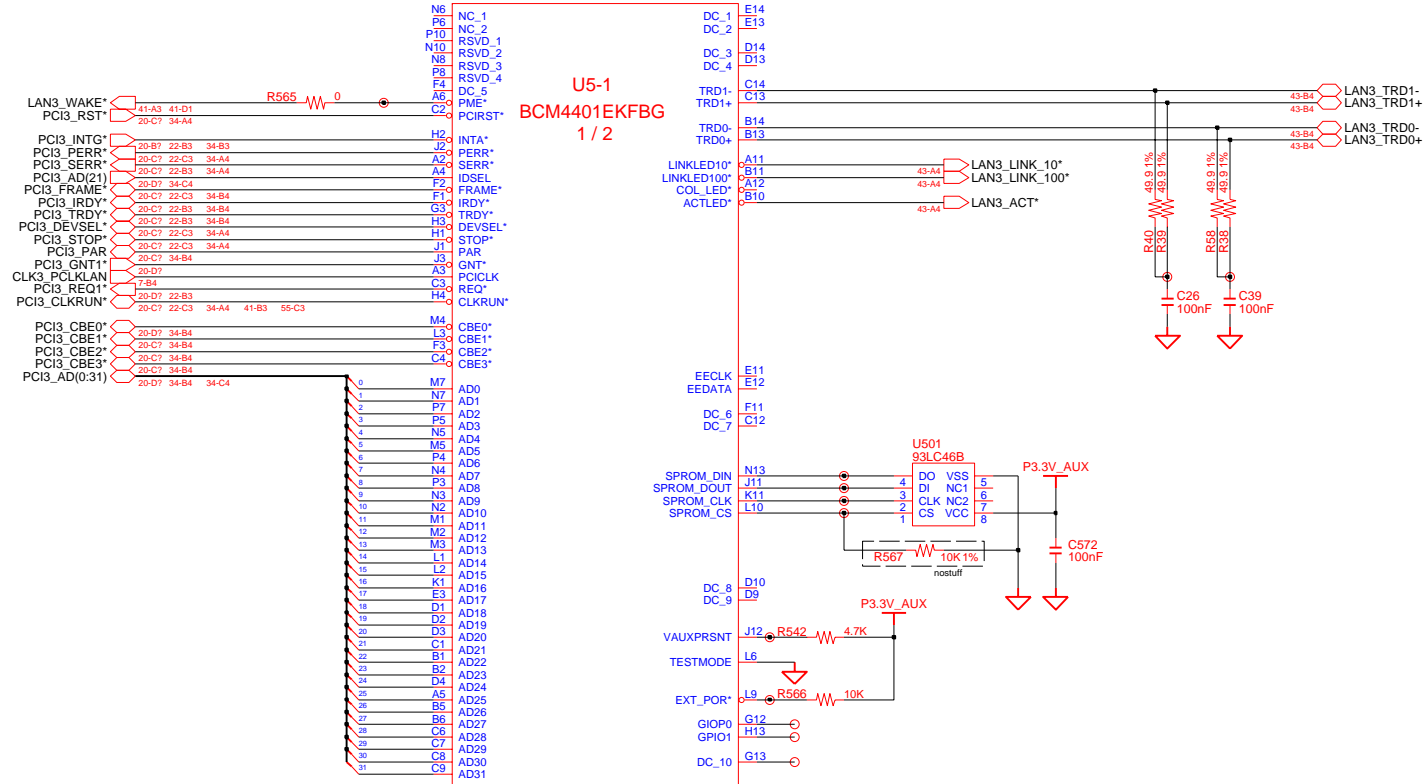
DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN MICOM	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-xxxxxx
CHECK	YUN, C.Y	DEV. STEP	SR			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undef ined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	40 OF 55	



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# LAN Controller (Only 10/100M)



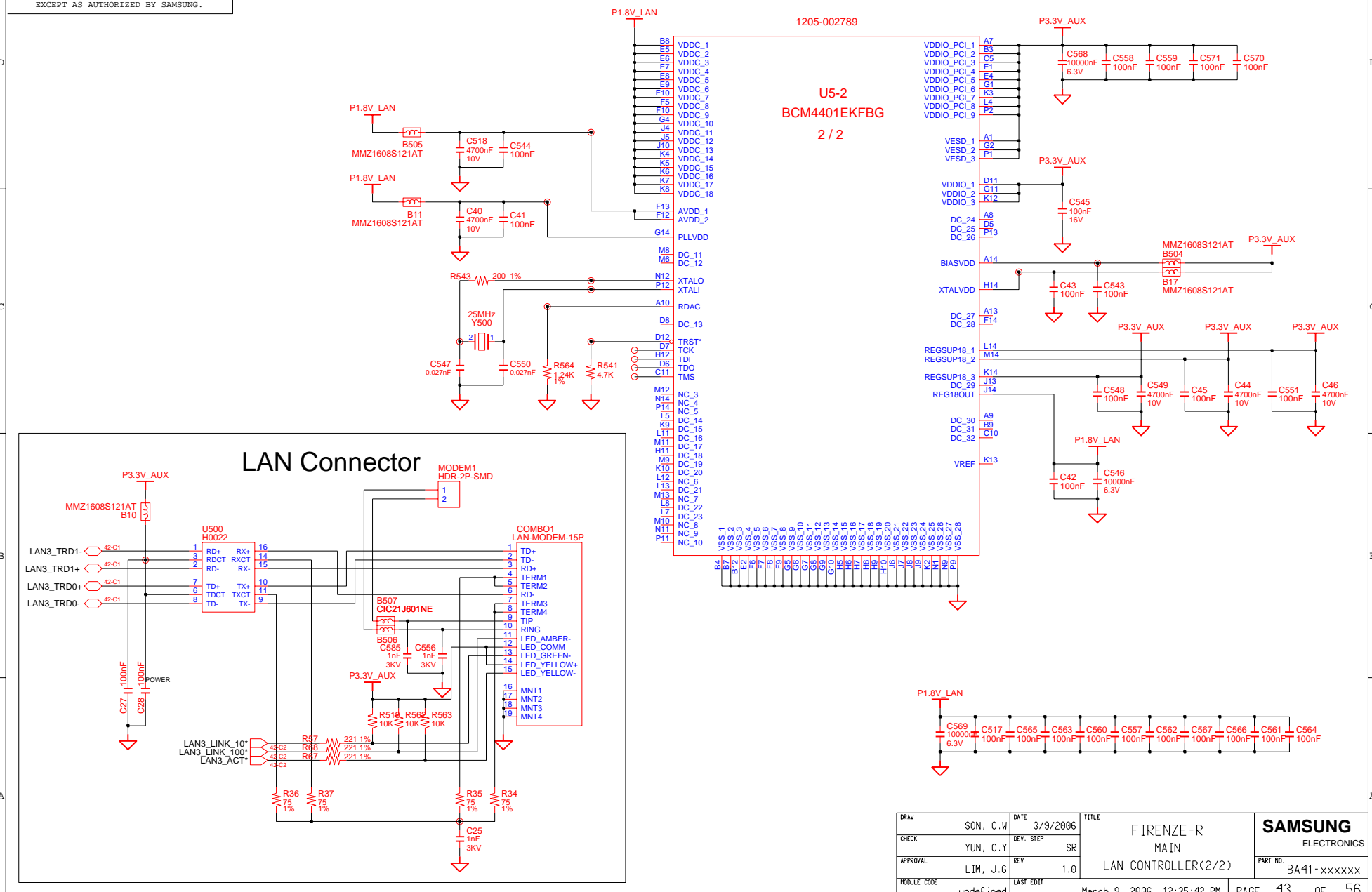
1205-002789

DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	SR	LAN CONTROLLER(1/2)		
APPROVAL	LIM, J.G	REV	1.0			PART NO. BA41-xxxxxx
MODULE CODE	undef ined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	41	OF 55

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# LAN Controller (Only 10/100M)



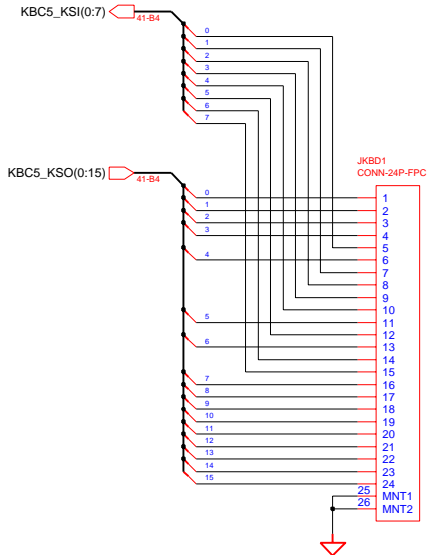
DRAW	SON, C. W	DATE	3/9/2006	TITLE	FIRENZE-R	SAMSUNG ELECTRONICS
CHECK	YUN, C. Y	DEV. STEP	SR	MAIN		
APPROVAL	LIM, J. G	REV	1.0	LAN CONTROLLER(2/2)		PART NO. BA41-xxxxxx
MODULE CODE	undef ined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	43	OF 56

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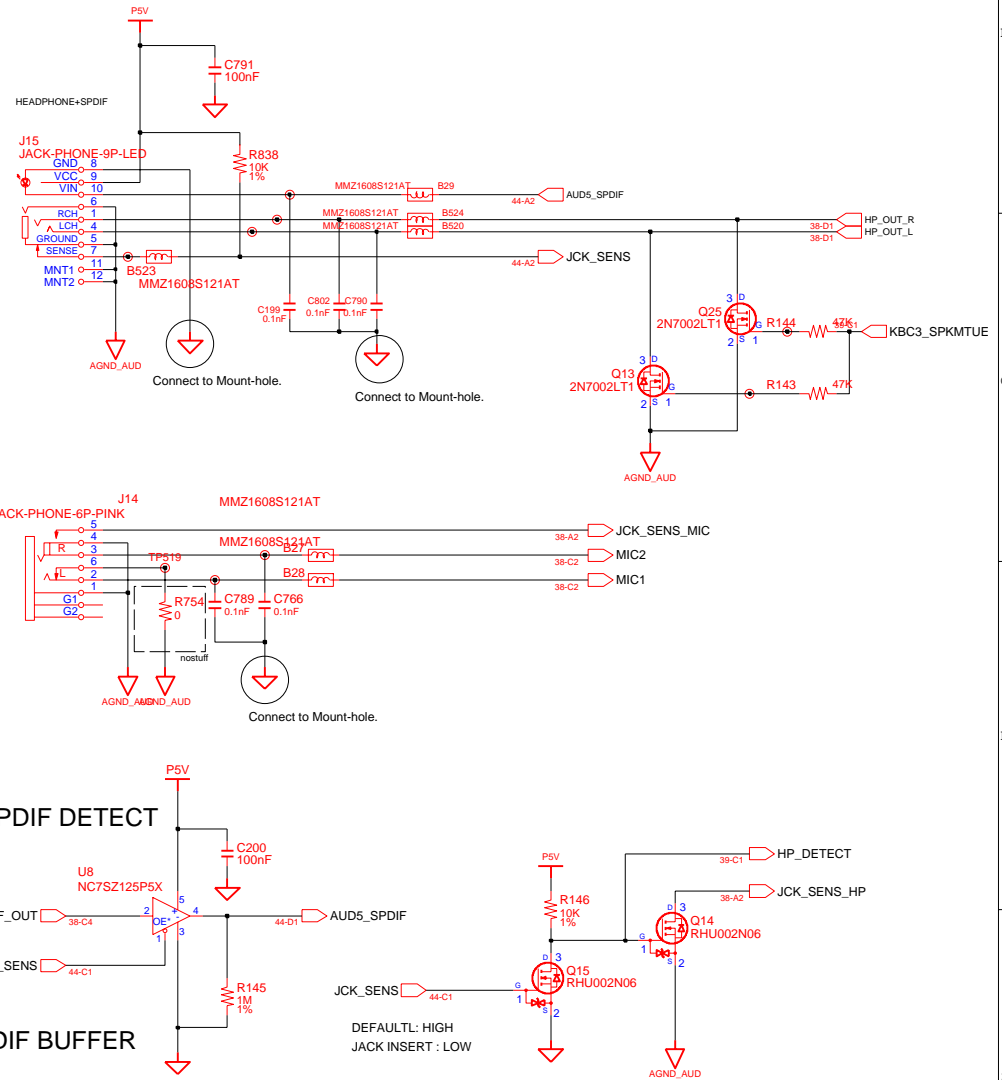
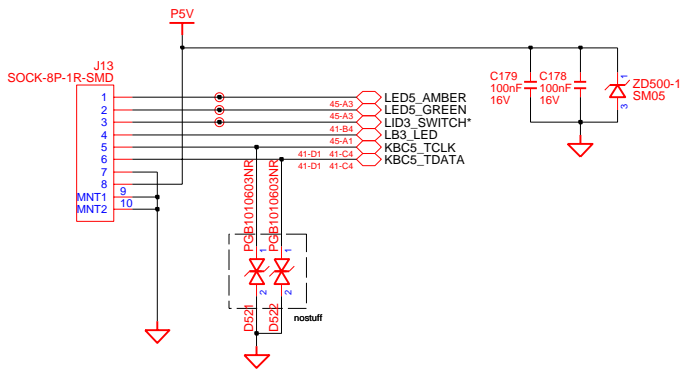
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# OPTICAL SPDIF OUTPUT & HEADPHONE

## KEYBOARD



## TOUCH PAD



DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN	<b>SAMSUNG</b> ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	SR	KBD/TPAD/HP/MIC		
APPROVAL	LIM, J.G	REV	1.0	PART NO.		BA41-xxxxxx
MODULE CODE	undef:ind	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	43	OF 55

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**USB PORT**

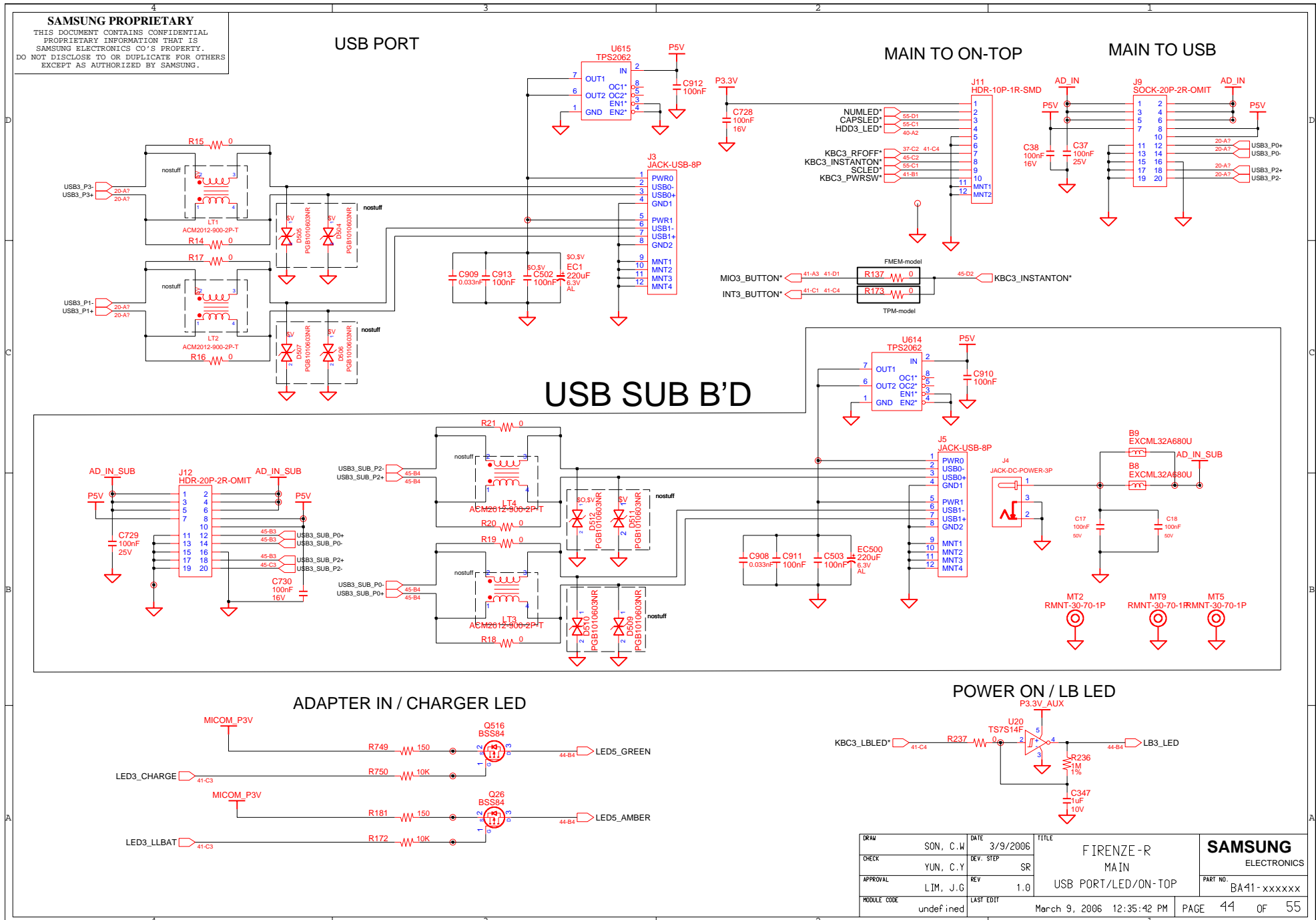
**MAIN TO ON-TOP**

**MAIN TO USB**

**USB SUB B'D**

**ADAPTER IN / CHARGER LED**

**POWER ON / LB LED**



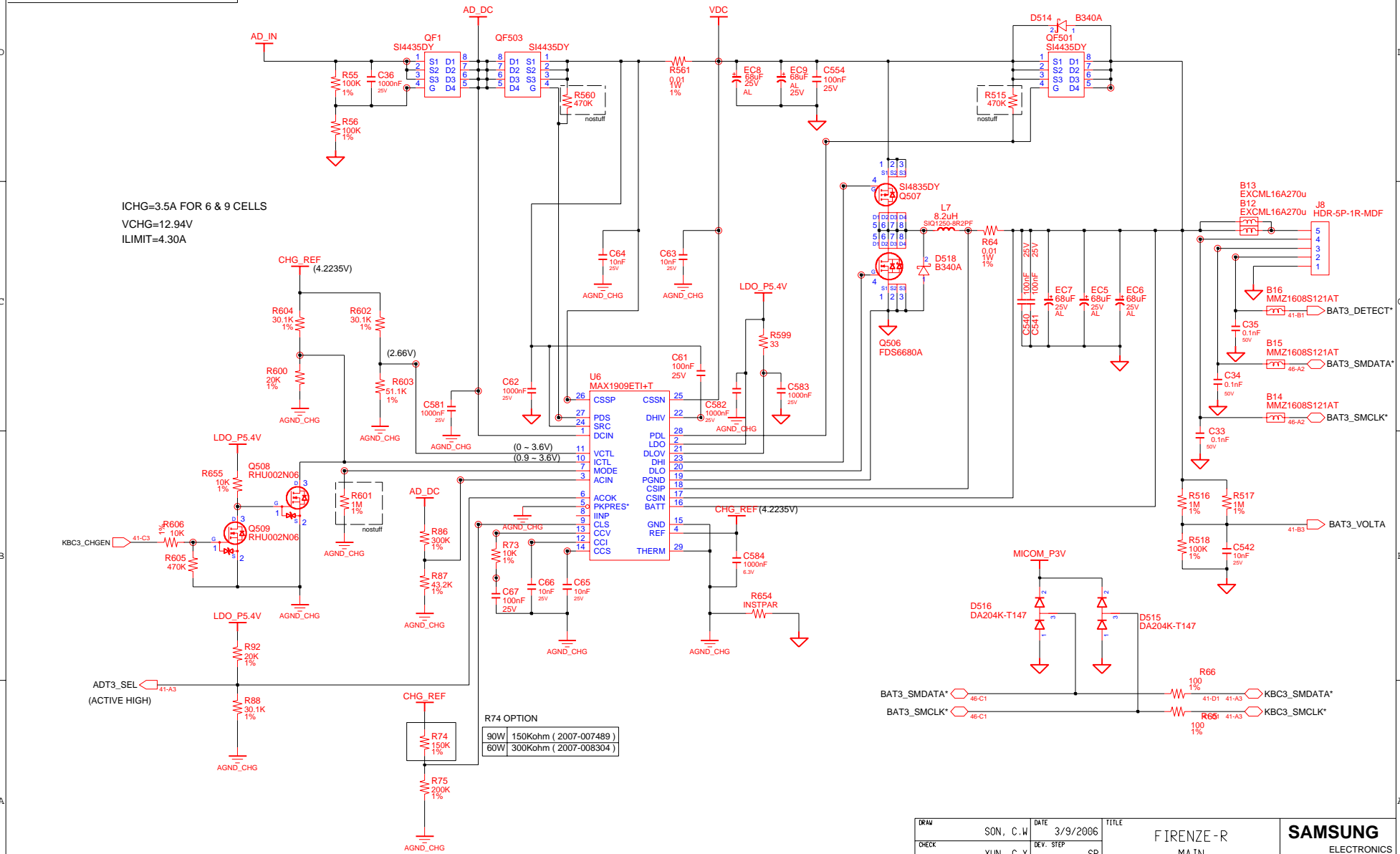
DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	SR	MAIN	PART NO.	
APPROVAL	LIM, J.G	REV	1.0	USB PORT/LED/ON-TOP	BA41-xxxxxx	
MODULE CODE	undef ined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	44	OF 55

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# CHARGER & POWER MANAGEMENT

ICHG=3.5A FOR 6 & 9 CELLS  
 VCHG=12.94V  
 ILIMIT=4.30A



R74 OPTION

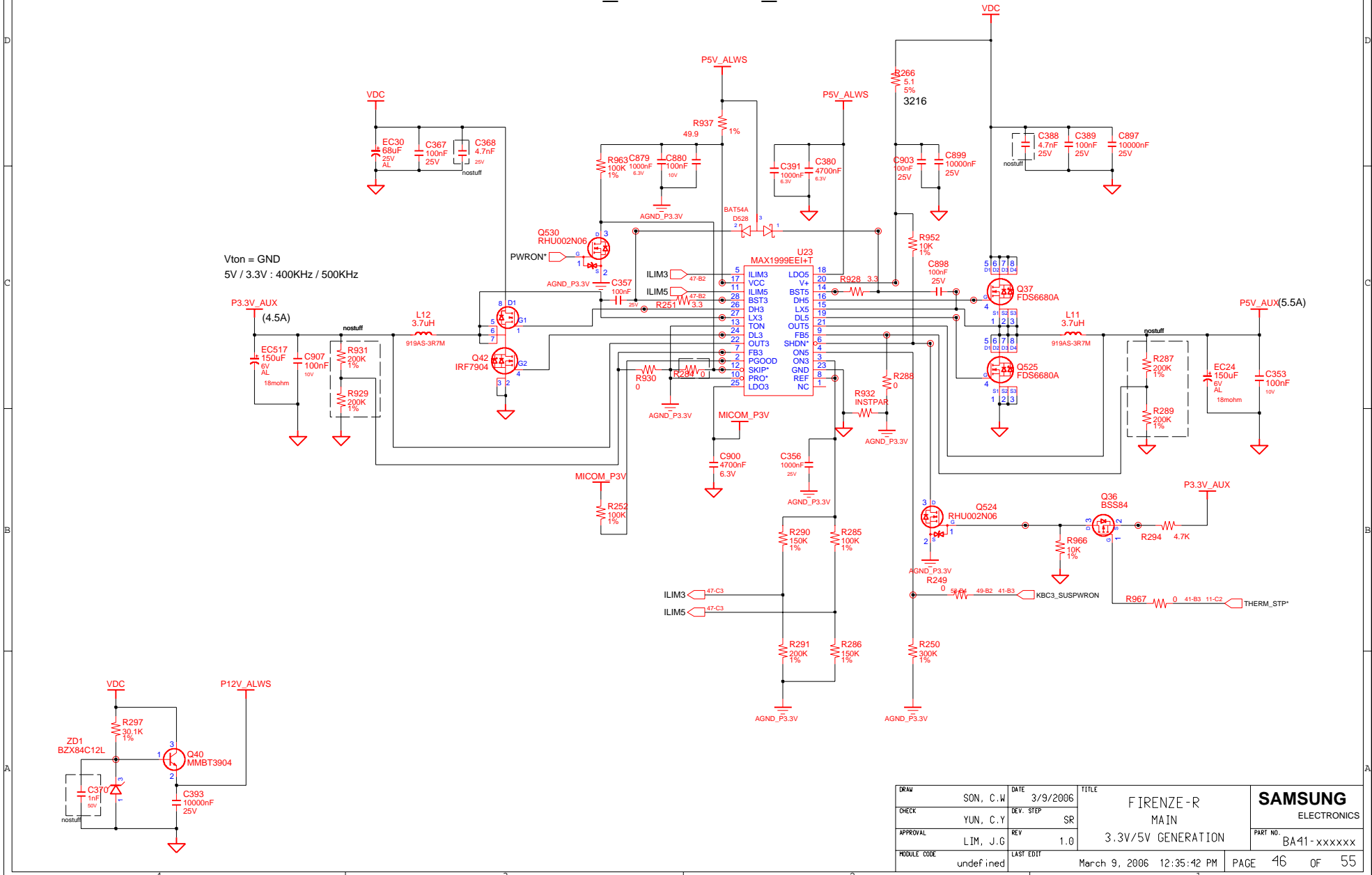
90W	150Kohm ( 2007-007489 )
60W	300Kohm ( 2007-008304 )

DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN CHARGER	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-xxxxxx
CHECK	YUN, C.Y	DEV. STEP	SR			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undef ined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	45 OF 55	

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# P3.3V\_AUX & P5V\_AUX

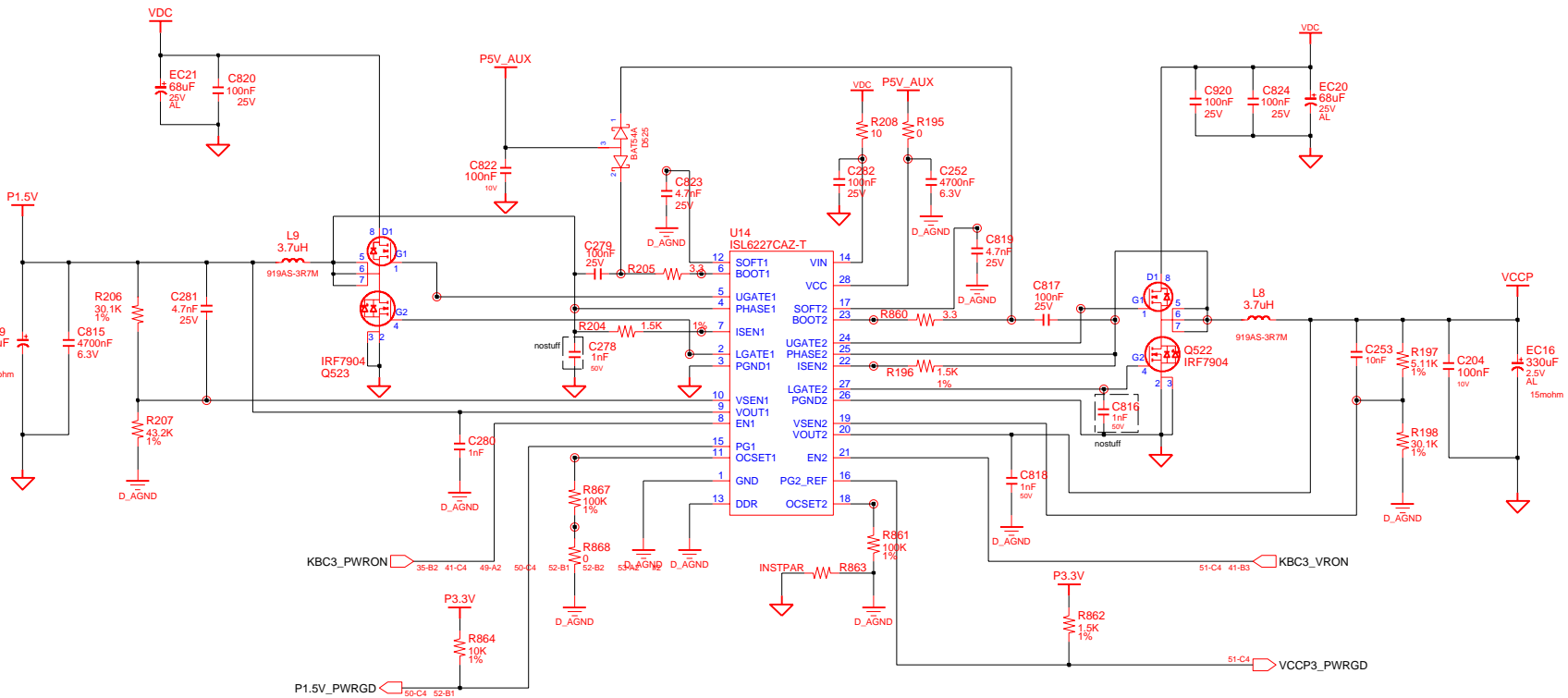


DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	SR	MAIN		
APPROVAL	LIM, J.G	REV	1.0	3.3V/5V GENERATION		PART NO. BA41-xxxxxx
MODULE CODE	undef ined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	46	OF 55

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# P1.5V & VCCP (1.05V)

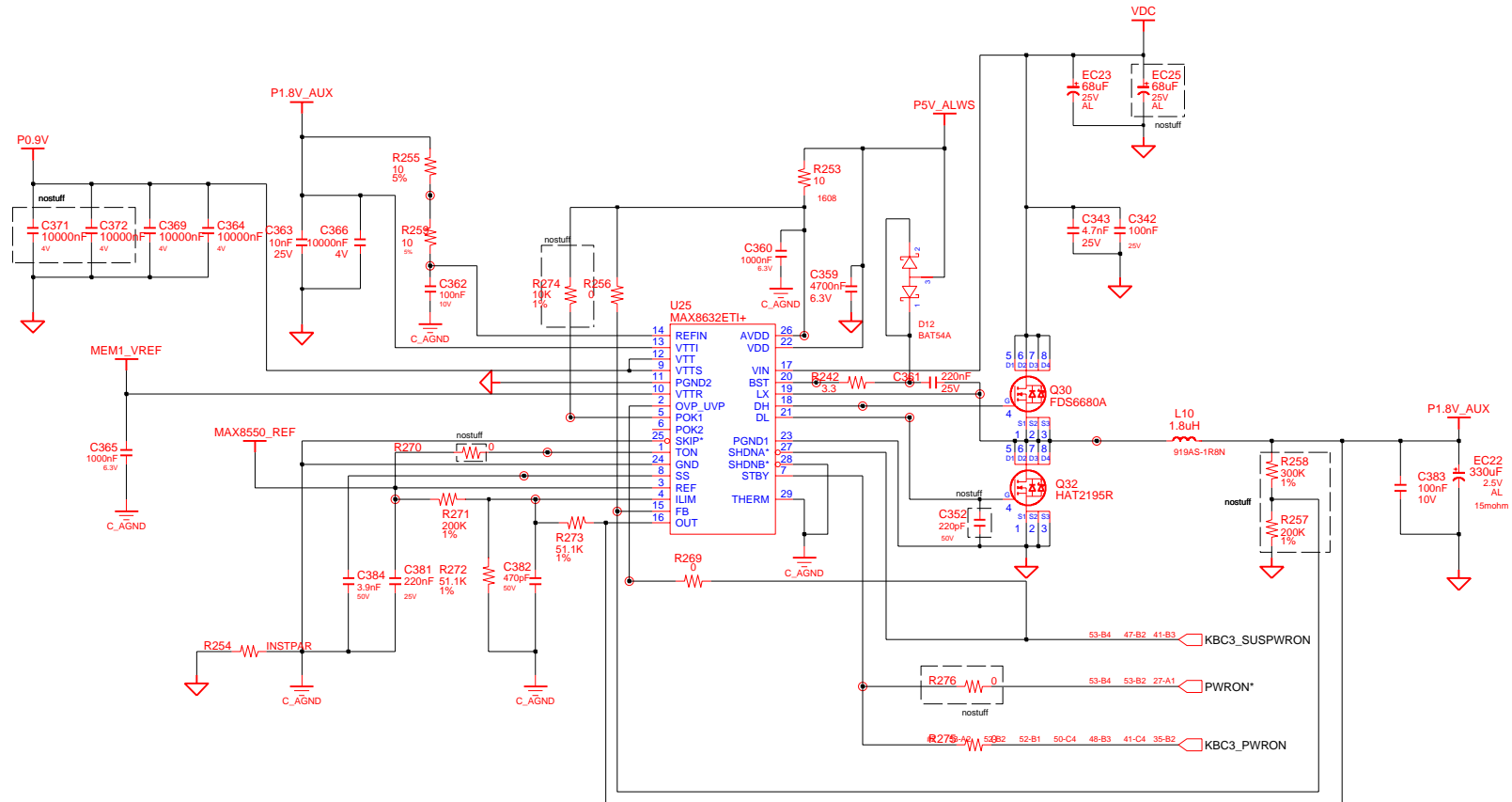


DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN 1.5V_AUX/VTT	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-xxxxxx
CHECK	YUN, C.Y	DEV. STEP	SR			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undef ined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	47 OF 55	

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# DDR2 Power

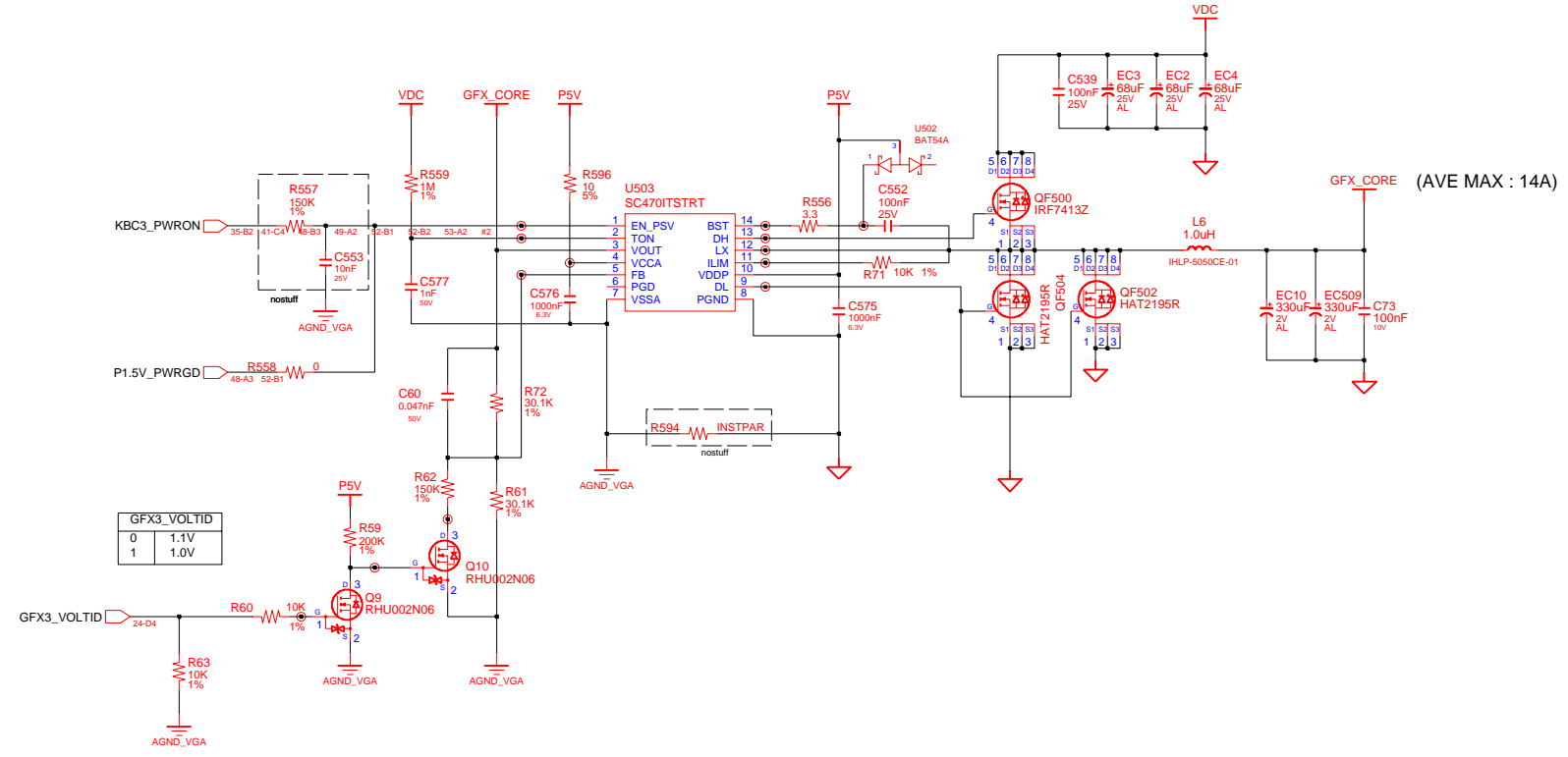


DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN DDR2 POWER	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-xxxxxx
CHECK	YUN, C.Y	DEV. STEP	SR			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undef ined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE 48 OF 55		



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# Graphic Core Power



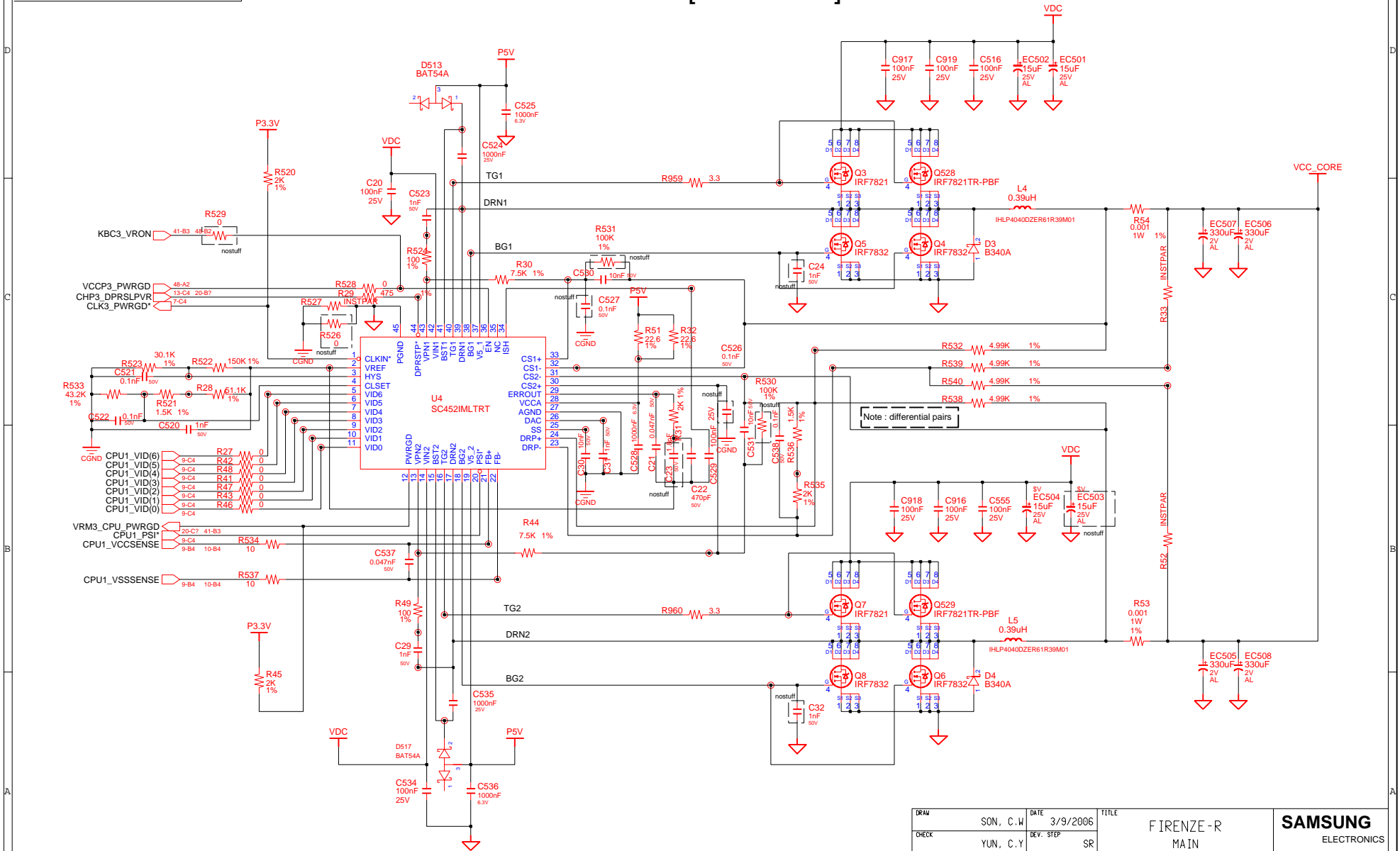
GFX3_VOLTID	
0	1.1V
1	1.0V

DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN GRAPHIC CORE POWER	<b>SAMSUNG</b> ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	SR			
APPROVAL	LIM, J.G	REV	1.0			PART NO. BA41-xxxxxx
MODULE CODE	undef ined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	49	OF 55

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# CPU VRM [SEMTECH]

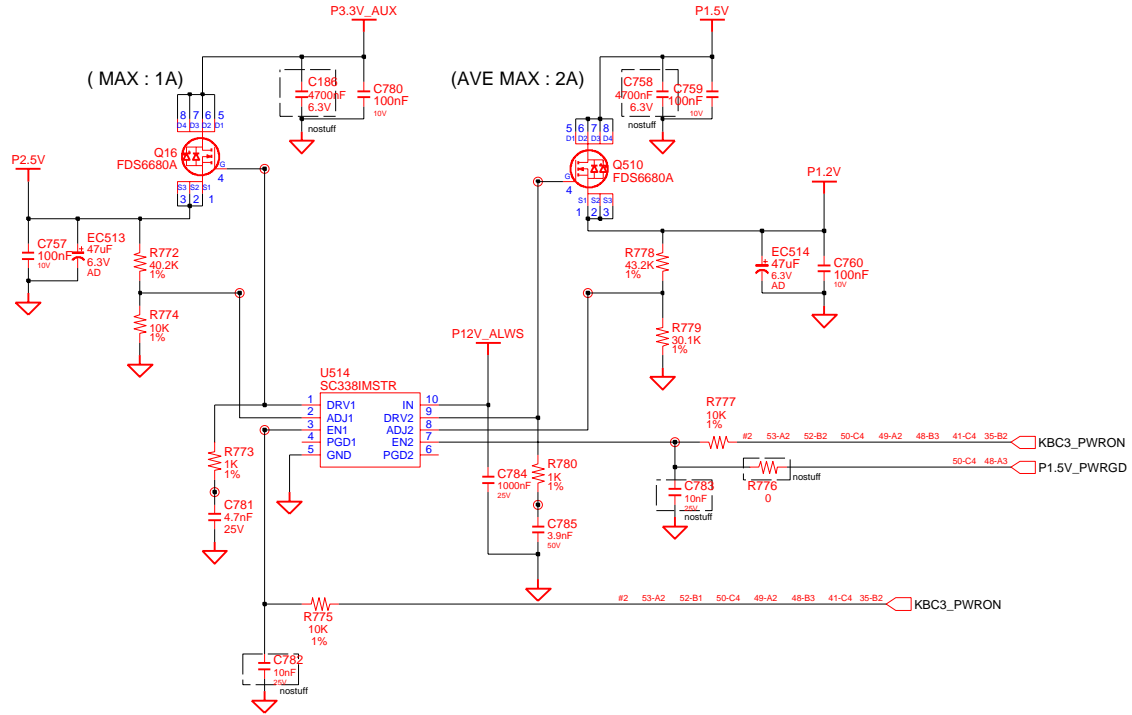


DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN CPU POWER	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-xxxxxx
CHECK	YUN, C.Y	DEV. STEP	SR			
APPROVAL	LIM, J.G	REV	1.0			
MODULE CODE	undef ined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	50 OF 55	

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# P1.2V / P2.5V POWER

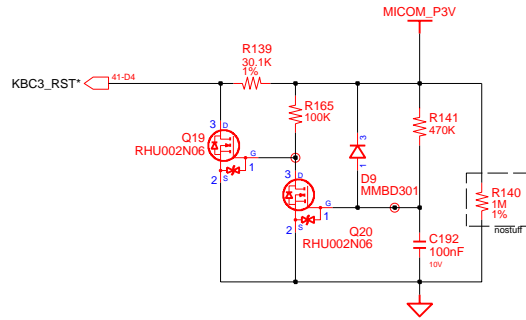


DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	SR	REV	1.0	
APPROVAL	LIM, J.G	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	51	OF 55
MODULE CODE	undef ined					

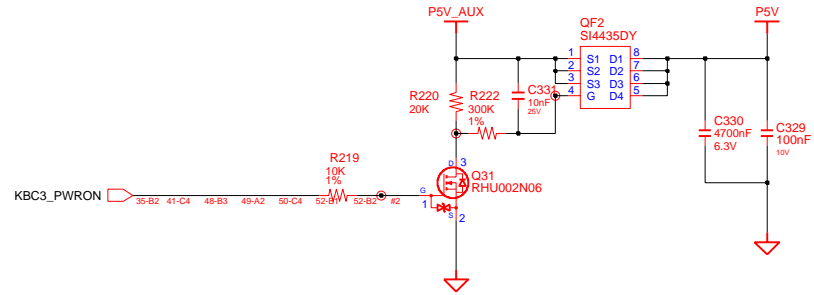
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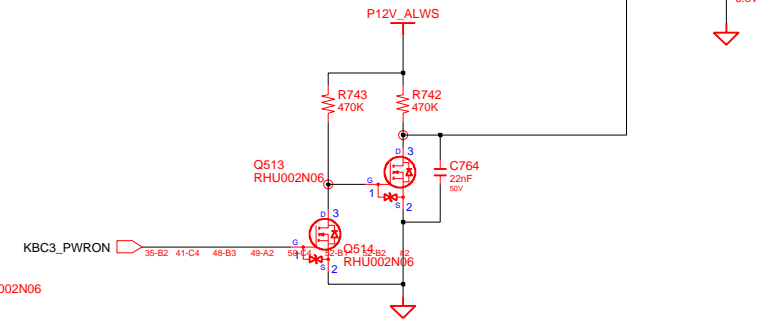
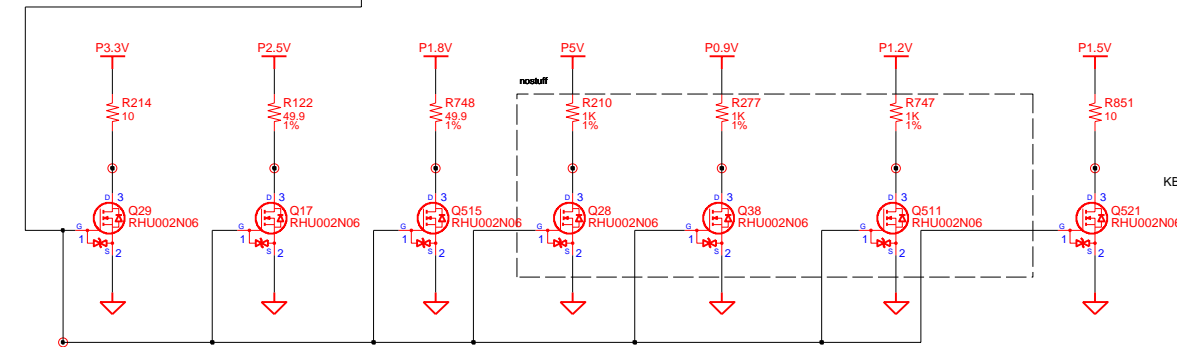
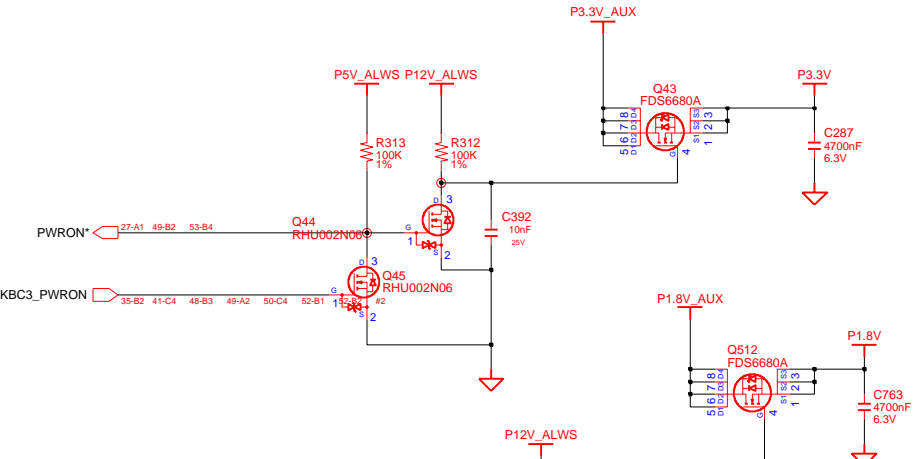
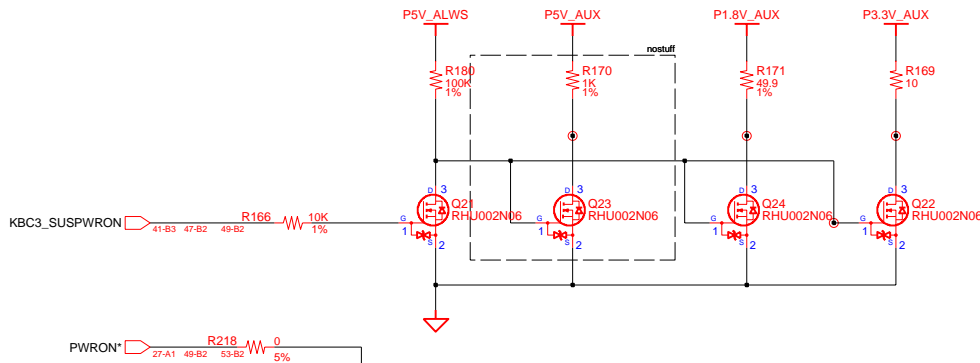
**MICOM RESET**



**Switched Power On (P5V)**



**Switched Power On (P3.3V & 1.8V)**

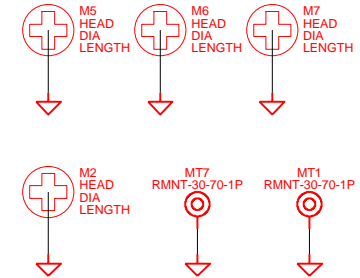
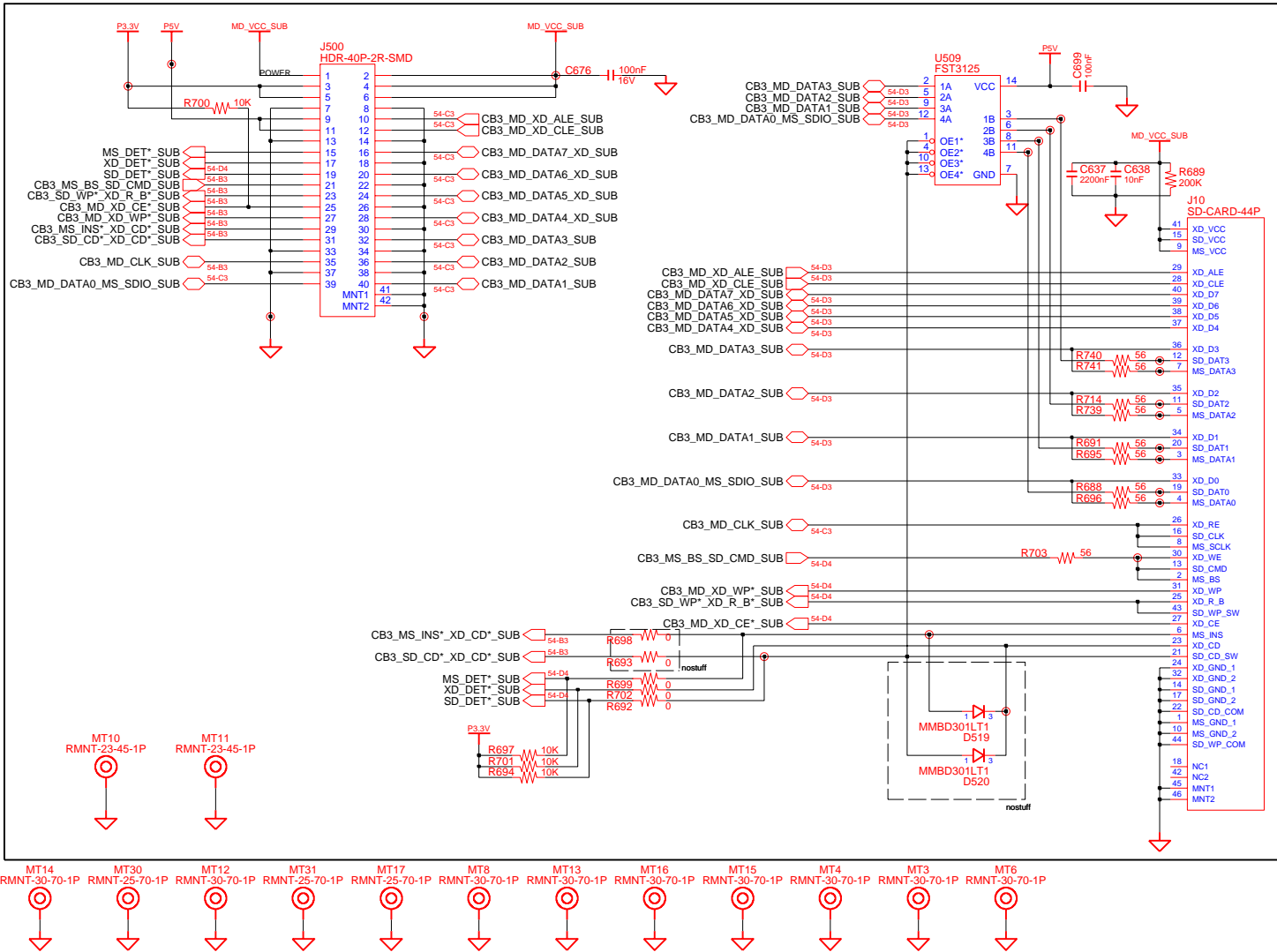


DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R MAIN	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	SR	MICOM&SWITCHED POWER	PART NO.	
APPROVAL	LIM, J.G	REV	1.0		BA41-xxxxxx	
MODULE CODE	undef ined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	52	OF 55

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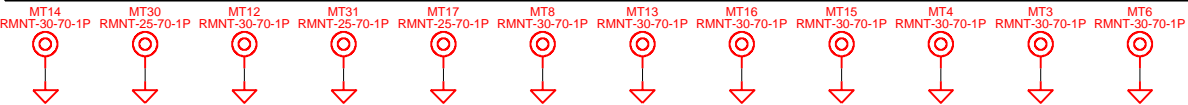
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# 5-IN-1 SUB B'D

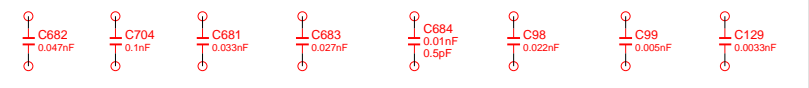


PCB REVISION CONTROL ( ICT )				
NO	CONNECTION	DATE(Y/M/D)	REVISION	STEP
1	N.C.			
2	1-2			
3	2-3			
4	3-1			
5	1-2-3			
6	N.C.			
7	1-2			
8	2-3			
9	3-1			
10	1-2-3			

REV500  
1 ○  
2 ○ 3



**CAPS FOR ICT TEST**

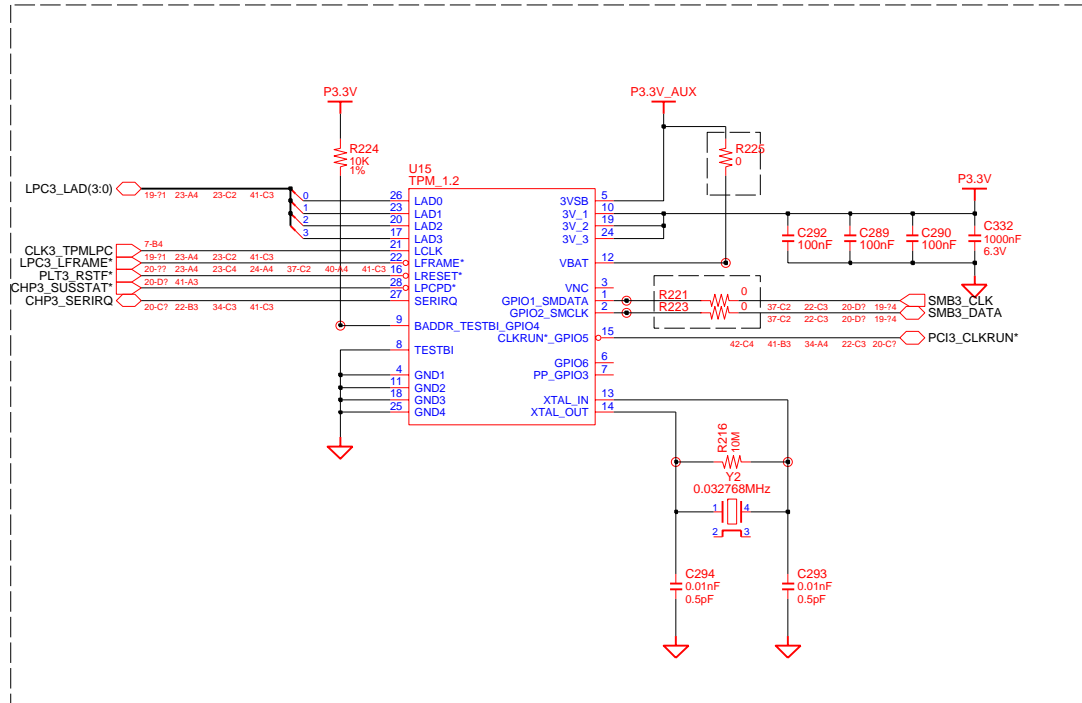


DRAW	DATE 3/9/2006	TITLE	FIRENZE-R MAIN 5-IN-1 SUB B'D	<b>SAMSUNG</b> ELECTRONICS
CHECK	DEV. STEP SR	REV 1.0	PART NO. BA41-XXXXXA	
APPROVAL	REV 1.0	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE 53 OF 55
MODULE CODE	undef:ined			

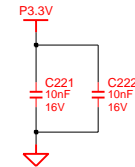
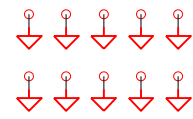
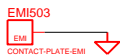
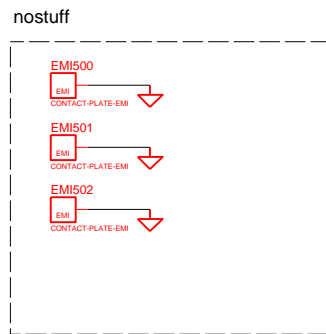
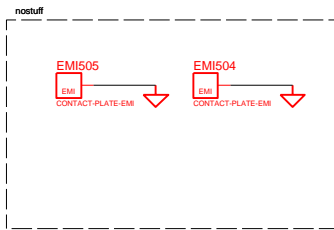
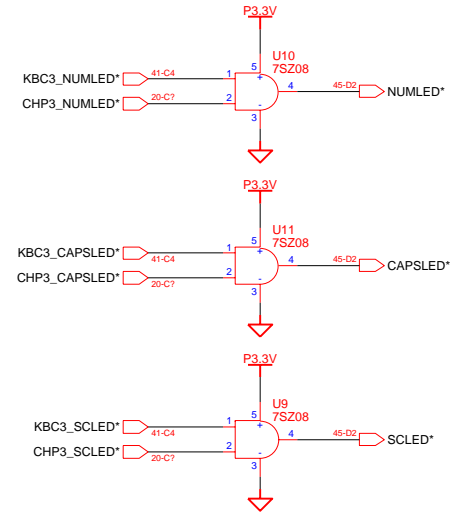
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**nostuff**



**LED SIGNAL**



DRAW	SON, C.W	DATE	3/9/2006	TITLE	FIRENZE-R	SAMSUNG ELECTRONICS
CHECK	YUN, C.Y	DEV. STEP	SR	MAIN		
APPROVAL	LIM, J.G	REV	1.0	TPM		PART NO. BA41-xxxxxx
MODULE CODE	undefined	LAST EDIT	March 9, 2006 12:35:42 PM	PAGE	54	OF 55

