OSLO2

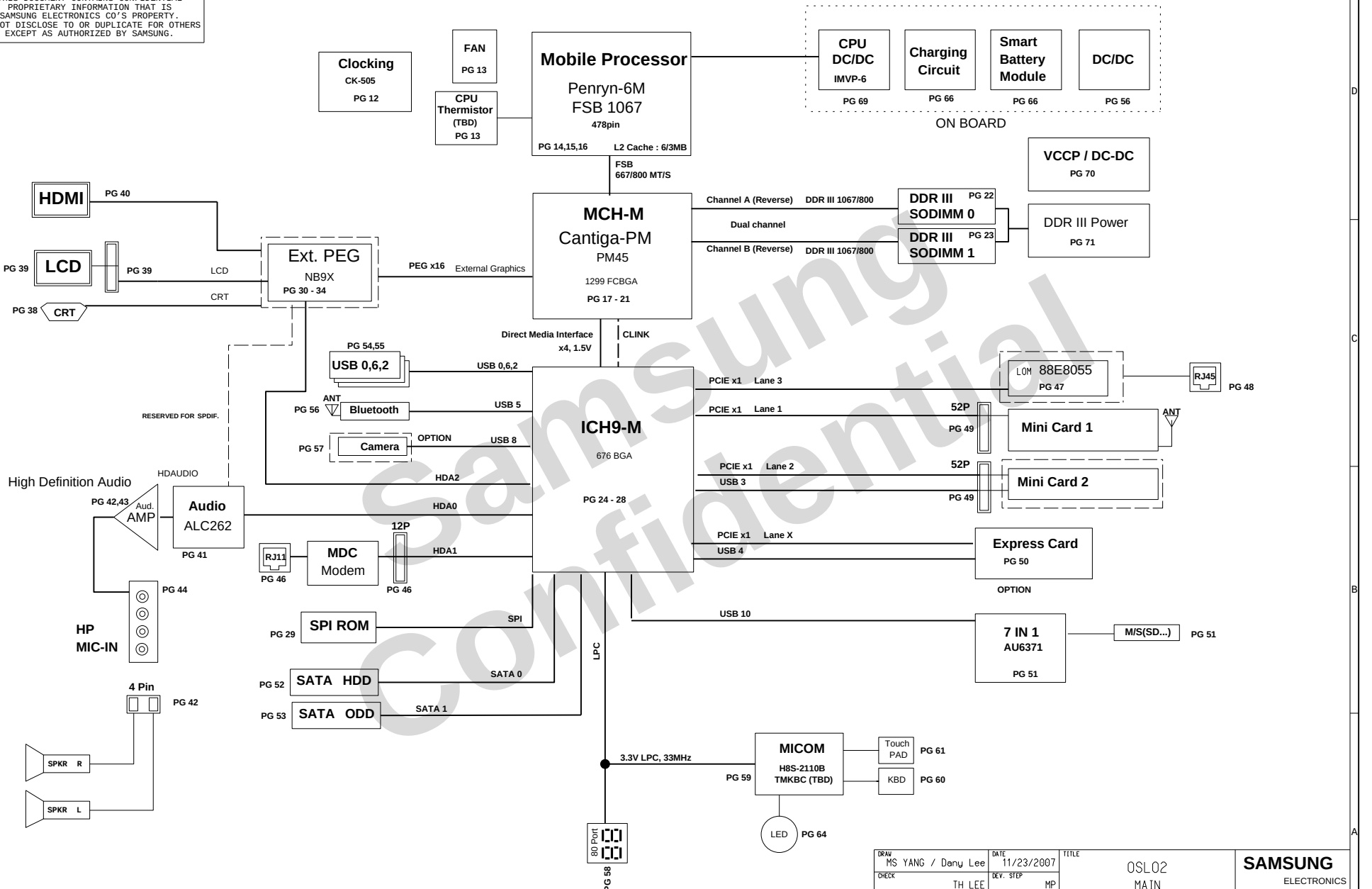
CPU : Intel Penryn-6M (1067/800) MHz
Chip Set : Intel Cantiga & ICH9M
Remarks : Montevina Platform

Model Name : Oslo2_DDR3
PBA Name : MAIN
PCB Code : BA41-00866A
BA41-00867A
Dev. Step : MP
Revision : 1.1
T.R. Date : 2008. 05.15

DRAW	CHECK	APPROVAL
MS YANG TH LEE	TH LEE	MK KIM

■ *Owner : SEC Mobile R & D* *Signature :* *X*

DRAW: MS YANG / Dany Lee	DATE: 11/23/2007	TITLE: OSLO2 MAIN COVER	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		
APPROVAL: MK KIM	REV: REV 1.1		PART NO.: BA41-00866A
MODULE CODE:	LAST EDIT: May 15, 2008 08:19:32 AM	PAGE 1 OF 13	



DRAW: MS YANG / Dany Lee	DATE: 11/23/2007	TITLE: OSLO2 MAIN BLOCK DIAGRAM	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		
APPROVAL: MK KIM	REV: REV 1.1		PART NO.: BA41-00866A
MODULE CODE: undefined	LAST EDIT: May 15, 2008 08:19:32 AM	PAGE 2 OF 13	

BOARD INFORMATION

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
Cardbus	AD25	3	A,B,C
USB	AD29(internal)	-	USB2.0 #0 (USB0) : A USB2.0 #1 (USB1) : D USB2.0 #2 (USB4) : C USB2.0 #3 (USB5) : E USB2.0 #4 (EHCI) : H
Hub to PCI	AD30(internal)	-	-
LPC bridge/IDE/AC97/SMBUS	AD31(internal)	-	B
Internal MAC	AD24(internal)	-	E
AC Link	-	-	B
GLAN	-	-	F

Voltage Rails

VDC	Primary DC system power supply (7 to 21V)
VCC_CORE	Core Voltage for CPU
GFX_CORE	Core Voltage for GPU
P1.05V (VCCP)	VTT for CPU, Crestline & ICH9-M
P3.3V_MICOM	3.3V always power rail (for Micom)
P1.8V	1.8V switched power rail (off in S3-S5)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.5V_AUX	1.5V power rail for DDR (off in S4-S5)
P0.75V	0.75V power rail for DDR (off in S3-S5)
P3.3V	3.3V switched power rail (off in S3-S5)
P3.3V_AUX	3.3V switched on power rail (off in S4-S5)
P5.0V	5.0V switched power rail (off in S3-S5)
P5.0V_AUX	5.0V switched on power rail (off in S4-S5)
P5.0V_ALW	5.0V always power rail

USB PORT Assign

PORT #	ASSIGNED TO
0	SYSTEM PORT 2
1	NC
2	SYSTEM PORT 1
3	Mini Card
4	Express Card
5	Bluetooth
6	SYSTEM PORT 2
7	NC
8	Camera
9	NC
10	Multi Card Reader (7-in-1)
11	NC

PCI Express Assign

PORT #	ASSIGNED TO
1	Mini Card 1 (WLAN)
2	Mini Card 2 (ROBSON or DVB-T)
3	Express Card
4	LOM
5	NC
6	NC

Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	ICH9-M	Real Time Clock
Crystal	10MHz	MICOM	HD64F2169/2160
Crystal	14.318MHz	CLOCK-Generator	CK-505
Crystal	25MHz	LAN	Marvell LAN (88E8850)
Crystal	12MHz	Multi Card Reader	Alkor AU6371

LCD Pannel Detect (EDID)

Devices	Resolution	PANNEL_DETECT_0

I²C / SMB Address

Devices	Address	Hex	Bus
ICH9-m	Master	-	SMBUS Master
SODIMM0	1010 000x	A0h	-
SODIMM1	1010 010x	A4h	-
Thermal Sensor on SODIMM0	0011 000x	30h	-
Thermal Sensor on SODIMM1	0011 010x	34h	-
CK-505M (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable
MICOM	Master	-	SMBUS Master
Battery	0001011x	16h	Battery
CPU Thermal Sensor	0111 101x	7Ah	Thermal Sensor (EMC2012)

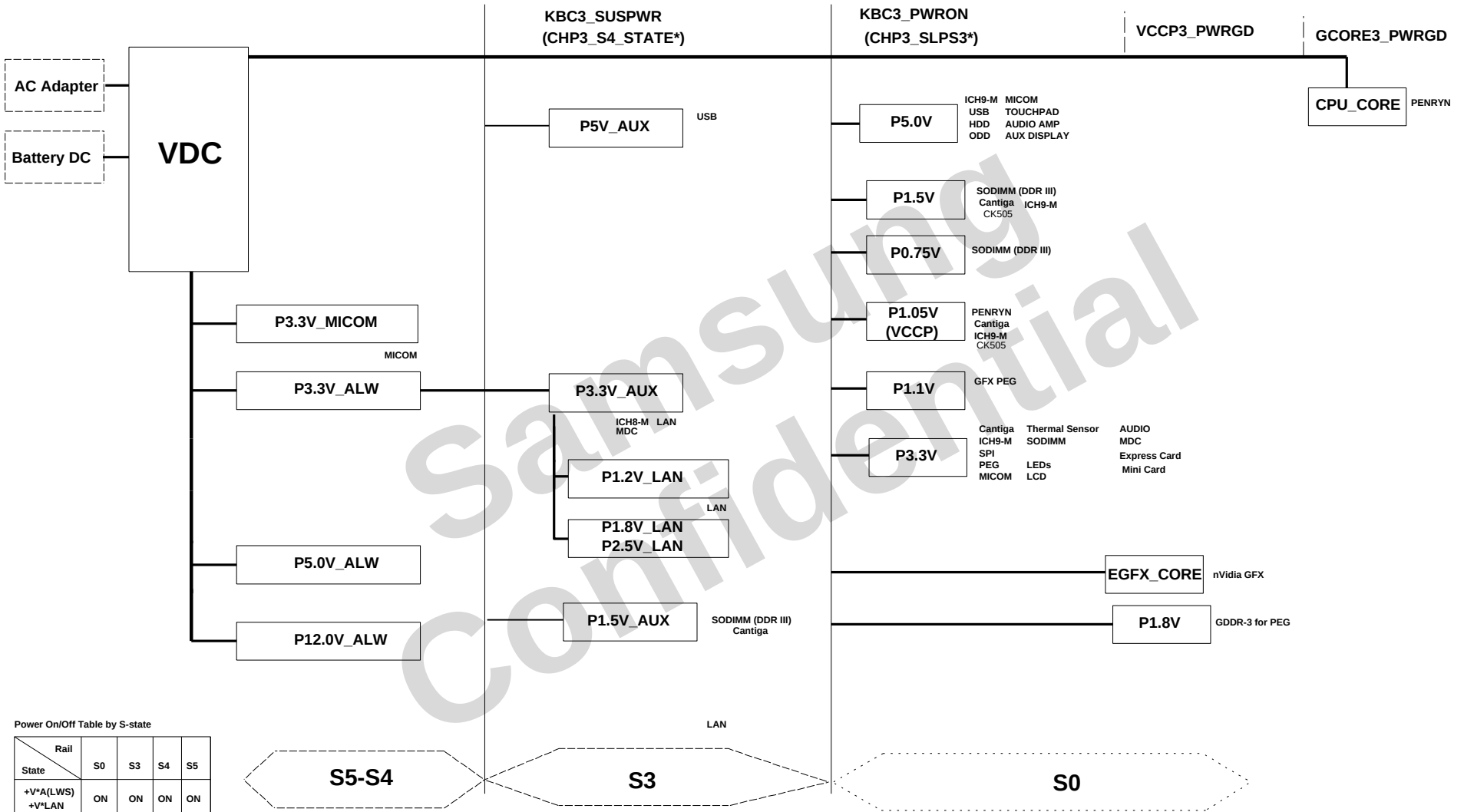
REVISION HISTORY

See rev notes for more information.

DRAW: MS YANG / Dany Lee	DATE: 11/23/2007	TITLE: OSL02 MAIN BOARD INFO	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		
APPROVAL: MK KIM	REV: REV 1.1		PART NO.: BA41-00866A
MODULE CODE: undefined	LAST EDIT: May 15, 2008 08:19:32 AM	PAGE 3 OF 13	

POWER DIAGRAM

Rev 0.1



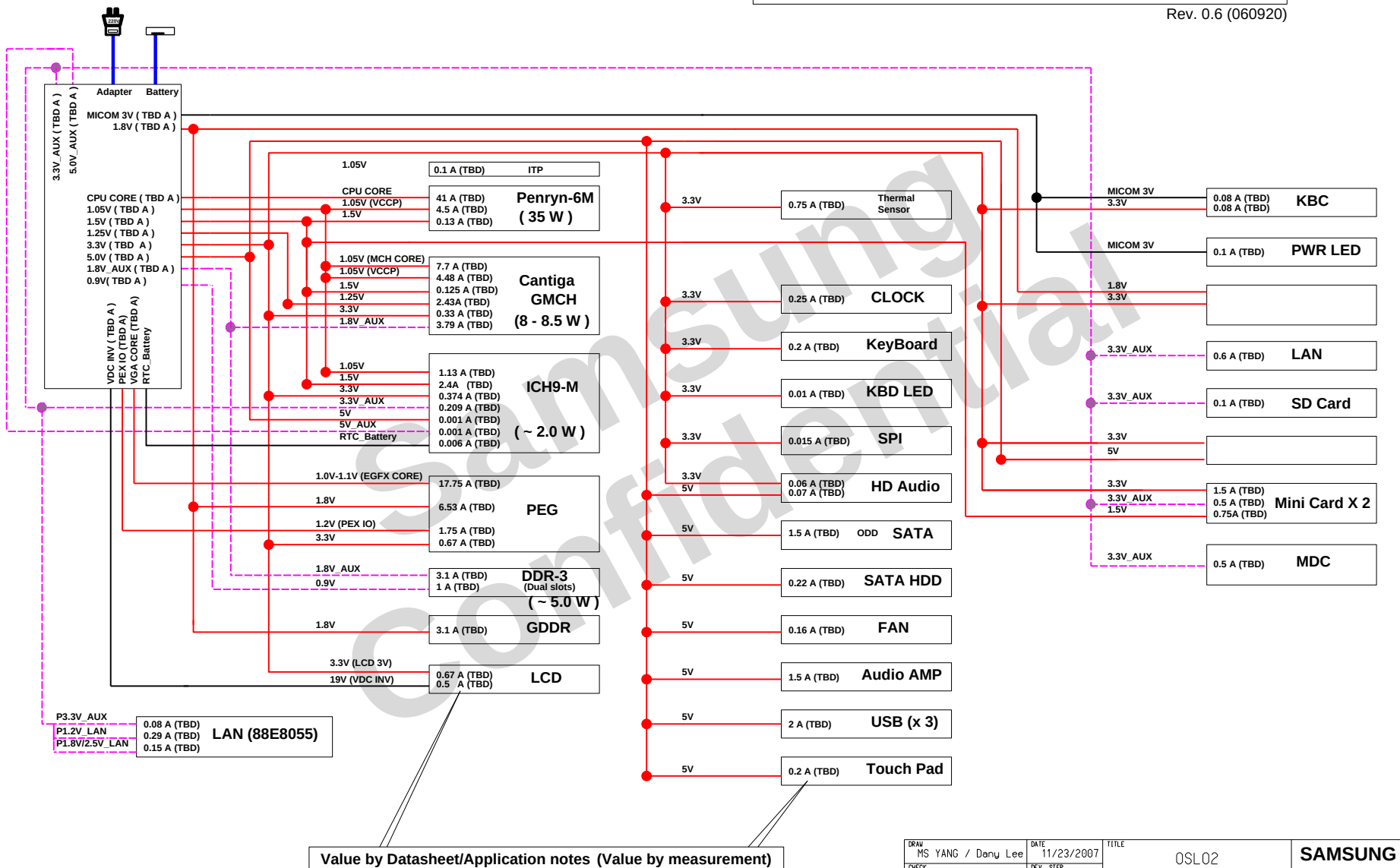
Power On/Off Table by S-state

Rail / State	S0	S3	S4	S5
+V*A(LWS) +V*LAN	ON	ON	ON	ON
+1.8V_AUX +0.9V	ON	ON	—	—
+V*AUX	ON	ON	—	—
+V	ON	—	—	—
+V* (CORE)	ON	—	—	—

DRAW: MS YANG / Dany Lee	DATE: 11/23/2007	TITLE: OSLO2 MAIN POWER DIAGRAM	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		PART NO.: BA41-00866A
APPROVAL: MK KIM	REV: REV 1.1		
MODULE CODE: undefined	LAST EDIT: May 15, 2008 08:19:32 AM	PAGE 4 OF 13	

POWER RAILS ANALYSIS

Rev. 0.6 (060920)



Value by Datasheet/Application notes (Value by measurement)

DRAW: MS YANG / Dany Lee	DATE: 11/23/2007	TITLE: OSLO2 MAIN POWER RAILS	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		
APPROVAL: MK KIM	REV: REV 1.1		PART NO.: BA41-00866A
MODULE CODE: undefined	LAST EDIT: May 15, 2008 08:19:32 AM		PAGE 5 OF 13

POWER SEQUENCE

Rev. 0.9

Host Boot / ME Off
(SLPS4* = S4_STATE*) > (SLPM* = SLPS3*)
M-1) KBC3_DDR_PWRON (TBD) = 8) KBC3_SUSPWR
M-2) KBC3_ME_PWRON = 15) KBC3_PWRON

Host / ME Boot
(SLPS4* = S4_STATE*) > SLPM* > SLPS3*

Host S5 / ME Boot
(SLPS4* = SLPM*) > S4_STATE* > SLPS3*

POWER S/W

4) POWER_SW*

KBC
110ms Delay
Sheet 59

8) CHP3_SLPS5#/4#/3#
7) KBC3_RSMRST#
17) KBC3_PWRGD
15)VRM3_CPU_PWRGD
13) KBC3_VRON
5) KBC3_SUSPWR
9) KBC3_PWRON

ICH9-M
PRTC PRTC
LAN100_SLP
INTVRMEN
PWROK
CL_PWROK
VRMPWRGD
Sheet 24-28

6) P3.3V_AUX
10-1) ICH_CORE (P1.05V)
19) PCI3_RST*
19) PLT3_RST*
17) KBC3_PWRGD
17) KBC3_PWRGD
15) VRM3_CPU_PWRGD

7) P1.05V_AUX
7) P1.5V_AUX

18) CPU1_PWRGDCPU
10-1) P1.05V
10-1) P1.5V
CPU
Sheet 14-16
20) CPU1_CPURST*

16) CLK3_PWRGD
CK-505
Sheet 12
16-1) Clock Running

Adapter
Battery
AC_DC / Battery
ISL6256A
Sheet 66
2) VDC
2-1) P12.0V_ALW
P3.3V_MICOM
5) KBC3_SUSPWR

6) P3.3V_AUX
9) KBC3_PWRON
AP6680AGM
Sheet 68
9-1) KBC3_PWRON_INV#
10-1) P3.3V

6) P1.5V_AUX
AP6680AGM
Sheet 68
10-1) P1.5V

6) P5.0V_AUX
AP4435GM
Sheet 68
10-1) P5.0V
10-2) P5.0V_AUD

11) VCCP3_PWRGD (Back-upl)
12)GCORE3_PWRGD (PM-model)
13) KBC3_VRON (Back-up)
CPU VRM
Sheet 69
14) CPU_CORE

10) P1.05V
GMCH
PWROK
CL_PWROK
Sheet 15-19
19) PLT3_RST*
17) KBC3_PWRGD
6) P1.8V_AUX
10-1) P3.3V

2) VDC
10) P5.0V

P3.3V_AUX & P5V_AUX
TPS51124
Sheet 67
P5.0V_ALW
P3.3V_ALW
6) P5.0V_AUX

2) VDC
SC415
Sheet 70
10) P1.1V
10) P1.05V (VCCP)
11) VCCP3_PWRGD
9) KBC3_PWRON

GDDR3 POWER
SC486
Sheet 72
11-2) P1.8V

SC471
Sheet 73
11-1) EGFX_CORE
12)GCORE3_PWRGD

Devices
10-1) P5.0V
10-1) P3.3V
10-1) P1.5V
10-1) P1.05V

GFX
Sheet 30-40
10-1) P1.1V
10-1) P3.3V
11-1) EGFX_CORE
11-2) P1.8V

6) P3.3V_AUX
CHP3_RTCRST#
RTC Battery

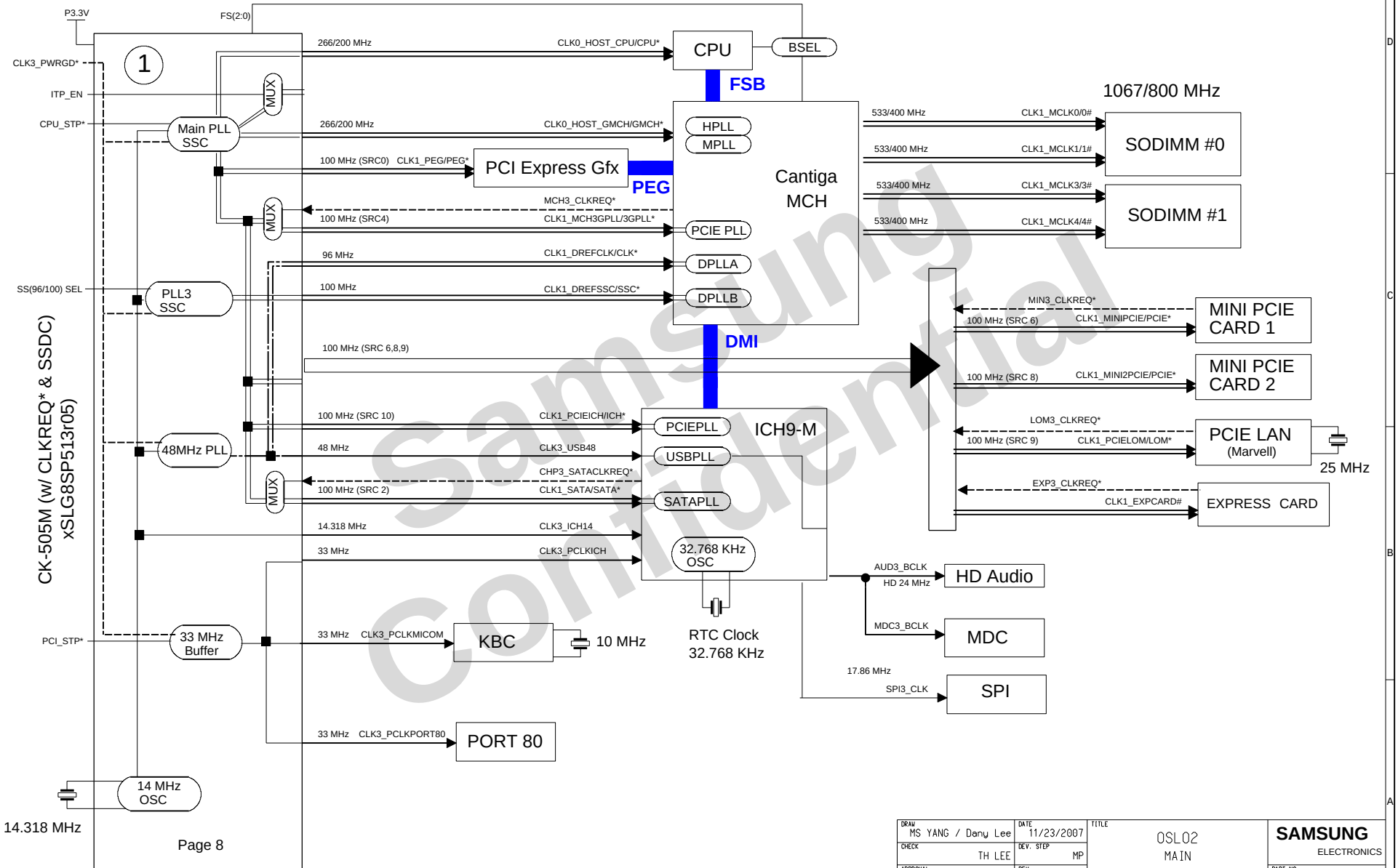
DDR3 POWER
SC486
Sheet 71
10) P5.0V
2) VDC
5) KBC3_SUSPWR
6) P1.5V_AUX
6) MEM1_VREF
10-2) 0.75V

LOM Marvell
Sheet 47-48
6-1) P1.2V_LAN
6-1) P1.8V/P2.5V_LAN
BCP69
Sheet 47

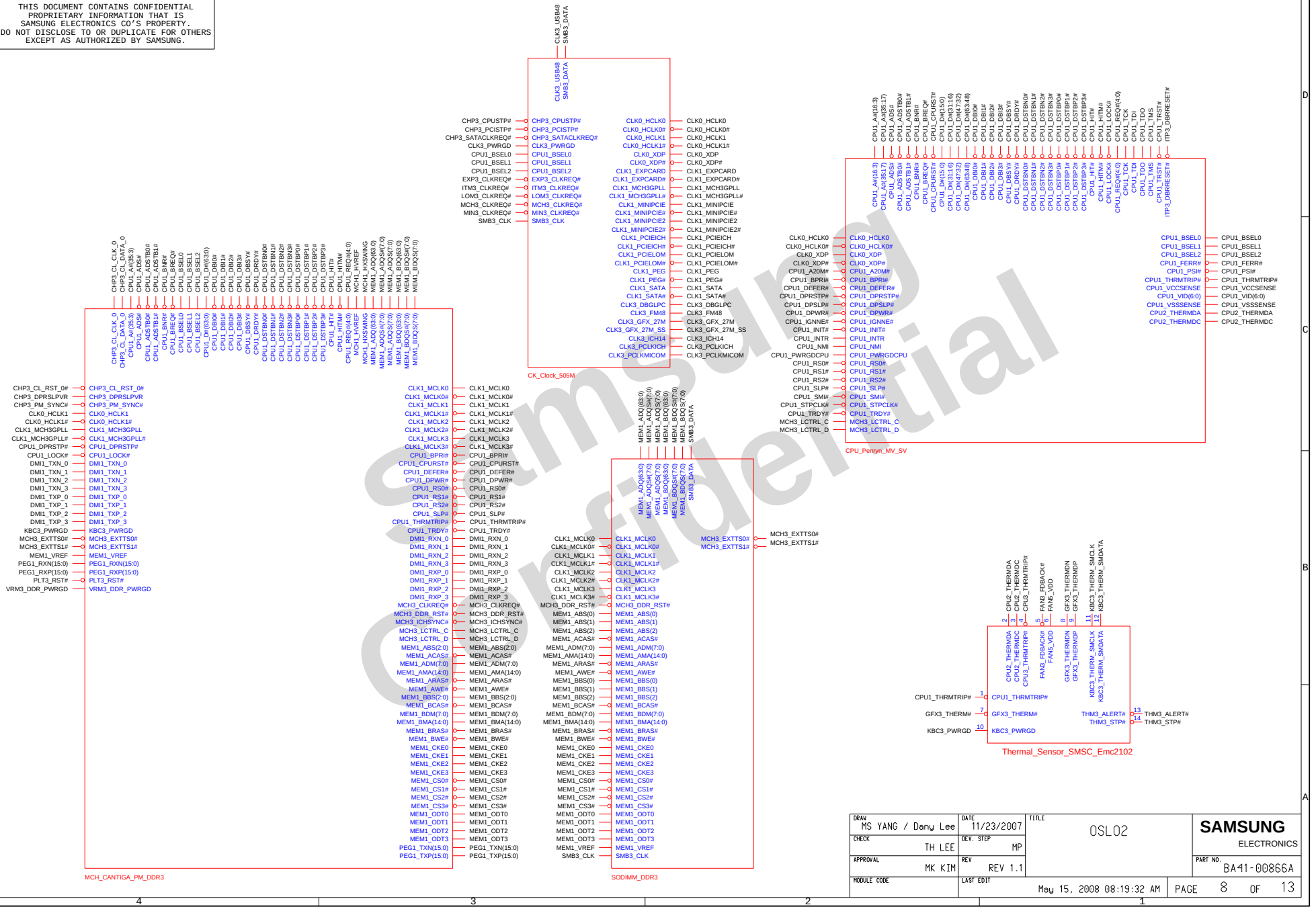
6) P1.5V_AUX
10-2) P0.75V
DDR3 Memory
Sheet 22-23

DRAW: MS YANG / Dany Lee	DATE: 11/23/2007	TITLE: OSLO2 MAIN POWER SEQUENCE	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		PART NO.: BA41-00866A
APPROVAL: MK KIM	REV: REV 1.1		
MODULE CODE: undefined	LAST EDIT: May 15, 2008 08:19:32 AM	PAGE 6 OF 13	

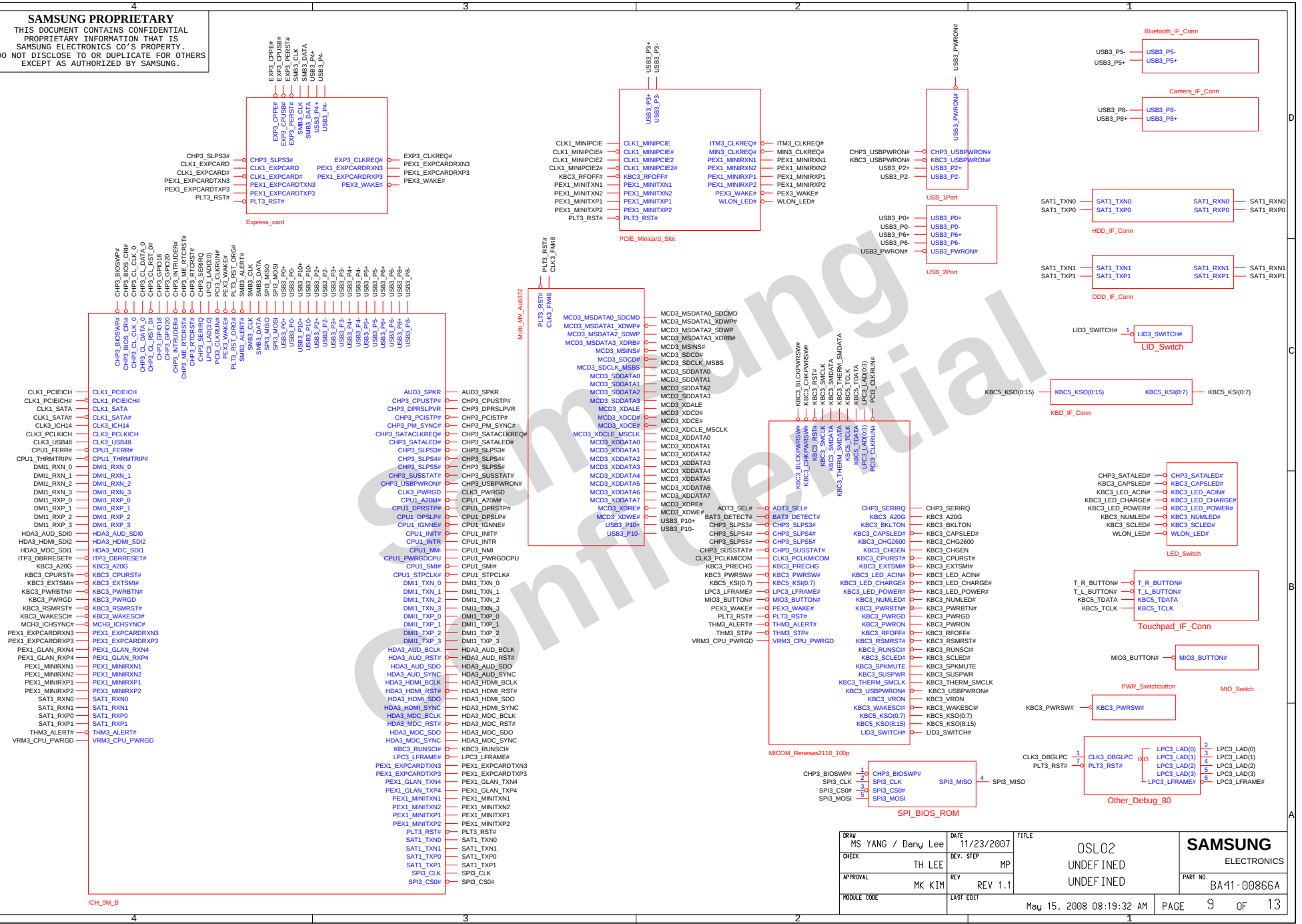
CLOCK DISTRIBUTION Rev. 0.1



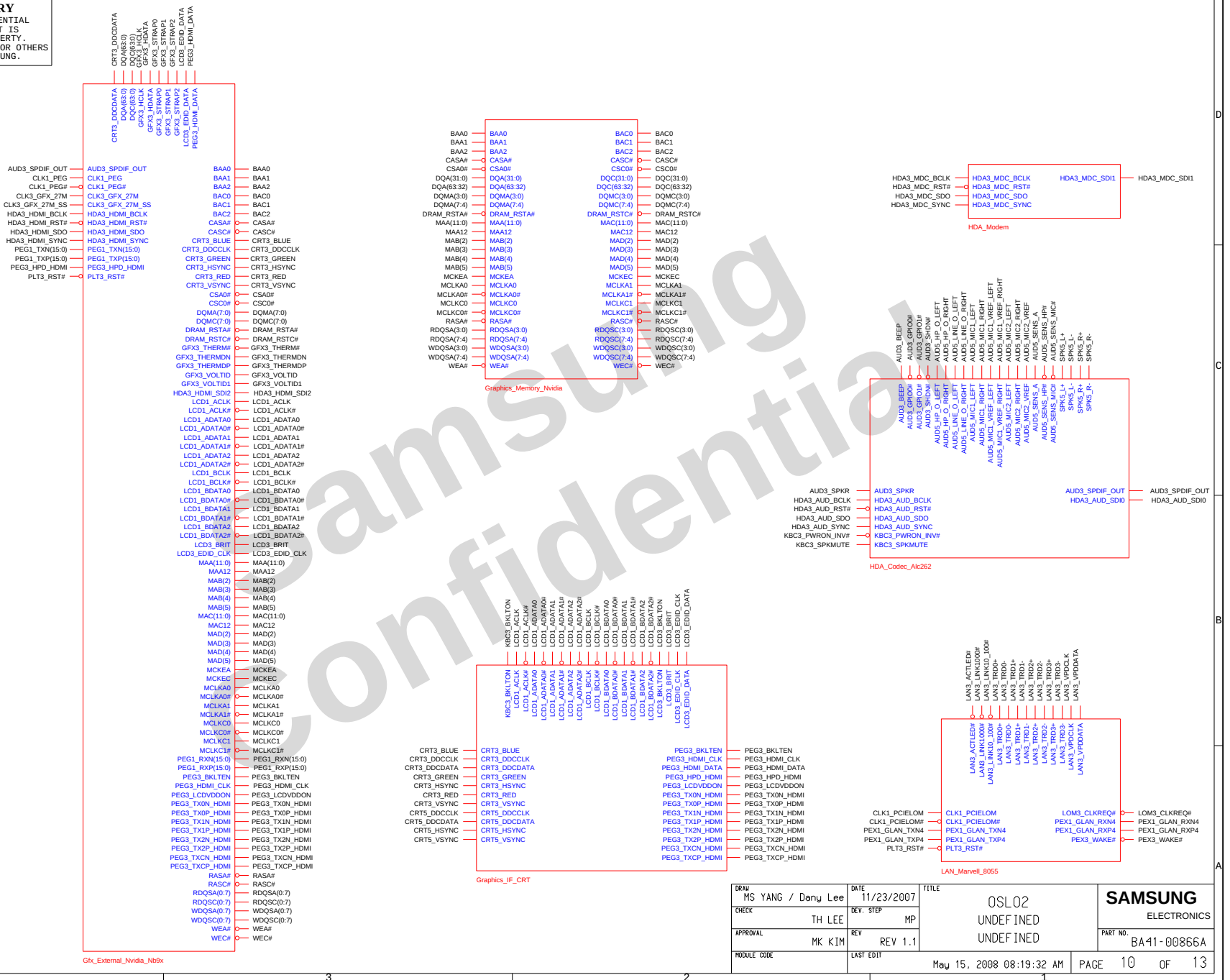
DRAW: MS YANG / Dany Lee	DATE: 11/23/2007	TITLE: OSLO2 MAIN CLOCK DIAGRAM	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		
APPROVAL: MK KIM	REV: REV 1.1		PART NO.: BA41-00866A
MODULE CODE: undefined	LAST EDIT: May 15, 2008 08:19:32 AM		PAGE 7 OF 13



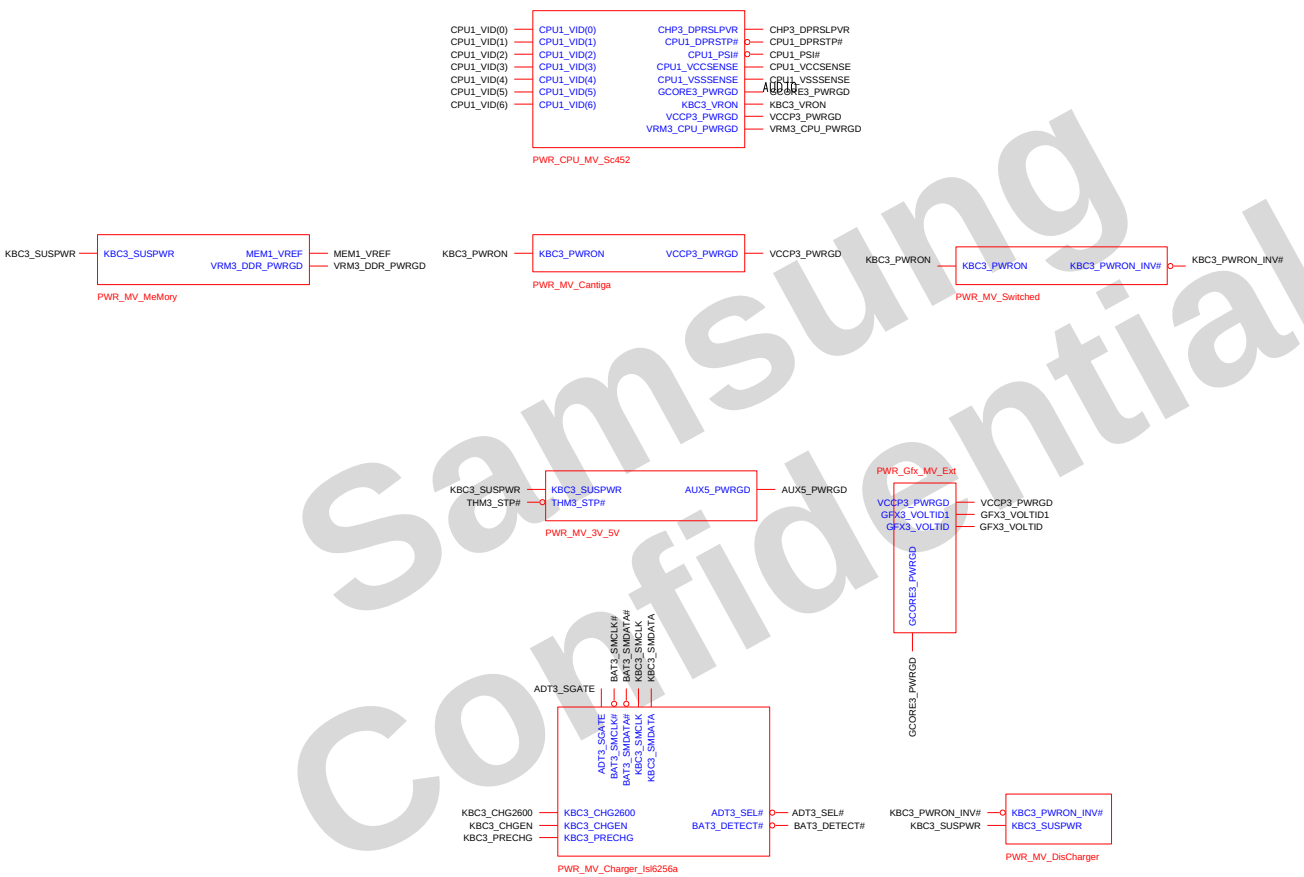
DRAW: MS YANG / Dany Lee	DATE: 11/23/2007	TITLE: OSL02	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		PART NO.: BA41-00866A
APPROVAL: MK KIM	REV: REV 1.1		
MODULE CODE:	LAST EDIT: May 15, 2008 08:19:32 AM	PAGE 8 OF 13	



DRAW: MS YANG / Dany Lee	DATE: 11/23/2007	TITLE: OSLO2 UNDEFINED UNDEFINED	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		PART NO.: BA41-00866A
APPROVAL: MK KIM	REV: REV 1.1		
MODULE CODE:	LAST EDIT: May 15, 2008 08:19:32 AM	PAGE 9 OF 13	

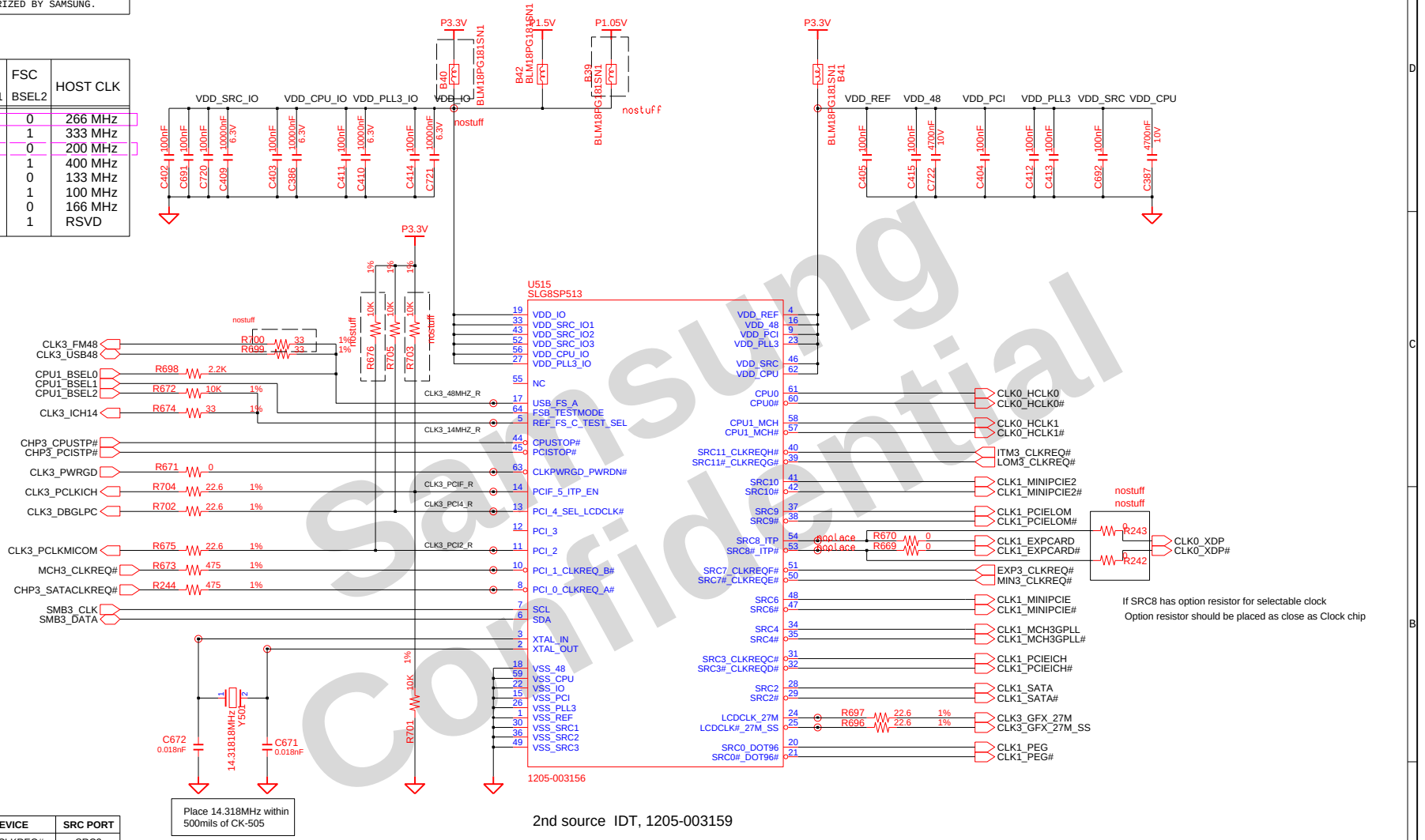


DRAW: MS YANG / Dany Lee	DATE: 11/23/2007	TITLE: OSLO2 UNDEFINED UNDEFINED	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		PART NO.: BA41-00866A
APPROVAL: MK KIM	REV: REV 1.1		
MODULE CODE:	LAST EDIT: May 15, 2008 08:19:32 AM	PAGE 10 OF 13	



DRAW: MS YANG / Dany Lee	DATE: 11/23/2007	TITLE: OSLO2 UNDEFINED UNDEFINED	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		
APPROVAL: MK KIM	REV: REV 1.1		PART NO.: BA41-00866A
MODULE CODE:	LAST EDIT: May 15, 2008 08:19:32 AM	PAGE 11 OF 13	

FSA BSEL0	FSB BSEL1	FSC BSEL2	HOST CLK
0	0	0	266 MHz
0	0	1	333 MHz
0	1	0	200 MHz
0	1	1	400 MHz
1	0	0	133 MHz
1	0	1	100 MHz
1	1	0	166 MHz
1	1	1	RSVD



If SRC8 has option resistor for selectable clock
Option resistor should be placed as close as Clock chip

Place 14.318MHz within 500mils of CK-505

2nd source IDT, 1205-003159

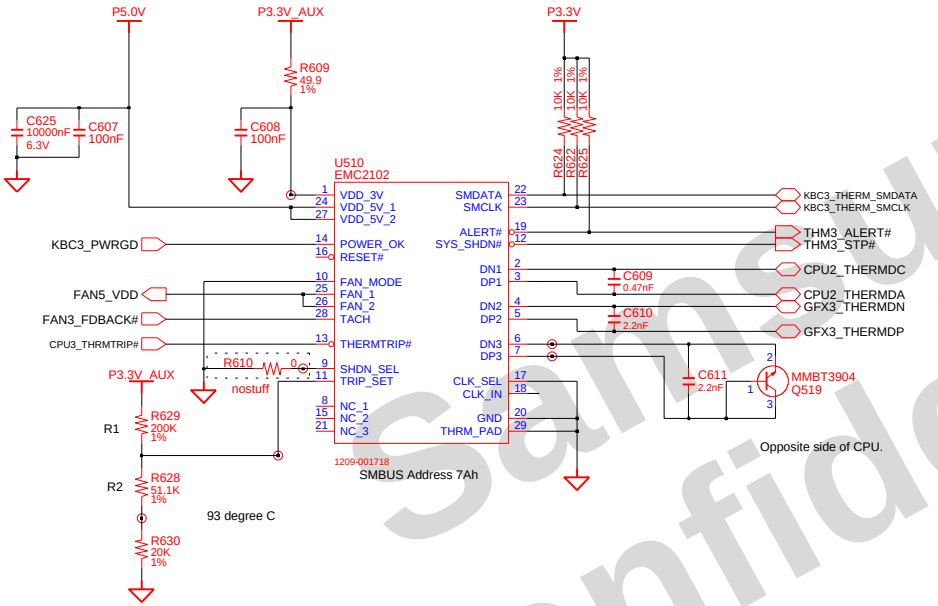
This part is 64pin QFN package.

CLK REQ	DEVICE	SRC PORT
CLK REQ A	SATACLKREQ#	SRC2
CLK REQ B	MCH3_CLKREQ#	SRC4
CLK REQ E	MIN3_CLKREQ#	SRC6
CLK REQ F	EXP3_CLKREQ#	SRC8
CLK REQ G	LOM3_CLKREQ#	SRC9

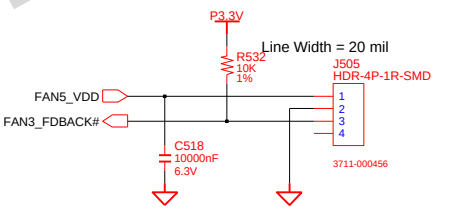
SEL_LCDCLK*	Pin 20/21	Pin 24/25
LOW	DOT_96/DOT_96#	PEG_CLK/PEG_CLK#
HIGH	SRC_0/SRC_0#	27M & 27M_SS

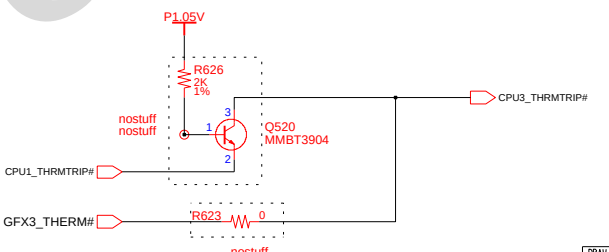
DRAW: MS YANG / Dany Lee	DATE: 8/12/2006	TITLE: OSLO2 Main_Clock_Circuit CK_Clock_505M	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		
APPROVAL: MK KIM	REV: REV 1.1		PART NO.: BA41-00866A
MODULE CODE: undefined	LAST EDIT: May 15, 2008 08:19:32 AM	PAGE 1 OF 1	

THERMAL SENSOR & FAN CONTROL



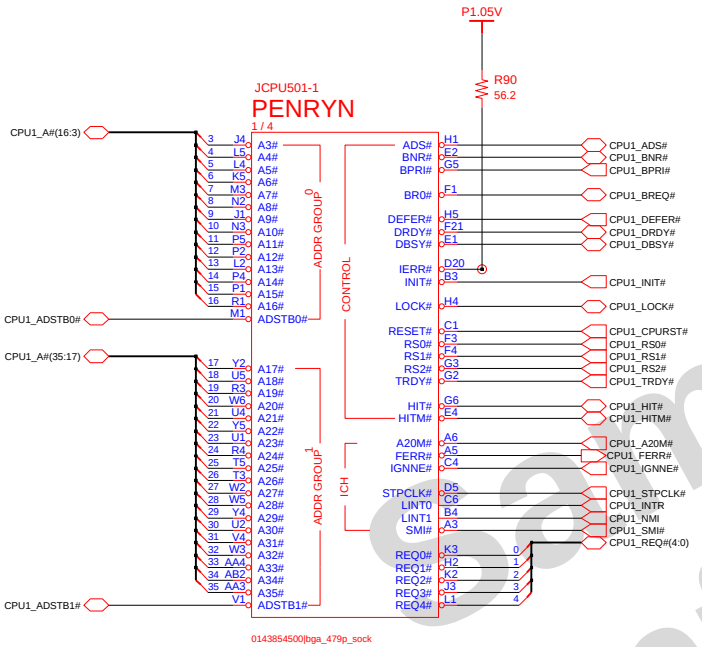
10mil width and 10mil spacing.

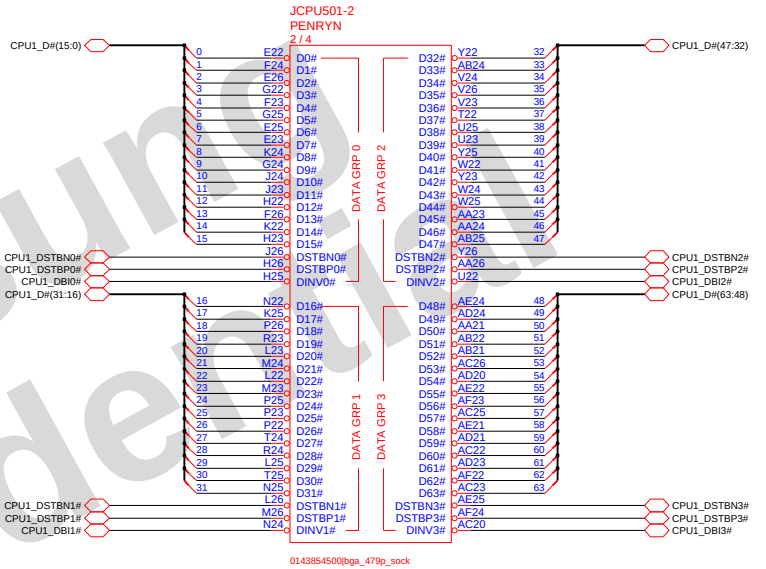


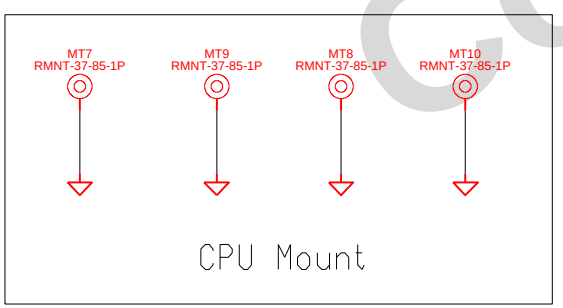


DRAW: MS YANG / Dany Lee	DATE: 8/12/2006	TITLE: OSLO2	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP	Thermal_Sensor_SMSC_Emc2102	
APPROVAL: MK KIM	REV: REV 1.1	Thermal_Sensor_SMSC_Emc2102	PART NO.: BA41-00866A
MODULE CODE:	LAST EDIT: May 15, 2008 08:19:32 AM	PAGE 1 OF 1	

479P CPU socket is 3704-001153

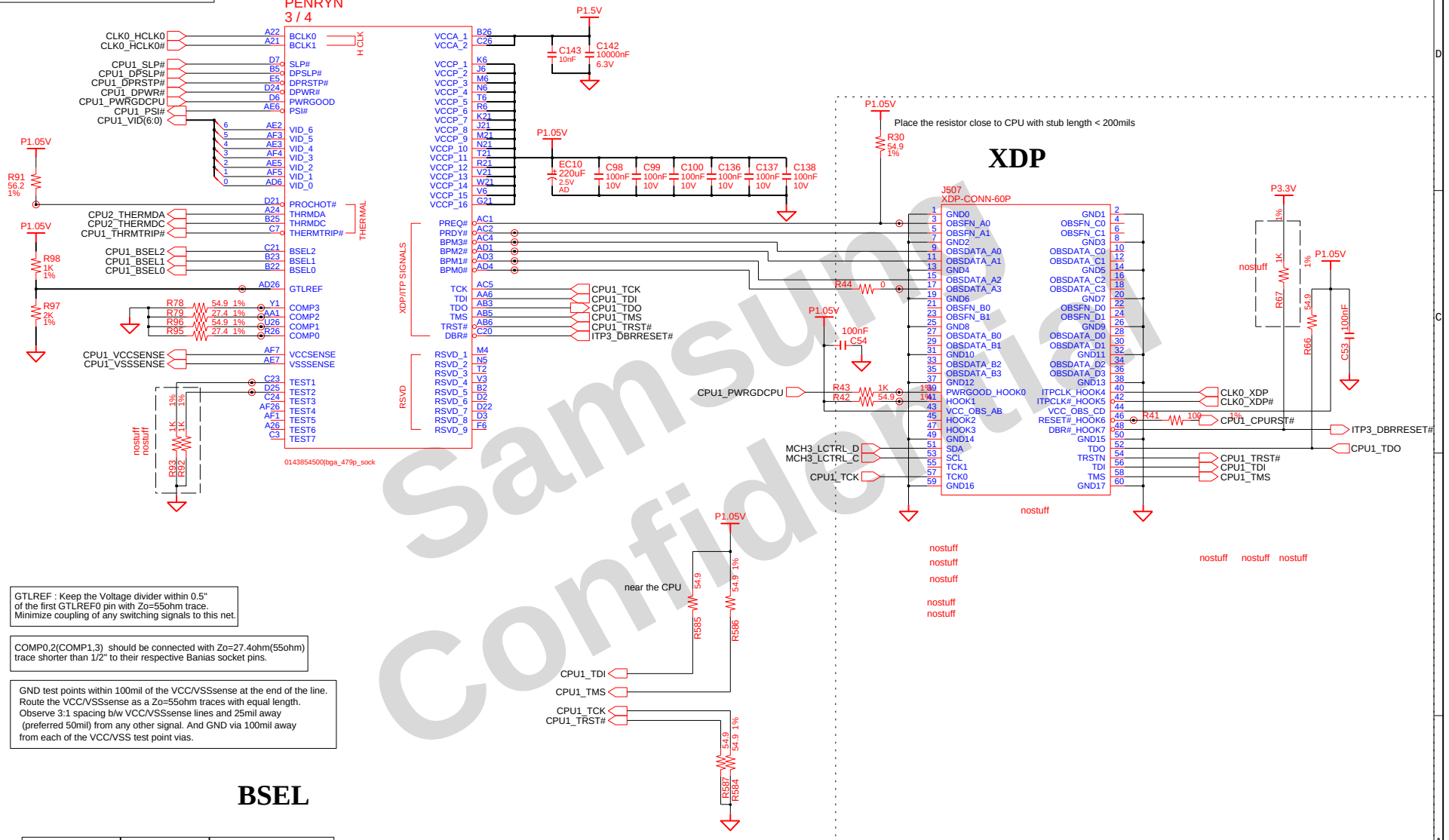






DRAW: MS YANG / Dany Lee	DATE: 11/8/2006	TITLE: OSL02 CPU PENRYN (1/3)	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		
APPROVAL: MK KIM	REV: REV 1.1		PART NO.: BA41-00866A
MODULE CODE: undefined	LAST EDIT: May 15, 2008 08:19:32 AM		PAGE 1 OF 3

JCPU501-3
PENRYN
3 / 4



GTLREF : Keep the Voltage divider within 0.5" of the first GTLREF0 pin with Zo=55ohm trace. Minimize coupling of any switching signals to this net.

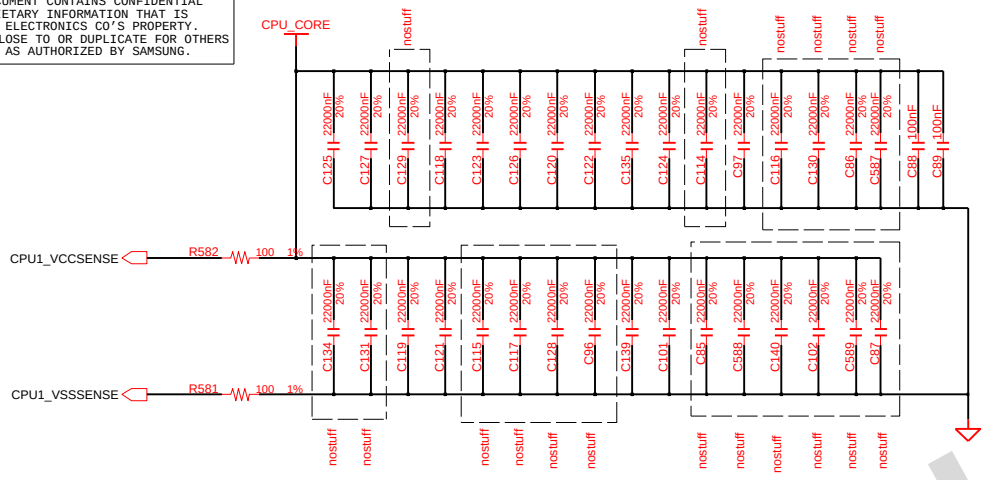
COMP0,2(COMP1,3) should be connected with Zo=27.4ohm(55ohm) trace shorter than 1/2" to their respective Banias socket pins.

GND test points within 100mil of the VCC/VSSsense at the end of the line. Route the VCC/VSSsense as a Zo=55ohm traces with equal length. Observe 3:1 spacing b/w VCC/VSSsense lines and 25mil away (preferred 50mil) from any other signal. And GND via 100mil away from each of the VCC/VSS test point vias.

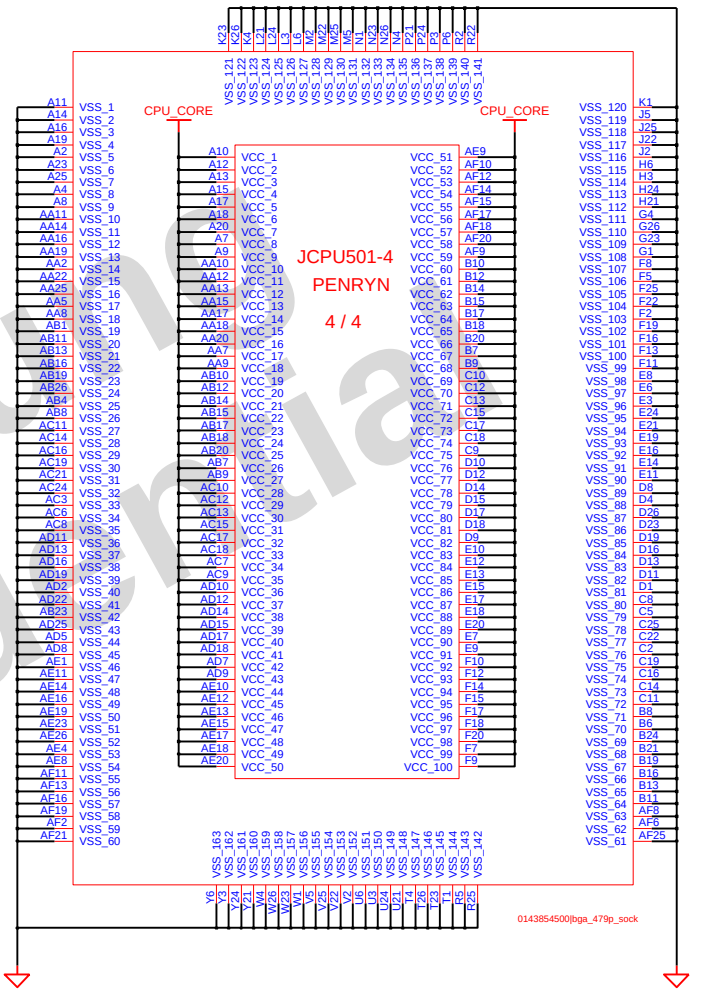
BSEL

	Pull-up	Pull-down
FSB 1067 MHz FSB 800 MHz	BSEL1	BSEL0, BSEL1, BSEL2 BSEL0, BSEL2

DRAW: MS YANG / Dany Lee	DATE: 11/8/2006	TITLE: OSLO2 CPU PENRYN (2/3)	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		
APPROVAL: MK KIM	REV: REV 1.1		PART NO.: BA41-00866A
MODULE CODE: undefined	LAST EDIT: May 15, 2008 08:19:32 AM	PAGE 2 OF 3	



6x 330 uF : CPU VR side



CPU Core Voltage Table IMVP-6

Active Mode VID(6:0)	Voltage	Active/Deeper Sleep Dual Mode Region VID(6:0)	Voltage	Deeper Sleep/Extended Deeper Sleep Dual Mode Region VID(6:0)	Voltage
0 0 0 0 0 0 0	1.5000 V	0 1 0 1 0 0 0	1.0000 V	1 0 1 0 0 0 1	0.4875 V
0 0 0 0 0 0 1	1.4875 V	0 1 0 1 0 0 1	0.9875 V	1 0 1 0 0 1 0	0.4750 V
0 0 0 0 0 1 0	1.4750 V	0 1 0 1 0 1 0	0.9750 V	1 0 1 0 0 1 1	0.4625 V
0 0 0 0 0 1 1	1.4625 V	0 1 0 1 0 1 1	0.9625 V	1 0 1 0 1 0 0	0.4500 V
0 0 0 0 1 0 0	1.4500 V	0 1 0 1 1 0 0	0.9500 V	1 0 1 0 1 0 1	0.4375 V
0 0 0 0 1 0 1	1.4375 V	0 1 0 1 1 0 1	0.9375 V	1 0 1 0 1 1 0	0.4250 V
0 0 0 0 1 1 0	1.4250 V	0 1 0 1 1 1 0	0.9250 V	1 0 1 0 1 1 1	0.4125 V
0 0 0 0 1 **1** **1**	1.4125 V	0 1 0 1 1 **1** **1**	0.9125 V	1 0 1 1 0 **0** 0	0.4000 V
0 0 0 1 0 0 0	1.4000 V	0 1 1 0 0 0 0	0.9000 V	1 0 1 1 0 0 1	0.3875 V
0 0 0 1 0 0 1	1.3875 V	0 1 1 0 0 0 1	0.8875 V	1 0 1 1 0 1 0	0.3750 V
0 0 0 1 0 1 0	1.3750 V	0 1 1 0 0 1 0	0.8750 V	1 0 1 1 0 1 1	0.3625 V
0 0 0 1 0 1 1	1.3625 V	0 1 1 0 0 1 1	0.8625 V	1 0 1 1 1 0 0	0.3500 V
0 0 0 1 1 0 0	1.3500 V	0 1 1 0 1 0 0	0.8500 V	1 0 1 1 1 0 1	0.3375 V
0 0 0 1 1 0 1	1.3375 V	0 1 1 0 1 0 1	0.8375 V	1 0 1 1 1 1 0	0.3250 V
0 0 0 1 1 1 0	1.3250 V	0 1 1 0 1 1 0	0.8250 V	1 0 1 1 1 1 1	0.3125 V
0 0 0 1 1 1 1	1.3125 V	0 1 1 0 1 1 1	0.8125 V	1 1 0 0 0 0 0	0.3000 V
0 0 1 0 0 0 0	1.3000 V	0 1 1 1 0 0 0	0.8000 V	1 1 0 0 0 0 1	0.2875 V
0 0 1 0 0 0 1	1.2875 V	0 1 1 1 0 0 1	0.7875 V	1 1 0 0 0 1 0	0.2750 V
0 0 1 0 0 1 0	1.2750 V	0 1 1 1 0 1 0	0.7750 V	1 1 0 0 0 1 1	0.2625 V
0 0 1 0 0 1 1	1.2625 V	0 1 1 1 0 1 1	0.7625 V	1 1 0 0 1 0 0	0.2500 V
0 0 1 0 1 0 0	1.2500 V	0 1 1 1 1 1 0	0.7500 V	1 1 0 0 1 0 1	0.2375 V
0 0 1 0 1 0 1	1.2375 V	0 1 1 1 1 1 1	0.7375 V	1 1 0 0 1 1 0	0.2250 V
0 0 1 0 1 1 0	1.2250 V	0 1 **1** 1 1 1 0	0.7250 V	1 1 0 0 1 1 1	0.2125 V
0 0 **1** 0 1 **1** **1**	1.2125 V	0 1 **1** 1 1 **1** **1**	0.7125 V	1 1 **0** 1 0 0 **0**	0.2000 V
0 0 1 1 0 0 0	1.2000 V	1 0 0 0 0 0 0	0.7000 V	1 1 0 1 0 0 1	0.1875 V
0 0 1 1 0 0 1	1.1875 V	1 0 0 0 0 0 1	0.6875 V	1 1 0 1 0 1 0	0.1750 V
0 0 1 1 0 1 0	1.1750 V	1 0 0 0 0 0 1 0	0.6750 V	1 1 0 1 0 1 1	0.1625 V
0 0 1 1 0 1 1	1.1625 V	1 0 0 0 0 1 1	0.6625 V	1 1 0 1 1 0 0	0.1500 V
0 0 1 1 1 0 0	1.1500 V	1 0 0 0 0 1 1 0	0.6500 V	1 1 0 1 1 0 1	0.1375 V
0 0 1 1 1 0 1	1.1375 V	1 0 0 0 0 1 0 1	0.6375 V	1 1 0 1 1 1 0	0.1250 V
0 0 1 1 1 1 0	1.1250 V	1 0 0 0 0 1 1 0	0.6250 V	1 1 0 1 1 1 1	0.1125 V
0 0 1 1 1 1 1	1.1125 V	1 0 0 0 0 1 1 1	0.6125 V	1 1 1 0 0 0 0	0.1000 V
0 1 0 0 0 0 0	1.1000 V	1 0 0 0 1 0 0 0	0.6000 V	1 1 1 0 0 0 1	0.0875 V
0 1 0 0 0 0 1	1.0875 V	1 0 0 0 1 0 0 1	0.5875 V	1 1 1 0 0 1 0	0.0750 V
0 1 0 0 0 1 0	1.0750 V	1 0 0 0 1 0 1 0	0.5750 V	1 1 1 0 0 1 1	0.0625 V
0 1 0 0 0 1 1	1.0625 V	1 0 0 0 1 0 1 1	0.5625 V	1 1 1 0 1 0 0	0.0500 V
0 1 0 0 1 0 0	1.0500 V	1 0 0 0 1 1 0 0	0.5500 V	1 1 1 0 1 0 1	0.0375 V
0 1 0 0 1 0 1	1.0375 V	1 0 0 0 1 1 0 1	0.5375 V	1 1 1 0 1 1 0	0.0250 V
0 1 0 0 1 1 0	1.0250 V	1 0 0 0 1 1 1 0	0.5250 V	1 1 1 0 1 1 1	0.0125 V
0 **1** 0 0 **1** **1** 1	1.0125 V	1 **0** 0 0 1 **1** **1** 1	0.5125 V	1 **1** 1 1 0 **0** 0	0.0000 V
		1 **0** 1 0 **0** **0** 0	0.5000 V	1 1 1 1 0 0 1	0.0000 V
				1 1 1 1 0 1 0	0.0000 V
				1 1 1 1 0 1 1	0.0000 V
				1 1 1 1 1 0 0	0.0000 V
				1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0	0.0000 V
				1 1 1 1 1 1 1	0.0000 V

Active

DPRSLPVR	0
DPRSTP*	1
PSI2*	0 or 1

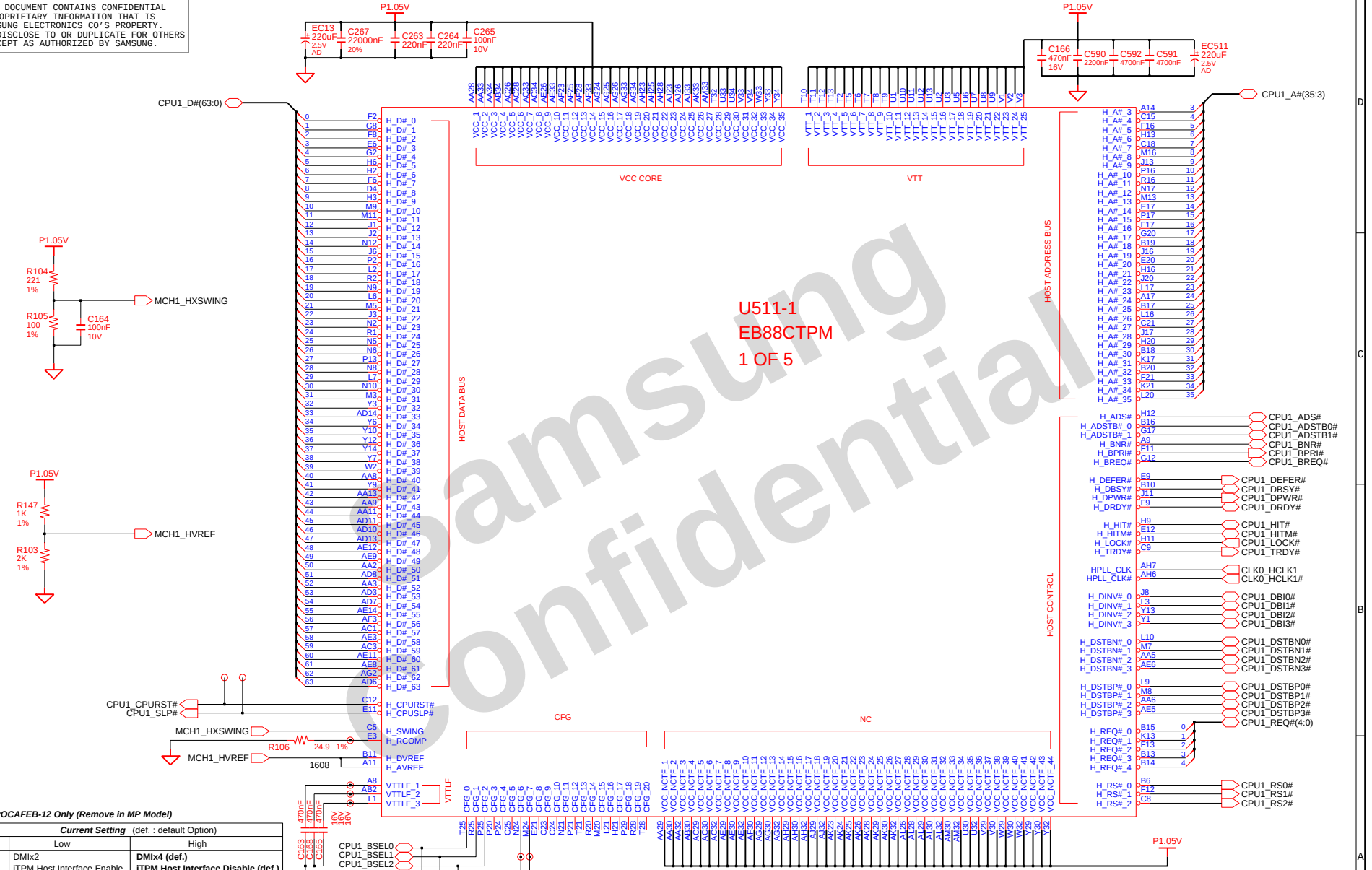
Deeper Slp

DPRSLPVR	1
DPRSTP*	0
PSI2*	0 or 1

*"1111111" : 0V power good asserted.

*Yonah Processor (2.33 GHz / 800 MHz : TBD)

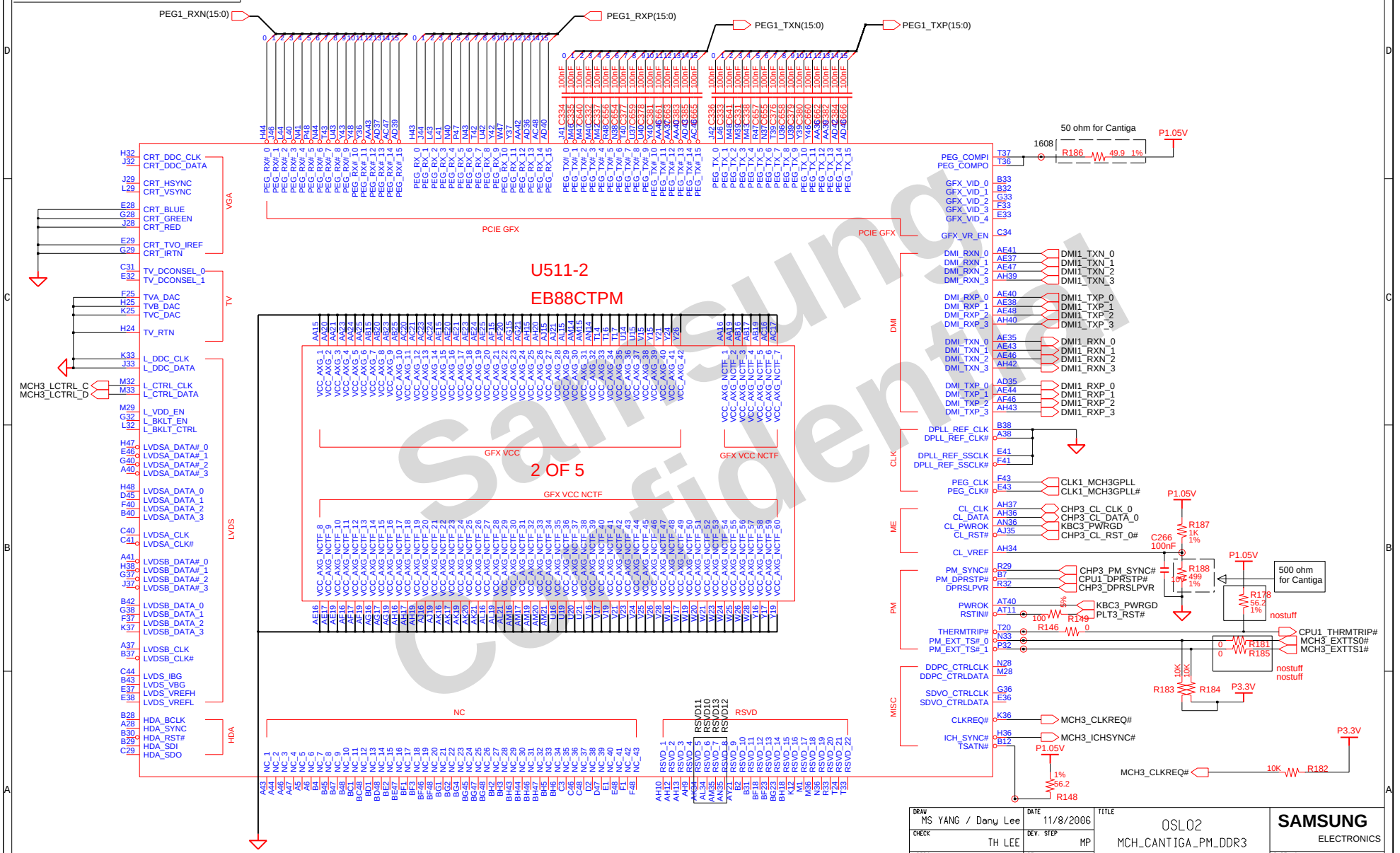
DRAW: MS YANG / Dany Lee	DATE: 11/8/2006	TITLE: OSLO2 CPU PENRYN (3/3)	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		
APPROVAL: MK KIM	REV: REV 1.1		PART NO.: BA41-00866A
MODULE CODE: undefined	LAST EDIT: May 15, 2008 08:19:32 AM		PAGE 3 OF 3



***POCAFEB-12 Only (Remove in MP Model)**

	Current Setting (def. : default Option)	
CFG#	Low	High
CFG(5)	DMIx2	**DMIx4 (def.)**
CFG(6)	iTPM Host Interface Enable	**iTPM Host Interface Disable (def.)**
CFG(7)	ME Crypto no confidentiality	**ME Crypto confidentiality (def.)**
CFG(9)	PEG Reversal (def.)	**Normal**
CFG(10)	PCIE Loop Back Enable	**PCIE Loop Back Disable(def)**
CFG(16)	Dynamic ODT Disabled	**Dynamic ODT Enabled (def.)**
CFG(19)	**DMI Lane Normal (def.)**	DMI Lane Reversal
CFG(20)	**SDVO or PCIE X1 Only(def.)**	SDVO and PCIE X1 Simultaneously

DRAW: MS YANG / Dany Lee	DATE: 11/8/2006	TITLE: OSL02 MCH_CANTIGA_PM_DDR3 CANTIGA (1/5)	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		PART NO.: BA41-00866A
APPROVAL: MK KIM	REV: REV 1.1		
MODULE CODE: undefined	LAST EDIT: May 15, 2008 08:19:32 AM	PAGE 1 OF 5	



DRAW: MS YANG / Dany Lee	DATE: 11/8/2006	TITLE: OSL02 MCH_CANTIGA_PM_DDR3 CANTIGA (2/5)	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		
APPROVAL: MK KIM	REV: REV 1.1		PART NO.: BA41-00866A
MODULE CODE: undefined	LAST EDIT: May 15, 2008 08:19:32 AM	PAGE 2 OF 5	

PLACE EACH CAP NEAR AV42 PIN

MEM1_ADQ(63:0)

MEM1_ABS(2:0)

MEM1_ADM(7:0)

MEM1_ADQS#(7:0)

MEM1_ADQS(7:0)

MEM1_AMA(14:0)

MEM1_ACAS#
MEM1_ARAS#
MEM1_AWE#

MEM1_CS0#
MEM1_CS1#

MEM1_ODT0
MEM1_ODT1

MEM1_CKE0
MEM1_CKE1

CLK1_MCLK0
CLK1_MCLK0#
CLK1_MCLK1
CLK1_MCLK1#

SYSTEM MEMORY A

U511-3
EB88CTPM
3 OF 5

SYSTEM MEMORY B

SM_RCOMP
SM_RCOMP#

SM_RCOMP_V_OH
SM_RCOMP_V_OL

MEM1_VREF

R613 499 1%

SM_REXT
SM_VREF

SM_DRAMRST#
SM_PWROK

SHT5 0
SHT7 0

MCH3_DDR_RST#
VRM3_DDR_PWRGD

SB_CAS#
SB_RAS#
SB_WE#

MEM1_BCAS#
MEM1_BRAS#
MEM1_BWE#

SB_CS#_0
SB_CS#_1

MEM1_CS2#
MEM1_CS3#

SB_ODT_0
SB_ODT_1

MEM1_ODT2
MEM1_ODT3

SB_CKE_0
SB_CKE_1

MEM1_CKE2
MEM1_CKE3

SB_CK_0
SB_CK#_0
SB_CK_1
SB_CK#_1

CLK1_MCLK2
CLK1_MCLK2#
CLK1_MCLK3
CLK1_MCLK3#

MEM1_BDM(7:0)

MEM1_BDQS#(7:0)

MEM1_BDQS(7:0)

MEM1_BMA(14:0)

MEM1_BBS(2:0)

MEM1_BDQ(63:0)

C343 100nF 10V
C344 100nF 10V
nostuff
nostuff

P1.5V_AUX

R611 80.6 1%
R612 80.6 1%

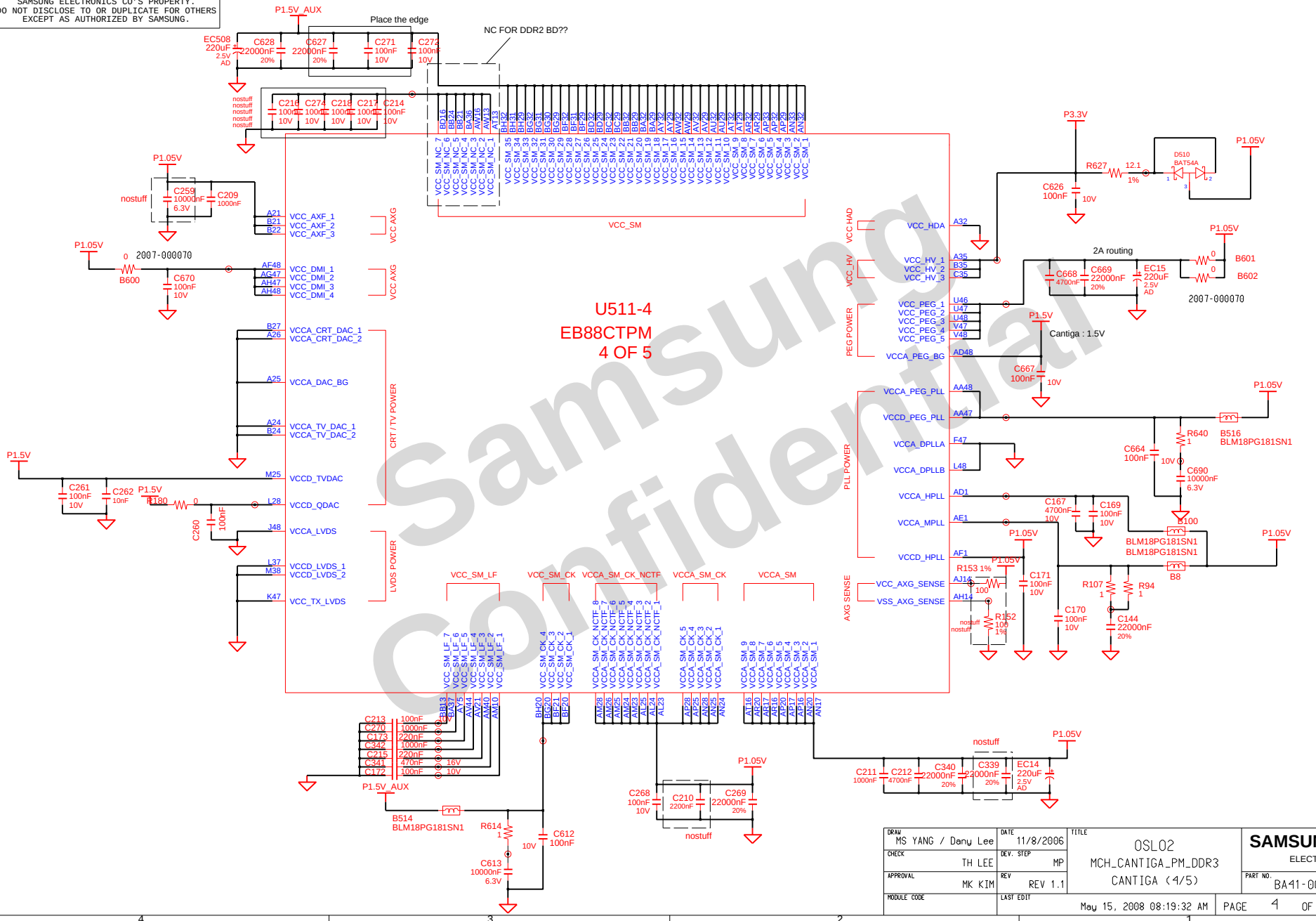
R632 1K 1%
R189 3.01K 1%
R190 1K 1%

C273 10nF
C275 2200nF
C277 10nF
C276 2200nF

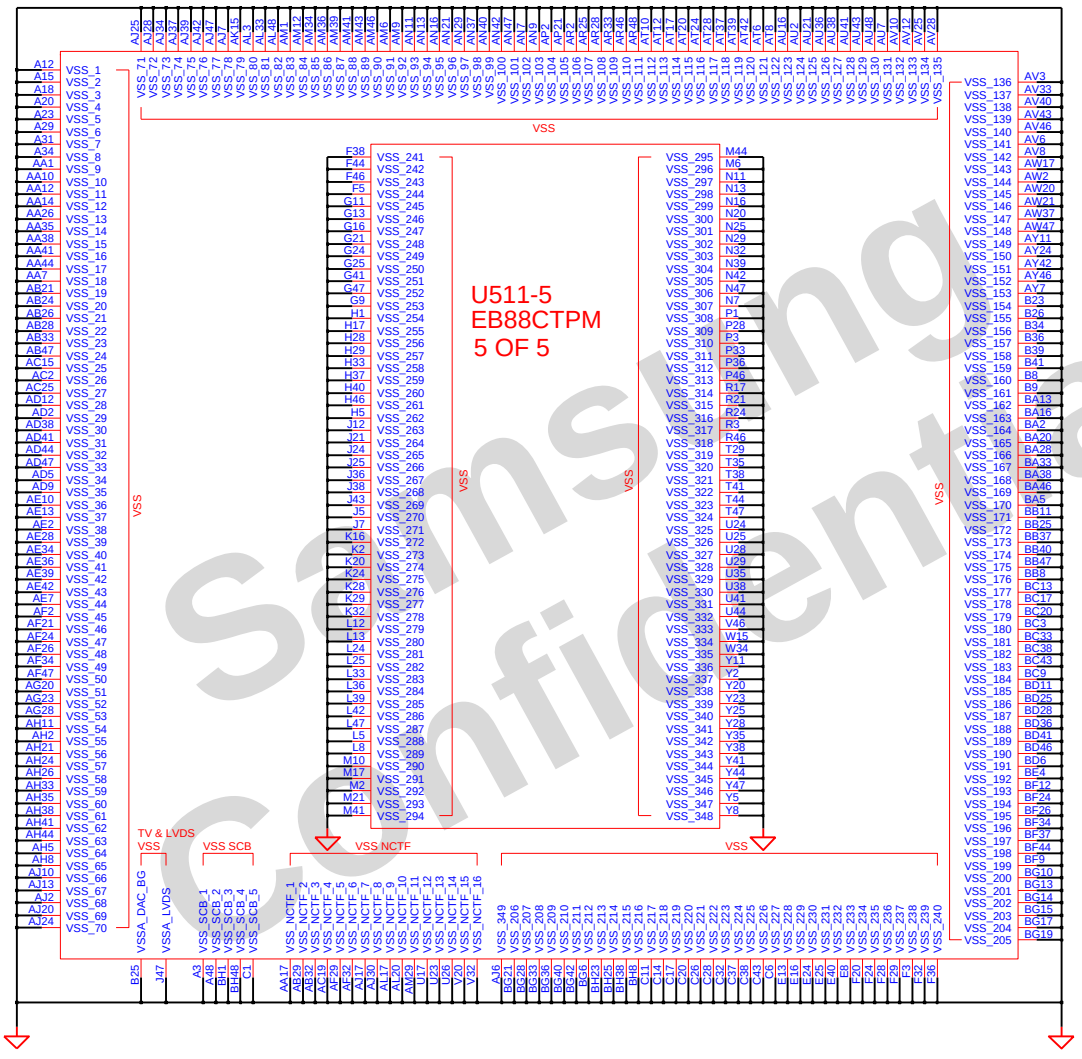
Route as short as possible

Cantiga	SM_RCOMP : 80 ohm to P1.5V_AUX SM_RCOMP# : 80 ohm to VSS

DRAW: MS YANG / Dany Lee	DATE: 11/8/2006	TITLE: OSLO2 MCH_CANTIGA_PM_DDR3 CANTIGA (3/5)	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		PART NO.: BA41-00866A
APPROVAL: MK KIM	REV: REV 1.1		
MODULE CODE:	LAST EDIT: May 15, 2008 08:19:32 AM	PAGE 3 OF 5	



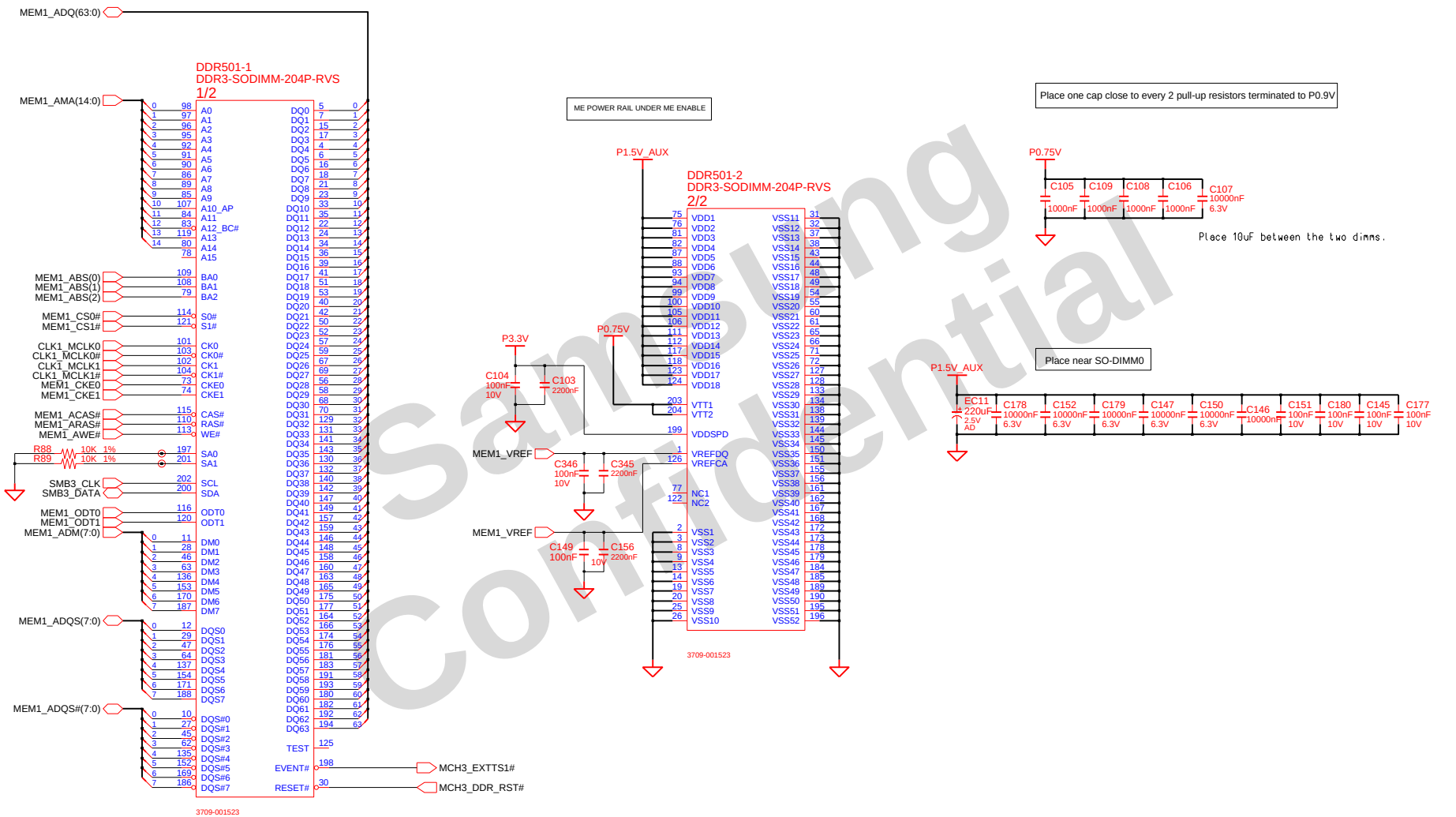
DRAW: MS YANG / Dany Lee	DATE: 11/8/2006	TITLE: OSLO2 MCH_CANTIGA_PM_DDR3 CANTIGA (4/5)	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		
APPROVAL: MK KIM	REV: REV 1.1		PART NO.: BA41-00866A
MODULE CODE:	LAST EDIT: May 15, 2008 08:19:32 AM		PAGE 4 OF 5



DRAW: MS YANG / Dany Lee	DATE: 11/8/2006	TITLE: OSLO2 MCH_CANTIGA_PM_DDR3 CANTIGA (5/5)	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		
APPROVAL: MK KIM	REV: REV 1.1		PART NO.: BA41-00866A
MODULE CODE:	LAST EDIT: May 15, 2008 08:19:32 AM		PAGE 5 OF 5

DDR SO-DIMM #0

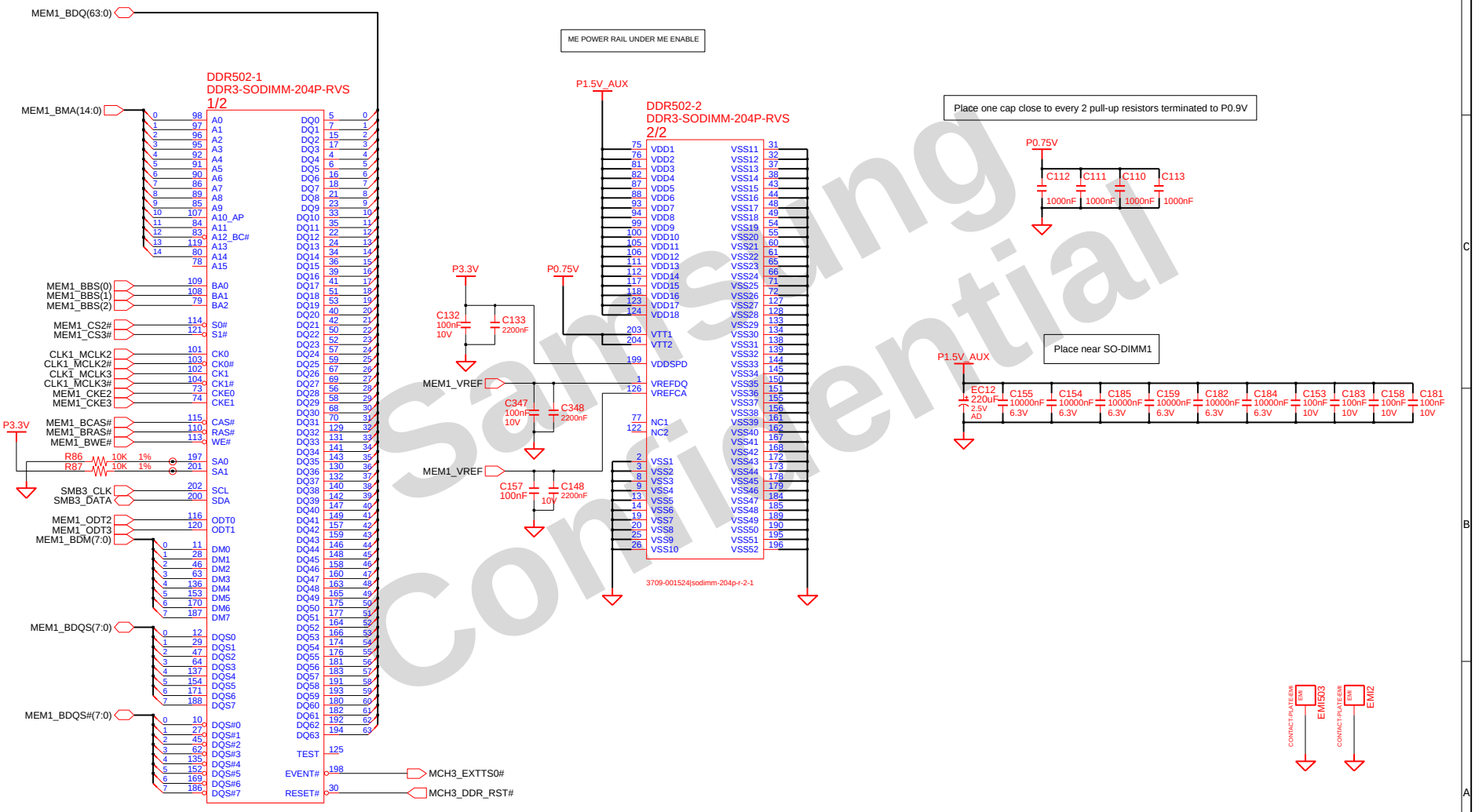
Height : 5.2mm (Reverse)



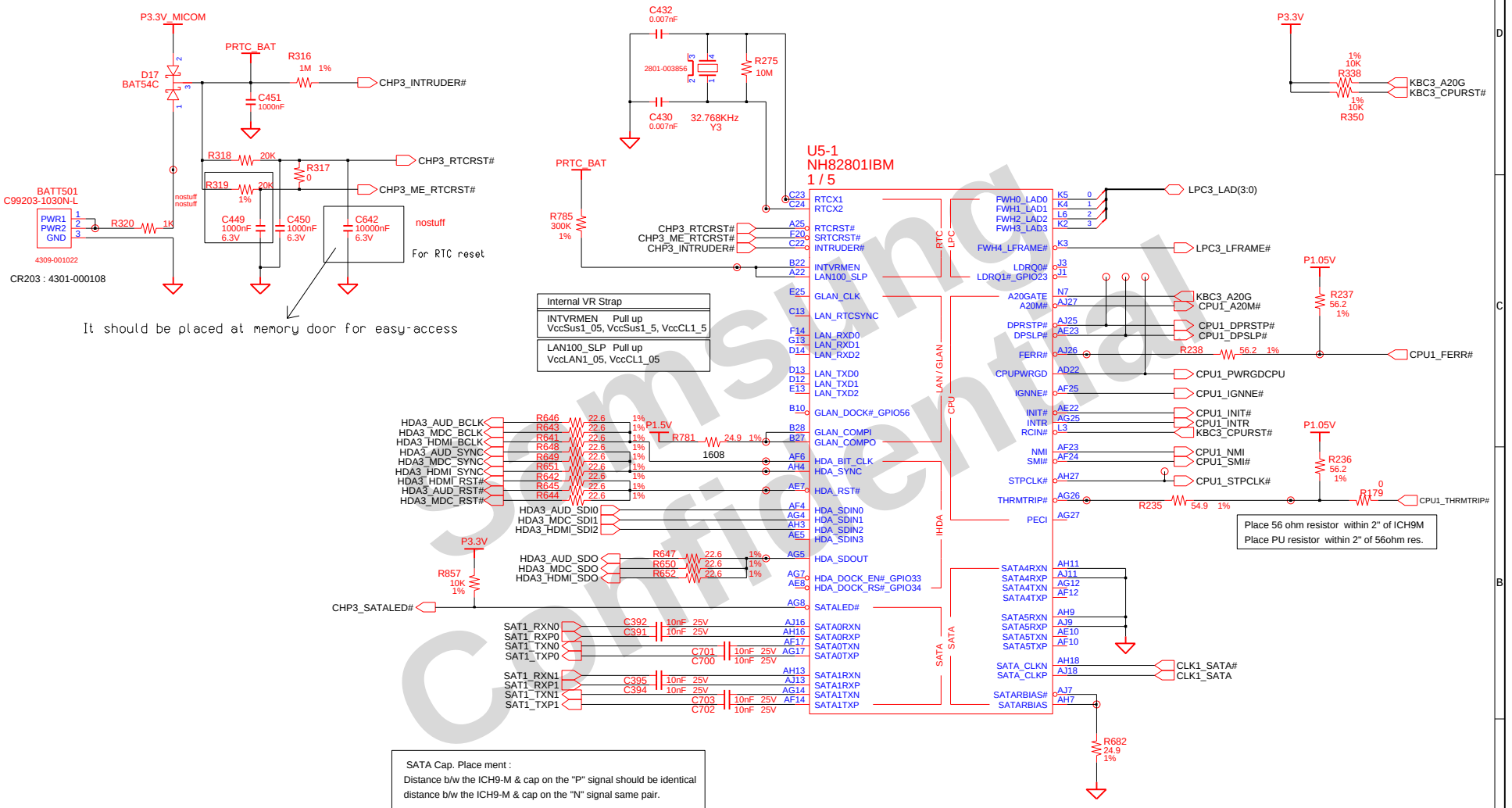
DRAW: MS YANG / Dany Lee	DATE: 11/8/2006	TITLE: OSLO2 SODIMM_REV DDR3 CH A	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		
APPROVAL: MK KIM	REV: REV 1.1		PART NO.: BA41-00866A
MODULE CODE:	LAST EDIT: May 15, 2008 08:19:32 AM	PAGE 1 OF 2	

DDR SO-DIMM #1

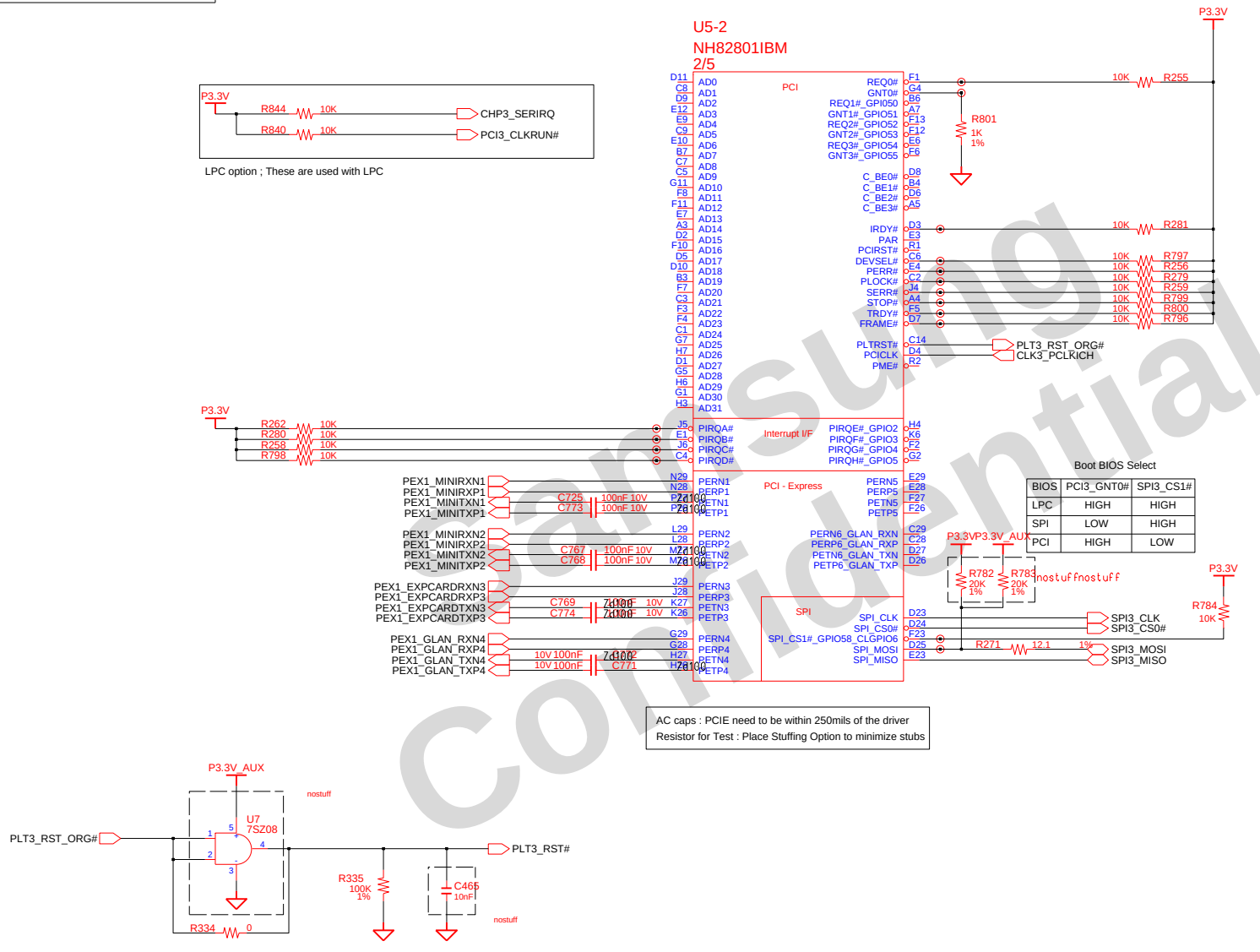
Height : 9.2mm (Reverse)



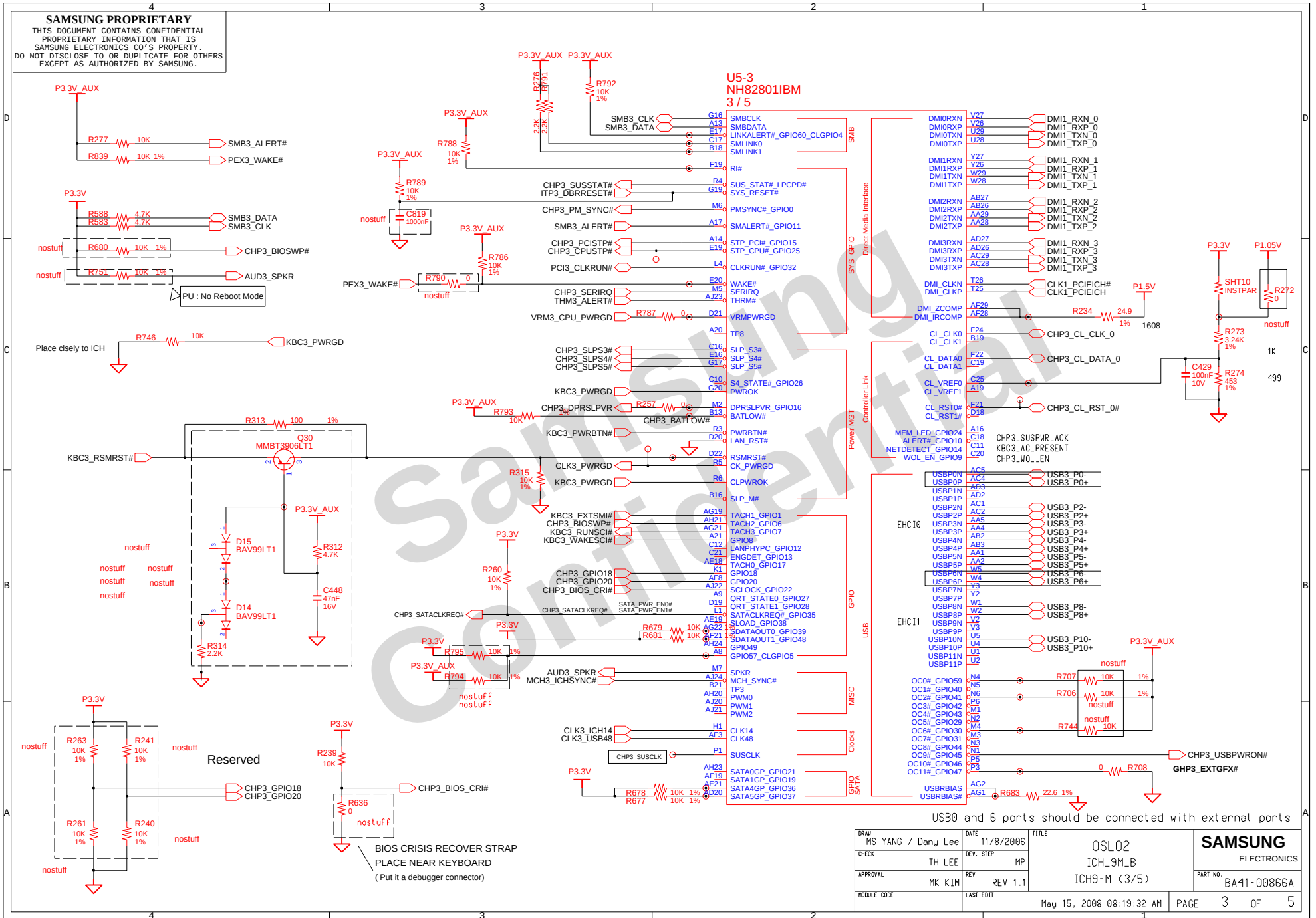
DRAW: MS YANG / Dany Lee	DATE: 11/8/2006	TITLE: OSLO2 SODIMM_REV DDR3 CH B	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		
APPROVAL: MK KIM	REV: REV 1.1		PART NO.: BA41-00866A
MODULE CODE:	LAST EDIT: May 15, 2008 08:19:32 AM	PAGE 2 OF 2	



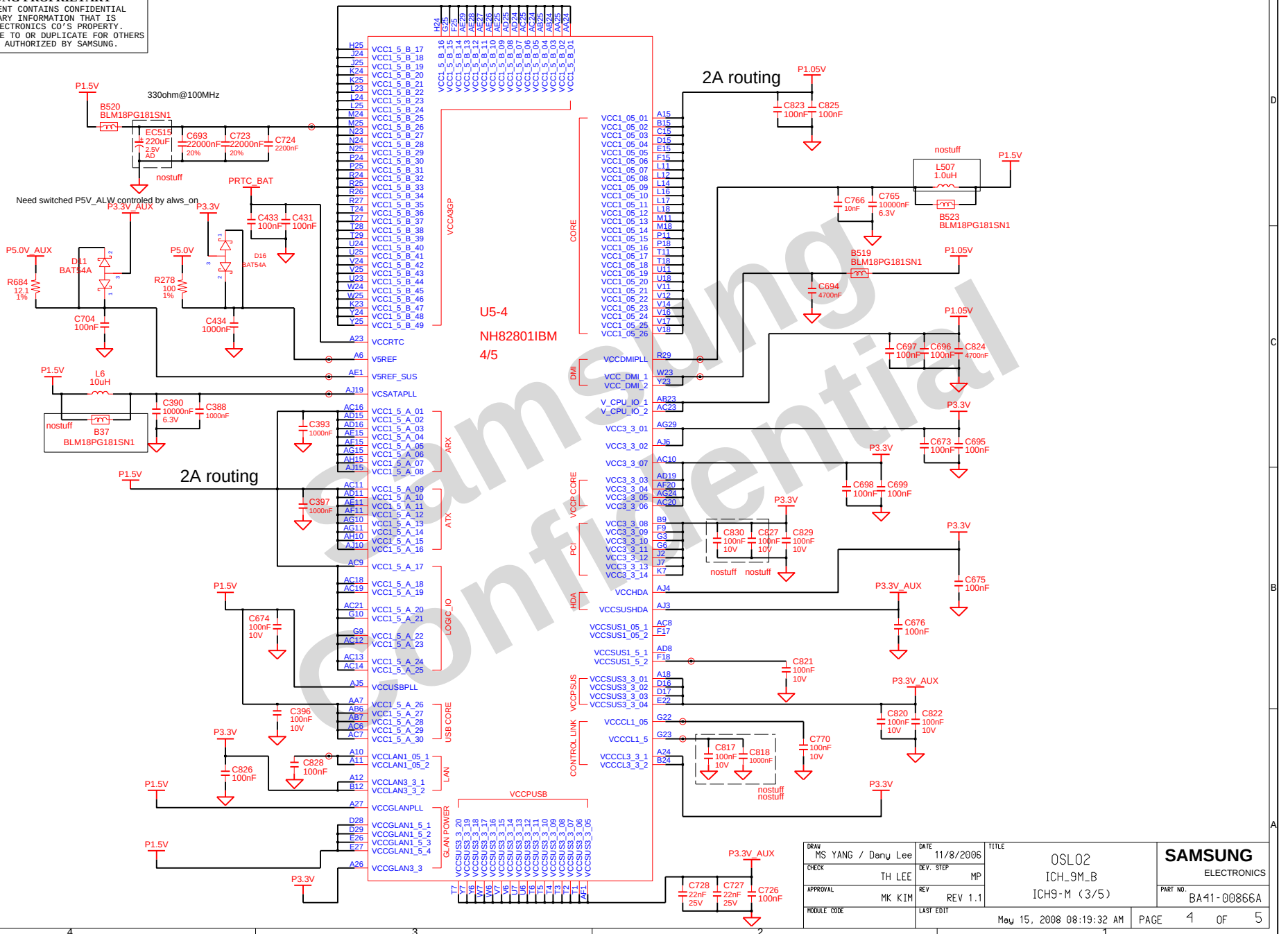
DRAW: MS YANG / Dany Lee	DATE: 11/8/2006	TITLE: OSLO2 ICH_9M_B ICH9-M (1/5)	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		
APPROVAL: MK KIM	REV: REV 1.1		PART NO.: BA41-00866A
MODULE CODE:	LAST EDIT: May 15, 2008 08:19:32 AM	PAGE 1 OF 5	



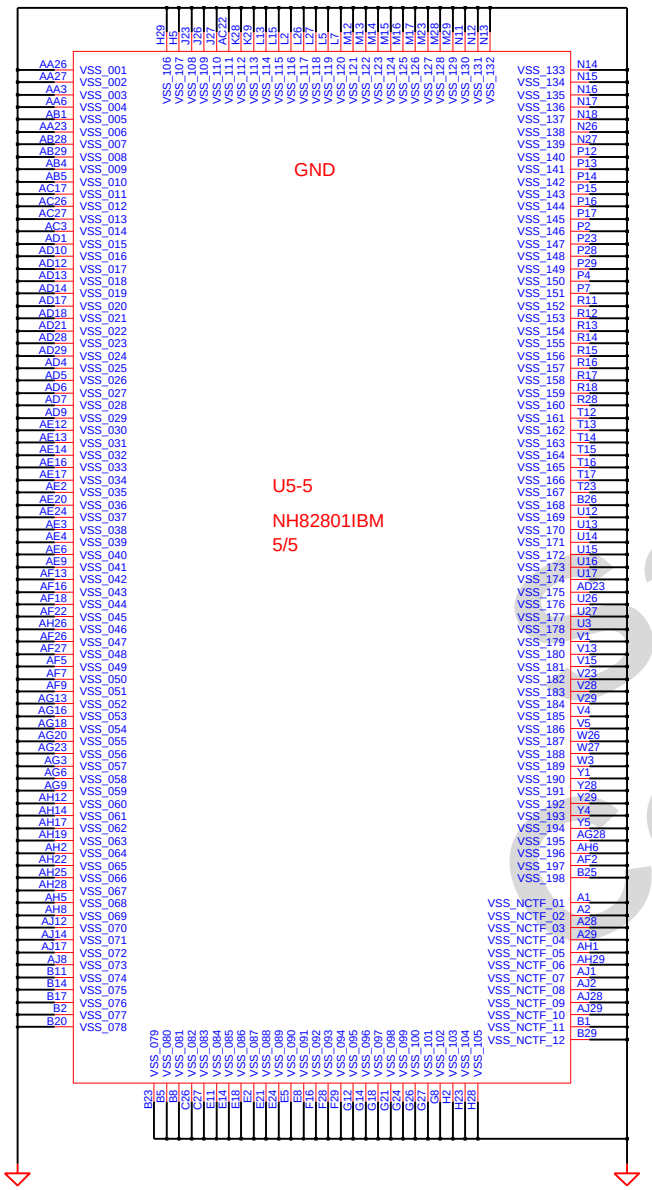
DRAW: MS YANG / Dany Lee	DATE: 11/8/2006	TITLE: OSLO2 ICH_9M_B ICH9-M (2/5)	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		
APPROVAL: MK KIM	REV: REV 1.1		PART NO.: BA41-00866A
MODULE CODE: undefined	LAST EDIT: May 15, 2008 08:19:32 AM	PAGE 2 OF 5	



DRAW: MS YANG / Dany Lee	DATE: 11/8/2006	TITLE: OSLO2 ICH_9M_B ICH9-M (3/5)	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		PART NO.: BA41-00866A
APPROVAL: MK KIM	REV: REV 1.1		
MODULE CODE:	LAST EDIT: May 15, 2008 08:19:32 AM	PAGE 3 OF 5	



DRAW: MS YANG / Dany Lee	DATE: 11/8/2006	TITLE: OSLO2 ICH_9M_B ICH9-M (3/5)	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		PART NO.: BA41-00866A
APPROVAL: MK KIM	REV: REV 1.1		
MODULE CODE:	LAST EDIT: May 15, 2008 08:19:32 AM	PAGE 4 OF 5	



DRAW: MS YANG / Dany Lee	DATE: 11/8/2006	TITLE: OSLO2 ICH_9M_B ICH9-M (5/5)	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		
APPROVAL: MK KIM	REV: REV 1.1		PART NO.: BA41-00866A
MODULE CODE:	LAST EDIT: May 15, 2008 08:19:32 AM	PAGE 5 OF 5	

- SPI ROM LIST (8M)-

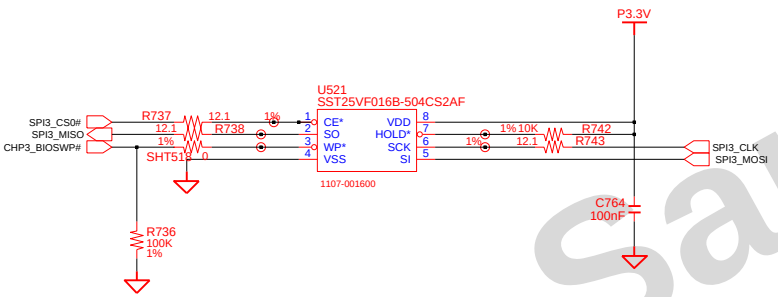
Macronix - MX25L8005M2C-15G
-> 1107-001646

STM - M25PE80
-> 1107-001674

- SPI ROM LIST (16M)-

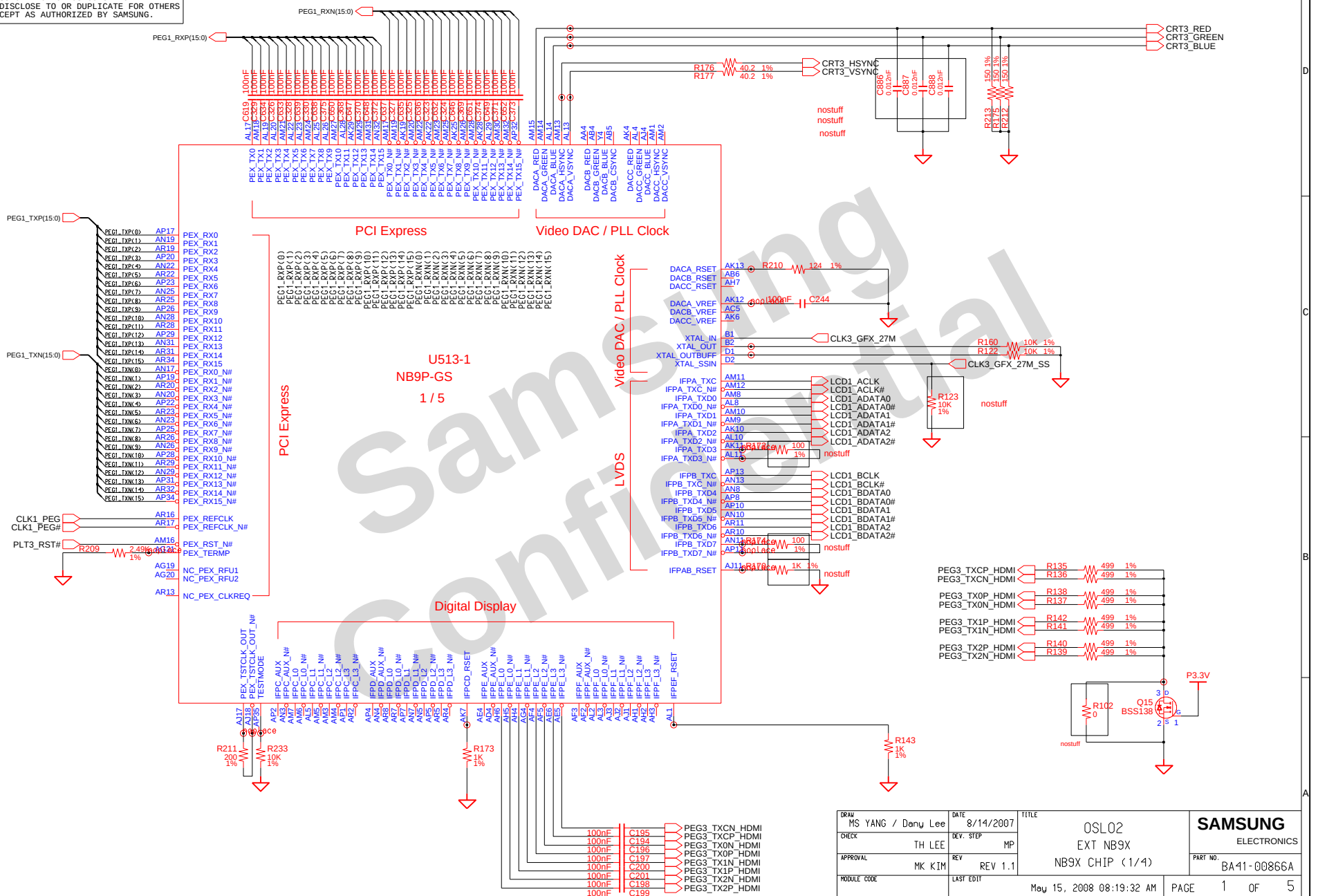
Macronix - MX25L1605A
-> 1107-001600

SST - SST25VF016B
-> 1107-001600



02 VERIFY REAL MODE	66 CONFIGURE ADVANCE CACHE REG.
03 DISABLE NMI	6A DISPLAY EXTERNAL CACHE SIZE
04 GET CPU TYPE	6C DISPLAY SHADOW MESSAGE
06 INIT. SYSTEM H/W	6E DISPLAY NON-DISPOSABLE SEGMENT
08 INIT. CHIPSET REG.	70 DISPLAY ERROR MESSAGE
09 SET IN POST FLAG	72 CHECK FOR CONFIGURATION ERROR
0A INIT CPU.REG	74 TEST REAL-TIME CLOCK
0B CPU CACHE ON	76 CHECK FOR KEYBOARD EERROR
0C INIT.CACHE TO POST	7C SETUP HARDWARE INTERRUPT VECTOR
OE INIT. I/O VALUE	7E TEST COPROCESSER IF PRESENT
0F ENABLE THE L-BUS IDE	80 DISABLE ON-BOARD I/O PORT
10 INIT. POWER MANAGER	82 DETECT AND INSTALL EXT.RS232C
11 LOAD ALTERNATE REG.	84 DETECT AND INSTALL EXT.PARALLEL
13 PCI BUS MASTER RESET WITH INITIAL POST VALUE	86 RE-INIT. ON-BOARD I/O PORT
	88 INIT. BIOS DATA ROM
14 INIT. KEYBOARD CONTROLLER	8A INIT.EXTENDED BIOS DATA AREA
16 CHECK CHECKSUM	8C INIT. FDD CONTROLLER
18 8254 TIMER INIT.	9A SHADOW OPTION ROMS
1A 8237 DMA CONTROLLER INIT.	9C SETUP POWER MANAGEMENT
1C RESET INTERRUP CONTROLLER	9E ENABLE H/W INTERRUPT
20 TEST DRAM REFRESH	A0 SET TIME OF DAY
22 TEST 8742 KEYBOARD CONTROLLER	A4 INIT. TYPEMATIC RATE
24 SET ES SEGMENT REG. TO 4GB	A8 ERASE F2 PROMPT
26 ENABLE A20	AA SCAN FOR F2 KEY STROKE
28 AUTO SIZING DRAM	AC ENTER SETUP
32 COMPUTE THE CPU SPEED	AE CLEAR IN POST FLAG
34 TESET CMOS RAM	B0 CHECK FOR ERRORS
38 SHADOW SYSTEM BIOS ROM	B2 POST DONE-PREPARE TO BOOT O/S
3A AUTO SIZING CACHE	B4 ONE BEEP
3C CONFIGURE ADVANCED CHIPSET REG.	B6 CHECK PASSWORD (OPTION)
3D LOAD ALTER REG. WITH CMOS VALUE	B7 ACPI INIT
42 INIT. INTERRUPT VECTOR	BA DMI INIT
44 INIT. BIOS INTERRUPT	BE CLEAR SCREEN
46 CHECK ROM COPYRIGHT NOTICE	C0 TRY BOOT WITH INT19
47 INIT. I20 SUPPORT IF INSTALLED	D0 INTERRUPT HANDLER ERROR
48 CHECK VIDEO CONFIGURE AGAINST CMOS	D2 UNKNOWN INTERRUPT ERROR
49 INIT. PCI BUS AND DEVICE	D4 PENDING INTERRUPT ERROR
4A INIT. ALL VIDEO BIOS ROM	D6 SHUTDOWN 5
4C SHADOW VIDEO BIOS ROM	D8 SHUTDOWN ERROR
50 DISPLAY CPU TYPE AND SPEED	DA EXTENDED BLOCK MOVE
52 TEST KEYBOARD	DC SHUTDOWN 10
54 SET KEYCLICK IF ENABLED	89 ENABLE NMI
56 ENABLE KEYBOARD	90 INIT. HDD CONTROLLER
58 TEST FOR UNEXPECTED INTERRUPTS	91 INIT. LOCAL BUS HDD CONTROLLER
5A DISPLAY " PRESS ..... SETUP"	92 JUMP TO USER PATCH 2
5C TEST RAM GETWEEN 512K AND 640K	94 DISABLE A20 ADDRESS LINE
60 TEST EXTENDED MEMORY	96 CLEAR HUGE ES SEGMENT REG.
62 TEST EXTENDED MEMORY ADDRESS LINE	98 SEARCH FOR OPTION ROMS
64 JUMP TO USER PATCH 1	

DRAW: MS YANG / Dany Lee	DATE: 8/12/2006	TITLE: OSLO2 SPI_BIOS_ROM SPI_BIOS_ROM	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		
APPROVAL: MK KIM	REV: REV 1.1		PART NO.: BA41-00866A
MODULE CODE:	LAST EDIT: May 15, 2008 08:19:32 AM	PAGE 1 OF 1	



DRAW: MS YANG / Dany Lee	DATE: 8/14/2007	TITLE: OSLO2 EXT NB9X NB9X CHIP (1/4)	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		PART NO.: BA41-00866A
APPROVAL: MK KIM	REV: REV 1.1		
MODULE CODE:	LAST EDIT: May 15, 2008 08:19:32 AM		PAGE 1 OF 5

Pin	Description	Activate
GPIO(0)	DVI detect	High
GPIO(1)	TV detect	Low
GPIO(2)	PWM Brigtness control	High
GPIO(3)	LCD VDD on enable	High
GPIO(4)	Backlight on/off	High
GPIO(5)	GPU VID0	00 = 0.89V, 01 = 1.0V
GPIO(6)	GPU VID1	10 = 1.05V, 11 = Reserved
GPIO(7)	GPU VID2 or Mem VID	NC
GPIO(8)	Thermal diode Alert	LOW
GPIO(9)	Fan control	NC
GPIO(10)	Memory VREF switch	NC
GPIO(11)	SLI Rater sync	HIGH
GPIO(12)	AC Power dection input	NC
GPIO(13)	Power supply control	NC
GPIO(14)	Power supply control	NC
GPIO(15)	HDMI Detect	High
GPIO(16)	DP Detect	High

Strap option	Bit 3	Bit 2	Bit 1	Bit 0
ROM_SO	XCLK_27	TVMODE[2]	TVMODE[1]	TVMODE[0]
ROM_SCLK	DEVID[4]	VENID	CLK_CFG	PLL_TERM
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	DEVID[3]	DEVID[2]	DEVID[1]	DEVID[0]
STRAP1	PADCFG[3]	PADCFG[2]	PADCFG[1]	PADCFG[0]
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]
Resistor value	PU to VDD	PD to GND	XCLK27 = 1 27MHz	
5K ohm	1000	0000	RAM CFG (SEC)	
10 Kohm	1001	0001	0011 512Mbit 0111 1Gbit	
15K ohm	1010	0010	USER[3:0]=1111 for EDID	
20K ohm	1011	0011	PADCFG[3:0]=0001 of NP	
25K ohm	1100	0100	NB9M-GS:0x06E9 (01001)	
30K ohm	1101	0101	NB9M-GE:0x06E8 (01000)	
35K ohm	1110	0110	NB9P-GE:0x0406 (00110)	
45K ohm	1111	0111	NB9P-GS:0x0649 (01001)	
			NB9P-GE2:0x0648 (01000)	

U513-2

NB9P-GS

2 / 5

NB9P-GE2 : 5K PU
NB9P-GS : 10K PU

GDDR3 512MB (1Gb*4) : 45K PD
GDDR3 256MB (512Mb*4) : 20K PD

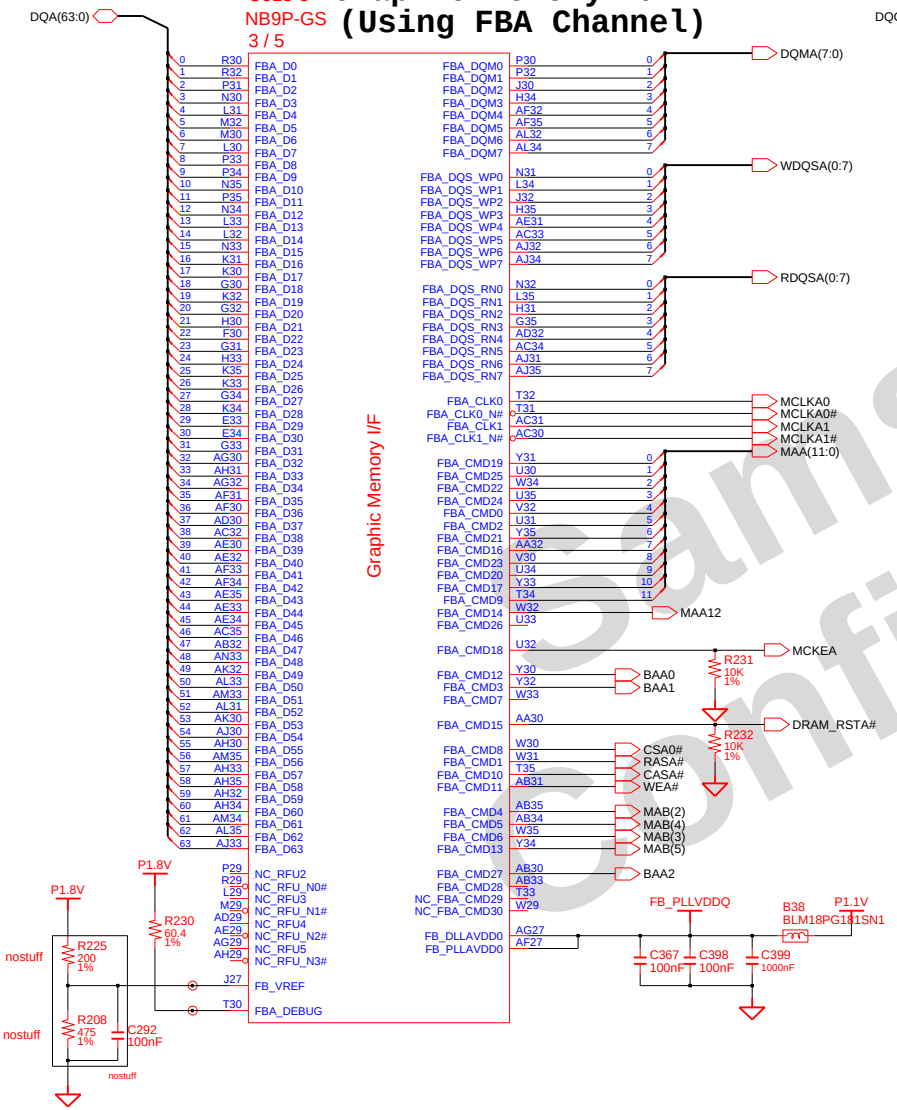
10mil width and spacing

HDCP (EEPROM)

DRAW: MS YANG / Dany Lee	DATE: 8/14/2007	TITLE: OSLO2 EXT NB9X NB9X CHIP (2/4)	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		
APPROVAL: MK KIM	REV: REV 1.1		PART NO.: BA41-00866A
MODULE CODE:	LAST EDIT: May 15, 2008 08:19:32 AM		PAGE 2 OF 5

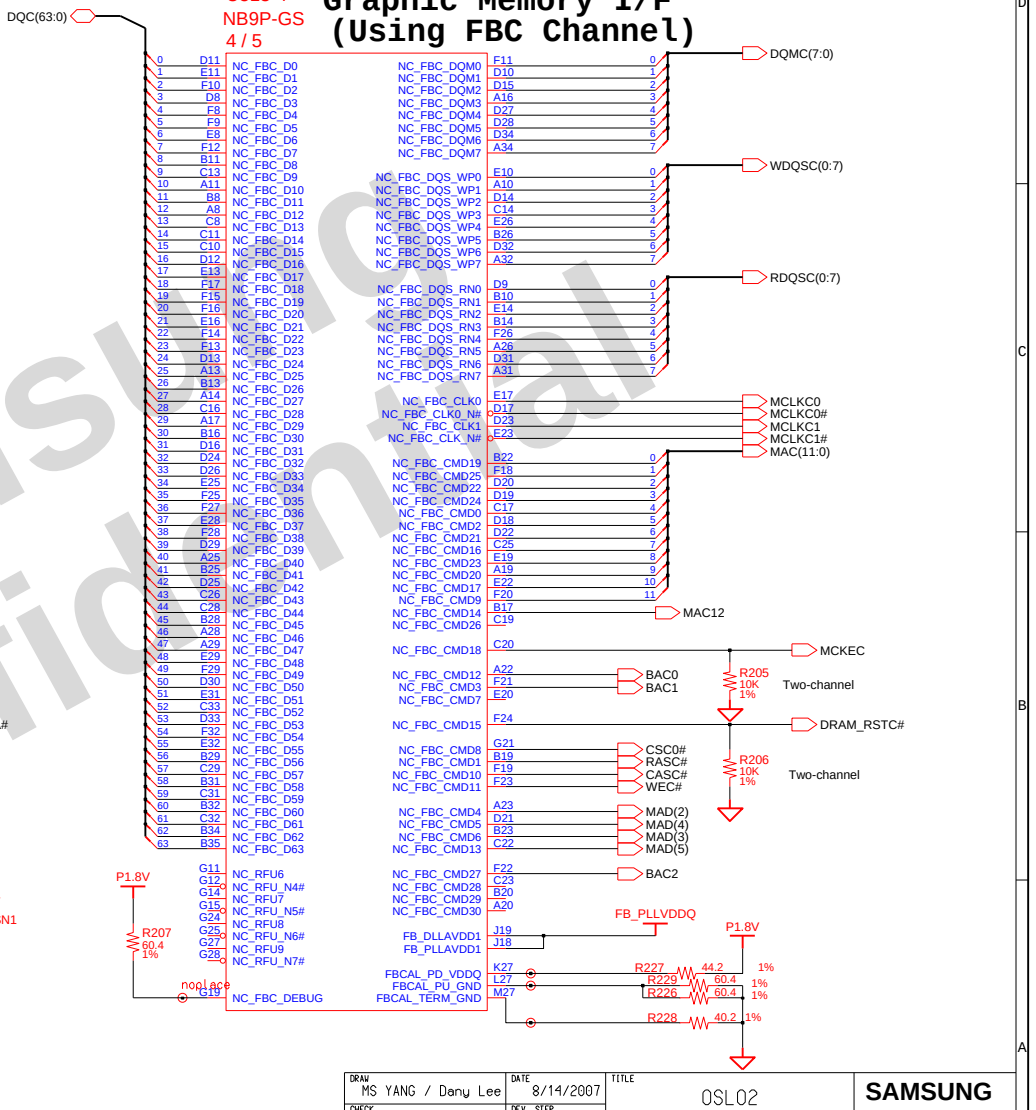
Graphic Memory I/F (Using FBA Channel)

U513-3 NB9P-GS 3 / 5

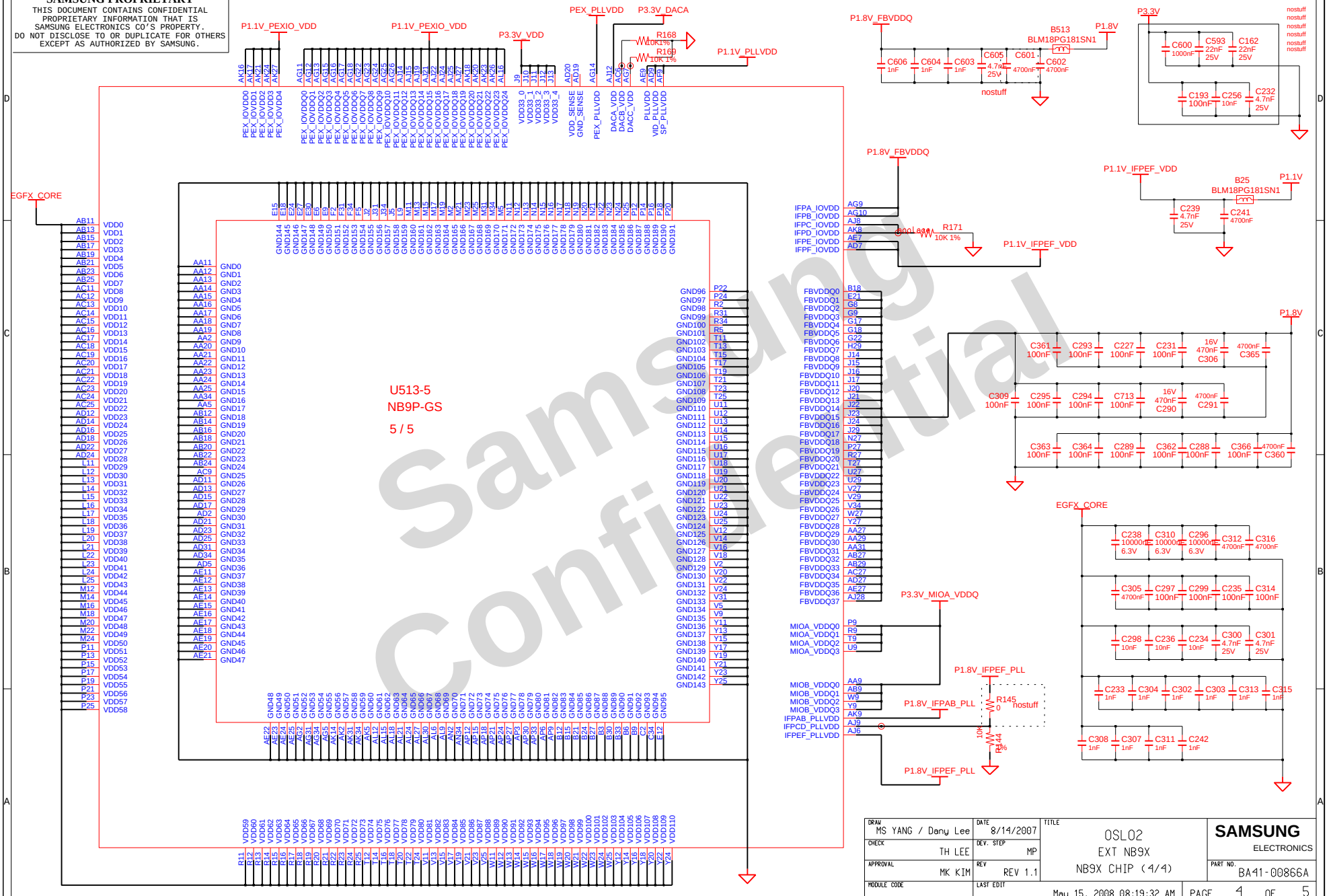


Graphic Memory I/F (Using FBC Channel)

U513-4 NB9P-GS 4 / 5

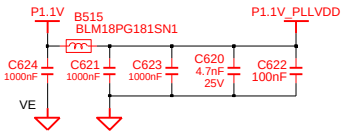


DRAW: MS YANG / Dany Lee	DATE: 8/14/2007	TITLE: OSLO2 EXT NB9X NB9X CHIP (3/4)	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		
APPROVAL: MK KIM	REV: REV 1.1		PART NO.: BA41-00866A
MODULE CODE:	LAST EDIT: May 15, 2008 08:19:32 AM	PAGE 3 OF 5	

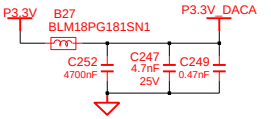


DRAW: MS YANG / Dany Lee	DATE: 8/14/2007	TITLE: OSLO2 EXT NB9X NB9X CHIP (4/4)	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		
APPROVAL: MK KIM	REV: REV 1.1		PART NO.: BA41-00866A
MODULE CODE:	LAST EDIT: May 15, 2008 08:19:32 AM		PAGE 4 OF 5

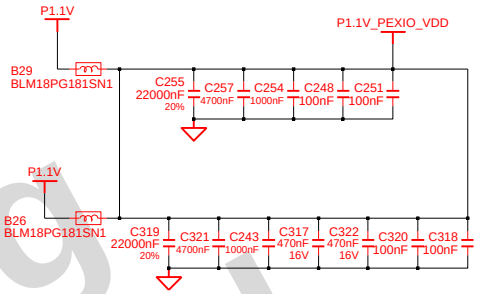
PLL_VDD



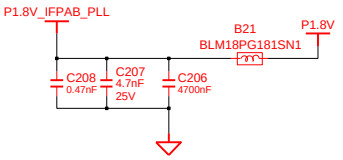
DACA/B/C



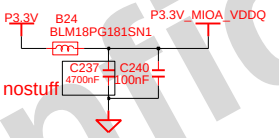
PEX_IOVDD (/w PEX_IOVDDQ)



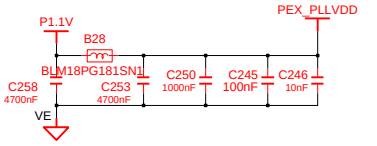
IFPAB_PLLVDD



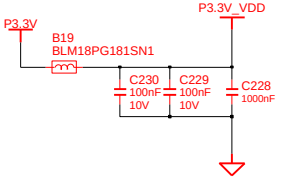
MIOA/B_VDDQ



PEX_PLL_VDD



3.3V_VDD



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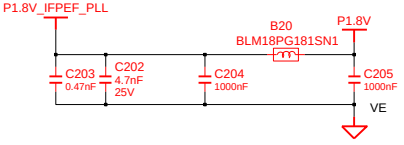
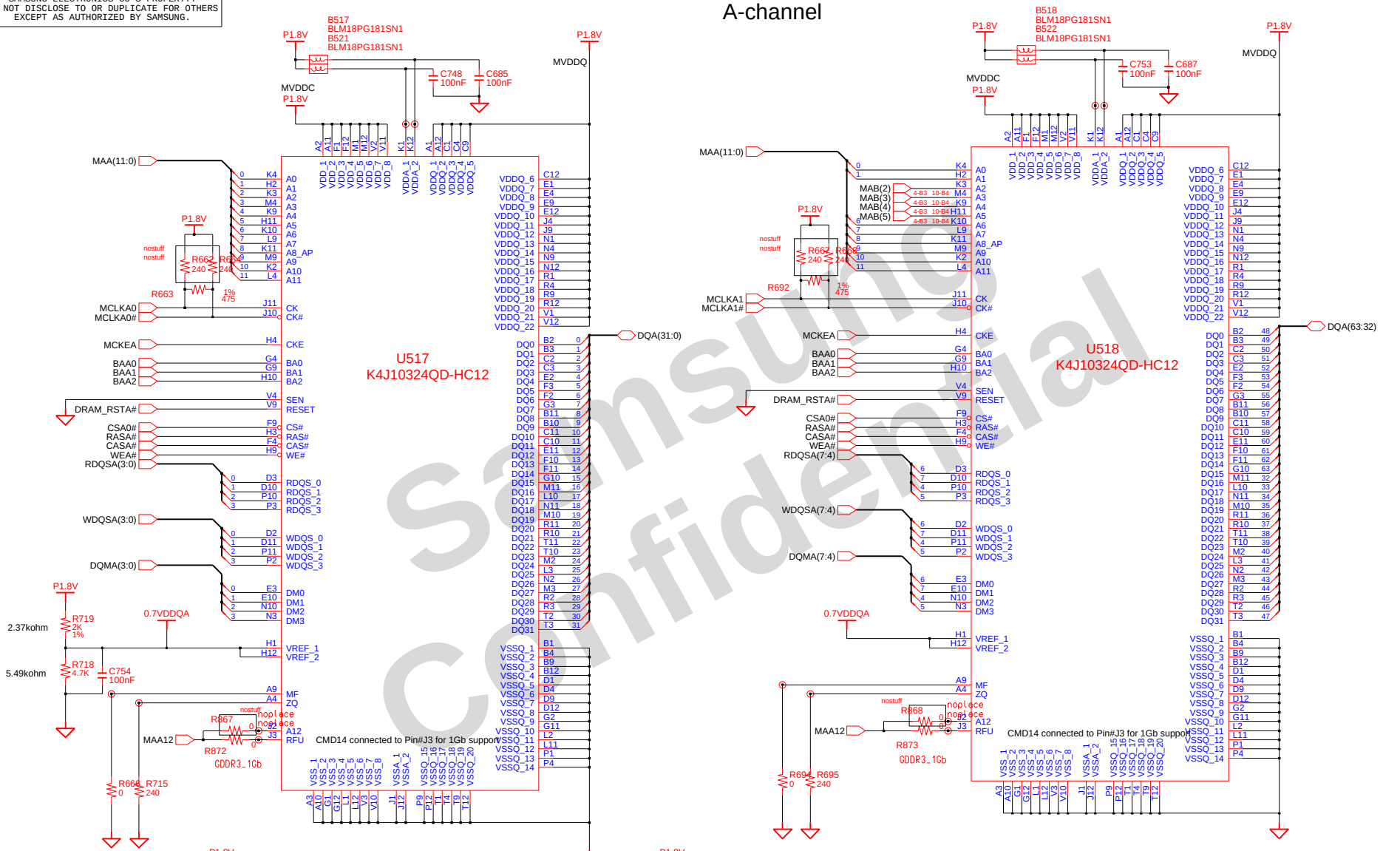


DRAW: MS YANG / Dany Lee	DATE: 8/14/2007	TITLE: OSLO2 EXT NB9X NB9X POWER RAIL	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		
APPROVAL: MK KIM	REV: REV 1.1		PART NO.: BA41-00866A
MODULE CODE:	LAST EDIT: May 15, 2008 08:19:32 AM	PAGE 5 OF 5	

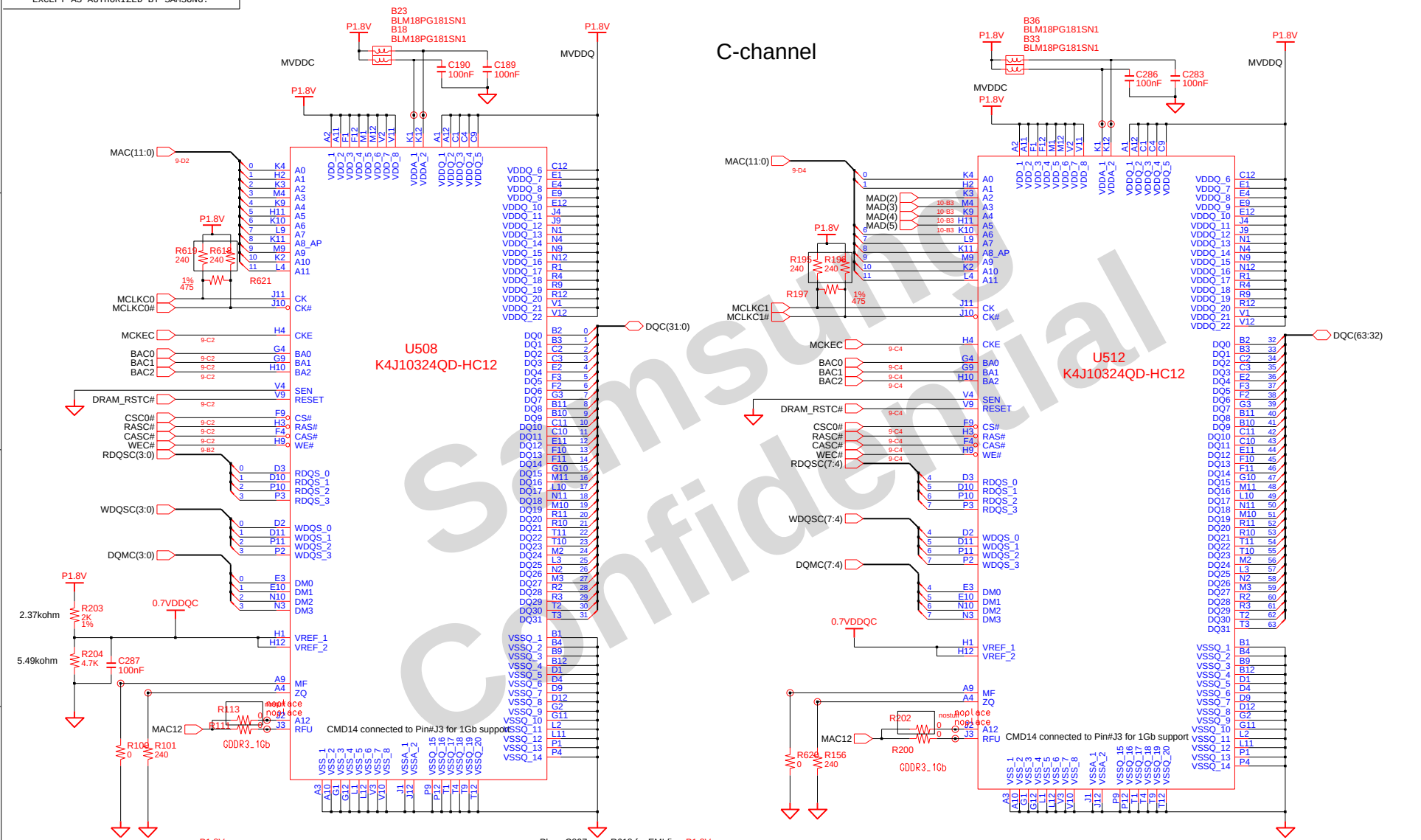
A-channel



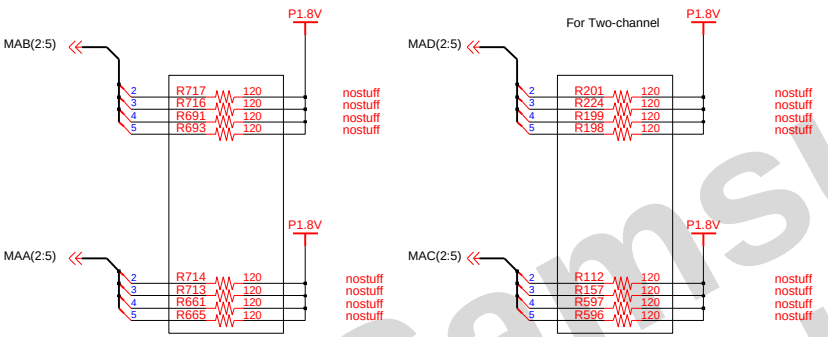
DRAW: MS YANG / Dany Lee	DATE: 8/12/2006	TITLE: OSLO2 Graphics_Memory Graphics_Memory_Nvidia #1	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		
APPROVAL: MK KIM	REV: REV 1.1		PART NO.: BA41-00866A
MODULE CODE:	LAST EDIT: May 15, 2008 08:19:32 AM		PAGE 1 OF 3

This page is for "2channel-model".

C-channel

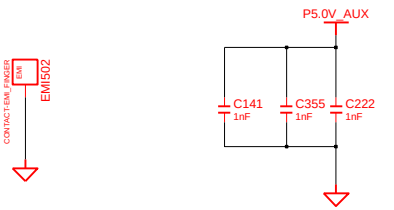


DRAW: MS YANG / Dany Lee	DATE: 8/12/2006	TITLE: OSLO2 Graphics_Memory Graphics_Memory_Nvidia #2	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		
APPROVAL: MK KIM	REV: REV 1.1		PART NO.: BA41-00866A
MODULE CODE:	LAST EDIT: May 15, 2008 08:19:32 AM		PAGE 2 OF 3

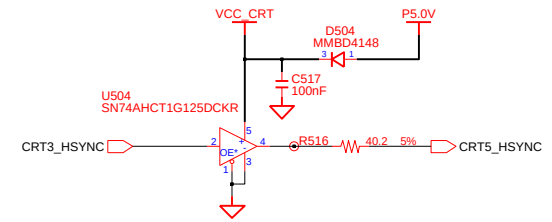


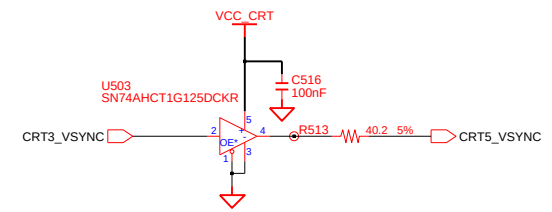
EMI solution @ OSLO2

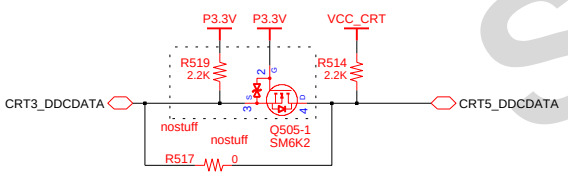
Place three 1nF capacitor around C-channnel component

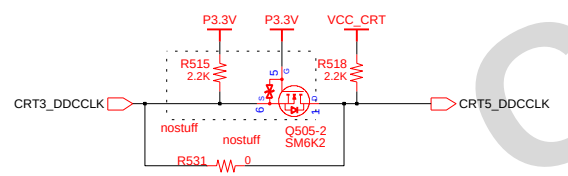


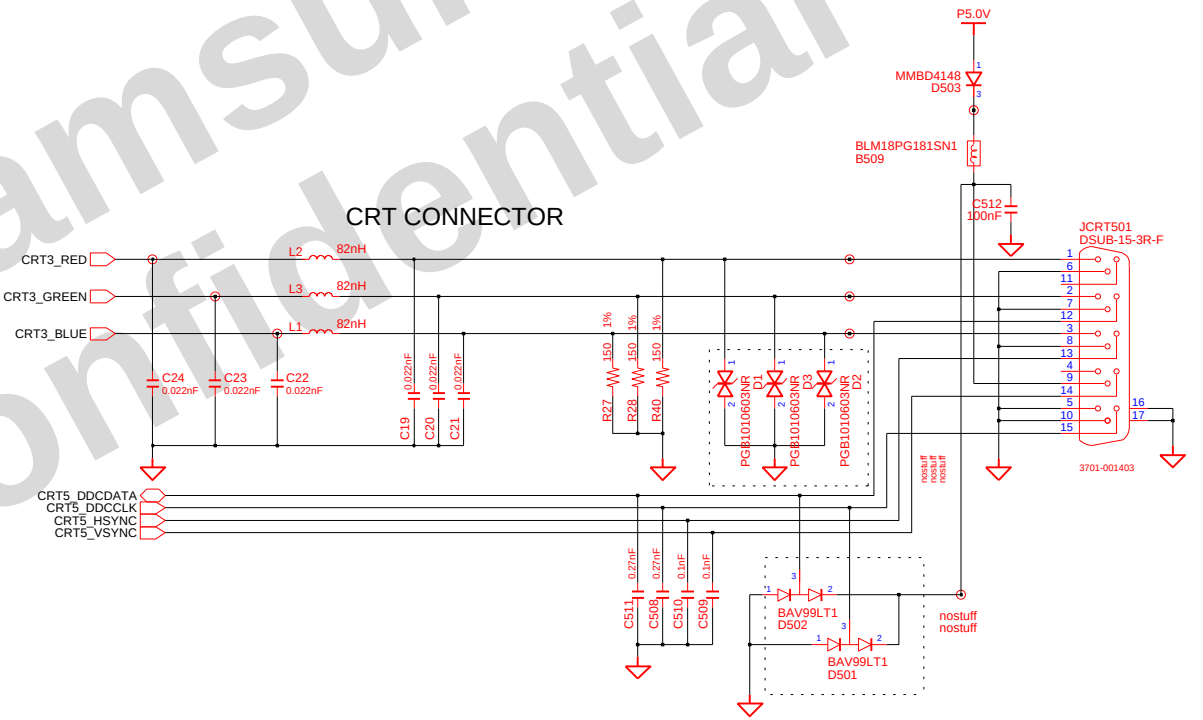
DRAW: MS YANG / Dany Lee	DATE: 8/12/2006	TITLE: OSLO2 Graphics_Memory Graphics_Memory_Nvidia #3	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		
APPROVAL: MK KIM	REV: REV 1.1		PART NO.: BA41-00866A
MODULE CODE:	LAST EDIT: May 15, 2008 08:19:32 AM		PAGE 3 OF 3



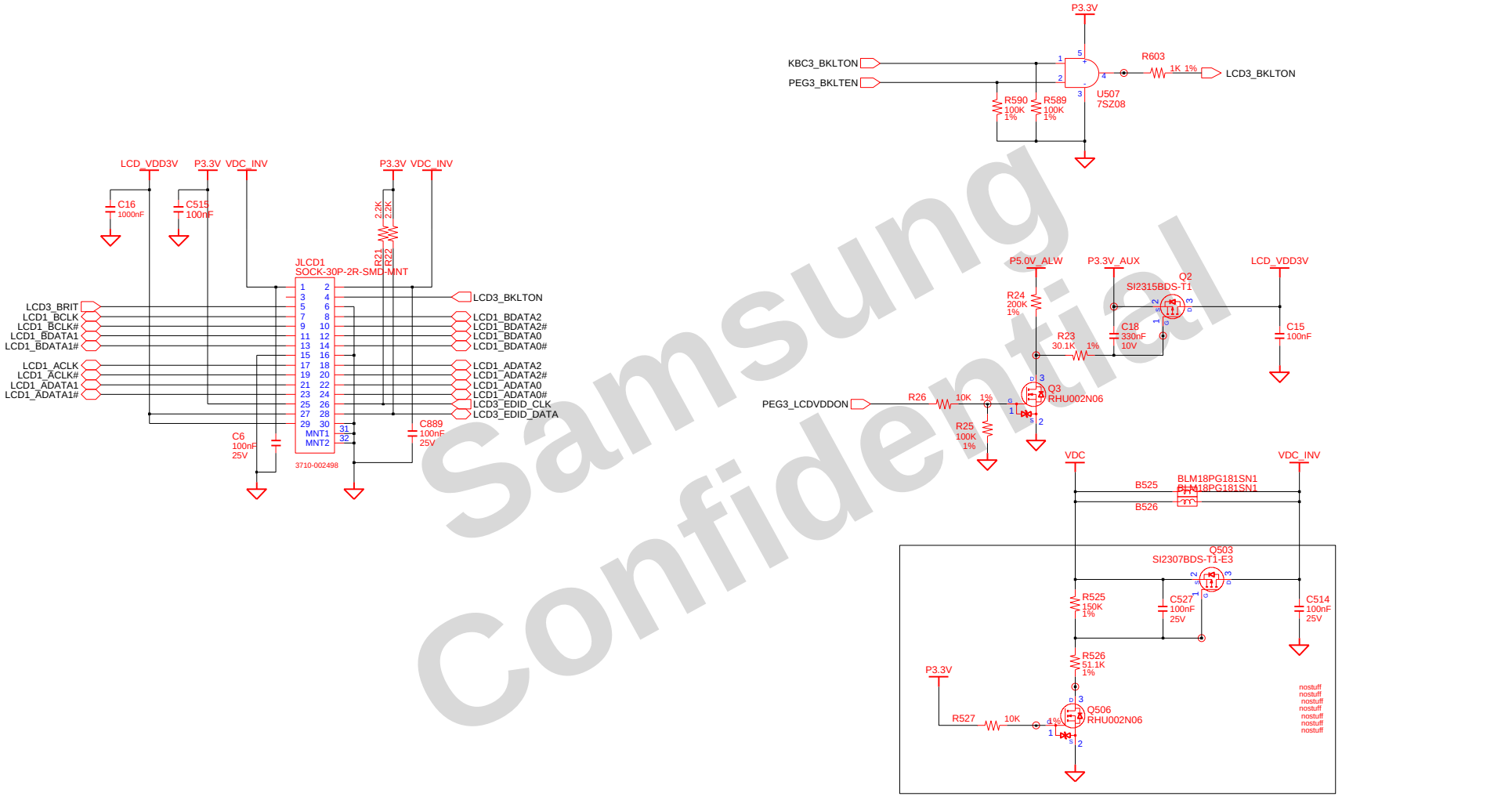




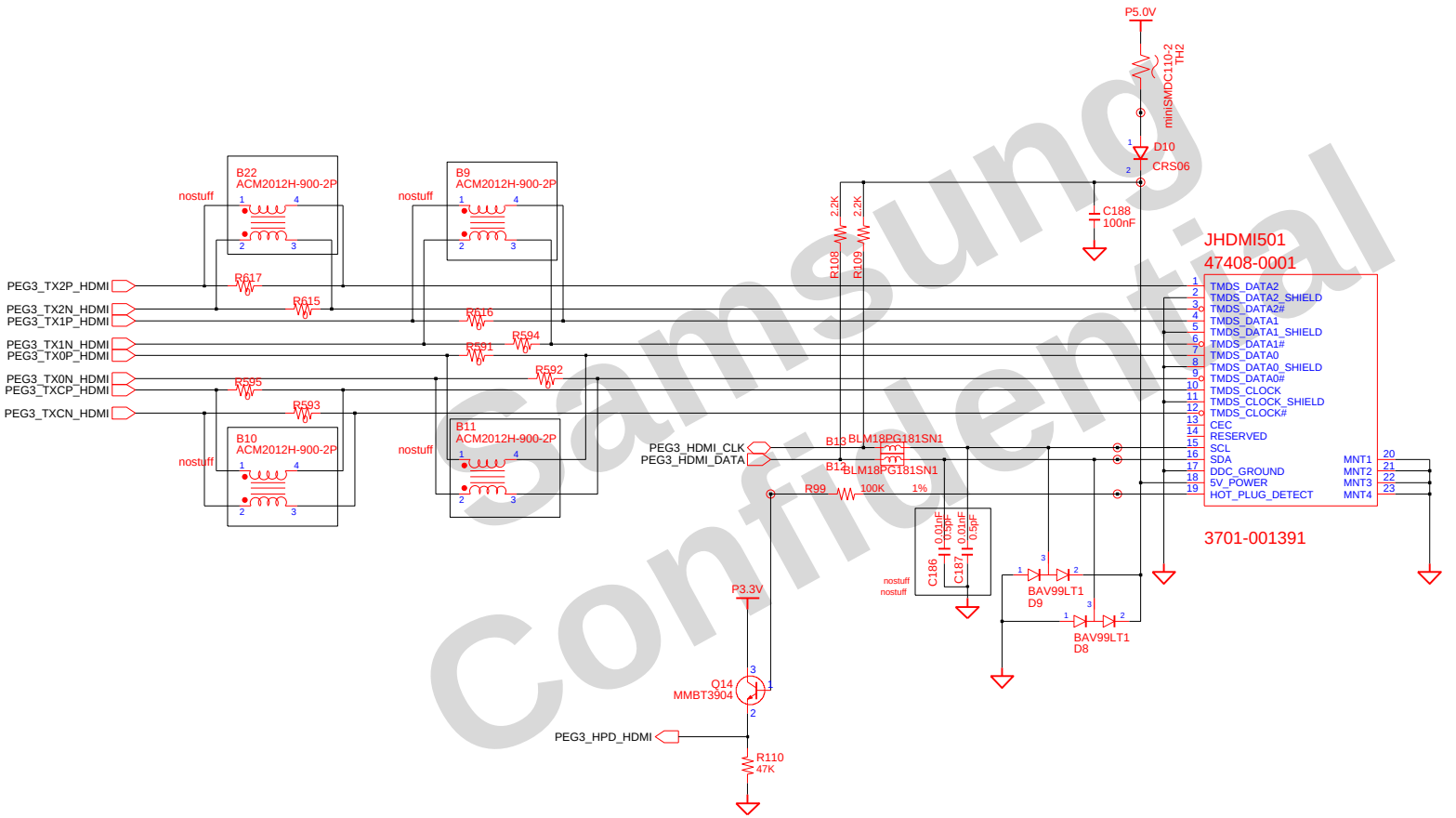




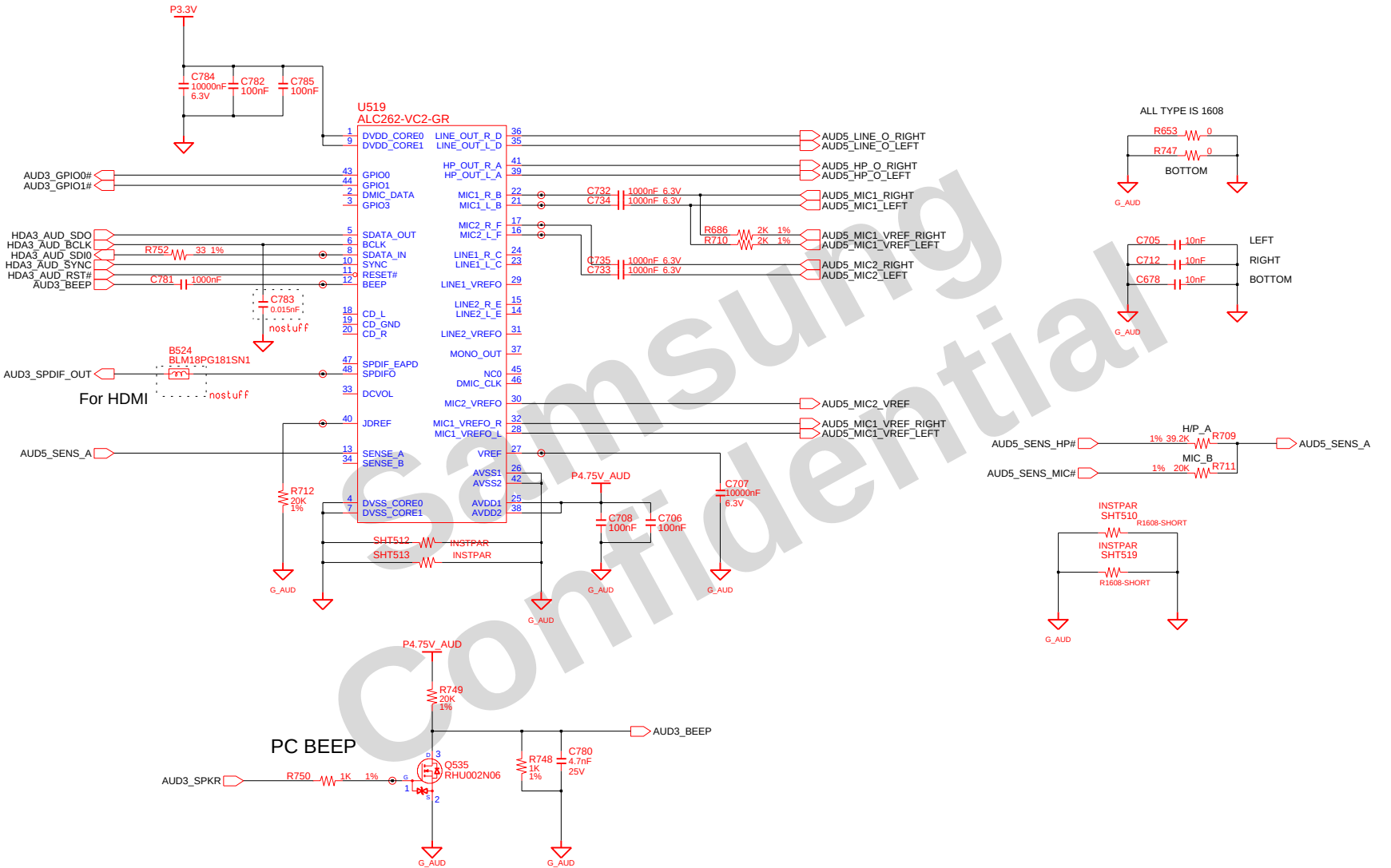
DRAW: MS YANG / Dany Lee	DATE: 8/12/2006	TITLE: OSL02 Interface_Circuit Graphics_IF_CRT	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		PART NO.: BA41-00866A
APPROVAL: MK KIM	REV: REV 1.1		
MODULE CODE:	LAST EDIT: May 15, 2008 08:19:32 AM	PAGE 1 OF 3	



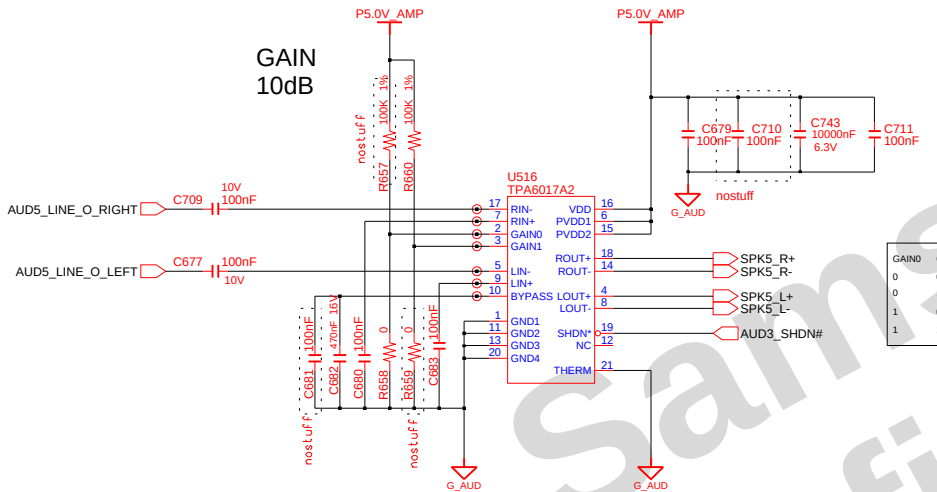
DRAW: MS YANG / Dany Lee	DATE: 8/17/2007	TITLE: OSLO2 UNDEFINED	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		
APPROVAL: MK KIM	REV: REV 1.1		PART NO.: BA41-00866A
MODULE CODE:	LAST EDIT: May 15, 2008 08:19:32 AM	PAGE: 12	

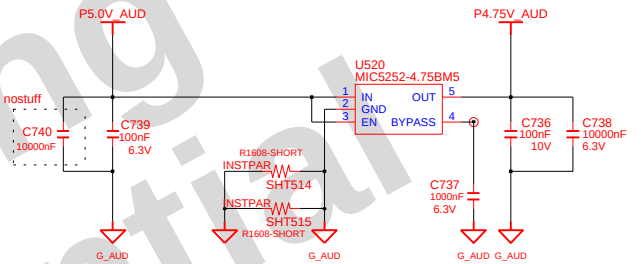


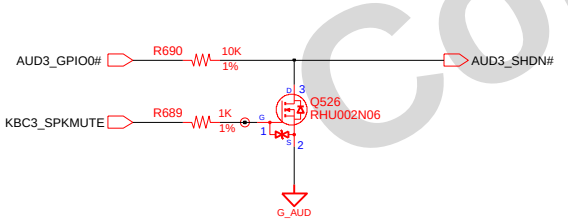
DRAW: MS YANG / Dany Lee	DATE: 8/17/2007	TITLE: OSL02 UNDEFINED	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		
APPROVAL: MK KIM	REV: REV 1.1		PART NO.: BA41-00866A
MODULE CODE:	LAST EDIT: May 15, 2008 08:19:32 AM	PAGE: 13	

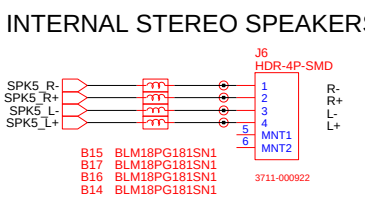


DRAW: MS YANG / Dany Lee	DATE: 8/12/2006	TITLE: OSL02	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP	HDA_Codec_Alc262	
APPROVAL: MK KIM	REV: REV 1.1	HDA_Codec_Alc262 #1	PART NO.: BA41-00866A
MODULE CODE: undefined	LAST EDIT: May 15, 2008 08:19:32 AM	PAGE 1 OF 5	

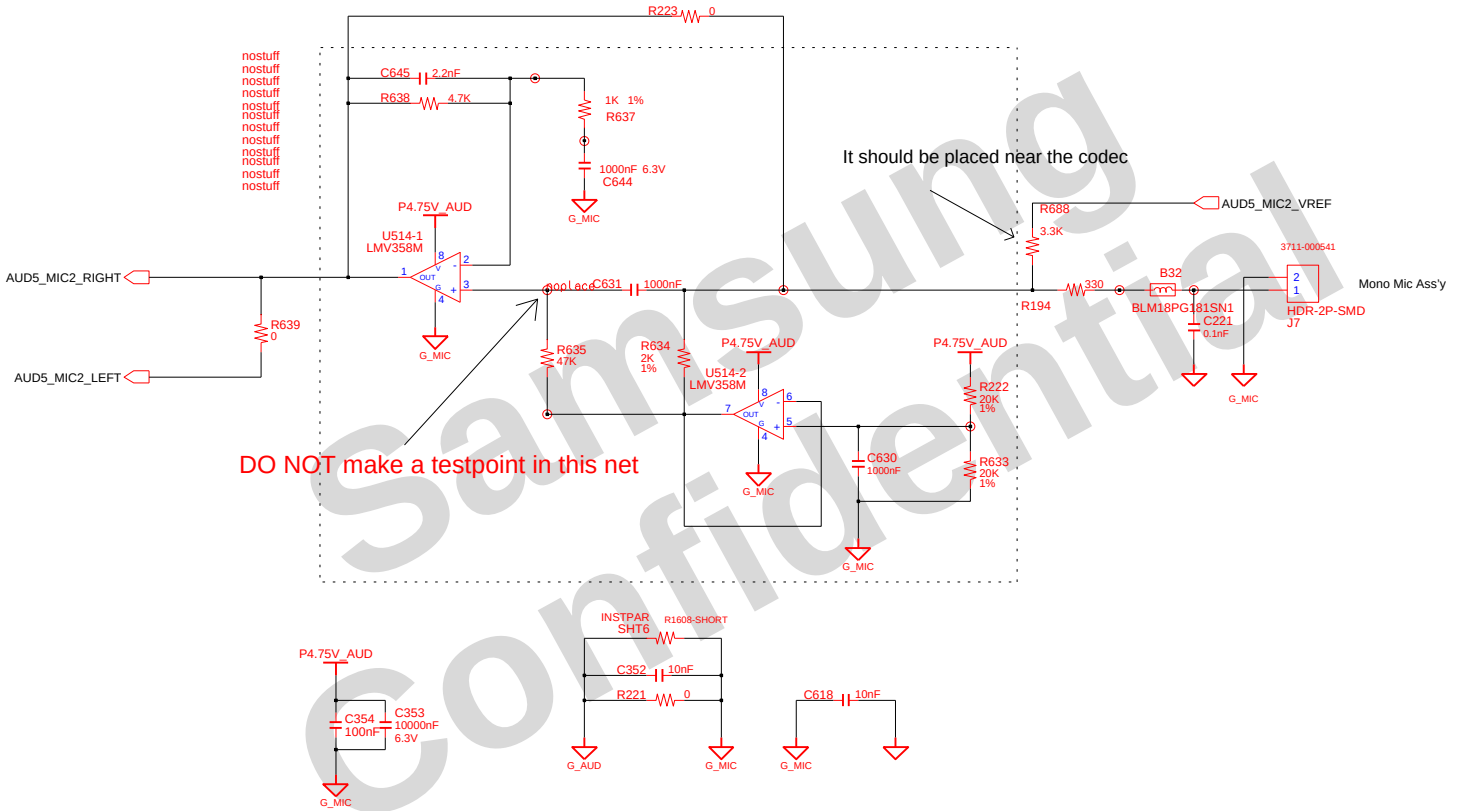






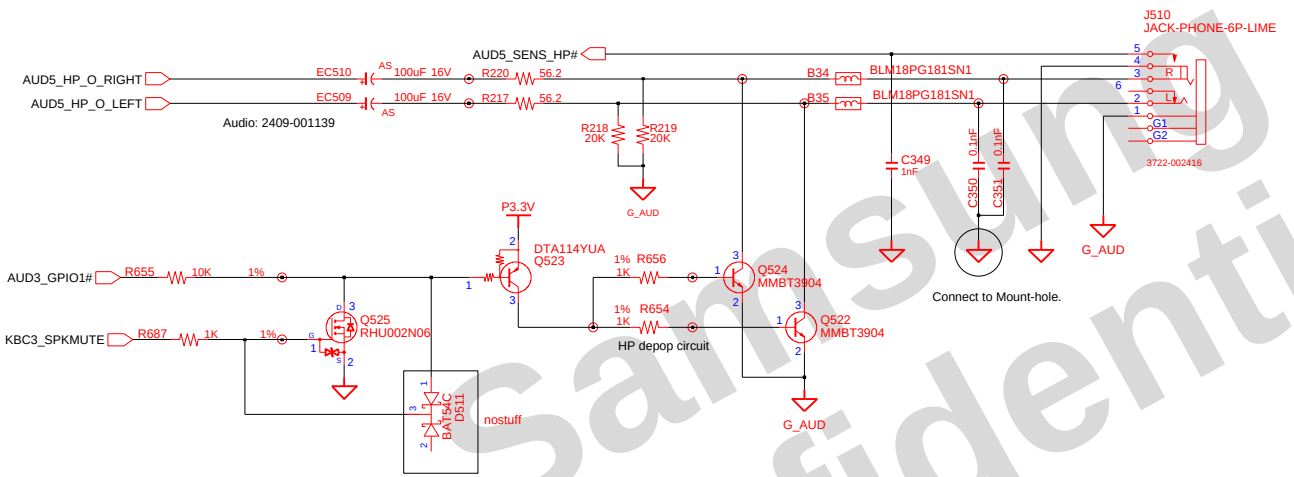


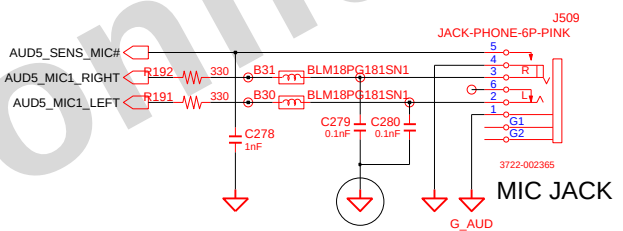
DRAW: MS YANG / Dany Lee	DATE: 8/12/2006	TITLE: OSL02	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP	HDA_Codec_Alc262	
APPROVAL: MK KIM	REV: REV 1.1	HDA_Codec_Alc262 #2	PART NO.: BA41-00866A
MODULE CODE:	LAST EDIT: May 15, 2008 08:19:32 AM	PAGE 2 OF 5	



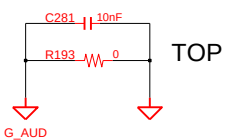
DRAW: MS YANG / Dany Lee	DATE: 8/12/2006	TITLE: OSL02 HDA_Codec_Alc262 HDA_Codec_Alc262 #3	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		
APPROVAL: MK KIM	REV: REV 1.1		PART NO.: BA41-00866A
MODULE CODE: undefined	LAST EDIT: May 15, 2008 08:19:32 AM	PAGE 3 OF 5	

HEADPHONE





MIC JACK

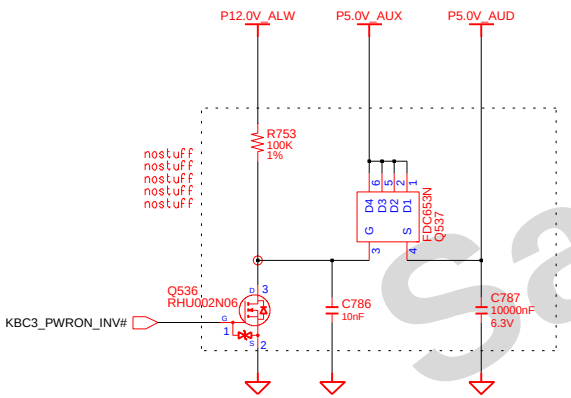


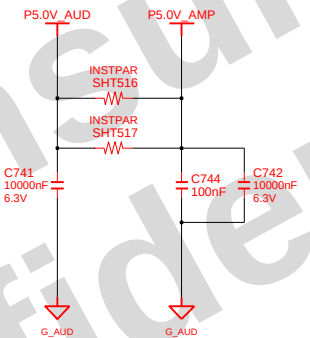
TOP

The traces led to Audio Jacks have the width over 10mil

DRAW: MS YANG / Dany Lee	DATE: 8/12/2006	TITLE: OSL02	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP	HDA_Codec_Alc262	
APPROVAL: MK KIM	REV: REV 1.1	HDA_Codec_Alc262 #4	PART NO.: BA41-00866A
MODULE CODE:	LAST EDIT: May 15, 2008 08:19:32 AM	PAGE 4 OF 5	

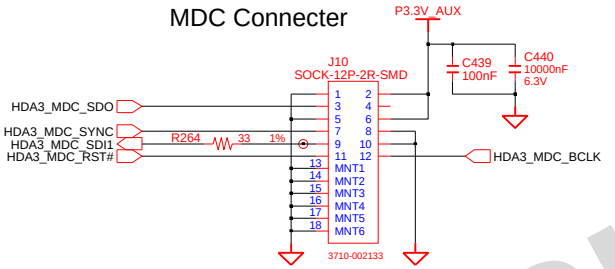
AUDIO POWER





DRAW: MS YANG / Dany Lee	DATE: 8/12/2006	TITLE: OSL02 HDA_Codec_Alc262 HDA_Codec_Alc262 #5	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		
APPROVAL: MK KIM	REV: REV 1.1		PART NO.: BA41-00866A
MODULE CODE: undefined	LAST EDIT: May 15, 2008 08:19:32 AM	PAGE 5 OF 5	

MDC Connecter



MDC-model MDC-model
MDC-model MDC-model
MDC-model
MDC-model
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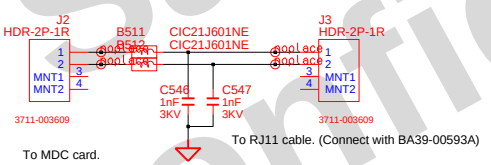
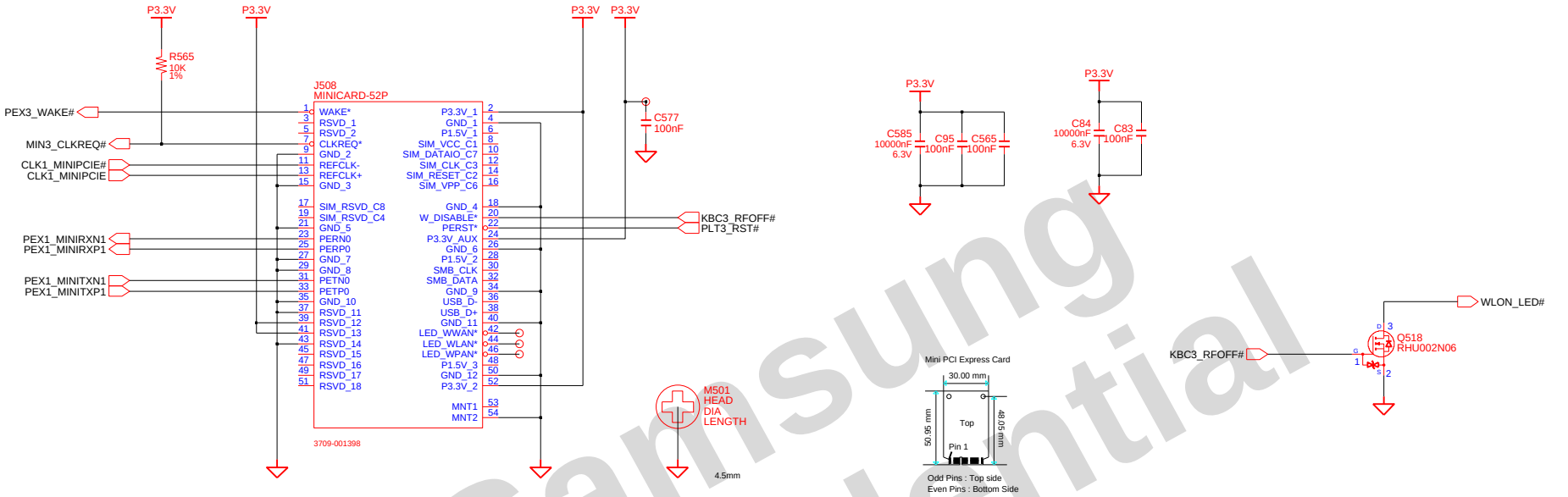
MDC-model
MDC-model
MDC-model



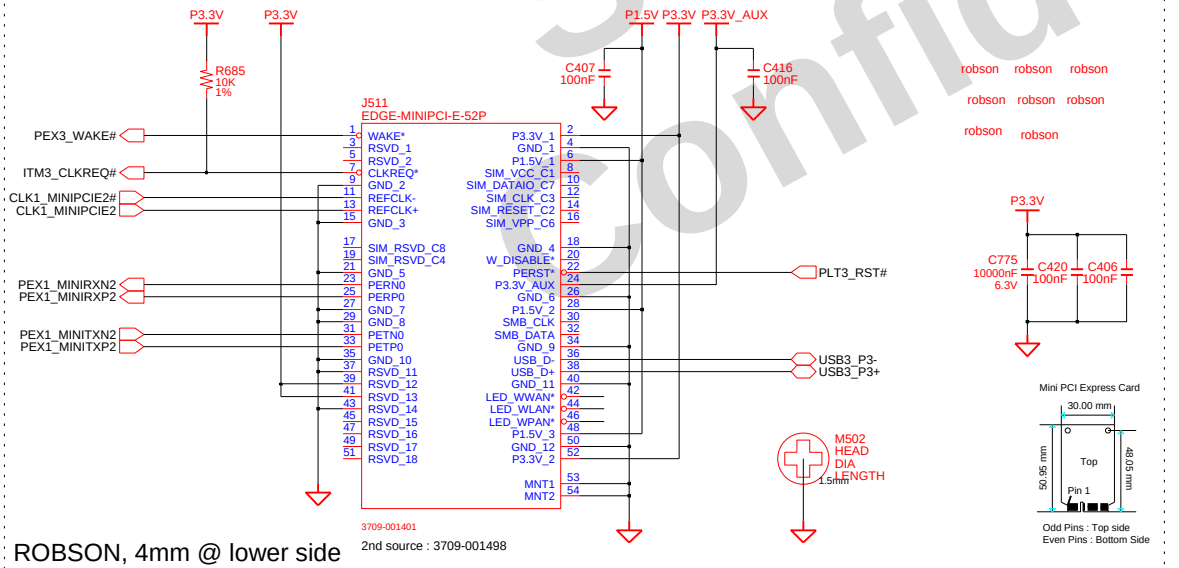
DRAW: MS YANG / Dany Lee	DATE: 8/12/2006	TITLE: OSL02 HDA_Modem HDA_Modem	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		
APPROVAL: MK KIM	REV: REV 1.1		PART NO.: BA41-00866A
MODULE CODE:	LAST EDIT: May 15, 2008 08:19:32 AM	PAGE 1 OF 1	

WLAN, 7mm @ Upper side

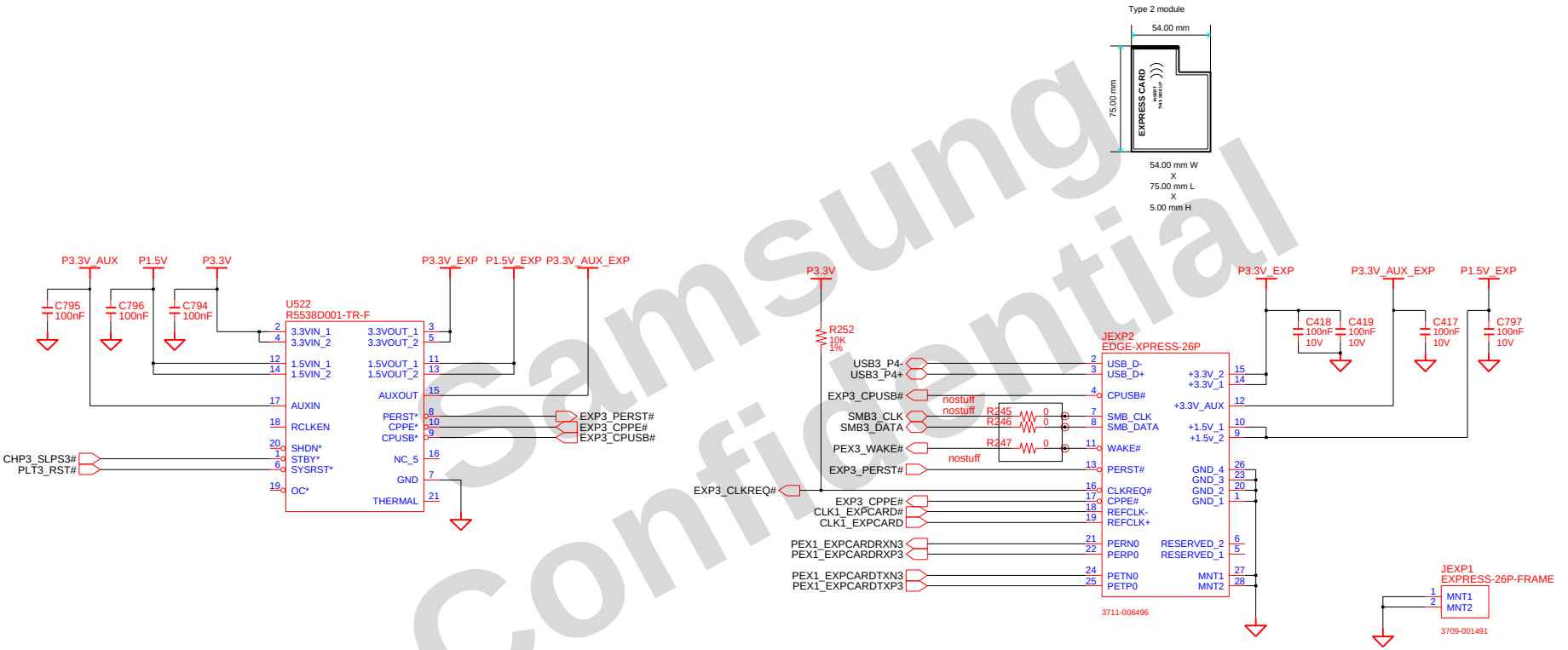


To fix Shirley Peak EMI issue
Place it at the old rubber area

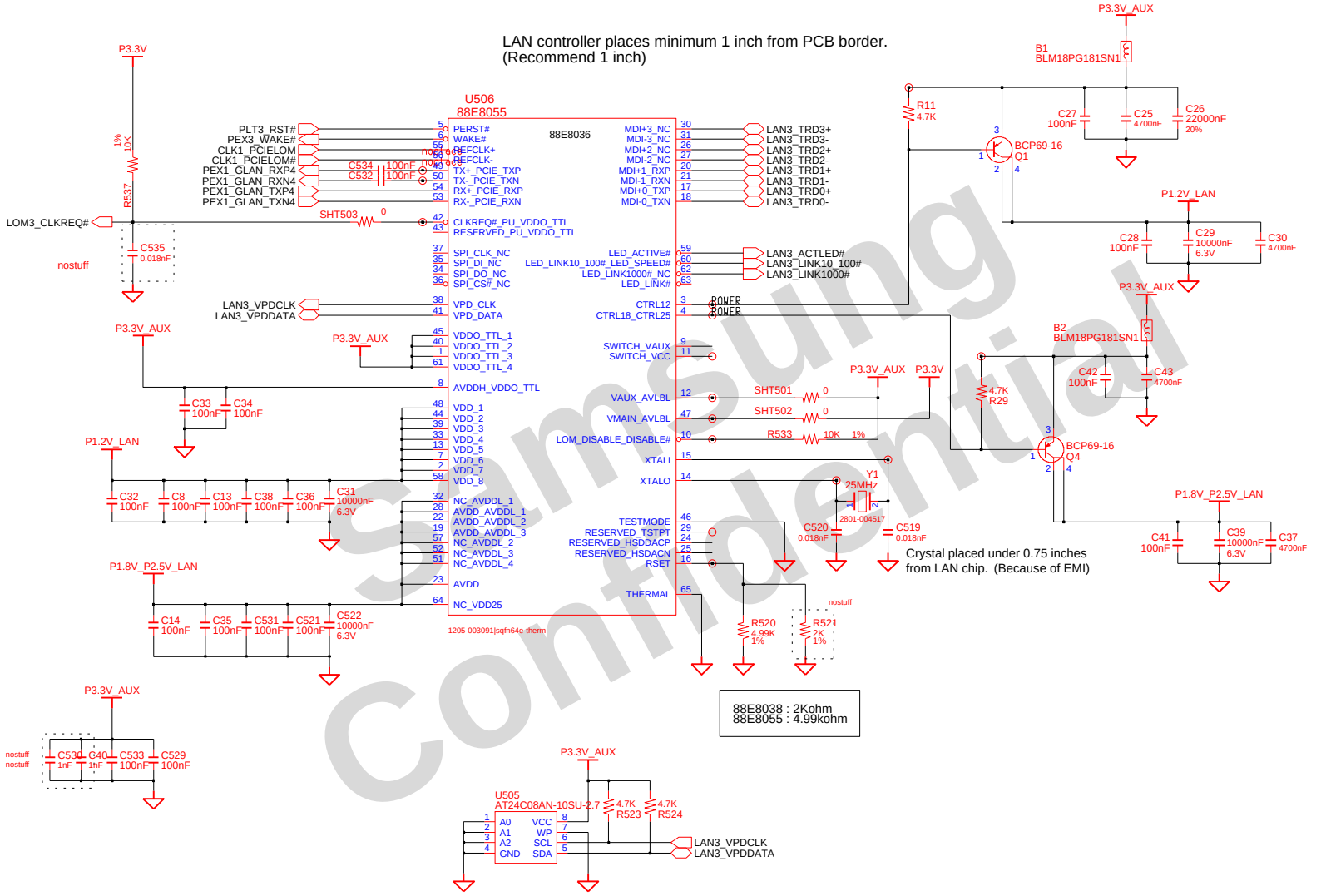
ROBSON, 4mm @ lower side



DRAW: MS YANG / Dany Lee	DATE: 8/12/2006	TITLE: OSL02 PCIE_Minicard_Slot PCIE_Minicard_Slot	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		
APPROVAL: MK KIM	REV: REV 1.1		PART NO.: BA41-00866A
MODULE CODE: undefined	LAST EDIT: May 15, 2008 08:19:32 AM	PAGE 1 OF 1	

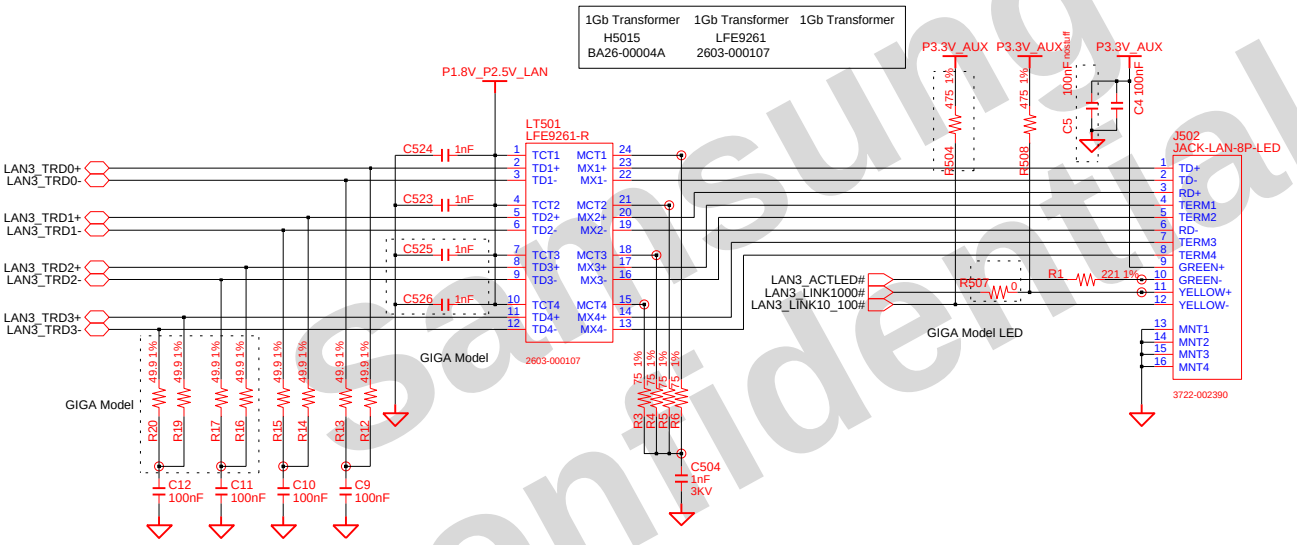


DRAW: MS YANG / Dany Lee	DATE:	TITLE: OSL02	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		
APPROVAL: MK KIM	REV: REV 1.1		PART NO.: BA41-00866A
MODULE CODE: undefined	LAST EDIT: May 15, 2008 08:19:32 AM	PAGE	OF



DRAW: MS YANG / Dany Lee	DATE: 8/12/2006	TITLE: OSLO2 LAN_Marvell_8055 LAN_Marvell_8055	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		
APPROVAL: MK KIM	REV: REV 1.1		PART NO.: BA41-00866A
MODULE CODE:	LAST EDIT: May 15, 2008 08:19:32 AM		PAGE 1 OF 2

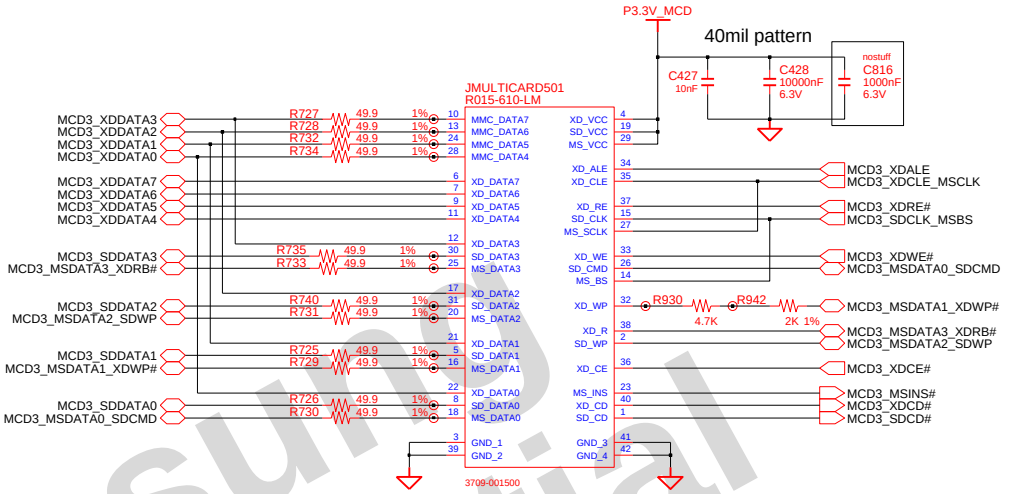
The distance between LAN controller
and transformer is designed to extend less than two inches.



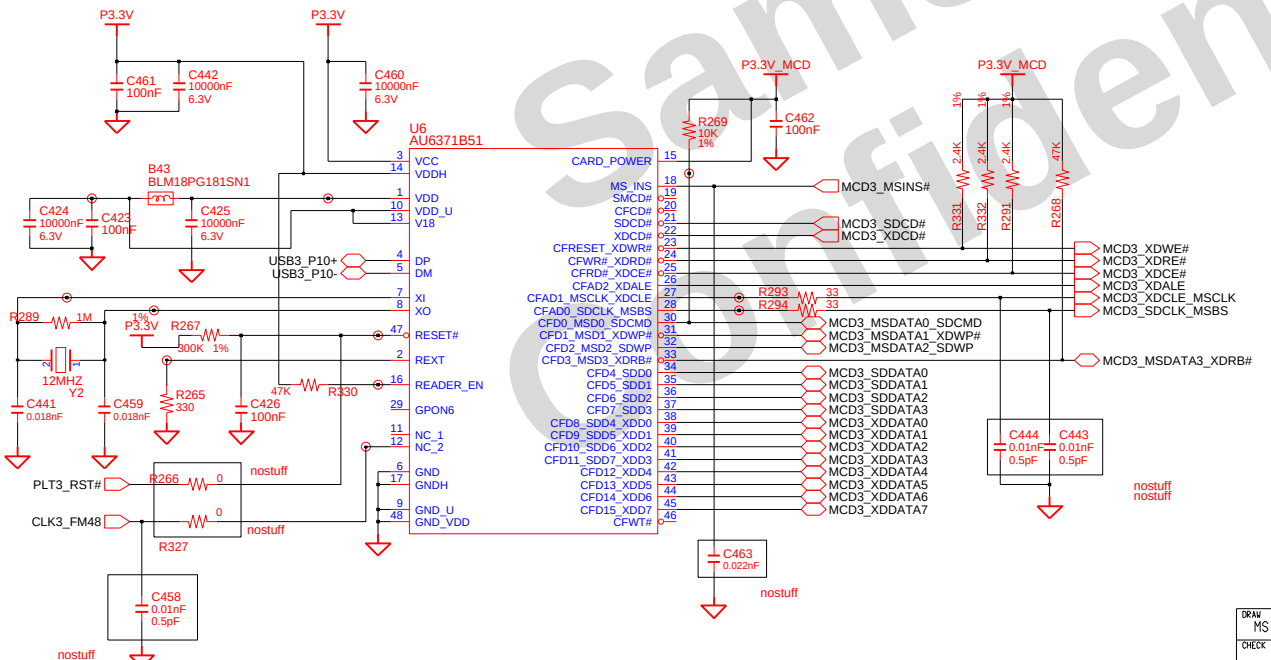
Place near to the Marvell chip.

DRAW: MS YANG / Dany Lee	DATE: 8/12/2006	TITLE: OSL02 LAN_Marvell_8055 LAN_Marvell_8055	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		
APPROVAL: MK KIM	REV: REV 1.1		PART NO.: BA41-00866A
MODULE CODE:	LAST EDIT: May 15, 2008 08:19:32 AM	PAGE 2 OF 2	

P3.3V_MCD distance between Controller and socket should be less than 2 inches

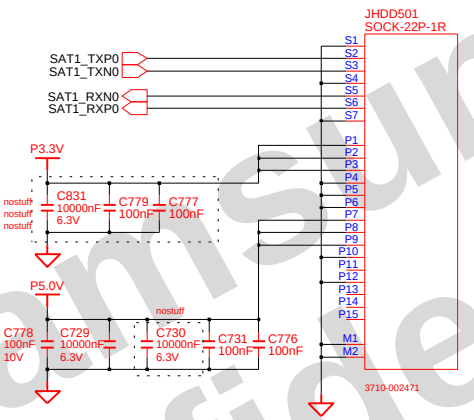


40 mil trace for medica card socket ground



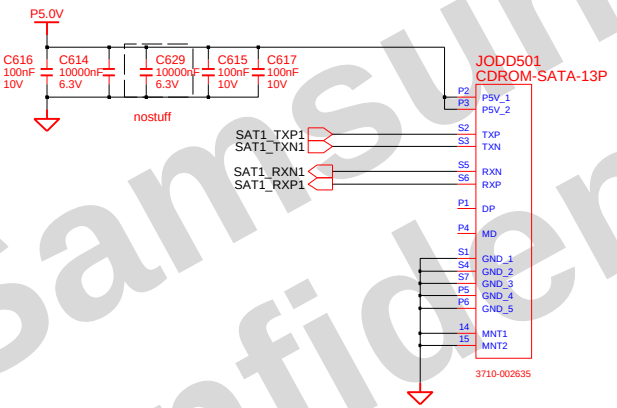
DRAW: MS YANG / Dany Lee	DATE: 8/17/2007	TITLE: OSLO2 UNDEFINED	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		
APPROVAL: MK KIM	REV: REV 1.1		PART NO.: BA41-00866A
MODULE CODE:	LAST EDIT: May 15, 2008 08:19:32 AM	PAGE: 15	

FOR SATA HDD



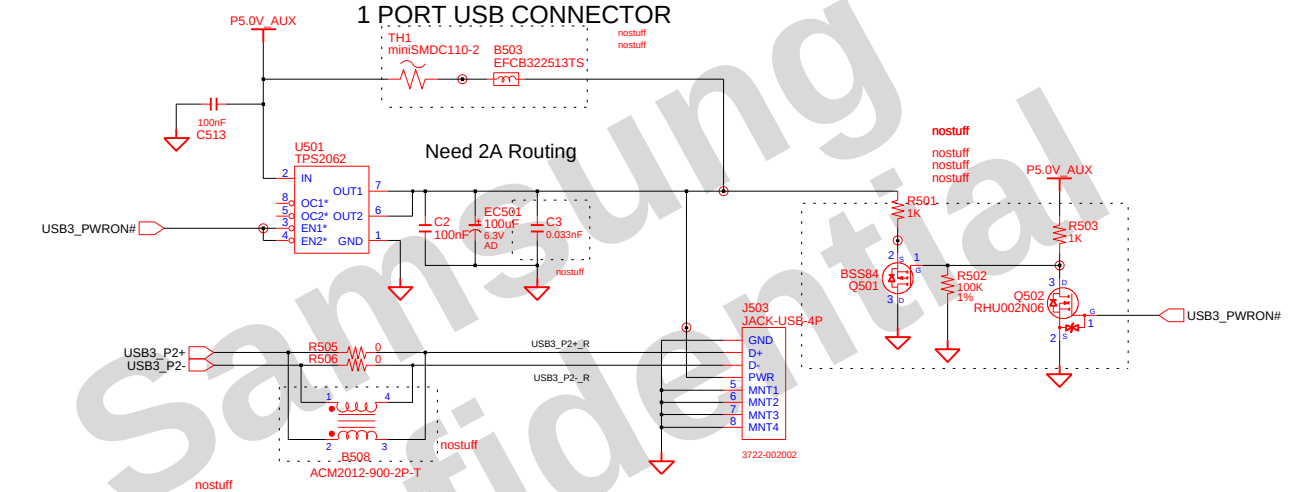
DRAW: MS YANG / Dany Lee	DATE: 8/12/2006	TITLE: OSL02 HDD_IF_Conn HDD_IF_Conn	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		
APPROVAL: MK KIM	REV: REV 1.1		PART NO.: BA41-00866A
MODULE CODE:	LAST EDIT: May 15, 2008 08:19:32 AM	PAGE 1 OF 1	

SATA ODD



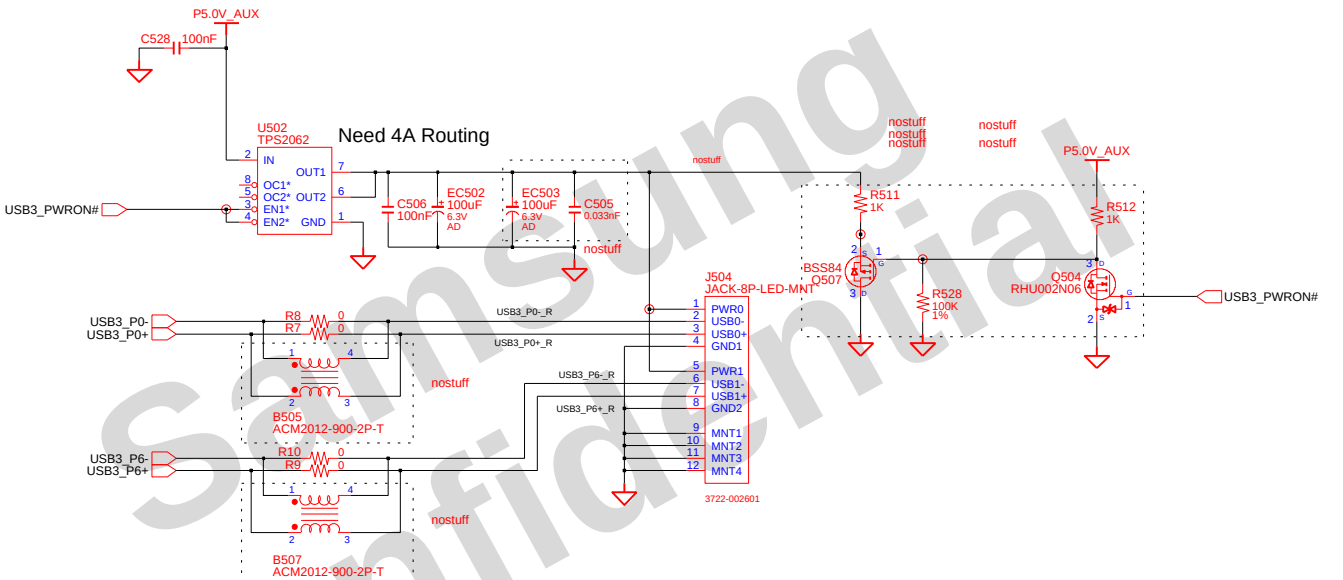
DRAW: MS YANG / Dany Lee	DATE: 8/12/2006	TITLE: OSL02 ODD_IF_Conn ODD_IF_Conn	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		
APPROVAL: MK KIM	REV: REV 1.1		PART NO.: BA41-00866A
MODULE CODE:	LAST EDIT: May 15, 2008 08:19:32 AM	PAGE 1 OF 1	

1 PORT USB CONNECTOR



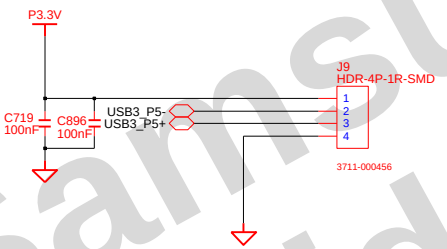
DRAW: MS YANG / Dany Lee	DATE: 8/12/2006	TITLE: OSL02 USB_1Port USB_1Port	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		
APPROVAL: MK KIM	REV: REV 1.1		PART NO.: BA41-00866A
MODULE CODE:	LAST EDIT: May 15, 2008 08:19:32 AM	PAGE 1 OF 1	

2 PORT USB CONNECTOR



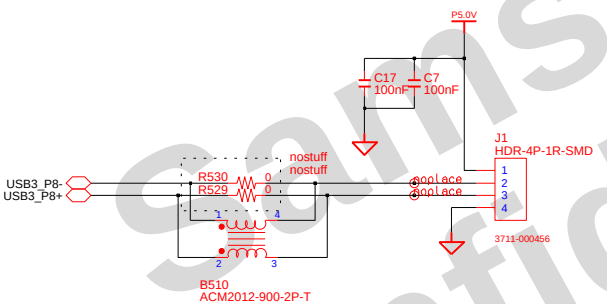
DRAW: MS YANG / Dany Lee	DATE: 8/12/2006	TITLE: OSL02 USB_2Port USB_2Port	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		
APPROVAL: MK KIM	REV: REV 1.1		PART NO.: BA41-00866A
MODULE CODE:	LAST EDIT: May 15, 2008 08:19:32 AM	PAGE 1 OF 1	

Bluetooth Interface



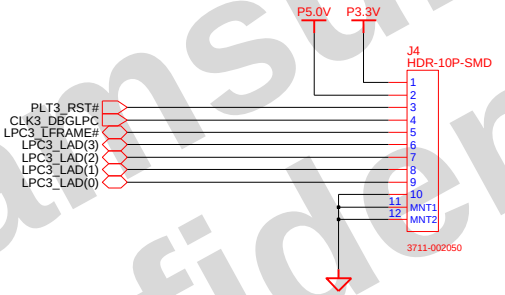
DRAW: MS YANG / Dany Lee	DATE: 8/12/2006	TITLE: OSL02 Bluetooth_IF_Conn Bluetooth_IF_Conn	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		
APPROVAL: MK KIM	REV: REV 1.1		PART NO.: BA41-00866A
MODULE CODE:	LAST EDIT: May 15, 2008 08:19:32 AM	PAGE 1 OF 1	

CAMERA



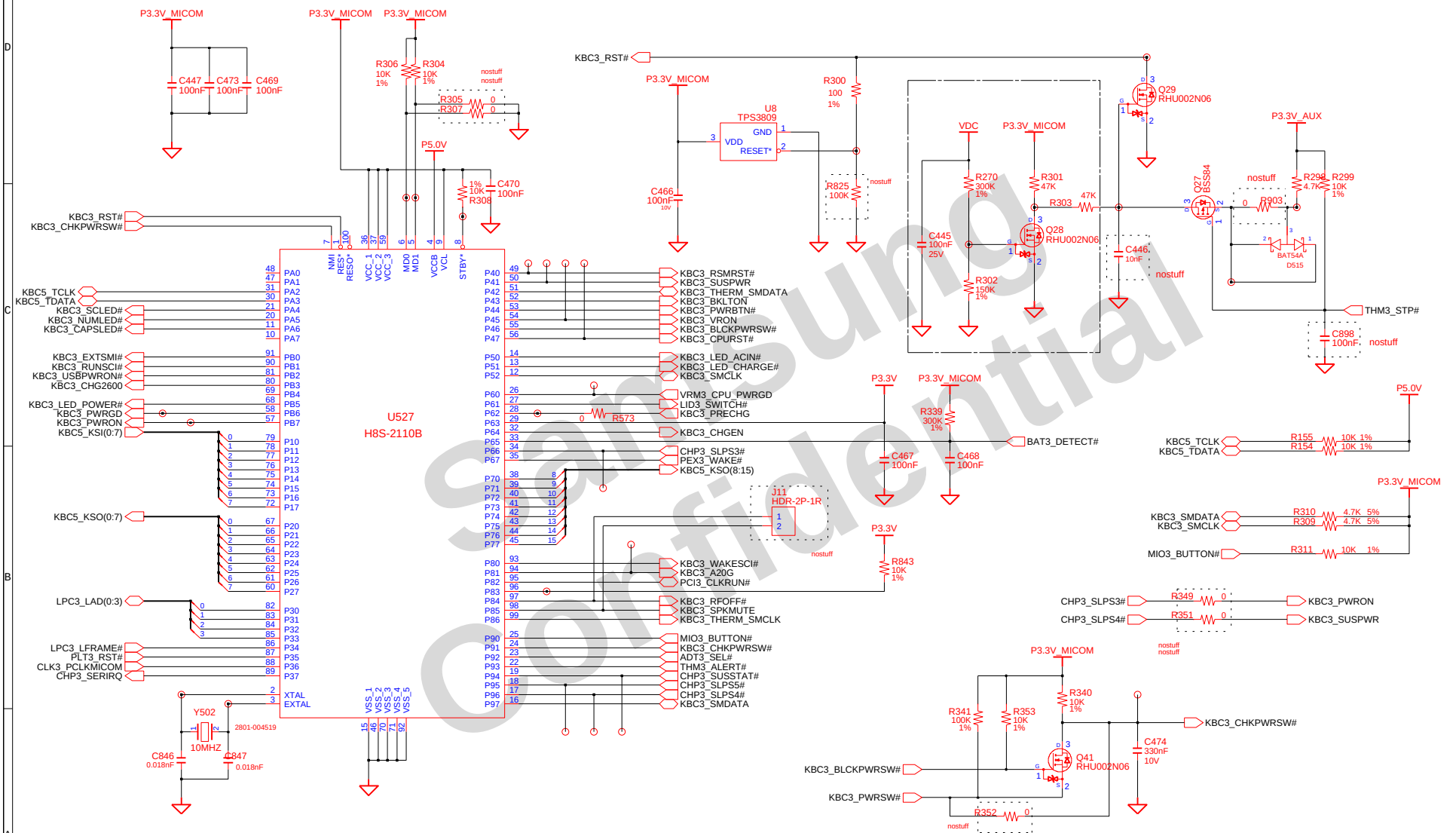
DRAW: MS YANG / Dany Lee	DATE: 8/12/2006	TITLE: OSL02 Camera_IF_Conn Camera_IF_Conn	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		
APPROVAL: MK KIM	REV: REV 1.1		PART NO.: BA41-00866A
MODULE CODE:	LAST EDIT: May 15, 2008 08:19:32 AM	PAGE 1 OF 1	

80H DECODER CONNECTOR



DRAW: MS YANG / Dany Lee	DATE: 8/12/2006	TITLE: OSL02 Other_Debug_80 Other_Debug_80	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		
APPROVAL: MK KIM	REV: REV 1.1		PART NO.: BA41-00866A
MODULE CODE:	LAST EDIT: May 15, 2008 08:19:32 AM	PAGE 1 OF 1	

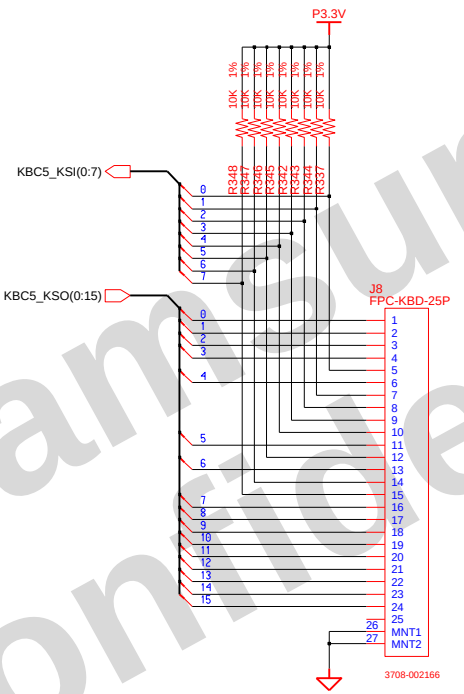
MICOM RESET



POWER SWITCH BLOCK WHILE MICOM UPDATE

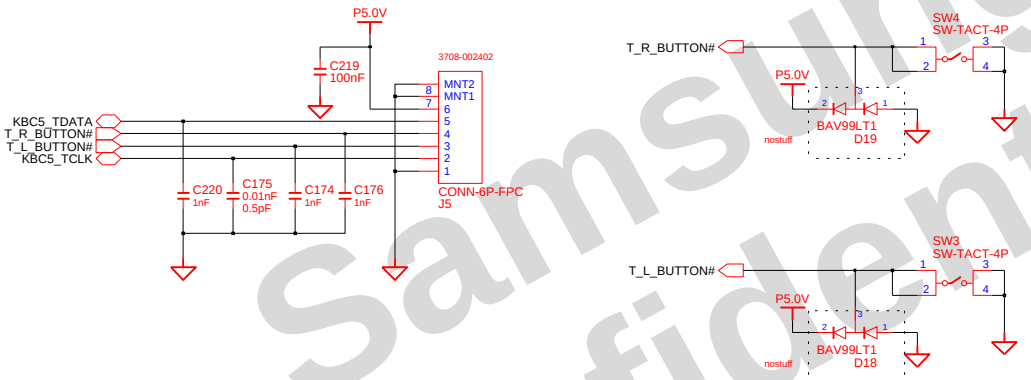
DRAW: MS YANG / Dany Lee	DATE: 8/12/2006	TITLE: OSLO2 MICOM_Renesas2110_100p	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP	MICOM_Renesas2110_100p	
APPROVAL: MK KIM	REV: REV 1.1		PART NO.: BA41-00866A
MODULE CODE:	LAST EDIT: May 15, 2008 08:19:32 AM		PAGE 1 OF 1

KEYBOARD



DRAW: MS YANG / Dany Lee	DATE: 8/12/2006	TITLE: OSL02 KBD_IF_Conn KBD_IF_Conn	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		PART NO.: BA41-00866A
APPROVAL: MK KIM	REV: REV 1.1		
MODULE CODE:	LAST EDIT: May 15, 2008 08:19:32 AM	PAGE 1 OF 1	

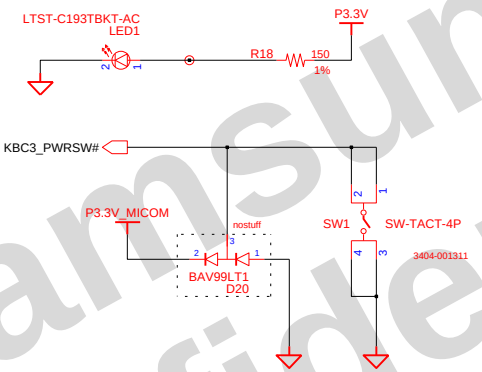
TOUCHPAD



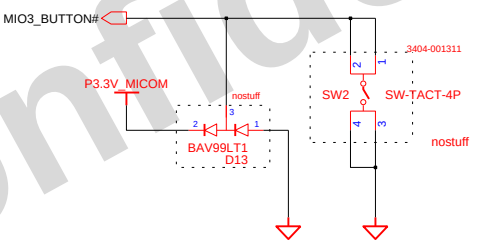
DRAW: MS YANG / Dany Lee	DATE: 8/12/2006	TITLE: OSL02 Touchpad_IF_Conn Touchpad_IF_Conn	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		
APPROVAL: MK KIM	REV: REV 1.1		PART NO.: BA41-00866A
MODULE CODE:	LAST EDIT: May 15, 2008 08:19:32 AM	PAGE 1 OF 1	

Put this LED located near PWRSW from ME recommedation

Power LED, Blue color

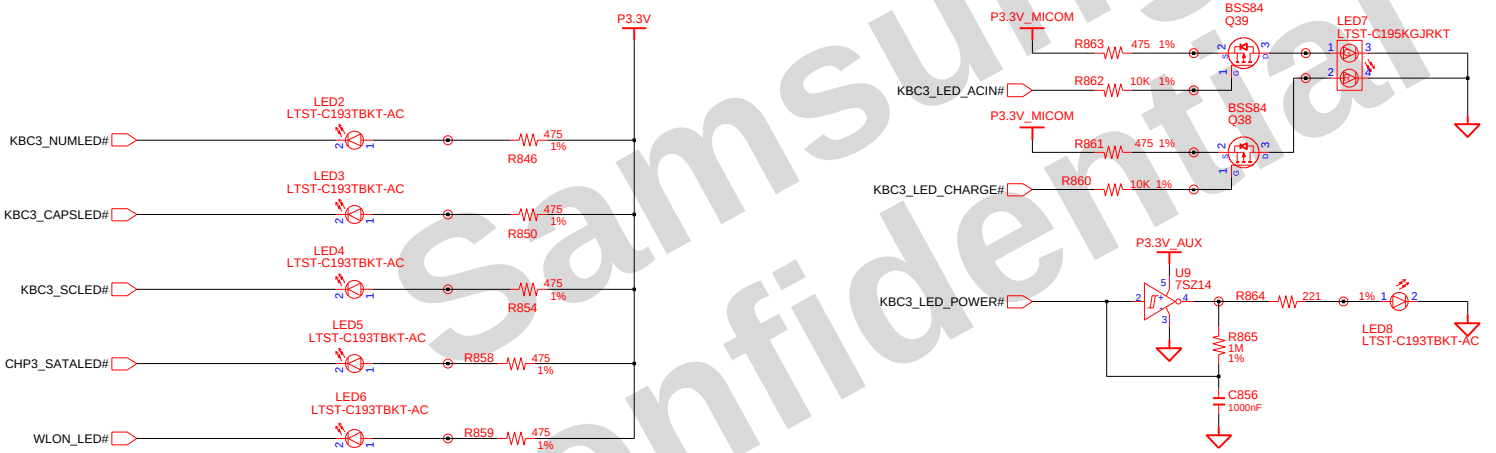


DRAW: MS YANG / Dany Lee	DATE: 8/12/2006	TITLE: OSL02 PWR_Switchbutton PWR_Switchbutton	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		
APPROVAL: MK KIM	REV: REV 1.1		PART NO.: BA41-00866A
MODULE CODE:	LAST EDIT: May 15, 2008 08:19:32 AM	PAGE 1 OF 1	



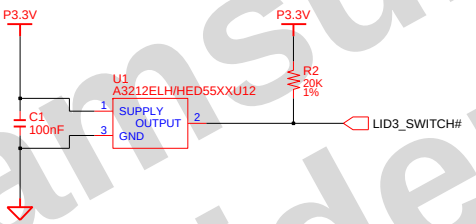
DRAW: MS YANG / Dany Lee	DATE: 8/12/2006	TITLE: OSL02 MIO_Switch MIO_Switch	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		
APPROVAL: MK KIM	REV: REV 1.1		PART NO.: BA41-00866A
MODULE CODE:	LAST EDIT: May 15, 2008 08:19:32 AM	PAGE 1 OF 1	

ADAPTERIN/CHARGING LED



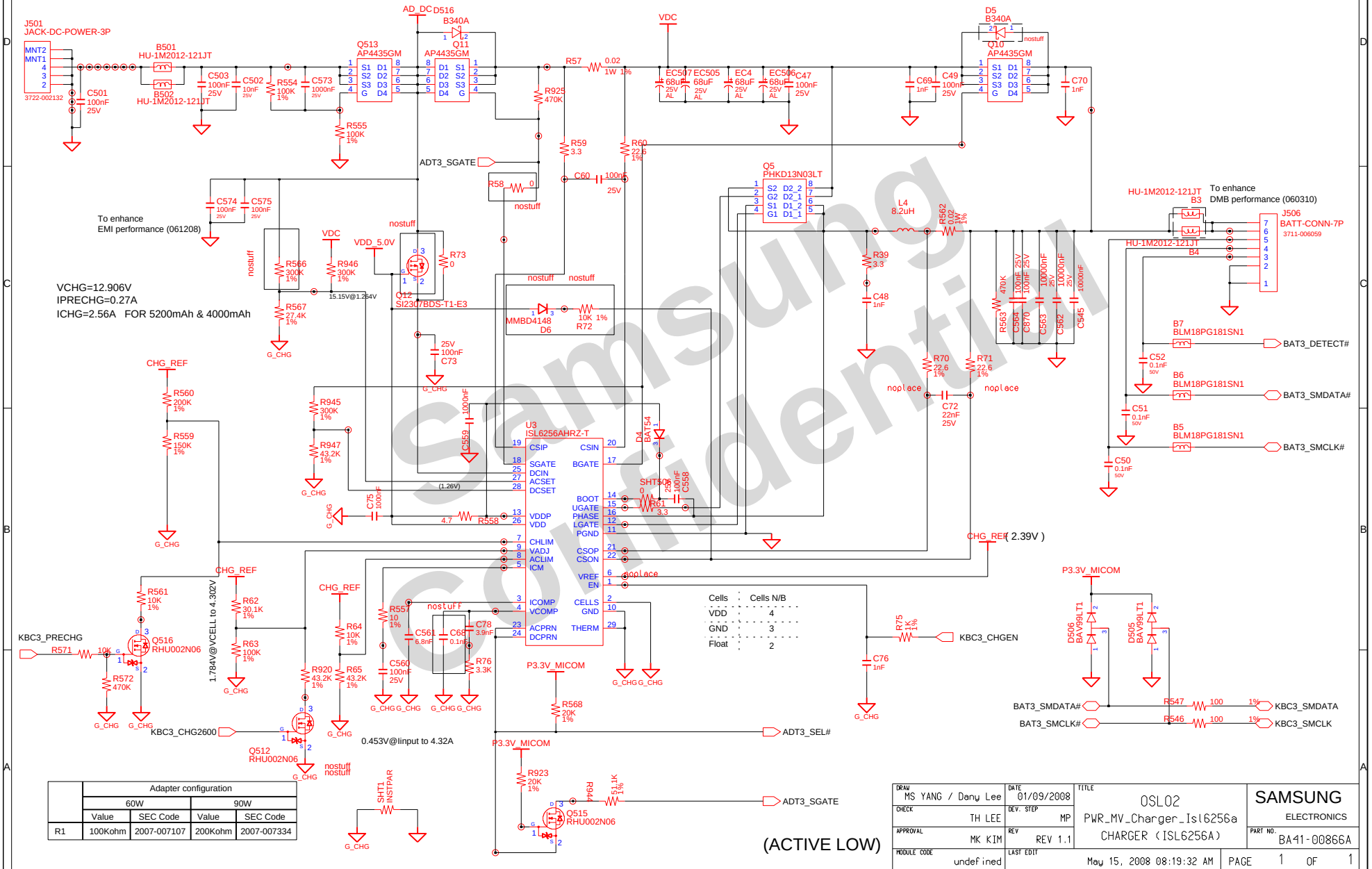
DRAW: MS YANG / Dany Lee	DATE: 8/12/2006	TITLE: OSL02 LED_Switch LED_Switch	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		
APPROVAL: MK KIM	REV: REV 1.1		PART NO.: BA41-00866A
MODULE CODE:	LAST EDIT: May 15, 2008 08:19:32 AM	PAGE 1 OF 1	

LID_SWITCH



DRAW: MS YANG / Dany Lee	DATE: 8/12/2006	TITLE: OSL02 LID_Switch LID_Switch	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		
APPROVAL: MK KIM	REV: REV 1.1		PART NO.: BA41-00866A
MODULE CODE:	LAST EDIT: May 15, 2008 08:19:32 AM	PAGE 1 OF 1	

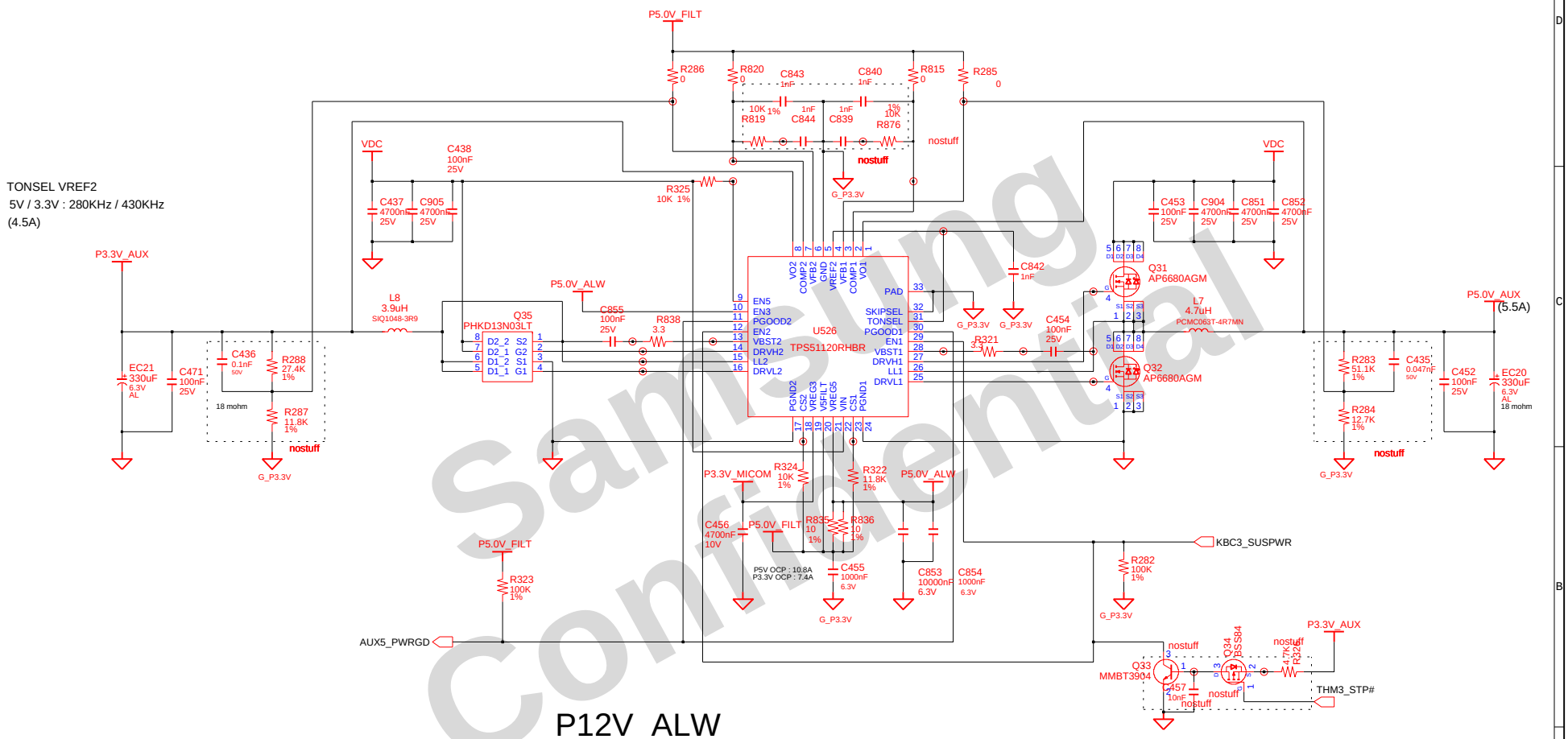
CHARGER & POWER MANAGEMENT



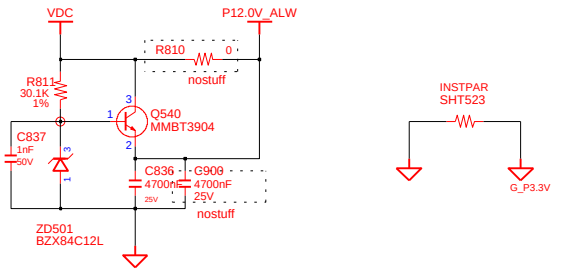
	Adapter configuration			
	60W		90W	
	Value	SEC Code	Value	SEC Code
R1	100Kohm	2007-007107	200Kohm	2007-007334

DRAW: MS YANG / Dany Lee	DATE: 01/09/2008	TITLE: OSL02 PWR_MV_Charger_Isl6256a CHARGER (ISL6256A)	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		PART NO.: BA41-00866A
APPROVAL: MK KIM	REV: REV 1.1		
MODULE CODE: undefined	LAST EDIT: May 15, 2008 08:19:32 AM	PAGE 1 OF 1	

P3.3V_AUX & P5.0V_AUX



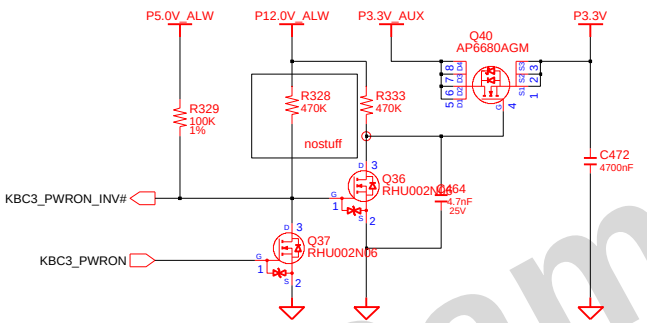
P12V_ALW



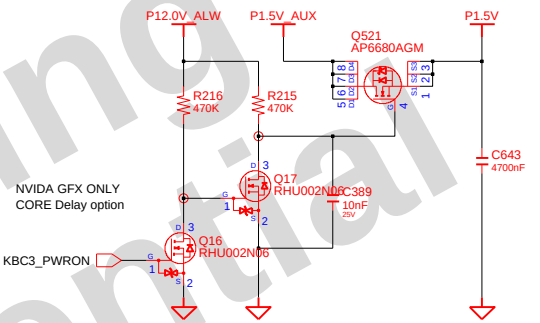
DRAW: MS YANG / Dany Lee	DATE: 11/8/2006	TITLE: OSLO2 PWR_MV_3V_5V P3.3V_AUX / P5.0V_AUX	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		
APPROVAL: MK KIM	REV: REV 1.1		PART NO.: BA41-00866A
MODULE CODE: undefined	LAST EDIT: May 15, 2008 08:19:32 AM		PAGE 1 OF 1

Switched Power

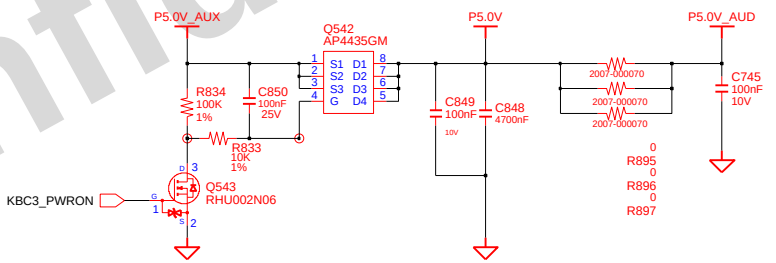
Switched Power On (P3.3V)



Switched Power On (P1.5V)

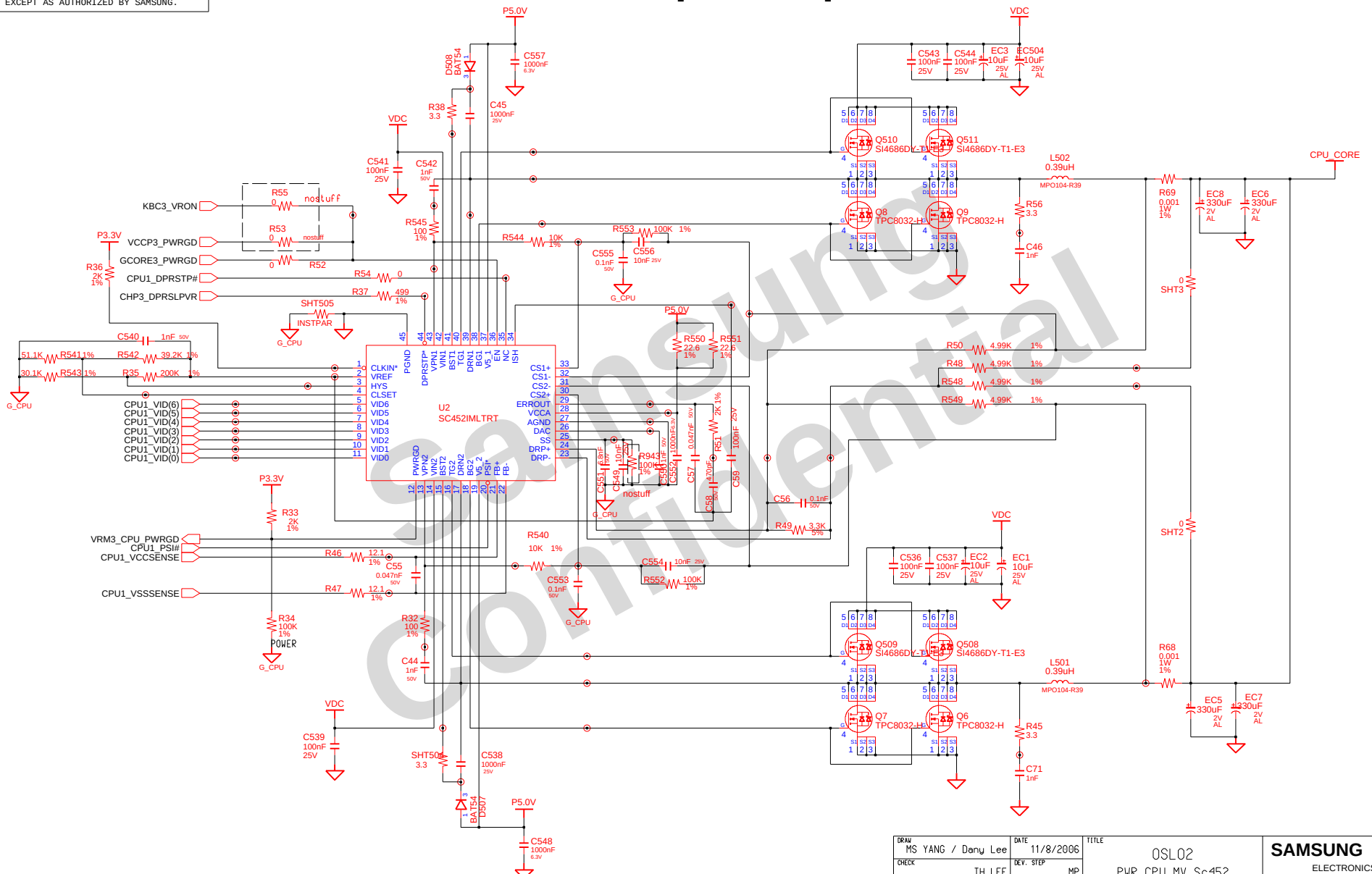


Switched Power On (P5.0V)



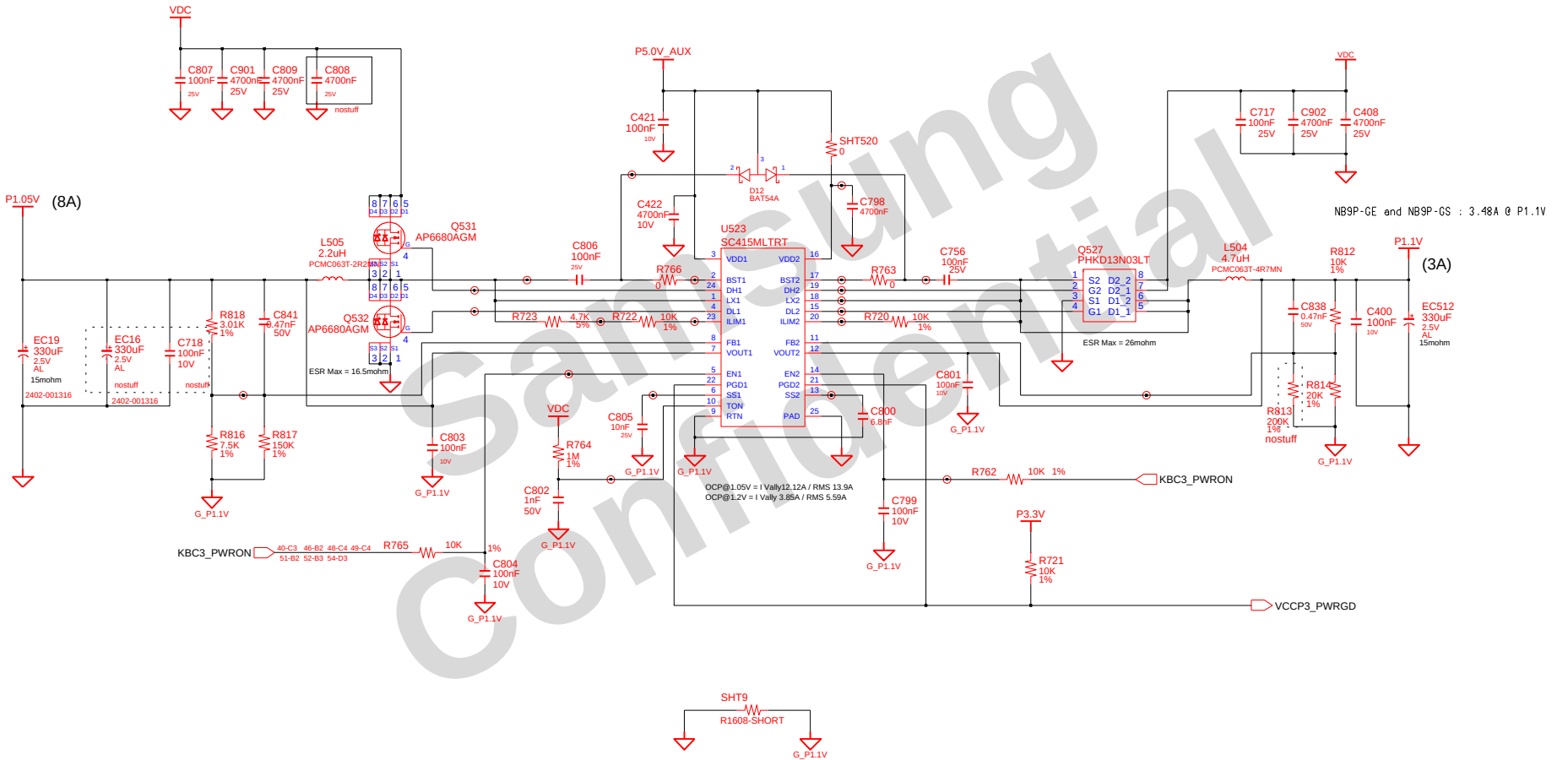
DRAW: MS YANG / Dany Lee	DATE: 01/09/2008	TITLE: OSLO2 PWR_MV_Switched SWITCHED POWER	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		PART NO.: BA41-00866A
APPROVAL: MK KIM	REV: REV 1.1		
MODULE CODE:	LAST EDIT: May 15, 2008 08:19:32 AM	PAGE 1 OF 1	

CPU VRM [SEMTECH]



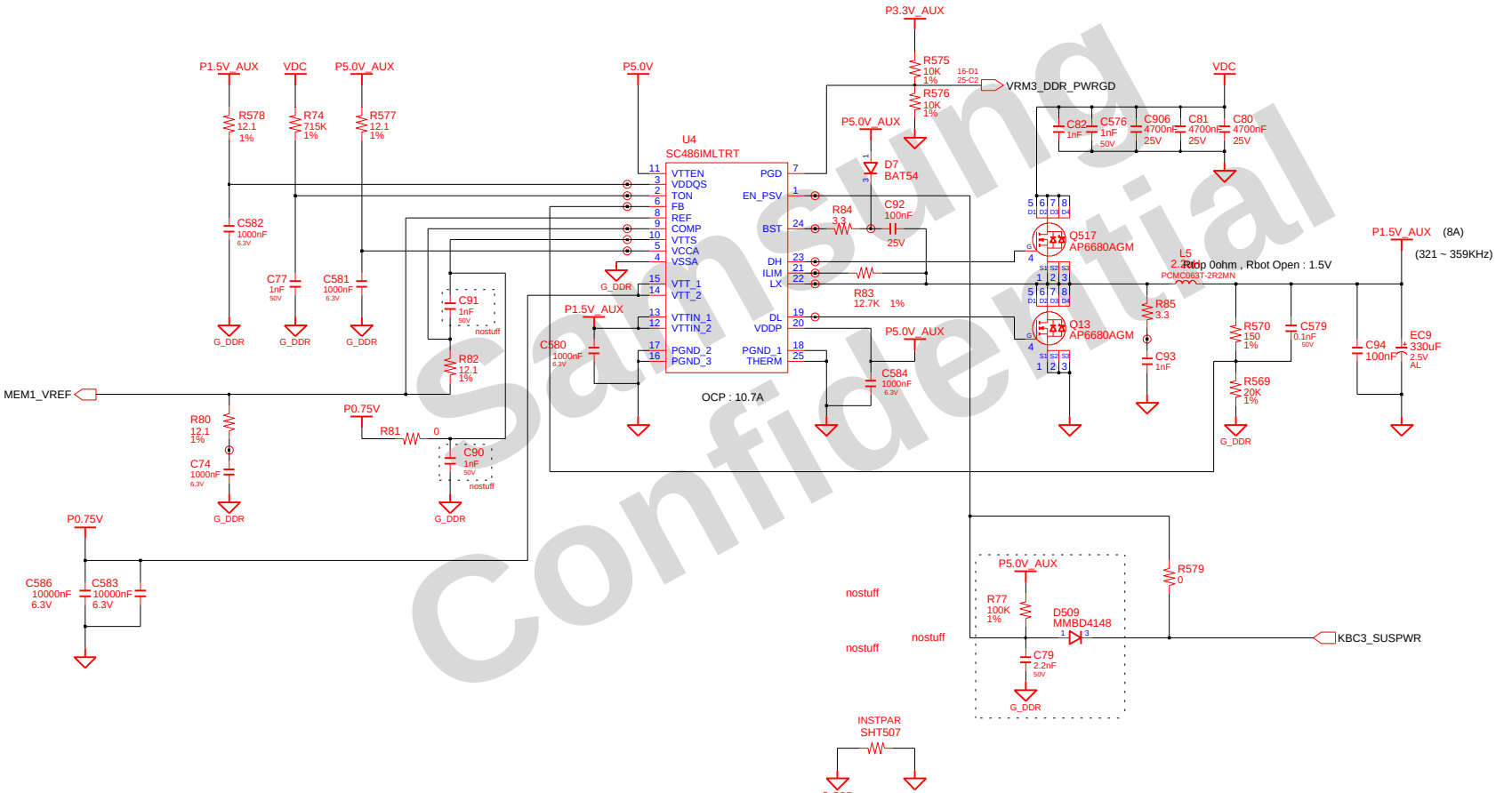
DRAW: MS YANG / Dany Lee	DATE: 11/8/2006	TITLE: OSLO2 PWR_CPU_MV_Sc452 CPUI VRM (IMVP6+)	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		
APPROVAL: MK KIM	REV: REV 1.1		PART NO.: BA41-00866A
MODULE CODE: undefined	LAST EDIT: May 15, 2008 08:19:32 AM		PAGE 1 OF 1

CHIPSET POWER(P1.05V & P1.1V)



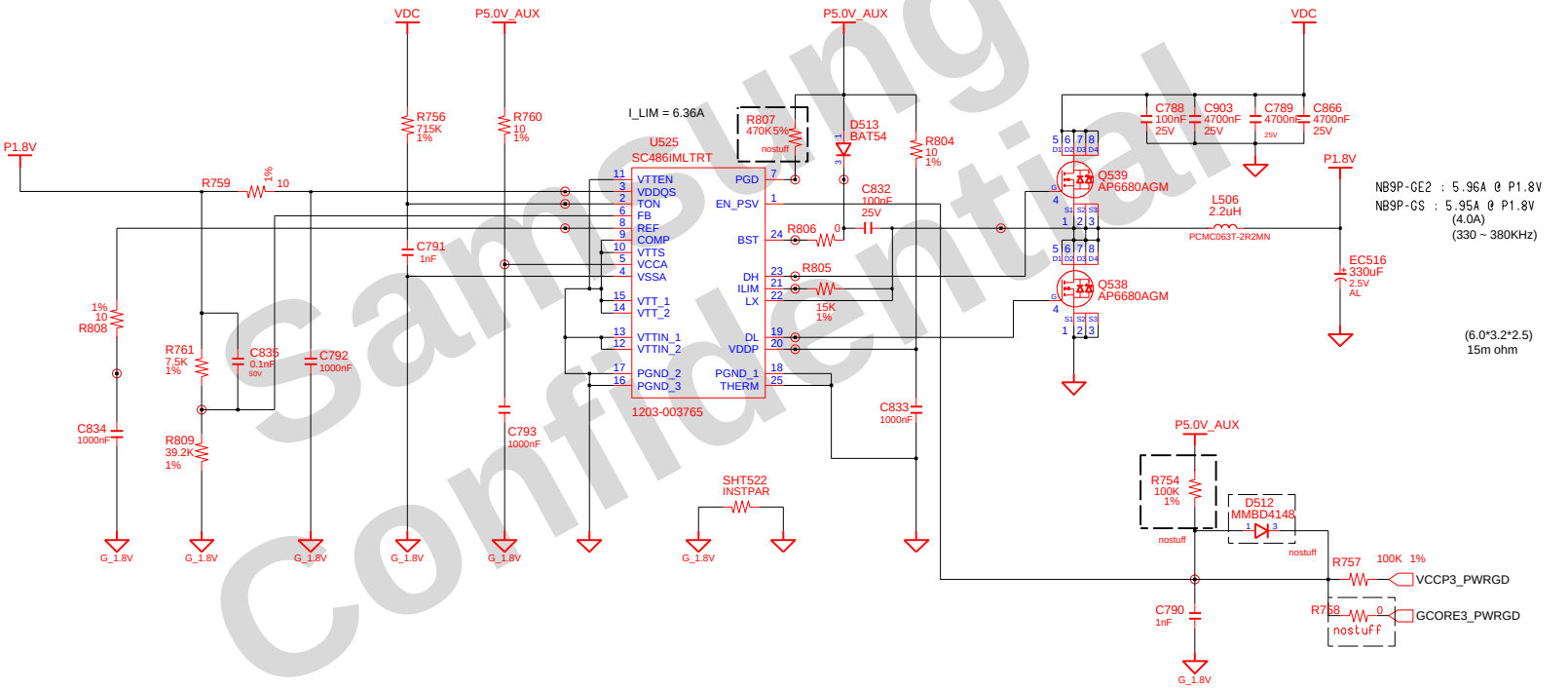
DRAW: MS YANG / Dany Lee	DATE: 8/14/2007	TITLE: OSL02 PWR_MV_Cantiga Chipset Power (P1.05V_M,P1.2V)	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		
APPROVAL: MK KIM	REV: REV 1.0		PART NO.: BA41-00866A
MODULE CODE: undefined	LAST EDIT: May 15, 2008 08:19:32 AM		PAGE 1 OF 1

DDR3 Power



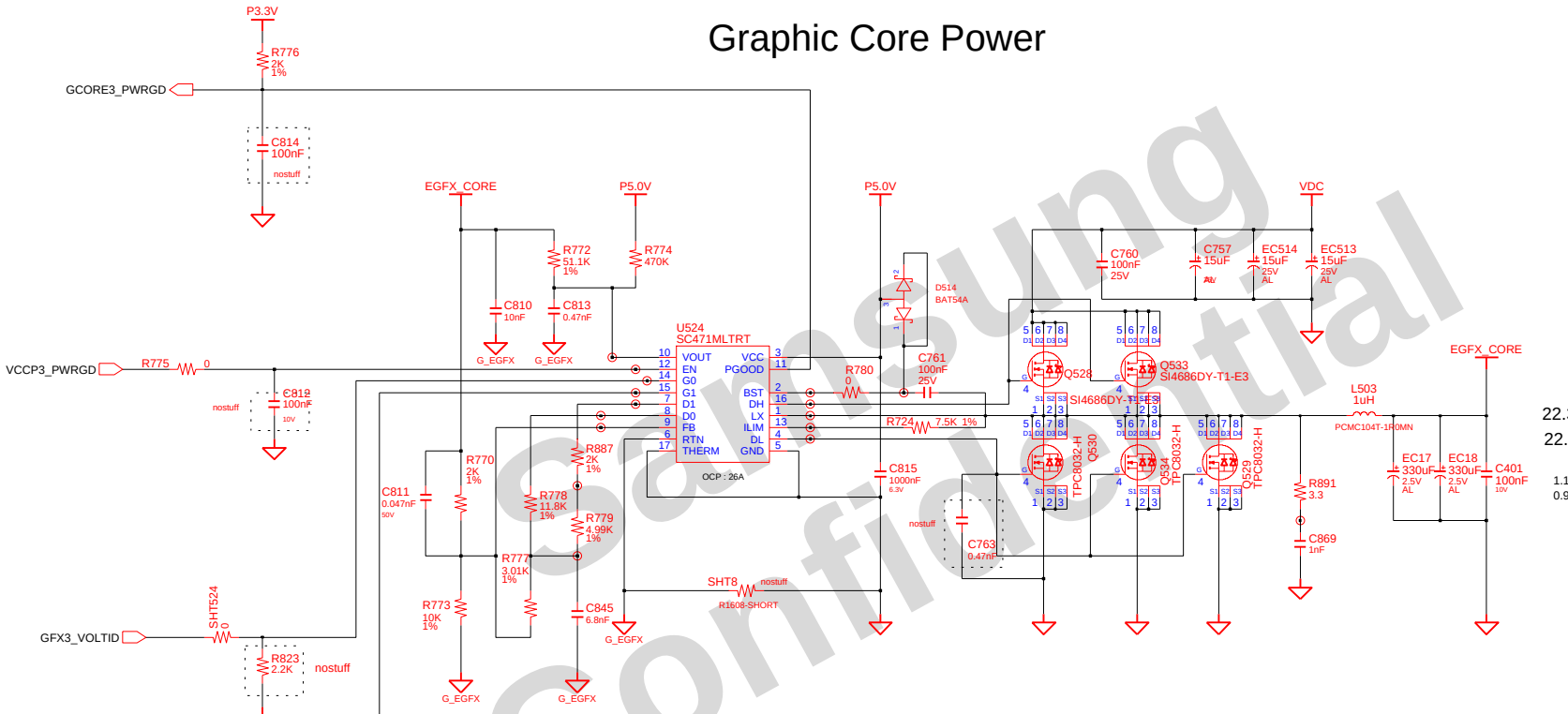
DRAW: MS YANG / Dany Lee	DATE: 11/8/2006	TITLE: OSLO2 PWR_MV_MeMory DDR3 POWER (P1.5V_AUX)	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		
APPROVAL: MK KIM	REV: REV 1.1		PART NO.: BA41-00866A
MODULE CODE: undefined	LAST EDIT: May 15, 2008 08:19:32 AM		PAGE 1 OF 1

P1.8V (External Gfx Memory)



DRAW: MS YANG / Dany Lee	DATE: 8/14/2007	TITLE: OSLO2 PWR_Gfx_MV_Ext Ext Gfx Memory(SC486)	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		
APPROVAL: MK KIM	REV: REV 1.1		PART NO.: BA41-00866A
MODULE CODE:	LAST EDIT: May 15, 2008 08:19:32 AM		PAGE 1 OF 2

Graphic Core Power



22.38 A @ NB9P-GE2 / GDDR3
22.89 A @ NB9P-GS / GDDR3

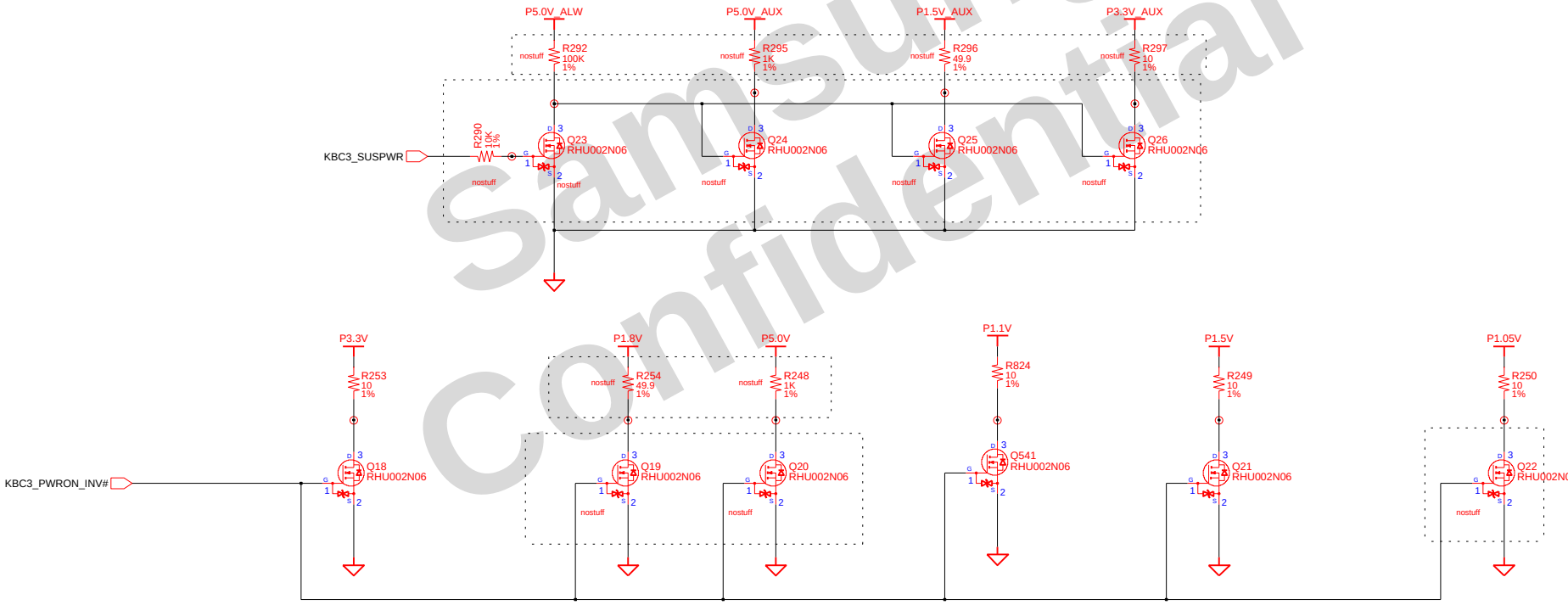
1.1V (1.125V) @ 207KHz
0.95V (0.959V) @ 222KHz

Location	Value	VID0	VID1	SPEC	RESULT
R770	2 K	0	0	0.89 V	0.9000
R778	11.8K	1	0	1.00 V	1.0013
R777	3.01 K	0	1	1.05 V	1.0500
R773	10 K	1	1	Reserved	1.1027
R779	6.99 K				

Location	Value	VID0	VID1	SPEC	RESULT
R770		0	0		
R778		1	0		
R777		0	1		
R773		1	1		
R779					

DRAW: MS YANG / Dany Lee	DATE: 8/14/2007	TITLE: OSLO2 PWR_Gfx_MV_Ext Ext Gfx Core(SC471)	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		
APPROVAL: MK KIM	REV: REV 1.1		PART NO.: BA41-00866A
MODULE CODE:	LAST EDIT: May 15, 2008 08:19:32 AM	PAGE 2 OF 2	

POWER DISCHARGER



DRAW: MS YANG / Dany Lee	DATE: 8/14/2007	TITLE: OSL02 PWR_MV_DisCharger DISCHARGING LOGIC	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		
APPROVAL: MK KIM	REV: REV 1.1		PART NO.: BA41-00866A
MODULE CODE: undefined	LAST EDIT: May 15, 2008 08:19:32 AM		PAGE 1 OF 1

MT15 RMNT-32-80-1P
MT16 RMNT-32-80-1P
MT1 RMNT-32-80-1P
MT3 RMNT-25-65-1P
MT501 RMNT-32-80-1P
MT4 RMNT-32-80-1P
MT13 RMNT-32-90-1P
Place it near the MDC
32,90

For KBD support
MT6 RMNT-25-80-1P
MT11 RMNT-25-80-1P

C572 0.033nF
C571 0.0033nF
C568 0.018nF
C570 0.047nF
C567 0.1nF
C566 0.01nF 0.5pF
C569 0.007nF 50V 0.5pF
C67 0.033nF
C66 0.0033nF
C63 0.018nF
C65 0.047nF
C62 0.1nF
C61 0.01nF 0.5pF
C64 0.007nF 50V 0.5pF

MT2009 RMNT-25-60-1P
MT2000 RMNT-25-60-1P
25,60

MT14 RMNT-32-100-1P
MT2 RMNT-32-100-1P
32,100
MT12 RMNT-32-100-1P
MT5 RMNT-25-45-1P

M2 HEAD DIA LENGTH
M1 HEAD DIA LENGTH
For GFX PEM

REV1
1 no place 2 3

PCB REVISION CONTROL (ICT)				
NO	CONNECTION	DATE(YY/MM/DD)	REVISION	STEP
1	N.C.			
2	1-2			
3	2-3			
4	3-1			
5	1-2-3			
6	N.C.			
7	1-2			
8	2-3			
9	3-1			
10	1-2-3			

ICT PORT

J512 HDR-10P-1R-SMD
VDC P1.05V P1.8V P1.1V P1.5V
POWER
AUX5_PWRGD
R802 1K 1%
R803 1K 1%
VRM3_CPU_PWRGD
CPU1_PWRGDCPU
CPU1_CPURST#
MNT1 MNT2

DRAW: MS YANG / Dany Lee	DATE: 11/23/2007	TITLE: OSL02 UNDEFINED	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		
APPROVAL: MK KIM	REV: REV 1.1		PART NO.: BA41-00866A
MODULE CODE:	LAST EDIT: May 15, 2008 08:19:32 AM	PAGE 12 OF 13	

AUD3_BEEP
AUD3_GPIO0#
AUD3_GPIO1#
AUD3_SHDN#
AUD3_SPDIF_OUT
AUD3_SPKR
AUD5_HP_O_LEFT
AUD5_HP_O_RIGHT
AUD5_LINE_O_LEFT
AUD5_LINE_O_RIGHT
AUD5_MIC1_LEFT
AUD5_MIC1_RIGHT
AUD5_MIC1_VREF_LEFT
AUD5_MIC1_VREF_RIGHT
AUD5_MIC2_LEFT
AUD5_MIC2_RIGHT
AUD5_MIC2_VREF
AUD5_SENS_A
AUD5_SENS_HP#
AUD5_SENS_MIC#
AUX5_PWRGD

BAT3_DETECT#
BAT3_SMCLK#
BAT3_SMDATA#

CHP3_BIOSWP#
CHP3_BIOS_CRI#
CHP3_CL_CLK_0
CHP3_CL_DATA_0
CHP3_DPRSLPVR
CHP3_GPIO18
CHP3_GPIO20
CHP3_INTRUDER#
CHP3_ME_RTCRST#
CHP3_PCISTP#
CHP3_PM_SYNC#
CHP3_RTCRST#
CHP3_SATACLKREQ#
CHP3_SATALED#
CHP3_SERIRQ

CLK3_DBGLPC
CLK3_FM48
CLK3_GFX_27M
CLK3_GFX_27M_SS
CLK3_ICH14
CLK3_PCLKICH
CLK3_PCLKMICOM
CLK3_USB48

CPU1_A20M#
CPU1_FERR#
CPU1_IGNNE#
CPU1_INIT#
CPU1_INTR
CPU1_NMI
CPU1_PSI#
CPU1_SMI#
CPU1_TCK
CPU1_TDI
CPU1_TDO
CPU1_THRMTRIP#
CPU1_TMS
CPU1_TRST#
CPU1_VCCSENSE
CPU1_VSSSENSE
CPU2_THERMDA
CPU2_THERMDC
CPU3_THRMTRIP#
CRT3_DDCCLK
CRT3_DDCDATA
CRT3_HSYNC
CRT3_VSYNC
CRT5_DDCCLK

CRT5_DDCDATA
CRT5_HSYNC
CRT5_VSYNC

EXP3_CLKREQ#
EXP3_CPPE#
EXP3_CPUSB#
EXP3_PERST#
FAN3_FDBACK#
FAN5_VDD
GCORE3_PWRGD

GFX3_HCLK
GFX3_HDATA
GFX3_STRAP0
GFX3_STRAP1
GFX3_STRAP2
GFX3_THERM#
GFX3_THERMDN
GFX3_THERMDP
GFX3_VOLTID

HDA3_AUD_BCLK
HDA3_AUD_RST#
HDA3_AUD_SDIO
HDA3_AUD_SDO
HDA3_AUD_SYNC
HDA3_HDMI_BCLK
HDA3_HDMI_RST#
HDA3_HDMI_SDI2
HDA3_HDMI_SDO
HDA3_HDMI_SYNC
HDA3_MDC_BCLK
HDA3_MDC_RST#
HDA3_MDC_SDI1
HDA3_MDC_SDO
HDA3_MDC_SYNC

ITP3_DBRRESET#

KBC3_BKLTON
KBC3_BLCKPWRSW#
KBC3_CAPSLED#
KBC3_CHGEN
KBC3_EXTSMI#
KBC3_LED_ACIN#
KBC3_LED_CHARGE#
KBC3_LED_POWER#
KBC3_NUMLED#
KBC3_PWRBTN#
KBC3_PWRON_INV#
KBC3_PWRSW#
KBC3_RFOFF#
KBC3_RST#
KBC3_RUNSCI#
KBC3_SCLED#
KBC3_SMCLK
KBC3_SMDATA
KBC3_SPKMUTE
KBC3_THERM_SMCLK
KBC3_THERM_SMDATA
KBC3_WAKESCI#
KBC5_KSI(0)
KBC5_KSI(1)
KBC5_KSI(2)
KBC5_KSI(3)
KBC5_KSI(4)
KBC5_KSI(5)
KBC5_KSI(6)
KBC5_KSI(7)
KBC5_KSO(0)
KBC5_KSO(1)
KBC5_KSO(10)
KBC5_KSO(11)
KBC5_KSO(12)
KBC5_KSO(13)
KBC5_KSO(14)
KBC5_KSO(15)
KBC5_KSO(2)
KBC5_KSO(3)
KBC5_KSO(4)
KBC5_KSO(5)
KBC5_KSO(6)
KBC5_KSO(7)

KBC5_KSO(8)
KBC5_KSO(9)
KBC5_ICLK
KBC5_IDATA
LAN3_ACTLED#
LAN3_LINK1000#
LAN3_LINK10_100#
LAN3_VPDCLK
LAN3_VPDDATA

LCD3_BKLTON
LCD3_BRIT
LCD3_EDID_CLK
LCD3_EDID_DATA
LID3_SWITCH#
LOM3_CLKREQ#
LPC3_LAD(0)
LPC3_LAD(1)
LPC3_LAD(2)
LPC3_LAD(3)
LPC3_LFRAME#

MCH1_HVREF
MCH1_HXSWING
MCH3_CLKREQ#
MCH3_DDR_RST#
MCH3_EXITS0#
MCH3_EXITS1#
MCH3_ICHSYNC#
MCH3_LCTRL_C
MCH3_LCTRL_D

SMB3_ALERT#
SMB3_CLK
SMB3_DATA
SPI3_CLK
SPI3_CS0#
SPI3_MISO
SPI3_MOSI
SPK5_L+
SPK5_L-
SPK5_R+
SPK5_R-
THM3_ALERT#
THM3_STP#
T_L_BUTTON#
T_R_BUTTON#

MEM1_VREF
MIN3_CLKREQ#
MIO3_BUTTON#

PEG3_BKLTEN
PEG3_HDMI_CLK
PEG3_HDMI_DATA
PEG3_HPD_HDMI
PEG3_LCDVDDON

PEX3_WAKE#
PLT3_RST#
PLT3_RST_ORG#

WLON_LED#

VCCP3_PWRGD
VRM3_DDR_PWRGD

PCI3_CLKRUN#

VDC
VDC
VDC
VDC
VDC

VDC_INV
VDC_INV
VCC_CRT
VCC_CRT

P12.0V_ALW
P12.0V_ALW

P5.0V_ALW
P5.0V_ALW
P5.0V_ALW

P5.0V_AMP
P5.0V_AMP

P5.0V
P5.0V
P5.0V
P5.0V
P5.0V

P5.0V_AUD
P5.0V_AUD

P5.0V_AUX
P5.0V_AUX
P5.0V_AUX
P5.0V_AUX
P5.0V_AUX

P5.0V_FILT

P4.75V_AUD
P4.75V_AUD

P3.3V_VDD

P3.3V_EXP
P3.3V_EXP

P3.3V_MCD

P3.3V_MICOM
P3.3V_MICOM
P3.3V_MICOM
P3.3V_MICOM
P3.3V_MICOM
P3.3V_MIOA_VDDQ
P3.3V_MIOA_VDDQ

PRTC_BAT
PRTC_BAT

P3.3V
P3.3V
P3.3V
P3.3V
P3.3V
P3.3V_AUX_EXP

P3.3V_DACA

G_P3.3V

LCD_VDD3V
LCD_VDD3V

G_1.8V

P1.8V
P1.8V
P1.8V
P1.8V
P1.8V
P1.8V_FBVDDQ
P1.8V_FBVDDQ

P1.8V_IFPAB_PLL

P1.8V_IFPEF_PLL
P1.8V_P2.5V_LAN
P1.8V_P2.5V_LAN

P1.5V
P1.5V
P1.5V
P1.5V
P1.5V
P1.5V_AUX
P1.5V_AUX
P1.5V_AUX
P1.5V_AUX
P1.5V_AUX
P1.5V_EXP

P1.2V_LAN
P1.2V_LAN

P1.1V
P1.1V

P1.1V_IFPEF_VDD

P1.1V_PEXIO_VDD
P1.1V_PEXIO_VDD

P1.1V_PLLVDD
P1.1V_PLLVDD

P1.05V
P1.05V

0.7VDDQA
0.7VDDQC

CPU_CORE
CPU_CORE

AD_DC
AD_DC
AD_DC
AD_DC
AD_DC
CHG_REF

FB_PLLVDDQ

EGFX_CORE
EGFX_CORE

PEX_PLLVDD

G_AUD
G_AUD
G_AUD
G_AUD
G_AUD
G_CHG
G_CHG

G_DDR
G_DDR

G_EGFX

G_MIC
G_MIC

G_P1.1V

GROUND
GROUND
GROUND
GROUND
GROUND
GROUND
GROUND
GROUND
GROUND
GROUND

TP21801 P0.75V
TP21802 VDD_5.0V

TP21803 ADT3_SEL#
TP21804 CHP3_USBPWRON#
TP21798 ITM3_CLKREQ#
TP21799 KBC3_PRECHG
TP21800 KBC3_USBPWRON#

KBC3_CHG2600
MCD3_SDDATA0
MCD3_SDDATA1
MCD3_SDDATA2
MCD3_SDDATA3
MCD3_XDDATA0
MCD3_XDDATA1
MCD3_XDDATA2
MCD3_XDDATA3
MCD3_XDDATA4
MCD3_XDDATA5
MCD3_XDDATA6
MCD3_XDDATA7
MCD3_MSDATA2_SDWP
MCD3_MSDATA1_XDWP#
MCD3_MSDATA3_XDRB#
MCD3_SDCLK_MSBS
MCD3_XDCLE_MSCLK
MCD3_MSINS#
MCD3_SDCD#
MCD3_XDALE
MCD3_XDCD#
MCD3_XDCE#

DESIGN: MS YANG / Dany Lee	DATE: 11/23/2007	TITLE: OSLO2 UNDEFINED	SAMSUNG ELECTRONICS
CHECK: TH LEE	DEV. STEP: MP		
APPROVAL: MK KIM	REV: REV 1.1		PART NO.: BA41-00866A
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