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# GENEVA

CPU : MEROM  
 Chip Set : SANTAROSA CHIPSET  
 Remarks : Mobility Platform

Model Name : GENEVA  
 PBA Name : MAIN  
 PCB Code : BA41-XXXXX  
 Dev. Step : PV2  
 Revision : 1.0  
 T.R. Date :

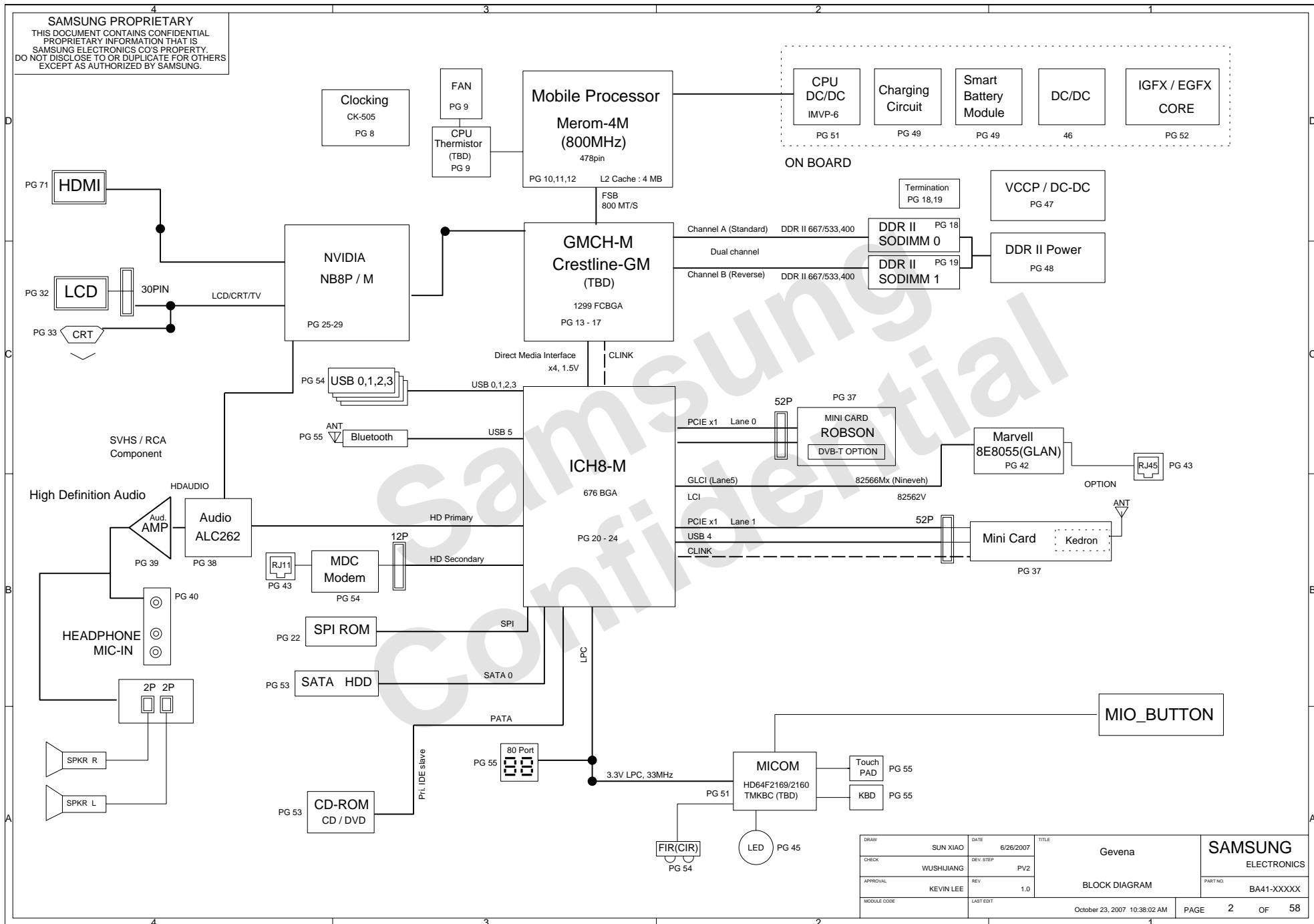
DRAW	CHECK	APPROVAL

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DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Geneva	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-XXXXX
CHECK	WUSHUIJANG	DEV STEP	PV2	MILAN		
APPROVAL	KEVIN LEE	REV	1.0	COVER		
MODULE CODE		LAST EDIT	October 23, 2007 10:38:02 AM	PAGE 1 OF 58		

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CHECK	WUSHUJIANG	DEV STEP	PV2				
APPROVAL	KEVIN LEE	REV	1.0		BLOCK DIAGRAM	PART NO. BA41-XXXXX	
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# BOARD INFORMATION

## SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

### PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
Cardbus	AD25	3	B,C,D
DT PCI SLOT	AD22	1	B,C,D,C
MiniPCI SLOT	AD23	2	A,B
USB	AD29(internal)	-	USB2.0 #0 (USB0) : A USB2.0 #1 (USB1) : D USB2.0 #2 (USB4) : C USB2.0 #3 (USB5) : E USB2.0 #4 (EHCI) : H
Hub to PCI	AD30(internal)	-	-
LPC bridge/IDE/AC97/SMBUS	AD31(internal)	-	B
Internal MAC	AD24(internal)	-	E
AC Link	-	-	B
GLAN	-	-	F

### Voltage Rails

VDC	Primary DC system power supply (7 to 21V)
VCC_CORE	Core Voltage for CPU
MCH_CORE	Core Voltage for CPU
ICH_CORE	Core Voltage for CPU
P1.05V (VCCP)	VTT for CPU, Crestline & ICH8-M
P1.05V_M	1.05V switched power rail for ME (on in M0/M1)
P1.25V_M	1.25V switched power rail for ME (on in M0/M1)
P3.3V_M	3.3V switched power rail for ME (on in M0/M1)
P3.3V_A	3.3V always power rail (by KBC3_ALWS_ON)
MICOM_P3V	3.3V always power rail (for Micom)
LAN_3.3V	3.3V always power rail (for LAN)
P1.5V	1.5V switched off power rail (off in S3-S5)
P1.5V_AUX	1.5V switched on power rail
P2.5V	2.5V switched off power rail (off in S3-S5)
P1.8V	1.8V switched off power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail for DDR
P0.9V	0.9V power rail for DDR
P3.3V	3.3V switched off power rail (off in S3-S5)
P3.3V_AUX	3.3V switched on power rail
PSV	5.0V switched off power rail (off in S3-S5)
PSV_AUX	5.0V switched on power rail

### USB PORT Assign

PORT #	ASSIGNED TO
0	SYSTEM PORT 0
1	SYSTEM PORT 1
2	DMB
3	Expressas Card
4	DOCKING PORT 0
5	Bluetooth
6	Mini PCI Express
7	Aux Display
8	Test Port (RSVD)
9	WWAN/WIBRO (TBD)

### PCI Express Assign

PORT #	ASSIGNED TO
0	PCIe x1 Slot
1	Mini Card (Golan)
2	Mini Card (WIBRO : RSVD)
3	Expressas Card
4	DOCKING PORT 0
5	GLAN

### Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	ICH8-M	Real Time Clock
Crystal	10MHz	MICOM	HD84F2169/2160
Crystal	14.318MHz	CLOCK-Generator	CK-505
Crystal	24.576MHz	Cardbus Controller	1394
Crystal	25MHz	LAN	Intel LAN
Crystal	27MHz (TBD)	VIDEO	PEG
Crystal	24.576MHz (TBD)	HD Audio	Audio

### LCD Pannel Detect (TBD)

Devices	Resolution	PANNEL_DETECT_0

### I<sup>2</sup>C / SMB Address

Devices	Address	Hex	Bus
ICH8-m	Master	-	SMBUS Master
CPU Thermal Sensor	1001 110x	9Ch	Thermal Sensor
SODIMM0	1010 000x	A0h	-
SODIMM1	1010 010x	A4h	-
Thermal Sensor on SODIMM0	0011 000x	30h	-
Thermal Sensor on SODIMM1	0011 010x	34h	-
CK-505M (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable
DB400 (PCI Express Clocks)	1101 110x	DCh	Clock Buffer for PCI Express
TBD	0100 1100	4Ch	Thermal Sensor
TBD : (LVDS BackLight Inverter)	0101 1000	58h	-
TBD : (ALS)	0111 0010	72h	Ambient Light Sensor
TBD : (AUX DISPLAY)	0011 110x	3Ch	EMA
LAN	1100 1000	C8h	82566
PCI Express Docking	TBD	TBD	TBD
TPM	TBD	TBD	TBD

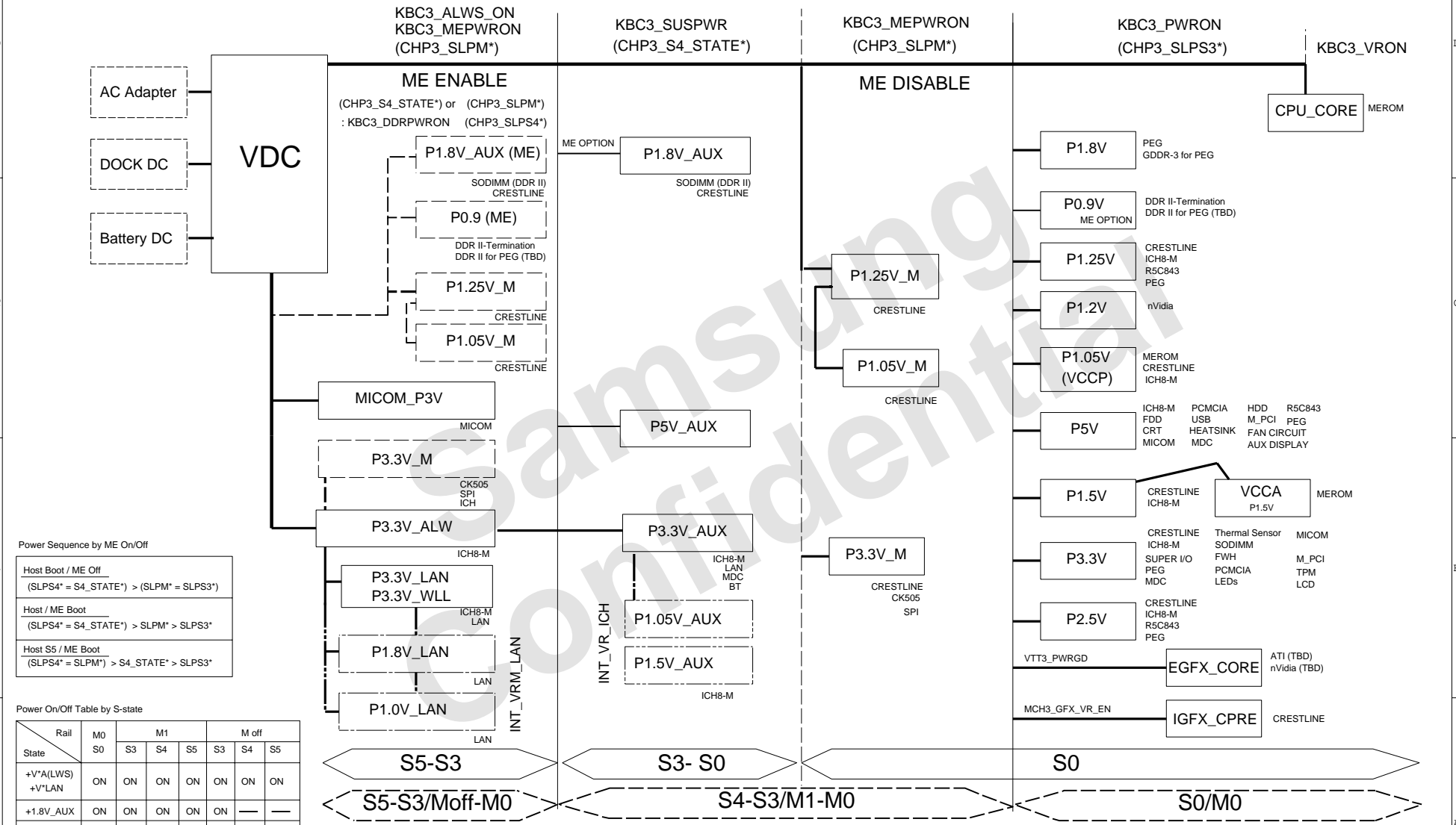
## REVISION HISTORY

See rev notes for more information.

DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Geneva	SAMSUNG
CHECK	WUSHUJIANG	DEV. STEP	PV2			ELECTRONICS
APPROVAL	KEVIN LEE	REV	1.0		BOARD INFO	PART NO. BA41-XXXXX
MODULE CODE		LAST EDIT		October 23, 2007 10:38:02 AM	PAGE	3 OF 58

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# POWER DIAGRAM



**Power Sequence by ME On/Off**

Host Boot / ME Off  
(SLPS4\* = S4\_STATE\*) > (SLPM\* = SLPS3\*)

Host / ME Boot  
(SLPS4\* = S4\_STATE\*) > SLPM\* > SLPS3\*

Host S5 / ME Boot  
(SLPS4\* = SLPM\*) > S4\_STATE\* > SLPS3\*

**Power On/Off Table by S-state**

Rail State	M0 S0	M1			M off		
		S3	S4	S5	S3	S4	S5
+V*(LWS)	ON	ON	ON	ON	ON	ON	ON
+V*LAN	ON	ON	ON	ON	ON	ON	ON
+1.8V_AUX	ON	ON	ON	ON	ON	---	---
+0.9V	ON	ON	ON	ON	---	---	---
+V*AUX	ON	ON	---	---	ON	---	---
+V* M	ON	ON	ON	ON	---	---	---
+V* (CORE)	ON	---	---	---	---	---	---

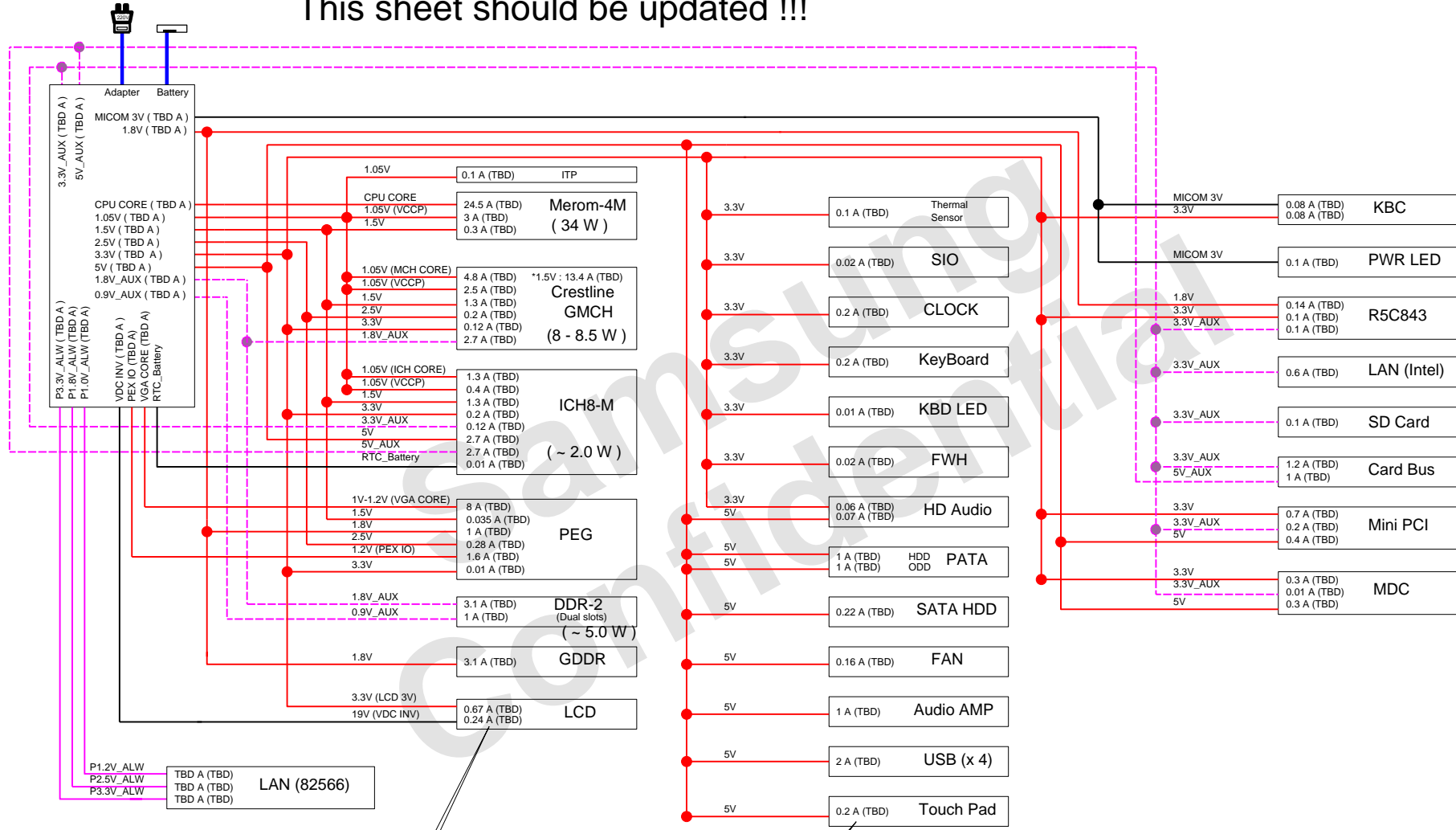
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CHECK	WUSHIJIANG	DEV. STEP	PV2	POWER DIAGRAM		
APPROVAL	KEVIN LEE	REV	1.0	October 23, 2007 10:38:02 AM		PART NO. BA41-XXXXX
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# POWER RAILS ANALYSIS

Rev. 0.5

This sheet should be updated !!!



Value by Datasheet/Application notes (Value by measurement)

DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena	SAMSUNG ELECTRONICS
CHECK	WUSHIJIANG	DEV. STEP	PV2			
APPROVAL	KEVIN LEE	REV	1.0		POWER RAILS	PART NO. BA41-XXXXX
MODULE CODE		LAST EDIT			October 23, 2007 10:38:02 AM	PAGE 5 OF 58

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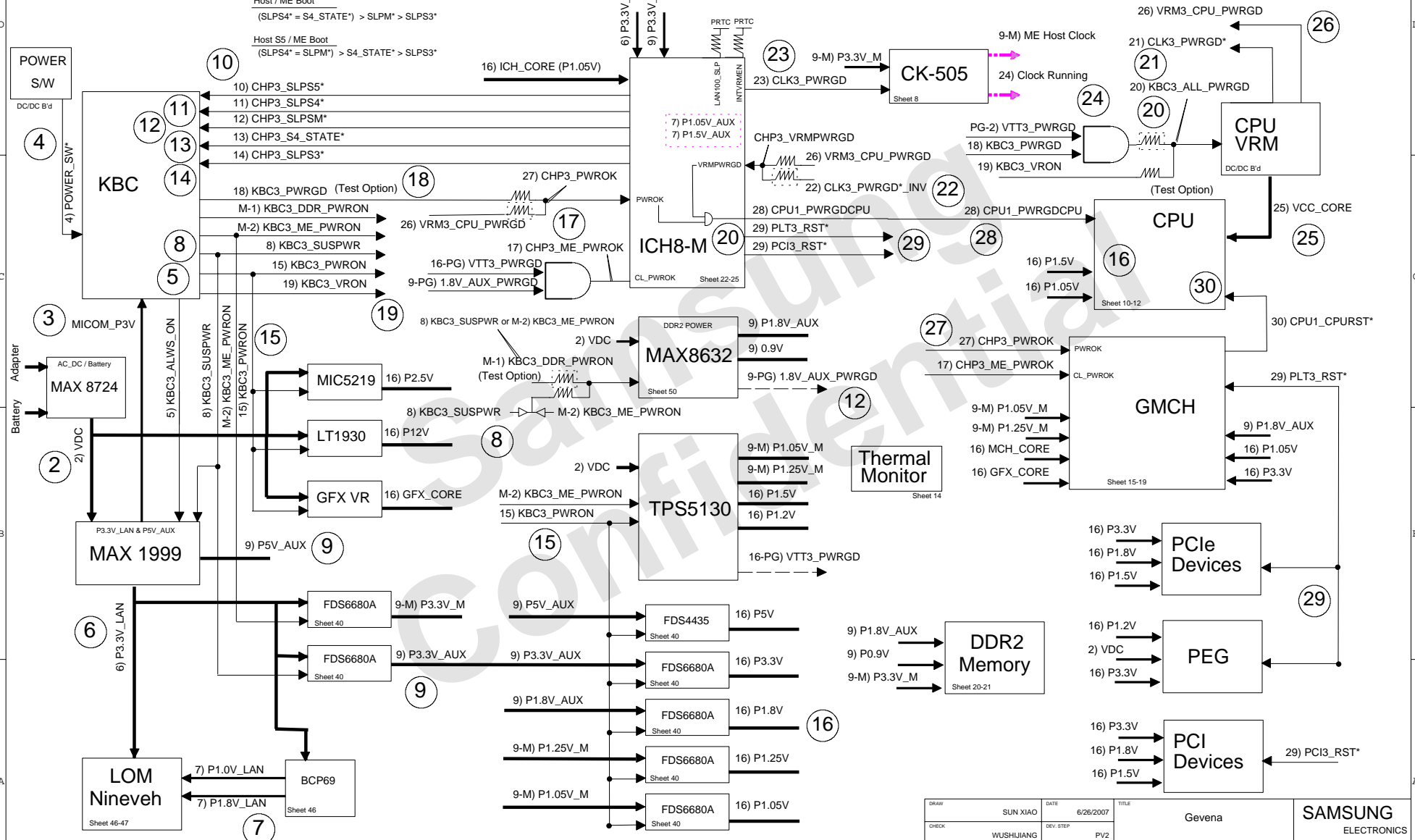
**TO BE UPDATED!!**

**POWER SEQUENCE** Rev. 0.5

Host Boot / ME Off  
 (SLPS4\* = S4\_STATE\*) > (SLPM\* = SLPS3\*)  
 M-1) KBC3\_DDR\_PWRON (TBD) = 8) KBC3\_SUSPWR  
 M-2) KBC3\_ME\_PWRON = 15) KBC3\_PWRON

Host / ME Boot  
 (SLPS4\* = S4\_STATE\*) > SLPM\* > SLPS3\*

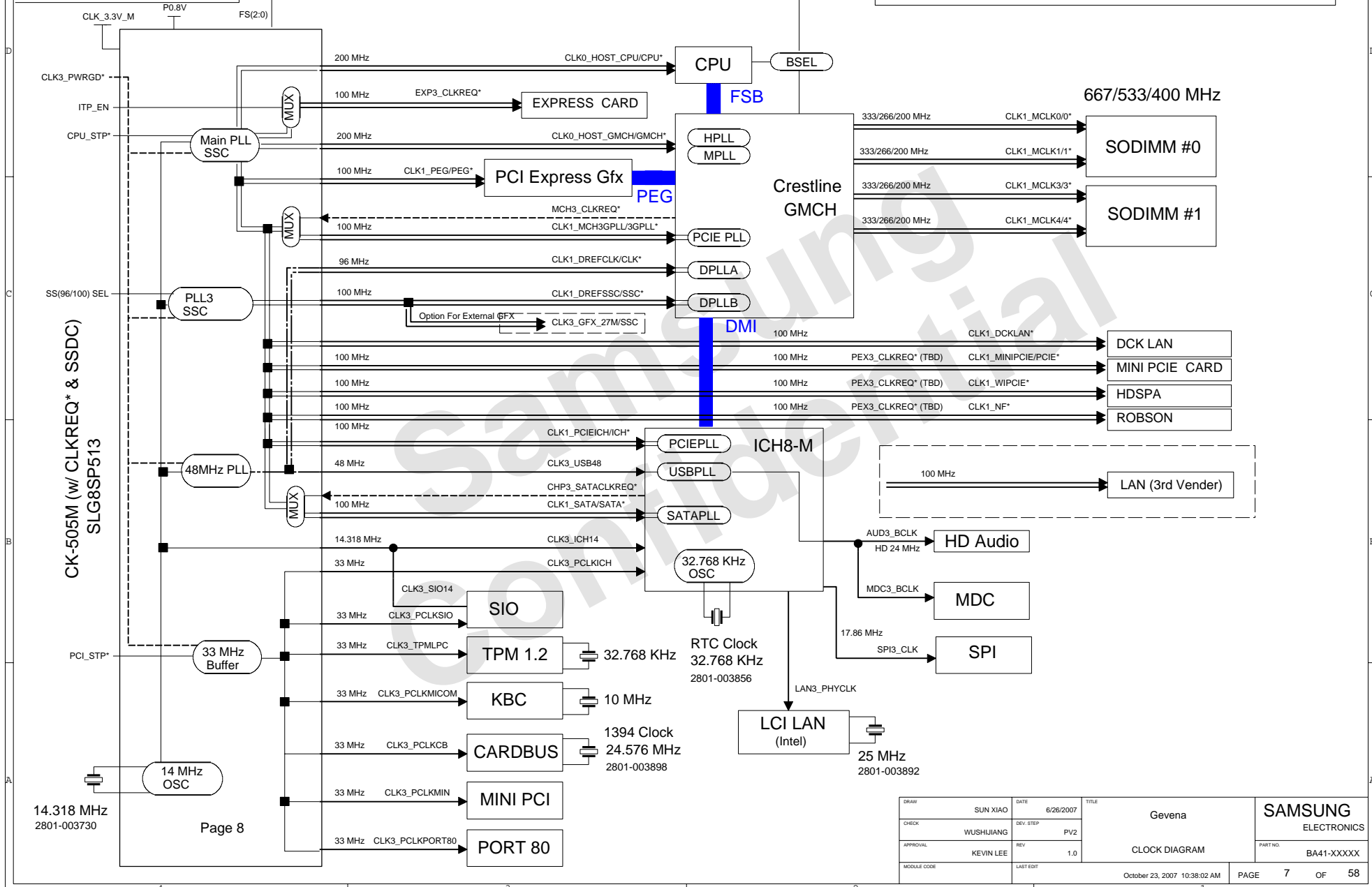
Host S5 / ME Boot  
 (SLPS4\* = SLPM\*) > S4\_STATE\* > SLPS3\*



DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena	<b>SAMSUNG</b> ELECTRONICS
CHECK	WUSHUJIANG	DEV. STEP	PV2			
APPROVAL	KEVIN LEE	REV	1.0		POWER SEQUENCE	PART NO. BA41-XXXXX
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# CLOCK DISTRIBUTION Rev. 0.8



CK-505M (w/ CLKREQ\* & SSDC) SLG8SP513

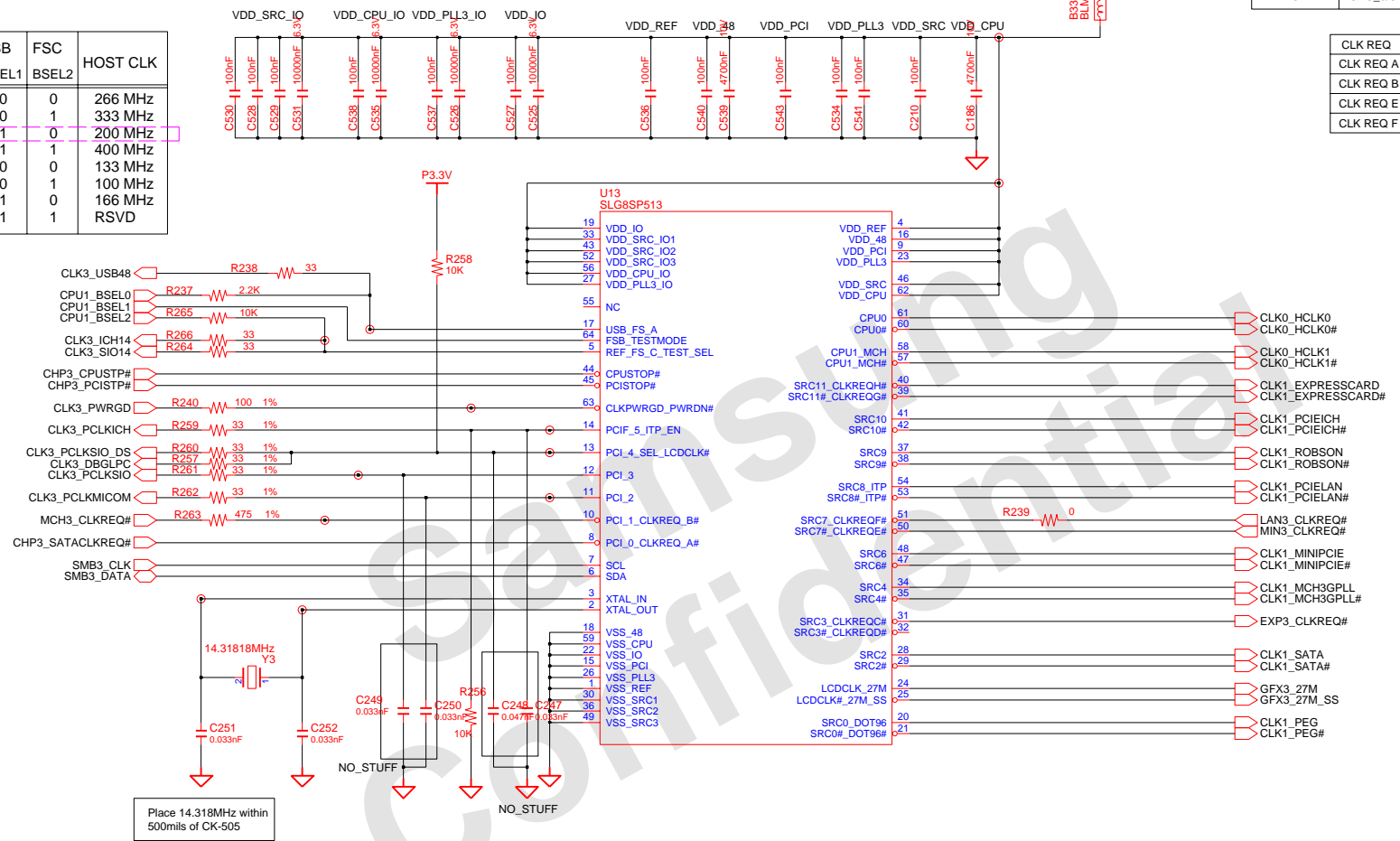
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CHECK	WUSHUJIANG	DEV. STEP	PV2			
APPROVAL	KEVIN LEE	REV	1.0		CLOCK DIAGRAM	PART NO. BA41-XXXXX
MODULE CODE		LAST EDIT			October 23, 2007 10:38:02 AM	PAGE 7 OF 58

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SEL_LCDCLK*	Pin 20/21	Pin 24/25
LOW	DOT_96/DOT_96#	LCDCCLK/LCDCCLK#
HIGH	SRC_0/SRC_0#	27M & 27M_SS

FSA	FSB	FSC	HOST CLK
BSEL0	BSEL1	BSEL2	
0	0	0	266 MHz
0	0	1	333 MHz
0	1	0	200 MHz
0	1	1	400 MHz
1	0	0	133 MHz
1	0	1	100 MHz
1	1	0	166 MHz
1	1	1	RSVD

CLK REQ	DEVICE	SRC PORT
CLK REQ A	SATA	SRC2
CLK REQ B	GMCH	SRC4
CLK REQ E	MINI CARD	SRC6
CLK REQ F	EXPRESS CARD	SRC8

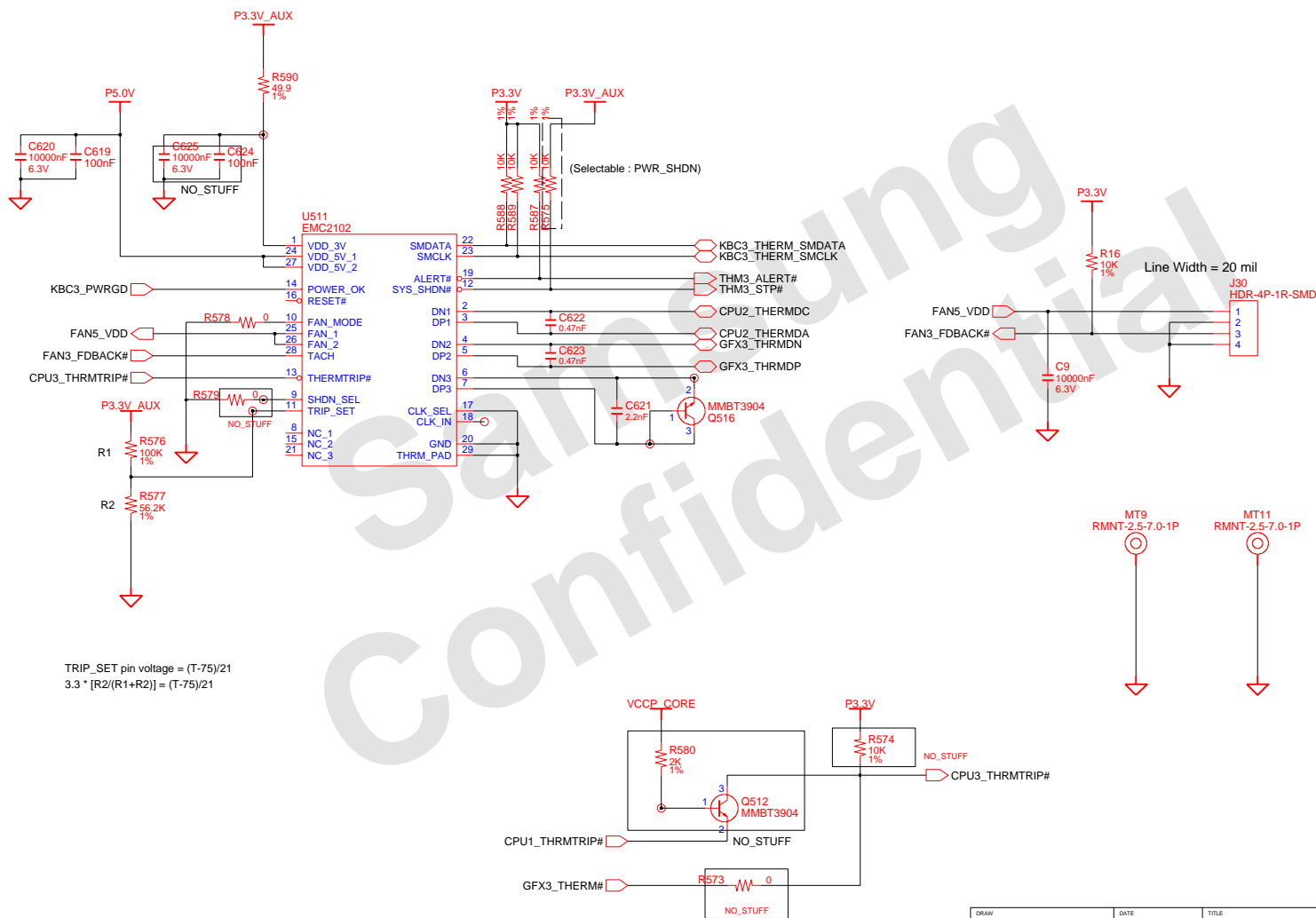


DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Geneva	SAMSUNG ELECTRONICS
CHECK	WUSHUJIANG	DEV. STEP	PV2	CLOCK GENERATOR	CLOCK GENERATOR	
APPROVAL	KEVIN LEE	REV	1.0	CK-505	CK-505	PART NO. BA41-XXXXX
MODULE CODE		LAST EDIT				
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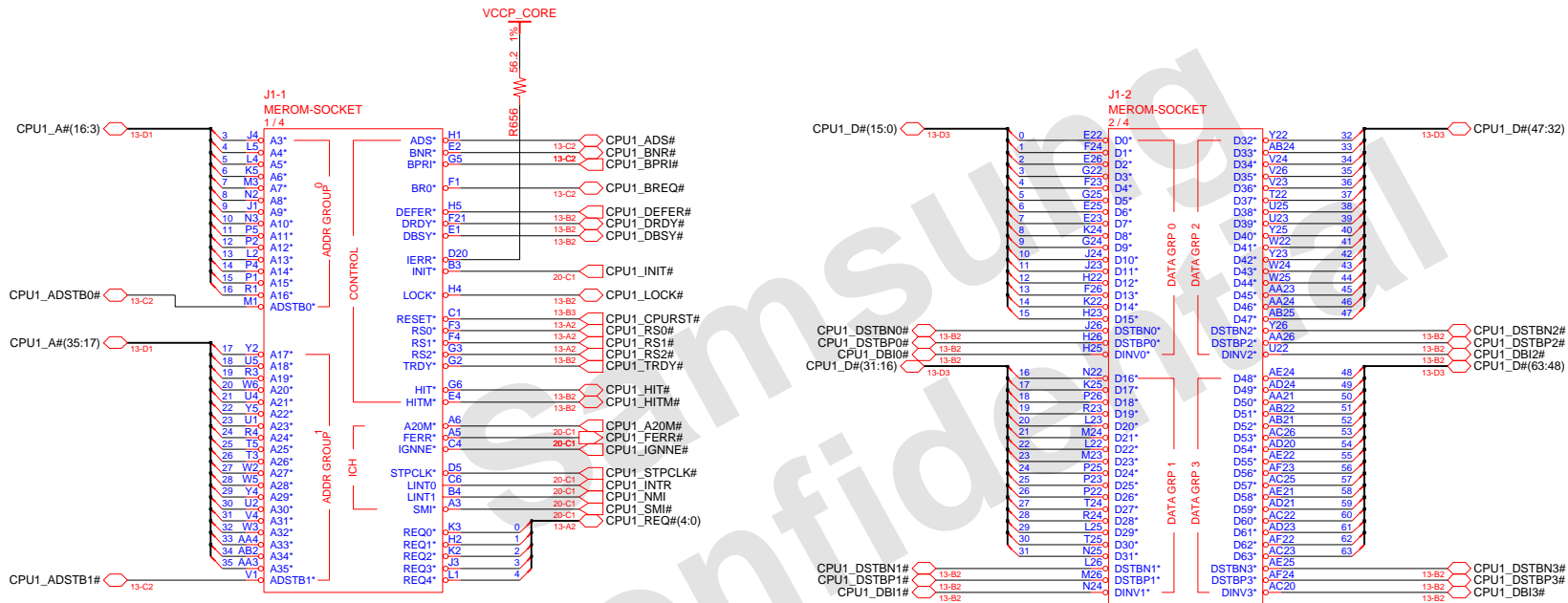
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# THERMAL SENSOR & FAN CONTROL

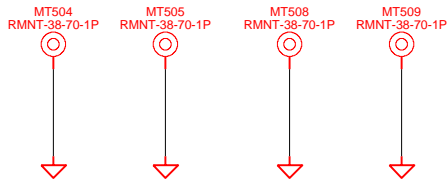


DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena THERMAL BLOCK	<b>SAMSUNG</b> ELECTRONICS
CHECK	WUSHUJIANG	DEV. STEP	PV2	THERMAL & FAN CONTROL		
APPROVAL	KEVIN LEE	REV	1.0			PART NO. BA41-XXXXX
MODULE CODE		LAST EDIT	October 23, 2007 10:38:02 AM	PAGE	9	OF 58

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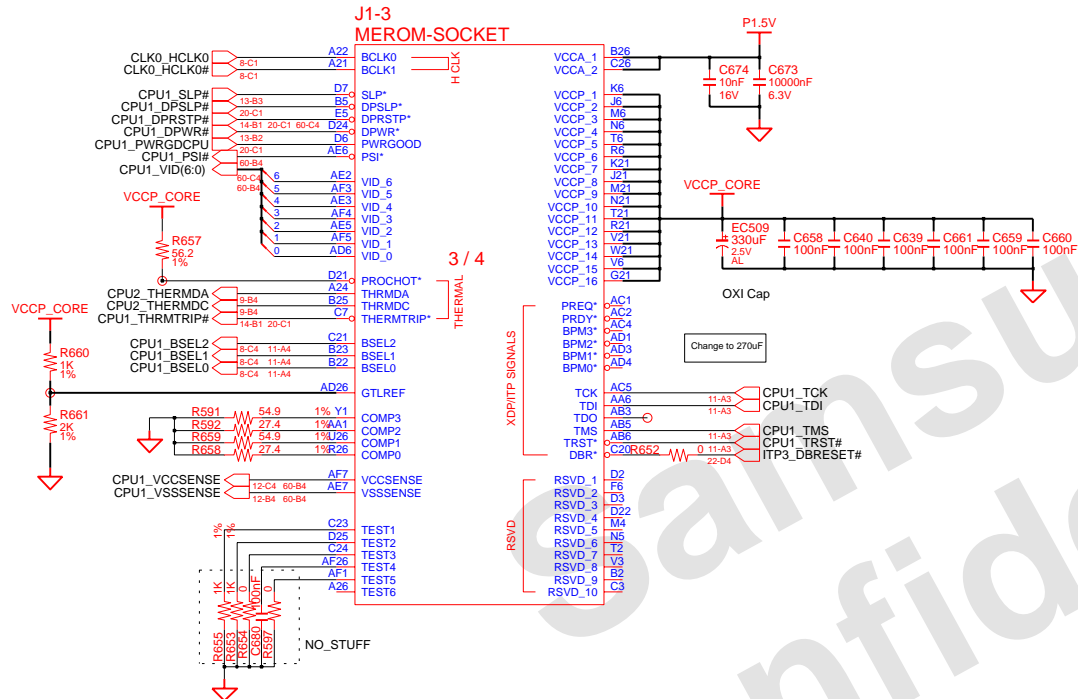


CPU CONNECTOR PART NUMBER 3704-001153

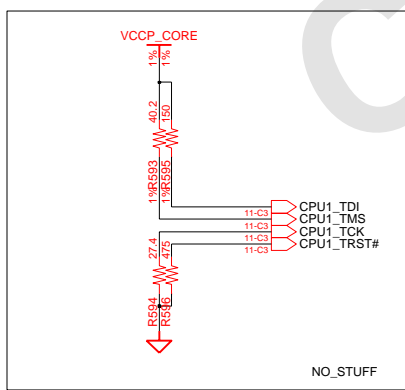


DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Geneva CPU MEROM(1/3)	<b>SAMSUNG</b> ELECTRONICS	
CHECK	WUSHIJIANG	DEV. STEP	PV2				
APPROVAL	KEVIN LEE	REV	1.0				
MODULE CODE	undefined	LAST ENT	October 23, 2007 10:38:02 AM	PAGE 10 OF 58			
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**ITP DISABLE**



**CPU Core Voltage Table** IMVP-6

Active Mode		Active/Deeper Sleep Dual Mode Region		Deeper Sleep/Extended Deeper Sleep Dual Mode Region	
VID(6:0)	Voltage	VID(6:0)	Voltage	VID(6:0)	Voltage
0 0 0 0 0 0 0	1.5000 V	0 1 0 1 0 0 0	1.0000 V	1 0 1 0 0 0 1	0.4875 V
0 0 0 0 0 0 1	1.4875 V	0 1 0 1 0 0 1	0.9875 V	1 0 1 0 0 1 0	0.4750 V
0 0 0 0 0 1 0	1.4750 V	0 1 0 1 0 1 0	0.9750 V	1 0 1 0 0 1 1	0.4625 V
0 0 0 0 0 1 1	1.4625 V	0 1 0 1 1 0 1	0.9625 V	1 0 1 0 1 0 0	0.4500 V
0 0 0 0 1 0 0	1.4500 V	0 1 0 1 1 0 1	0.9500 V	1 0 1 0 1 0 1	0.4375 V
0 0 0 0 1 0 1	1.4375 V	0 1 0 1 1 1 0	0.9375 V	1 0 1 0 1 1 0	0.4250 V
0 0 0 0 1 1 0	1.4250 V	0 1 0 1 1 1 1	0.9250 V	1 0 1 0 1 1 1	0.4125 V
0 0 0 0 1 1 1	1.4125 V	0 1 1 0 1 1 1	0.9125 V	1 0 1 1 0 0 0	0.4000 V
0 0 0 1 0 0 0	1.4000 V	0 1 1 0 0 0 0	0.9000 V	1 0 1 1 0 0 1	0.3875 V
0 0 0 1 0 0 1	1.3875 V	0 1 1 0 0 0 1	0.8875 V	1 0 1 1 0 1 0	0.3750 V
0 0 0 1 0 1 0	1.3750 V	0 1 1 0 0 1 0	0.8750 V	1 0 1 1 0 1 1	0.3625 V
0 0 0 1 0 1 1	1.3625 V	0 1 1 0 1 0 1	0.8625 V	1 0 1 1 1 0 0	0.3500 V
0 0 0 1 1 0 0	1.3500 V	0 1 1 0 1 0 1	0.8500 V	1 0 1 1 1 0 1	0.3375 V
0 0 0 1 1 0 1	1.3375 V	0 1 1 0 1 1 0	0.8375 V	1 0 1 1 1 1 0	0.3250 V
0 0 0 1 1 1 0	1.3250 V	0 1 1 0 1 1 1	0.8250 V	1 0 1 1 1 1 1	0.3125 V
0 0 0 1 1 1 1	1.3125 V	0 1 1 1 0 0 0	0.8125 V	1 1 0 0 0 0 0	0.3000 V
0 0 1 0 0 0 0	1.3000 V	0 1 1 1 0 0 1	0.8000 V	1 1 0 0 0 0 1	0.2875 V
0 0 1 0 0 0 1	1.2875 V	0 1 1 1 0 1 0	0.7875 V	1 1 0 0 0 1 0	0.2750 V
0 0 1 0 0 1 0	1.2750 V	0 1 1 1 0 1 1	0.7750 V	1 1 0 0 0 1 1	0.2625 V
0 0 1 0 0 1 1	1.2625 V	0 1 1 1 1 0 0	0.7625 V	1 1 0 0 1 0 0	0.2500 V
0 0 1 0 1 0 0	1.2500 V	0 1 1 1 1 0 1	0.7500 V	1 1 0 0 1 0 1	0.2375 V
0 0 1 0 1 0 1	1.2375 V	0 1 1 1 1 1 0	0.7375 V	1 1 0 0 1 1 0	0.2250 V
0 0 1 0 1 1 0	1.2250 V	0 1 1 1 1 1 1	0.7250 V	1 1 0 0 1 1 1	0.2125 V
0 0 1 0 1 1 1	1.2125 V	1 0 0 0 0 0 0	0.7125 V	1 1 0 0 1 1 1	0.2000 V
0 0 1 1 0 0 0	1.2000 V	1 0 0 0 0 0 1	0.7000 V	1 1 0 1 0 0 0	0.1875 V
0 0 1 1 0 0 1	1.1875 V	1 0 0 0 0 0 1	0.6875 V	1 1 0 1 0 0 1	0.1750 V
0 0 1 1 0 1 0	1.1750 V	1 0 0 0 0 1 0	0.6750 V	1 1 0 1 0 1 0	0.1625 V
0 0 1 1 0 1 1	1.1625 V	1 0 0 0 0 1 1	0.6625 V	1 1 0 1 0 1 1	0.1500 V
0 0 1 1 1 0 0	1.1500 V	1 0 0 0 1 0 0	0.6500 V	1 1 0 1 1 0 0	0.1375 V
0 0 1 1 1 0 1	1.1375 V	1 0 0 0 1 0 1	0.6375 V	1 1 0 1 1 0 1	0.1250 V
0 0 1 1 1 1 0	1.1250 V	1 0 0 0 1 1 0	0.6250 V	1 1 0 1 1 1 0	0.1125 V
0 0 1 1 1 1 1	1.1125 V	1 0 0 0 1 1 1	0.6125 V	1 1 0 1 1 1 1	0.1000 V
0 1 0 0 0 0 0	1.1000 V	1 0 0 1 0 0 0	0.6000 V	1 1 0 1 1 1 1	0.0875 V
0 1 0 0 0 0 1	1.0875 V	1 0 0 1 0 0 1	0.5875 V	1 1 0 1 1 1 1	0.0750 V
0 1 0 0 0 1 0	1.0750 V	1 0 0 1 0 1 0	0.5750 V	1 1 1 0 0 0 0	0.0625 V
0 1 0 0 0 1 1	1.0625 V	1 0 0 1 0 1 1	0.5625 V	1 1 1 0 0 0 1	0.0500 V
0 1 0 0 1 0 0	1.0500 V	1 0 0 1 1 0 0	0.5500 V	1 1 1 0 0 0 1	0.0375 V
0 1 0 0 1 0 1	1.0375 V	1 0 0 1 1 0 1	0.5375 V	1 1 1 0 0 1 0	0.0250 V
0 1 0 0 1 1 0	1.0250 V	1 0 0 1 1 1 0	0.5250 V	1 1 1 0 0 1 1	0.0125 V
0 1 0 0 1 1 1	1.0125 V	1 0 0 1 1 1 1	0.5125 V	1 1 1 1 0 0 0	0.0000 V
0 1 0 1 0 0 0	1.0000 V	1 0 0 1 1 1 1	0.5000 V	1 1 1 1 0 0 1	0.0000 V
0 1 0 1 0 0 1	0.9875 V	1 0 0 1 1 1 1	0.4875 V	1 1 1 1 0 1 0	0.0000 V
0 1 0 1 0 0 1	0.9750 V	1 0 0 1 1 1 1	0.4750 V	1 1 1 1 0 1 1	0.0000 V
0 1 0 1 0 1 0	0.9625 V	1 0 0 1 1 1 1	0.4625 V	1 1 1 1 1 0 0	0.0000 V
0 1 0 1 0 1 1	0.9500 V	1 0 0 1 1 1 1	0.4500 V	1 1 1 1 1 0 1	0.0000 V
0 1 0 1 1 0 0	0.9375 V	1 0 0 1 1 1 1	0.4375 V	1 1 1 1 1 1 0	0.0000 V
0 1 0 1 1 0 1	0.9250 V	1 0 0 1 1 1 1	0.4250 V	1 1 1 1 1 1 1	0.0000 V
0 1 0 1 1 1 0	0.9125 V	1 0 0 1 1 1 1	0.4125 V	1 1 1 1 1 1 1	0.0000 V
0 1 0 1 1 1 1	0.9000 V	1 0 0 1 1 1 1	0.4000 V	1 1 1 1 1 1 1	0.0000 V
0 1 1 0 0 0 0	0.8875 V	1 0 0 1 1 1 1	0.3875 V	1 1 1 1 1 1 1	0.0000 V
0 1 1 0 0 0 1	0.8750 V	1 0 0 1 1 1 1	0.3750 V	1 1 1 1 1 1 1	0.0000 V
0 1 1 0 0 1 0	0.8625 V	1 0 0 1 1 1 1	0.3625 V	1 1 1 1 1 1 1	0.0000 V
0 1 1 0 0 1 1	0.8500 V	1 0 0 1 1 1 1	0.3500 V	1 1 1 1 1 1 1	0.0000 V
0 1 1 0 1 0 0	0.8375 V	1 0 0 1 1 1 1	0.3375 V	1 1 1 1 1 1 1	0.0000 V
0 1 1 0 1 0 1	0.8250 V	1 0 0 1 1 1 1	0.3250 V	1 1 1 1 1 1 1	0.0000 V
0 1 1 0 1 1 0	0.8125 V	1 0 0 1 1 1 1	0.3125 V	1 1 1 1 1 1 1	0.0000 V
0 1 1 0 1 1 1	0.8000 V	1 0 0 1 1 1 1	0.3000 V	1 1 1 1 1 1 1	0.0000 V
0 1 1 1 0 0 0	0.7875 V	1 0 0 1 1 1 1	0.2875 V	1 1 1 1 1 1 1	0.0000 V
0 1 1 1 0 0 1	0.7750 V	1 0 0 1 1 1 1	0.2750 V	1 1 1 1 1 1 1	0.0000 V
0 1 1 1 0 1 0	0.7625 V	1 0 0 1 1 1 1	0.2625 V	1 1 1 1 1 1 1	0.0000 V
0 1 1 1 0 1 1	0.7500 V	1 0 0 1 1 1 1	0.2500 V	1 1 1 1 1 1 1	0.0000 V
0 1 1 1 1 0 0	0.7375 V	1 0 0 1 1 1 1	0.2375 V	1 1 1 1 1 1 1	0.0000 V
0 1 1 1 1 0 1	0.7250 V	1 0 0 1 1 1 1	0.2250 V	1 1 1 1 1 1 1	0.0000 V
0 1 1 1 1 1 0	0.7125 V	1 0 0 1 1 1 1	0.2125 V	1 1 1 1 1 1 1	0.0000 V
0 1 1 1 1 1 1	0.7000 V	1 0 0 1 1 1 1	0.2000 V	1 1 1 1 1 1 1	0.0000 V
1 0 0 0 0 0 0	0.6875 V	1 0 0 1 1 1 1	0.1875 V	1 1 1 1 1 1 1	0.0000 V
1 0 0 0 0 0 1	0.6750 V	1 0 0 1 1 1 1	0.1750 V	1 1 1 1 1 1 1	0.0000 V
1 0 0 0 0 1 0	0.6625 V	1 0 0 1 1 1 1	0.1625 V	1 1 1 1 1 1 1	0.0000 V
1 0 0 0 0 1 1	0.6500 V	1 0 0 1 1 1 1	0.1500 V	1 1 1 1 1 1 1	0.0000 V
1 0 0 0 1 0 0	0.6375 V	1 0 0 1 1 1 1	0.1375 V	1 1 1 1 1 1 1	0.0000 V
1 0 0 0 1 0 1	0.6250 V	1 0 0 1 1 1 1	0.1250 V	1 1 1 1 1 1 1	0.0000 V
1 0 0 0 1 1 0	0.6125 V	1 0 0 1 1 1 1	0.1125 V	1 1 1 1 1 1 1	0.0000 V
1 0 0 0 1 1 1	0.6000 V	1 0 0 1 1 1 1	0.1000 V	1 1 1 1 1 1 1	0.0000 V
1 0 0 1 0 0 0	0.5875 V	1 0 0 1 1 1 1	0.0875 V	1 1 1 1 1 1 1	0.0000 V
1 0 0 1 0 0 1	0.5750 V	1 0 0 1 1 1 1	0.0750 V	1 1 1 1 1 1 1	0.0000 V
1 0 0 1 0 1 0	0.5625 V	1 0 0 1 1 1 1	0.0625 V	1 1 1 1 1 1 1	0.0000 V
1 0 0 1 0 1 1	0.5500 V	1 0 0 1 1 1 1	0.0500 V	1 1 1 1 1 1 1	0.0000 V
1 0 0 1 1 0 0	0.5375 V	1 0 0 1 1 1 1	0.0375 V	1 1 1 1 1 1 1	0.0000 V
1 0 0 1 1 0 1	0.5250 V	1 0 0 1 1 1 1	0.0250 V	1 1 1 1 1 1 1	0.0000 V
1 0 0 1 1 1 0	0.5125 V	1 0 0 1 1 1 1	0.0125 V	1 1 1 1 1 1 1	0.0000 V
1 0 0 1 1 1 1	0.5000 V	1 0 0 1 1 1 1	0.0000 V	1 1 1 1 1 1 1	0.0000 V

GTLREF : Keep the Voltage divider within 0.5" of the first GTLREF0 pin with Zo=55ohm trace. Minimize coupling of any switching signals to this net.

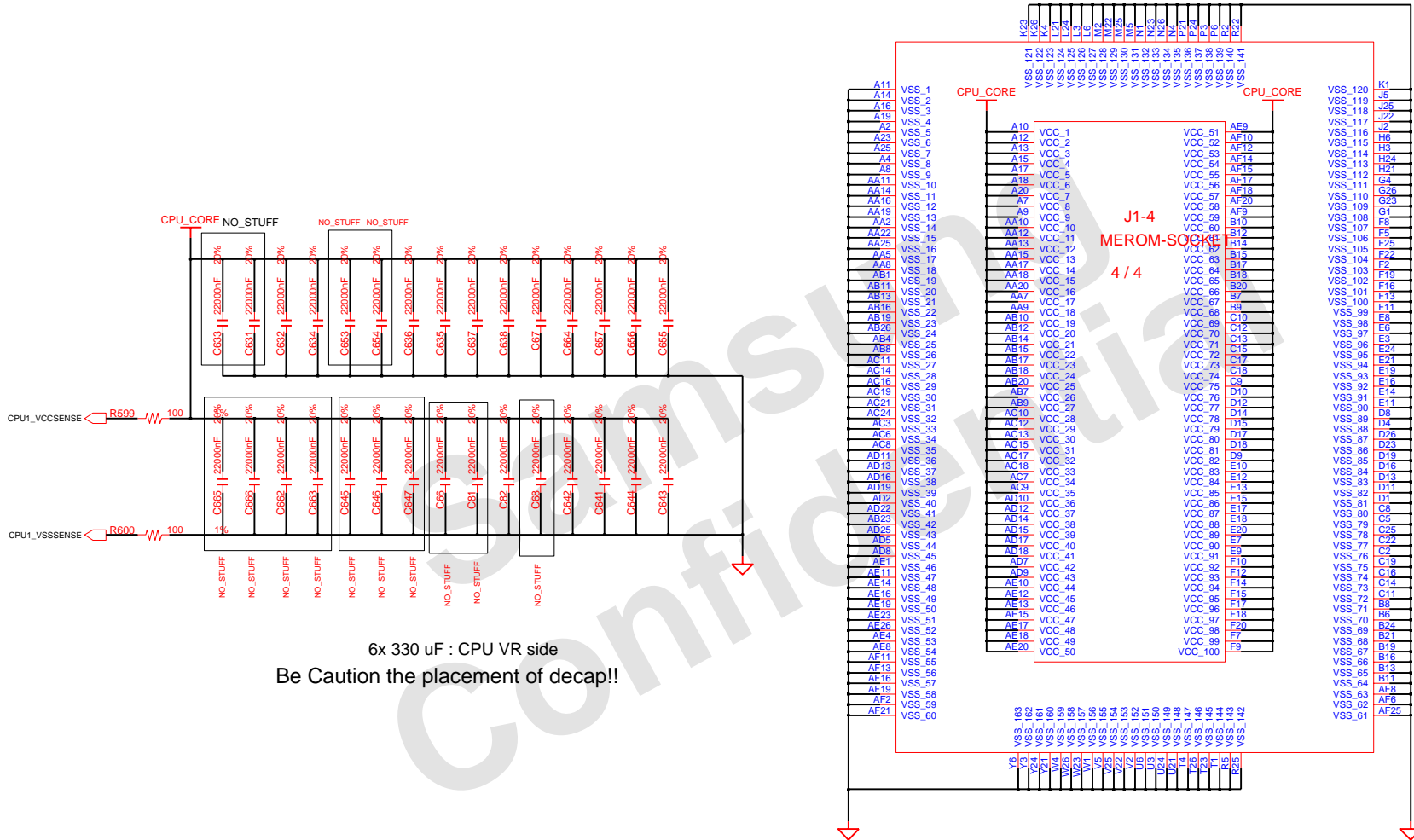
COMP0\_2(COMP1\_3) should be connected with Zo=27.4ohm(55ohm) trace shorter than 1/2" to their respective Banias socket pins.

GND test points within 100mil of the VCC/VSSsense at the end of the line. Route the VCC/VSSsense as a Zo=55ohm traces with equal length. Observe 3:1 spacing b/w VCC/VSSsense lines and 25mil away (preferred 50mil) from any other signal. And GND via 100mil away from each of the VCC/VSS test point vias.

\*Yonah Processor (2.33 GHz / 800 MHz : TBD)

DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Geneva	SAMSUNG ELECTRONICS
CHECK	WUSHUJIANG	DEV. STEP	PV2	CPU		
APPROVAL	KEVIN LEE	REV	1.0	MEROM(2/3)	PART NO.	BA41-XXXX
MODULE CODE		LAST EDIT			October 23, 2007 10:38:02 AM	PAGE 11 OF 58

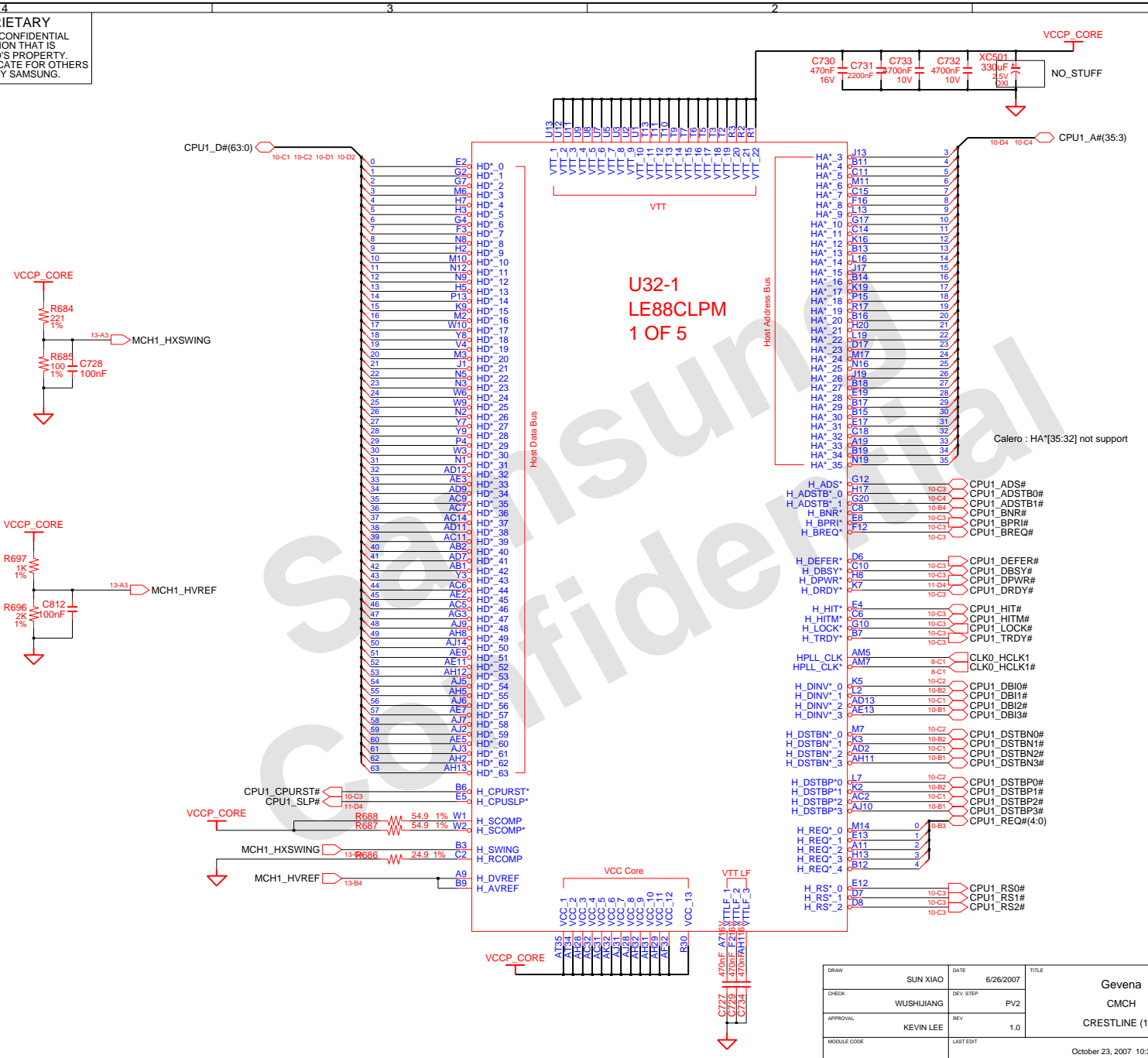
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6x 330 uF : CPU VR side  
 Be Caution the placement of decap!!

DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Geneva CPU	SAMSUNG ELECTRONICS
CHECK	WUSHUJIANG	DEV. STEP	PV2			
APPROVAL	KEVIN LEE	REV	1.0		MEROM(3/3)	PART NO. BA41-XXXXX
MODULE CODE		LAST EDIT		October 23, 2007 10:38:02 AM	PAGE	12 OF 58

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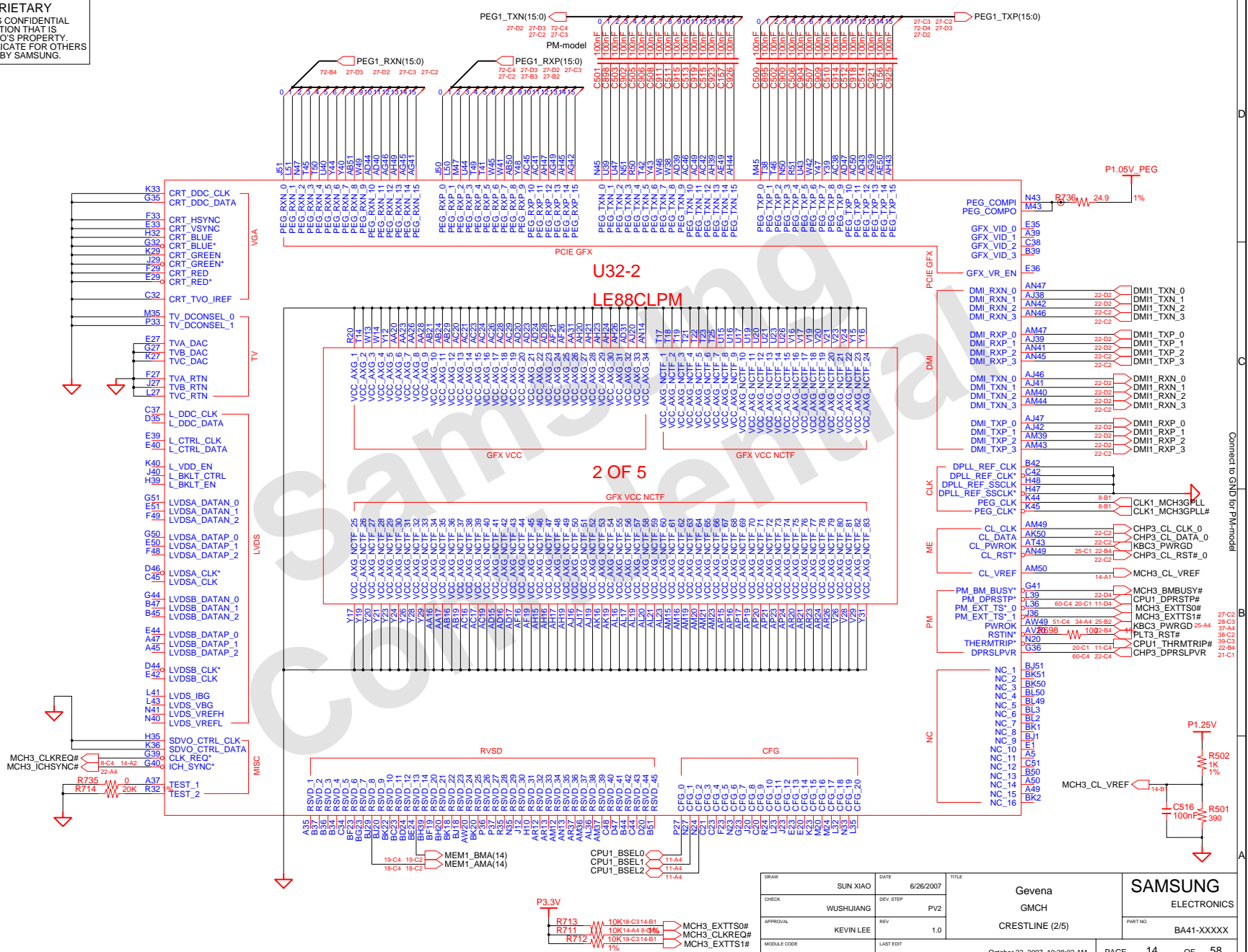


- HA\* 3 J13 3
  - HA\* 4 B11 4
  - HA\* 5 G11 5
  - HA\* 6 M11 6
  - HA\* 7 C15 7
  - HA\* 8 F16 8
  - HA\* 9 L13 9
  - HA\* 10 G17 10
  - HA\* 11 C14 11
  - HA\* 12 K16 12
  - HA\* 13 B13 13
  - HA\* 14 L16 14
  - HA\* 15 B14 15
  - HA\* 16 K19 16
  - HA\* 17 P19 17
  - HA\* 18 G17 18
  - HA\* 19 B16 19
  - HA\* 20 H20 20
  - HA\* 21 L19 21
  - HA\* 22 D17 22
  - HA\* 23 M17 23
  - HA\* 24 N16 24
  - HA\* 25 N16 25
  - HA\* 26 J19 26
  - HA\* 27 B18 27
  - HA\* 28 B17 28
  - HA\* 29 B19 29
  - HA\* 30 B15 30
  - HA\* 31 E17 31
  - HA\* 32 A19 32
  - HA\* 33 B19 33
  - HA\* 34 B19 34
  - HA\* 35 N19 35
- 
- H\_ADS\* G12 CPU1\_ADS#
  - H\_ADSTB\*\_0 H17 CPU1\_ADSTB0#
  - H\_ADSTB\*\_1 G20 CPU1\_ADSTB1#
  - H\_BNR\* C8 CPU1\_BNR#
  - H\_BPRI\* E9 CPU1\_BPRI#
  - H\_BREQ\* F12 CPU1\_BREQ#
- 
- H\_DEFER\* D6 CPU1\_DEFER#
  - H\_DBSY\* C10 CPU1\_DBSY#
  - H\_DPWR\* H8 CPU1\_DPWR#
  - H\_DRDY\* K7 CPU1\_DRDY#
- 
- H\_HIT\* E4 CPU1\_HIT#
  - H\_HITM\* C6 CPU1\_HITM#
  - H\_LOCK\* G10 CPU1\_LOCK#
  - H\_TRDY\* B7 CPU1\_TRDY#
- 
- HPLL\_CLK AM5 CLK0\_HCLK1
  - HPLL\_CLK\* AM7 CLK0\_HCLK1#
- 
- H\_DINV\*\_0 K5 CPU1\_DBI0#
  - H\_DINV\*\_1 R2 CPU1\_DBI1#
  - H\_DINV\*\_2 AD13 CPU1\_DBI2#
  - H\_DINV\*\_3 AE13 CPU1\_DBI3#
- 
- H\_DSTBN\*\_0 M7 CPU1\_DSTBN0#
  - H\_DSTBN\*\_1 K3 CPU1\_DSTBN1#
  - H\_DSTBN\*\_2 AD2 CPU1\_DSTBN2#
  - H\_DSTBN\*\_3 AH11 CPU1\_DSTBN3#
- 
- H\_DSTBP\*\_0 L7 CPU1\_DSTBP0#
  - H\_DSTBP\*\_1 K2 CPU1\_DSTBP1#
  - H\_DSTBP\*\_2 AC2 CPU1\_DSTBP2#
  - H\_DSTBP\*\_3 AJ10 CPU1\_DSTBP3#
- 
- H\_REQ\*\_0 AM4 CPU1\_REQ#(4:0)
  - H\_REQ\*\_1 E13 1
  - H\_REQ\*\_2 A11 2
  - H\_REQ\*\_3 H13 3
  - H\_REQ\*\_4 B12 4
- 
- H\_RS\*\_0 E12 CPU1\_RS0#
  - H\_RS\*\_1 D7 CPU1\_RS1#
  - H\_RS\*\_2 D8 CPU1\_RS2#

Calero : HA\*[35:32] not support

DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena	SAMSUNG ELECTRONICS
CHECK	WUSHUIJIANG	DEV_STEP	PV2		CMCH	
APPROVAL	KEVIN LEE	REV	1.0		CRESTLINE (1/5)	PART NO. BA41-XXXX
MODULE CODE		LAST EDIT			October 23, 2007 10:38:02 AM	PAGE 13 OF 58

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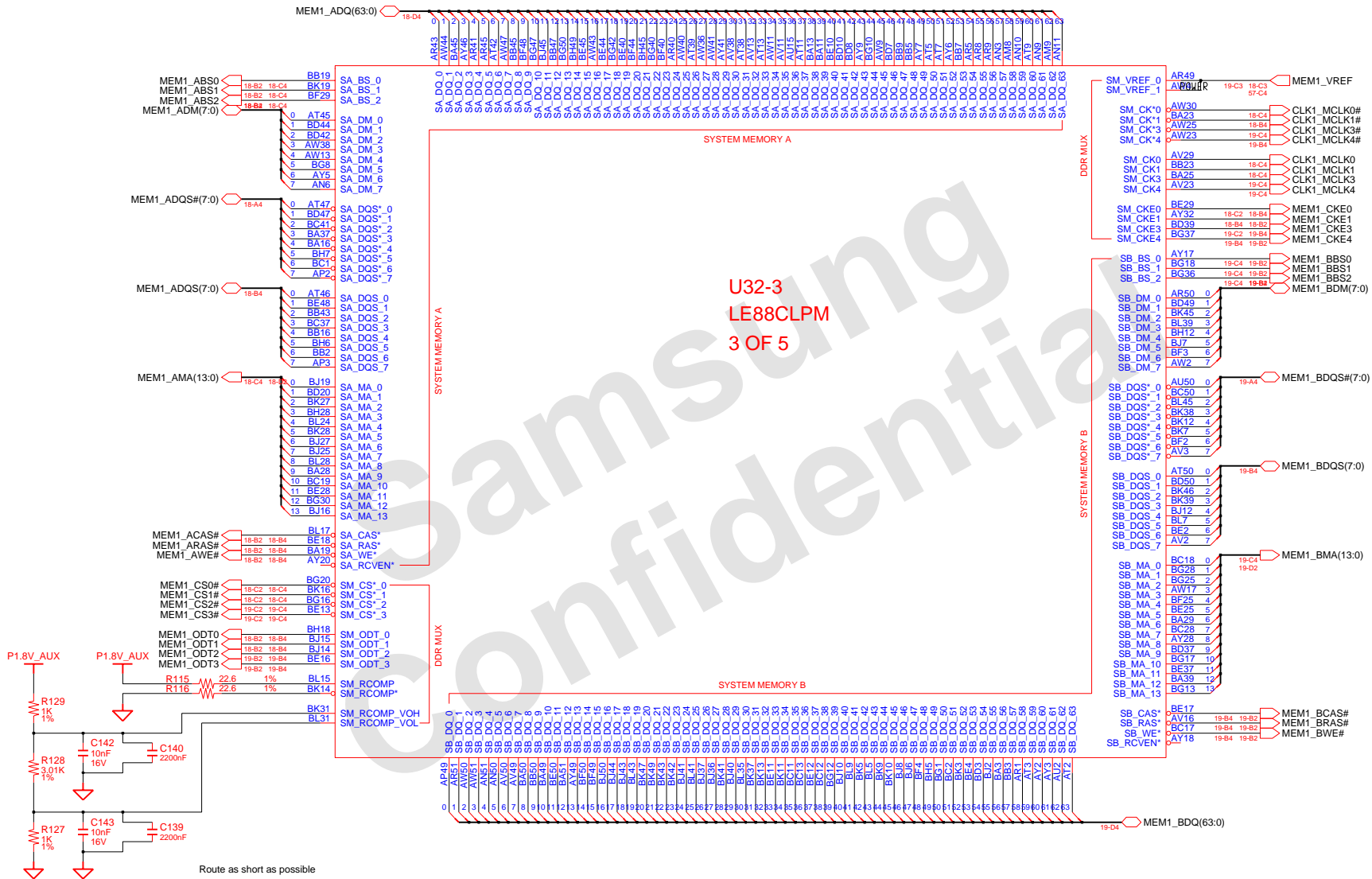
Connect to GND for PM-model

DRWN	SUN XIAO	DATE	6/26/2007	TITLE	Gevena
CHECK	WUSHUJIANG	DEV. STEP	PV2	DEV. CODE	GMCH
APPROVAL	KEVIN LEE	REV	1.0	CRESTLINE (2/5)	
MODULE CODE		LAST EDIT	October 23, 2007 10:38:02 AM	PAGE	14 OF 58

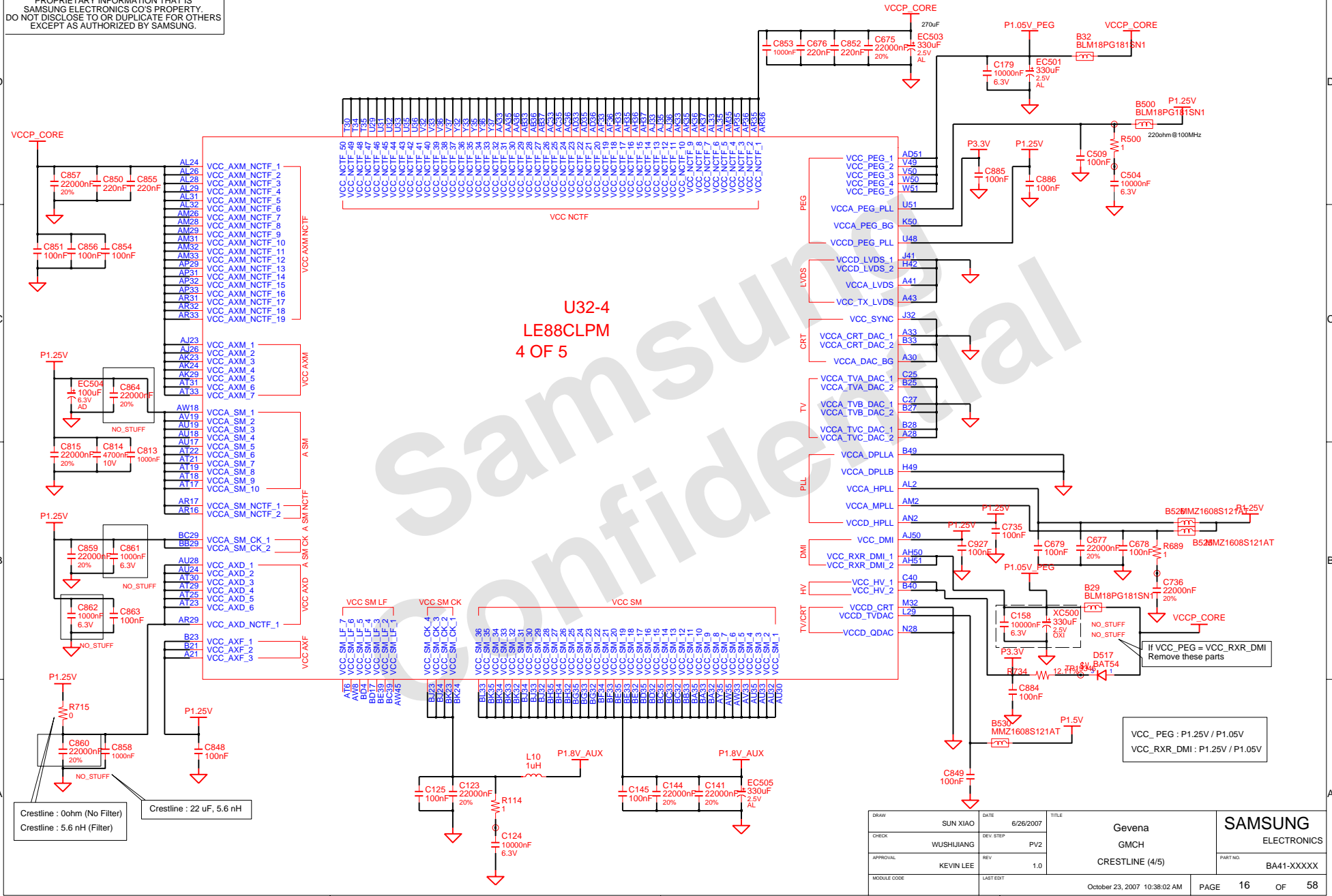
SAMSUNG ELECTRONICS	
PART NO.	BA41-XXXX

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DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Geneva	<b>SAMSUNG</b> ELECTRONICS
CHECK	WUSHUJIANG	DEV_STEP	PV2		GMCH	
APPROVAL	KEVIN LEE	REV	1.0		CRESTLINE (3/5)	PART NO. BA41-XXXX
MODULE CODE		LAST EDIT			October 23, 2007 10:38:02 AM	PAGE 15 OF 58

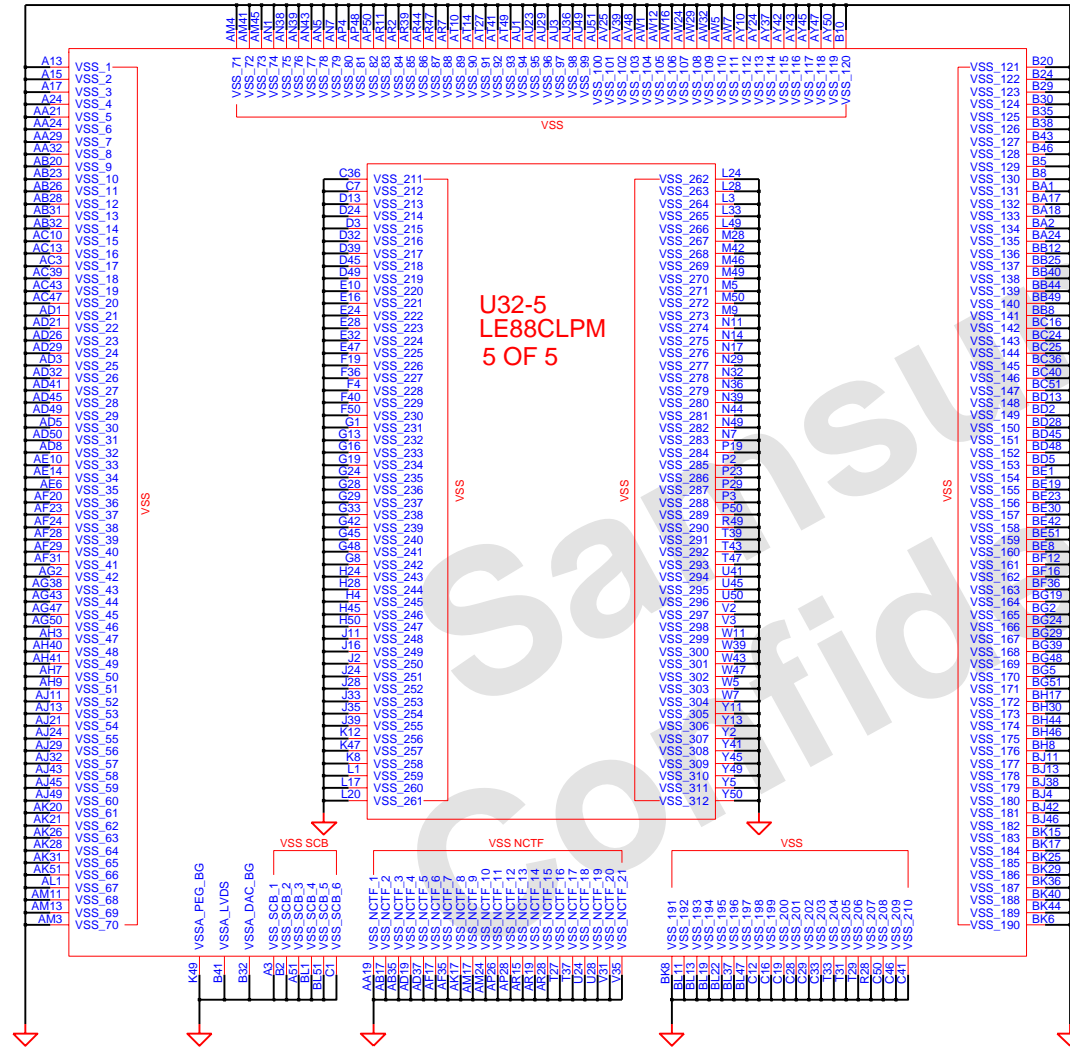
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DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena	<b>SAMSUNG</b> ELECTRONICS
CHECK	WUSHUIJIANG	DEV_STEP	PV2	GMCH	PART NO.	
APPROVAL	KEVIN LEE	REV	1.0	CRESTLINE (4/5)	BA41-XXXX	
MODULE CODE		LAST EDIT				
				October 23, 2007 10:38:02 AM	PAGE	16 OF 58



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\*POCAFEB-11 Only (Remove in MP Model)

CFG#	Current Setting (def.: default Option)	
	Low	High
CFG(5)	DMix2	DMix4 (def.)
CFG(6)	Reserved	DDR-II (def.)
CFG(7)	DT/Transportable	Mobile CPU (def.)
CFG(9)	PEG Reversal	Normal
CFG(16)	Dynamic ODT	Dynamic ODT
	Disabled	Enabled (def.)
CFG(18)	VCC 1.05V (def.)	VCC 1.5V
CFG(19)	DMI Lane Normal	DMI Lane Reversal
CFG(20)	SDVO or PCIE X1 Only(def.)	SDVO and PCIE X1 Simultaneously

DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena	<b>SAMSUNG</b> ELECTRONICS
CHECK	WUSHUIJIANG	DEV STEP	PV2		GMCH	
APPROVAL	KEVIN LEE	REV	1.0		CRESTLINE (5/5)	PART NO. BA41-XXXXX
MODULE CODE		LAST ENT			October 23, 2007 10:38:02 AM	PAGE 17 OF 58

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Array resistors & Single resistors used to improve layout & routing.

ME POWER RAIL UNDER ME ENABLE

P1.8V\_AUX

DDR1-2  
 DDR2-SODIMM-200P-RVS  
 2/2

P3.3V

MCH3\_EXTTSP#

MEM1\_VREF#

C62 C62

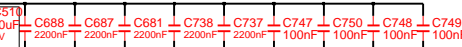
100nF 500nF

C62 C99

100nF 500nF

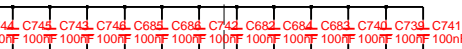
ME POWER RAIL UNDER ME ENABLE

P1.8V\_AUX



NO\_STUFF

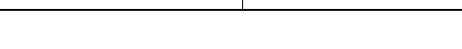
P0.9V



NO\_STUFF



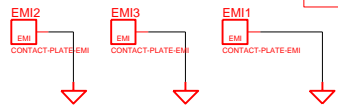
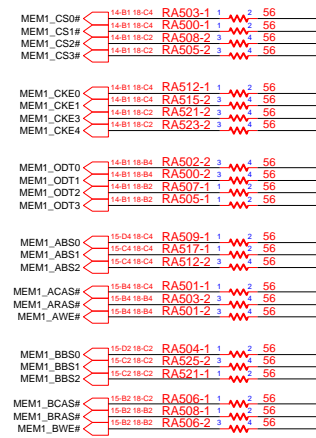
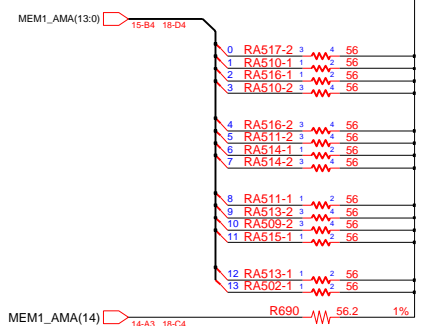
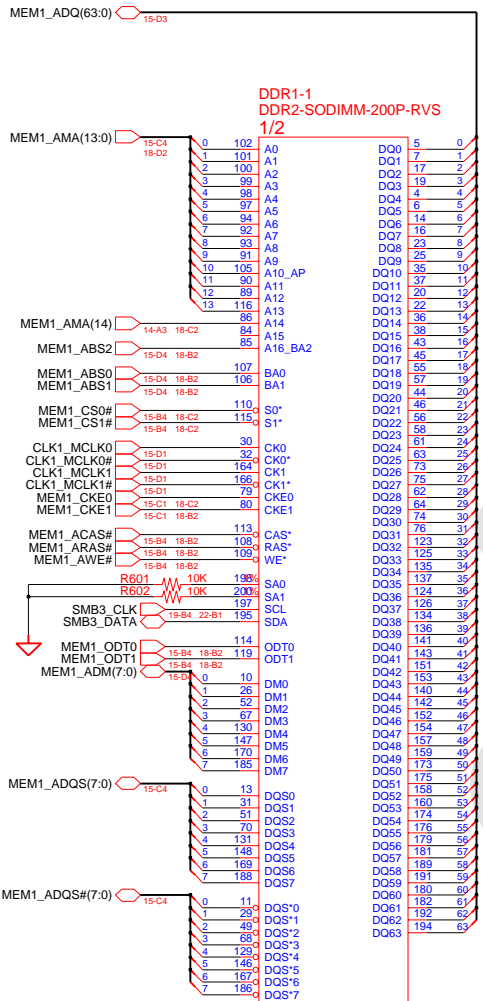
NO\_STUFF



NO\_STUFF



NO\_STUFF

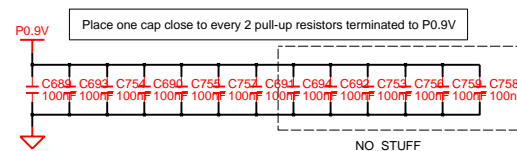
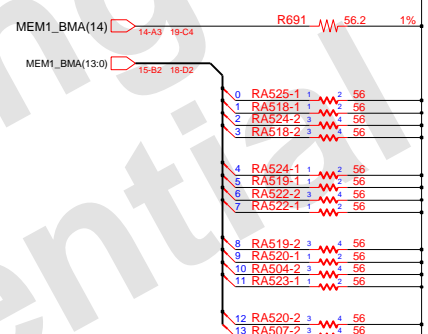
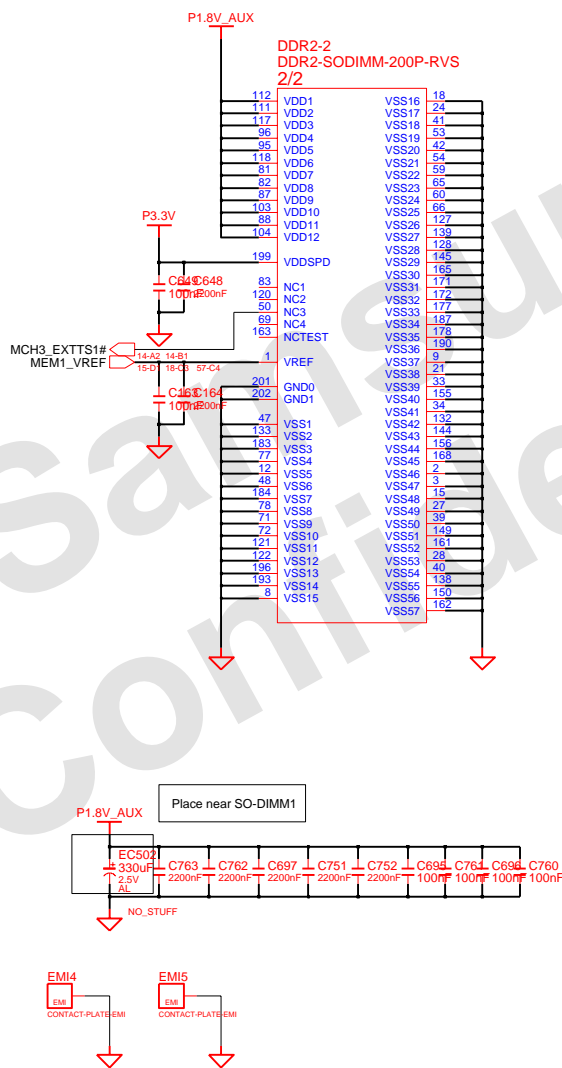
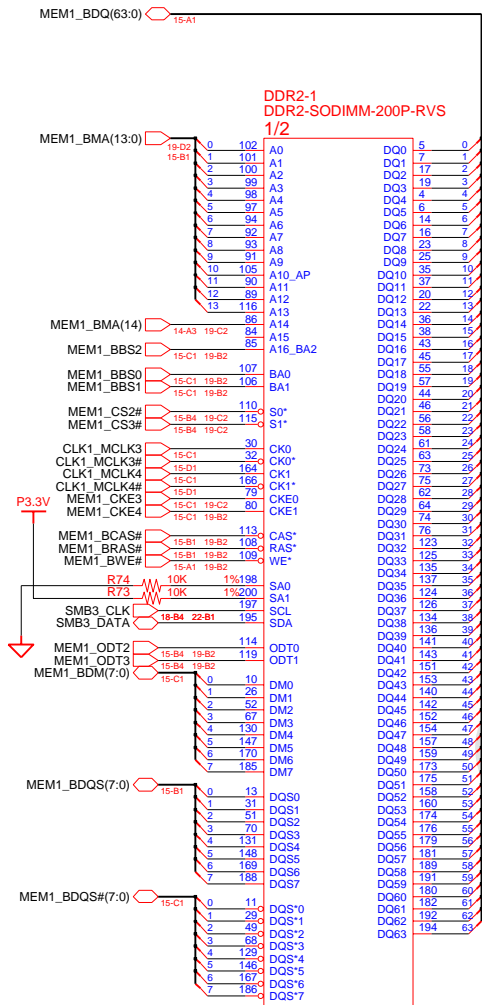


DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Geneva SODIMM DDR2 CH A	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-XXXXX
CHECK	WUSHUJIANG	DEV STEP	PV2			
APPROVAL	KEVIN LEE	REV	1.0			
MODULE CODE		LAST EDIT				

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DDR SO-DIMM #1

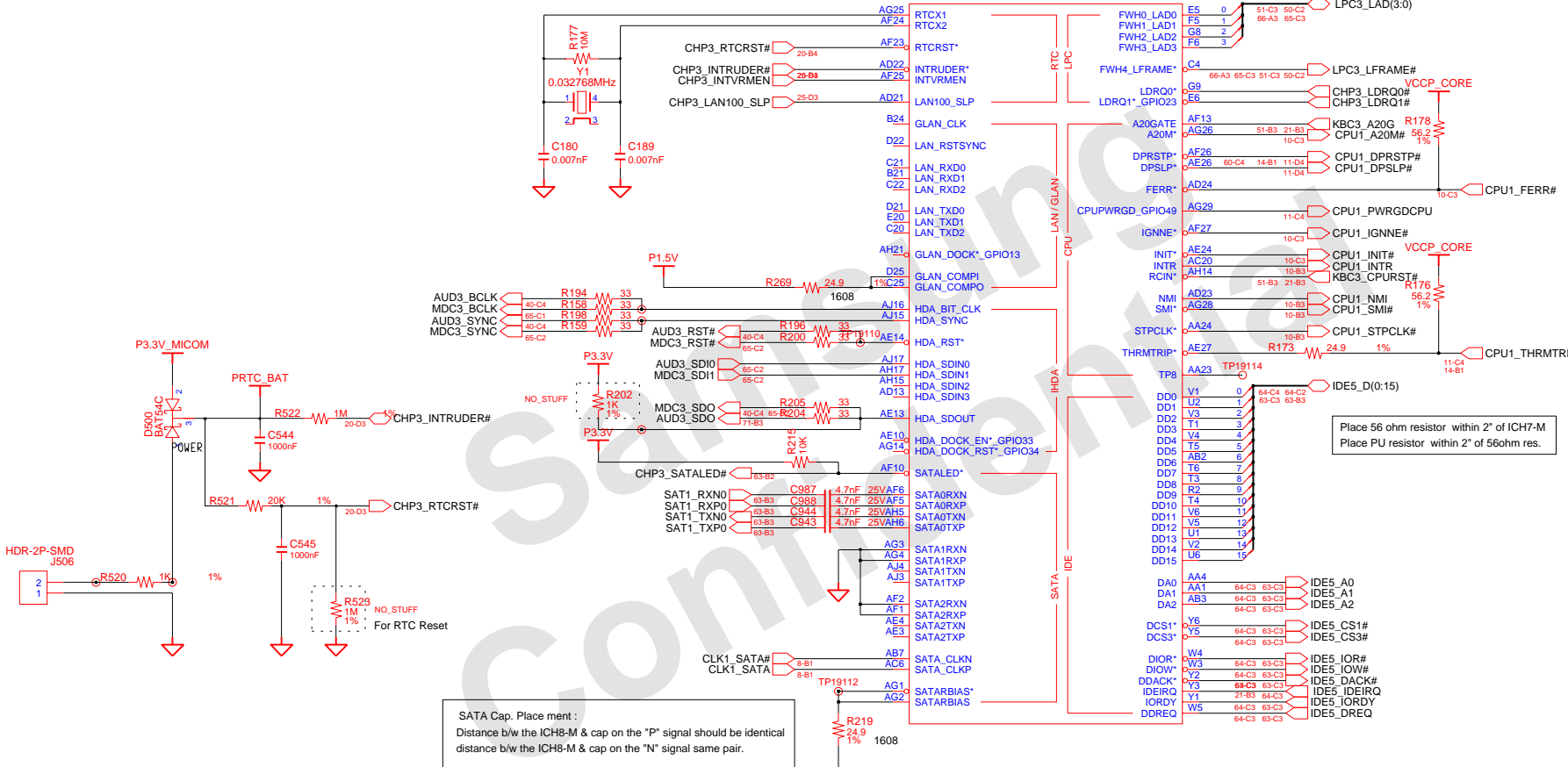
Array resistors & Single resistors used to improve layout & routing.



DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Geneva SODIMM	SAMSUNG ELECTRONICS
CHECK	WUSHUIJIANG	DEV. STEP	PV2			
APPROVAL	KEVIN LEE	REV	1.0		DDR2 CH B	PART NO. BA41-XXXXX
MODULE CODE		LAST EDIT		October 23, 2007 10:38:02 AM	PAGE	19 OF 58

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U33-1  
 NH82801HBM  
 1 / 5



SATA Cap. Placement :  
 Distance b/w the ICH8-M & cap on the "P" signal should be identical  
 distance b/w the ICH8-M & cap on the "N" signal same pair.

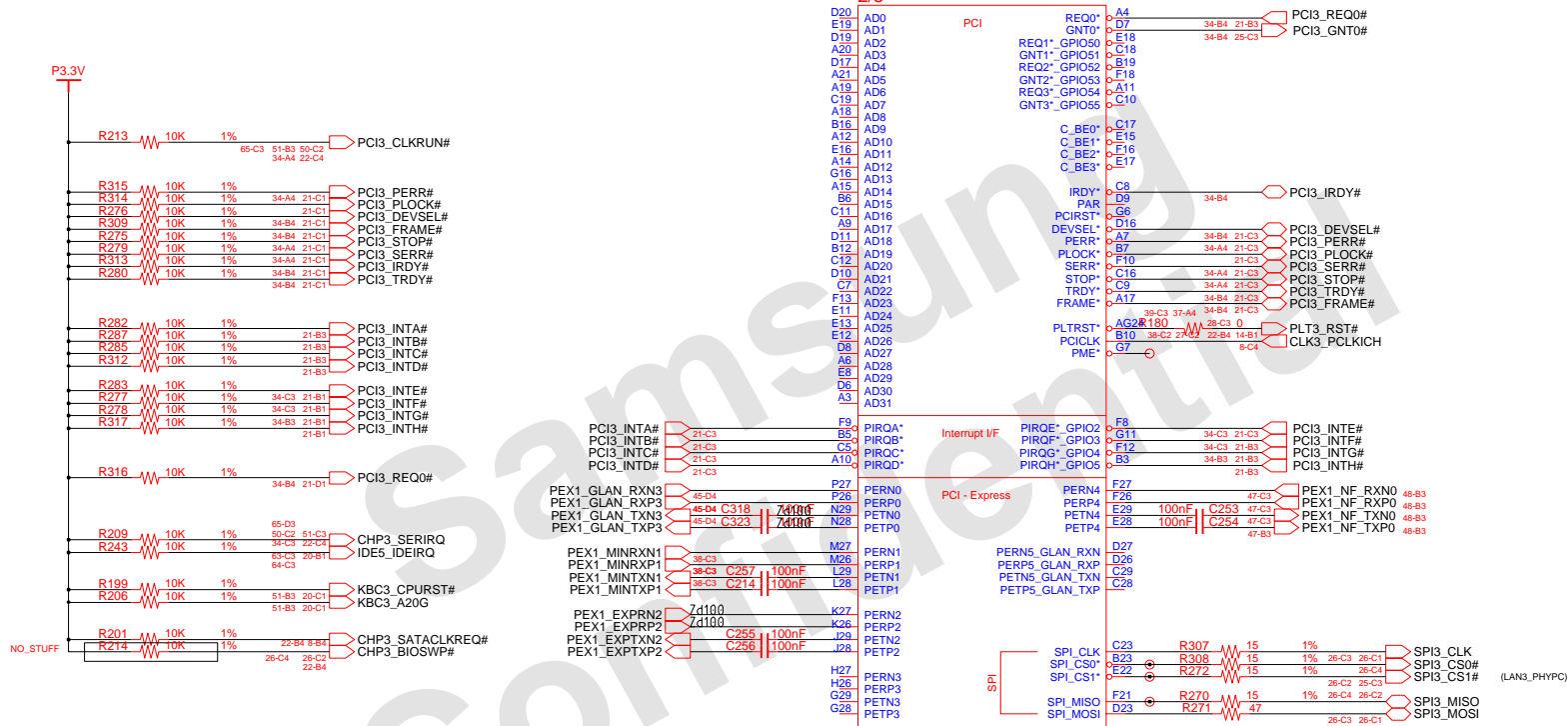
Place within 500 mils of ICH8-M

Place 56 ohm resistor within 2" of ICH7-M  
 Place PU resistor within 2" of 56ohm res.

DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena	SAMSUNG ELECTRONICS
CHECK	WUSHUJIANG	DEV. STEP	PV2		ICH8-M	
APPROVAL	KEVIN LEE	REV	1.0		ICH8-M (1/5)	PART NO. BA41-XXXX
MODULE CODE		LAST ENT		October 23, 2007 10:38:02 AM	PAGE	20 OF 58

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**U33-2**  
**NH82801HBM**  
**2/5**

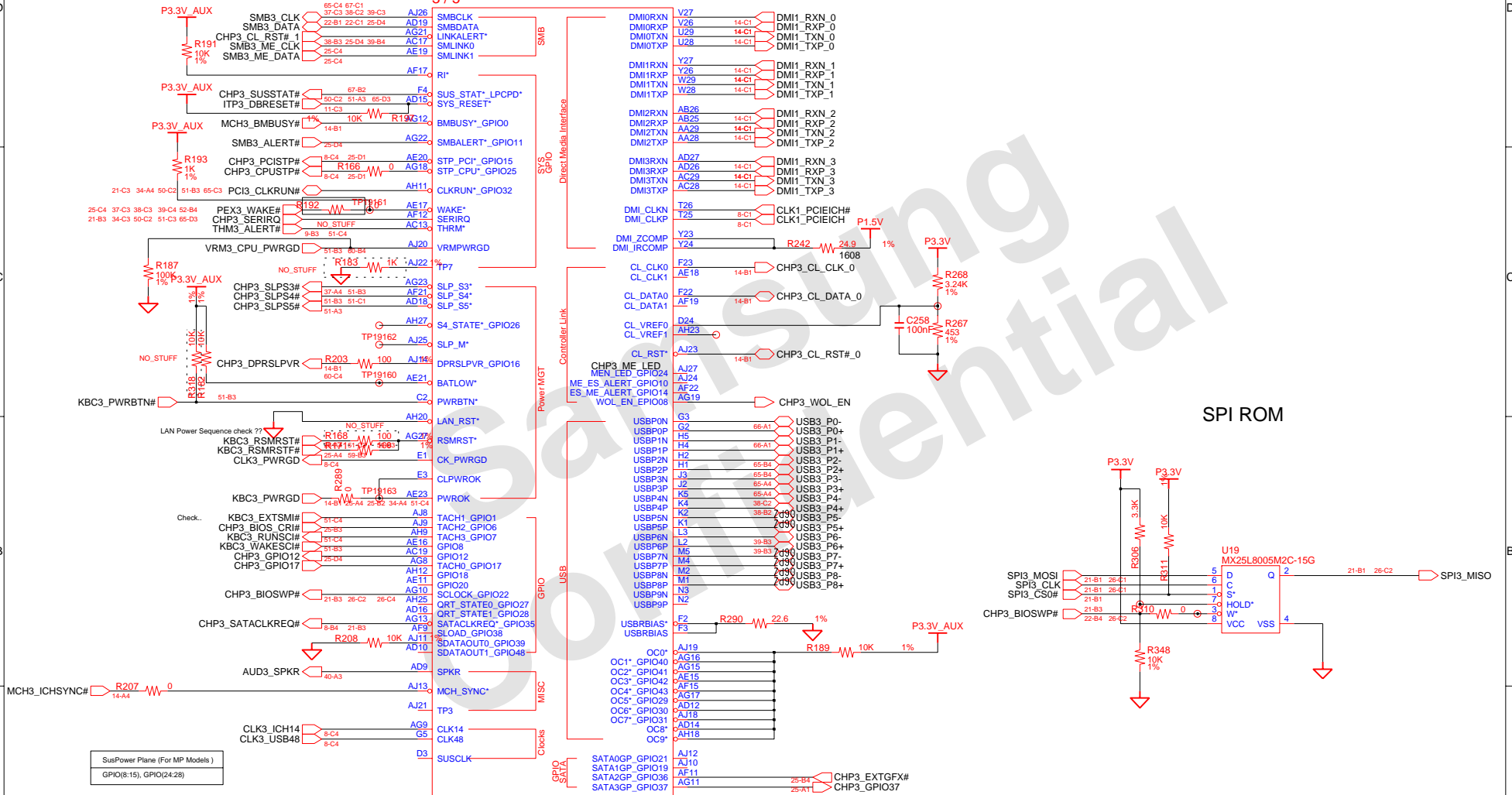


AC caps : PCIE need to be within 250mils of the driver  
 Resistor for Test : Place Stuffed Option to minimize stubs

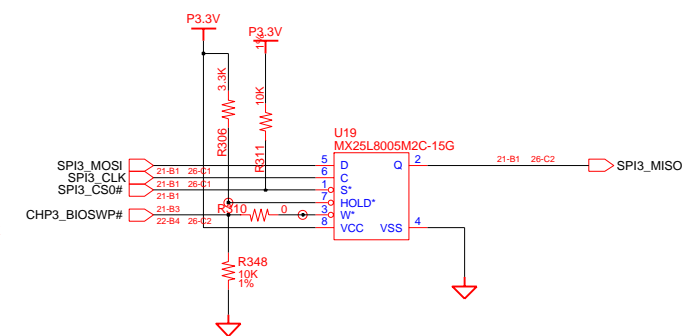
DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena	SAMSUNG ELECTRONICS
CHECK	WUSHUJIANG	DEV STEP	PV2	ICH8-M		
APPROVAL	KEVIN LEE	REV	1.0	ICH8-M (2/5)	PART NO.	BA41-XXXX
MODULE CODE		LAST EDIT				
				October 23, 2007 10:38:02 AM	PAGE	21 OF 58

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**U33-3  
 NH82801HBM  
 3 / 5**

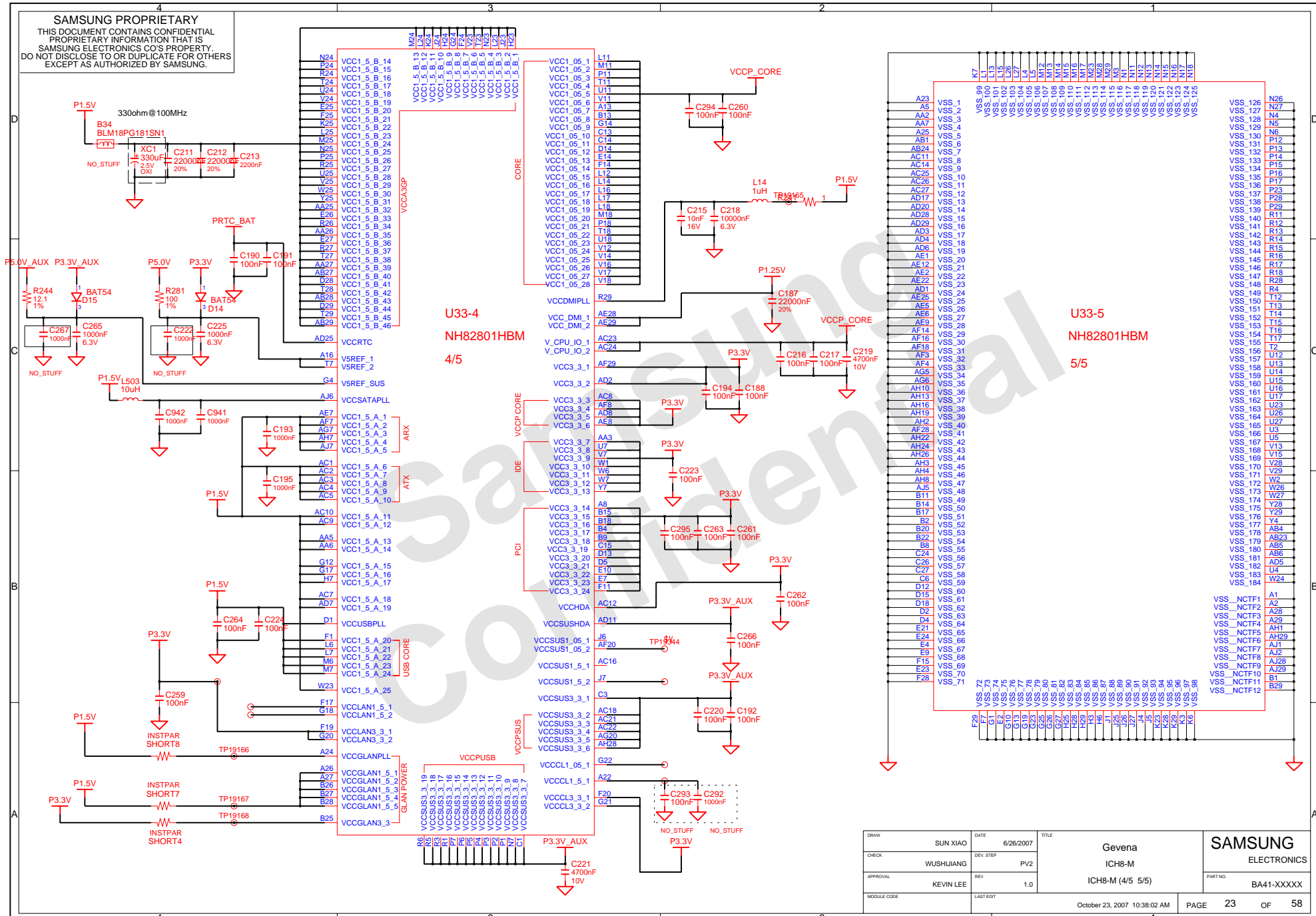


**SPI ROM**



DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena	<b>SAMSUNG</b> ELECTRONICS	
CHECK	WUSHUJIANG	DEV STEP	PV2		ICH8-M		
APPROVAL	KEVIN LEE	REV	1.0		ICH8-M (3/5)	PART NO. BA41-XXXXX	
MODULE CODE		LAST EDIT					
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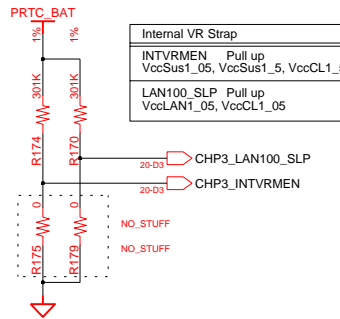
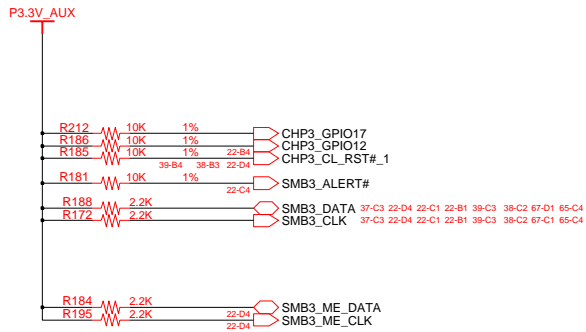
U33-4  
 NH82801HBM  
 4/5

U33-5  
 NH82801HBM  
 5/5

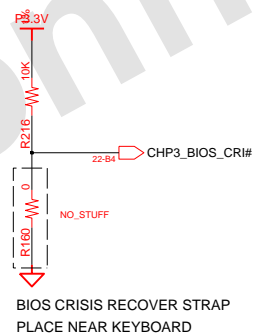
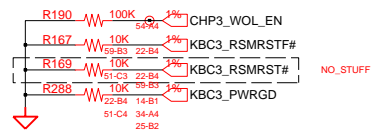
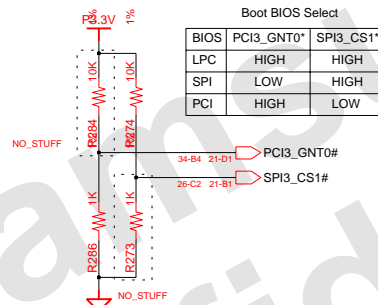
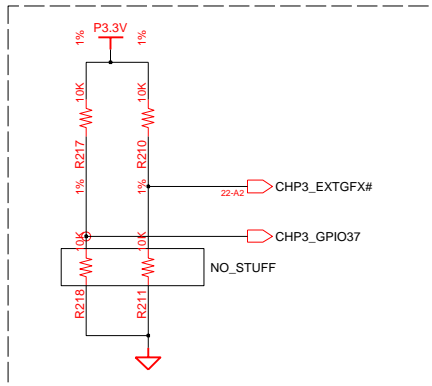
DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena
CHECK	WUSHUJIANG	DEV. STEP	PV2		ICH8-M
APPROVAL	KEVIN LEE	REV	1.0		ICH8-M (4/5 5/5)
MODULE CODE		LAST EDIT			
October 23, 2007 10:38:02 AM					
				PAGE	23 OF 58

**SAMSUNG**  
 ELECTRONICS  
 PART NO. BA41-XXXXX

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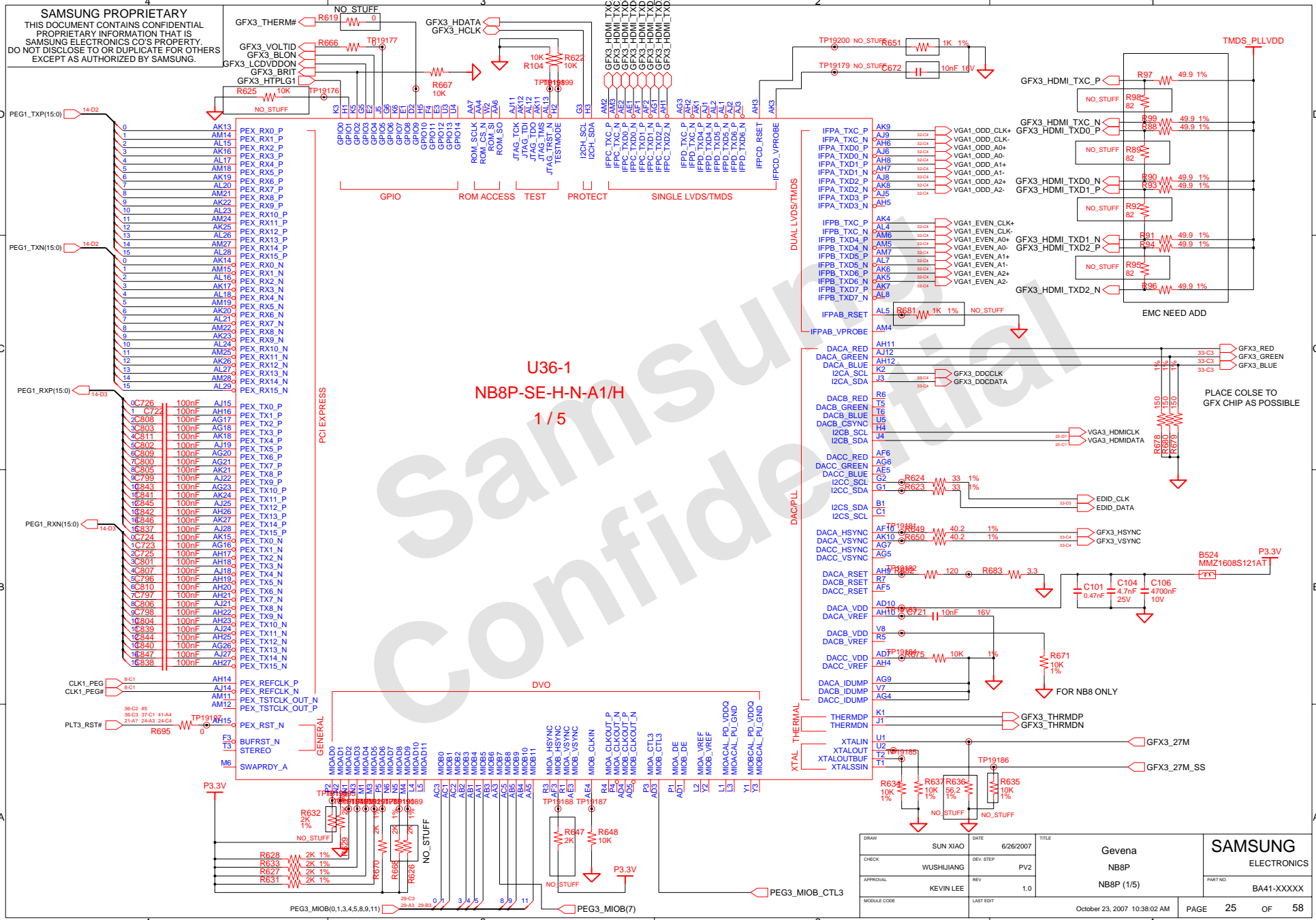


**Model Divalent**



DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena ICH8-M ICH8-M STAP	<b>SAMSUNG</b> ELECTRONICS
CHECK	WUSHUJIANG	DEV STEP	PV2			
APPROVAL	KEVIN LEE	REV	1.0			PART NO. BA41-XXXXX
MODULE CODE		LAST EDIT	October 23, 2007 10:38:02 AM	PAGE	24	OF 58





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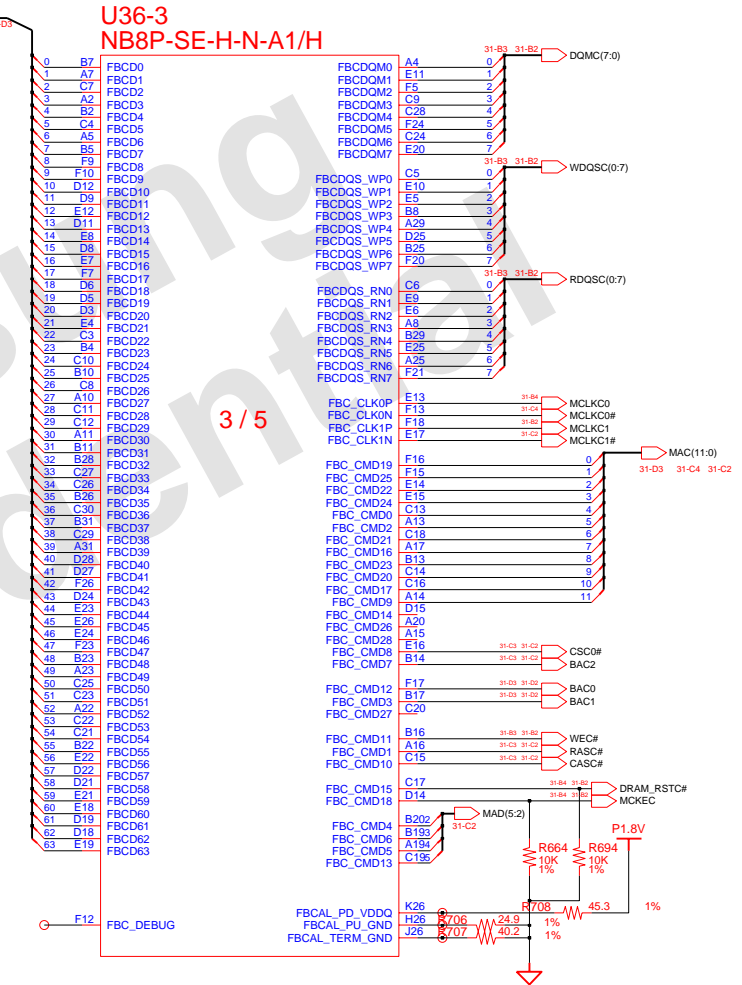
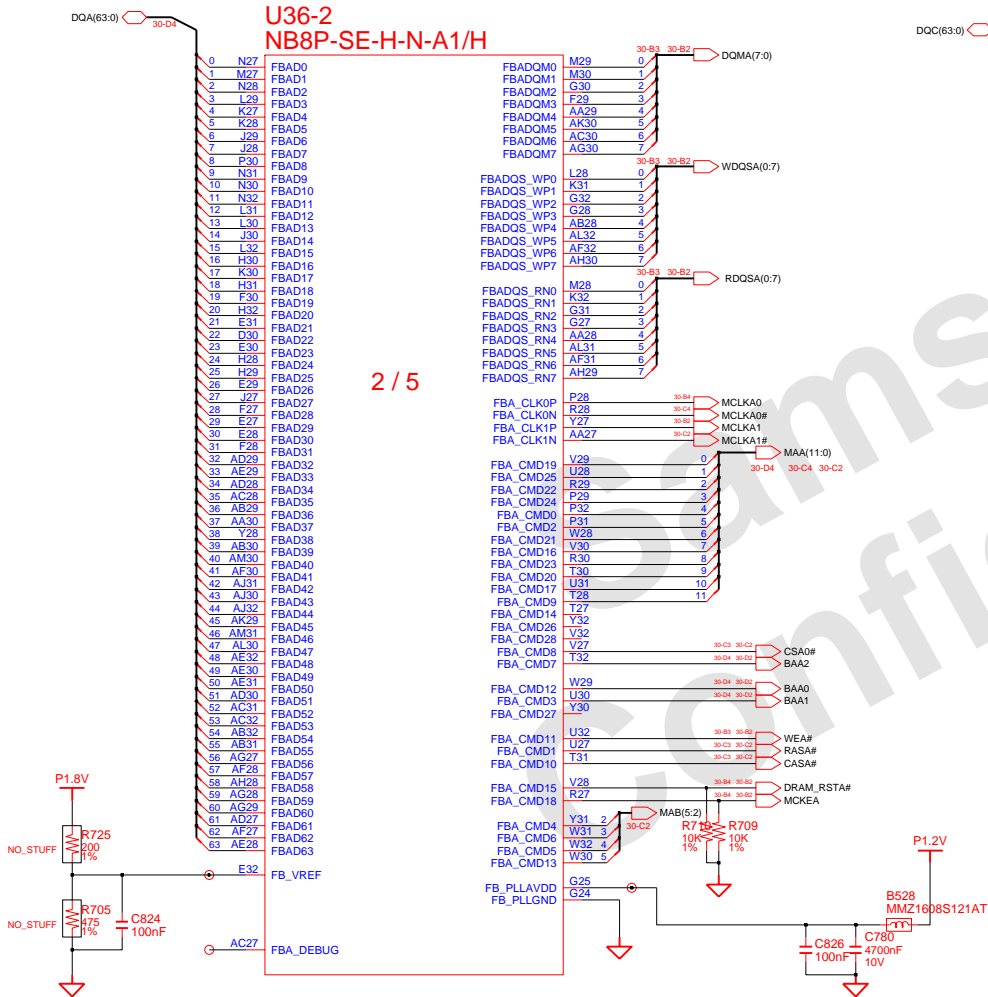
**U36-1**  
**NB8P-SE-H-N-A1/H**  
**1 / 5**

DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena	<b>SAMSUNG</b> ELECTRONICS
CHECK	WUSHUJIANG	DEV. STEP	PV2		NB8P	
APPROVAL	KEVIN LEE	REV	1.0		NB8P (1/5)	
MODULE CODE		LAST EDIT				
				October 23, 2007 10:38:02 AM	PAGE	25 OF 58

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### Graphic Memory I/F (Using FBA Channel)

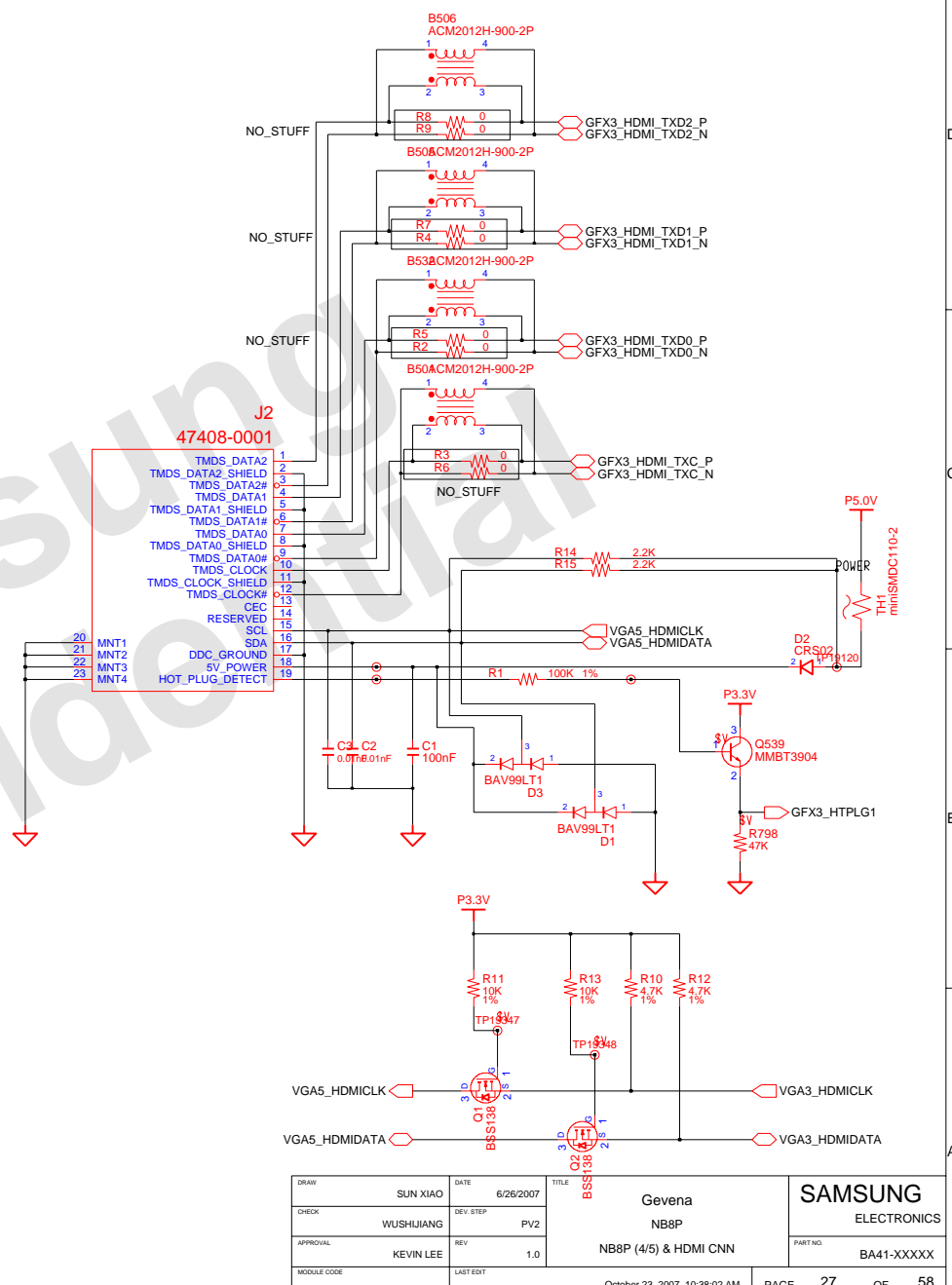
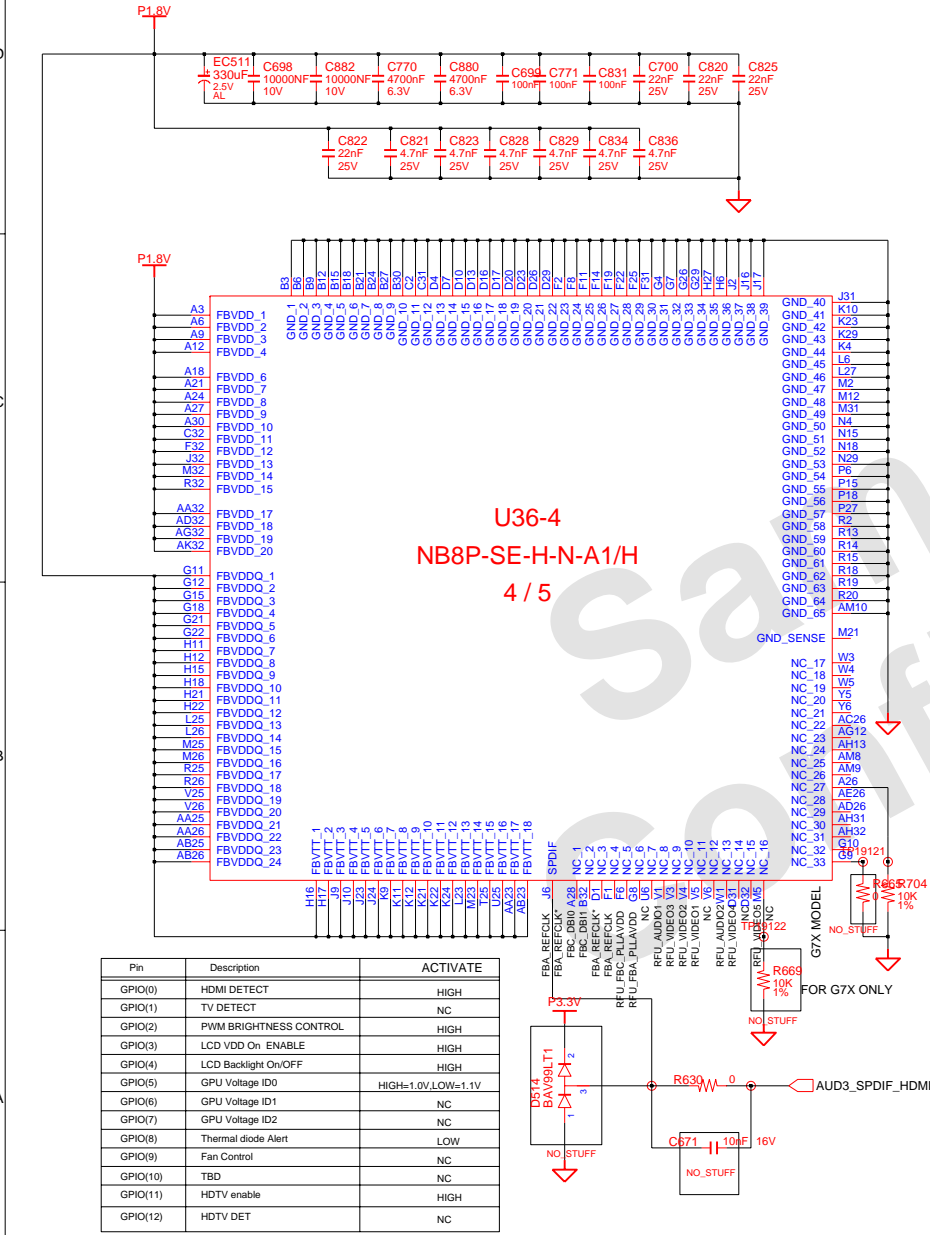
### Graphic Memory I/F (Using FBC Channel)



DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena
CHECK	WUSHUJIANG	DEV STEP	PV2		NB8P
APPROVAL	KEVIN LEE	REV	1.0		NB8P (2/5 3/5)
MODULE CODE		LAST ENT			
				October 23, 2007 10:38:02 AM	PAGE 26 OF 58

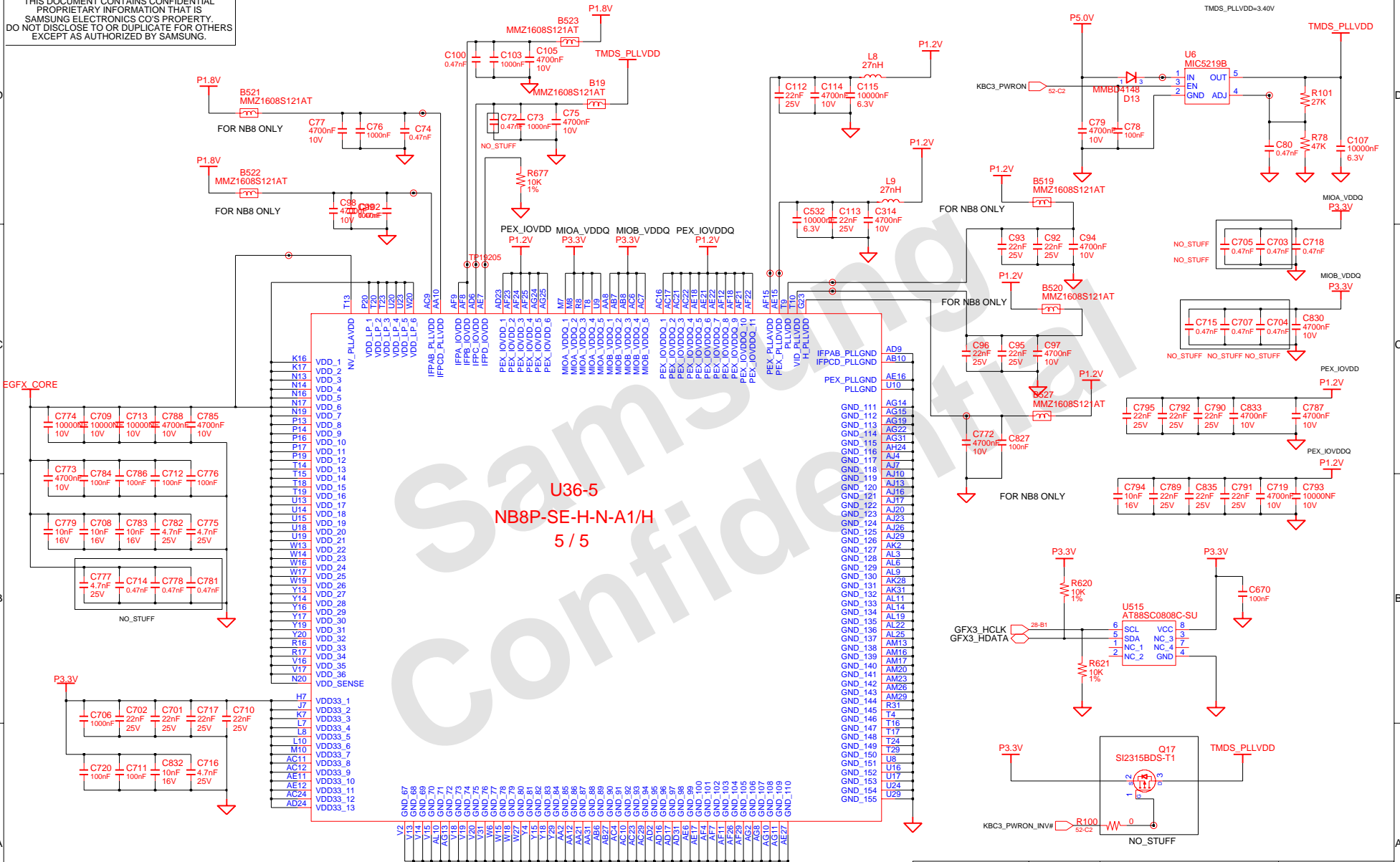
**SAMSUNG**  
 ELECTRONICS  
 PART NO. BA41-XXXXX

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DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena	SAMSUNG ELECTRONICS	
CHECK	WUSHUJIANG	DEV STEP	PV2		NB8P		
APPROVAL	KEVIN LEE	REV	1.0		NB8P (4/5) & HDMI CNN	PART NO. BA41-XXXXX	
MODULE CODE		LAST EDIT					
October 23, 2007 10:38:02 AM						PAGE	27 OF 58

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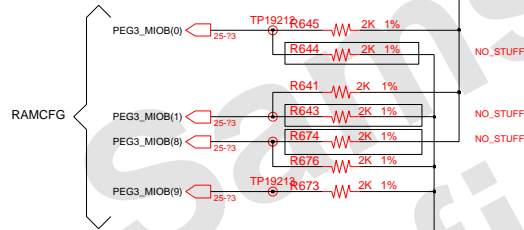
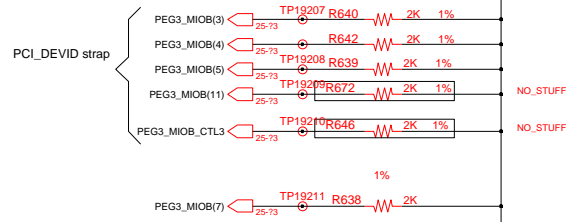
**U36-5**  
**NB8P-SE-H-N-A1/H**  
 5 / 5

DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena	<b>SAMSUNG</b> ELECTRONICS
CHECK	WUSHUJIANG	DEV STEP	PV2		NB8P	
APPROVAL	KEVIN LEE	REV	1.0		NB8P (5/5)	PART NO. BA41-XXXXX
MODULE CODE		LAST EDIT		October 23, 2007 10:38:02 AM	PAGE	28 OF 58

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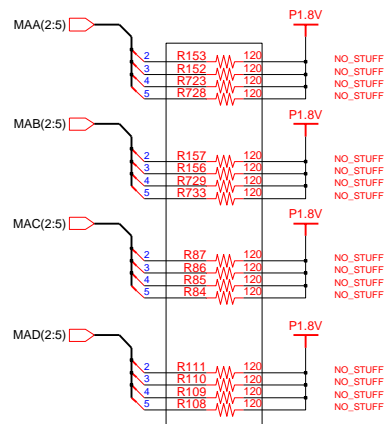
PCI\_DEVID strap

	R646	R672	R640	R639	R642
NB8P-SE	NO_STUFF	NO_STUFF	STUFF	NO_STUFF	STUFF
NB8M-GS	0	0	1	1	1
	NO_STUFF	NO_STUFF	STUFF	STUFF	STUFF
	0	0	1	1	1



RAMCFG

	R674	R676	R641	R643
SS 256Mbit	STUFF	NO_STUFF	STUFF	NO_STUFF
IF 256Mbit	STUFF	NO_STUFF	NO_STUFF	STUFF
SS 512Mbit	NO_STUFF	STUFF	STUFF	NO_STUFF
IF 512Mbit	NO_STUFF	STUFF	NO_STUFF	STUFF



Straps	Pin # (Rev.A02)	Descriptions
SUB_VENDOR	MIOAD(1)	0 : No BIOS 1 : Read from BIOS
RAMCFG(3:0) [9,8,1,0]	MIOB(9) MIOB(8) MIOB(1) MIOB(0)	0111 : SAMSUNG GDDR3 256Mbit 0101 : INFINEON GDDR3 256Mbit 0011 : SAMSUNG GDDR3 512Mbit 0001 : INFINEON GDDR3 512Mbit
CRYSTAL(1:0)	MIOB(2) MIOB(6)	01 : 14.318 MHz 10 : 27 MHz 11 : Unknown 00 : 13.5 MHz
TV_MODE(1:0)	MIOAD(7) MIOAD(10)	00 : SECAM 01 : NTSC 10 : PAL 11 : CRT
PCI_DEVID(4:0) [CTL3,11,3,5,4]	MIOB_CTL(3) MIOB(11) MIOB(3) MIOB(5) MIOB(4)	NB8M-GS: 00111 NB8M-SE: 01000 NB8M-GT: 00110 NB8P-GS: 00111 NB8P-SE: 00101 NB8P-GT: 01000
ROM_TYPE(1:0)	MIOB(10) MIOBVSYN	NO ROM(NC)
USER STRAP	MIOAD(2:5)	EDID
GPIO(12:0)	Sheet 25	Refer to Sheet 25

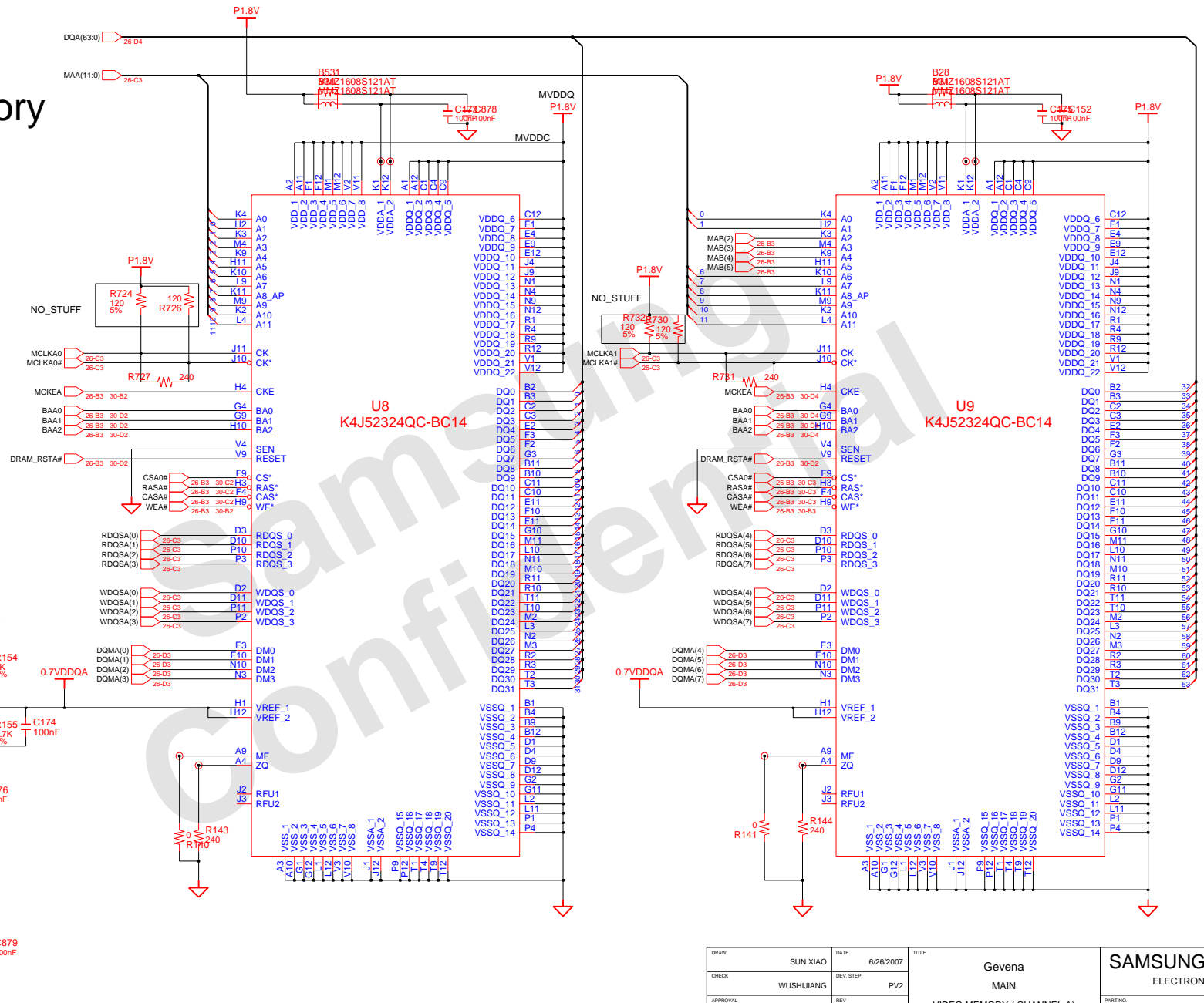
Test Options for GPIO should be updated..

Samsung		Infineon	
256Mbit	512Mbit	256Mbit	512Mbit
K4J55323QG (1.2/1.4/1.6/2.0) K4J55323QF (1.4/1.6/2.0)	K4J52324QC (1.2/1.4/1.6/2.0)	HYB18H256321AF120(2.0) HYB18H256321AF16(1.6) HYB18H256324AF-20(2.0) HYB18H256321AF-14(1.4) HYB18H256321AF-12(1.2)	HYB18H512321AF120(2.0) HYB18H512321AF16(1.6) HYB18H512324AF-20(1.6) HYB18H512321AF-14(1.4) HYB18H512321AF-12(1.2)
8M*32BIT	16M*32BIT	8M*32BIT	16M*32BIT

DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena	SAMSUNG ELECTRONICS
CHECK	WUSHUIJIANG	DEV_STEP	PV2		NB8P	
APPROVAL	KEVIN LEE	REV	1.0		NB8P STRAP	PART NO. BA41-XXXXX
MODULE CODE		LAST EDIT		October 23, 2007 10:38:02 AM	PAGE	29 OF 58

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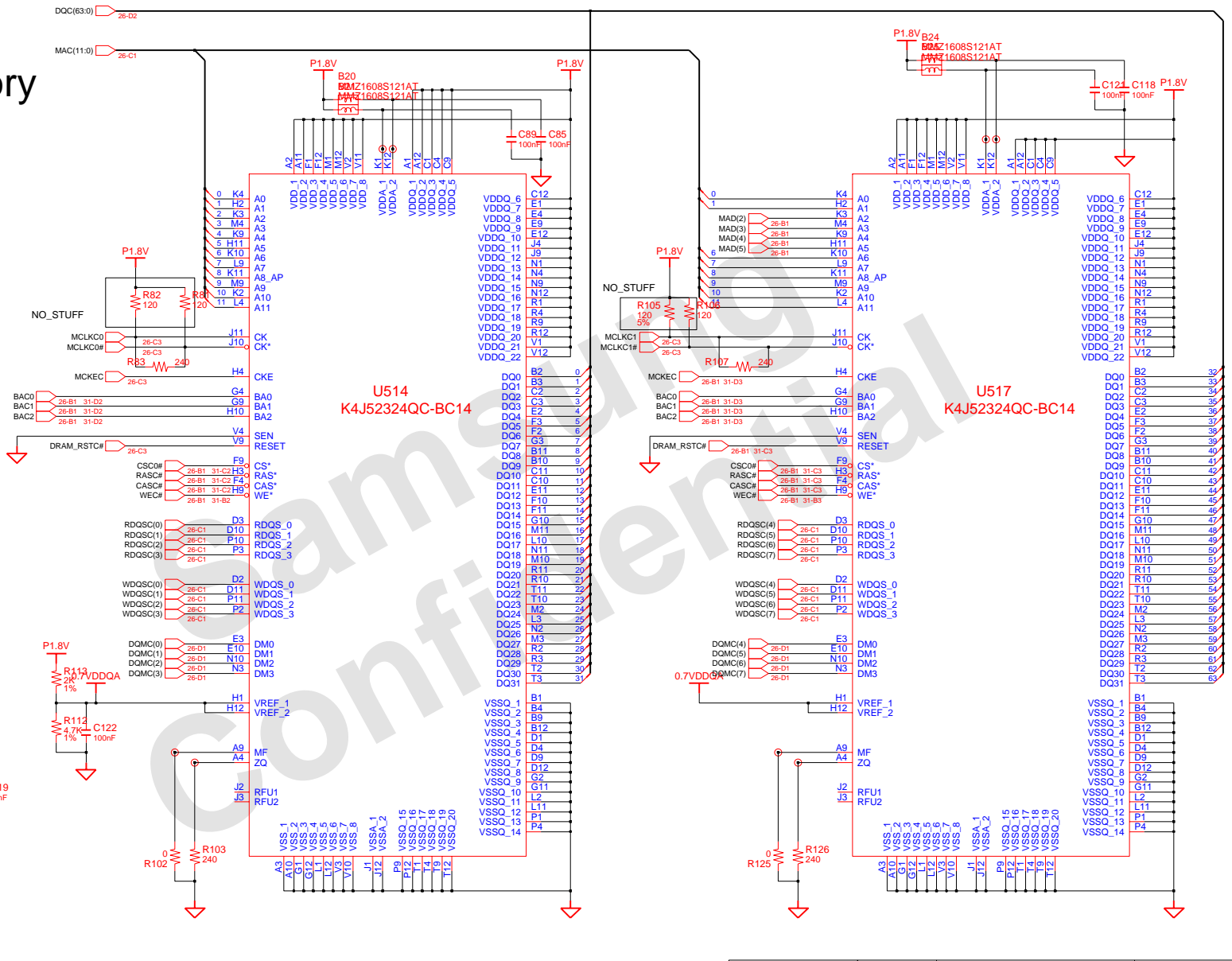
# Video Memory (A Channel)



DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena	SAMSUNG ELECTRONICS
CHECK	WUSHUJIANG	DEV. STEP	PV2	MAIN		
APPROVAL	KEVIN LEE	REV	1.0	VIDEO MEMORY ( CHANNEL A)	PART NO.	BA41-XXXX
MODULE CODE		LAST ENT		October 23, 2007 10:38:02 AM	PAGE	30 OF 58

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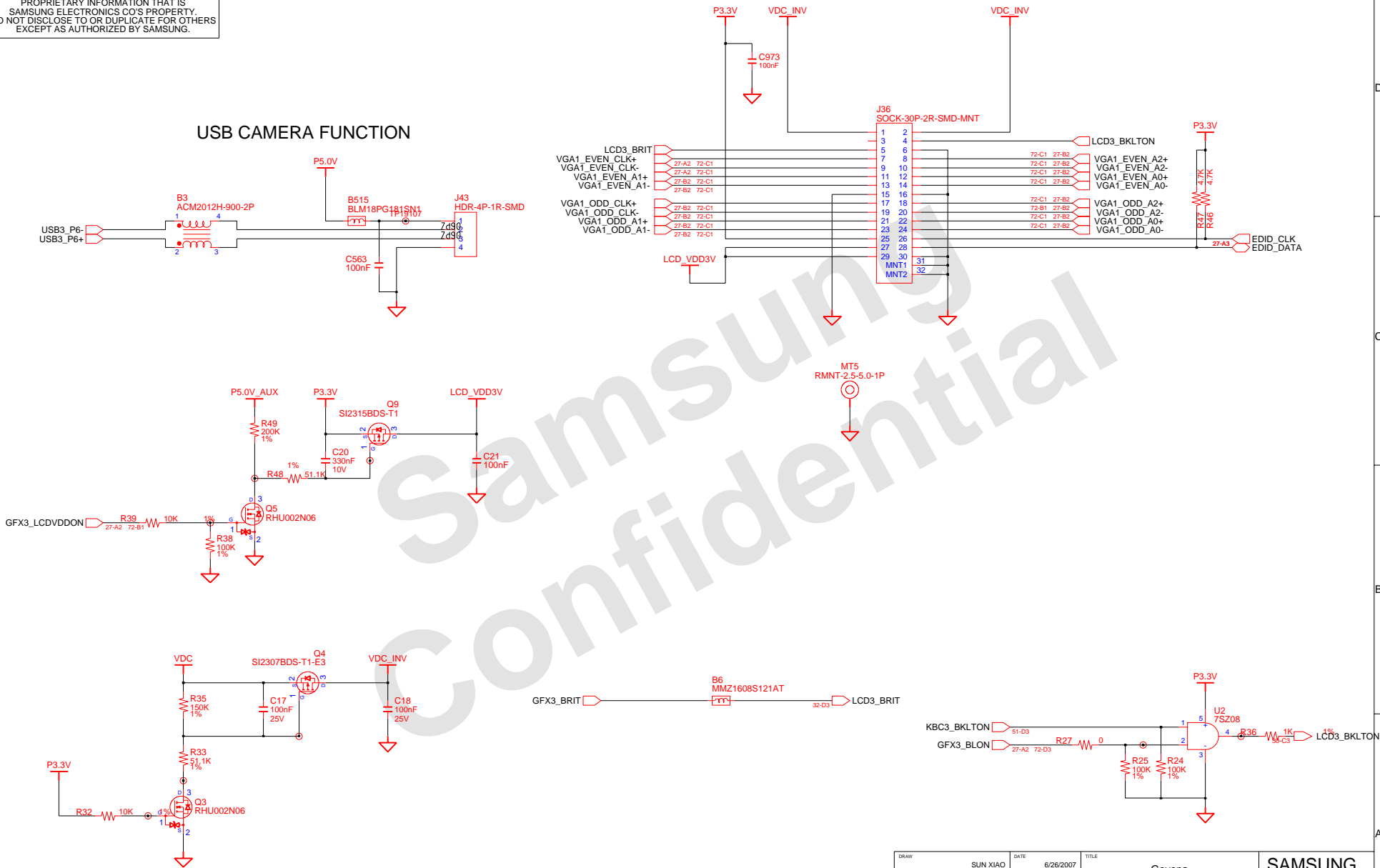
# Video Memory (C Channel)



DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena	SAMSUNG ELECTRONICS
CHECK	WUSHUJIANG	DEV_STEP	PV2	MAIN		
APPROVAL	KEVIN LEE	REV	1.0	VIDEO MEMORY ( CHANNEL B)	PART NO.	BA41-XXXXX
MODULE CODE		LAST ENT			October 23, 2007 10:38:02 AM	PAGE 31 OF 58

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### USB CAMERA FUNCTION

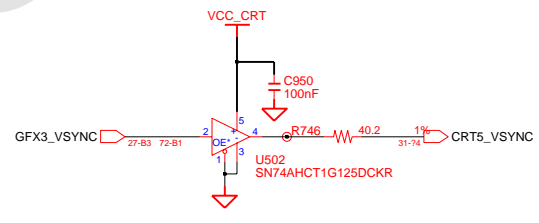
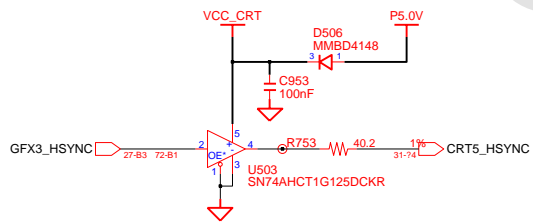
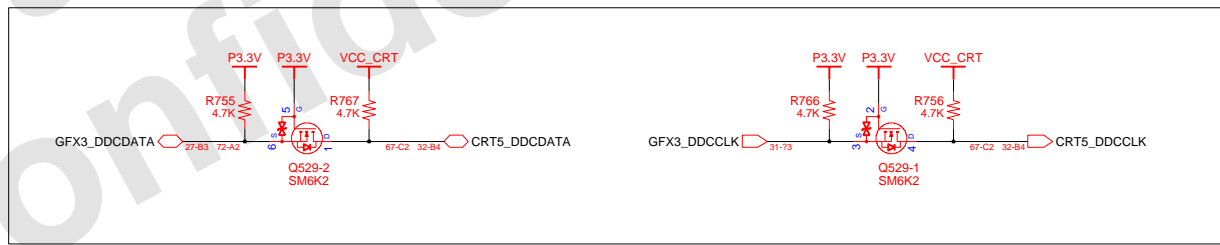
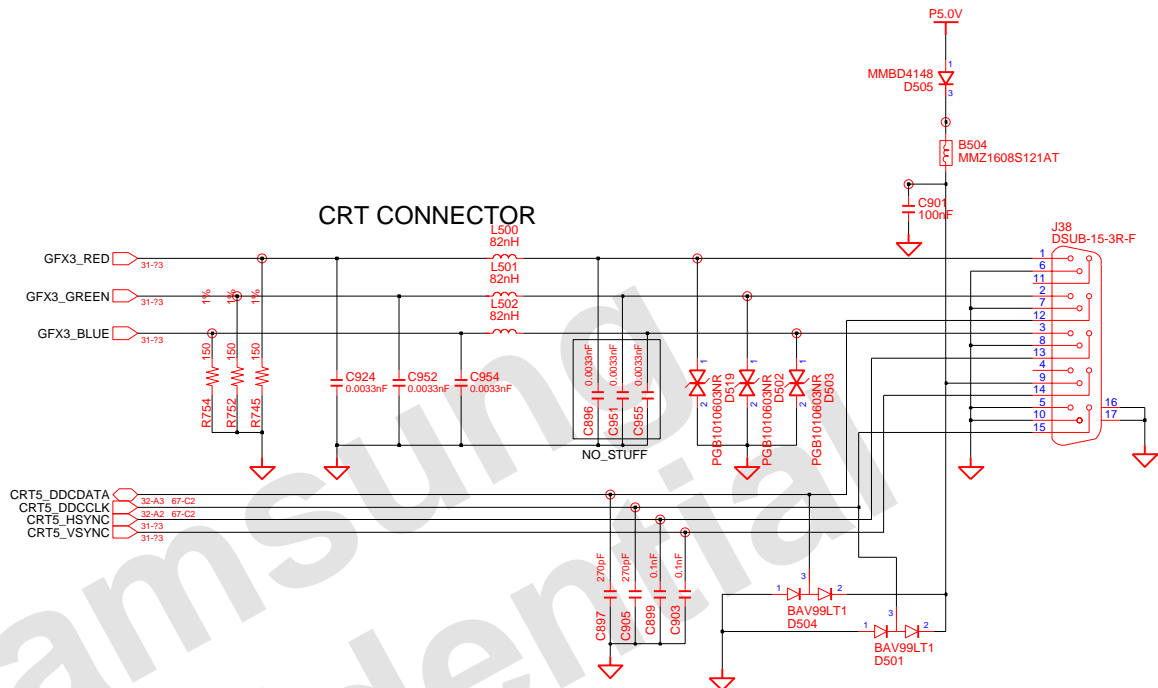


DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Geneva	SAMSUNG ELECTRONICS	
CHECK	WUSHUIJIANG	DEV. STEP	PV2		LCD CONNECTER & SPEED SPECTRUM		PART NO. BA41-XXXXX
APPROVAL	KEVIN LEE	REV	1.0				
MODULE CODE		LAST ENT					
October 23, 2007 10:38:02 AM						PAGE	32 OF 58



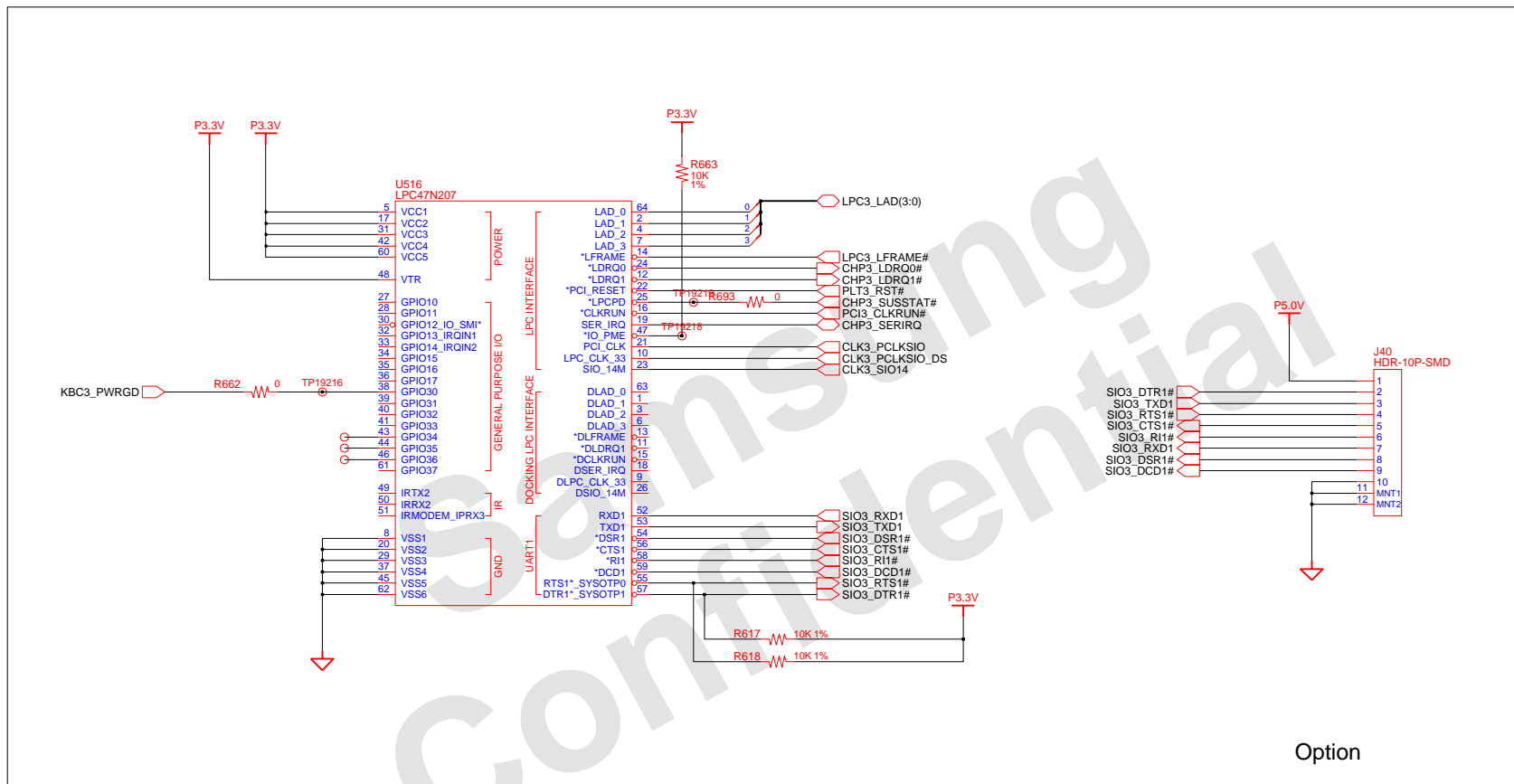
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### CRT CONNECTOR



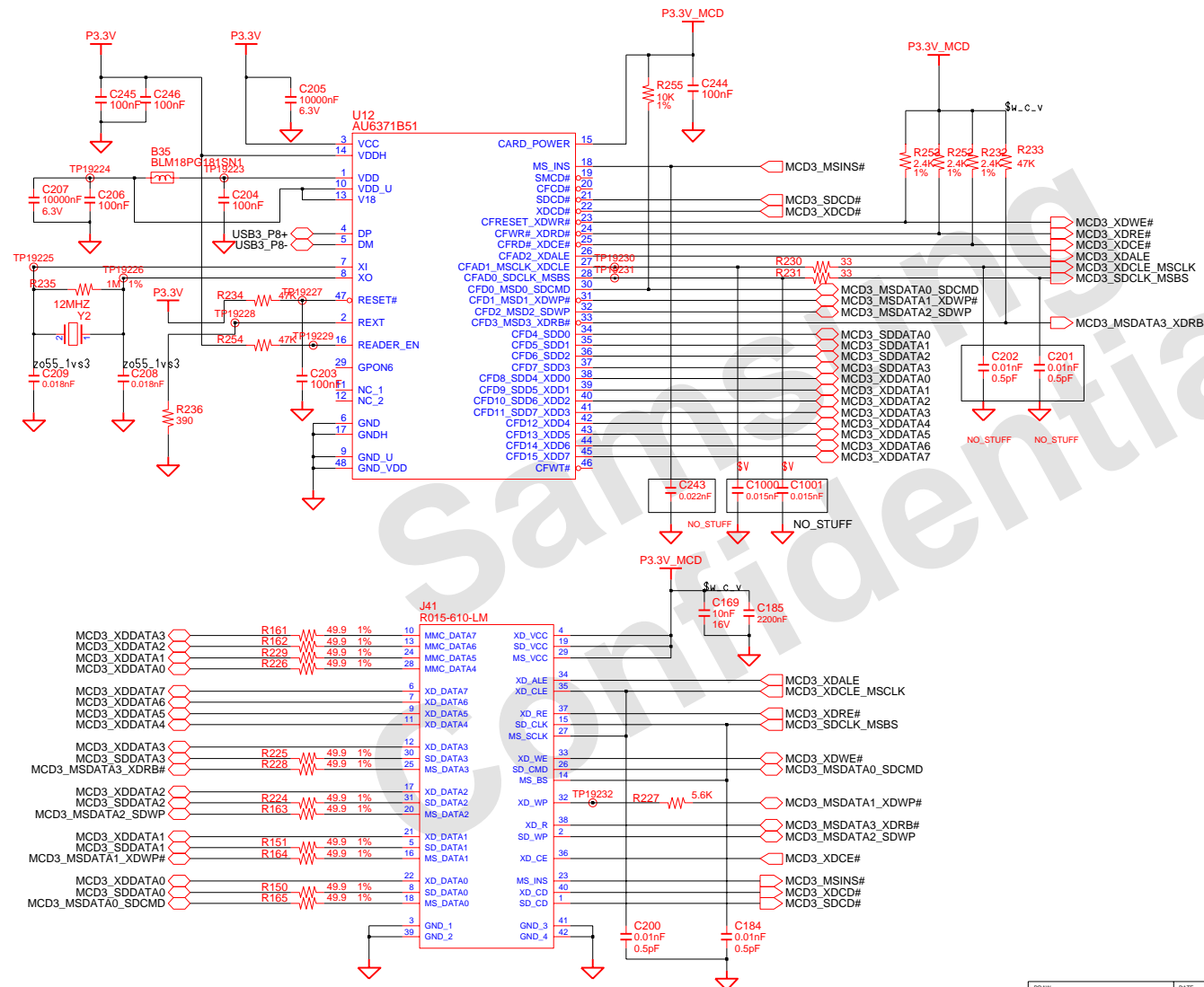
DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Geneva	<b>SAMSUNG</b> ELECTRONICS
CHECK	WUSHUIJIANG	DEV STEP	PV2		MIAN	
APPROVAL	KEVIN LEE	REV	1.0		CRT PORT	PART NO. BA41-XXXXX
MODULE CODE		LAST EDIT		October 23, 2007 10:38:02 AM	PAGE	33 OF 58

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DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena SIO CHIPSET	SAMSUNG ELECTRONICS
CHECK	WUSHUIJIANG	DEV STEP	PV2			
APPROVAL	KEVIN LEE	REV	1.0			PART NO. BA41-
MODULE CODE		LAST EDIT	October 23, 2007 10:38:02 AM	PAGE	34	OF 68

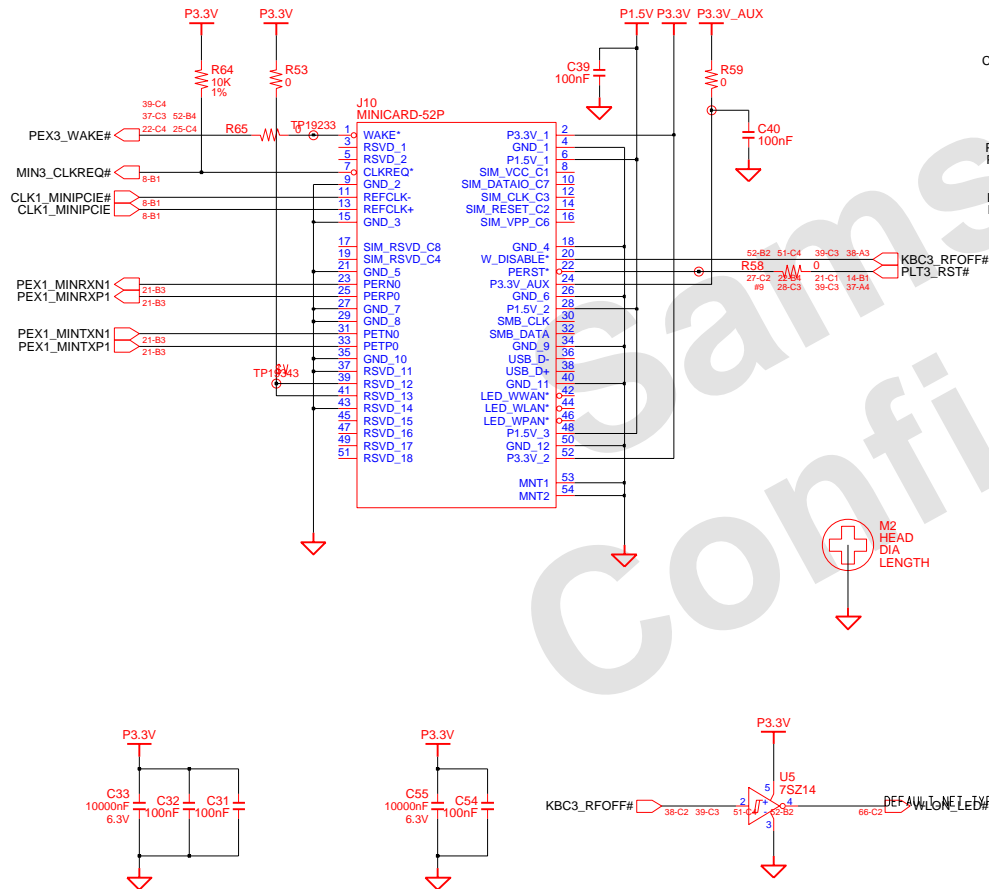
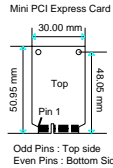
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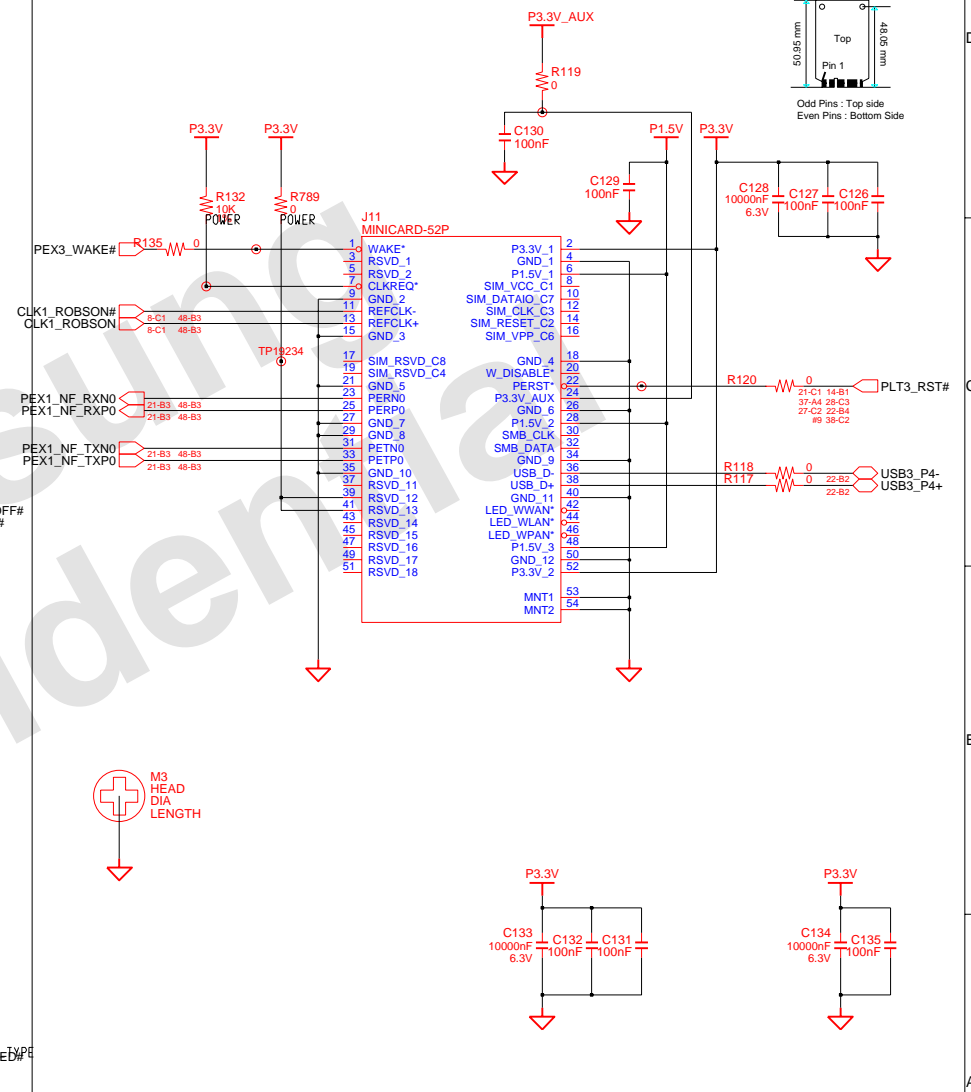
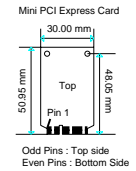
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CHECK	WUSHUJIANG	DEV_STEP	PV2	CARDREADER 7 IN 1		
APPROVAL	KEVIN LEE	REV	1.0			PART NO. BA41-
MODULE CODE		LAST ENT		October 23, 2007 10:38:02 AM	PAGE	35 OF 68

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# Mini Card



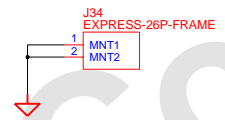
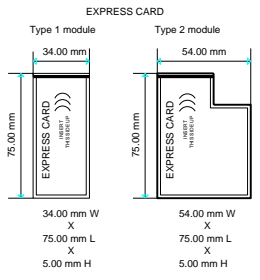
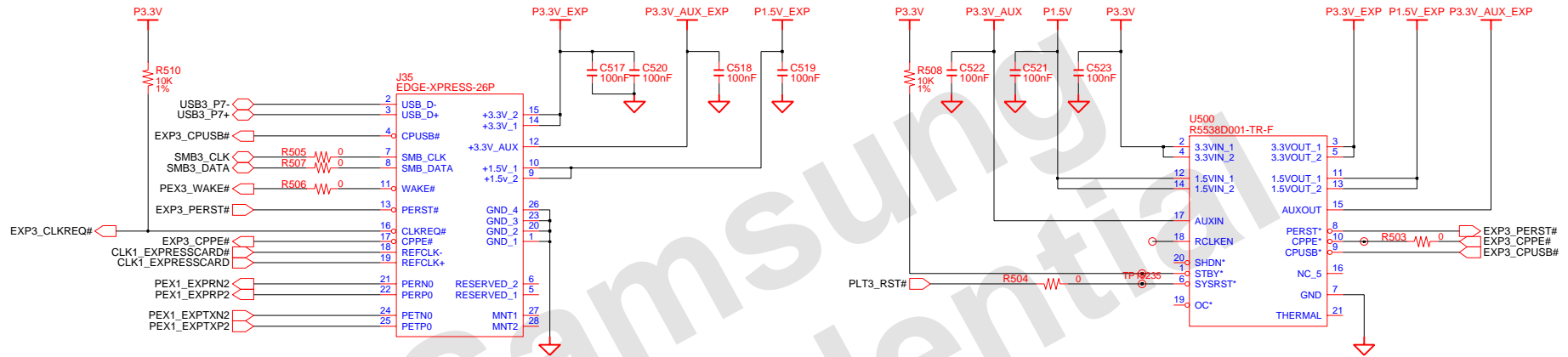
# MINI CARD FOR ROBSON



DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena	SAMSUNG ELECTRONICS
CHECK	WUSHUJIANG	DEV_STEP	PV2	MINI CARD		
APPROVAL	KEVIN LEE	REV	1.0	FRO BOBSON AND DVB-T		PARTNO
MODULE CODE		LAST ENT		October 23, 2007 10:38:02 AM		BA41-XXXXX
PAGE 36 OF 58						

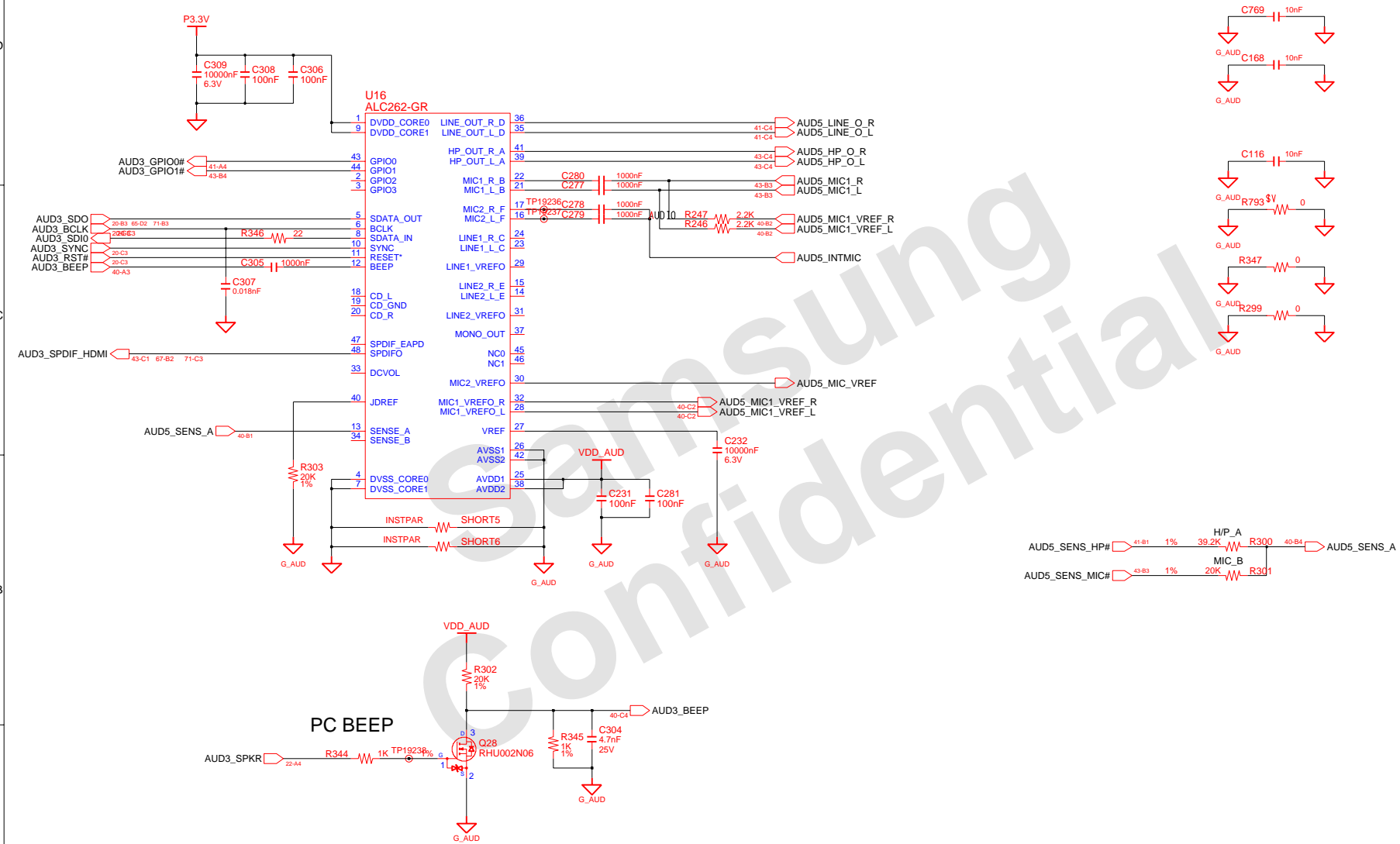
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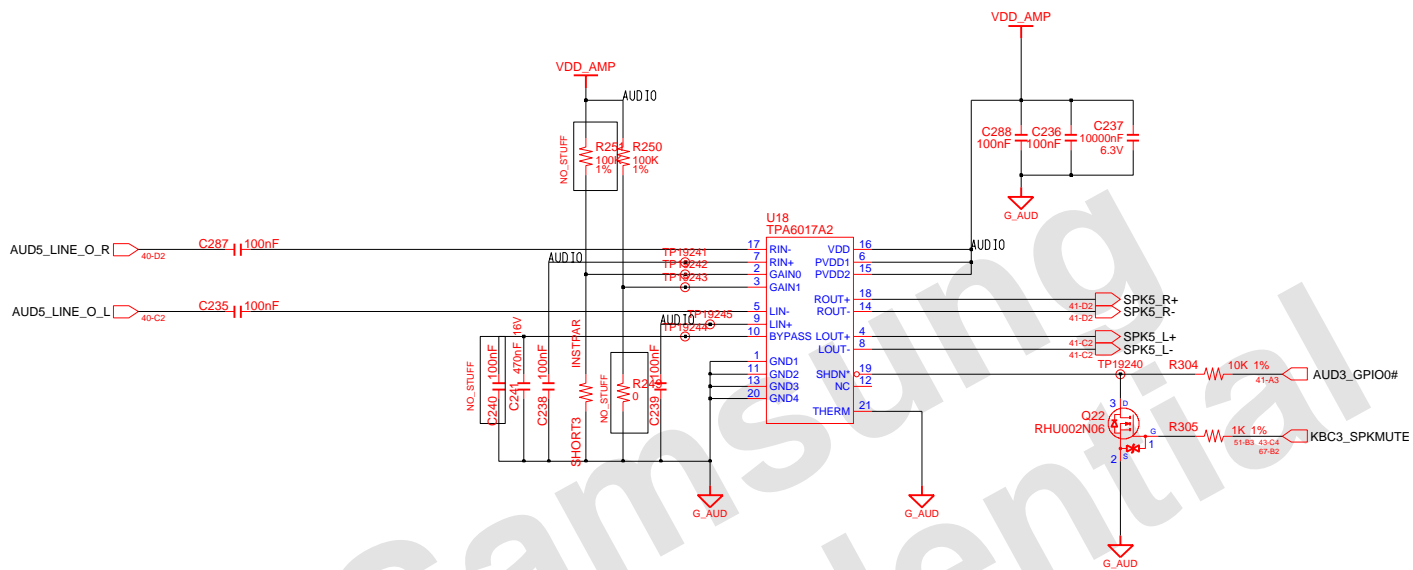
DRAW	SUN XIAO	DATE	6/27/2007	TITLE	Geneva MIO BOARD EXPRESS CARD	<b>SAMSUNG</b> ELECTRONICS
CHECK	WUSHIJIANG	DEV. STEP	PV2	PART NO.		
APPROVAL	KEVIN LEE	REV	1.0	PAGE 37 OF 60		
MODULE CODE	LAST EDIT			October 23, 2007 10:38:02 AM	PAGE 37 OF 60	

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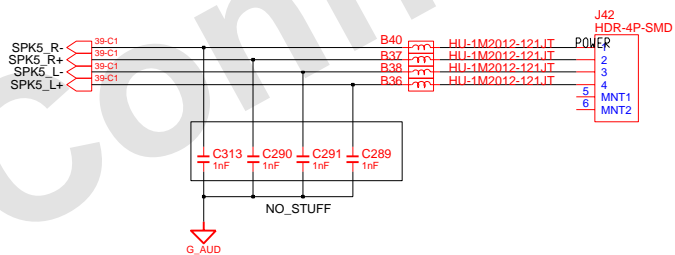


DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena	SAMSUNG ELECTRONICS
CHECK	WUSHUIJIANG	DEV STEP	PV2	AUDIO CODEC	FRO HDMI	
APPROVAL	KEVIN LEE	REV	1.0			PART NO. BA41-XXXXX
MODULE CODE		LAST EDIT				
				October 23, 2007 10:38:02 AM	PAGE	38 OF 58

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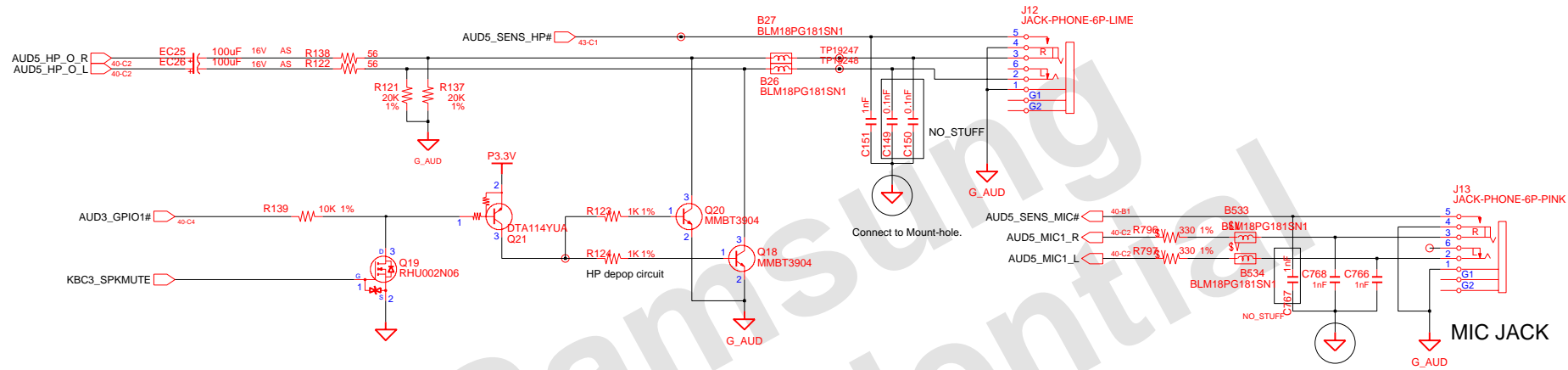
**INTERNAL STEREO SPEAKERS**



DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena	SAMSUNG ELECTRONICS			
CHECK	WUSHUIJIANG	DEV STEP	PV2	AUDIO	AUDIO				
APPROVAL	KEVIN LEE	REV	1.0	AMP	AMP				
MODULE CODE		LAST EDIT	October 23, 2007 10:38:02 AM						
						PAGE	39	OF	58

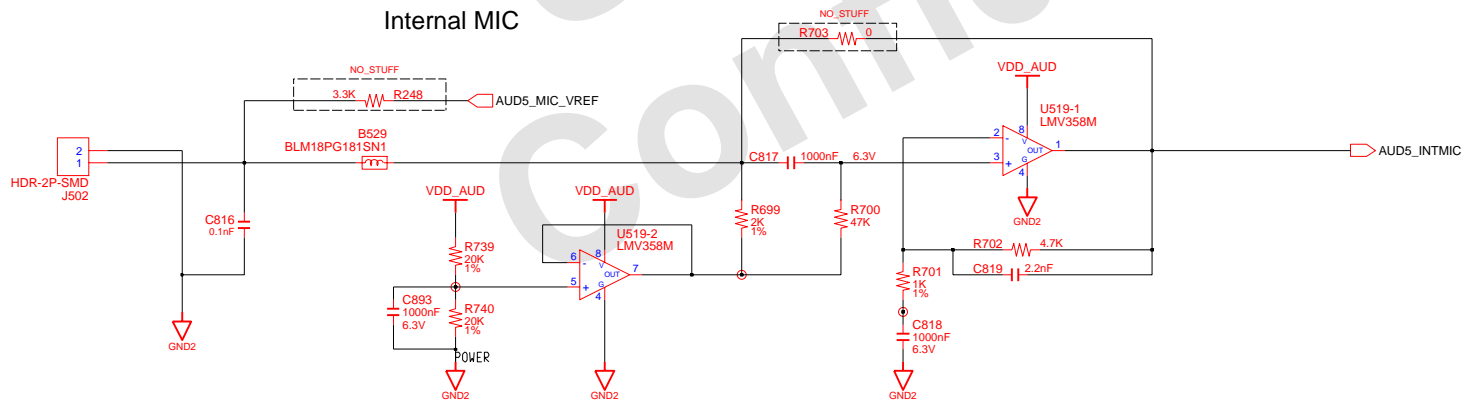
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### HEADPHONE



The traces led to Audio Jacks have the width over 10mil

### Internal MIC

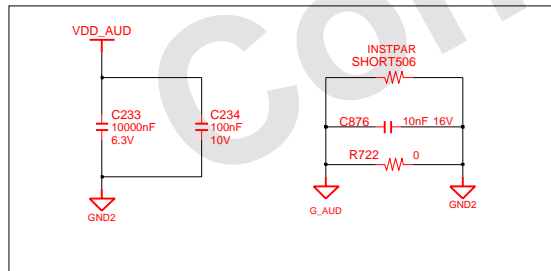
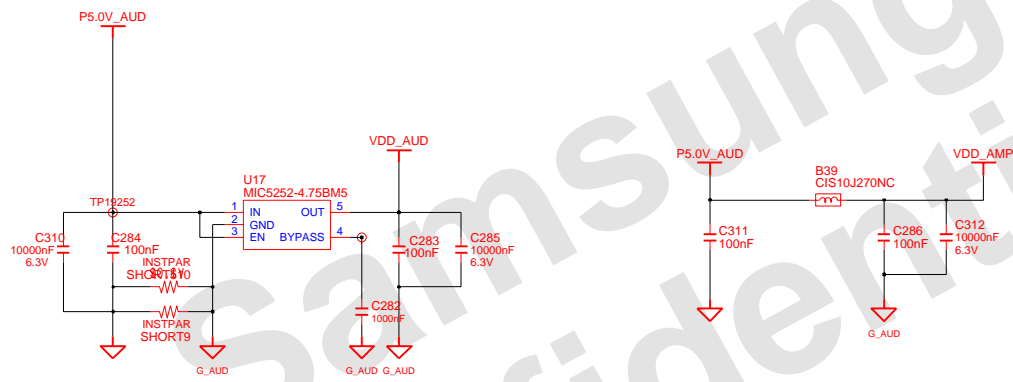


DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena	SAMSUNG ELECTRONICS
CHECK	WUSHUIJIANG	DEV. STEP	PV2	HEAD PHONE JACK	PART NO.	
APPROVAL	KEVIN LEE	REV	1.0	AND MIC JACK	BA41-XXXXX	
MODULE CODE		LAST EDIT		October 23, 2007 10:38:02 AM	PAGE 40 OF 58	



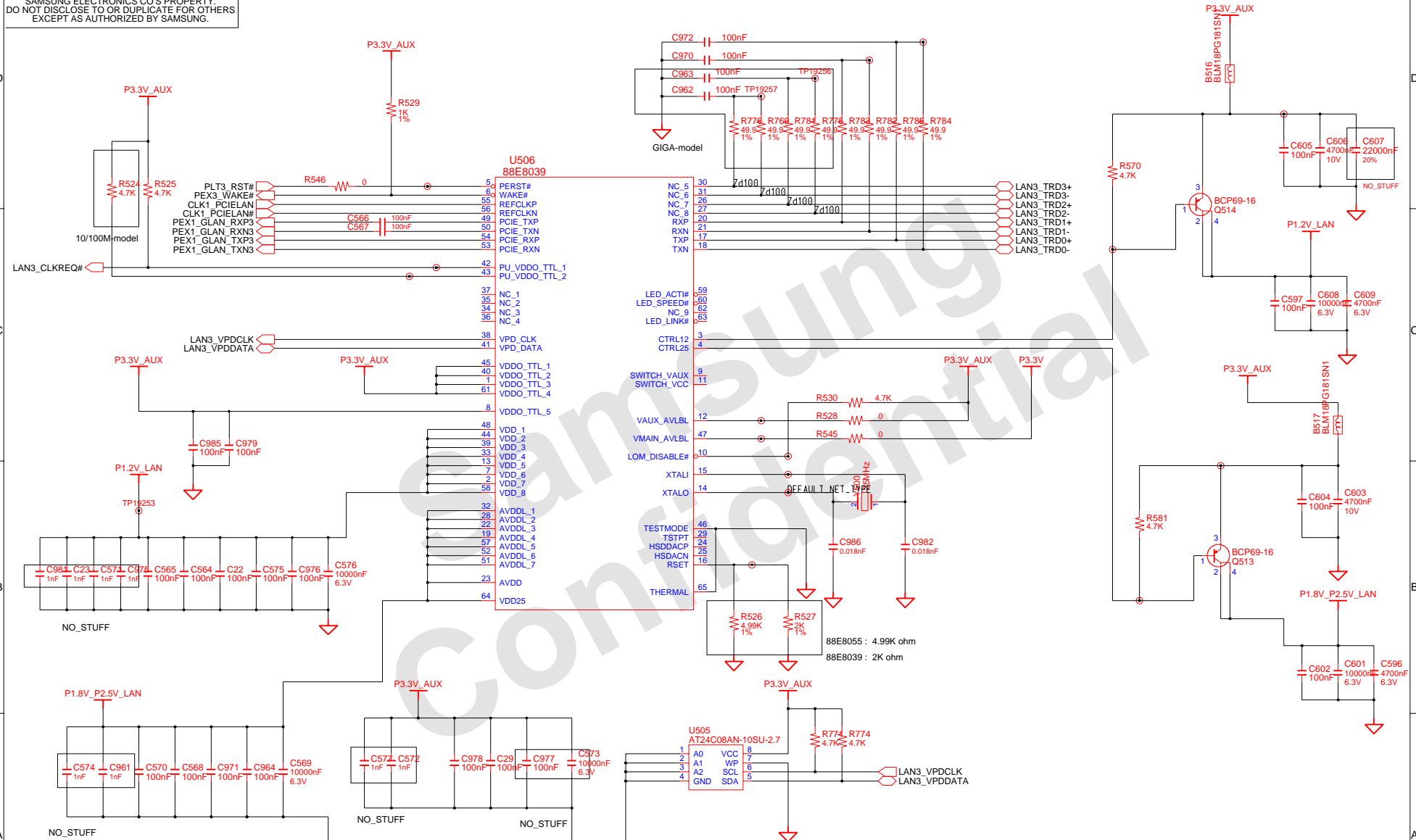
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# AUDIO POWER



DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena AUDIO AUDIO POWER	SAMSUNG ELECTRONICS
CHECK	WUSHUIJIANG	DEV. STEP	PV2			
APPROVAL	KEVIN LEE	REV	1.0			
MODULE CODE		LAST EDIT	October 23, 2007 10:38:02 AM	PAGE 41 OF 58		
					PART NO.	BA41-XXXXX

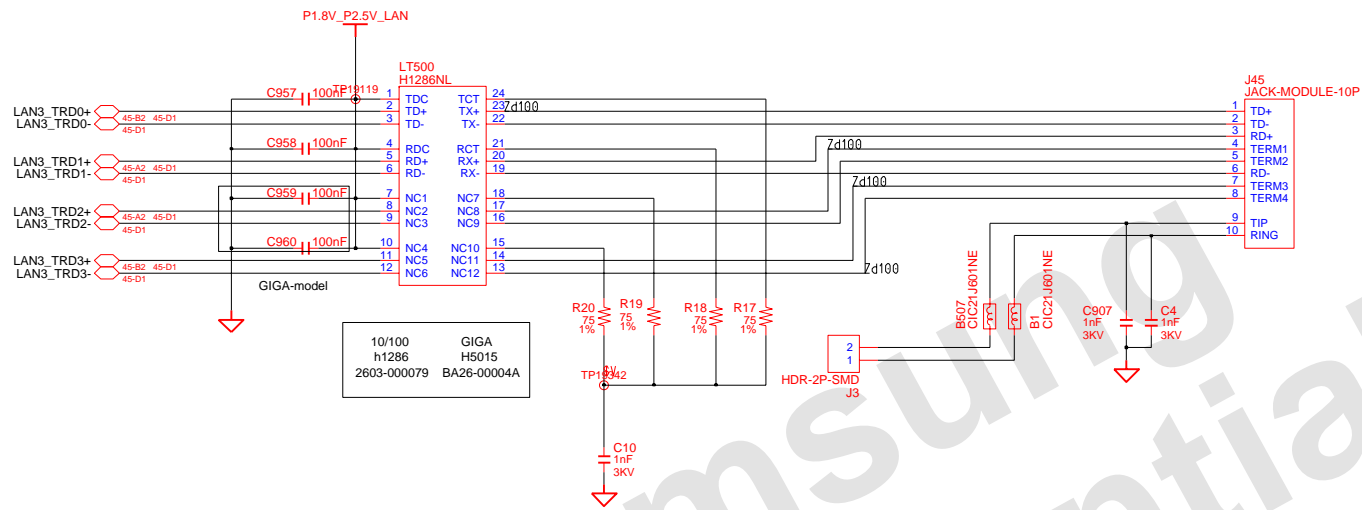
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DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Geneva	SAMSUNG ELECTRONICS
CHECK	WUSHUJIANG	DEV STEP	PV2		LAN	
APPROVAL	KEVIN LEE	REV	1.0		88E8055	PART NO. BA41-XXXXX
MODULE CODE		LAST EDIT		October 23, 2007 10:38:02 AM	PAGE	42 OF 58

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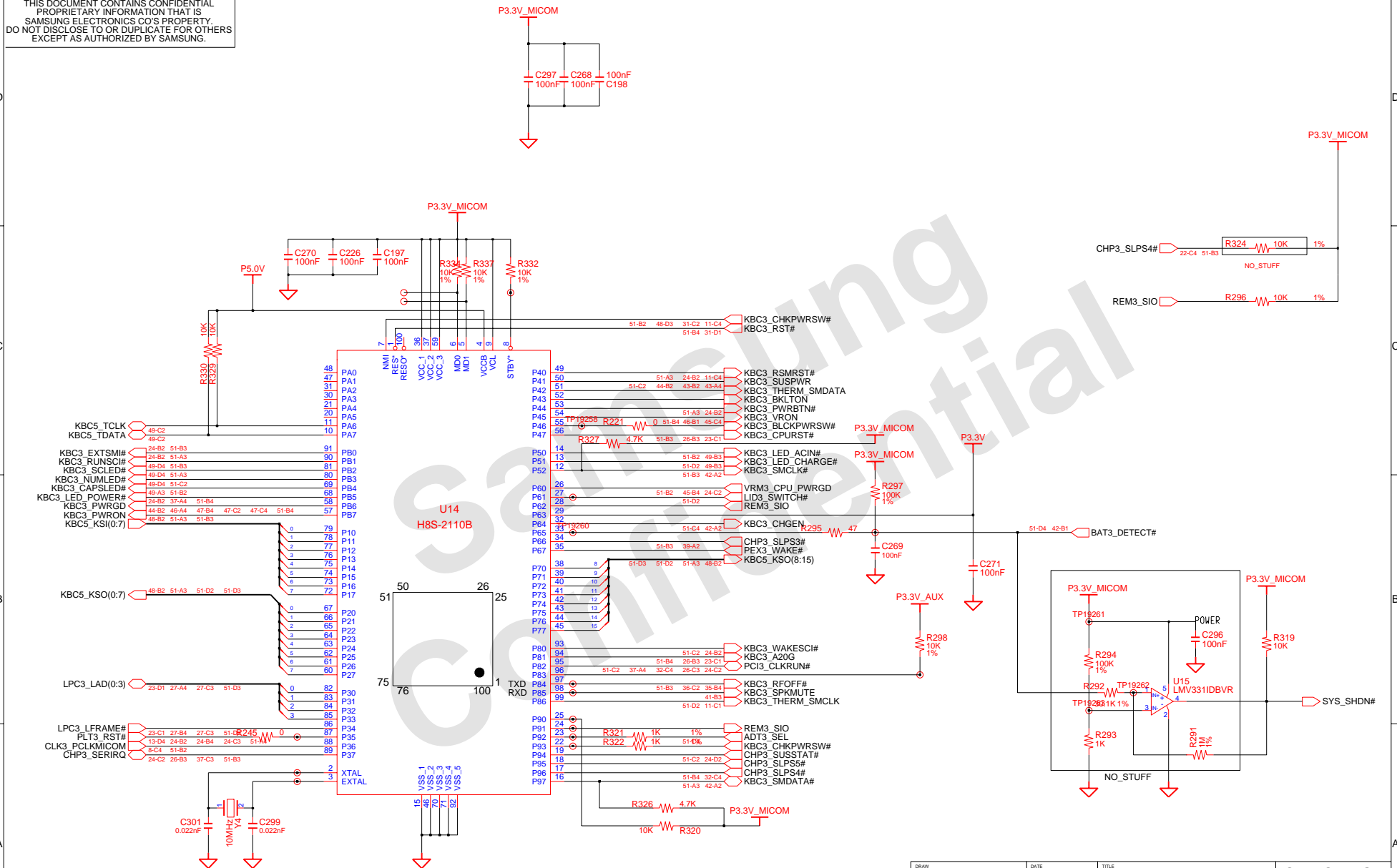
The distance between LAN controller  
 and transformer is designed to extend less than two inches.



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DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena LAN LAN JACK RJ45	<b>SAMSUNG</b> ELECTRONICS
CHECK	WUSHUJIANG	DEV. STEP	PV2			
APPROVAL	KEVIN LEE	REV	1.0			PART NO. BA41-XXXXX
MODULE CODE		LAST EDIT	October 23, 2007 10:38:02 AM	PAGE	43	OF 58

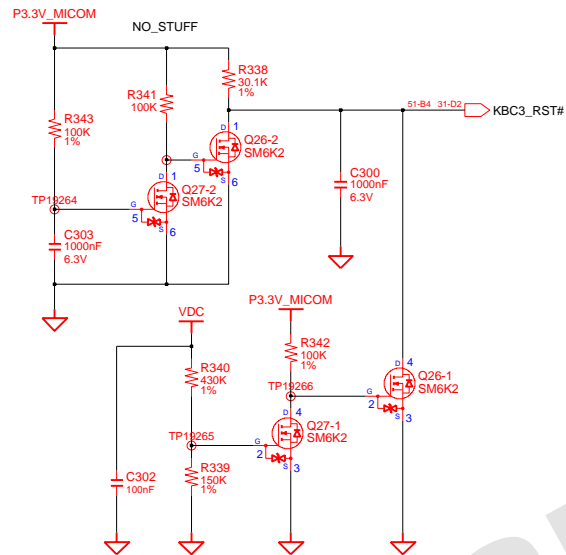
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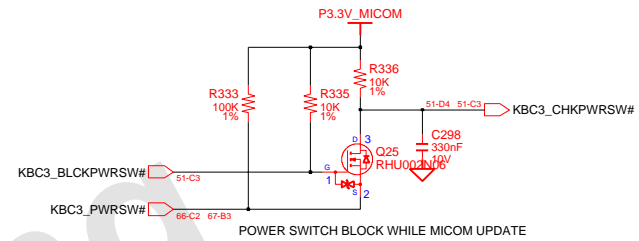
DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Geneva	SAMSUNG ELECTRONICS
CHECK	WUSHUJIANG	DEV STEP	PV2		MICOM	
APPROVAL	KEVIN LEE	REV	1.0		211B	PART NO. BA41-XXXXX
MODULE CODE		LAST ENT				
				October 23, 2007 10:38:02 AM	PAGE	44 OF 58

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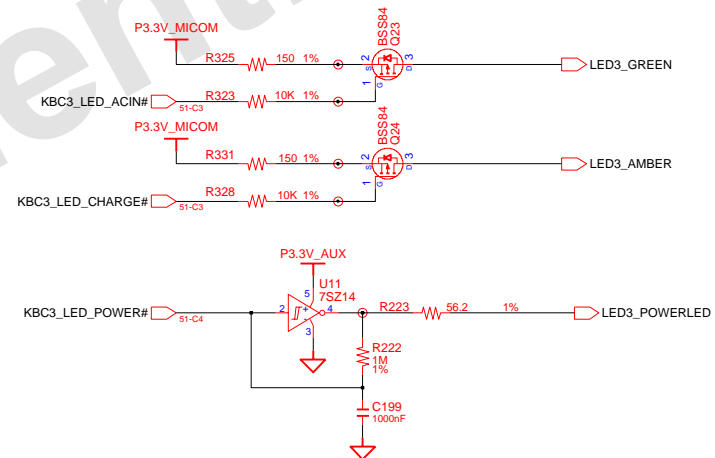
### MICOM RESET



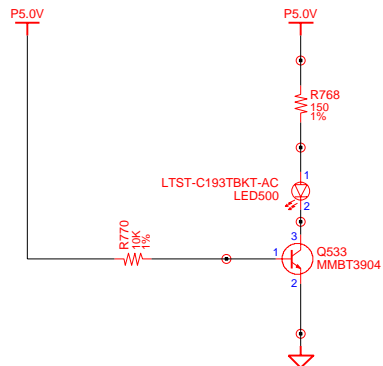
### FOR MICOM UPDATE



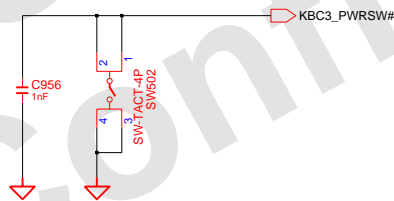
### ADAPTERIN/CHARGING LED



### POWER ON LED



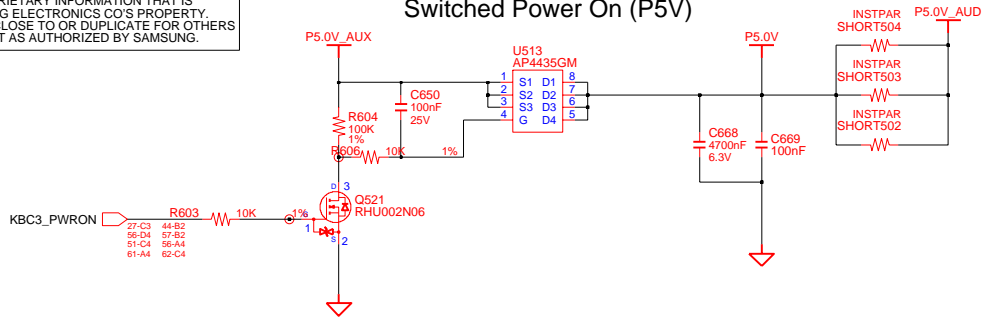
### POWER ON SW BUTTON



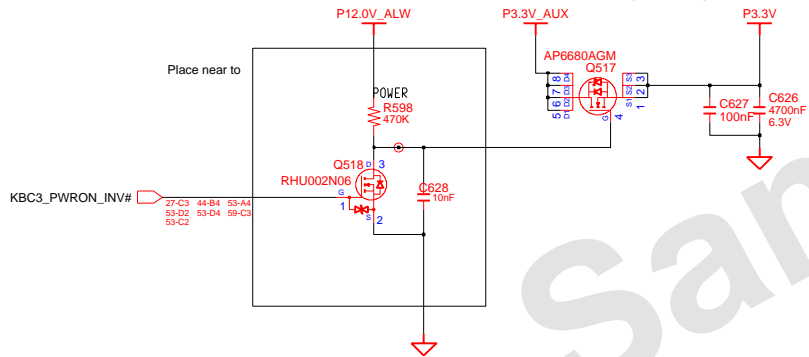
DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena	SAMSUNG ELECTRONICS
CHECK	WUSHUIJIANG	DEV. STEP	PV2		MICOM	
APPROVAL	KEVIN LEE	REV	1.0		MICOM LOGIC SCH	PART NO. BA41-XXXXX
MODULE CODE		LAST EDIT		October 23, 2007 10:38:02 AM	PAGE	45 OF 58

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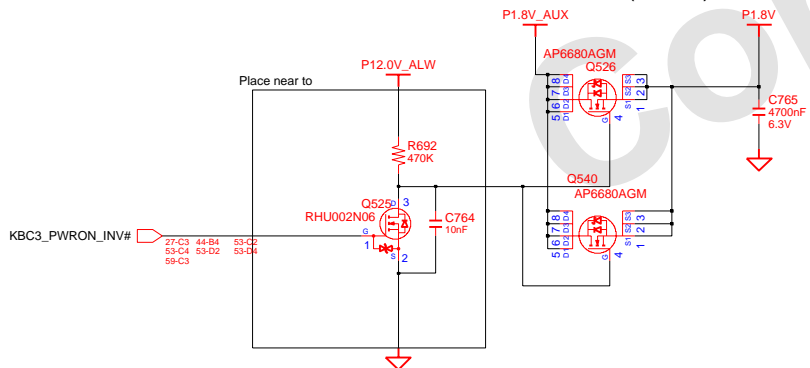
### Switched Power On (P5V)



### Switched Power On (P3.3V)



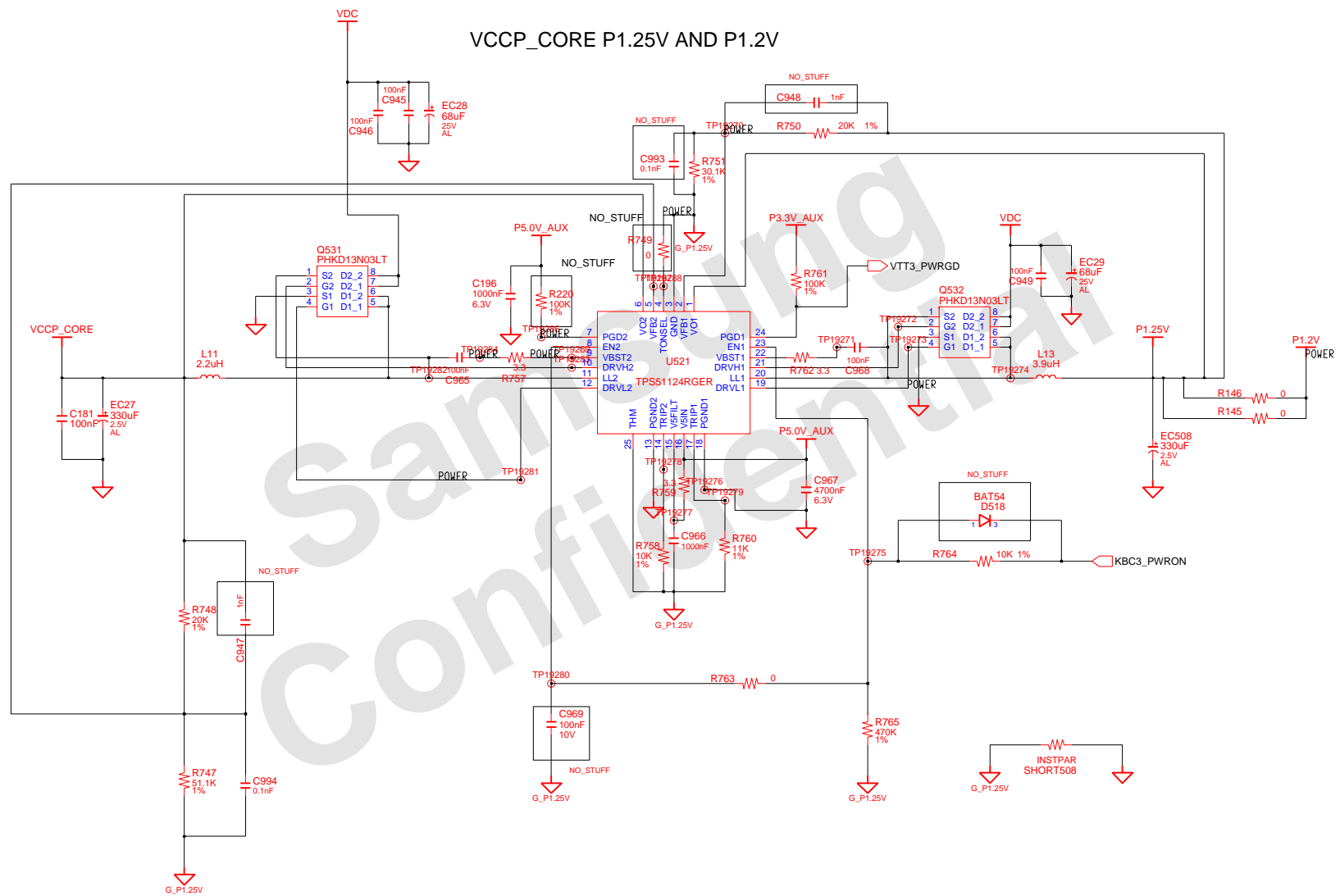
### Switched Power On (P1.8V)



DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena MAIN	SAMSUNG ELECTRONICS
CHECK	WUSHUIJIANG	DEV STEP	PV2	SWITCH POWER P1.5V		
APPROVAL	KEVIN LEE	REV	1.0			PART NO. BA41-XXXXX
MODULE CODE		LAST EDIT	October 23, 2007 10:38:02 AM	PAGE	46	OF 58

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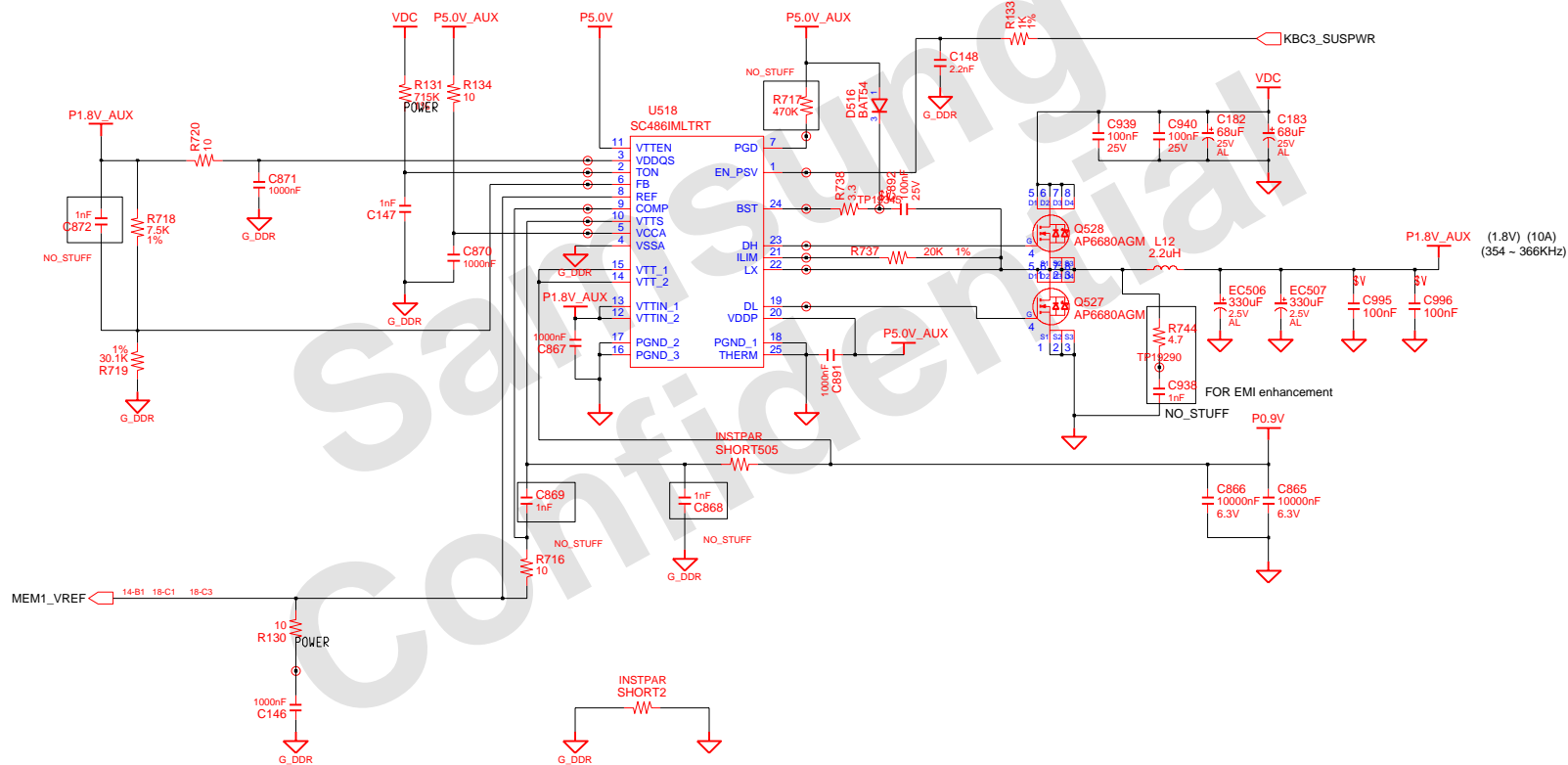
### VCCP\_CORE P1.25V AND P1.2V



DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena	SAMSUNG ELECTRONICS
CHECK	WUSHUJIANG	DEV. STEP	PV2		MAIN	
APPROVAL	KEVIN LEE	REV	1.0		VCCP P1.25V AND P1.2V	PART NO. BA41-XXXXX
MODULE CODE		LAST EDIT			October 23, 2007 10:38:02 AM	PAGE 47 OF 58

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# DDR2 Power

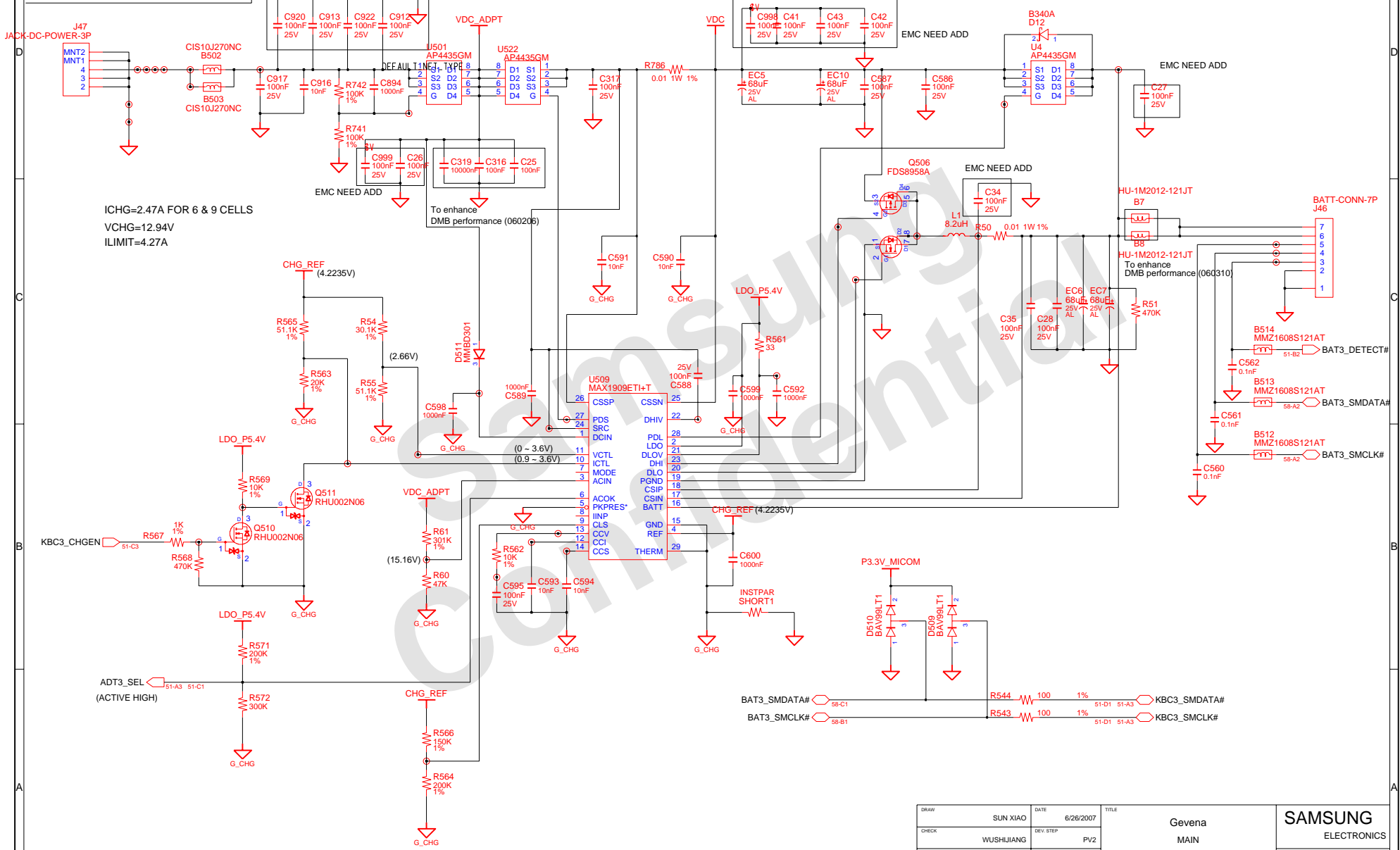


DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena MAIN DDR2 POWER	SAMSUNG ELECTRONICS
CHECK	WUSHUIJANG	DEV. STEP	PV2			
APPROVAL	KEVIN LEE	REV	1.0			PART NO. BA41-XXXXX
MODULE CODE		LAST EDIT			October 23, 2007 10:38:02 AM	PAGE 48 OF 58



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# CHARGER & POWER MANAGEMENT

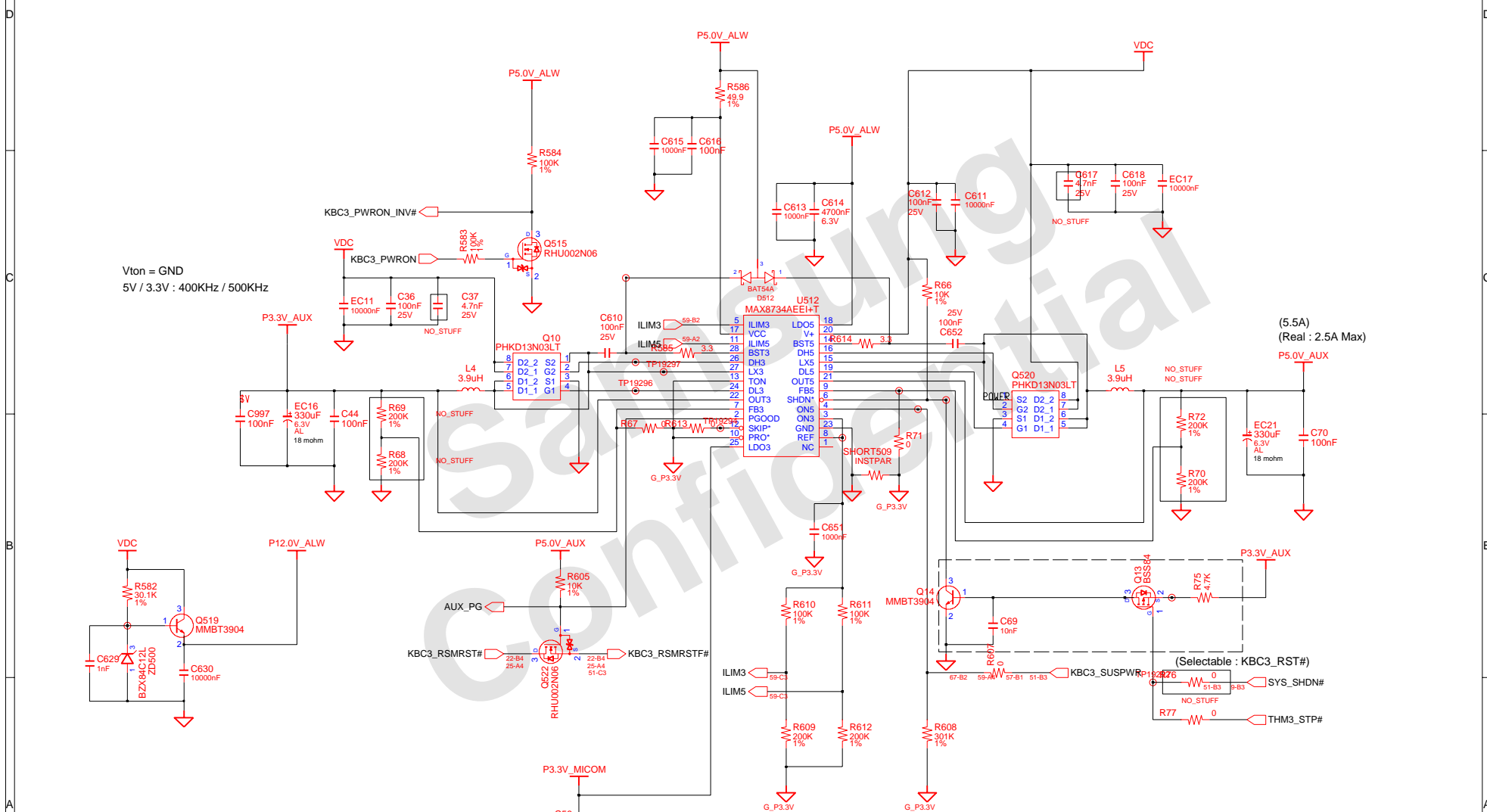


ICHG=2.47A FOR 6 & 9 CELLS  
 VCHG=12.94V  
 ILIMIT=4.27A

DRAW	SUN XIAO	DATE	6/28/2007	TITLE	Gevena MAIN	SAMSUNG ELECTRONICS
CHECK	WUSHUIJANG	DEV STEP	PV2	CHARGE & BATTERY CONN		
APPROVAL	KEVIN LEE	REV	1.0	PART NO.		BA41-XXXX
MODULE CODE		LAST EDIT		October 23, 2007 10:38:02 AM		PAGE 49 OF 58

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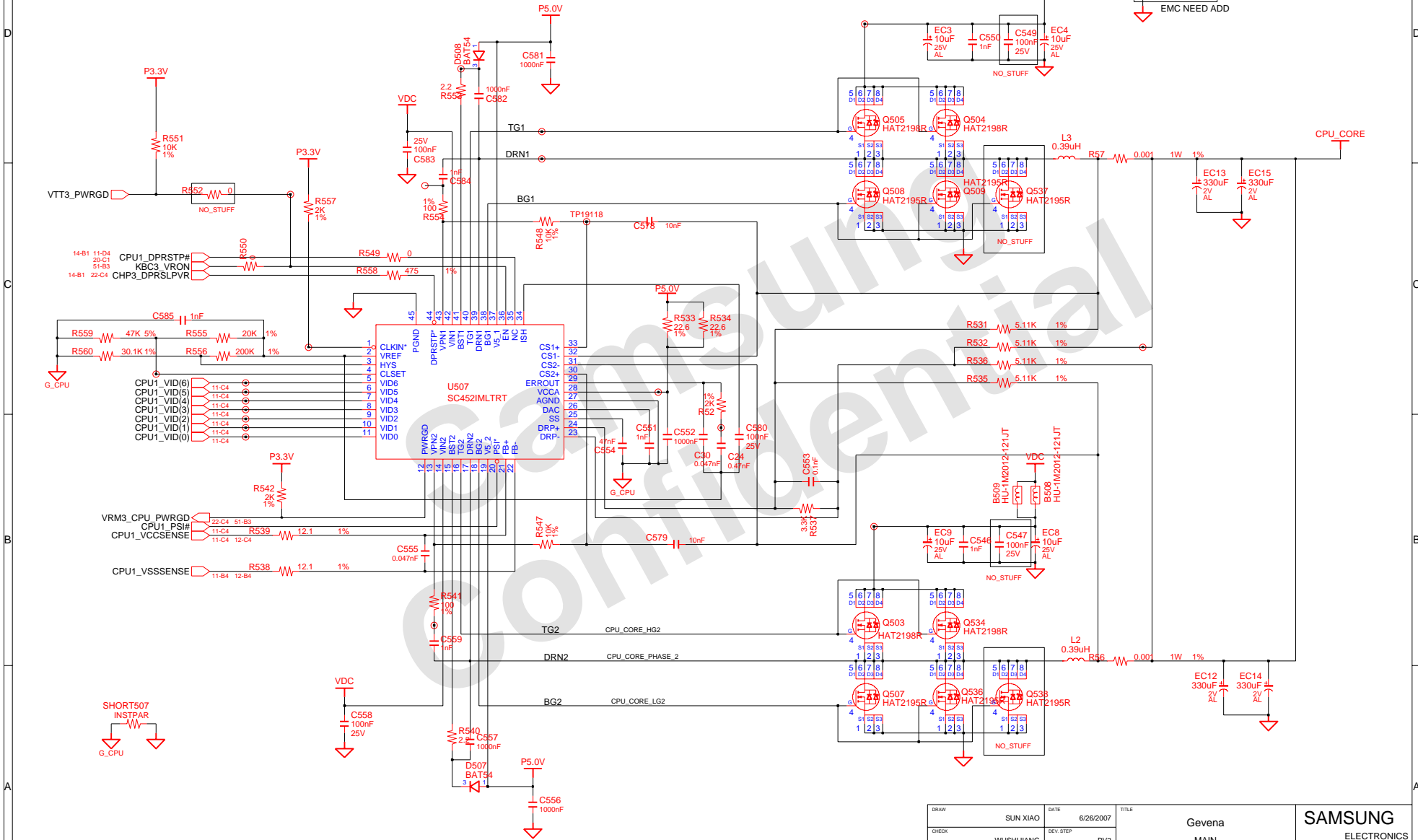
# P3.3V\_ALW/AUX & P5V\_AUX



DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena MAIN	SAMSUNG ELECTRONICS
CHECK	WUSHUIJANG	DEV STEP	PV2			PART NO. BA41-XXXXX
APPROVAL	KEVIN LEE	REV	1.0		P3.3V_ALW/AUX & P5.0V_ALW	
MODULE CODE		LAST ENT				
				October 23, 2007 10:38:02 AM	PAGE	50 OF 58

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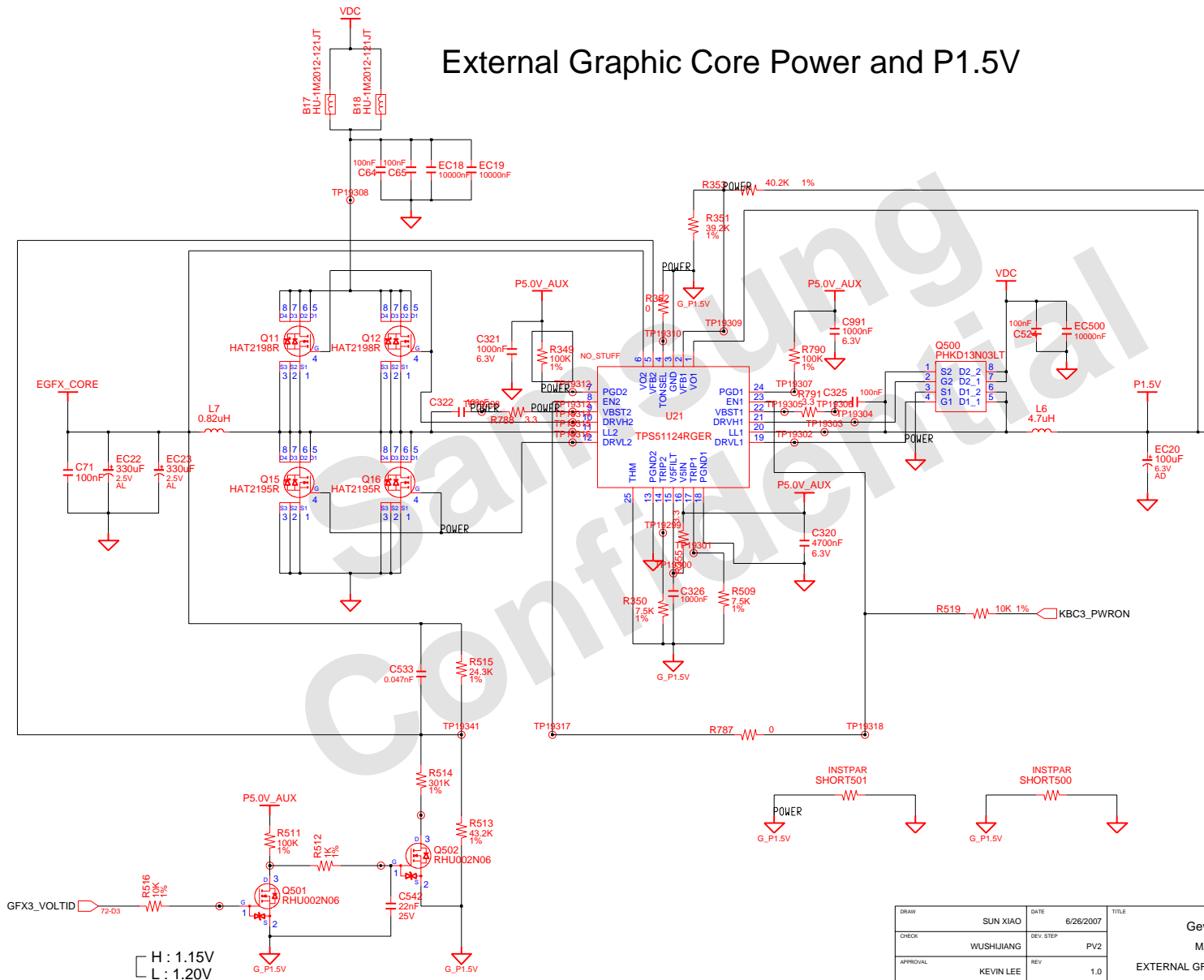
# CPU VRM [SEMTECH]



DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena MAIN CPU VRM	SAMSUNG ELECTRONICS
CHECK	WUSHUJIANG	DEV STEP	PV2			
APPROVAL	KEVIN LEE	REV	1.0			PART NO. BA41-XXXXX
MODULE CODE		LAST EDIT				
October 23, 2007 10:38:02 AM						PAGE 51 OF 58

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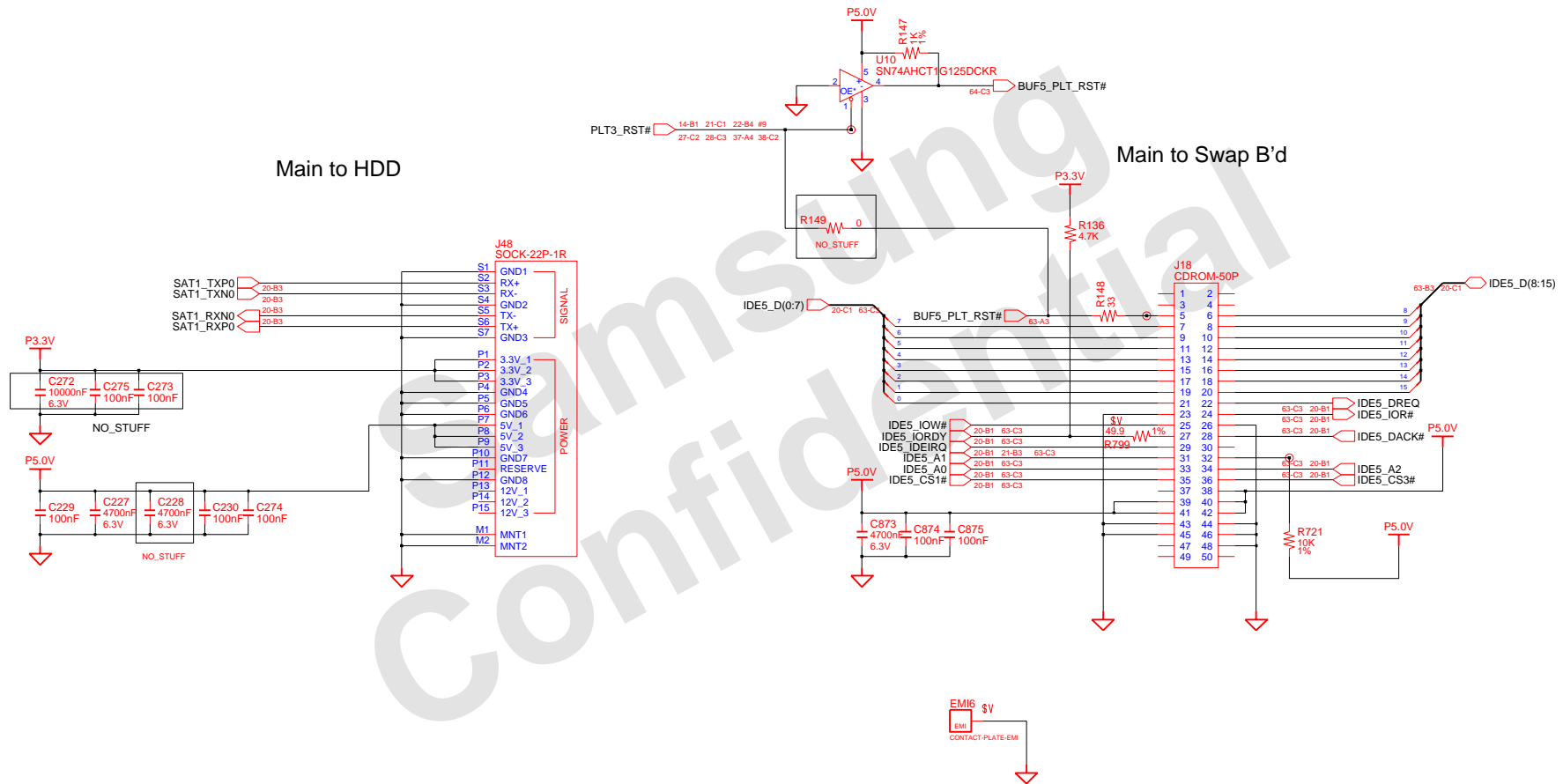
## External Graphic Core Power and P1.5V



H : 1.15V  
 L : 1.20V

DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena MAIN	SAMSUNG ELECTRONICS
CHECK	WUSHUIJIANG	DEV. STEP	PV2	EXTERNAL GFX POWER VRM		
APPROVAL	KEVIN LEE	REV	1.0			PART NO. BA41-XXXXX
MODULE CODE		LAST EDIT		October 23, 2007 10:38:02 AM	PAGE	52 OF 58

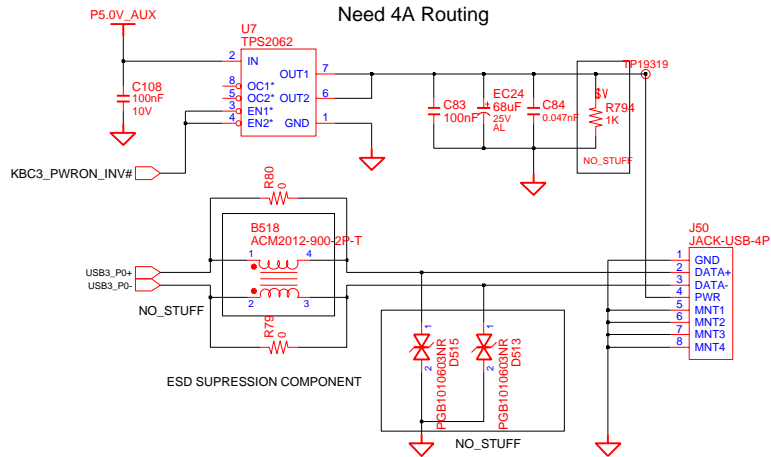
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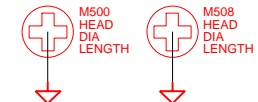
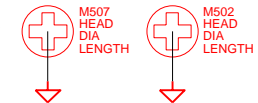
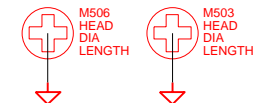
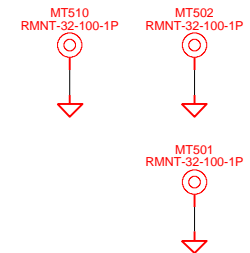
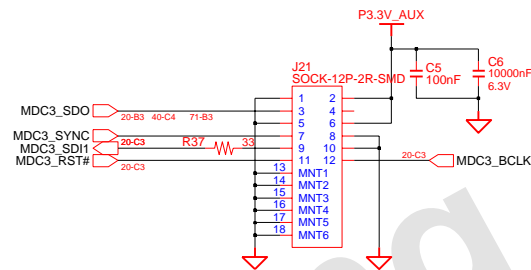
DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena CONNECTOR	SAMSUNG ELECTRONICS
CHECK	WUSHUJIANG	DEV STEP	PV2	HDD & ODD CONNECTOR		
APPROVAL	KEVIN LEE	REV	1.0			PART NO. BA41-XXXXX
MODULE CODE		LAST ENT		October 23, 2007 10:38:02 AM	PAGE	53 OF 58

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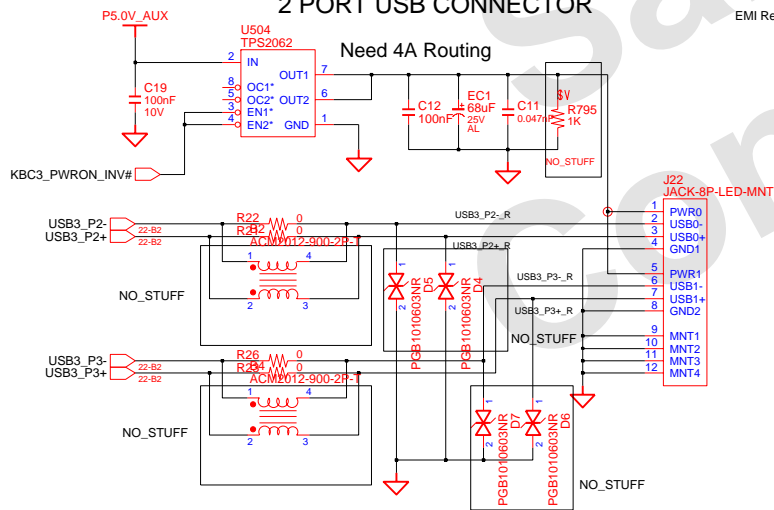
### 1 PORT USB CONNECTOR



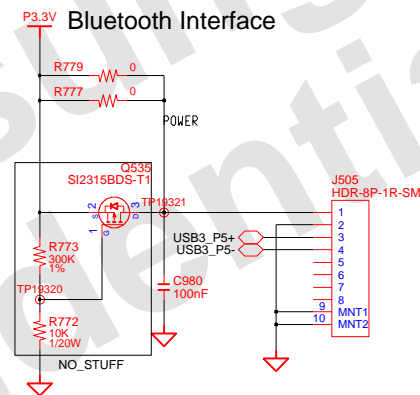
### MDC Connector



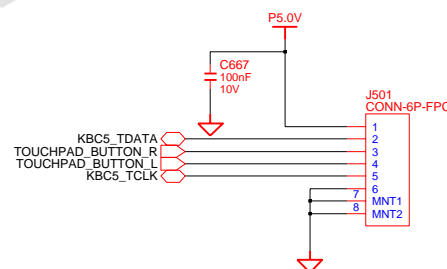
### 2 PORT USB CONNECTOR



### Bluetooth Interface

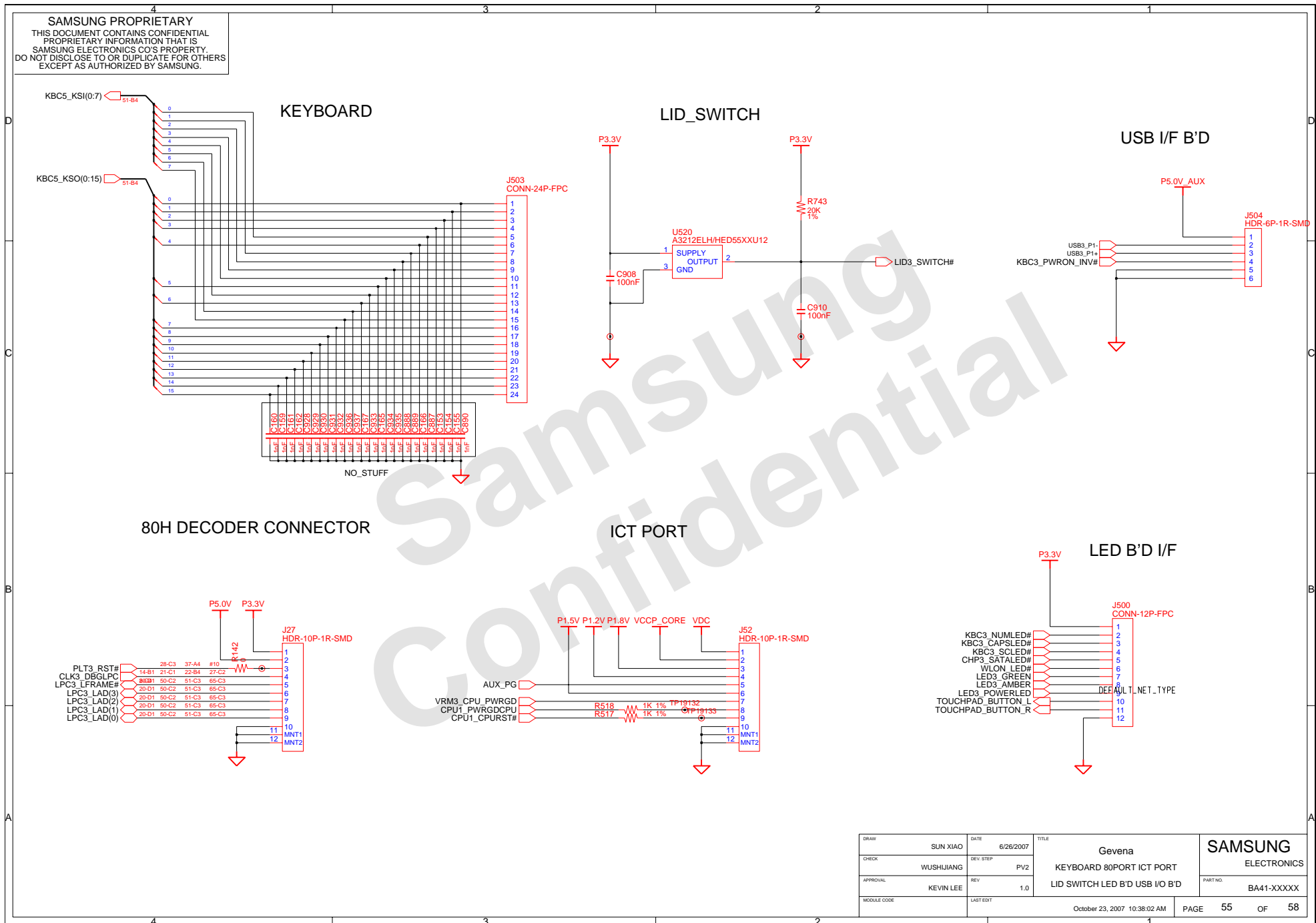


### TOUCHPAD CONNECTOR



DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena	SAMSUNG ELECTRONICS
CHECK	WUSHUJIANG	DEV. STEP	PV2	USB MDC &		
APPROVAL	KEVIN LEE	REV	1.0	TOUCHPAD BLUETOOTH I/F		PART NO. BA41-XXXXX
MODULE CODE		LAST EDIT		October 23, 2007 10:38:02 AM	PAGE	54 OF 58

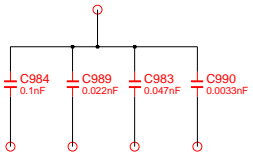
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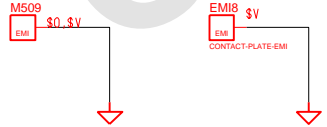
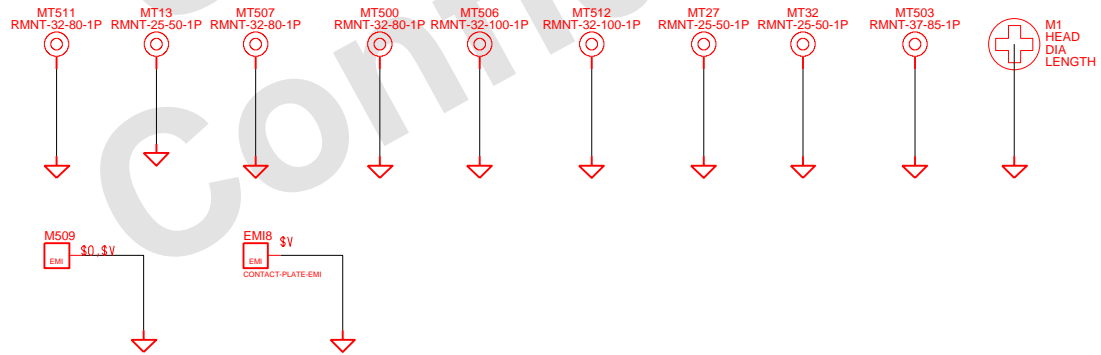
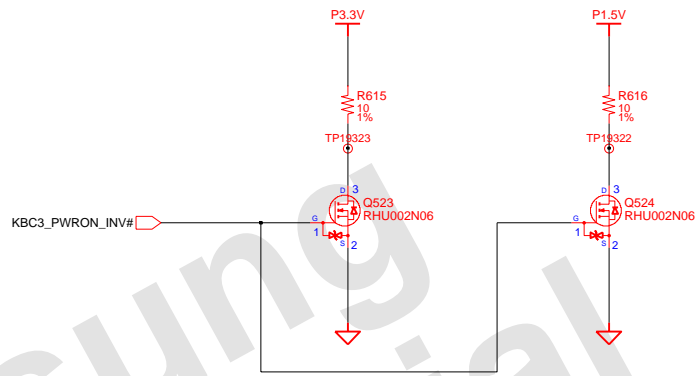
DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena	SAMSUNG ELECTRONICS
CHECK	WUSHUJIANG	DEV_STEP	PV2	KEYBOARD 80PORT ICT PORT		
APPROVAL	KEVIN LEE	REV	1.0	LID SWITCH LED B'D I/O B'D		PART NO. BA41-XXXXX
MODULE CODE		LAST EDIT		October 23, 2007 10:38:02 AM	PAGE	55 OF 58

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TOP SIDE



BOTTOM SIDE



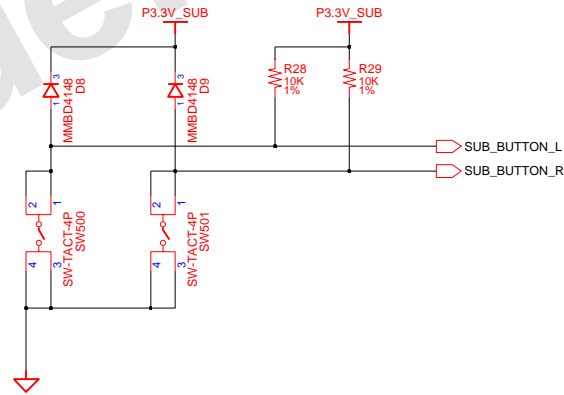
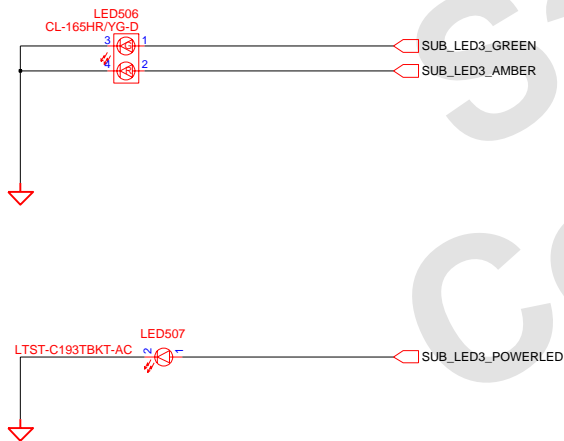
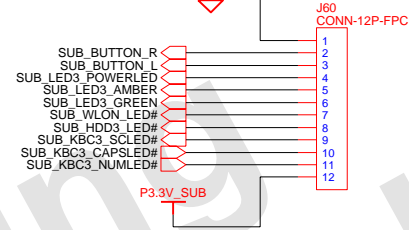
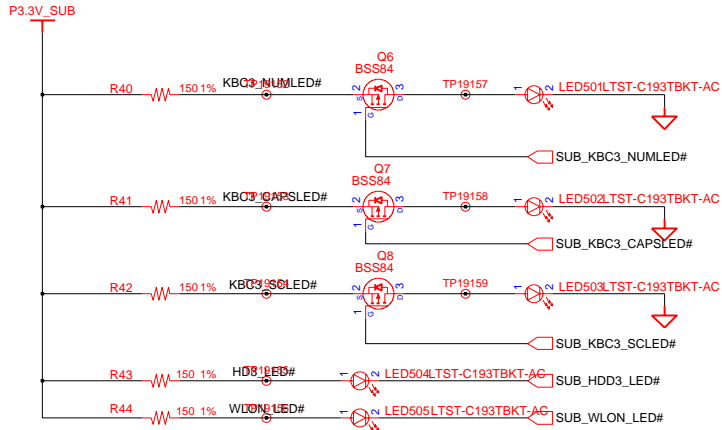
DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Geneva OTHERS	<b>SAMSUNG</b> ELECTRONICS
CHECK	WUSHIJIANG	DEV. STEP	PV2			
APPROVAL	KEVIN LEE	REV	1.0			PART NO. BA41-XXXXX
MODULE CODE		LAST EDIT	October 23, 2007 10:38:02 AM	PAGE	56	OF 58



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**TOUCHPAD AND LED B'D**



DRAW	SUN XIAO	DATE	6/26/2007
CHECK	WUSHIJIANG	DEV. STEP	PV2
APPROVAL	KEVIN LEE	REV	1.0
MODULE CODE		LAST EDIT	

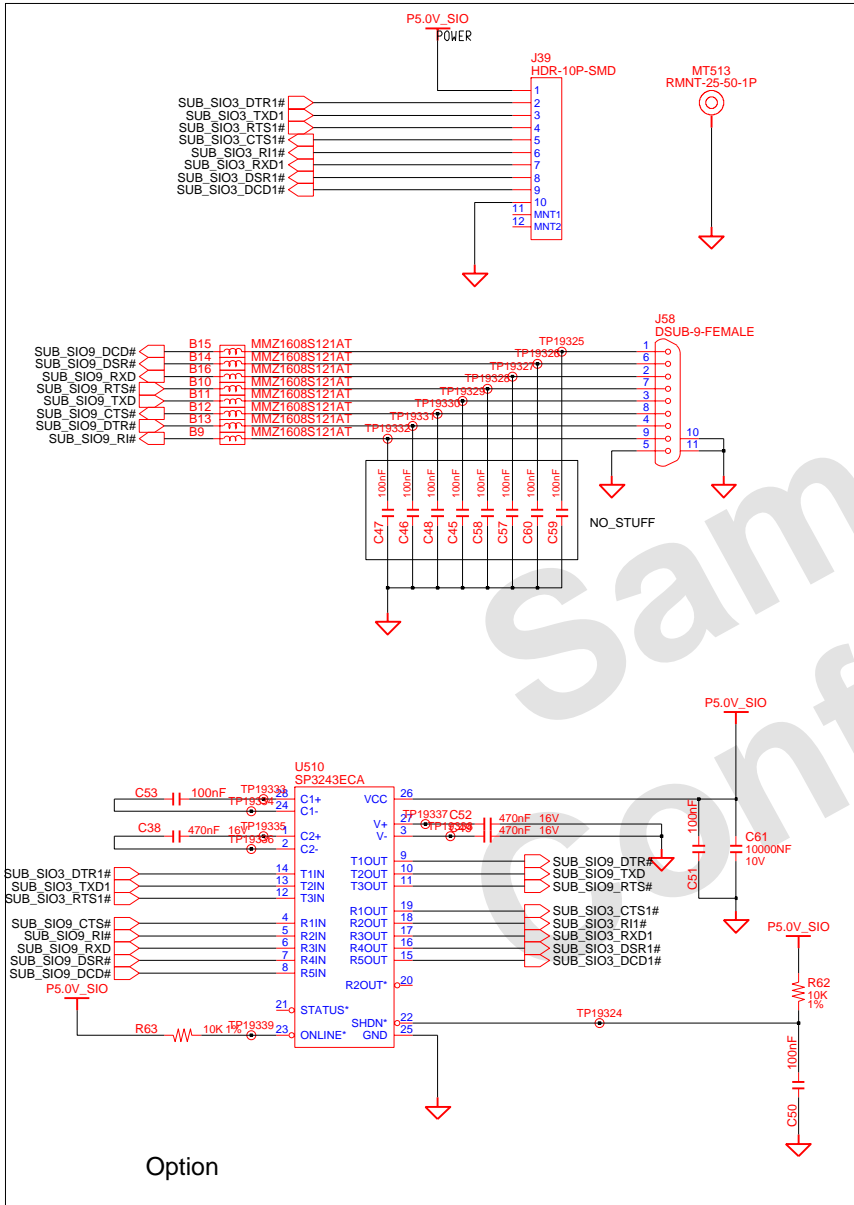
TITLE	Geneva TOUCHPAD AND LED B'D
DATE	October 23, 2007 10:38:02 AM

<b>SAMSUNG</b> ELECTRONICS
PART NO. BA41-

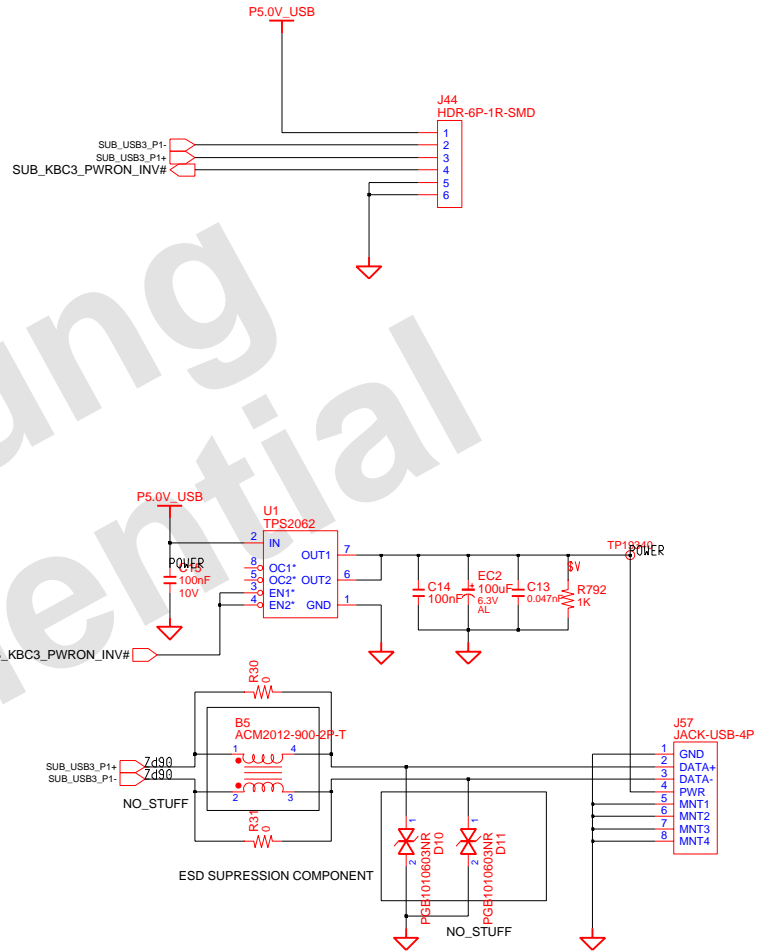
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**SIO AND USB SUB B'D**



Option



DRAW	SUN XIAO	DATE	6/30/2007	TITLE	Geneva MIO BOARD	<b>SAMSUNG</b> ELECTRONICS
CHECK	WUSHIJIANG	DEV. STEP	PV2			
APPROVAL	KEVIN LEE	REV	1.0		USB AND SIO SUB B'D	PART NO. BA41-undef ined
MODULE CODE		LAST EDIT	October 23, 2007 10:38:02 AM	PAGE	58	OF 60

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TP18380OADI3\_SEL  
 TP18381OAU03\_BCLK  
 TP18382OAU03\_BEEP  
 TP18383OAU03\_BEEP\_CU  
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 TP18394OAU05\_HP\_0\_L  
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 TP18348OAU05\_MIC1\_VREF\_R  
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 TP18369OCHP3\_BIOS\_CR1#  
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 TP18336OCHP3\_R1CRST#  
 TP18337OCHP3\_SATACLKREQ#  
 TP18338OCHP3\_SATALED#  
 TP18339OCHP3\_SERIRQ  
 TP18340OCHP3\_SLP3#  
 TP18341OCHP3\_SLP3#4  
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 TP18345OCHP3\_USBRRTAS\_R  
 TP18346OCHP3\_USBR0C9#\_R  
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 TP18320OCLK3\_TCH14  
 TP18321OCLK3\_PCLKICH  
 TP18322OCLK3\_PCLKMICOM  
 TP18323OCLK3\_PCLKSIO  
 TP18324OCLK3\_PCLKSIO\_DS  
 TP18325OCLK3\_PWR0D  
 TP18326OCLK3\_S1014  
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 TP18316OCPU1\_ADS#  
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 TP18311OCPU1\_COMP1\_R  
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 TP18282OCPU1\_TEST5\_R  
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 TP18284OCPU1\_THRMTRIP#\_R  
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 TP18286OCPU1\_TRDY#  
 TP18287OCPU1\_TRST#  
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 TP17819OEXP3\_FDBACK#  
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 TP17821OAFX3\_BLON  
 TP17822OAFX3\_BRIT

TP17799OAFX3\_HSYNC  
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 TP17805OAFX3\_VSYNC

TP17808OIDE5\_CS1#  
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CHECK	WUSHIJIANG,	DEV. STEP	PV2			
APPROVAL	KEVIN.LEE,	REV	1.0			
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TP18605OMCH1\_HRCOMP\_R  
 TP18606OMCH1\_HSCOMP#\_R  
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 TP18608OMCH1\_HVREF#  
 TP18609OMCH1\_HKSWING  
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 TP18611OMCH1\_VTILF2\_C  
 TP18612OMCH1\_VTILF3\_C  
 TP18585OMCH3\_BMBUSY#  
 TP18587OMCH3\_CLKREQ#  
 TP18588OMCH3\_CL\_VREF#  
 TP18589OMCH3\_EXTISO#  
 TP18590OMCH3\_EXITS1#  
 TP18591OMCH3\_ICHSYNC#  
 TP18592OMCH3\_ICHSYNC#\_R  
 TP18593OMCH3\_TEST1\_R  
 TP18594OMCH3\_TEST2\_R  
 TP18595OMDC3\_BCLK#  
 TP18596OMDC3\_RST#  
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 TP18598OMDC3\_SD11\_R  
 TP18599OMDC3\_SDO  
 TP18600OMDC3\_SYNC#  
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 TP18602OMEM1\_VREF#  
 TP18538OMEM1\_VREF#  
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 TP19070OSP13\_CLK\_R\_ICH#  
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 TP19072OSP13\_CS1#  
 TP19073OSP13\_MISO#  
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 TP19077OSP13\_R+  
 TP19078OSP13\_R+  
 TP19079OSP13\_R-  
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 TP19081OSUB\_BUTTON\_R  
 TP19082OSUB\_HDD3\_LED#  
 TP19083OSUB\_KBC3\_CAPSLD#  
 TP19084OSUB\_KBC3\_NUMLED#  
 TP19085OSUB\_KBC3\_PWRON\_INV#  
 TP19086OSUB\_KBC3\_SCLE#  
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 TP19088OSUB\_LED3\_GREEN  
 TP19089OSUB\_LED3\_POWERLED  
 TP19090OSUB\_S103\_CTS1#  
 TP19091OSUB\_S103\_DCD1#  
 TP19092OSUB\_S103\_DSR1#  
 TP19093OSUB\_S103\_DTR1#  
 TP19094OSUB\_S103\_R1#  
 TP19095OSUB\_S103\_RTS1#  
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 TP19097OSUB\_S103\_TXD1#  
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 TP19100OSUB\_S109\_DSR#  
 TP19056OSUB\_S109\_DTR#  
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 TP19060OSUB\_S109\_TXD#  
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 TP19066OTHM3\_STP#  
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 TP18248OVCCSATAPLL  
 TP18249OVCC\_DM1PLL  
 TP18250OVCC\_HPLL

TP18612OP1\_25V\_M\_VCC\_AYD  
 TP18613OP1\_5V\_CRT\_TVDA0  
 TP18614OP1\_5V\_GLAN\_COMP10\_R  
 TP18615OP1\_8V\_AUX\_RCOMP#\_R  
 TP18616OP1\_8V\_AUX\_RCOMP\_R  
 TP18617OP1\_8V\_AUX\_RCOMP\_VOL\_R  
 TP18618OP1\_8V\_AUX\_RCOMP\_VOL\_L  
 TP18619OP1\_8V\_AUX\_VCC\_SM\_CK  
 TP18620OP5\_0V\_ALW\_VREF\_SUS  
 TP18621OP5\_0V\_AUX\_BST1  
 TP18622OP5\_0V\_AUX\_HG  
 TP18623OP5\_0V\_AUX\_LG  
 TP18624OP5\_0V\_AUX\_PHASE  
 TP18625OP5\_0V\_VREF#  
 TP18626OP13\_CLKRUN#  
 TP18627OP13\_DEVSEL#  
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 TP18021OSC452\_HYS  
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 TP18023OSC452\_BST2  
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 TP18025OSC452\_CS2+  
 TP18026OSC452\_CS2-  
 TP18027OSC452\_DAC  
 TP18028OSC452\_DPRS1P  
 TP18029OSC452\_DPRS2P#  
 TP18030OSC452\_DRP+  
 TP18031OSC452\_DRP-  
 TP18032OSC452\_ERR0UT  
 TP18033OSC452\_FB+  
 TP18034OSC452\_FB-  
 TP18035OSC452\_ISH  
 TP18036OSC452\_SS  
 TP18037OSC452\_VPN1  
 TP18038OSC452\_VPN2  
 TP18039OSC452\_VREF#  
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 TP18208CG\_P1\_25V  
 TP18212CG\_P1\_5V  
 TP18217CG\_P3\_3V  
 TP18222CLCD\_VDD3V  
 TP18223CLCD\_VDD3V  
 TP18224CLDO\_P5\_4V  
 TP18225CLDO\_P5\_4V  
 TP18116OPRTC\_BAT  
 TP18122OTMDS\_P1\_VDD  
 TP18124OVCCP\_CORE  
 TP18125OVCCP\_CORE  
 TP18130OVCC\_CRT  
 TP18131OVCC\_CRT  
 TP18081OVDC  
 TP18084OVDC\_ADPT  
 TP18089OVDC\_INV  
 TP18095OVDD\_AMP  
 TP18098OVDD\_AUD

TP18164OP0\_9V  
 TP18170OP1\_05V\_PEG  
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 TP18192OP1\_8V\_AUX  
 TP18134OP12\_0V\_ALW  
 TP18136OP3\_3V\_AUX  
 TP18141OP3\_3V\_AUX\_EXP  
 TP18146OP3\_3V\_EXP  
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 TP18158OP3\_3V\_SUB  
 TP18161OP5\_0V\_ALW  
 TP18104OP5\_0V\_AUX  
 TP18109OP5\_0V\_S10  
 TP18112OP5\_0V\_USB

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APPROVAL	KEVIN.LEE	REV	1.0					
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