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SHANGHAI

CPU : Intel Merom
 Chip Set : CALISTOGA & ICH7-M
 Remarks : Mobility Platform

Model Name : Shanghai
 PBA Name : MAIN
 PCB Code : BA41-00774A/00732A
 Dev. Step : SR
 Revision : 1.0
 T.R. Date : 2007-03-15

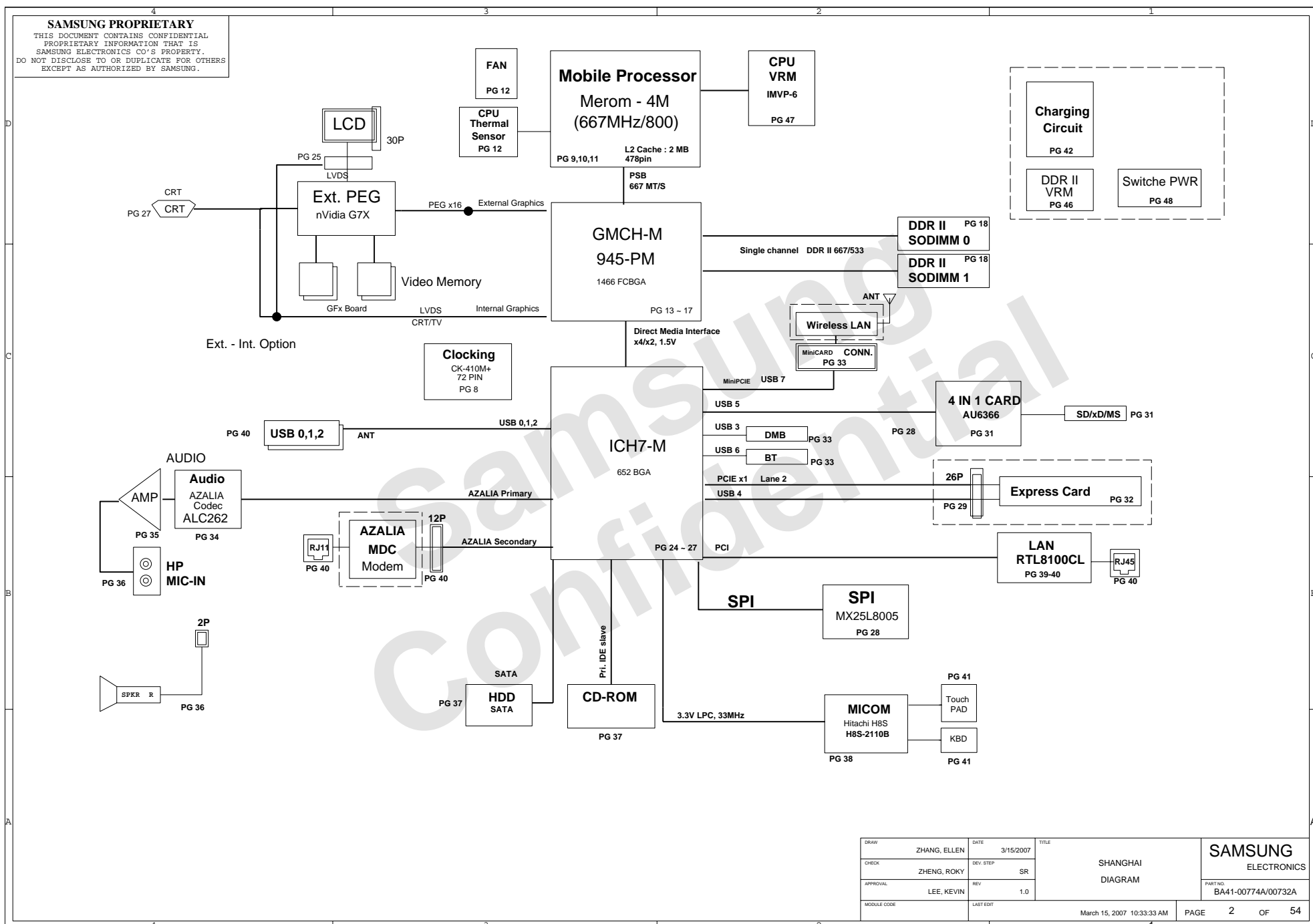
DRAW	CHECK	APPROVAL
ELLEN.ZHANG	ROKY ZHENG	KEVIN LEE

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DRAW	ZHANG, ELLEN	DATE	3/15/2007	TITLE	SHANGHAI COVER	SAMSUNG ELECTRONICS PART NO. BA41-00774A/00732A
CHECK	ZHENG, ROKY	DEV. STEP	SR			
APPROVAL	LEE, KEVIN	REV	1.0			
MODULE CODE		LAST EDIT	March 15, 2007 10:33:33 AM	PAGE	1	OF 54

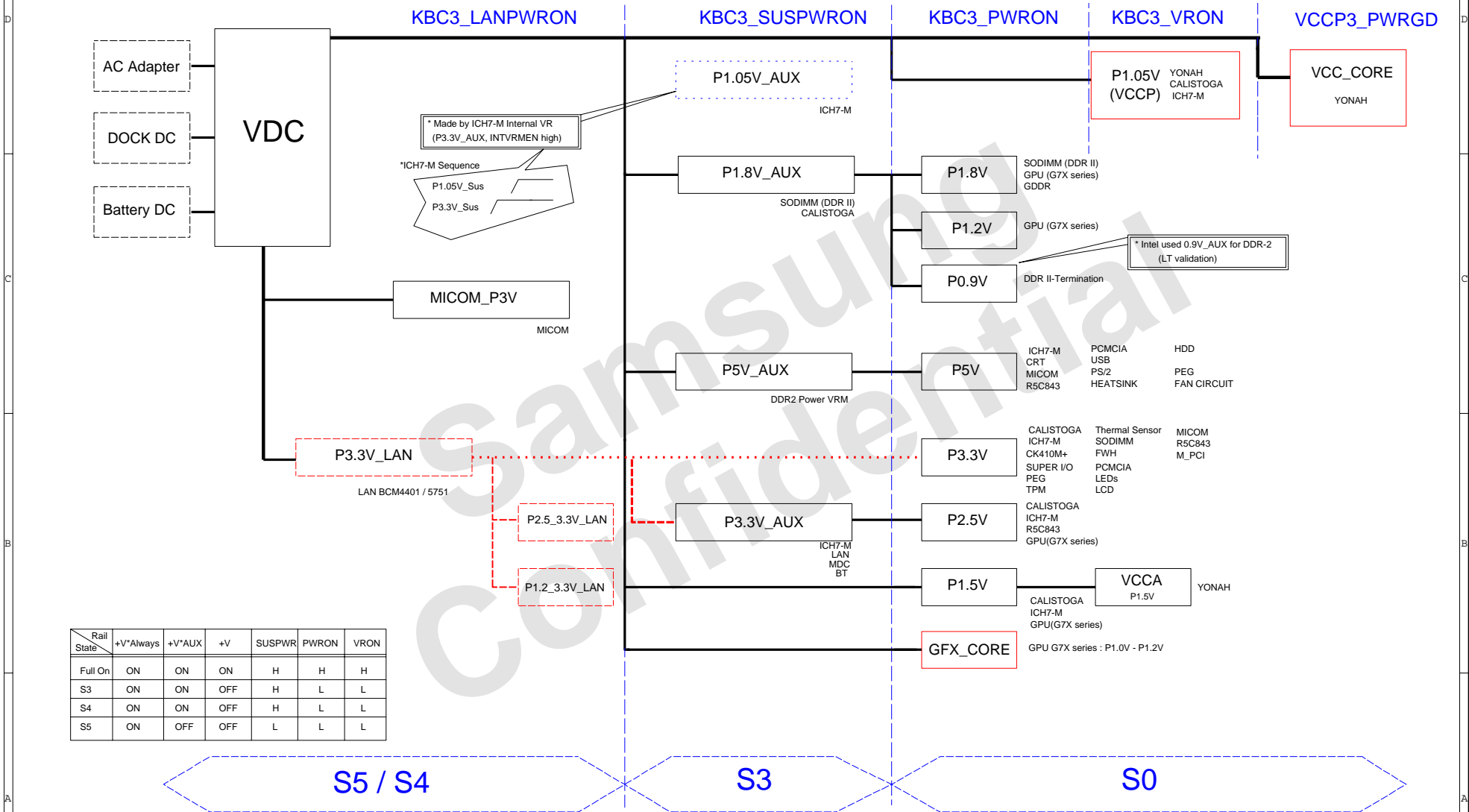
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DRAW	ZHANG, ELLEN	DATE	3/15/2007	TITLE	SHANGHAI DIAGRAM	SAMSUNG ELECTRONICS
CHECK	ZHENG, ROKY	DEV. STEP	SR			
APPROVAL	LEE, KEVIN	REV	1.0			
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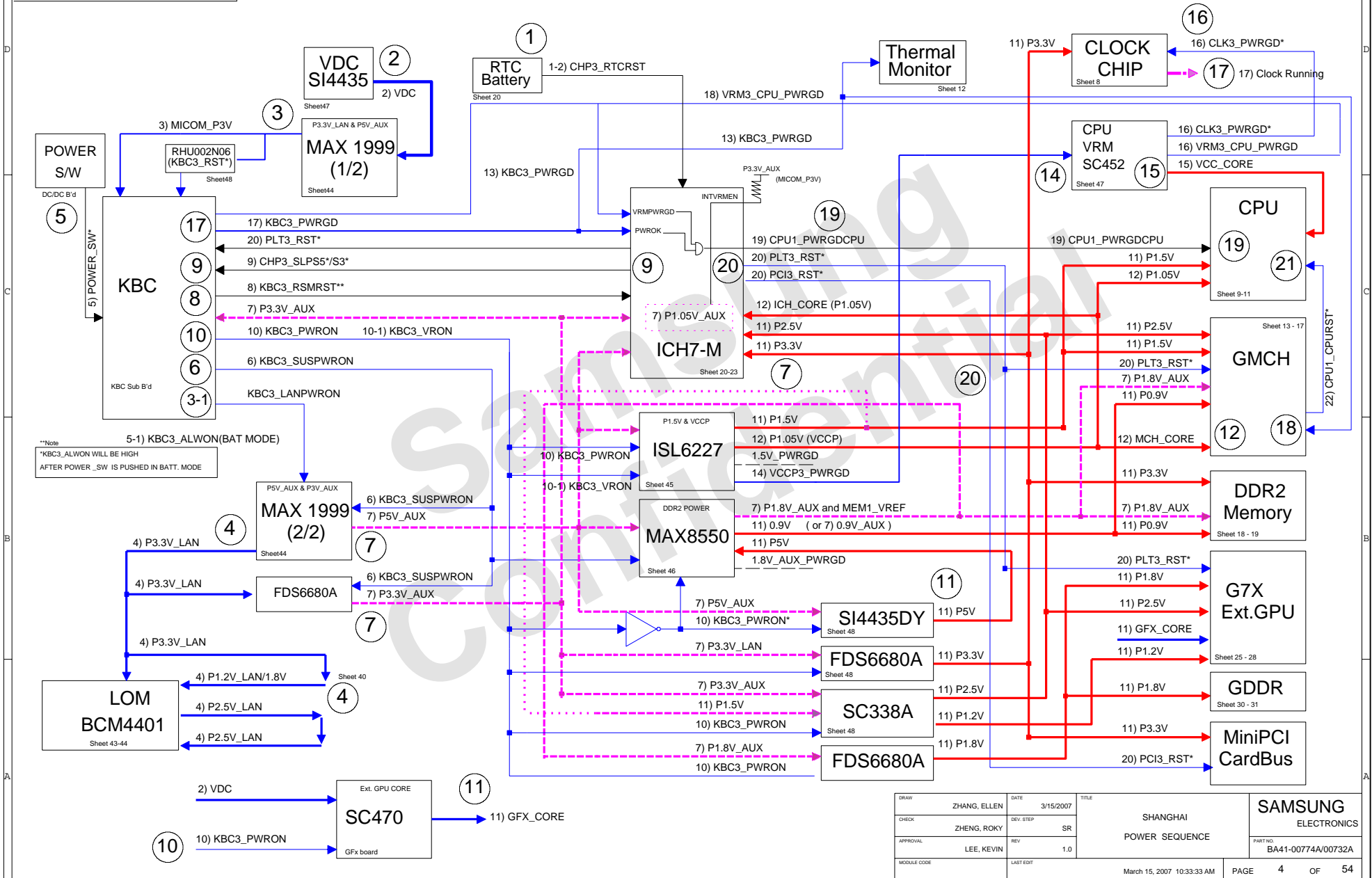
Power Diagram



DRAW	ZHANG, ELLEN	DATE	3/15/2007	TITLE	SHANGHAI POWER DIAGRAM	SAMSUNG ELECTRONICS PART NO. BA41-00774A/00732A
CHECK	ZHENG, ROKY	DEV. STEP	SR			
APPROVAL	LEE, KEVIN	REV	1.0			
MODULE CODE		LAST EDIT				
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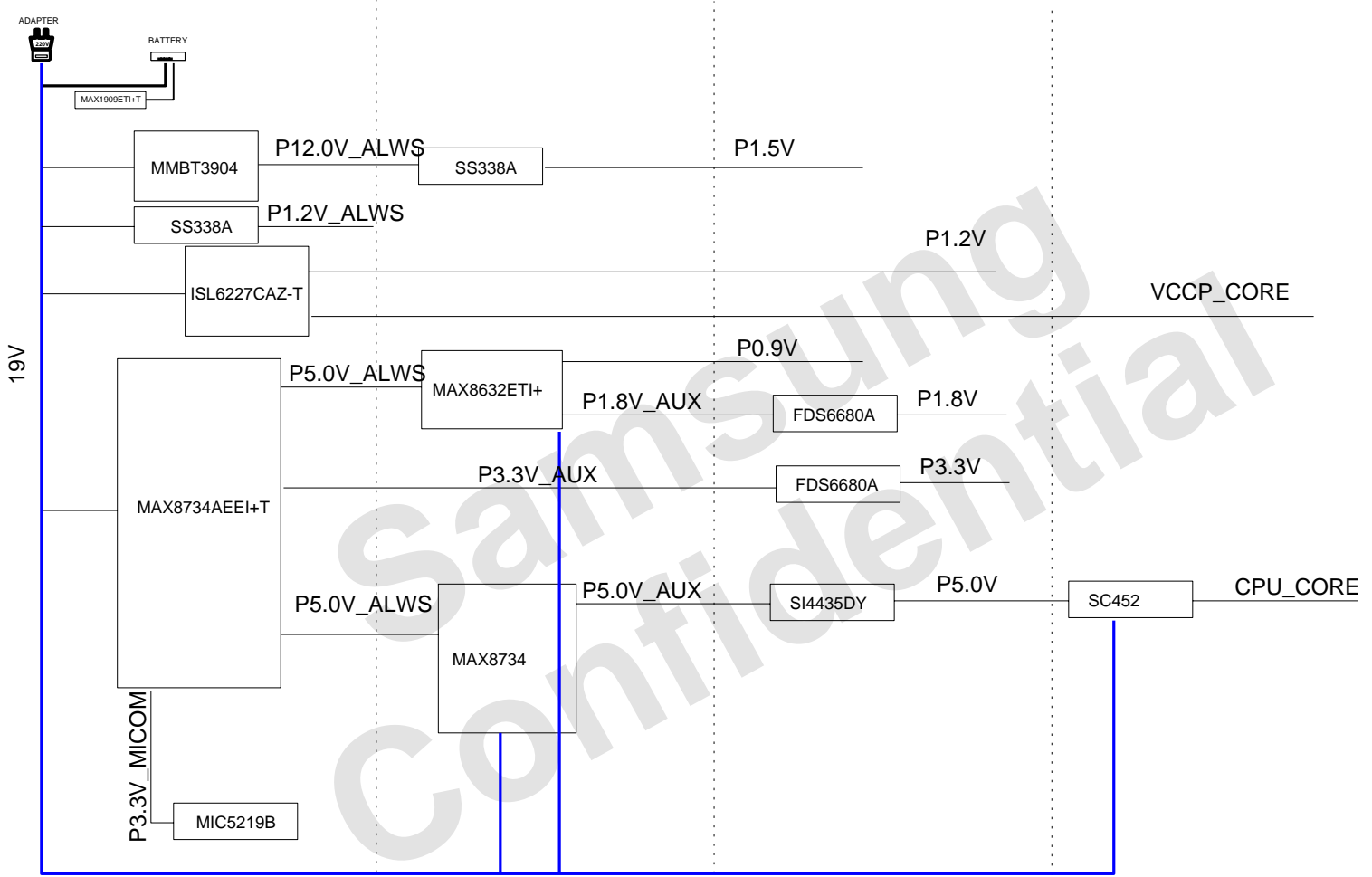
RESET DIAGRAM



DRAW	ZHANG, ELLEN	DATE	3/15/2007	TITLE	SHANGHAI POWER SEQUENCE	SAMSUNG ELECTRONICS PART NO. BA41-00774A/00732A
CHECK	ZHENG, ROKY	DEV. STEP	SR			
APPROVAL	LEE, KEVIN	REV	1.0			
MODULE CODE		LAST EDIT				
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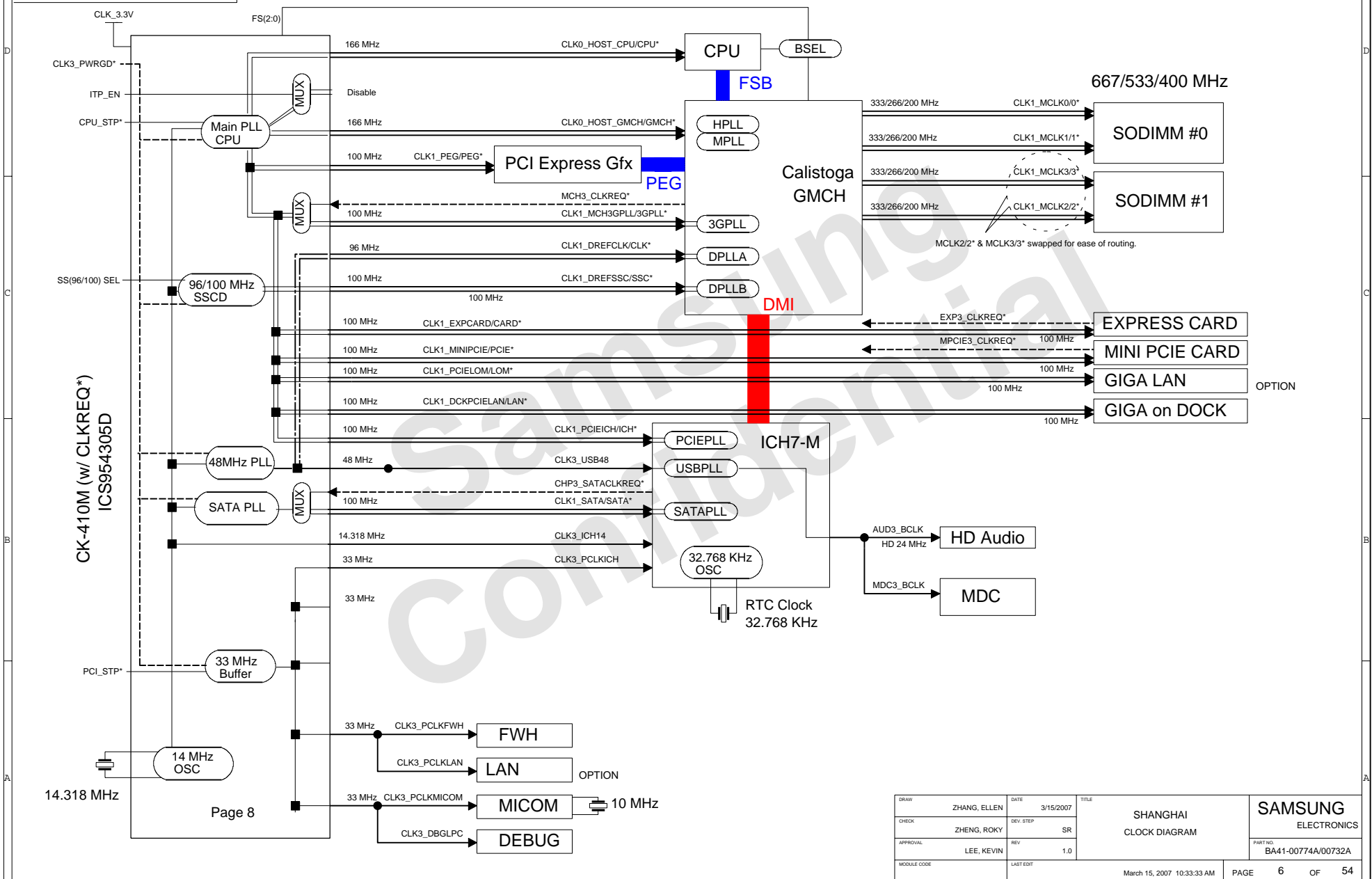
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POWER RAILS ANALYSIS



DRAW	ZHANG, ELLEN	DATE	3/15/2007	TITLE	SHANGHAI POWER BLOCK	SAMSUNG ELECTRONICS PART NO. BA41-00774A/00732A
CHECK	ZHENG, ROKY	DEV. STEP	SR			
APPROVAL	LEE, KEVIN	REV	1.0			
MODULE CODE		LAST EDIT	March 15, 2007 10:33:33 AM	PAGE 5 OF 54		

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DRAW	ZHANG, ELLEN	DATE	3/15/2007	TITLE	SHANGHAI	SAMSUNG
CHECK	ZHENG, ROKY	DEV. STEP	SR	CLOCK DIAGRAM	CLOCK DIAGRAM	ELECTRONICS
APPROVAL	LEE, KEVIN	REV	1.0			PART NO. BA41-00774A/00732A
MODULE CODE		LAST EDIT		March 15, 2007 10:33:33 AM	PAGE	6 OF 54

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SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
LAN	AD21	1	G
USB	AD30(internal)	-	-
Hub to PCI	AD31(internal)	-	-
LPC bridge/IDE/AC97/SMBUS	AD31(internal)	-	-
Internal MAC	AD31(internal)	-	-
AC Link	-	-	-

Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	SB600	Real Time Clock
Crystal	10MHz	MICOM	HS64FZ110B
Crystal	14.318MHz	CLOCK-Generator	ICS95451
Crystal	12MHz	AU6366	4 IN 1 CARD
Crystal	25MHz	LAN	LOM

Voltage Rails

CPU_CORE	CPU	CPU RS600 SB600
VCCP_CORE	CPU	RS600 SB600
P1.2V		
P1.5V	CPU EXPCARD	
P1.8V	RS600	
P0.9V	DDR2	
P5.0V	FAN THERMAL CRT SB600 AU6366 MINIPCI ALC262 HDD ODD MICOM USB TOUCH-PAD CPU_CORE	
P3.3V	SYSTEM POWER	
P2.5V_LAN	RTL8100	
P1.8V_AUX	DDR2 P1.8V RS600	
P5.0V_AUX	THERMAL LCD P1.2V P5.0V	
P3.3V_AUX	MDC MICOM MINIPCI EXP-CARD SB600 THERMAL	
P12.0V_ALWS	P1.5V P3.3V P1.8V	
P5.0V_ALWS	P3.3V DDR2-PWR	
P3.3V_MICOM	THERMAL SB600 MICOM LED P1.8V_ALWS	
P1.2V_ALWS	SB600,P1.2V	
VDC	Primary DC system power supply (7 to 21V)	

CPU Core Voltage Table IMVP-6

Active Mode		Active/Deeper Sleep Dual Mode Region		Deeper Sleep/Extended Deeper Sleep Dual Mode Region	
VID(6:0)	Voltage	VID(6:0)	Voltage	VID(6:0)	Voltage
0 0 0 0 0 0 0	1.5000 V	0 1 0 1 0 0 0	1.0000 V	1 0 1 0 0 0 1	0.4875 V
0 0 0 0 0 0 0	1.4875 V	0 1 0 1 0 0 0	0.9875 V	1 0 1 0 0 0 1	0.4750 V
0 0 0 0 0 0 1	1.4750 V	0 1 0 1 0 0 1	0.9750 V	1 0 1 0 0 0 1	0.4625 V
0 0 0 0 0 1 0	1.4625 V	0 1 0 1 0 1 0	0.9625 V	1 0 1 0 1 0 0	0.4500 V
0 0 0 0 0 1 1	1.4500 V	0 1 0 1 1 0 0	0.9500 V	1 0 1 0 1 0 0	0.4375 V
0 0 0 0 1 0 0	1.4375 V	0 1 0 1 1 0 1	0.9375 V	1 0 1 0 1 0 1	0.4250 V
0 0 0 0 1 0 1	1.4250 V	0 1 0 1 1 1 0	0.9250 V	1 0 1 0 1 1 0	0.4125 V
0 0 0 0 1 1 0	1.4125 V	0 1 0 1 1 1 1	0.9125 V	1 0 1 1 0 0 0	0.4000 V
0 0 0 1 0 0 0	1.4000 V	0 1 1 0 0 0 0	0.9000 V	1 0 1 1 0 0 0	0.3875 V
0 0 0 1 0 0 1	1.3875 V	0 1 1 0 0 0 1	0.8875 V	1 0 1 1 0 0 1	0.3750 V
0 0 0 1 0 1 0	1.3750 V	0 1 1 0 0 1 0	0.8750 V	1 0 1 1 0 1 0	0.3625 V
0 0 0 1 0 1 1	1.3625 V	0 1 1 0 0 1 1	0.8625 V	1 0 1 1 1 0 0	0.3500 V
0 0 0 1 1 0 0	1.3500 V	0 1 1 0 1 0 0	0.8500 V	1 0 1 1 1 0 1	0.3375 V
0 0 0 1 1 0 1	1.3375 V	0 1 1 0 1 0 1	0.8375 V	1 0 1 1 1 1 0	0.3250 V
0 0 0 1 1 1 0	1.3250 V	0 1 1 0 1 1 0	0.8250 V	1 0 1 1 1 1 1	0.3125 V
0 0 0 1 1 1 1	1.3125 V	0 1 1 1 0 1 0	0.8125 V	1 1 0 0 0 0 0	0.3000 V
0 0 1 0 0 0 0	1.3000 V	0 1 1 1 0 0 0	0.8000 V	1 1 0 0 0 0 0	0.2875 V
0 0 1 0 0 0 1	1.2875 V	0 1 1 1 0 0 1	0.7875 V	1 1 0 0 0 0 1	0.2750 V
0 0 1 0 0 1 0	1.2750 V	0 1 1 1 0 1 0	0.7750 V	1 1 0 0 0 1 0	0.2625 V
0 0 1 0 0 1 1	1.2625 V	0 1 1 1 0 1 1	0.7625 V	1 1 0 0 1 0 0	0.2500 V
0 0 1 0 1 0 0	1.2500 V	0 1 1 1 1 0 0	0.7500 V	1 1 0 0 1 0 1	0.2375 V
0 0 1 0 1 0 1	1.2375 V	0 1 1 1 1 0 1	0.7375 V	1 1 0 0 1 1 0	0.2250 V
0 0 1 0 1 1 0	1.2250 V	0 1 1 1 1 1 0	0.7250 V	1 1 0 0 1 1 1	0.2125 V
0 0 1 1 0 0 0	1.2125 V	0 1 1 1 1 1 1	0.7125 V	1 1 0 1 0 0 0	0.2000 V
0 0 1 1 0 0 1	1.2000 V	1 0 0 0 0 0 0	0.7000 V	1 1 0 1 0 0 1	0.1875 V
0 0 1 1 0 0 1	1.1875 V	1 0 0 0 0 0 1	0.6875 V	1 1 0 1 0 1 0	0.1750 V
0 0 1 1 0 1 0	1.1750 V	1 0 0 0 0 1 0	0.6750 V	1 1 0 1 0 1 1	0.1625 V
0 0 1 1 0 1 1	1.1625 V	1 0 0 0 0 1 1	0.6625 V	1 1 0 1 1 0 0	0.1500 V
0 0 1 1 1 0 0	1.1500 V	1 0 0 0 1 0 0	0.6500 V	1 1 0 1 1 0 1	0.1375 V
0 0 1 1 1 0 1	1.1375 V	1 0 0 0 1 0 1	0.6375 V	1 1 0 1 1 1 0	0.1250 V
0 0 1 1 1 1 0	1.1250 V	1 0 0 0 1 1 0	0.6250 V	1 1 0 1 1 1 1	0.1125 V
0 0 1 1 1 1 1	1.1125 V	1 0 0 0 1 1 1	0.6125 V	1 1 1 0 0 0 0	0.1000 V
0 1 0 0 0 0 0	1.1000 V	1 0 0 0 1 1 0	0.6000 V	1 1 1 0 0 0 1	0.0875 V
0 1 0 0 0 0 1	1.0875 V	1 0 0 0 1 0 0	0.5875 V	1 1 1 0 0 1 0	0.0750 V
0 1 0 0 0 1 0	1.0750 V	1 0 0 0 1 0 1	0.5750 V	1 1 1 0 0 1 1	0.0625 V
0 1 0 0 0 1 1	1.0625 V	1 0 0 0 1 0 1	0.5625 V	1 1 1 0 1 0 0	0.0500 V
0 1 0 0 1 0 0	1.0500 V	1 0 0 0 1 1 0	0.5500 V	1 1 1 0 1 0 1	0.0375 V
0 1 0 0 1 0 1	1.0375 V	1 0 0 0 1 1 0	0.5375 V	1 1 1 0 1 1 0	0.0250 V
0 1 0 0 1 1 0	1.0250 V	1 0 0 0 1 1 1	0.5250 V	1 1 1 0 1 1 1	0.0125 V
0 1 0 0 1 1 1	1.0125 V	1 0 0 0 1 1 1	0.5125 V	1 1 1 1 0 0 0	0.0000 V
		1 0 0 1 0 0 0	0.5000 V	1 1 1 1 0 0 1	0.0000 V
				1 1 1 1 0 1 0	0.0000 V
				1 1 1 1 0 1 1	0.0000 V
				1 1 1 1 1 0 0	0.0000 V
				1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0	0.0000 V
				1 1 1 1 1 1 1	0.0000 V

I C / SMB Address

Devices	Address	Hex	Bus
SB600	Master	-	SMBUS Master
EMCN300(CPU Thermal Sensor)	1001 110X	9Ch	Thermal Sensor
SODIMM0	1010 0000	A0h	-
SODIMM1	1010 001X	A2h	-
ICS95411 (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable

USB PORT Assign

PORT NUMBER	ASSIGNED TO
0	SYSTEM PORT A
1,2	SYSTEM PORT B
3	DMB
4	EXPRESS CARD
5	4 IN 1 CARD
6	BT
7	MINICARD

System Power States

CHP3_SLPS1* S1, Powered-On-Suspend(POS) : In this state, all clocks(except the 32.768KHz clock) are stopped. The system context is maintained in system DRAM. Power is maintained to PCI, the CPU, memory controller, memory, and all other critical subsystems. Note that this state does not preclude power being removed from non-essential devices, such as disk drives. During this state, CPU can be selected for either Deep Sleep or Deeper Sleep.

In Deeper Sleep, CPU voltage reduced in this state to reduce the leakage power.

CHP3_SLPS3* S3, Suspend-To-RAM(STR) : The system context is maintained in system DRAM, but power is shut off to non-critical circuits. Memory is retained, and refreshes continue. All clocks stop except RTC clock.

CHP3_SLPS4* S4, Suspend-To-Disk(STD) : The Context of the system is maintained on the disk. All power is then shut off to the system except for the logic required to resume. Externally appears same as S5, but may have different wake events.

CHP3_SLPS5* S5, Soft Off(SOFF) : System context is not maintained. All power is shut off except for the logic required to restart. A full boot is required when waking.

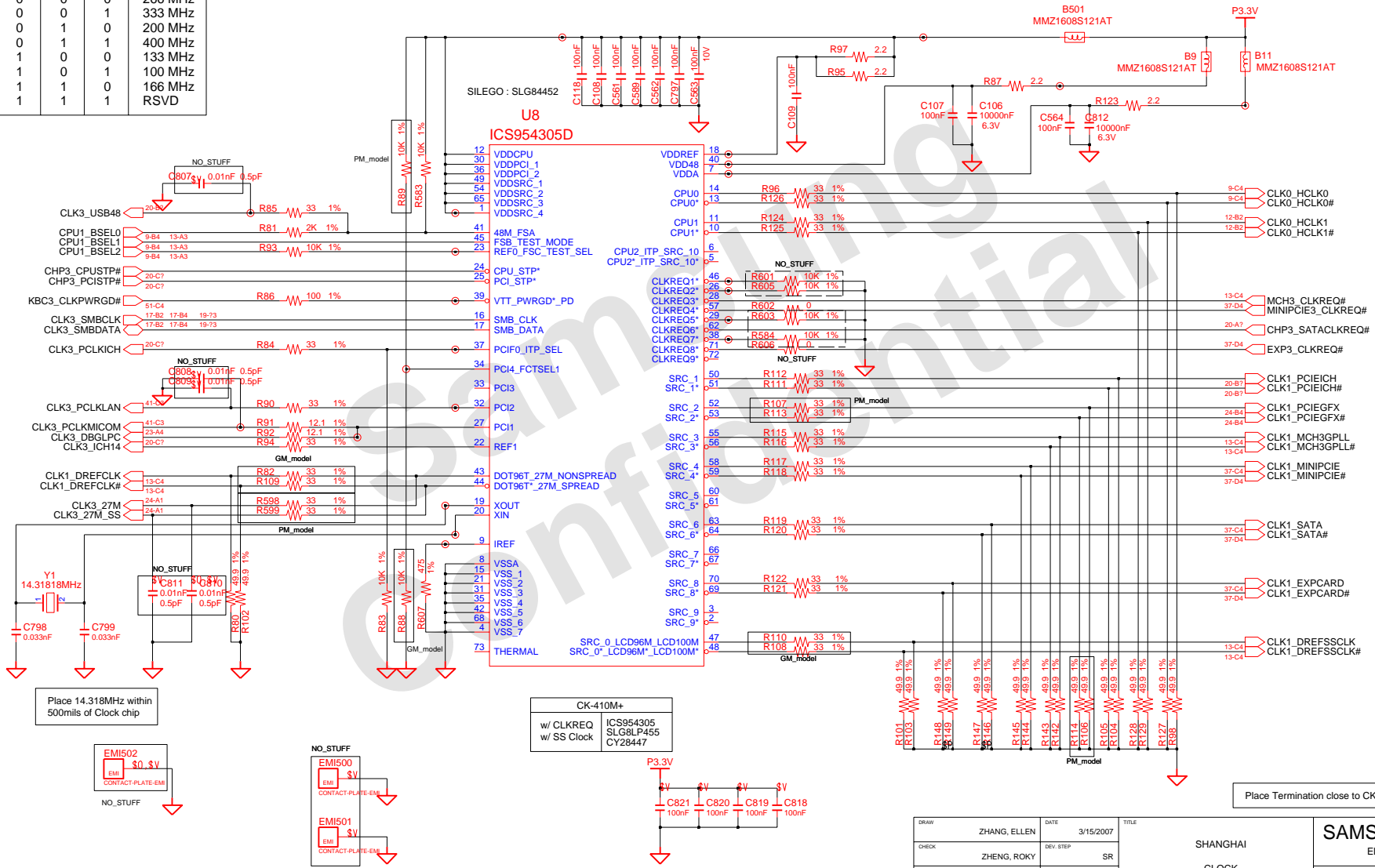
*Yonah Processor (2.33 GHz / 800 MHz : TBD)

DRAW	ZHANG, ELLEN	DATE	3/15/2007	TITLE	SAMSUNG ELECTRONICS
CHECK	ZHENG, ROKY	DEV. STEP	SR	SHANGHAI	
APPROVAL	LEE, KEVIN	REV	1.0	ANNOTATIONS	
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CPU	FSA	FSB	FSC	HOST CLK
	BSEL0	BSEL1	BSEL2	
	0	0	0	266 MHz
	0	0	1	333 MHz
	0	1	0	200 MHz
	0	1	1	400 MHz
	1	0	0	133 MHz
	1	0	1	100 MHz
	1	1	0	166 MHz
	1	1	1	RSVD



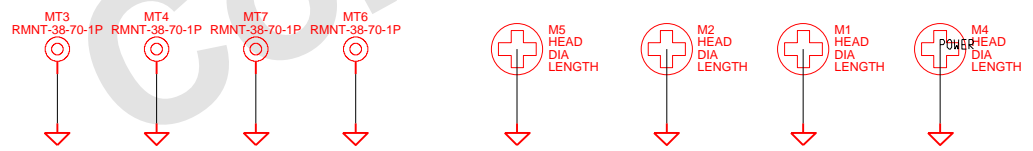
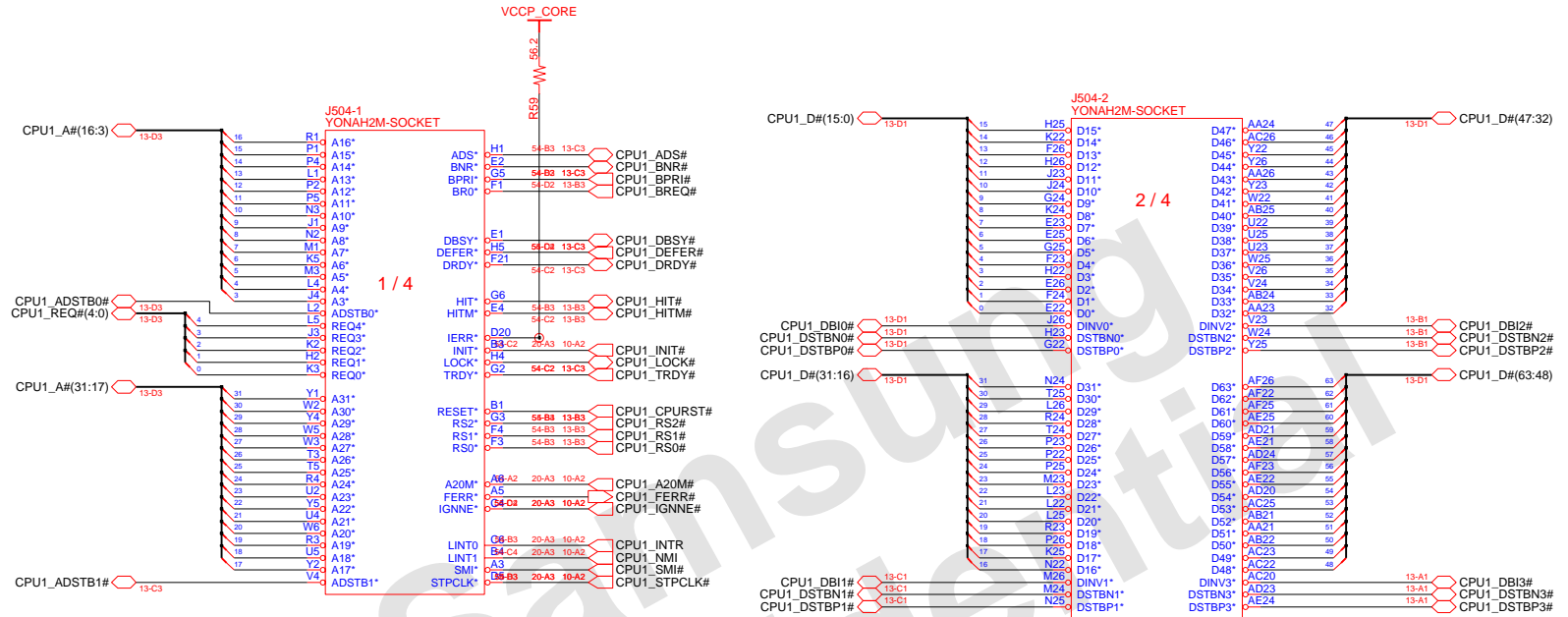
Place 14.318MHz within 500mils of Clock chip

CK-410M+
w/ CLKREQ
w/ SS Clock

Place Termination close to CK-410M

DRAW	ZHANG, ELLEN	DATE	3/15/2007	TITLE	SHANGHAI CLOCK	SAMSUNG ELECTRONICS
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MODULE CODE		LAST EDIT				
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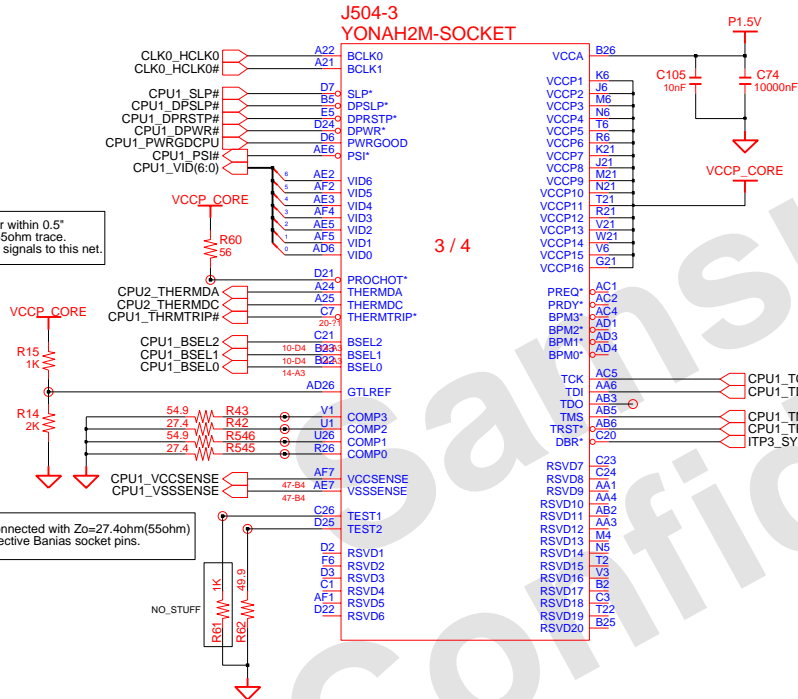
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DRAW	ZHANG, ELLEN	DATE	3/15/2007	TITLE	SHANGHAI MEROM(1/3)	SAMSUNG ELECTRONICS
CHECK	ZHENG, ROKY	DEV. STEP	SR			
APPROVAL	LEE, KEVIN	REV	1.0			
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GTLREF : Keep the Voltage divider within 0.5" of the first GTLREF0 pin with Zo=55ohm trace. Minimize coupling of any switching signals to this net.

COMP0.2(COMP1,3) should be connected with Zo=27.4ohm(55ohm) trace shorter than 1/2" to their respective Banias socket pins.

CPU Core Voltage Table IMVP-6

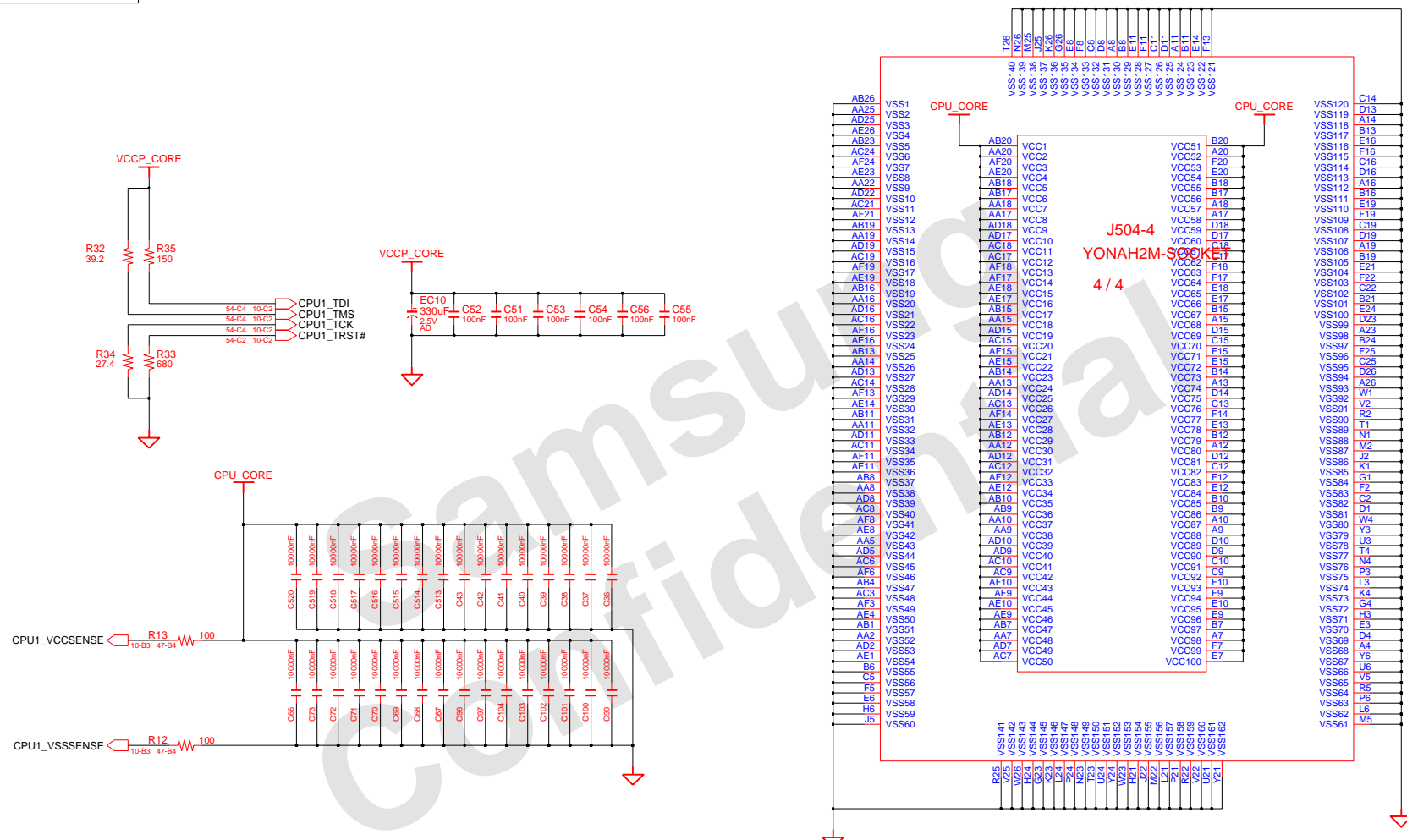
Active Mode		Active/Deeper Sleep Dual Mode Region		Deeper Sleep/Extended Deeper Sleep Dual Mode Region	
VID(6:0)	Voltage	VID(6:0)	Voltage	VID(6:0)	Voltage
0 0 0 0 0 0 0	1.5000 V	0 1 0 1 0 0 0	1.0000 V	1 0 1 0 0 0 1	0.4875 V
0 0 0 0 0 0 1	1.4875 V	0 1 0 1 0 0 1	0.9875 V	1 0 1 0 0 1 0	0.4750 V
0 0 0 0 0 1 0	1.4750 V	0 1 0 1 0 1 0	0.9750 V	1 0 1 0 0 1 1	0.4625 V
0 0 0 0 0 1 1	1.4625 V	0 1 0 1 1 0 0	0.9625 V	1 0 1 0 1 0 0	0.4500 V
0 0 0 0 1 0 0	1.4500 V	0 1 0 1 1 0 1	0.9500 V	1 0 1 0 1 0 1	0.4375 V
0 0 0 0 1 0 1	1.4375 V	0 1 0 1 1 1 0	0.9375 V	1 0 1 0 1 1 0	0.4250 V
0 0 0 0 1 1 0	1.4250 V	0 1 0 1 1 1 1	0.9250 V	1 0 1 0 1 1 1	0.4125 V
0 0 0 0 1 1 1	1.4125 V	0 1 1 0 0 0 0	0.9125 V	1 0 1 1 0 0 0	0.4000 V
0 0 0 1 0 0 0	1.4000 V	0 1 1 0 0 0 1	0.9000 V	1 0 1 1 0 0 1	0.3875 V
0 0 0 1 0 0 1	1.3875 V	0 1 1 0 0 1 0	0.8875 V	1 0 1 1 0 1 0	0.3750 V
0 0 0 1 0 1 0	1.3750 V	0 1 1 0 0 1 1	0.8750 V	1 0 1 1 0 1 1	0.3625 V
0 0 0 1 0 1 1	1.3625 V	0 1 1 0 1 0 0	0.8625 V	1 0 1 1 1 0 0	0.3500 V
0 0 0 1 1 0 0	1.3500 V	0 1 1 0 1 0 1	0.8500 V	1 0 1 1 1 0 1	0.3375 V
0 0 0 1 1 0 1	1.3375 V	0 1 1 0 1 1 0	0.8375 V	1 0 1 1 1 1 0	0.3250 V
0 0 0 1 1 1 0	1.3250 V	0 1 1 0 1 1 1	0.8250 V	1 0 1 1 1 1 1	0.3125 V
0 0 0 1 1 1 1	1.3125 V	0 1 1 1 0 0 0	0.8125 V	1 1 0 0 0 0 0	0.3000 V
0 0 1 0 0 0 0	1.3000 V	0 1 1 1 0 0 1	0.8000 V	1 1 0 0 0 0 1	0.2875 V
0 0 1 0 0 0 1	1.2875 V	0 1 1 1 0 1 0	0.7875 V	1 1 0 0 0 1 0	0.2750 V
0 0 1 0 0 1 0	1.2750 V	0 1 1 1 0 1 1	0.7750 V	1 1 0 0 0 1 1	0.2625 V
0 0 1 0 0 1 1	1.2625 V	0 1 1 1 1 0 0	0.7625 V	1 1 0 0 1 0 0	0.2500 V
0 0 1 0 1 0 0	1.2500 V	0 1 1 1 1 0 1	0.7500 V	1 1 0 0 1 0 1	0.2375 V
0 0 1 0 1 0 1	1.2375 V	0 1 1 1 1 1 0	0.7375 V	1 1 0 0 1 1 0	0.2250 V
0 0 1 0 1 1 0	1.2250 V	0 1 1 1 1 1 1	0.7250 V	1 1 0 0 1 1 1	0.2125 V
0 0 1 0 1 1 1	1.2125 V	1 0 0 0 0 0 0	0.7125 V	1 1 0 0 1 0 0	0.2000 V
0 0 1 1 0 0 0	1.2000 V	1 0 0 0 0 0 1	0.7000 V	1 1 0 1 0 0 1	0.1875 V
0 0 1 1 0 0 1	1.1875 V	1 0 0 0 0 1 0	0.6875 V	1 1 0 1 0 1 0	0.1750 V
0 0 1 1 0 1 0	1.1750 V	1 0 0 0 0 1 1	0.6750 V	1 1 0 1 0 1 1	0.1625 V
0 0 1 1 0 1 1	1.1625 V	1 0 0 0 1 0 0	0.6625 V	1 1 0 1 1 0 0	0.1500 V
0 0 1 1 1 0 0	1.1500 V	1 0 0 0 1 0 1	0.6500 V	1 1 0 1 1 0 1	0.1375 V
0 0 1 1 1 0 1	1.1375 V	1 0 0 0 1 1 0	0.6375 V	1 1 0 1 1 1 0	0.1250 V
0 0 1 1 1 1 0	1.1250 V	1 0 0 0 1 1 1	0.6250 V	1 1 0 1 1 1 1	0.1125 V
0 0 1 1 1 1 1	1.1125 V	1 0 0 1 0 0 0	0.6125 V	1 1 1 0 0 0 0	0.1000 V
0 1 0 0 0 0 0	1.1000 V	1 0 0 1 0 0 1	0.6000 V	1 1 1 0 0 0 1	0.0875 V
0 1 0 0 0 0 1	1.0875 V	1 0 0 1 0 1 0	0.5875 V	1 1 1 0 0 1 0	0.0750 V
0 1 0 0 0 1 0	1.0750 V	1 0 0 1 0 1 1	0.5750 V	1 1 1 0 0 1 1	0.0625 V
0 1 0 0 0 1 1	1.0625 V	1 0 0 1 1 0 0	0.5625 V	1 1 1 0 1 0 0	0.0500 V
0 1 0 0 1 0 0	1.0500 V	1 0 0 1 1 0 1	0.5500 V	1 1 1 0 1 0 1	0.0375 V
0 1 0 0 1 0 1	1.0375 V	1 0 0 1 1 1 0	0.5375 V	1 1 1 0 1 1 0	0.0250 V
0 1 0 0 1 1 0	1.0250 V	1 0 0 1 1 1 1	0.5250 V	1 1 1 0 1 1 1	0.0125 V
0 1 0 0 1 1 1	1.0125 V	1 0 0 1 1 1 1	0.5125 V	1 1 1 1 0 0 0	0.0000 V
		1 0 0 1 1 1 1	0.5000 V	1 1 1 1 0 0 1	0.0000 V
				1 1 1 1 0 1 0	0.0000 V
				1 1 1 1 0 1 1	0.0000 V
				1 1 1 1 1 0 0	0.0000 V
				1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0	0.0000 V
				1 1 1 1 1 1 1	0.0000 V

*Yonah Processor (2.33 GHz / 800 MHz : TBD)

DRAW	ZHANG, ELLEN	DATE	3/15/2007	TITLE	SHANGHAI MEROM(2/3)	SAMSUNG ELECTRONICS
CHECK	ZHENG, ROKY	DEV. STEP	SR			
APPROVAL	LEE, KEVIN	REV	1.0			
MODULE CODE		LAST ENT				
				March 15, 2007 10:33:33 AM	PAGE	10 OF 54

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DRAW	ZHANG, ELLEN	DATE	3/15/2007	TITLE	SHANGHAI		SAMSUNG ELECTRONICS
CHECK	ZHENG, ROKY	DEV. STEP	SR	MEROM(3/3)		PART NO. BA41-00774A/00732A	
APPROVAL	LEE, KEVIN	REV	1.0	March 15, 2007 10:33:33 AM		PAGE 11 OF 54	
MODULE CODE	LAST EDIT						

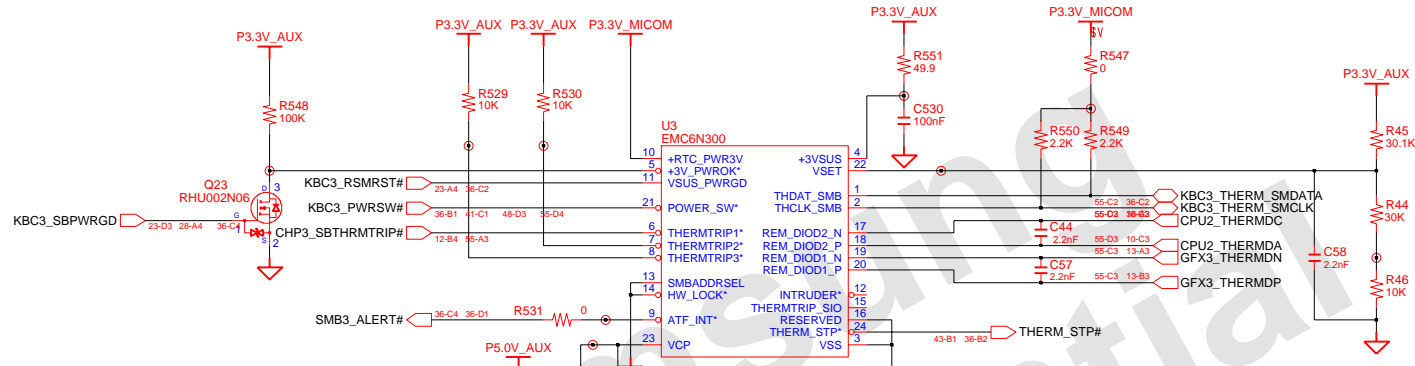
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Refer To Thermal Sensor Layout Guidelines.

- Place the Thermal Sensor close to a remote diode.
- Keep traces away from high voltage (+12V bus)
- Keep traces away from fast data buses and CRT signal.
- Use recommended trace widths and spacings (10mil)
- Place a ground plane under the traces.
- Use guard traces flanking DXP and DXN and connecting to GND

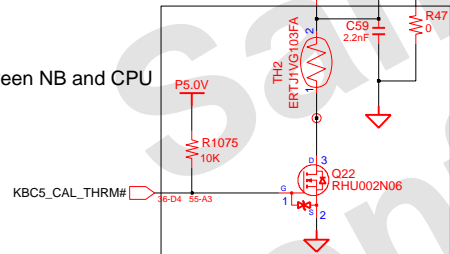
CPU / RS600 Thermal Sensor



Please place this part between CPU & MCH

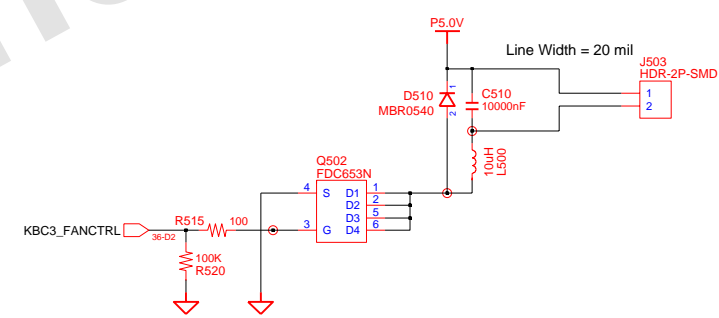
PLACE THIS AT THE OPPOSITE SIDE OF CPU

Place between NB and CPU



NO_STUFF

FAN Control Logic

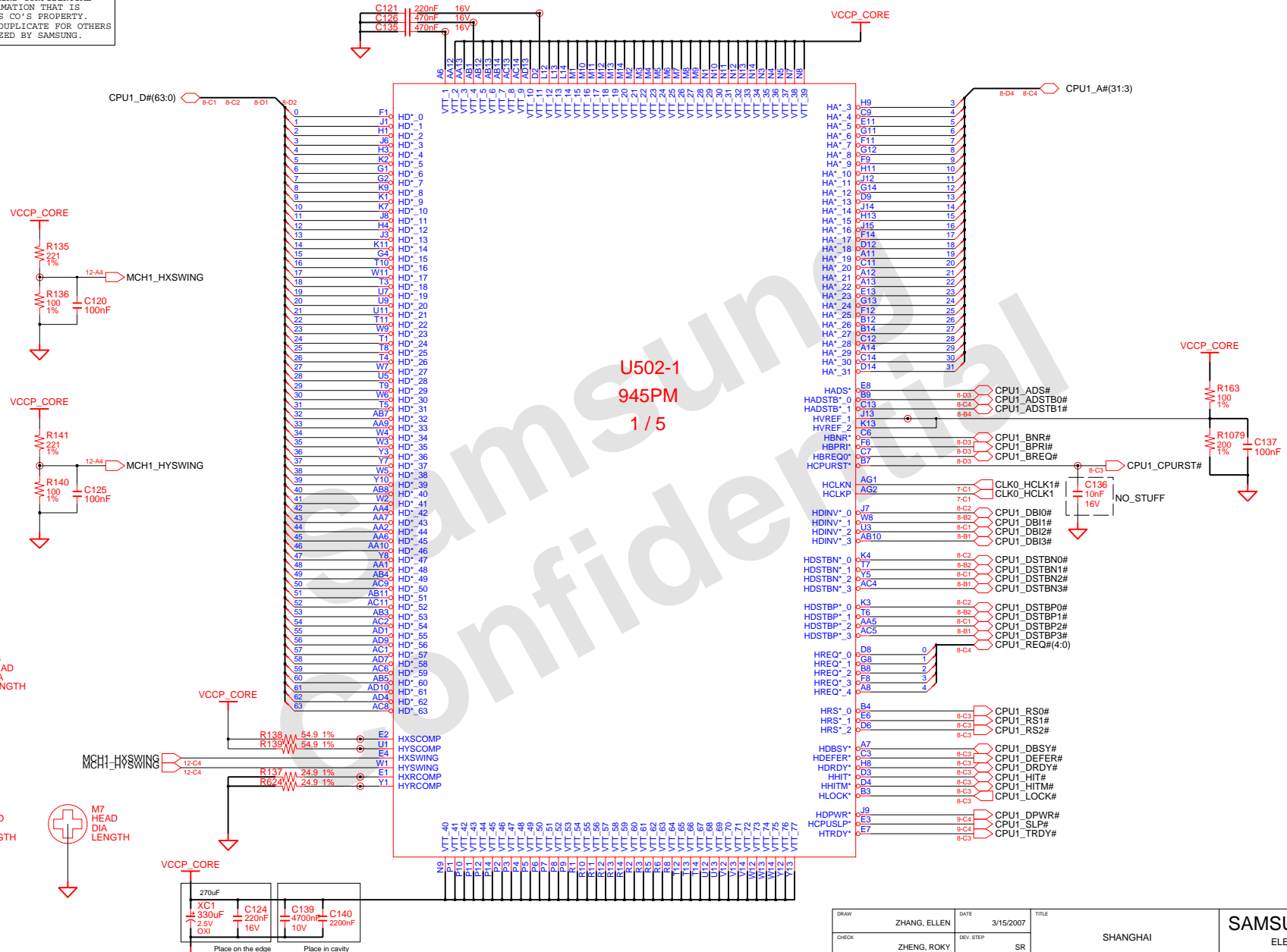


Line Width = 20 mil

DRAW	ZHANG, ELLEN	DATE	3/15/2007	TITLE	SHANGHAI THERMAL & FAN	SAMSUNG ELECTRONICS
CHECK	ZHENG, ROKY	DEV. STEP	SR			
APPROVAL	LEE, KEVIN	REV	1.0			
MODULE CODE		LAST EDIT				
March 15, 2007 10:33:33 AM						PAGE 12 OF 54

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DRAW	ZHANG, ELLEN	DATE	3/15/2007	TITLE	
CHECK	ZHENG, ROKY	DEV. STEP	SR	SHANGHAI	
APPROVAL	LEE, KEVIN	REV	1.0	CALISTOGA(1/5)	
MODULE CODE		LAST EDIT			

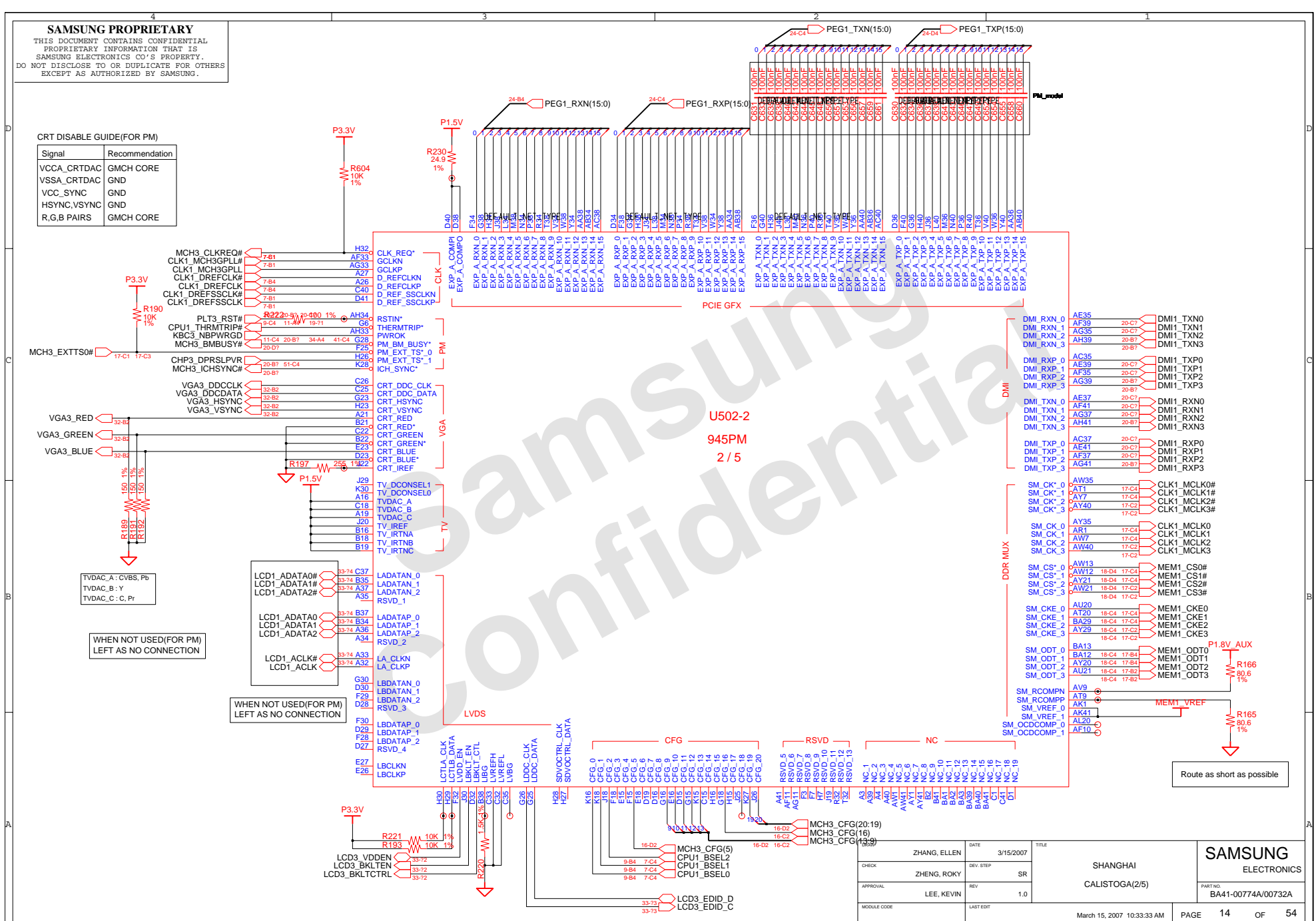
SAMSUNG	
ELECTRONICS	
PART NO.	BA41-00774A/00732A
March 15, 2007 10:33:33 AM	PAGE 13 OF 54

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CRT DISABLE GUIDE(FOR PM)

Signal	Recommendation
VCCA_CRTDAC	GMCH CORE
VSSA_CRTDAC	GND
VCC_SYNC	GND
HSYNC_VSYNC	GND
R,G,B PAIRS	GMCH CORE



WHEN NOT USED(FOR PM)
LEFT AS NO CONNECTION

WHEN NOT USED(FOR PM)
LEFT AS NO CONNECTION

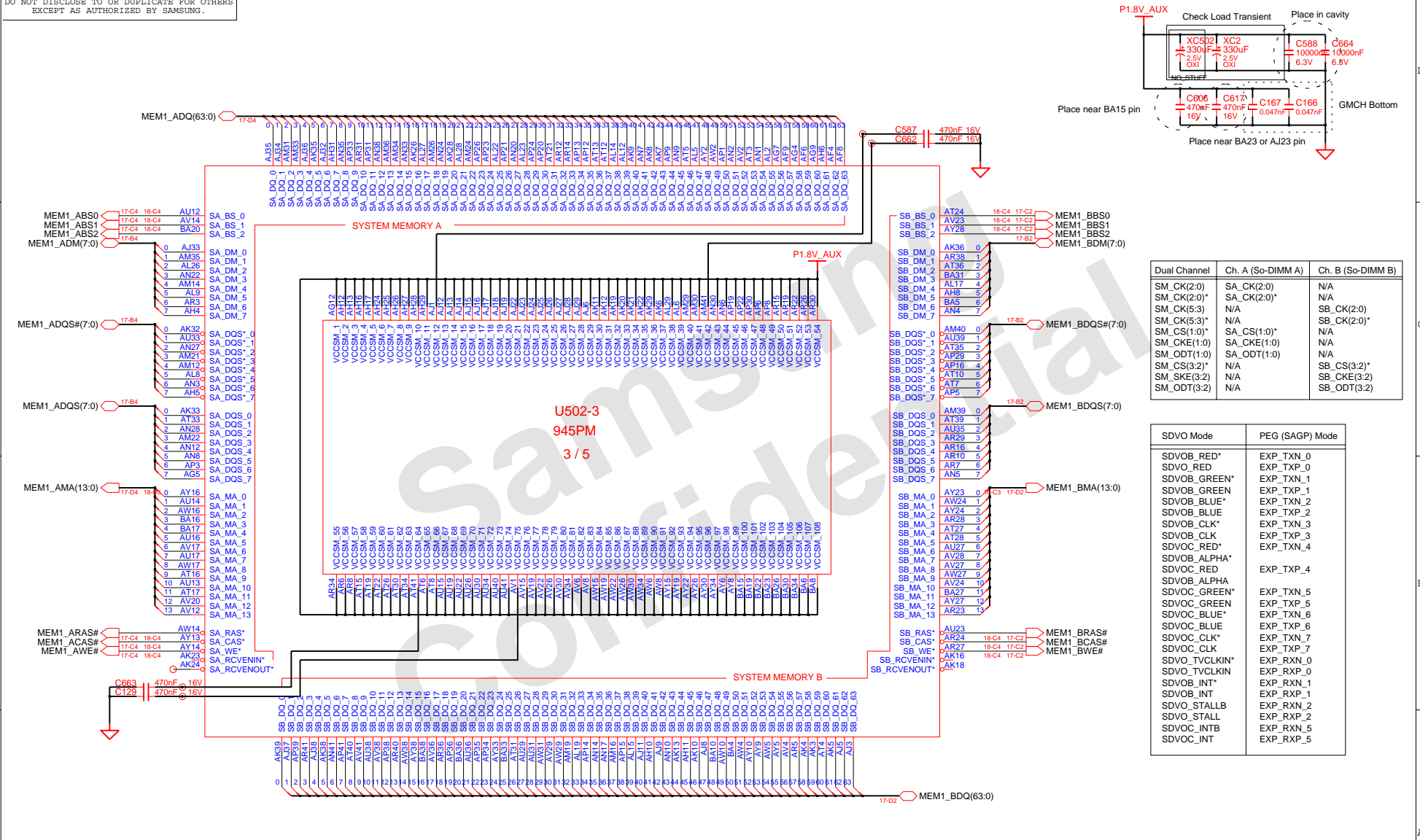
Route as short as possible

CHECK	DATE	TITLE
ZHANG, ELLEN	3/15/2007	
ZHENG, ROKY	DEV. STEP	SR
APPROVAL	REV	1.0
LEE, KEVIN	LAST EDIT	
MODULE CODE		

DATE	TITLE
3/15/2007	
March 15, 2007 10:33:33 AM	

SAMSUNG ELECTRONICS	
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Dual Channel	Ch. A (So-DIMM A)	Ch. B (So-DIMM B)
SM_CK(2:0)	SA_CK(2:0)	N/A
SM_CK(2:0)*	SA_CK(2:0)*	N/A
SM_CK(5:3)	N/A	SB_CK(2:0)
SM_CK(5:3)*	N/A	SB_CK(2:0)*
SM_CS(1:0)	SA_CS(1:0)	N/A
SM_CKE(1:0)	SA_CKE(1:0)	N/A
SM_ODT(1:0)	SA_ODT(1:0)	N/A
SM_CS(3:2)	N/A	SB_CS(3:2)*
SM_SKE(3:2)	N/A	SB_CKE(3:2)
SM_ODT(3:2)	N/A	SB_ODT(3:2)

SDVO Mode	PEG (SAGP) Mode
SDVO_RED*	EXP_TXN_0
SDVO_RED	EXP_TXP_0
SDVO_GREEN*	EXP_TXN_1
SDVO_GREEN	EXP_TXP_1
SDVO_BLUE*	EXP_TXN_2
SDVO_BLUE	EXP_TXP_2
SDVO_CLK*	EXP_TXN_3
SDVO_CLK	EXP_TXP_3
SDVOC_RED*	EXP_TXN_4
SDVOC_RED	EXP_TXP_4
SDVOC_ALPHA*	EXP_TXN_5
SDVOC_ALPHA	EXP_TXP_5
SDVOC_GREEN*	EXP_TXN_6
SDVOC_GREEN	EXP_TXP_6
SDVOC_BLUE*	EXP_TXN_7
SDVOC_BLUE	EXP_TXP_7
SDVOC_CLK*	EXP_TXN_8
SDVOC_CLK	EXP_TXP_8
SDVO_TVCLKIN*	EXP_RXN_0
SDVO_TVCLKIN	EXP_RXP_0
SDVOC_INT*	EXP_RXN_1
SDVOC_INT	EXP_RXP_1
SDVO_STALLB	EXP_RXN_2
SDVO_STALL	EXP_RXP_2
SDVOC_INTB	EXP_RXN_5
SDVOC_INT	EXP_RXP_5

DRAW	ZHANG, ELLEN	DATE	3/15/2007	TITLE		SAMSUNG ELECTRONICS PART NO. BA41-00774A/00732A
CHECK	ZHENG, ROKY	DEV. STEP	SR	SHANGHAI		
APPROVAL	LEE, KEVIN	REV	1.0	CALISTOGA (3/5)		
MODULE CODE		LAST EDIT				
				March 15, 2007 10:33:33 AM	PAGE 15 OF 54	

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P1.5V

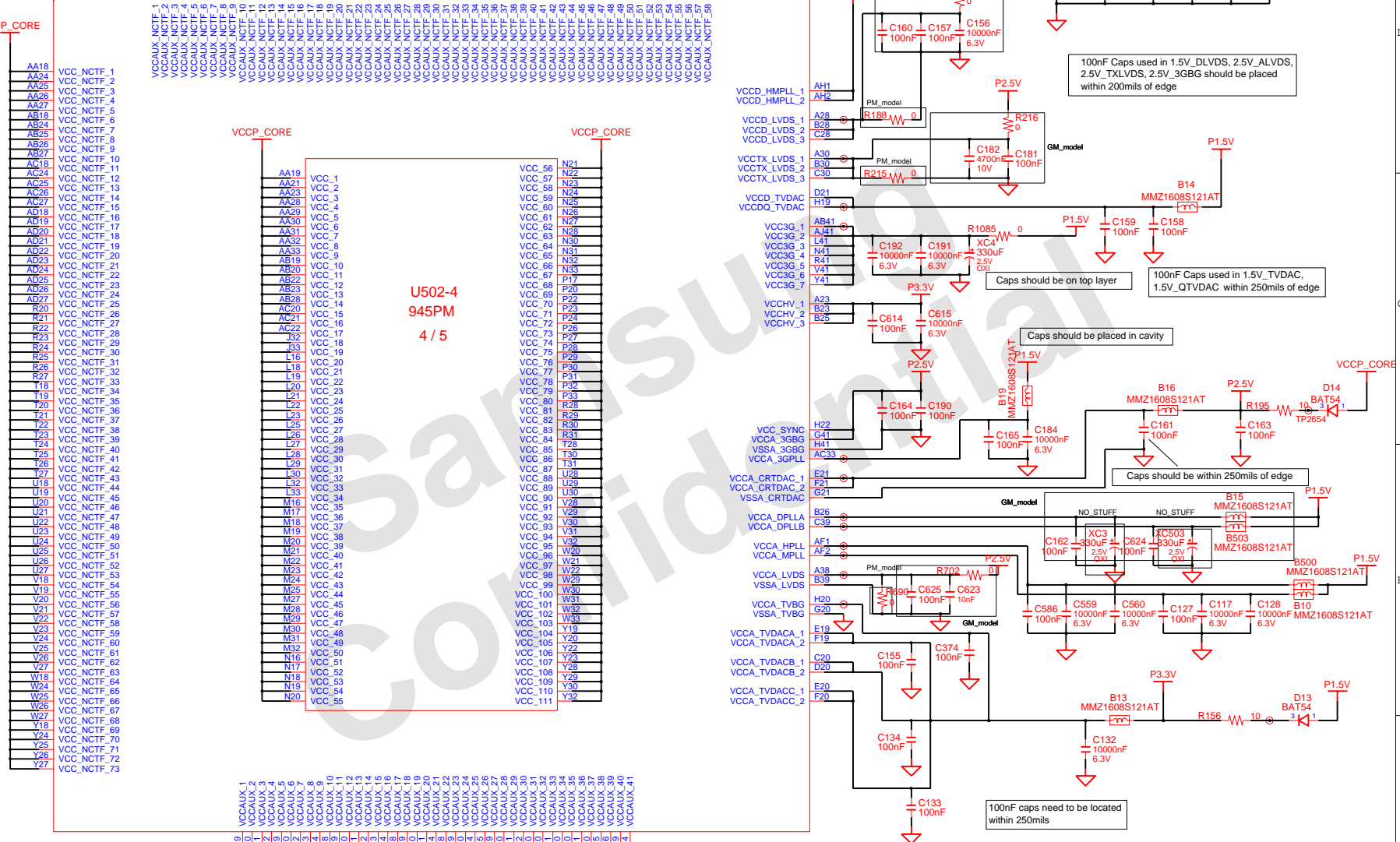
AA18	VCCAUX_NCTIF_1	AA18	VCCAUX_NCTIF_1
AA19	VCCAUX_NCTIF_2	AA19	VCCAUX_NCTIF_2
AA20	VCCAUX_NCTIF_3	AA20	VCCAUX_NCTIF_3
AA21	VCCAUX_NCTIF_4	AA21	VCCAUX_NCTIF_4
AA22	VCCAUX_NCTIF_5	AA22	VCCAUX_NCTIF_5
AA23	VCCAUX_NCTIF_6	AA23	VCCAUX_NCTIF_6
AA24	VCCAUX_NCTIF_7	AA24	VCCAUX_NCTIF_7
AA25	VCCAUX_NCTIF_8	AA25	VCCAUX_NCTIF_8
AA26	VCCAUX_NCTIF_9	AA26	VCCAUX_NCTIF_9
AA27	VCCAUX_NCTIF_10	AA27	VCCAUX_NCTIF_10
AA28	VCCAUX_NCTIF_11	AA28	VCCAUX_NCTIF_11
AA29	VCCAUX_NCTIF_12	AA29	VCCAUX_NCTIF_12
AA30	VCCAUX_NCTIF_13	AA30	VCCAUX_NCTIF_13
AA31	VCCAUX_NCTIF_14	AA31	VCCAUX_NCTIF_14
AA32	VCCAUX_NCTIF_15	AA32	VCCAUX_NCTIF_15
AA33	VCCAUX_NCTIF_16	AA33	VCCAUX_NCTIF_16
AA34	VCCAUX_NCTIF_17	AA34	VCCAUX_NCTIF_17
AA35	VCCAUX_NCTIF_18	AA35	VCCAUX_NCTIF_18
AA36	VCCAUX_NCTIF_19	AA36	VCCAUX_NCTIF_19
AA37	VCCAUX_NCTIF_20	AA37	VCCAUX_NCTIF_20
AA38	VCCAUX_NCTIF_21	AA38	VCCAUX_NCTIF_21
AA39	VCCAUX_NCTIF_22	AA39	VCCAUX_NCTIF_22
AA40	VCCAUX_NCTIF_23	AA40	VCCAUX_NCTIF_23
AA41	VCCAUX_NCTIF_24	AA41	VCCAUX_NCTIF_24
AA42	VCCAUX_NCTIF_25	AA42	VCCAUX_NCTIF_25
AA43	VCCAUX_NCTIF_26	AA43	VCCAUX_NCTIF_26
AA44	VCCAUX_NCTIF_27	AA44	VCCAUX_NCTIF_27
AA45	VCCAUX_NCTIF_28	AA45	VCCAUX_NCTIF_28
AA46	VCCAUX_NCTIF_29	AA46	VCCAUX_NCTIF_29
AA47	VCCAUX_NCTIF_30	AA47	VCCAUX_NCTIF_30
AA48	VCCAUX_NCTIF_31	AA48	VCCAUX_NCTIF_31
AA49	VCCAUX_NCTIF_32	AA49	VCCAUX_NCTIF_32
AA50	VCCAUX_NCTIF_33	AA50	VCCAUX_NCTIF_33
AA51	VCCAUX_NCTIF_34	AA51	VCCAUX_NCTIF_34
AA52	VCCAUX_NCTIF_35	AA52	VCCAUX_NCTIF_35
AA53	VCCAUX_NCTIF_36	AA53	VCCAUX_NCTIF_36
AA54	VCCAUX_NCTIF_37	AA54	VCCAUX_NCTIF_37
AA55	VCCAUX_NCTIF_38	AA55	VCCAUX_NCTIF_38
AA56	VCCAUX_NCTIF_39	AA56	VCCAUX_NCTIF_39
AA57	VCCAUX_NCTIF_40	AA57	VCCAUX_NCTIF_40
AA58	VCCAUX_NCTIF_41	AA58	VCCAUX_NCTIF_41
AA59	VCCAUX_NCTIF_42	AA59	VCCAUX_NCTIF_42
AA60	VCCAUX_NCTIF_43	AA60	VCCAUX_NCTIF_43
AA61	VCCAUX_NCTIF_44	AA61	VCCAUX_NCTIF_44
AA62	VCCAUX_NCTIF_45	AA62	VCCAUX_NCTIF_45
AA63	VCCAUX_NCTIF_46	AA63	VCCAUX_NCTIF_46
AA64	VCCAUX_NCTIF_47	AA64	VCCAUX_NCTIF_47
AA65	VCCAUX_NCTIF_48	AA65	VCCAUX_NCTIF_48
AA66	VCCAUX_NCTIF_49	AA66	VCCAUX_NCTIF_49
AA67	VCCAUX_NCTIF_50	AA67	VCCAUX_NCTIF_50
AA68	VCCAUX_NCTIF_51	AA68	VCCAUX_NCTIF_51
AA69	VCCAUX_NCTIF_52	AA69	VCCAUX_NCTIF_52
AA70	VCCAUX_NCTIF_53	AA70	VCCAUX_NCTIF_53
AA71	VCCAUX_NCTIF_54	AA71	VCCAUX_NCTIF_54
AA72	VCCAUX_NCTIF_55	AA72	VCCAUX_NCTIF_55
AA73	VCCAUX_NCTIF_56	AA73	VCCAUX_NCTIF_56
AA74	VCCAUX_NCTIF_57	AA74	VCCAUX_NCTIF_57
AA75	VCCAUX_NCTIF_58	AA75	VCCAUX_NCTIF_58
AA76	VCCAUX_NCTIF_59	AA76	VCCAUX_NCTIF_59
AA77	VCCAUX_NCTIF_60	AA77	VCCAUX_NCTIF_60

VCCP_CORE

VCCP_CORE

VCCP_CORE

U502-4
945PM
4 / 5

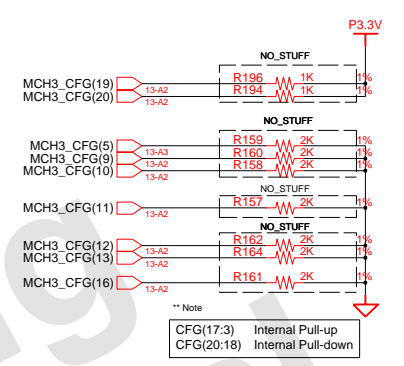
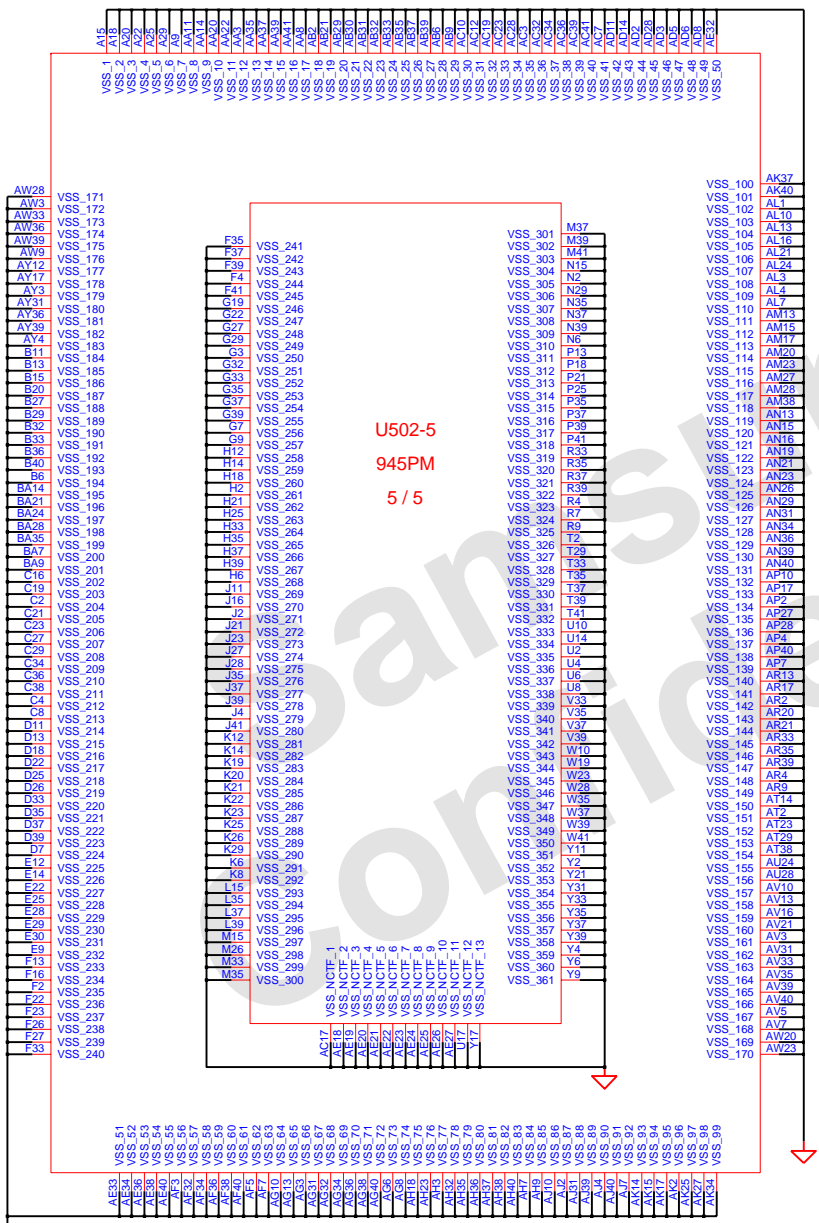


DRAW	ZHANG, ELLEN	DATE	3/15/2007	TITLE	
CHECK	ZHENG, ROKY	DEV. STEP	SR	SHANGHAI	
APPROVAL	LEE, KEVIN	REV	1.0	CALISTOGA (4/5)	
MODULE CODE		LAST EDIT			

SAMSUNG ELECTRONICS	
PART NO.	BA41-00774A/00732A
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** Note
CFG(17:3) Internal Pull-up
CFG(20:18) Internal Pull-down

** Note *POCAFEB-10 Only (Remove in MP Model)

CFG#	Current Setting (def.: default Option)	
	Low	High
CFG(5)	DMIX2	DMIX4 (def.)
CFG(6)	Reserved	DDR-II (def.)
CFG(7)	DT/Transportable	Mobile CPU (def.)
CFG(9)	PEG Reversal	Normal
CFG(16)	Dynamic ODT	Enabled ODT (def.)
CFG(18)	VCC 1.05V (def.)	VCC 1.5V
CFG(19)	DMI Lane Normal	DMI Lane Reversal
CFG(20)	SDVO or PCIE X1 Only(def.)	SDVO and PCIE X1 Simultaneously

When CFG 13:12 are pulled down to '00', certain clocks within Calistoga will become free-running clocks.

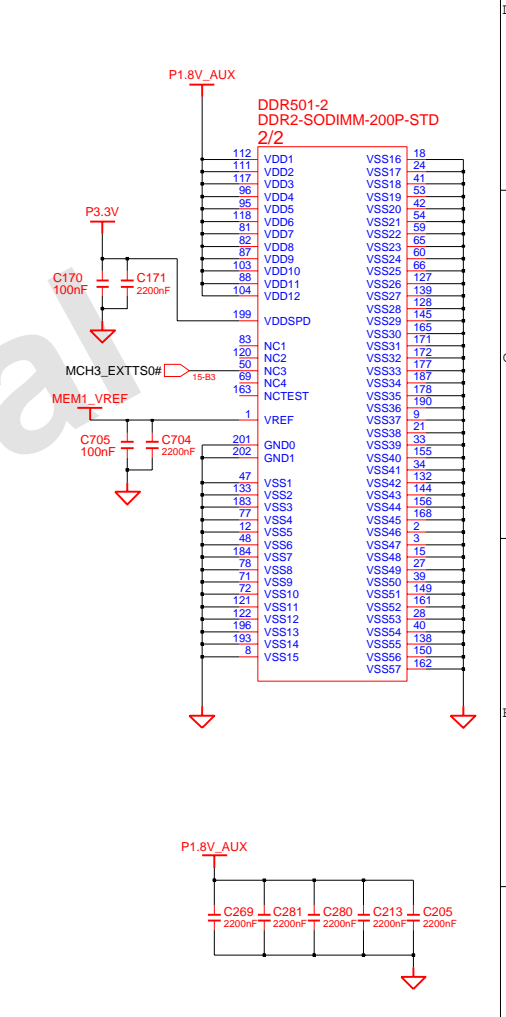
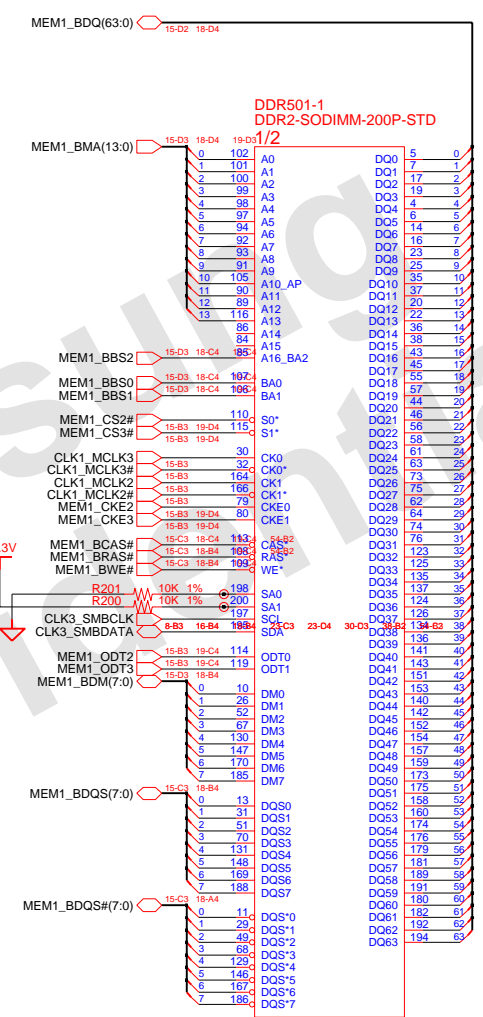
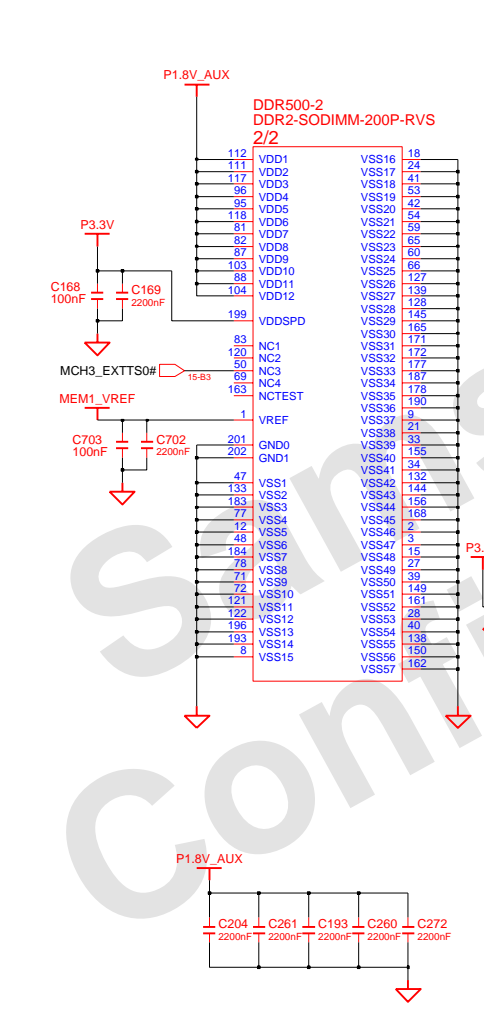
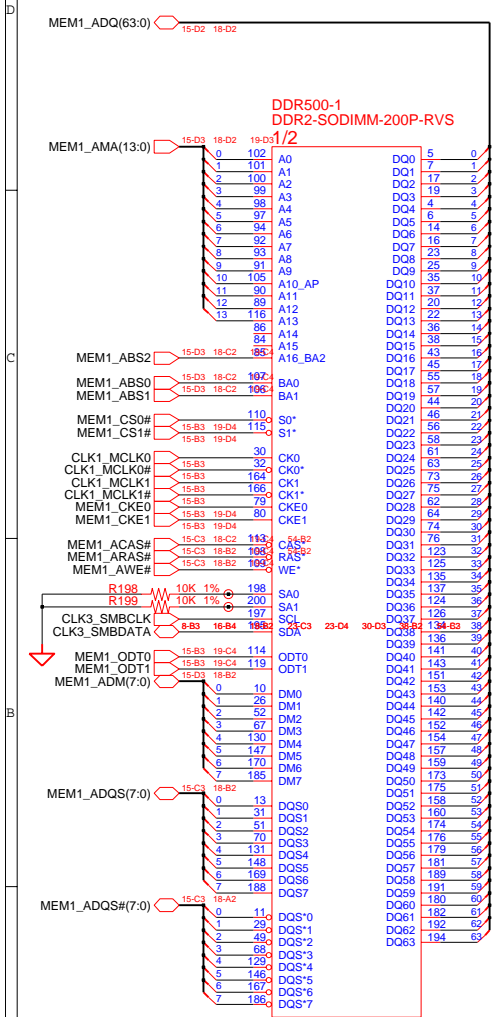
This will lead to a rise in avg. power, but eliminates any possible clock-timing marginalities involved in clock power-up/power-down.

Intel strongly recommends leaving CFG 13:12 = NC (Internal PU to '11) to ensure low avg.power.

DRAW	ELLEN,ZHANG	DATE	03/15/2007	TITLE	SHANGHAI CALISTOGA(5/5)	SAMSUNG ELECTRONICS	
CHECK	ROKY,ZHENG	DEV. STEP	SR				
APPROVAL	KEVIN,LEE	REV	1. 0				
MODULE CODE		LAST EDIT	MARCH,15,2007 10:24:38AM				
						PART NO.	BA41-00774A/00732A
						PAGE	17 OF 54

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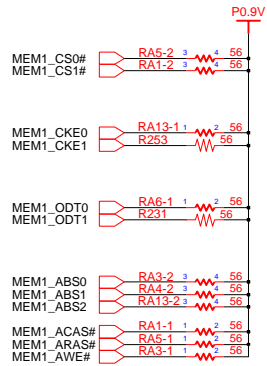


DRAW	ZHANG, ELLEN	DATE	3/15/2007	TITLE	SHANGHAI MEMORY SODIMM	SAMSUNG ELECTRONICS
CHECK	ZHENG, ROKY	DEV. STEP	SR	APPROVAL	LEE, KEVIN	
MODULE CODE		LAST EDIT		March 15, 2007 10:33:33 AM	PAGE	18 OF 54

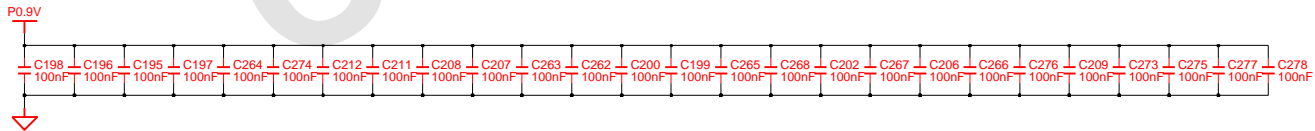
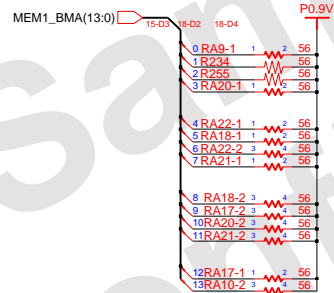
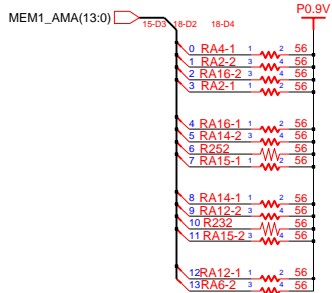
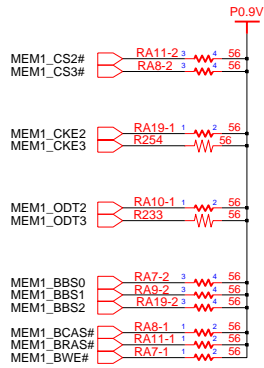
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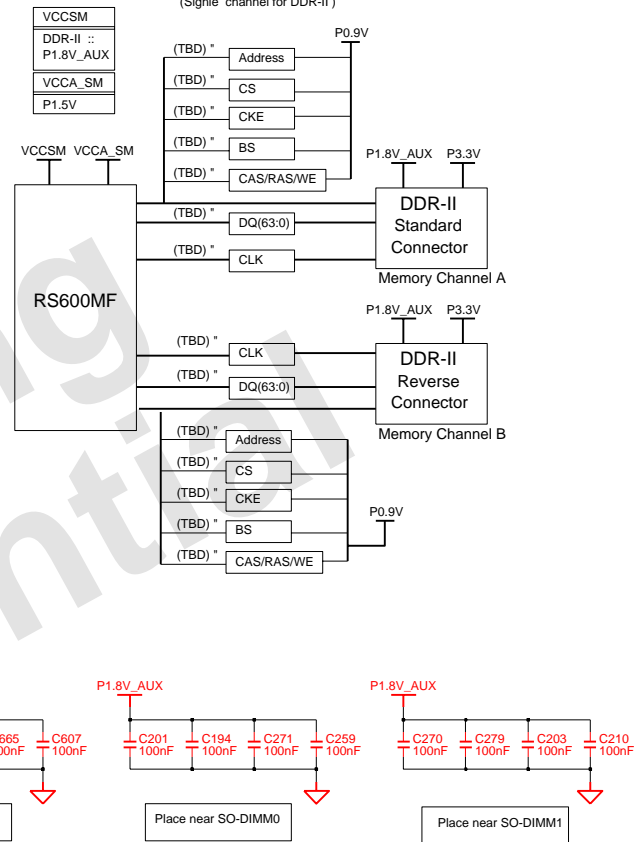
Channel 1



Channel 2

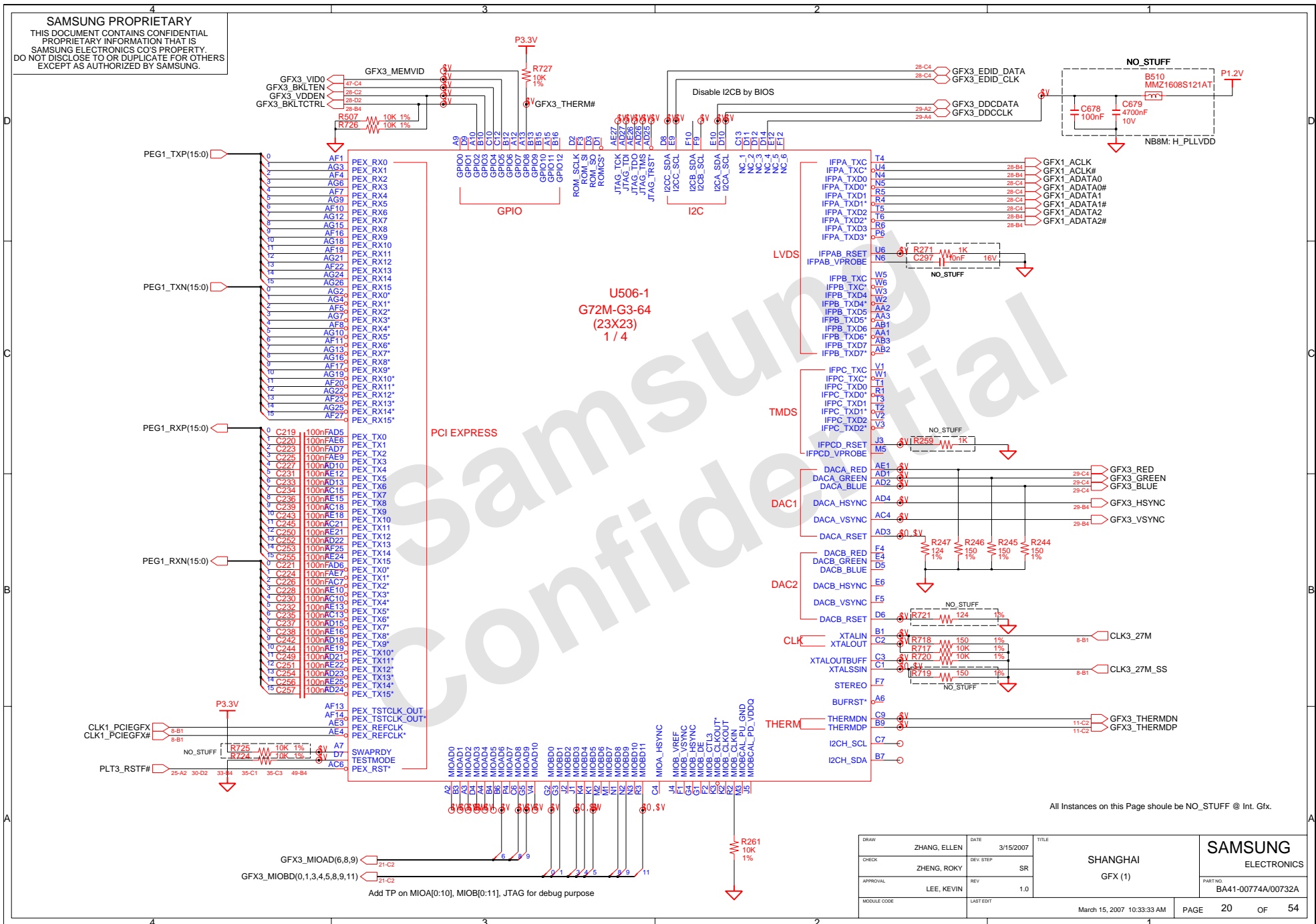


Memory Topology



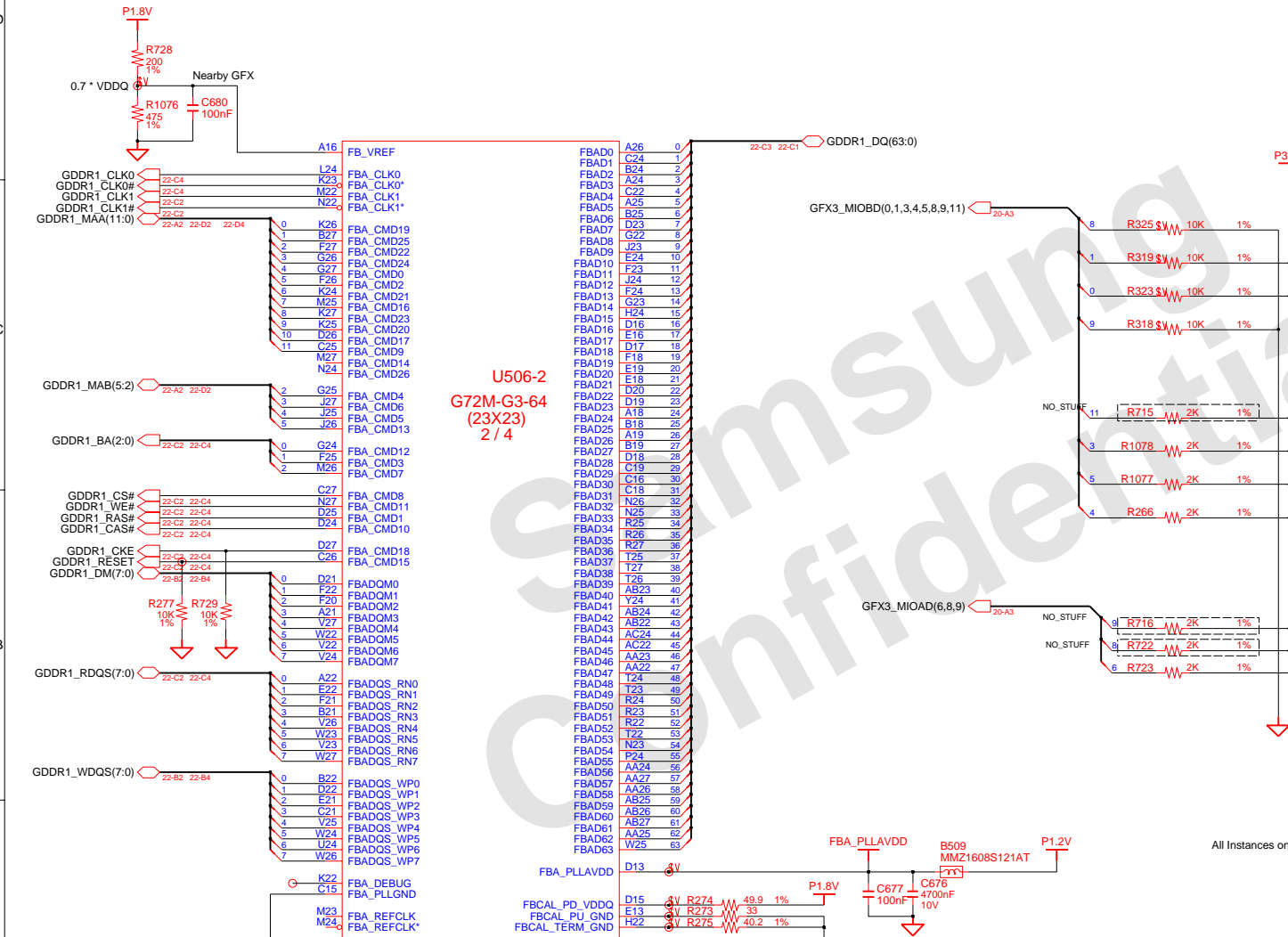
DRAW	ZHANG, ELLEN	DATE	3/15/2007	TITLE	SHANGHAI DDR2 TERMINATION	SAMSUNG ELECTRONICS PART NO. BA41-00774A/00732A
CHECK	ZHENG, ROKY	DEV. STEP	SR			
APPROVAL	LEE, KEVIN	REV	1.0			
MODULE CODE		LAST EDIT				
March 15, 2007 10:33:33 AM				PAGE		

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DRAW	ZHANG, ELLEN	DATE	3/15/2007	TITLE	SHANGHAI GFX (1)	SAMSUNG ELECTRONICS			
CHECK	ZHENG, ROKY	DEV STEP	SR						
APPROVAL	LEE, KEVIN	REV	1.0						
MODULE CODE		LAST ENT							
March 15, 2007 10:33:33 AM						PAGE	20	OF	54

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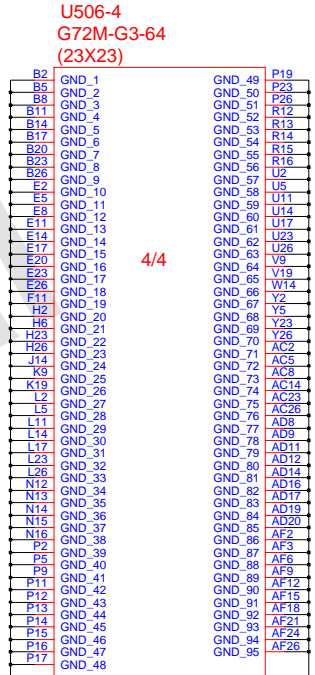
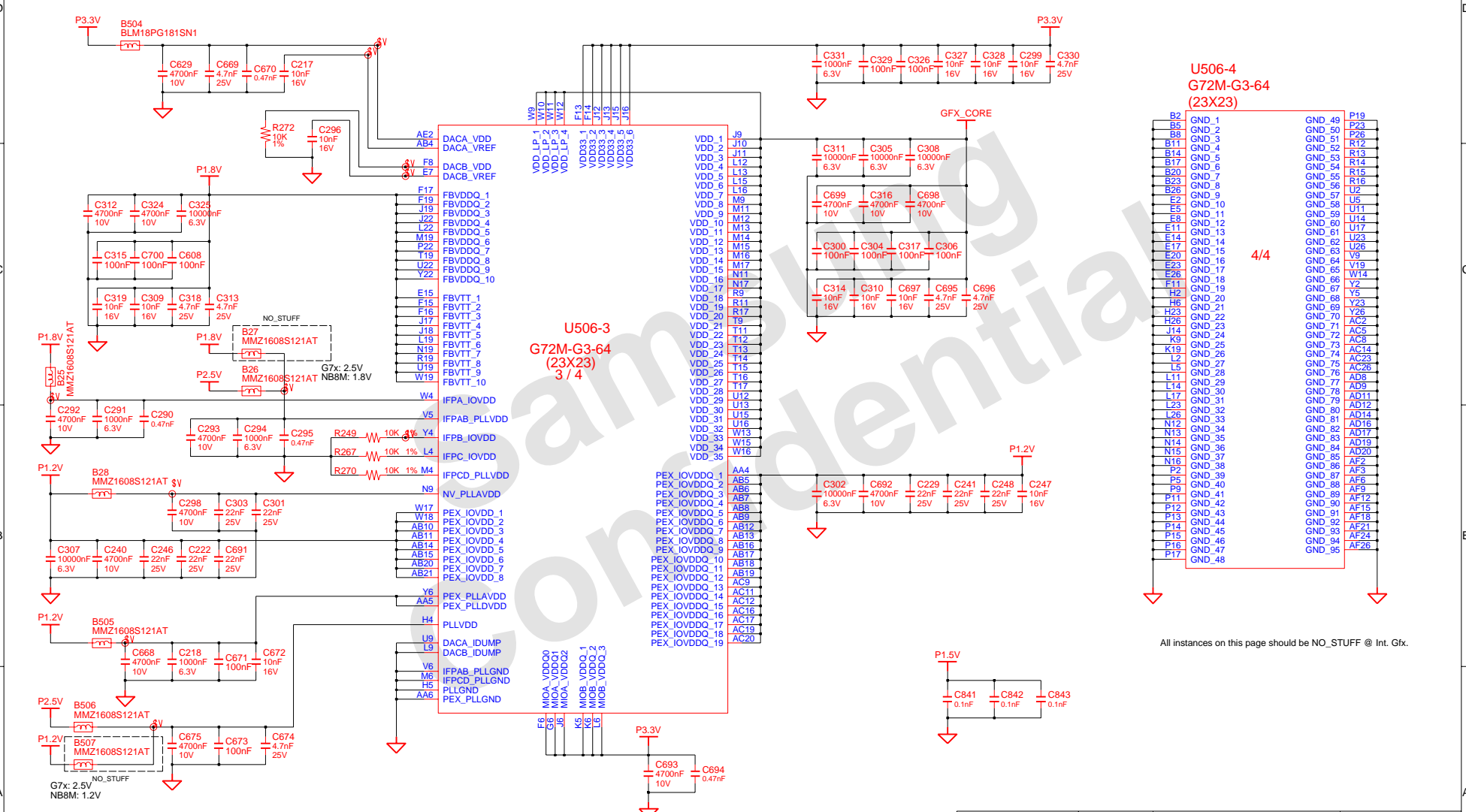
STRAPS

SUB_VENDOR		MIOD[1]
0	No Video BIOS ROM	
1	Video BIOS ROM is present (DEF.) (For merged BIOS)	
RAM_CFG[2:0]		MIOD[8, 1, 0]
000	8M x 32 DDR, Monolithic, 2.5V I/O	
001	8M x 32 DDR, Monolithic, 1.8V I/O	
010	8M x 32 DDR, 1.8V I/O Analog DLL (SEC K4D55320F-GC)	
011	16M x 32 DDR, 1.8V I/O, Hynix Stacked Die (2 x 8M x32)	
100	4M x 32 DDR, 1.8V I/O	
101	Reserved	
110	4M x 32 DDR, 2.5V I/O	
111	Reserved	
RAM_CFG[3]		MIOD[9]
0	Full Width	
1	Half Width	
CRYSTAL[1:0]		MIOD[6, 2]
00	13.5MHz	
01	14.318MHz	
10	27.0MHz (DEF.)	
11	Reserved	
TMODE[1:0]		MIOD[10, 7]
000	SECAM	
001	NTSC (DEF.)	
010	PAL	
011	VGA	
PCI_DEVID[3:0]		MIOD[11, 3, 5, 4]
G72M	0x01D8	
G72MIV	0x01D7	
G73M	0x0398	
3GIO_PADCFG[2:0]		MIOD[9, 8, 6]
000	Desktop (DEF.)	
001	Mobile1 (G72M)	
010	Mobile2 G7x or NV42	
011	Mobile3	
PEX_PLL_EN_TERM		MIOD[0]
0	Enabled (DEF.)	
1	Disabled	

All Instances on this Page should be NO_STUFF @ Int. Gfx.

DRAW	ZHANG, ELLEN	DATE	3/15/2007	TITLE	SHANGHAI GFX (2)	SAMSUNG ELECTRONICS
CHECK	ZHENG, ROKY	DEV_STEP	SR			
APPROVAL	LEE, KEVIN	REV	1.0			
MODULE CODE		LAST ENT				
March 15, 2007 10:33:33 AM					PAGE	21 OF 54

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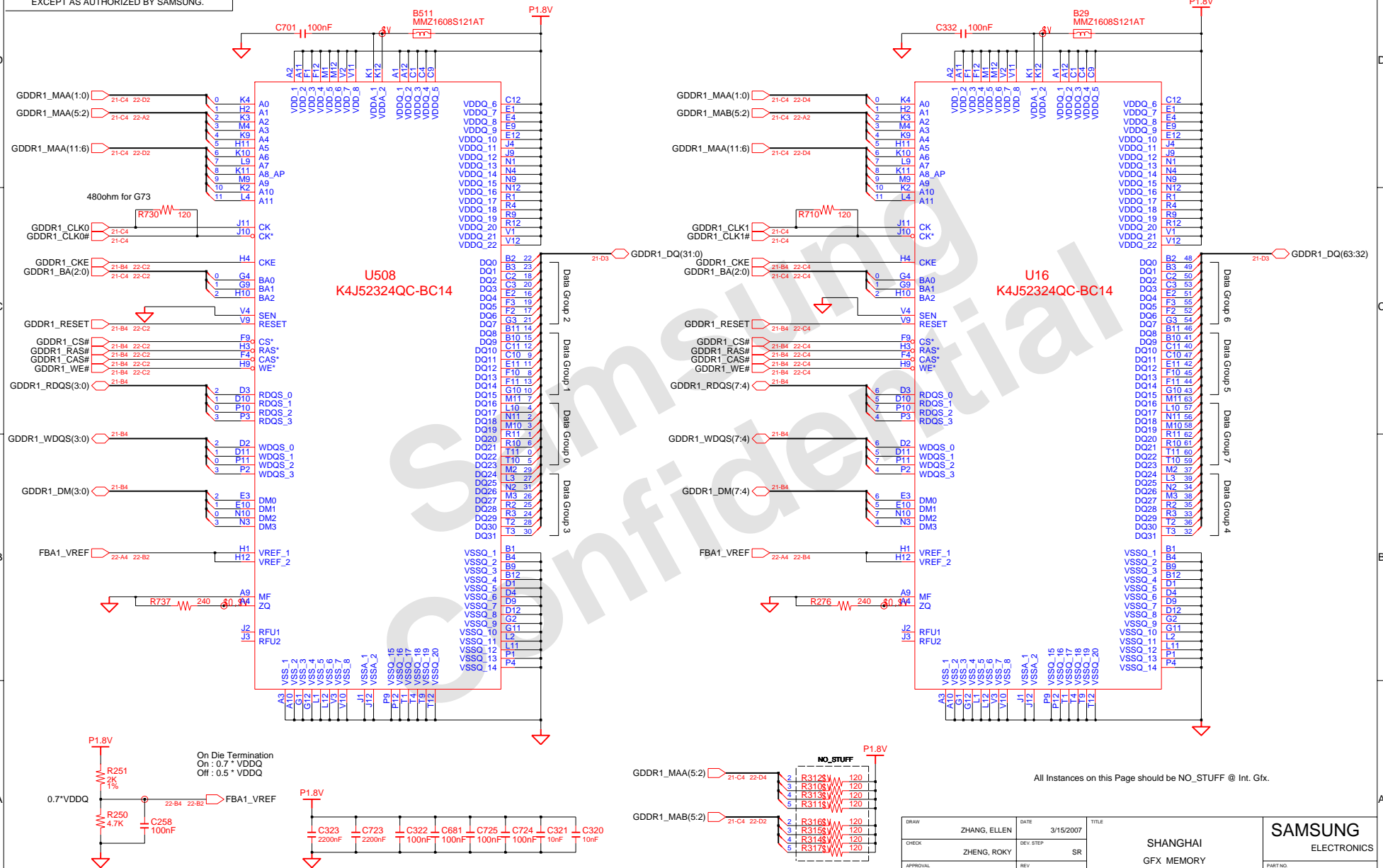


All instances on this page should be NO_STUFF @ Int. Gfx.

DRAW	ZHANG, ELLEN	DATE	3/15/2007	TITLE	SAMSUNG ELECTRONICS SHANGHAI GFX (3) & (4) PART NO. BA41-00774A/00732A March 15, 2007 10:33:33 AM
CHECK	ZHENG, ROKY	DEV_STEP	SR		
APPROVAL	LEE, KEVIN	REV	1.0		
MODULE CODE		LAST ENT			

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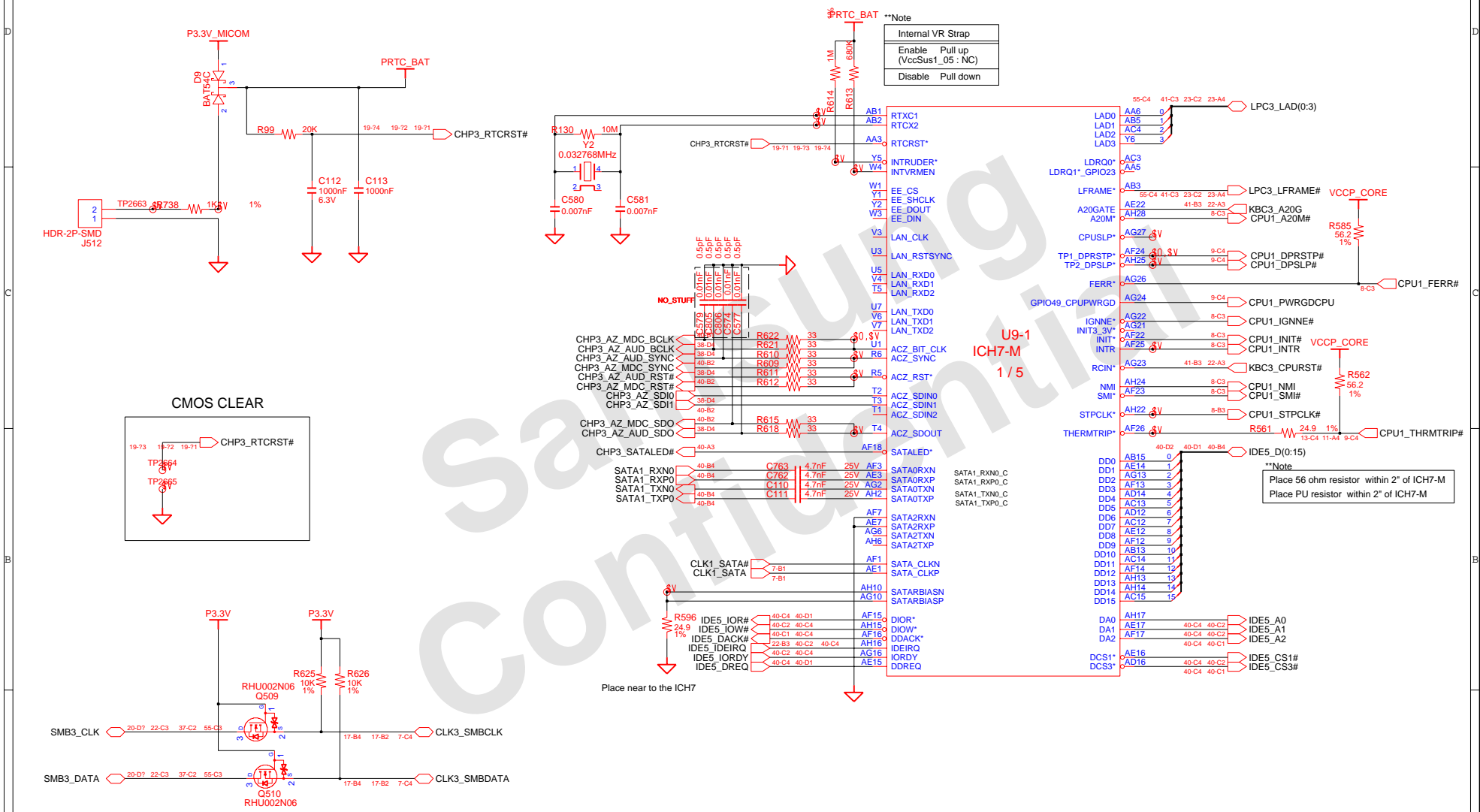


All instances on this Page should be NO_STUFF @ Int. Gfx.

DRAW	ZHANG, ELLEN	DATE	3/15/2007	TITLE	SHANGHAI GFX MEMORY	SAMSUNG ELECTRONICS PART NO. BA41-00774A/00732A
CHECK	ZHENG, ROKY	DEV STEP	SR			
APPROVAL	LEE, KEVIN	REV	1.0			
MODULE CODE		LAST EDIT				
March 15, 2007 10:33:33 AM						PAGE 23 OF 52

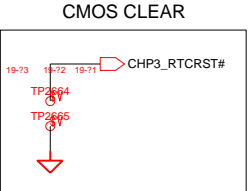
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****Note**

Internal VR Strap	
Enable	Pull up
	(VccSus1_05 : NC)
Disable	Pull down



****Note**

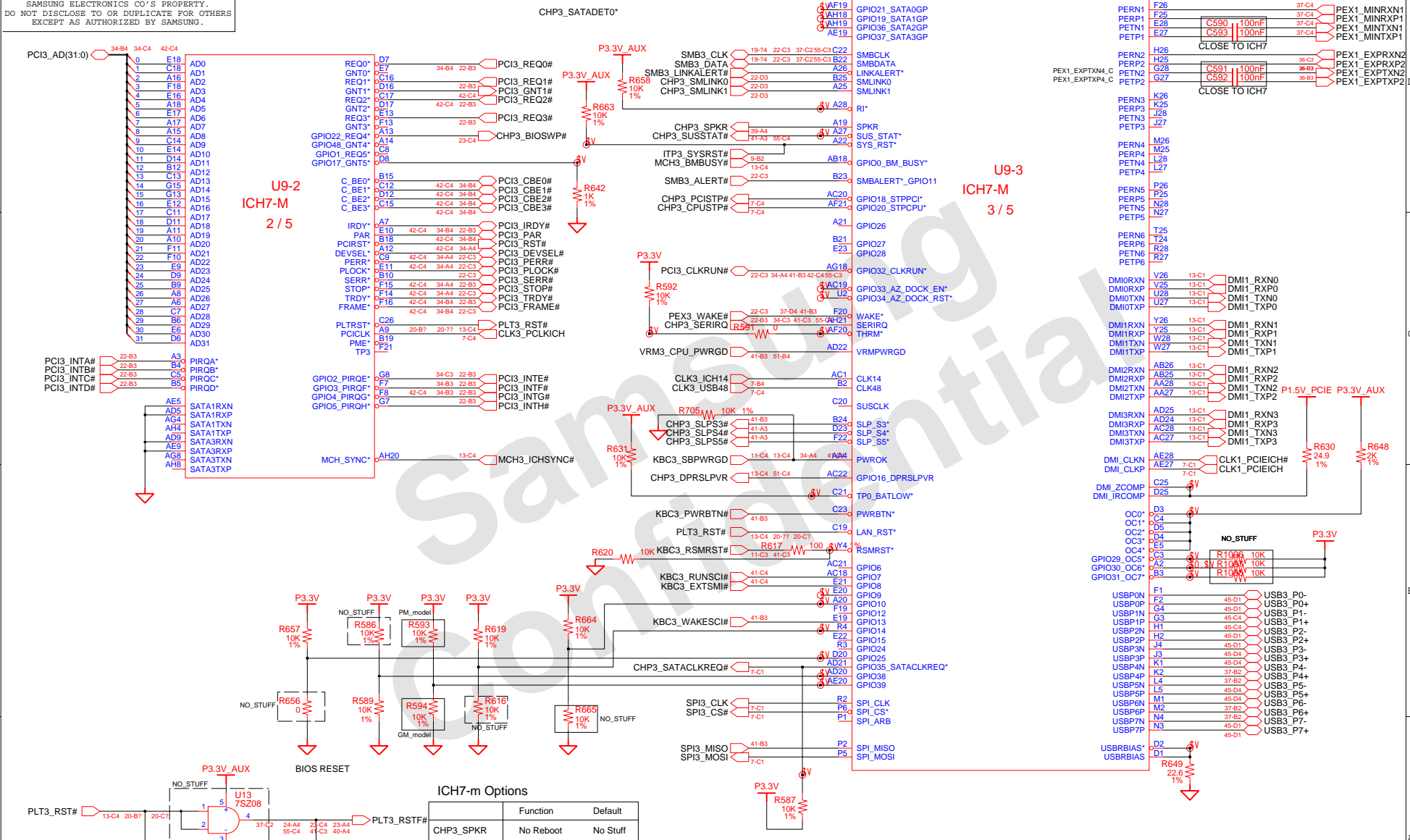
Place 56 ohm resistor within 2" of ICH7-M

Place PU resistor within 2" of ICH7-M

DRAW	ZHANG, ELLEN	DATE	3/15/2007	TITLE	SHANGHAI ICH7(1/4)	SAMSUNG ELECTRONICS
CHECK	ZHENG, ROKY	DEV. STEP	SR			
APPROVAL	LEE, KEVIN	REV	1.0			
MODULE CODE	undefined	LAST EDIT	March 15, 2007 10:33:33 AM	PAGE 24 OF 54		

PART NO. BA41-00774A/00732A

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ICH7-m Options

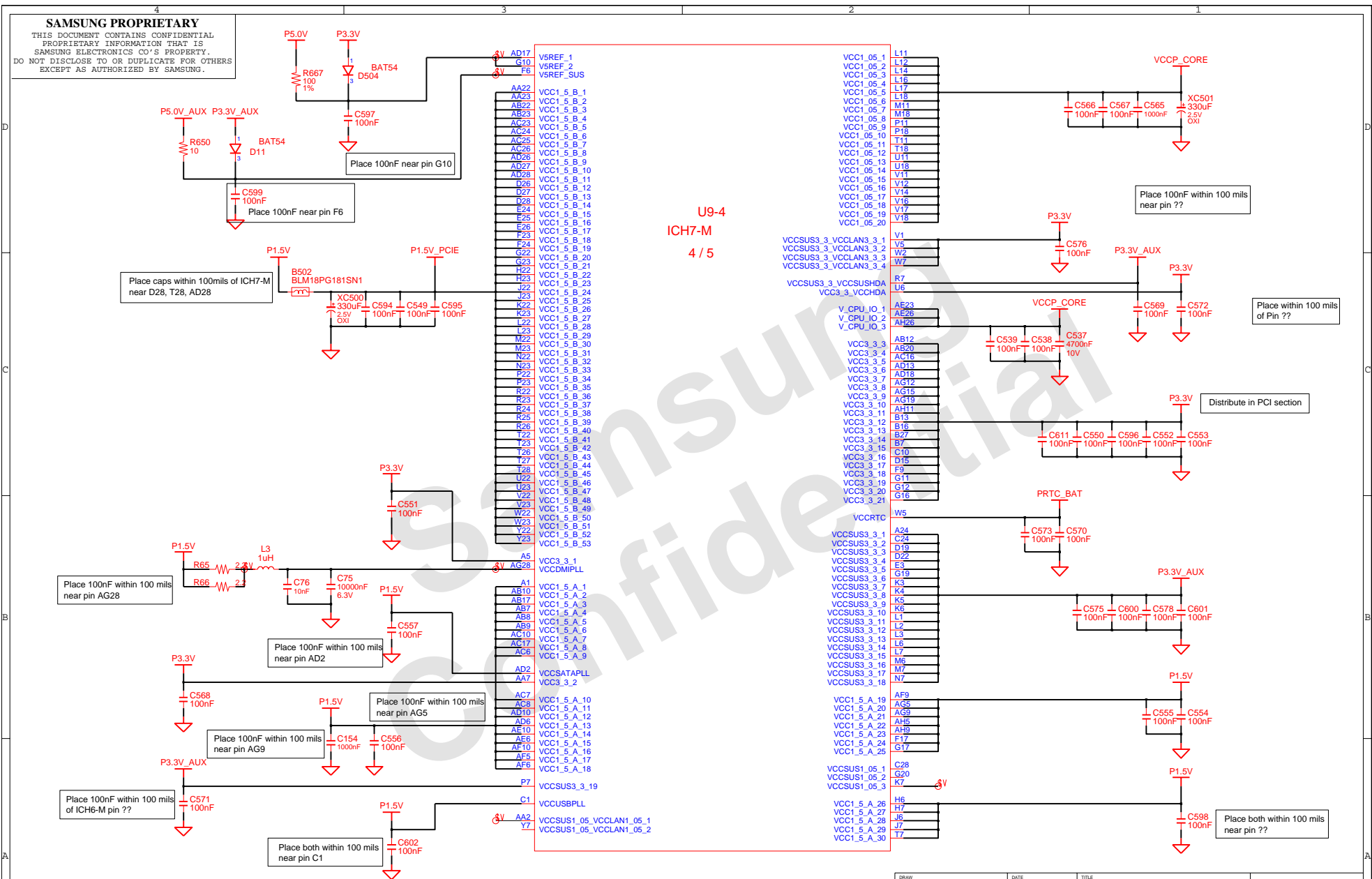
Function	Default
CHP3_SPKR	No Reboot
CHP3_GNT3	A16 swap override
AC97_SDOUT	Safe Mode
CHP3_GNT(5:4)	Boot BIOS Option

DRAW	ZHANG, ELLEN	DATE	3/15/2007	TITLE		
CHECK	ZHENG, ROKY	DEV. STEP	SR	SHANGHAI		SAMSUNG ELECTRONICS
APPROVAL	LEE, KEVIN	REV	1.0	ICH7(2/4)		
MODULE CODE	undefined	LAST EDIT	March 15, 2007 10:33:33 AM	PAGE	25	OF 54

PART NO. BA41-00774A/00732A

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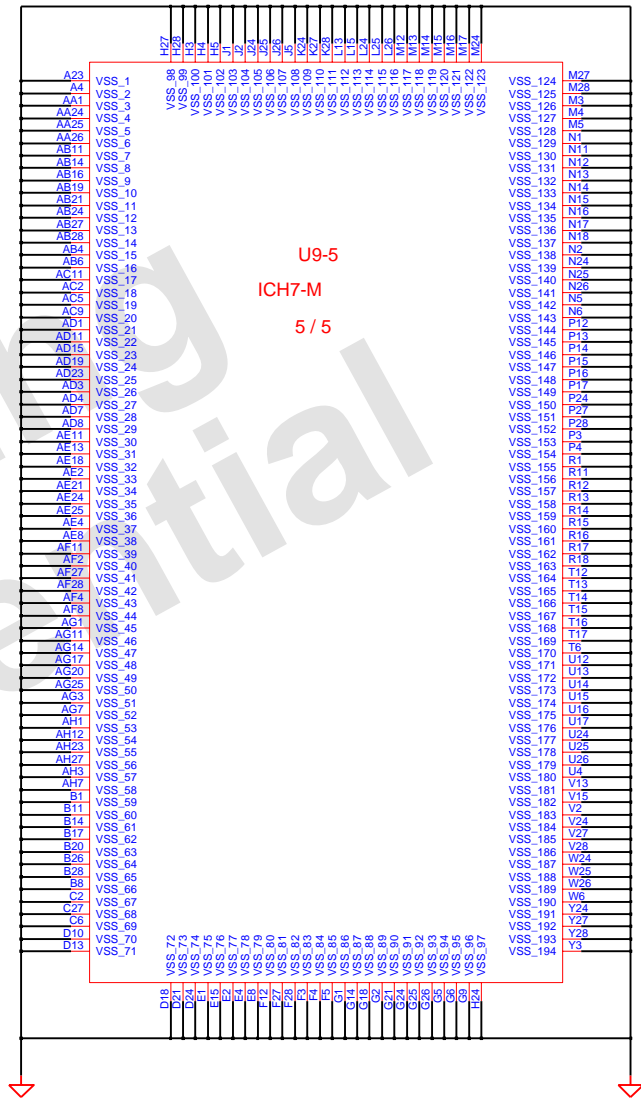
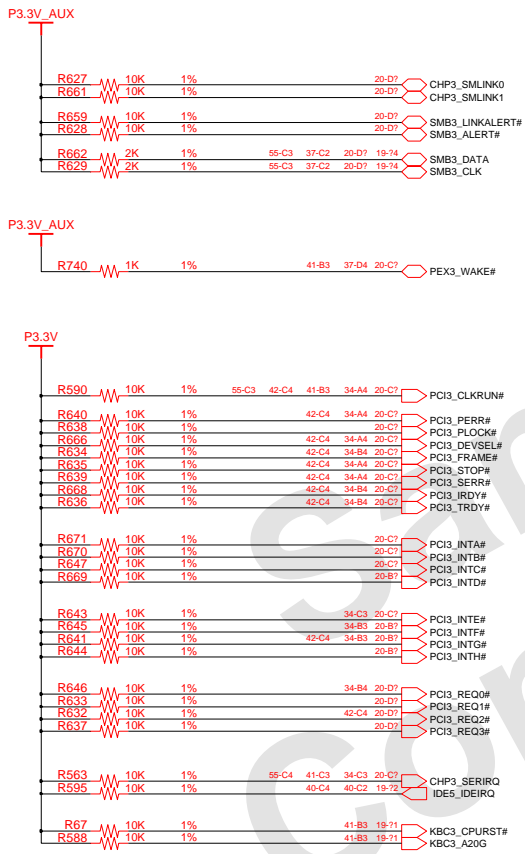
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DRAW	ZHANG, ELLEN	DATE	3/15/2007	TITLE	
CHECK	ZHENG, ROKY	DEV. STEP	SR	SHANGHAI	
APPROVAL	LEE, KEVIN	REV	1.0	ICH7(3/4)	
MODULE CODE	undefined	LAST EDIT	March 15, 2007 10:33:33 AM	PAGE	26 OF 54

SAMSUNG
ELECTRONICS
PART NO.
BA41-00774A/00732A

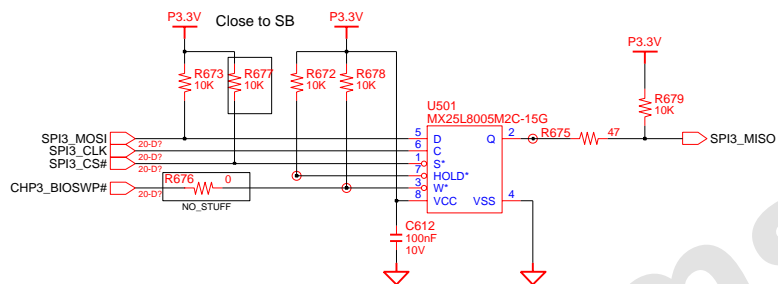
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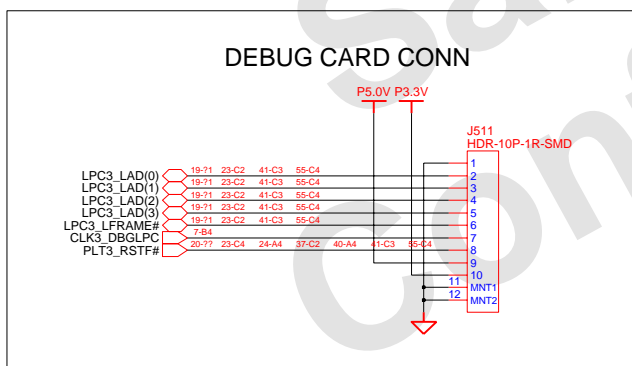
DRAW	ZHANG, ELLEN	DATE	3/15/2007	TITLE	SHANGHAI ICH7(4/4)	SAMSUNG ELECTRONICS
CHECK	ZHENG, ROKY	DEV. STEP	SR			
APPROVAL	LEE, KEVIN	REV	1.0			PART NO. BA41-00774A/00732A
MODULE CODE	undefined	LAST EDIT	March 15, 2007 10:33:33 AM	PAGE	27	OF 52

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DEBUG CARD CONN

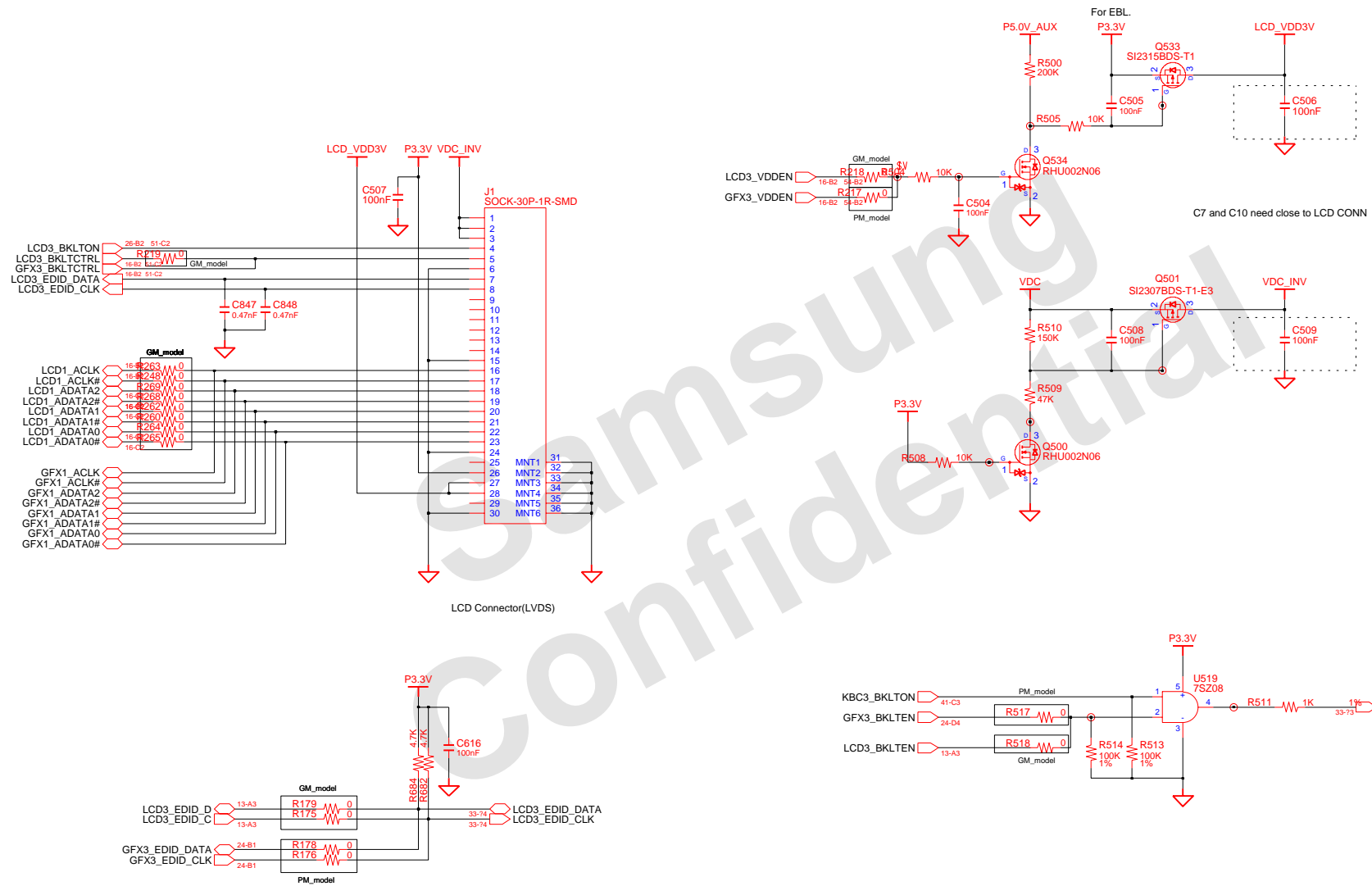


- | | |
|---|------------------------------------|
| 02 VERIFY REAL MODE | 66 CONFIGURE ADVANCE CACHE REG. |
| 03 DISABLE NMI | 6A DISPLAY EXTERNAL CACHE SIZE |
| 04 GET CPU TYPE | 6C DISPLAY SHADOW MESSAGE |
| 06 INIT. SYSTEM H/W | 6E DISPLAY NON-DISPOSABLE SEGMENT |
| 08 INIT. CHIPSET REG. | 70 DISPLAY ERROR MESSAGE |
| 09 SET IN POST FLAG | 72 CHECK FOR CONFIGURATION ERROR |
| 0A INIT CPU.REG | 74 TEST REAL-TIME CLOCK |
| 0B CPU CACHE ON | 76 CHECK FOR KEYBOARD ERROR |
| 0C INIT.CACHE TO POST | 7C SETUP HARDWARE INTERRUPT VECTOR |
| 0E INIT. I/O VALUE | 7E TEST COPROCESSER IF PRESENT |
| 0F ENABLE THE L-BUS IDE | 80 DISABLE ON-BOARD I/O PORT |
| 10 INIT. POWER MANAGER | 82 DETECT AND INSTALL EXT.RS232C |
| 11 LOAD ALTERNATE REG. | 84 DETECT AND INSTALL EXT.PARALLEL |
| 13 PCI BUS MASTER RESET WITH INITIAL POST VALUE | 86 RE-INIT. ON-BOARD I/O PORT |
| 14 INIT. KEYBOARD CONTROLLER | 88 INIT. BIOS DATA ROM |
| 16 CHECK CHECKSUM | 8A INIT.EXTENDED BIOS DATA AREA |
| 18 8254 TIMER INIT. | 8C INIT. FDD CONTROLLER |
| 1A 8237 DMA CONTROLLER INIT. | 9A SHADOW OPTION ROMS |
| 1C RESET INTERRUPT CONTROLLER | 9C SETUP POWER MANAGEMENT |
| 20 TEST DRAM REFRESH | 9E ENABLE H/W INTERRUPT |
| 22 TEST 8742 KEYBOARD CONTROLLER | A0 SET TIME OF DAY |
| 24 SET ES SEGMENT REG. TO 4GB | A4 INIT. TYPOMATIC RATE |
| 26 ENABLE A20 | A8 ERASE F2 PROMPT |
| 28 AUTO SIZING DRAM | AA SCAN FOR F2 KEY STROKE |
| 32 COMPUTE THE CPU SPEED | AC ENTER SETUP |
| 34 TESET CMOS RAM | AE CLEAR IN POST FLAG |
| 38 SHADOW SYSTEM BIOS ROM | B0 CHECK FOR ERRORS |
| 3A AUTO SIZING CACHE | B2 POST DONE-PREPARE TO BOOT O/S |
| 3C CONFIGURE ADVANCED CHIPSET REG. | B4 ONE BEEP |
| 3D LOAD ALTER REG. WITH CMOS VALUE | B6 CHECK PASSWORD (OPTION) |
| 42 INIT. INTERRUPT VECTOR | B7 ACPI INIT |
| 44 INIT. BIOS INTERRUPT | BA DMI INIT |
| 46 CHECK ROM COPYRIGHT NOTICE | BE CLEAR SCREEN |
| 47 INIT. I20 SUPPORT IF INSTALLED | C0 TRY BOOT WITH INT19 |
| 48 CHECK VIDEO CONFIGURE AGAINST CMOS | D0 INTERRUPT HANDLER ERROR |
| 49 INIT. PCI BUS AND DEVICE | D2 UNKNOWN INTERRUPT ERROR |
| 4A INIT. ALL VIDEO BIOS ROM | D4 PENDING INTERRUPT ERROR |
| 4C SHADOW VIDEO BIOS ROM | D6 SHUTDOWN 5 |
| 50 DISPLAY CPU TYPE AND SPEED | D8 SHUTDOWN ERROR |
| 52 TEST KEYBOARD | DA EXTENDED BLOCK MOVE |
| 54 SET KEYCLICK IF ENABLED | DC SHUTDOWN 10 |
| 56 ENABLE KEYBOARD | 89 ENABLE NMI |
| 58 TEST FOR UNEXPECTED INTERRUPTS | 90 INIT. HDD CONTROLLER |
| 5A DISPLAY " PRESS SETUP" | 91 INIT. LOCAL BUS HDD CONTROLLER |
| 5C TEST RAM BETWEEN 512K AND 640K | 92 JUMP TO USER PATCH 2 |
| 60 TEST EXTENDED MEMORY | 94 DISABLE A20 ADDRESS LINE |
| 62 TEST EXTENDED MEMORY ADDRESS LINE | 96 CLEAR HUGE ES SEGMENT REG. |
| 64 JUMP TO USER PATCH 1 | 98 SEARCH FOR OPTION ROMS |

DRAW	ZHANG, ELLEN	DATE	3/15/2007	TITLE	SHANGHAI	SAMSUNG ELECTRONICS
CHECK	ZHENG, ROKY	DEV. STEP	SR	FWH		
APPROVAL	LEE, KEVIN	REV	1.0			PART NO. BA41-00774A/00732A
MODULE CODE	undefined	LAST EDIT	March 15, 2007 10:33:33 AM	PAGE	28	OF 54

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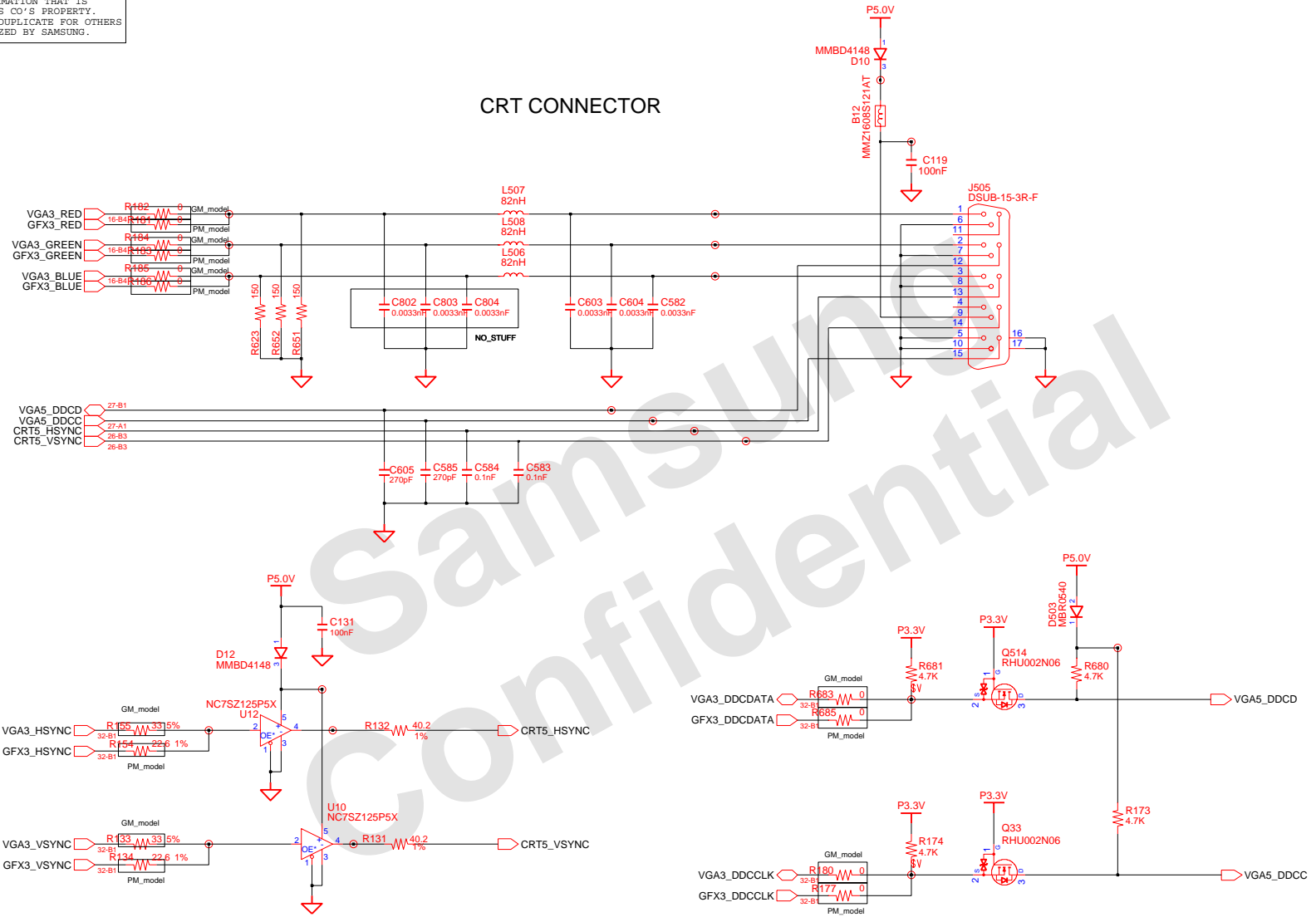


DRAW	ZHANG, ELLEN	DATE	3/15/2007	TITLE	SHANGHAI LCD	SAMSUNG ELECTRONICS
CHECK	ZHENG, ROKY	DEV. STEP	SR			
APPROVAL	LEE, KEVIN	REV	1.0		PART NO.	BA41-00774A/00732A
MODULE CODE	undefined	LAST EDIT	March 15, 2007 10:33:33 AM	PAGE	29	OF 54

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CRT CONNECTOR

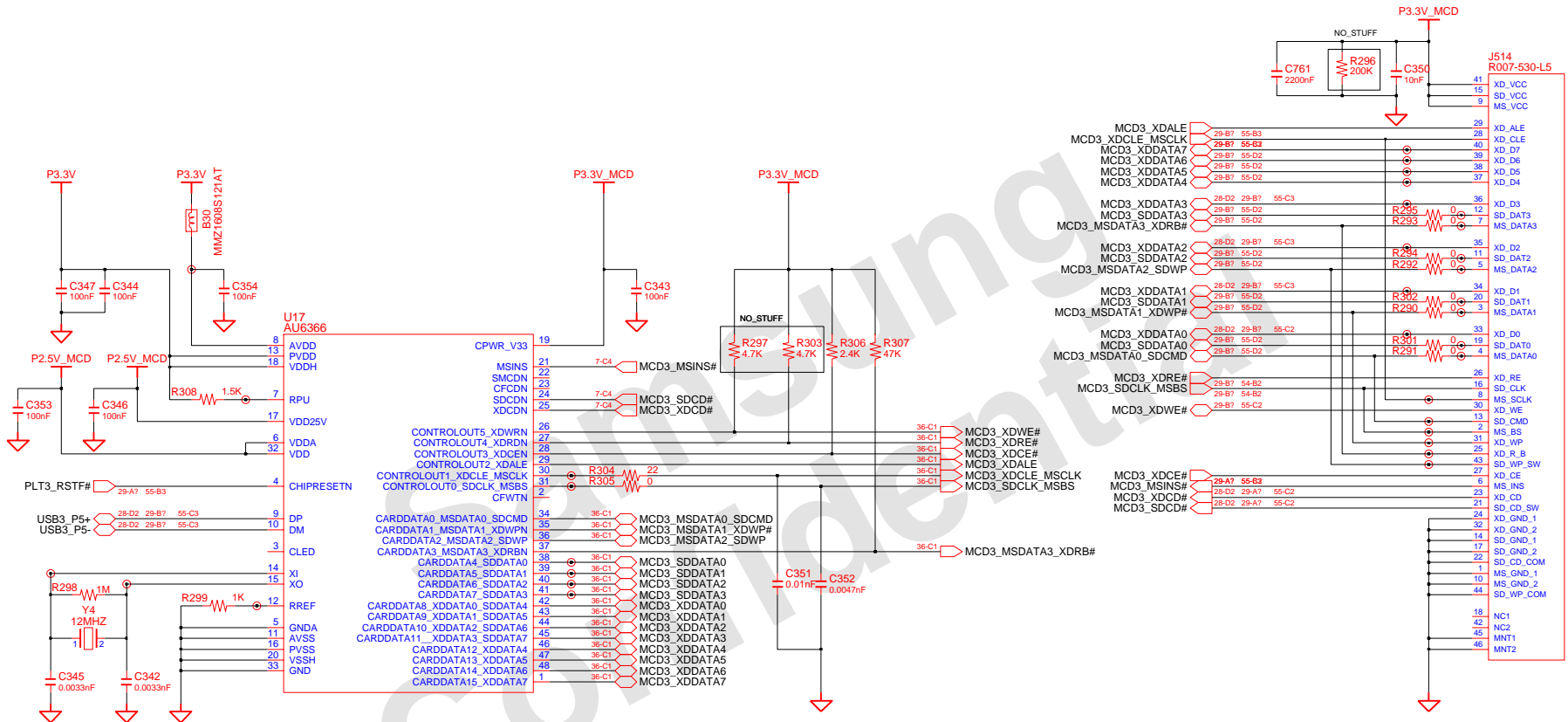


DRAW	ZHANG, ELLEN	DATE	3/15/2007	TITLE	SHANGHAI CRT	SAMSUNG ELECTRONICS PART NO. BA41-00774A/00732A
CHECK	ZHENG, ROKY	DEV. STEP	SR			
APPROVAL	LEE, KEVIN	REV	1.0			
MODULE CODE	undefined	LAST EDIT	March 15, 2007 10:33:33 AM	PAGE 30 OF 54		

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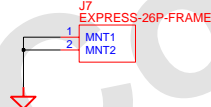
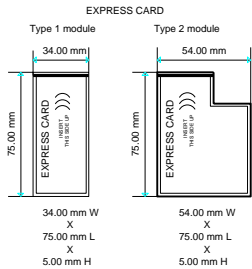
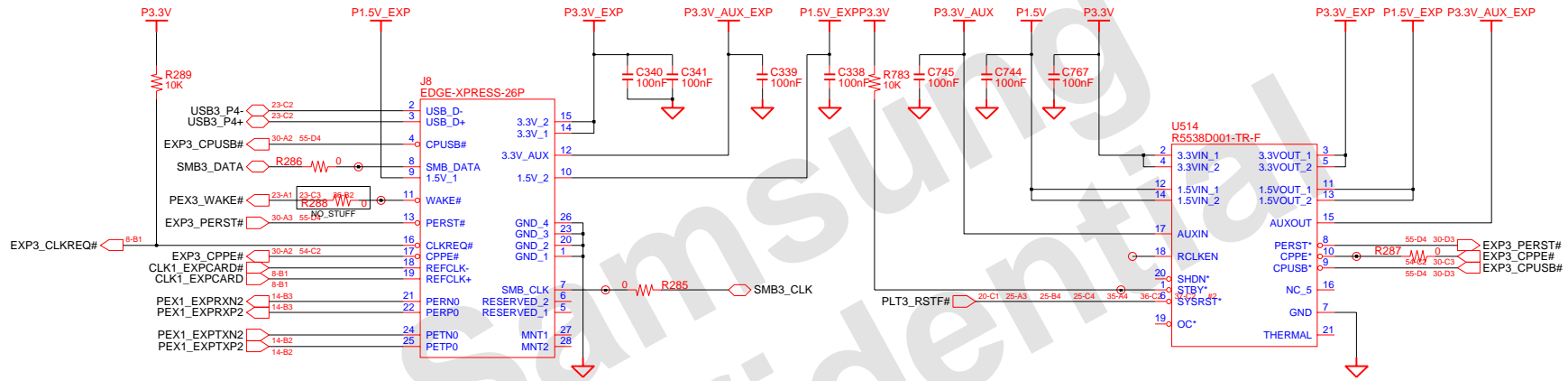
4 IN 1 CARD



DRAW	ZHANG, ELLEN	DATE	3/15/2007	TITLE	SHANGHAI 4 IN 1 CARD	SAMSUNG ELECTRONICS	
CHECK	ZHENG, ROKY	DEV. STEP	SR				
APPROVAL	LEE, KEVIN	REV	1.0				
MODULE CODE	undefined	LAST EDIT	March 15, 2007 10:33:33 AM	PAGE			31 OF 54
							PART NO.

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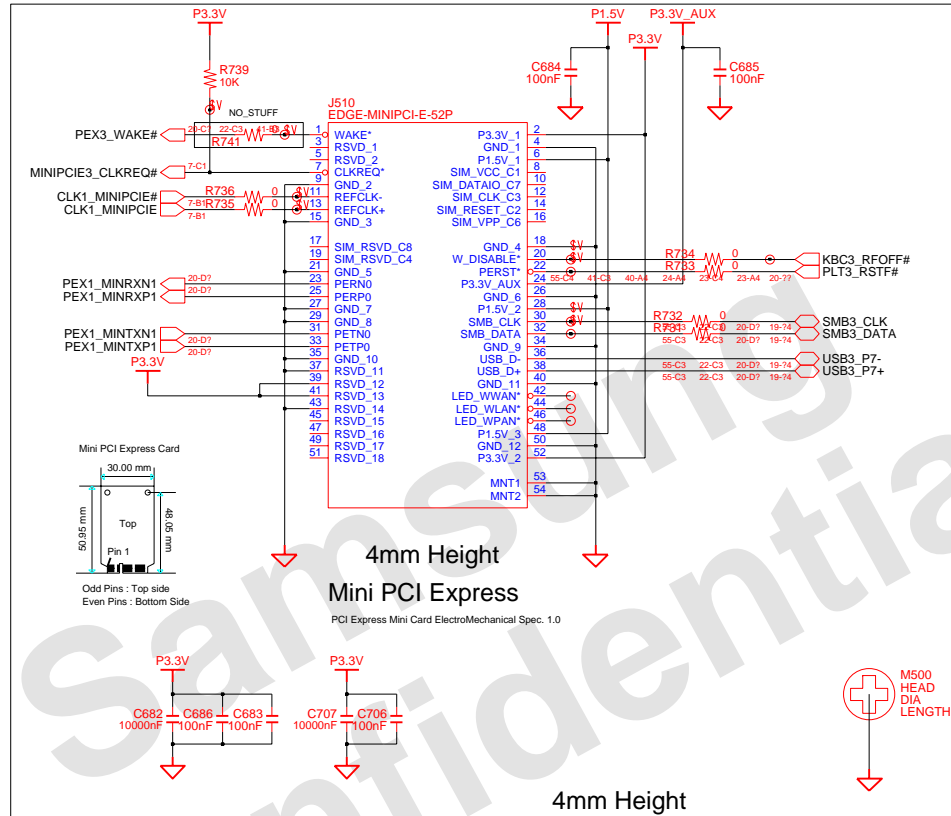
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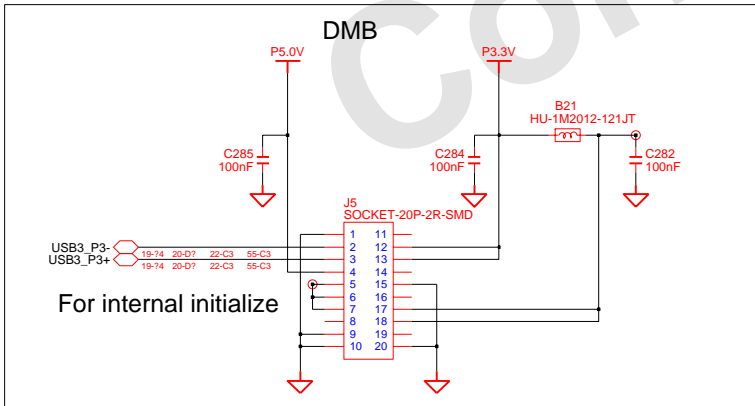
DRAW	ZHANG, ELLEN	DATE	3/15/2007	TITLE	SHANGHAI EXPRESS CARD	SAMSUNG ELECTRONICS
CHECK	ZHENG, ROKY	DEV. STEP	SR			
APPROVAL	LEE, KEVIN	REV	1.0		PART NO.	BA41-00774A/00732A
MODULE CODE	undefined	LAST EDIT	March 15, 2007 10:33:33 AM	PAGE	32	OF 54

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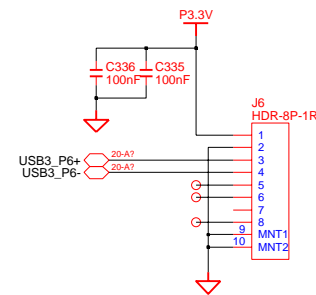
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factory option



Bluetooth Interface



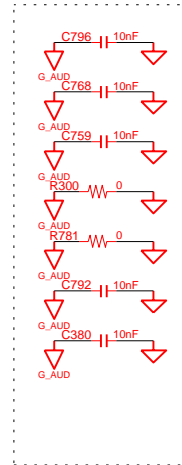
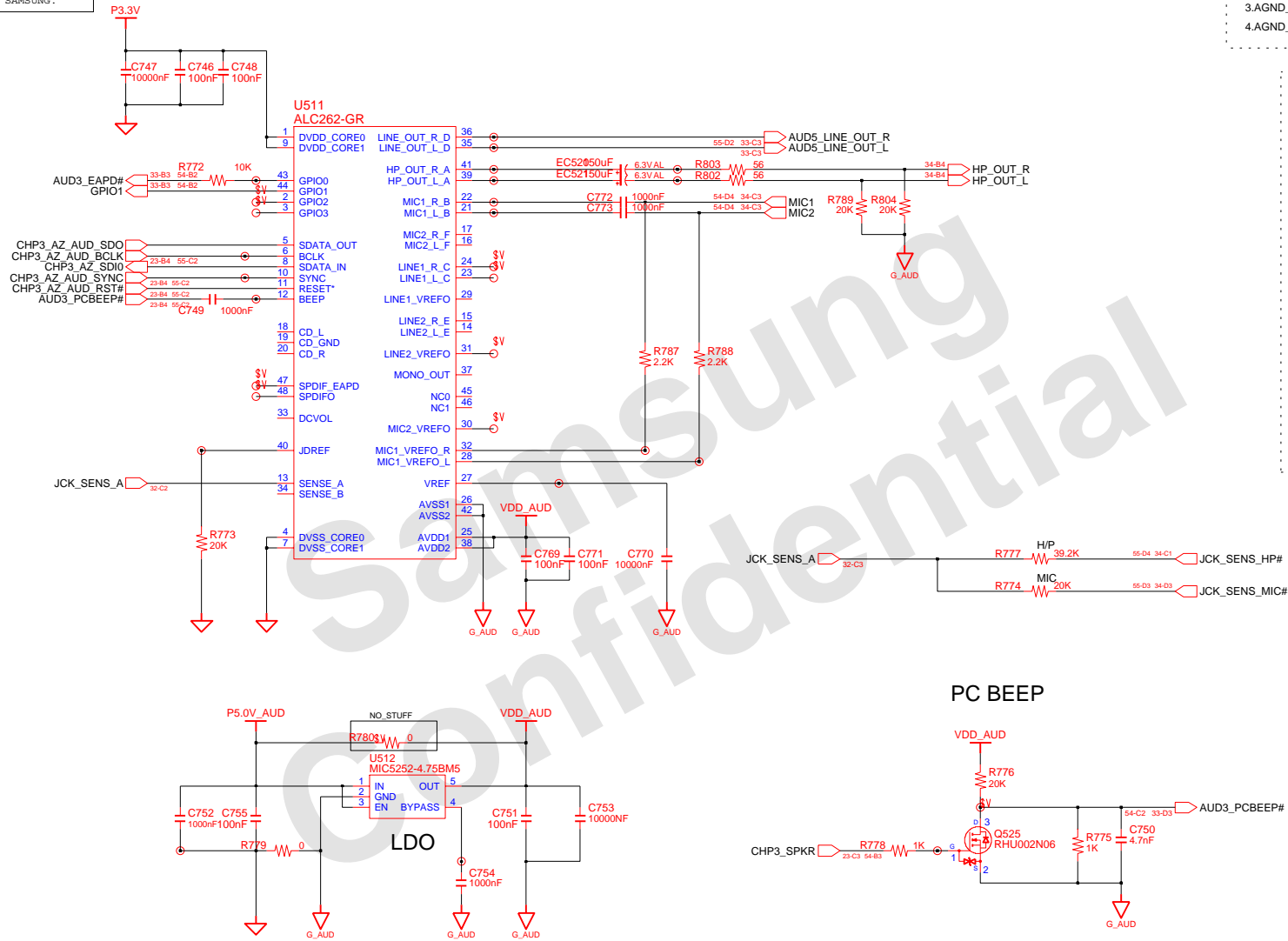
DRAW	ZHANG, ELLEN	DATE	3/15/2007	TITLE	SHANGHAI MINI CARD	SAMSUNG ELECTRONICS	
CHECK	ZHENG, ROKY	DEV. STEP	SR				
APPROVAL	LEE, KEVIN	REV	1.0				
MODULE CODE	undefined	LAST EDIT	March 15, 2007 10:33:33 AM	PAGE			33 OF 54
							PART NO.

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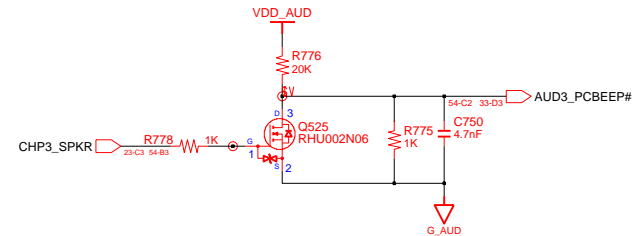
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- 1.AGND_AUD IS AUDIO GROUND
- 2. GND IS DIGITAL GROUND
- 3.AGND_MIC IS MIC GROUND
- 4.AGND_CHS IS CHASSIS GROUND

ALL TYPE IS 1608



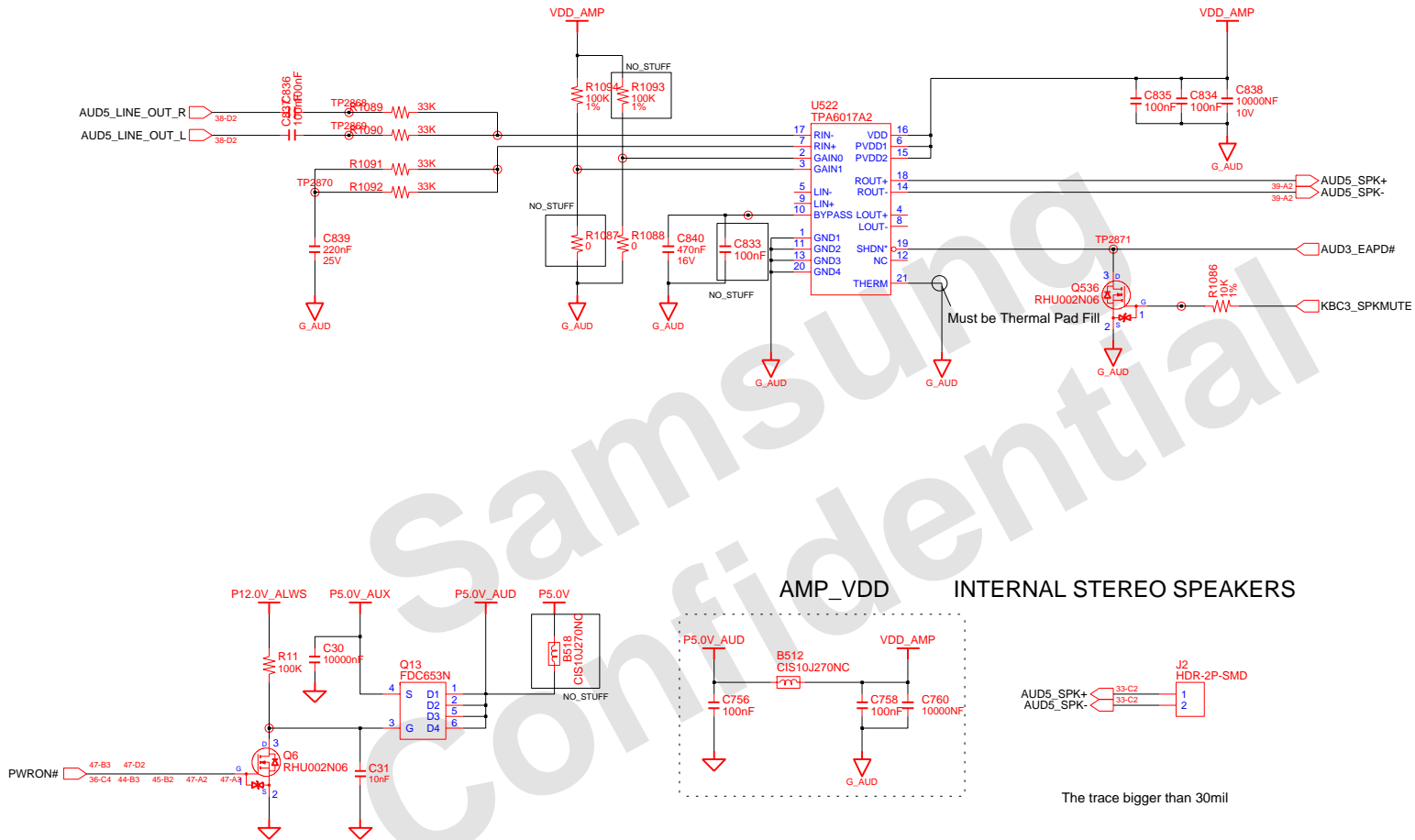
PC BEEP



DRAW	ZHANG, ELLEN	DATE	3/15/2007	TITLE	SHANGHAI AUDIO(1/3)	SAMSUNG ELECTRONICS	
CHECK	ZHENG, ROKY	DEV. STEP	SR				
APPROVAL	LEE, KEVIN	REV	1.0				
MODULE CODE	undefined	LAST EDIT	March 15, 2007 10:33:33 AM	PAGE			34 OF 54
							PART NO.

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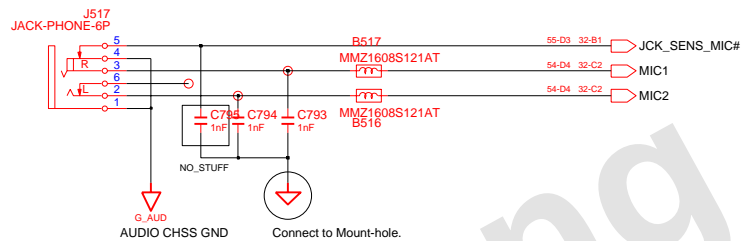


DRAW	ZHANG, ELLEN	DATE	3/15/2007	TITLE	SHANGHAI AUDIO(2/3)	SAMSUNG ELECTRONICS PART NO. BA41-00774A/00732A
CHECK	ZHENG, ROKY	DEV. STEP	SR			
APPROVAL	LEE, KEVIN	REV	1.0			
MODULE CODE	undefined	LAST EDIT	March 15, 2007 10:33:33 AM	PAGE 35 OF 54		

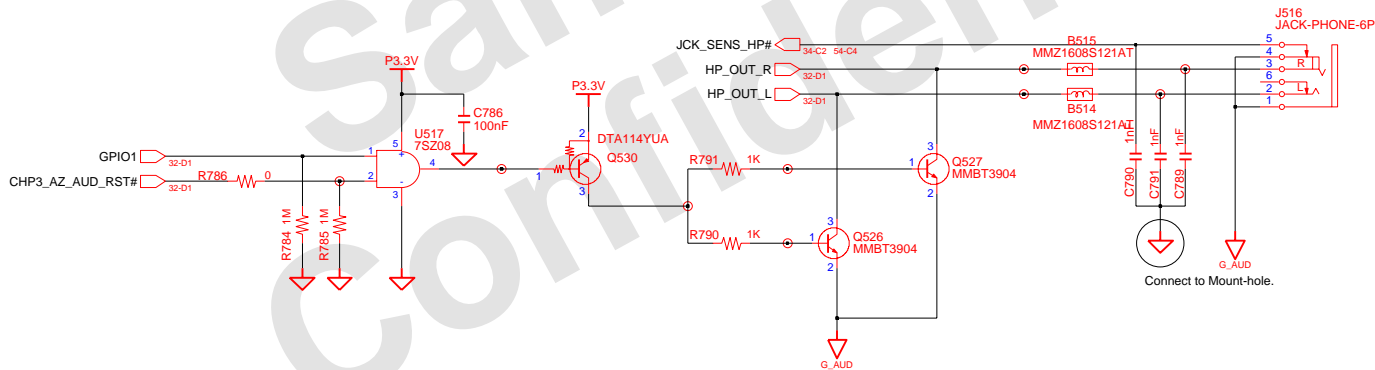
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MIC JACK



HEADPHONE



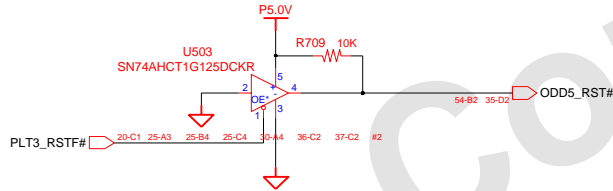
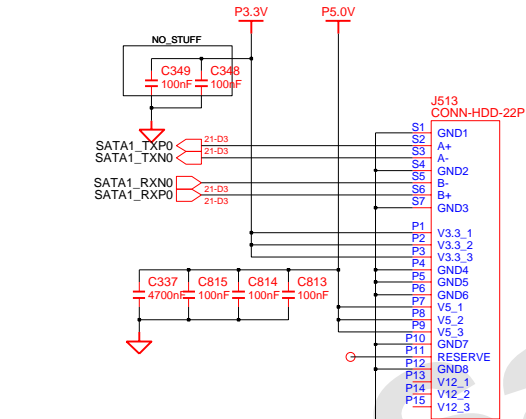
The traces led to Audio Jacks have the width over 10mil

DRAW	ZHANG, ELLEN	DATE	3/15/2007	TITLE	SHANGHAI AUDIO(3/3)	SAMSUNG ELECTRONICS
CHECK	ZHENG, ROKY	DEV. STEP	SR			
APPROVAL	LEE, KEVIN	REV	1.0			
MODULE CODE	undefined	LAST EDIT	March 15, 2007 10:33:33 AM	PAGE 36 OF 54		

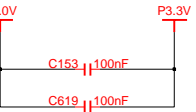
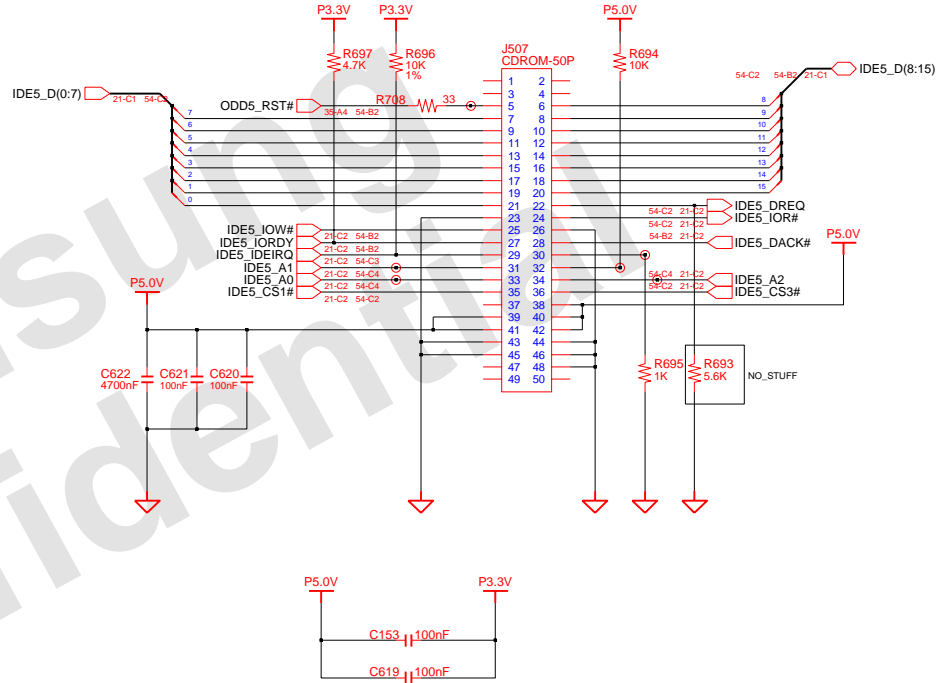
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Main to HDD



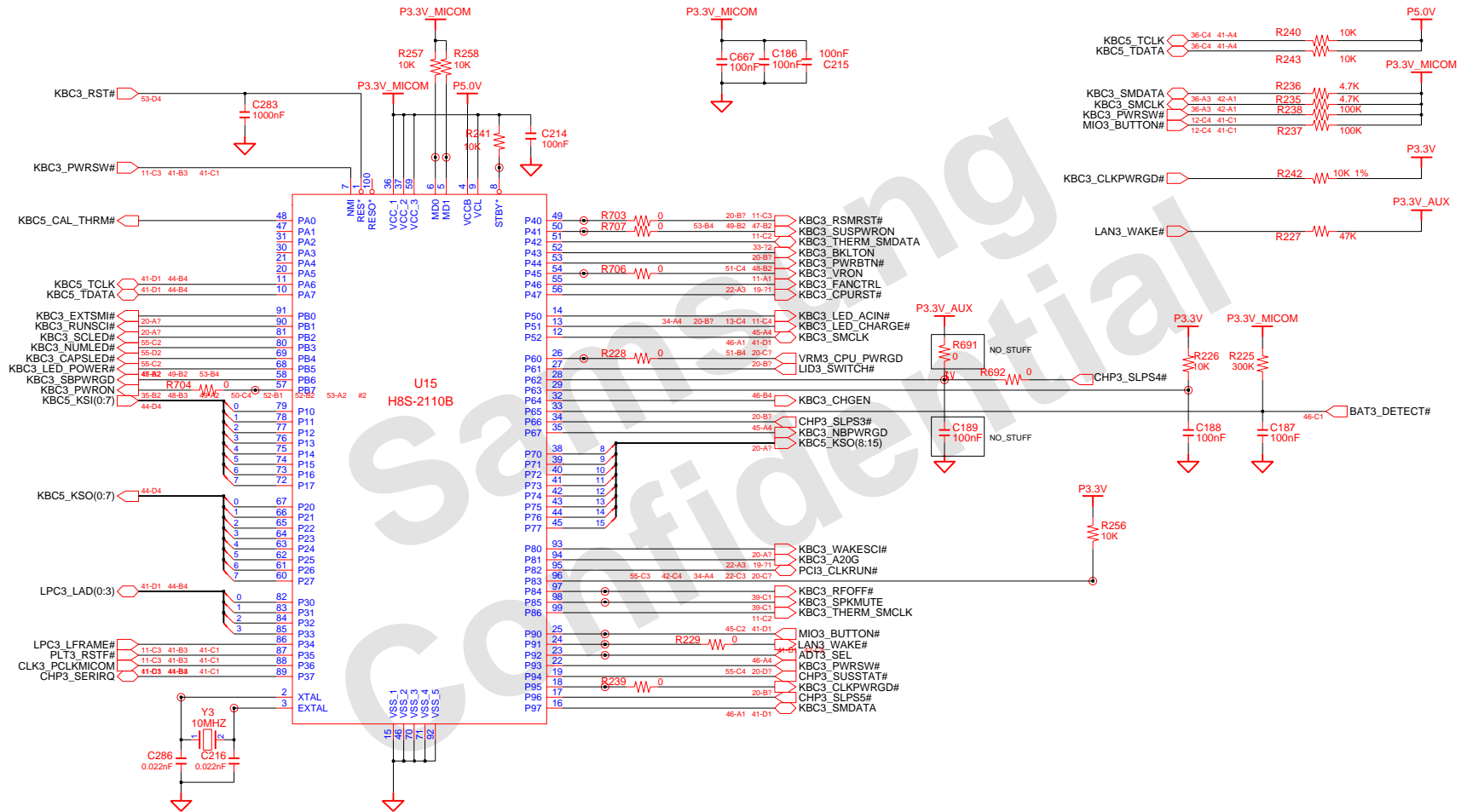
Main to ODD



DRAW	ZHANG, ELLEN	DATE	3/15/2007	TITLE	SHANGHAI HDD & ODD	SAMSUNG ELECTRONICS PART NO. BA41-00774A/00732A
CHECK	ZHENG, ROKY	DEV. STEP	SR			
APPROVAL	LEE, KEVIN	REV	1.0			
MODULE CODE	undefined	LAST EDIT	March 15, 2007 10:33:33 AM	PAGE 37 OF 54		

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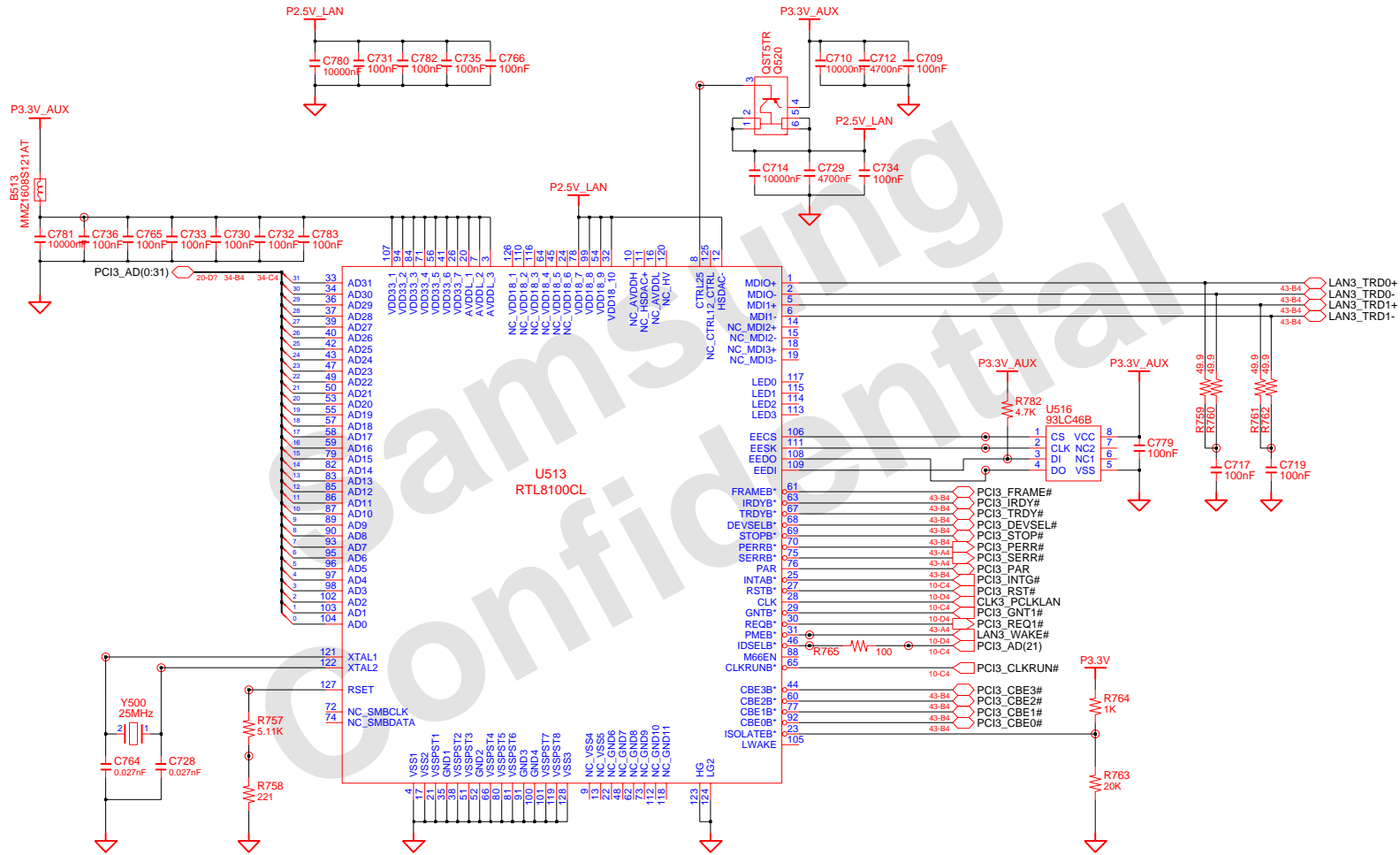
TP FOR UPDATE MICOM:
 P84=>TXD;P85=>RXD
 MD0 and MD1 =>GND
 P90,P91,P92=>VCC

DRAW	ZHANG, ELLEN	DATE	3/15/2007	TITLE	SAMSUNG ELECTRONICS SHANGHAI MICOM PART NO. BA41-00774A/00732A	
CHECK	ZHENG, ROKY	DEV. STEP	SR			
APPROVAL	LEE, KEVIN	REV	1.0			
MODULE CODE	undefined	LAST EDIT	March 15, 2007 10:33:33 AM	PAGE		38 OF 54

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LAN Controller (Only 10/100M)

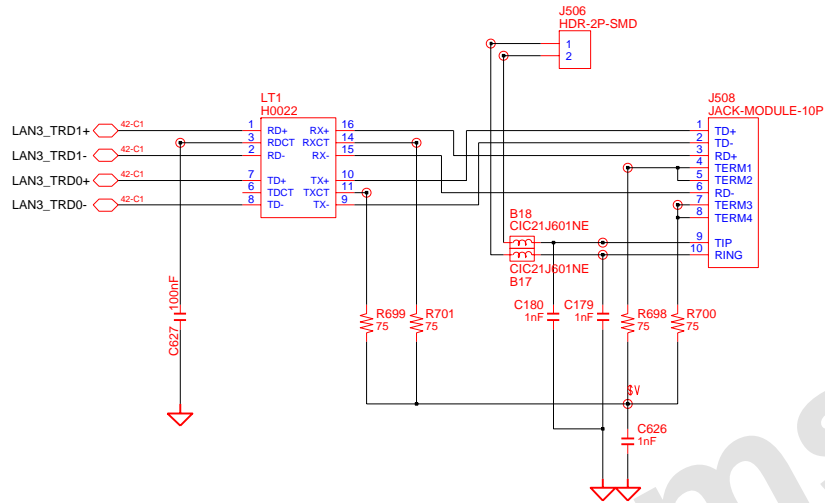


DRAW	ZHANG, ELLEN	DATE	3/15/2007	TITLE	SHANGHAI LAN	SAMSUNG ELECTRONICS
CHECK	ZHENG, ROKY	DEV. STEP	SR			
APPROVAL	LEE, KEVIN	REV	1.0			PART NO. BA41-00774A/00732A
MODULE CODE	undefined	LAST EDIT	March 15, 2007 10:33:33 AM	PAGE	39	OF 54

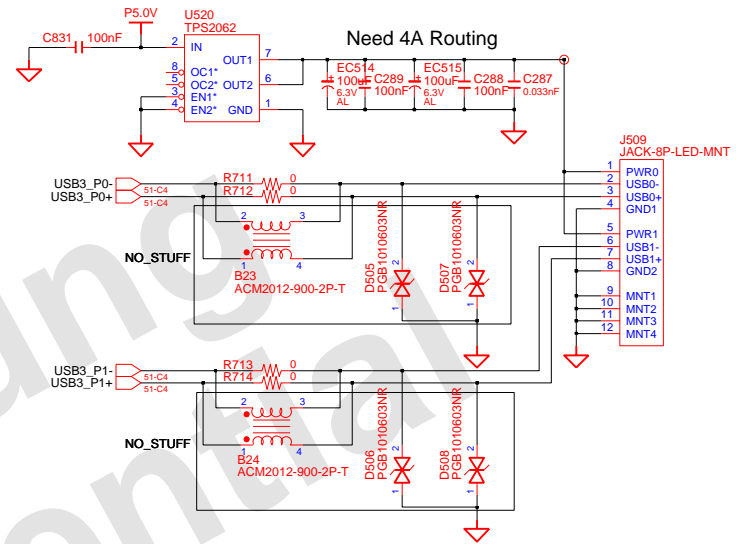
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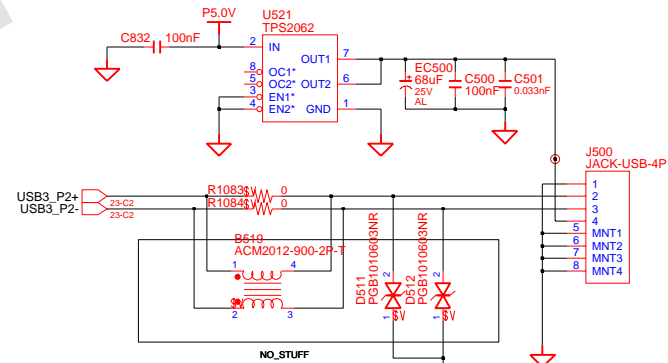
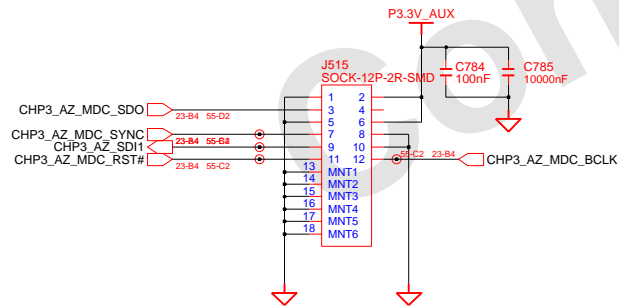
LAN Connector



USB Connector



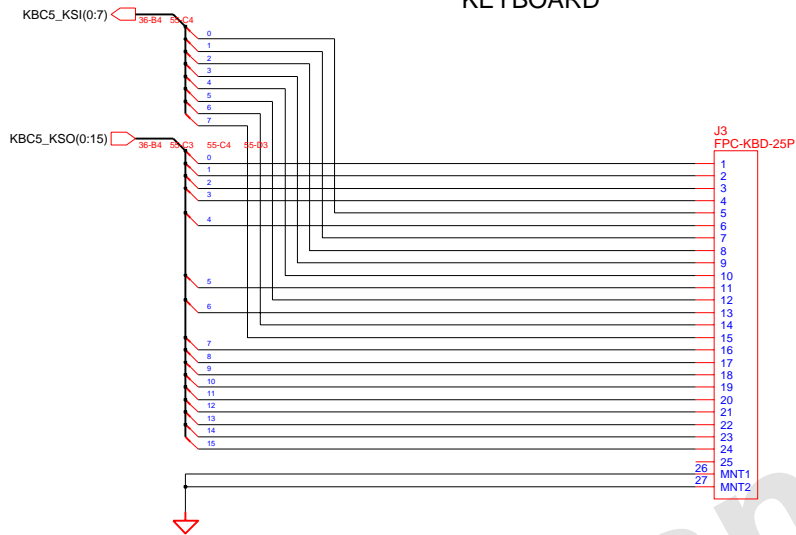
MDC Connector



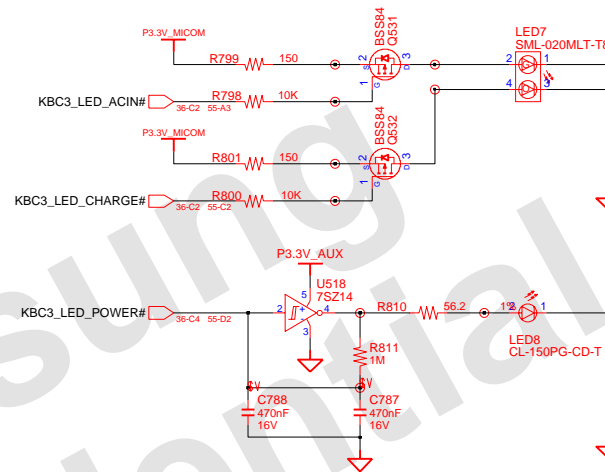
DRAW	ZHANG, ELLEN	DATE	3/15/2007	TITLE	SHANGHAI LAN & MDC CONN	SAMSUNG ELECTRONICS	
CHECK	ZHENG, ROKY	DEV. STEP	SR				
APPROVAL	LEE, KEVIN	REV	1.0				
MODULE CODE	undefined	LAST EDIT	March 15, 2007 10:33:33 AM	PAGE			40 OF 54
				PART NO.			BA41-00774A/00732A

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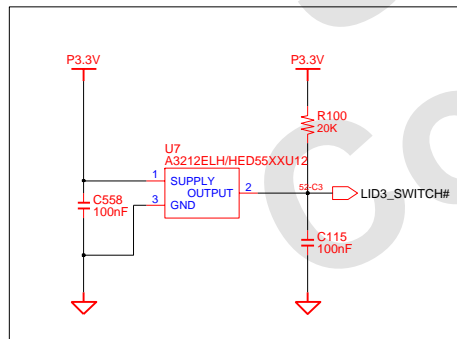
KEYBOARD



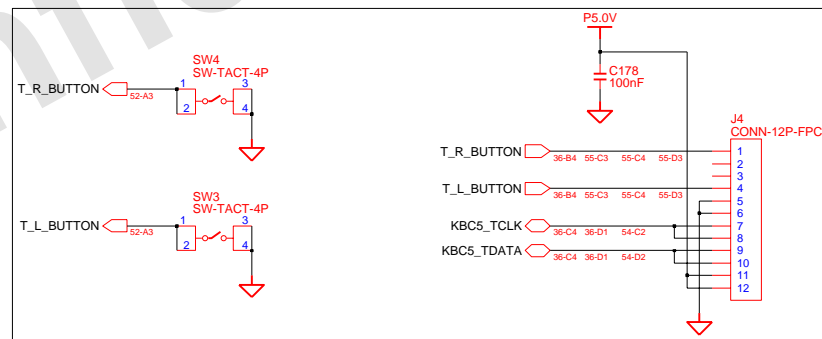
ADAPTERIN/CHARGING LED



LID SWITCH



TOUCHPAD

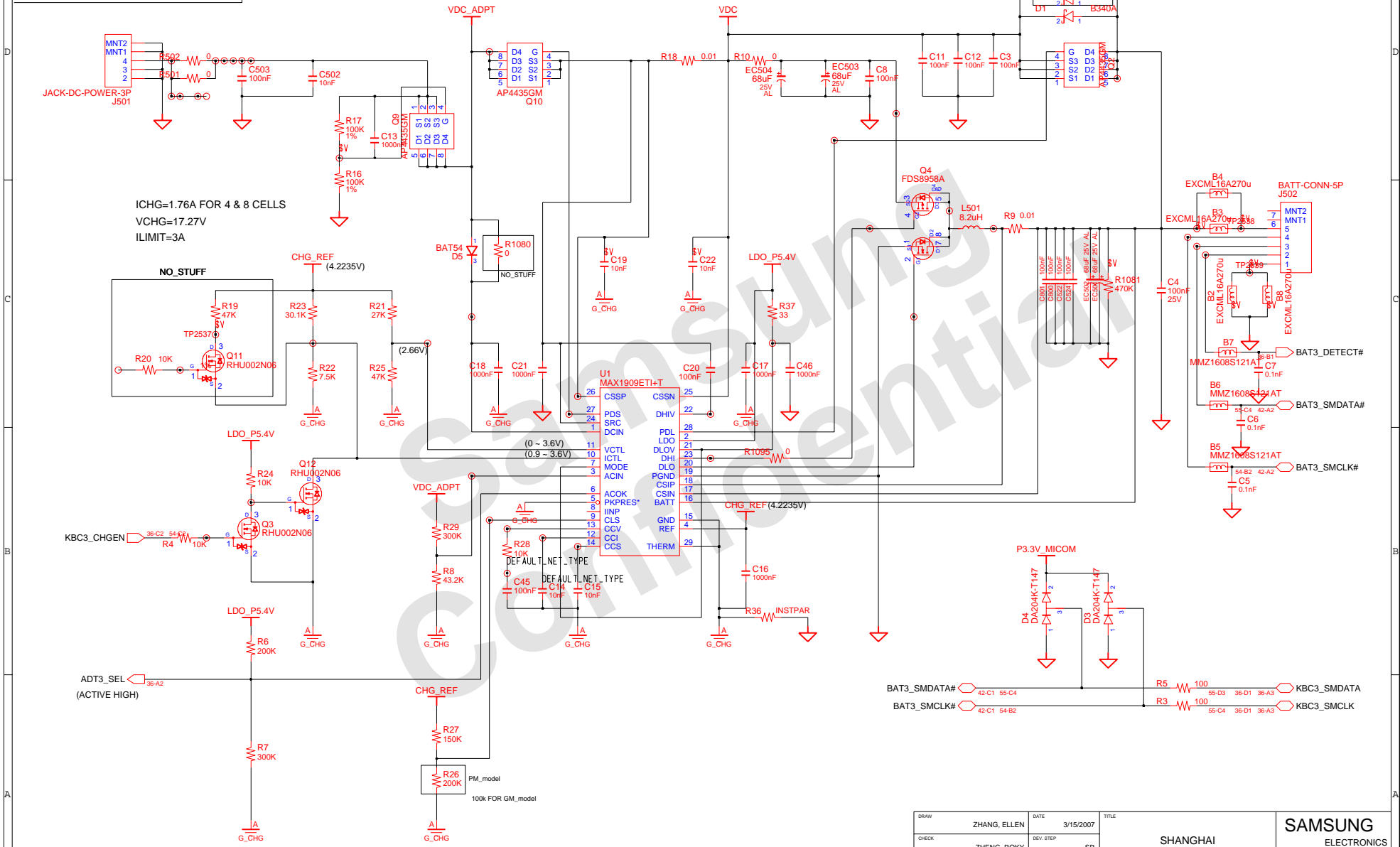


DRAW	ZHANG, ELLEN	DATE	3/15/2007	TITLE	SHANGHAI BOARD CONN	SAMSUNG ELECTRONICS
CHECK	ZHENG, ROKY	DEV. STEP	SR			
APPROVAL	LEE, KEVIN	REV	1.0			
MODULE CODE	undefined	LAST EDIT	March 15, 2007 10:33:33 AM	PAGE 41 OF 54		

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CHARGER & POWER MANAGEMENT

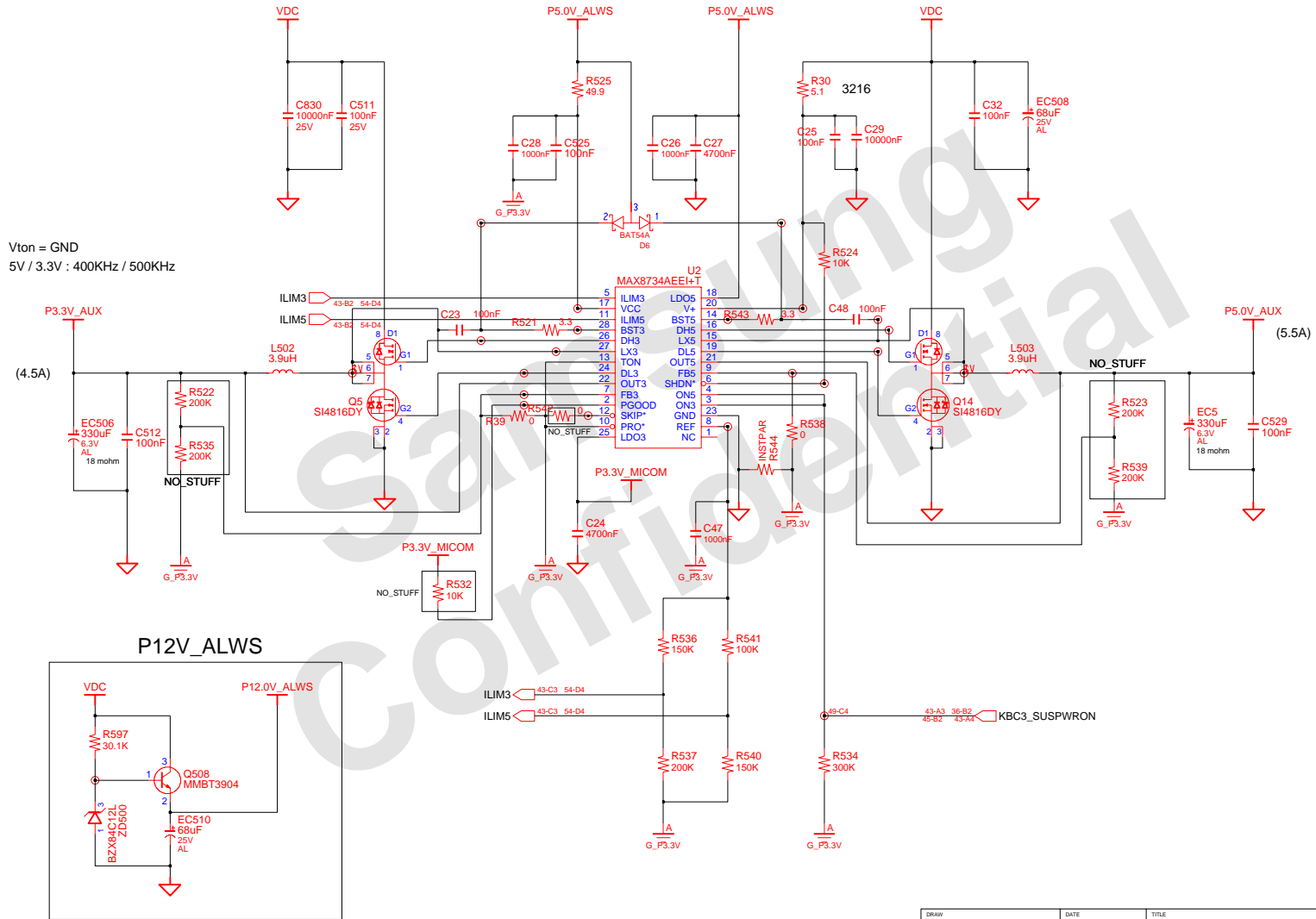


DRAW	ZHANG, ELLEN	DATE	3/15/2007	TITLE	
CHECK	ZHENG, ROKY	DEV. STEP	SR	SHANGHAI CHARGE	SAMSUNG ELECTRONICS
APPROVAL	LEE, KEVIN	REV	1.0		PART NO. BA41-00774A/00732A
MODULE CODE	undefined	LAST EDIT	March 15, 2007 10:33:33 AM	PAGE	42 OF 54

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P3.3V_AUX & P5V_AUX

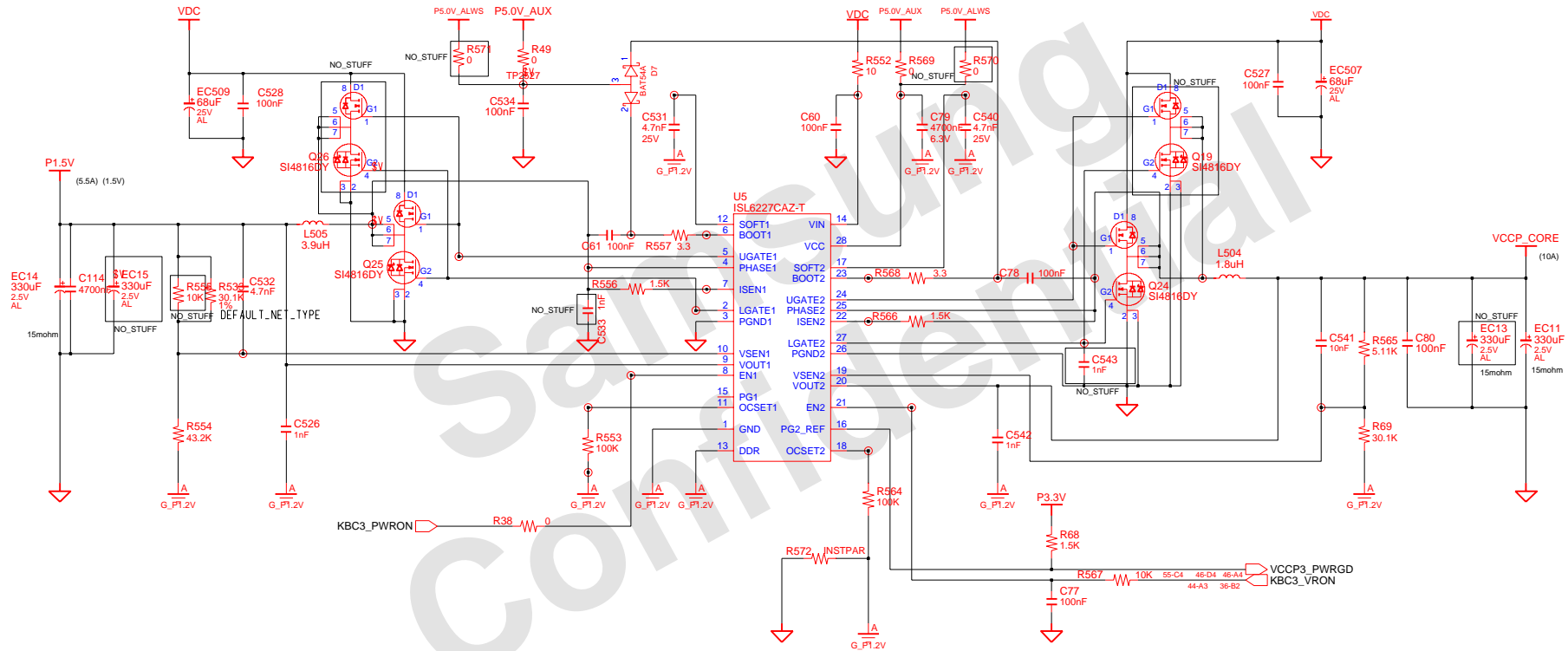


DRAW	ZHANG, ELLEN	DATE	3/15/2007	TITLE	SHANGHAI P3.3V_AUX & P5V_AUX	SAMSUNG ELECTRONICS
CHECK	ZHENG, ROKY	DEV. STEP	SR			
APPROVAL	LEE, KEVIN	REV	1.0			
MODULE CODE	undefined	LAST EDIT	March 15, 2007 10:33:33 AM	PAGE 43 OF 54		

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P1.5V & VCCP_CORE(1.05V)

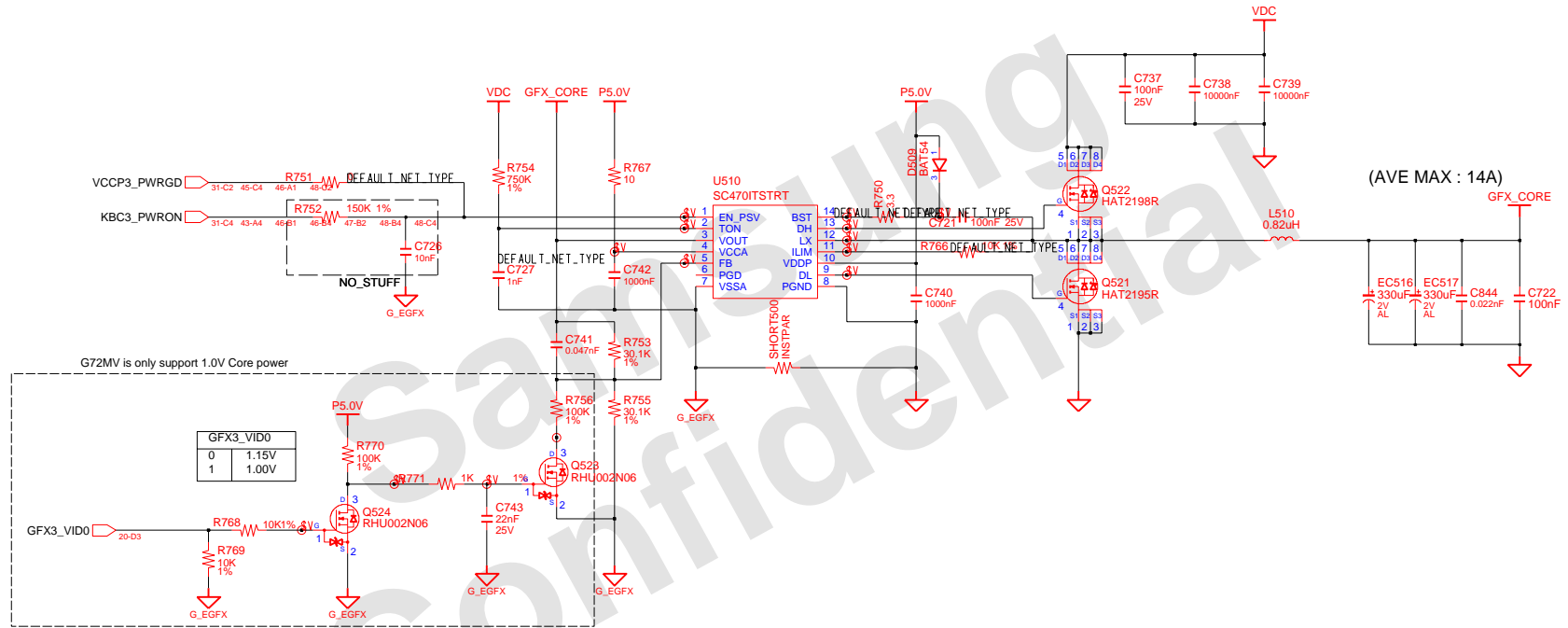


DRAW	ZHANG, ELLEN	DATE	3/15/2007	TITLE	SHANGHAI P1.2V & VCCP		SAMSUNG ELECTRONICS	
CHECK	ZHENG, ROKY	DEV. STEP	SR	PART NO. BA41-00774A/00732A				
APPROVAL	LEE, KEVIN	REV	1.0					
MODULE CODE	undefined	LAST EDIT	March 15, 2007 10:33:33 AM	PAGE	44	OF	54	

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Graphic Core Power

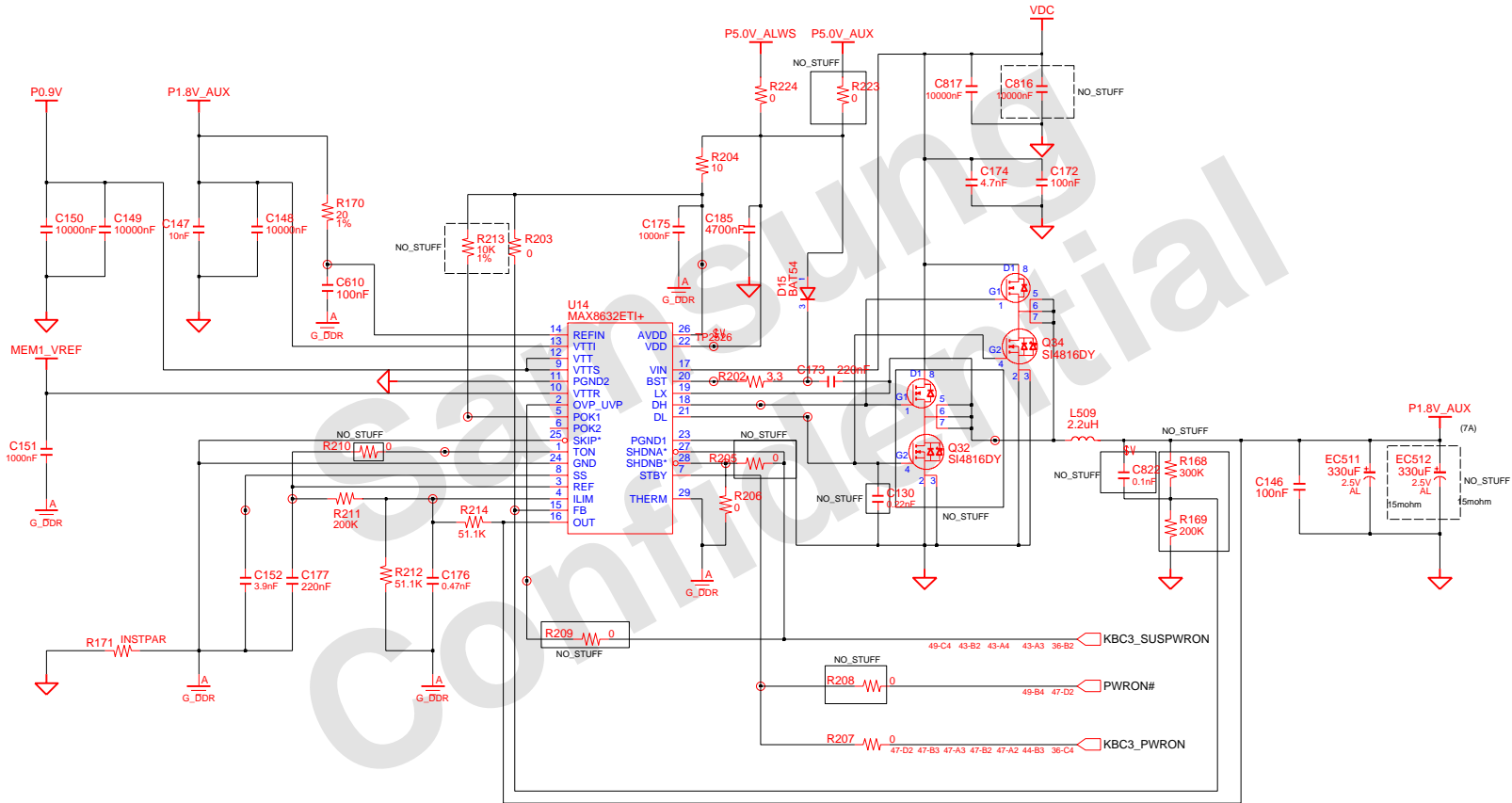


(AVE MAX : 14A)

DRAW	ZHANG, ELLEN	DATE	3/15/2007	TITLE	SHANGHAI GFX_CORE & P1.5V	SAMSUNG ELECTRONICS PART NO. BA41-00774A/00732A
CHECK	ZHENG, ROKY	DEV. STEP	SR			
APPROVAL	LEE, KEVIN	REV	1.0			
MODULE CODE		LAST EDIT				
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DDR2 Power

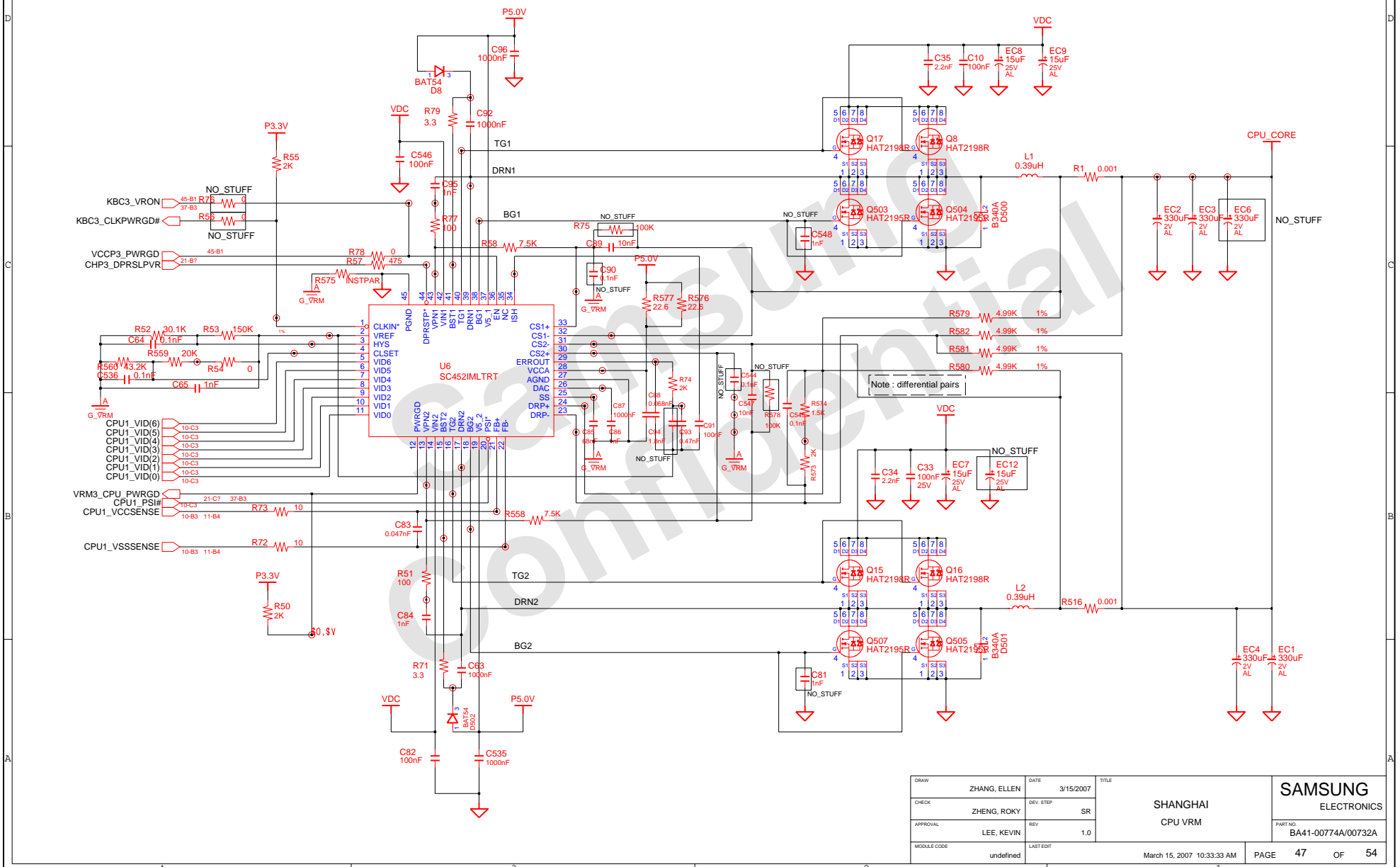


DRAW	ZHANG, ELLEN	DATE	3/15/2007	TITLE	SAMSUNG ELECTRONICS SHANGHAI DDR2 POWER PART NO. BA41-00774A/00732A	
CHECK	ZHENG, ROKY	DEV. STEP	SR			
APPROVAL	LEE, KEVIN	REV	1.0			
MODULE CODE	undefined	LAST EDIT	March 15, 2007 10:33:33 AM	PAGE		46 OF 54

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CPU VRM [SEMTECH]

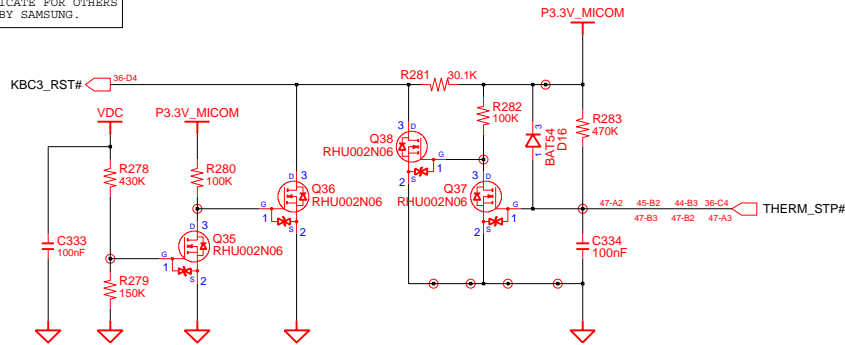


DRAW	ZHANG, ELLEN	DATE	3/15/2007	TITLE	SHANGHAI CPU VRM	SAMSUNG ELECTRONICS	
CHECK	ZHENG, ROKY	DEV. STEP	SR				
APPROVAL	LEE, KEVIN	REV	1.0				
MODULE CODE	undefined	LAST EDIT	March 15, 2007 10:33:33 AM	PAGE			47 OF 54
						PART NO. BA41-00774A/00732A	

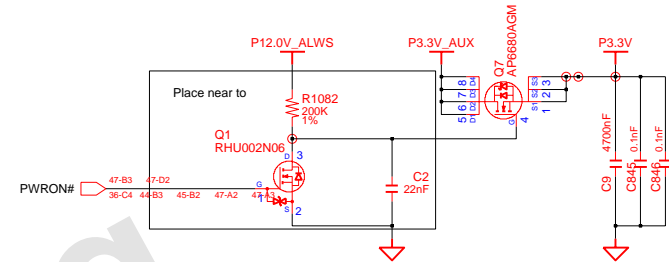
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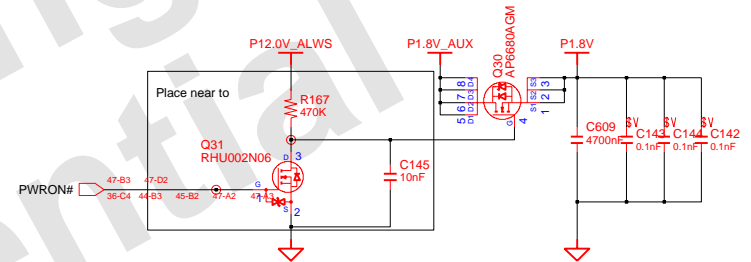
MICOM RESET



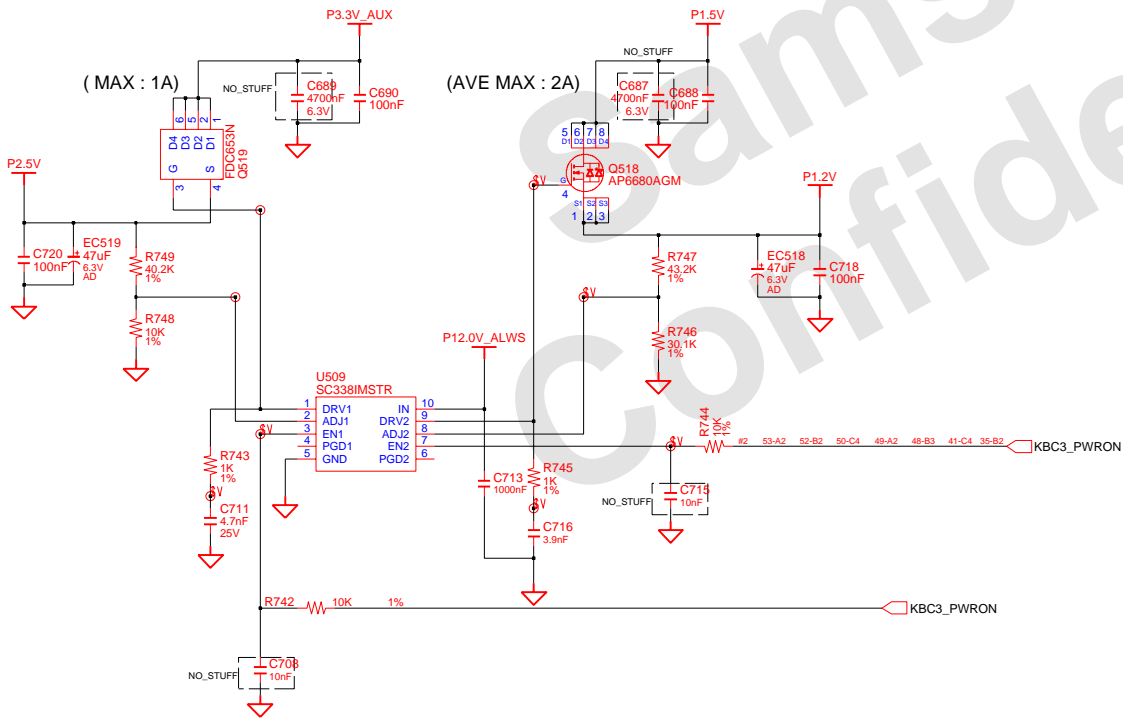
Switched Power On (P3.3V)



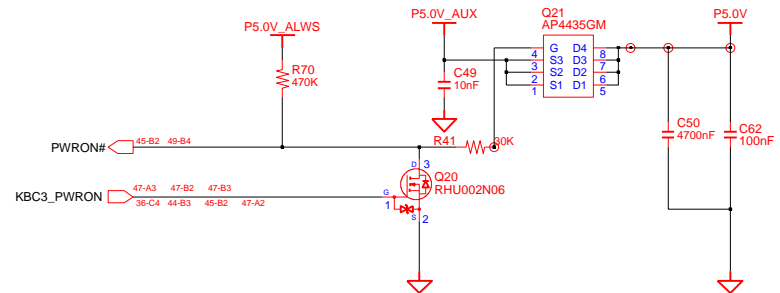
Switched Power On (1.8V)



P1.2V / P2.5V POWER



Switched Power On (P5V)

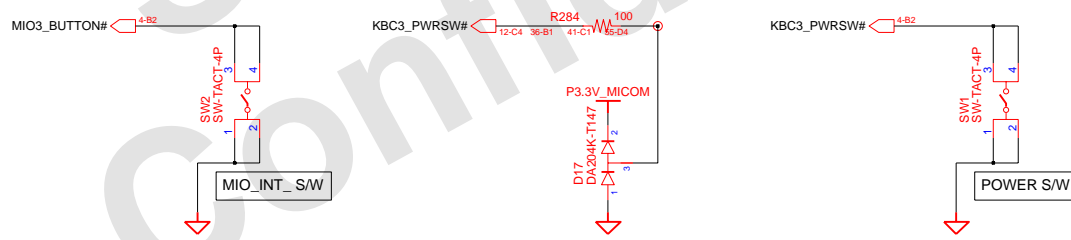
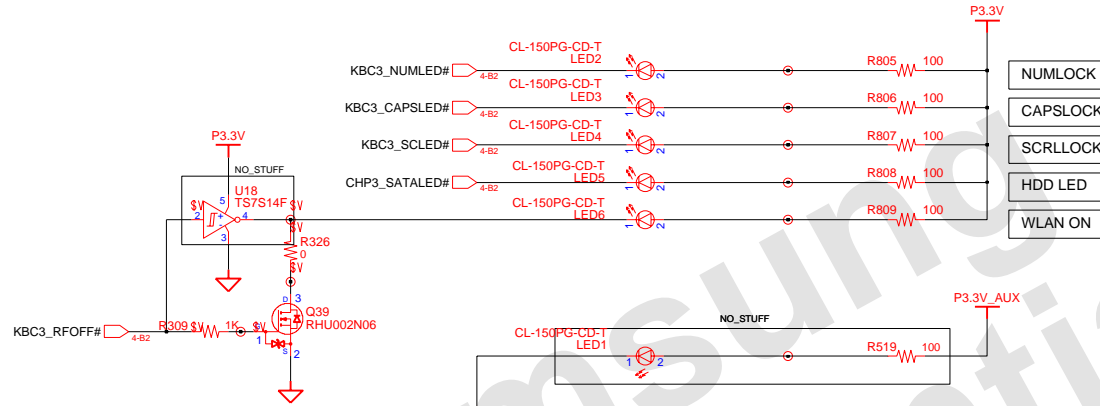


DRAW	ZHANG, ELLEN	DATE	3/15/2007	TITLE	SHANGHAI SWITCH POWER	SAMSUNG ELECTRONICS	
CHECK	ZHENG, ROKY	DEV. STEP	SR				
APPROVAL	LEE, KEVIN	REV	1.0				
MODULE CODE	undefined	LAST EDIT	March 15, 2007 10:33:33 AM	PAGE			48 OF 54

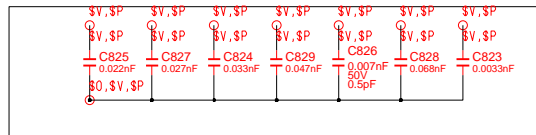
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LED
0801-002195

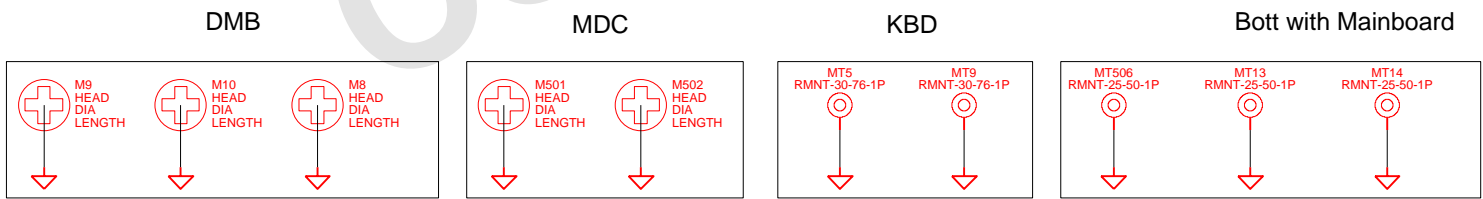
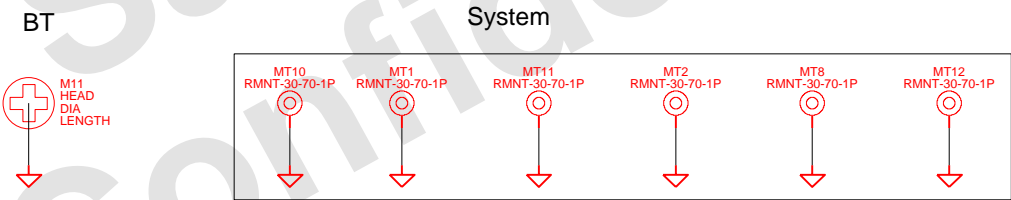
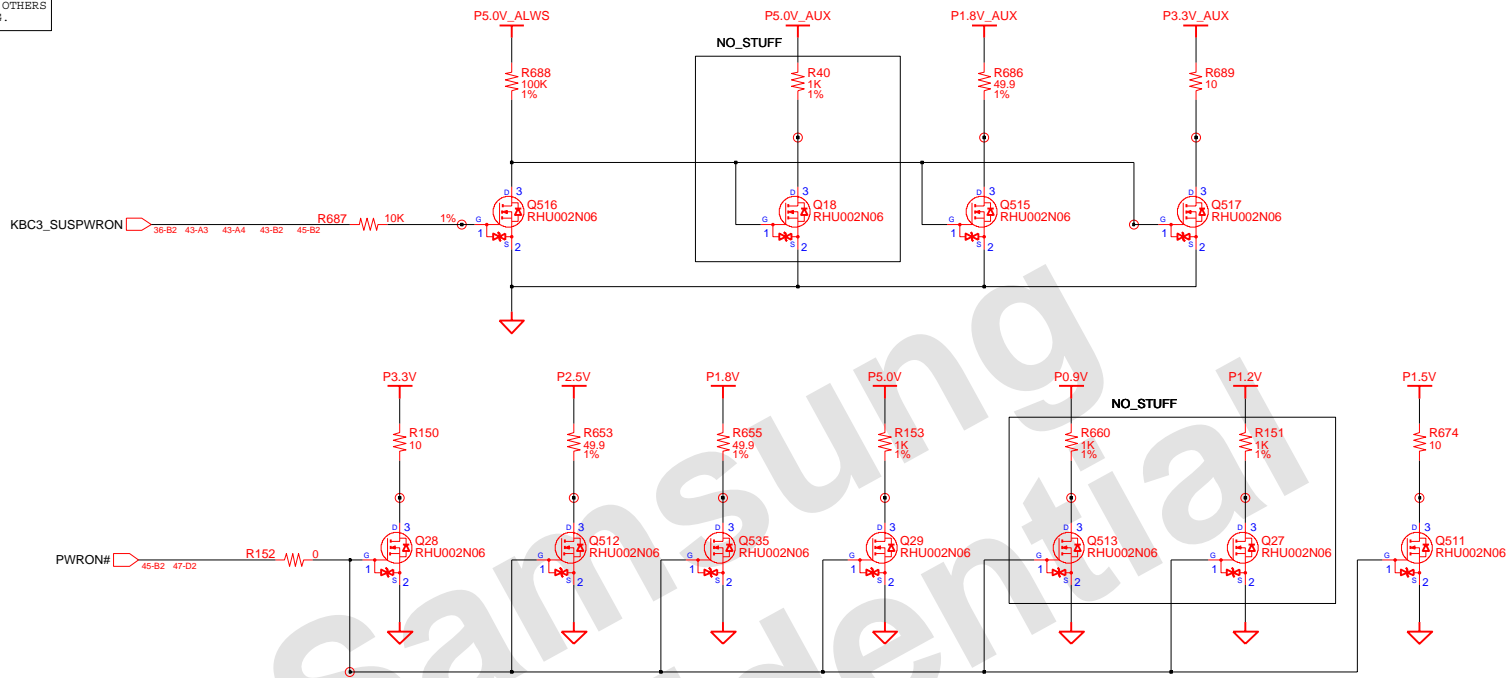


ON TOP



DRAW	ZHANG, ELLEN	DATE	3/15/2007	TITLE	SHANGHAI POWER SWITCH	SAMSUNG ELECTRONICS PART NO. BA41-00774A/00732A
CHECK	ZHENG, ROKY	DEV. STEP	SR			
APPROVAL	LEE, KEVIN	REV	1.0			
MODULE CODE	undefined	LAST EDIT	March 15, 2007 10:33:33 AM	PAGE 49 OF 54		

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DRAW	ZHANG, ELLEN	DATE	3/15/2007	TITLE	SHANGHAI POWER STRAPS	SAMSUNG ELECTRONICS
CHECK	ZHENG, ROKY	DEV. STEP	SR			
APPROVAL	LEE, KEVIN	REV	1.0			
MODULE CODE	undefined	LAST EDIT	March 15, 2007 10:33:33 AM	PAGE 50 OF 54		

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TP2020 CPU1_TDI
 TP2021 CPU1_TMS
 TP2022 PCI3_PAR
 TP2024 SMB3_CLK
 TP2025 SPI3_CLK
 TP2026 SPI3_CS#

TP1968 CPU1_A20M#

TP1971 CPU1_BSEL0
 TP1972 CPU1_BSEL1
 TP1973 CPU1_BSEL2

TP1939 PCI3_CBE#
 TP1940 PCI3_CBE1#
 TP1941 PCI3_CBE2#
 TP1942 PCI3_CBE3#
 TP1943 PCI3_GNT1#

TP1945 PCI3_IRDY#
 TP1946 PCI3_PERR#
 TP1947 PCI3_REQ1#

TP1915 PCI3_SERR#
 TP1916 PCI3_STOP#
 TP1917 PCI3_TRDY#

TP1888 KBC5_KSO(0)
 TP1889 KBC5_KSO(1)
 TP1890 KBC5_KSO(2)
 TP1891 KBC5_KSO(3)
 TP1892 KBC5_KSO(4)
 TP1893 KBC5_KSO(5)
 TP1894 KBC5_KSO(6)
 TP1895 KBC5_KSO(7)
 TP1896 KBC5_KSO(8)
 TP1897 KBC5_KSO(9)

TP1898 LCD3_EKLTON
 TP1899 LPC3_LAD(0)
 TP1900 LPC3_LAD(1)
 TP1869 LPC3_LAD(2)
 TP1870 LPC3_LAD(3)
 TP1871 MCD3_MSINS#

TP2002 CHP3_SPKR

TP2007 CPU1_PSI#

TP2011 CPU1_SLP#

TP2013 IDE5_CS1#
 TP2014 IDE5_CS3#

TP1950 CPU1_TRST#
 TP1951 EXP3_CPPE#

TP1918 PEX3_WAKE#
 TP1919 PLT3_RST#

TP1952 IDE5_DACK#
 TP1953 IDE5_IORDY
 TP1954 JCK_SENS_A
 TP1955 KBC3_CHGEN
 TP1956 KBC3_SMLCLK
 TP1957 KBC5_TDATA

TP1920 OT_L_BUTTON
 TP1921 OT_R_BUTTON
 TP1922 VGA3_HSYNC
 TP1923 VGA3_VSYNC
 TP1924 BAT3_SMLCLK#

TP1980 IDE5_DREQ
 TP1981 IDE5_IOR#
 TP1982 IDE5_IOW#
 TP1983 KBC3_A20#
 TP1984 KBC3_RST#
 TP1985 KBC3_VRON
 TP1986 KBC5_TCLK

TP1958 LCD3_VDDEN
 TP1959 MCD3_SDCDF
 TP1960 MCD3_XDALE
 TP1961 MCD3_XDCDF#
 TP1962 MCD3_XDCE#
 TP1963 MCD3_XDRE#
 TP1964 MCD3_XDWE#

TP1911 CHP3_SERIRQ
 TP1912 CHP3_SLPS3#
 TP1913 CHP3_SLPS5#

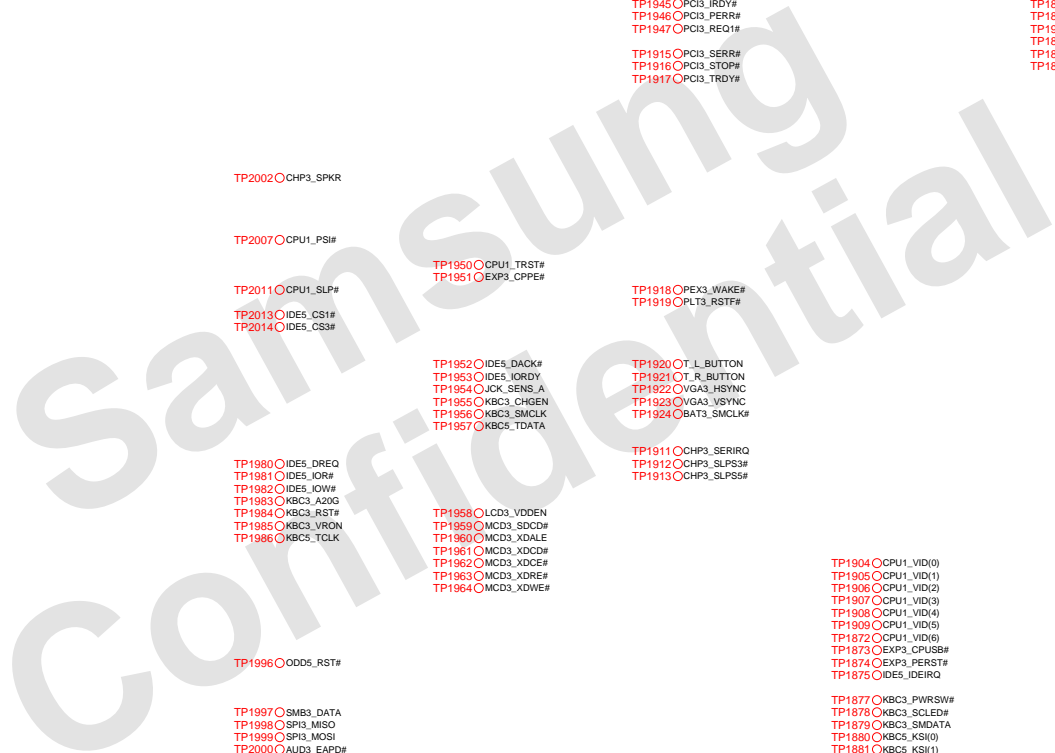
TP1904 CPU1_VID(0)
 TP1905 CPU1_VID(1)
 TP1906 CPU1_VID(2)
 TP1907 CPU1_VID(3)
 TP1908 CPU1_VID(4)
 TP1909 CPU1_VID(5)
 TP1872 CPU1_VID(6)
 TP1873 EXP3_CPUSB#
 TP1874 EXP3_PERST#
 TP1875 IDE5_IDEIRQ

TP1996 ODD5_RST#

TP1997 SMB3_DATA
 TP1998 SPI3_MISO
 TP1999 SPI3_MOSI
 TP2000 AUD3_EAPD#

TP1877 KBC3_PWRSW#
 TP1878 KBC3_SCLE#
 TP1879 KBC3_SMDATA
 TP1880 KBC5_KSI(0)
 TP1881 KBC5_KSI(1)
 TP1882 KBC5_KSI(2)
 TP1883 KBC5_KSI(3)
 TP1884 KBC5_KSI(4)
 TP1885 KBC5_KSI(5)
 TP1886 KBC5_KSI(6)
 TP1887 KBC5_KSI(7)

TP2018 CPU1_NMI
 TP2019 CPU1_TCK



DRAW	ZHANG, ELLEN	DATE	3/15/2007	TITLE	SHANGHAI TP	SAMSUNG ELECTRONICS PART NO. BA41-00774A/00732A
CHECK	ZHENG, ROKY	DEV. STEP	SR			
APPROVAL	LEE, KEVIN	REV	1.0			
MODULE CODE		LAST EDIT	March 15, 2007 10:33:33 AM	PAGE 51 OF 54		

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- TP2195 ○ CHP3_DPRSPLVR
- TP2196 ○ CHP3_SATALED#
- TP2129 ○ G_DDR
- TP2130 ○ G_DDR
- TP2198 ○ CPU1_PWRGDCPU
- TP2199 ○ CPU1_VCCSENSE
- TP2200 ○ CPU1_VSSSENSE
- TP2201 ○ JCK_SENS_MCHP
- TP2246 ○ KBC3_CAPSLED#
- TP2203 ○ KBC3_WAKESCI#
- TP2204 ○ LCD3_BKLTCTRL
- TP2205 ○ LCD3_EDID_CLK
- TP2132 ○ G_P3.3V
- TP2133 ○ G_P3.3V
- TP2134 ○ G_P3.3V
- TP2135 ○ G_P3.3V
- TP2136 ○ LCD_VDD3V
- TP2137 ○ LCD_VDD3V
- TP2088 ○ P5.0V_ALWS
- TP2089 ○ P5.0V_ALWS
- TP2090 ○ P5.0V_ALWS
- TP2091 ○ P5.0V_ALWS
- TP2092 ○ P12.0V_ALWS
- TP2093 ○ P12.0V_ALWS
- TP2032 ○ P12.0V_ALWS
- TP2033 ○ P12.0V_ALWS
- TP2233 ○ PCI3_FRAME#
- TP2235 ○ VCCP3_PWRGD
- TP2236 ○ AUD3_PCBEEP#
- TP2237 ○ BAT3_DETECT#
- TP2238 ○ BAT3_SMDATA#
- TP2239 ○ CHP3_AZ_SDI0
- TP2240 ○ CHP3_BIOSWP#
- TP2241 ○ CHP3_CPUSTP#
- TP2142 ○ LDO_P5.4V
- TP2143 ○ LDO_P5.4V
- TP2146 ○ MEM1_VREF
- TP2147 ○ MEM1_VREF
- TP2148 ○ P0.9V
- TP2149 ○ P0.9V
- TP2150 ○ P0.9V
- TP2151 ○ P0.9V
- TP2152 ○ P1.2V
- TP2153 ○ P1.2V
- TP2154 ○ P1.2V
- TP2155 ○ P1.2V
- TP2156 ○ P1.5V
- TP2157 ○ P1.5V
- TP2094 ○ P1.5V
- TP2095 ○ P1.5V
- TP2096 ○ P1.8V
- TP2097 ○ P1.8V
- TP2098 ○ P1.8V
- TP2099 ○ P1.8V
- TP2035 ○ P3.3V_AUX_EXP
- TP2037 ○ P3.3V_AUX_EXP
- TP2038 ○ VDC
- TP2039 ○ VDC
- TP2040 ○ VDC
- TP2041 ○ VDC
- TP2202 ○ ITP3_SYSRST#
- TP2180 ○ CHP3_PCISTP#
- TP2181 ○ CPU1_THRMTRIP#
- TP2182 ○ KBC3_CLKPWRGD#
- TP2183 ○ KBC3_LED_ACIN#
- TP2184 ○ KBC5_CAL_THRM#
- TP2185 ○ LCD3_EDID_DATA
- TP2186 ○ VRM3_CPU_PWRGD
- TP2046 ○ VDC_INV
- TP2047 ○ VDC_INV
- TP2050 ○ VDD_AMP
- TP2051 ○ VDD_AMP
- TP2052 ○ VDD_AMP
- TP2053 ○ VDD_AMP
- TP2054 ○ VDD_AUD
- TP2055 ○ VDD_AUD
- TP2056 ○ VDD_AUD
- TP2057 ○ VDD_AUD
- TP2058 ○ VCCP_CORE
- TP2059 ○ VCCP_CORE
- TP2060 ○ VCCP_CORE
- TP2061 ○ VCCP_CORE
- TP2188 ○ CHP3_AZ_AUD_SDO
- TP2189 ○ CHP3_AZ_MDC_SDO
- TP2103 ○ PRTC_BAT
- TP2192 ○ KBC3_LED_POWER#
- TP2158 ○ CHP3_AZ_AUD_RST#
- TP2159 ○ CHP3_SBTHRMTRIP#
- TP2162 ○ KBC3_LED_CHARGE#
- TP2163 ○ KBC3_THERM_SMCLK
- TP2109 ○ P1.5V_EXP
- TP2110 ○ P1.5V_EXP
- TP2111 ○ P1.5V_EXP
- TP2112 ○ P1.8V_AUX
- TP2113 ○ P1.8V_AUX
- TP2114 ○ P1.8V_AUX
- TP2115 ○ P1.8V_AUX
- TP2116 ○ P2.5V_LAN
- TP2117 ○ P2.5V_LAN
- TP2118 ○ P2.5V_LAN
- TP2119 ○ P2.5V_LAN
- TP2164 ○ KBC3_THERM_SMDATA
- TP2123 ○ P2.5V_MCD
- TP2124 ○ P3.3V_AUX
- TP2125 ○ P3.3V_AUX
- TP2062 ○ P3.3V_AUX
- TP2063 ○ P3.3V_AUX
- TP2065 ○ P3.3V_EXP
- TP2066 ○ P3.3V_EXP
- TP2169 ○ CHG_REF
- TP2170 ○ G_AUD
- TP2171 ○ G_AUD
- TP2172 ○ G_AUD
- TP2173 ○ G_AUD
- TP2174 ○ G_CHG
- TP2175 ○ G_CHG
- TP2176 ○ G_CHG
- TP2177 ○ G_CHG
- TP2068 ○ P3.3V_MCD
- TP2069 ○ P3.3V_MCD
- TP2070 ○ P3.3V_MCD
- TP2071 ○ P3.3V_MCD
- TP2072 ○ P5.0V_AUD
- TP2074 ○ P5.0V_AUD
- TP2075 ○ P5.0V_AUD
- TP2076 ○ P5.0V_AUD
- TP2077 ○ P5.0V_AUD
- TP2193 ○ PCI3_CLKRUN#
- TP2194 ○ PCI3_DEVSSEL#
- TP2224 ○ EXP3_CLKREQ#
- TP2225 ○ ITP3_SYSRST#
- TP2226 ○ JCK_SENS_HP#
- TP2227 ○ KBC3_CPURST#
- TP2228 ○ KBC3_EXTSMI#
- TP2229 ○ KBC3_FANCTRL
- TP2230 ○ KBC3_NBPWRGD
- TP2231 ○ KBC3_NUMLED#
- TP2232 ○ KBC3_PWRBTN#
- TP2207 ○ KBC3_RSMRST#
- TP2208 ○ KBC3_RUNS#
- TP2209 ○ KBC3_SBPWRGD
- TP2210 ○ KBC5_KSO(10)
- TP2211 ○ KBC5_KSO(11)
- TP2212 ○ KBC5_KSO(12)
- TP2213 ○ KBC5_KSO(13)
- TP2214 ○ KBC5_KSO(14)
- TP2215 ○ KBC5_KSO(15)
- TP2216 ○ LID3_SWITCH#
- TP2217 ○ LPC3_LFRAME#

PCB REVISION CONTROL (ICT)				
NO	CONNECTION	DATE(Y/M/D)	REVISION	STEP
1	N.C.			
2	1-2			
3	2-3			
4	3-1			
5	1-2-3			
6	N.C.			
7	1-2			
8	2-3			
9	3-1			
10	1-2-3			

REV1
1 ○
2 ○ 03

DRAW	ZHANG, ELLEN	DATE	3/15/2007	TITLE	SHANGHAI TP	SAMSUNG ELECTRONICS
CHECK	ZHENG, ROKY	DEV. STEP	SR			
APPROVAL	LEE, KEVIN	REV	1.0			
MODULE CODE		LAST EDIT	March 15, 2007 10:33:33 AM	PAGE 52 OF 54		

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- TP2797 CLK3_AUD5_SPK+
- TP2798 CLK3_AUD5_SPK-
- TP2799 CHP3_SATACLKREQ#
- TP2800 CHP3_SLP#
- TP2801 CHP3_SMLINK0
- TP2802 CHP3_SMLINK1
- TP2792 CLK3_DBG_LPC
- TP2793 CLK3_PCLKICH
- TP2794 CLK3_PCLKLAN
- TP2795 CLK3_SMBCLK
- TP2796 CLK3_SMBDATA
- TP2790 CPU2_THERMDA
- TP2791 CPU2_THERMDC
- TP2784 SPI01
- TP2785 LIM3
- TP2786 LIM5
- TP2787 KBC3_BKLTON
- TP2788 KBC3_CAPSLED#
- TP2789 KBC3_PWRON
- TP2775 CD3_BKLTEN
- TP2776 CD3_EDID_C
- TP2777 CD3_EDID_D
- TP2778 MCH1_HXSWING
- TP2779 MCH1_HYSWING
- TP2780 MCH3_BMBUS#
- TP2781 MCH3_CLKREQ#
- TP2782 MCH3_EXTTSS#
- TP2783 MCH3_IHSYNCS#
- TP2735 MIC1
- TP2736 MIC2
- TP2737 MINIPIC3_CLKREQ#

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DRAW	ZHANG, ELLEN	DATE	3/15/2007	TITLE	SHANGHAI TP	SAMSUNG ELECTRONICS
CHECK	ZHENG, ROKY	DEV. STEP	SR			
APPROVAL	LEE, KEVIN	REV	1.0			PART NO. BA41-00774A/00732A
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TP2755 PCB_INTA#
 TP2756 PCB_INTB#
 TP2757 PCB_INTC#
 TP2758 PCB_INTD#
 TP2759 PCB_INTE#
 TP2760 PCB_INTF#
 TP2761 PCB_INTG#
 TP2762 PCB_INTH#
 TP2763 PCB_PLOCK#
 TP2764 PCB_REQ0#
 TP2765 PCB_REQ2#
 TP2753 PCB_REQ3#
 TP2754 PCB_RST#

TP2752 MLT3_RST#

TP2740 SMB3_ALERT#
 TP2741 SMB3_LINKALERT#

TP2751 VGA3_BLUE
 TP2750 VGA3_DDCLK
 TP2749 VGA3_DDCDATA
 TP2748 VGA3_GREEN
 TP2747 VGA3_RED
 TP2746 SFX_CORE
 TP2745 SFX_CORE
 TP2744 SFX_CORE
 TP2743 SFX_CORE
 TP2742 S_EGFX
 TP2739 S_EGFX
 TP2738 S_EGFX
 TP2766 S_EGFX
 TP2767 P1.5V_PCIE
 TP2768 P1.5V_PCIE
 TP2769 P1.5V_PCIE
 TP2770 P1.5V_PCIE
 TP2771 P2.5V
 TP2772 P2.5V
 TP2773 P2.5V
 TP2774 P2.5V

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CHECK	ZHENG, ROKY	DEV. STEP	SR			
APPROVAL	LEE, KEVIN	REV	1.0			
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