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HAINAN C

CPU : Intel Yonah/Merom
 Chip Set : Intel Calistoga & ICH7-M
 Remarks : Mobility Platform

Model Name : HAINAN C
 PBA Name : MAIN
 PCB Code : BA41-00694A GCE
 BA41-00695A TPT
 Dev. Step : MP
 Revision : 1.0
 T.R. Date : 2006.07.17

DRAW	CHECK	APPROVAL
BW YOO	SS BAIK	KK BIN

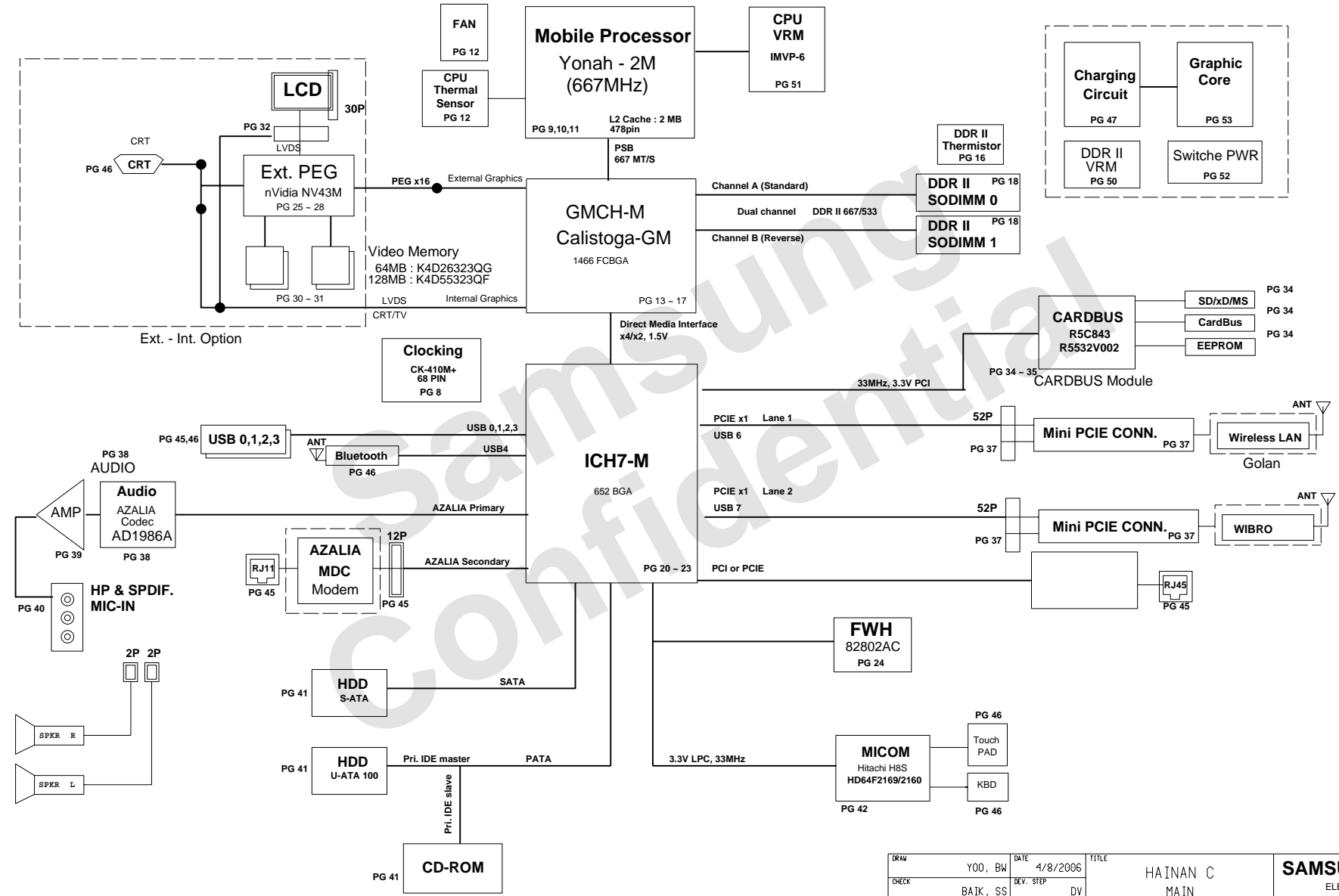
Owner : SEC Mobile R & D Signature : *X*

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DRAW	YOO, BW	DATE	4/8/2006	TITLE	HAINAN C	SAMSUNG ELECTRONICS
CHECK	BAIK, SS	DEV. STEP	DV	COVER	PART NO.	
APPROVAL	BIN, KK	REV	1.0		BA41-####A	
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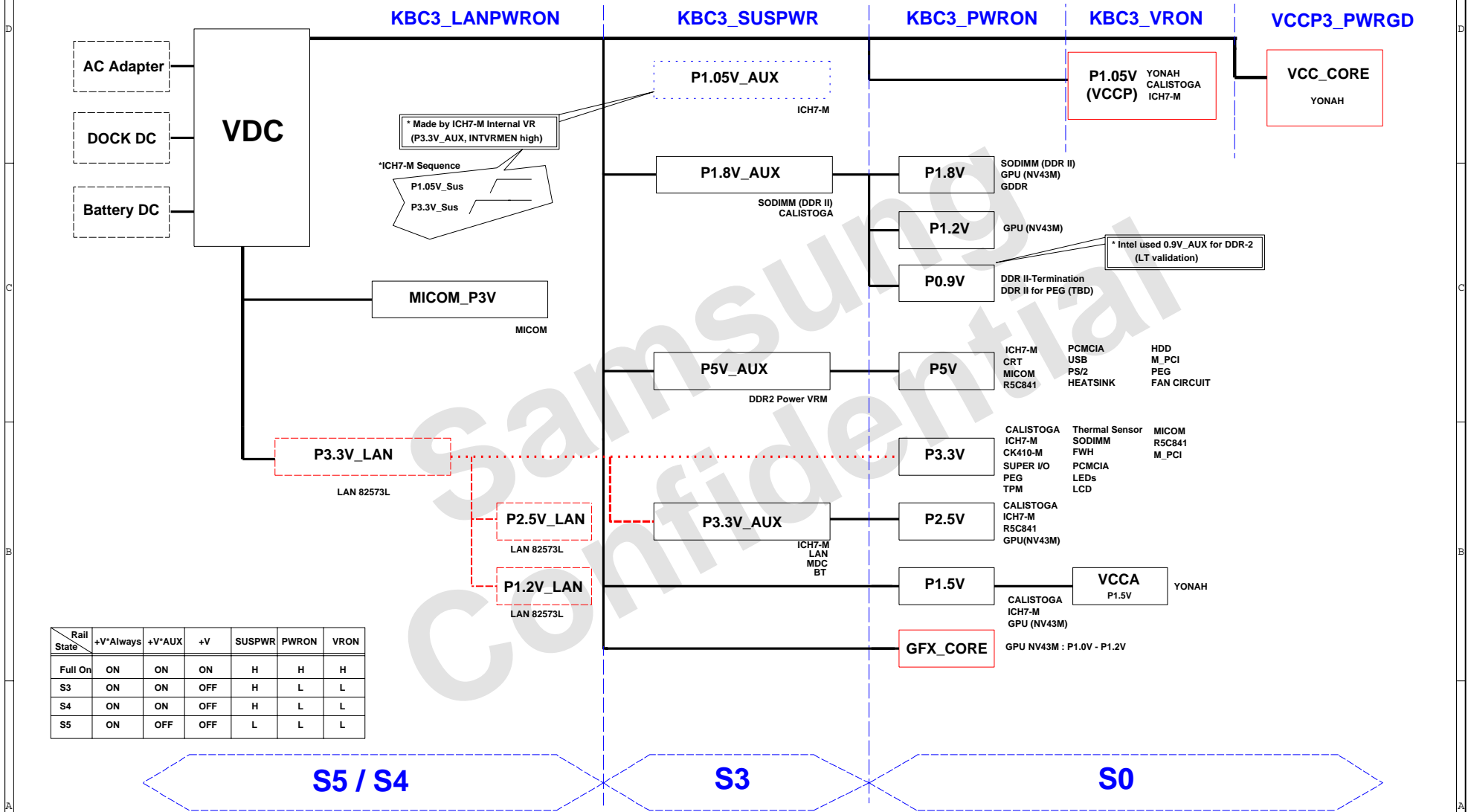
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DRAW	Y00, BW	DATE	4/8/2006	TITLE	HAINAN C	SAMSUNG ELECTRONICS
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APPROVAL	BIN, KK	REV	1.0	OPERATION BLOCK DIAGRAM		PART NO. BA41-####A
MODULE CODE	undefined	LAST EDIT	April, 13, 2006 5:00:42 PM	PAGE	2	OF 50

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Power Diagram



Rail State	+V*Always	+V*AUX	+V	SUSPWR	PWRON	VRON
Full On	ON	ON	ON	H	H	H
S3	ON	ON	OFF	H	L	L
S4	ON	ON	OFF	H	L	L
S5	ON	OFF	OFF	L	L	L

S5 / S4

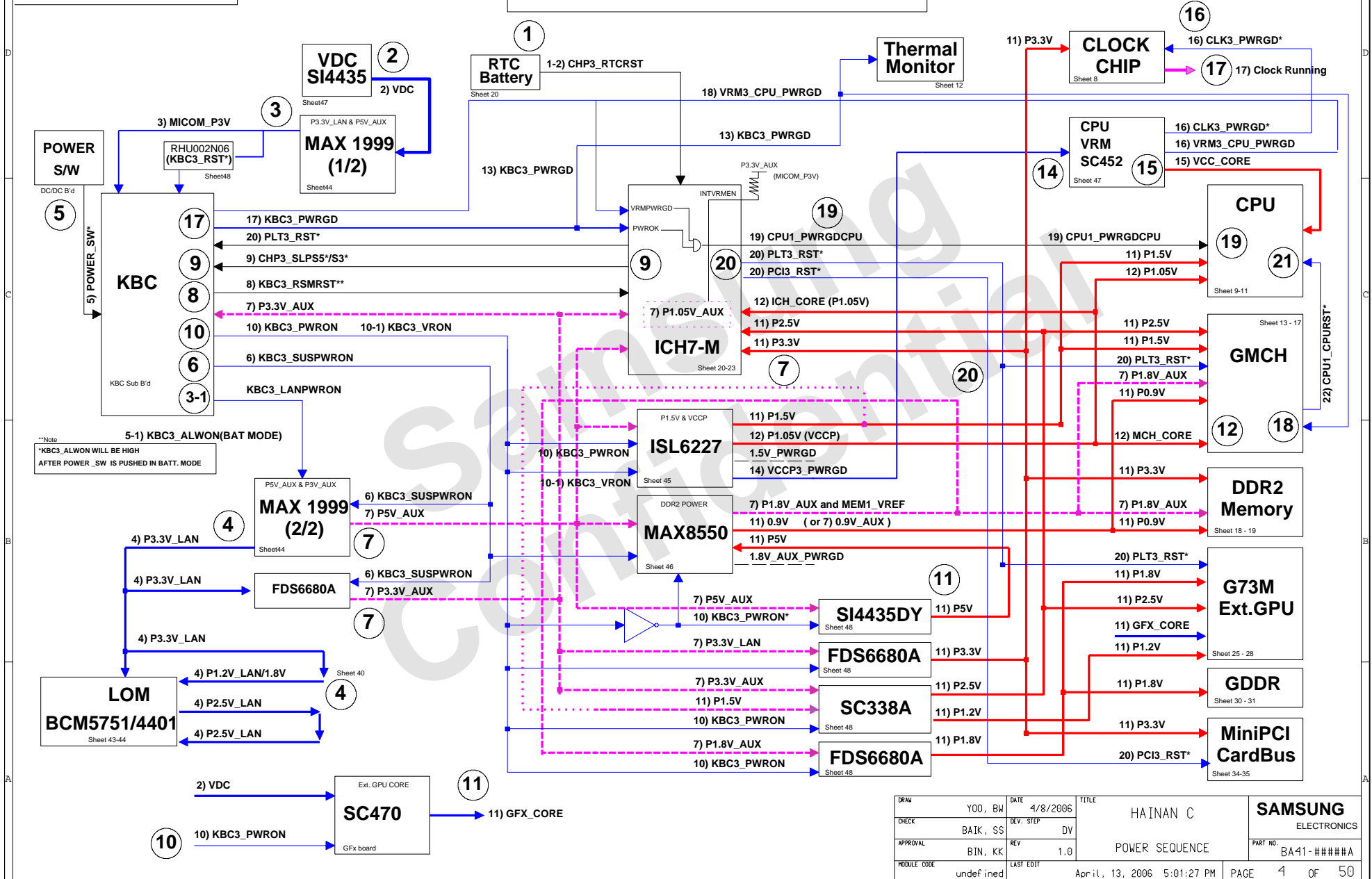
S3

S0

DRAW	Y00, BW	DATE	4/8/2006	TITLE	HAINAN C MAIN POWER DIAGRAM	SAMSUNG ELECTRONICS PART NO. BA41-####A
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APPROVAL	BIN, KK	REV	1.0			
MODULE CODE	undefined	LAST EDIT	April, 13, 2006 5:00:55 PM	PAGE	3 OF 50	

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POWER SEQUENCE Rev. 0.8

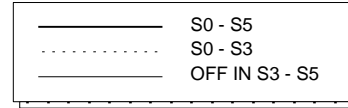


Note
 *KBC3_ALWON WILL BE HIGH
 AFTER POWER_SW IS PUSHED IN BATT. MODE

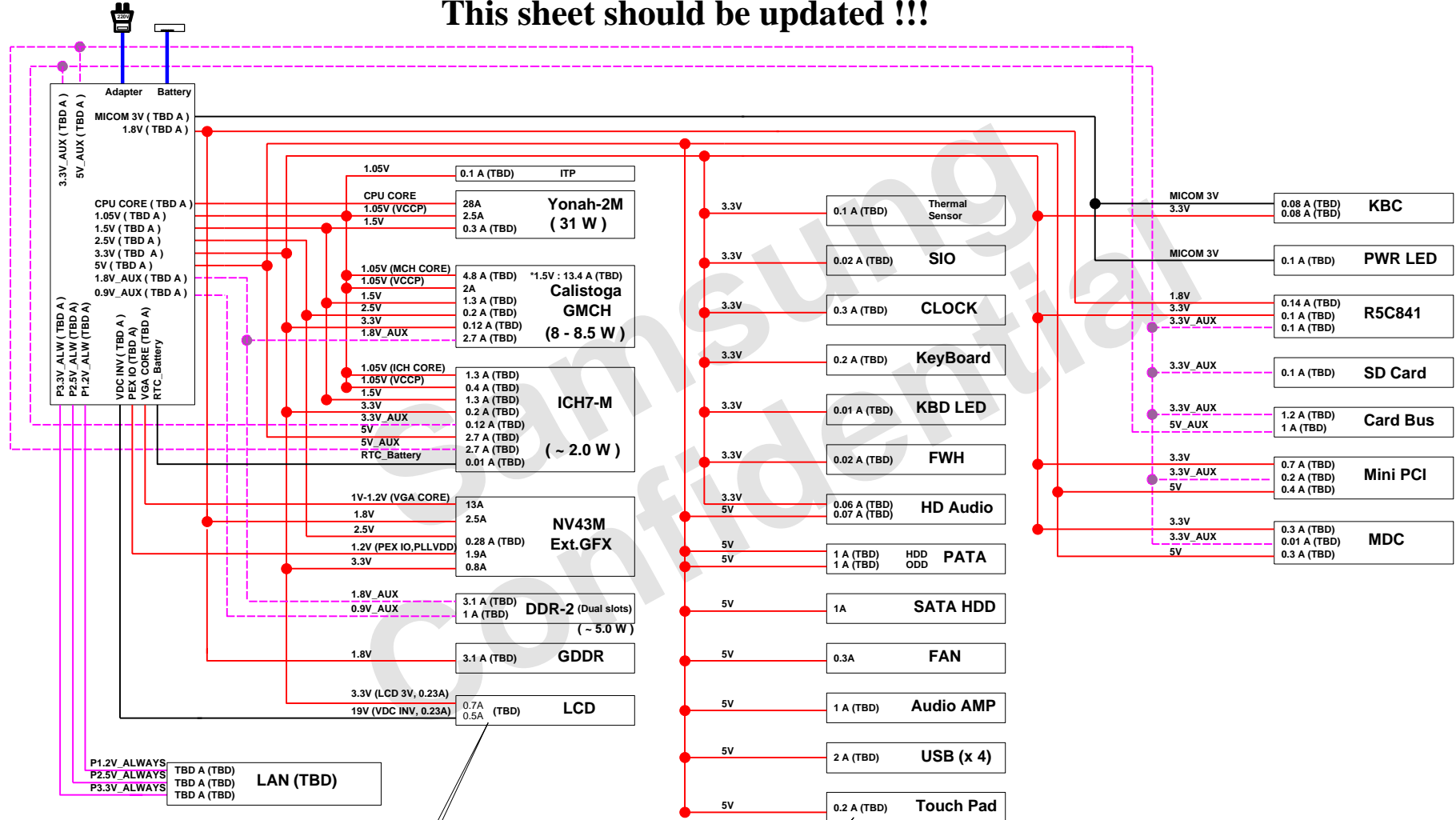
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APPROVAL	BIN, KK	REV	1.0	Apr 11, 2006 5:01:27 PM		
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COM-22C-015(1996.6.5) REV. 3						

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POWER RAILS ANALYSIS Rev. 0.8



This sheet should be updated !!!

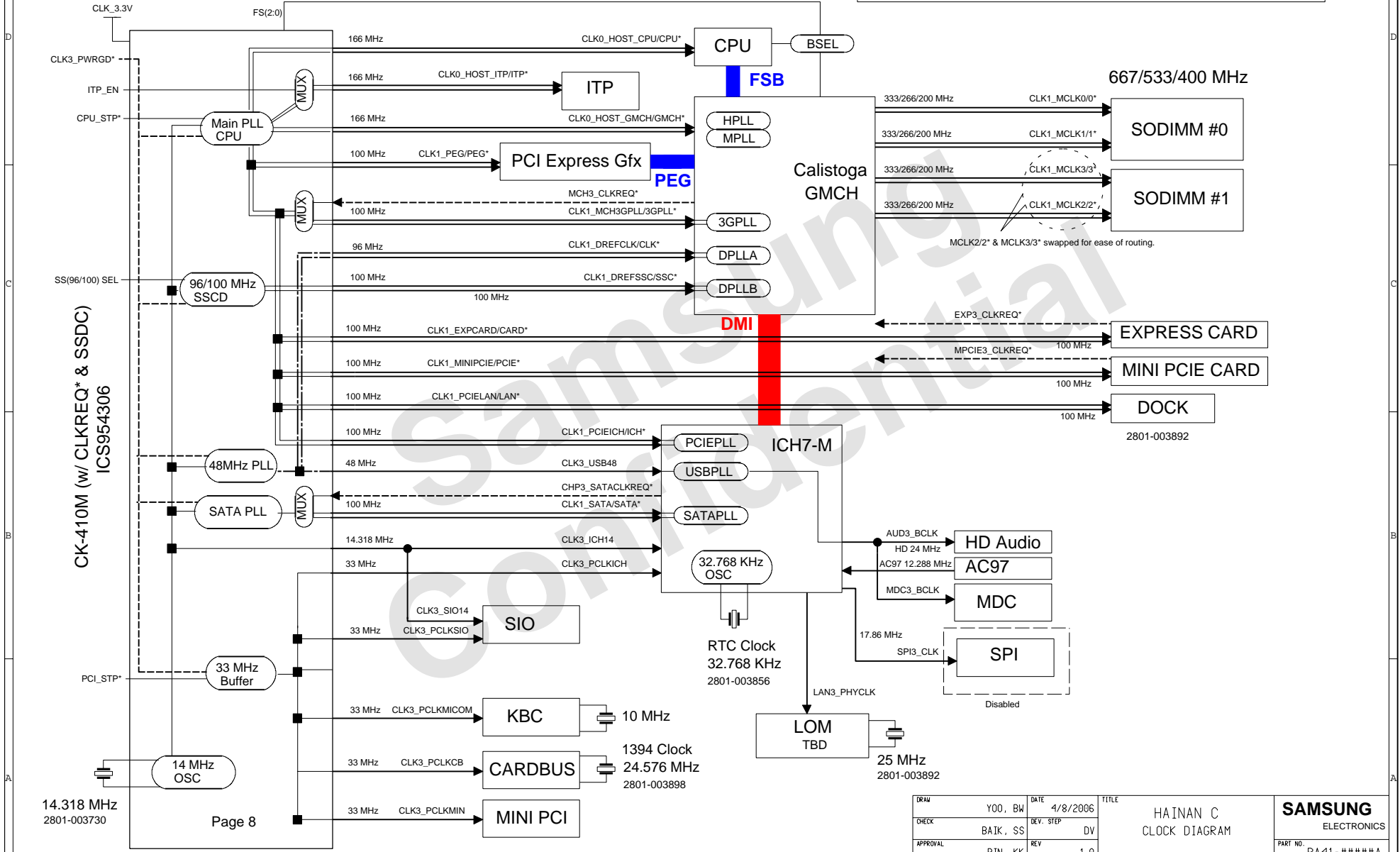


Value by Datasheet/Application notes (Value by measurement)

DRAW	Y00, BW	DATE	4/8/2006	TITLE	HAINAN C POWER BLOCK	SAMSUNG ELECTRONICS
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APPROVAL	BIN, KK	REV	1.0			PART NO. BA41-####A
MODULE CODE	undefined	LAST EDIT	April, 13, 2006 5:01:42 PM	PAGE	5	OF 50

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CLOCK DISTRIBUTION Rev. 0.7



14.318 MHz
2801-003730

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DRAW	Y00, BW	DATE	4/8/2006	TITLE	HAINAN C CLOCK DIAGRAM	SAMSUNG ELECTRONICS
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APPROVAL	BIN, KK	REV	1.0			PART NO. BA41-####A
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SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
Cardbus LAN	AD25 AD21	0 1	E, F, G G
USB	AD29(internal)	-	USB2.0 #0 : A USB2.0 #1 : D USB2.0 #2 : C
Hub to PCI	AD30(internal)	-	
LPC bridge/IDE/AC97/SMBUS	AD31(internal)	-	B
Internal MAC	AD24(internal)	-	E
AC Link	-	-	B

Voltage Rails

VDC	Primary DC system power supply (7 to 21V)
VCC_CORE	Core voltage for DOTHAN (1.308-1.068V)
VTT	DOTHAN/ALVISO Processor System Bus(PSB) Termination (1.05V) MCH-M Core Voltage
P0_9V	0.9V switched power rail (off in S3-S5)
P1_2V	1.2V switched power rail (off in S3-S5)
P1_5V	1.5V switched power rail (off in S3-S5)
P1.5V_AUX	1.5V power rail (off in S4-S5)
P1.8V	1.8V switched power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail(off in S4-S5)
P2_5V	2.5V switched power rail (off in S3-S5)
MICOM_P3V	3.3V always on power rail for MICOM
P3_3V	3.3V switched power rail (off in S3-S5)
P3.3V_AUX	3.3V power rail (off in S4-S5)
P3.3V_DTV	3.3V power rail (off in S4-S5)
P5V	5.0V switched power rail (off in S3-S5)
P5V_AUX	5.0V power rail (off in S4-S5)
P3.3V_ALWS	3.3V power rail (Always On)
P2.5V_ALWS	2.5V power rail (Always On)
P1.2V_ALWS	1.2V power rail (Always On)

Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	ICH7-M	Real Time Clock
Crystal	10MHz	MICOM	HD64F2169/2160
Crystal	14.318MHz	CLOCK-Generator	CK-410M
Crystal	24.576MHz	Cardbus Controller	1394
Crystal	25MHz	LAN	Intel LAN

CPU Core Voltage Table IMVP-6

Active Mode		Active/Deeper Sleep Dual Mode Region		Deeper Sleep/Extended Deeper Sleep Dual Mode Region	
VID(6:0)	Voltage	VID(6:0)	Voltage	VID(6:0)	Voltage
0 0 0 0 0 0 0	1.5000 V	0 1 0 1 0 0 0	1.0000 V	1 0 1 0 0 0 1	0.4875 V
0 0 0 0 0 0 1	1.4875 V	0 1 0 1 0 0 1	0.9875 V	1 0 1 0 0 1 0	0.4750 V
0 0 0 0 0 1 0	1.4750 V	0 1 0 1 0 1 0	0.9750 V	1 0 1 0 0 1 1	0.4625 V
0 0 0 0 0 1 1	1.4625 V	0 1 0 1 0 1 1	0.9625 V	1 0 1 0 1 0 0	0.4500 V
0 0 0 0 1 0 0	1.4500 V	0 1 0 1 1 0 0	0.9500 V	1 0 1 0 1 0 1	0.4375 V
0 0 0 0 1 0 1	1.4375 V	0 1 0 1 1 0 1	0.9375 V	1 0 1 0 1 0 1	0.4250 V
0 0 0 0 1 1 0	1.4250 V	0 1 0 1 1 1 0	0.9250 V	1 0 1 0 1 1 1	0.4125 V
0 0 0 0 1 1 1	1.4125 V	0 1 0 1 1 1 1	0.9125 V	1 0 1 1 0 0 0	0.4000 V
0 0 0 1 0 0 0	1.4000 V	0 1 1 0 0 0 0	0.9000 V	1 0 1 1 0 0 1	0.3875 V
0 0 0 1 0 0 1	1.3875 V	0 1 1 0 0 0 1	0.8875 V	1 0 1 1 0 1 0	0.3750 V
0 0 0 1 0 1 0	1.3750 V	0 1 1 0 0 1 0	0.8750 V	1 0 1 1 0 1 1	0.3625 V
0 0 0 1 0 1 1	1.3625 V	0 1 1 0 0 1 1	0.8625 V	1 0 1 1 1 0 0	0.3500 V
0 0 0 1 1 0 0	1.3500 V	0 1 1 0 1 0 0	0.8500 V	1 0 1 1 1 0 1	0.3375 V
0 0 0 1 1 0 1	1.3375 V	0 1 1 0 1 0 1	0.8375 V	1 0 1 1 1 1 0	0.3250 V
0 0 0 1 1 1 0	1.3250 V	0 1 1 0 1 1 0	0.8250 V	1 0 1 1 1 1 1	0.3125 V
0 0 0 1 1 1 1	1.3125 V	0 1 1 1 0 0 0	0.8125 V	1 1 0 0 0 0 0	0.3000 V
0 0 1 0 0 0 0	1.3000 V	0 1 1 1 0 0 0	0.8000 V	1 1 0 0 0 0 1	0.2875 V
0 0 1 0 0 0 1	1.2875 V	0 1 1 1 0 0 1	0.7875 V	1 1 0 0 0 1 0	0.2750 V
0 0 1 0 0 1 0	1.2750 V	0 1 1 1 0 1 0	0.7750 V	1 1 0 0 0 1 1	0.2625 V
0 0 1 0 0 1 1	1.2625 V	0 1 1 1 1 0 0	0.7625 V	1 1 0 0 1 0 0	0.2500 V
0 0 1 0 1 0 0	1.2500 V	0 1 1 1 1 0 1	0.7500 V	1 1 0 0 1 0 1	0.2375 V
0 0 1 0 1 0 1	1.2375 V	0 1 1 1 1 0 1	0.7375 V	1 1 0 0 1 1 0	0.2250 V
0 0 1 0 1 1 0	1.2250 V	0 1 1 1 1 1 0	0.7250 V	1 1 0 0 1 1 1	0.2125 V
0 0 1 0 1 1 1	1.2125 V	0 1 1 1 1 1 1	0.7125 V	1 1 0 1 0 0 0	0.2000 V
0 0 1 1 0 0 0	1.2000 V	1 0 0 0 0 0 0	0.7000 V	1 1 0 1 0 0 1	0.1875 V
0 0 1 1 0 0 1	1.1875 V	1 0 0 0 0 0 1	0.6875 V	1 1 0 1 0 1 0	0.1750 V
0 0 1 1 0 1 0	1.1750 V	1 0 0 0 0 1 0	0.6750 V	1 1 0 1 0 1 1	0.1625 V
0 0 1 1 0 1 1	1.1625 V	1 0 0 0 0 1 1	0.6625 V	1 1 0 1 1 0 0	0.1500 V
0 0 1 1 1 0 0	1.1500 V	1 0 0 0 1 0 0	0.6500 V	1 1 0 1 1 0 1	0.1375 V
0 0 1 1 1 0 1	1.1375 V	1 0 0 0 1 0 1	0.6375 V	1 1 0 1 1 1 0	0.1250 V
0 0 1 1 1 1 0	1.1250 V	1 0 0 0 1 1 0	0.6250 V	1 1 0 1 1 1 1	0.1125 V
0 0 1 1 1 1 1	1.1125 V	1 0 0 0 1 1 1	0.6125 V	1 1 1 0 0 0 0	0.1000 V
0 1 0 0 0 0 0	1.1000 V	1 0 0 1 0 0 0	0.6000 V	1 1 1 0 0 0 1	0.0875 V
0 1 0 0 0 0 1	1.0875 V	1 0 0 1 0 0 1	0.5875 V	1 1 1 0 0 1 0	0.0750 V
0 1 0 0 0 1 0	1.0750 V	1 0 0 1 0 1 0	0.5750 V	1 1 1 0 0 1 1	0.0625 V
0 1 0 0 0 1 1	1.0625 V	1 0 0 1 0 1 1	0.5625 V	1 1 1 0 1 0 0	0.0500 V
0 1 0 0 1 0 0	1.0500 V	1 0 0 1 1 0 0	0.5500 V	1 1 1 0 1 0 1	0.0375 V
0 1 0 0 1 0 1	1.0375 V	1 0 0 1 1 0 1	0.5375 V	1 1 1 0 1 1 0	0.0250 V
0 1 0 0 1 1 0	1.0250 V	1 0 0 1 1 1 0	0.5250 V	1 1 1 0 1 1 1	0.0125 V
0 1 0 0 1 1 1	1.0125 V	1 0 0 1 1 1 1	0.5125 V	1 1 1 1 0 0 0	0.0000 V
1 0 0 0 0 0 0	0.5000 V	1 0 0 0 0 0 0	0.5000 V	1 1 1 1 0 0 1	0.0000 V
				1 1 1 1 0 1 0	0.0000 V
				1 1 1 1 0 1 1	0.0000 V
				1 1 1 1 1 0 0	0.0000 V
				1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0	0.0000 V
				1 1 1 1 1 1 1	0.0000 V
				1 1 1 1 1 1 1	0.0000 V

Active: DPRSLPVR 0, DPRSTP* 1, PSI2* 0 or 1
 Deeper Slip: DPRSLPVR 1, DPRSTP* 0, PSI2* 0 or 1

11111111 - 0V power good asserted.

*Yonah Processor (2.33 GHz / 800 MHz : TBD)

C / SMB Address

Devices	Address	Hex	Bus
ICH7	Master	-	SMBUS Master
EMC6N300(CPU Thermal Sensor)	1001 110X	9Ch	Thermal Sensor
SODIMM0	1010 0000	A0h	-
SODIMM1	1010 001X	A4h	-
CK-408 (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable

USB PORT Assign

PORT NUMBER	ASSIGNED TO
0,1	SYSTEM PORT A, B
2	RESERVED
3	RESERVED
4	BLUETOOTH
5	RESERVED
6	MINI PCI/E EXPRESS CARD
7	RESERVED

System Power States

CHP3_SLPS1* S1, Powered-On-Suspend(POS) : In this state, all clocks(except the 32.768KHz clock) are stopped. The system context is maintained in system DRAM. Power is maintained to PCI, the CPU, memory controller, memory, and all other critical subsystems. Note that this state does not preclude power being removed from non-essential devices, such as disk drives. During this state, CPU can be selected for either Deep Sleep or Deeper Sleep.

CHP3_SLPS3* S3, Suspend-To-RAM(STR) : The system context is maintained in system DRAM, but power is shut off to non-critical circuits. Memory is retained, and refreshes continue. All clocks stop except RTC clock.

CHP3_SLPS4* S4, Suspend-To-Disk(STD) : The Context of the system is maintained on the disk. All power is then shut off to the system except for the logic required to resume. Externally appears same as S5, but may have different wake events.

CHP3_SLPS5* S5, Soft Off(SOFF) : System context is not maintained. All power is shut off except for the logic required to restart. A full boot is required when waking.

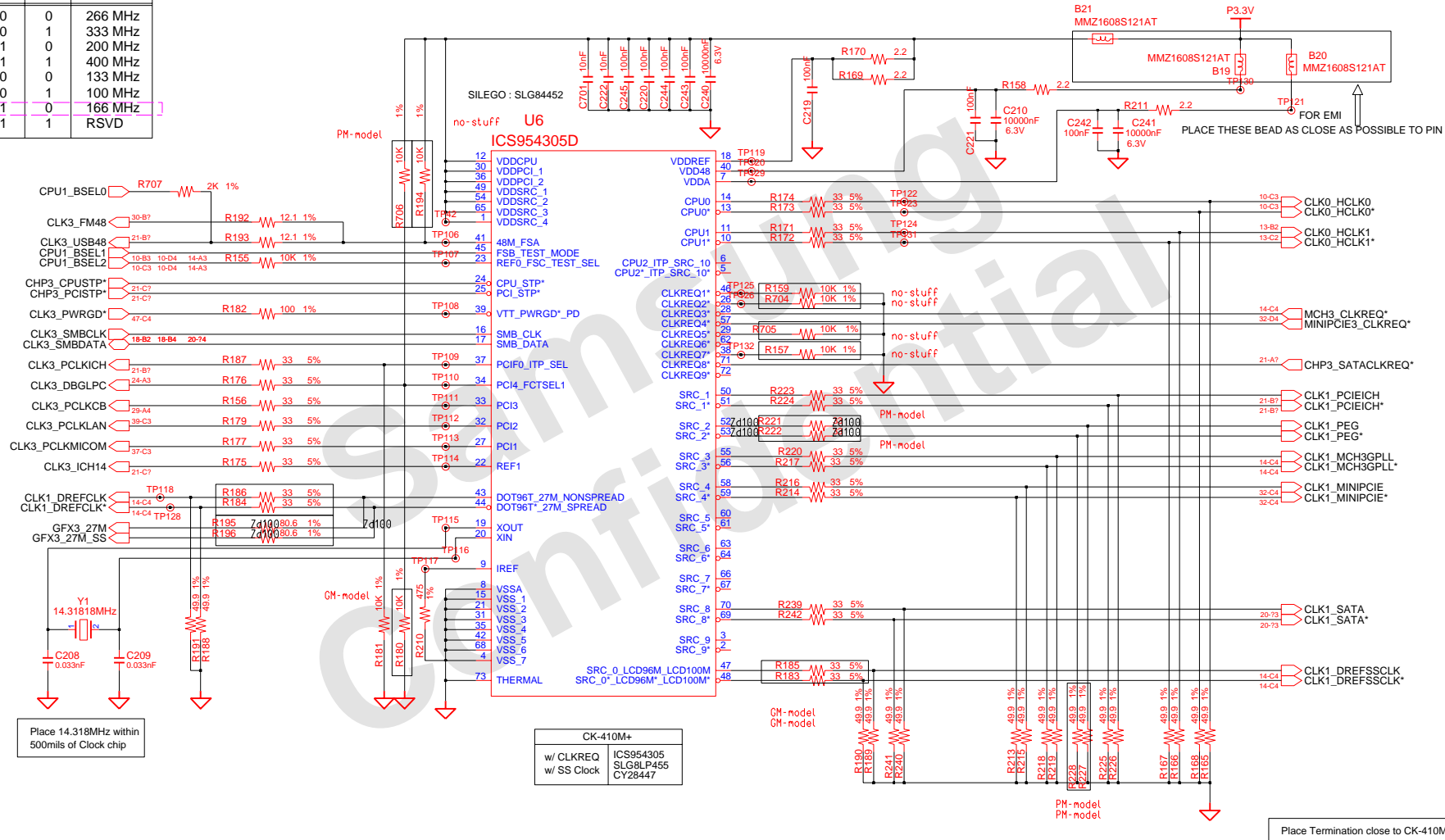
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APPROVAL	BIN, KK	REV	1.0	BOARD INFORMATION		PART NO. BA41-#####A
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PCI4_FCTSEL1(PIN34)	PIN 43, 44	PIN 47, 48
0	DOT96	LCD96/100
1	27MHZ	SRC0

CPU	FSA	FSB	FSC	HOST CLK
	BSEL0	BSEL1	BSEL2	
0	0	0	0	266 MHz
0	0	1	1	333 MHz
0	1	0	0	200 MHz
0	1	1	1	400 MHz
1	0	0	0	133 MHz
1	0	1	1	100 MHz
1	1	0	0	166 MHz
1	1	1	1	RSVD



Place 14.31818MHz within 500mils of Clock chip

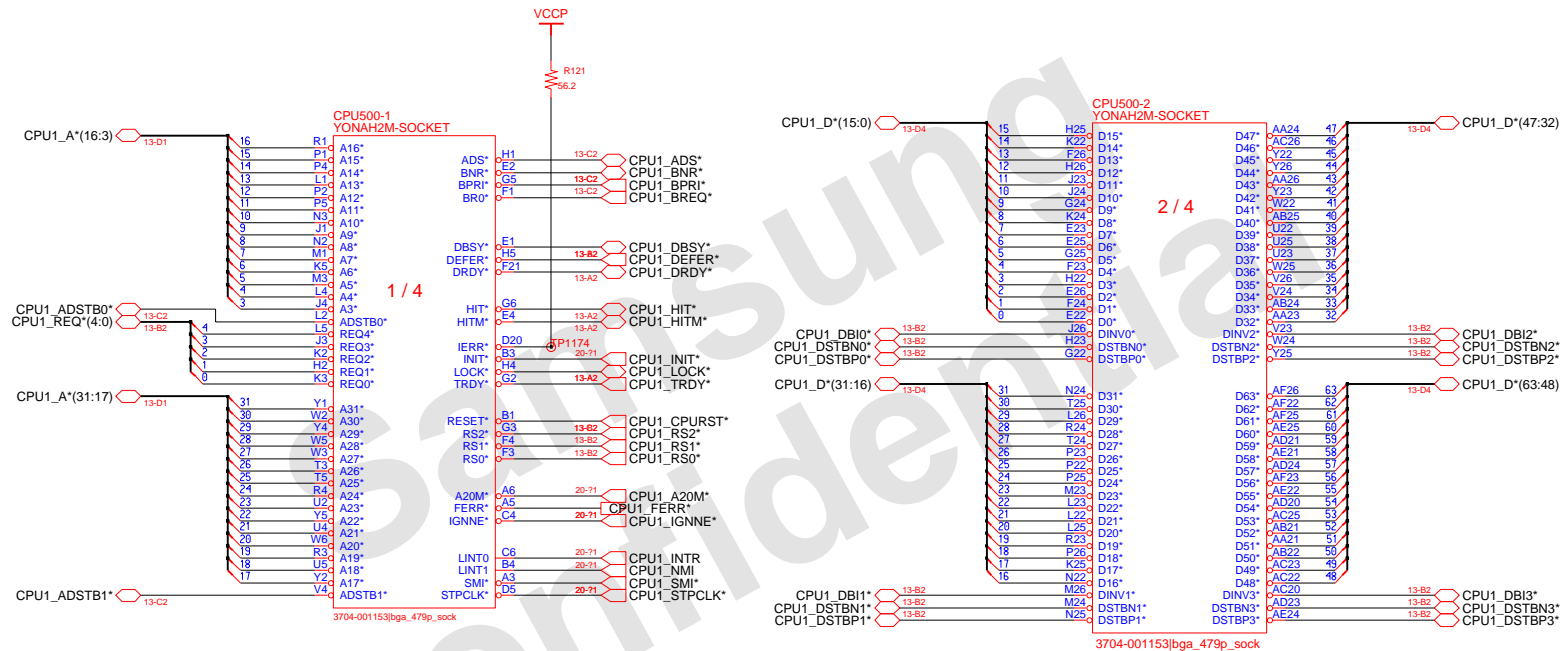
CK-410M+	
w/ CLKREQ	ICS954305 SLG9L455 CY28447
w/ SS Clock	SLG9L455 CY28447

Place Termination close to CK-410M

DRAW	Y00, BW	DATE	4/8/2006	TITLE	HAINAN C MAIN CLOCK GENERATOR	SAMSUNG ELECTRONICS PART NO. BA41-####A
CHECK	BAIK, SS	DEV. STEP	DV	APPROVAL	REV	
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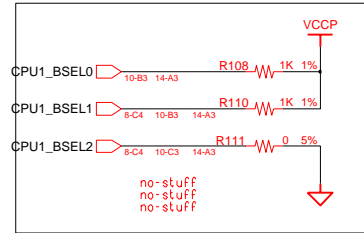
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CHECK	BAIK, SS	DEV. STEP	DV	MAIN		
APPROVAL	BIN, KK	REV	1.0	YONAH CPU (1/3)		PART NO. BA41-####A
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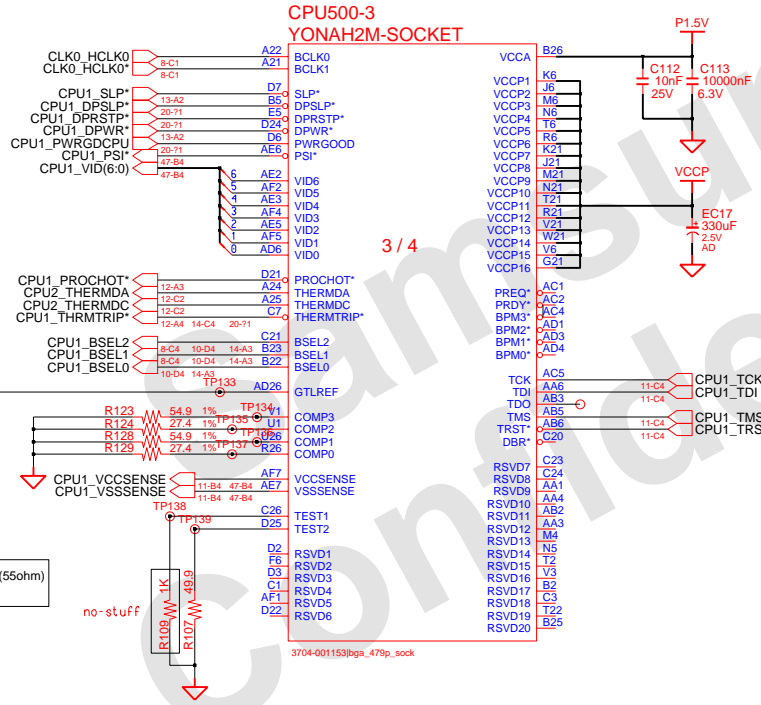


	Pull-up	Pull-down
FSB 533 MHz	BSEL0	BSEL1, BSEL2
FSB 667 MHz	BSEL0, BSEL1	BSEL2

CPU Core Voltage Table IMVP-6

Active Mode		Active/Deeper Sleep Dual Mode Region		Deeper Sleep/Extended Deeper Sleep Dual Mode Region	
VID(6:0)	Voltage	VID(6:0)	Voltage	VID(6:0)	Voltage
0 0 0 0 0 0 0	1.5000 V	0 1 0 1 0 0 0	1.0000 V	1 0 1 0 0 0 1	0.4875 V
0 0 0 0 0 0 1	1.4875 V	0 1 0 1 0 0 1	0.9875 V	1 0 1 0 0 1 0	0.4750 V
0 0 0 0 0 1 0	1.4750 V	0 1 0 1 0 1 0	0.9750 V	1 0 1 0 0 1 1	0.4625 V
0 0 0 0 0 1 1	1.4625 V	0 1 0 1 0 1 1	0.9625 V	1 0 1 0 1 0 0	0.4500 V
0 0 0 0 1 0 0	1.4500 V	0 1 0 1 1 0 0	0.9500 V	1 0 1 0 1 0 1	0.4375 V
0 0 0 0 1 0 1	1.4375 V	0 1 0 1 1 0 1	0.9375 V	1 0 1 0 1 0 1	0.4250 V
0 0 0 0 1 1 0	1.4250 V	0 1 0 1 1 1 0	0.9250 V	1 0 1 0 1 1 0	0.4125 V
0 0 0 0 1 1 1	1.4125 V	0 1 0 1 1 1 1	0.9125 V	1 0 1 1 0 0 0	0.4000 V
0 0 0 1 0 0 0	1.4000 V	0 1 1 0 0 0 0	0.9000 V	1 0 1 1 0 0 1	0.3875 V
0 0 0 1 0 0 1	1.3875 V	0 1 1 0 0 0 1	0.8875 V	1 0 1 1 0 1 0	0.3750 V
0 0 0 1 0 1 0	1.3750 V	0 1 1 0 0 1 0	0.8750 V	1 0 1 1 0 1 1	0.3625 V
0 0 0 1 0 1 1	1.3625 V	0 1 1 0 0 1 1	0.8625 V	1 0 1 1 1 0 0	0.3500 V
0 0 0 1 1 0 0	1.3500 V	0 1 1 0 1 0 0	0.8500 V	1 0 1 1 1 0 1	0.3375 V
0 0 0 1 1 0 1	1.3375 V	0 1 1 0 1 0 1	0.8375 V	1 0 1 1 1 1 0	0.3250 V
0 0 0 1 1 1 0	1.3250 V	0 1 1 0 1 1 0	0.8250 V	1 0 1 1 1 1 1	0.3125 V
0 0 0 1 1 1 1	1.3125 V	0 1 1 1 0 0 0	0.8125 V	1 1 0 0 0 0 0	0.3000 V
0 0 1 0 0 0 0	1.3000 V	0 1 1 1 0 0 0	0.8000 V	1 1 0 0 0 0 1	0.2875 V
0 0 1 0 0 0 1	1.2875 V	0 1 1 1 0 0 1	0.7875 V	1 1 0 0 0 1 0	0.2750 V
0 0 1 0 0 1 0	1.2750 V	0 1 1 1 0 1 0	0.7750 V	1 1 0 0 0 1 1	0.2625 V
0 0 1 0 0 1 1	1.2625 V	0 1 1 1 1 0 0	0.7625 V	1 1 0 0 1 0 0	0.2500 V
0 0 1 0 1 0 0	1.2500 V	0 1 1 1 1 0 0	0.7500 V	1 1 0 0 1 0 1	0.2375 V
0 0 1 0 1 0 1	1.2375 V	0 1 1 1 1 0 1	0.7375 V	1 1 0 0 1 1 0	0.2250 V
0 0 1 0 1 1 0	1.2250 V	0 1 1 1 1 1 0	0.7250 V	1 1 0 0 1 1 1	0.2125 V
0 0 1 0 1 1 1	1.2125 V	0 1 1 1 1 1 1	0.7125 V	1 1 0 1 0 0 0	0.2000 V
0 0 1 1 0 0 0	1.2000 V	1 0 0 0 0 0 0	0.7000 V	1 1 0 1 0 0 1	0.1875 V
0 0 1 1 0 0 1	1.1875 V	1 0 0 0 0 0 1	0.6875 V	1 1 0 1 0 1 0	0.1750 V
0 0 1 1 0 1 0	1.1750 V	1 0 0 0 0 1 0	0.6750 V	1 1 0 1 0 1 1	0.1625 V
0 0 1 1 0 1 1	1.1625 V	1 0 0 0 1 0 0	0.6625 V	1 1 0 1 1 0 0	0.1500 V
0 0 1 1 1 0 0	1.1500 V	1 0 0 0 1 0 0	0.6500 V	1 1 0 1 1 0 1	0.1375 V
0 0 1 1 1 0 1	1.1375 V	1 0 0 0 1 0 1	0.6375 V	1 1 0 1 1 1 0	0.1250 V
0 0 1 1 1 1 0	1.1250 V	1 0 0 0 1 1 0	0.6250 V	1 1 0 1 1 1 1	0.1125 V
0 0 1 1 1 1 1	1.1125 V	1 0 0 1 0 0 0	0.6125 V	1 1 1 0 0 0 0	0.1000 V
0 1 0 0 0 0 0	1.1000 V	1 0 0 1 0 0 0	0.6000 V	1 1 1 0 0 0 1	0.0875 V
0 1 0 0 0 0 1	1.0875 V	1 0 0 1 0 0 1	0.5875 V	1 1 1 0 0 1 0	0.0750 V
0 1 0 0 0 1 0	1.0750 V	1 0 0 1 0 1 0	0.5750 V	1 1 1 0 0 1 1	0.0625 V
0 1 0 0 0 1 1	1.0625 V	1 0 0 1 1 0 0	0.5625 V	1 1 1 0 1 0 0	0.0500 V
0 1 0 0 1 0 0	1.0500 V	1 0 0 1 1 0 0	0.5500 V	1 1 1 0 1 0 1	0.0375 V
0 1 0 0 1 0 1	1.0375 V	1 0 0 1 1 0 1	0.5375 V	1 1 1 0 1 1 0	0.0250 V
0 1 0 0 1 1 0	1.0250 V	1 0 0 1 1 1 0	0.5250 V	1 1 1 0 1 1 1	0.0125 V
0 1 0 0 1 1 1	1.0125 V	1 0 0 1 1 1 1	0.5125 V	1 1 1 1 0 0 0	0.0000 V
0 1 0 1 0 0 0	1.0000 V	1 0 0 1 1 1 1	0.5000 V	1 1 1 1 0 0 1	0.0000 V
				1 1 1 1 0 1 0	0.0000 V
				1 1 1 1 0 1 1	0.0000 V
				1 1 1 1 1 0 0	0.0000 V
				1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0	0.0000 V
				1 1 1 1 1 1 1	0.0000 V

*Yonah Processor (2.33 GHz / 800 MHz : TBD)

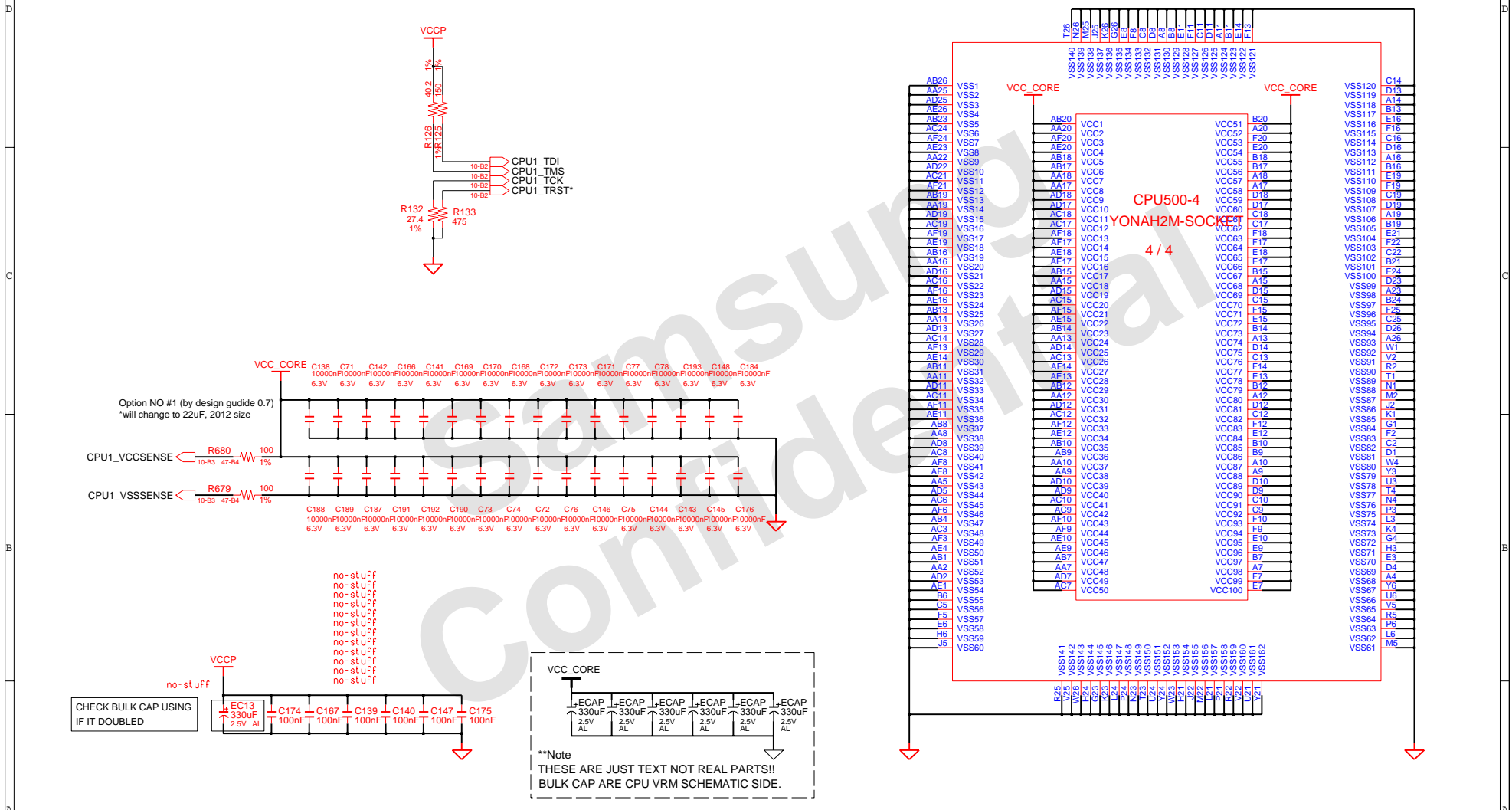


GTLREF : Keep the Voltage divider within 0.5° of the first GTLREF0 pin with Zo=55ohm trace. Minimize coupling of any switching signals to this net.

COMP0.2(COMP1.3) should be connected with Zo=27.4ohm(55ohm) trace shorter than 1/2" to their respective Banias socket pins.

DRAW	Y00, BW	DATE	4/8/2006	TITLE	HAINAN C	SAMSUNG ELECTRONICS
CHECK	BAIK, SS	DEV. STEP	DV	MAIN		
APPROVAL	BIN, KK	REV	1.0	YONAH CPU(2/3)		PART NO. BA41-####A
MODULE CODE	undefined	LAST EDIT	April, 13, 2006 5:08:33 PM	PAGE	10	OF 50

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DRAW	Y00, BW	DATE	4/8/2006	TITLE	HAINAN C	SAMSUNG ELECTRONICS
CHECK	BAIK, SS	DEV. STEP	DV	MAIN		
APPROVAL	BIN, KK	REV	1.0	YONAH CPU(3/3)		PART NO. BA41-#####A
MODULE CODE	undefined	LAST EDIT	Apr 11, 13, 2006 5:08:46 PM	PAGE	11	OF 50

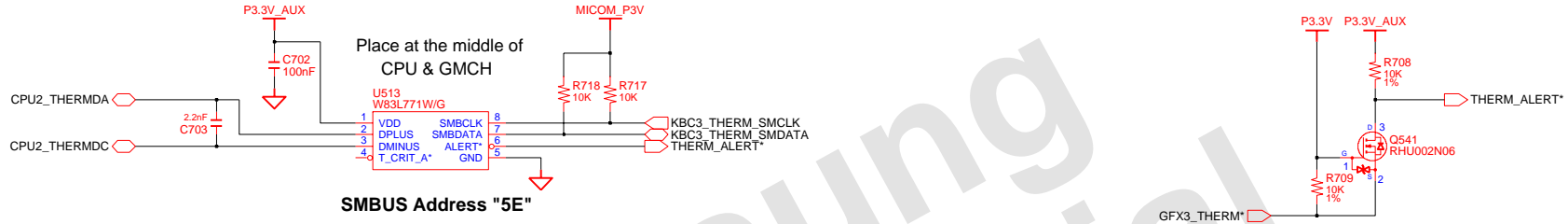
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Refer To Thermal Sensor Layout Guidelines.

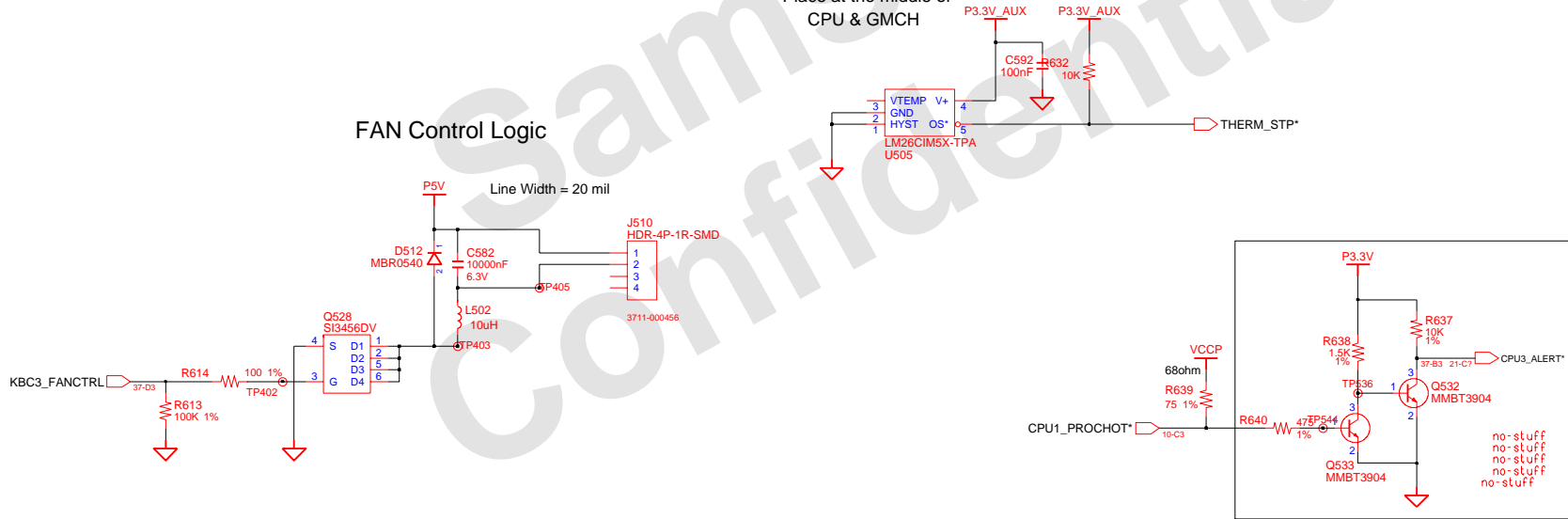
- Place the Thermal Sensor close to a remote diode.
- Keep traces away from high voltage (+12V bus)
- Keep traces away from fast data buses and CRT signal.
- Use recommended trace widths and spacings (10mil)
- Place a ground plane under the traces.
- Use guard traces flanking DXP and DXN and connecting to GND

Thermal Monitor



Place at the middle of CPU & GMCH

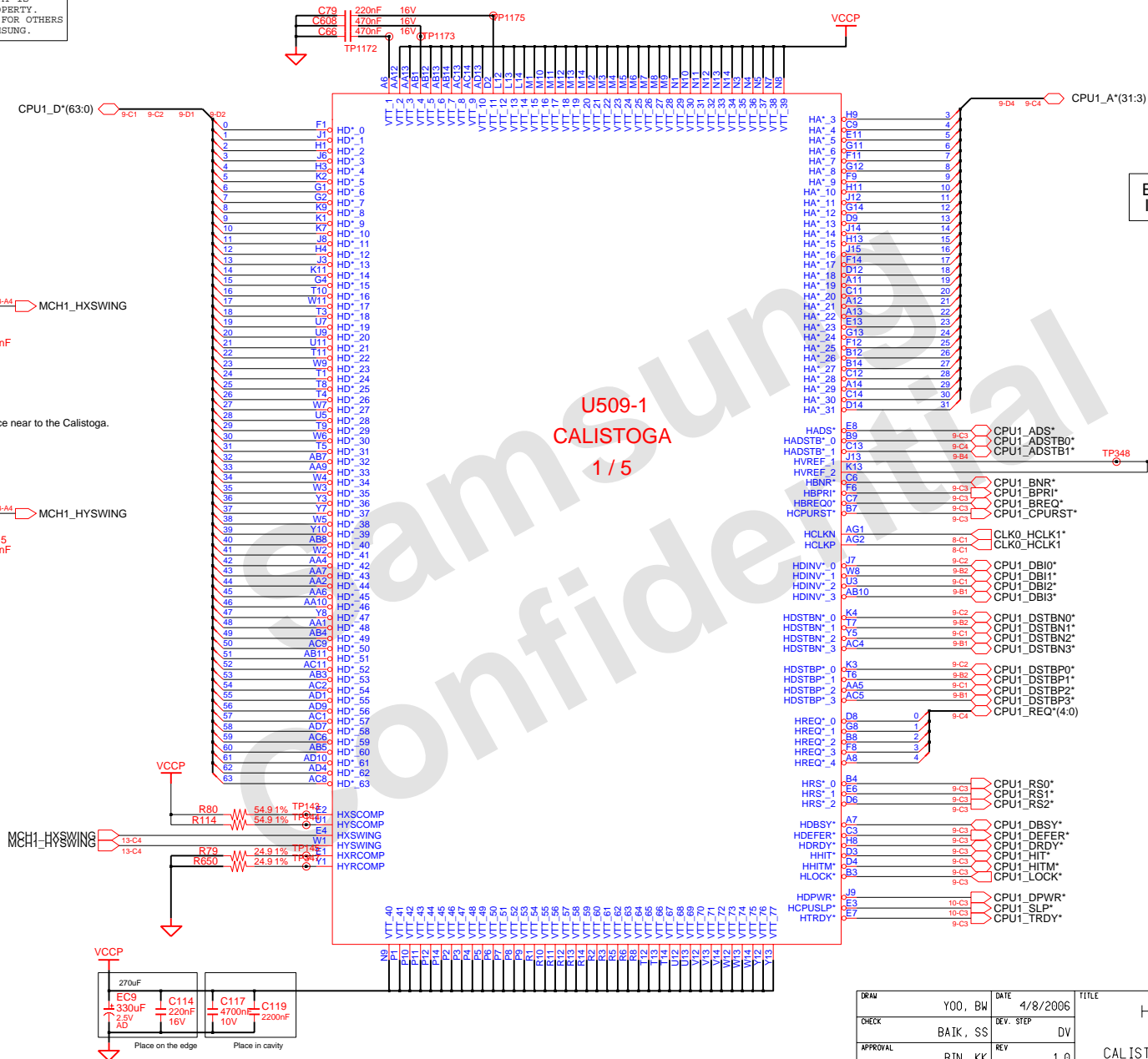
FAN Control Logic



DRAW	Y00, BW	DATE	4/8/2006	TITLE	HAINAN C	SAMSUNG ELECTRONICS
CHECK	BAIK, SS	DEV. STEP	DV	MAIN		
APPROVAL	BIN, KK	REV	1.0	THERMAL SENSOR/FAN Control	PART NO.	BA41-####A
MODULE CODE	undefined	LAST EDIT	April, 13, 2006 5:09:14 PM	PAGE	12	OF 50

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External GFx model : PM
Internal GFx model : GM

Place near to the Callistoga.

Place near to the Callistoga.

Place on the edge Place in cavity

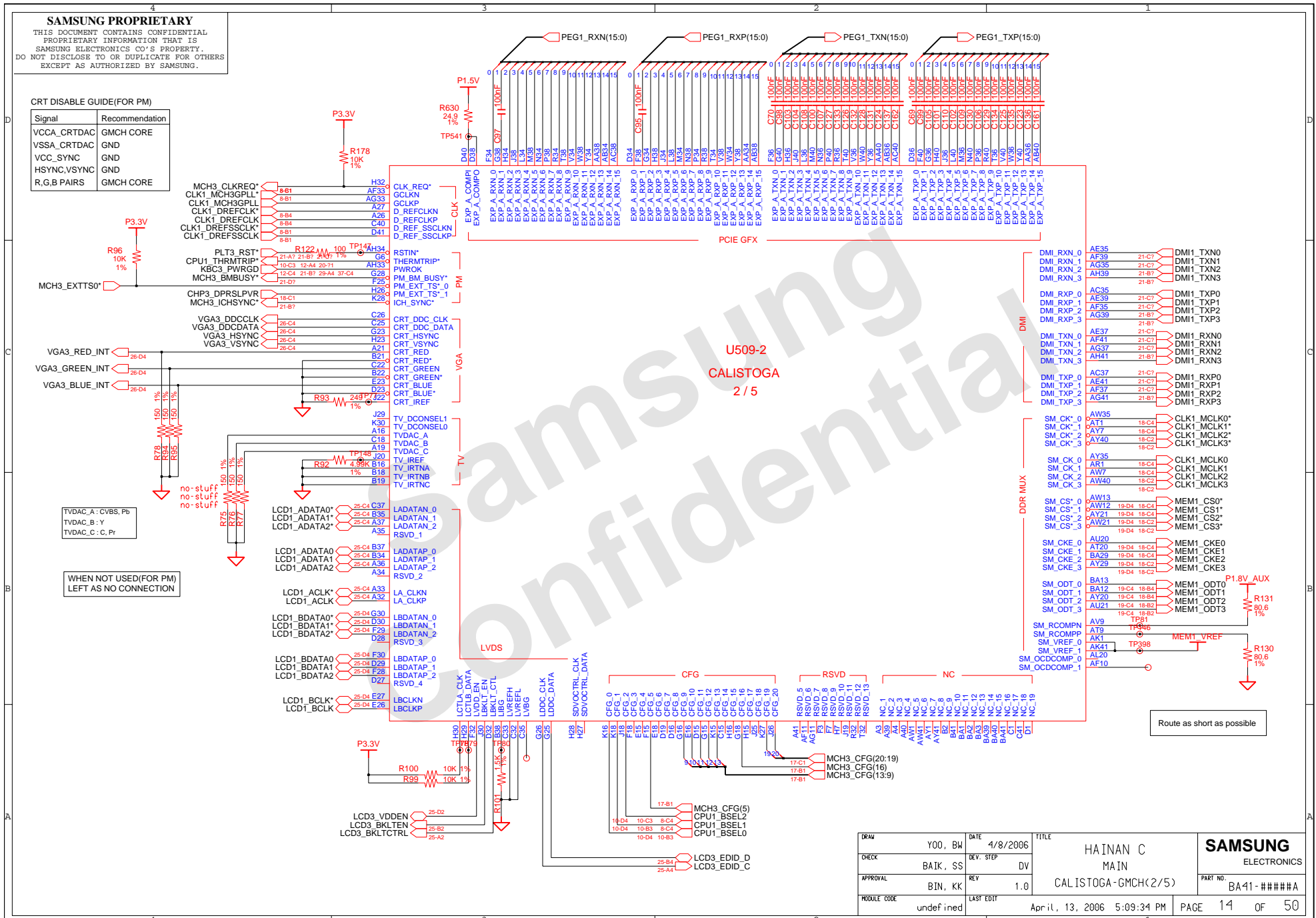
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CHECK	BAIK, SS	DEV. STEP	DV	MAIN		
APPROVAL	BIN, KK	REV	1.0	CALISTOGA-GMCH(1/5)		PART NO. BA41-####A
MODULE CODE	undefined	LAST EDIT	April, 13, 2006 5:09:24 PM	PAGE	13	OF 50

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CRT DISABLE GUIDE(FOR PM)

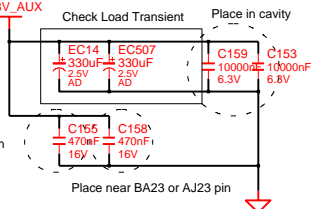
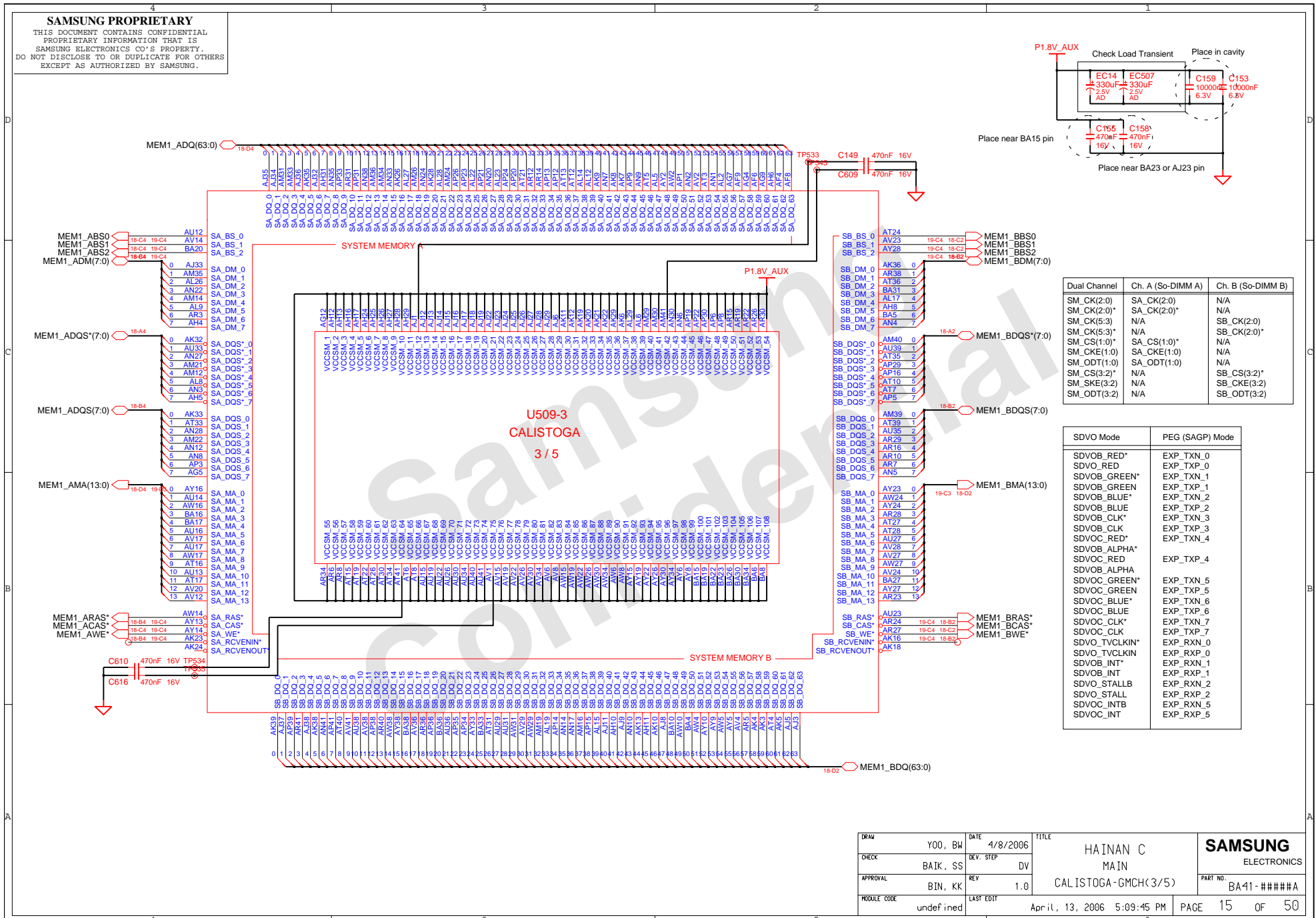
Signal	Recommendation
VCCA_CRTDAC	GMCH CORE
VSSA_CRTDAC	GND
VCC_SYNC	GND
HSYNC,VSYNC	GND
R,G,B PAIRS	GMCH CORE



Route as short as possible

DRAW	Y00, BW	DATE	4/8/2006	TITLE	HAINAN C	SAMSUNG ELECTRONICS
CHECK	BAIK, SS	DEV. STEP	DV		MAIN	
APPROVAL	BIN, KK	REV	1.0		CALISTOGA-GMCH(2/5)	PART NO. BA41-#####A
MODULE CODE	undefined	LAST EDIT	Apr 11, 2006 5:09:34 PM	PAGE	14	OF 50

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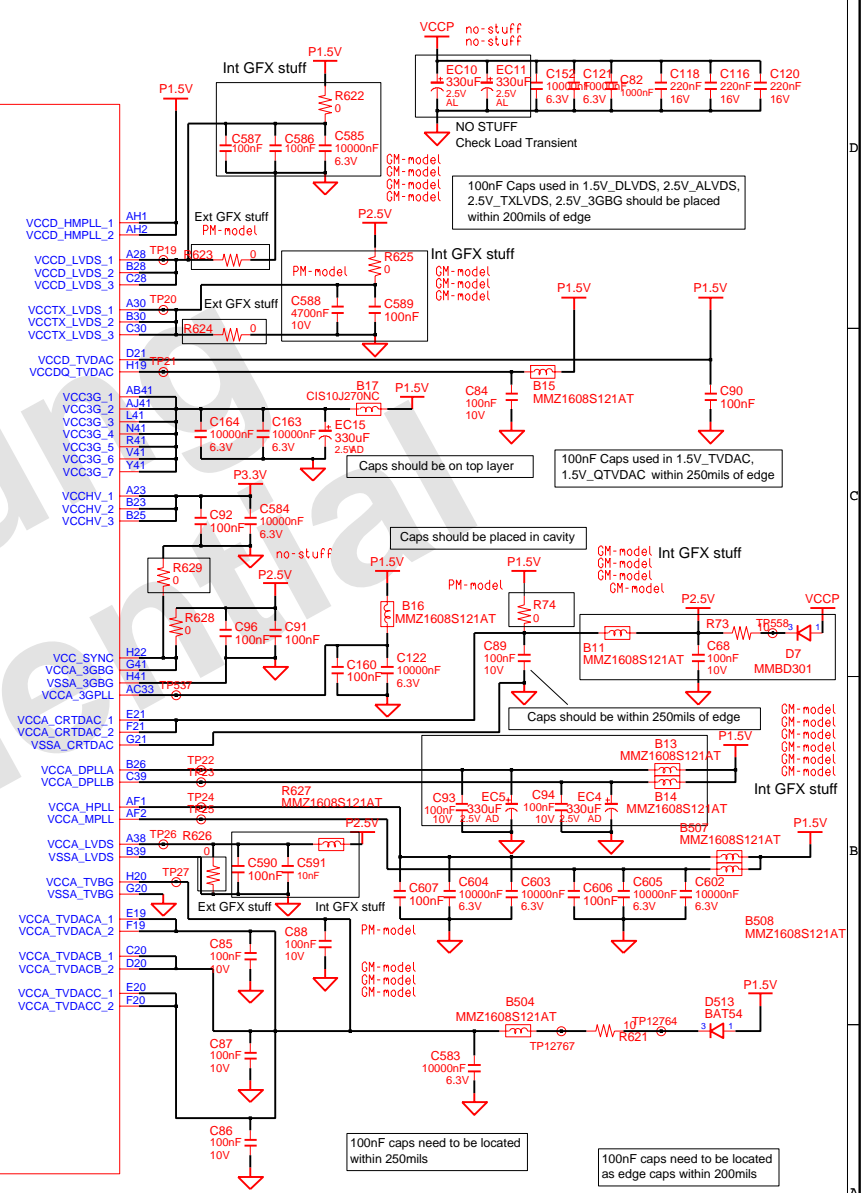
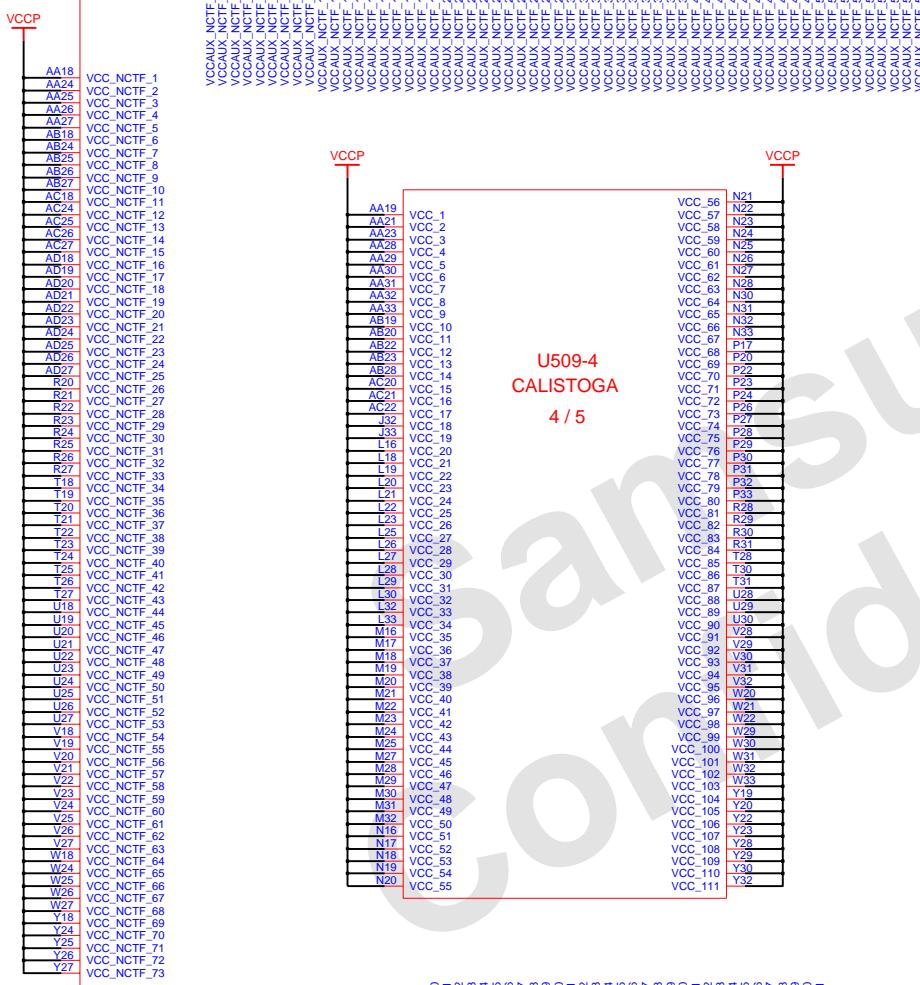


Dual Channel	Ch. A (So-Dimm A)	Ch. B (So-Dimm B)
SM_CK(2:0)	SA_CK(2:0)	N/A
SM_CK(2:0)*	SA_CK(2:0)*	N/A
SM_CK(5:3)	N/A	SB_CK(2:0)
SM_CK(5:3)*	N/A	SB_CK(2:0)*
SM_CS(1:0)	SA_CS(1:0)*	N/A
SM_CKE(1:0)	SA_CKE(1:0)	N/A
SM_ODT(1:0)	SA_ODT(1:0)	N/A
SM_CS(3:2)	N/A	SB_CS(3:2)*
SM_SKE(3:2)	N/A	SB_CKE(3:2)
SM_ODT(3:2)	N/A	SB_ODT(3:2)

SDVO Mode	PEG (SAGP) Mode
SDVOB_RED*	EXP_TXN_0
SDVO_RED	EXP_TXP_0
SDVOB_GREEN*	EXP_TXN_1
SDVOB_GREEN	EXP_TXP_1
SDVOB_BLUE*	EXP_TXN_2
SDVOB_BLUE	EXP_TXP_2
SDVOB_CLK*	EXP_TXN_3
SDVOB_CLK	EXP_TXP_3
SDVOC_RED*	EXP_TXN_4
SDVOB_ALPHA*	EXP_TXN_5
SDVOC_RED	EXP_TXP_4
SDVOB_ALPHA	EXP_TXN_6
SDVOC_GREEN*	EXP_TXN_5
SDVOC_GREEN	EXP_TXP_5
SDVOC_BLUE*	EXP_TXN_6
SDVOC_BLUE	EXP_TXP_6
SDVOC_CLK*	EXP_TXN_7
SDVOC_CLK	EXP_TXP_7
SDVO_TVCLKIN*	EXP_RXN_0
SDVO_TVCLKIN	EXP_RXP_0
SDVOB_INT*	EXP_RXN_1
SDVOB_INT	EXP_RXP_1
SDVO_STALLB	EXP_RXN_2
SDVO_STALL	EXP_RXP_2
SDVOC_INTB	EXP_RXN_5
SDVOC_INT	EXP_RXP_5

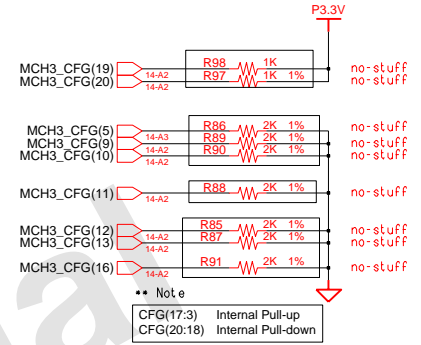
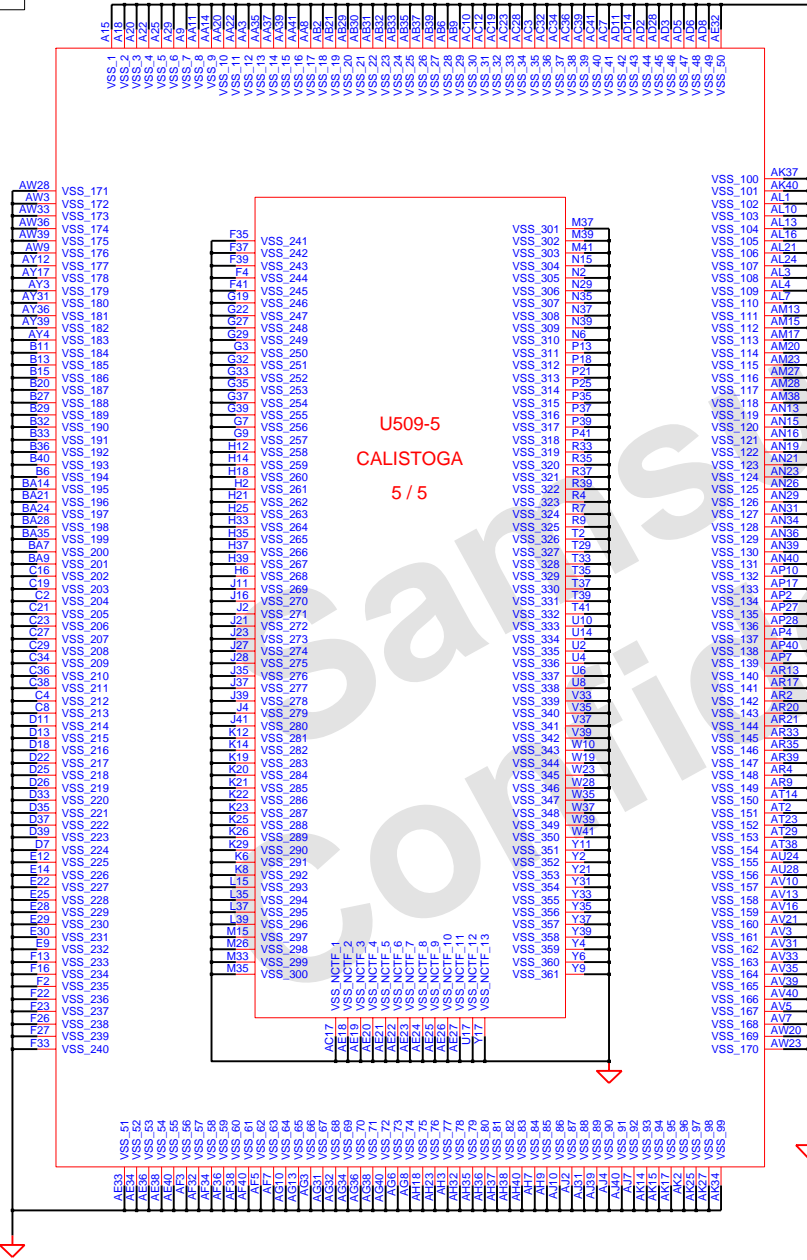
DRAW	Y00, BW	DATE	4/8/2006	TITLE	HAINAN C	SAMSUNG ELECTRONICS
CHECK	BAIK, SS	DEV. STEP	DV	MAIN		
APPROVAL	BIN, KK	REV	1.0	CALISTOGA-GMCH(3/5)		PART NO. BA41-####A
MODULE CODE	undefined	LAST EDIT	Apr 11, 2006 5:09:45 PM	PAGE	15	OF 50

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DRAW	Y00, BW	DATE	4/8/2006	TITLE	Hainan_C	SAMSUNG ELECTRONICS
CHECK	BAIK, SS	DEV. STEP	DV	MAIN		
APPROVAL	BIN, KK	REV	1.0	CALISTOGA-GMCH(4/5)		PART NO. BA41-####A
MODULE CODE		LAST EDIT	Jul., 15, 2006 2:17:33 PM	PAGE	16	OF 50

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•• Note
 CFG(17:3) Internal Pull-up
 CFG(20:18) Internal Pull-down

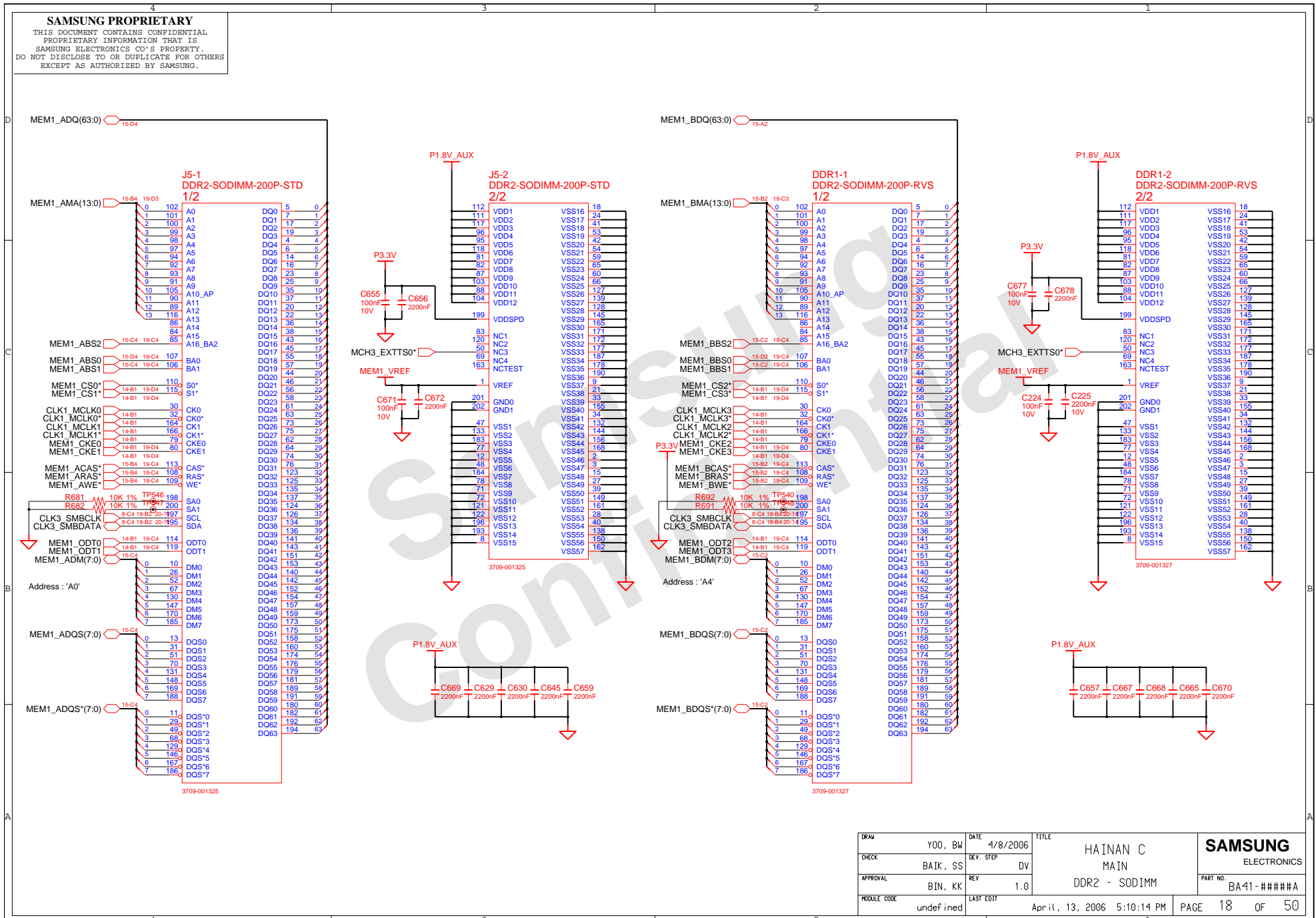
When CFG13:12 are pulled down to '00', certain clocks within Calistoga will become free-running clocks. This will lead to a rise in avg. power, but eliminates any possible clock-timing marginalities involved in clockpower-up/power-down. Intel strongly recommends leaving CFG13:12=NC (Internal PU to '11') to ensure low avg.

•• Note ***POCAFEB-10 Only (Remove in MP Model)**

CFG#	Current Setting (def.: default Option)	
	Low	High
CFG(5)	DMix2	DMix4 (def.)
CFG(6)	Reserved	DDR-II (def.)
CFG(7)	DT/Transportable	Mobile CPU (def.)
CFG(9)	PEG Reversal	Normal
CFG(16)	Dynamic ODT Disabled	Dynamic ODT Enabled (def.)
CFG(18)	VCC 1.05V (def.)	VCC 1.5V
CFG(19)	DMI Lane Normal	DMI Lane Reversal
CFG(20)	SDVO or PCIE X1 Only(def.)	SDVO and PCIE X1 Simultaneously

DRAW	Y00, BW	DATE	4/8/2006	TITLE	HAINAN C	SAMSUNG ELECTRONICS
CHECK	BAIK, SS	DEV. STEP	DV	MAIN		
APPROVAL	BIN, KK	REV	1.0	CALISTOGA-GMCH(5/5)		PART NO. BA41-####A
MODULE CODE	undefined	LAST EDIT	Apr 11, 2006 5:10:03 PM	PAGE	17	OF 50

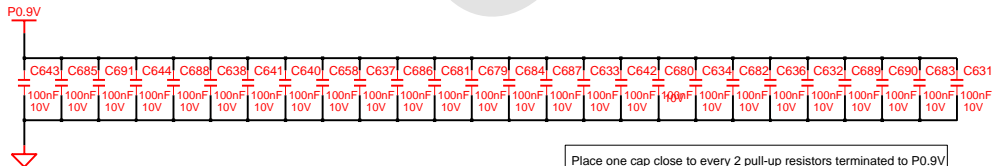
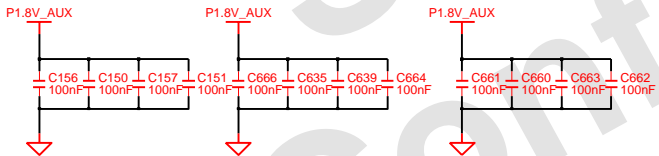
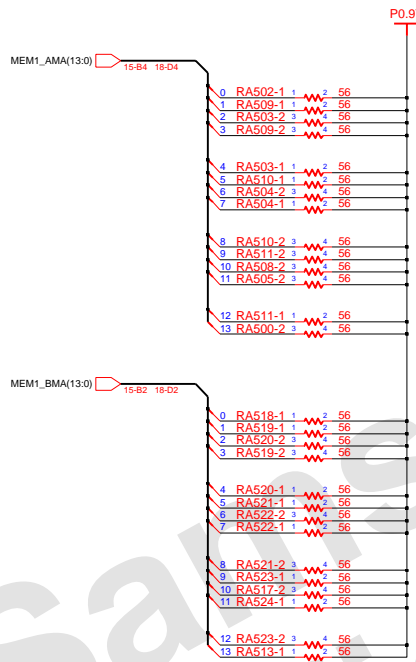
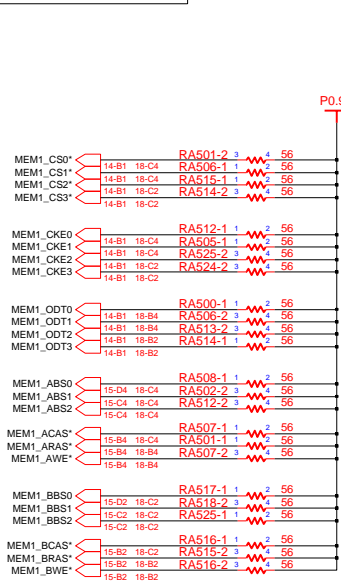
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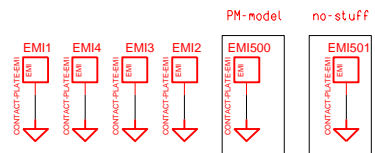
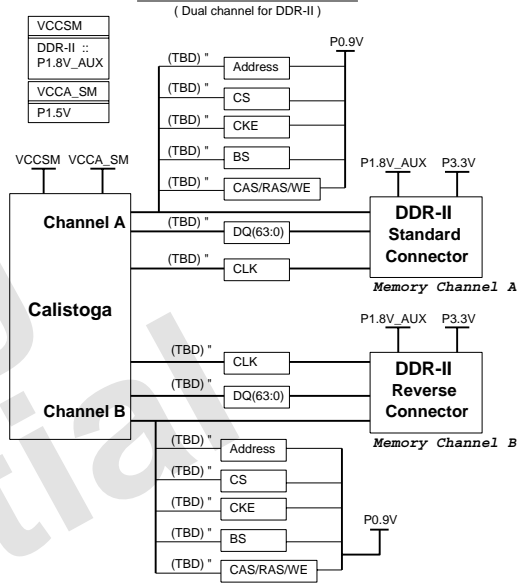
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CHECK	BAIK, SS	DEV. STEP	DV	MAIN		
APPROVAL	BIN, KK	REV	1.0	DDR2 - SODIMM		PART NO. BA41-####A
MODULE CODE	undefined	LAST EDIT	Apr 11, 2006 5:10:14 PM	PAGE	18	OF 50

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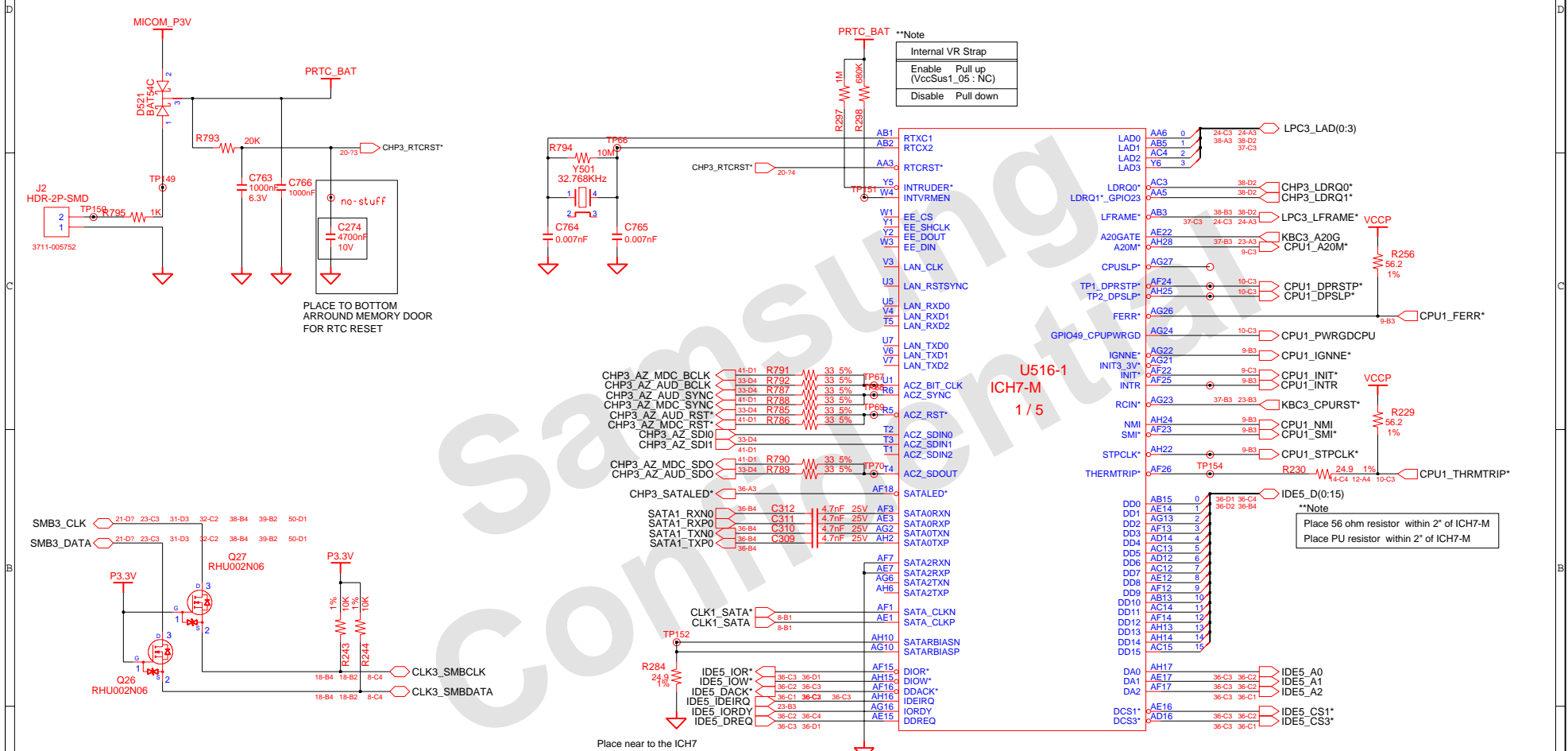
Memory Topology



DRAW	Y00, BW	DATE	4/8/2006	TITLE	HAINAN C	SAMSUNG ELECTRONICS
CHECK	BAIK, SS	DEV. STEP	DV	MAIN		
APPROVAL	BIN, KK	REV	1.0	DDR2 - TERMINATION		PART NO. BA41-####A
MODULE CODE	undefined	LAST EDIT	April, 13, 2006 5:10:25 PM	PAGE	19	OF 50

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****Note**

Internal VR Strap	
Enable	Pull up (VccSus1_05 : NC)
Disable	Pull down

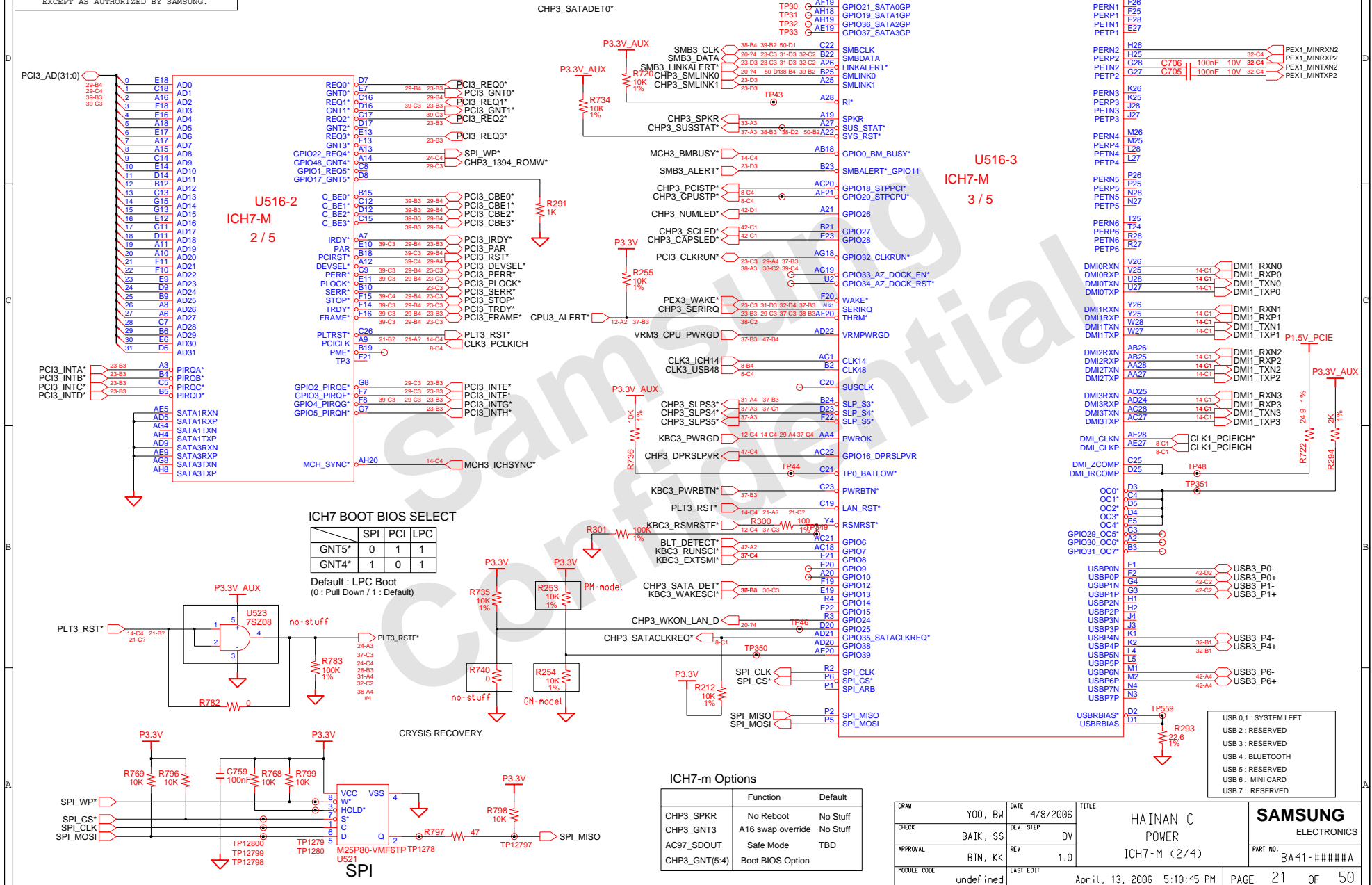
****Note**
Place 56 ohm resistor within 2" of ICH7-M
Place PU resistor within 2" of ICH7-M

DRAW	Y00, BW	DATE	4/8/2006	TITLE	HAINAN C	SAMSUNG ELECTRONICS
CHECK	BAIK, SS	DEV. STEP	DV	MAIN		
APPROVAL	BIN, KK	REV	1.0	ICH7 - M(1/4)		PART NO. BA41-####A
MODULE CODE	undefined	LAST EDIT	April, 13, 2006 5:10:35 PM	PAGE	20	OF 50

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AC caps : PCIe need to be within 250mils of the driver
Resistor for Test : Place Stuffing Option to minimize stubs



ICH7 BOOT BIOS SELECT

	SPI	PCI	LPC
GNT5*	0	1	1
GNT4*	1	0	1

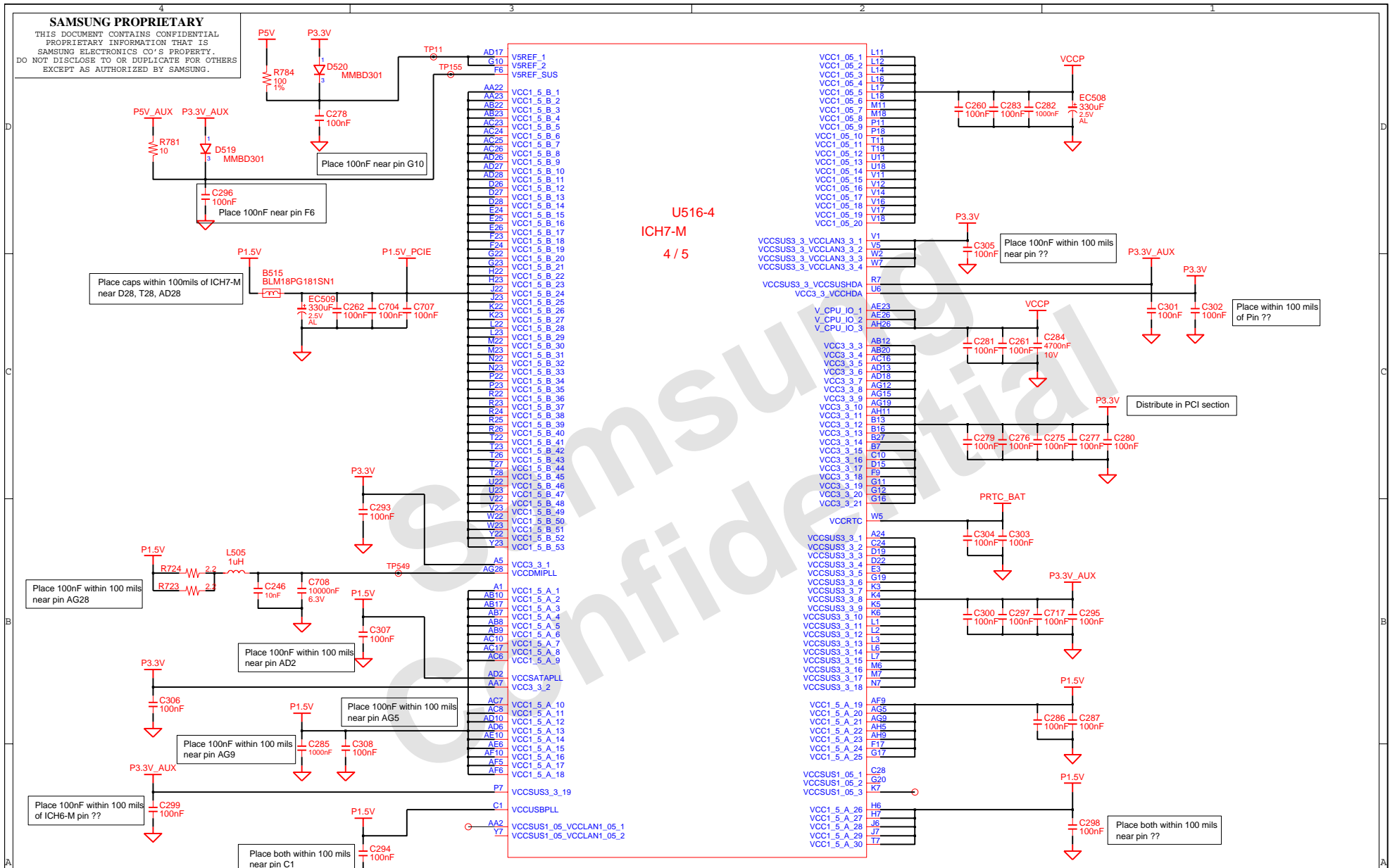
Default : LPC Boot
(0 : Pull Down / 1 : Default)

ICH7-m Options

Function	Default
CHP3_SPKR	No Reboot No Stuff
CHP3_GNT3	A16 swap override No Stuff
AC97_SDOUT	Safe Mode TBD
CHP3_GNT(5:4)	Boot BIOS Option

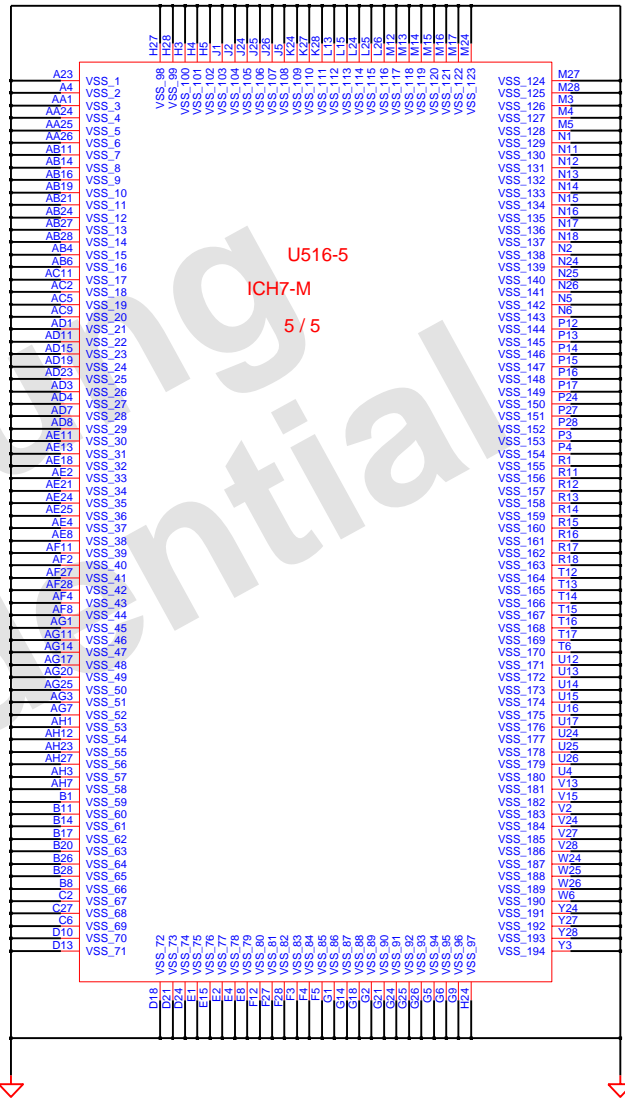
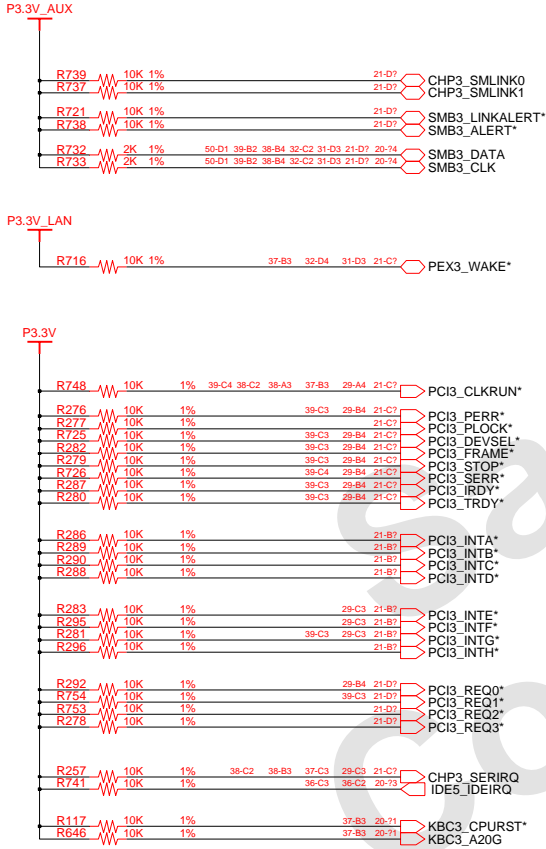
DRAW	Y00, BW	DATE	4/8/2006	TITLE	HAINAN C POWER ICH7-M (2/4)	SAMSUNG ELECTRONICS PART NO. BA41-#####A
CHECK	BAJK, SS	DEV. STEP	DV			
APPROVAL	REV	REV	1.0			
MODULE CODE	undefined	LAST EDIT	Apr 11, 2006 5:10:45 PM	PAGE	21 OF 50	

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DRAW	Y00, BW	DATE	4/8/2006	TITLE	HAINAN C	SAMSUNG ELECTRONICS
CHECK	BAIK, SS	DEV. STEP	DV	MAIN		
APPROVAL	BIN, KK	REV	1.0	ICH7 - M(3/4)		PART NO. BA41-####A
MODULE CODE	undefined	LAST EDIT	Apr 11, 13, 2006 5:10:54 PM	PAGE	22	OF 50

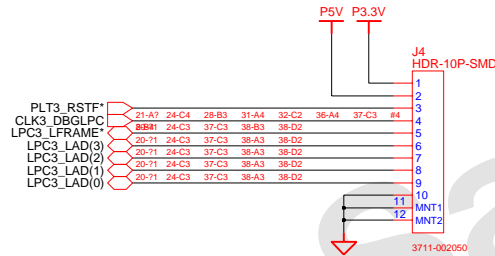
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DRAW	Y00, BW	DATE	4/8/2006	TITLE	HAINAN C	SAMSUNG ELECTRONICS
CHECK	BAIK, SS	DEV. STEP	DV	MAIN		
APPROVAL	BIN, KK	REV	1.0	ICH7 - M(4/4)	PART NO.	BA41-#####A
MODULE CODE	undefined	LAST EDIT	April, 13, 2006 5:11:07 PM	PAGE	23	OF 50

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BIOS CODE

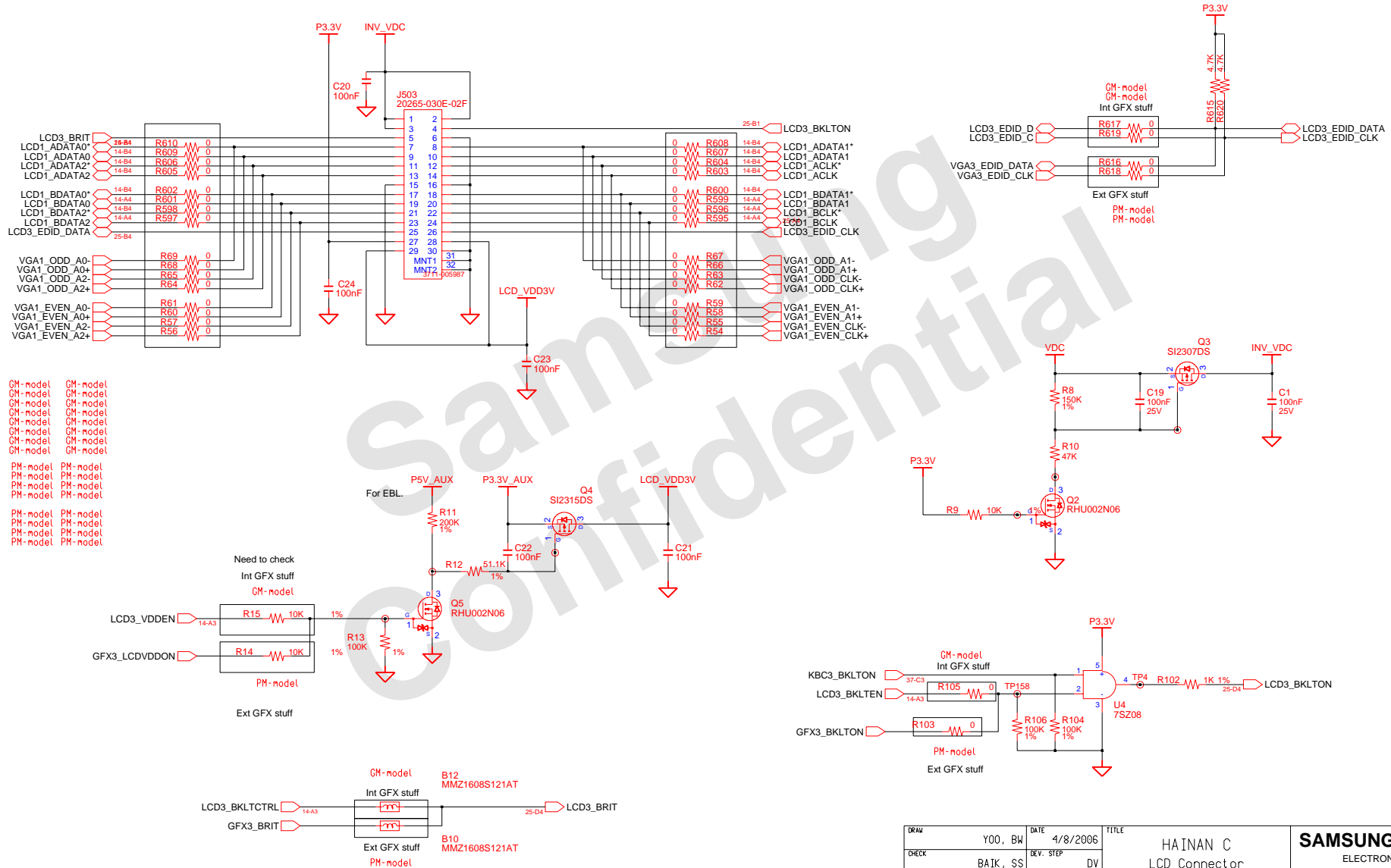


02	VERIFY REAL MODE	66	CONFIGURE ADVANCE CACHE REG.
03	DISABLE NMI	6A	DISPLAY EXTERNAL CACHE SIZE
04	GET CPU TYPE	6C	DISPLAY SHADOW MESSAGE
06	INIT. SYSTEM H/W	6E	DISPLAY NON-DISPOSABLE SEGMENT
08	INIT. CHIPSET REG.	70	DISPLAY ERROR MESSAGE
09	SET IN POST FLAG	72	CHECK FOR CONFIGURATION ERROR
0A	INIT CPU.REG	74	TEST REAL-TIME CLOCK
0B	CPU CACHE ON	76	CHECK FOR KEYBOARD EERROR
0C	INIT.CACHE TO POST	7C	SETUP HARDWARE INTERRUPT VECTOR
0E	INIT. I/O VALUE	7E	TEST COPROCESSER IF PRESENT
0F	ENABLE THE L-BUS IDE	80	DISABLE ON-BOARD I/O PORT
10	INIT. POWER MANAGER	82	DETECT AND INSTALL EXT.RS232C
11	LOAD ALTERNATE REG.	84	DETECT AND INSTALL EXT.PARALLEL
13	PCI BUS MASTER RESET WITH INITIAL POST VALUE	86	RE-INIT. ON-BOARD I/O PORT
14	INIT. KEYBOARD CONTROLLER	88	INIT. BIOS DATA ROM
16	CHECK CHECKSUM	8A	INIT.EXTENDED BIOS DATA AREA
18	8254 TIMER INIT.	8C	INIT. FDD CONTROLLER
1A	8237 DMA CONTROLLER INIT.	9A	SHADOW OPTION ROMS
1C	RESET INTERRUPT CONTROLLER	9C	SETUP POWER MANAGEMENT
20	TEST DRAM REFRESH	9E	ENABLE H/W INTERRUPT
22	TEST 8742 KEYBOARD CONTROLLER	A0	SET TIME OF DAY
24	SET ES SEGMENT REG. TO 4GB	A4	INIT. TYPEMATIC RATE
26	ENABLE A20	A8	ERASE F2 PROMPT
28	AUTO SIZING DRAM	AA	SCAN FOR F2 KEY STROKE
32	COMPUTE THE CPU SPEED	AC	ENTER SETUP
34	TESET CMOS RAM	AE	CLEAR IN POST FLAG
38	SHADOW SYSTEM BIOS ROM	B0	CHECK FOR ERRORS
3A	AUTO SIZING CACHE	B2	POST DONE-PREPARE TO BOOT O/S
3C	CONFIGURE ADVANCED CHIPSET REG.	B4	ONE BEEP
3D	LOAD ALTER REG. WITH CMOS VALUE	B6	CHECK PASSWORD (OPTION)
42	INIT. INTERRUPT VECTOR	B7	ACPI INIT
44	INIT. BIOS INTERRUPT	BA	DMI INIT
46	CHECK ROM COPYRIGHT NOTICE	BE	CLEAR SCREEN
47	INIT. I2O SUPPORT IF INSTALLED	C0	TRY BOOT WITH INT19
48	CHECK VIDEO CONFIGURE AGAINST CMOS	D0	INTERRUPT HANDLER ERROR
49	INIT. PCI BUS AND DEVICE	D2	UNKNOWN INTERRUPT ERROR
4A	INIT. ALL VIDEO BIOS ROM	D4	PENDING INTERRUPT ERROR
4C	SHADOW VIDEO BIOS ROM	D6	SHUTDOWN 5
50	DISPLAY CPU TYPE AND SPEED	D8	SHUTDOWN ERROR
52	TEST KEYBOARD	DA	EXTENDED BLOCK MOVE
54	SET KEYCLICK IF ENABLED	DC	SHUTDOWN 10
56	ENABLE KEYBOARD	89	ENABLE NMI
58	TEST FOR UNEXPECTED INTERRUPTS	90	INIT. HDD CONTROLLER
5A	DISPLAY "PRESS SETUP"	91	INIT. LOCAL BUS HDD CONTROLLER
5C	TEST RAM BETWEEN 512K AND 640K	92	JUMP TO USER PATCH 2
60	TEST EXTENDED MEMORY	94	DISABLE A20 ADDRESS LINE
62	TEST EXTENDED MEMORY ADDRESS LINE	96	CLEAR HUGE ES SEGMENT REG.
64	JUMP TO USER PATCH 1	98	SEARCH FOR OPTION ROMS

DRAW	YOO, BW	DATE	4/8/2006	TITLE	HAINAN C	SAMSUNG ELECTRONICS
CHECK	BAIK, SS	DEV. STEP	DV		MAIN	
APPROVAL	BIN, KK	REV	1.0		FIRMWARE HUB	PART NO. BA41-####A
MODULE CODE	undefined	LAST EDIT	April, 13, 2006 5:15:06 PM	PAGE	24	OF 50

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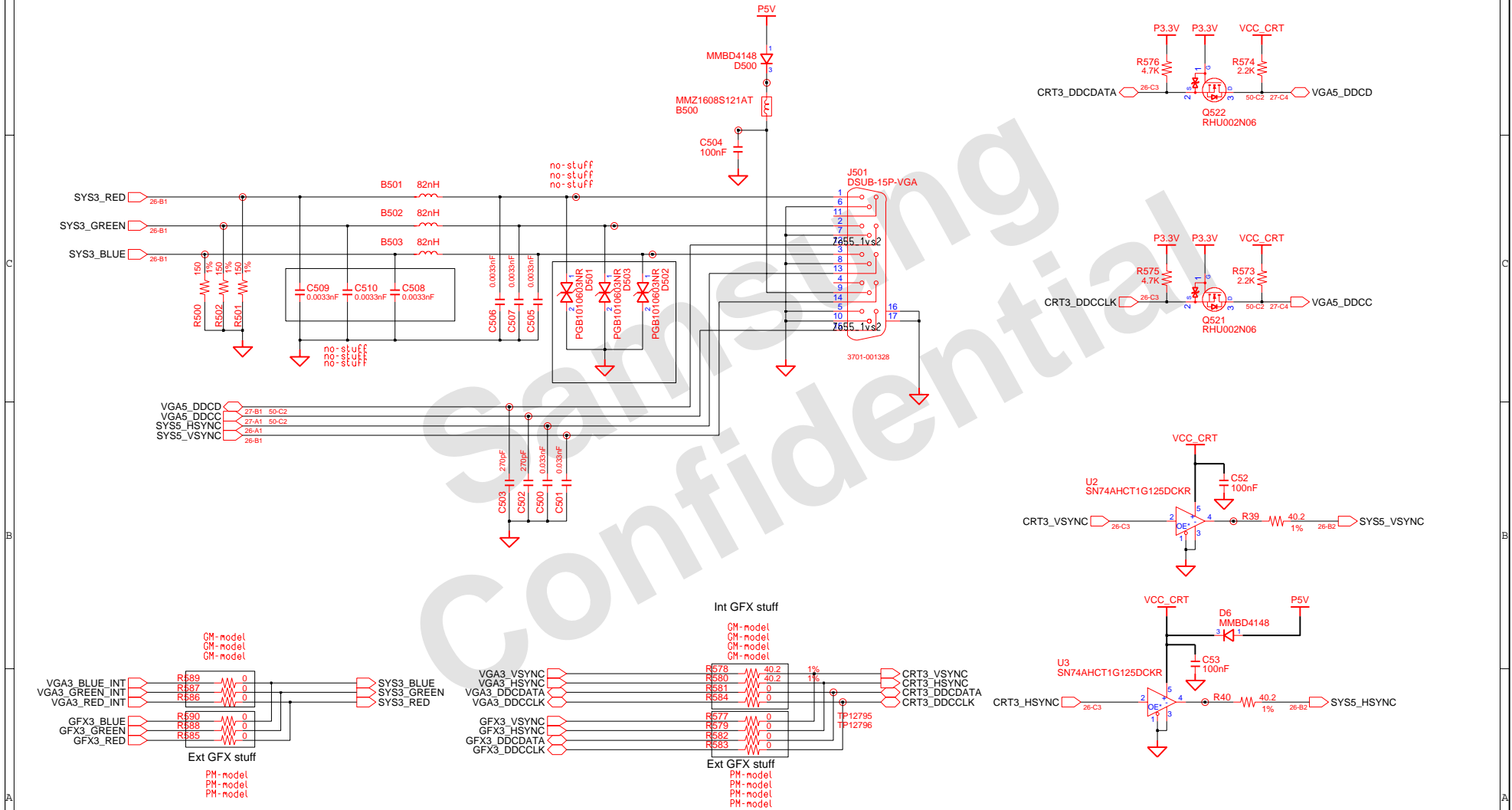
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DRAW	Y00, BW	DATE	4/8/2006	TITLE	HAINAN C	SAMSUNG ELECTRONICS
CHECK	BAIK, SS	DEV. STEP	DV	LCD Connector		
APPROVAL	BIN, KK	REV	1.0			PART NO. BA41-####A
MODULE CODE	undefined	LAST EDIT	April, 13, 2006 5:15:16 PM	PAGE	25	OF 50

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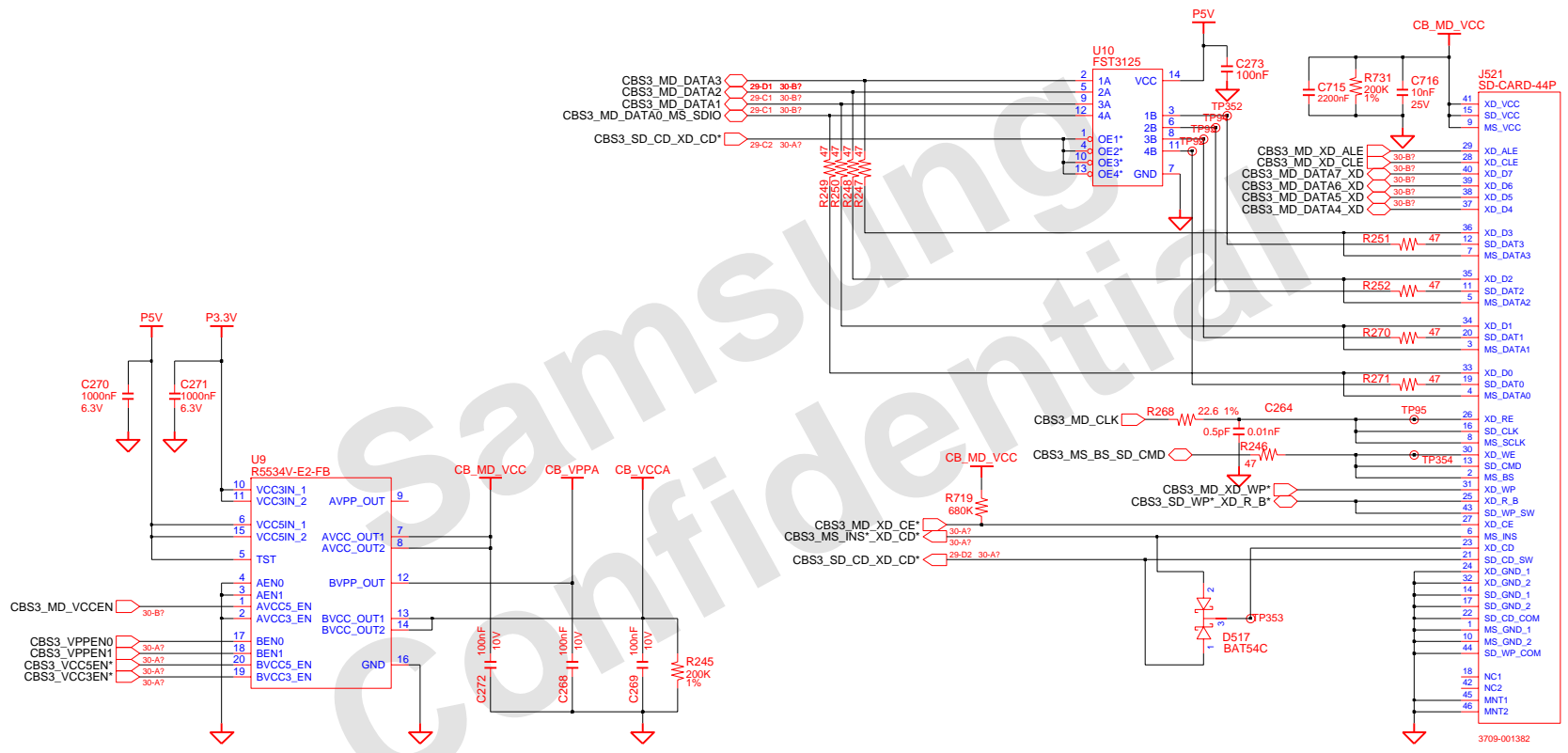
CRT CONNECTOR



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CHECK	BAIK, SS	DEV. STEP	DV			
APPROVAL	BIN, KK	REV	1.0			PART NO. BA41-####A
MODULE CODE	undefined	LAST EDIT	April, 13, 2006 5:15:34 PM	PAGE	26	OF 50

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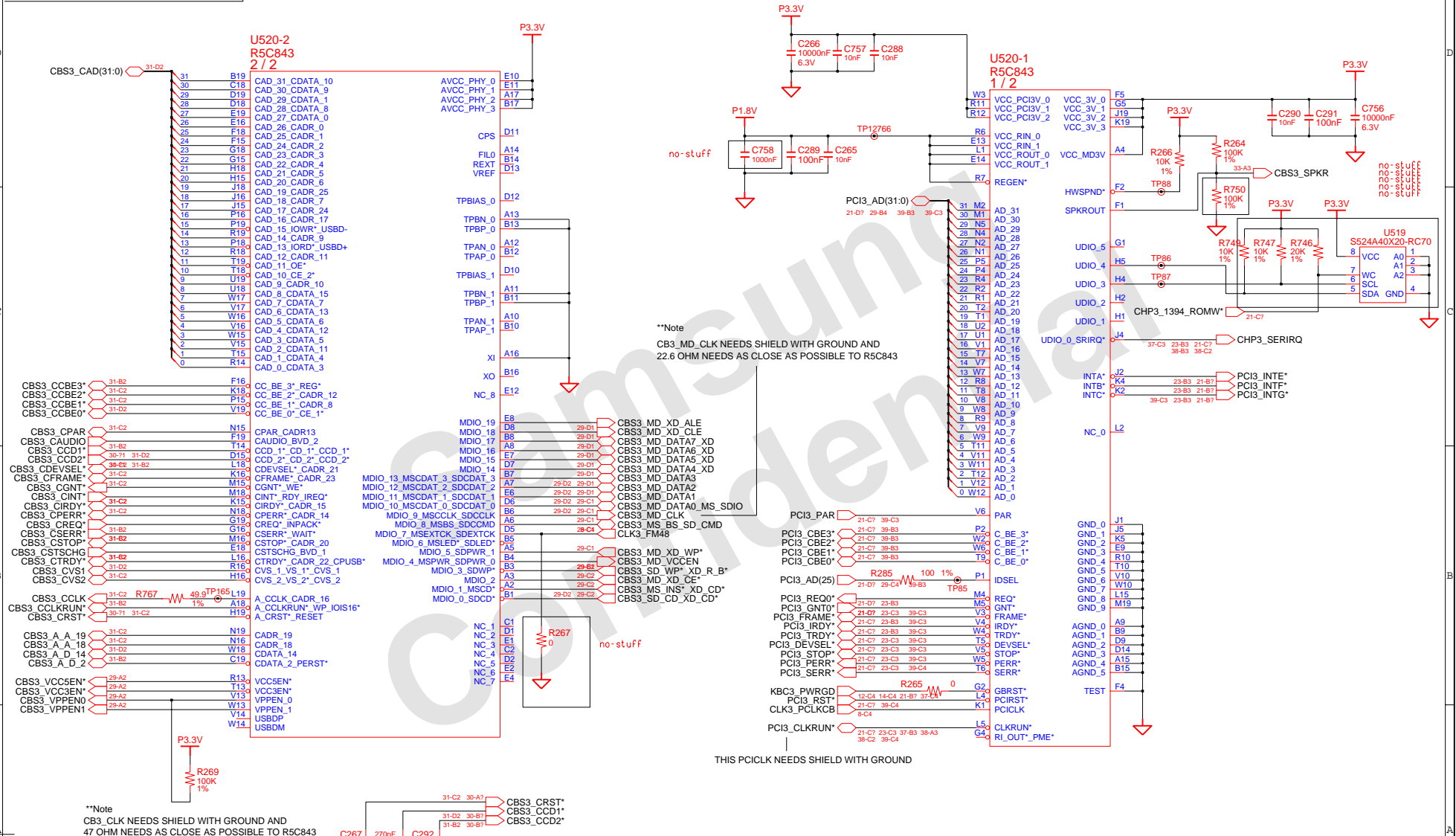
5in1 Socket



DRAW	Y00, BW	DATE	4/8/2006	TITLE	HAINAN C POWER	SAMSUNG ELECTRONICS
CHECK	BAIK, SS	DEV. STEP	DV	CARDBUS Controller (1/2)		
APPROVAL	BIN, KK	REV	1.0	LAST EDIT		PART NO. BA41-####A
MODULE CODE	undefined	LAST EDIT		April, 13, 2006 5:15:45 PM	PAGE	27 OF 50

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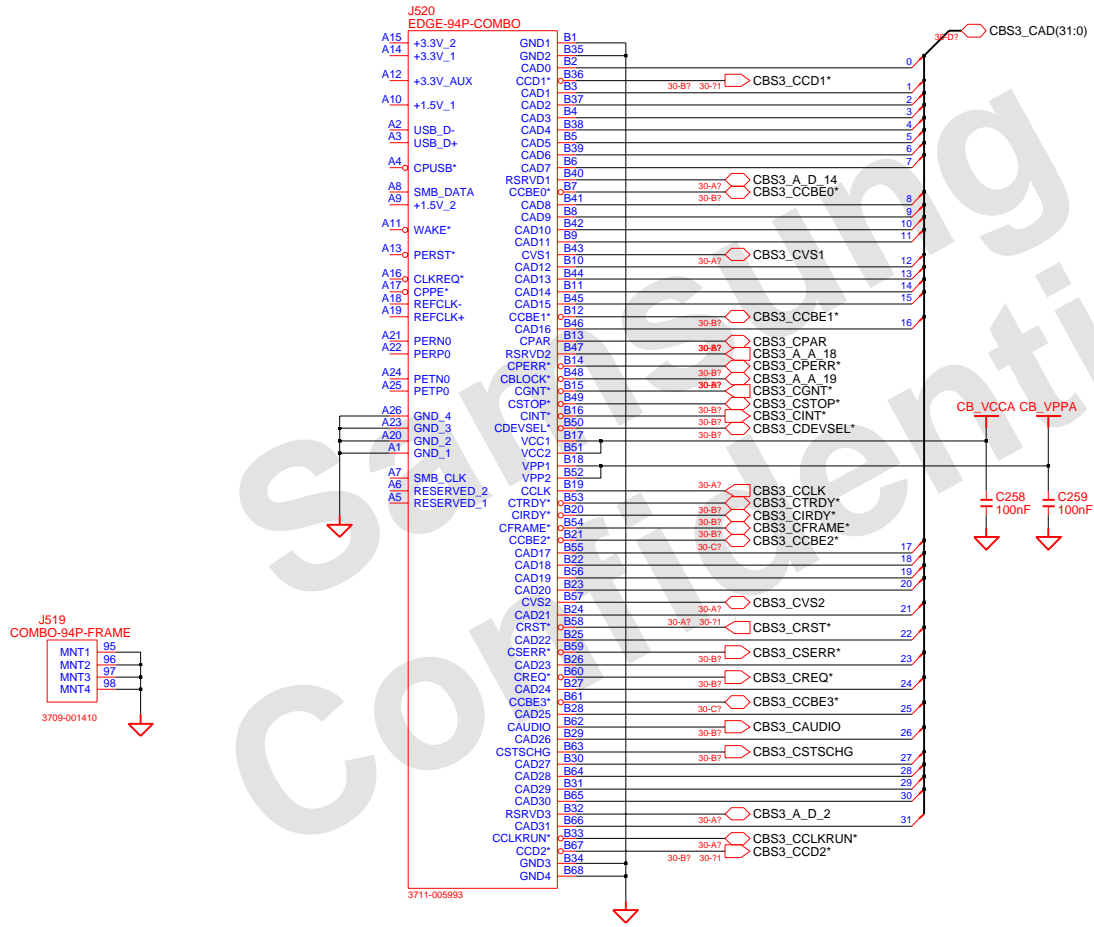
CARDBUS Controller



DRAW	Y00, BW	DATE	4/8/2006	TITLE	HAINAN C MAIN	SAMSUNG ELECTRONICS
CHECK	BAIK, SS	REV. STEP	DV	CARDBUS Controller (1/2)		
APPROVAL	BIN, KK	REV	1.0	PART NO. BA41-#####		
MODULE CODE	undefined	LAST EDIT	April, 13, 2006 5:15:56 PM	PAGE	28	OF 50

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PCMCIA / EXPRESS CARD Connector

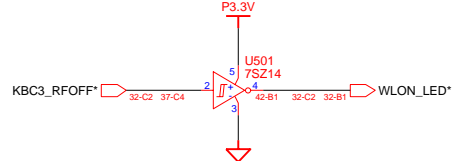
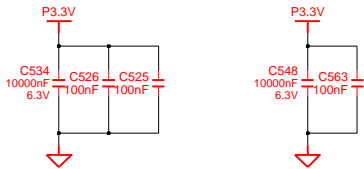
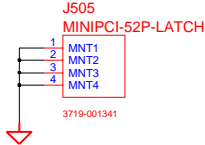
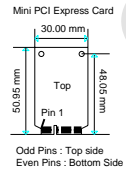
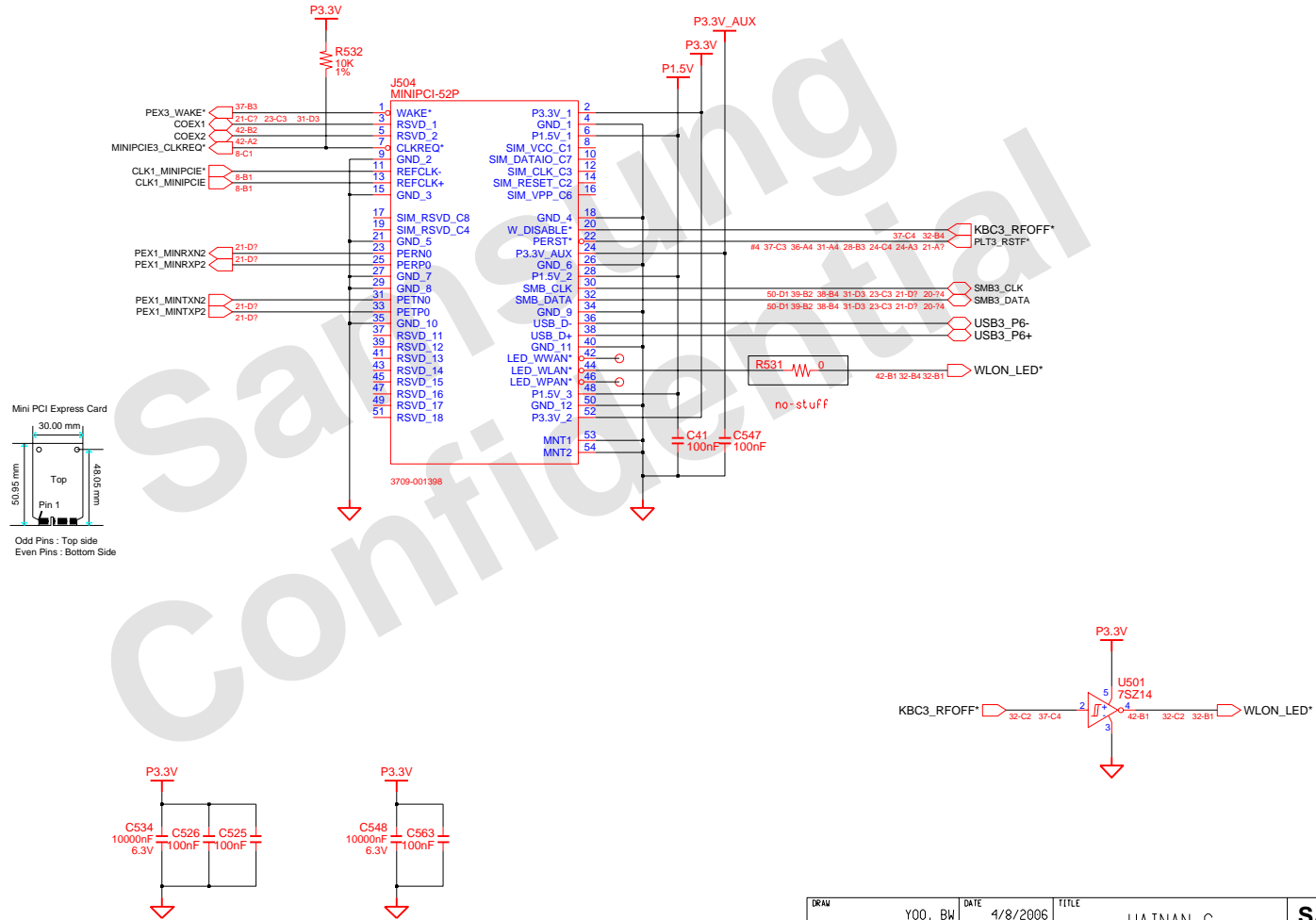


DRAW	Y00, BW	DATE	4/8/2006	TITLE	HAINAN C	SAMSUNG ELECTRONICS
CHECK	BAIK, SS	DEV. STEP	DV	POWER		
APPROVAL	BIN, KK	REV	1.0	PCMCIA/EXPRESS Connector	PART NO.	BA41-####A
MODULE CODE	undefined	LAST EDIT	April, 13, 2006 5:16:07 PM	PAGE	29	OF 50

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PCI Express Mini Card

PCI Express Mini Card ElectroMechanical Spec. 1.0



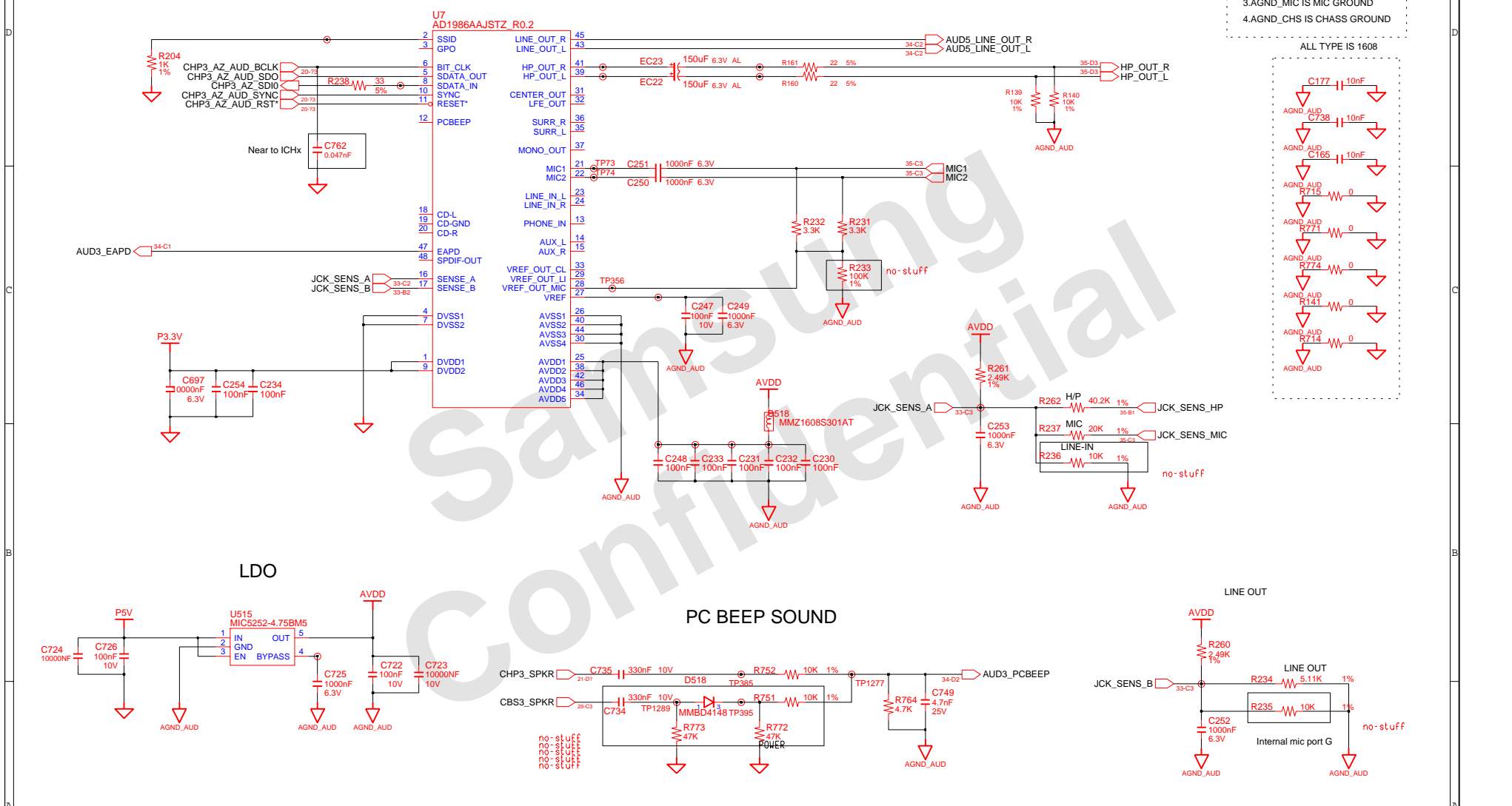
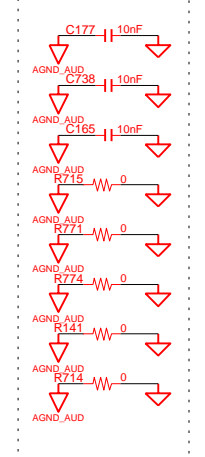
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CHECK	BAIK, SS	DEV. STEP	DV	MAIN		
APPROVAL	BIN, KK	REV	1.0	MINI Card (WLAN) & DMB	PART NO.	BA41-####A
MODULE CODE	undefined	LAST EDIT	April, 13, 2006 5:17:05 PM	PAGE	31	OF 50

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AUDIO CODEC

1. AGND_AUD IS AUDIO GROUND
2. GND IS DIGITAL GROUND
3. AGND_MIC IS MIC GROUND
4. AGND_CHS IS CHASSIS GROUND

ALL TYPE IS 1608



LDO

PC BEEP SOUND

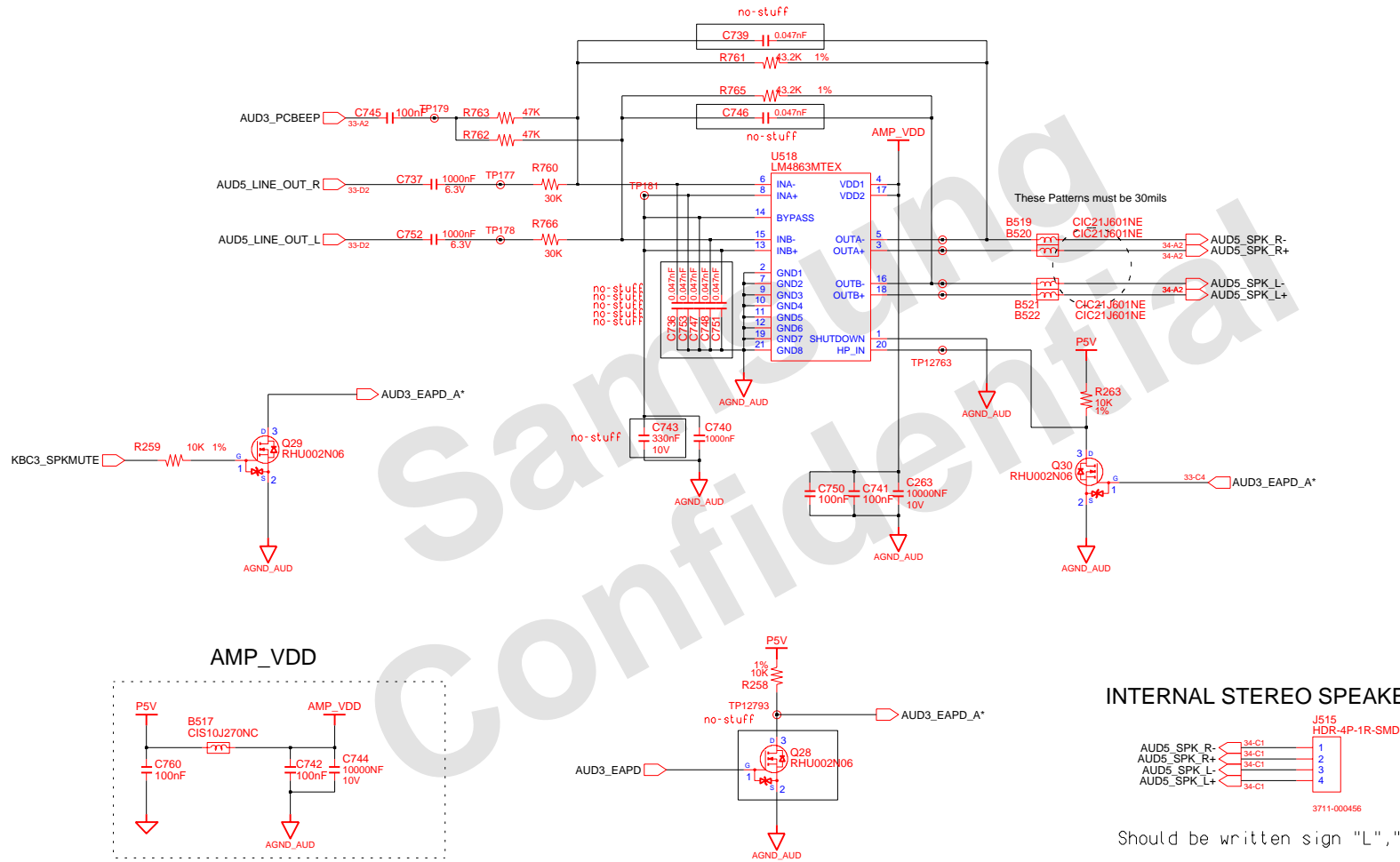
LINE OUT

DRAW	Y00, BW	DATE	4/8/2006	TITLE	HAINAN C MAIN AUDIO CODEC	SAMSUNG ELECTRONICS PART NO. BA41-####A
CHECK	BAIK, SS	DEV. STEP	DV			
APPROVAL	BIN, KK	REV	1.0			
MODULE CODE	undefined	LAST EDIT	Apr 13, 2006 5:17:16 PM	PAGE	32 OF 50	

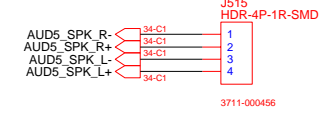
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AUDIO AMP



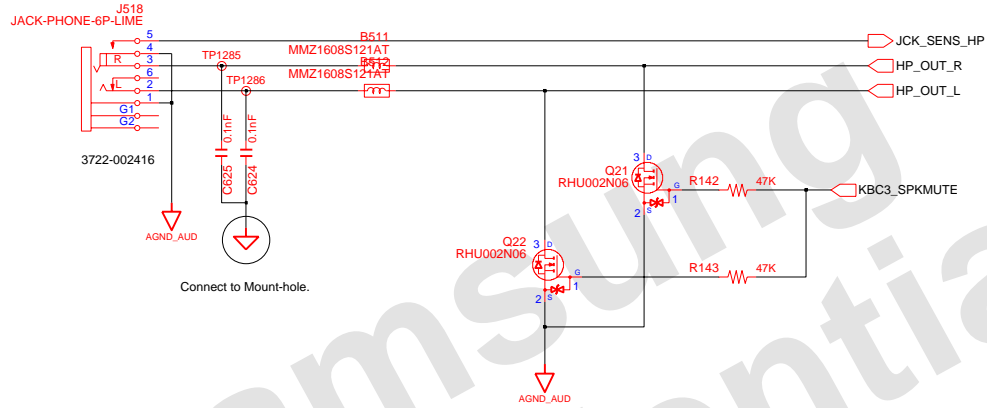
INTERNAL STEREO SPEAKERS



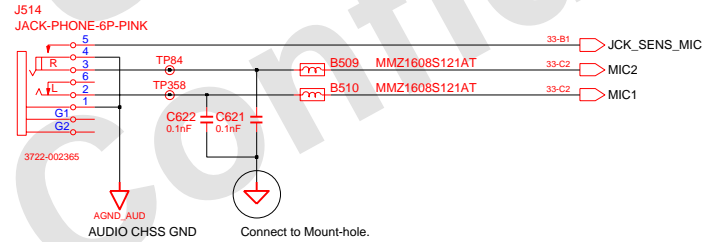
DRAW	Y00, BW	DATE	4/8/2006	TITLE	HAINAN C MAIN AUDIO AMP	SAMSUNG ELECTRONICS PART NO. BA41-####A
CHECK	BAIK, SS	DEV. STEP	DV			
APPROVAL	BIN, KK	REV	1.0			
MODULE CODE	undefined	LAST EDIT	April, 13, 2006 5:17:25 PM	PAGE	33 OF 50	

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HEADPHONE



MIC JACK

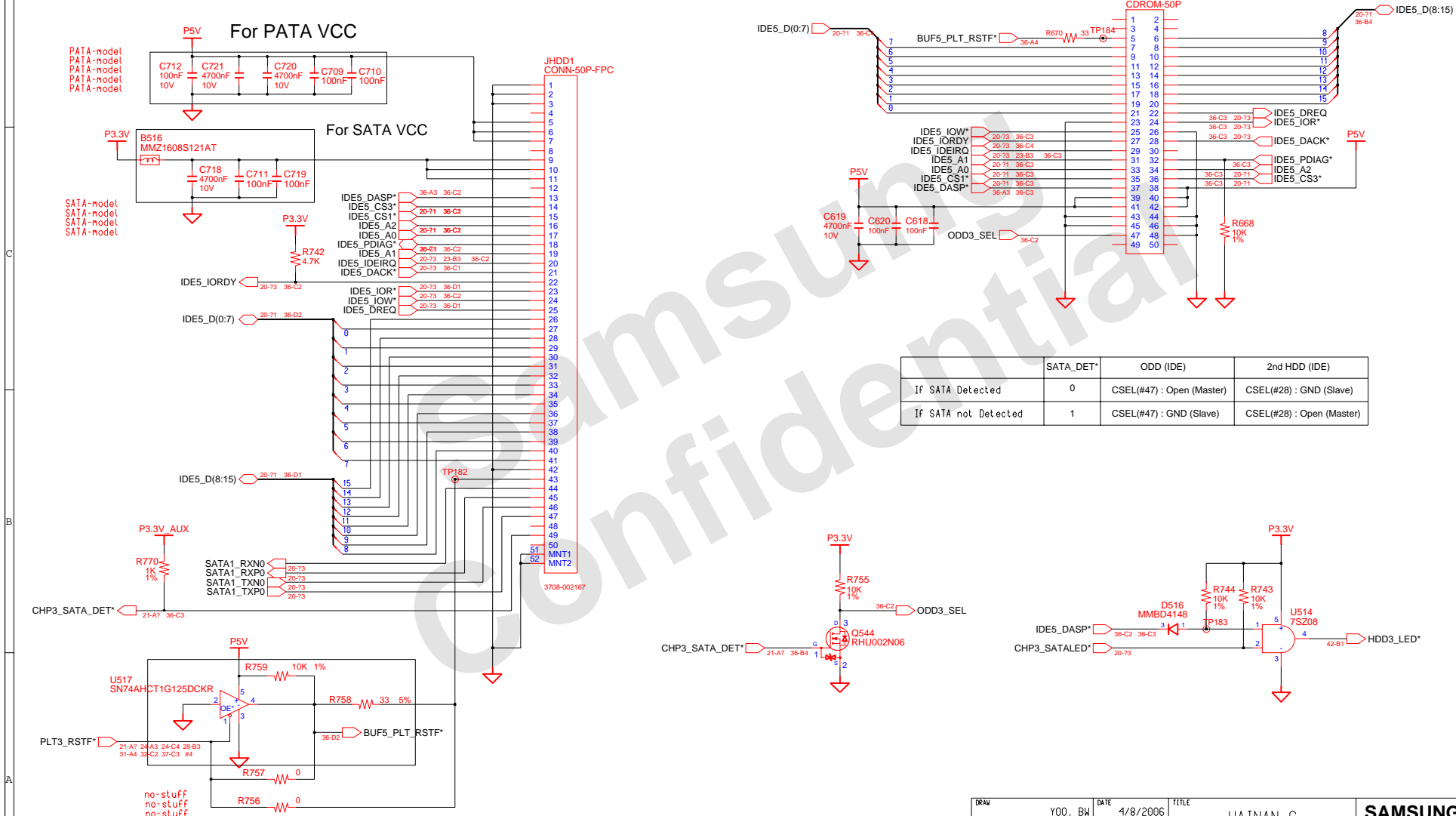


DRAW	Y00, BW	DATE	4/8/2006	TITLE	HAINAN C	SAMSUNG ELECTRONICS
CHECK	BAIK, SS	DEV. STEP	DV	MAIN		
APPROVAL	BIN, KK	REV	1.0	Headphone & MIC Jack	PART NO.	BA41-####A
MODULE CODE	undefined	LAST EDIT	April, 13, 2006 5:17:46 PM	PAGE	34	OF 50

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Main to Swap B'd

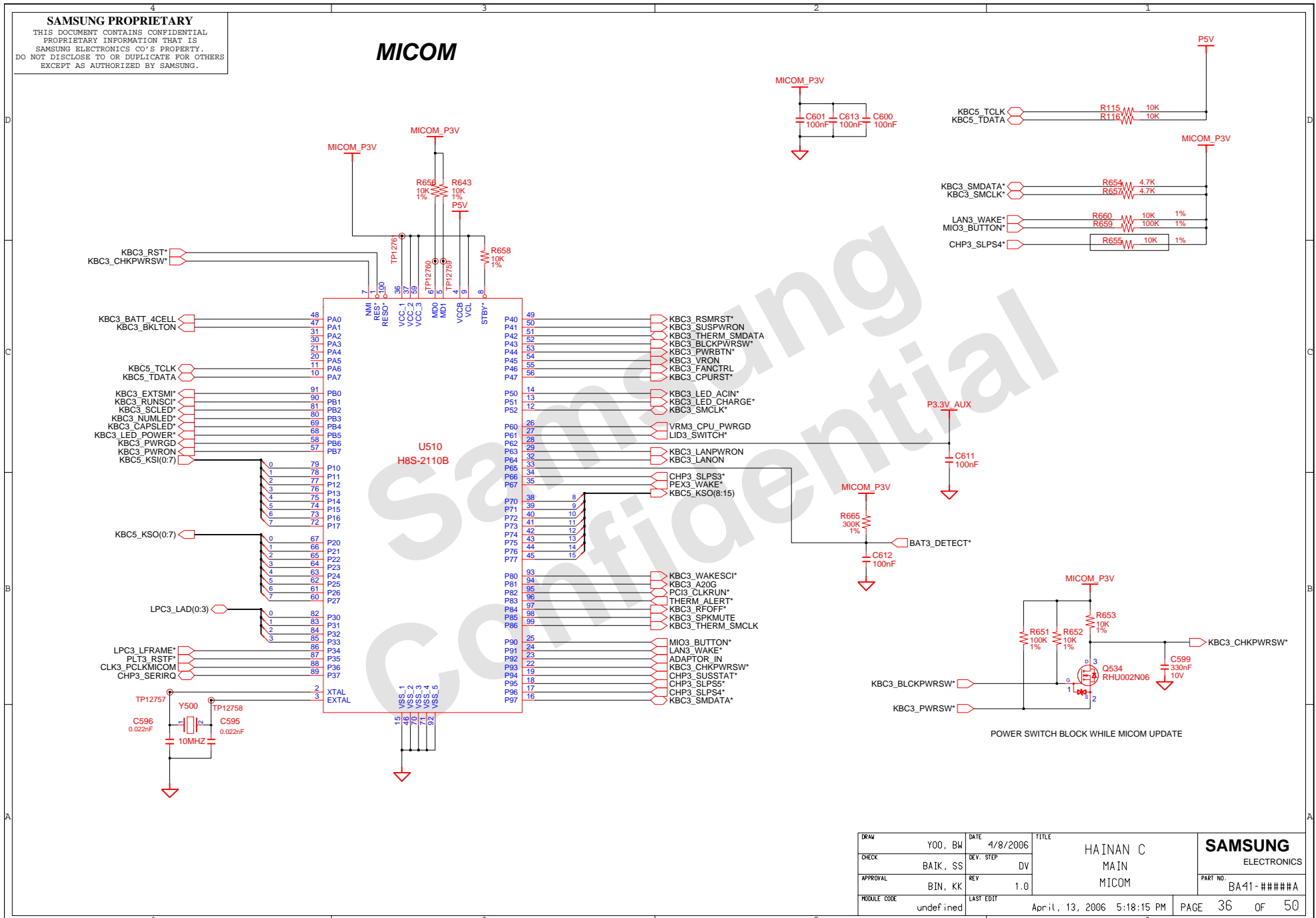
Main to HDD



	SATA_DET*	ODD (IDE)	2nd HDD (IDE)
If SATA Detected	0	CSEL(#47) : Open (Master)	CSEL(#28) : GND (Slave)
If SATA not Detected	1	CSEL(#47) : GND (Slave)	CSEL(#28) : Open (Master)

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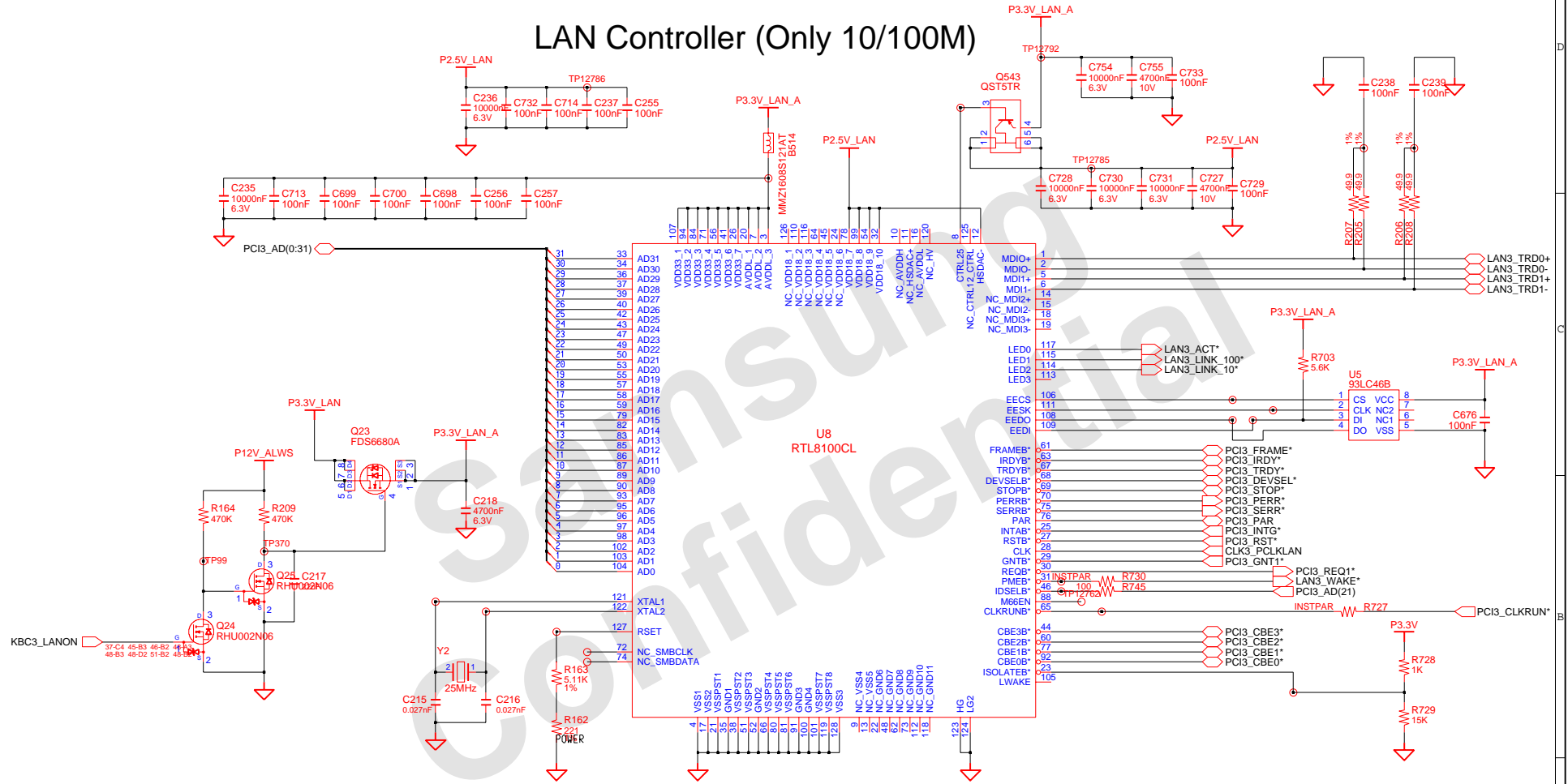
MICOM



DRAW	Y00, BW	DATE	4/8/2006	TITLE	HAINAN C	SAMSUNG ELECTRONICS
CHECK	BAIK, SS	DEV. STEP	DV	MAIN	MICOM	
APPROVAL	BIN, KK	REV	1.0			PART NO. BA41-####A
MODULE CODE	undefined	LAST EDIT	April, 13, 2006 5:18:15 PM	PAGE	36	OF 50

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LAN Controller (Only 10/100M)

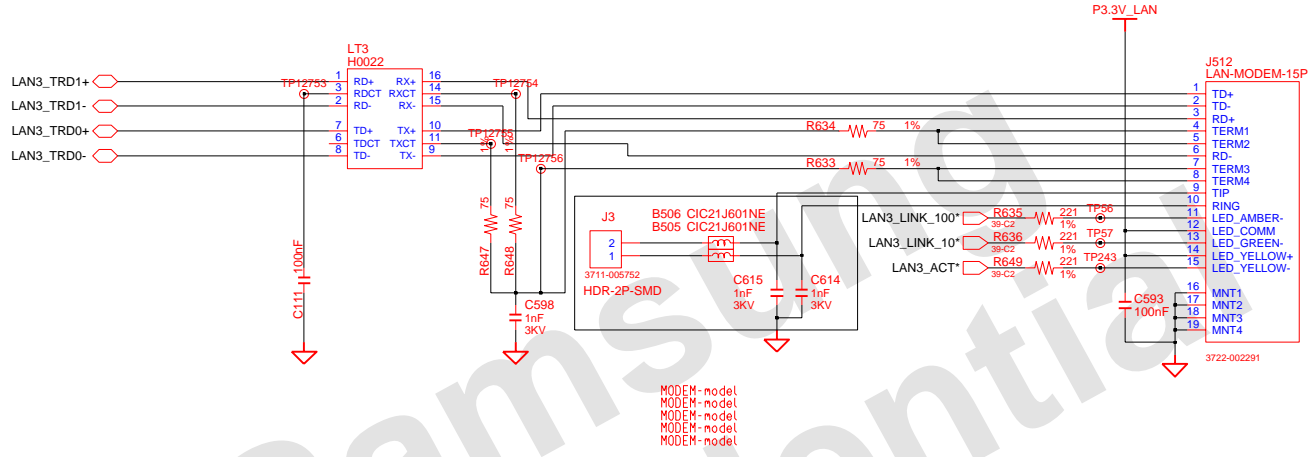


DRAW	Y00, BW	DATE	4/8/2006	TITLE	HAINAN C	SAMSUNG ELECTRONICS
CHECK	BAIK, SS	DEV. STEP	DV	MAIN		
APPROVAL	BIN, KK	REV	1.0	BCM 5751/4401 (1/2)		PART NO. BA41-####A
MODULE CODE	undefined	LAST EDIT	Apr 11, 2006 5:18:26 PM	PAGE	37	OF 50

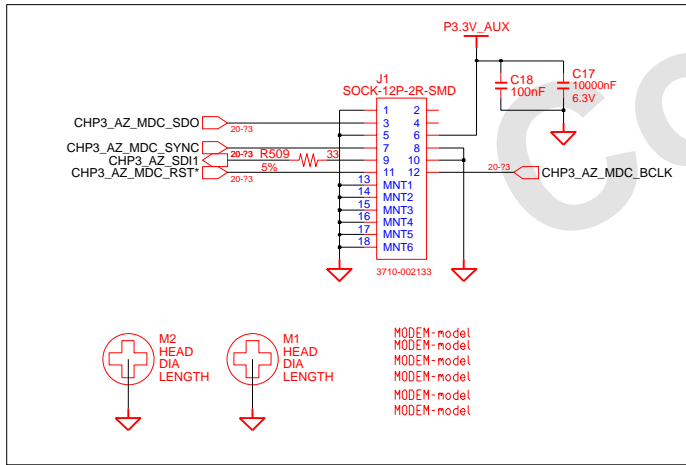
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LAN Transformer

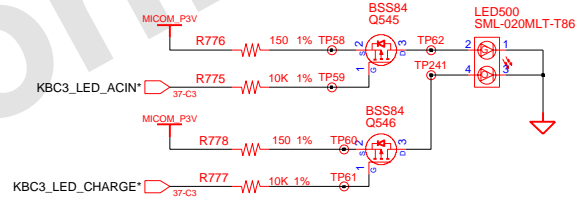
LAN Connector



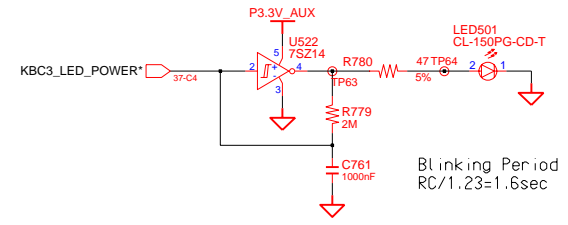
MDC Connector



ADAPTERIN/CHARGING LED



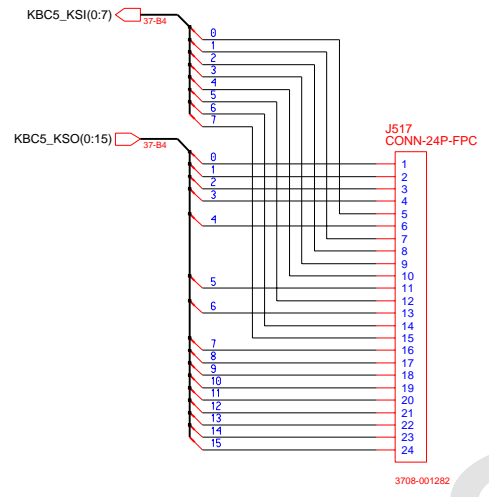
POWER_ON / LB LED



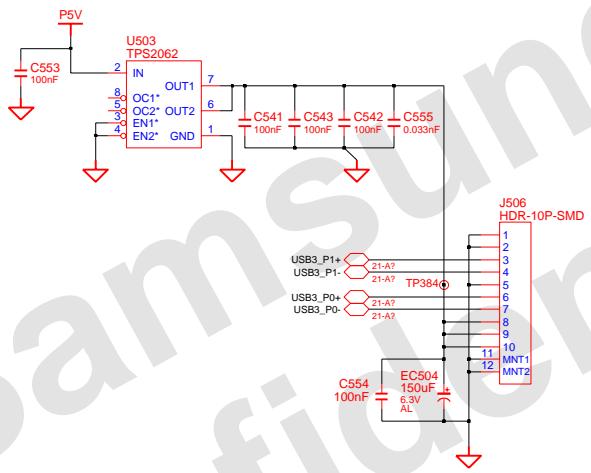
DRAW	Y00, BW	DATE	4/8/2006	TITLE	HAINAN C	SAMSUNG ELECTRONICS
CHECK	BAIK, SS	DEV. STEP	DV	MAIN		
APPROVAL	BIN, KK	REV	1.0	LAN / MODEM Conn & LED.	PART NO.	BA41-####A
MODULE CODE	undefined	LAST EDIT	April, 13, 2006 5:18:39 PM	PAGE	38	OF 50

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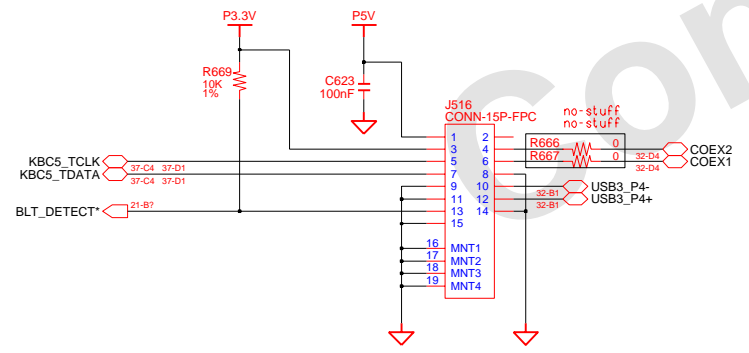
KEYBOARD



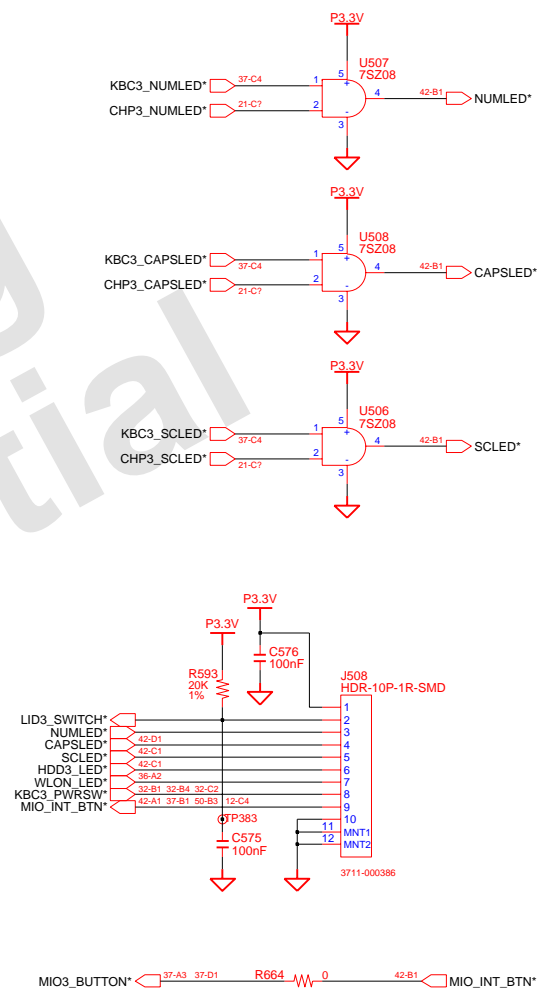
USB_I/F Connector



TOUCHPAD BLUETOOTH I/F



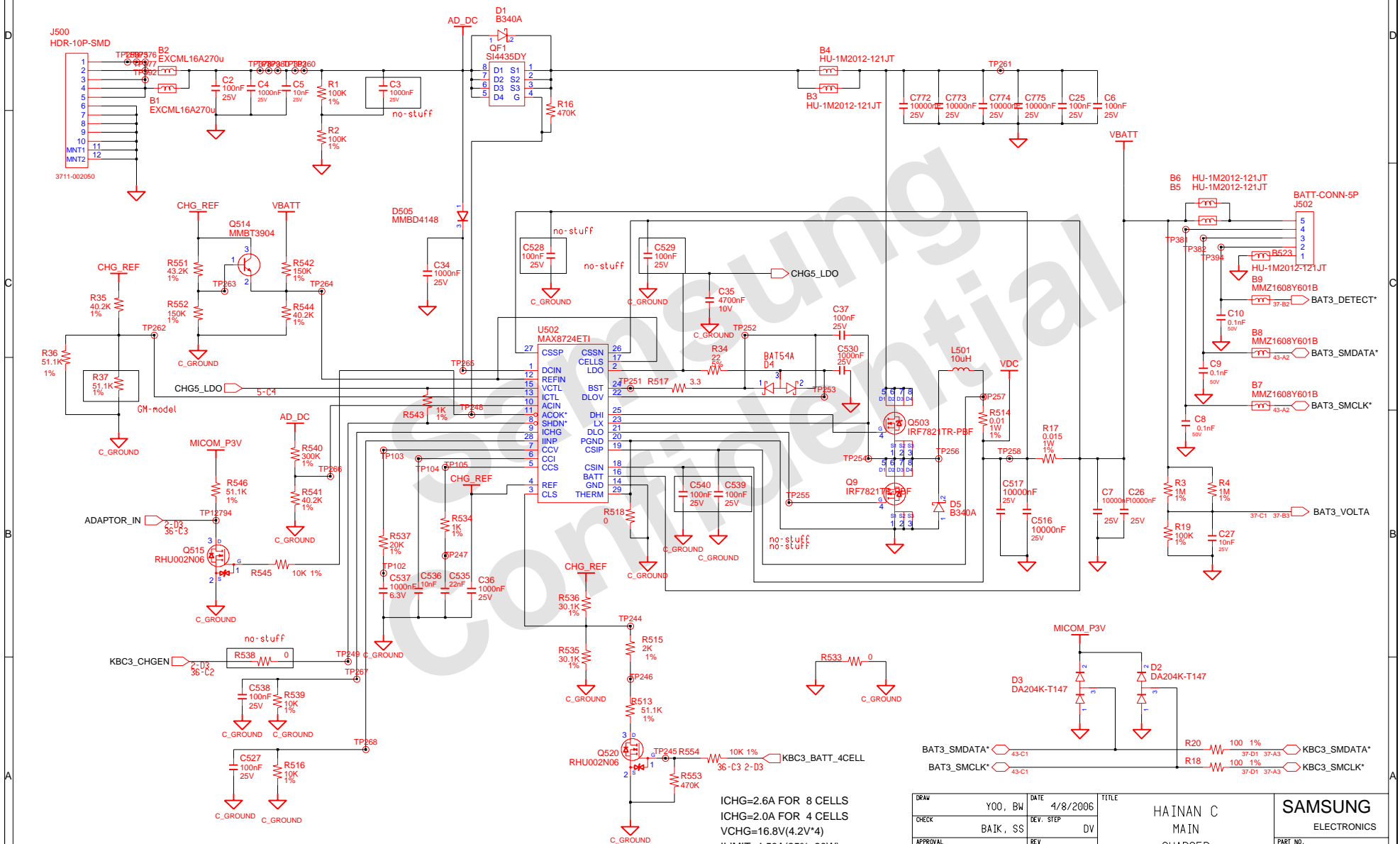
LED BOARD



DRAW	Y00, BW	DATE	4/8/2006	TITLE	HAINAN C	SAMSUNG ELECTRONICS
CHECK	BAIK, SS	DEV. STEP	DV	MAIN		
APPROVAL	BIN, KK	REV	1.0	SUB B'D CONNECTOR		PART NO. BA41-#####A
MODULE CODE	undefined	LAST EDIT	April, 13, 2006 5:19:12 PM	PAGE	39	OF 50

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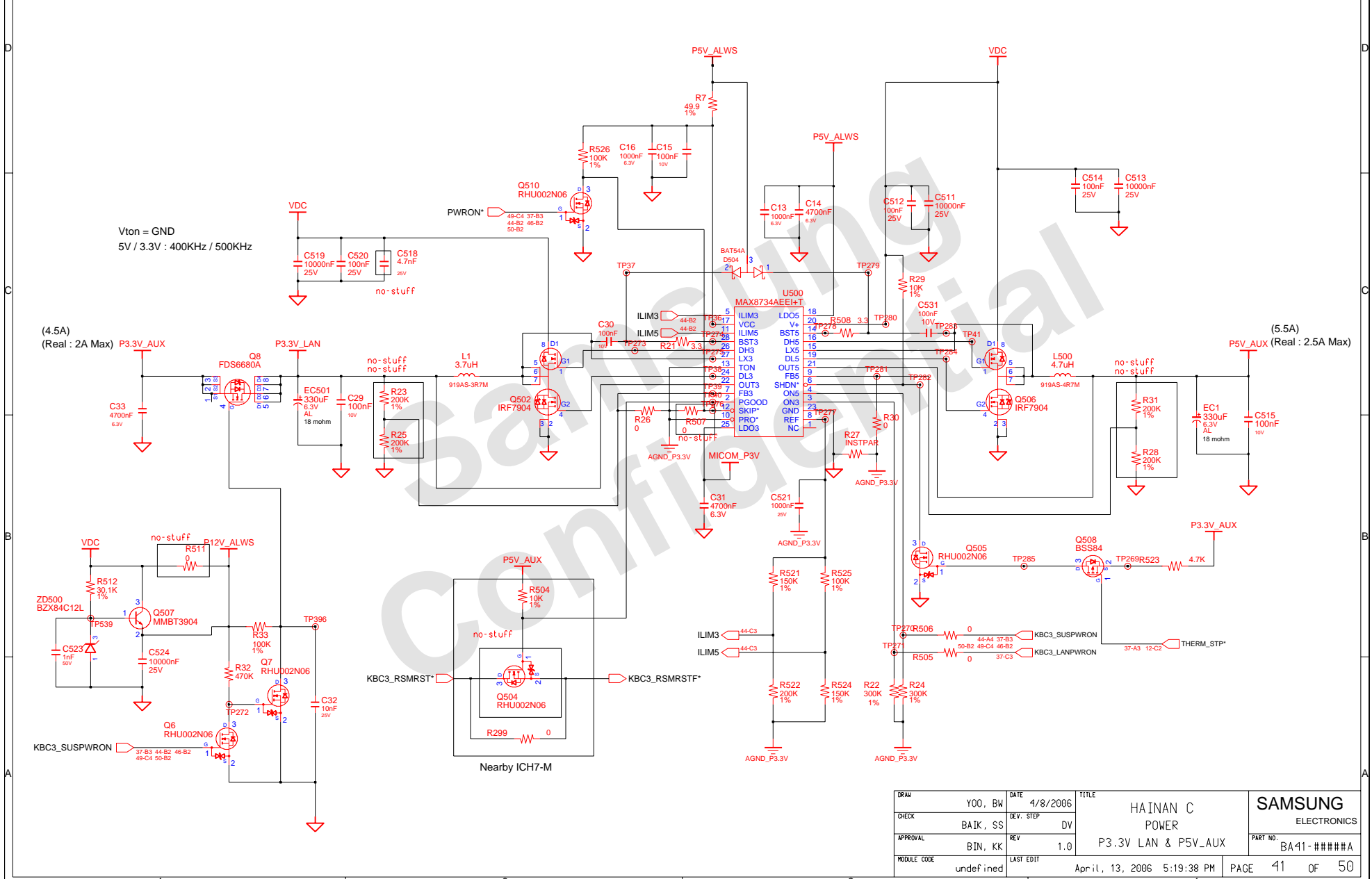
CHARGER & POWER MANAGEMENT



DRAW	Y00, BW	DATE	4/8/2006	TITLE	HAINAN C MAIN CHARGER	SAMSUNG ELECTRONICS
CHECK	BAJK, SS	REV. STEP	DV			
APPROVAL	BJN, KK	REV	1.0			PART NO. BA41-#####A
MODULE CODE	undefined	LAST EDIT	April, 13, 2006 5:19:26 PM	PAGE	40	OF 50

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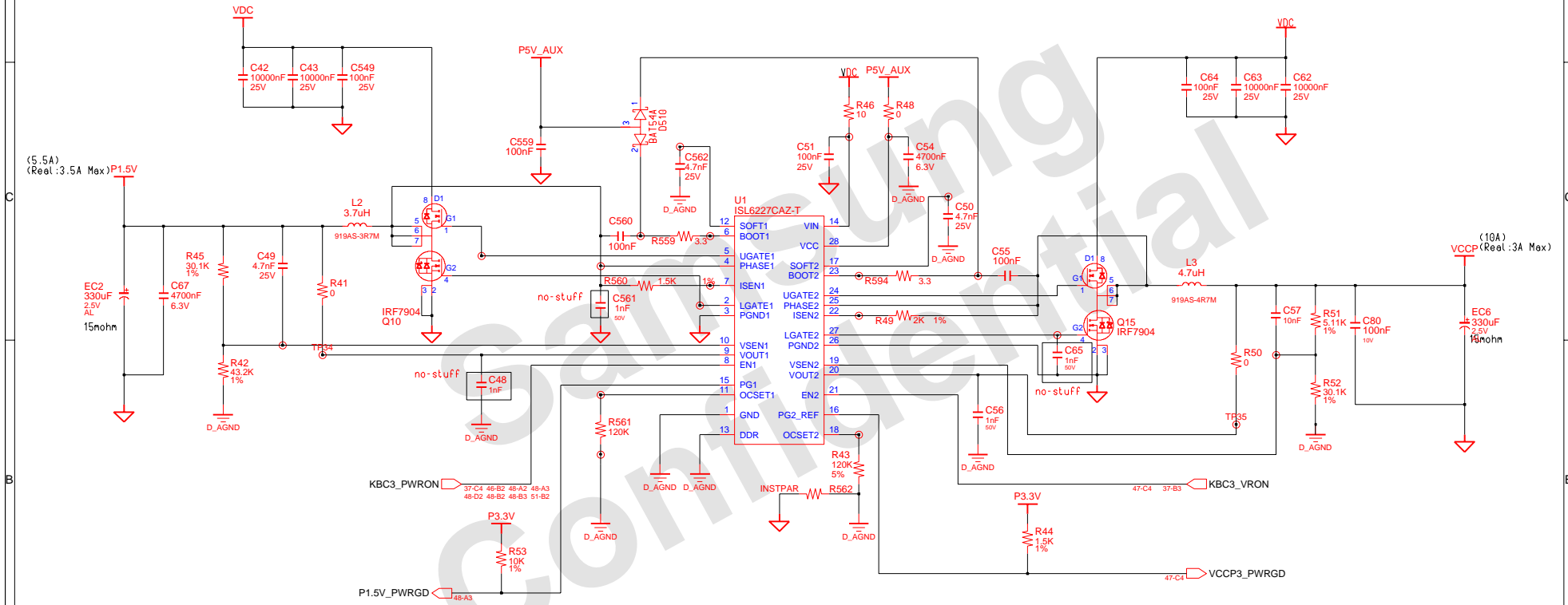
P3.3V_LAN/AUX & P5V_AUX



DRAW	Y00, BW	DATE	4/8/2006	TITLE	HAINAN C	SAMSUNG ELECTRONICS
CHECK	BAJK, SS	REV. STEP	DV	POWER		
APPROVAL	BIN, KK	REV	1.0	P3.3V LAN & P5V_AUX	PART NO.	BA41-#####A
MODULE CODE	undefined	LAST EDIT	April, 13, 2006 5:19:38 PM	PAGE	41	OF 50

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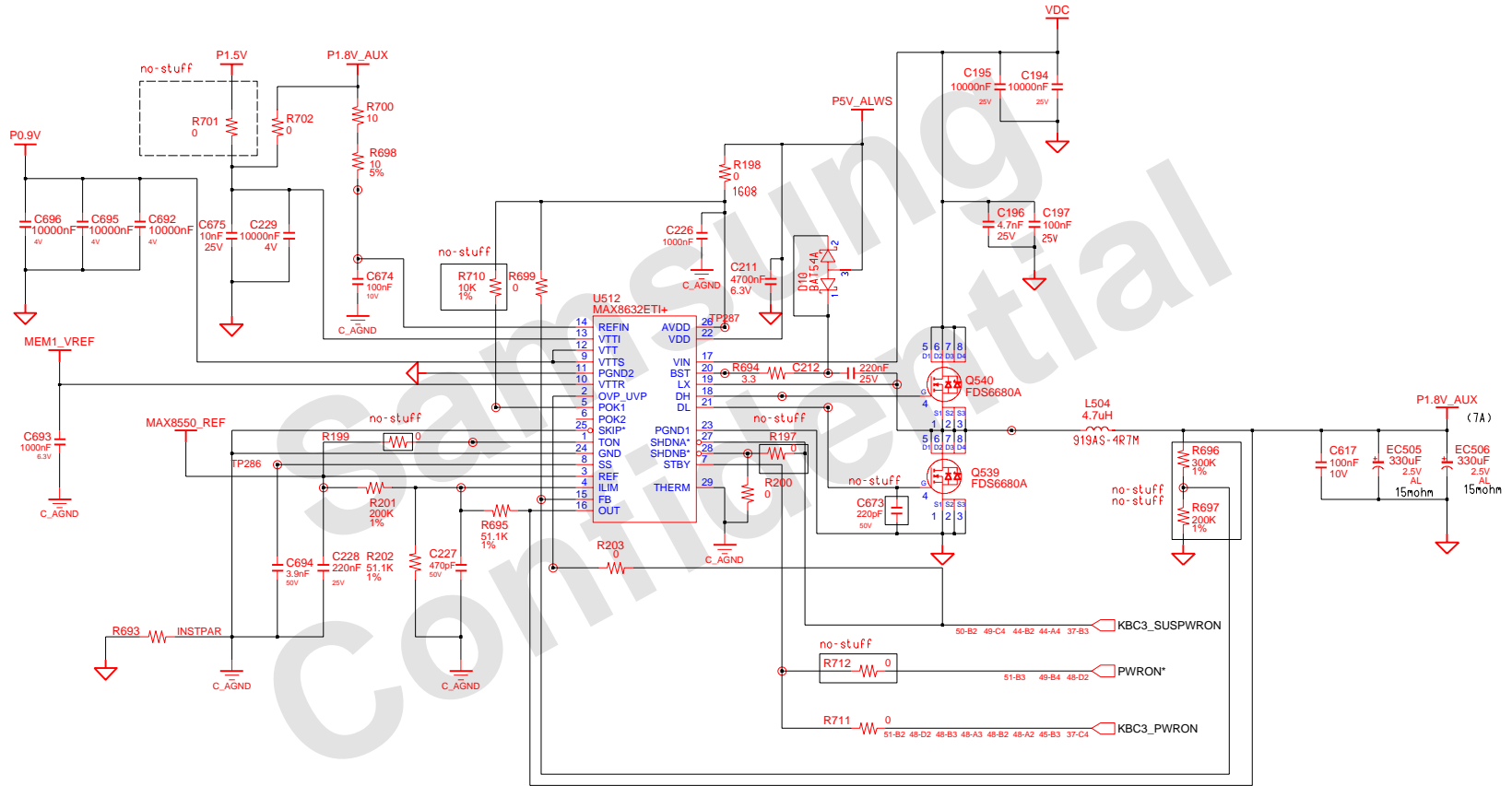
P1.5V & VCCP (1.05V)



DRAW	Y00, BW	DATE	4/8/2006	TITLE	HAINAN C POWER P1.5V & VCCP	SAMSUNG ELECTRONICS
CHECK	BAJK, SS	DEV. STEP	DV			
APPROVAL	BIN, KK	REV	1.0			PART NO. BA41-#####A
MODULE CODE	undefined	LAST EDIT	April, 13, 2006 5:19:58 PM	PAGE	42	OF 50

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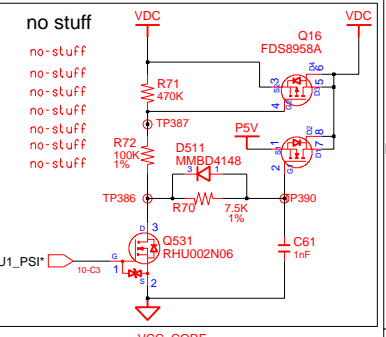
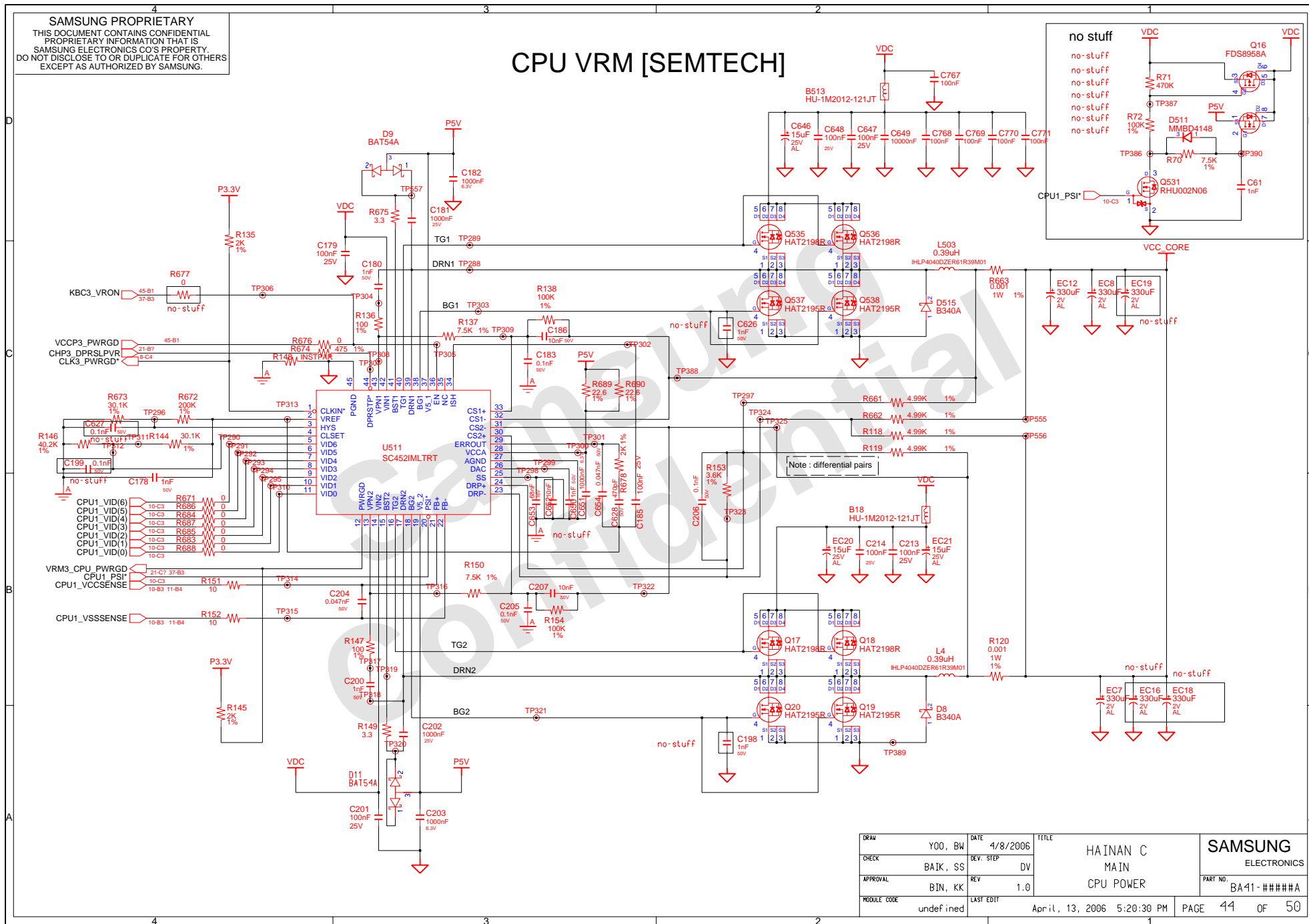
DDR2 Power



DRAW	Y00, BW	DATE	4/8/2006	TITLE	HAINAN C MAIN DDR2 POWER	SAMSUNG ELECTRONICS PART NO. BA41-####A
CHECK	BAIK, SS	DEV. STEP	DV			
APPROVAL	BIN, KK	REV	1.0			
MODULE CODE	undefined	LAST EDIT	April, 13, 2006 5:20:19 PM	PAGE	43	OF 50

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CPU VRM [SEMTECH]

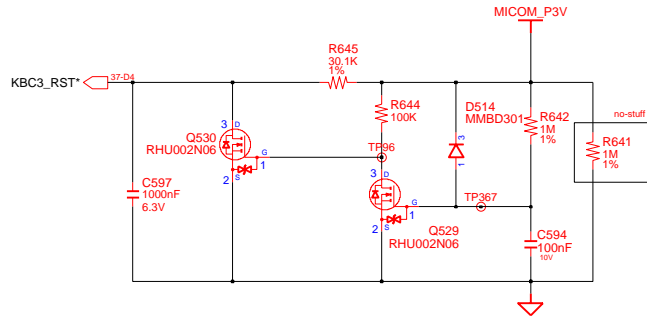


Note: differential pairs

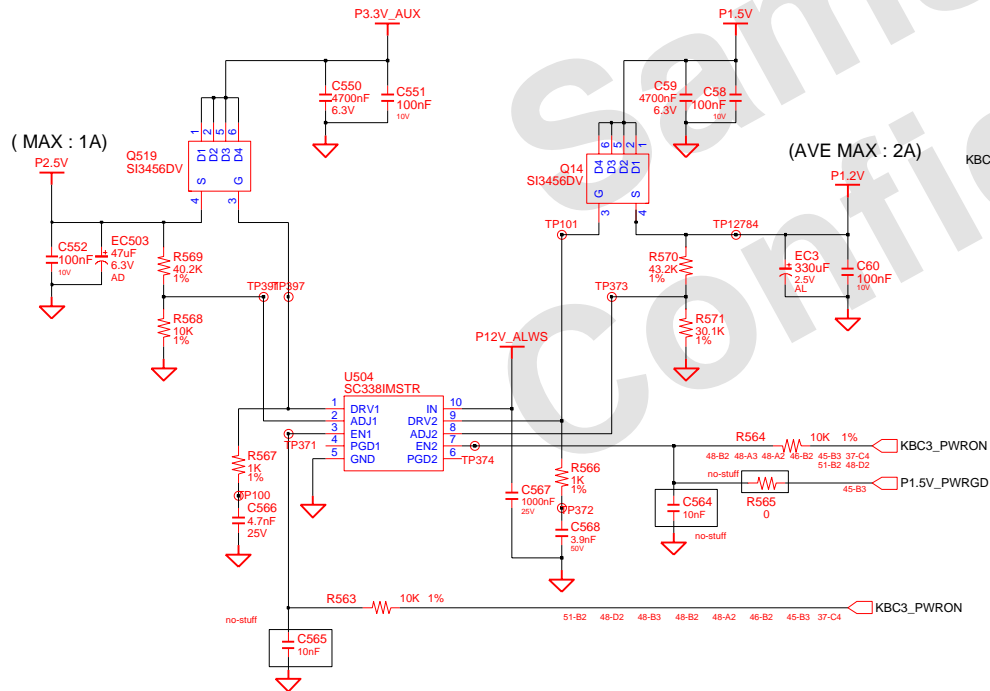
DRAW	Y00, BW	DATE	4/8/2006	TITLE	HAINAN C	SAMSUNG ELECTRONICS PART NO. BA41-####A
CHECK	BAIK, SS	REV. STEP	DV	MAIN	CPU POWER	
APPROVAL	BIN, KK	REV	1.0			
MODULE CODE	undefined	LAST EDIT	April, 13, 2006 5:20:30 PM	PAGE	44 OF 50	

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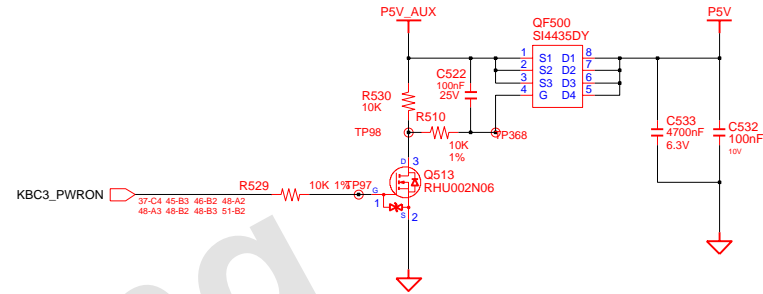
MICOM RESET



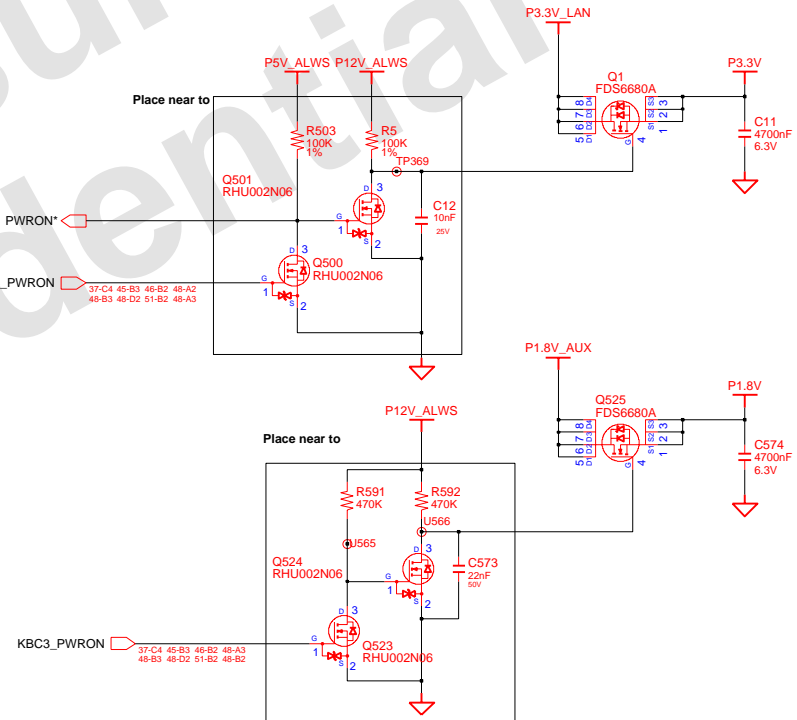
P1.2V / P2.5V POWER



Switched Power On (P5V)

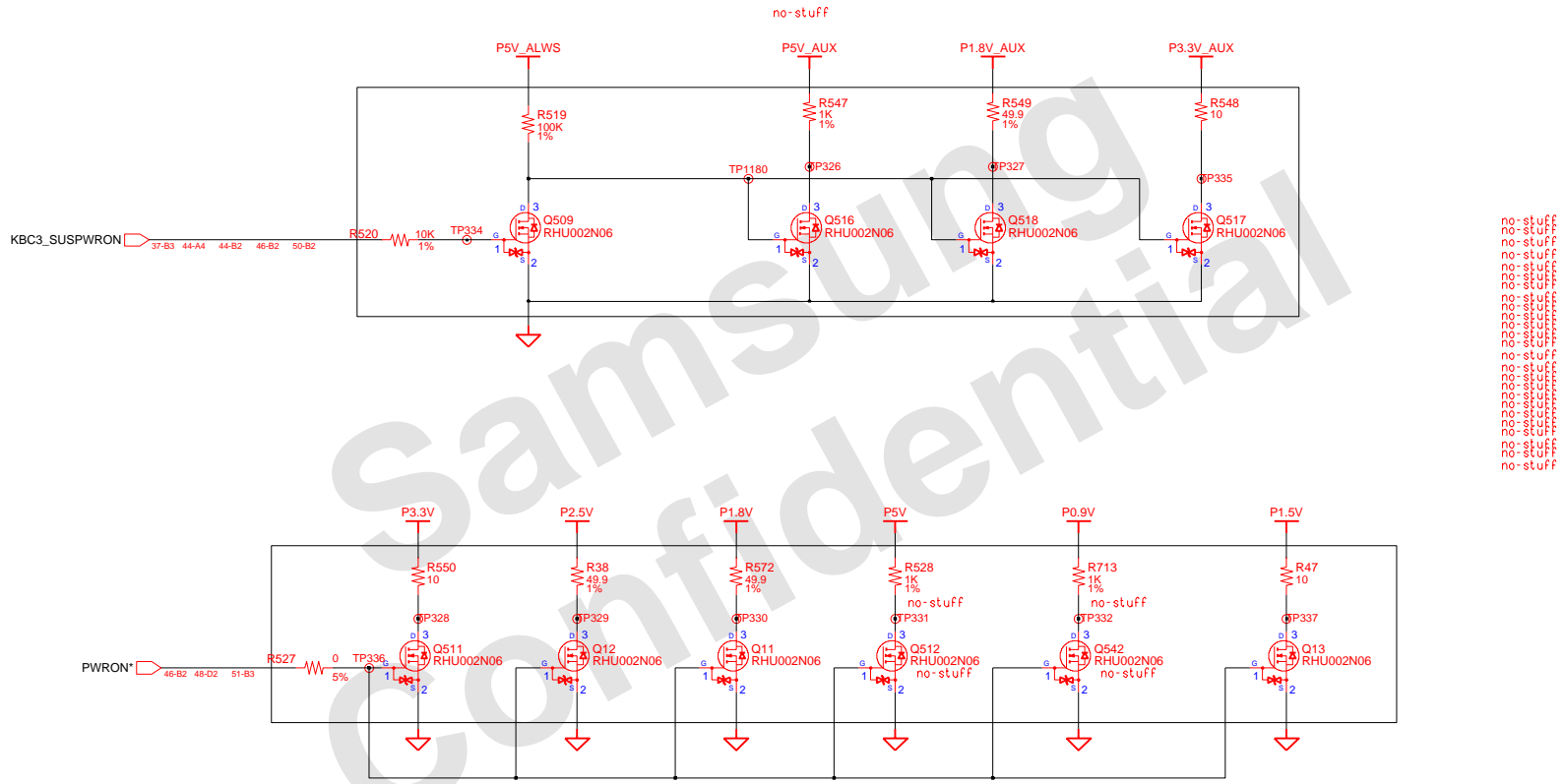


Switched Power On (P3.3V & 1.8V)



DATE	4/8/2006	TITLE	HAINAN C MAIN	SAMSUNG ELECTRONICS
DEV. STEP	DV	MICOM & SWITCHED POWER		
REV	1.0	PART NO. BA41-#####		PAGE 45 OF 50
LAST EDIT	April, 13, 2006 5:20:41 PM			

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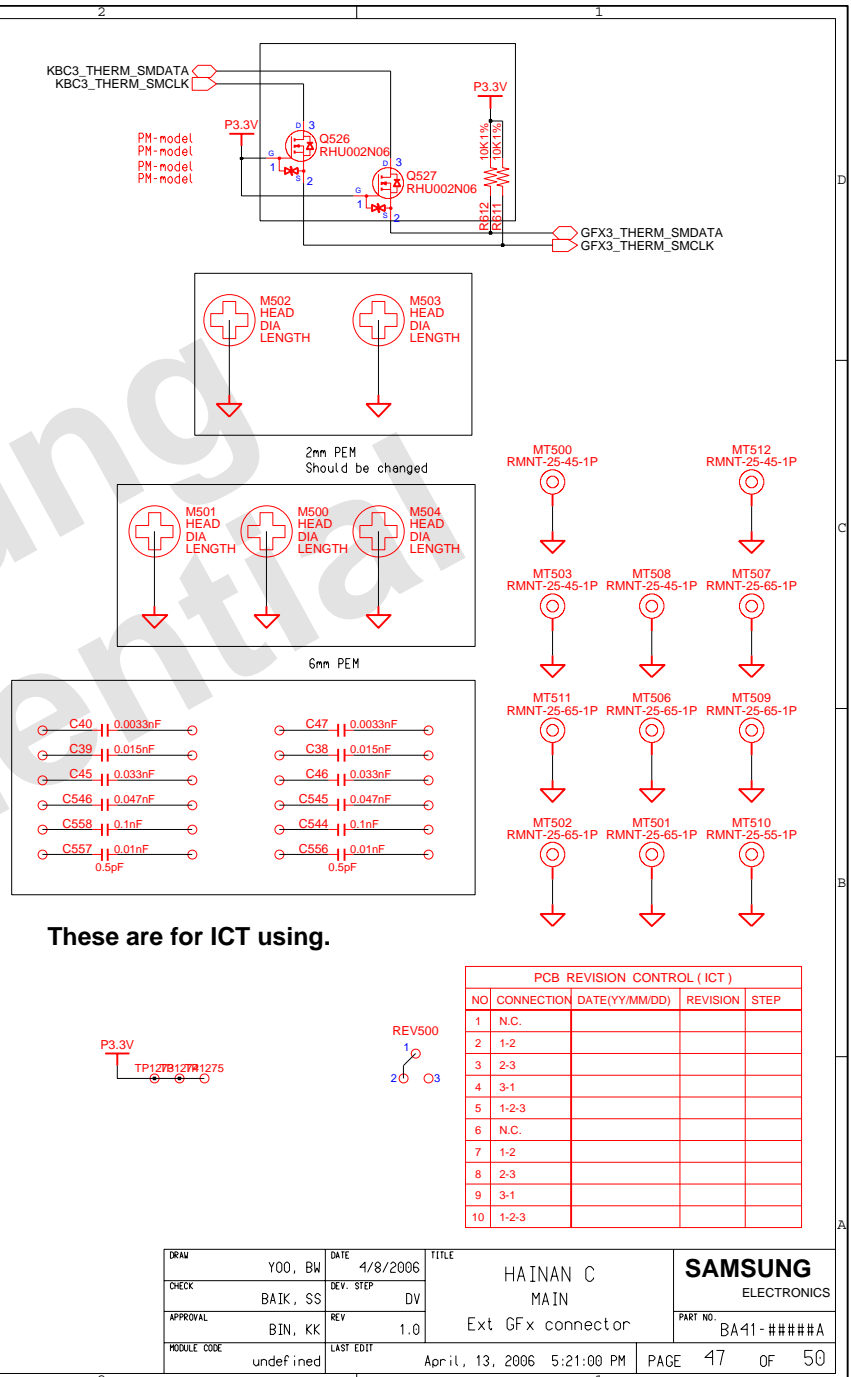
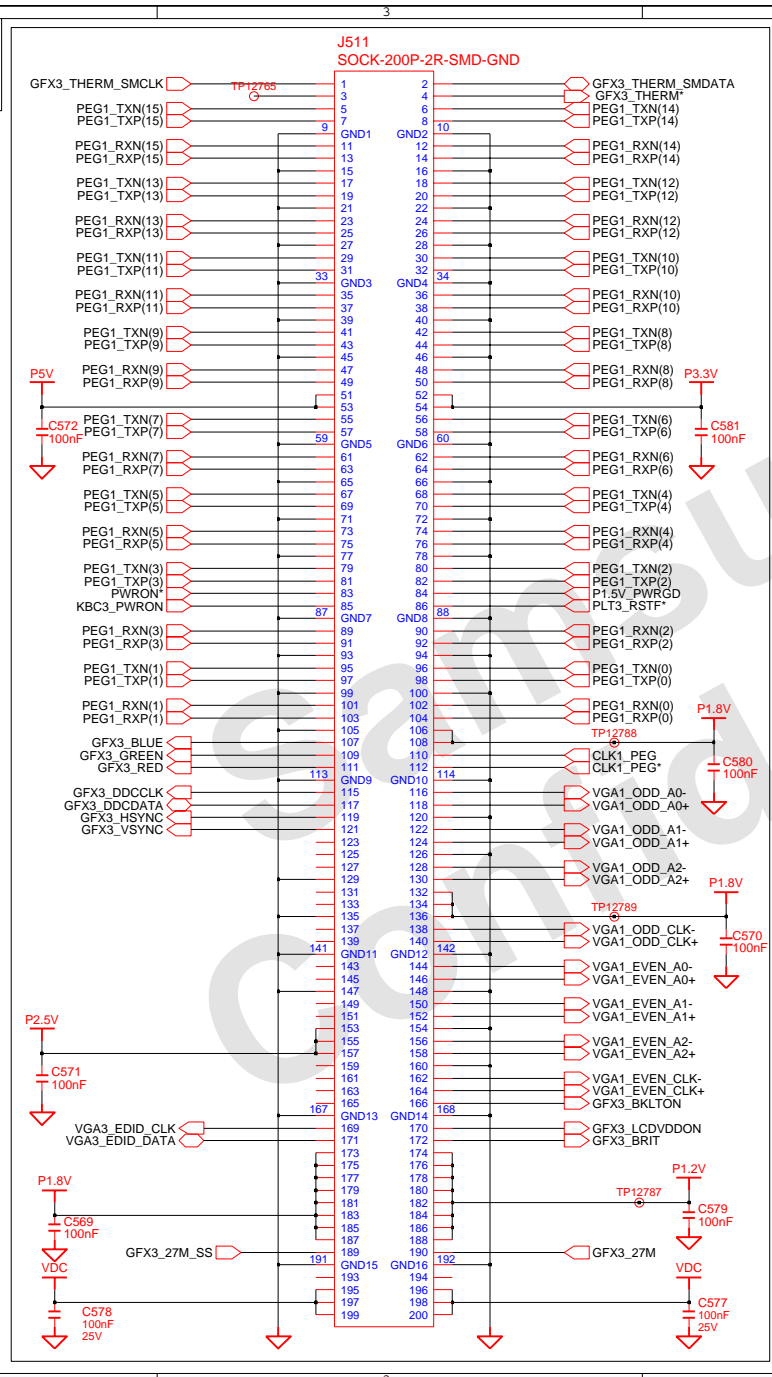


no-stuff
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DRW	Y00, BW	DATE	4/8/2006	TITLE	HAINAN C	SAMSUNG ELECTRONICS
CHECK	BAIK, SS	DEV. STEP	DV	GFX POWER		
APPROVAL	BIN, KK	REV	1.0	Discharging Logic		PART NO.
MODULE CODE	undefined	LAST EDIT	April, 13, 2006 5:20:51 PM	PAGE	46	OF 50

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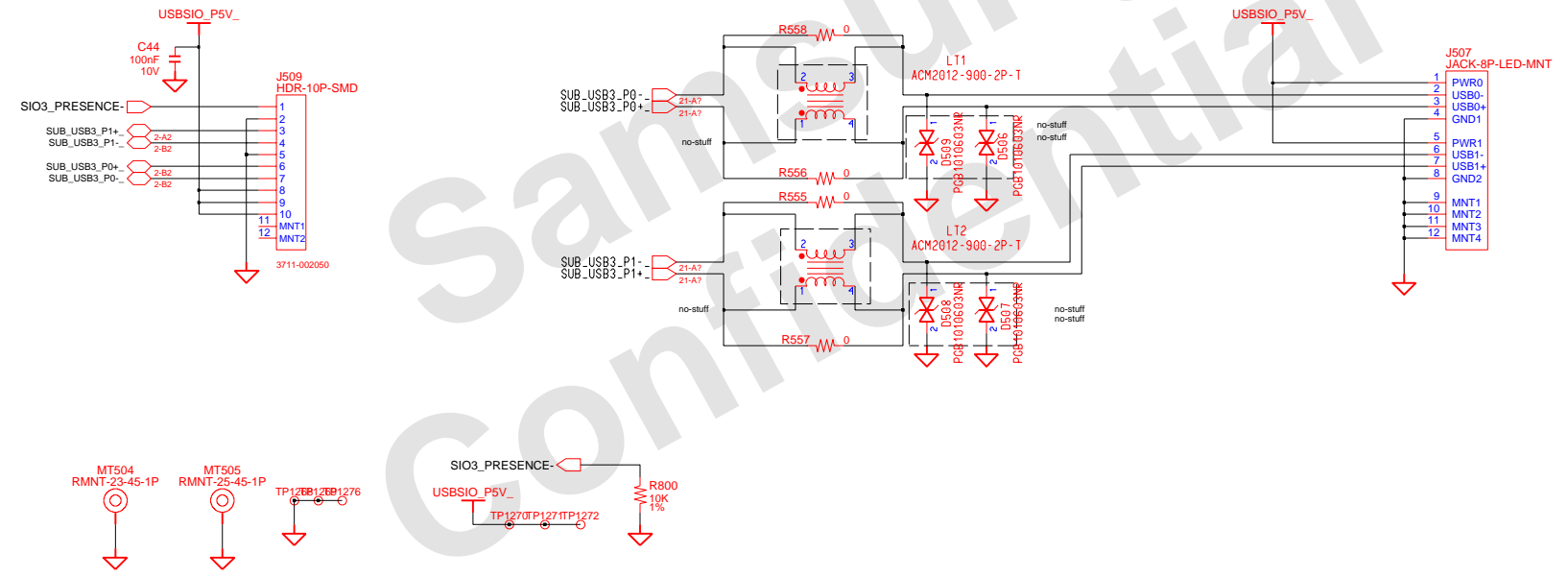
PCB REVISION CONTROL (ICT)				
NO	CONNECTION	DATE(Y/M/MD)	REVISION	STEP
1	N.C.			
2	1-2			
3	2-3			
4	3-1			
5	1-2-3			
6	N.C.			
7	1-2			
8	2-3			
9	3-1			
10	1-2-3			

DRAW	Y00, BW	DATE	4/8/2006	TITLE	HAINAN C	SAMSUNG ELECTRONICS
CHECK	BAIK, SS	DEV. STEP	DV	MAIN	Ext Gfx connector	
APPROVAL	BIN, KK	REV	1.0			PART NO. BA41-#####A
MODULE CODE	undefined	LAST EDIT	April, 13, 2006 5:21:00 PM	PAGE	47	OF 50

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USB & DMB SUBBOARD

USB0, 1 Connector



DRAW	Y00, BW	DATE	4/8/2006	TITLE	HAINAN C POWER USB BOARD	SAMSUNG ELECTRONICS PART NO. BA41-####A
CHECK	BAIK, SS	DEV. STEP	DV			
APPROVAL	BIN, KK	REV	1.0			
MODULE CODE	undefined	LAST EDIT	April, 13, 2006 5:21:20 PM	PAGE	49 OF 50	

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EXT GFx

CPU :
Chip Set : NVIDIA 7X series
Remarks :

Model Name : HABANA EXT GFx
PBA Name :
PCB Code :
Dev. Step : MP
Revision : 1.0
T.R. Date : 2005.11.14

- Sheet 1. COVER
- Sheet 2. GFX CONNECTOR
- Sheet 3~6. GFX CHIP (G73M)
- Sheet 7. GFX STRAP OPTION
- Sheet 8~9. GDDR3 MEMORY
- Sheet 10. GDDR3 TERMINATION, THERMAL SENSOR, HDCP ROM
- Sheet 11. GFX CORE REGULATOR

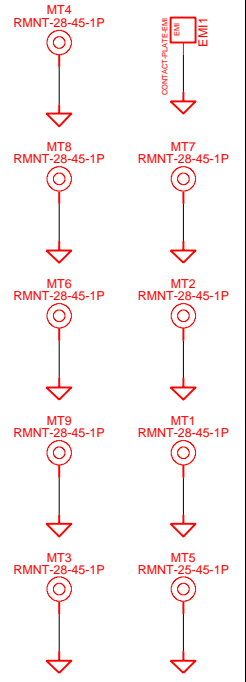
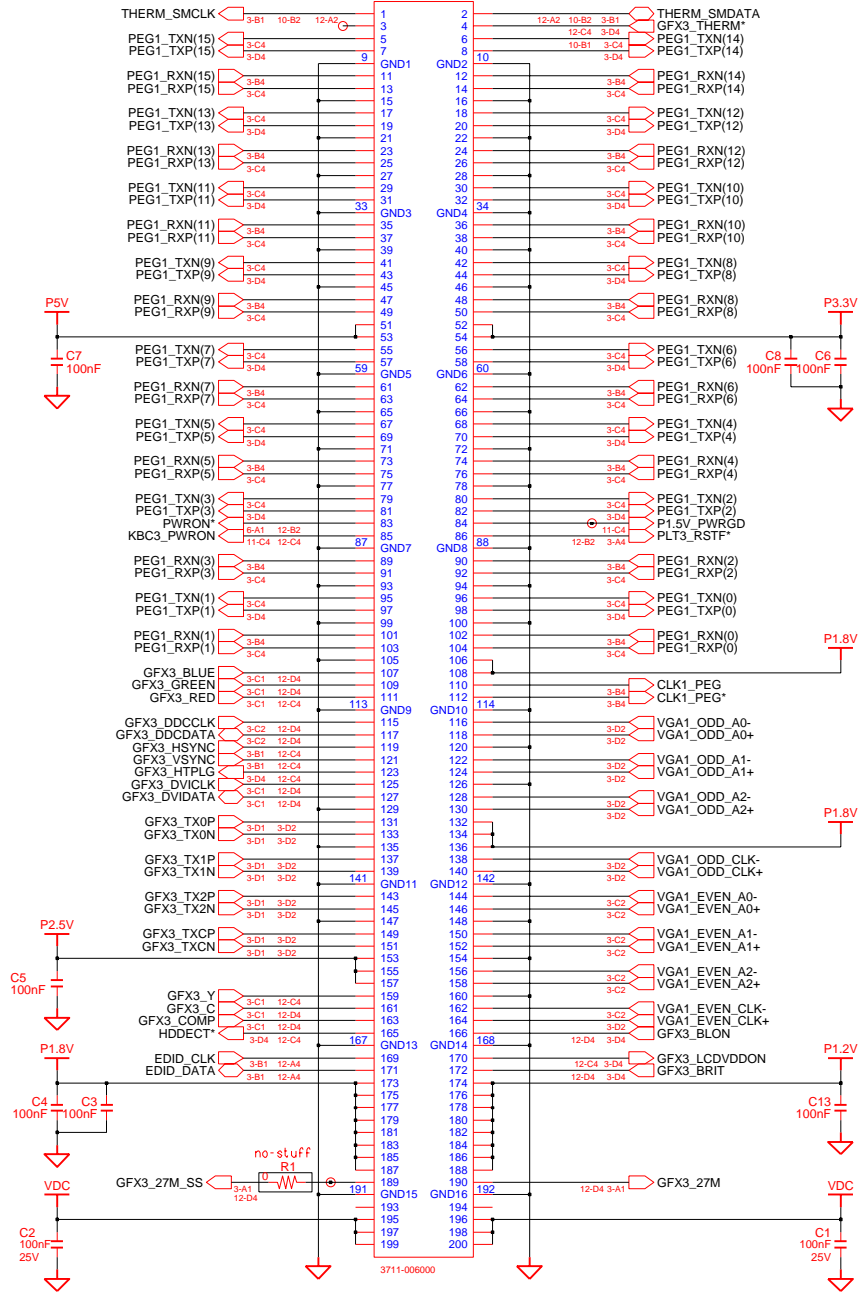
DRAW	CHECK	APPROVAL
SE LEE	ES CHO	BL LEE

DRAW	LEE, SE	DATE	11/14/2005	TITLE	HABANA EXT GFX COVER	SAMSUNG ELECTRONICS	
CHECK	CHO, ES	DEV. STEP	MP	PART NO.			BA41-00545A
APPROVAL	LEE, BL	REV	1.0				
MODULE CODE		LAST EDIT	November 14, 2005 10:24:53 PM	PAGE	1	OF 12	

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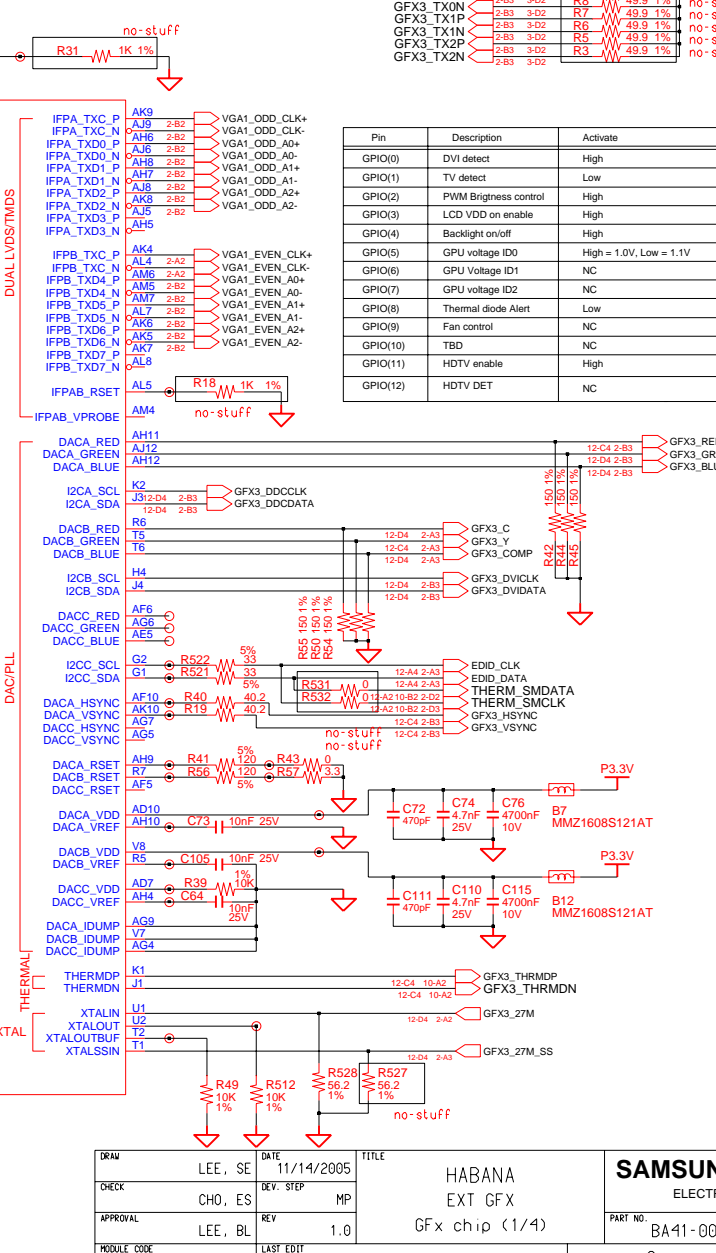
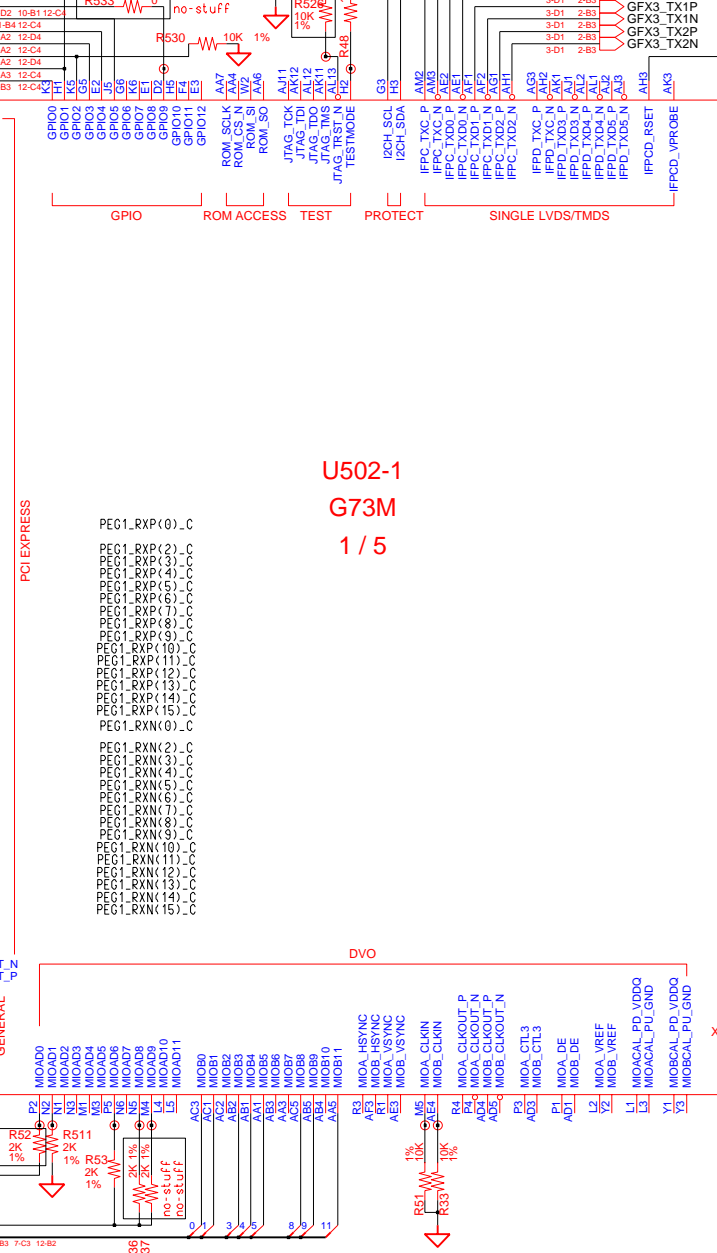
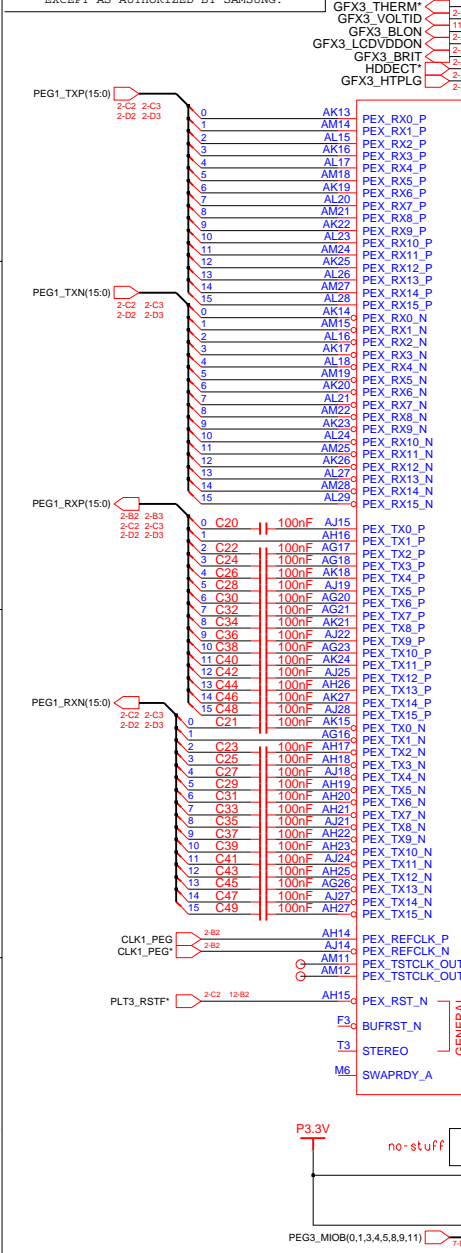
J501 HEAD-200P-2R-SMD-GND



DRAW	LEE, SE	DATE	11/14/2005	TITLE	HABANA EXT GFX	SAMSUNG ELECTRONICS
CHECK	CHO, ES	DEV. STEP	MP	Gfx connector		
APPROVAL	LEE, BL	REV	1.0			PART NO. BA41-00545A
MODULE CODE	LAST EDIT		November 14, 2005 10:24:53 PM		PAGE	2 OF 12

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Pin	Description	Activate
GPIO(0)	DVI detect	Low
GPIO(1)	TV detect	High
GPIO(2)	PWM Brightness control	High
GPIO(3)	LCD VDD on enable	High
GPIO(4)	Backlight on/off	High
GPIO(5)	GPU voltage ID0	High = 1.0V, Low = 1.1V
GPIO(6)	GPU Voltage ID1	NC
GPIO(7)	GPU voltage ID2	NC
GPIO(8)	Thermal diode Alert	Low
GPIO(9)	Fan control	NC
GPIO(10)	TBD	NC
GPIO(11)	HDTV enable	High
GPIO(12)	HDTV DET	NC

Pin	Description	Activate
GFX3_TXCP	2-83 3-02	R4 49.9 1% no-stuff
GFX3_TXCN	2-83 3-02	R9 49.9 1% no-stuff
GFX3_TXOP	2-83 3-02	R7 49.9 1% no-stuff
GFX3_TXON	2-83 3-02	R8 49.9 1% no-stuff
GFX3_TX1P	2-83 3-02	R8 49.9 1% no-stuff
GFX3_TX1N	2-83 3-02	R6 49.9 1% no-stuff
GFX3_TX2P	2-83 3-02	R5 49.9 1% no-stuff
GFX3_TX2N	2-83 3-02	R3 49.9 1% no-stuff

U502-1
G73M
1 / 5

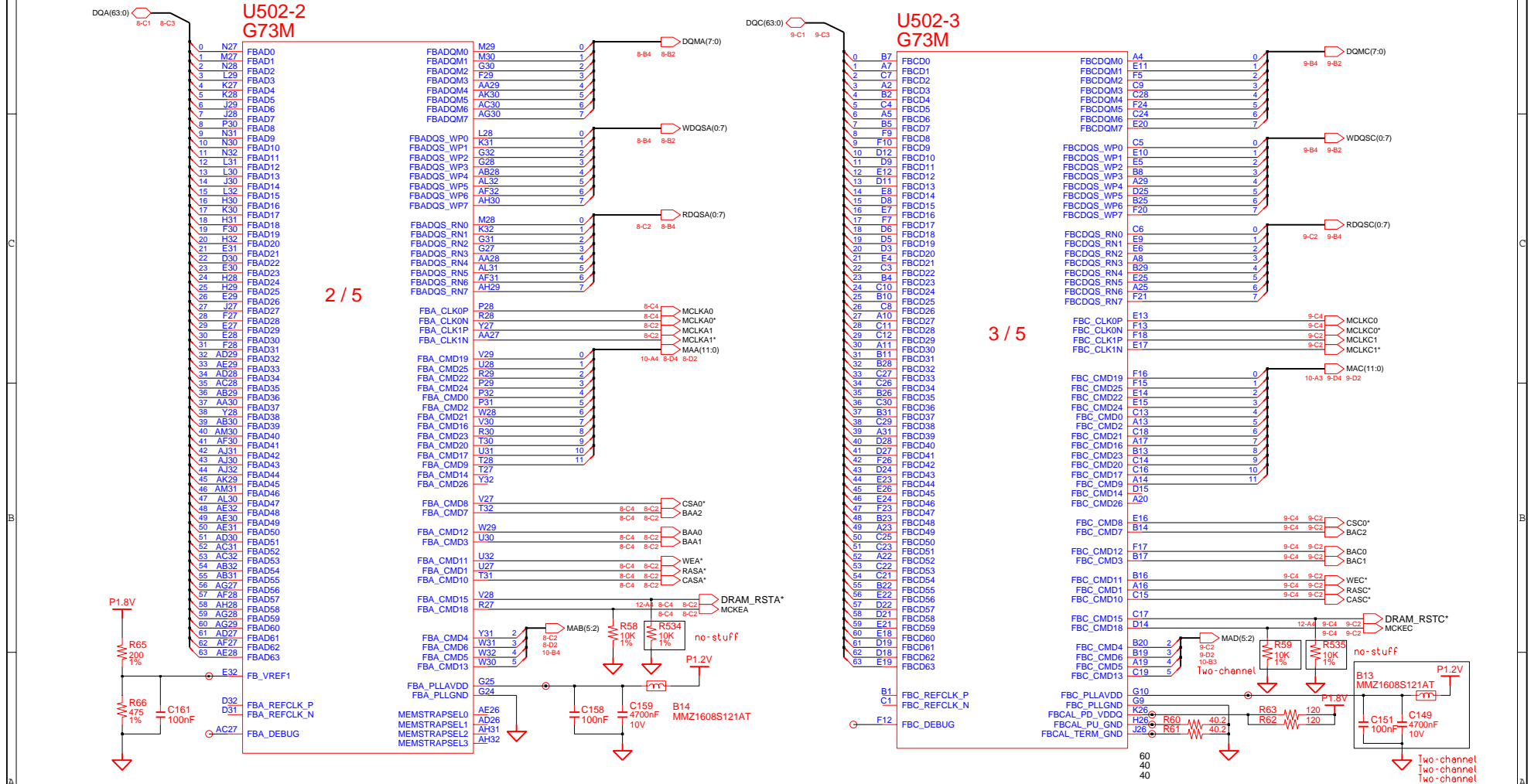
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CHECK	CHO, ES	DEV. STEP	MP	REV	Gfx chip (1/4)	
APPROVAL	LEE, BL	REV	1.0	LAST EDIT	November 14, 2005 10:24:53 PM	PART NO. BA41-00545A
MODULE CODE						PAGE 3 OF 12

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Graphic Memory I/F (Using FBA Channel)

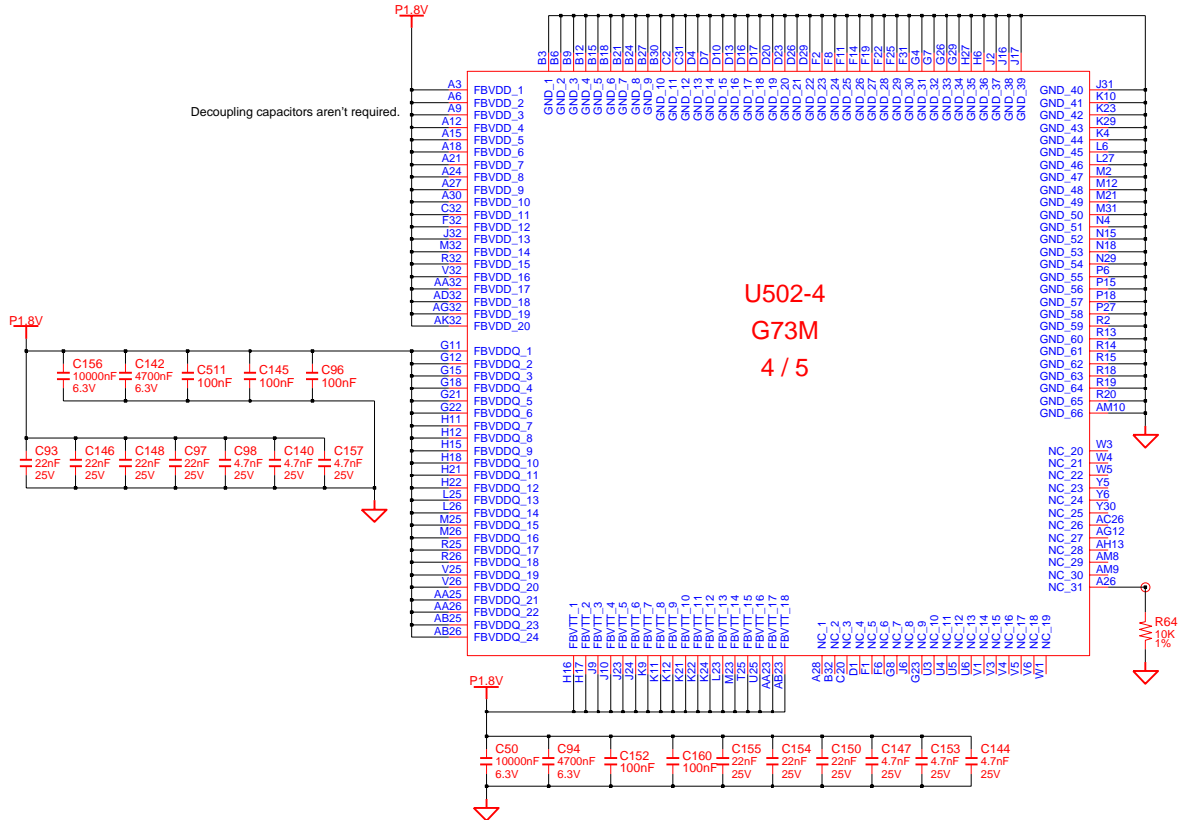
Graphic Memory I/F (Using FBC Channel)



DATE	11/14/2005	TITLE	HABANA EXT GFX	SAMSUNG ELECTRONICS
DEV. STEP	MP	REV	GfX chip (2/4)	
DRAW	LEE, SE	REV	1.0	PART NO. BA41-00545A
CHECK	CHO, ES	LAST EDIT	November 14, 2005 10:24:53 PM	PAGE 4 OF 12
APPROVAL	LEE, BL			
MODULE CODE				

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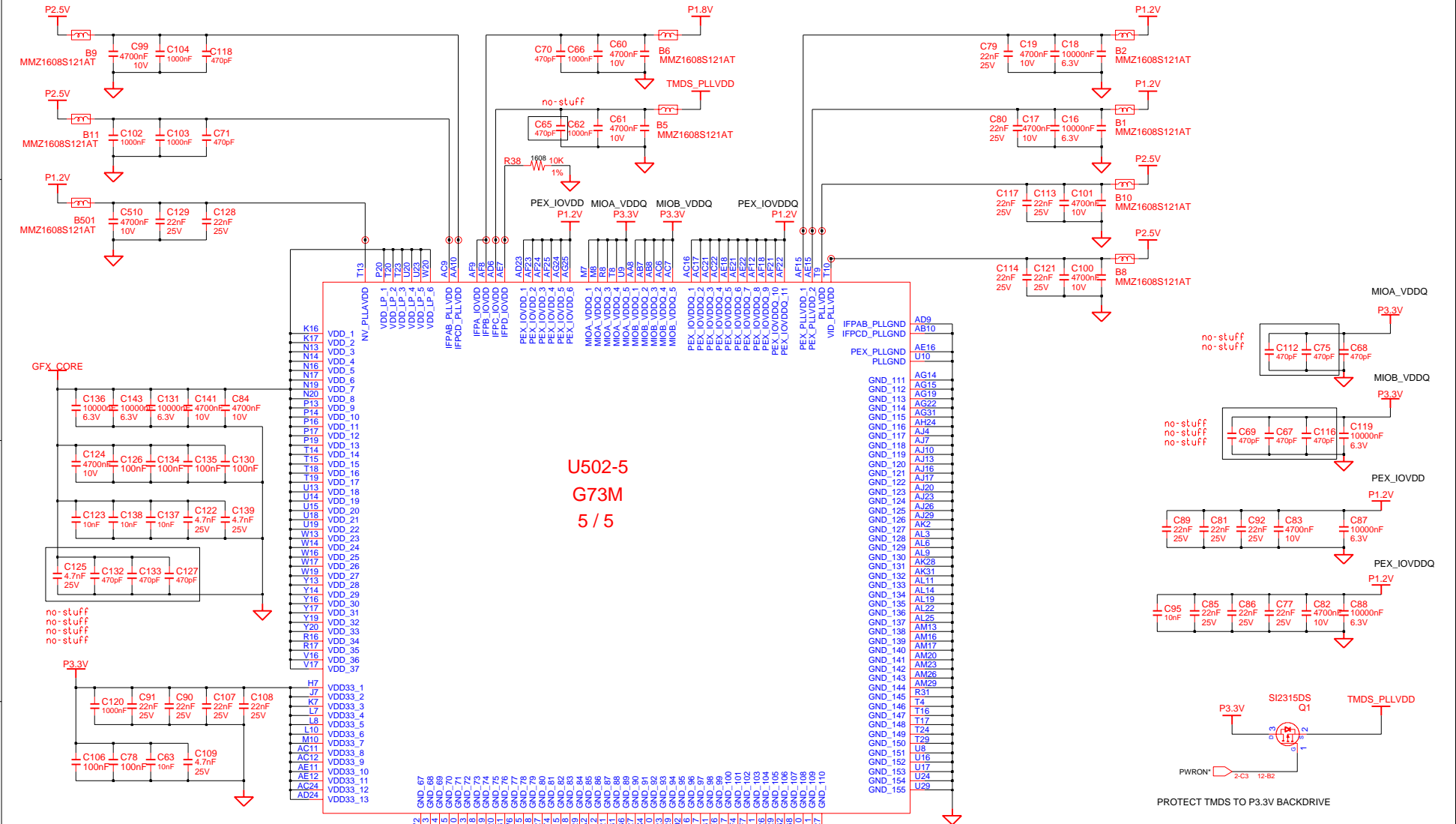
Decoupling capacitors aren't required.

U502-4
G73M
4/5

DRAW	LEE, SE	DATE	11/14/2005	TITLE	HABANA EXT GFX	
CHECK	CHO, ES	DEV. STEP	MP	GFx chip (3/4)		
APPROVAL	LEE, BL	REV	1.0			PART NO. BA41-00545A
MODULE CODE	LAST EDIT		November 14, 2005 10:24:53 PM		PAGE	5 OF 12

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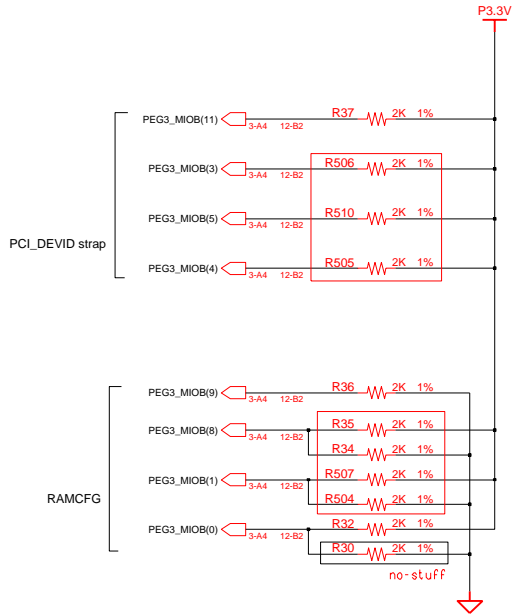


DRAW	LEE, SE	DATE	11/14/2005	TITLE	HABANA EXT GFX	SAMSUNG ELECTRONICS
CHECK	CHO, ES	DEV. STEP	MP	GFX chip (4/4)		
APPROVAL	LEE, BL	REV	1.0			PART NO. BA41-00545A
MODULE CODE	LAST EDIT		November 14, 2005 10:24:53 PM		PAGE	6 OF 12

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	R37	R506	R510	R505
72M-V	no-stuff	stuff	stuff	stuff
72M	stuff	no-stuff	no-stuff	no-stuff
73M	stuff	no-stuff	no-stuff	no-stuff

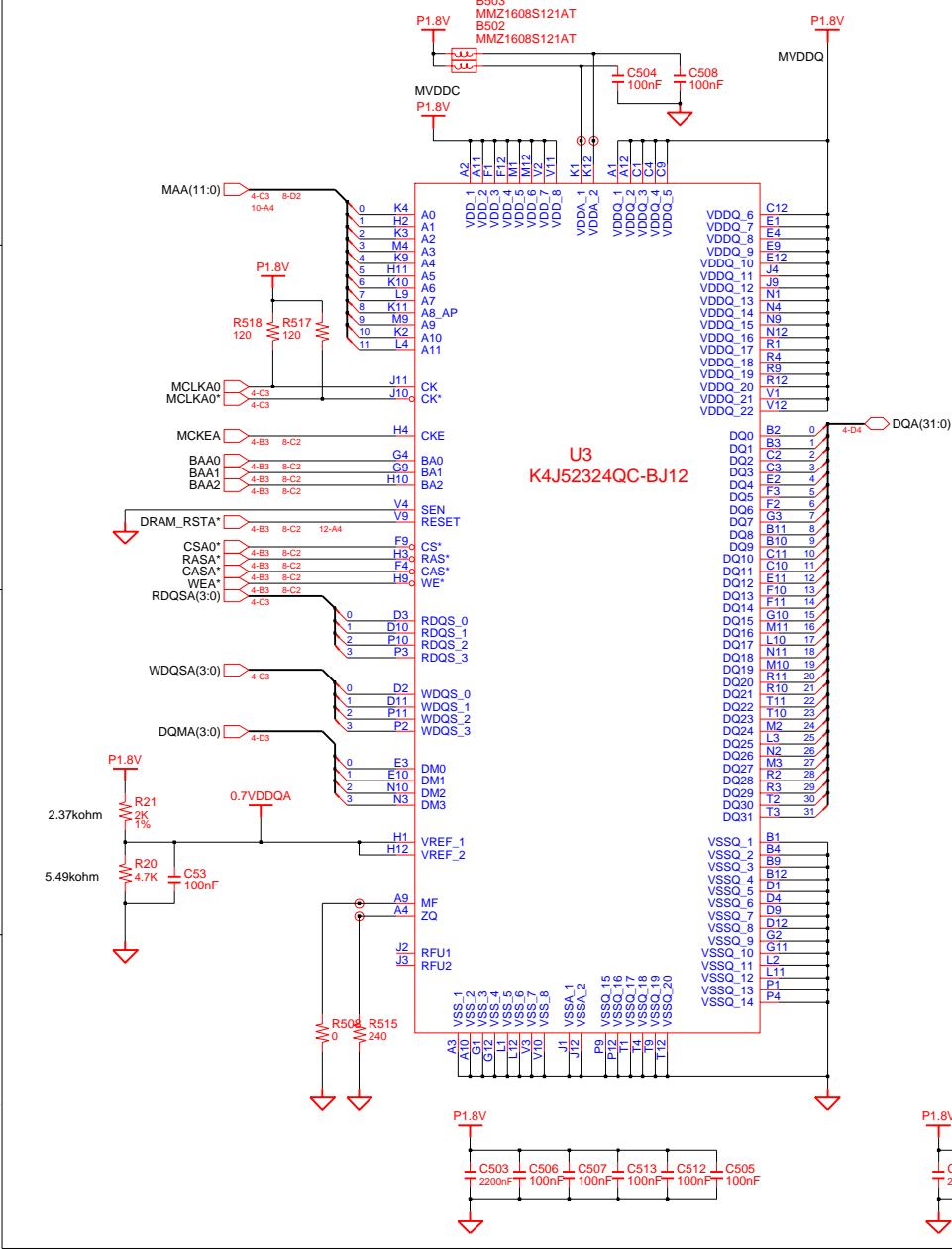


	R35	R34	R507	R504
SS 256Mb	stuff	no-stuff	stuff	no-stuff
INF 256Mb	stuff	no-stuff	no-stuff	stuff
SS 512Mb	no-stuff	stuff	stuff	no-stuff
INF 512Mb	no-stuff	stuff	no-stuff	stuff

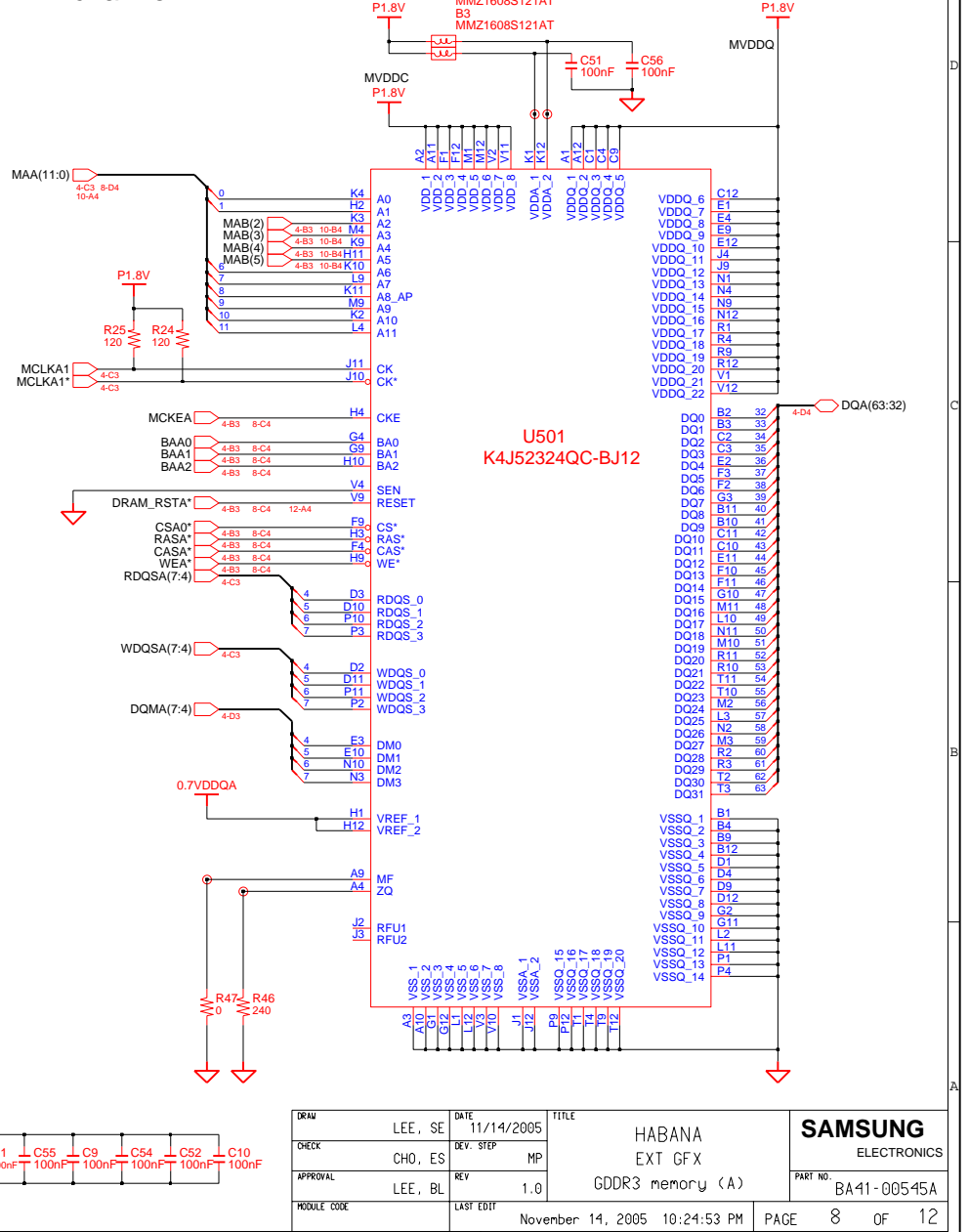
Straps	Pin # (Rev.A02)	Descriptions
SUB_VENDOR	MIOAD(1)	0 : No BIOS 1 : Read from BIOS(Default)
RAMCFG(3:0) [9,8,1,0]	MIOB(9) MIOB(8) MIOB(1) MIOB(0)	0111 : samsung GDDR3 256Mbit 0101 : infineon GDDR3 256Mbit 0011 : samsung GDDR3 512Mbit 0001 : infineon GDDR3 512Mbit
CRYSTAL(1:0)	MIOB(2) MIOB(6)	01 : 14.318 MHz 10 : 27 MHz (Default) 11 : Unknown 00 : 13.5 MHz
TV_MODE(1:0)	MIOAD(7) MIOAD(10)	00 : SECAM 01 : NTSC (Default) 10 : PAL 11 : CRT
PCI_DEVID(3:0) [11,3,5,4]	MIOB(11) MIOB(3) MIOB(5) MIOB(4)	72M : 0X01D8 72M-V : 0X01D7 73M : 0X0398
ROM_TYPE(1:0)	MIOB(10) MIOBVSYN	No ROM (NC)
USER STRAP	MIOAD(2:5)	EDID

DRAW	LEE, SE	DATE	11/14/2005	TITLE	HABANA EXT GFX	SAMSUNG ELECTRONICS
CHECK	CHO, ES	DEV. STEP	MP			
APPROVAL	LEE, BL	REV	1.0	Gfx strap option		PART NO. BA41-00545A
MODULE CODE		LAST EDIT	November 14, 2005 10:24:53 PM	PAGE	7	OF 12

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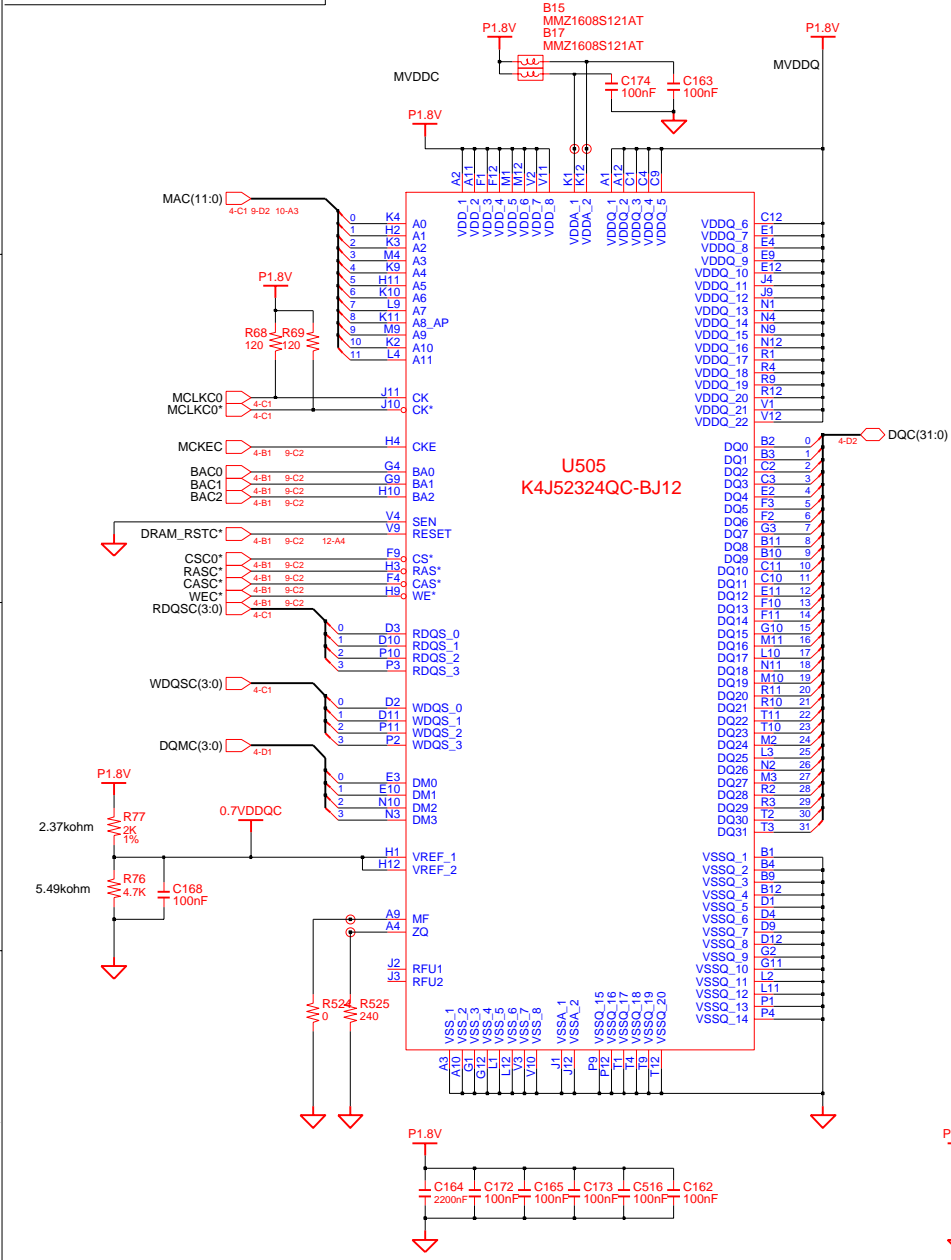
A-channel



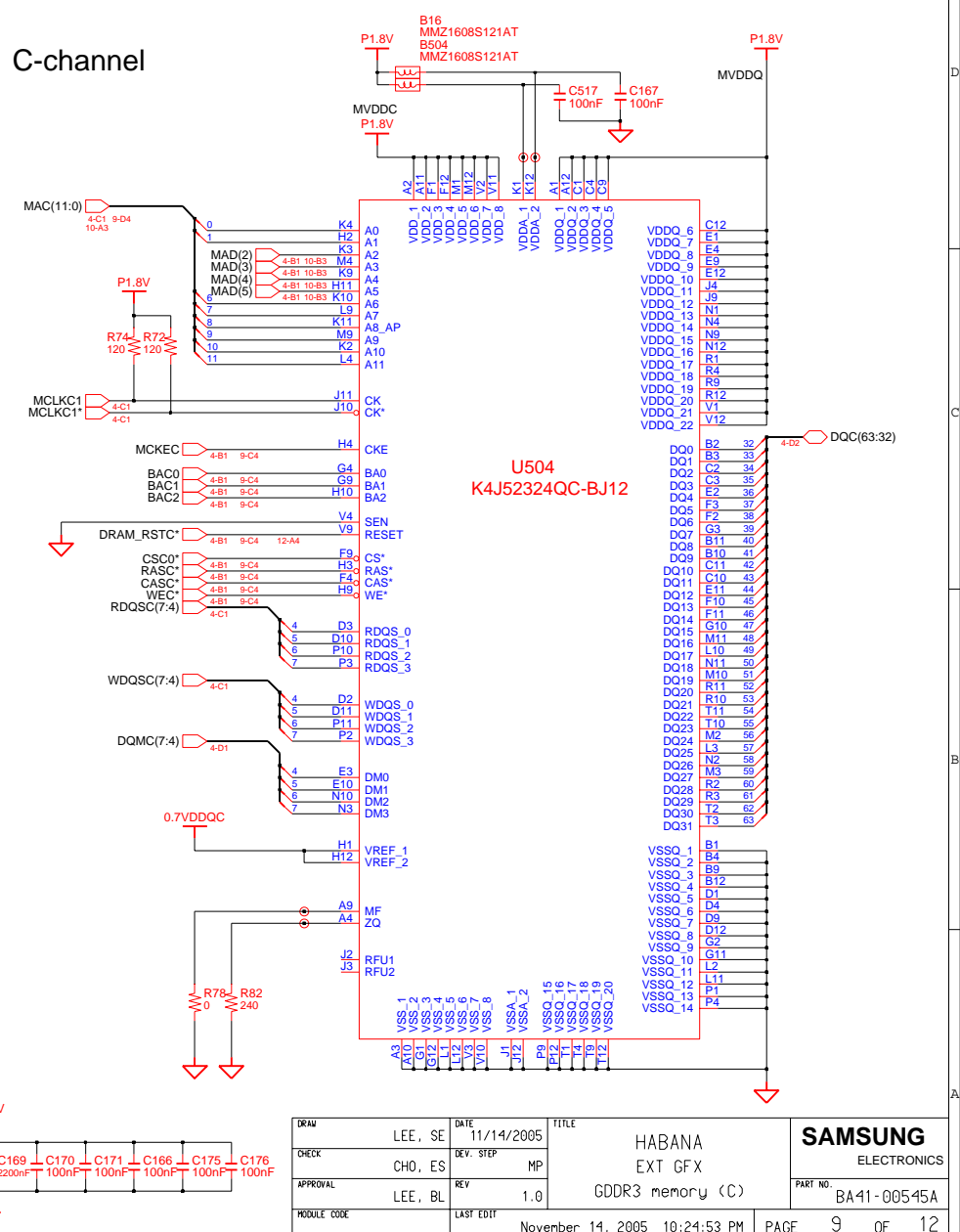
DRAW LEE, SE CHECK CHO, ES APPROVAL LEE, BL MODULE CODE	DATE 11/14/2005 DEV. STEP MP REV 1.0 LAST EDIT	TITLE HABANA EXT GFX GDDR3 memory (A)	SAMSUNG ELECTRONICS PART NO. BA41-00545A
November 14, 2005 10:24:53 PM			PAGE 8 OF 12

This page is for "2channel-model".

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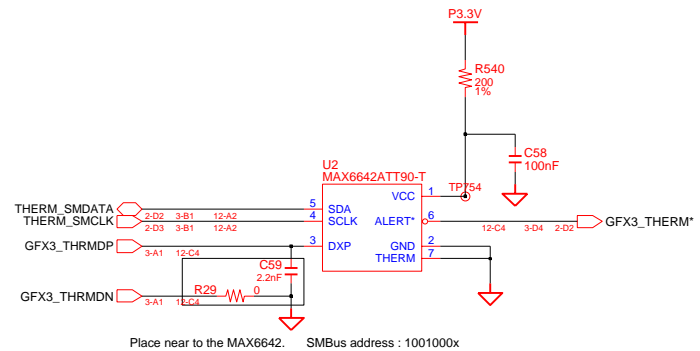
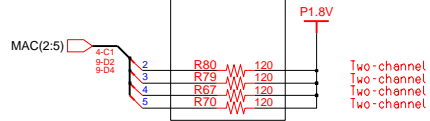
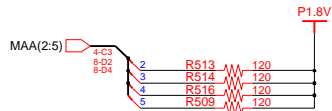
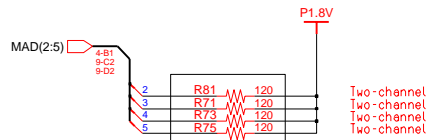
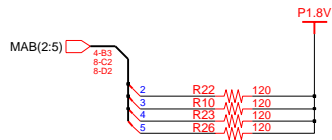
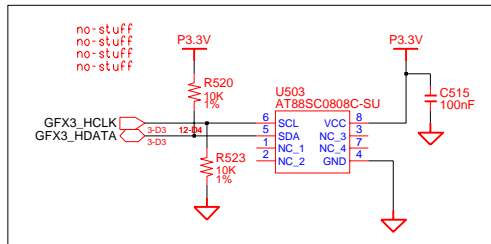
C-channel



DRAW	LEE, SE	DATE	11/14/2005	TITLE	HABANA EXT GFX	SAMSUNG ELECTRONICS
CHECK	CHO, ES	DEV. STEP	MP	GDDR3 memory (C)		
APPROVAL	LEE, BL	REV	1.0	November 14, 2005 10:24:53 PM		PART NO. BA41-00545A
MODULE CODE	LAST EDIT		PAGE		9	OF 12

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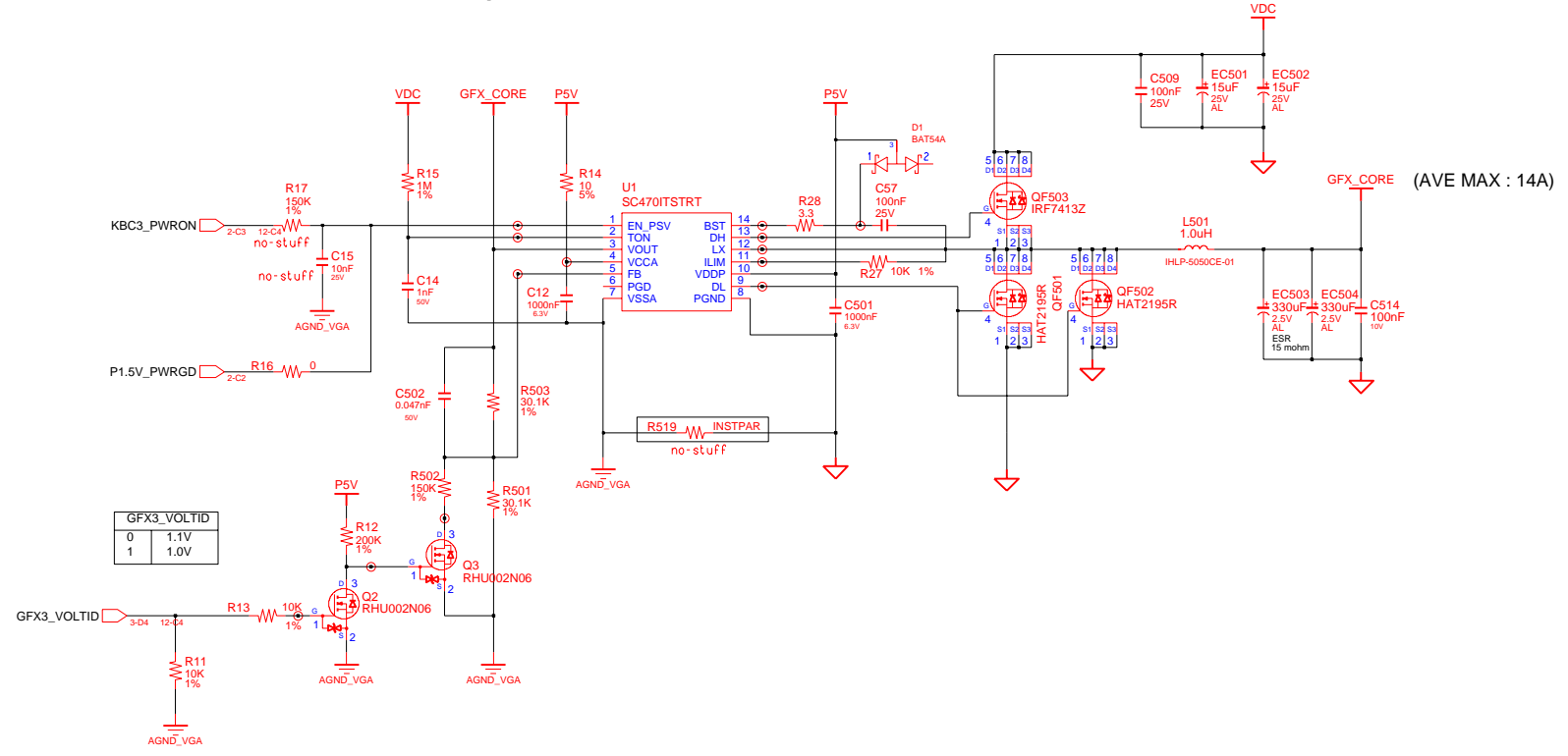
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DRW	LEE, SE	DATE	11/14/2005	TITLE	HABANA EXT GFX	SAMSUNG ELECTRONICS PART NO. BA41-00545A
CHECK	CHO, ES	DEV. STEP	MP			
APPROVAL	LEE, BL	REV	1.0	GDDR3 Term. Thermal sensor		
MODULE CODE		LAST EDIT	November 14, 2005 10:24:53 PM	PAGE	10	OF 12

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Graphic Core Power



GFX3_VOLTID	
0	1.1V
1	1.0V

DRAW	LEE, SE	DATE	11/14/2005	TITLE	HABANA EXT GFX		SAMSUNG ELECTRONICS
CHECK	CHO, ES	DEV. STEP	MP	Gfx core Regulator		PART NO. BA41-00545A	
APPROVAL	LEE, BL	REV	1.0	November 14, 2005 10:24:53 PM		PAGE	11 OF 12
MODULE CODE	LAST EDIT						

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○GFX3_27M
○GFX3_27M_SS
○GFX3_BLON
○GFX3_BLUE
○GFX3_BR11
○GFX3_C
○GFX3_COMP
○GFX3_DDCCLK
○GFX3_DDCDATA
○GFX3_DVICLK
○GFX3_DVIDATA

○GFX3_GREEN
○GFX3_HCLK
○GFX3_HDATA
○GFX3_HSYNC
○GFX3_HITPLG
○GFX3_CDVDDON
○GFX3_RED
○GFX3_THERM*
○GFX3_THRMDN
○GFX3_THRMOP

○GFX3_VOLTID
○GFX3_VSYNC
○GFX3_Y
○HDDTECT*
○KBC3_PWRON

○DRAM_RSTA*
○DRAM_RSTC*
○EDID_CLK
○EDID_DATA

○PSV
○PSV
○PSV
○PSV
○TMSD_PLLVDD
○TMSD_PLLVDD

○VDC
○VDC
○VDC
○VDC

○0.7VDDQA
○0.7VDDQA

○0.7VDDQC
○0.7VDDQC

○AGND_VGA
○AGND_VGA

○PEG3_MIOB(0)
○PEG3_MIOB(1)
○PEG3_MIOB(11)
○PEG3_MIOB(3)
○PEG3_MIOB(4)
○PEG3_MIOB(5)
○PEG3_MIOB(8)
○PEG3_MIOB(9)
○PL13_RST1*
○PWRON*

○CFX_CORE
○GFX_CORE
○GFX_CORE
○GFX_CORE
○GFX_CORE

○GROUND
○GROUND
○GROUND
○GROUND
○GROUND

○P1_2V
○P1_2V
○P1_2V
○P1_2V
○P1_2V

○P1_8V
○P1_8V
○P1_8V
○P1_8V
○P1_8V

○P2_5V
○P2_5V
○P2_5V
○P2_5V
○P2_5V

○P3_3V
○P3_3V
○P3_3V
○P3_3V
○P3_3V

○PSV

○THERM_SMCLK
○THERM_SMDATA

DRAW	LEE, SE	DATE	11/14/2005	TITLE	HABANA EXT GFX		SAMSUNG ELECTRONICS
CHECK	CHO, ES	DEV. STEP	MP	GDDR3 Term. Thermal sensor		PART NO. BA41-00545A	
APPROVAL	LEE, BL	REV	1.0	November 14, 2005 10:24:53 PM		PAGE	12 OF 12
MODULE CODE	LAST EDIT						