

PALAU

CPU : Intel Merom-4M (800/667 MHz)
 Chip Set : Intel Crestline & ICH8-M
 Remarks : Mobility Platform

Model Name : SANTA ROSA STD
 PBA Name : MAIN
 PCB Code : BA41-00753A NANYA
 PCB Code : BA41-00786A GCE
 Dev. Step : PV - 2
 Revision : 1.0
 T.R. Date : 2007. 03.30

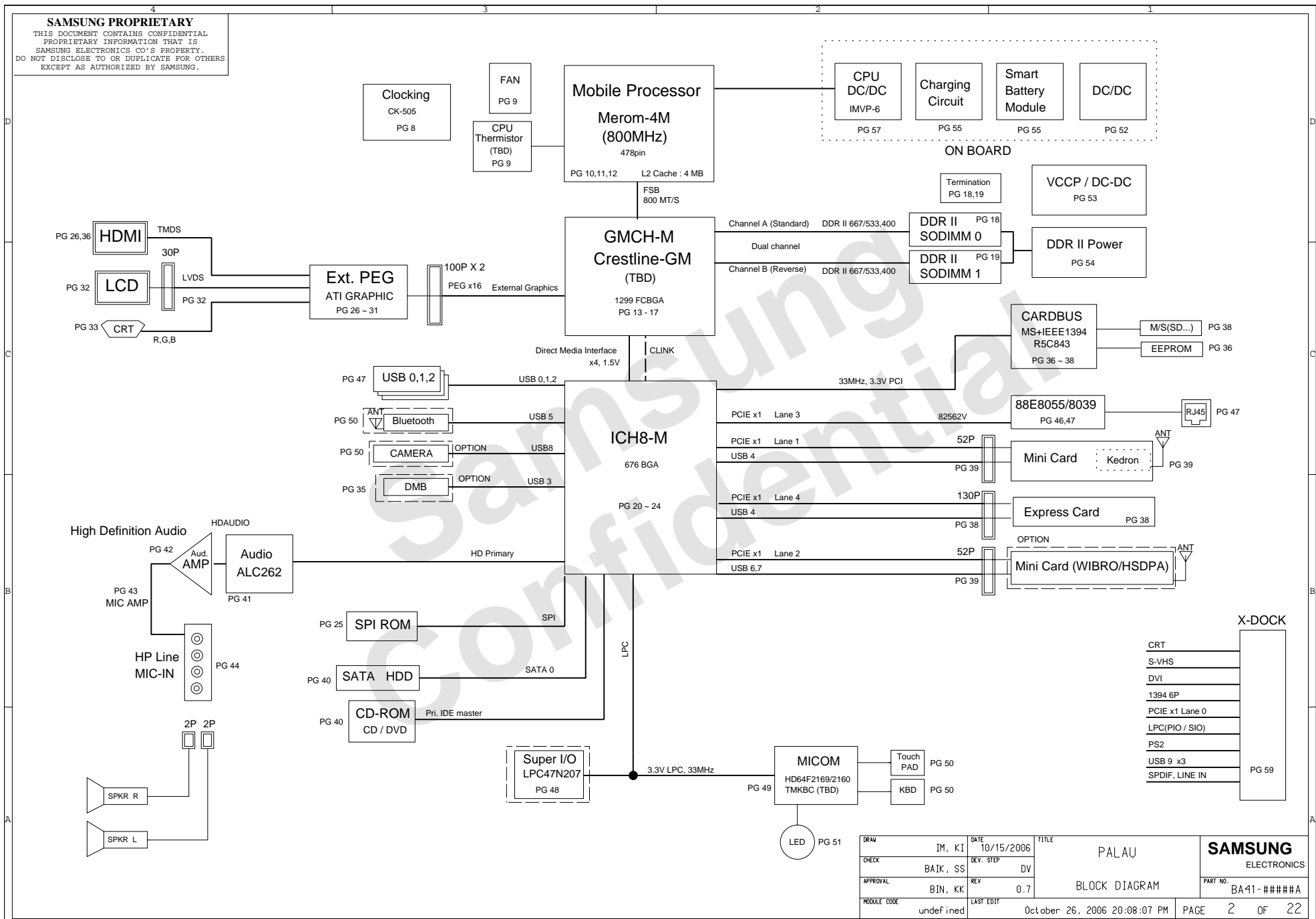
DRAW	CHECK	APPROVAL

Owner : SEC Mobile R & D Signature : X

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CHECK	BAIK, SS	DEV. STEP	DV			
APPROVAL	BIN, KK	REV	0.7	COVER		PART NO. BA41-#####
MODULE CODE		LAST EDIT	October 26, 2006 20:08:07 PM	PAGE	1	OF 22

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BOARD INFORMATION

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
Cardbus	AD25	3	B,C
USB	AD29(internal)	-	USB2.0 #0 (USB0) : A USB2.0 #1 (USB1) : D USB2.0 #2 (USB4) : C USB2.0 #3 (USB5) : E USB2.0 #4 (EHCI) : H
Hub to PCI LPC bridge/IDE/AC97/SMBUS	AD30(internal) AD31(internal)	- -	- B
Internal MAC AC Link GLAN	AD24(internal) - -	- - -	E B F

Voltage Rails

VDC	Primary DC system power supply (7 to 21V)
VCC_CORE	Core Voltage for CPU
GFX_CORE	Core Voltage for GPU
P1.05V (VCCP)	VTT for CPU, Crestline & ICH8-M
P3.3V_MICOM	3.3V always power rail (for Micom)
P1.5V	1.5V switched off power rail (off in S3-S5)
P1.8V	1.8V switched off power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail for DDR
P0.9V	0.9V power rail for DDR
P3.3V	3.3V switched off power rail (off in S3-S5)
P3.3V_AUX	3.3V switched on power rail
P5.0V	5.0V switched off power rail (off in S3-S5)
P5.0V_AUX	5.0V switched on power rail
P5.0V_ALW	5.0V always power rail

USB PORT Assign

PORT #	ASSIGNED TO
0	SYSTEM PORT 0
1	SYSTEM PORT 1
2	SYSTEM PORT 2
3	DMB or DOCKING
4	EXPRESS CARD TYPE I
5	Bluetooth
6	WIBRO / HSDPA
7	CAMERA
8	USIM CONTROL FOR WIBRO
9	MEMORY CARD CONTROLLER

PCI Express Assign

PORT #	ASSIGNED TO
0	DOCKING FOR GIGA LAN
1	Mini Card (KEDRON)
2	EXPRESS CARD TYPE I
3	SYSTEM FOR LAN
4	Mini Card (WIBRO / HSDPA)
5	RESERVED

Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	ICH8-M	Real Time Clock
Crystal	10MHz	MICOM	HD64F2169/2160
Crystal	14.318MHz	CLOCK-Generator	CK-505
Crystal	12.0MHz	Memory Card Controller	AUG371
Crystal	25MHz	LAN	Intel LAN

LCD Panel Detect (TBD)

Devices	Resolution	PANNEL_DETECT_0

I²C / SMB Address

Devices	Address	Hex	Bus
ICH8-m	Master	-	SMBUS Master
CPU Thermal Sensor	0111 101x	7Ah	Thermal Sensor
SODIMMO	1010 000x	A0h	-
SODIMM1	1010 010x	A4h	-
Thermal Sensor on SODIMM0	0011 000x	30h	-
Thermal Sensor on SODIMM1	0011 010x	34h	-
CK-505M (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable
MICOM	Master	-	SMBUS Master
EMC2102	0101 110X	5Ch	Thermal Sensor
BATTERY	0001 011X	16h	BATTERY

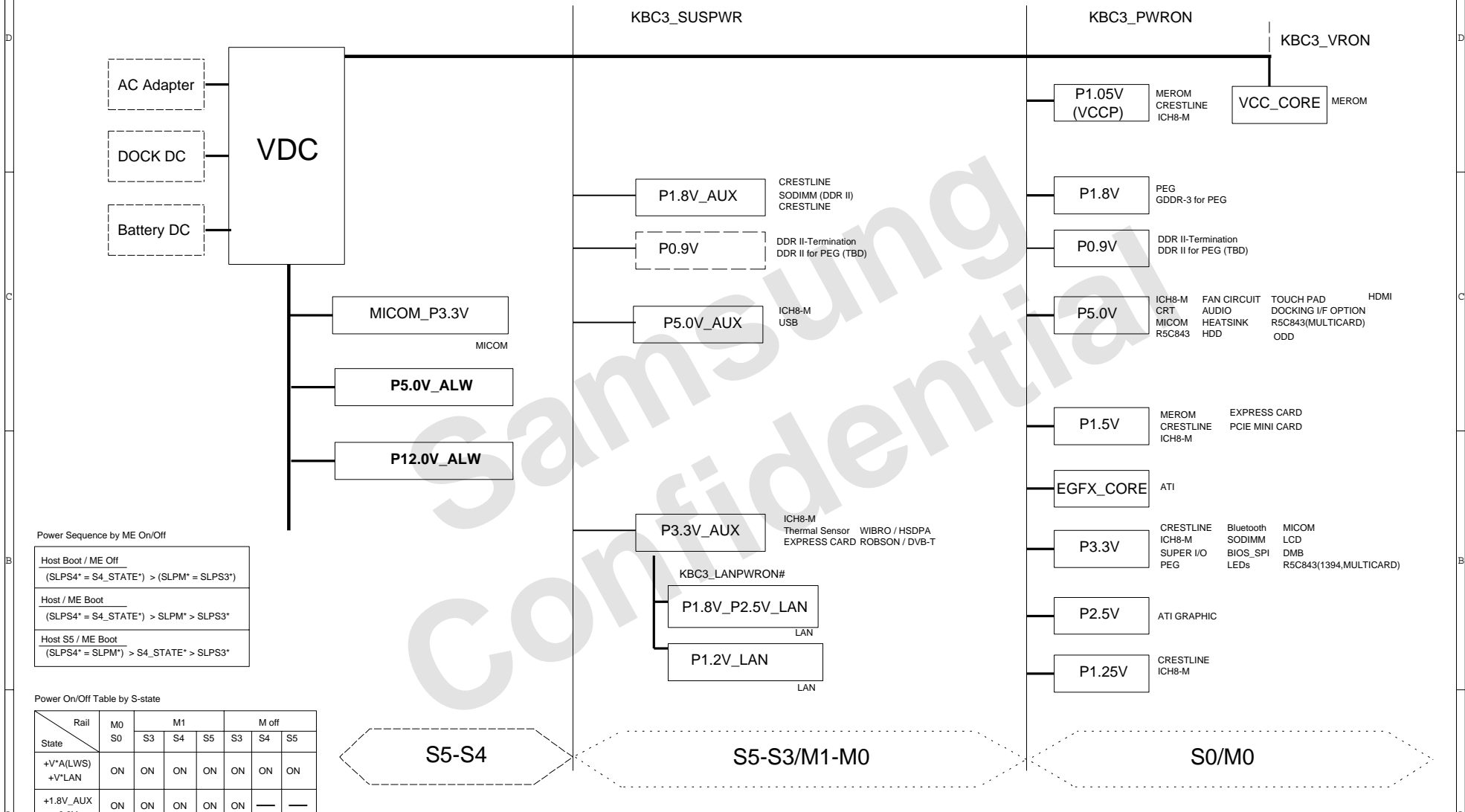
REVISION HISTORY

See rev notes for more information.

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POWER DIAGRAM



Power Sequence by ME On/Off

Host Boot / ME Off (SLPS4* = S4_STATE*) > (SLPM* = SLPS3*)
Host / ME Boot (SLPS4* = S4_STATE*) > SLPM* > SLPS3*
Host S5 / ME Boot (SLPS4* = SLPM*) > S4_STATE* > SLPS3*

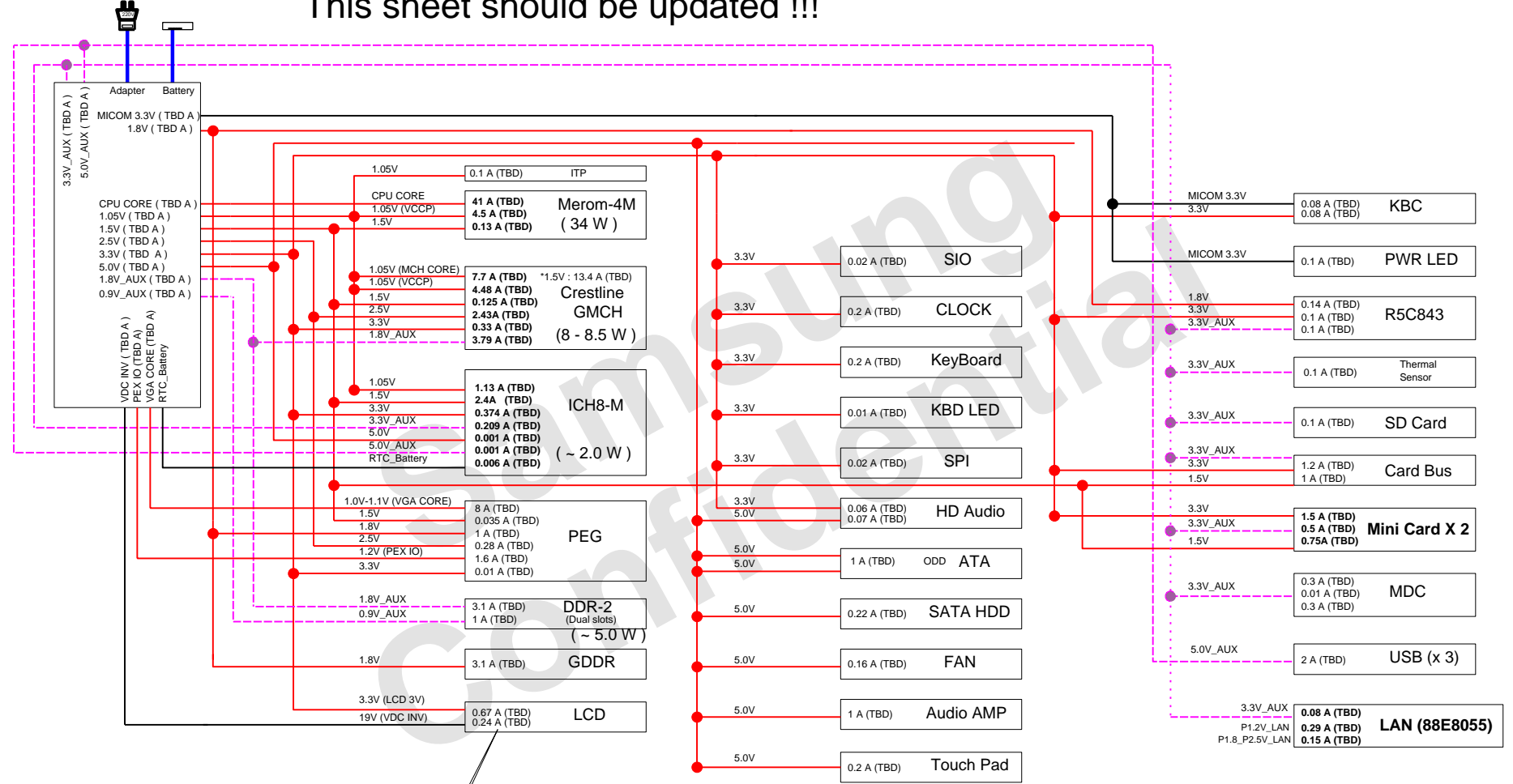
Power On/Off Table by S-state

Rail / State	M0 S0	M1			M off		
		S3	S4	S5	S3	S4	S5
+V*(LWS) +V*LAN	ON	ON	ON	ON	ON	ON	ON
+1.8V_AUX +0.9V	ON	ON	ON	ON	ON	---	---
+V*_AUX	ON	ON	---	---	ON	---	---
+V*_M	ON	ON	ON	ON	---	---	---
+V* (CORE)	ON	---	---	---	---	---	---



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This sheet should be updated !!!



Value by Datasheet/Application notes (Value by measurement)

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CHECK	BAIK, SS	DEV. STEP	DV	POWER RAILS		
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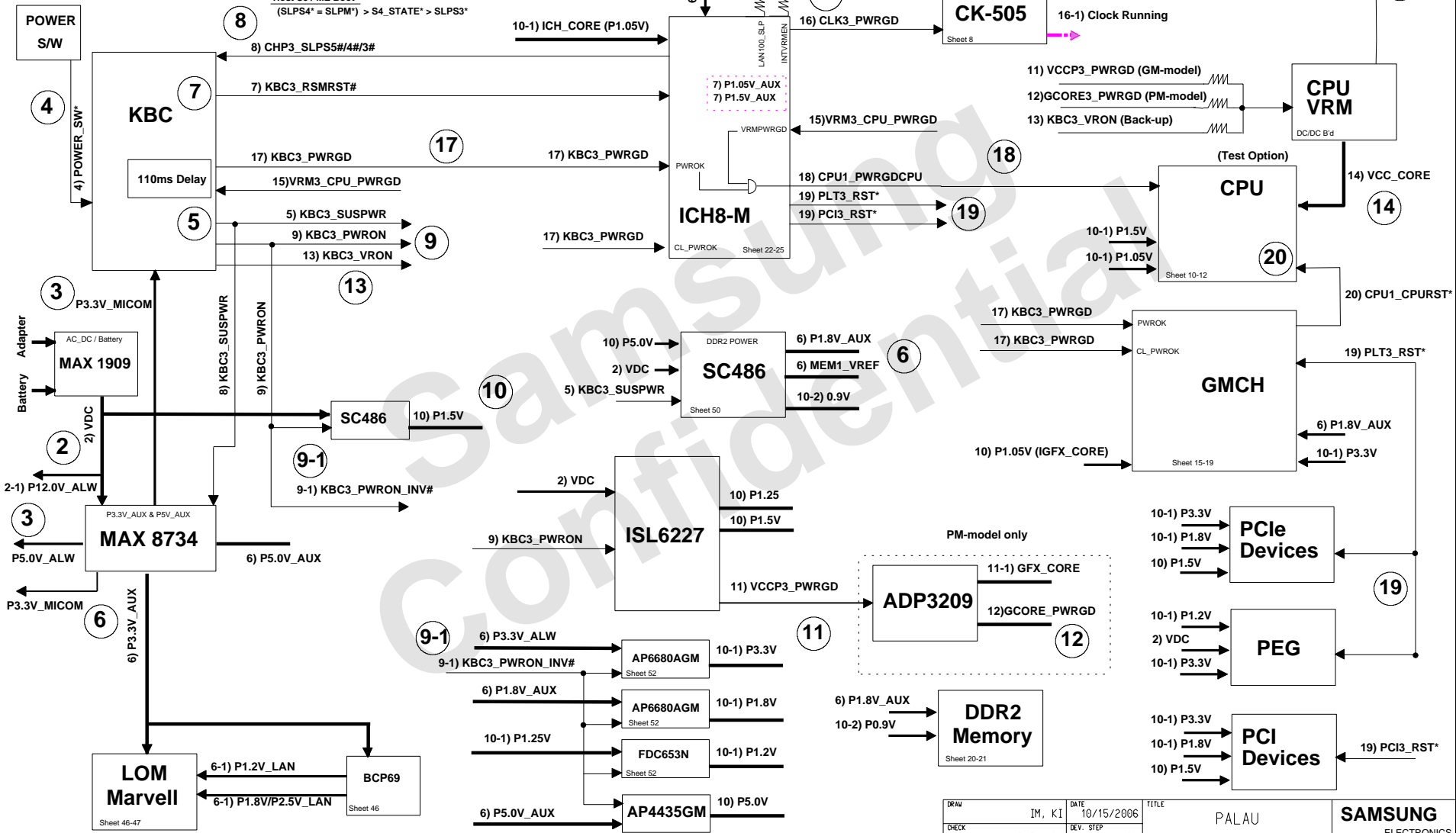
POWER SEQUENCE

Rev. 0.7

Host Boot / ME Off
 (SLPS4* = S4_STATE*) > (SLPM* = SLPS3*)
 M-1) KBC3_DDR_PWRON (TBD) = 8) KBC3_SUSPWR
 M-2) KBC3_ME_PWRON = 15) KBC3_PWRON

Host / ME Boot
 (SLPS4* = S4_STATE*) > SLPM* > SLPS3*

Host S5 / ME Boot
 (SLPS4* = SLPM*) > S4_STATE* > SLPS3*



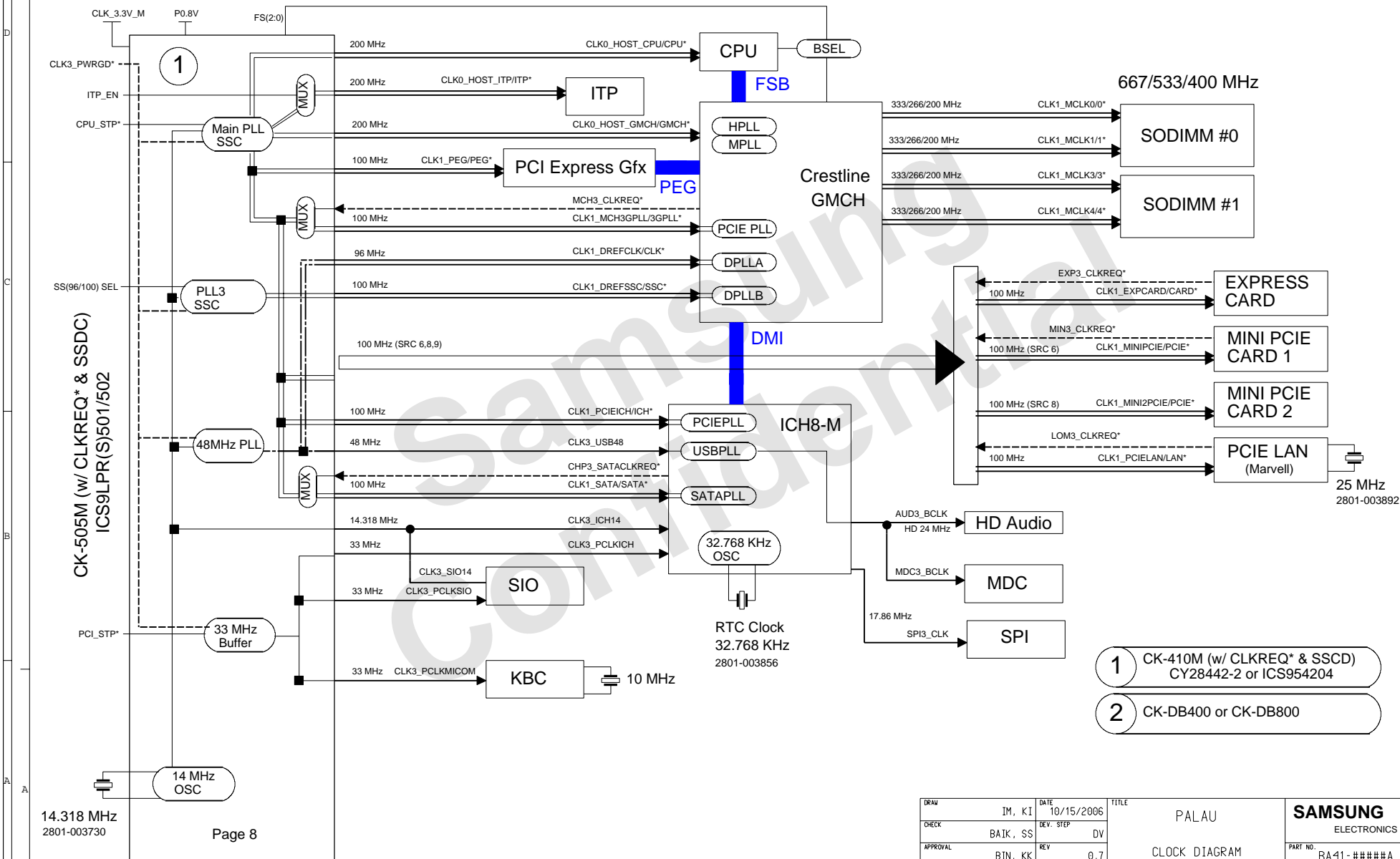
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MODULE CODE	undef ined	LAST EDIT	October 26, 2006 20:08:07 PM	PAGE	6	OF 22

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CLOCK DISTRIBUTION

Rev. 0.5



- 1 CK-410M (w/ CLKREQ* & SSDC) CY28442-2 or ICS954204
- 2 CK-DB400 or CK-DB800

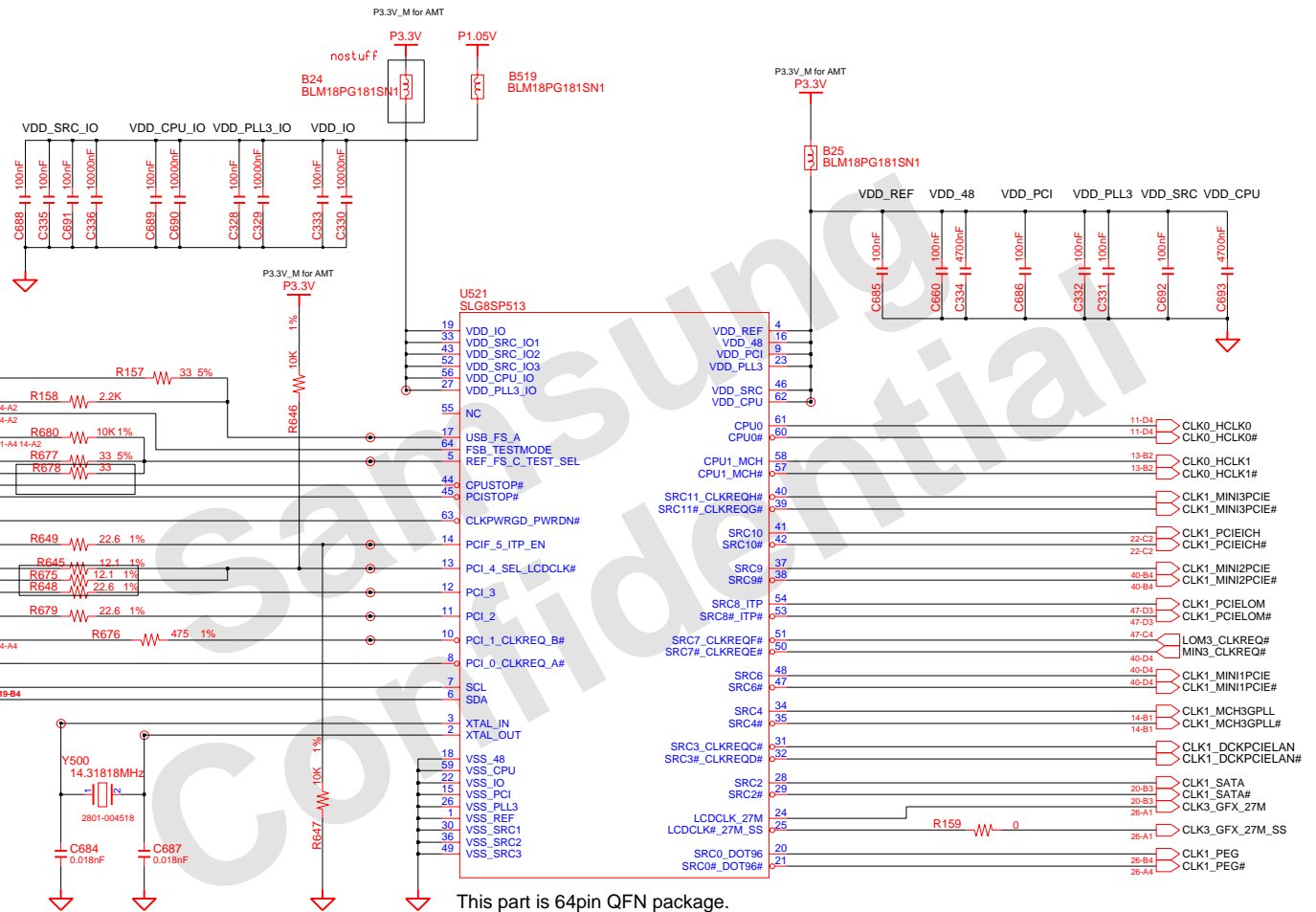
14.318 MHz
2801-003730

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APPROVAL	BIN, KK	REV	0.7		CLOCK DIAGRAM	PART NO. BA41-#####A
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FSA	FSB	FSC	HOST CLK
BSEL0	BSEL1	BSEL2	
0	0	0	266 MHz
0	0	1	333 MHz
0	1	0	200 MHz
0	1	1	400 MHz
1	0	0	133 MHz
1	0	1	100 MHz
1	1	0	166 MHz
1	1	1	RSVD



with-docking

with-docking

with-docking

Place 14.318MHz within
500mils of CK-505

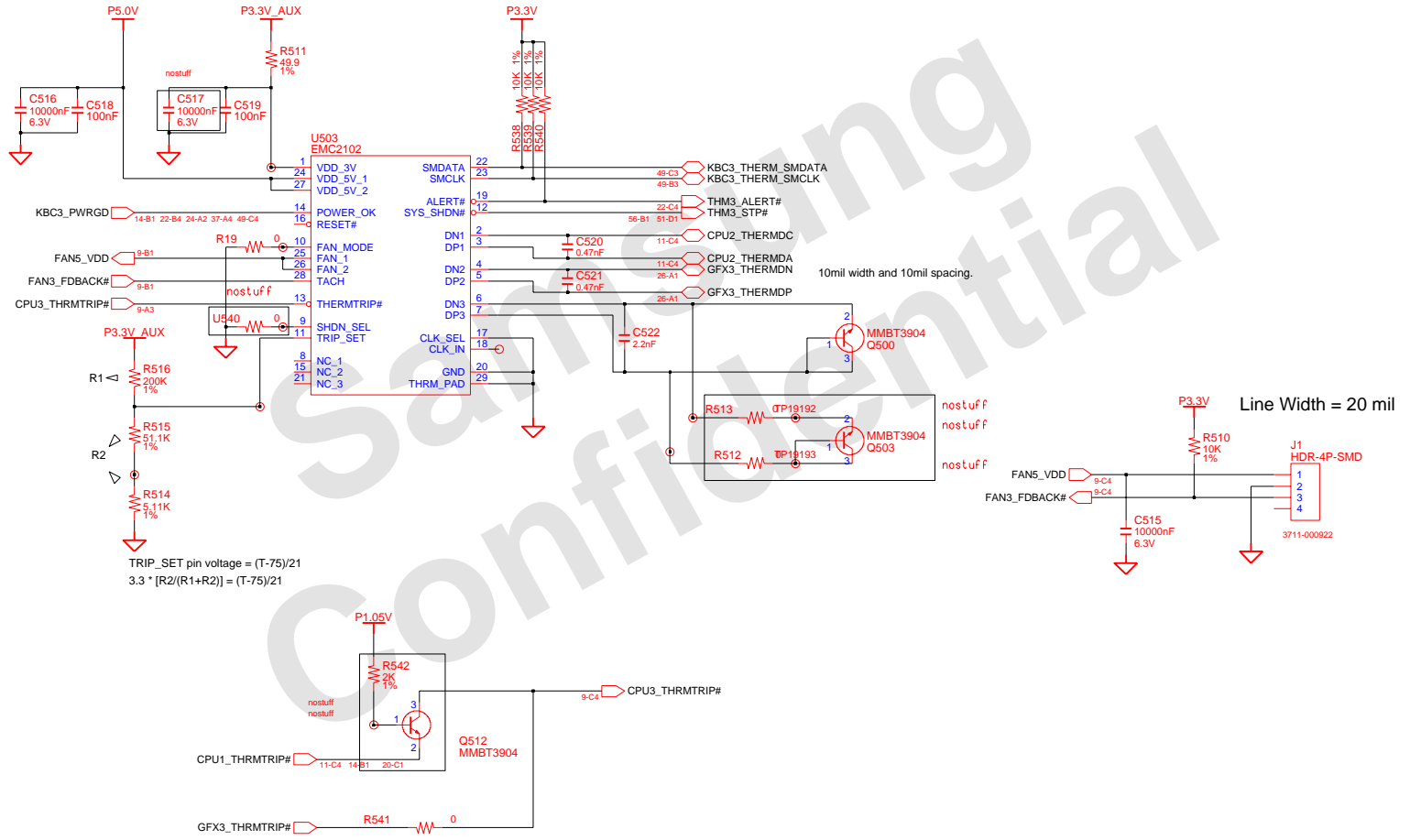
This part is 64pin QFN package.

Please near to the MCH.

CLK REQ	DEVICE	SRC PORT
CLK REQ A	SATA	SRC2
CLK REQ B	GMCH	SRC4
CLK REQ E	MINI CARD	SRC6
CLK REQ F	LOM	SRC8

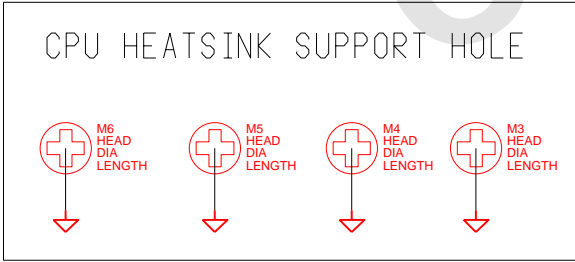
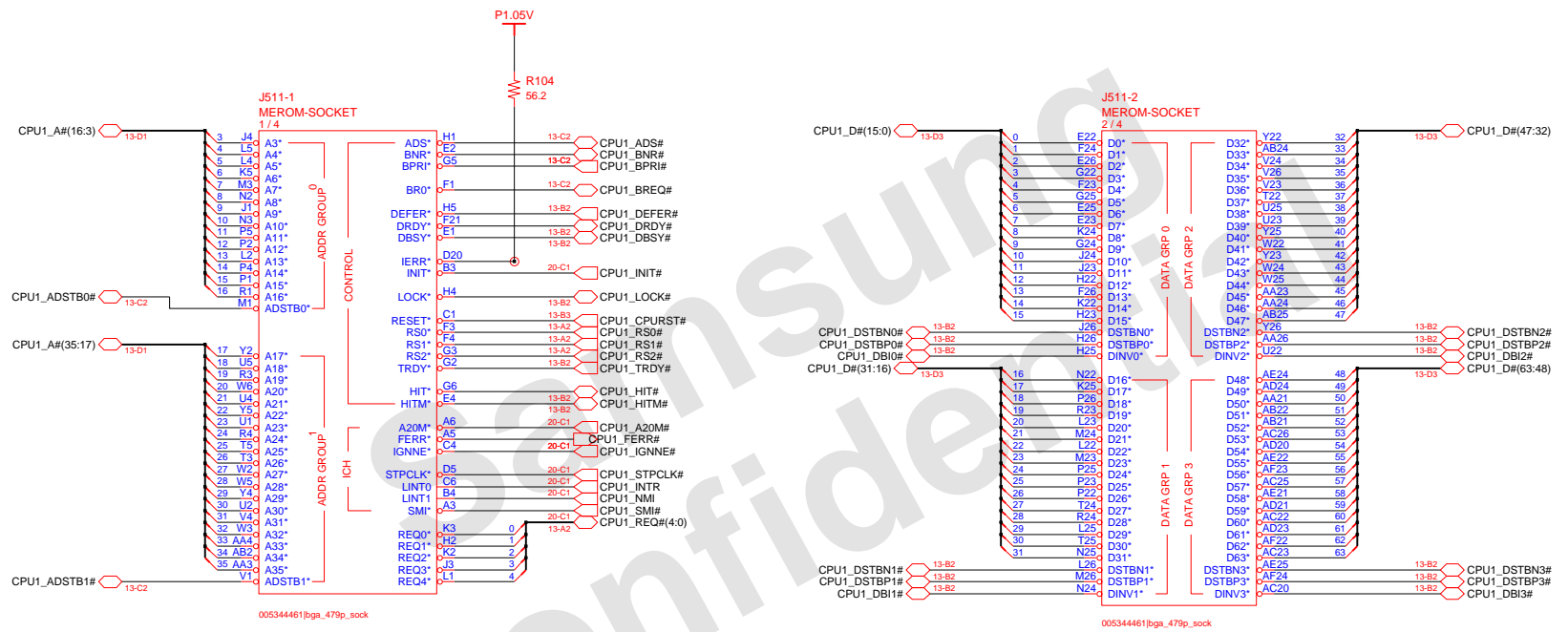
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MODULE CODE	undef ined	LAST EDIT	October 10, 2006 20:28:50 PM	PAGE	1 OF 1	

THERMAL SENSOR & FAN CONTROL



DRAW	TF Member	DATE	8/12/2006	TITLE	LIB	SAMSUNG ELECTRONICS PART NO. BA41-#####A
CHECK	TF Member	DEV. STEP	DVT	thermal_Sensor_SMSC_Emc2102		
APPROVAL	TF Member	REV	0.8	thermal_Sensor_SMSC_Emc2102		
MODULE CODE		LAST EDIT	October 10, 2006 20:56:52 PM			
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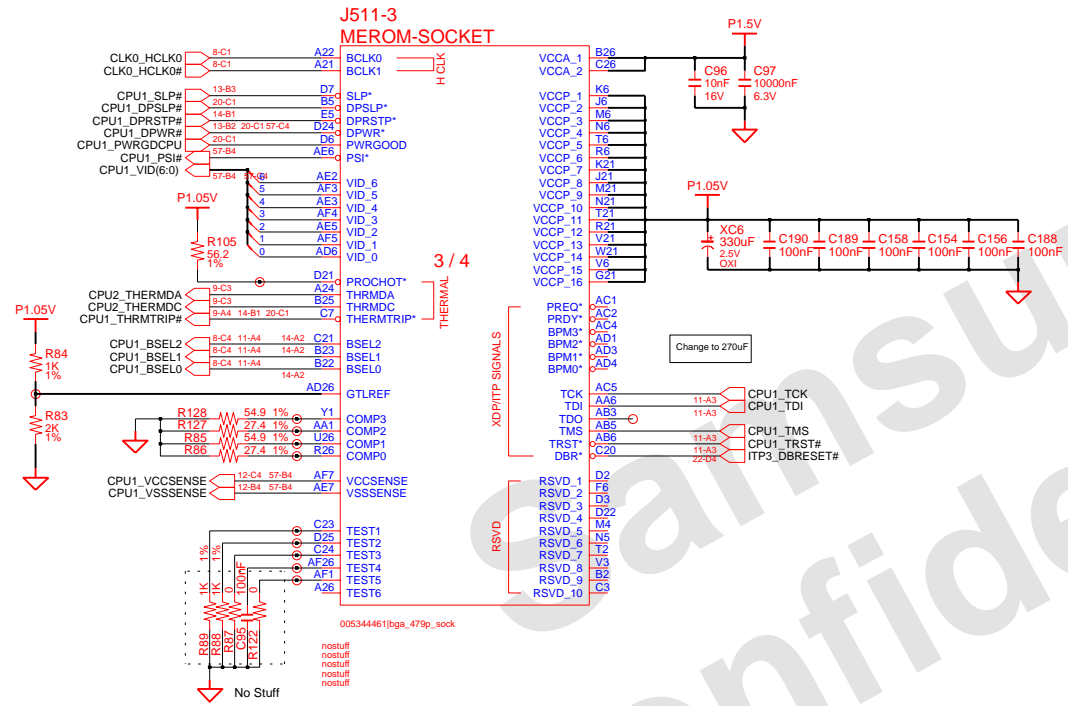
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MODULE CODE	undef ined	LAST EDIT	October 13, 2006 13:49:51 PM	PAGE	1	OF 3

CPU Core Voltage Table IMVP-6

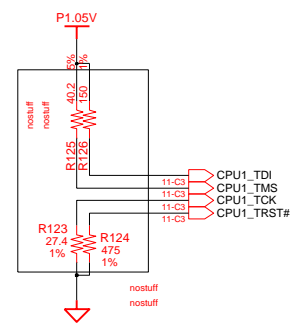
Active Mode		Active/Deeper Sleep Dual Mode Region		Deeper Sleep/Extended Deeper Sleep Dual Mode Region	
VID(6:0)	Voltage	VID(6:0)	Voltage	VID(6:0)	Voltage
0 0 0 0 0 0 0	1.5000 V	0 1 0 1 0 0 0	1.0000 V	1 0 1 0 0 0 0	0.4875 V
0 0 0 0 0 0 1	1.4875 V	0 1 0 1 0 0 1	0.9875 V	1 0 1 0 0 1 0	0.4750 V
0 0 0 0 0 1 0	1.4750 V	0 1 0 1 0 1 0	0.9750 V	1 0 1 0 0 1 1	0.4625 V
0 0 0 0 0 1 1	1.4625 V	0 1 0 1 0 1 1	0.9625 V	1 0 1 0 1 0 0	0.4500 V
0 0 0 0 1 0 0	1.4500 V	0 1 0 1 1 0 0	0.9500 V	1 0 1 0 1 0 1	0.4375 V
0 0 0 0 1 0 1	1.4375 V	0 1 0 1 1 0 1	0.9375 V	1 0 1 0 1 1 0	0.4250 V
0 0 0 0 1 1 0	1.4250 V	0 1 0 1 1 1 0	0.9250 V	1 0 1 0 1 1 1	0.4125 V
0 0 0 1 0 0 0	1.4125 V	0 1 1 0 0 0 0	0.9125 V	1 0 1 1 0 0 0	0.4000 V
0 0 0 1 0 0 1	1.4000 V	0 1 1 0 0 0 1	0.9000 V	1 0 1 1 0 0 1	0.3875 V
0 0 0 1 0 1 0	1.3875 V	0 1 1 0 0 1 0	0.8875 V	1 0 1 1 0 1 0	0.3750 V
0 0 0 1 0 1 1	1.3750 V	0 1 1 0 0 1 1	0.8750 V	1 0 1 1 0 1 1	0.3625 V
0 0 0 1 1 0 0	1.3625 V	0 1 1 0 1 0 0	0.8625 V	1 0 1 1 1 0 0	0.3500 V
0 0 0 1 1 0 1	1.3500 V	0 1 1 0 1 0 1	0.8500 V	1 0 1 1 1 0 1	0.3375 V
0 0 0 1 1 1 0	1.3375 V	0 1 1 0 1 1 0	0.8375 V	1 0 1 1 1 1 0	0.3250 V
0 0 0 1 1 1 1	1.3250 V	0 1 1 1 0 0 0	0.8250 V	1 0 1 1 1 1 1	0.3125 V
0 0 1 0 0 0 0	1.3125 V	0 1 1 1 0 0 1	0.8125 V	1 0 1 1 0 0 0	0.3000 V
0 0 1 0 0 0 1	1.3000 V	0 1 1 1 0 0 1	0.8000 V	1 1 1 0 0 0 0	0.2875 V
0 0 1 0 0 1 0	1.2875 V	0 1 1 1 0 1 0	0.7875 V	1 1 1 0 0 0 1	0.2750 V
0 0 1 0 0 1 1	1.2750 V	0 1 1 1 1 0 0	0.7750 V	1 1 1 0 0 0 1	0.2625 V
0 0 1 0 1 0 0	1.2625 V	0 1 1 1 1 0 1	0.7625 V	1 1 1 0 0 1 0	0.2500 V
0 0 1 0 1 0 1	1.2500 V	0 1 1 1 1 0 1	0.7500 V	1 1 1 0 0 1 1	0.2375 V
0 0 1 0 1 1 0	1.2375 V	0 1 1 1 1 1 0	0.7375 V	1 1 1 0 0 1 1	0.2250 V
0 0 1 0 1 1 1	1.2250 V	0 1 1 1 1 1 1	0.7250 V	1 1 1 0 0 1 1	0.2125 V
0 0 1 1 0 0 0	1.2125 V	0 1 1 1 1 1 1	0.7125 V	1 1 1 0 0 0 0	0.2000 V
0 0 1 1 0 0 1	1.2000 V	1 0 0 0 0 0 0	0.7000 V	1 1 1 0 0 0 1	0.1875 V
0 0 1 1 0 1 0	1.1875 V	1 0 0 0 0 0 1	0.6875 V	1 1 1 0 0 1 0	0.1750 V
0 0 1 1 0 1 1	1.1750 V	1 0 0 0 0 1 0	0.6750 V	1 1 1 0 0 1 1	0.1625 V
0 0 1 1 1 0 0	1.1625 V	1 0 0 0 0 1 1	0.6625 V	1 1 1 0 1 0 0	0.1500 V
0 0 1 1 1 0 1	1.1500 V	1 0 0 0 1 0 0	0.6500 V	1 1 1 0 1 0 1	0.1375 V
0 0 1 1 1 1 0	1.1375 V	1 0 0 0 1 0 1	0.6375 V	1 1 1 0 1 1 0	0.1250 V
0 0 1 1 1 1 1	1.1250 V	1 0 0 0 1 1 0	0.6250 V	1 1 1 0 1 1 1	0.1125 V
0 0 1 1 1 1 1	1.1125 V	1 0 0 0 1 1 1	0.6125 V	1 1 1 1 0 0 0	0.1000 V
0 1 0 0 0 0 0	1.1000 V	1 0 0 0 1 1 0	0.6000 V	1 1 1 1 0 0 1	0.0875 V
0 1 0 0 0 0 1	1.0875 V	1 0 0 0 1 1 0	0.5875 V	1 1 1 1 0 1 0	0.0750 V
0 1 0 0 0 1 0	1.0750 V	1 0 0 0 1 1 1	0.5750 V	1 1 1 1 0 1 1	0.0625 V
0 1 0 0 0 1 1	1.0625 V	1 0 0 0 1 1 1	0.5625 V	1 1 1 1 1 0 0	0.0500 V
0 1 0 0 1 0 0	1.0500 V	1 0 0 0 1 1 0	0.5500 V	1 1 1 1 1 0 1	0.0375 V
0 1 0 0 1 0 1	1.0375 V	1 0 0 0 1 1 0	0.5375 V	1 1 1 1 1 1 0	0.0250 V
0 1 0 0 1 1 0	1.0250 V	1 0 0 1 1 1 0	0.5250 V	1 1 1 1 1 1 1	0.0125 V
0 1 0 0 1 1 1	1.0125 V	1 0 0 1 1 1 1	0.5125 V	1 1 1 1 1 0 0	0.0000 V
0 1 0 0 1 1 1	1.0125 V	1 0 0 1 1 0 0	0.5000 V	1 1 1 1 1 0 1	0.0000 V
		1 0 0 1 1 0 1	0.0000 V	1 1 1 1 1 1 0	0.0000 V
		1 0 0 1 1 1 0	0.0000 V	1 1 1 1 1 1 1	0.0000 V
		1 0 0 1 1 1 1	0.0000 V		

Active: DPRSLPVR 0, DPRSTP* 1, PSI2* 0 or 1
 Deeper Slp: DPRSLPVR 1, DPRSTP* 0, PSI2* 0 or 1

***11111111** : 0V power good asserted.



ITP DISABLE



GTLREF : Keep the Voltage divider within 0.5" of the first GTLREF0 pin with Zo=55ohm trace. Minimize coupling of any switching signals to this net.

COMP0,2(COMP1,3) should be connected with Zo=27.4ohm(55ohm) trace shorter than 1/2" to their respective Banias socket pins.

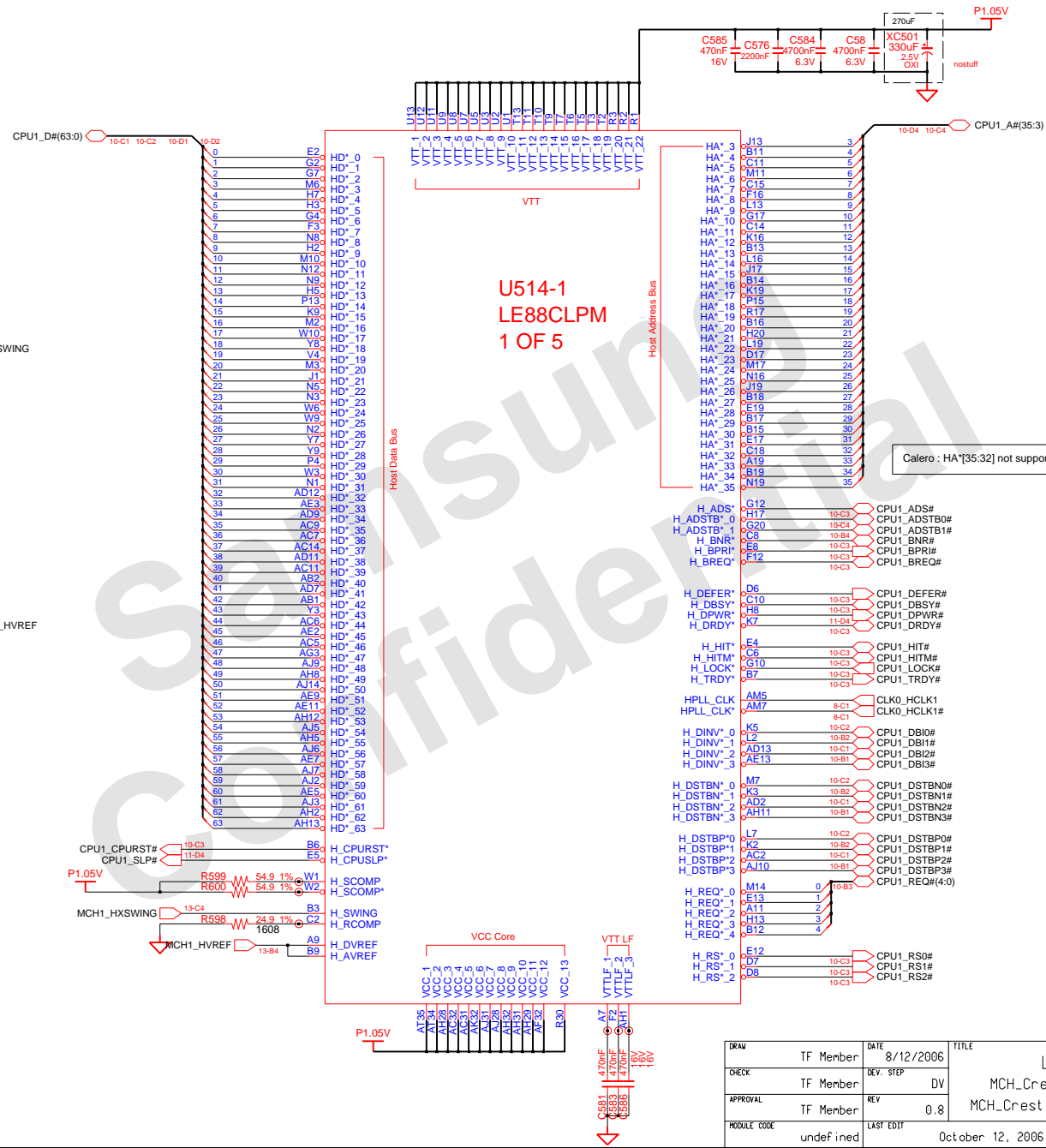
GND test points within 100mil of the VCC/VSSsense at the end of the line. Route the VCC/VSSsense as a Zo=55ohm traces with equal length. Observe 3:1 spacing b/w VCC/VSSsense lines and 25mil away (preferred 50mil) from any other signal. And GND via 100mil away from each of the VCC/VSS test point vias.

*Yonah Processor (2.33 GHz / 800 MHz : TBD)

DRAW	TF Member	DATE	8/12/2006	TITLE	LIB	SAMSUNG ELECTRONICS
CHECK	TF Member	DEV. STEP	DV	CPU_Merom_SR_SV		
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Calero : HA[35:32] not support

DRAW	TF Member	DATE	8/12/2006	TITLE	LIB	SAMSUNG ELECTRONICS
CHECK	TF Member	DEV. STEP	DV	MCH_Crestline_PM		
APPROVAL	TF Member	REV	0.8	MCH_Crestline_PM(1/5)		PART NO. BA41-#####A
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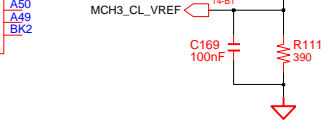
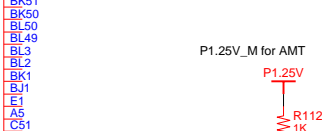
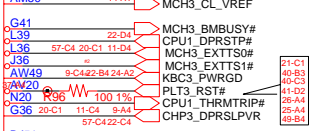
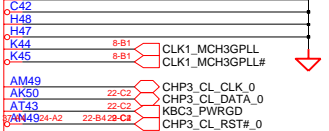
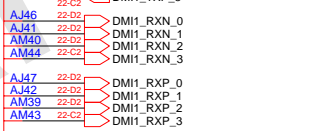
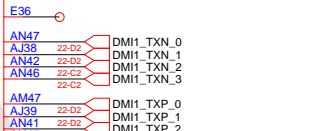
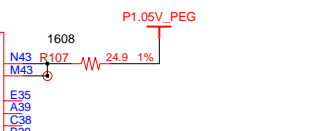
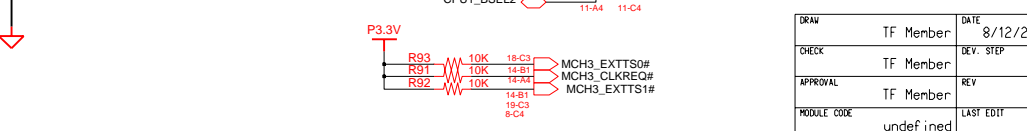
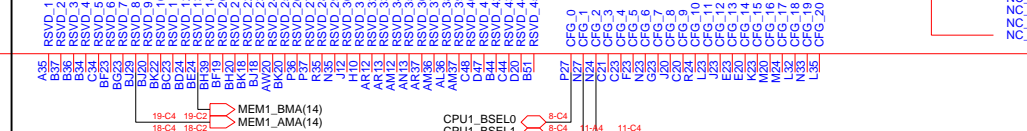
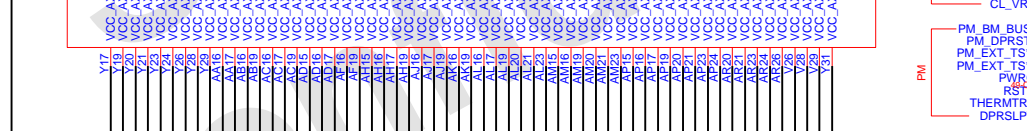
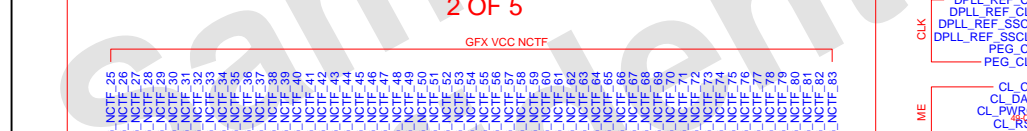
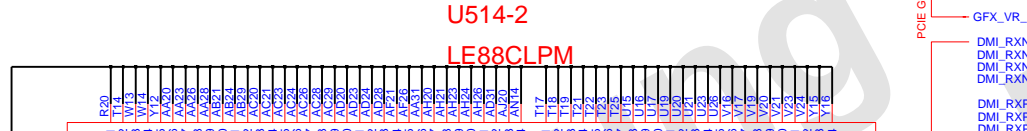
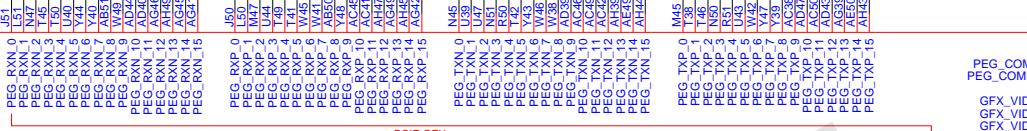
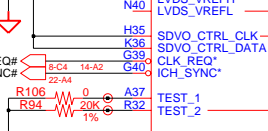
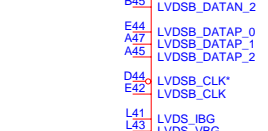
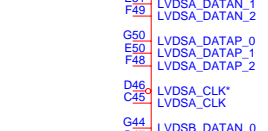
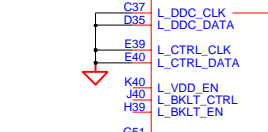
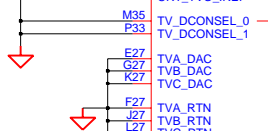
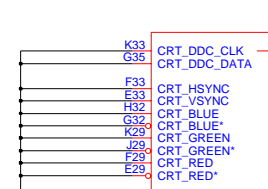
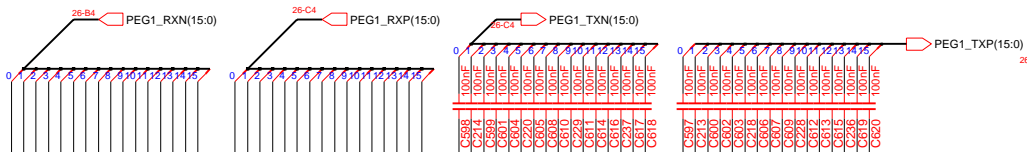
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D

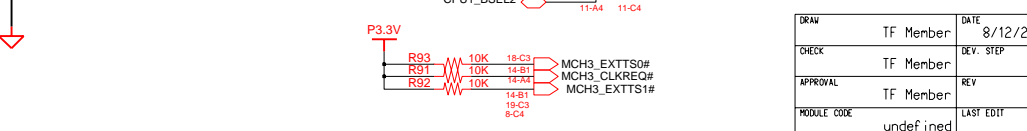
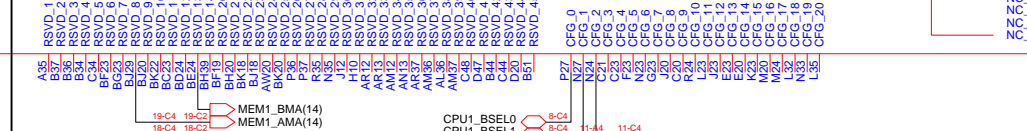
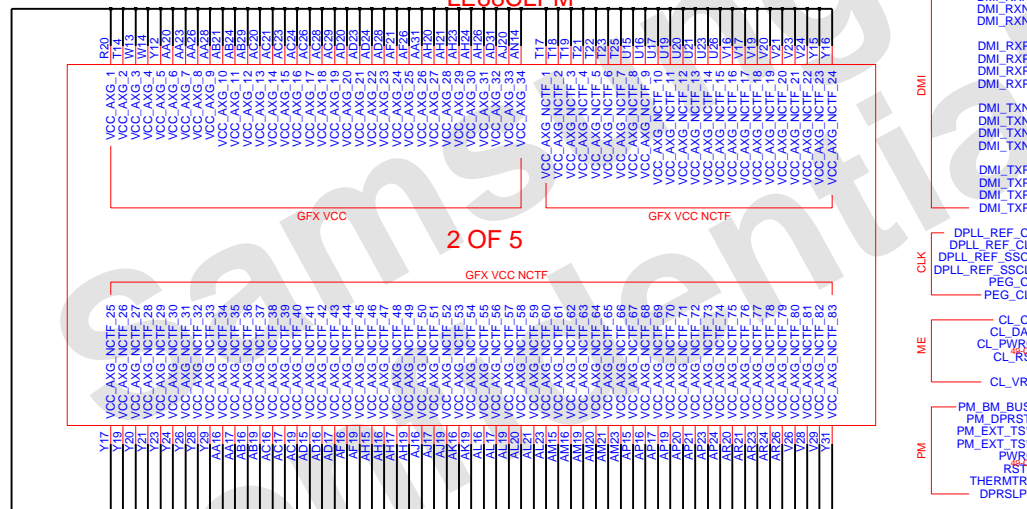
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B

A



U514-2 LE88CLPM



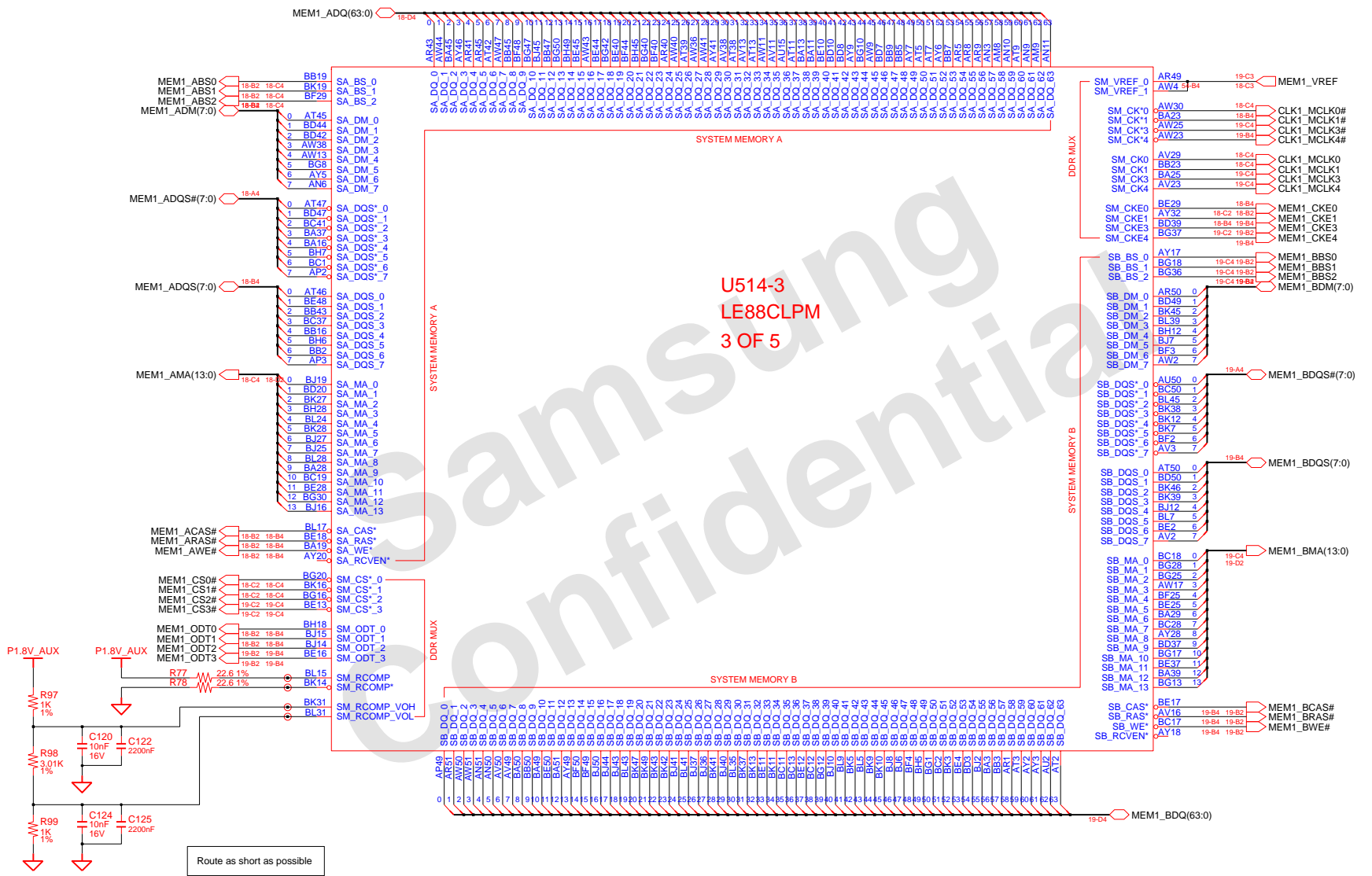
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APPROVAL	TF Member	REV	0.8	MCH_Crestline_PM(2/5)		PART NO. BA41-####A
MODULE CODE	undef in ed	LAST EDIT	October 12, 2006 10:33:14 AM	PAGE	2 OF 5	

D

C

B

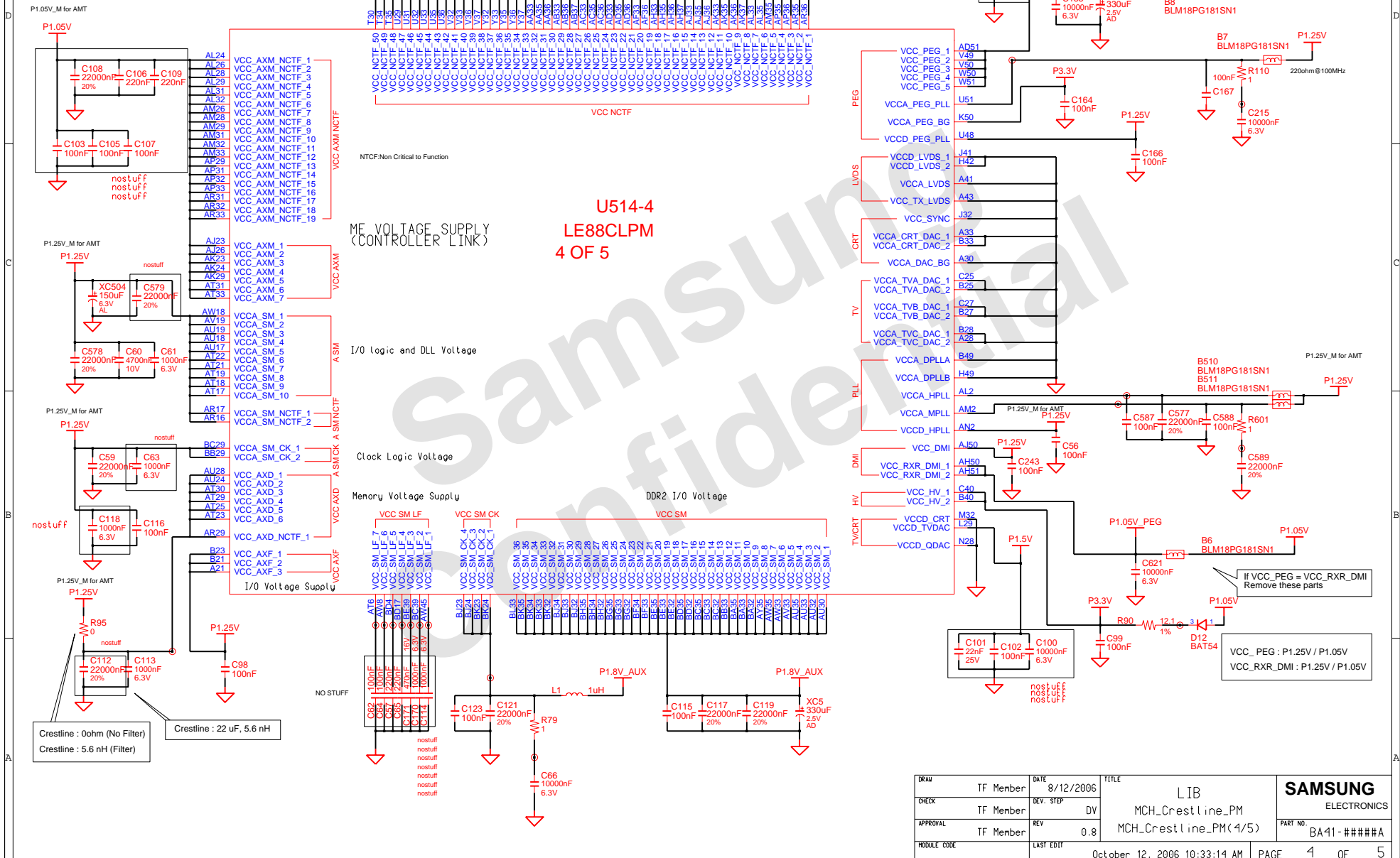
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U514-3
 LE88CLPM
 3 OF 5

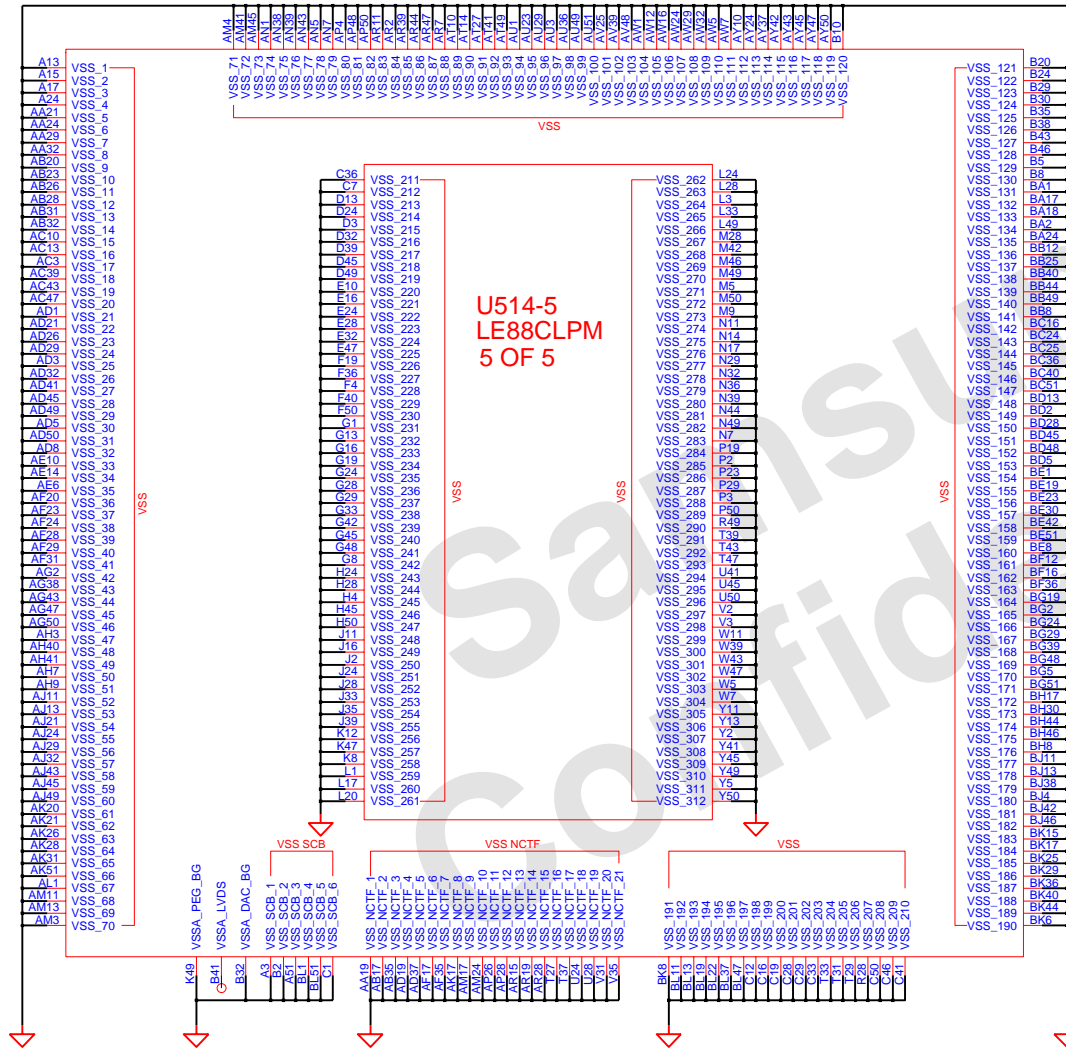
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APPROVAL	TF Member	REV	0.8	MCH_Crestline_PM(3/5)	PART NO.	BA41-#####A
MODULE CODE		LAST EDIT		October 12, 2006 10:33:14 AM	PAGE	3 OF 5

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*POCAFEB-11 Only (Remove in MP Model)

CFG#	Current Setting (def.: default Option)	
	Low	High
CFG(5)	DMix2	DMix4 (def.)
CFG(6)	Reserved	DDR-II (def.)
CFG(7)	DT/Transportable	Mobile CPU (def.)
CFG(9)	PEG Reversal	Normal
CFG(16)	Dynamic ODT	Dynamic ODT
	Disabled	Enabled (def.)
CFG(18)	VCC 1.05V (def.)	VCC 1.5V
CFG(19)	DMI Lane Normal	DMI Lane Reversal
CFG(20)	SDVO or PCIE X1 Only(def.)	SDVO and PCIE X1 Simultaneously

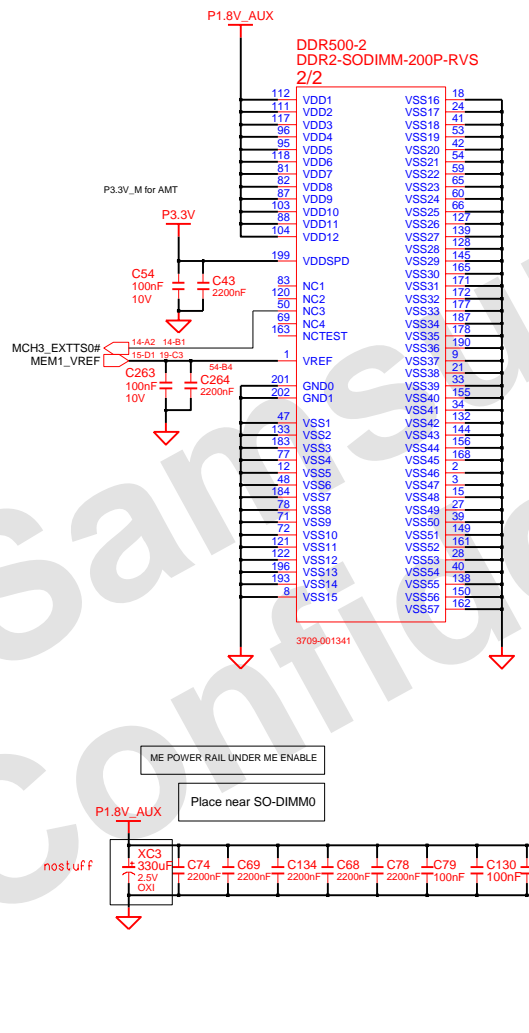
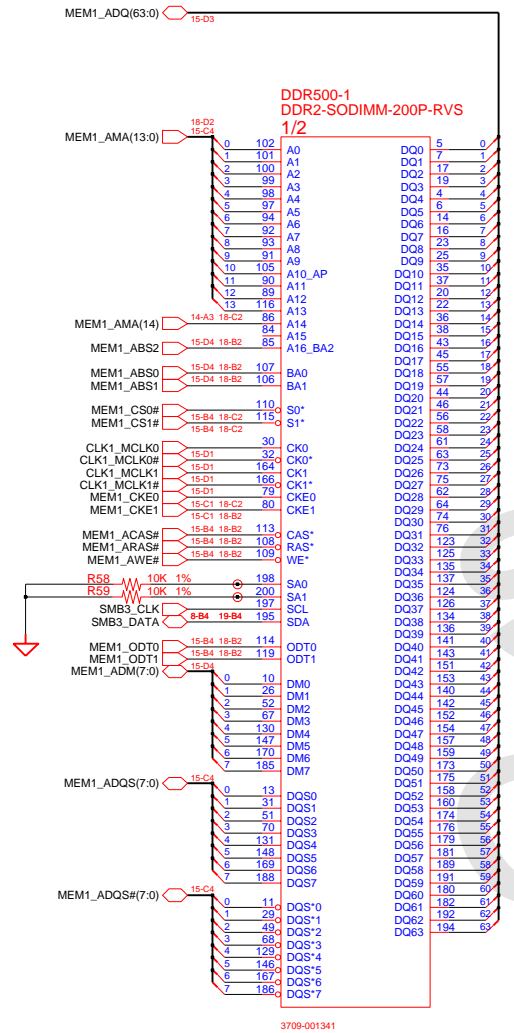
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APPROVAL	TF Member	REV	0.8	MCH_CrestLine_PM(5/5)		BA41-#####A	
MODULE CODE		LAST EDIT	October 12, 2006 10:33:14 AM		PAGE	5	OF 5

DDR SO-DIMM #0

D
C
B
A

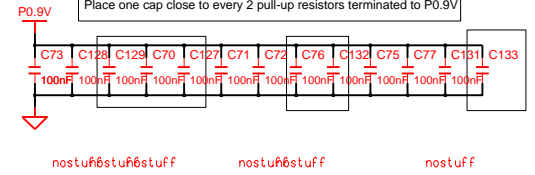
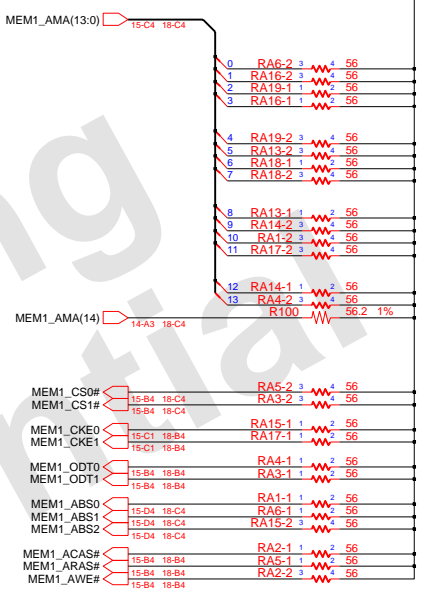
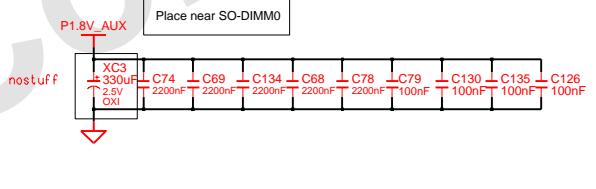
ME POWER RAIL UNDER ME ENABLE

Array resistors & Single resistors used to improve layout & routing.



ME POWER RAIL UNDER ME ENABLE

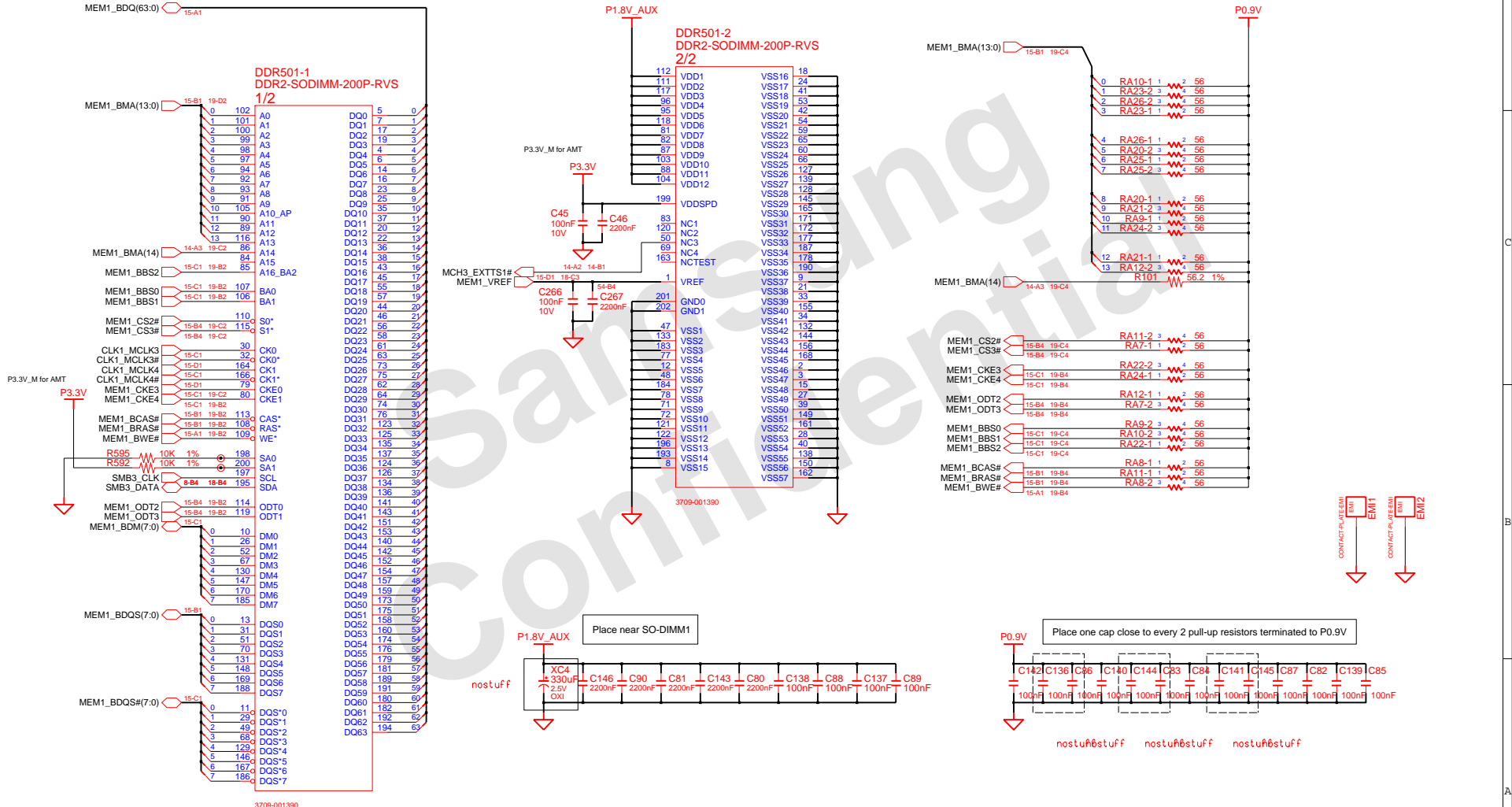
Place one cap close to every 2 pull-up resistors terminated to P0.9V



DRAW	TF Member	DATE	8/12/2006	TITLE	LIB		SAMSUNG ELECTRONICS
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MODULE CODE		LAST EDIT	October 10, 2006 20:55:25 PM	PAGE	1	OF	

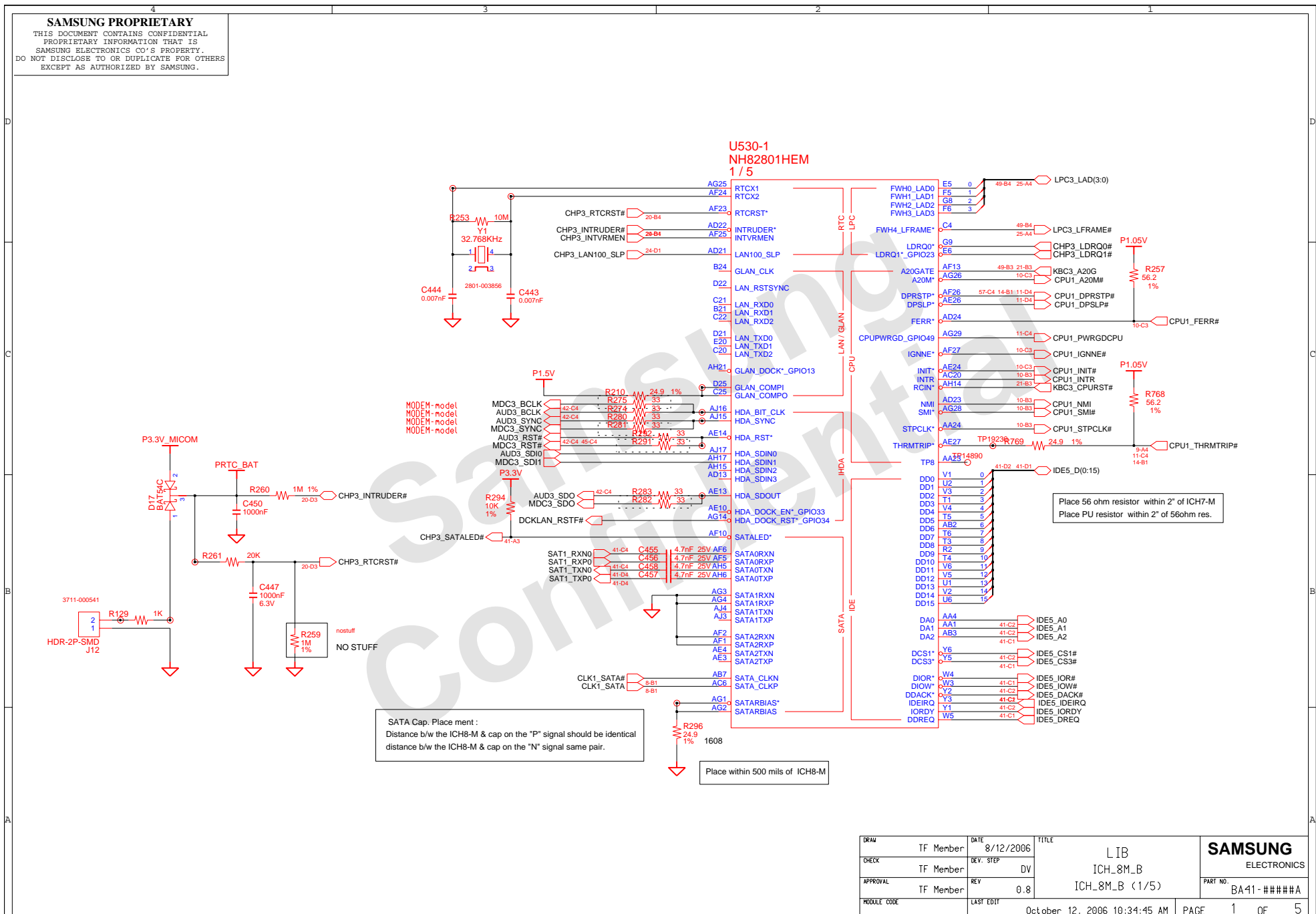
DDR SO-DIMM #1

Array resistors & Single resistors used to improve layout & routing.



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CHECK	TF Member	DEV. STEP	DV	SODIMM_DDR2		
APPROVAL	TF Member	REV	0.8	SODIMM_DDR2 #2		
MODULE CODE		LAST EDIT	October 10, 2006 20:55:25 PM	PAGE	2 OF 2	

**U530-1
 NH82801HEM
 1 / 5**



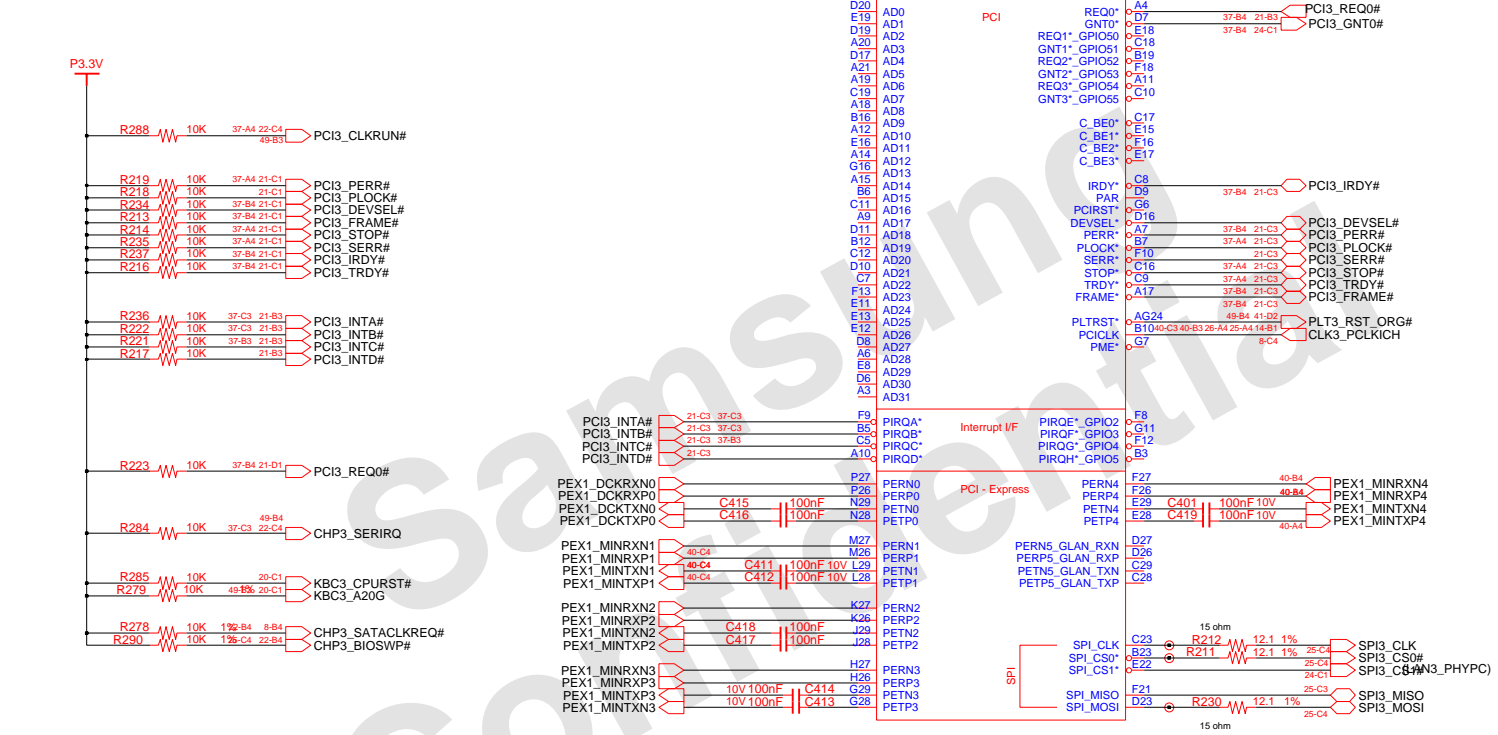
SATA Cap. Place ment :
 Distance b/w the ICH8-M & cap on the "P" signal should be identical
 distance b/w the ICH8-M & cap on the "N" signal same pair.

Place within 500 mils of ICH8-M

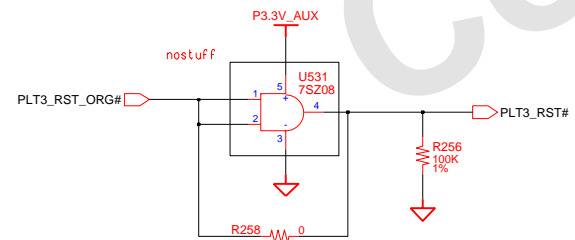
Place 56 ohm resistor within 2" of ICH7-M
 Place PU resistor within 2" of 56ohm res.

DRAW	TF Member	DATE	8/12/2006	TITLE	LIB	SAMSUNG ELECTRONICS
CHECK	TF Member	DEV. STEP	DV	ICH_8M_B		
APPROVAL	TF Member	REV	0.8	ICH_8M_B (1/5)		PART NO. BA41-#####A
MODULE CODE		LAST EDIT		October 12, 2006 10:34:45 AM	PAGE	1 OF 5

U530-2
NH82801HEM
2/5



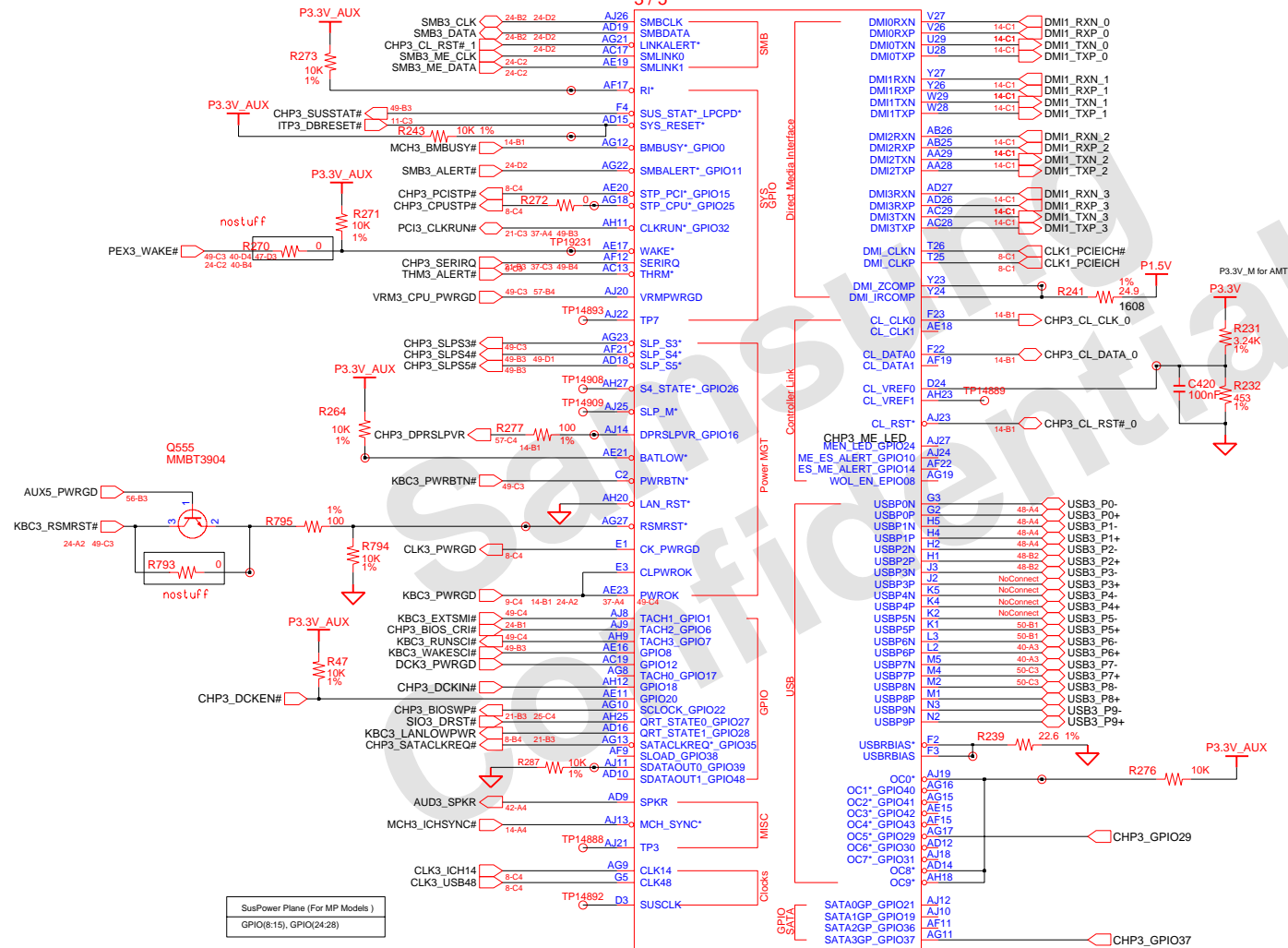
AC caps : PCIe need to be within 250mils of the driver
 Resistor for Test : Place Stuffing Option to minimize stubs



DRAW	TF Member	DATE	8/12/2006	TITLE	LIB	SAMSUNG ELECTRONICS
CHECK	TF Member	DEV. STEP	DV	ICH_8M_B		
APPROVAL	TF Member	REV	0.8	ICH_8M_B (2/5)		PART NO. BA41-#####A
MODULE CODE	undef ined	LAST EDIT	October 12, 2006 10:34:45 AM	PAGE	2	OF 5

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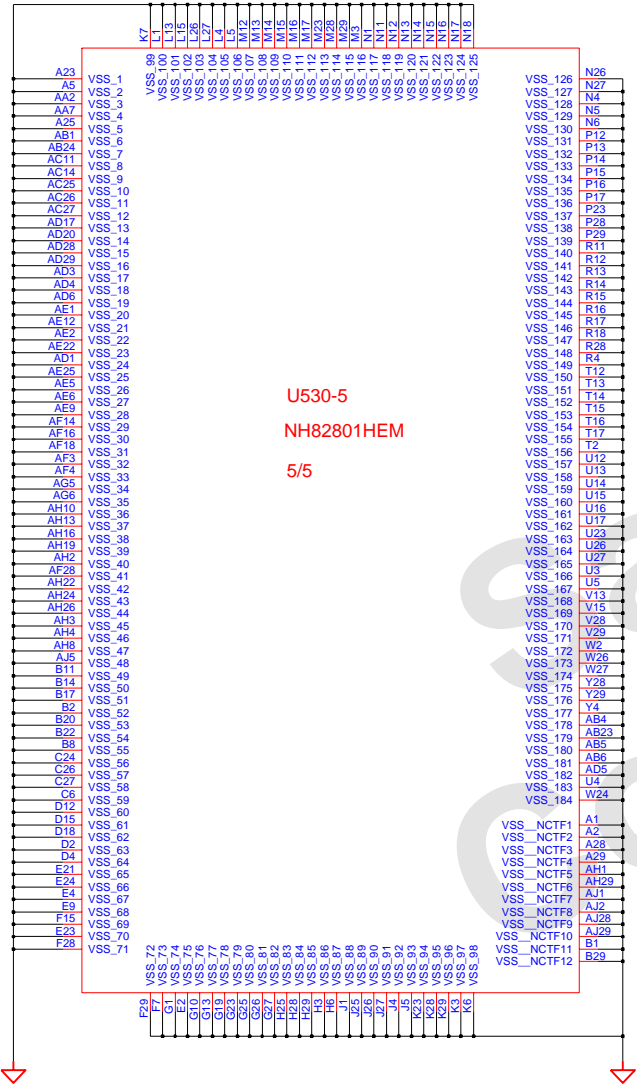
**U530-3
 NH82801HEM
 3/5**



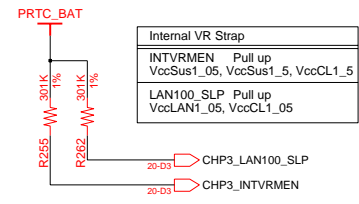
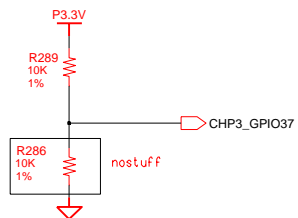
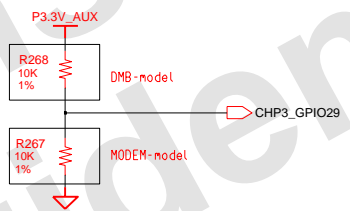
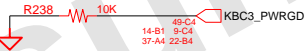
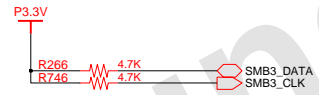
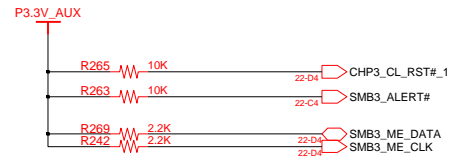
SusPower Plane (For MP Models)
 GPIO(8:15), GPIO(24:28)

DRAW	TF Member	DATE	8/12/2006	TITLE	LIB	SAMSUNG ELECTRONICS PART NO. BA41-#####A
CHECK	TF Member	DEV. STEP	DV	ICH_8M_B		
APPROVAL	TF Member	REV	0.8	ICH_8M_B (3/5)		
MODULE CODE		LAST EDIT	October 12, 2006 10:34:45 AM	PAGE	3 OF 5	

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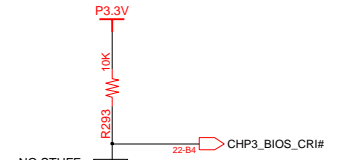
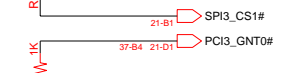


U530-5
 NH82801HEM
 5/5



Boot BIOS Select

BIOS	PCI3_GNT0*	SPI3_CS1*
LPC	HIGH	HIGH
SPI	LOW	HIGH
PCI	HIGH	LOW



BIOS CRISIS RECOVER STRAP
 PLACE NEAR KEYBOARD

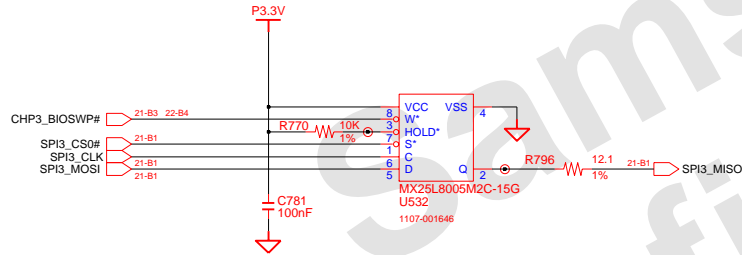
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CHECK	TF Member	DEV. STEP	DV		ICH_8M_B		
APPROVAL	TF Member	REV	0.8		ICH_8M_B (5/5)	PART NO. BA41-#####A	
MODULE CODE		LAST EDIT	October 12, 2006 10:34:45 AM	PAGE	5	OF	5

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- SPI ROM LIST -

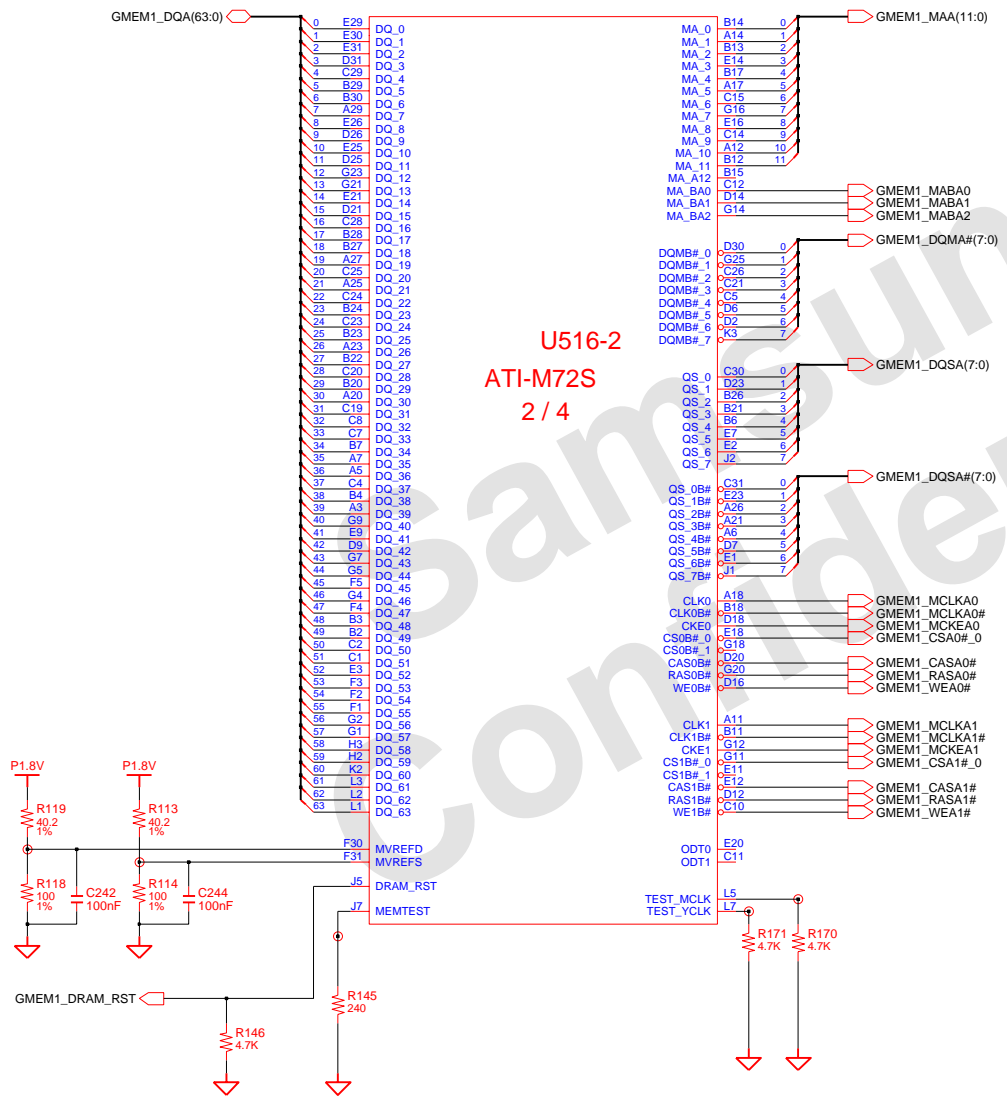
- ▶ Macronix - MX25L8005M2C-15G
- ▶ STM - M25PE80
- ▶ ATMEL - AT26DF081A-SU
- SST - 25VF080B-50-4C-S2AF
- WINBOND - W25X80-VSSI-G



- | | |
|---|------------------------------------|
| 02 VERIFY REAL MODE | 66 CONFIGURE ADVANCE CACHE REG. |
| 03 DISABLE NMI | 6A DISPLAY EXTERNAL CACHE SIZE |
| 04 GET CPU TYPE | 6C DISPLAY SHADOW MESSAGE |
| 06 INIT. SYSTEM H/W | 6E DISPLAY NON-DISPOSABLE SEGMENT |
| 08 INIT. CHIPSET REG. | 70 DISPLAY ERROR MESSAGE |
| 09 SET IN POST FLAG | 72 CHECK FOR CONFIGURATION ERROR |
| 0A INIT CPU.REG | 74 TEST REAL-TIME CLOCK |
| 0B CPU CACHE ON | 76 CHECK FOR KEYBOARD EERROR |
| 0C INIT.CACHE TO POST | 7C SETUP HARDWARE INTERRUPT VECTOR |
| 0E INIT. I/O VALUE | 7E TEST COPROCESSER IF PRESENT |
| 0F ENABLE THE L-BUS IDE | 80 DISABLE ON-BOARD I/O PORT |
| 10 INIT. POWER MANAGER | 82 DETECT AND INSTALL EXT.RS232C |
| 11 LOAD ALTERNATE REG. | 84 DETECT AND INSTALL EXT.PARALLEL |
| 13 PCI BUS MASTER RESET WITH INITIAL POST VALUE | 86 RE-INIT. ON-BOARD I/O PORT |
| 14 INIT. KEYBOARD CONTROLLER | 88 INIT. BIOS DATA ROM |
| 16 CHECK CHECKSUM | 8A INIT.EXTENDED BIOS DATA AREA |
| 18 8254 TIMER INIT. | 8C INIT. FDD CONTROLLER |
| 1A 8237 DMA CONTROLLER INIT. | 9A SHADOW OPTION ROMS |
| 1C RESET INTERRUPT CONTROLLER | 9C SETUP POWER MANAGEMENT |
| 20 TEST DRAM REFRESH | 9E ENABLE H/W INTERRUPT |
| 22 TEST 8742 KEYBOARD CONTROLLER | A0 SET TIME OF DAY |
| 24 SET ES SEGMENT REG. TO 4GB | A4 INIT. TYPEMATIC RATE |
| 26 ENABLE A20 | A8 ERASE F2 PROMPT |
| 28 AUTO SIZING DRAM | AA SCAN FOR F2 KEY STROKE |
| 32 COMPUTE THE CPU SPEED | AC ENTER SETUP |
| 34 TESET CMOS RAM | AE CLEAR IN POST FLAG |
| 38 SHADOW SYSTEM BIOS ROM | B0 CHECK FOR ERRORS |
| 3A AUTO SIZING CACHE | B2 POST DONE-PREPARE TO BOOT O/S |
| 3C CONFIGURE ADVANCED CHIPSET REG. | B4 ONE BEEP |
| 3D LOAD ALTER REG. WITH CMOS VALUE | B6 CHECK PASSWORD (OPTION) |
| 42 INIT. INTERRUPT VECTOR | B7 ACPI INIT |
| 44 INIT. BIOS INTERRUPT | BE CLEAR SCREEN |
| 46 CHECK ROM COPYRIGHT NOTICE | C0 TRY BOOT WITH INT19 |
| 47 INIT. I20 SUPPORT IF INSTALLED | D0 INTERRUPT HANDLER ERROR |
| 48 CHECK VIDEO CONFIGURE AGAINST CMOS | D2 UNKNOWN INTERRUPT ERROR |
| 49 INIT. PCI BUS AND DEVICE | D4 PENDING INTERRUPT ERROR |
| 4A INIT. ALL VIDEO BIOS ROM | D6 SHUTDOWN 5 |
| 4C SHADOW VIDEO BIOS ROM | D8 SHUTDOWN ERROR |
| 50 DISPLAY CPU TYPE AND SPEED | DA EXTENDED BLOCK MOVE |
| 52 TEST KEYBOARD | DC SHUTDOWN 10 |
| 54 SET KEYCLICK IF ENABLED | 89 ENABLE NMI |
| 56 ENABLE KEYBOARD | 90 INIT. HDD CONTROLLER |
| 58 TEST FOR UNEXPECTED INTERRUPTS | 91 INIT. LOCAL BUS HDD CONTROLLER |
| 5A DISPLAY * PRESS SETUP* | 92 JUMP TO USER PATCH 2 |
| 5C TEST RAM BETWEEN 512K AND 640K | 94 DISABLE A20 ADDRESS LINE |
| 60 TEST EXTENDED MEMORY | 96 CLEAR HUGE ES SEGMENT REG. |
| 62 TEST EXTENDED MEMORY ADDRESS LINE | 98 SEARCH FOR OPTION ROMS |
| 64 JUMP TO USER PATCH 1 | |

DRAW	TF Member	DATE	8/12/2006	TITLE	LIB	SAMSUNG ELECTRONICS PART NO. BA41-#####A
CHECK	TF Member	DEV. STEP	DV	SPI_LIBIOS_ROM		
APPROVAL	TF Member	REV	0.8	SPI_LIBIOS_ROM		
MODULE CODE		LAST EDIT	October 10, 2006 20:56:20 PM	PAGE	1 OF 1	

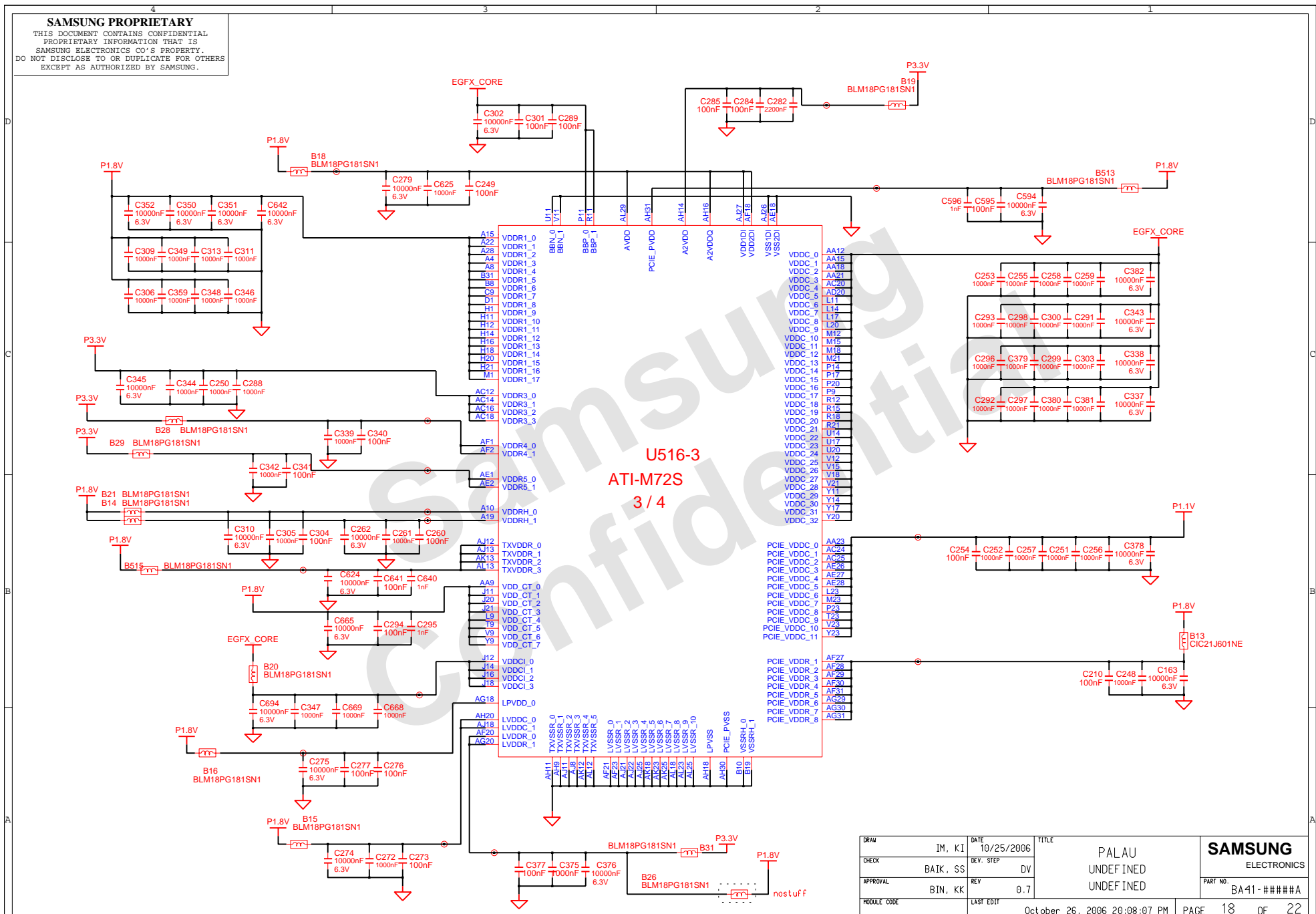
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DRAW	IM, KI	DATE	10/25/2006	TITLE	PALAU UNDEFINED	SAMSUNG ELECTRONICS
CHECK	BAIK, SS	DEV. STEP	DV			
APPROVAL	BIN, KK	REV	0.7		UNDEFINED	PART NO. BA41-#####A
MODULE CODE		LAST EDIT	October 26, 2006 20:08:07 PM	PAGE	17	OF 22

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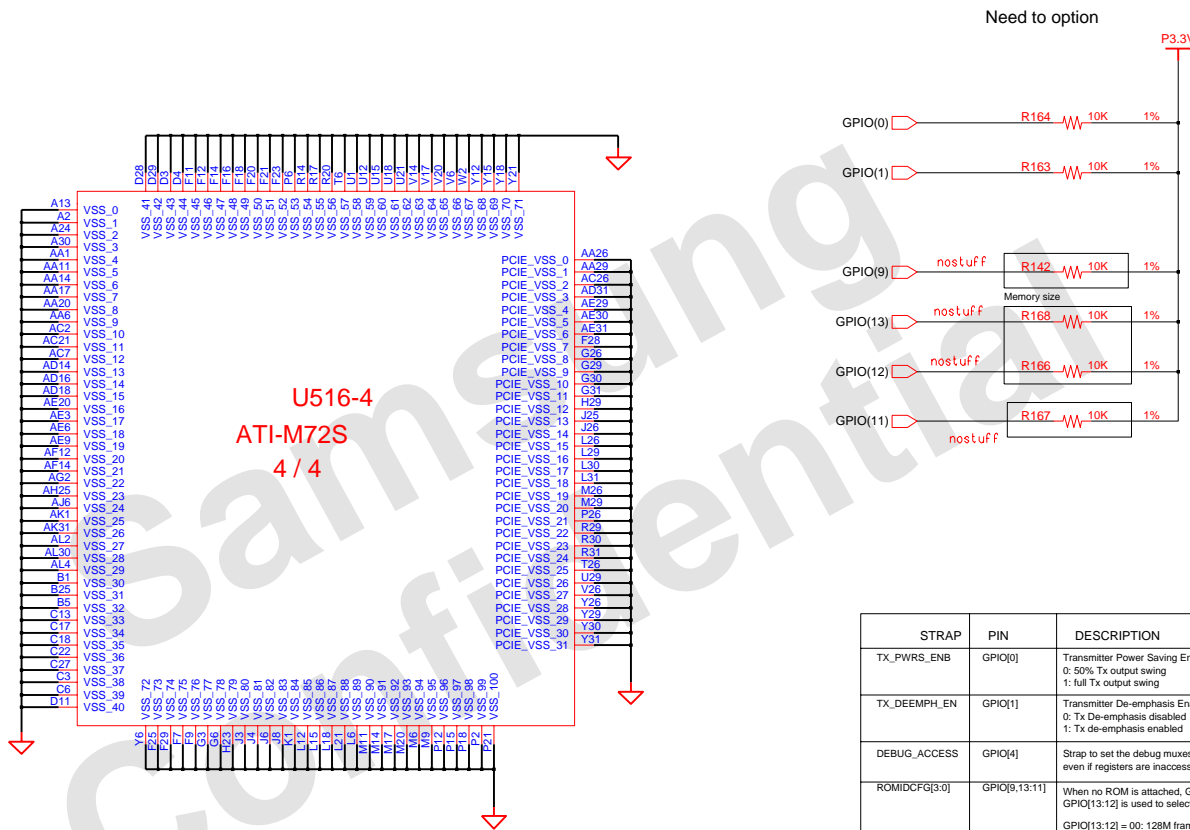
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U16-3
ATI-M72S
3 / 4

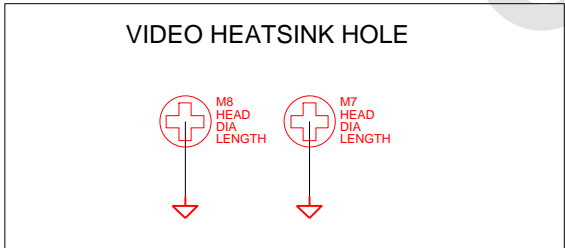
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CHECK	BAIK, SS	DEV. STEP	DV		UNDEFINED	
APPROVAL	BIN, KK	REV	0.7			PART NO. BA41-#####A
MODULE CODE		LAST EDIT	October 26, 2006 20:08:07 PM	PAGE	18	OF 22

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(DEFAULT : pull-down)

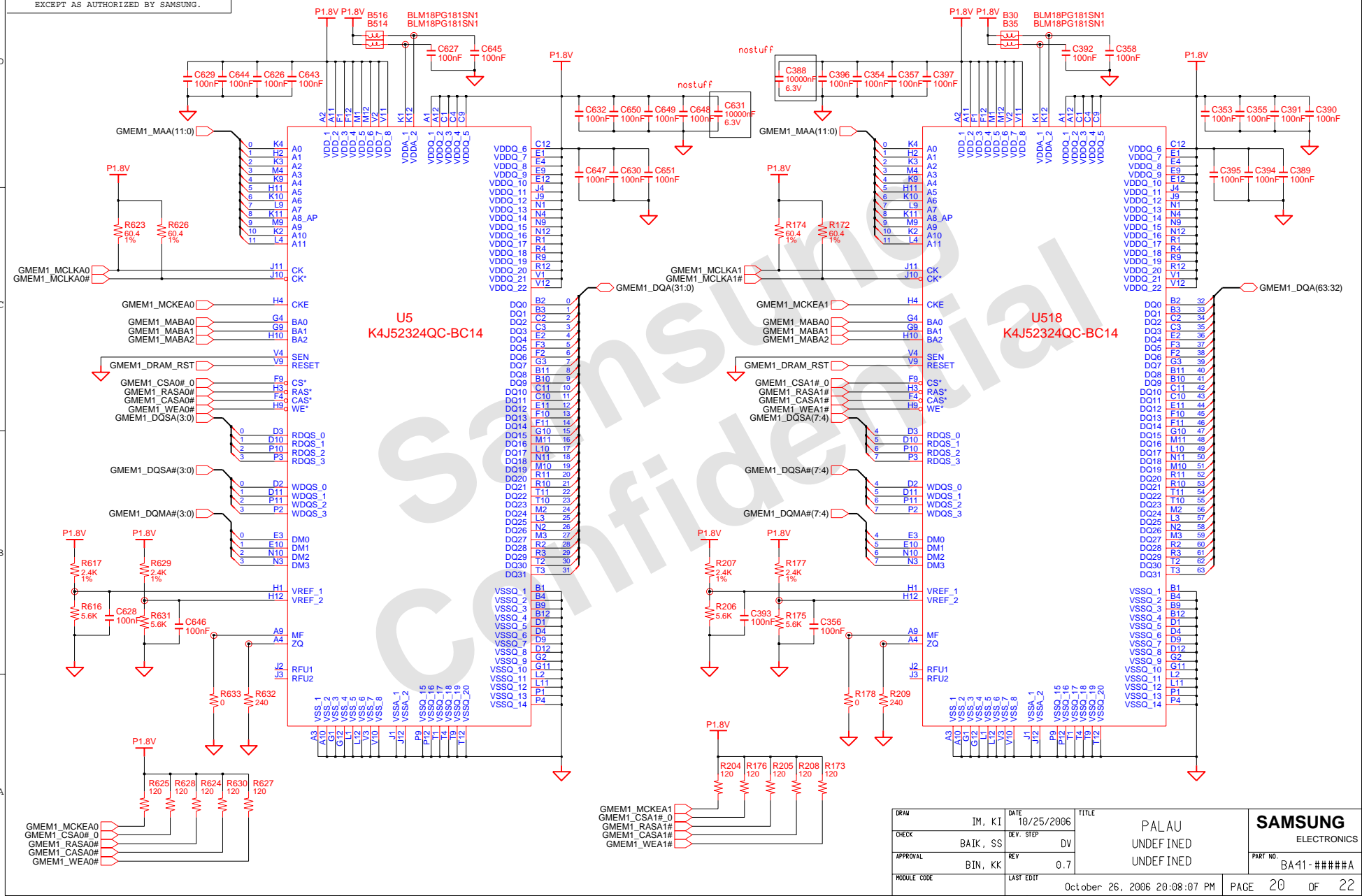
STRAP	PIN	DESCRIPTION
TX_PWRS_ENB	GPIO[0]	Transmitter Power Saving Enable 0: 50% Tx output swing 1: full Tx output swing
TX_DEEMPH_EN	GPIO[1]	Transmitter De-emphasis Enable 0: Tx De-emphasis disabled 1: Tx de-emphasis enabled
DEBUG_ACCESS	GPIO[4]	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible.
ROMIDCFG[3:0]	GPIO[9,13:11]	When no ROM is attached, GPIO[9] is set to 0. GPIO[13:12] is used to select the frame buffer aperture size. GPIO[13:12] = 00: 128M frame buffer GPIO[13:12] = 01: 256M frame buffer GPIO[13:12] = 10: 64M frame buffer GPIO[13:12] = 11: reserved



DRAW	IM, KI	DATE	10/25/2006	TITLE	PALAU UNDEFINED UNDEFINED	SAMSUNG ELECTRONICS PART NO. BA41-#####A
CHECK	BAIK, SS	DEV. STEP	DV			
APPROVAL	BIN, KK	REV	0.7			
MODULE CODE		LAST EDIT				
				October 26, 2006 20:08:07 PM	PAGE	19 OF 22

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A-channel



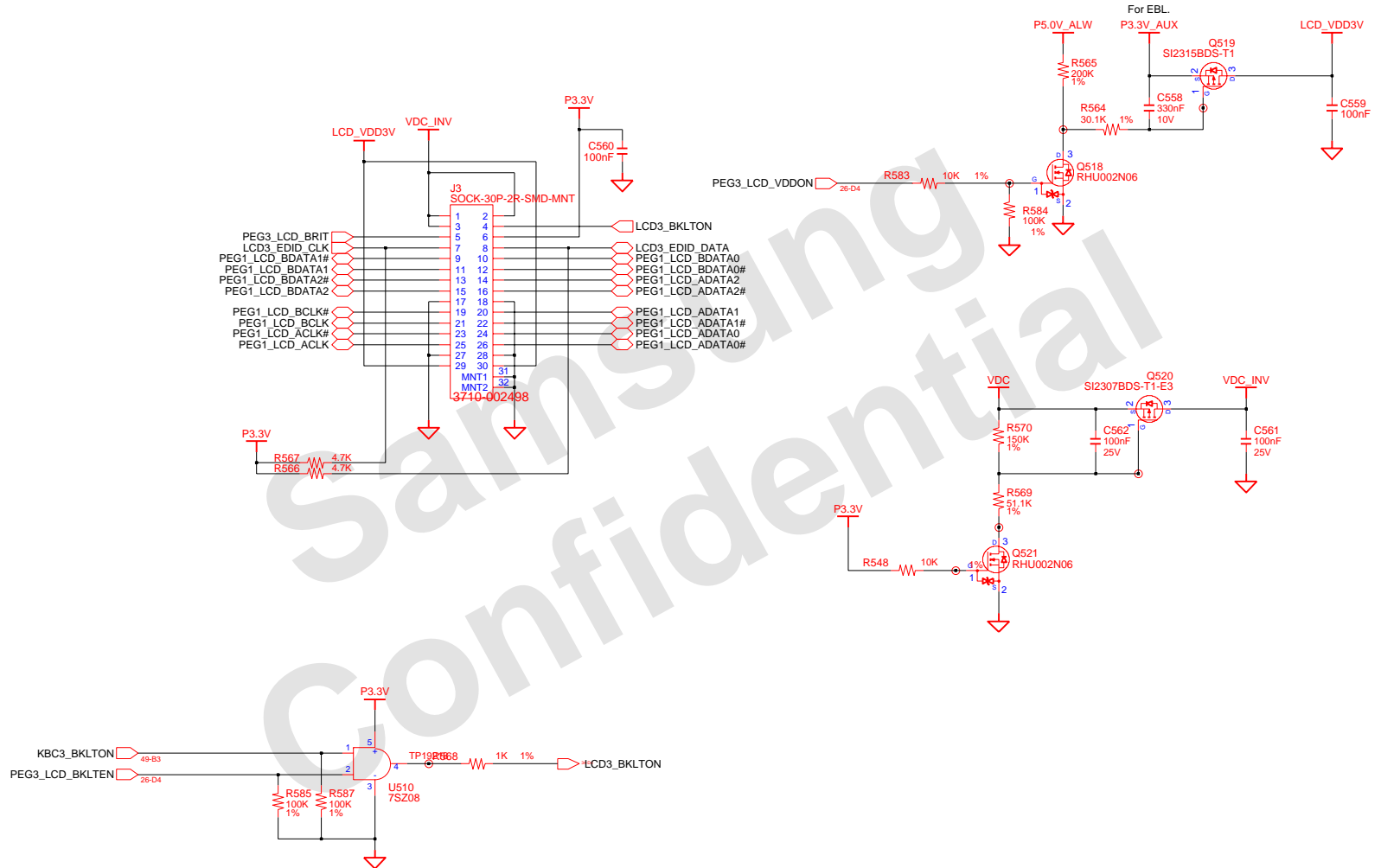
U5
K4J52324QC-BC14

U18
K4J52324QC-BC14

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CHECK	BAIK, SS	DEV. STEP	DV		UNDEFINED	
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MODULE CODE		LAST EDIT				PAGE 20 OF 22

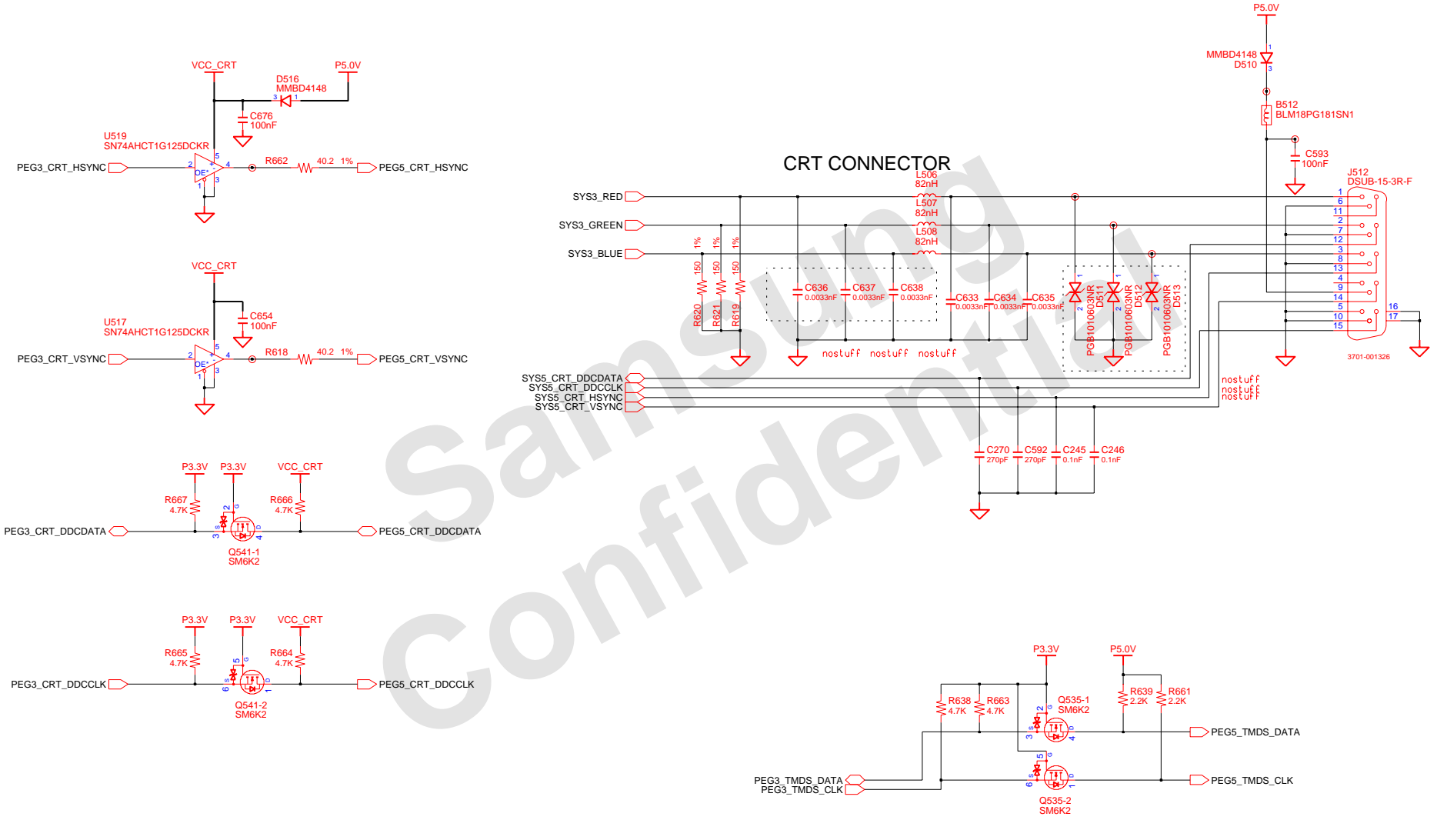
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DRAW	TF Member	DATE	8/12/2006	TITLE	LIB	SAMSUNG ELECTRONICS
CHECK	TF Member	DEV. STEP	DV	LCD_IF_14p1		
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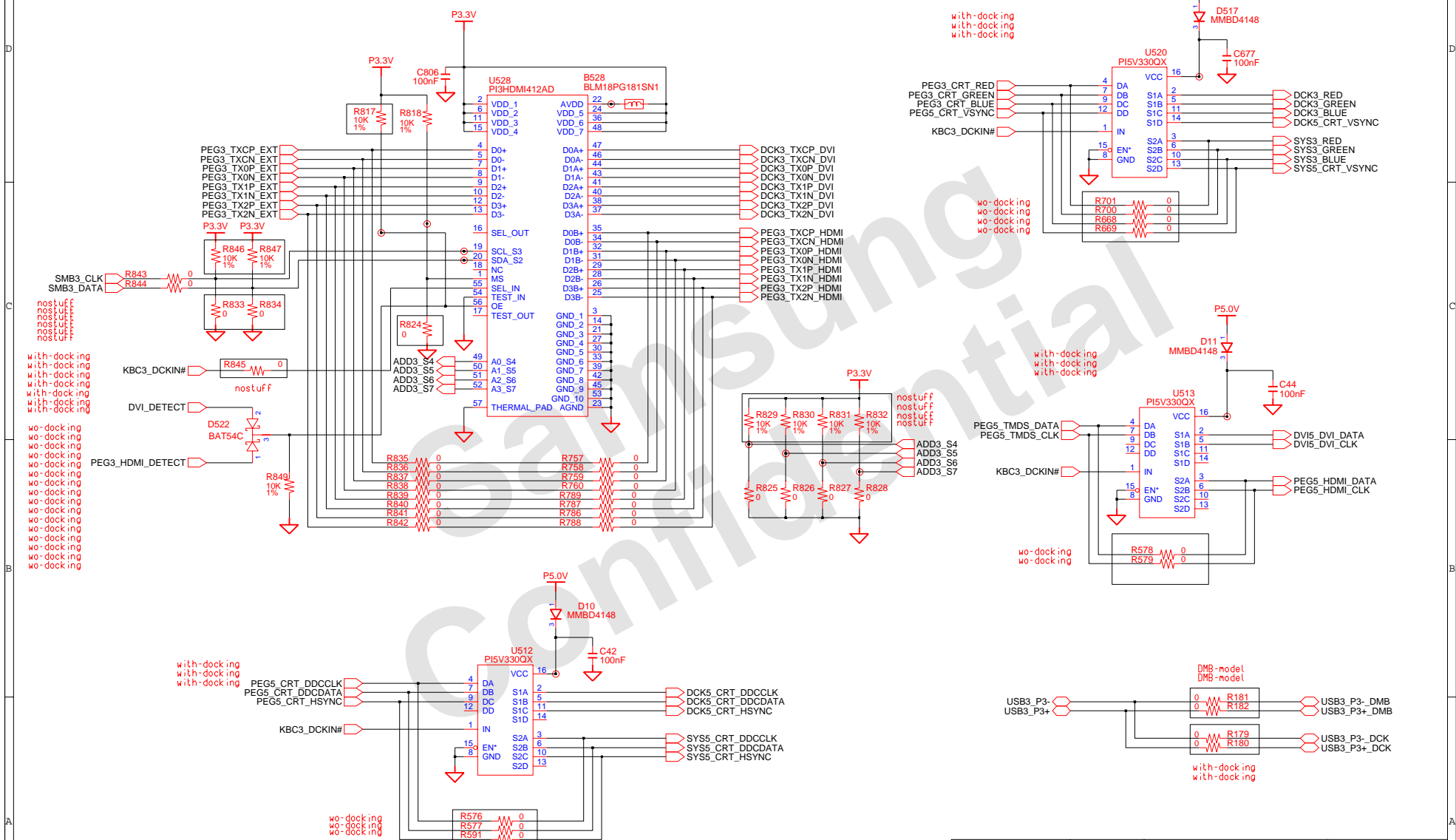
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DRAW	TF Member	DATE	8/12/2006	TITLE	LIB	SAMSUNG ELECTRONICS
CHECK	TF Member	DEV. STEP	DV	Interface_Circuit		
APPROVAL	TF Member	REV	0.8	Graphics_IF_CRT		
MODULE CODE		LAST EDIT	October 10, 2006 20:30:38 PM	PAGE	1 OF 1	

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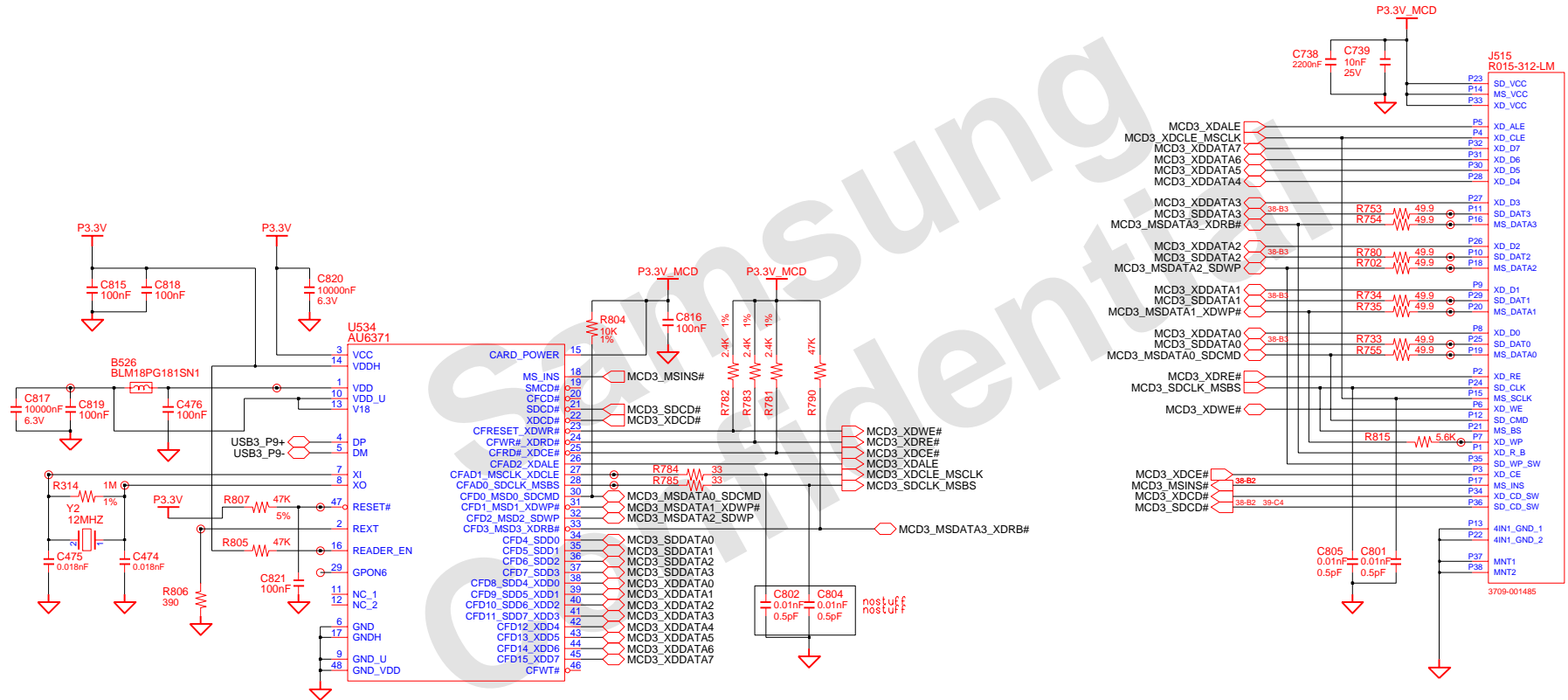
DOCKING OPTION



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MODULE CODE		LAST EDIT	October 26, 2006 20:08:07 PM	PAGE	11 OF 22	

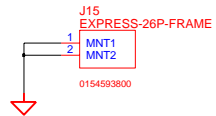
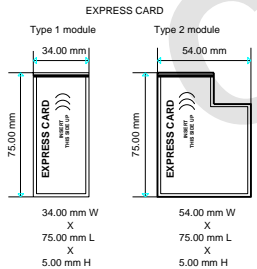
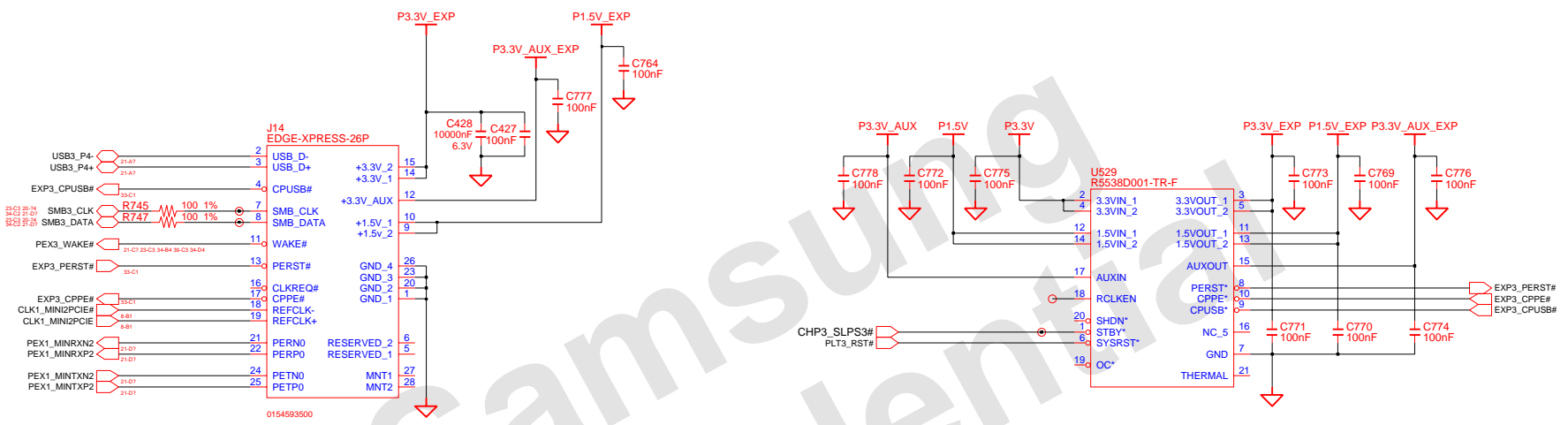
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MEMORY CARD CONTROLLER



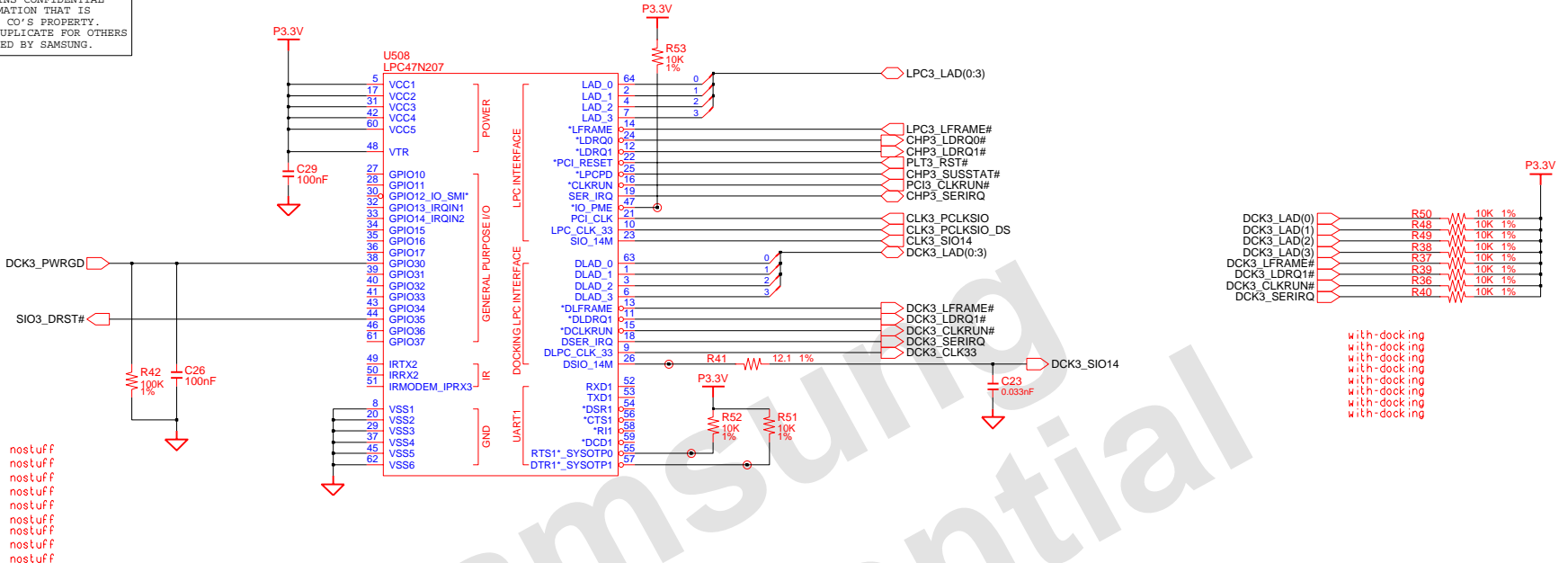
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MODULE CODE		LAST EDIT	October 26, 2006 20:08:07 PM	PAGE	12 OF 22	

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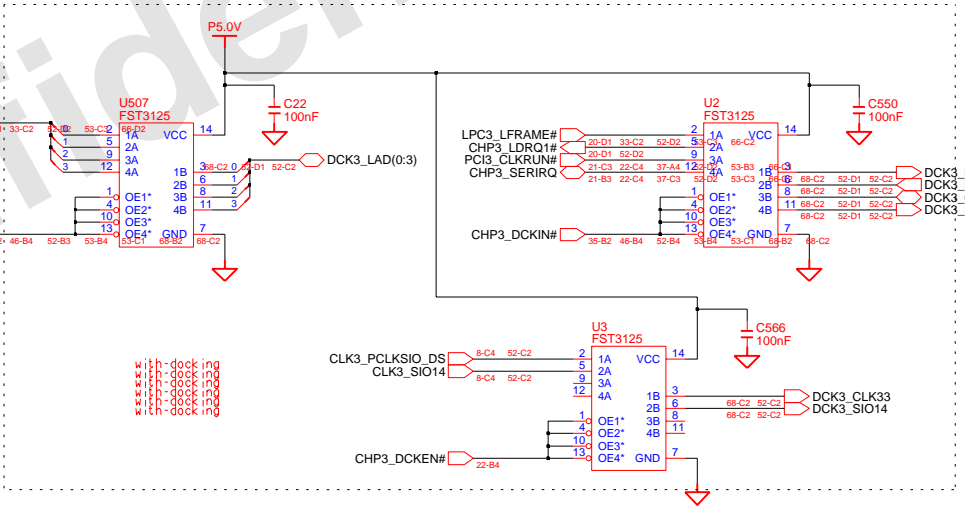
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APPROVAL	BIN, KK	REV	0.7	PART NO. BA41-#####A		
MODULE CODE	LAST EDIT		October 26, 2006 20:08:07 PM		PAGE	13 OF 22

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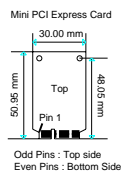
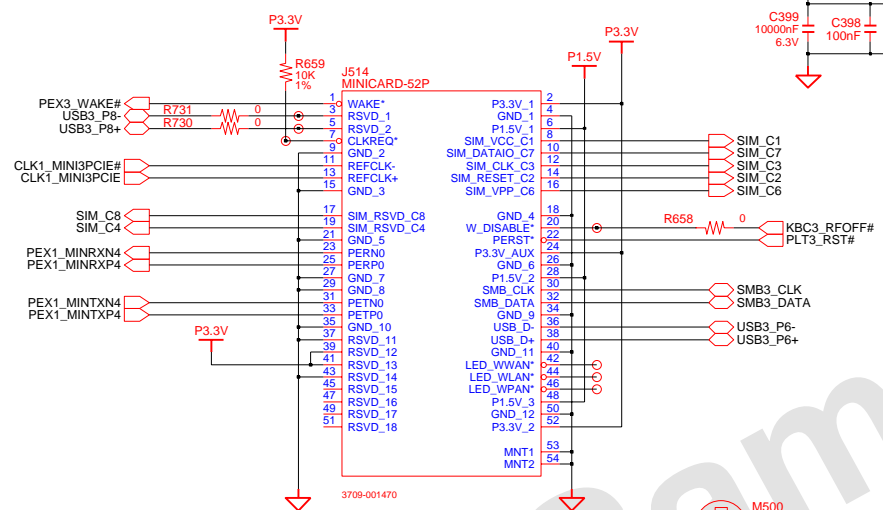


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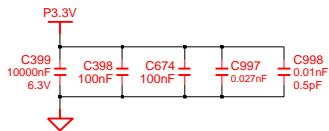
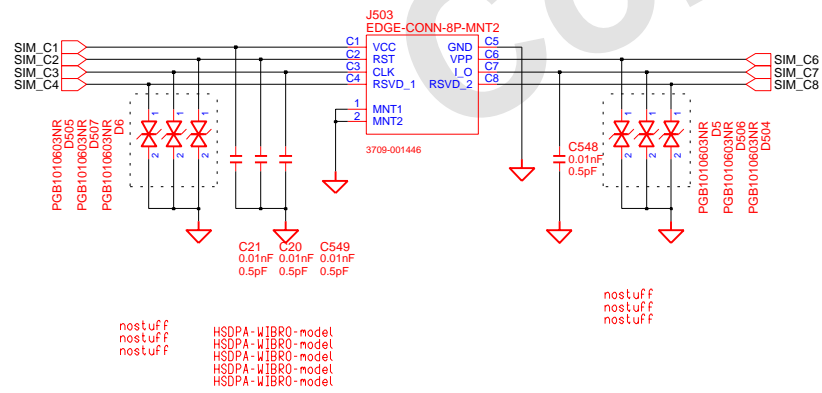
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MODULE CODE		LAST EDIT				
				October 26, 2006 20:08:07 PM	PAGE	14 OF 22

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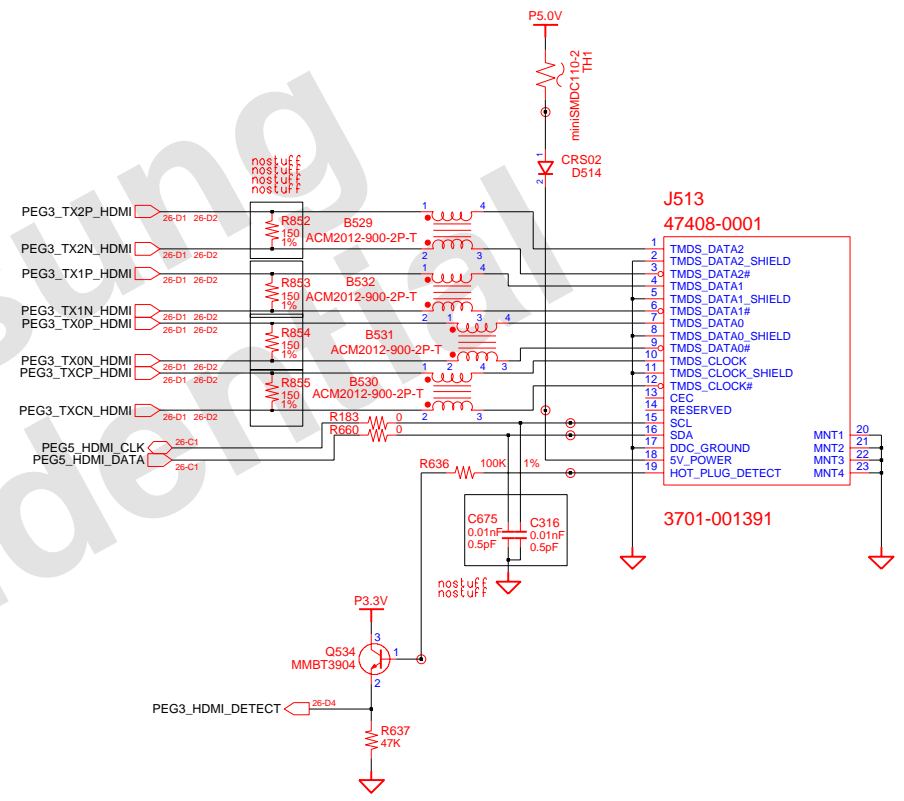
HSDPA / WIBRO, 5.2mm



SIM CARD CONN.

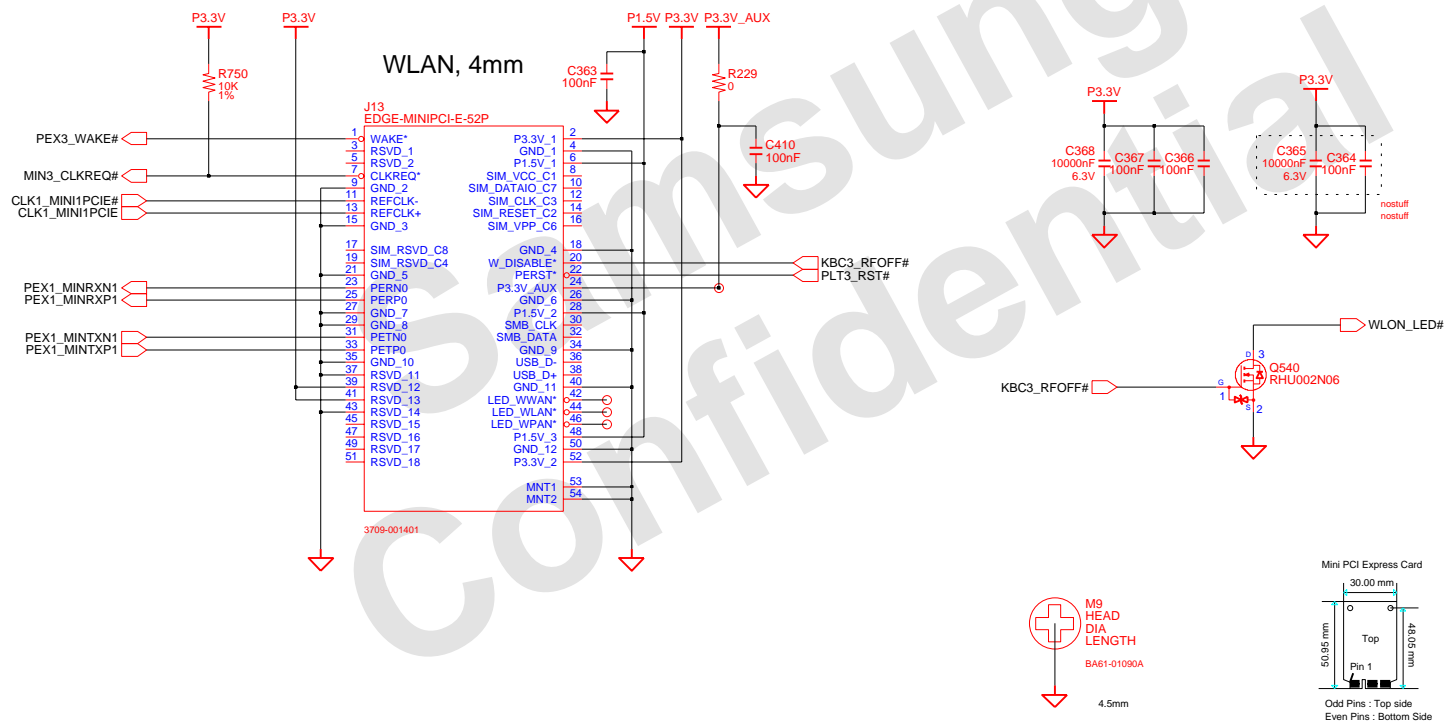


HDMI for External



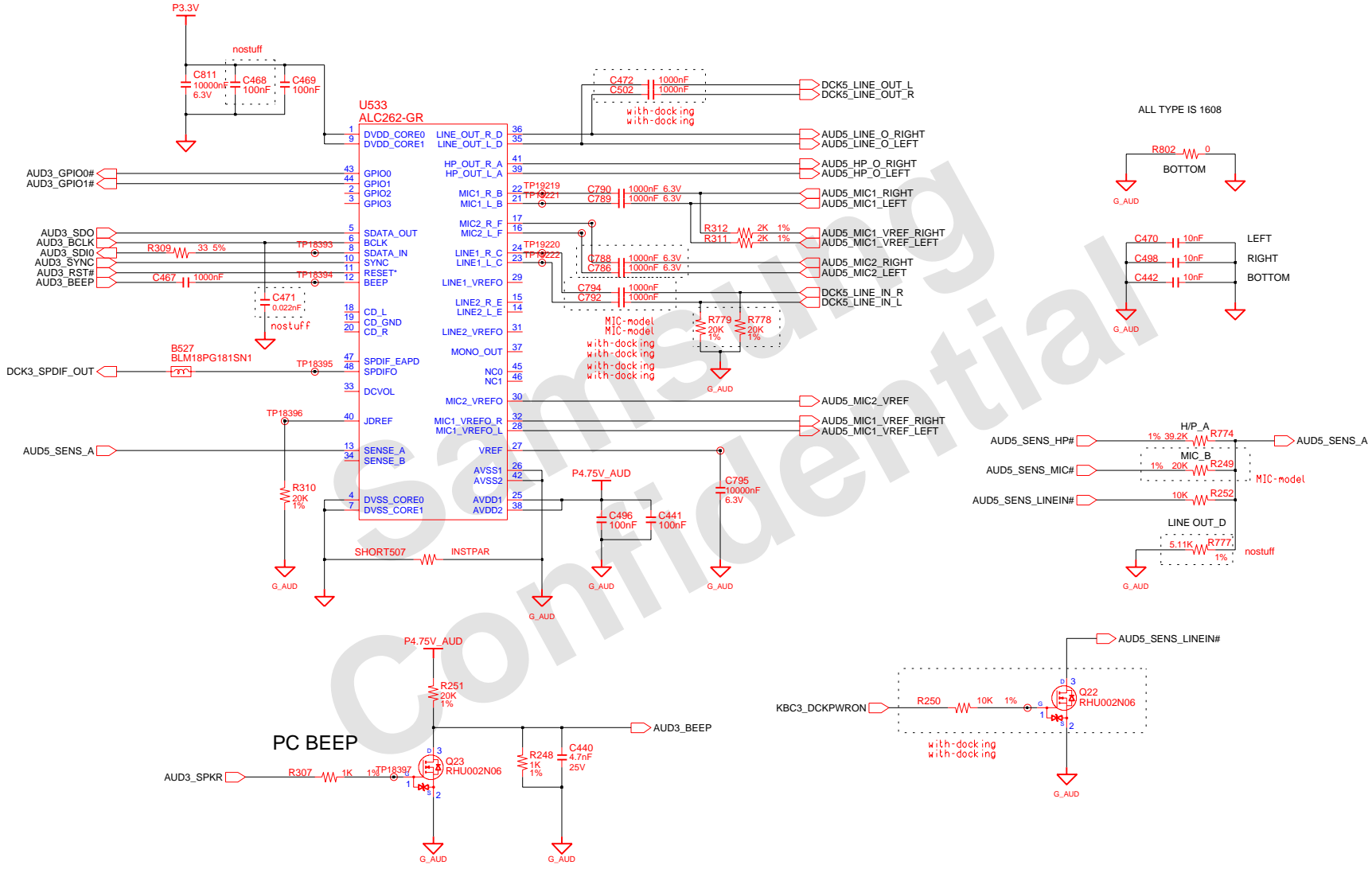
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MODULE CODE		LAST EDIT	October 26, 2006 20:08:07 PM	PAGE	15	OF 22

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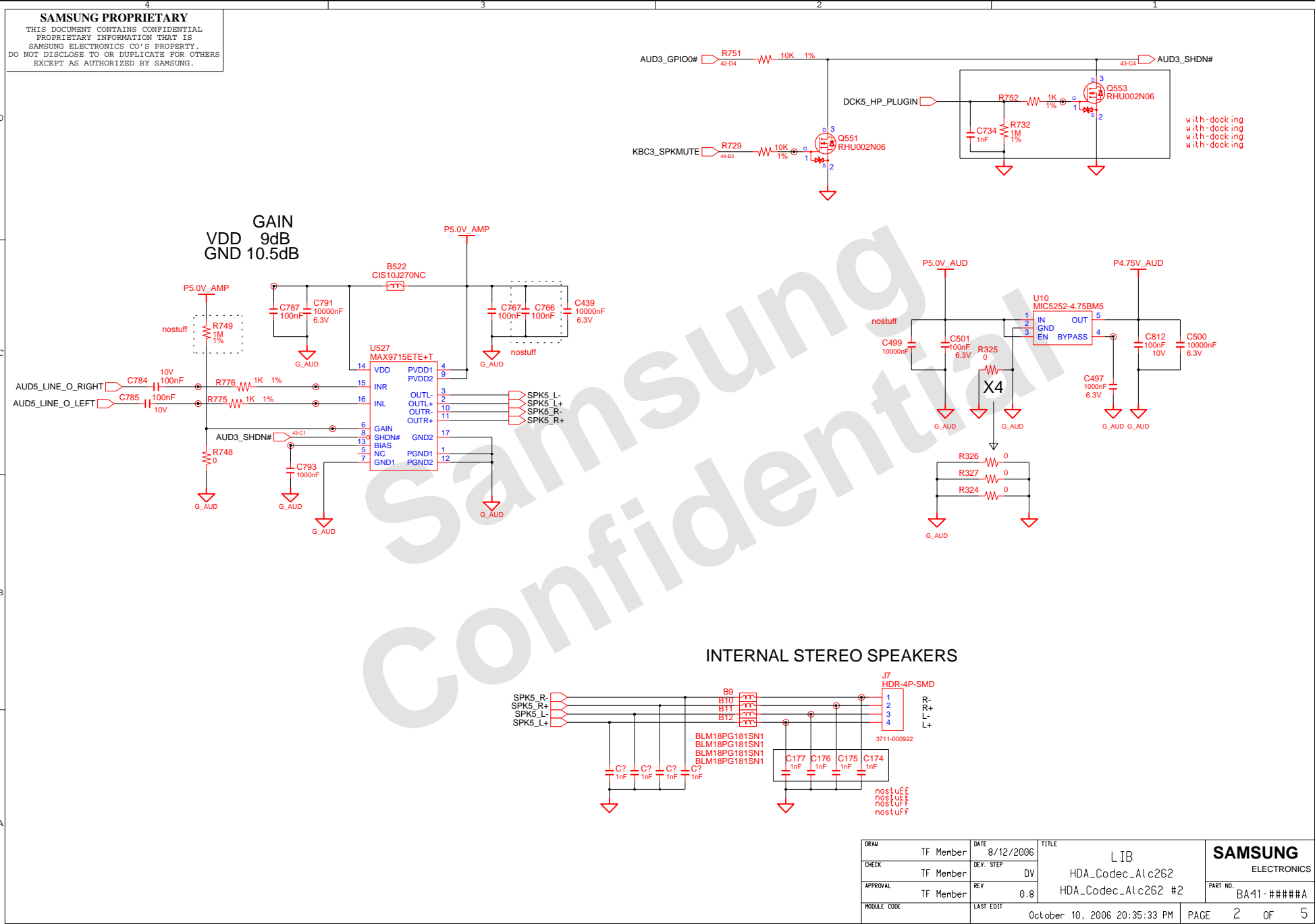
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CHECK	TF Member	DEV. STEP	DV	PCIE_Minicard_Slot		
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MODULE CODE	undef ined	LAST EDIT	October 10, 2006 20:46:07 PM	PAGE	1	OF 1

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DRAW	TF Member	DATE	8/12/2006	TITLE	LIB	SAMSUNG ELECTRONICS
CHECK	TF Member	DEV. STEP	DV	HDA_Codec_A1c262		
APPROVAL	TF Member	REV	0.8	HDA_Codec_A1c262 #1		PART NO. BA41-####A
MODULE CODE	undef ined	LAST EDIT	October 10, 2006 20:35:33 PM	PAGE	1	OF 5

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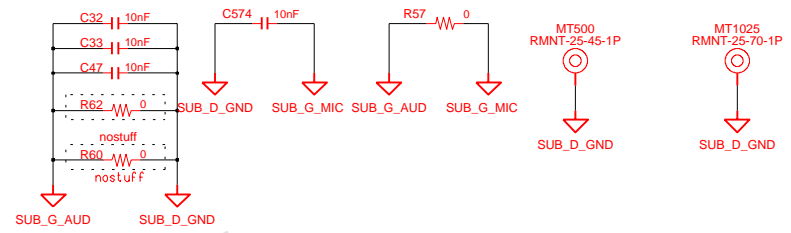
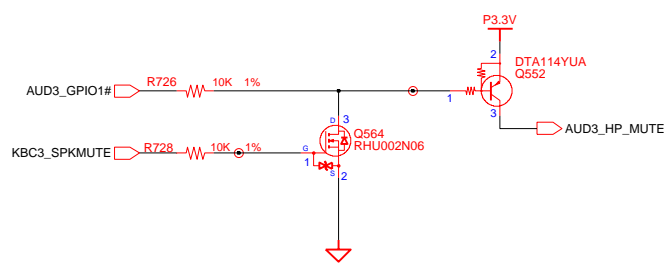


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INTERNAL STEREO SPEAKERS

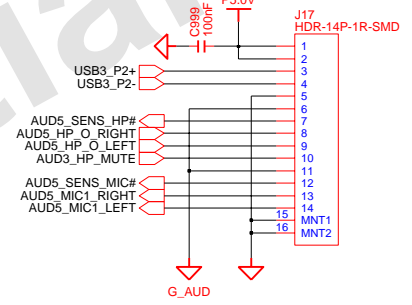
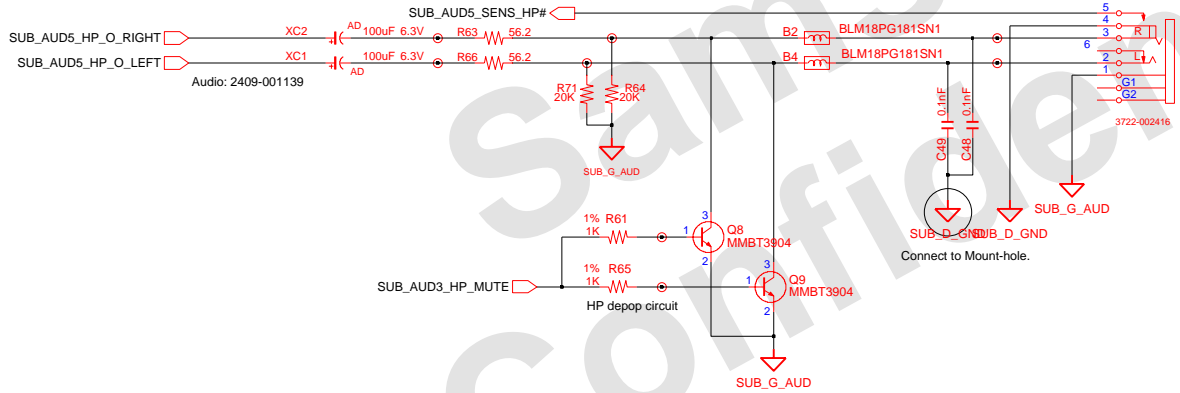
DRAW	TF Member	DATE	8/12/2006	TITLE	LIB		SAMSUNG ELECTRONICS
CHECK	TF Member	DEV. STEP	DV	HDA_Codec_At c262		PART NO. BA41-####A	
APPROVAL	TF Member	REV	0.8	HDA_Codec_At c262 #2			
MODULE CODE		LAST EDIT	October 10, 2006 20:35:33 PM	PAGE	2	OF	5

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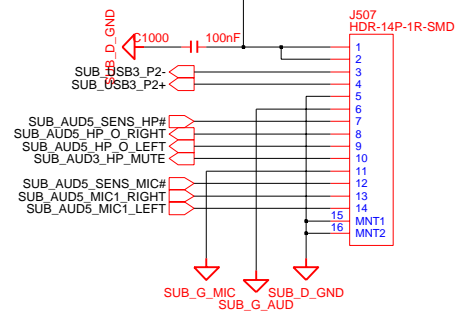
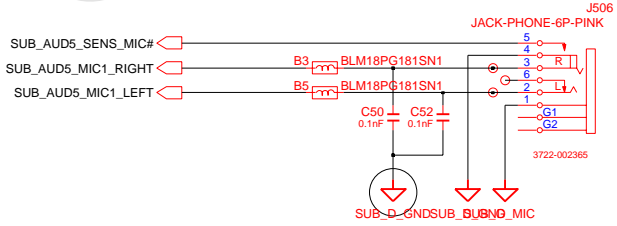
HEADPHONE

MAIN BOARD SIDE



MIC JACK

SUB BOARD SIDE

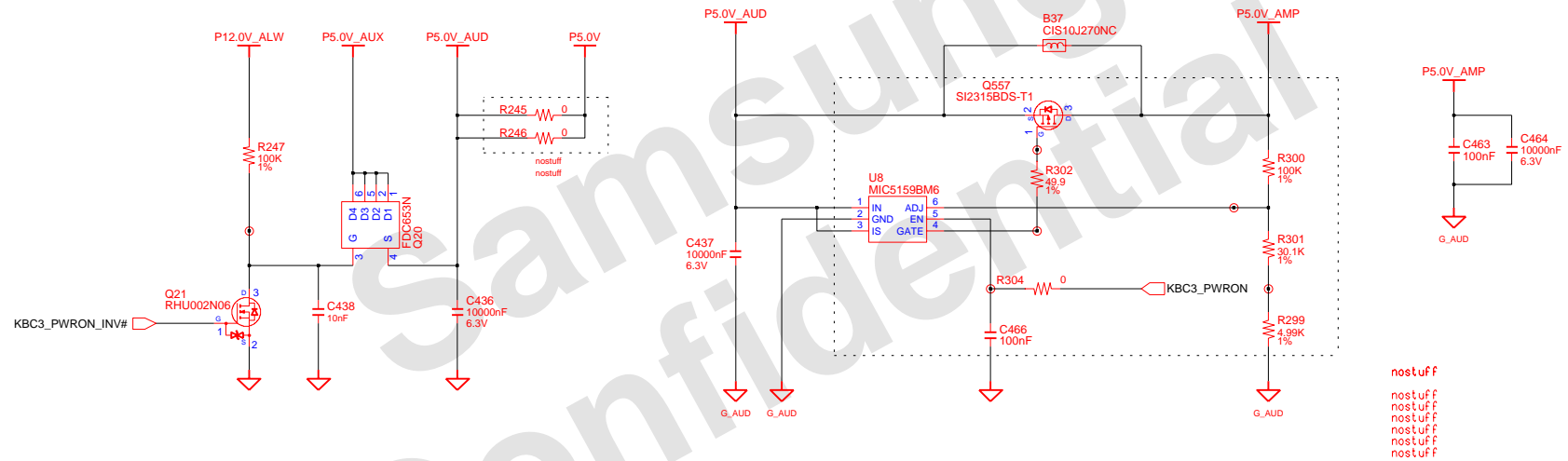


The traces led to Audio Jacks have the width over 10mil

DRAW	TF Member	DATE	8/12/2006	TITLE	LIB	SAMSUNG ELECTRONICS
CHECK	TF Member	DEV. STEP	DV	HDA_Codec_A1c262		
APPROVAL	TF Member	REV	0.8	HDA_Codec_A1c262 #4		PART NO. BA41-#####A
MODULE CODE		LAST EDIT	October 10, 2006 20:35:33 PM	PAGE	4	OF 5

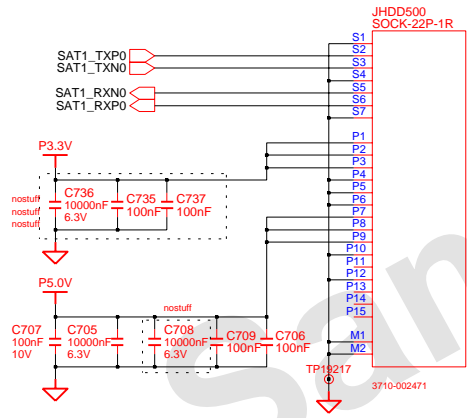
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AUDIO POWER



DRAW	TF Member	DATE	8/12/2006	TITLE	LIB		SAMSUNG ELECTRONICS
CHECK	TF Member	DEV. STEP	DV	HDA_Codec_Al c262		PART NO. BA41 - #####A	
APPROVAL	TF Member	REV	0.8	HDA_Codec_Al c262 #5			
MODULE CODE	undef ined	LAST EDIT	October 10, 2006 20:35:33 PM		PAGE	5 OF 5	

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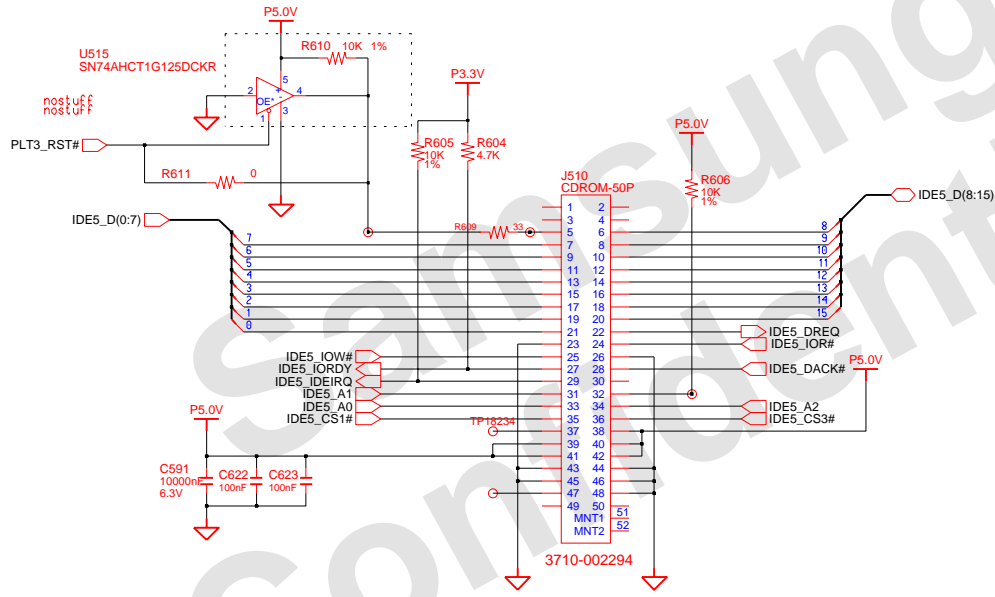


	SATA_DET*	ODD (IDE)	2nd HDD (IDE)
If SATA Detected	0	CSEL(#47) : Open (Master)	CSEL(#28) : GND (Master)
If SATA not Detected	1	CSEL(#47) : GND (Slave)	CSEL(#28) : Open (Slave)

DRAW	TF Member	DATE	8/12/2006	TITLE	LIB HDD_IF_Conn HDD_IF_Conn	SAMSUNG ELECTRONICS PART NO. BA41-#####A
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APPROVAL	TF Member	REV	0.8			
MODULE CODE		LAST EDIT	October 12, 2006 12:18:59 PM		PAGE	1 OF 1

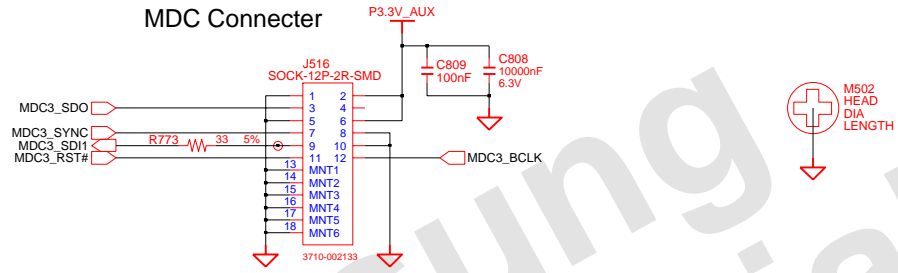
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	SATA_DET*	ODD (IDE)	2nd HDD (IDE)
If SATA Detected	0	CSEL(#47) : Open (Master)	CSEL(#28) : GND (Master)
If SATA not Detected	1	CSEL(#47) : GND (Slave)	CSEL(#28) : Open (Slave)

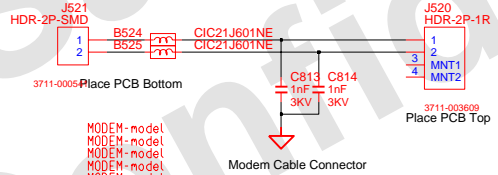


DRAW	TF Member	DATE	8/12/2006	TITLE	LIB	SAMSUNG ELECTRONICS
CHECK	TF Member	DEV. STEP	DV	ODD_IF_Conn	ODD_IF_Conn	
APPROVAL	TF Member	REV	0.8	ODD_IF_Conn	ODD_IF_Conn	PART NO. BA41-####A
MODULE CODE		LAST EDIT	October 12, 2006 12:19:50 PM	PAGE	1	OF 1

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MODEM-model
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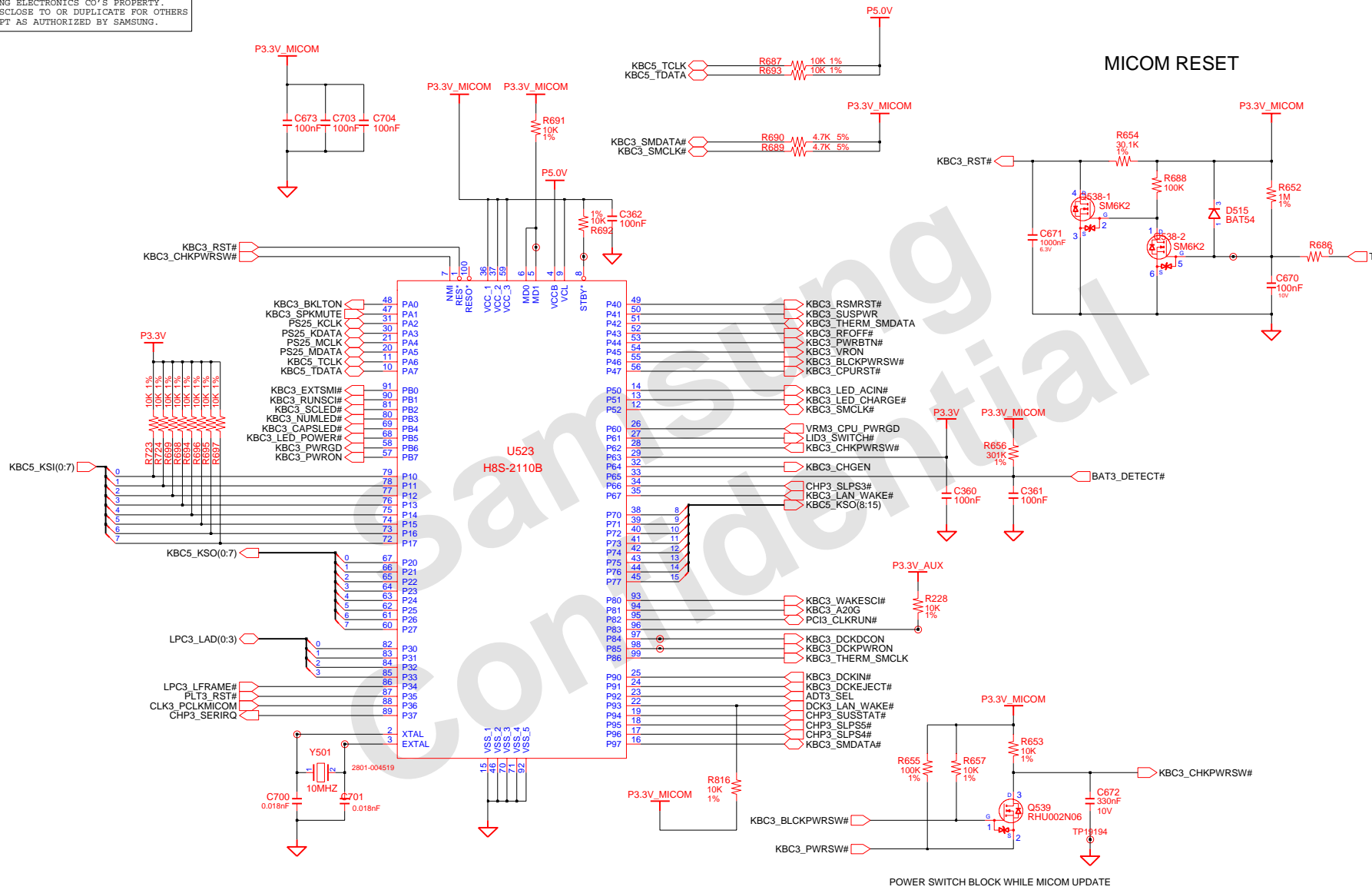


MODEM-model
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Modem Cable Connector

DRAW	TF Member	DATE	8/12/2006	TITLE	LIB HDA_Modem	SAMSUNG ELECTRONICS
CHECK	TF Member	DEV. STEP	DV			
APPROVAL	TF Member	REV	0.8			PART NO. BA41-#####A
MODULE CODE		LAST EDIT	October 10, 2006 20:37:02 PM	PAGE	1	OF 1

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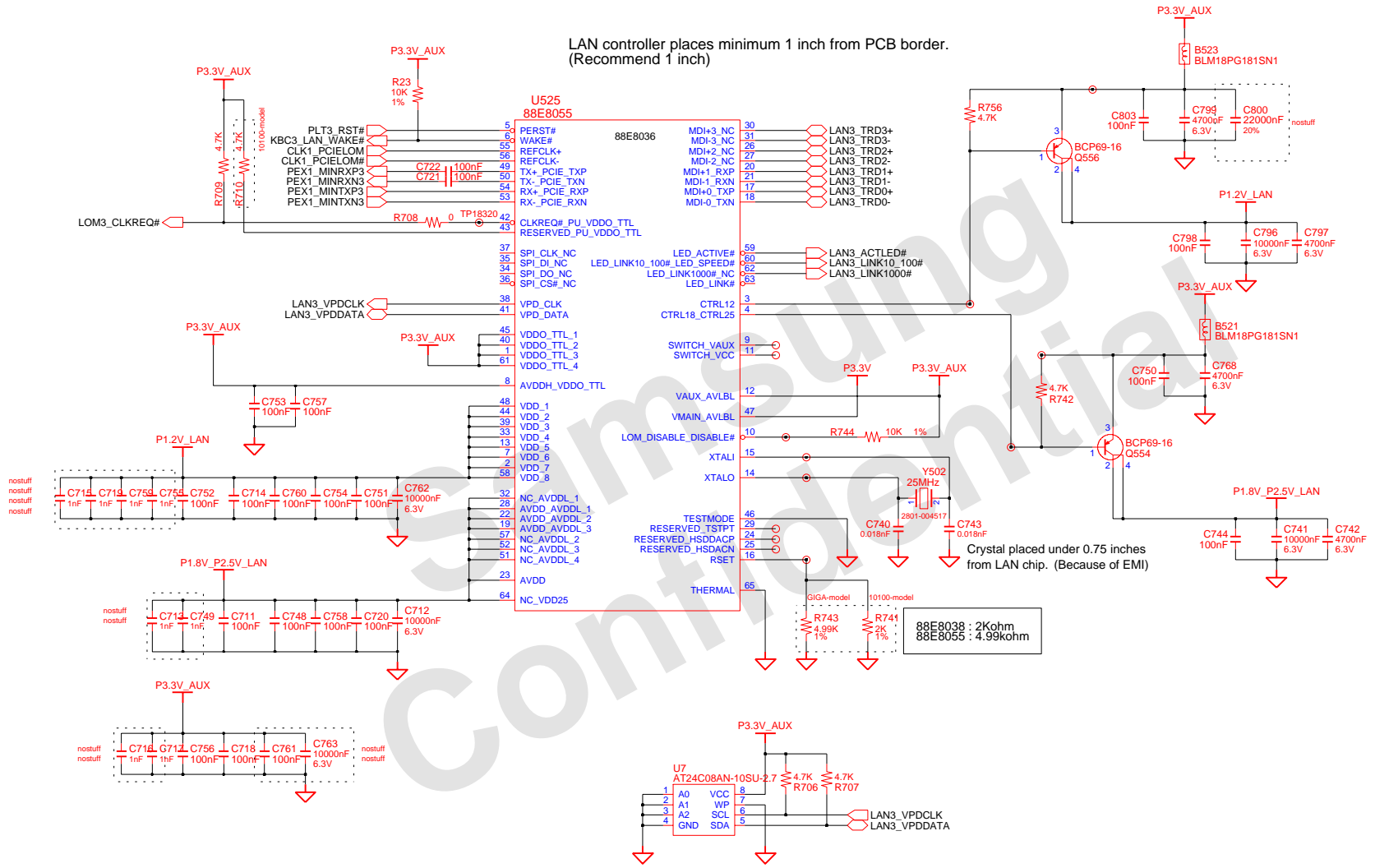
U523 H8S-2110B

KBC3_BKLTON	48	PA0	49	KBC3_RSMRST#
KBC3_SPKMUTE	47	PA1	50	KBC3_SUSPWR
PS25_KCLK	31	PA2	51	KBC3_THERM_SMDATA
PS25_KDATA	30	PA3	52	KBC3_RFOFF#
PS25_MCLK	21	PA4	53	KBC3_PWRBTN#
PS25_MDATA	20	PA5	54	KBC3_VRON
KBC5_TCLK	11	PA6	55	KBC3_BLKPPWRSW#
KBC5_TDATA	10	PA7	56	KBC3_CPURST#
KBC3_EXTSM#	91	PB0	14	KBC3_LED_ACIN#
KBC3_RUNSCH#	81	PB1	13	KBC3_LED_CHARGE#
KBC3_SOLEDR	80	PB2	12	KBC3_SMCLK#
KBC3_NUMLED#	80	PB3	26	VRM3_CPU_PWRGD
KBC3_CAPSLED#	69	PB4	27	LID3_SWITCH#
KBC3_LED_POWER#	68	PB5	28	KBC3_CHKPPWRSW#
KBC3_PWRGD	58	PB6	29	
KBC3_PWRON	57	PB7	32	KBC3_CHGEN
	79	P10	33	
	78	P11	34	CHP3_SLPS3#
	77	P12	35	KBC3_LAN_WAKE#
	76	P13	38	KBC5_KSO(3:15)
	74	P14	39	
	73	P15	40	
	72	P16	41	
	71	P17	42	
	67	P20	43	
	66	P21	44	
	65	P22	45	
	64	P23	93	KBC3_WAKESCI#
	63	P24	94	KBC3_A20G
	62	P25	95	PCI3_CLKRUN#
	61	P26	96	
	60	P27	97	KBC3_DCKDCON
	82	P30	98	KBC3_DCKPWRON
	81	P31	99	KBC3_THERM_SMCLK
	84	P32	25	KBC3_DCKIN#
	85	P33	24	KBC3_DCKEJECT#
	86	P34	23	ADT3_SEL
	87	P35	22	DCK3_LAN_WAKE#
	88	P36	19	CHP3_SUSSTAT#
	89	P37	18	CHP3_SLPS5#
	2	XTAL	17	CHP3_SLPS4#
	3	EXTAL	16	KBC3_SMDATA#
	15	VSS1		
	46	VSS2		
	47	VSS3		
	71	VSS4		
	72	VSS5		

DRAW	TF Member	DATE	8/12/2006	TITLE	LIB	SAMSUNG ELECTRONICS PART NO. BA41-#####A
CHECK	TF Member	DEV. STEP	DV	MICOM_Renasas2110_100p		
APPROVAL	TF Member	REV	0.8	MICOM_Renasas2110_100p		
MODULE CODE		LAST EDIT	October 12, 2006 11:48:20 AM	PAGE	1 OF 1	

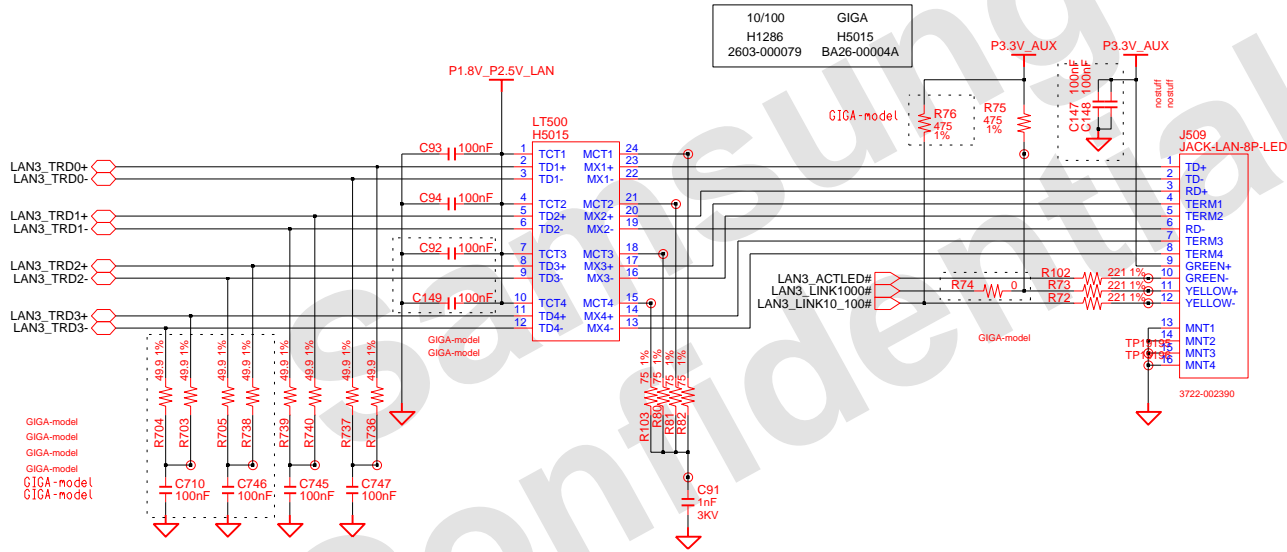
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LAN controller places minimum 1 inch from PCB border.
 (Recommend 1 inch)

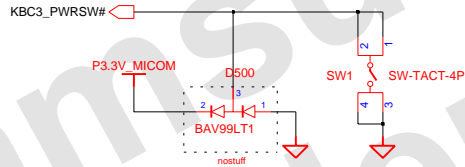


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APPROVAL	TF Member	REV	0.8	LAN_Marvell_8055		
MODULE CODE		LAST EDIT	October 12, 2006 12:07:59 PM	PAGE	1 OF 2	

The distance between LAN controller
 and transformer is designed to extend less than two inches.



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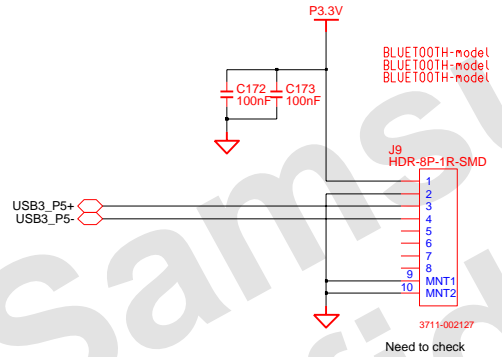


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DRAW	TF Member	DATE	8/12/2006	TITLE	LIB PWR_Switchbutton PWR_Switchbutton	SAMSUNG ELECTRONICS
CHECK	TF Member	DEV. STEP	DV	PART NO.		
APPROVAL	TF Member	REV	0.8			
MODULE CODE	LAST EDIT		October 10, 2006 20:53:26 PM	PAGE	1 OF	1

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Bluetooth Interface

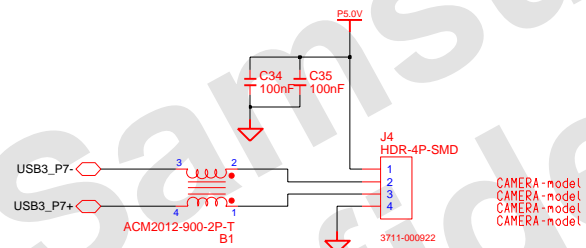


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DRAW	TF Member	DATE	8/12/2006	TITLE	LIB	SAMSUNG ELECTRONICS
CHECK	TF Member	DEV. STEP	DV	Bluetooth_IF_Conn		
APPROVAL	TF Member	REV	0.1	Bluetooth_IF_Conn		PART NO. BA41-####A
MODULE CODE		LAST EDIT	October 12, 2006 12:10:35 PM	PAGE	1 OF	1

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CAMERA

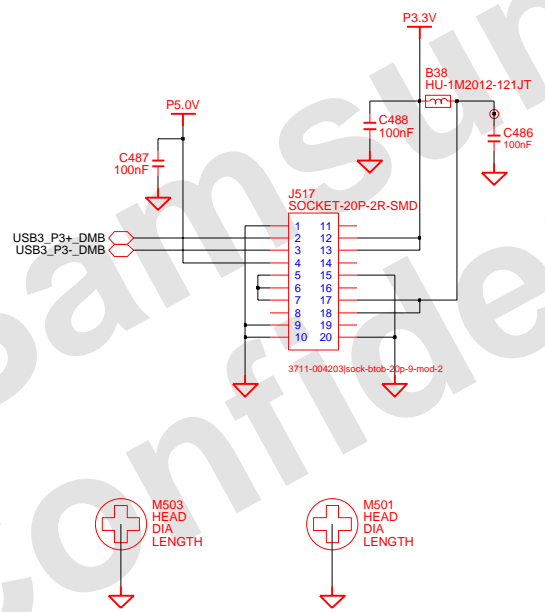


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DRAW	TF Member	DATE	8/12/2006	TITLE	LIB Camera_IF_Conn Camera_IF_Conn	SAMSUNG ELECTRONICS
CHECK	TF Member	DEV. STEP	DV			
APPROVAL	TF Member	REV	0.8			PART NO. BA41-####A
MODULE CODE		LAST EDIT	October 12, 2006 12:13:19 PM	PAGE	1	OF 1

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DMB

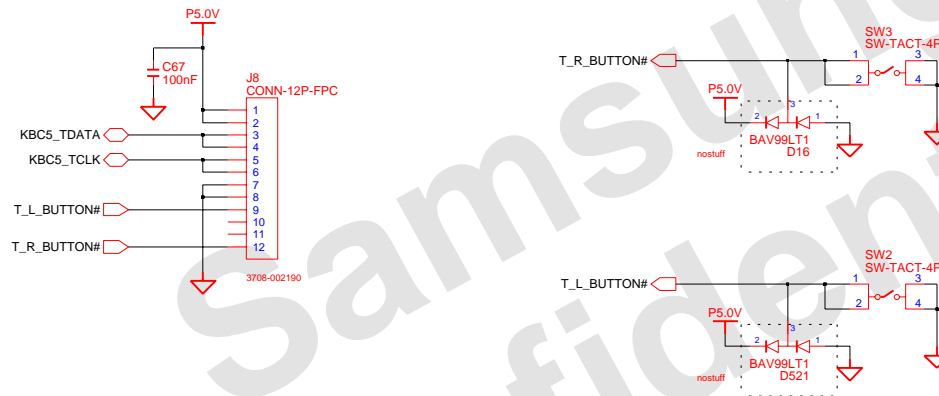


DMB-model
 DMB-model
 DMB-model
 DMB-model
 DMB-model
 DMB-model

DRAW	TF Member	DATE	TITLE	SAMSUNG ELECTRONICS PART NO. BA41-xxxxxx
CHECK	TF Member	DEV. STEP	LIB	
APPROVAL	TF Member	REV	DMB_IF_Conn	
MODULE CODE		LAST EDIT	DMB_IF_Conn	
		October 11, 2006 16:17:06 PM	PAGE	1 OF 1

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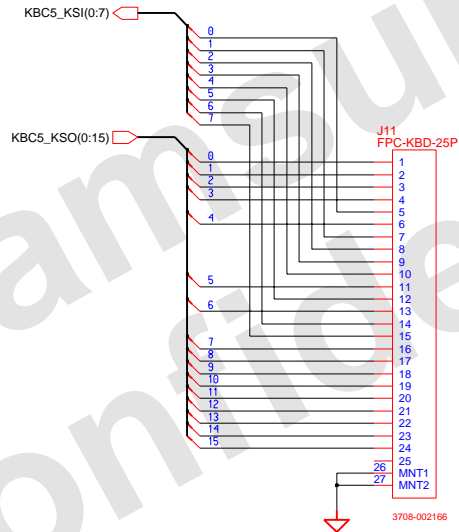
TOUCHPAD



DRAW	TF Member	DATE	8/12/2006	TITLE	LIB	SAMSUNG ELECTRONICS
CHECK	TF Member	DEV. STEP	DV	Touchpad_IF_Conn		
APPROVAL	TF Member	REV	0.8	Touchpad_IF_Conn		PART NO. BA41-####A
MODULE CODE		LAST EDIT	October 12, 2006 12:11:36 PM		PAGE	1 OF 1

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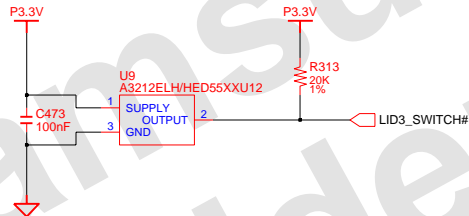
KEYBOARD



DRAW	TF Member	DATE	8/12/2006	TITLE	L IB	SAMSUNG ELECTRONICS
CHECK	TF Member	DEV. STEP	DV	KBD_IF_Conn		
APPROVAL	TF Member	REV	0.8	KBD_IF_Conn		PART NO. BA41-####A
MODULE CODE		LAST EDIT	October 12, 2006 12:09:29 PM	PAGE	1	OF 1

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LID_SWITCH

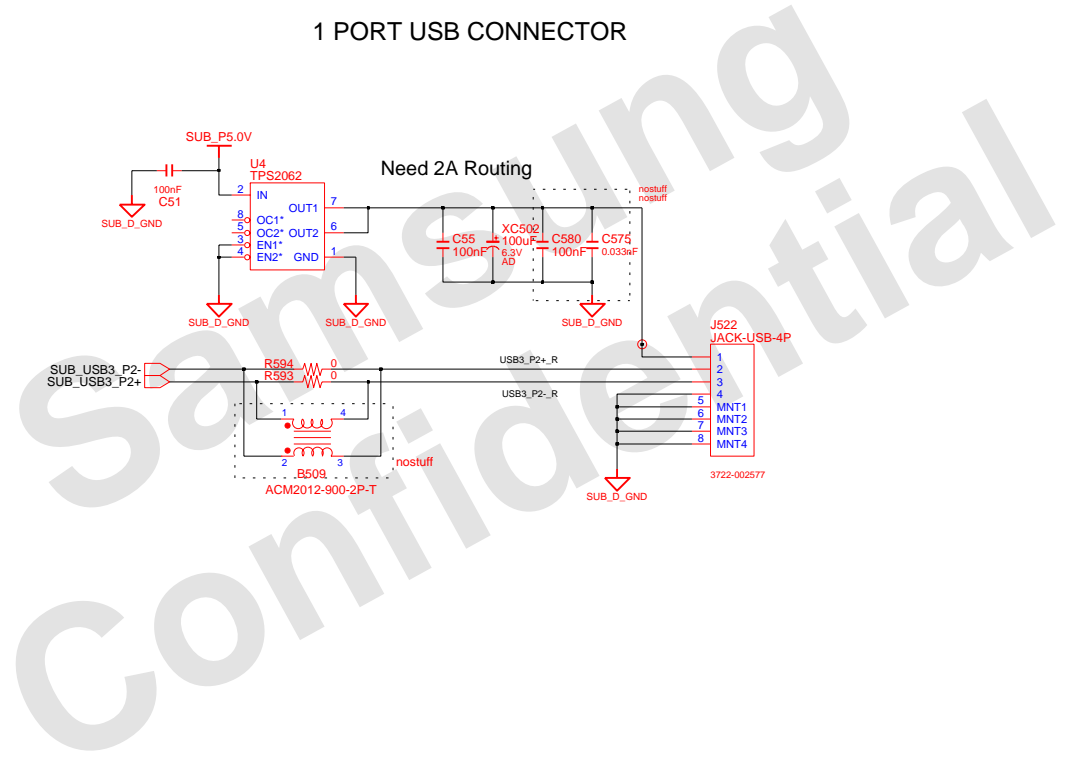


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DRAW	TF Member	DATE	8/12/2006	TITLE	LIB LID_Switch	SAMSUNG ELECTRONICS
CHECK	TF Member	DEV. STEP	DV			
APPROVAL	TF Member	REV	0.8			PART NO. BA41-####A
MODULE CODE		LAST EDIT	October 12, 2006 12:14:03 PM	PAGE	1	OF 1

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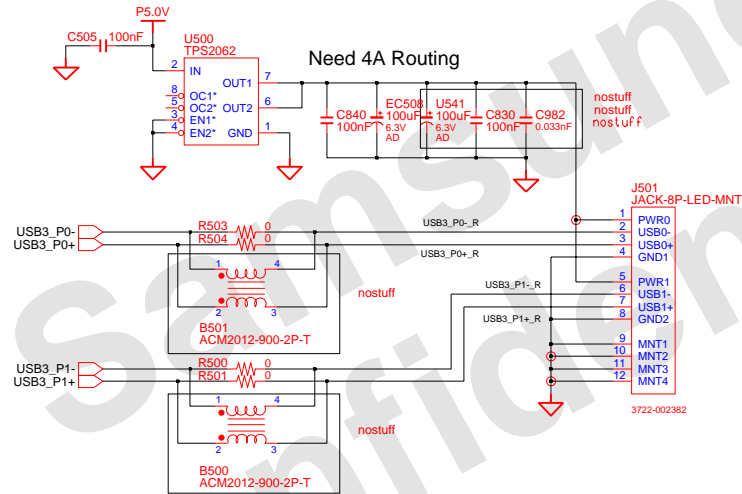
1 PORT USB CONNECTOR



DRAW	TF Member	DATE	8/12/2006	TITLE	LIB	SAMSUNG ELECTRONICS
CHECK	TF Member	DEV. STEP	DV	USB_1Port		
APPROVAL	TF Member	REV	0.8	USB_1Port		PART NO. BA41-#####A
MODULE CODE		LAST EDIT	October 10, 2006 20:57:32 PM	PAGE	1	OF 1

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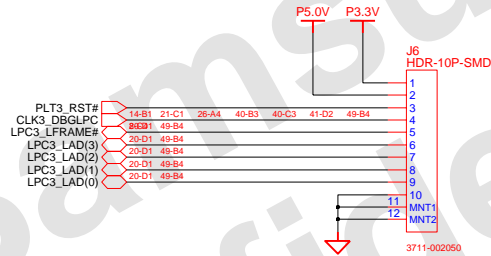
2 PORT USB CONNECTOR



DRAW	TF Member	DATE	8/12/2006	TITLE	LIB	SAMSUNG ELECTRONICS
CHECK	TF Member	DEV. STEP	DV	USB_2Port	USB_2Port	
APPROVAL	TF Member	REV	0.8	USB_2Port		PART NO. BA41-####A
MODULE CODE		LAST EDIT	October 10, 2006 20:58:16 PM	PAGE	1	OF 1

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80H DECODER CONNECTOR

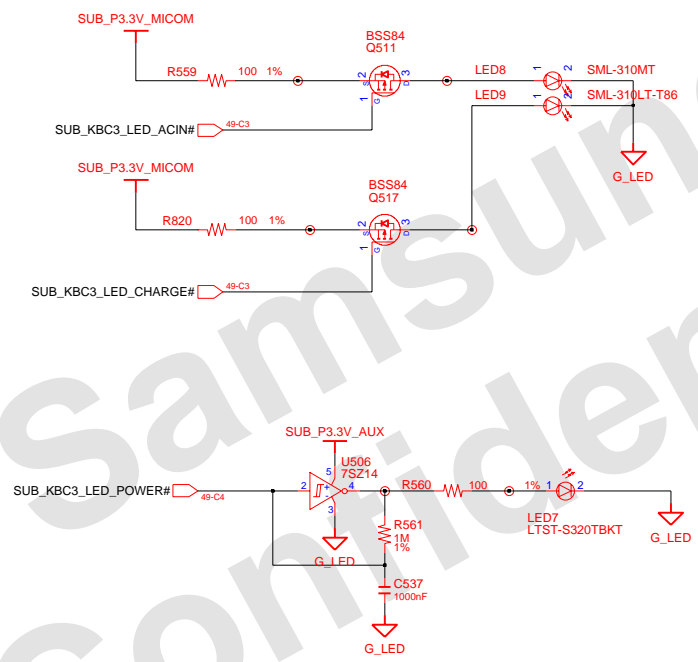


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DRAW	TF Member	DATE	8/12/2006	TITLE	LIB Other_Debug_80	SAMSUNG ELECTRONICS
CHECK	TF Member	DEV. STEP	DV	Other_Debug_80		
APPROVAL	TF Member	REV	0.8	Other_Debug_80	PART NO.	BA41-####A
MODULE CODE		LAST EDIT	October 10, 2006 20:45:09 PM	PAGE	1	OF 1

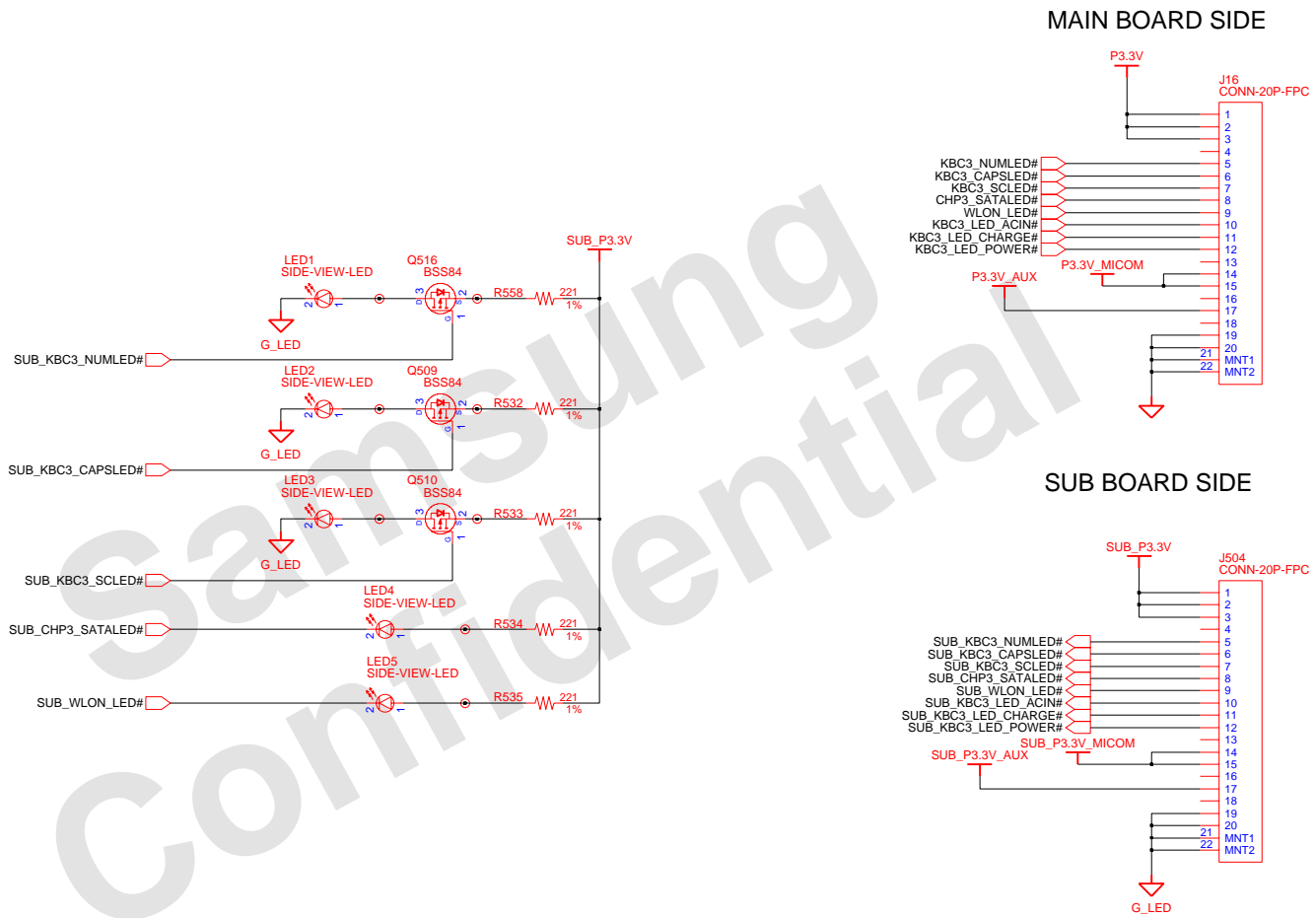
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ADAPTERIN/CHARGING LED



DRAW	TF Member	DATE	8/12/2006	TITLE	LIB	SAMSUNG ELECTRONICS
CHECK	TF Member	DEV. STEP	DV	PWR_Charger		
APPROVAL	TF Member	REV	0.8	PWR_Charger #1		PART NO. BA41-####A
MODULE CODE		LAST EDIT	October 10, 2006 20:48:53 PM	PAGE	1	OF 2

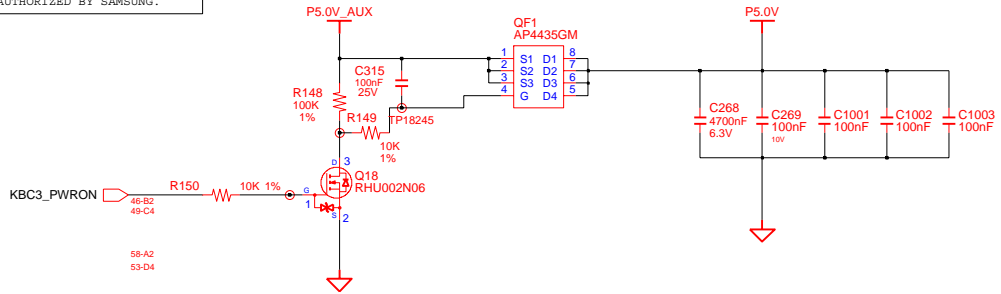
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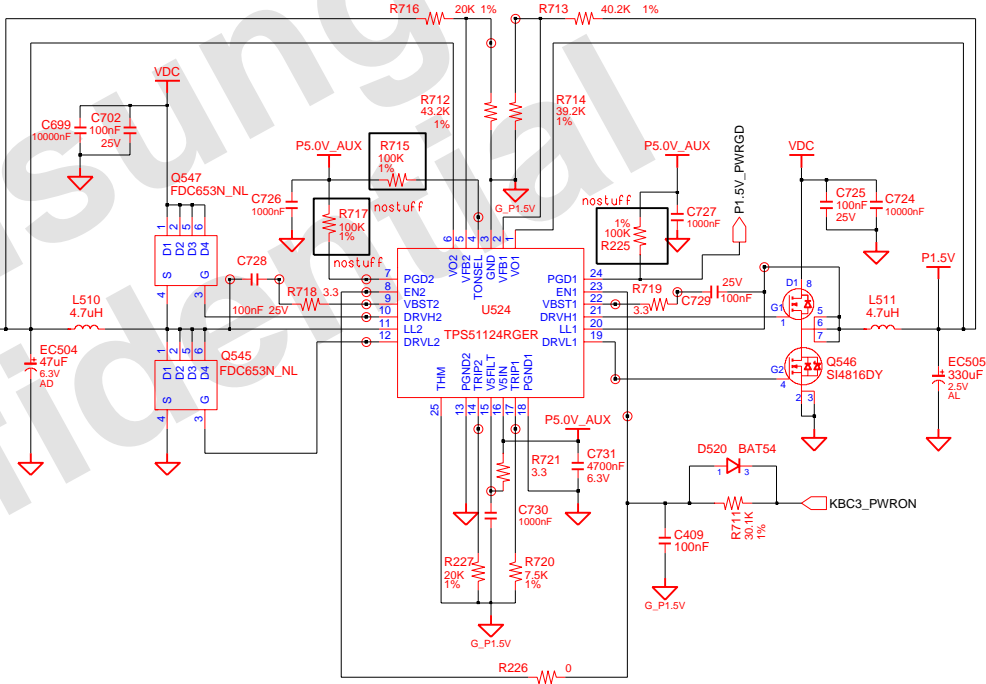
DRAW	TF Member	DATE	8/12/2006	TITLE	LIB	SAMSUNG ELECTRONICS
CHECK	TF Member	DEV. STEP	DV	LED_Switch		
APPROVAL	TF Member	REV	0.8	LED_Switch		PART NO. BA41-#####A
MODULE CODE		LAST EDIT	October 10, 2006 20:43:43 PM	PAGE	1 OF 1	

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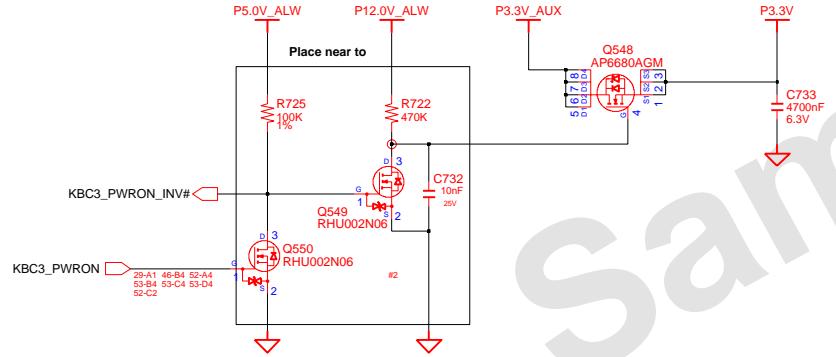
Switched Power On (P5V)



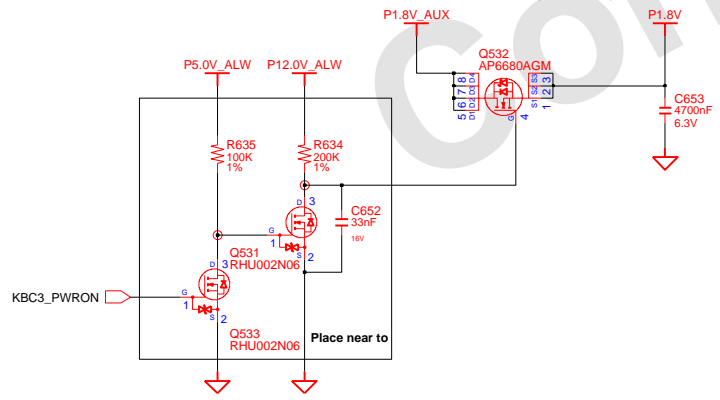
Power (P1.5V & P1.1V)



Switched Power On (P3.3V)



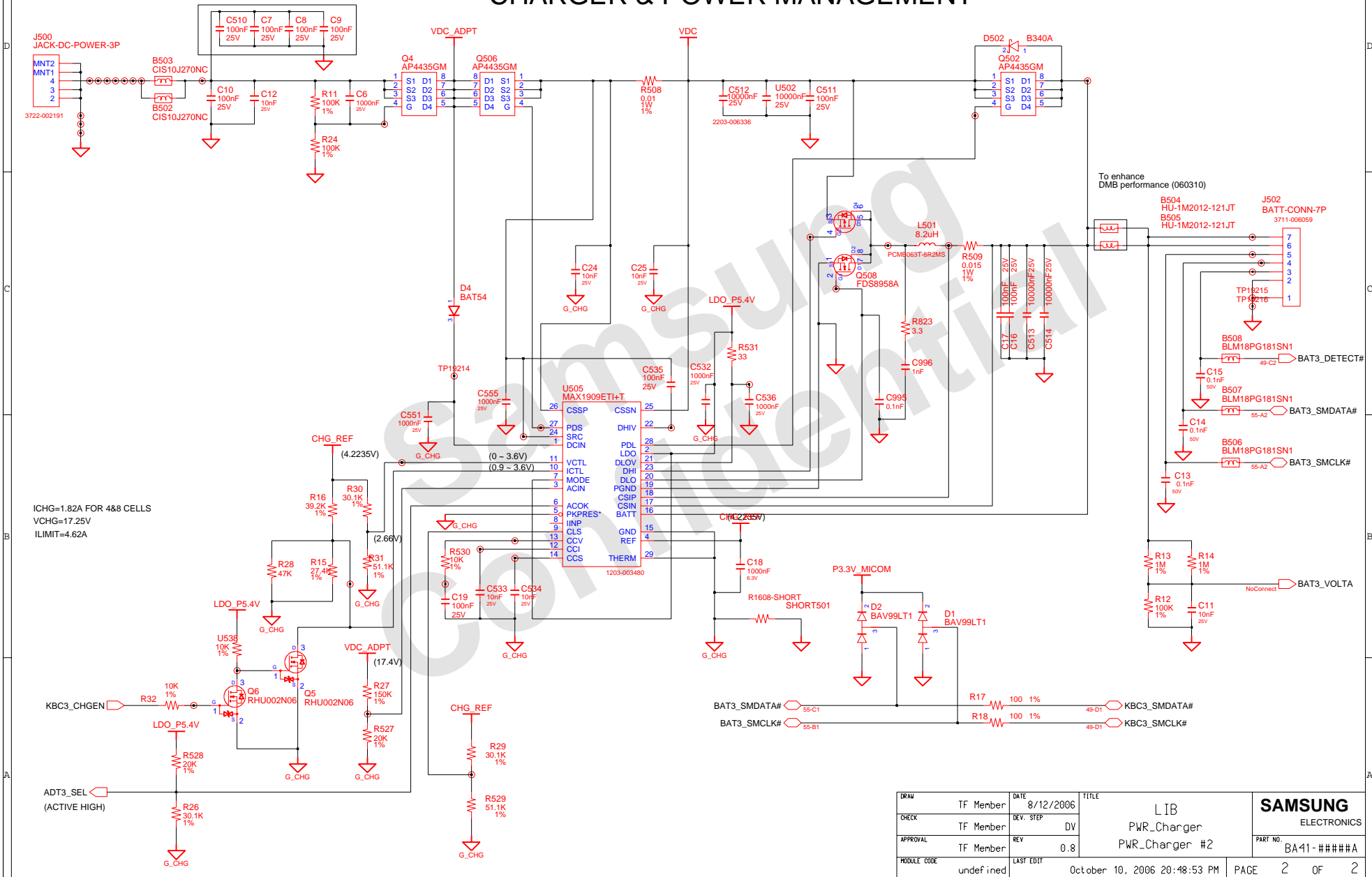
Switched Power On (P1.8V)



DRAW	TF Member	DATE	8/12/2006	TITLE	LIB	SAMSUNG ELECTRONICS
CHECK	TF Member	DEV. STEP	DV	PWR_Switched		
APPROVAL	TF Member	REV	0.8	PWR_Switched		PART NO. BA41-#####A
MODULE CODE	undef ined	LAST EDIT	October 10, 2006 20:54:08 PM	PAGE	1	OF 1

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CHARGER & POWER MANAGEMENT



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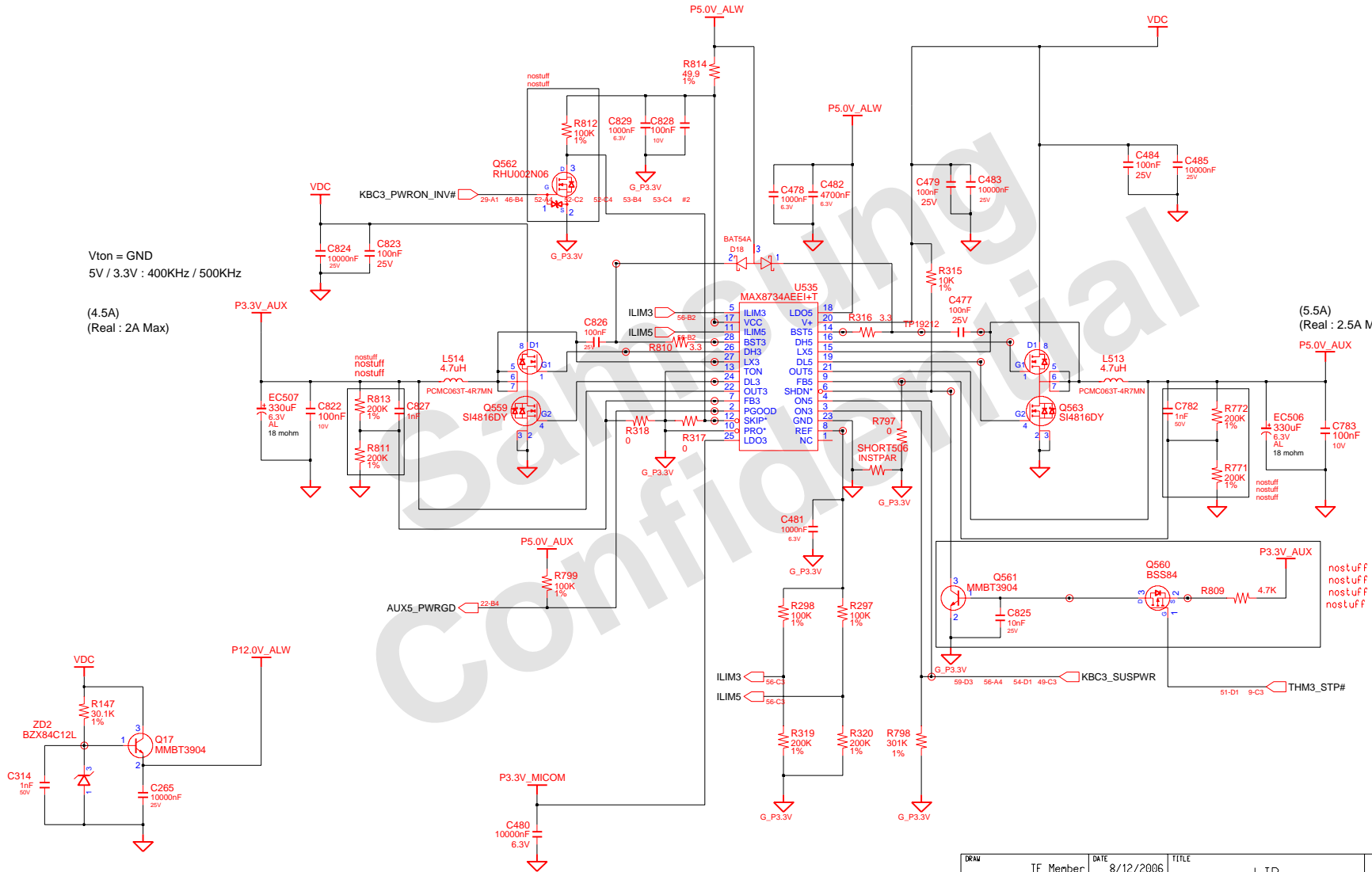
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P3.3V_ALW/AUX & P5V_AUX

Vton = GND
5V / 3.3V : 400KHz / 500KHz

(4.5A)
(Real : 2A Max)

(5.5A)
(Real : 2.5A Max)

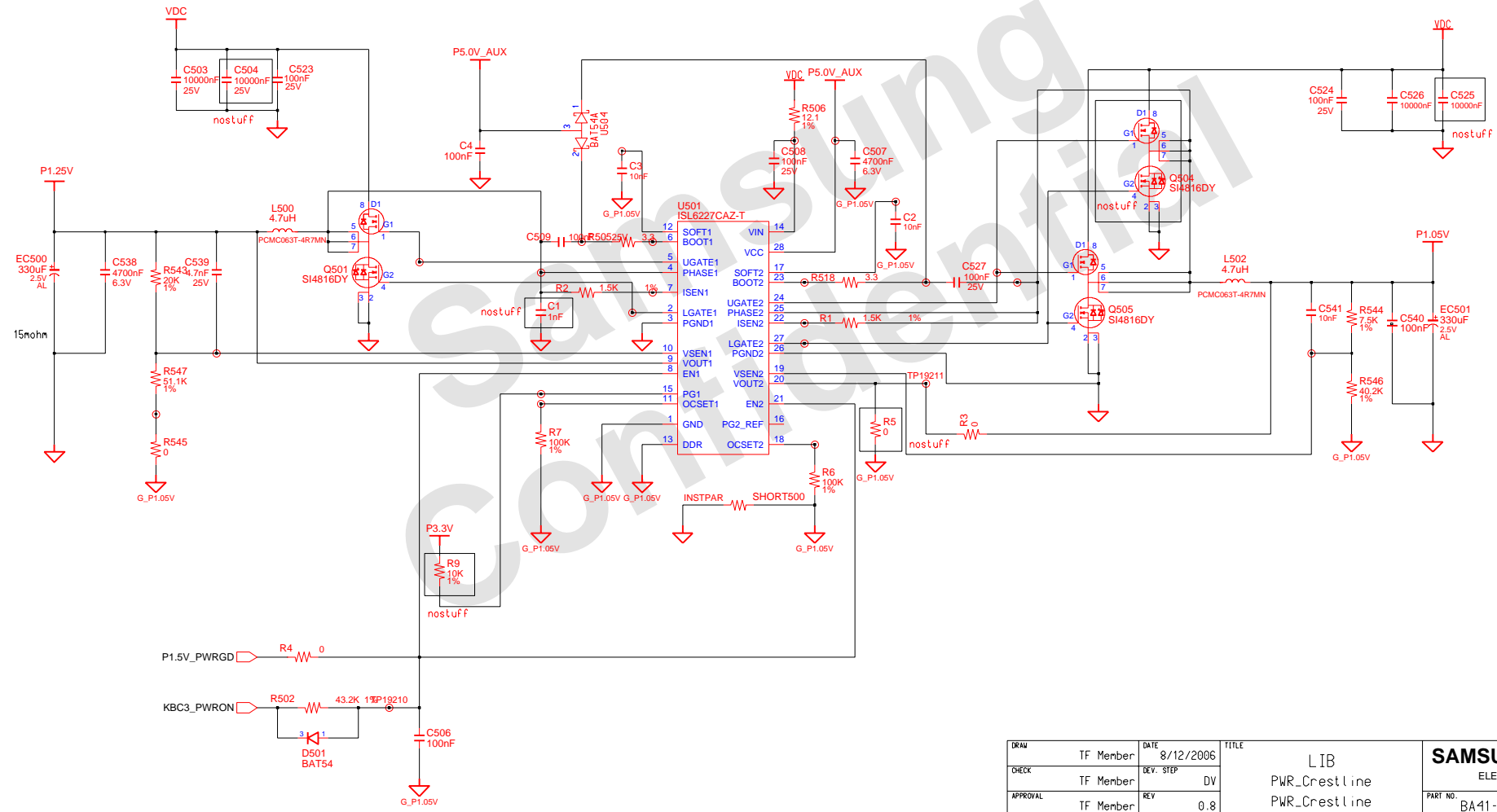


DRAW	TF Member	DATE	8/12/2006	TITLE	LIB	SAMSUNG ELECTRONICS
CHECK	TF Member	DEV. STEP	DV	PWR_3V_5V		
APPROVAL	TF Member	REV	0.8	PWR_3V_5V		PART NO. BA41-####A
MODULE CODE	undef ined	LAST EDIT	October 10, 2006 20:47:11 PM	PAGE	1	OF 1

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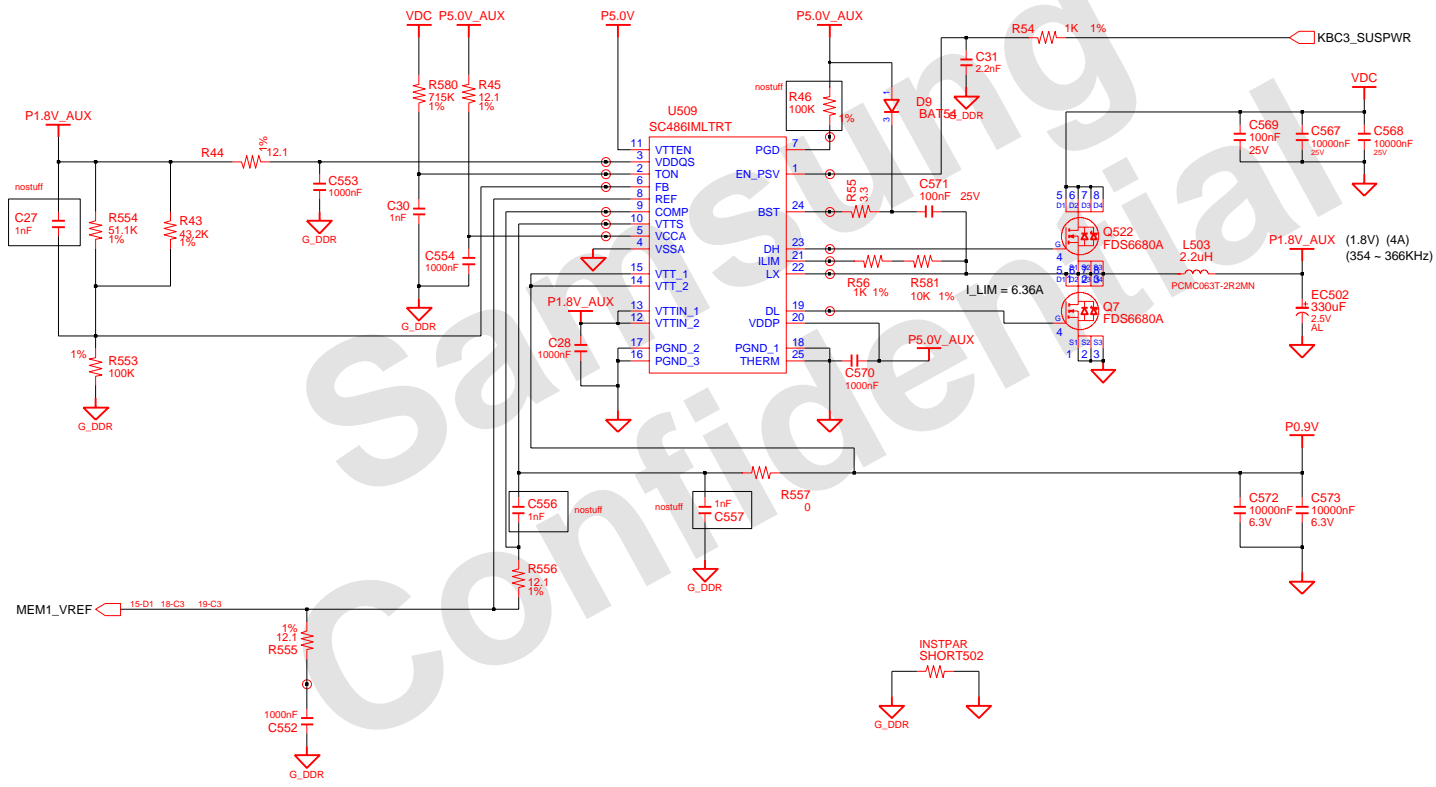
LOCATION	PM-model	
	SEC P/N	VENDOR P/N
R2563	2007-007528	1.5Kohm, 1%, 1005
Q967	0505-001386	FDS6680A
Q968	0505-001386	FDS6680A
L815	2703-002530	IHLP2525CZ-01 2.2uH
EC845	2402-001168	2R5TPE330MF

VCCP & P1.25V



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DDR2 Power



DRAW	TF Member	DATE	8/12/2006	TITLE	LIB	SAMSUNG ELECTRONICS
CHECK	TF Member	DEV. STEP	DV	PWR_Memory		
APPROVAL	TF Member	REV	0.8	PWR_Memory		PART NO. BA41-####A
MODULE CODE	undef ined	LAST EDIT	October 10, 2006 20:52:43 PM	PAGE	1 OF	1

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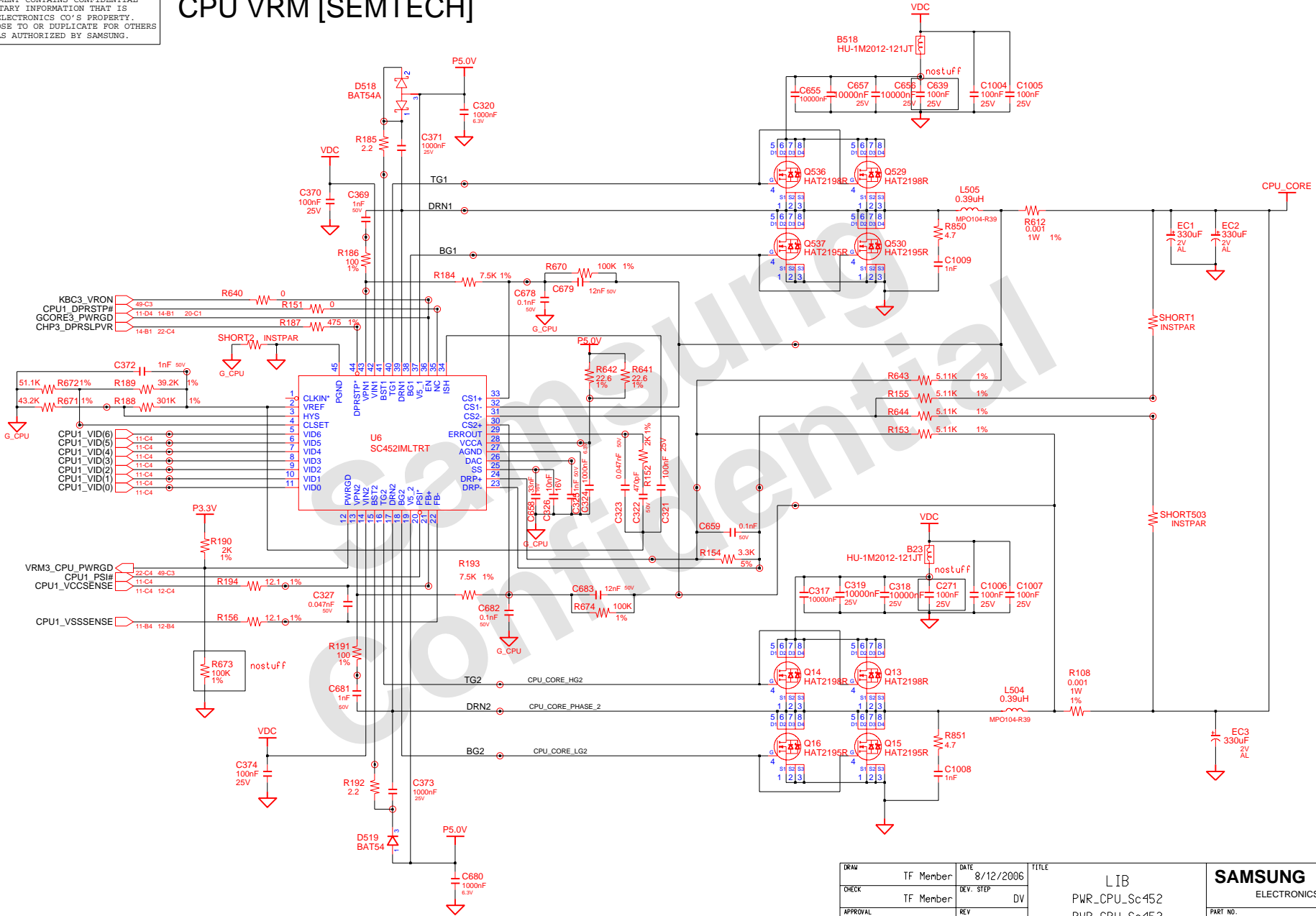
CPU VRM [SEMTECH]

D

C

B

A



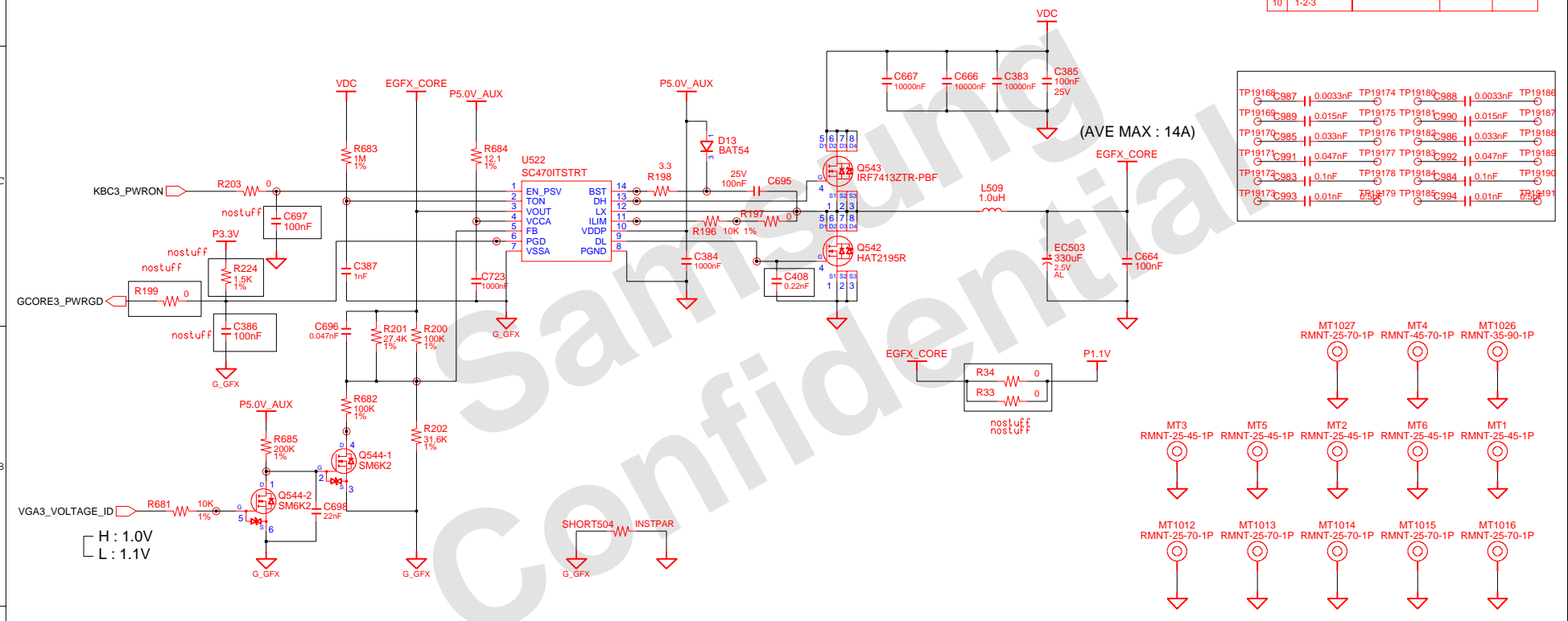
DRAW	TF Member	DATE	8/12/2006	TITLE	LIB	SAMSUNG ELECTRONICS
CHECK	TF Member	DEV. STEP	DV	PWR_CPU_Sc452		
APPROVAL	TF Member	REV	0.8	PWR_CPU_Sc452		PART NO. BA41-#####A
MODULE CODE	undef ined	LAST EDIT	October 10, 2006 20:48:08 PM	PAGE	1	OF 1

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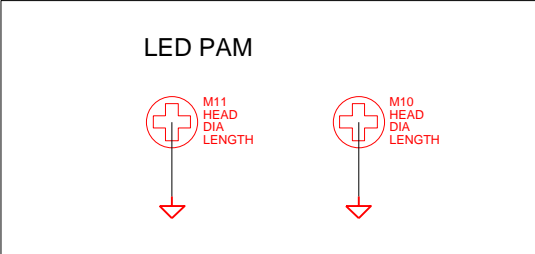
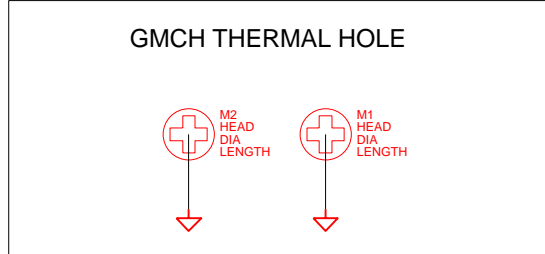
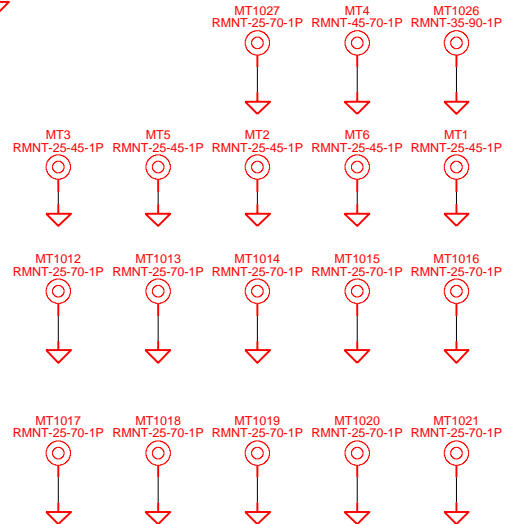
GFX CORE [SEMTECH]

PCB REVISION CONTROL (ICT)				
NO	CONNECTION	DATE(Y/M/DD)	REVISION	STEP
1	N.C.			
2	1-2			
3	2-3			
4	3-1			
5	1-2-3			
6	N.C.			
7	1-2			
8	2-3			
9	3-1			
10	1-2-3			

REV1
 1 O
 2 O 3



TP1916	C987	0.0033nF	TP19174	TP1918	C988	0.0033nF	TP19186
TP1916	C989	0.015nF	TP19175	TP19181	C990	0.015nF	TP19187
TP1917	C985	0.033nF	TP19176	TP19182	C986	0.033nF	TP19188
TP1917	C991	0.047nF	TP19177	TP19183	C992	0.047nF	TP19189
TP1917	C983	0.1nF	TP19178	TP19184	C984	0.1nF	TP19190
TP1917	C993	0.01nF	TP19179	TP19185	C994	0.01nF	TP19191



DRAW	IM, KI	DATE	10/26/2006	TITLE	PALAU UNDEFINED	SAMSUNG ELECTRONICS PART NO. BA41-#####A
CHECK	BAIK, SS	DEV. STEP	DV			
APPROVAL	BIN, KK	REV	0.7			
MODULE CODE		LAST EDIT	October 26, 2006 20:08:07 PM	PAGE	22 OF 22	

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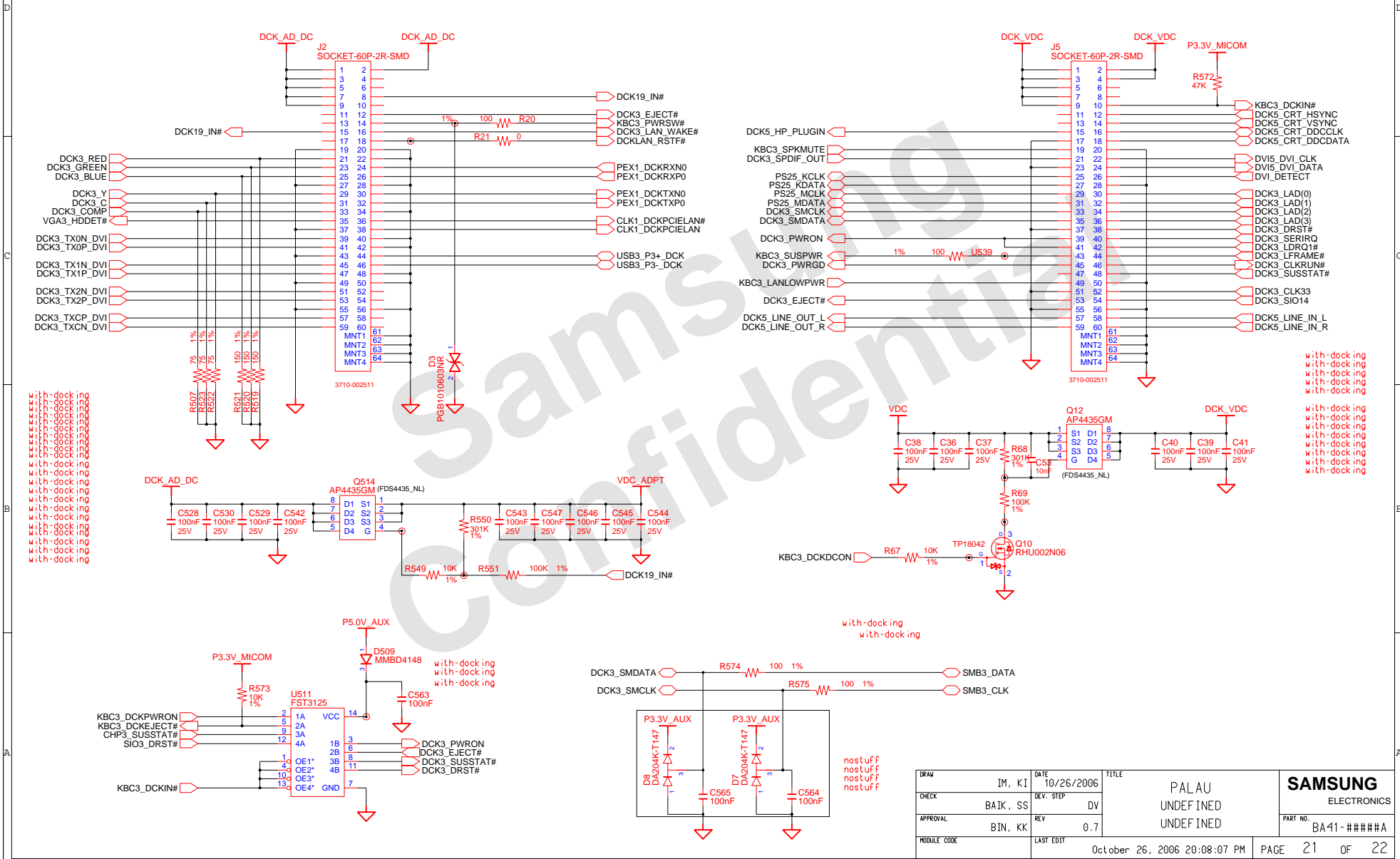
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DOCKING OPTION

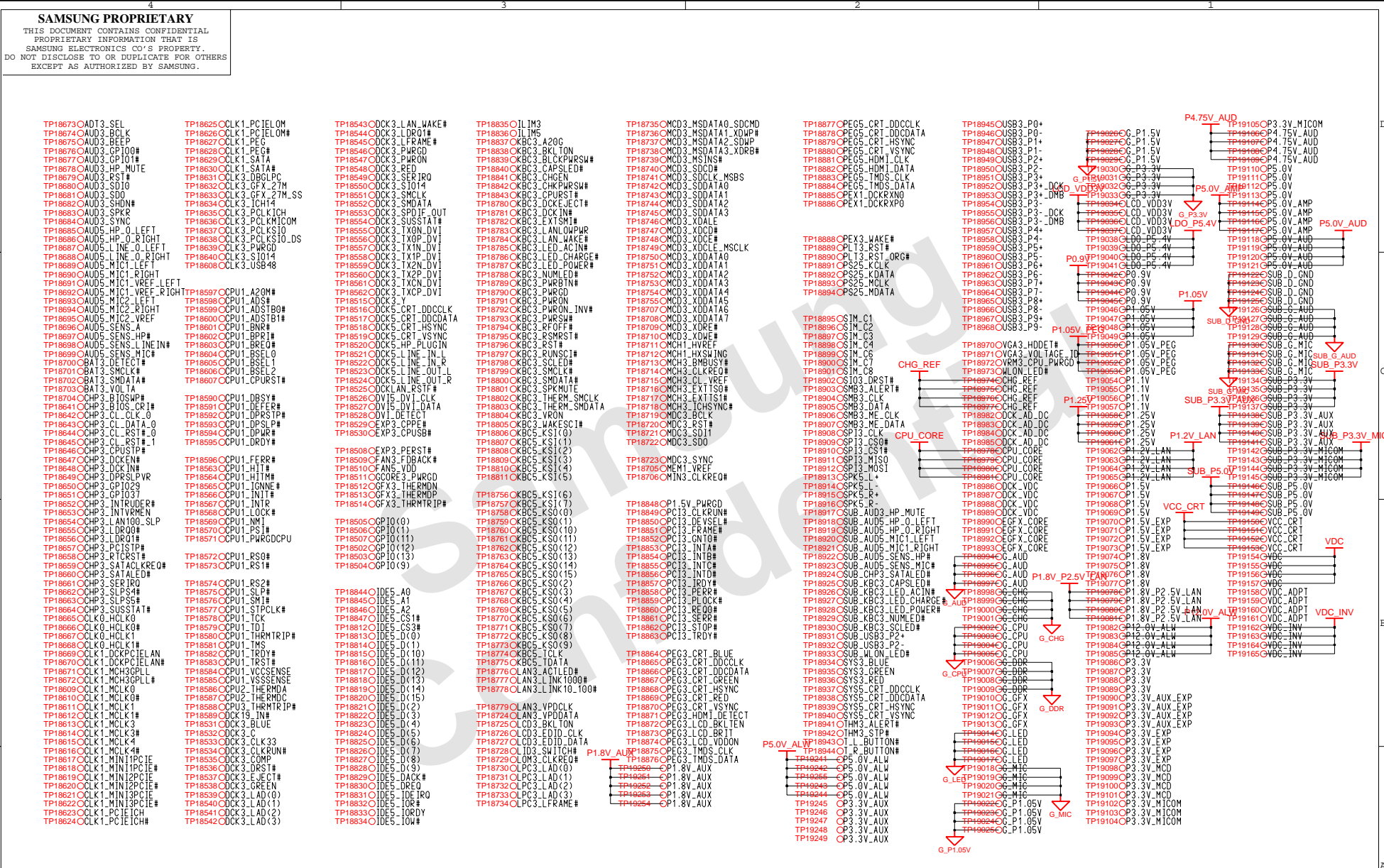
DOCKING CONNECTOR (130PIN)

Docking Placement

PWR1	1	129	PWR4
Top View			
PWR3	2	130	PWR2



DRAW	IM, KI	DATE	10/26/2006	TITLE	PALAU UNDEFINED	SAMSUNG ELECTRONICS PART NO. BA41-#####A
CHECK	BAIK, SS	DEV. STEP	DV		UNDEFINED	
APPROVAL	BIN, KK	REV	0.7		UNDEFINED	
MODULE CODE		LAST EDIT				
October 26, 2006 20:08:07 PM				PAGE	21	OF 22



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