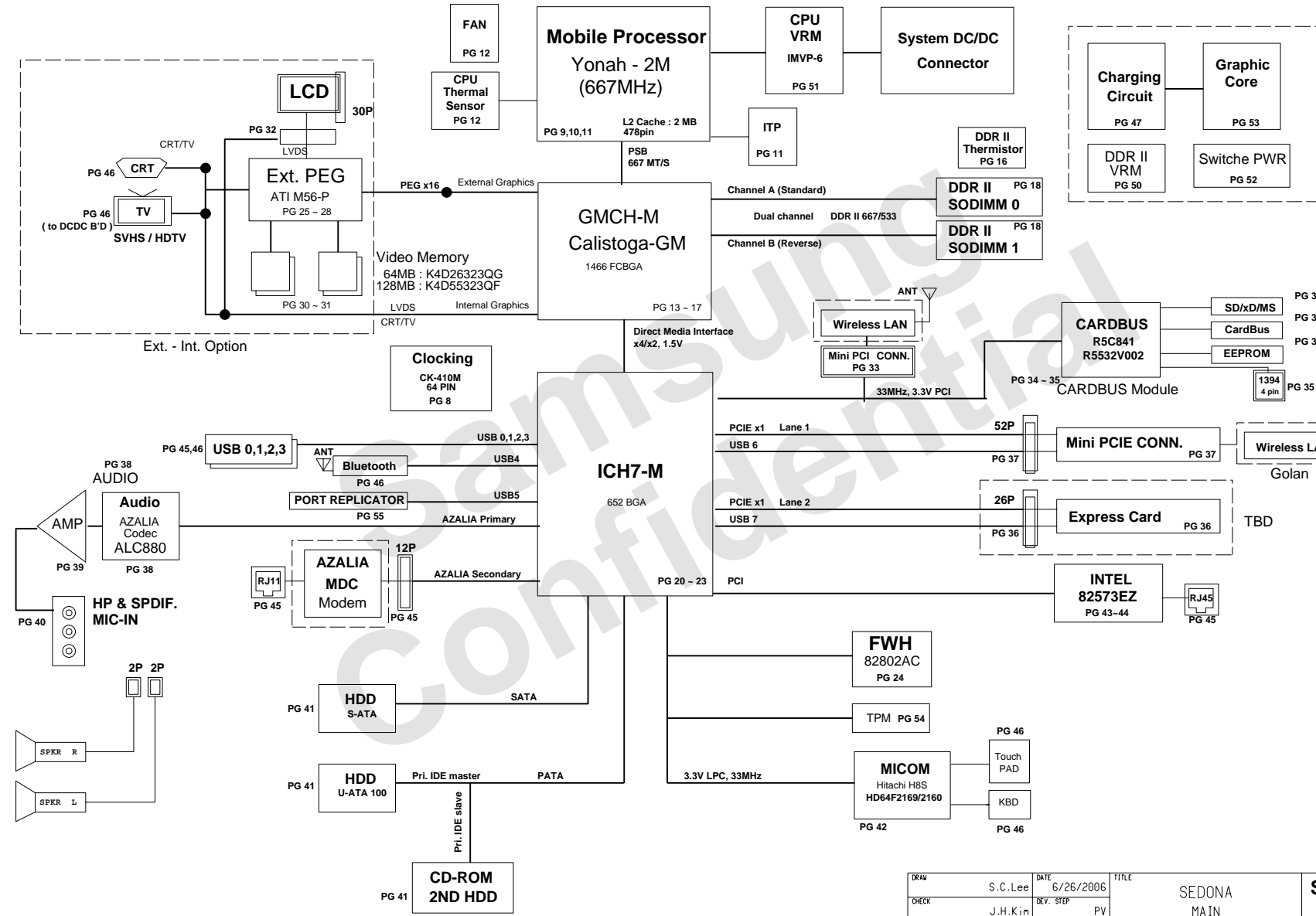


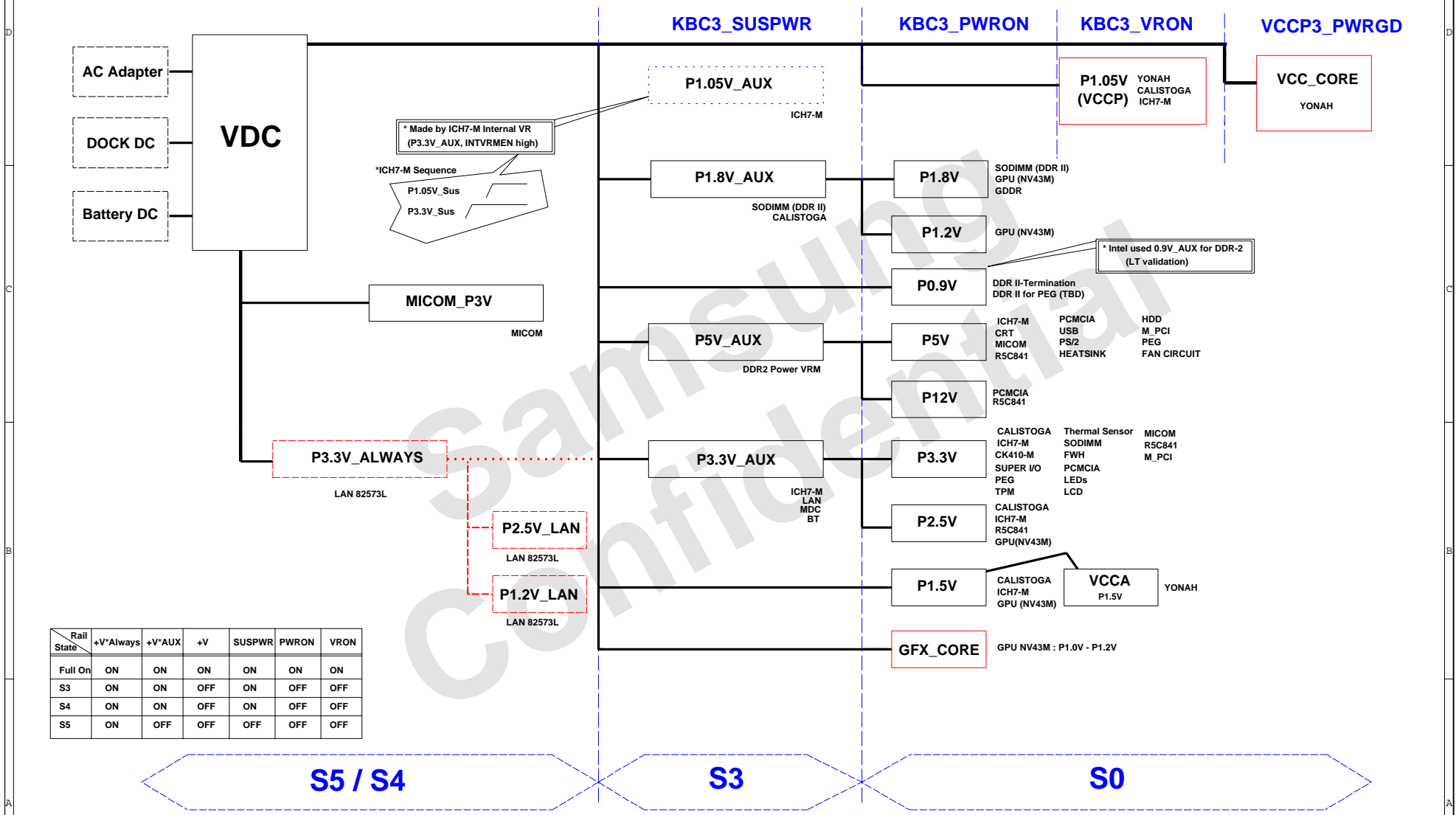
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DRAW	S.C.Lee	DATE	6/26/2006	TITLE	SEDONA	SAMSUNG ELECTRONICS
CHECK	J.H.Kim	DEV. STEP	PV	MAIN		
APPROVAL	S.S.Boek	REV	1.0	OPERATION BLOCK DIAGRAM	PART NO.	BA41-00697A
MODULE CODE		LAST EDIT		June 14, 2005 11:46:41 AM	PAGE	2 OF 58

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Power Diagram

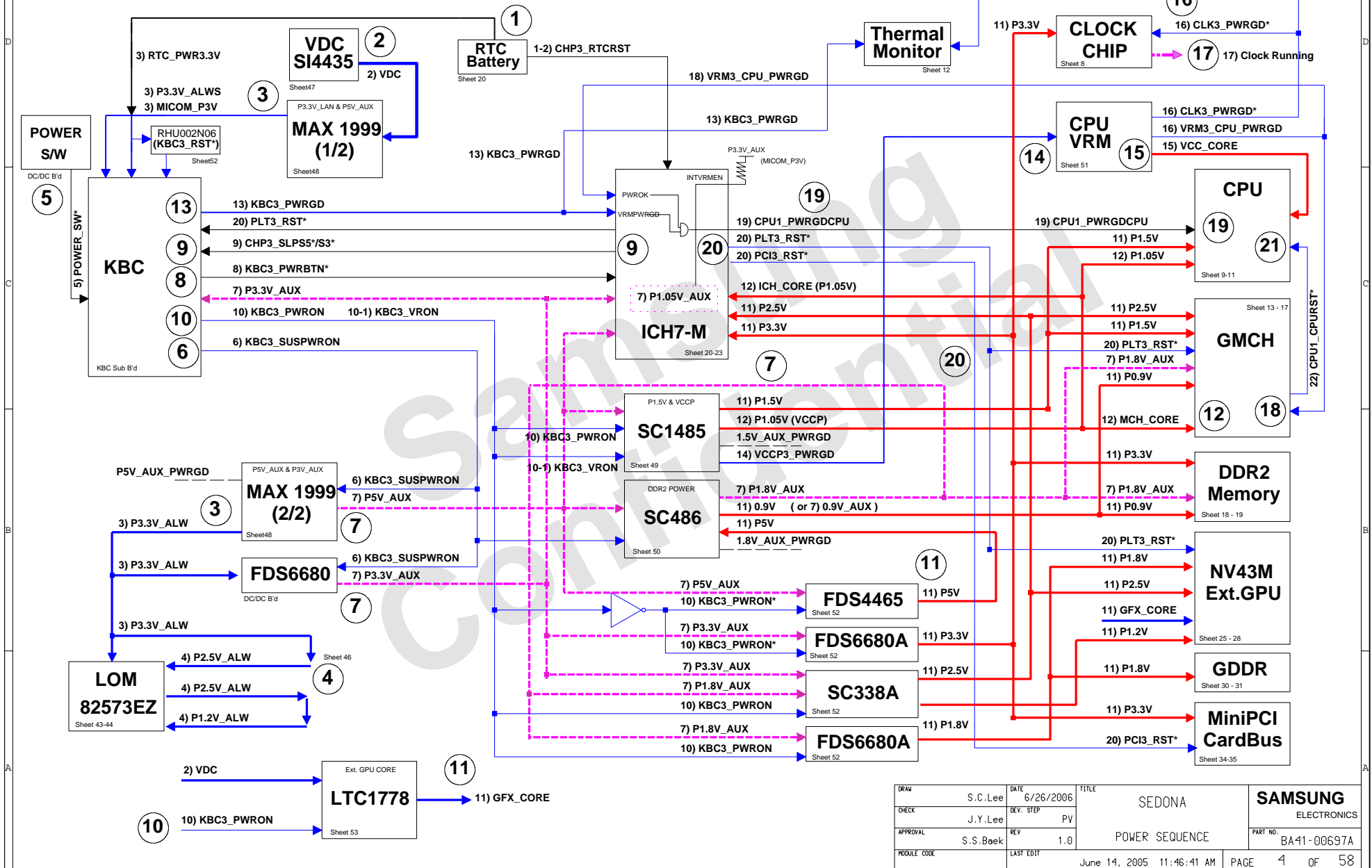


Rail State	+V*Always	+V*AUX	+V	SUSPWR	PWRON	VRON
Full On	ON	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF	OFF
S4	ON	ON	OFF	ON	OFF	OFF
S5	ON	OFF	OFF	OFF	OFF	OFF

DRAW	S.C.Lee	DATE	6/26/2006	TITLE	SEDONA MAIN POWER DIAGRAM	SAMSUNG ELECTRONICS PART NO. BA41-00697A
CHECK	J.Y.Lee	DEV. STEP	PV			
APPROVAL	S.S.Boek	REV	1.0			
MODULE CODE		LAST EDIT	June 14, 2005 11:46:41 AM	PAGE	3 OF 58	

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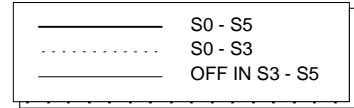
POWER SEQUENCE Rev. 0.7



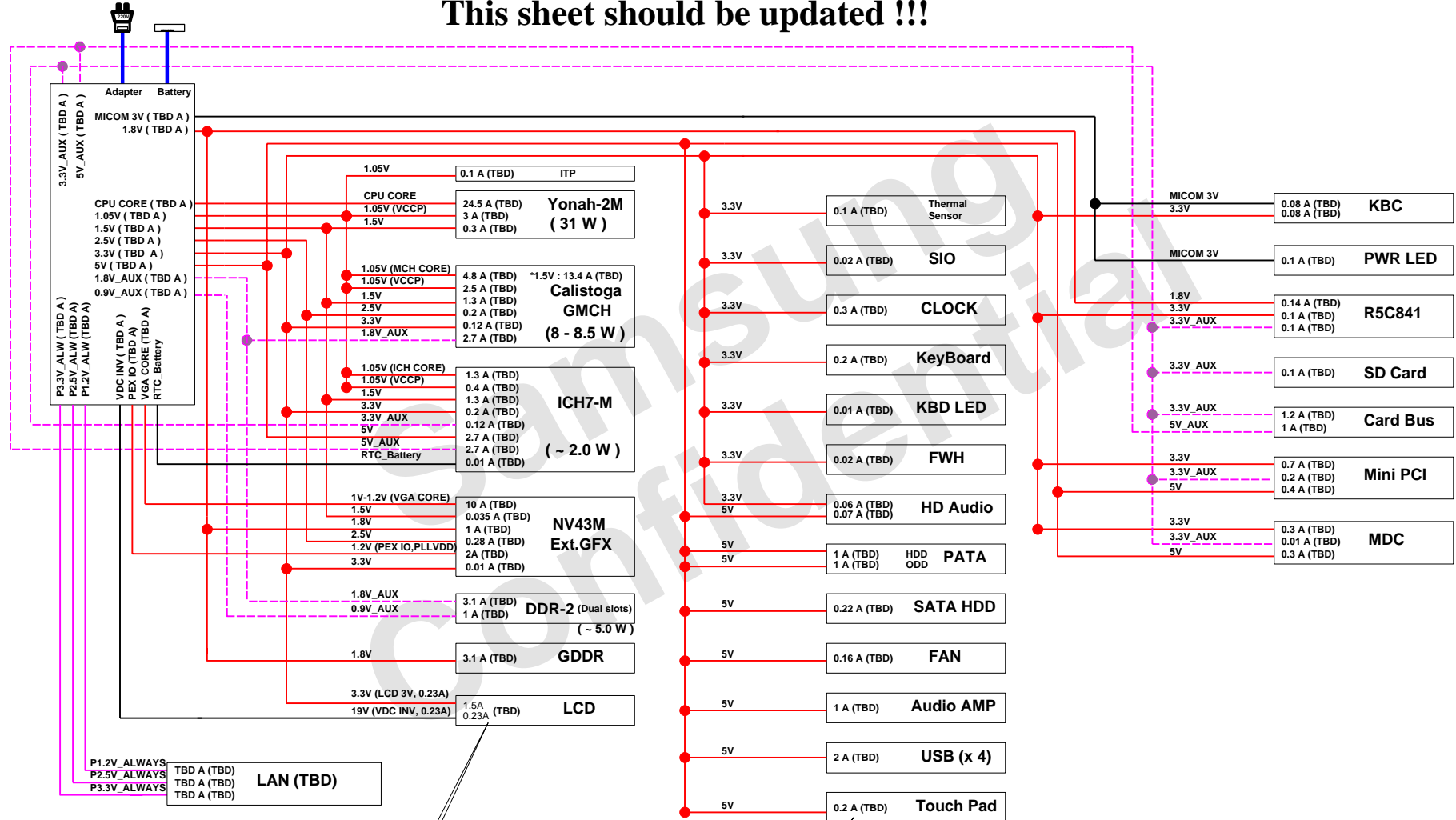
DRAW	S.C.Lee	DATE	6/26/2006	TITLE	SEDONA	SAMSUNG ELECTRONICS
CHECK	J.Y.Lee	DEV. STEP	PV	POWER SEQUENCE		
APPROVAL	S.S.Boek	REV	1.0	June 14, 2005 11:46:41 AM		PART NO. BA41-00697A
MODULE CODE		LAST EDIT		PAGE 4 OF 58		

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POWER RAILS ANALYSIS Rev. 0.7



This sheet should be updated !!!

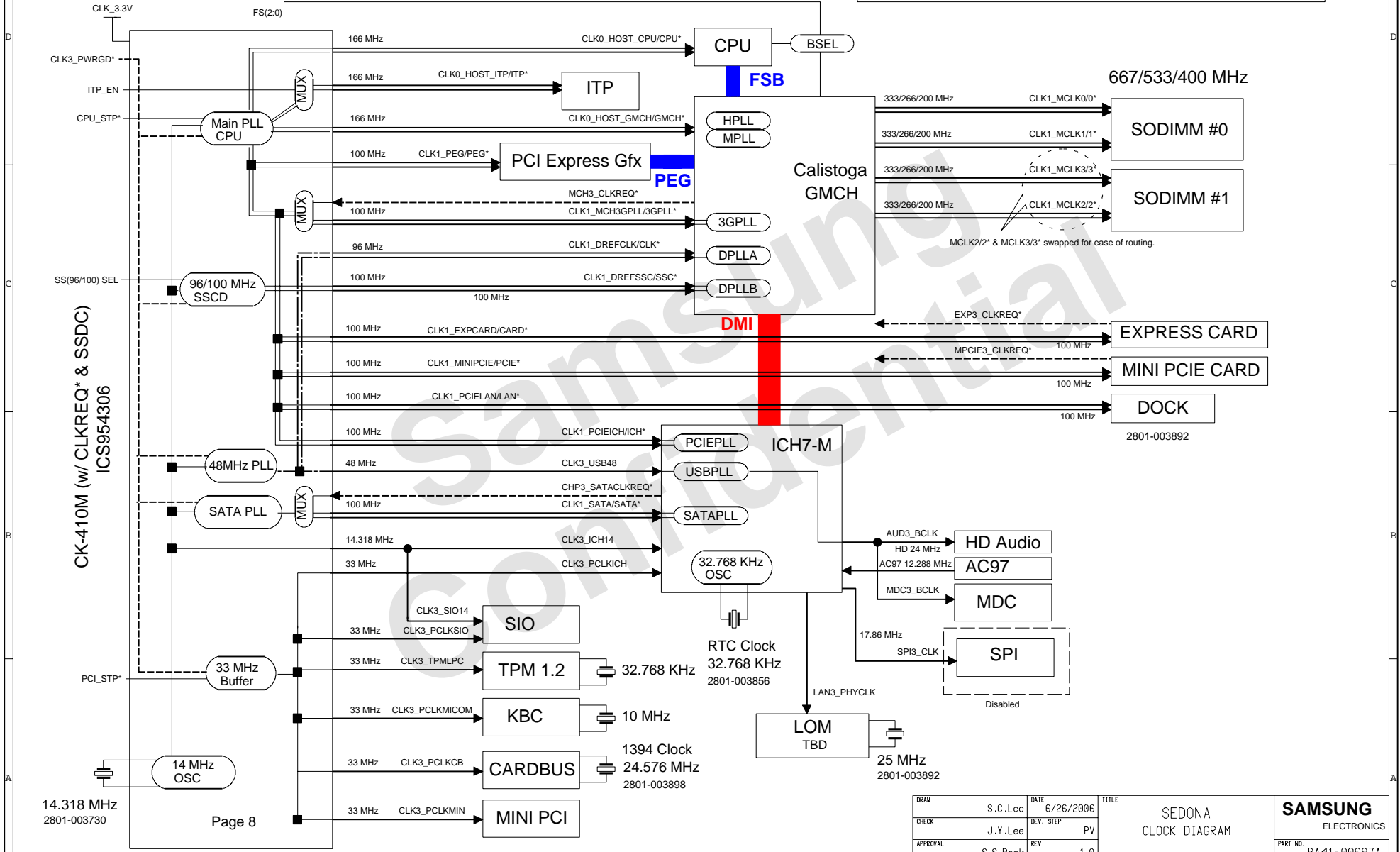


Value by Datasheet/Application notes (Value by measurement)

DRAW	S.C.Lee	DATE	6/26/2006	TITLE	SEDONA POWER BLOCK	SAMSUNG ELECTRONICS
CHECK	J.Y.Lee	DEV. STEP	PV			
APPROVAL	S.S.Boek	REV	1.0			PART NO. BA41-00697A
MODULE CODE		LAST EDIT	June 14, 2005 11:46:41 AM	PAGE	5	OF 58

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CLOCK DISTRIBUTION Rev. 0.7



CK-410M (w/ CLKREQ* & SSCD)
ICS954306

Page 8

DRAW	S.C.Lee	DATE	6/26/2006	TITLE	SEDONA CLOCK DIAGRAM	SAMSUNG ELECTRONICS PART NO. BA41-00697A
CHECK	J.Y.Lee	DEV. STEP	PV			
APPROVAL	S.S.Boek	REV	1.0			
MODULE CODE		LAST EDIT				
				June 14, 2005 11:46:41 AM	PAGE	6 OF 58

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TBD

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
Cardbus	AD25	0	A,B,C
LAN	AD21	3	G
MiniPCI SLOT1	AD23	2	D,E
USB	AD29(internal)	-	USB2.0 #0 : A USB2.0 #1 : D USB2.0 #2 : C
Hub to PCI	AD30(internal)	-	D
LPC Bridge/IDE/AC97/SMBUS	AD31(internal)	-	E
Internal MAC	AD24(internal)	-	E
AC Link	-	-	B

Voltage Rails

VDC	Primary DC system power supply (7 to 21V)
VCC_CORE	Core voltage for DOTHAN (1.308~1.068V)
VTT	DOTHAN/ALVISO Processor System Bus(PSB) Termination (1.05V) MCH-M Core Voltage
P0.9V	0.9V switched power rail (off in S3-S5)
P1.2V	1.2V switched power rail (off in S3-S5)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.5V_AUX	1.5V power rail (off in S4-S5)
P1.8V	1.8V switched power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail (off in S4-S5)
P2.5V	2.5V switched power rail (off in S3-S5)
MICOM_P3V	3.3V always on power rail for MICOM
P3.3V	3.3V switched power rail (off in S3-S5)
P3.3V_AUX	3.3V power rail (off in S4-S5)
P3.3V_DTV	3.3V power rail (off in S4-S5)
P5V	5.0V switched power rail (off in S3-S5)
P5V_AUX	5.0V power rail (off in S4-S5)
P3.3V_ALWS	3.3V power rail (Always On)
P2.5V_ALWS	2.5V power rail (Always On)
P1.2V_ALWS	1.2V power rail (Always On)

I / SMB Address

Devices	Address	Hex	Bus
ICH7	Master	-	SMBUS Master
EMC6N300(CPU Thermal Sensor)	1001 110X	9Ch	Thermal Sensor
SODIMM0	1010 0000	A0h	-
SODIMM1	1010 001X	A2h	-
CK-408 (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable

USB PORT Assign

PORT NUMBER	ASSIGNED TO
0	SYSTEM PORT A
1,2	SYSTEM PORT B
3	SYSTEM PORT C
4	BLUETOOTH
5	PORT REPLICATOR
6	MINI PCI EXPRESS FINGER PRINT
7	EXPRESS CARD

System Power States

- CHP3_SLPS1* S1, Powered-On-Suspend(POS) : In this state, all clocks(except the 32.768KHz clock) are stopped.
 The system context is maintained in system DRAM. Power is maintained to PCI, the CPU, memory controller, memory, and all other critical subsystems.
 Note that this state does not preclude power being removed from non-essential devices, such as disk drives. During this state, CPU can be selected for either Deep Sleep or Deeper Sleep.
 In Deeper Sleep, CPU voltage reduced in this state to reduce the leakage power.
- CHP3_SLPS3* S3, Suspend-To-RAM(STR) : The system context is maintained in system DRAM, but power is shut off to non-critical circuits.
 Memory is retained, and refreshes continue. All clocks stop except RTC clock.
- CHP3_SLPS4* S4, Suspend-To-Disk(STD) : The Context of the system is maintained on the disk. All power is then shut off to the system except for the logic required to resume.
 Externally appears same as S5, but may have different wake events.
- CHP3_SLPS5* S5, Soft Off(SOFF) : System context is not maintained. All power is shut off except for the logic required to restart. A full boot is required when waking.

Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	ICH7-M	Real Time Clock
Crystal	10MHz	MICOM	HD64F2169/2160
Crystal	14.318MHz	CLOCK-Generator	CK-410M
Crystal	24.576MHz	Cardbus Controller	Cardbus Controller
Crystal	25MHz	LAN	Intel LAN
Crystal	27MHz	VIDEO	PEG (NV43m)
Crystal	24.576MHz (TBD)	HD Audio	Audio

CPU Core Voltage Table MVP-6

Active Mode		Active/Deeper Sleep Dual Mode Region		Deeper Sleep/Extended Deeper Sleep Dual Mode Region	
VID(6.0)	Voltage	VID(6.0)	Voltage	VID(6.0)	Voltage
0 0 0 0 0 0 0	1.5000 V	0 1 0 1 0 0 0	1.0000 V	1 0 1 0 0 0 1	0.4875 V
0 0 0 0 0 0 1	1.4875 V	0 1 0 1 0 0 1	0.9875 V	1 0 1 0 0 1 0	0.4750 V
0 0 0 0 0 1 0	1.4750 V	0 1 0 1 0 1 0	0.9750 V	1 0 1 0 0 1 1	0.4625 V
0 0 0 0 0 1 1	1.4625 V	0 1 0 1 0 1 1	0.9625 V	1 0 1 0 0 1 0	0.4500 V
0 0 0 0 1 0 0	1.4500 V	0 1 0 1 1 0 0	0.9500 V	1 0 1 0 1 0 1	0.4375 V
0 0 0 0 1 0 1	1.4375 V	0 1 0 1 1 0 1	0.9375 V	1 0 1 0 1 0 0	0.4250 V
0 0 0 0 1 1 0	1.4250 V	0 1 0 1 1 1 0	0.9250 V	1 0 1 0 1 0 1	0.4125 V
0 0 0 0 1 1 1	1.4125 V	0 1 0 1 1 1 1	0.9125 V	1 0 1 0 1 0 0	0.4000 V
0 0 0 1 0 0 0	1.4000 V	0 1 1 0 0 0 0	0.9000 V	1 0 1 1 0 0 1	0.3875 V
0 0 0 1 0 0 1	1.3875 V	0 1 1 0 0 0 1	0.8875 V	1 0 1 1 0 0 0	0.3750 V
0 0 0 1 0 1 0	1.3750 V	0 1 1 0 0 1 0	0.8750 V	1 0 1 1 0 0 1	0.3625 V
0 0 0 1 0 1 1	1.3625 V	0 1 1 0 0 1 1	0.8625 V	1 0 1 1 0 0 0	0.3500 V
0 0 0 1 1 0 0	1.3500 V	0 1 1 0 1 0 0	0.8500 V	1 0 1 1 1 0 1	0.3375 V
0 0 0 1 1 0 1	1.3375 V	0 1 1 0 1 0 1	0.8375 V	1 0 1 1 1 0 0	0.3250 V
0 0 0 1 1 1 0	1.3250 V	0 1 1 0 1 1 0	0.8250 V	1 0 1 1 1 0 1	0.3125 V
0 0 0 1 1 1 1	1.3125 V	0 1 1 0 1 1 1	0.8125 V	1 1 0 0 0 0 0	0.3000 V
0 0 0 1 0 0 0	1.3000 V	0 1 1 1 0 0 0	0.8000 V	1 1 0 0 0 0 1	0.2875 V
0 0 0 1 0 0 1	1.2875 V	0 1 1 1 0 0 1	0.7875 V	1 1 0 0 0 0 0	0.2750 V
0 0 0 1 0 1 0	1.2750 V	0 1 1 1 0 1 0	0.7750 V	1 1 0 0 0 0 1	0.2625 V
0 0 0 1 0 1 1	1.2625 V	0 1 1 1 0 1 1	0.7625 V	1 1 0 0 0 1 0	0.2500 V
0 0 0 1 1 0 0	1.2500 V	0 1 1 1 1 0 0	0.7500 V	1 1 0 0 0 1 1	0.2375 V
0 0 0 1 1 0 1	1.2375 V	0 1 1 1 1 0 1	0.7375 V	1 1 0 0 0 1 0	0.2250 V
0 0 0 1 1 1 0	1.2250 V	0 1 1 1 1 1 0	0.7250 V	1 1 0 0 0 1 1	0.2125 V
0 0 0 1 1 1 1	1.2125 V	0 1 1 1 1 1 1	0.7125 V	1 1 0 0 1 0 0	0.2000 V
0 0 0 1 0 0 0	1.2000 V	1 0 0 0 0 0 0	0.7000 V	1 1 0 0 1 0 1	0.1875 V
0 0 0 1 0 0 1	1.1875 V	1 0 0 0 0 0 1	0.6875 V	1 1 0 0 1 0 0	0.1750 V
0 0 0 1 0 1 0	1.1750 V	1 0 0 0 0 1 0	0.6750 V	1 1 0 0 1 0 1	0.1625 V
0 0 0 1 0 1 1	1.1625 V	1 0 0 0 0 1 1	0.6625 V	1 1 0 0 1 1 0	0.1500 V
0 0 0 1 1 0 0	1.1500 V	1 0 0 0 1 0 0	0.6500 V	1 1 0 0 1 1 1	0.1375 V
0 0 0 1 1 0 1	1.1375 V	1 0 0 0 1 0 1	0.6375 V	1 1 0 0 1 1 0	0.1250 V
0 0 0 1 1 1 0	1.1250 V	1 0 0 0 1 1 0	0.6250 V	1 1 0 0 1 1 1	0.1125 V
0 0 0 1 1 1 1	1.1125 V	1 0 0 0 1 1 1	0.6125 V	1 1 0 0 0 0 0	0.1000 V
0 1 0 0 0 0 0	1.1000 V	1 0 0 0 0 0 0	0.6000 V	1 1 0 0 0 0 1	0.0875 V
0 1 0 0 0 0 1	1.0875 V	1 0 0 0 0 0 1	0.5875 V	1 1 0 0 0 1 0	0.0750 V
0 1 0 0 0 1 0	1.0750 V	1 0 0 0 0 1 0	0.5750 V	1 1 0 0 0 1 1	0.0625 V
0 1 0 0 0 1 1	1.0625 V	1 0 0 0 0 1 1	0.5625 V	1 1 0 0 1 0 0	0.0500 V
0 1 0 0 1 0 0	1.0500 V	1 0 0 0 1 0 0	0.5500 V	1 1 0 0 1 0 1	0.0375 V
0 1 0 0 1 0 1	1.0375 V	1 0 0 0 1 0 1	0.5375 V	1 1 0 0 1 0 0	0.0250 V
0 1 0 0 1 1 0	1.0250 V	1 0 0 0 1 1 0	0.5250 V	1 1 0 0 1 0 1	0.0125 V
0 1 0 0 1 1 1	1.0125 V	1 0 0 0 1 1 1	0.5125 V	1 1 0 0 1 1 0	0.0000 V
		1 0 0 0 0 0 0	0.5000 V	1 1 0 0 1 1 1	0.0000 V
				1 1 1 0 0 0 0	0.0000 V
				1 1 1 0 0 0 1	0.0000 V
				1 1 1 0 0 1 0	0.0000 V
				1 1 1 0 0 1 1	0.0000 V
				1 1 1 0 1 0 0	0.0000 V
				1 1 1 0 1 0 1	0.0000 V
				1 1 1 0 1 1 0	0.0000 V
				1 1 1 0 1 1 1	0.0000 V
				1 1 1 1 0 0 0	0.0000 V
				1 1 1 1 0 0 1	0.0000 V
				1 1 1 1 0 1 0	0.0000 V
				1 1 1 1 0 1 1	0.0000 V
				1 1 1 1 1 0 0	0.0000 V
				1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0	0.0000 V
				1 1 1 1 1 1 1	0.0000 V

Active: DPRSLPVR 0, DPRSTP* 1, PSI2* 0 or 1
 Deeper Slp: DPRSLPVR 1, DPRSTP* 0, PSI2* 0 or 1

**11111111* : 0V power good asserted.

*Yonah Processor (2.33 GHz / 800 MHz : TBD)

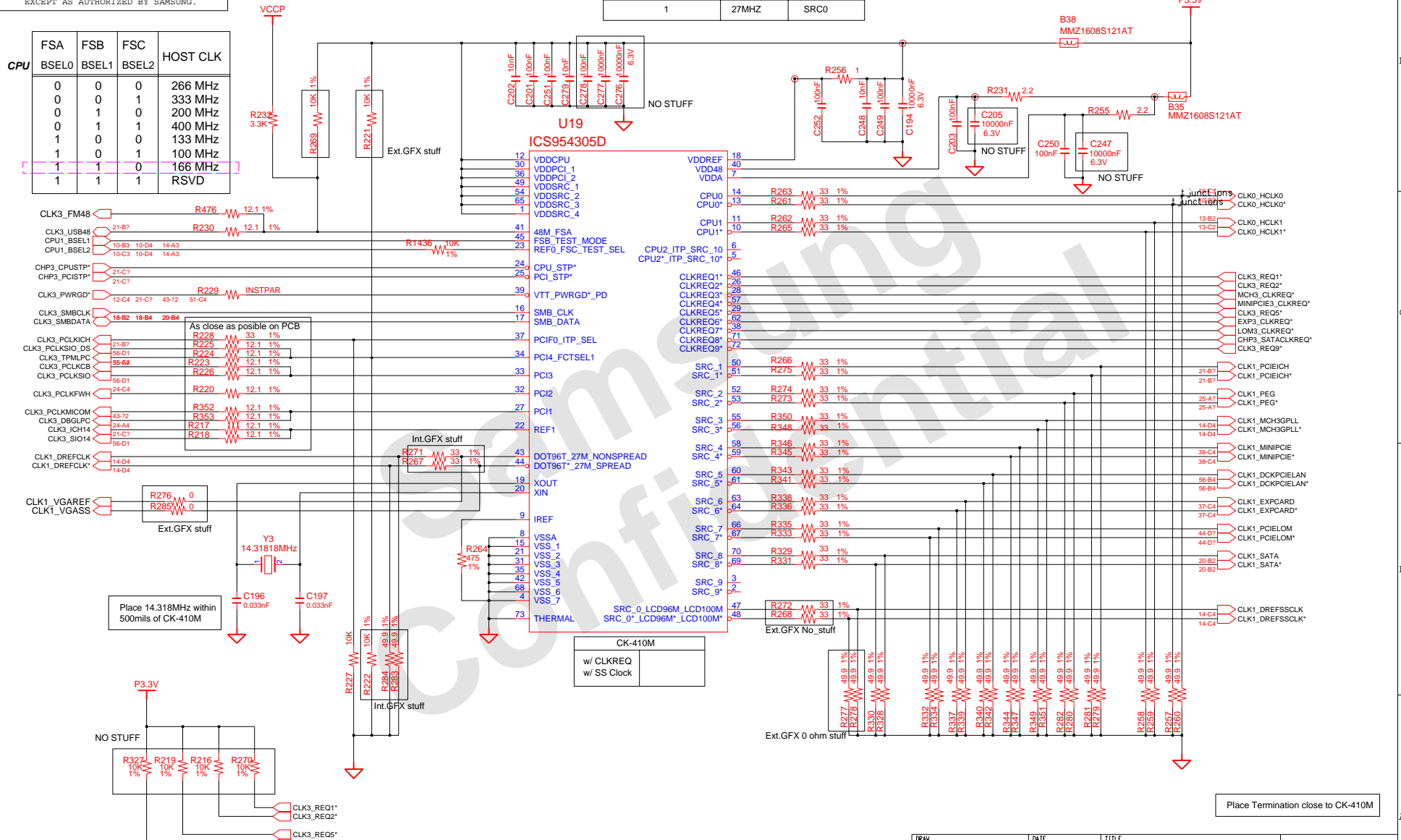
DRAW	S.C.Lee	DATE	6/26/2006	TITLE	SEDONA MAIN BOARD INFORMATION	SAMSUNG ELECTRONICS
CHECK	J.Y.Lee	REV. STEP	PV			
APPROVAL	S.S.Baek	REV	1.0			PART NO. BA41-00697A
MODULE CODE		LAST EDIT	June 14, 2005 11:46:41 AM	PAGE	7	OF 58

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PCI4_FCTSEL1(PIN34)	PIN 43, 44	PIN 47, 48
0	DOT96	LCD96/100
1	27MHZ	SRC0

CPU	FSA BSEL0	FSB BSEL1	FSC BSEL2	HOST CLK
	0	0	0	266 MHz
	0	0	1	333 MHz
	0	1	0	200 MHz
	0	1	1	400 MHz
	1	0	0	133 MHz
	1	0	1	100 MHz
	1	1	0	166 MHz
	1	1	1	RSVD

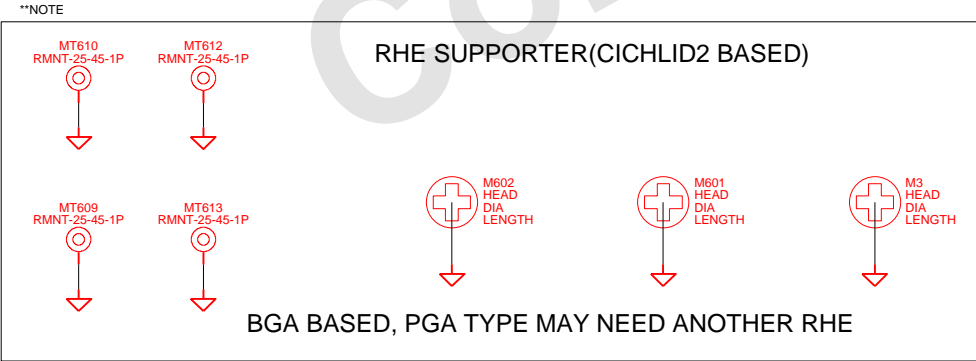
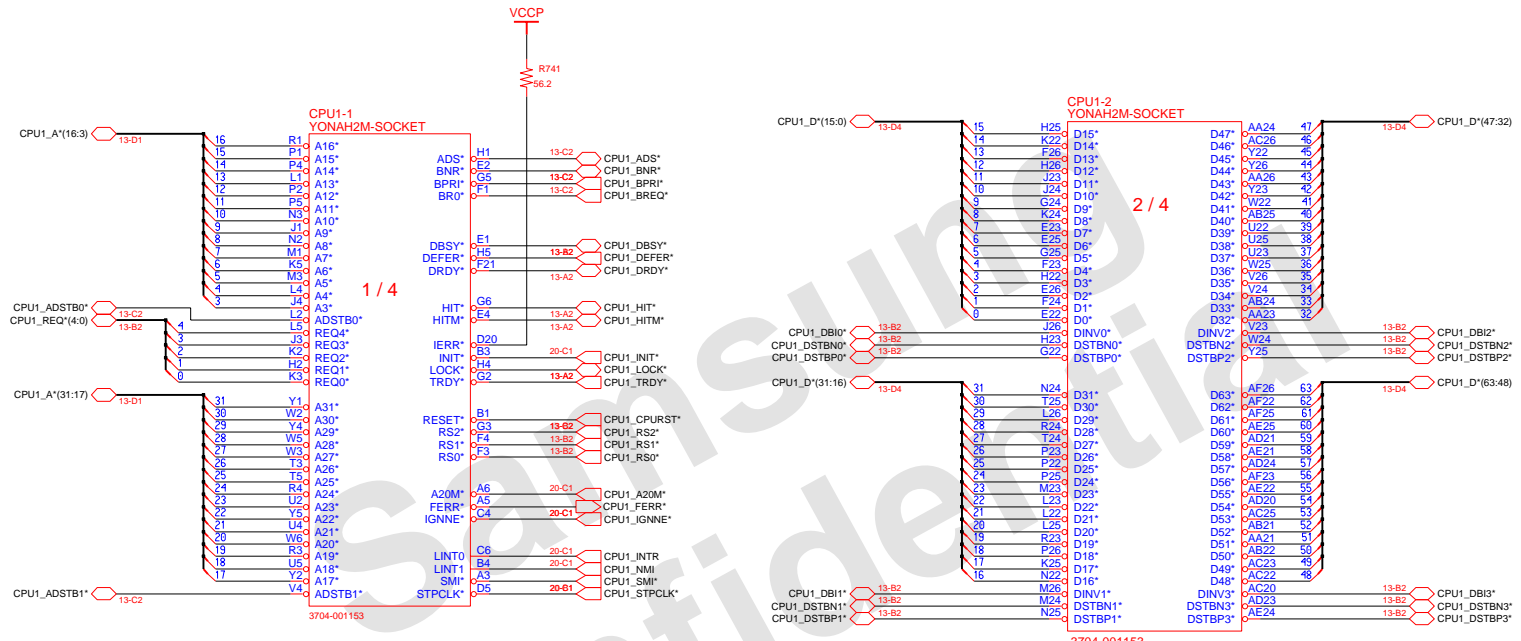


Place 14.318MHz within 500mils of CK-410M

Place Termination close to CK-410M

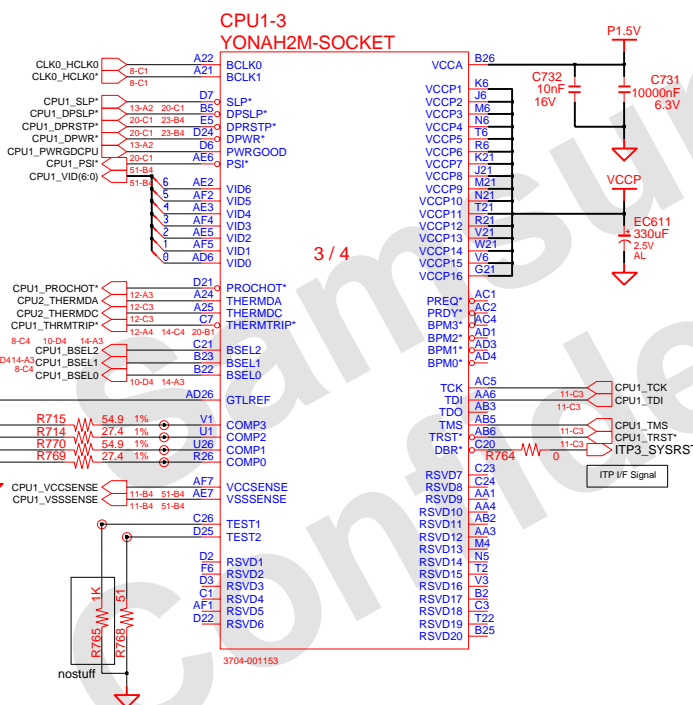
DRAW	S.C.Lee	DATE	6/26/2006	TITLE	SEDONA MAIN CLOCK GENERATOR	SAMSUNG ELECTRONICS PART NO. BA41-00697A
CHECK	J.Y.Lee	DEV. STEP	PV			
APPROVAL	S.S.Boek	REV	1.0			
MODULE CODE		LAST EDIT	June 14, 2005 11:46:41 AM	PAGE	8 OF 58	

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DRAW	S.C.Lee	DATE	6/26/2006	TITLE	SEDONA MAIN	SAMSUNG ELECTRONICS
CHECK	J.Y.Lee	DEV. STEP	PV	YONAH CPU (1/3)		
APPROVAL	S.S.Boek	REV	1.0	PART NO. BA41-00697A		PAGE 9 OF 58
MODULE CODE		LAST EDIT	June 14, 2005 11:46:41 AM			

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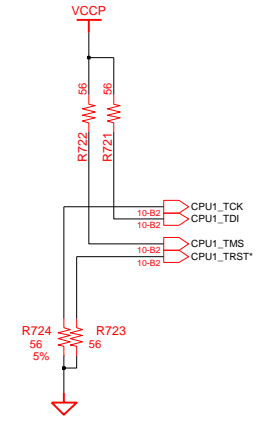
CPU Core Voltage Table IMVP-6

Active Mode		Active/Deeper Sleep Dual Mode Region		Deeper Sleep/Extended Deeper Sleep Dual Mode Region	
VID(6:0)	Voltage	VID(6:0)	Voltage	VID(6:0)	Voltage
0 0 0 0 0 0 0	1.5000 V	0 1 0 1 0 0 0	1.0000 V	1 0 1 0 0 0 1	0.4875 V
0 0 0 0 0 0 1	1.4875 V	0 1 0 1 0 0 1	0.9875 V	1 0 1 0 0 0 1	0.4750 V
0 0 0 0 0 1 0	1.4750 V	0 1 0 1 0 1 0	0.9750 V	1 0 1 0 0 1 1	0.4625 V
0 0 0 0 0 1 1	1.4625 V	0 1 0 1 0 1 1	0.9625 V	1 0 1 0 1 0 0	0.4500 V
0 0 0 0 1 0 0	1.4500 V	0 1 0 1 1 0 0	0.9500 V	1 0 1 0 1 0 1	0.4375 V
0 0 0 0 1 0 1	1.4375 V	0 1 0 1 1 0 1	0.9375 V	1 0 1 0 1 1 0	0.4250 V
0 0 0 0 1 1 0	1.4250 V	0 1 0 1 1 1 0	0.9250 V	1 0 1 0 1 1 1	0.4125 V
0 0 0 0 1 1 1	1.4125 V	0 1 1 0 0 0 0	0.9125 V	1 0 1 1 0 0 0	0.4000 V
0 0 0 1 0 0 0	1.4000 V	0 1 1 0 0 0 1	0.9000 V	1 0 1 1 0 0 1	0.3875 V
0 0 0 1 0 0 1	1.3875 V	0 1 1 0 0 1 0	0.8875 V	1 0 1 1 0 1 0	0.3750 V
0 0 0 1 0 1 0	1.3750 V	0 1 1 0 0 1 1	0.8750 V	1 0 1 1 1 0 0	0.3625 V
0 0 0 1 0 1 1	1.3625 V	0 1 1 0 1 0 0	0.8625 V	1 0 1 1 1 0 1	0.3500 V
0 0 0 1 1 0 0	1.3500 V	0 1 1 0 1 0 1	0.8500 V	1 0 1 1 1 1 0	0.3375 V
0 0 0 1 1 0 1	1.3375 V	0 1 1 0 1 1 0	0.8375 V	1 0 1 1 1 1 1	0.3250 V
0 0 0 1 1 1 0	1.3250 V	0 1 1 1 0 0 0	0.8250 V	1 0 1 1 1 1 1	0.3125 V
0 0 0 1 1 1 1	1.3125 V	0 1 1 1 0 0 1	0.8125 V	1 1 0 0 0 0 0	0.3000 V
0 0 1 0 0 0 0	1.3000 V	0 1 1 1 0 0 1	0.8000 V	1 1 0 0 0 0 1	0.2875 V
0 0 1 0 0 0 1	1.2875 V	0 1 1 1 0 1 0	0.7875 V	1 1 0 0 0 1 0	0.2750 V
0 0 1 0 0 1 0	1.2750 V	0 1 1 1 0 1 1	0.7750 V	1 1 0 0 1 0 0	0.2625 V
0 0 1 0 0 1 1	1.2625 V	0 1 1 1 1 0 0	0.7625 V	1 1 0 0 1 0 1	0.2500 V
0 0 1 0 1 0 0	1.2500 V	0 1 1 1 1 0 1	0.7500 V	1 1 0 0 1 1 0	0.2375 V
0 0 1 0 1 0 1	1.2375 V	0 1 1 1 1 1 0	0.7375 V	1 1 0 0 1 1 1	0.2250 V
0 0 1 0 1 1 0	1.2250 V	0 1 1 1 1 1 1	0.7250 V	1 1 0 1 0 0 0	0.2125 V
0 0 1 0 1 1 1	1.2125 V	0 1 1 1 1 1 1	0.7125 V	1 1 0 1 0 0 1	0.2000 V
0 0 1 1 0 0 0	1.2000 V	1 0 0 0 0 0 0	0.7000 V	1 1 0 1 0 1 0	0.1875 V
0 0 1 1 0 0 1	1.1875 V	1 0 0 0 0 0 1	0.6875 V	1 1 0 1 0 1 1	0.1750 V
0 0 1 1 0 1 0	1.1750 V	1 0 0 0 0 1 0	0.6750 V	1 1 0 1 1 0 0	0.1625 V
0 0 1 1 0 1 1	1.1625 V	1 0 0 0 0 1 1	0.6625 V	1 1 0 1 1 0 1	0.1500 V
0 0 1 1 1 0 0	1.1500 V	1 0 0 0 1 0 0	0.6500 V	1 1 0 1 1 1 0	0.1375 V
0 0 1 1 1 0 1	1.1375 V	1 0 0 0 1 0 1	0.6375 V	1 1 0 1 1 1 1	0.1250 V
0 0 1 1 1 1 0	1.1250 V	1 0 0 0 1 1 0	0.6250 V	1 1 1 0 0 0 0	0.1125 V
0 0 1 1 1 1 1	1.1125 V	1 0 0 0 1 1 1	0.6125 V	1 1 1 0 0 0 1	0.1000 V
0 1 0 0 0 0 0	1.1000 V	1 0 0 1 0 0 0	0.6000 V	1 1 1 0 0 1 0	0.0875 V
0 1 0 0 0 0 1	1.0875 V	1 0 0 1 0 0 1	0.5875 V	1 1 1 0 1 0 0	0.0750 V
0 1 0 0 0 1 0	1.0750 V	1 0 0 1 0 1 0	0.5750 V	1 1 1 0 1 0 1	0.0625 V
0 1 0 0 0 1 1	1.0625 V	1 0 0 1 0 1 1	0.5625 V	1 1 1 0 1 1 0	0.0500 V
0 1 0 0 1 0 0	1.0500 V	1 0 0 1 1 0 0	0.5500 V	1 1 1 0 1 1 1	0.0375 V
0 1 0 0 1 0 1	1.0375 V	1 0 0 1 1 0 1	0.5375 V	1 1 1 0 1 1 1	0.0250 V
0 1 0 0 1 1 0	1.0250 V	1 0 0 1 1 1 0	0.5250 V	1 1 1 1 0 0 0	0.0125 V
0 1 0 0 1 1 1	1.0125 V	1 0 0 1 1 1 1	0.5125 V	1 1 1 1 0 0 1	0.0000 V
0 1 0 1 0 0 0	1.0125 V	1 0 0 1 1 1 1	0.5000 V	1 1 1 1 0 1 0	0.0000 V
				1 1 1 1 0 1 1	0.0000 V
				1 1 1 1 1 0 0	0.0000 V
				1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0	0.0000 V
				1 1 1 1 1 1 1	0.0000 V

*Yonah Processor (2.33 GHz / 800 MHz : TBD)

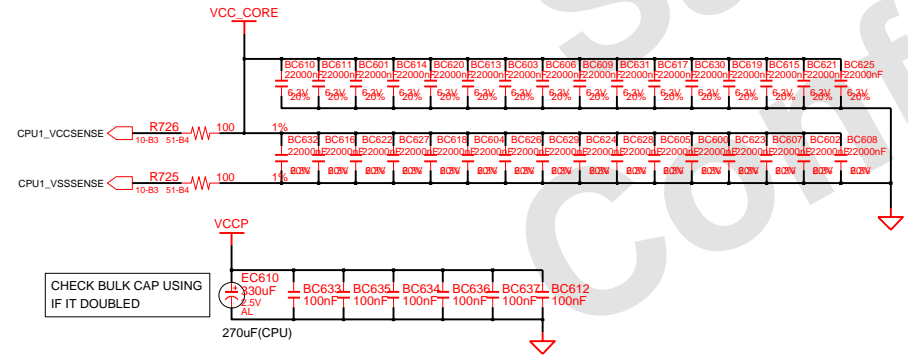
DRAW	S.C.Lee	DATE	6/26/2006	TITLE	SEDONA MAIN YONAH CPU(2/3)	SAMSUNG ELECTRONICS PART NO. BA41-00697A
CHECK	J.Y.Lee	DEV. STEP	PV			
APPROVAL	S.S.Boek	REV	1.0			
MODULE CODE		LAST EDIT	June 14, 2005 11:46:41 AM	PAGE	10 OF 58	

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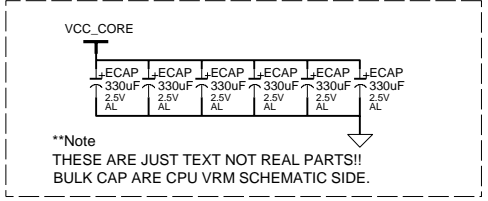


****Note**
 WHEN ITP NOT USED STUFF THIS BLOCK ONLY
 WITHIN 2.0" OF CPU & DELETE THE OTHERS

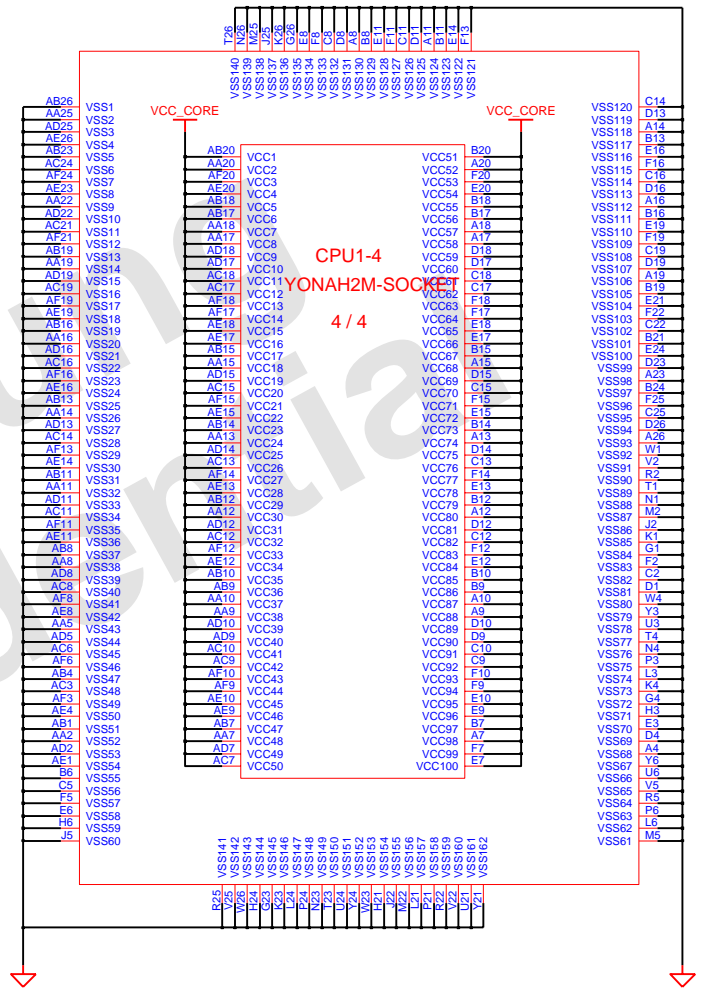
ITP/XDP



CHECK BULK CAP USING
 IF IT DOUBLED



****Note**
 THESE ARE JUST TEXT NOT REAL PARTS!!
 BULK CAP ARE CPU VRM SCHEMATIC SIDE.

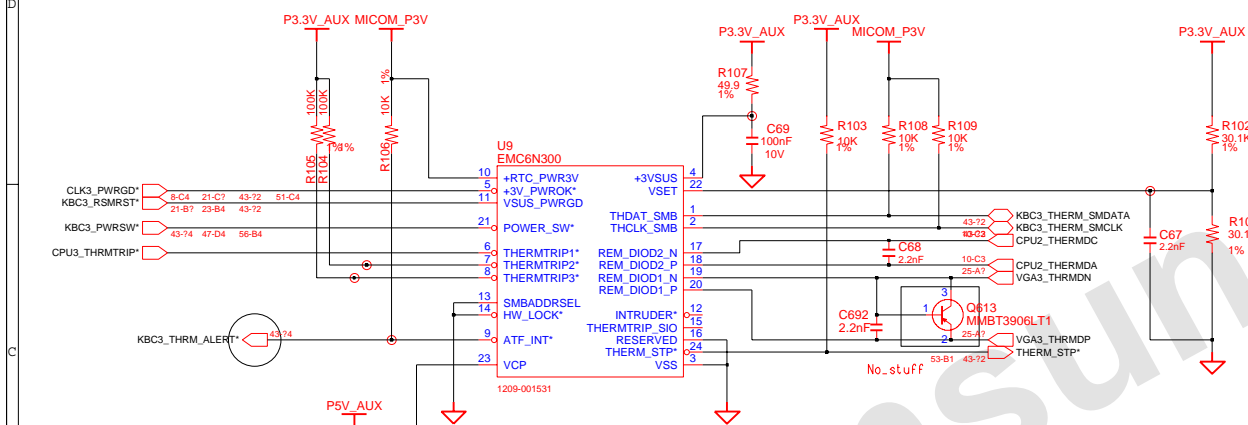


DRAW	S.C.Lee	DATE	6/26/2006	TITLE	SEDONA	SAMSUNG ELECTRONICS
CHECK	J.Y.Lee	DEV. STEP	PV	MAIN		
APPROVAL	S.S.Boek	REV	1.0	YONAH CPU(3/3)		PART NO. BA41-00697A
MODULE CODE		LAST EDIT				

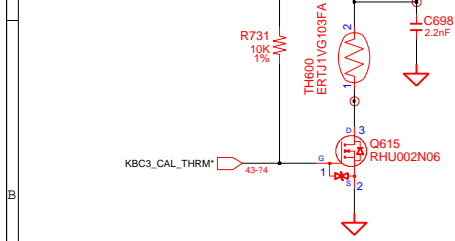
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CPU / DDR2 Thermal Sensor

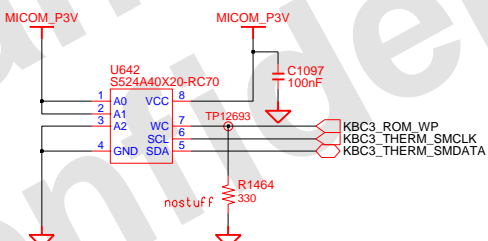
- Refer To Thermal Sensor Layout Guidelines.**
- Place the Thermal Sensor close to a remote diode.
 - Keep traces away from high voltage (+12V bus)
 - Keep traces away from fast data buses and CRT signal.
 - Use recommended trace widths and spacings (10mil)
 - Place a ground plane under the traces.
 - Use guard traces flanking DXP and DXN and connecting to GND



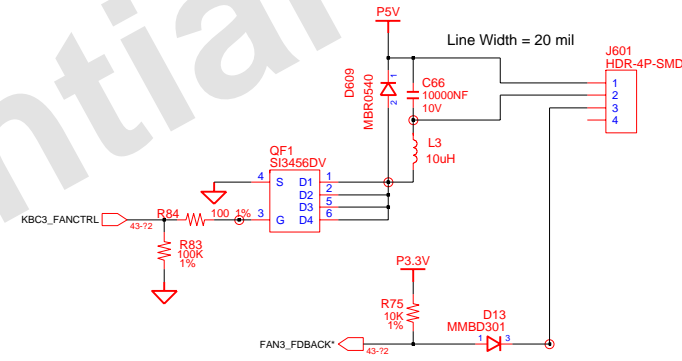
PLACE NEAR TO DDR2 SODIMM



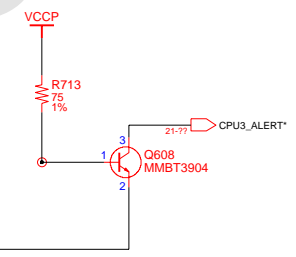
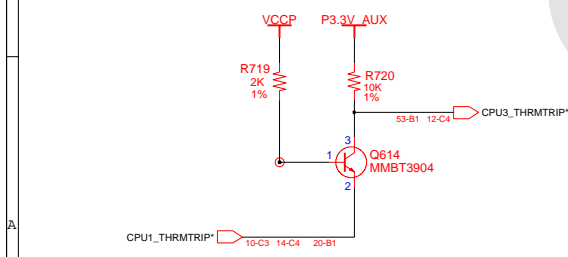
SMART KEY SOLUTION



FAN Control Logic

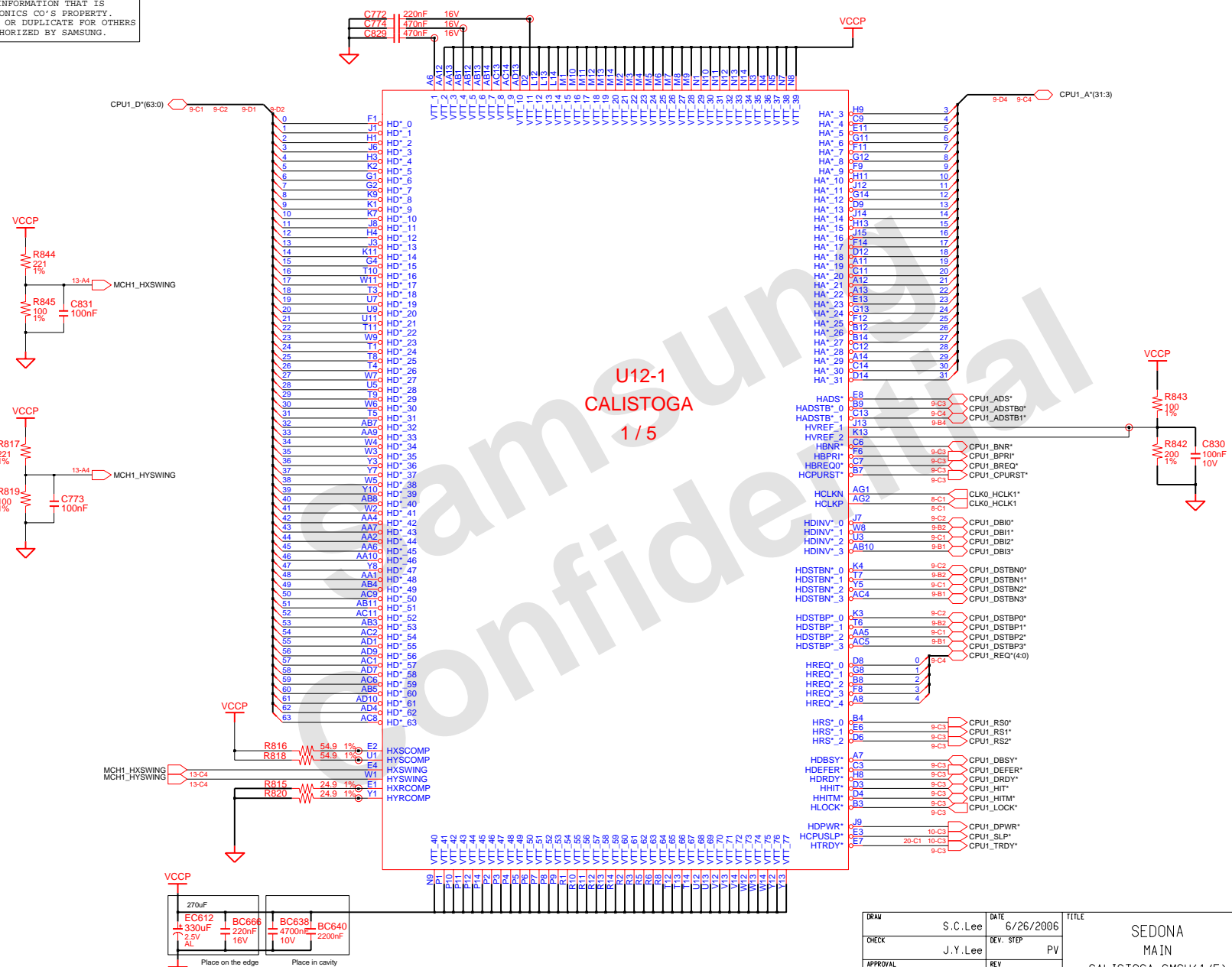


Changed to Control Methode(EBL)



DRAW	S.C.Lee	DATE	6/26/2006	TITLE	SEDONA	SAMSUNG ELECTRONICS
CHECK	J.Y.Lee	DEV. STEP	PV	MAIN		
APPROVAL	S.S.Boek	REV	1.0	THERMAL SENSOR/FAN CONTRL	PART NO.	BA41-00697A
MODULE CODE		LAST EDIT	June 14, 2005 11:46:41 AM	PAGE	12	OF 58

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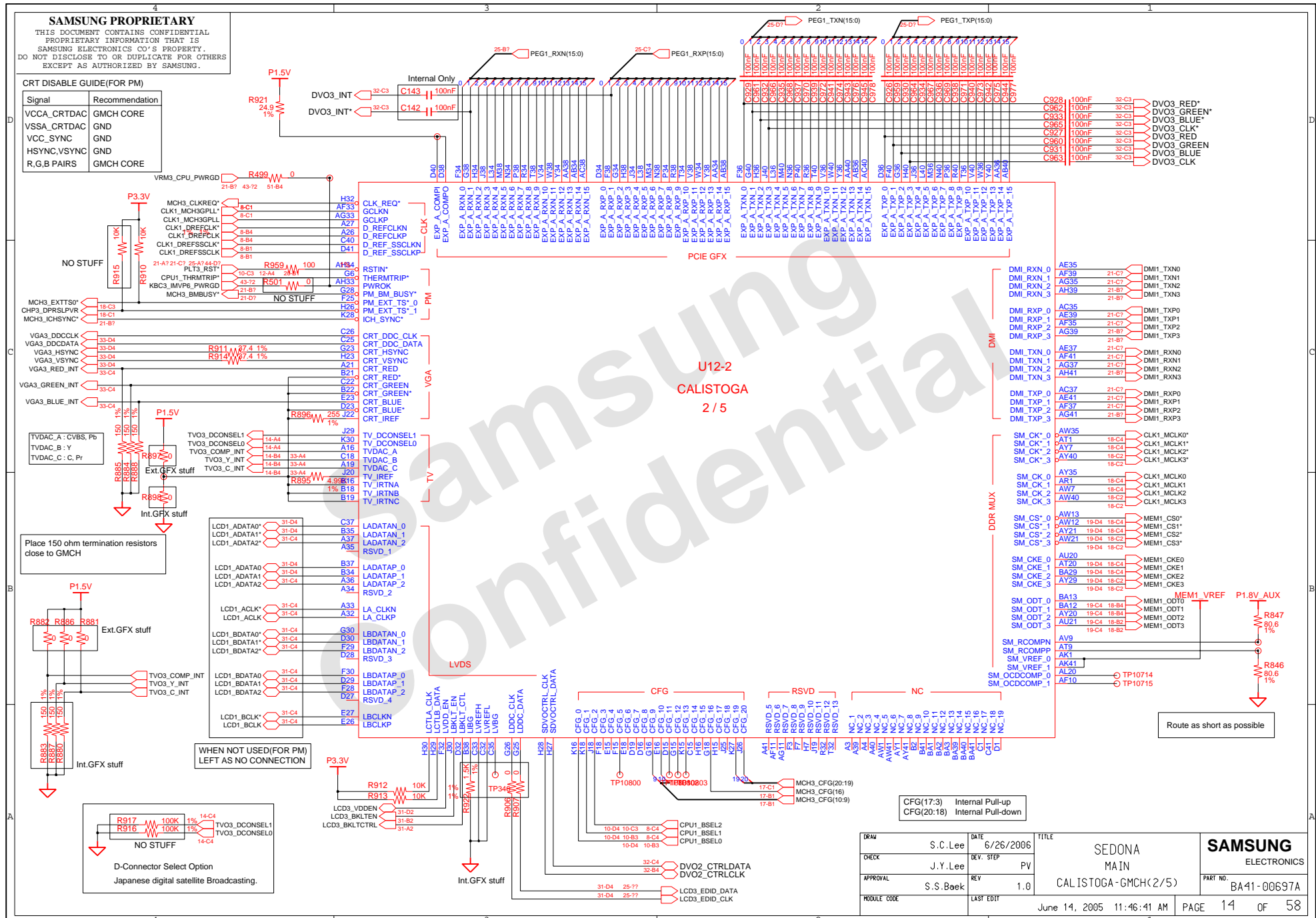
U12-1
 CALISTOGA
 1 / 5

DRAW	S.C.Lee	DATE	6/26/2006	TITLE	SEDONA MAIN CALISTOGA-GMCH(1/5)	SAMSUNG ELECTRONICS PART NO. BA41-00697A
CHECK	J.Y.Lee	DEV. STEP	PV			
APPROVAL	S.S.Boek	REV	1.0			
MODULE CODE		LAST EDIT	June 14, 2005 11:46:41 AM	PAGE	13 OF 58	

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CRT DISABLE GUIDE (FOR PM)

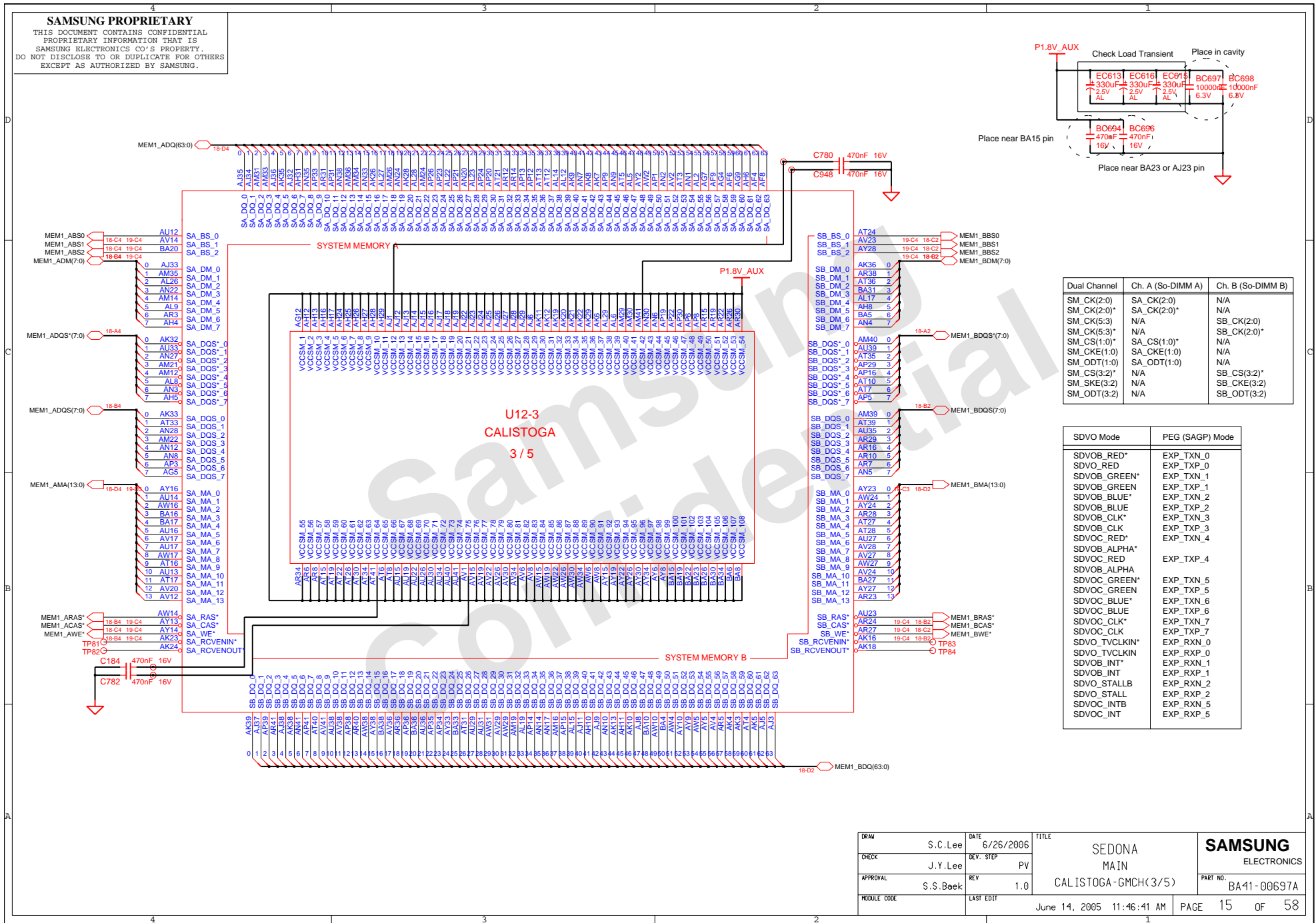
Signal	Recommendation
VCCA_CRTDAC	GMCH CORE
VSSA_CRTDAC	GND
VCC_SYNC	GND
HSYNC.VSYNC	GND
R.G.B PAIRS	GMCH CORE



DRAW	S.C.Lee	DATE	6/26/2006	TITLE	SEDONA MAIN	SAMSUNG ELECTRONICS
CHECK	J.Y.Lee	DEV. STEP	PV	CALISTOGA-GMCH(2/5)		
APPROVAL	S.S.Boek	REV	1.0			PART NO. BA41-00697A
MODULE CODE		LAST EDIT		June 14, 2005 11:46:41 AM		PAGE 14 OF 58

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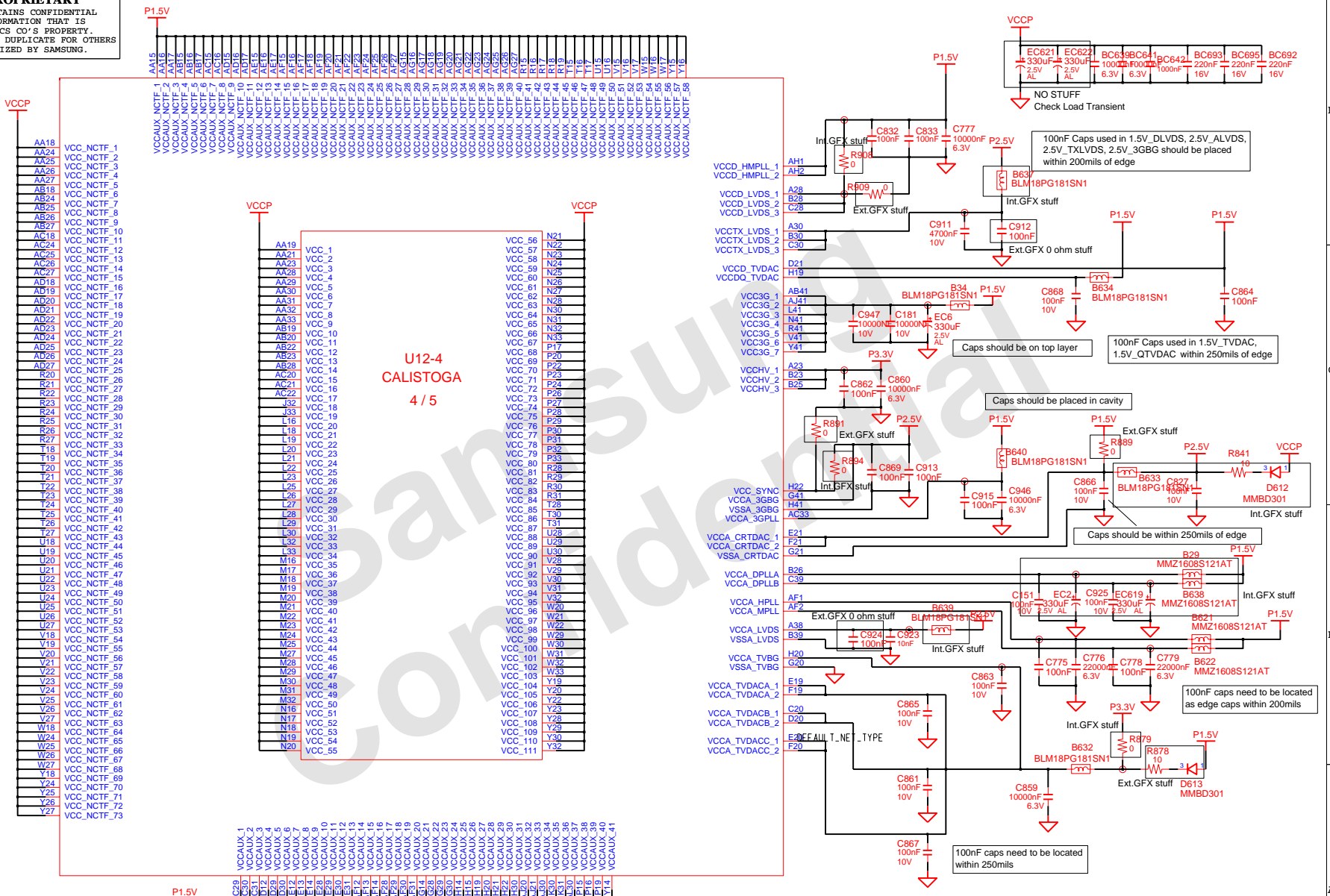


Dual Channel	Ch. A (So-Dimm A)	Ch. B (So-Dimm B)
SM_CK(2:0)	SA_CK(2:0)	N/A
SM_CK(2:0)*	SA_CK(2:0)*	N/A
SM_CK(5:3)	N/A	SB_CK(2:0)
SM_CK(5:3)*	N/A	SB_CK(2:0)*
SM_CS(1:0)	SA_CS(1:0)*	N/A
SM_CKE(1:0)	SA_CKE(1:0)	N/A
SM_ODT(1:0)	SA_ODT(1:0)	N/A
SM_CS(3:2)	N/A	SB_CS(3:2)*
SM_SKE(3:2)	N/A	SB_CKE(3:2)
SM_ODT(3:2)	N/A	SB_ODT(3:2)

SDVO Mode	PEG (SAGP) Mode
SDVOB_RED*	EXP_TXN_0
SDVO_RED	EXP_TXP_0
SDVOB_GREEN*	EXP_TXN_1
SDVOB_GREEN	EXP_TXP_1
SDVOB_BLUE*	EXP_TXN_2
SDVOB_BLUE	EXP_TXP_2
SDVOB_CLK*	EXP_TXN_3
SDVOB_CLK	EXP_TXP_3
SDVOC_RED*	EXP_TXN_4
SDVOC_RED	EXP_TXP_4
SDVOB_ALPHA*	
SDVOC_ALPHA	EXP_TXN_5
SDVOC_GREEN*	EXP_TXN_5
SDVOC_GREEN	EXP_TXP_5
SDVOC_BLUE*	EXP_TXN_6
SDVOC_BLUE	EXP_TXP_6
SDVOC_CLK*	EXP_TXN_7
SDVOC_CLK	EXP_TXP_7
SDVO_TVCLKIN*	EXP_RXN_0
SDVO_TVCLKIN	EXP_RXP_0
SDVOB_INT*	EXP_RXN_1
SDVOB_INT	EXP_RXP_1
SDVO_STALLB	EXP_RXN_2
SDVO_STALL	EXP_RXP_2
SDVOC_INTB	EXP_RXN_5
SDVOC_INT	EXP_RXP_5

DRAW	S.C.Lee	DATE	6/26/2006	TITLE	SEDONA MAIN CALISTOGA-GMCH(3/5)	SAMSUNG ELECTRONICS PART NO. BA41-00697A
CHECK	J.Y.Lee	DEV. STEP	PV			
APPROVAL	S.S.Boek	REV	1.0			
MODULE CODE		LAST EDIT				
			June 14, 2005 11:46:41 AM	PAGE	15 OF 58	

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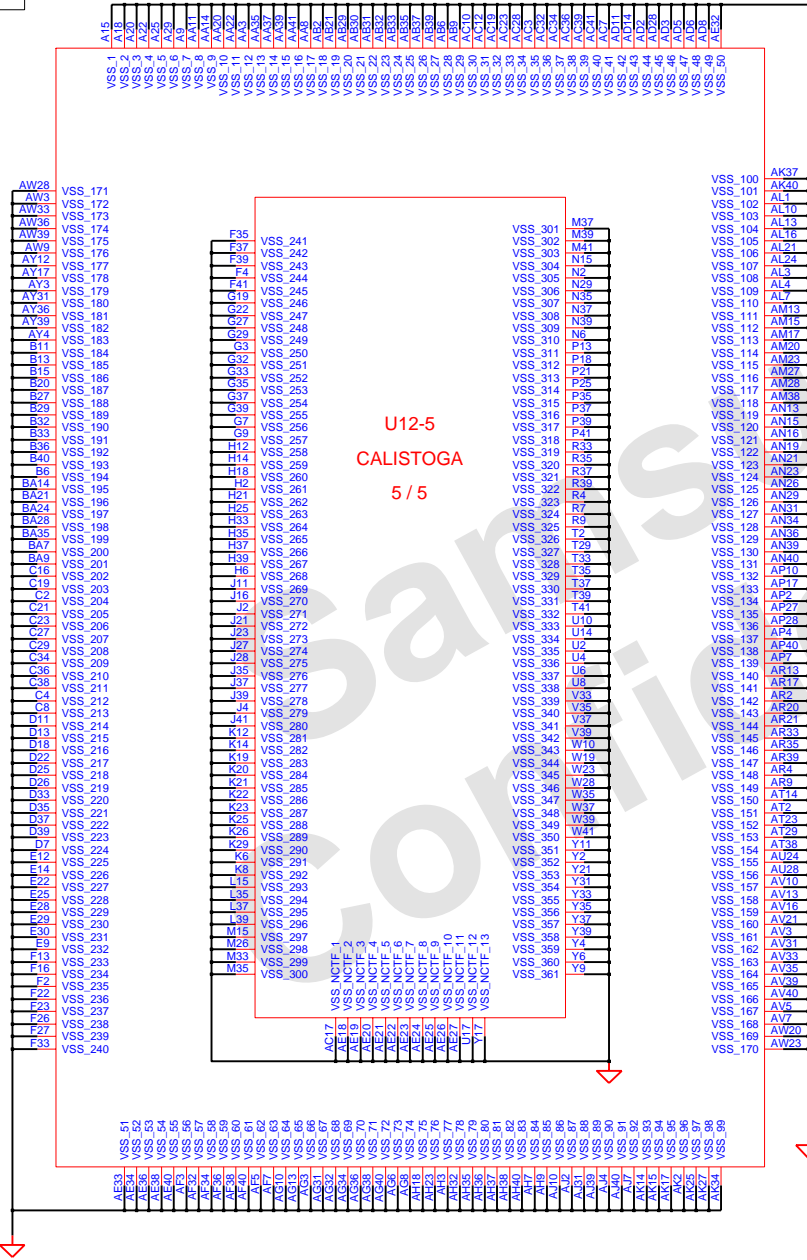
**U12-4
CALISTOGA
4 / 5**

AA18	VCC_NCTF_1	VCC_56	N21
AA24	VCC_NCTF_2	VCC_57	N22
AA25	VCC_NCTF_3	VCC_58	N23
AA26	VCC_NCTF_4	VCC_59	N24
AA27	VCC_NCTF_5	VCC_60	N25
AB18	VCC_NCTF_6	VCC_61	N26
AB24	VCC_NCTF_7	VCC_62	N27
AB25	VCC_NCTF_8	VCC_63	N28
AB26	VCC_NCTF_9	VCC_64	N30
AB27	VCC_NCTF_10	VCC_65	N31
AC18	VCC_NCTF_11	VCC_66	N33
AC24	VCC_NCTF_12	VCC_67	N32
AC25	VCC_NCTF_13	VCC_68	N34
AC26	VCC_NCTF_14	VCC_69	P20
AC27	VCC_NCTF_15	VCC_70	P25
AD18	VCC_NCTF_16	VCC_71	P24
AD19	VCC_NCTF_17	VCC_72	P28
AD21	VCC_NCTF_18	VCC_73	P26
AD22	VCC_NCTF_19	VCC_74	P27
AD23	VCC_NCTF_20	VCC_75	P29
AD24	VCC_NCTF_21	VCC_76	P30
AD25	VCC_NCTF_22	VCC_77	P31
AD26	VCC_NCTF_23	VCC_78	P32
AD27	VCC_NCTF_24	VCC_79	P33
AE20	VCC_NCTF_25	VCC_80	R28
R20	VCC_NCTF_26	VCC_81	R29
R21	VCC_NCTF_27	VCC_82	R29
R22	VCC_NCTF_28	VCC_83	VCC_27
R23	VCC_NCTF_29	VCC_84	VCC_28
R24	VCC_NCTF_30	VCC_85	VCC_29
R25	VCC_NCTF_31	VCC_86	VCC_30
R26	VCC_NCTF_32	VCC_87	VCC_31
R27	VCC_NCTF_33	VCC_88	VCC_32
T16	VCC_NCTF_34	VCC_89	VCC_33
T18	VCC_NCTF_35	VCC_90	VCC_34
T19	VCC_NCTF_36	VCC_91	VCC_35
T20	VCC_NCTF_37	VCC_92	VCC_36
T21	VCC_NCTF_38	VCC_93	VCC_37
T22	VCC_NCTF_39	VCC_94	VCC_38
T23	VCC_NCTF_40	VCC_95	VCC_39
T24	VCC_NCTF_41	VCC_96	VCC_40
T25	VCC_NCTF_42	VCC_97	VCC_41
T26	VCC_NCTF_43	VCC_98	VCC_42
T27	VCC_NCTF_44	VCC_99	VCC_43
U16	VCC_NCTF_45	VCC_100	VCC_44
U19	VCC_NCTF_46	VCC_101	VCC_45
U20	VCC_NCTF_47	VCC_102	VCC_46
U21	VCC_NCTF_48	VCC_103	VCC_47
U22	VCC_NCTF_49	VCC_104	VCC_48
U23	VCC_NCTF_50	VCC_105	VCC_49
U24	VCC_NCTF_51	VCC_106	VCC_50
U25	VCC_NCTF_52	VCC_107	VCC_51
U26	VCC_NCTF_53	VCC_108	VCC_52
V18	VCC_NCTF_54	VCC_109	VCC_53
V19	VCC_NCTF_55	VCC_110	VCC_54
V20	VCC_NCTF_56	VCC_111	VCC_55
V21	VCC_NCTF_57		
V22	VCC_NCTF_58		
V23	VCC_NCTF_59		
V24	VCC_NCTF_60		
V25	VCC_NCTF_61		
V26	VCC_NCTF_62		
V27	VCC_NCTF_63		
W18	VCC_NCTF_64		
W24	VCC_NCTF_65		
W25	VCC_NCTF_66		
W26	VCC_NCTF_67		
W27	VCC_NCTF_68		
Y18	VCC_NCTF_69		
Y24	VCC_NCTF_70		
Y25	VCC_NCTF_71		
Y26	VCC_NCTF_72		
Y27	VCC_NCTF_73		

DRAW	S.C.Lee	DATE	6/26/2006	TITLE	SEDONA	SAMSUNG ELECTRONICS
CHECK	J.Y.Lee	DEV. STEP	PV	MAIN		
APPROVAL	S.S.Boek	REV	1.0	CALISTOGA-GMCH(4/5)	PART NO.	BA41-00697A
MODULE CODE		LAST EDIT		June 14, 2005 11:46:41 AM	PAGE	16 OF 58

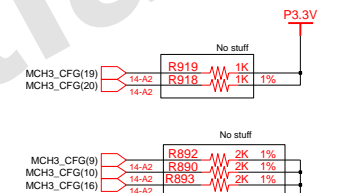
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**** Note *POCAFEB-10 Only (Remove in MP Model)**

CFG#	Current Setting (def.: default Option)	Low	High
CFG(5)	DMIX2	Reserved	DMIX4 (def.)
CFG(6)	Reserved	DT/transportable	DDR-II (def.)
CFG(7)	Reserved	PEG Reversal	Mobile CPU (def.)
CFG(9)	Reserved	Callistoga	Normal
CFG(11)	Reserved	PSB 4X CLK Enable	Normal
CFG(16)	Dynamic ODT	Dynamic ODT	Dynamic ODT
	Disabled	Enabled (def.)	Enabled (def.)
CFG(18)	VCC 1.05V (def.)	VCC 1.5V	VCC 1.5V
CFG(19)	DMI Lane Normal	DMI Lane Reversal	DMI Lane Reversal
CFG(20)	SDVO or PCIE X1 Only(def.)	SDVO and PCIE X1	SDVO and PCIE X1 Simultaneously

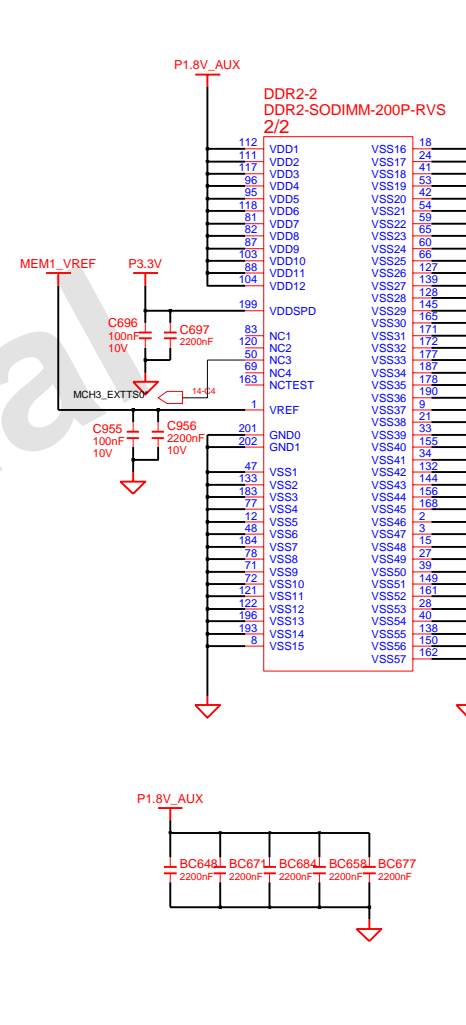
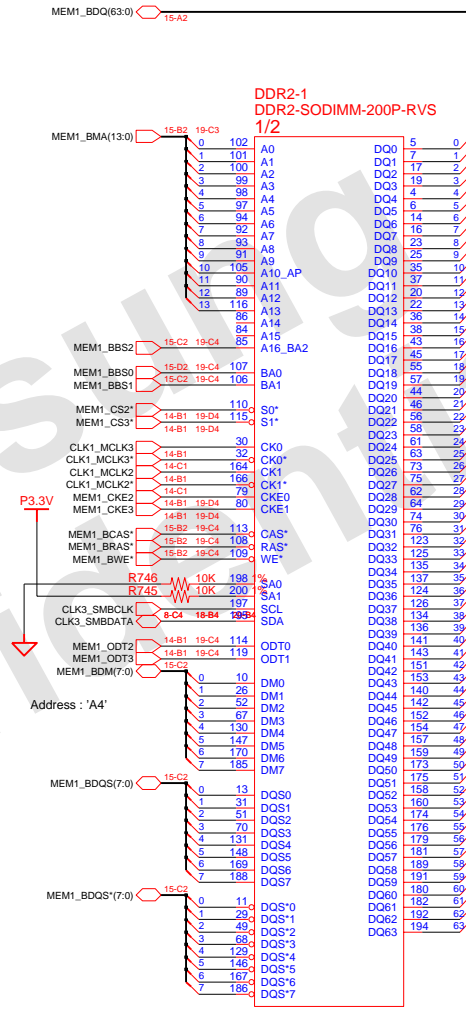
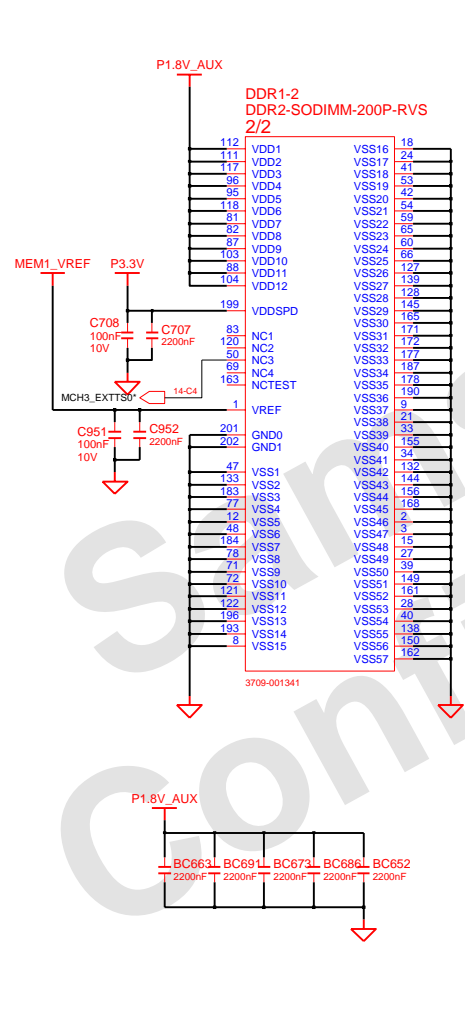
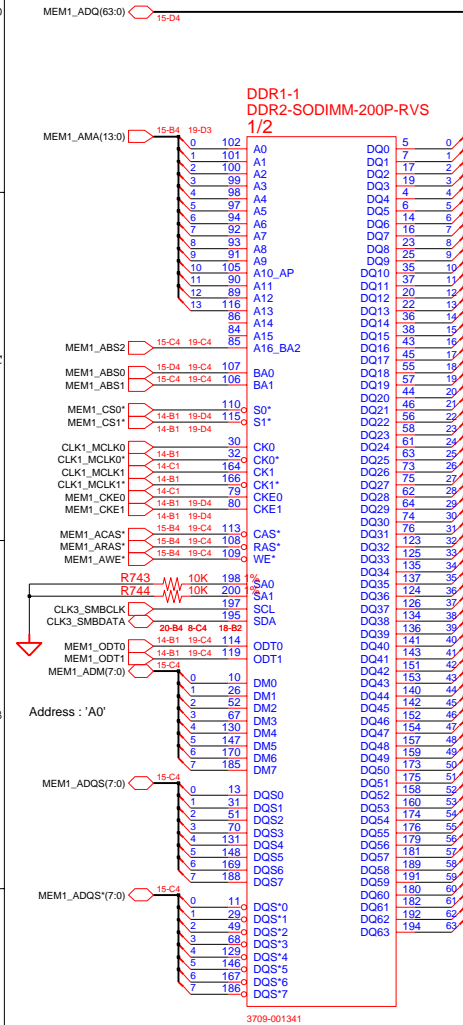


**** Note**
CFG(17:3) Internal Pull-up
CFG(20:18) Internal Pull-down

DRAW	S.C.Lee	DATE	6/26/2006	TITLE	SEDONA MAIN	SAMSUNG ELECTRONICS PART NO. BA41-00697A
CHECK	J.Y.Lee	DEV. STEP	PV	CALISTOGA-GMCH(5/5)		
APPROVAL	S.S.Boek	REV	1.0	June 14, 2005 11:46:41 AM		PAGE 17 OF 58
MODULE CODE		LAST EDIT				

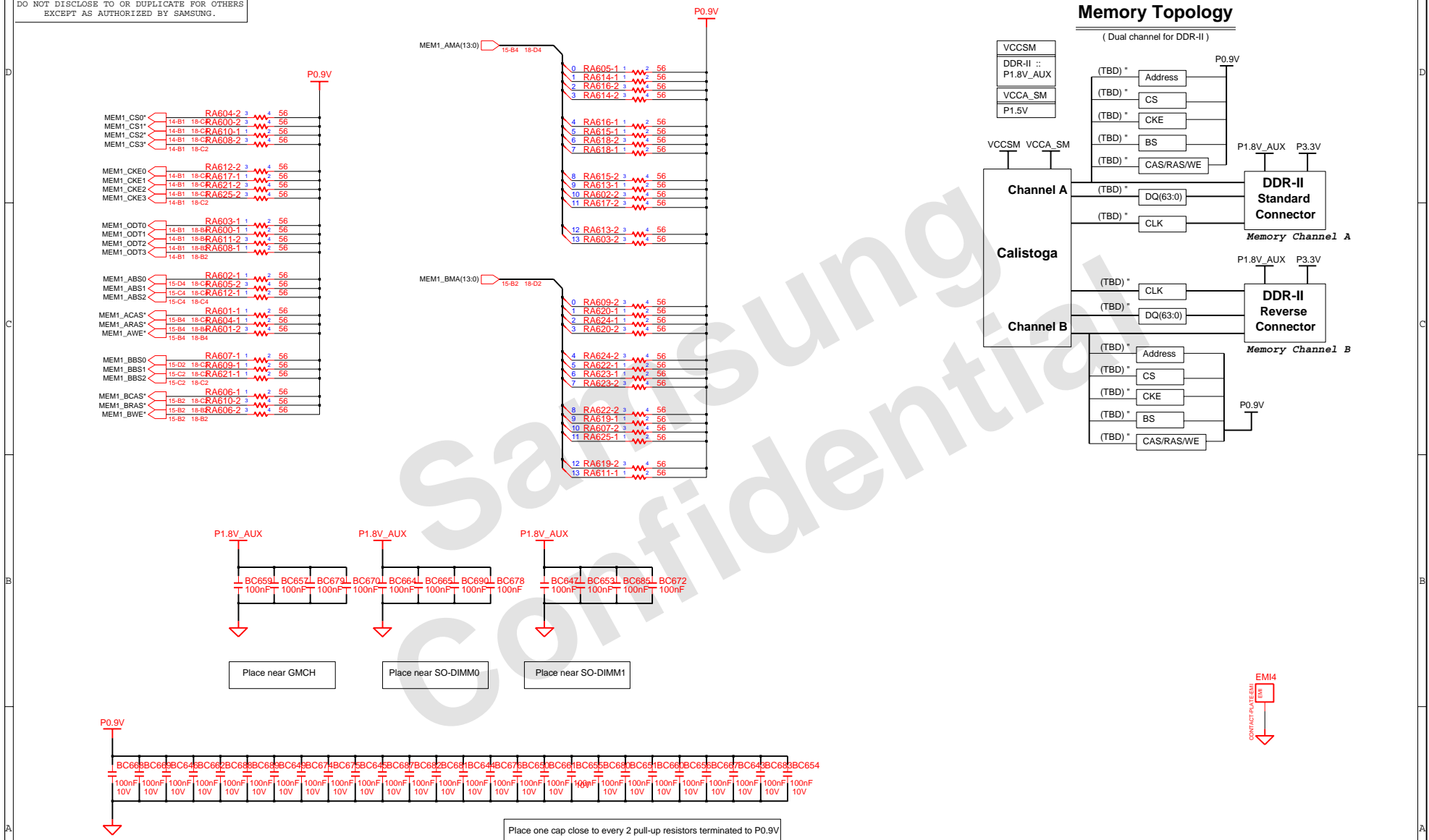
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DRAW	S.C.Lee	DATE	6/26/2006	TITLE	SEDONA	SAMSUNG ELECTRONICS
CHECK	J.Y.Lee	DEV. STEP	PV	MAIN		
APPROVAL	S.S.Boek	REV	1.0	DDR2 - SODIMM		PART NO. BA41-00697A
MODULE CODE		LAST EDIT	June 14, 2005 11:46:41 AM	PAGE	18	OF 58

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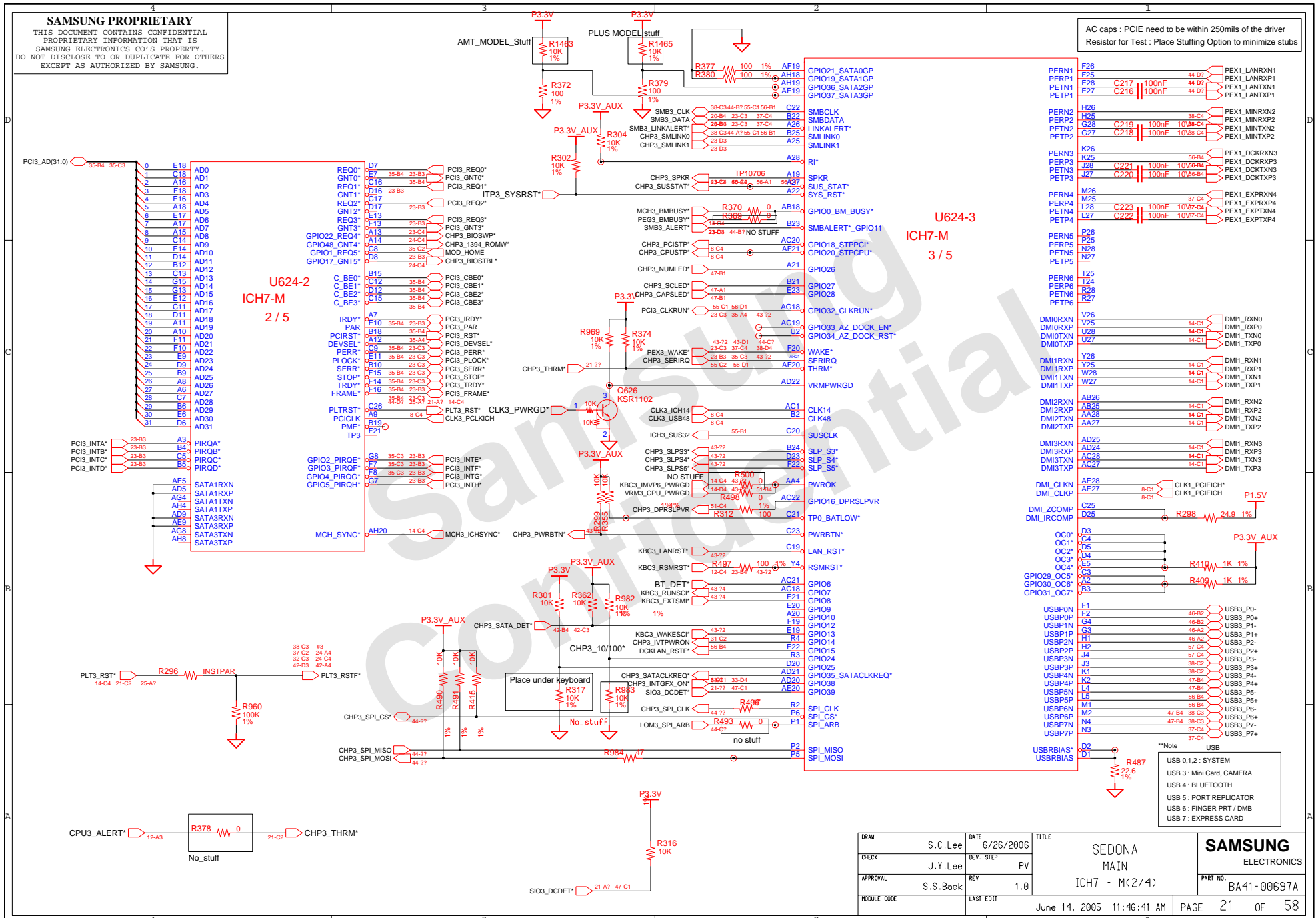


DRAW	S.C.Lee	DATE	6/26/2006	TITLE	SEDONA	SAMSUNG ELECTRONICS
CHECK	J.Y.Lee	DEV. STEP	PV	MAIN	PART NO.	
APPROVAL	S.S.Boek	REV	1.0	DDR2 - TERMINATION	BA41-00697A	
MODULE CODE		LAST EDIT	June 14, 2005 11:46:41 AM	PAGE	19 OF 58	

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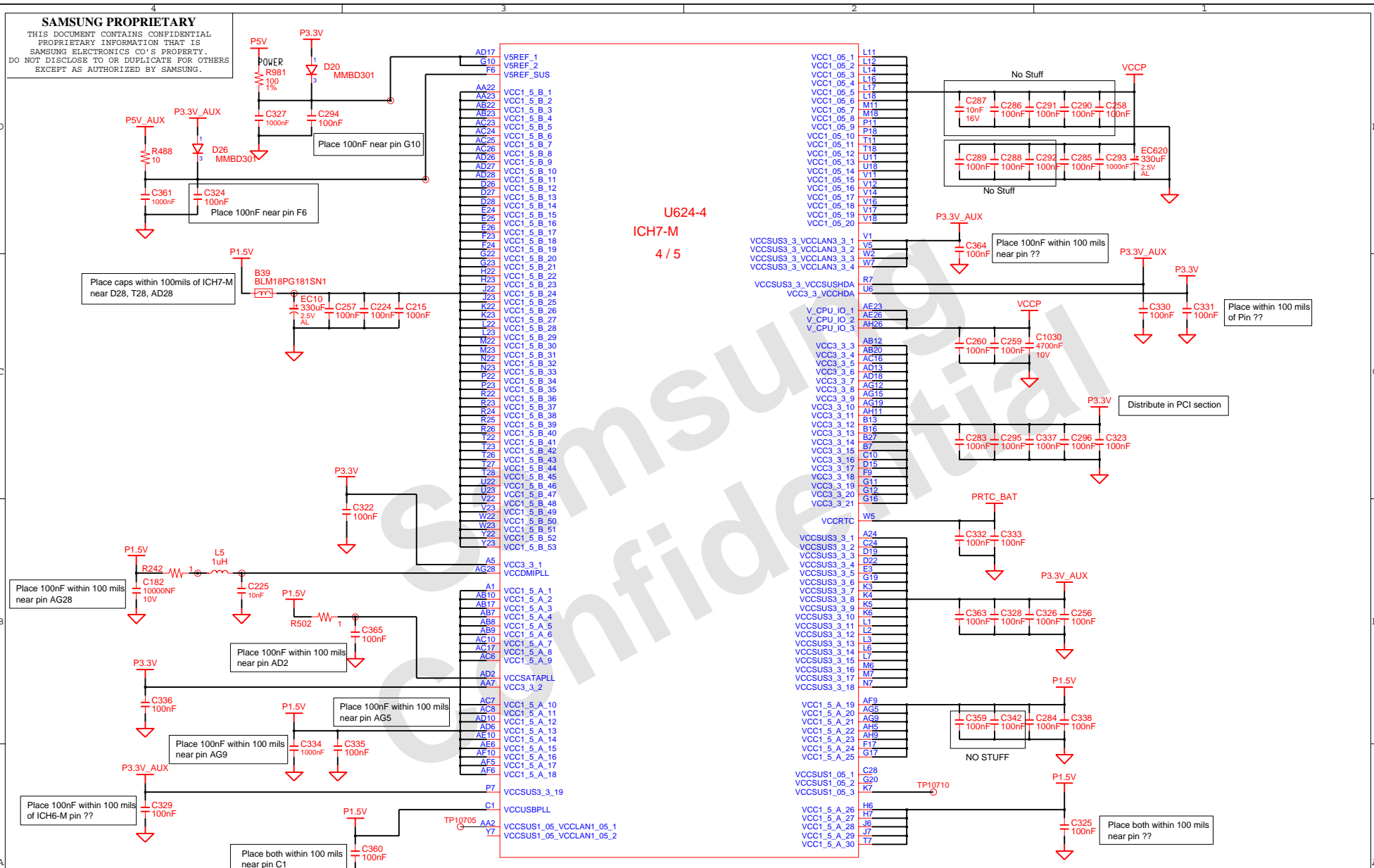
AC caps : PCIe need to be within 250mils of the driver Resistor for Test : Place Stuffing Option to minimize stubs



PERN1	F26			PEX1_LANRXN1	
PERP1	F25			PEX1_LANRXN1	
PETN1	E28	C217	100nF	44-D7	PEX1_LANTXN1
PETP1	E27	C216	1000F	44-D7	PEX1_LANTXP1
PERN2	H26			PEX1_MINRXN2	
PERP2	H25			PEX1_MINRXP2	
PETN2	G28	C219	100nF	10V6-C4	PEX1_MINTXN2
PETP2	G27	C218	100nF	10V6-C4	PEX1_MINTXP2
PERN3	K26			PEX1_DCKRXN3	
PERP3	K25			PEX1_DCKRXN3	
PETN3	J28	C221	100nF	10V6-B4	PEX1_DCKTXN3
PETP3	J27	C220	100nF	10V6-B4	PEX1_DCKTXP3
PERN4	M26			PEX1_EXPRXN4	
PERP4	L28	C223	100nF	10V7-C4	PEX1_EXPRXP4
PETN4	L27	C222	100nF	10V7-C4	PEX1_EXPTXN4
PETP4	L27	C222	100nF	10V7-C4	PEX1_EXPTXP4
PERN5	P26				
PERP5	P25				
PETN5	N28				
PETP5	N27				
PERN6	T25				
PERP6	T24				
PETN6	R28				
PETP6	R27				
DMIORXN	V26			DM1_RXN0	
DMIORXP	V25			DM1_RXP0	
DMIOTXN	U28			DM1_TXN0	
DMIOTXP	U27			DM1_TXP0	
DM1RXN	Y26			DM1_RXN1	
DM1RXN1	Y25			DM1_RXN1	
DM1TXN	W28			DM1_TXN1	
DM1TXN1	W27			DM1_TXP1	
DM1RXN2	AB26			DM1_RXN2	
DM1RXN2	AB25			DM1_RXP2	
DM1TXN2	AA28			DM1_TXN2	
DM1TXN2	AA27			DM1_TXP2	
DM1RXN3	AD25			DM1_RXN3	
DM1RXN3	AD24			DM1_RXP3	
DM1TXN3	AC28			DM1_TXN3	
DM1TXN3	AC27			DM1_TXP3	
DM1CLKN	AE28			CLK1_POEICH*	
DM1CLKP	AE27			CLK1_POEICH*	
DM1ZCOMP	C25				
DM1IRCOMP	D25				
OC0*	O3				
OC1*	O4				
OC2*	O5				
OC3*	O6				
OC4*	O7				
GPIO29_OC5*	A2				
GPIO30_OC6*	B3				
GPIO31_OC7*	B3				
USBP0N	F1			USB3_P0-	
USBP0P	F2			USB3_P0+	
USBP1N	G4			USB3_P1-	
USBP1P	G3			USB3_P1+	
USBP2N	H1			USB3_P2-	
USBP2P	H2			USB3_P2+	
USBP3N	J4			USB3_P3-	
USBP3P	J3			USB3_P3+	
USBP4N	K1			USB3_P4-	
USBP4P	K2			USB3_P4+	
USBP5N	L4			USB3_P5-	
USBP5P	L5			USB3_P5+	
USBP6N	M1			USB3_P6-	
USBP6P	M2			USB3_P6+	
USBP7N	N4			USB3_P7-	
USBP7P	N5			USB3_P7+	
USBRBIAS*	D2			USB	
USBRBIAS	D1			USB	

**Note USB
 USB 0,1,2 : SYSTEM
 USB 3 : Mini Card, CAMERA
 USB 4 : BLUETOOTH
 USB 5 : PORT REPLICATOR
 USB 6 : FINGER PRT / DMB
 USB 7 : EXPRESS CARD

DRAW	S.C.Lee	DATE	6/26/2006	TITLE	SEDONA MAIN	SAMSUNG ELECTRONICS
CHECK	J.Y.Lee	DEV. STEP	PV		ICH7 - M(2/4)	
APPROVAL	S.S.Boek	REV	1.0			PART NO. BA41-00697A
MODULE CODE		LAST EDIT	June 14, 2005 11:46:41 AM			PAGE 21 OF 58



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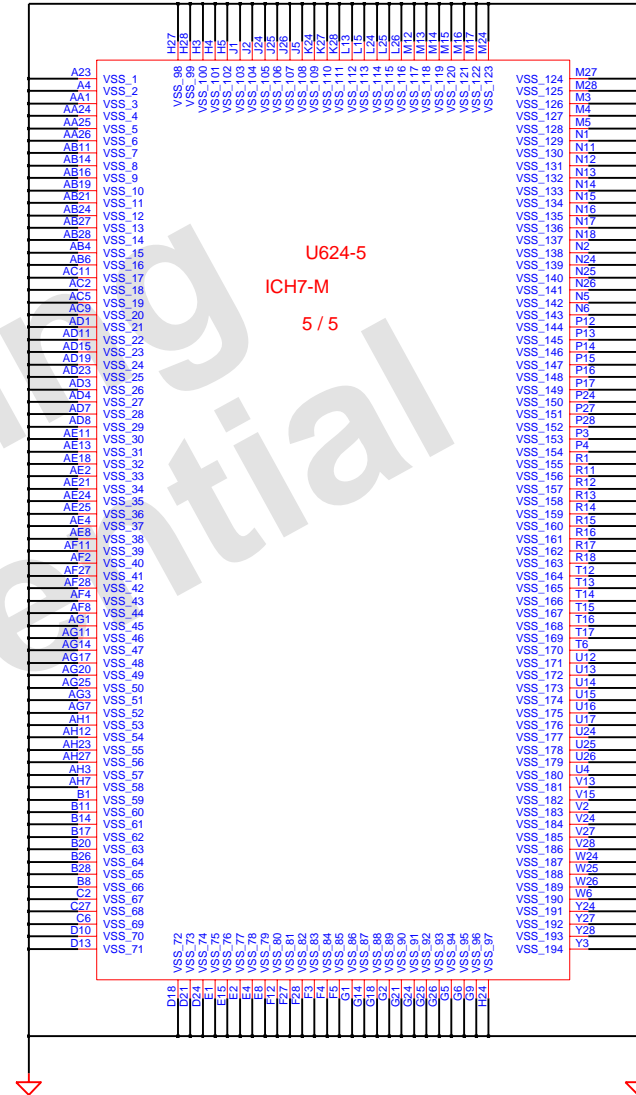
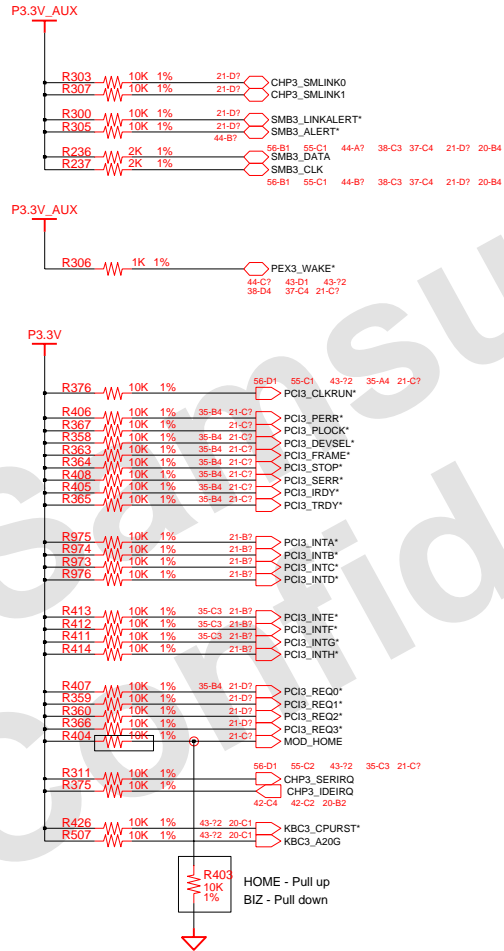
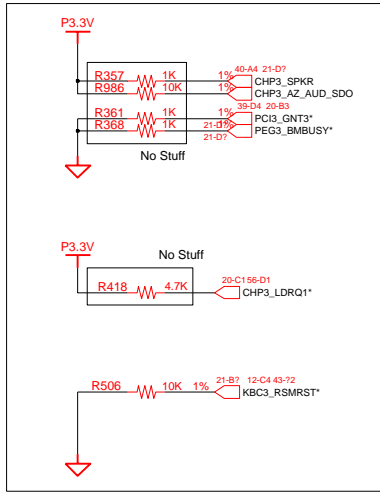
U624-4
 ICH7-M
 4 / 5

DRAW	S.C.Lee	DATE	6/26/2006	TITLE	SEDONA	SAMSUNG ELECTRONICS
CHECK	J.Y.Lee	DEV. STEP	PV	MAIN		
APPROVAL	S.S.Boek	REV	1.0	ICH7 - M(3/4)		PART NO. BA41-00697A
MODULE CODE		LAST EDIT	June 14, 2005 11:46:41 AM	PAGE	22	OF 58

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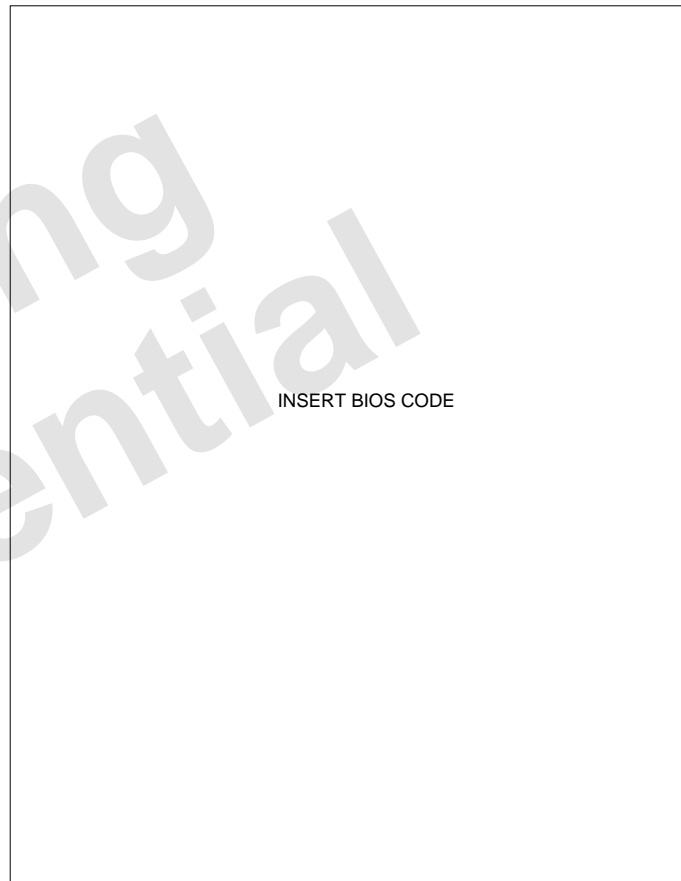
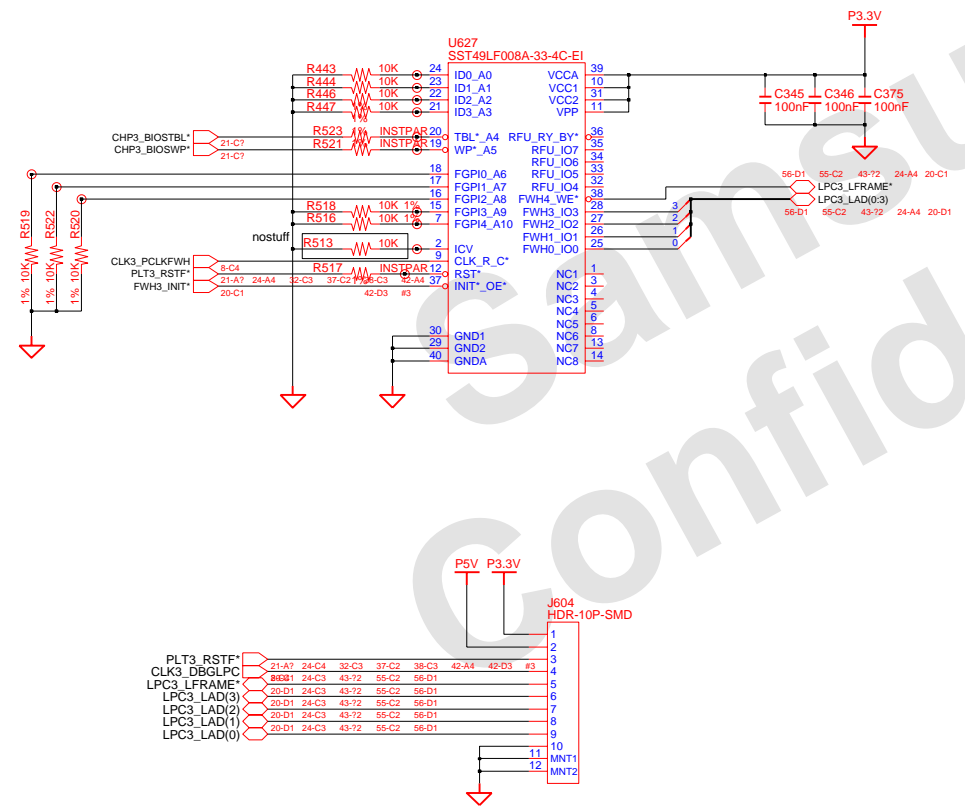
ICH7-m Options

Option	Function	Default
CHP3_SPKR	No Reboot	No Stuff
CHP3_GNT3	A16 swap override	No Stuff
AC97_SDOUT	Safe Mode	TBD
CHP3_GNT(5:4)	Boot BIOS Option	



DRAW	S.C.Lee	DATE	6/26/2006	TITLE	SEDONA	SAMSUNG ELECTRONICS
CHECK	J.Y.Lee	DEV. STEP	PV	MAIN		
APPROVAL	S.S.Boek	REV	1.0	ICH7 - M(4/4)		PART NO. BA41-00697A
MODULE CODE		LAST EDIT	June 14, 2005 11:46:41 AM	PAGE	23	OF 58

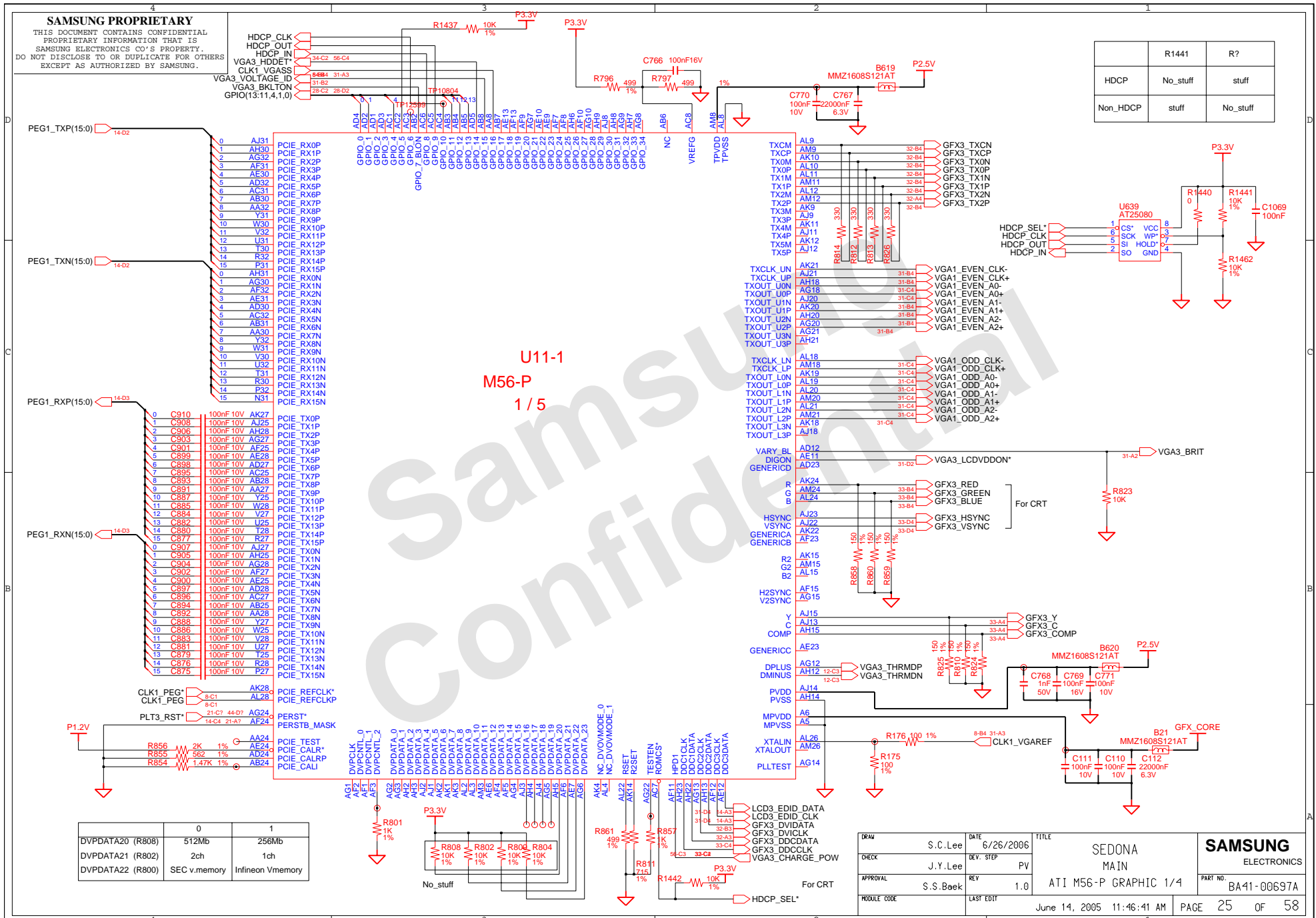
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DRAW	S.C.Lee	DATE	6/26/2006	TITLE	SEDONA MAIN FIRMWARE HUB	SAMSUNG ELECTRONICS PART NO. BA41-00697A
CHECK	J.Y.Lee	DEV. STEP	PV			
APPROVAL	S.S.Boek	REV	1.0			
MODULE CODE		LAST EDIT	June 14, 2005 11:46:41 AM	PAGE	24 OF 58	

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	R1441	R?
HDCP	No_stuff	stuff
Non_HDCP	stuff	No_stuff

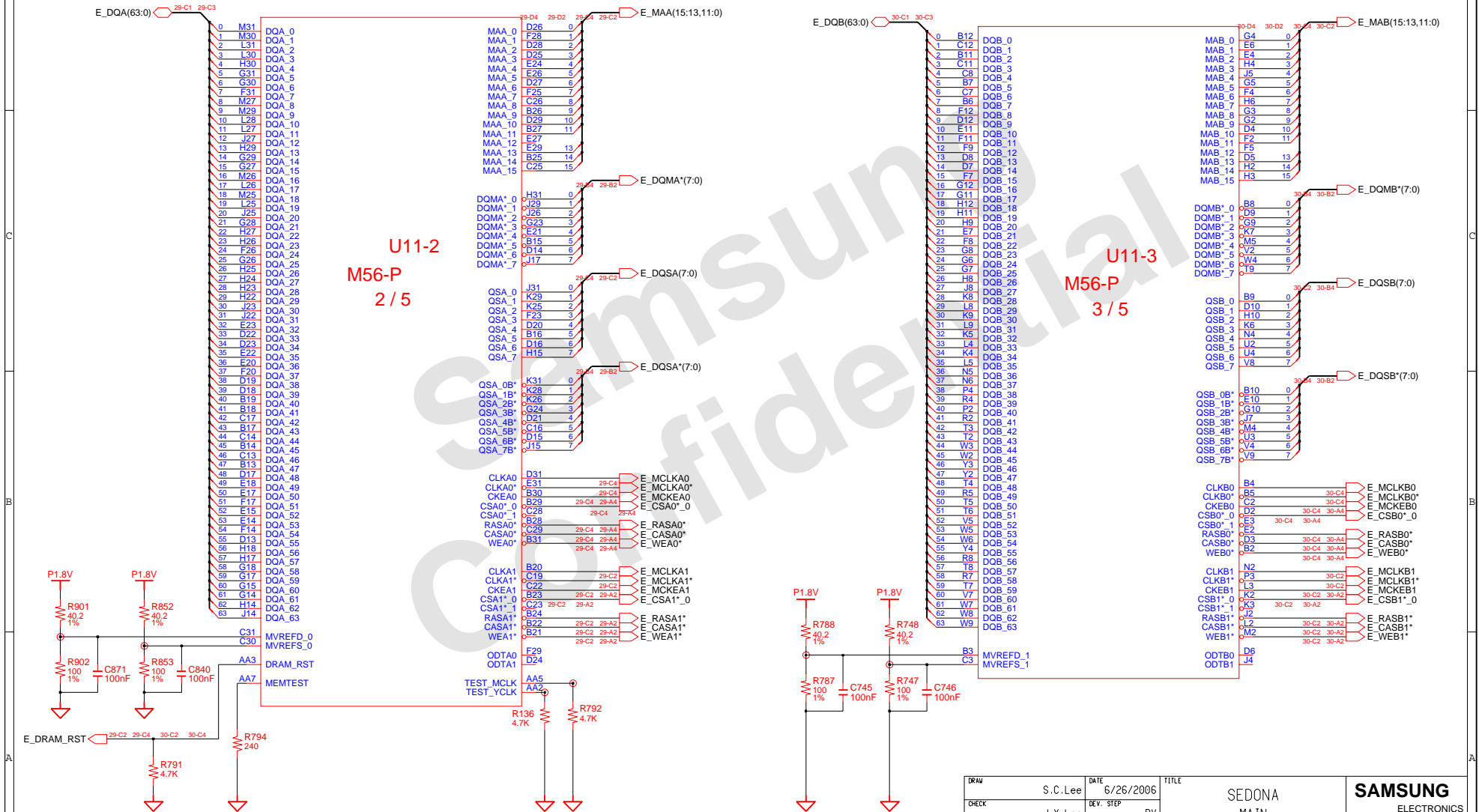
	0	1
DVPPDATA20 (R808)	512Mb	256Mb
DVPPDATA21 (R802)	2ch	1ch
DVPPDATA22 (R800)	SEC v.memory	Infinion Vmemory

DRAW	S.C.Lee	DATE	6/26/2006	TITLE	SEDONA MAIN	SAMSUNG ELECTRONICS PART NO. BA41-00697A
CHECK	J.Y.Lee	DEV. STEP	PV			
APPROVAL	S.S.Boek	REV	1.0			
MODULE CODE		LAST EDIT	June 14, 2005 11:46:41 AM			
					PAGE 25 OF 58	

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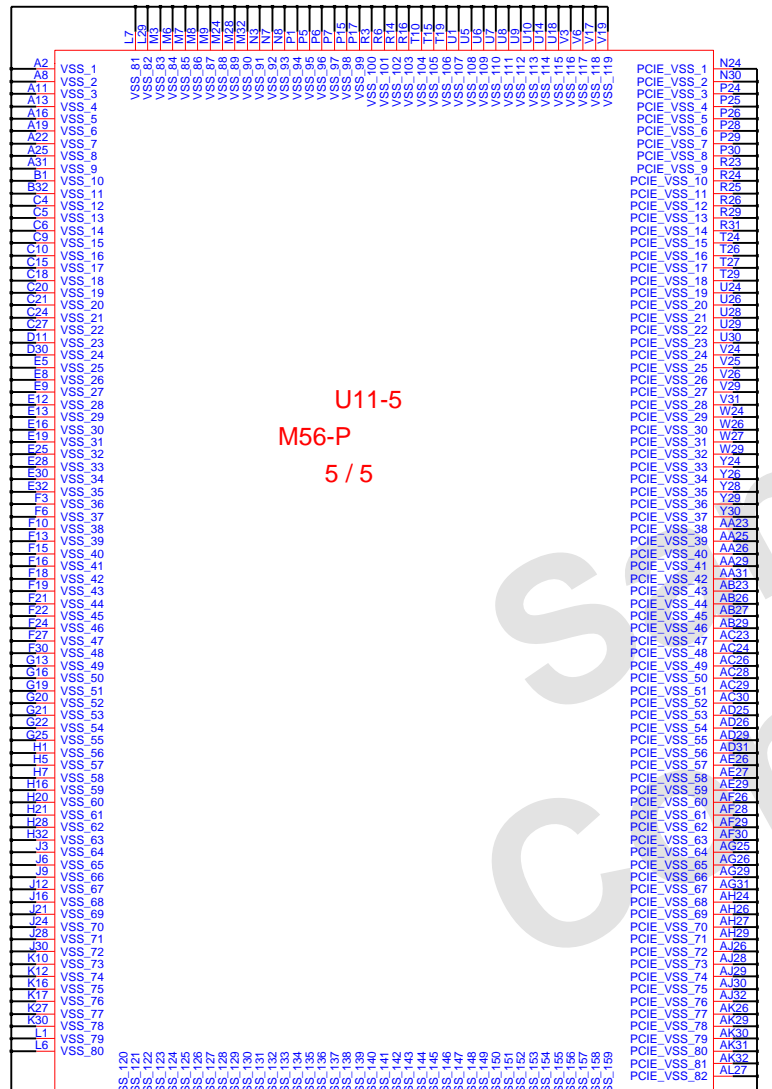
**Graphic Memory I/F
 (Using FBA Channel)**

**Graphic Memory I/F
 (Using FBC Channel)**



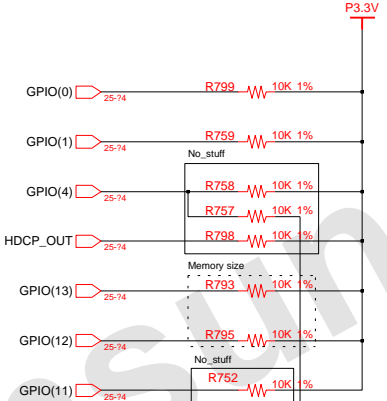
DRAW	S.C.Lee	DATE	6/26/2006	TITLE	SEDONA	SAMSUNG ELECTRONICS
CHECK	J.Y.Lee	DEV. STEP	PV	MAIN		
APPROVAL	S.S.Boek	REV	1.0	ATI M56-P GRAHIC 2/4	PART NO.	BA41-00697A
MODULE CODE		LAST EDIT	June 14, 2005 11:46:41 AM	PAGE	26	OF 58

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U11-5
 M56-P
 5 / 5

Need to option

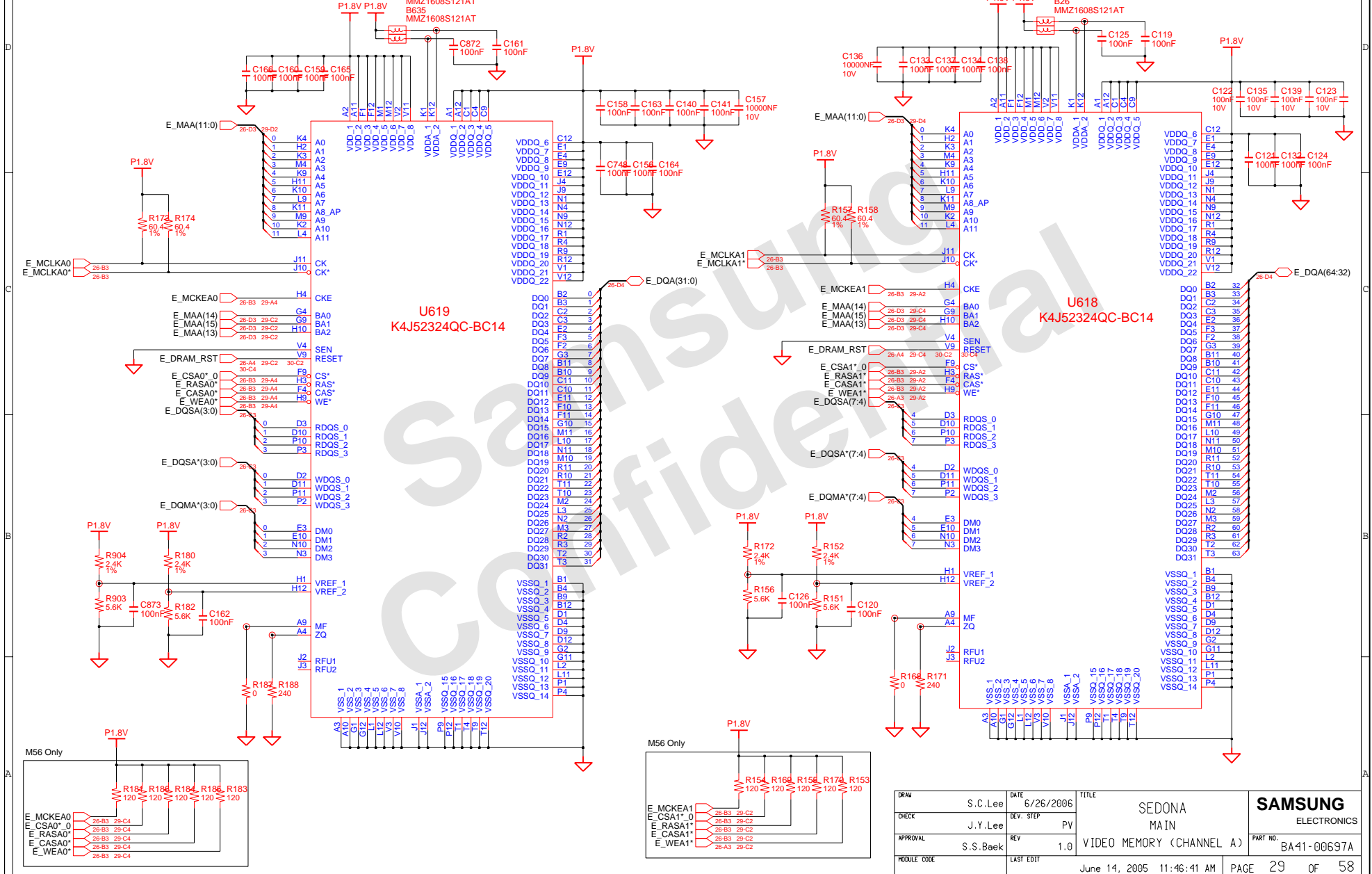


STRAP	PIN	DESCRIPTION	DEFAULT
TX_PWRS_ENB	GPIO[0]	Transmitter Power Saving Enable 0: 50% Tx output swing 1: Full Tx output swing	0 (internal pull-down)
TX_DEEMPH_EN	GPIO[1]	Transmitter De-emphasis Enable 0: Tx De-emphasis disabled 1: Tx de-emphasis enabled	0 (internal pull-down)
DEBUG_ACCESS	GPIO[4]	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible.	0 (internal pull-down)
ROMIDCFG[3:0]	GPIO[9,13:11]	If no ROM attached, controls chip ID's. If ROM attached, identifies ROM type. GPIO[9, 13, 12, 11] 000x - No ROM, MEM_AP_SIZE = 0 001x - No ROM, MEM_AP_SIZE = 01 010x - No ROM, MEM_AP_SIZE = 10 011x - No ROM, MEM_AP_SIZE = 11 1000 - Reserved (formerly Parallel ROM) 1001 - 1M Serial AT25F1024 ROM (Atmel) 1010 - 1M Serial AT45DB011 ROM (Atmel) 1011 - 1M Serial M25P10 ROM (ST) 1100 - 512K Serial M25P05 ROM (ST) 1101 - 1M Serial SST45LF010 ROM (SST) 1102 - 1M Serial W45B512 ROM (WinBond) 1103 - 512K Serial W45B012 ROM (WinBond) 1110 - 1M Serial SST25VF010 ROM (SST) 1111 - 512K Serial SST25VF512 ROM (SST) 1111 - 1M NX25F011B ROM (NextFlash)	GPIO[9,13,12,11] 0000 (internal pull-down)
VIP_DEVICE	VSYN	Indicate whether or not a VIP host port device is present. 0 - Slave VIP host port devices present 1 - No slave VIP host port devices present * Note : The readback of this strap is the inverted with respect to the value on the pin.	0 (internal pull-down)
PWR_CFG[0:2]	PWR_CFG[0:2]	Indicate how the various power regulators should be configured. Weak pull-up (e.g 100kohms) need to be provided on the motherboard for all three signals. D2, D1, D0 = 001 = M56 nominal voltages Only applicable to M56-CSP!	
Reserved	PCIE_TEST	ATI internal use only. Other logic must not affect this signal during RESET.	0
Reserved	HSYN	ATI internal use only. Other logic must not affect this signal during RESET.	0
Reserved	H2SYN V2SYN GENERIC	ATI internal use only. Other logic must not affect this signal during RESET.	0
Reserved	GPIO [3:2]	ATI internal use only. Other logic must not affect this signal during RESET.	00
Reserved	GPIO [6:5]	ATI internal use only. Other logic must not affect this signal during RESET.	00
Reserved	GPIO [8]	ATI internal use only. Other logic must not affect this signal during RESET.	0

DRAW	S.C.Lee	DATE	6/26/2006	TITLE	SEDONA MAIN	SAMSUNG ELECTRONICS
CHECK	J.Y.Lee	DEV. STEP	PV	ATI M56-P GRAPHIC 4/4		
APPROVAL	S.S.Boek	REV	1.0	June 14, 2005 11:46:41 AM		PART NO. BA41-00697A
MODULE CODE		LAST EDIT		PAGE 28 OF 58		

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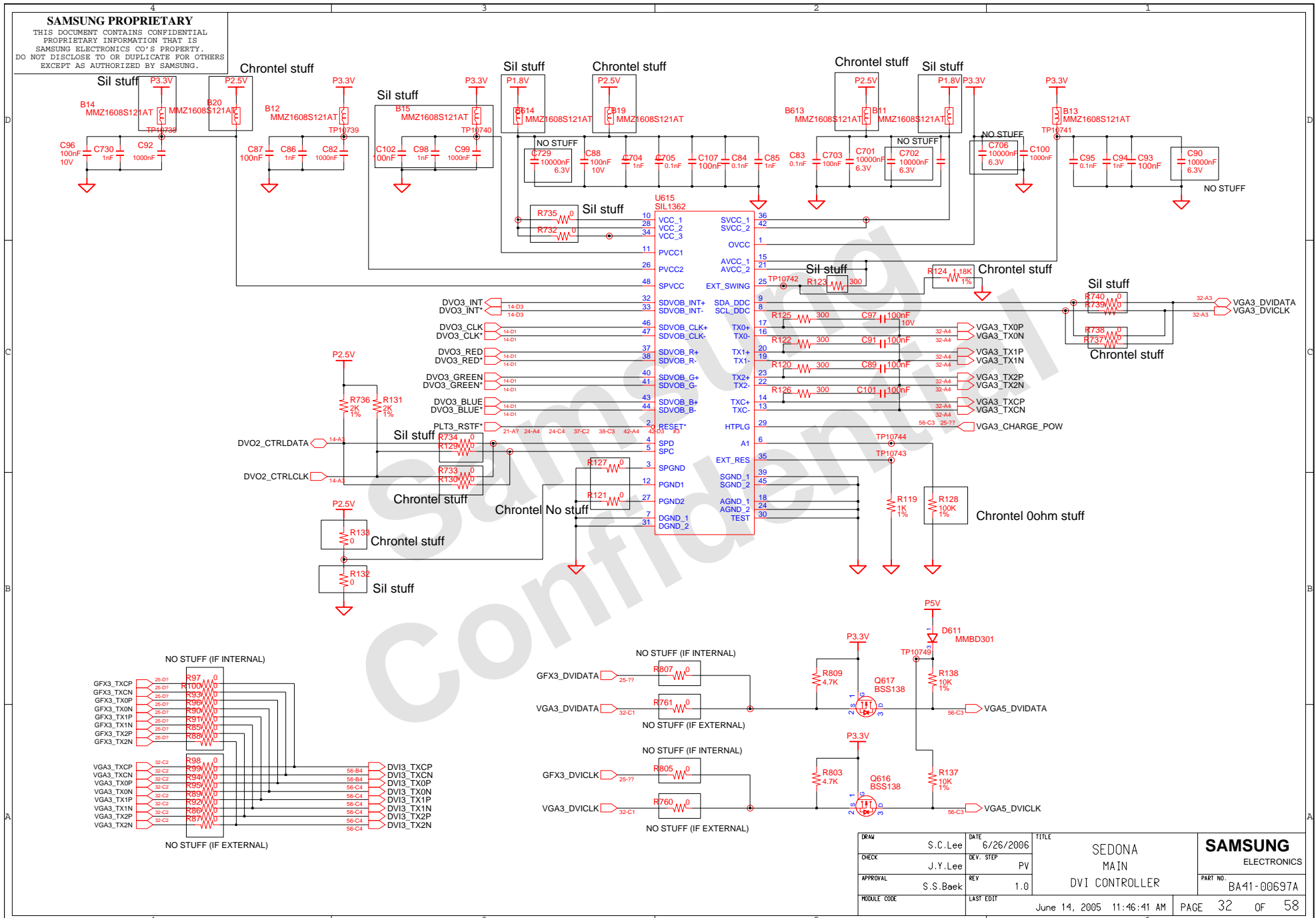
A-channel



DRAW	S.C.Lee	DATE	6/26/2006	TITLE	SEDONA	SAMSUNG ELECTRONICS
CHECK	J.Y.Lee	DEV. STEP	PV	MAIN		
APPROVAL	S.S.Boek	REV	1.0	VIDEO MEMORY (CHANNEL A)	PART NO.	BA41-00697A
MODULE CODE		LAST EDIT	June 14, 2005 11:46:41 AM	PAGE	29	OF 58

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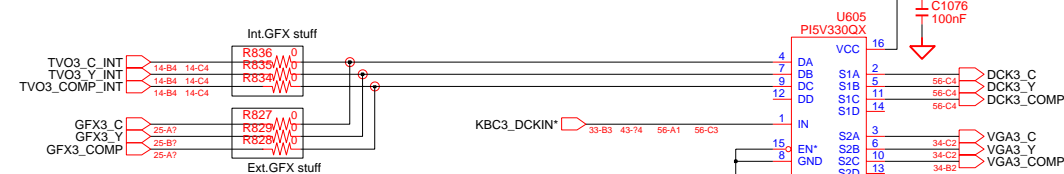
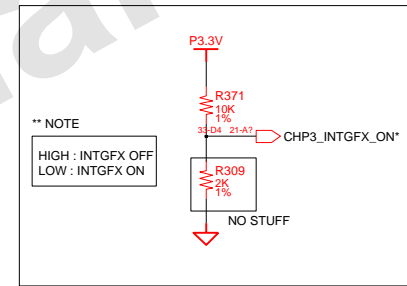
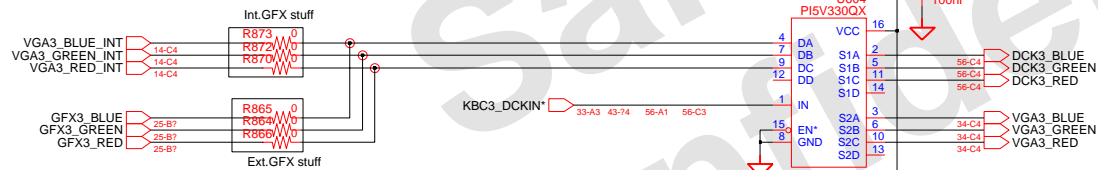
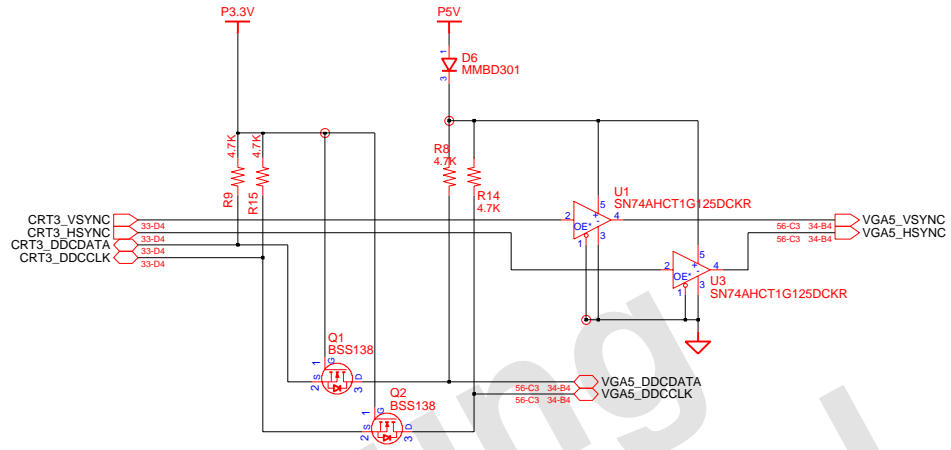
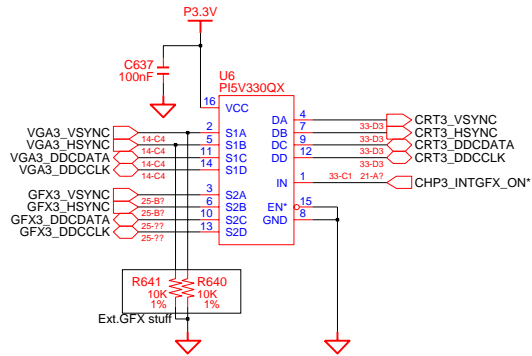
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DRAW	S.C.Lee	DATE	6/26/2006	TITLE	SEDONA MAIN DVI CONTROLLER	SAMSUNG ELECTRONICS PART NO. BA41-00697A
CHECK	J.Y.Lee	DEV. STEP	PV	REV	1.0	
APPROVAL	S.S.Boek	LAST EDIT	June 14, 2005 11:46:41 AM	PAGE	32	OF 58

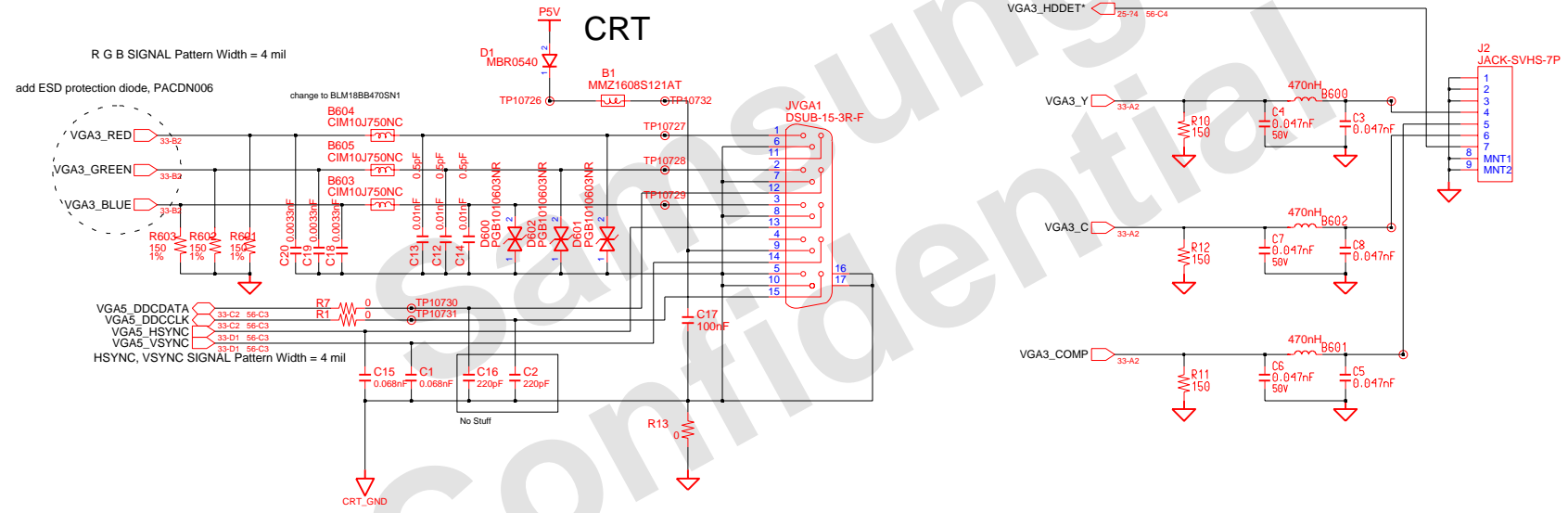
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DRAW	S.C.Lee	DATE	6/26/2006	TITLE	SEDONA MAIN CRT PORT	SAMSUNG ELECTRONICS
CHECK	J.Y.Lee	DEV. STEP	PV			
APPROVAL	S.S.Boek	REV	1.0			PART NO. BA41-00697A
MODULE CODE		LAST EDIT	June 14, 2005 11:46:41 AM	PAGE	33	OF 58

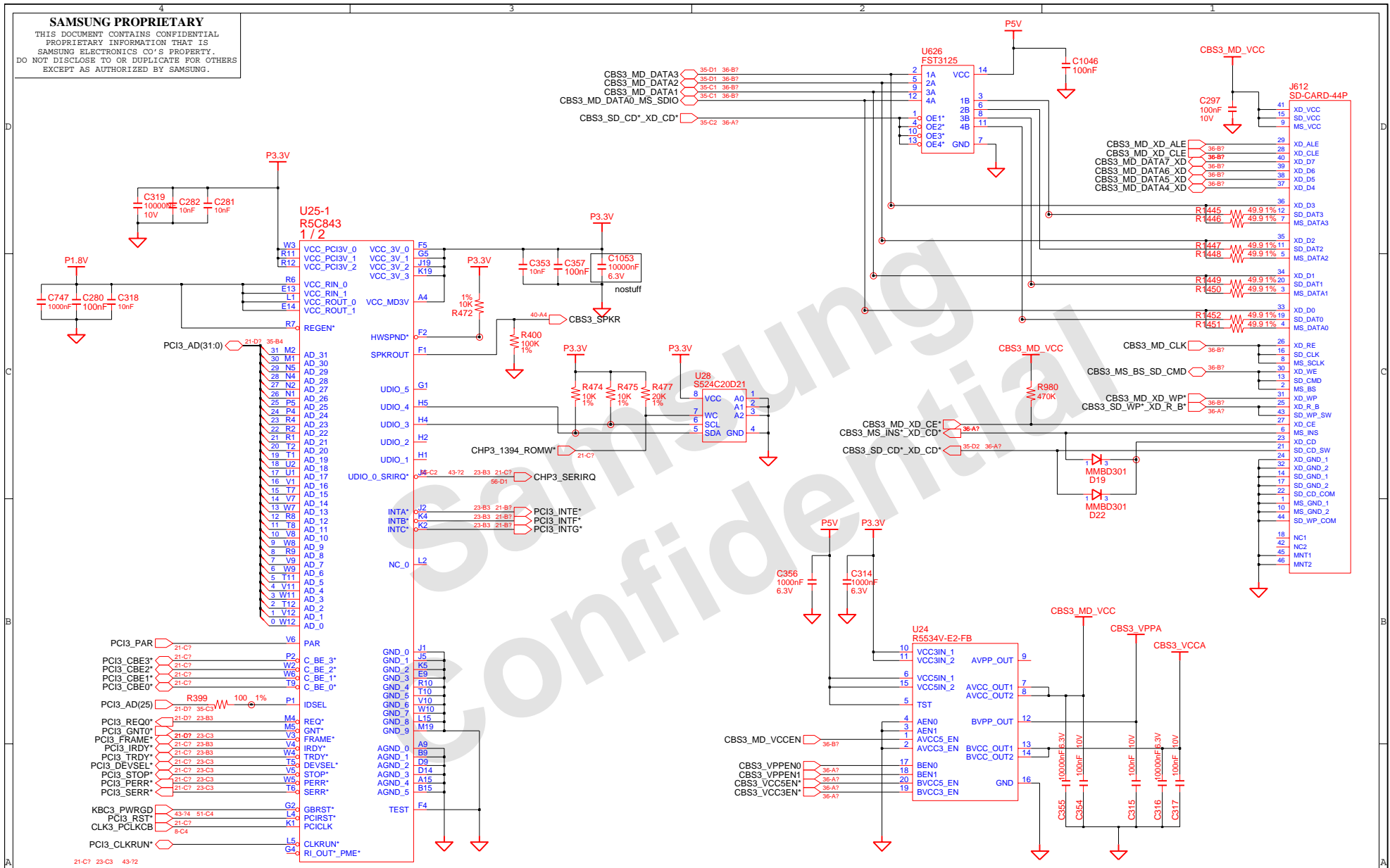
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DRAW	S.C.Lee	DATE	6/26/2006	TITLE	SEDONA MAIN	SAMSUNG ELECTRONICS
CHECK	J.Y.Lee	DEV. STEP	PV	CRT, S-VHS		
APPROVAL	S.S.Boek	REV	1.0			PART NO. BA41-00697A
MODULE CODE		LAST EDIT	June 14, 2005 11:46:41 AM	PAGE	34	OF 58

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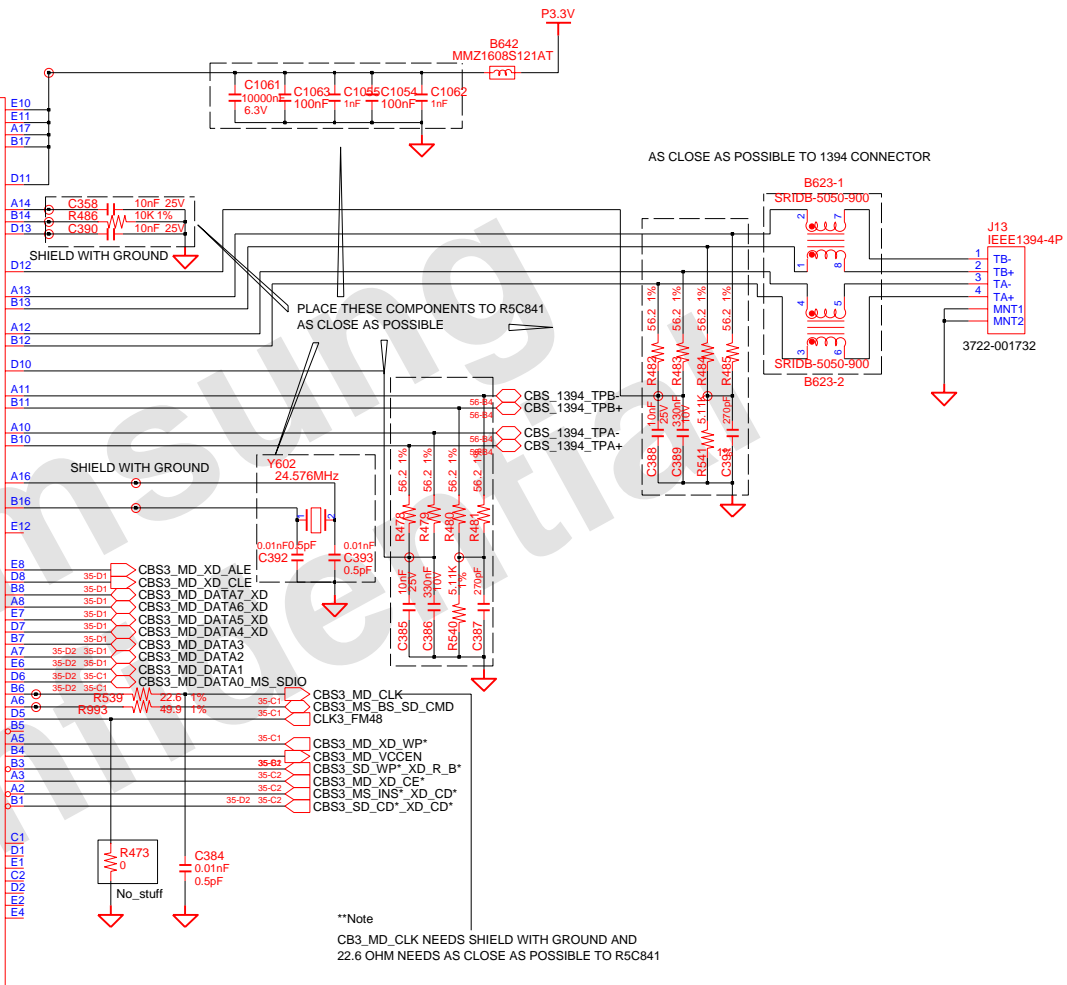
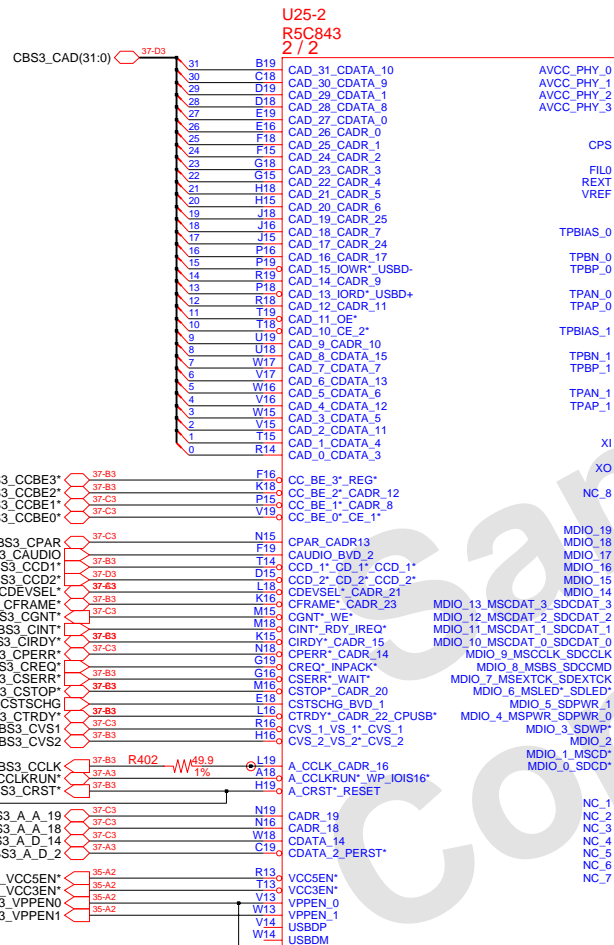


THIS PCICLK NEEDS SHIELD WITH GROUND

DRAW	S.C.Lee	DATE	6/26/2006	TITLE	SEDONA MAIN	SAMSUNG ELECTRONICS
CHECK	J.Y.Lee	DEV. STEP	PV	REV	CARDBUS / 1394	
APPROVAL	S.S.Boek	LAST EDIT	June 14, 2005 11:46:41 AM	PAGE	35	PART NO. BA41-00697A
MODULE CODE					OF 58	

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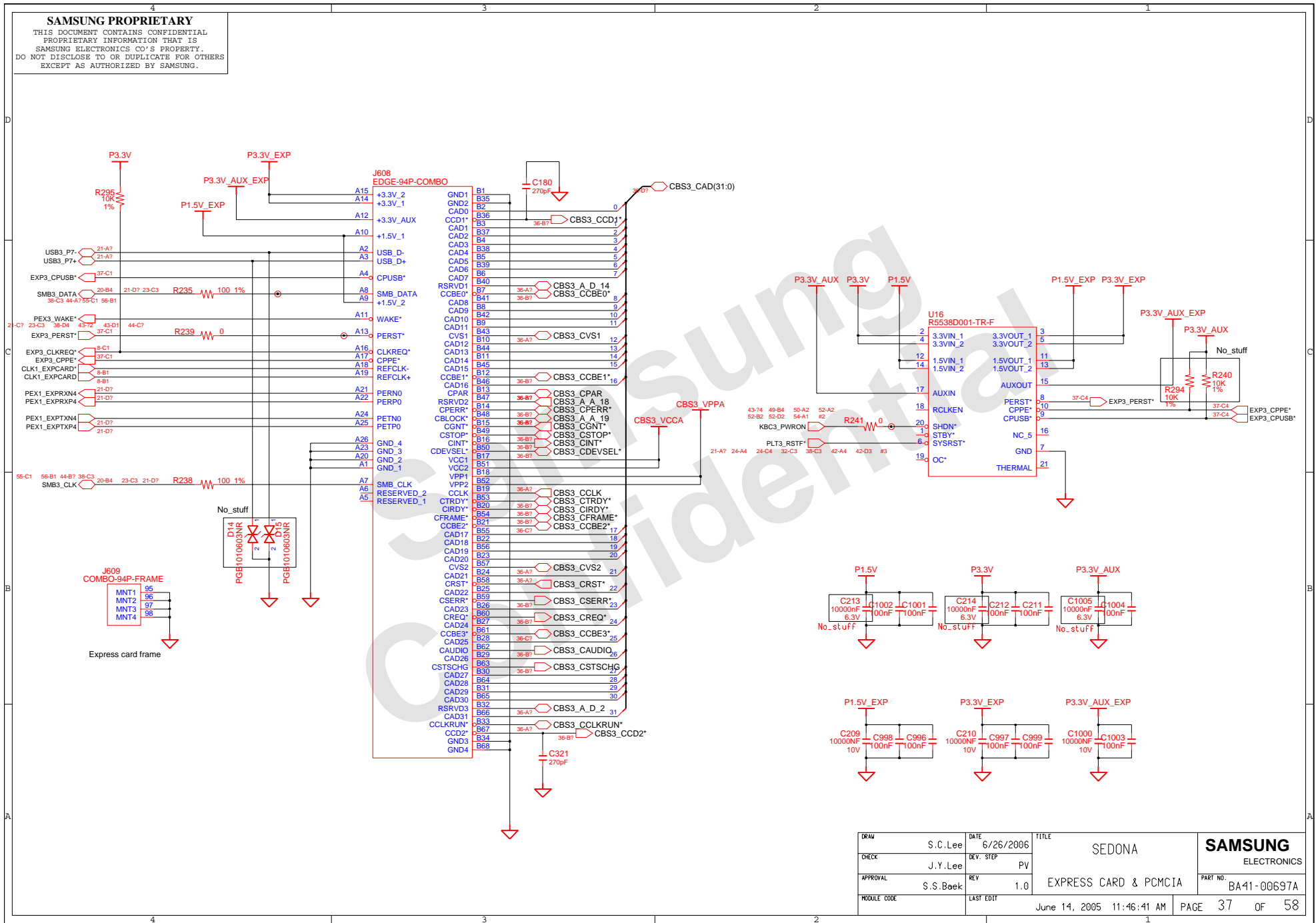


**Note
CB3_CLK NEEDS SHIELD WITH GROUND AND 47 OHM NEEDS AS CLOSE AS POSSIBLE TO R5C841

**Note
CB3_MD_CLK NEEDS SHIELD WITH GROUND AND 22.6 OHM NEEDS AS CLOSE AS POSSIBLE TO R5C841

DRAW	S.C.Lee	DATE	6/26/2006	TITLE	SEDONA	SAMSUNG ELECTRONICS
CHECK	J.Y.Lee	DEV. STEP	PV	MAIN		
APPROVAL	S.S.Boek	REV	1.0	CARDBUS SOCKET/MEDIA CARD	PART NO.	BA41-00697A
MODULE CODE		LAST EDIT	June 14, 2005 11:46:41 AM	PAGE	36	OF 58

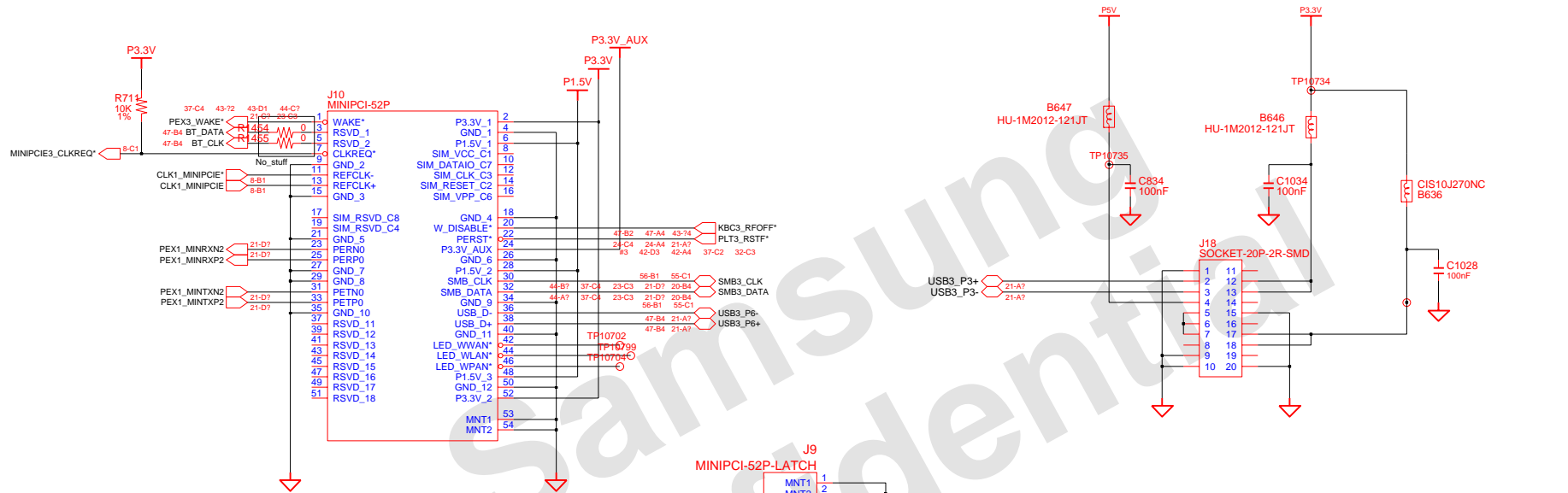
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DRAW	S.C.Lee	DATE	6/26/2006	TITLE	SEDONA	SAMSUNG ELECTRONICS
CHECK	J.Y.Lee	DEV. STEP	PV	EXPRESS CARD & PCMCIA		
APPROVAL	S.S.Boek	REV	1.0	PART NO. BA41-00697A		PAGE 37 OF 58
MODULE CODE		LAST EDIT	June 14, 2005 11:46:41 AM			

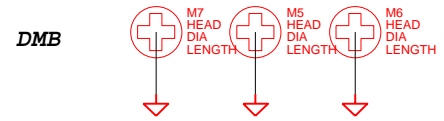
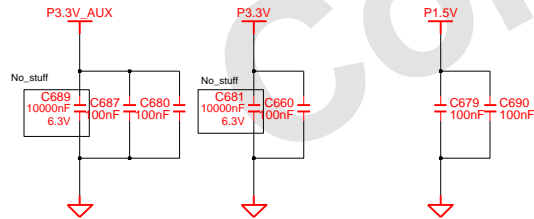
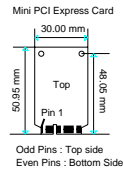
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Mini PCI Express

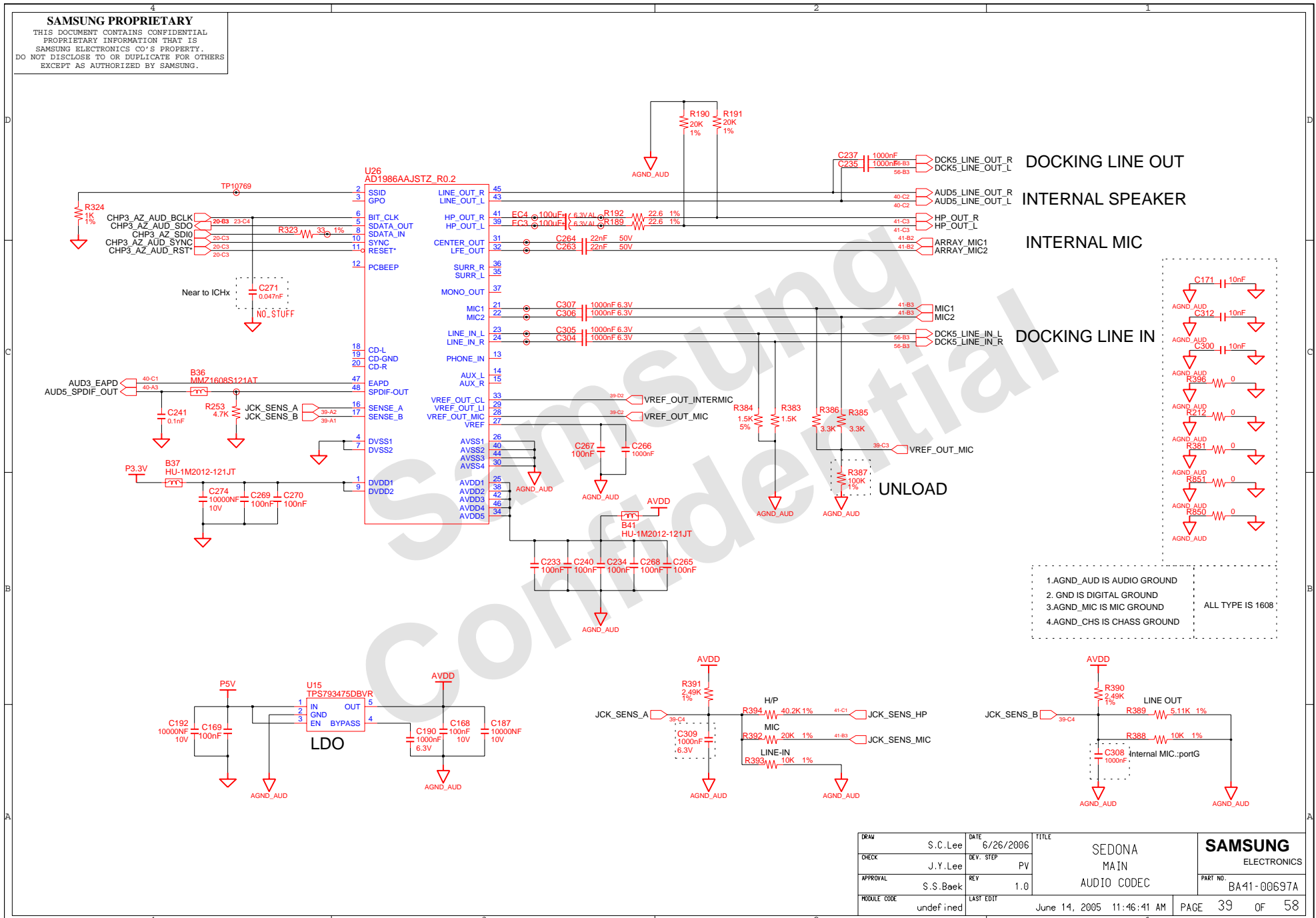
PCI Express Mini Card ElectroMechanical Spec. 1.0



DRAW	S.C.Lee	DATE	6/26/2006	TITLE	SEDONA MAIN	SAMSUNG ELECTRONICS
CHECK	J.Y.Lee	DEV. STEP	PV	MINI CARD & DMB		
APPROVAL	S.S.Boek	REV	1.0			PART NO. BA41-00697A
MODULE CODE	undefined	LAST EDIT	June 14, 2005 11:46:41 AM	PAGE	38	OF 58

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DOCKING LINE OUT

INTERNAL SPEAKER

INTERNAL MIC

DOCKING LINE IN

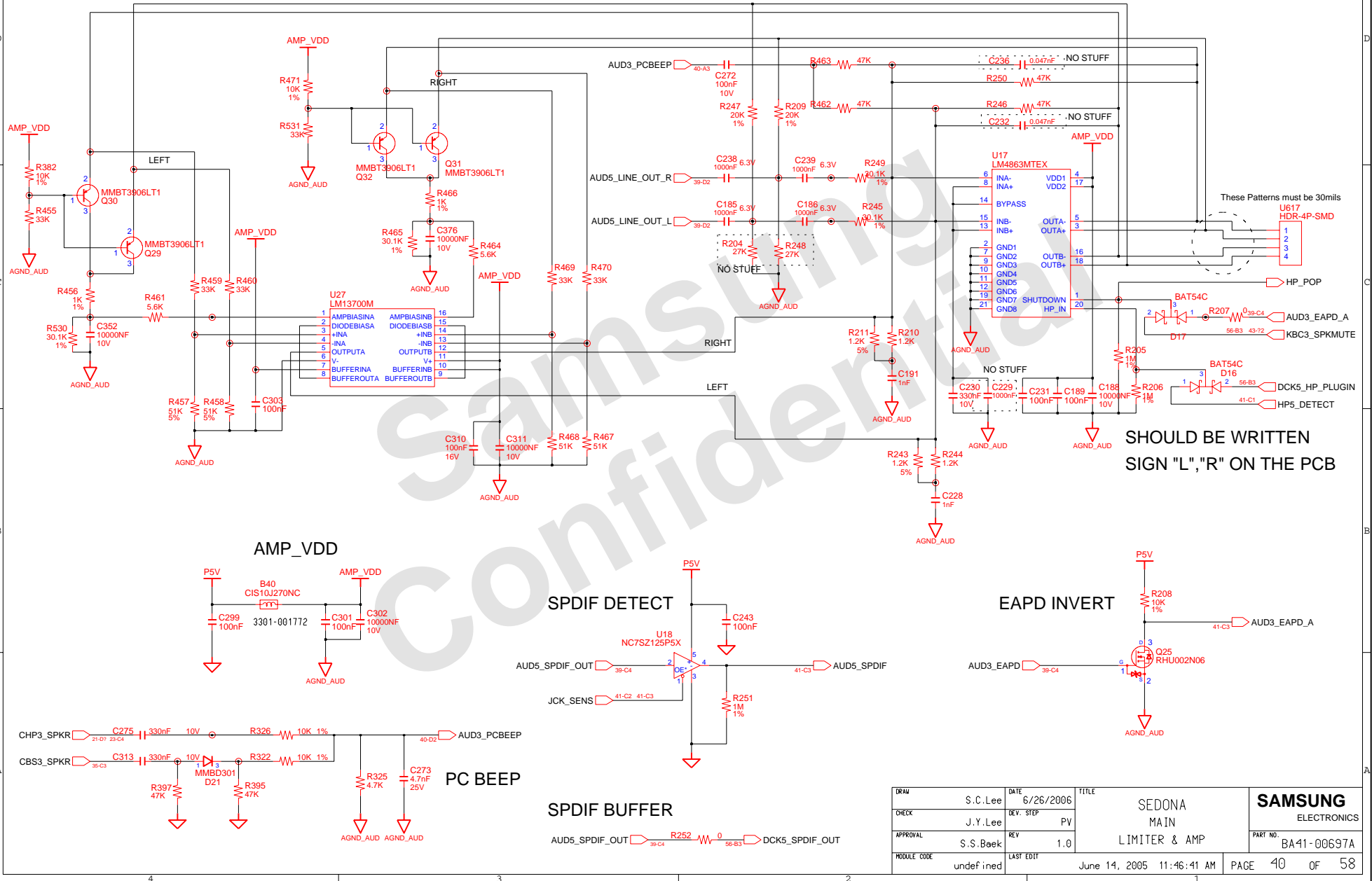
UNLOAD

- 1. AGND_AUD IS AUDIO GROUND
 - 2. GND IS DIGITAL GROUND
 - 3. AGND_MIC IS MIC GROUND
 - 4. AGND_CHS IS CHASSIS GROUND
- ALL TYPE IS 1608

DRAW	S.C.Lee	DATE	6/26/2006	TITLE	SEDONA MAIN	SAMSUNG ELECTRONICS
CHECK	J.Y.Lee	DEV. STEP	PV	AUDIO CODEC		
APPROVAL	S.S.Boek	REV	1.0			PART NO. BA41-00697A
MODULE CODE	undefined	LAST EDIT	June 14, 2005 11:46:41 AM	PAGE	39	OF 58

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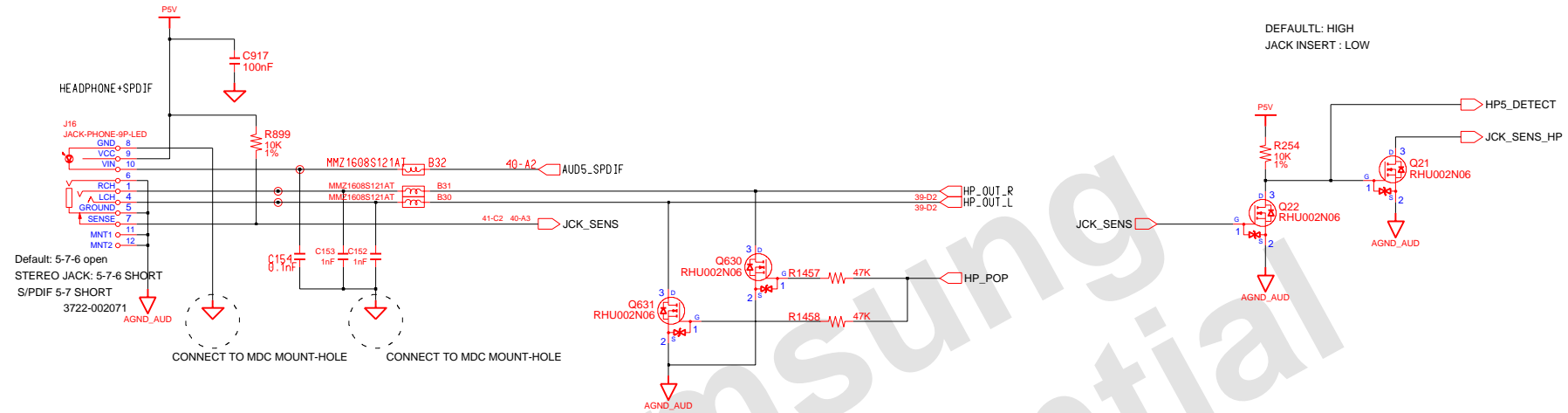
DRAW	S.C.Lee	DATE	6/26/2006	TITLE	SEDONA MAIN LIMITER & AMP	SAMSUNG ELECTRONICS
CHECK	J.Y.Lee	DEV. STEP	PV	REV	1.0	
APPROVAL	S.S.Boek	LAST EDIT	June 14, 2005 11:46:41 AM	PAGE	40 OF 58	
MODULE CODE	undefined					

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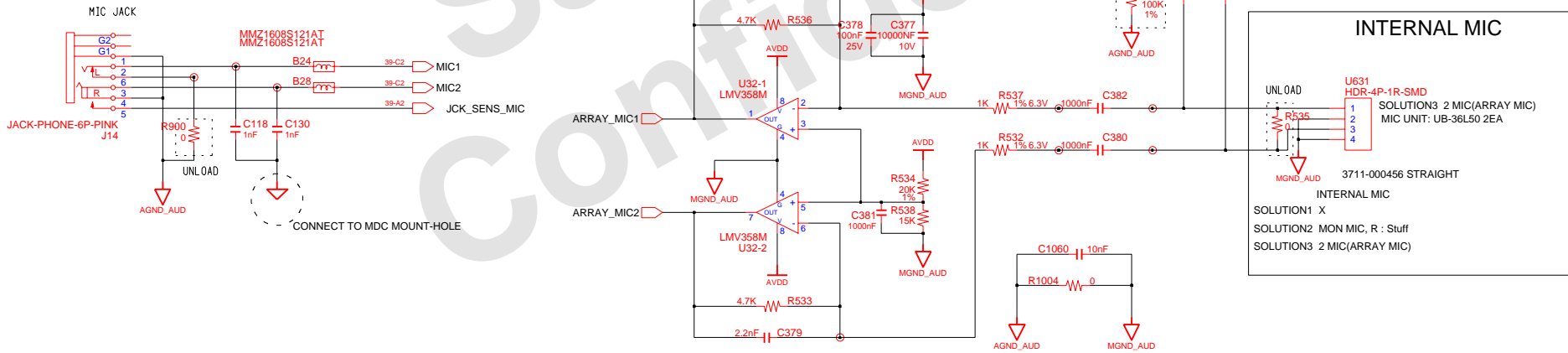
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JACK SENSE INVERT

DEFAULTL: HIGH
JACK INSERT : LOW



INVERTING AMP



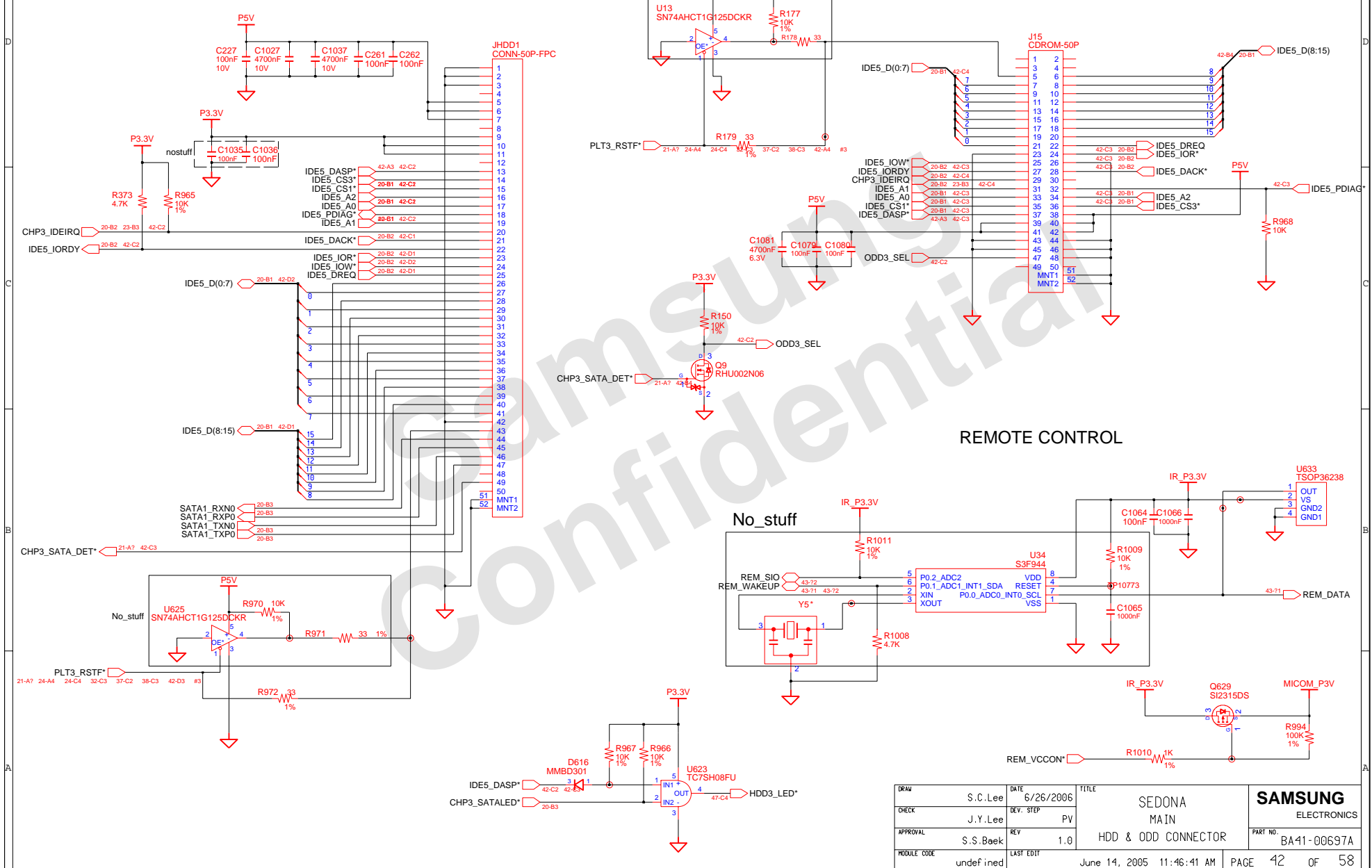
DRAW	S.C.Lee	DATE	6/26/2006	TITLE	SEDONA	SAMSUNG ELECTRONICS
CHECK	J.Y.Lee	DEV. STEP	PV		MAIN	
APPROVAL	S.S.Boek	REV	1.0		UPPER & AUDIO CONN	PART NO. BA41-00697A
MODULE CODE	undef ined	LAST EDIT	June 14, 2005 11:46:41 AM	PAGE	41	OF 58

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Main to HDD

NO STUFF

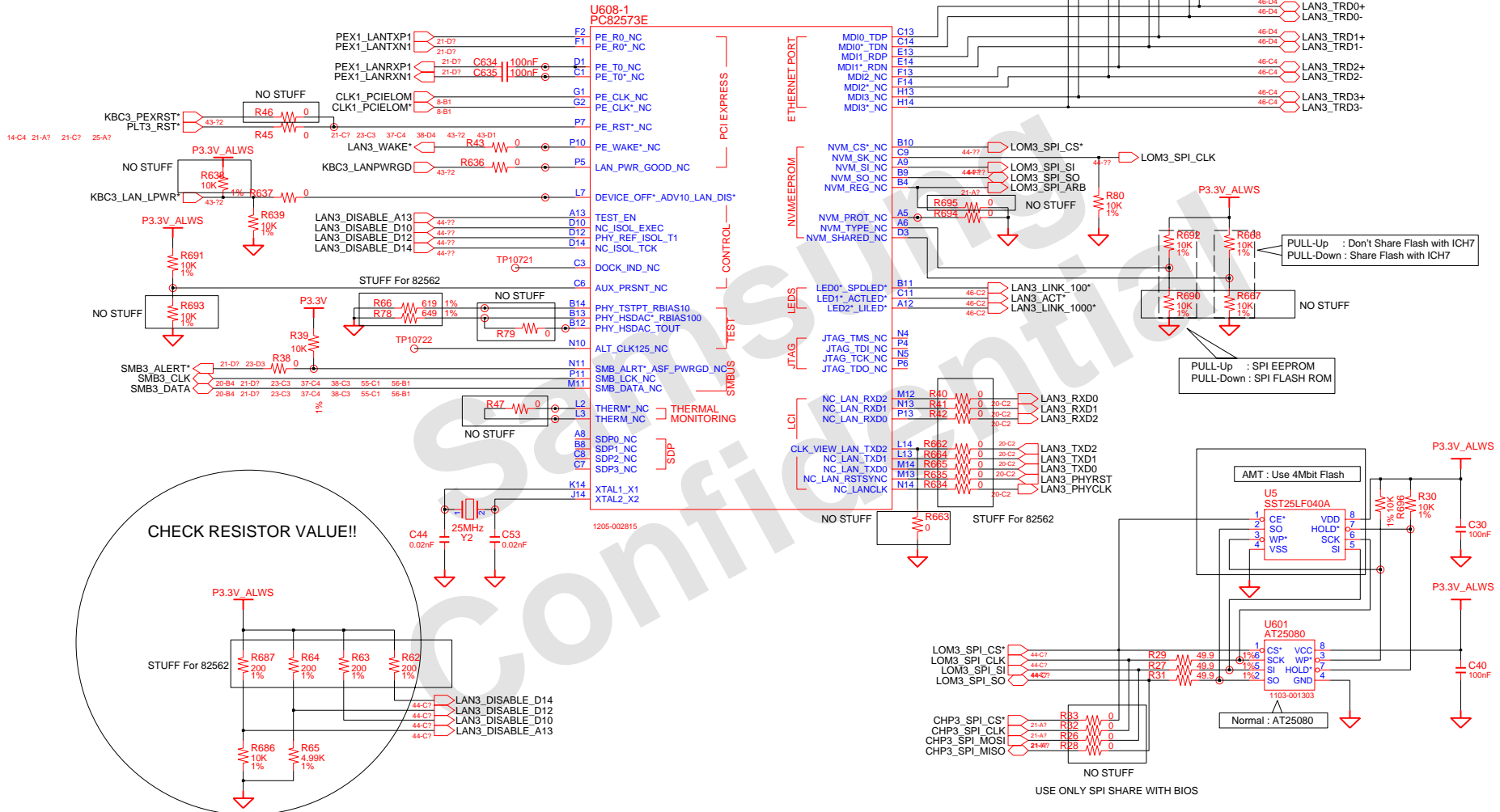
Main to ODD



DRAW	S.C.Lee	DATE	6/26/2006	TITLE	SEDONA MAIN	SAMSUNG ELECTRONICS
CHECK	J.Y.Lee	DEV. STEP	PV	HDD & ODD CONNECTOR		
APPROVAL	S.S.Boek	REV	1.0			PART NO. BA41-00697A
MODULE CODE	undefined	LAST EDIT	June 14, 2005 11:46:41 AM	PAGE	42	OF 58

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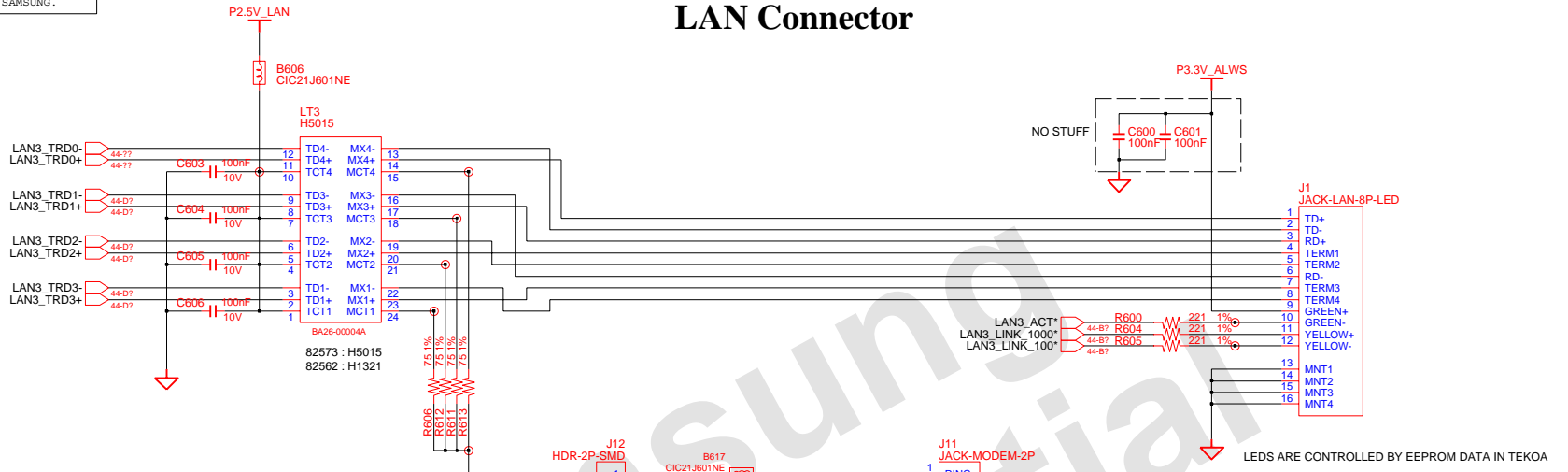


MODE	R698	R68	R66	R67
Normal Mode	NO STUFF	NO STUFF	NO STUFF	NO STUFF
Enhanced Mode	STUFF	NO STUFF	STUFF	STUFF
Full Disable Mode	STUFF	STUFF	STUFF	STUFF

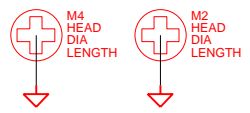
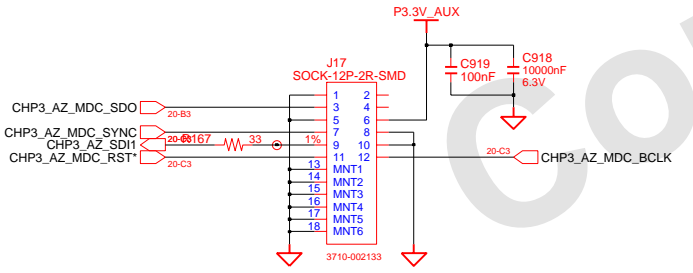
FOR 5705 STUFF			
DRAW	S.C.Lee	DATE	6/26/2006
CHECK	J.Y.Lee	DEV. STEP	PV
APPROVAL	S.S.Boek	REV	1.0
MODULE CODE	undef ined	LAST EDIT	June 14, 2005 11:46:41 AM
TITLE		SEDONA MAIN LOM 82573L	
SAMSUNG ELECTRONICS		PART NO. BA41-00697A	
PAGE		44 OF 58	

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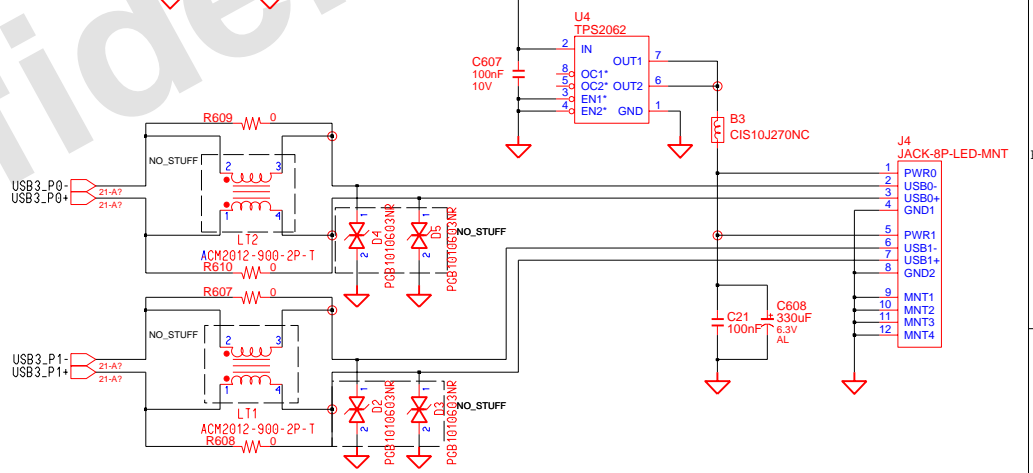
LAN Connector



MDC Connector



USB0,1 Connector

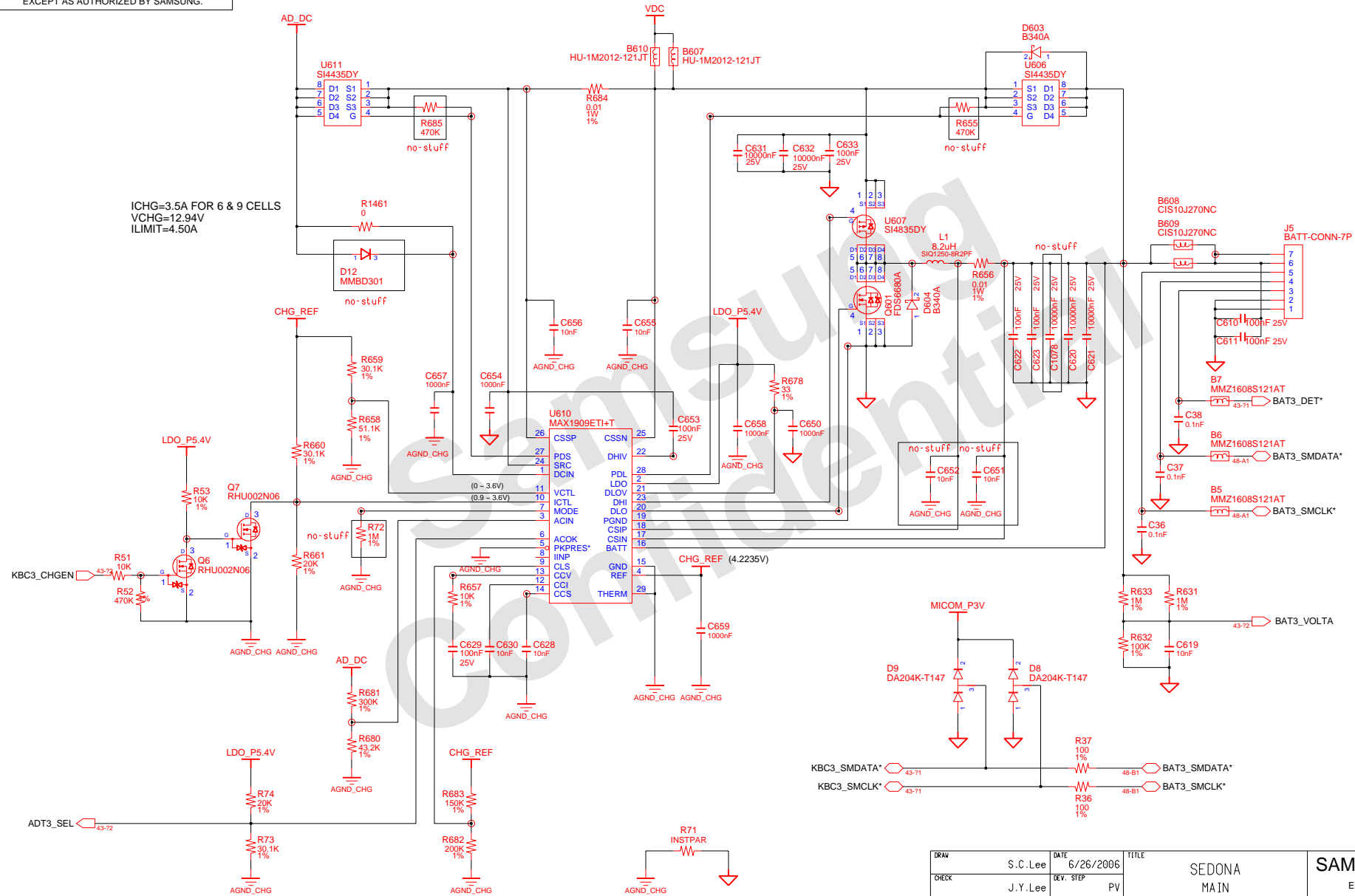


DRAW	S.C.Lee	DATE	6/26/2006	TITLE	SEDONA	SAMSUNG ELECTRONICS
CHECK	J.Y.Lee	DEV. STEP	PV	MAIN		
APPROVAL	S.S.Beek	REV	1.0	LAN & USB0 & MODEM Conn.	PART NO.	BA11-00697A
MODULE CODE	undefined	LAST EDIT	May, 24, 2005 1:20:49 PM	PAGE	46	OF 58

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CHARGER & POWER MANAGEMENT

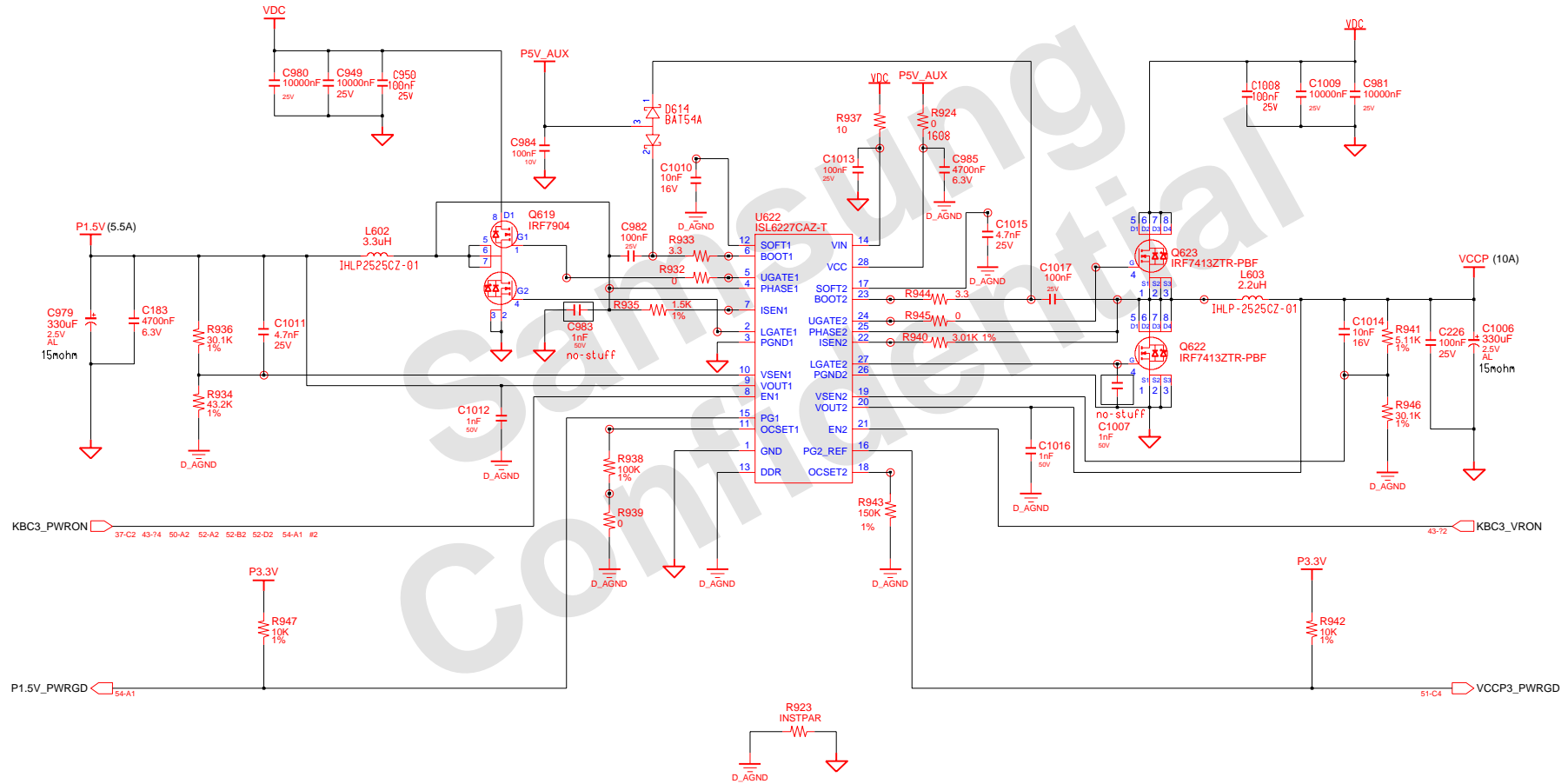
ICHG=3.5A FOR 6 & 9 CELLS
 VCHG=12.94V
 ILIMIT=4.50A



DRAW	S.C.Lee	DATE	6/26/2006	TITLE	SEDONA MAIN CHARGER	SAMSUNG ELECTRONICS
CHECK	J.Y.Lee	REV. STEP	PV			
APPROVAL	S.S.Boek	REV	1.0			PART NO. BA41-00697A
MODULE CODE	undefined	LAST EDIT	May, 24, 2005 1:21:14 PM	PAGE	48	OF 58

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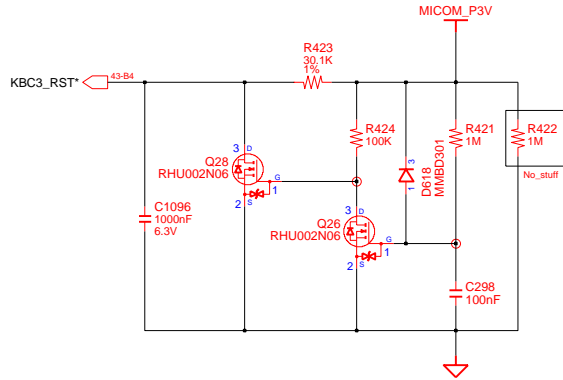
P1.5V & VCCP (1.05V)



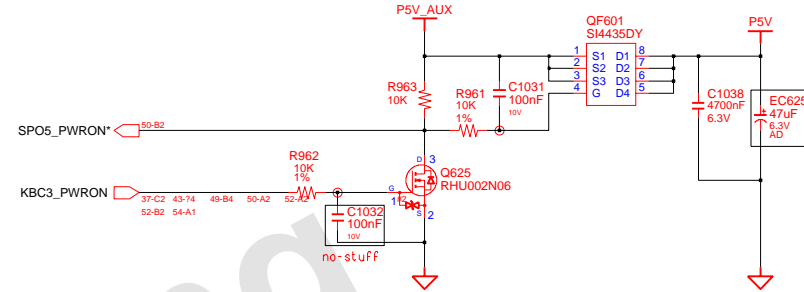
DRAW	S.C.Lee	DATE	6/26/2006	TITLE	SEDONA POWER P1.5V & VCCP	SAMSUNG ELECTRONICS
CHECK	J.Y.Lee	REV. STEP	PV			
APPROVAL	S.S.Boek	REV	1.0			PART NO. BA41-00697A
MODULE CODE	undefined	LAST EDIT	Mon, 24, 2005 1:21:25 PM	PAGE	49	OF 58

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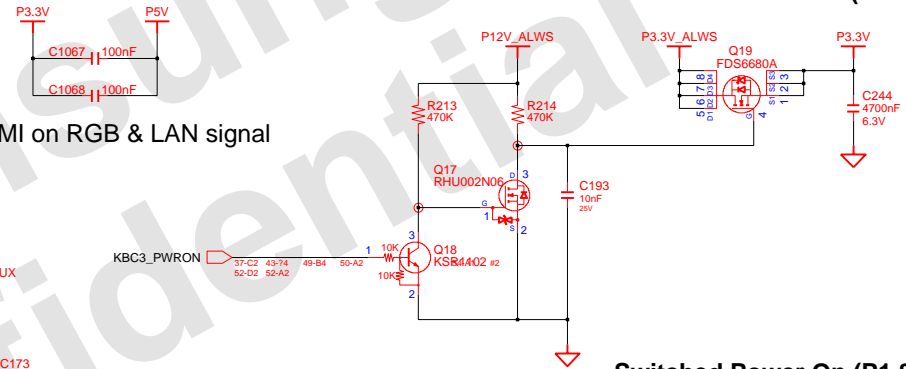
MICOM Reset



Switched Power On (P5V)

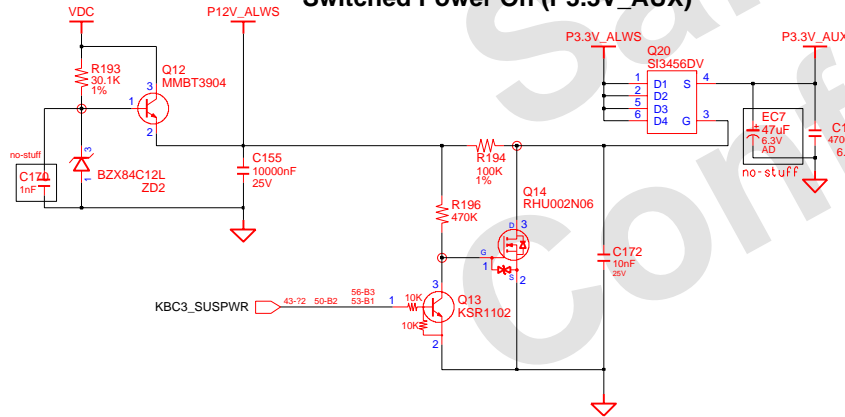


Switched Power On (P3.3V)

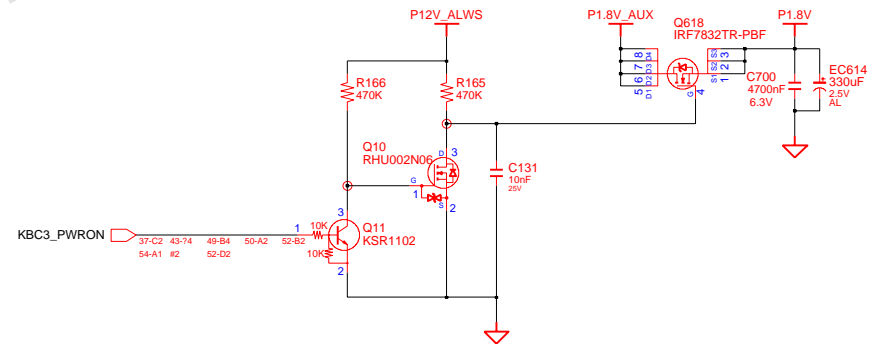


For EMI on RGB & LAN signal

Switched Power On (P3.3V_AUX)



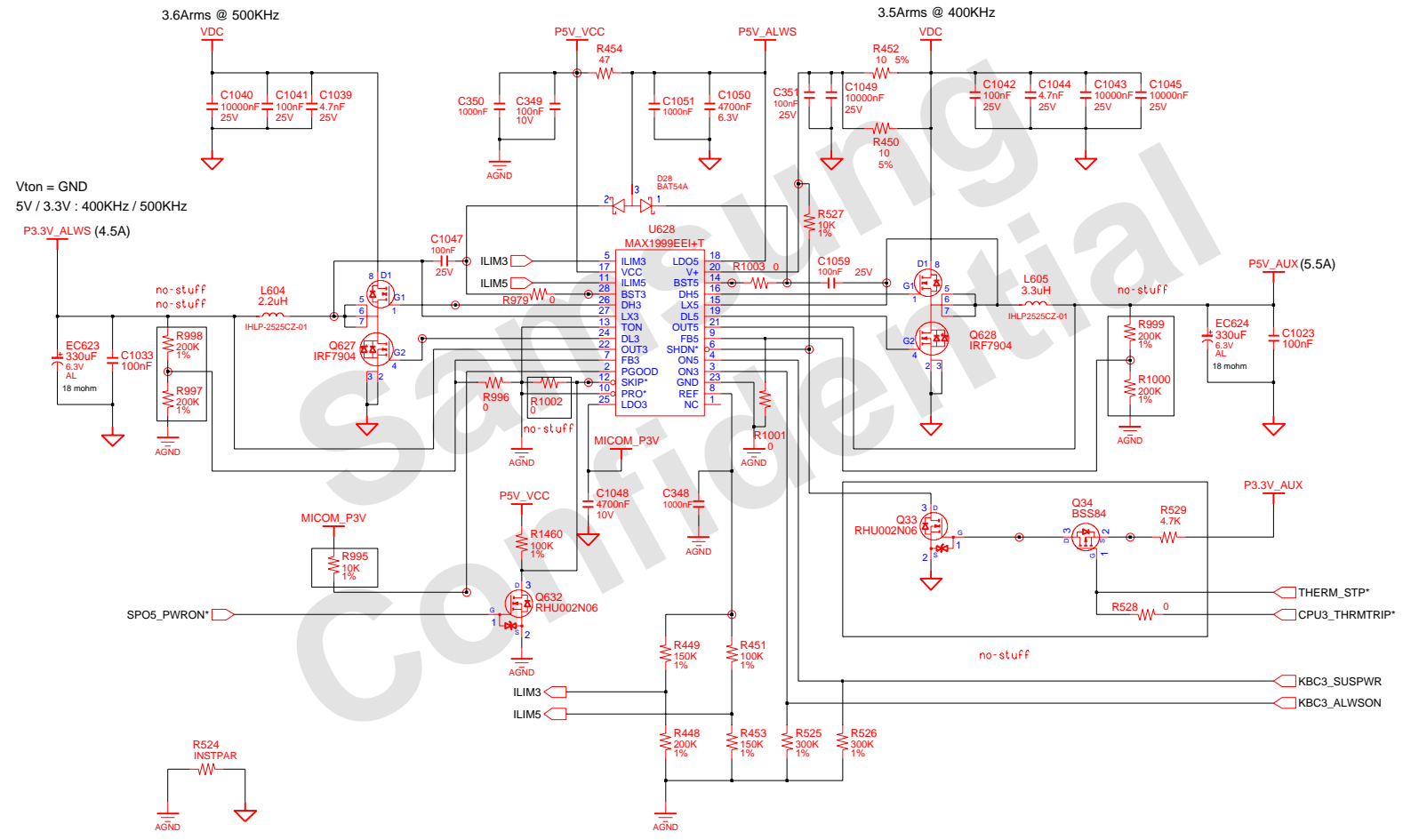
Switched Power On (P1.8V)



DRAWN	S.C.Lee	DATE	6/26/2006	TITLE	SEDONA MAIN	SAMSUNG ELECTRONICS
CHECK	J.Y.Lee	REV. STEP	PV	MICOM & SWITCHED POWER		
APPROVAL	S.S.Beek	REV	1.0	PARTNO		BA41-00697A
MODULE CODE	undefined	LAST EDIT	May, 24, 2005 1:21:53 PM	PAGE	52	OF 58

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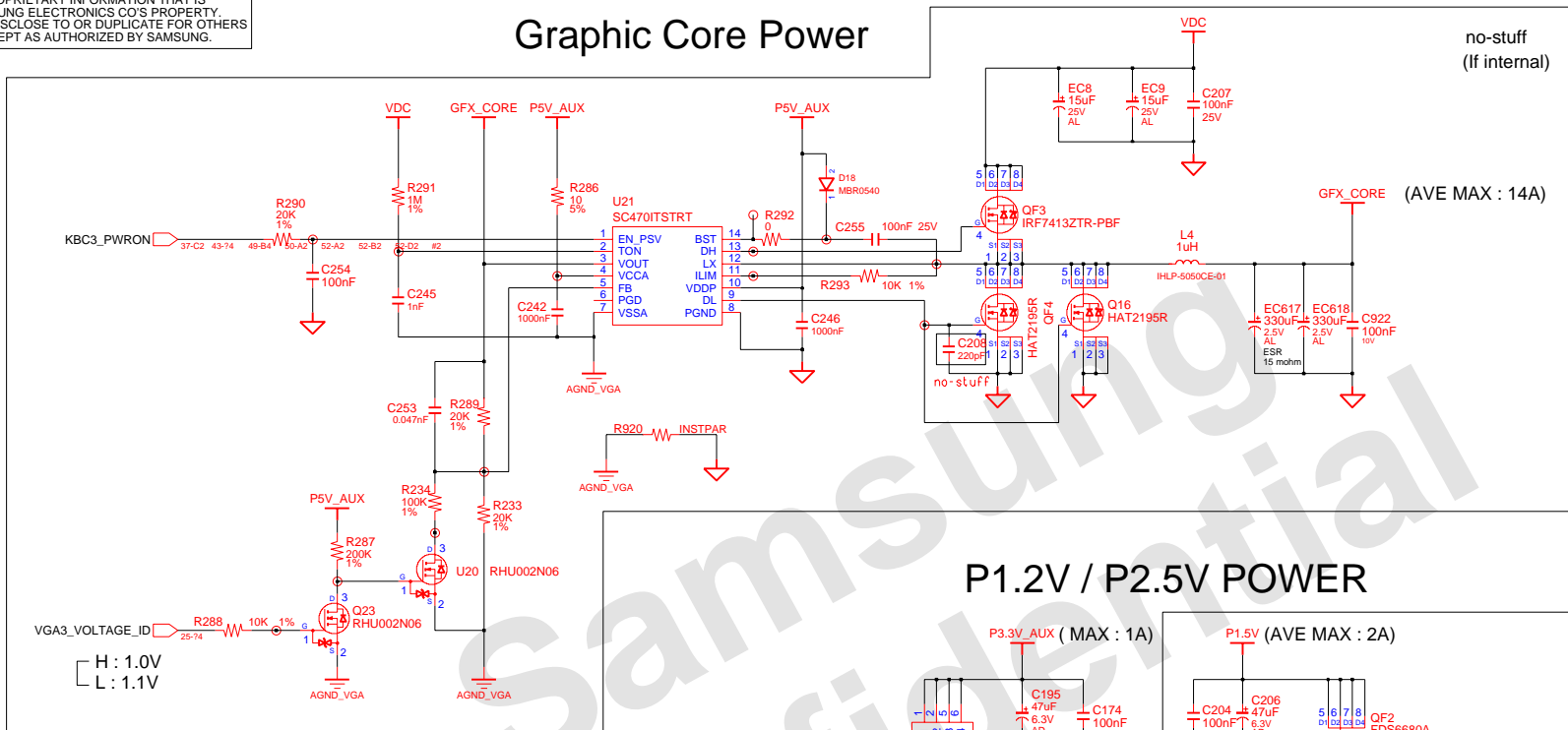
P3.3V_ALWS & P5V_AUX



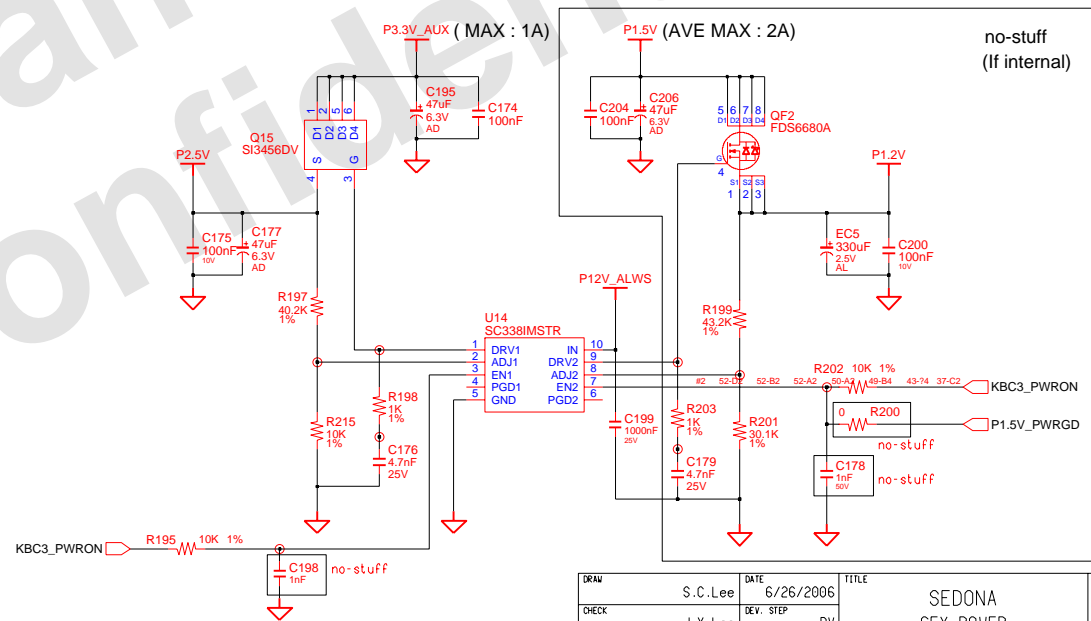
DRAW	KIM, DH	DATE	6/26/2006	TITLE	SEDONA MAIN	SAMSUNG ELECTRONICS
CHECK	J.Y.Lee	DEV. STEP		3.3V & 5V GENERATION	PART NO. BA41-00697A	
APPROVAL	S.S.Boek	REV	1.0	March, 9, 2002 4:21:54 PM	PAGE 53 OF 58	
MODULE CODE		LAST EDIT				

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Graphic Core Power



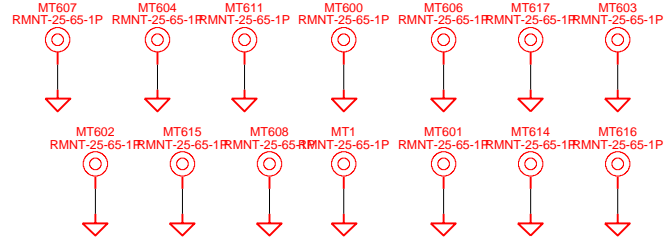
P1.2V / P2.5V POWER



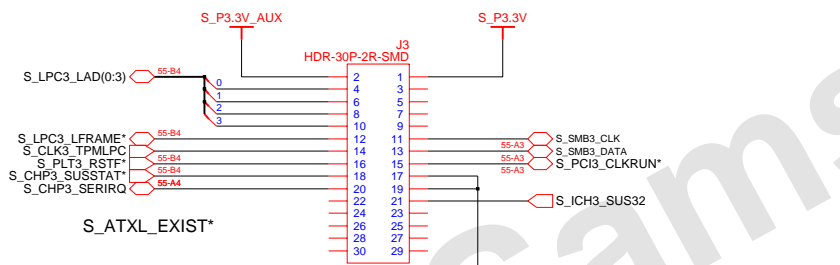
	M54/M56	M64	M66
R233	20K	20K	22.1K
R234	100K	51.1K	51.1K
Graphic Core	1.1v/1.0v	1.2v/1.0v	1.14v/0.95v

DRW	S.C.Lee	DATE	6/26/2006	TITLE	SEDONA	SAMSUNG ELECTRONICS
CHECK	J.Y.Lee	DEV. STEP	PV	GFX POWER		
APPROVAL	S.S.Beek	REV	1.0	P1.2V & P2.5V AUX POWER		PART NO. BA41-00697A
MODULE CODE	undefined	LAST EDIT	May, 24, 2005 1:22:04 PM	PAGE	54	OF 58

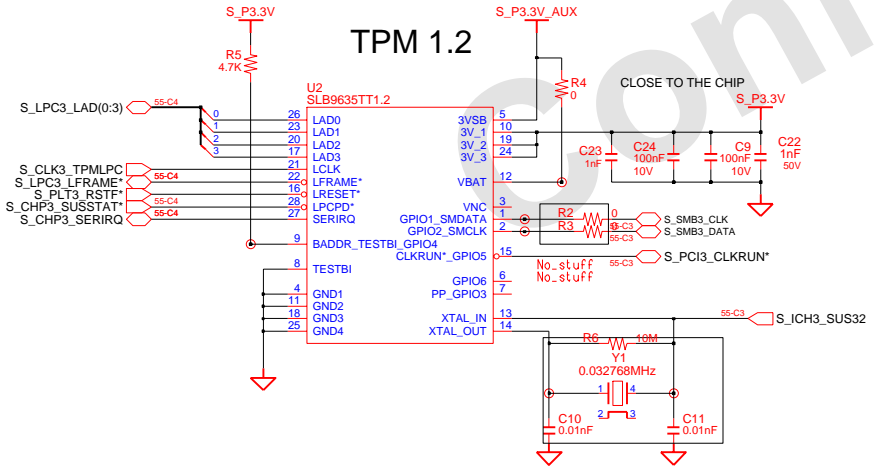
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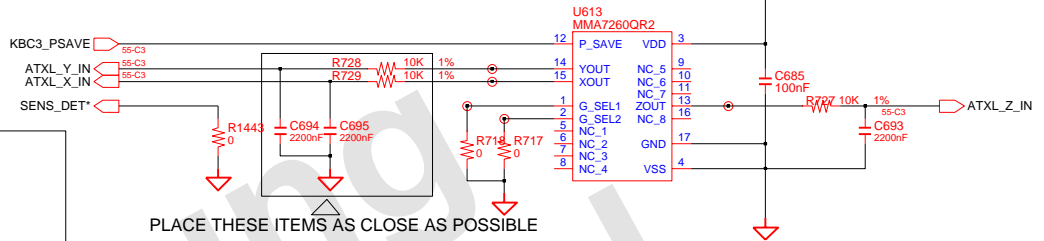
TPM_SUB Board



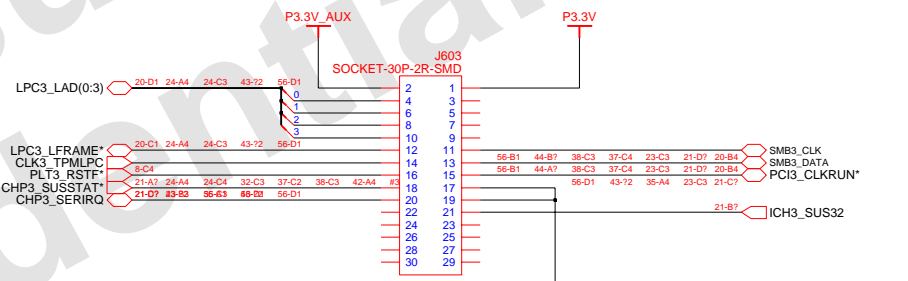
TPM 1.2



HDD PARKING

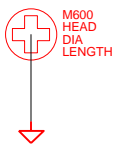
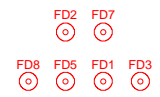


PLACE THESE ITEMS AS CLOSE AS POSSIBLE



PCB REVISION CONTROL (ICT)

NO	CONNECTION	DATE(Y/MM/DD)	REVISION	STEP
1	N.C.			
2	1-2			
3	2-3			
4	3-1			
5	1-2-3			
6	N.C.			
7	1-2			
8	2-3			
9	3-1			
10	1-2-3			



DRAW	S.C.Lee	DATE	6/26/2006	TITLE	SEDONA MAINBD AIRBAG & TPM	SAMSUNG ELECTRONICS PART NO. BA41-00697A
CHECK	J.Y.Lee	DEV. STEP	PV			
APPROVAL	S.S.Boek	REV	1.0			
MODULE CODE	undefined	LAST EDIT	May, 24, 2005 1:22:32 PM	PAGE	55 OF 58	

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Revision History

Page No. Cause And Actions (Revised Items)

Page No. Cause And Actions (Revised Items)

Revision From 0.75 to 0.8

Revision From 0.9 to 1.0

- 20 ADDED LCI INTERFACE SIGNAL
ADDED LAN EEPROM INTERFACE FOR INTEL 82562
- 21 CHANGED POWER SEQUENCE(POWEROK SWAPED TO VRMPWRGD)
- 43,44 CHANGE LOM FROM BCM5788 TO INTEL TEKOA(82573EZ)
- 42 ADD KBC3_LANRST*,KBC3_GATEDRST*,KBC3_LANLPWR PIN
- 38 CHAGED AUDIO GND NET NAME
U731 CHANGED TO 2N7002
ADD AUD3_GPID,AUD_DCVOL
ADD R1736,R1737,R1738,R1739,R1740,R1741
CHANGE POSITION & VALUE OF JACK SENSE A.B(C1309,C1310)
DELETE AMP6_PWRDN,KBC5_AVDD_ON SIGNAL OF U733
MOVE HP6_OUT_R,L TO LINE2_R,L
ADD C1445,C1446
ADD R1734,R1735,R1744,R1745,R1751,R1752,EC753,EC754,C1447,C1448

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DRAW	S.C.Lee	DATE	6/26/2006	TITLE	SEDONA	SAMSUNG ELECTRONICS
CHECK	Y.S.Lee	DEV. STEP	PV			
APPROVAL	S.S.Boek	REV	1.0	REVISION HISTORY		PART NO. BA41-00697A
MODULE CODE	undefined	LAST EDIT	May, 24, 2005 1:23:07 PM	PAGE	58	OF 58

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TP10872ONIC1
TP10873ONIC2
TP10874OLIM3
TP10875OLIMS
TP10876OBT_CLK
TP10877ODCK3_C
TP10878ODCK3_Y
TP10879OCFX3_C
TP10880OCFX3_Y
TP10881OVGA3_C
TP10882OVGA3_Y
TP10883OBT_DATA
TP10884OBT_DET*

TP10893OIDE5_A0
TP10894OIDE5_A1
TP10895OIDE5_A2
TP10896OAIT3_SEL

TP10898OCPU1_NMI
TP10899OCPU1_TCK
TP10900OCPU1_TDI
TP10901OCPU1_IMS
TP10902ODCK3_RED

TP11091OHDD3_LED*
TP11092OIDE5_CS1*
TP11093OIDE5_CS3*
TP11094OIDE5_D(0)
TP11095OIDE5_D(1)
TP11096OIDE5_D(2)
TP11097OIDE5_D(3)
TP11098OIDE5_D(4)
TP11099OIDE5_D(5)
TP11100OIDE5_D(6)
TP11101OIDE5_D(7)
TP11102OIDE5_D(8)
TP11103OIDE5_D(9)
TP11104OIDE5_DREQ
TP11105OIDE5_IOR*
TP11106OIDE5_IOW*
TP11107OKBC3_A20C
TP11108OKBC3_RST*
TP11109OKBC3_VRON
TP11110OKBC5_TCLK
TP11111OLAN3_ACT*
TP11112OLAN3_RXD0
TP11113OLAN3_RXD1
TP11114OLAN3_RXD2
TP11115OLAN3_TXD0
TP11116OLAN3_TXD1
TP11117OLAN3_TXD2

TP11120OLCD3_BRIT
TP11121OCPI3_RST*
TP11122OPLT3_RST*
TP11123OP25_KCLK

TP11256OIDE5_IORDY
TP11257ODCK3_SENS_A
TP11258ODCK3_SENS_B
TP11259OKBC3_CHEFN
TP11260OKBC3_PSAVE
TP11261OKBC3_PWRGD
TP11262OKBC3_PWRON
TP11263OKBC5_TDATA

TP11274OLCD3_VDDEN

TP11279OCPI3_AD(0)
TP11280OCPI3_AD(1)
TP11281OCPI3_AD(2)
TP11282OCPI3_AD(3)
TP11283OCPI3_AD(4)
TP11284OCPI3_AD(5)
TP11285OCPI3_AD(6)
TP11286OCPI3_AD(7)
TP11287OCPI3_AD(8)
TP11288OCPI3_AD(9)
TP11289OCPI3_CBE0*
TP11290OCPI3_CBE1*
TP11291OCPI3_CBE2*
TP11292OCPI3_CBE3*
TP11293OCPI3_GNT0*

TP11295OCPI3_INTA*
TP11296OCPI3_INTB*
TP11297OCPI3_INTC*
TP11298OCPI3_INTD*
TP11299OCPI3_INTE*
TP11300OCPI3_INTF*
TP11301OCPI3_INTG*

TP11303OCPI3_IRDY*
TP11304OCPI3_PERR*
TP11305OCPI3_REQ0*
TP11306OCPI3_REQ1*
TP11307OCPI3_REQ2*
TP11309OCPI3_SERR*
TP11310OCPI3_STOP*
TP11311OCPI3_TRDY*
TP11312OPEX3_WAKE*
TP11313OPLT3_RSTF*
TP11314OPS25_KDATA
TP11315OPS25_MDATA
TP11316OREM_VCCON*
TP11317OREM_WAKEUP

TP11322OSIO3_CTS1*
TP11323OSIO3_DCD1*
TP11324OSIO3_DRST*
TP11325OSIO3_DSRI*
TP11326OSIO3_DTR1*
TP11327OSIO3_RTS1*
TP11328OSIO3_TXD1*
TP11329OS_SMB3_CLK

TP11332OTHERM_STP*
TP11335OVGA3_GREEN

TP10904OQDD3_SEL
TP10905OCPI3_PAR
TP10906OSMB3_CLK

TP10834OCFX3_RED

TP10838OHP_OUT_L
TP10839OHP_OUT_R
TP10840OCHK_SENS
TP10908OATXL_Y_IN
TP10909OATXL_Y_IN
TP10910OATXL_Z_IN
TP10911OAUD3_EAPD
TP10912CBAT3_DET*
TP10913OCBS3_CCLK
TP10914OCBS3_CPAR
TP10915OCBS3_CVS1
TP10916OCBS3_CVS2
TP10917OCBS3_SPKR

TP10919OCHP3_SPKR

TP10922CLK3_FM48
TP10923OCPU1_ADS*
TP10924OCPU1_BNR*
TP10925OCPU1_H11*
TP10926OCPU1_PS1*
TP10927OCPU1_RS0*
TP10928OCPU1_RS1*
TP10929OCPU1_RS2*
TP10930OCPU1_SL5*
TP10931OCPU1_SWS*
TP10932ODCK19_IN*
TP10933ODCK3_BLUE
TP10934ODCK3_COMP

TP11124OP25_MCLK
TP11125OSIO3_R11*
TP11126OSIO3_RXD1

TP11199ODCK3_CLK33
TP11200ODCK3_DRST*
TP11201ODCK3_GREEN
TP11202ODCK3_PWRGD
TP11203ODCK3_PWRON
TP11204ODCK3_SIO14
TP11205ODCK3_SMCLK

TP11188OCPU1_DBSY*

TP11191OCPU1_FERR*

TP11196OCPU1_TRST*
TP11197OCRT3_HSYNC
TP11127OSMB3_DATA
TP11128OVGA3_BLUE
TP11129OVGA3_BRIT
TP11130OVGA3_COMP

TP11139OARRAY_MIC1
TP11140OARRAY_MIC2

TP11142OAU05_SPDIF
TP11143CBAT3_VOL_TA
TP11144OCBS3_A.D_2
TP11145OCBS3_CCD1*
TP11146OCBS3_CCD2*
TP11147OCBS3_CGN1*
TP11148OCBS3_CGN2*
TP11149OCBS3_CRE0*
TP11150OCBS3_CRE1*
TP11151OCHP3_EE_CS

TP11153OCHP3_THRM*

TP11161OCLK1_VGASS
TP11162OCLK3_ICH14

TP11167OCLK3_SIO14
TP11168OCLK3_USB48

TP11176OCPU1_A20M*

TP11179OCPU1_BSEL0
TP11180OCPU1_BSEL1
TP11181OCPU1_BSEL2

TP11434OKBC3_EJECT*
TP11435OKBC3_PWRSW*
TP12041OCPU1_DEFER*
TP12042OCPU1_IOWNE*
TP12043OCPU1_VID(9)
TP12044OCPU1_VID(1)
TP12045OCPU1_VID(2)
TP12046OCPU1_VID(3)
TP12047OCPU1_VID(4)
TP12048OCPU1_VID(5)
TP12049OCPU1_VID(6)
TP12050OCPU3_ALERT*
TP12051OCRT3_DDOCLK
TP12052ODCK3_EJECT*
TP12053ODCK3_LAD(0)
TP12054ODCK3_LAD(1)
TP12055ODCK3_LAD(2)
TP12056ODCK3_LAD(3)
TP12057ODCK3_LDR01*
TP12058ODCK3_SERIRQ
TP12059ODCK3_SMDATA

TP12015OEXP3_CPUSB*
TP12016OEXP3_PERST*
TP12017OCFX3_DDOCLK
TP12018OIDE5_PDIAG*
TP12019OIDE5_PDIAG*
TP12020OCHK_SENS_HP
TP12021OKBC3_ALWSON
TP12022OKBC3_BKLTON
TP12023OKBC3_DCKIN*
TP12024OCRT3_VSYNC
TP12025OEXP3_CPPE*

TP12019OIDE5_PDIAG*
TP12020OCHK_SENS_HP
TP12021OKBC3_ALWSON
TP12022OKBC3_BKLTON
TP12023OKBC3_DCKIN*
TP12024OCRT3_VSYNC
TP12025OEXP3_CPPE*

TP11139OARRAY_MIC1
TP11140OARRAY_MIC2
TP11142OAU05_SPDIF
TP11143CBAT3_VOL_TA
TP11144OCBS3_A.D_2
TP11145OCBS3_CCD1*
TP11146OCBS3_CCD2*
TP11147OCBS3_CGN1*
TP11148OCBS3_CGN2*
TP11149OCBS3_CRE0*
TP11150OCBS3_CRE1*
TP11151OCHP3_EE_CS

TP11153OCHP3_THRM*

TP11161OCLK1_VGASS
TP11162OCLK3_ICH14

TP11167OCLK3_SIO14
TP11168OCLK3_USB48

TP11242OFH3_INIT*
TP11243OCFX3_GREEN
TP11244OCFX3_HSYNC
TP11245OCFX3_VSYNC
TP11246OHP5_DETECT*
TP11247OICH3_SUS32
TP11248OIDE5_D(10)
TP11249OIDE5_D(11)
TP11250OIDE5_D(12)
TP11251OIDE5_D(13)
TP11252OIDE5_D(14)
TP11253OIDE5_D(15)
TP11254OIDE5_DACK*
TP11255OIDE5_DASP*

TP11124OP25_MCLK
TP11125OSIO3_R11*
TP11126OSIO3_RXD1

TP11339OCRT3_ON_LED*
TP11340OSIO3_DCD1*
TP11341OSMB3_ALERT*
TP11342OSPO5_PWRON*

TP11346OS_SMB3_DATA
TP11347OVCCP3_PWRGD

TP11349OVGA3_DDOCLK
TP11350OVGA3_DVICLK
TP11351OVGA3_HDD1*
TP11352OVGA3_THRNDP
TP11353OVGA3_THRMDP
TP11354OVGA5_DDOCLK
TP11355OVGA5_DVICLK
TP11356OAND3_NUMLED*
TP11357CBAT3_SMDATA*

TP11358OCBS3_CAD(10)
TP11359OCBS3_CAD(11)
TP11360OCBS3_CAD(12)
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TP11379OCBS3_CAD(31)
TP11380OCBS3_CFRAME*
TP11381OCBS3_CSTSCHG
TP11382OCBS3_VCC3EN*
TP11383OCBS3_VCC5EN*
TP11384OCHP3_AZ_SDIO
TP11385OCHP3_AZ_SDI1
TP11386OCHP3_BIOSWP*
TP11387OCHP3_EE_DOUT
TP11388OCHP3_NUMLED*
TP11389OCHP3_PCS1P*
TP11390OCHP3_PWRBTN*

TP11392OCHP3_SMLINK1
TP11393OCHP3_SP1_CLK
TP11394OCHP3_SP1_CS*

TP11396OCLK1_EXPCARD

TP11399OCLK3_PCLKFWH
TP11400OCLK3_PCLKICH
TP11401OCLK3_PCLKSIO
TP11402OCLK3_SMBDATA

TP11431OLAN3_PHYCLK
TP11432OLAN3_PHRST
TP11433OLAN3_LOW_PWR
TP11434OLPC3_LAD(0)
TP11435OLPC3_LAD(1)
TP11436OLPC3_LAD(2)
TP11437OLPC3_LAD(3)

TP11422OLCD3_BKLTON
TP11423OLCD3_BKLTON
TP11424OLCD3_SP1_S1
TP11425OLQMS_SP1_S0
TP11426OCP1_5V_PWRGD
TP11427OCPI3_AD(10)
TP11428OCPI3_AD(11)
TP11429OCPI3_AD(12)
TP11430OCPI3_AD(13)
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TP11440OCPI3_AD(23)
TP11441OCPI3_AD(24)
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TP11445OCPI3_AD(28)
TP11446OCPI3_AD(29)
TP11447OCPI3_AD(30)
TP11448OCPI3_AD(31)
TP11449OCPI3_PLCK*

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Table with 4 columns (labeled 4, 3, 2, 1) and 4 rows (labeled D, C, B, A). Each cell contains a list of component identifiers such as TP11932, TP11684, TP11680, etc., along with their respective pin names and functions.

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