

9. 회로도

9-1. External Graphic

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SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
Cardbus	AD25	0	A,B,C
	AD21	3	
MiniPCI SLOT1	AD23	2	D,E
USB	AD29(internal)	-	USB2.0 #0 : A USB2.0 #1 : D USB2.0 #2 : C
Hub to PCI	AD30(internal)	-	-
LPC bridge/IDE/AC97/SMBUS	AD31(internal)	-	B
	-	-	A,B
Internal MAC	AD24(internal)	-	E
AC Link	-	-	B

Voltage Rails

VDC	Primary DC system power supply (7 to 21V)
VCC_CORE	Core voltage for DOTHAN (1.308-1.068V)
VTT	DOTHAN/ALVISO Processor System Bus(PSB) Termination (1.05V) MCH-M Core Voltage
P0.9V	0.9V switched power rail (off in S3-S5)
P1.2V	1.2V switched power rail (off in S3-S5)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.5V_AUX	1.5V power rail (off in S4-S5)
P1.8V	1.8V switched power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail(off in S4-S5)
P2.5V	2.5V switched power rail (off in S3-S5)
MICOM_P3V	3.3V always on power rail for MICOM
P3.3V	3.3V switched power rail (off in S3-S5)
P3.3V_AUX	3.3V power rail (off in S4-S5)
P5V	5.0V switched power rail (off in S3-S5)
P5V_AUX	5.0V power rail (off in S4-S5)

CPU Core Voltage Table

VID5	VID4	VID3	VID2	VID1	VID0	Voltage	VID5	VID4	VID3	VID2	VID1	VID0	Voltage		
0	0	0	0	0	0	1.708 V	1	0	0	0	0	0	1.196 V	Northwood-B (Interposer B'd)	
0	0	0	0	0	1	1.692 V	1	0	0	0	0	1	1.180 V		
0	0	0	0	1	0	1.676 V	1	0	0	0	1	0	1.164 V		
0	0	0	1	1	0	1.660 V	1	0	0	0	1	1	1.148 V		
0	0	0	1	0	0	1.644 V	1	0	0	1	0	0	1.132 V		
0	0	0	1	0	1	1.628 V	1	0	0	1	0	1	1.116 V		
0	0	0	1	1	0	1.612 V	1	0	0	1	1	0	1.100 V		
0	0	1	1	1	1	1.596 V	1	0	0	1	1	1	1.084 V		
0	0	1	0	0	0	1.580 V	1	0	1	0	0	0	1.068 V		
0	0	1	0	0	1	1.564 V	1	0	1	0	0	1	1.052 V		
0	0	1	0	1	0	1.548 V	1	0	1	0	1	0	1.036 V		
0	0	1	0	1	1	1.532 V	1	0	1	0	1	1	1.020 V		
0	0	1	1	0	0	1.516 V	1	0	1	1	0	0	1.004 V		
0	0	1	1	0	1	1.500 V	1	0	1	1	0	1	0.988 V		
0	0	1	1	1	0	1.484 V	1	0	1	1	1	0	0.972 V		
0	0	1	1	1	1	1.468 V	1	0	1	1	1	1	0.956 V		
0	1	0	0	0	0	1.452 V	1	1	0	0	0	0	0.940 V		
0	1	0	0	0	1	1.436 V	1	1	0	0	0	1	0.924 V		
0	1	0	0	1	0	1.420 V	1	1	0	0	1	0	0.908 V		
0	1	0	0	1	1	1.404 V	1	1	0	0	1	1	0.892 V		
0	1	0	1	0	0	1.388 V	1	1	0	1	0	0	0.876 V		
0	1	0	1	0	1	1.372 V	1	1	0	1	0	1	0.860 V		
Highest Freq.	0	1	0	1	1	1.356 V	1	1	0	1	1	0	0.844 V	Lowest Freq.	
0	1	0	1	1	1	1.340 V	1	1	0	1	1	1	0.828 V		
0	1	1	0	0	0	1.324 V	1	1	1	0	0	0	0.812 V		
0	1	1	0	0	1	1.308 V	1	1	1	0	0	1	0.796 V		
0	1	1	0	1	0	1.292 V	1	1	1	0	1	0	0.780 V		
0	1	1	0	1	1	1.276 V	1	1	1	0	1	1	0.764 V		
0	1	1	1	0	0	1.260 V	1	1	1	1	0	0	0.748 V		Deeper Sleep
0	1	1	1	0	1	1.244 V	1	1	1	0	1	0	0.732 V		
0	1	1	1	1	0	1.228 V	1	1	1	1	1	0	0.716 V		
0	1	1	1	1	1	1.212 V	1	1	1	1	1	1	0.700 V		

IC / SMB Address

Devices	Address	Hex	Bus
ICH6	Master	-	SMBUS Master
EMC6N300(CPU Thermal Sensor)	1001 110X	9Ch	Thermal Sensor
SODIMM0	1010 0000	A0h	-
SODIMM1	1010 001X	A2h	-
CK-408 (Clock Generator)	1101 001X	D2h	Clock, Unused Clock Output Disable

USB PORT Assign

PORT NUMBER	ASSIGNED TO
0	SYSTEM PORT A
1,2	SYSTEM PORT B
3	BLUETOOTH
4	FINGER PRINT
	OPTION OPTION

System Power States

- CHP3_SLP5* S1, Powered-On-Suspend(POS) : In this state, all clocks(except the 32.768KHz clock) are stopped. The system context is maintained in system DRAM. Power is maintained to PCI, the CPU, memory controller, memory, and all other critical subsystems. Note that this state does not preclude power being removed from non-essential devices, such as disk drives. During this state, CPU can be selected for either Deep Sleep or Deeper Sleep.
- In Deeper Sleep, CPU voltage reduced in this state to reduce the leakage power.
- CHP3_SLP3* S3, Suspend-To-RAM(STR) : The system context is maintained in system DRAM, but power is shut off to non-critical circuits. Memory is retained, and refreshes continue. All clocks stop except RTC clock.
- CHP3_SLP4* S4, Suspend-To-Disk(STD) : The Context of the system is maintained on the disk. All power is then shut off to the system except for the logic required to resume. Externally appears same as S5, but may have different wake events.
- CHP3_SLP5* S5, Soft Off(SOFF) : System context is not maintained. All power is shut off except for the logic required to restart. A full boot is required when waking.

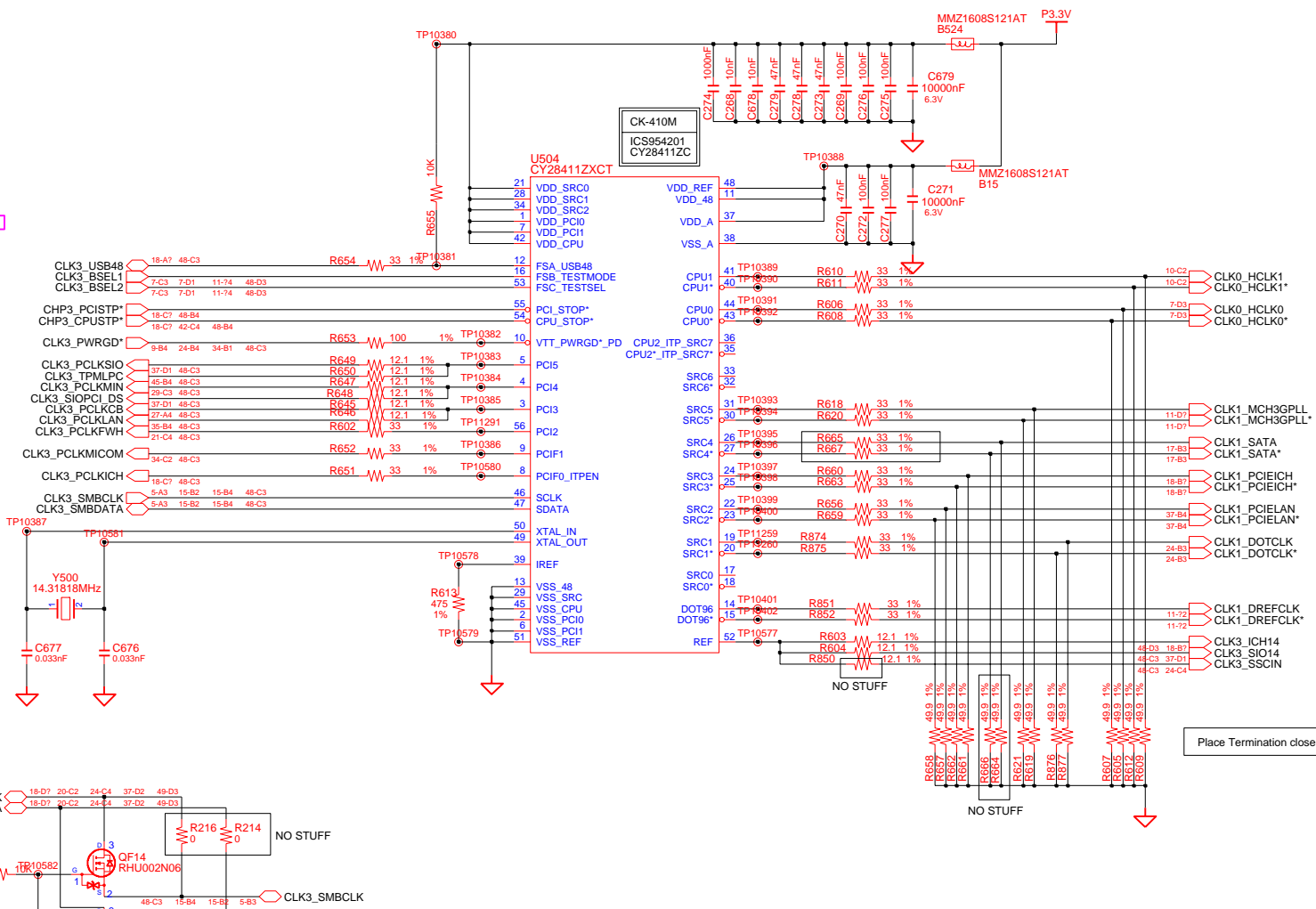
REVISION HISTORY

See rev notes in the changes file for more information.

DRAW	IM, KI	DATE	11/5/2004	TITLE	CYGNUS C MAIN BOARD INFORMATION	SAMSUNG ELECTRONICS
CHECK	BIN, KK	DEV. STEP	PR			
APPROVAL	KIM, DW	REV	1.0			
MODULE CODE		LAST EDIT	November 5, 2004 8:27:10 PM			
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FSA	FSB	FSC	HOST CLK
BSEL2	BSEL1	BSEL0	
0	0	0	266 MHz
0	0	1	333 MHz
0	1	0	200 MHz
0	1	1	400 MHz
1	0	0	133 MHz
1	0	1	100 MHz
1	1	0	166 MHz
1	1	1	RSVD

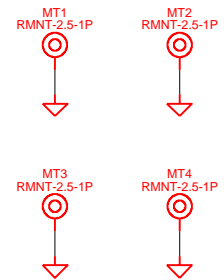
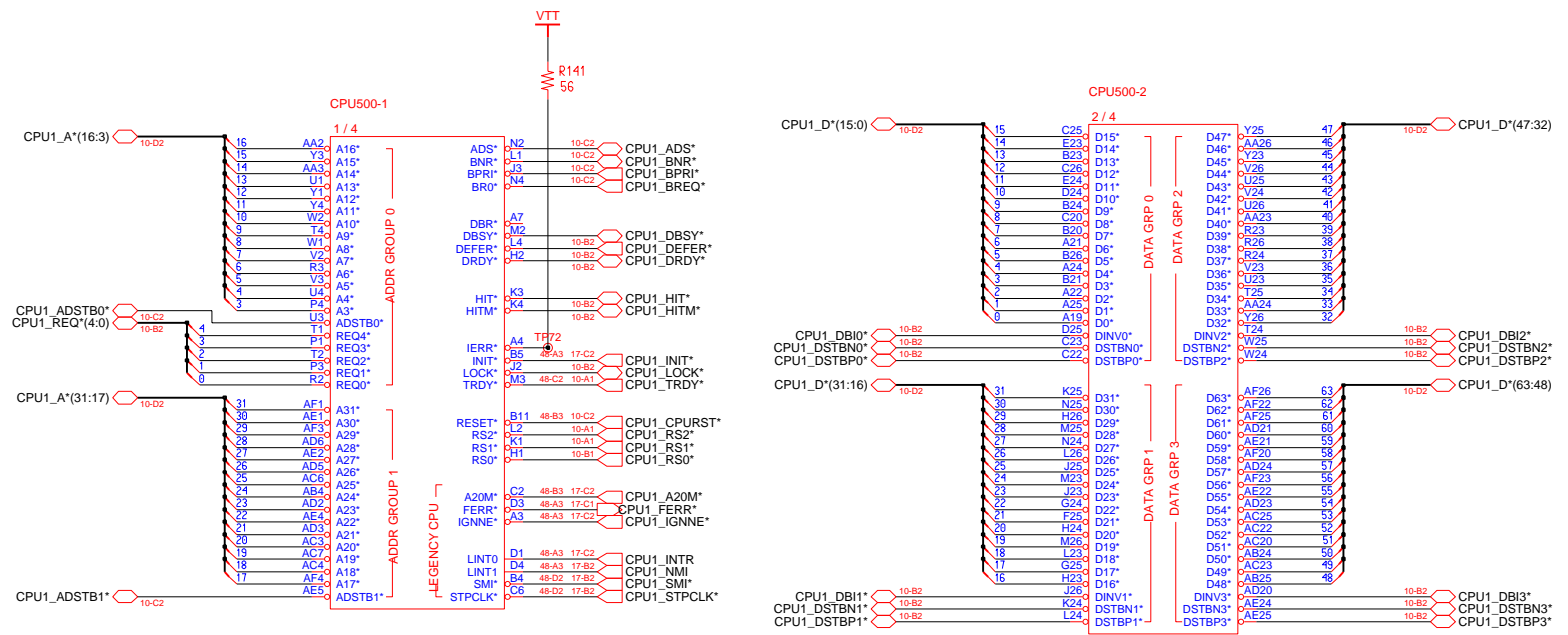


Place 14.318MHz within 500mils of CK-410M

Place Termination close to CK-410M

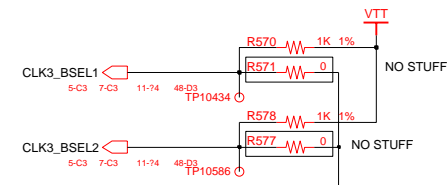
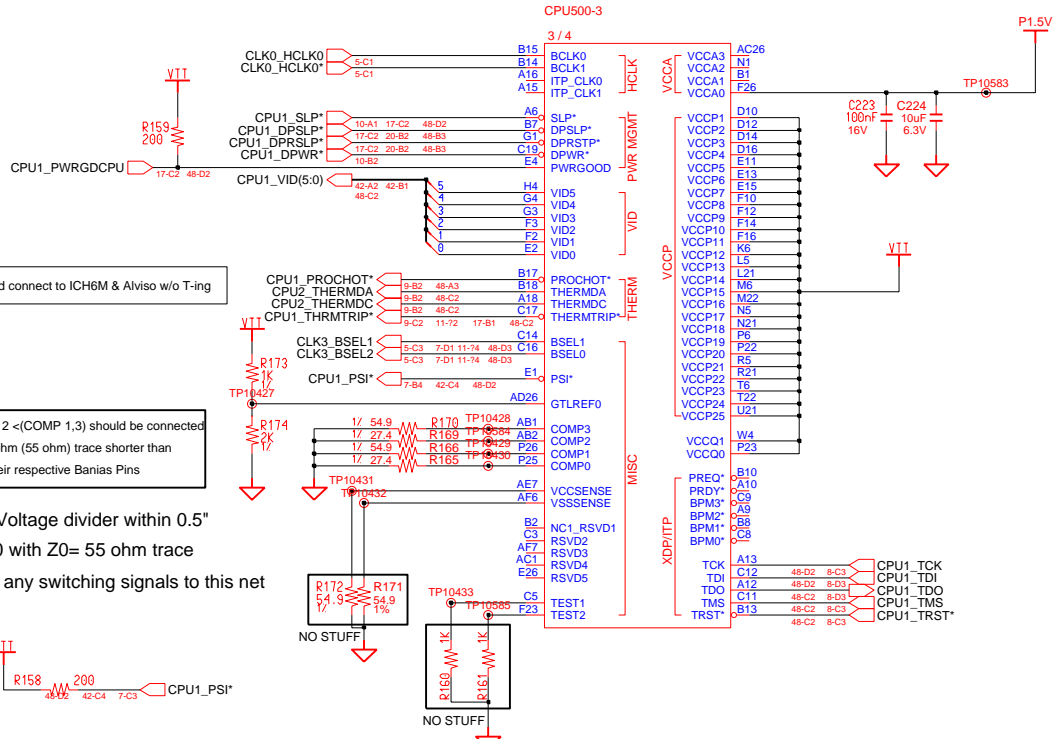
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CHECK	BIN, KK	DEV. STEP	PR	REV	1.0	
APPROVAL	KIM, DW	LAST EDIT	November 5, 2004 8:27:10 PM	PAGE	5	OF 49
MODULE CODE						PART NO. BA41-00451A

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DRAW	IM, KI	DATE	11/5/2004	TITLE	CYGNUS C MAIN DOTHAN CPU (1/3)	SAMSUNG ELECTRONICS
CHECK	BIN, KK	DEV. STEP	PR	PART NO.		
APPROVAL	KIM, DW	REV	1.0	BA41-00451A		
MODULE CODE		LAST EDIT	November 5, 2004 8:27:10 PM	PAGE 6 OF 49		

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THERTRIP* should connect to ICH6M & Alviso w/o T-ing

COMP 0, 2 <(COMP 1,3) should be connected
 Z0=27.4 ohm (55 ohm) trace shorter than
 1/2" to their respective Banias Pins

GTLREF : Keep the Voltage divider within 0.5"
 of the First GTLREF0 with Z0= 55 ohm trace
 Minimize coupling of any switching signals to this net

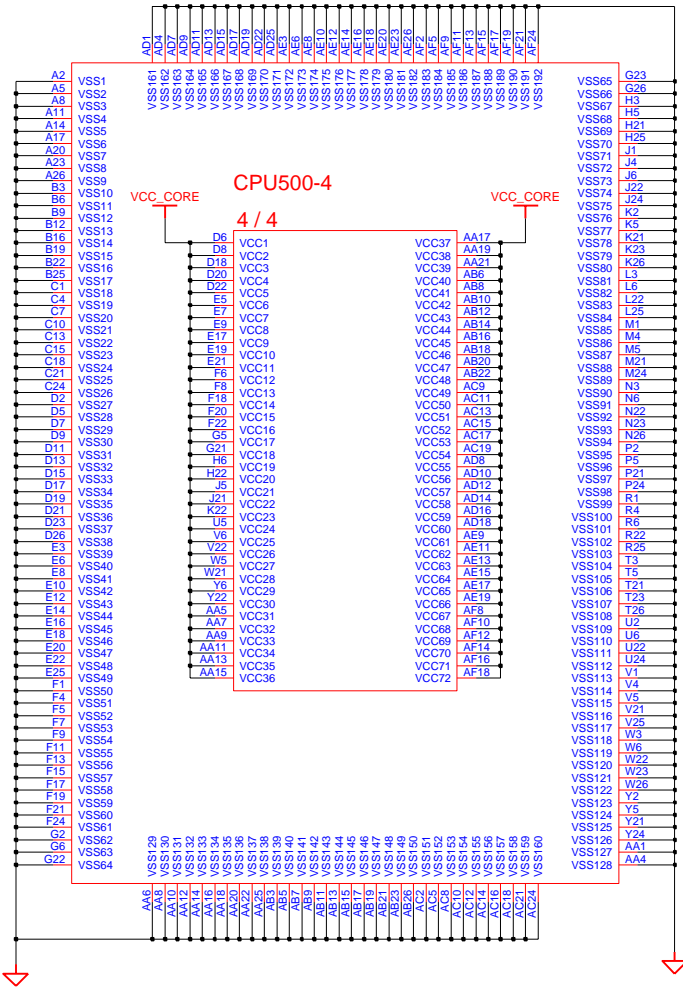
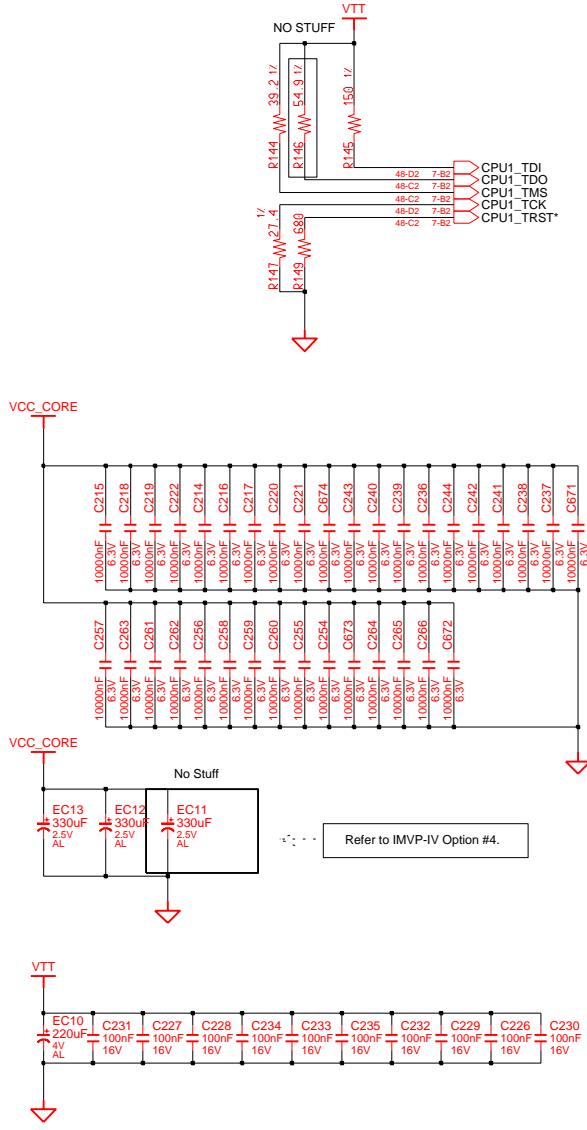
CPU Core Voltage Table

VID(5:0)	Voltage	VID(5:0)	Voltage
0 0 0 0 0	1.708 V	1 0 0 0 0	1.196 V
0 0 0 0 1	1.692 V	1 0 0 0 1	1.180 V
0 0 0 1 0	1.676 V	1 0 0 1 0	1.164 V
0 0 0 1 1	1.660 V	1 0 0 1 1	1.148 V
0 0 1 0 0	1.644 V	1 0 1 0 0	1.132 V
0 0 1 0 1	1.628 V	1 0 1 0 1	1.116 V
0 0 1 1 0	1.612 V	1 0 1 1 0	1.100 V
0 0 1 1 1	1.596 V	1 0 1 1 1	1.084 V
0 1 0 0 0	1.580 V	1 1 0 0 0	1.068 V
0 1 0 0 1	1.564 V	1 1 0 0 1	1.052 V
0 1 0 1 0	1.548 V	1 1 0 1 0	1.036 V
0 1 0 1 1	1.532 V	1 1 0 1 1	1.020 V
0 1 1 0 0	1.516 V	1 1 1 0 0	1.004 V
0 1 1 0 1	1.500 V	1 1 1 0 1	0.988 V
0 1 1 1 0	1.484 V	1 1 1 1 0	0.972 V
0 1 1 1 1	1.468 V	1 1 1 1 1	0.956 V
0 1 0 0 0	1.452 V	1 1 0 0 0	0.940 V
0 1 0 0 1	1.436 V	1 1 0 0 1	0.924 V
0 1 0 1 0	1.420 V	1 1 0 1 0	0.908 V
0 1 0 1 1	1.404 V	1 1 0 1 1	0.892 V
0 1 1 0 0	1.388 V	1 1 1 0 0	0.876 V
0 1 1 0 1	1.372 V	1 1 1 0 1	0.860 V
0 1 1 1 0	1.356 V	1 1 1 1 0	0.844 V
0 1 1 1 1	1.340 V	1 1 1 1 1	0.828 V
0 1 0 0 0	1.324 V	1 1 0 0 0	0.812 V
0 1 0 0 1	1.308 V	1 1 0 0 1	0.796 V
0 1 0 1 0	1.292 V	1 1 0 1 0	0.780 V
0 1 0 1 1	1.276 V	1 1 0 1 1	0.764 V
0 1 1 0 0	1.260 V	1 1 1 0 0	0.748 V
0 1 1 0 1	1.244 V	1 1 1 0 1	0.732 V
0 1 1 1 0	1.228 V	1 1 1 1 0	0.716 V
0 1 1 1 1	1.212 V	1 1 1 1 1	0.700 V

Highest Freq. of Dothan400(1.8GHz)
 * Highest Freq. of Dothan533(?? GHz : TBD)

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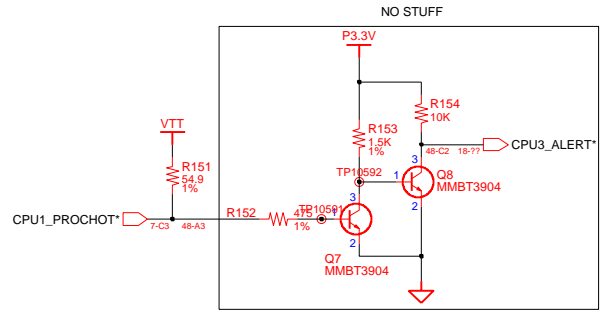
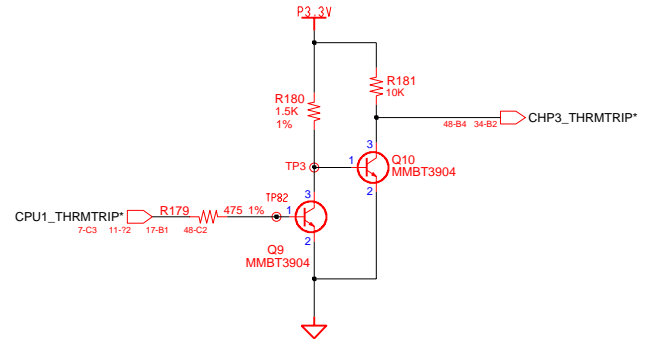
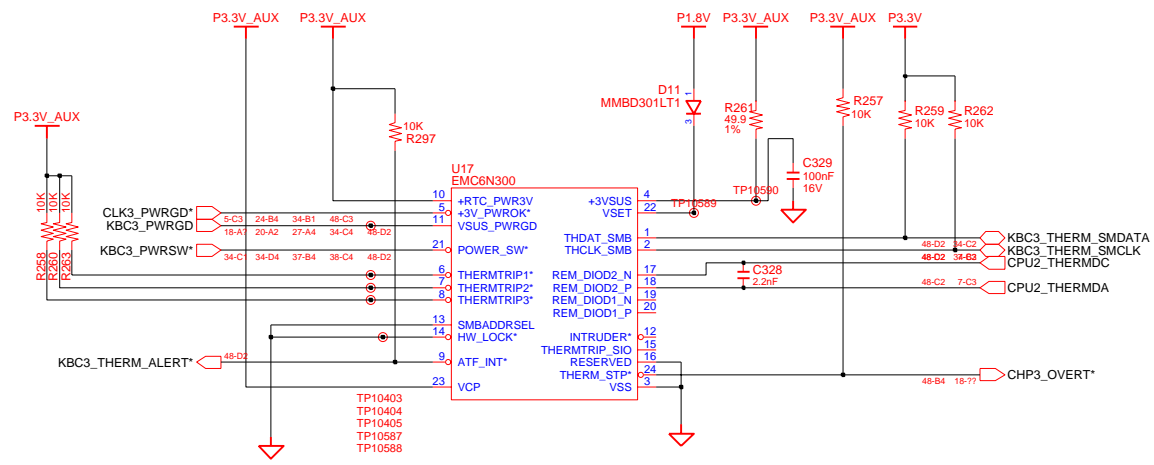
Refer to Sonoma Platform Design Guide(4.6.1.4)



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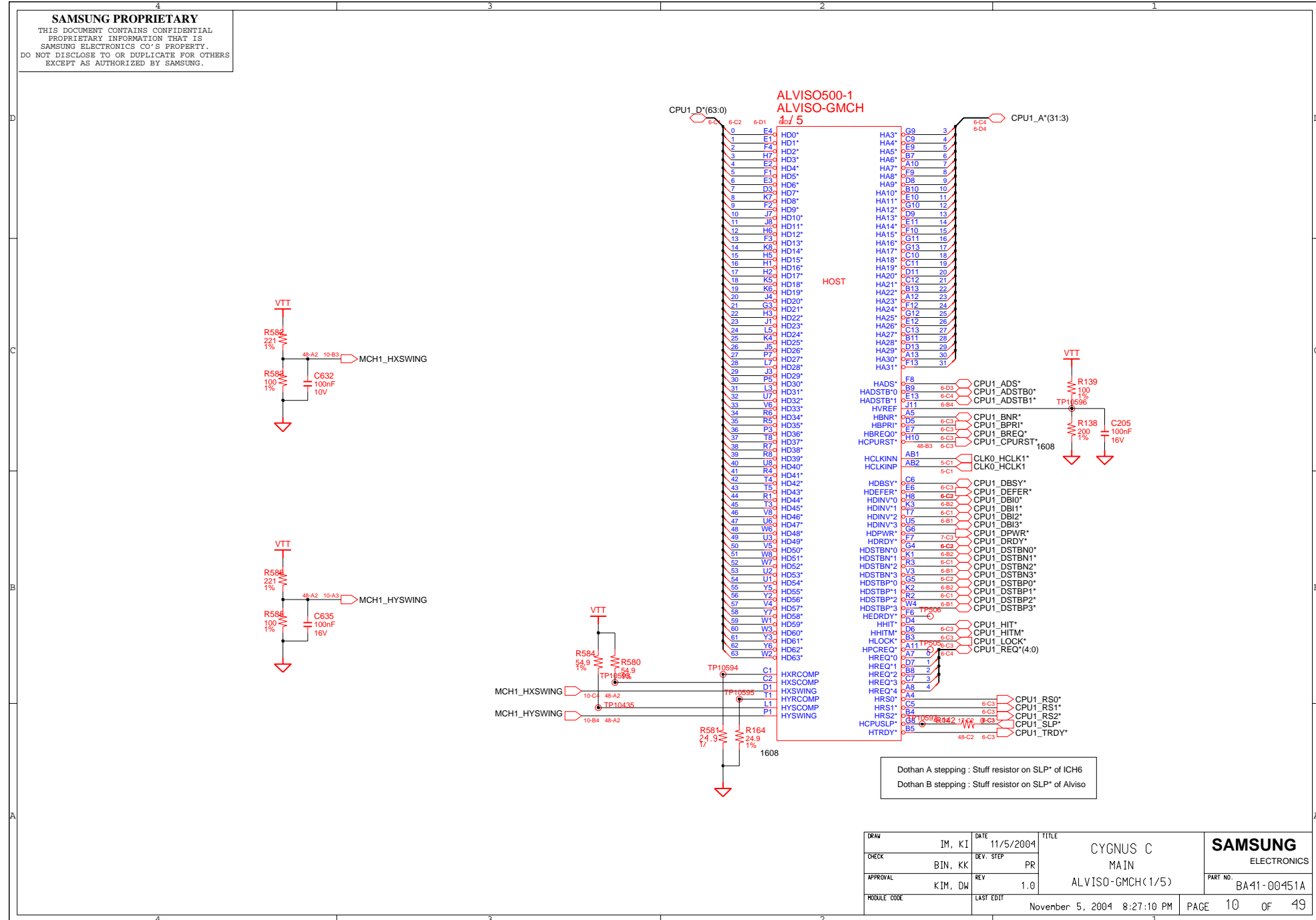
- Refer To Thermal Sensor Layout Guidelines.**
- Place the Thermal Sensor close to a remote diode.
 - Keep traces away from high voltage (+12V bus)
 - Keep traces away from fast data buses and CRT signal.
 - Use recommended trace widths and spacings (10mil)
 - Place a ground plane under the traces.
 - Use guard traces flanking DXP and DXN and connecting to GND

CPU / DDR Thermal Sensor



DRAW	IM, KI	DATE	11/5/2004	TITLE	CYGNUS C MAIN	SAMSUNG ELECTRONICS
CHECK	BIN, KK	DEV. STEP	PR	THERMAL SENSOR/FAN CONTRL		
APPROVAL	KIM, DW	REV	1.0	PART NO. BA41-00451A		PAGE 9 OF 49
MODULE CODE		LAST EDIT	November 5, 2004 8:27:10 PM			

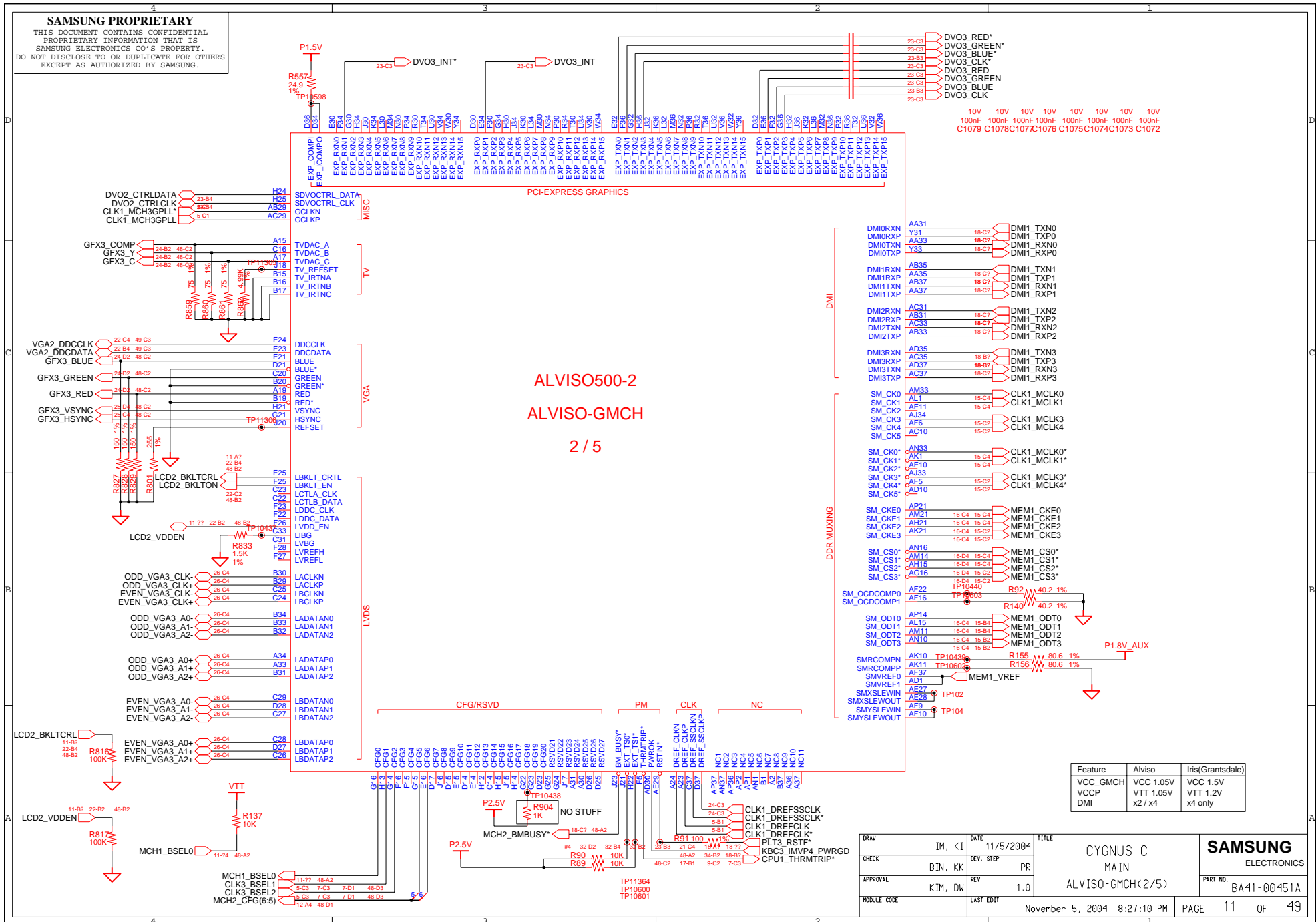
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CHECK	BIN, KK	DEV. STEP	PR	ALVISO-GMCH(1/5)		
APPROVAL	KIM, DW	REV	1.0	November 5, 2004 8:27:10 PM		PART NO. BA41-00451A
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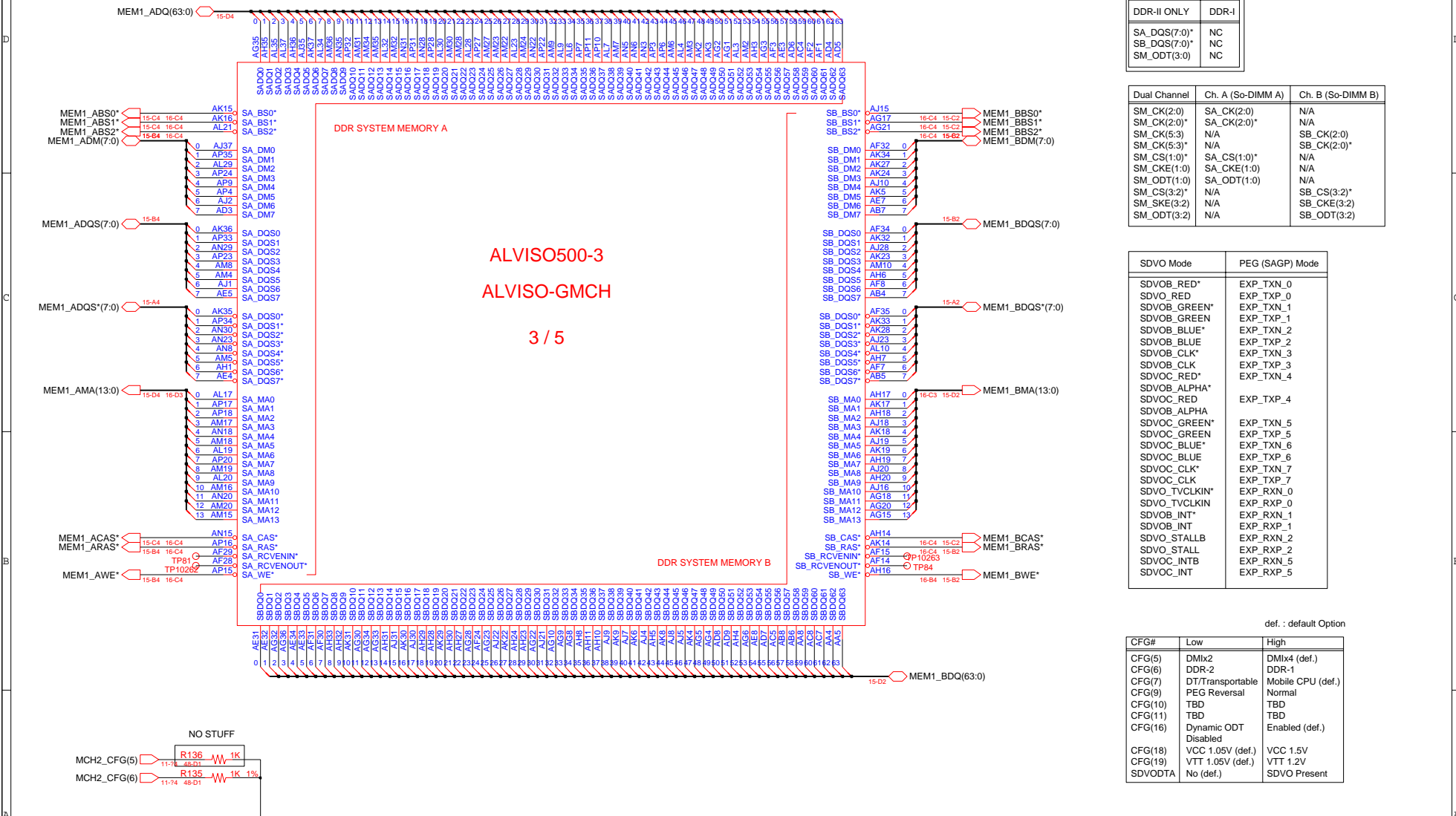


**ALVISO500-2
ALVISO-GMCH
2 / 5**

Feature	Alviso	Iris(Grantsdale)
VCC_GMCH	VCC 1.05V	VCC 1.5V
VCCP	VTT 1.05V	VTT 1.2V
DMI	x2 / x4	x4 only

DRAW	IM, KI	DATE	11/5/2004	TITLE	CYGNUS C	SAMSUNG ELECTRONICS
CHECK	BIN, KK	DEV. STEP	PR		MAIN	
APPROVAL	KIM, DW	REV	1.0		ALVISO-GMCH(2/5)	PART NO. BA41-00451A
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DDR-II ONLY	DDR-I
SA_DQS(7:0)*	NC
SB_DQS(7:0)*	NC
SM_ODT(3:0)	NC

Dual Channel	Ch. A (So-DIMM A)	Ch. B (So-DIMM B)
SM_CK(2:0)	SA_CK(2:0)	N/A
SM_CK(2:0)*	SA_CK(2:0)*	N/A
SM_CK(5:3)	N/A	SB_CK(2:0)
SM_CK(5:3)*	N/A	SB_CK(2:0)*
SM_CS(1:0)*	SA_CS(1:0)*	N/A
SM_CKE(1:0)	SA_CKE(1:0)	N/A
SM_ODT(1:0)	SA_ODT(1:0)	N/A
SM_CS(3:2)*	N/A	SB_CS(3:2)*
SM_SKE(3:2)	N/A	SB_CKE(3:2)
SM_ODT(3:2)	N/A	SB_ODT(3:2)

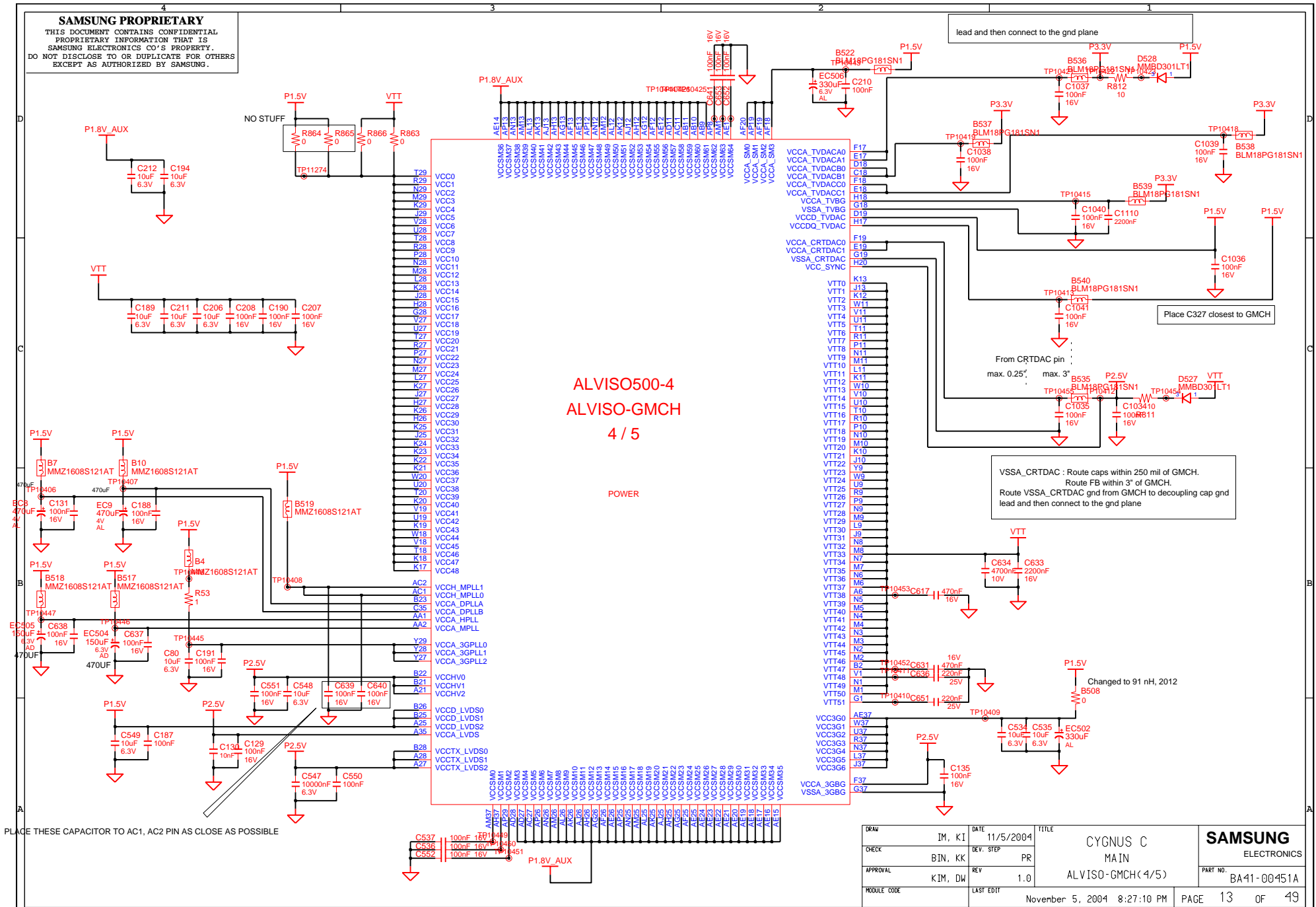
SDVO Mode	PEG (SAGP) Mode
SDVOB_RED*	EXP_TXN_0
SDVO_RED	EXP_TXP_0
SDVOB_GREEN*	EXP_TXN_1
SDVOB_GREEN	EXP_TXP_1
SDVOB_BLUE*	EXP_TXN_2
SDVOB_BLUE	EXP_TXP_2
SDVOB_CLK*	EXP_TXN_3
SDVOB_CLK	EXP_TXP_3
SDVOC_RED*	EXP_TXN_4
SDVOB_ALPHA*	EXP_TXN_5
SDVOC_RED	EXP_TXP_4
SDVOB_ALPHA	EXP_TXN_6
SDVOC_GREEN*	EXP_TXN_7
SDVOC_GREEN	EXP_TXP_5
SDVOC_BLUE*	EXP_TXN_8
SDVOC_BLUE	EXP_TXP_6
SDVOC_CLK*	EXP_TXN_9
SDVOC_CLK	EXP_TXP_7
SDVO_TVCLKIN*	EXP_RXN_0
SDVO_TVCLKIN	EXP_RXP_0
SDVOB_INT*	EXP_RXN_1
SDVOB_INT	EXP_RXP_1
SDVO_STALLB	EXP_RXN_2
SDVO_STALL	EXP_RXP_2
SDVOC_INTB	EXP_RXN_5
SDVOC_INT	EXP_RXP_5

def. : default Option

CFG#	Low	High
CFG(5)	DMix2	DMix4 (def.)
CFG(6)	DDR-2	DDR-1
CFG(7)	DT/Transportable	Mobile CPU (def.)
CFG(9)	PEG Reversal	Normal
CFG(10)	TBD	TBD
CFG(11)	TBD	TBD
CFG(16)	Dynamic ODT Disabled	Enabled (def.)
CFG(18)	VCC 1.05V (def.)	VCC 1.5V
CFG(19)	VTT 1.05V (def.)	VTT 1.2V
SDVODTA	No (def.)	SDVO Present

DRAW	IM, KI	DATE	11/5/2004	TITLE	CYGNUS C	SAMSUNG ELECTRONICS
CHECK	BIN, KK	DEV. STEP	PR	MAIN		
APPROVAL	KIM, DW	REV	1.0	ALVISO-GMCH(3/5)		PART NO. BA41-00451A
MODULE CODE		LAST EDIT	November 5, 2004 8:27:10 PM	PAGE	12	OF 49

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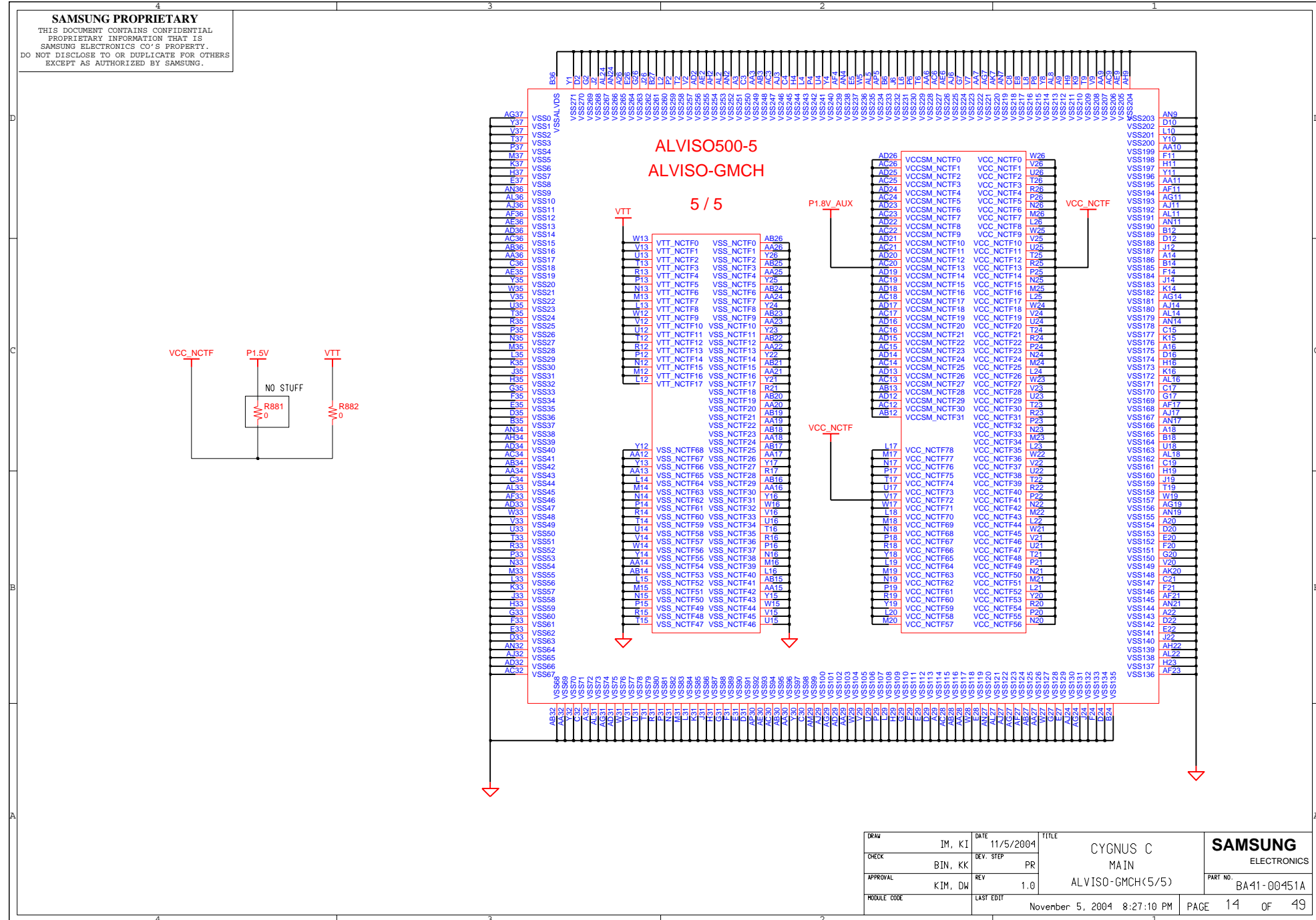


**ALVISO500-4
 ALVISO-GMCH
 4 / 5
 POWER**

PLACE THESE CAPACITOR TO AC1, AC2 PIN AS CLOSE AS POSSIBLE

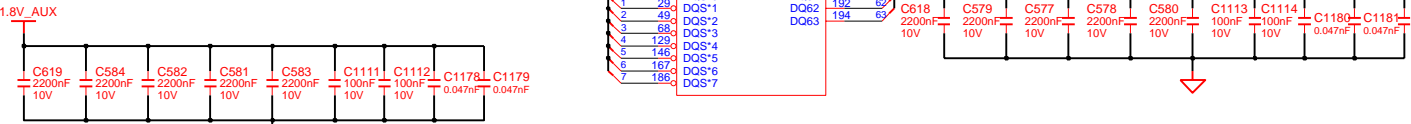
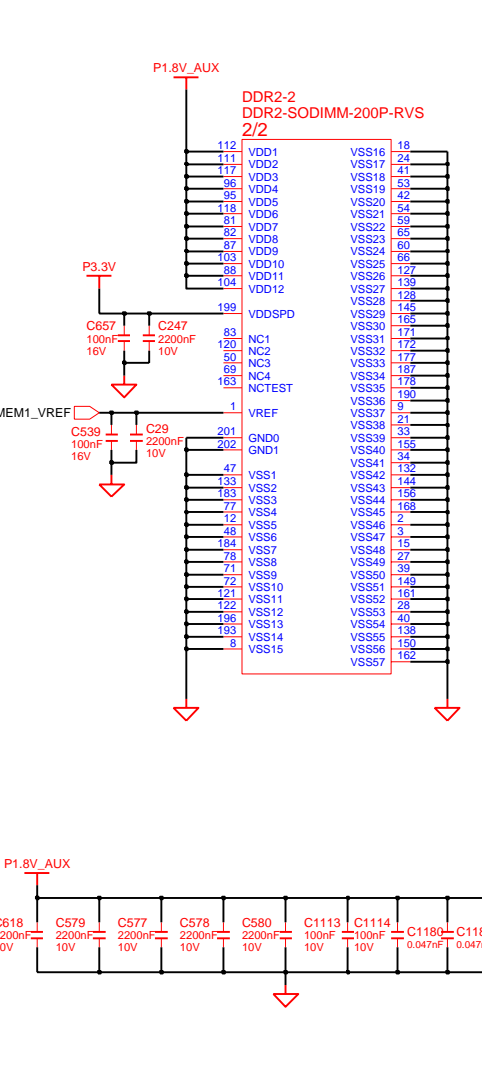
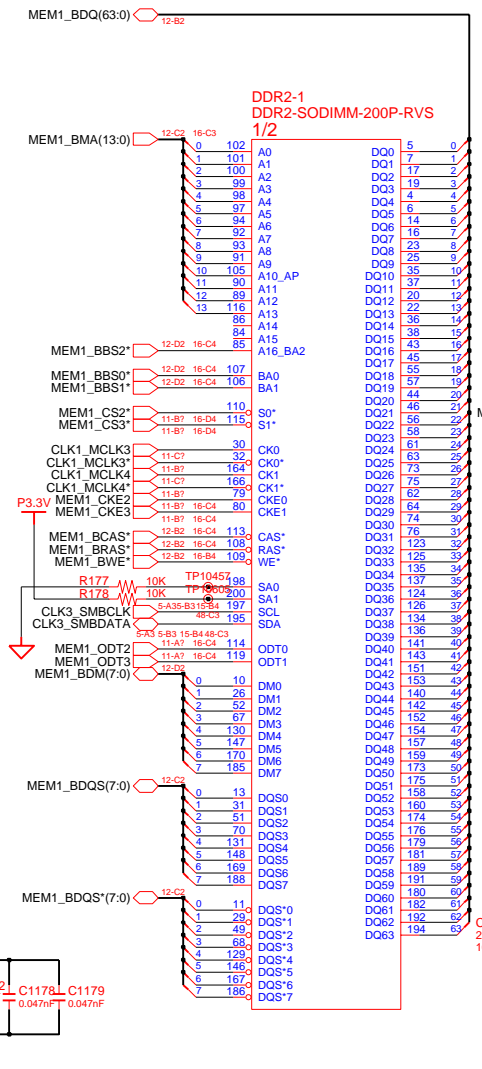
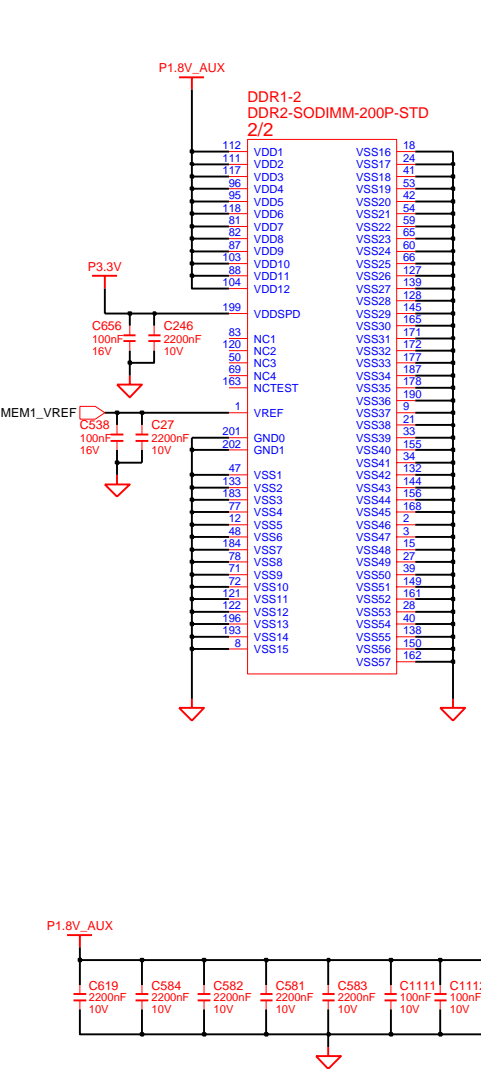
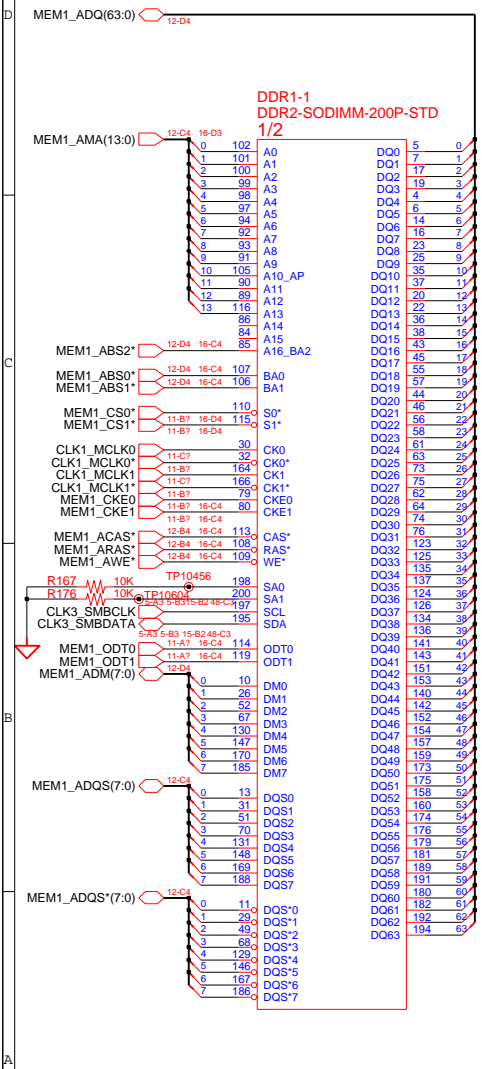
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CHECK	BIN, KK	DEV. STEP	PR	ALVISO-GMCH(4/5)		
APPROVAL	KIM, DW	REV	1.0	November 5, 2004 8:27:10 PM		PAGE 13 OF 49
MODULE CODE	LAST EDIT					

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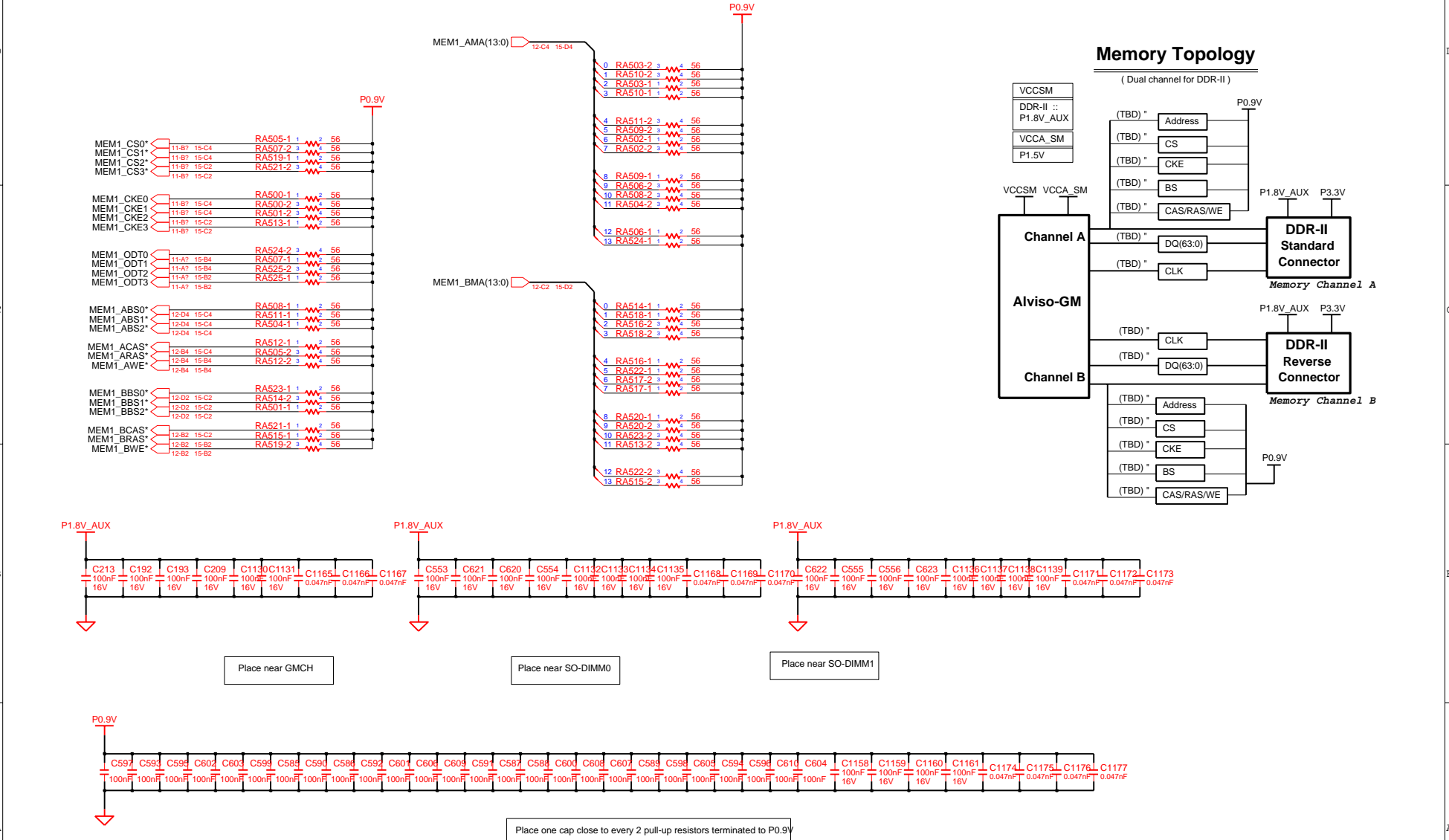
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CHECK	BIN, KK	DEV. STEP	PR			
APPROVAL	KIM, DW	REV	1.0			
MODULE CODE		LAST EDIT	November 5, 2004 8:27:10 PM	PAGE 14 OF 49		

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DRAW	IM, KI	DATE	11/5/2004	TITLE	CYGNUS C	SAMSUNG ELECTRONICS
CHECK	BIN, KK	DEV. STEP	PR	MAIN		
APPROVAL	KIM, DW	REV	1.0	DDR - SODIMM		PART NO. BA41-00451A
MODULE CODE		LAST EDIT	November 5, 2004 8:27:10 PM	PAGE	15	OF 49

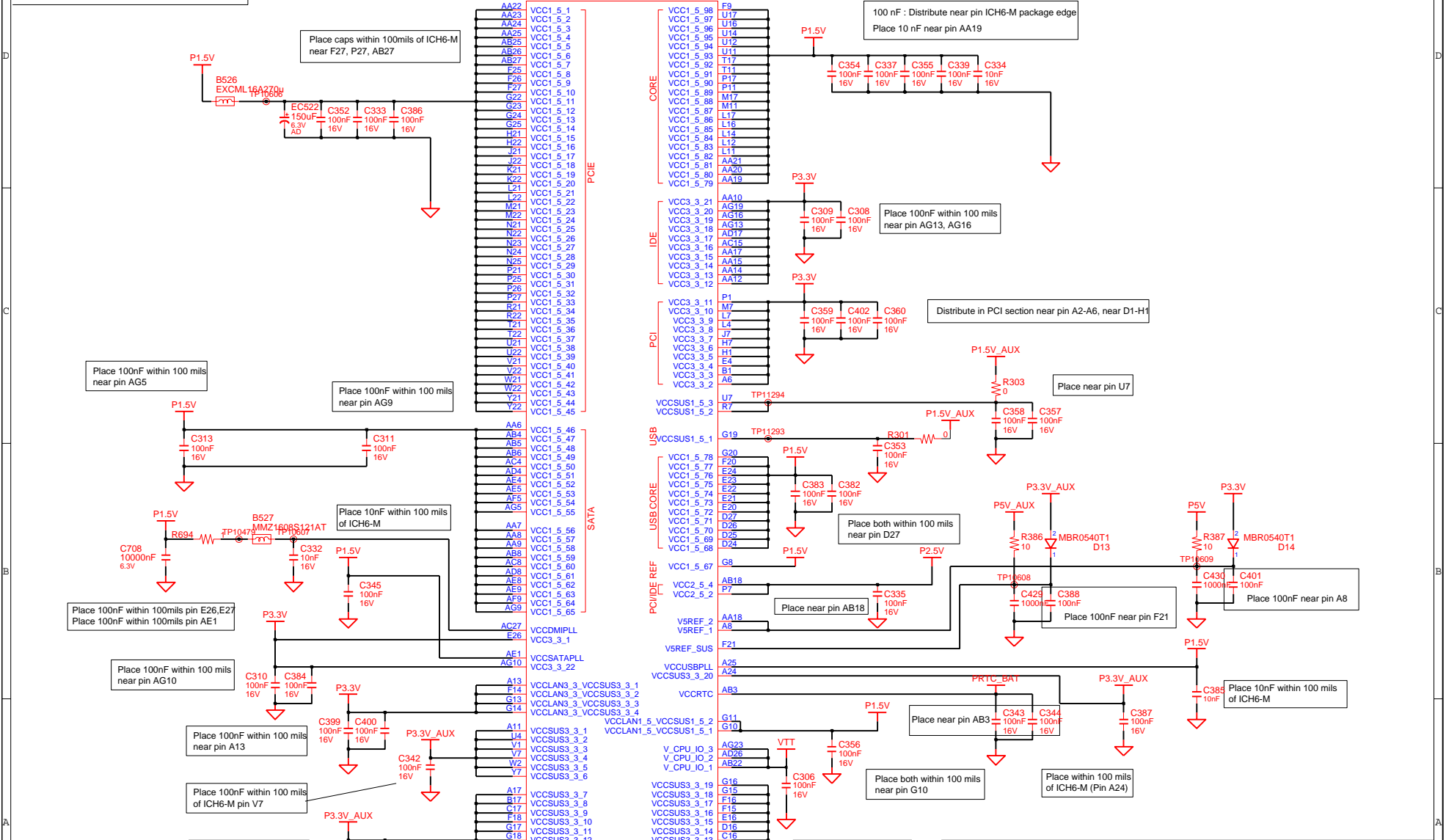
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DRAW	IM, KI	DATE	11/5/2004	TITLE	CYGNUS C	SAMSUNG ELECTRONICS
CHECK	BIN, KK	DEV. STEP	PR		MAIN	
APPROVAL	KIM, DW	REV	1.0		DDR - TERMINATION	PART NO. BA41-00451A
MODULE CODE		LAST EDIT			November 5, 2004 8:27:10 PM	PAGE 16 OF 49

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**U507-4
 82801FBM
 4 / 5**



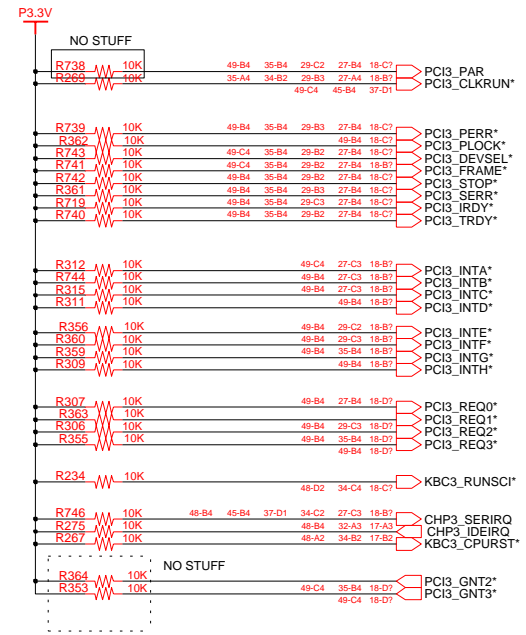
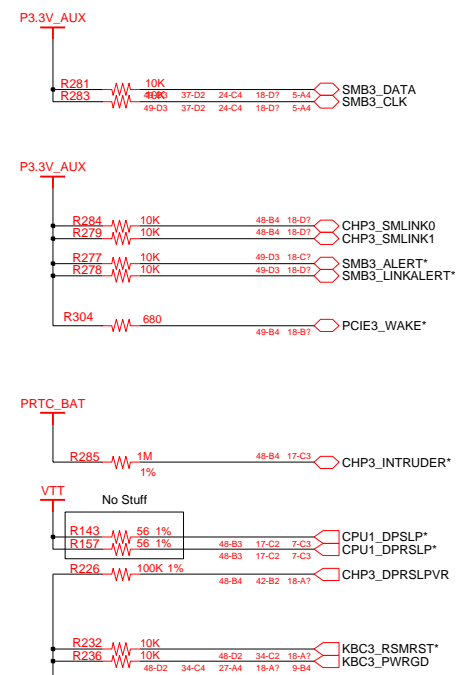
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ICH6-m Strapping Options

	Function	Default
CHP3_SPKR	No Reboot	No Stuff
CHP3_BIOSWP*	Boot BIOS	No Stuff
PC/PCI_GNTA*	A16 swap override	No Stuff
AC97_SDOUT	Safe Mode	TBD
ECP_DOUT		TBD

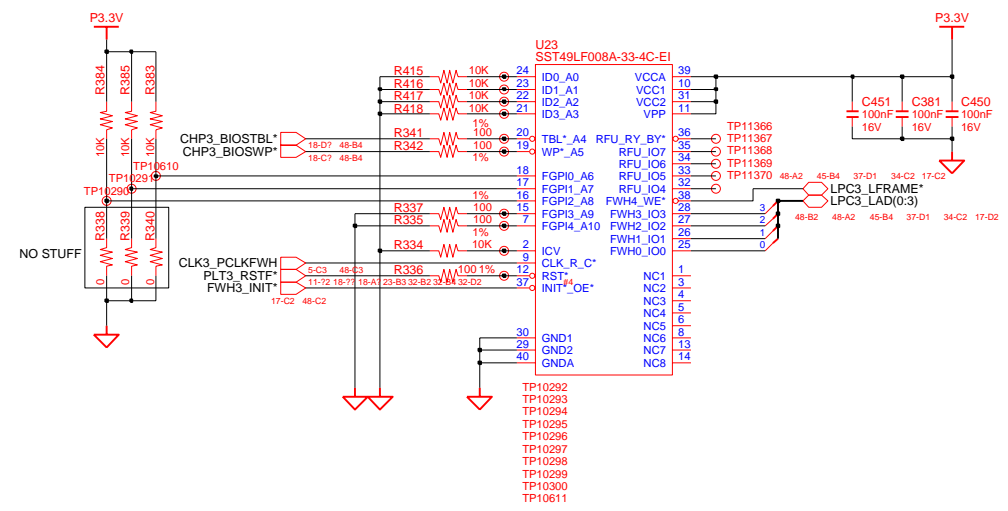
U507-5 82801FBM 5 / 5

AG22	VSS_172	P22
AG20	VSS_171	P16
AG17	VSS_170	P15
AG14	VSS_169	P14
AG12	VSS_168	P13
AG7	VSS_167	P12
AG3	VSS_166	N17
AG1	VSS_165	N16
AF26	VSS_164	N15
AF12	VSS_163	N14
AF10	VSS_162	N13
AF7	VSS_161	N12
AF3	VSS_160	N11
AF1	VSS_159	N7
AE25	VSS_158	N1
AE21	VSS_157	M27
AE12	VSS_156	M26
AE11	VSS_155	M23
AE10	VSS_154	M15
AE7	VSS_153	M18
AE6	VSS_152	M14
AE2	VSS_151	M13
AD24	VSS_150	M12
AD18	VSS_149	M4
AD15	VSS_148	L25
AD10	VSS_147	L24
AD6	VSS_146	L23
AD2	VSS_145	L15
AD1	VSS_144	L13
AC26	VSS_143	K27
AC23	VSS_142	K26
AC22	VSS_141	K7
AC12	VSS_139	K1
AC10	VSS_138	J25
AC6	VSS_137	J23
AC3	VSS_136	J4
AB19	VSS_135	H27
AB9	VSS_134	H23
AB7	VSS_133	H25
AB2	VSS_132	G21
AB1	VSS_131	G22
AA16	VSS_130	G12
AA13	VSS_129	G9
AA11	VSS_128	G1
AA4	VSS_127	F22
Y27	VSS_126	F19
Y26	VSS_125	F17
Y23	VSS_124	F4
Y6	VSS_123	E27
W25	VSS_122	E25
W24	VSS_121	E18
W23	VSS_120	E15
W7	VSS_119	E14
W1	VSS_117	E11
V27	VSS_116	D22
V26	VSS_115	D20
V23	VSS_114	D19
V4	VSS_113	D14
U24	VSS_112	D11
U23	VSS_111	D10
U15	VSS_110	D1
U13	VSS_108	C22
T27	VSS_107	C20
T26	VSS_106	C18
T23	VSS_105	C14
T16	VSS_104	C4
T15	VSS_103	B25
T14	VSS_102	B24
T13	VSS_101	B23
T12	VSS_100	B21
T7	VSS_99	B19
T1	VSS_98	B15
R25	VSS_97	A26
R24	VSS_96	A23
R23	VSS_95	A21
R17	VSS_94	A19
R16	VSS_93	A15
R15	VSS_92	A12
R14	VSS_91	A9
R13	VSS_90	A7
R12	VSS_89	A4
R11	VSS_88	A1
R4	VSS_87	A1



DRAW	IM, KI	DATE	11/5/2004	TITLE	CYGNUS C	SAMSUNG ELECTRONICS
CHECK	BIN, KK	DEV. STEP	PR		MAIN	
APPROVAL	KIM, DW	REV	1.0		ICH6 - M(4/4)	PART NO. BA41-00451A
MODULE CODE		LAST EDIT	November 5, 2004 8:27:10 PM	PAGE	20	OF 49

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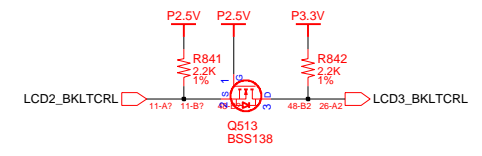
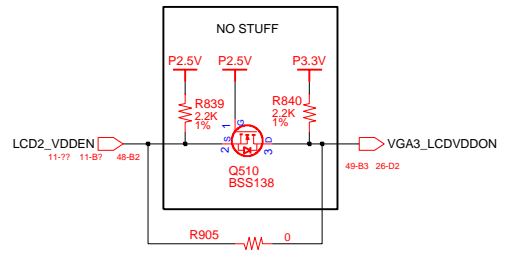
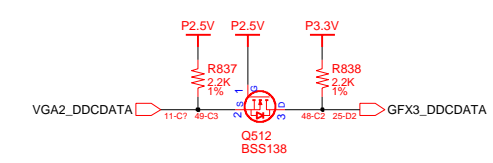
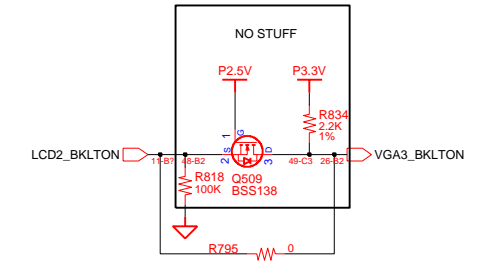
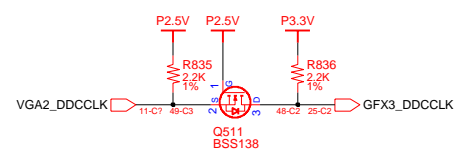


- | | | | |
|----|----------------------------------------------|----|---------------------------------|
| 02 | VERIFY REAL MODE | 66 | CONFIGURE ADVANCE CACHE REG. |
| 03 | DISABLE NMI | 6A | DISPLAY EXTERNAL CACHE SIZE |
| 04 | GET CPU TYPE | 6C | DISPLAY SHADOW MESSAGE |
| 06 | INIT. SYSTEM H/W | 6E | DISPLAY NON-DISPOSABLE SEGMENT |
| 08 | INIT. CHIPSET REG. | 70 | DISPLAY ERROR MESSAGE |
| 09 | SET IN POST FLAG | 72 | CHECK FOR CONFIGURATION ERROR |
| 0A | INIT CPU.REG | 74 | TEST REAL-TIME CLOCK |
| 0B | CPU CACHE ON | 76 | CHECK FOR KEYBOARD ERROR |
| 0C | INIT.CACHE TO POST | 7C | SETUP HARDWARE INTERRUPT VECTOR |
| OE | INIT. I/O VALUE | 7E | TEST COPROCESSER IF PRESENT |
| 0F | ENABLE THE L-BUS IDE | 80 | DISABLE ON-BOARD I/O PORT |
| 10 | INIT. POWER MANAGER | 82 | DETECT AND INSTALL EXT.RS232C |
| 11 | LOAD ALTERNATE REG. | 84 | DETECT AND INSTALL EXT.PARALLEL |
| 13 | PCI BUS MASTER RESET WITH INITIAL POST VALUE | 86 | RE-INIT. ON-BOARD I/O PORT |
| 16 | CHECK CHECKSUM | 88 | INIT. BIOS DATA ROM |
| 18 | 8254 TIMER INIT. | 8A | INIT.EXTENDED BIOS DATA AREA |
| 1A | 8237 DMA CONTROLLER INIT. | 8C | INIT. FDD CONTROLLER |
| 1C | RESET INTERRUPT CONTROLLER | 9A | SHADOW OPTION ROMS |
| 20 | TEST DRAM REFRESH | 9C | SETUP POWER MANAGEMENT |
| 22 | TEST 8742 KEYBOARD CONTROLLER | 9E | ENABLE H/W INTERRUPT |
| 24 | SET ES SEGMENT REG. TO 4GB | A0 | SET TIME OF DAY |
| 26 | ENABLE A20 | A4 | INIT. TYPOMATIC RATE |
| 28 | AUTO SIZING DRAM | A8 | ERASE F2 PROMPT |
| 32 | COMPUTE THE CPU SPEED | AA | SCAN FOR F2 KEY STROKE |
| 34 | TESET CMOS RAM | AC | ENTER SETUP |
| 38 | SHADOW SYSTEM BIOS ROM | AE | CLEAR IN POST FLAG |
| 3A | AUTO SIZING CACHE | B0 | CHECK FOR ERRORS |
| 3C | CONFIGURE ADVANCED CHIPSET REG. | B2 | POST DONE-PREPARE TO BOOT O/S |
| 3D | LOAD ALTER REG. WITH CMOS VALUE | B4 | ONE BEEP |
| 42 | INIT. INTERRUPT VECTOR | B6 | CHECK PASSWORD (OPTION) |
| 44 | INIT. BIOS INTERRUPT | B7 | ACPI INIT |
| 46 | CHECK ROM COPYRIGHT NOTICE | BA | DMI INIT |
| 47 | INIT. I20 SUPPORT IF INSTALLED | BE | CLEAR SCREEN |
| 48 | CHECK VIDEO CONFIGURE AGAINST CMOS | C0 | TRY BOOT WITH INT19 |
| 49 | INIT. PCI BUS AND DEVICE | D0 | INTERRUPT HANDLER ERROR |
| 4A | INIT. ALL VIDEO BIOS ROM | D2 | UNKNOWN INTERRUPT ERROR |
| 4C | SHADOW VIDEO BIOS ROM | D4 | PENDING INTERRUPT ERROR |
| 50 | DISPLAY CPU TYPE AND SPEED | D6 | SHUTDOWN 5 |
| 52 | TEST KEYBOARD | D8 | SHUTDOWN ERROR |
| 54 | SET KEYCLICK IF ENABLED | DA | EXTENDED BLOCK MOVE |
| 56 | ENABLE KEYBOARD | DC | SHUTDOWN 10 |
| 58 | TEST FOR UNEXPECTED INTERRUPTS | 89 | ENABLE NMI |
| 5A | DISPLAY "PRESS SETUP" | 90 | INIT. HDD CONTROLLER |
| 5C | TEST RAM BETWEEN 512K AND 640K | 91 | INIT. LOCAL BUS HDD CONTROLLER |
| 60 | TEST EXTENDED MEMORY | 92 | JUMP TO USER PATCH 2 |
| 62 | TEST EXTENDED MEMORY ADDRESS LINE | 94 | DISABLE A20 ADDRESS LINE |
| 64 | JUMP TO USER PATCH 1 | 96 | CLEAR HUGE ES SEGMENT REG. |
| | | 98 | SEARCH FOR OPTION ROMS |

DRAW	IM, KI	DATE	11/5/2004	TITLE	CYGNUS C MAIN FIRMWARE HUB	SAMSUNG ELECTRONICS
CHECK	BIN, KK	DEV. STEP	PR			
APPROVAL	KIM, DW	REV	1.0			PART NO. BA41-00451A
MODULE CODE		LAST EDIT	November 5, 2004 8:27:10 PM	PAGE	21	OF 49

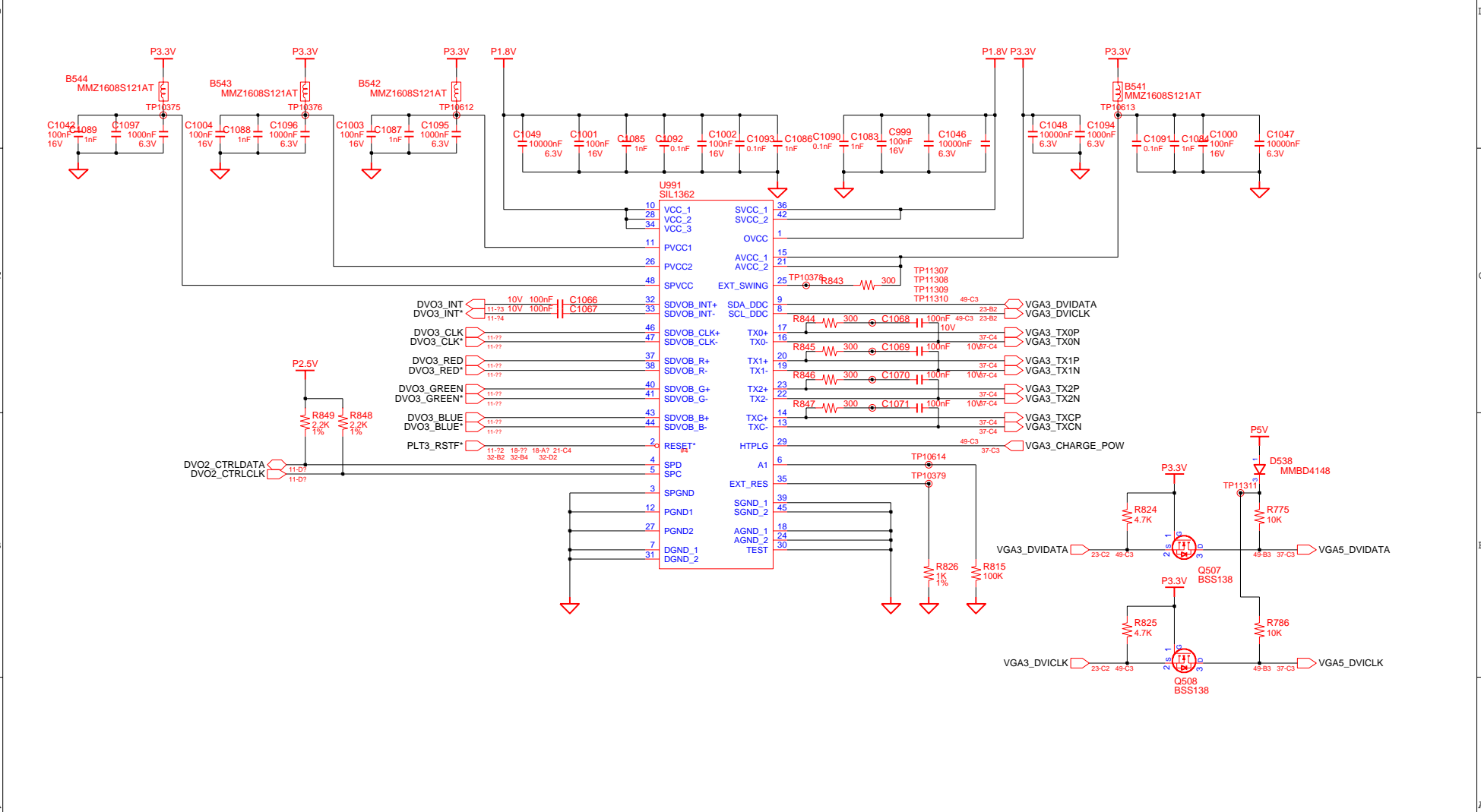
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LVDS Voltage Translation Logic (2.5V -> 3.3V)



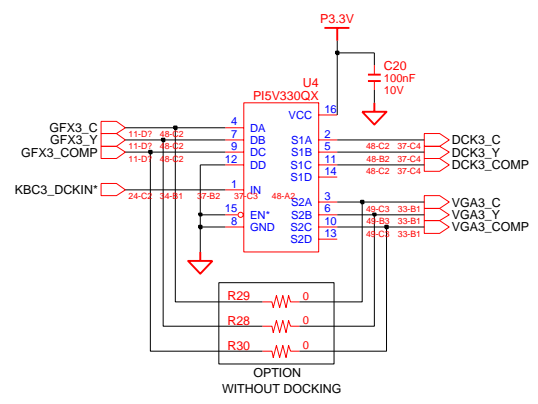
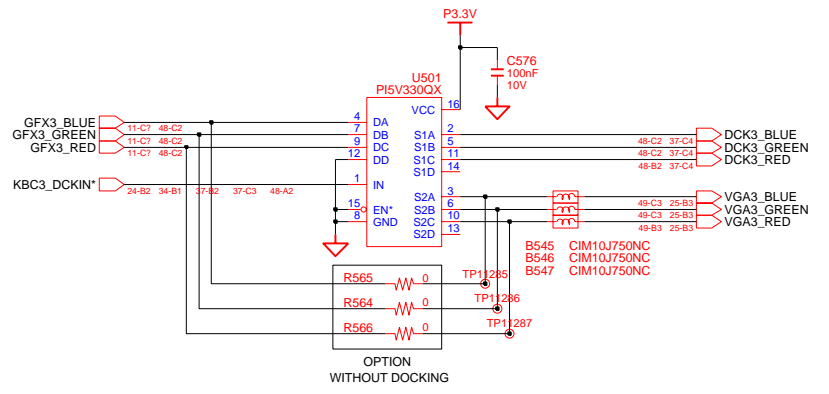
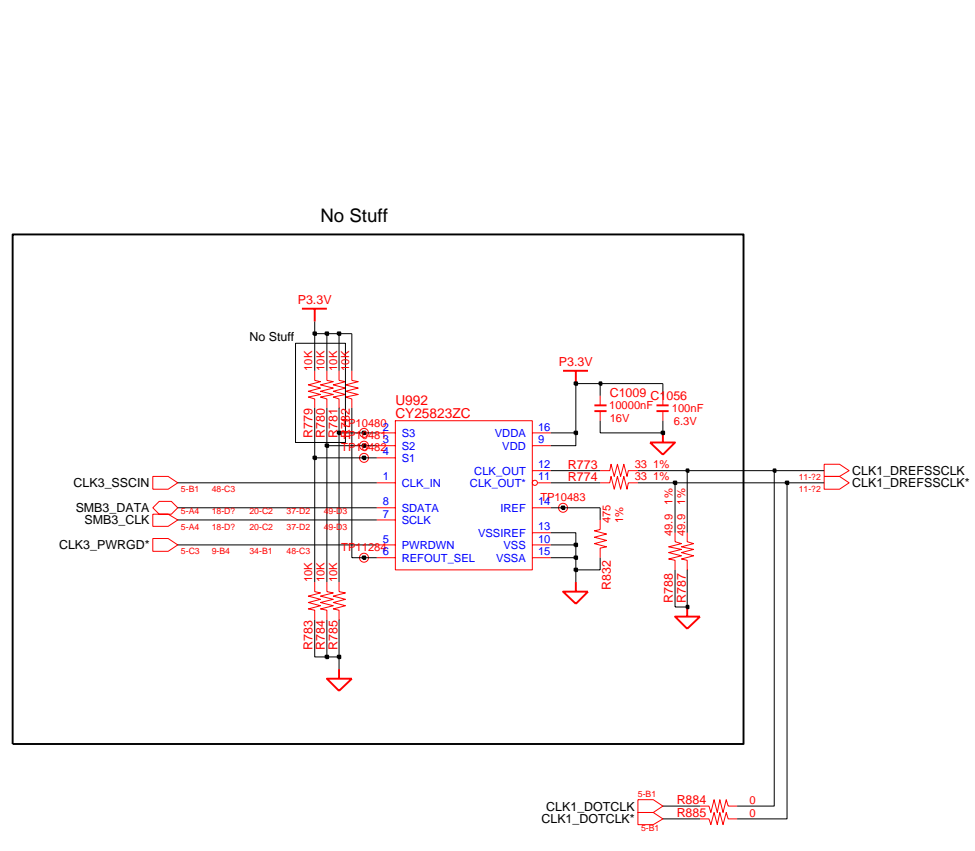
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CHECK	BIN, KK	DEV. STEP	PR		MAIN	
APPROVAL	KIM, DW	REV	1.0	ATI M24 GRAPHIC CONTROL1/4		PART NO. BA41-00451A
MODULE CODE		LAST EDIT	November 5, 2004 8:27:10 PM		PAGE	22 OF 49

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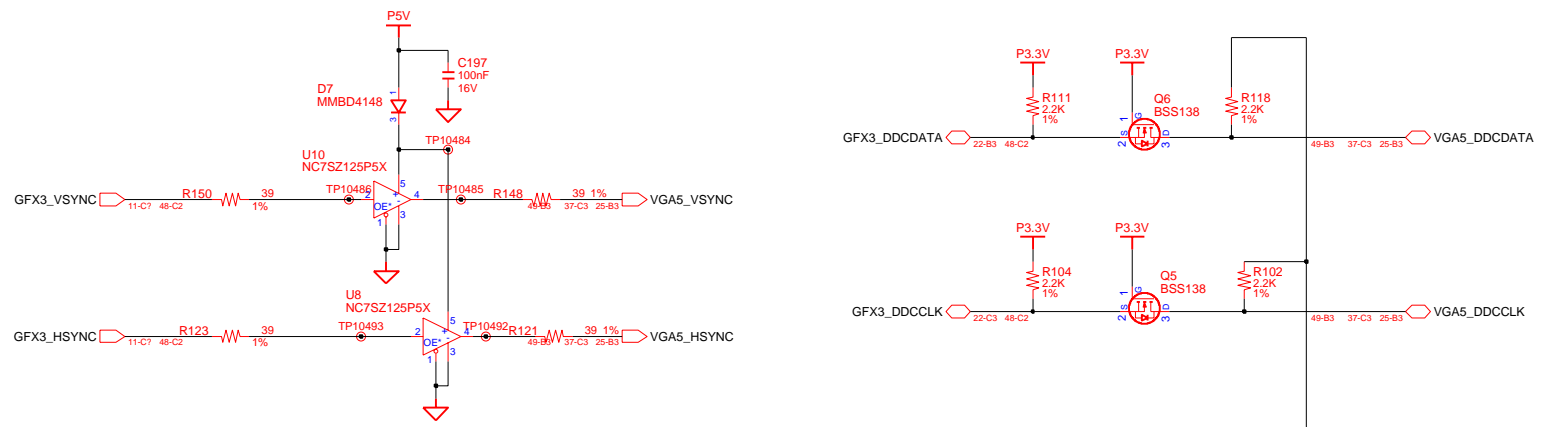
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CHECK	BIN, KK	DEV. STEP	PR			
APPROVAL	KIM, DW	REV	1.0			
MODULE CODE		LAST EDIT	November 5, 2004 8:27:10 PM	PAGE	23 OF 49	

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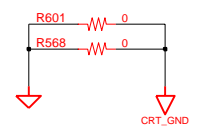
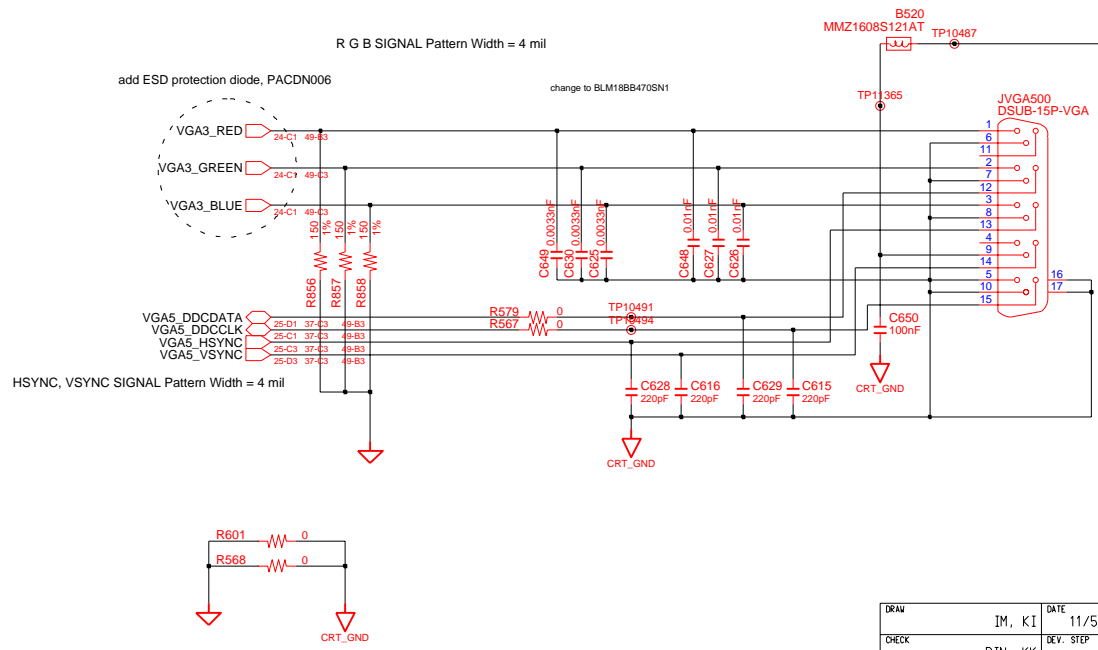


DRAW	IM, KI	DATE	11/5/2004	TITLE	CYGNUS C	PART NO.	SAMSUNG ELECTRONICS
CHECK	BIN, KK	DEV. STEP	PR		MAIN		
APPROVAL	KIM, DW	REV	1.0	ATI M24 GRAPHIC CONTROL3/4		BA41-00451A	PAGE 24 OF 49
MODULE CODE		LAST EDIT		November 5, 2004 8:27:10 PM			

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CRT

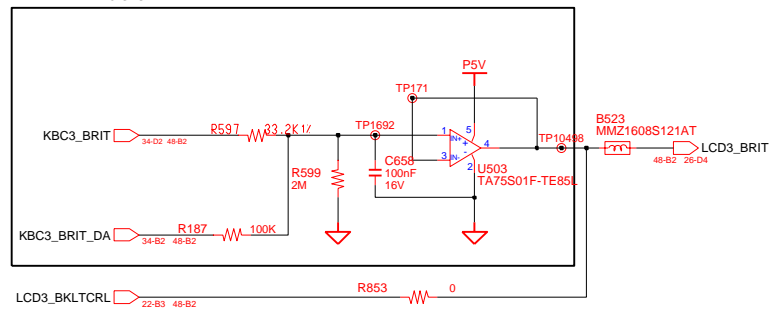
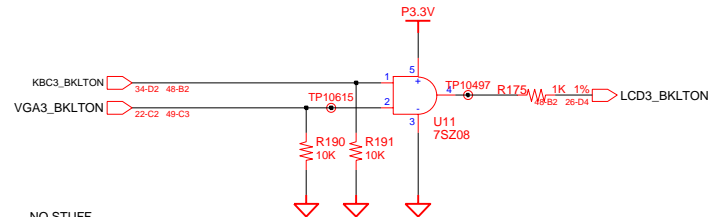
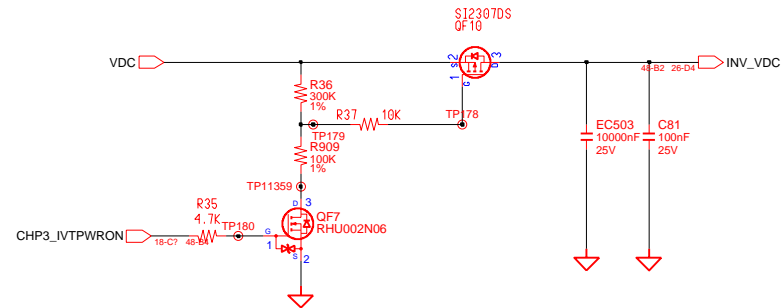
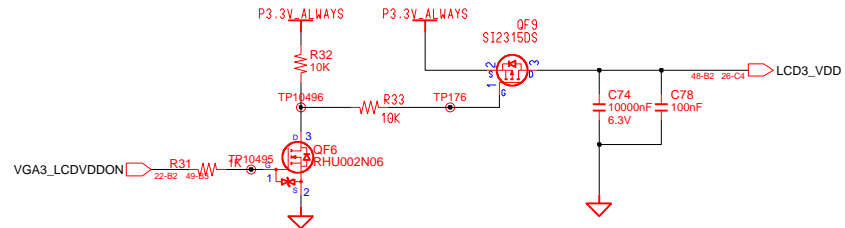
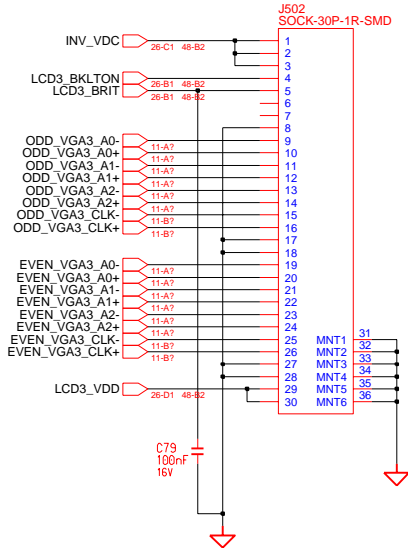


DRAW	IM, KI	DATE	11/5/2004	TITLE	CYGNUS C MAIN	SAMSUNG ELECTRONICS
CHECK	BIN, KK	DEV. STEP	PR	CRT PORT/SPREAD SPECTRUM		
APPROVAL	KIM, DW	REV	1.0	PART NO. BA41-00451A		PAGE 25 OF 49
MODULE CODE	LAST EDIT		November 5, 2004 8:27:10 PM			

Optional External Thermal Sensor

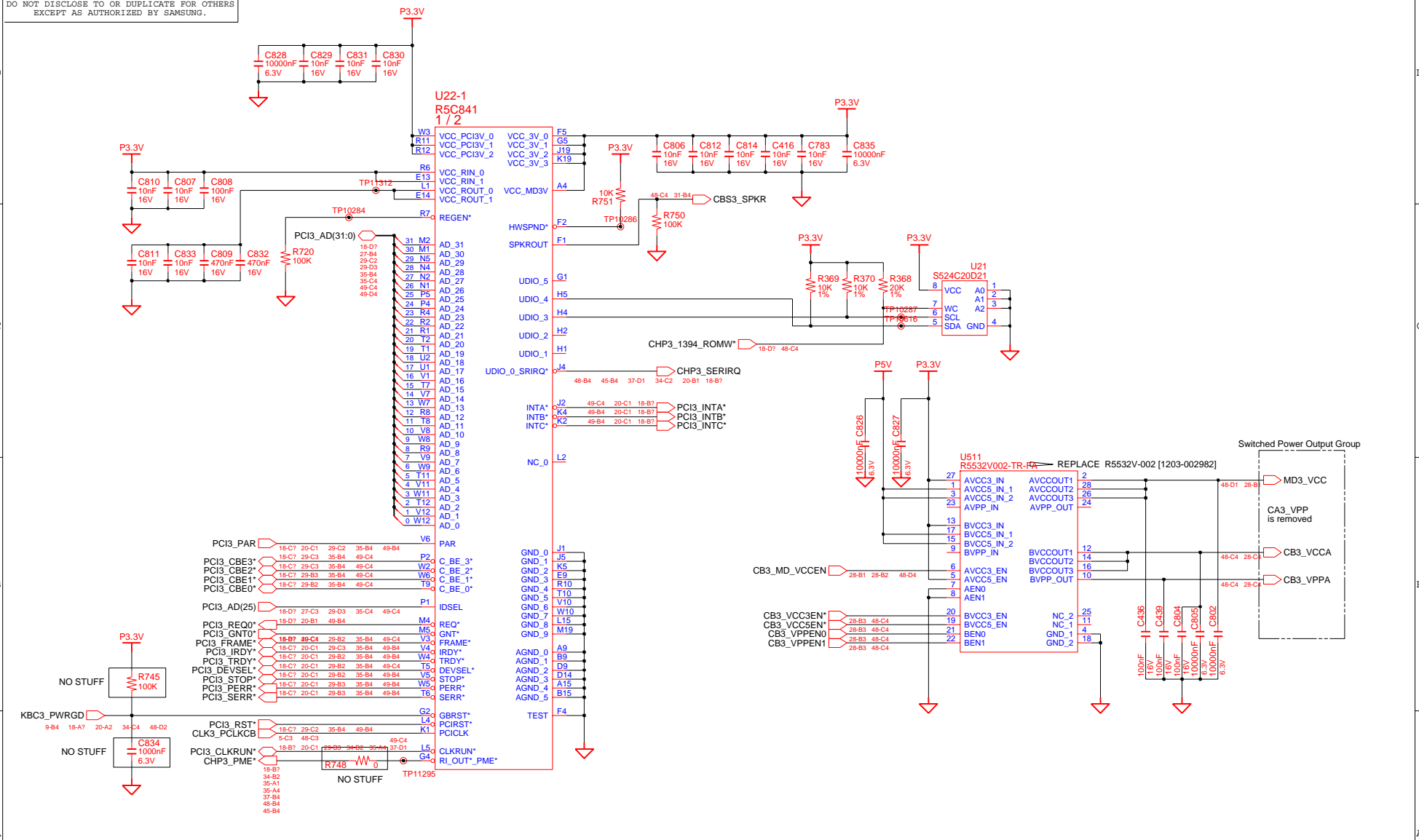
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LCD CONNECTOR



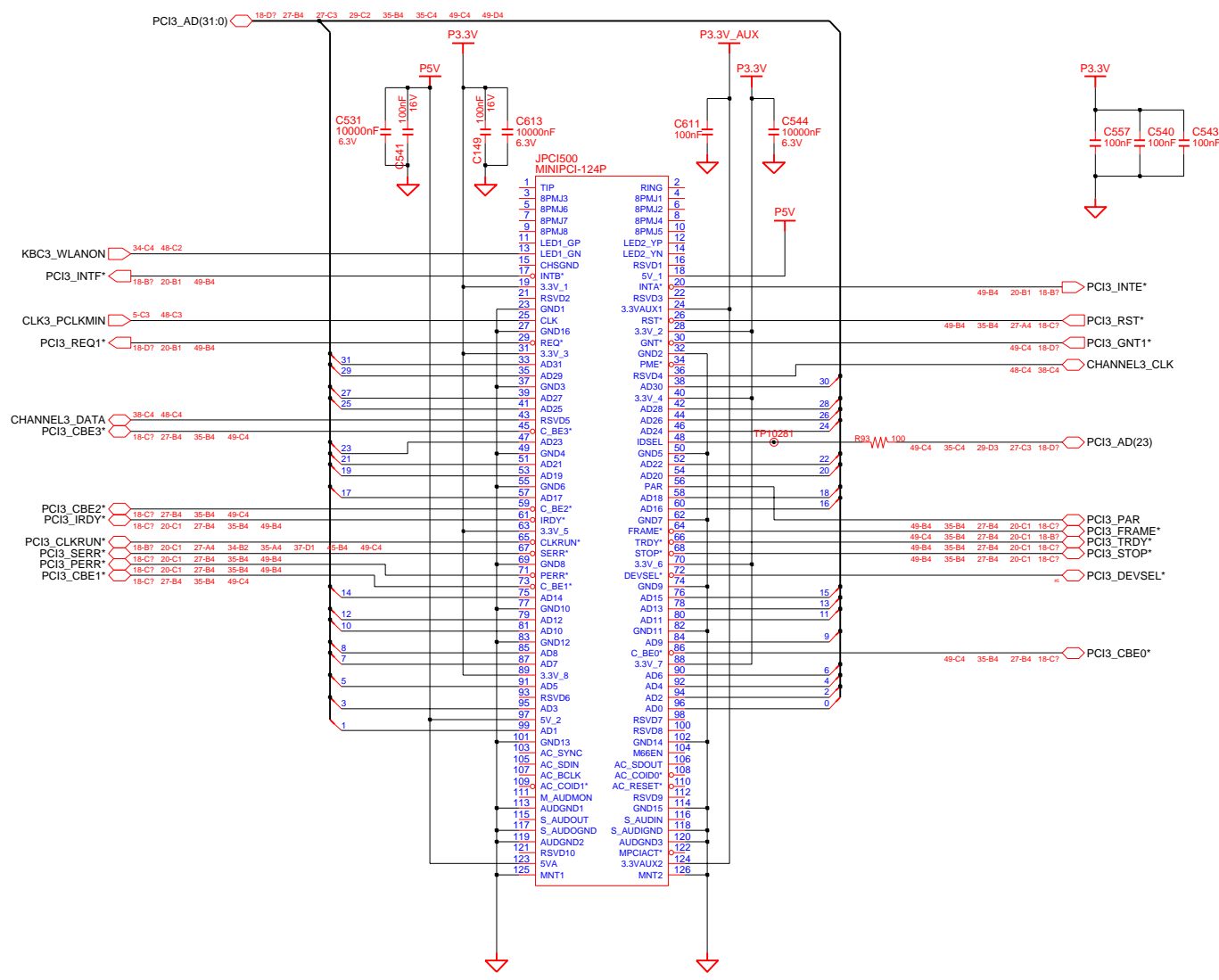
DRAW	IM, KI	DATE	11/5/2004	TITLE	CYGNUS C MAIN	SAMSUNG ELECTRONICS
CHECK	BIN, KK	DEV. STEP	PR	LCD_CONNECTOR / BKLT		
APPROVAL	KIM, DW	REV	1.0	November 5, 2004 8:27:10 PM		PAGE 26 OF 49
MODULE CODE		LAST EDIT				PART NO. BA41-00451A

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DRAW	IM, KI	DATE	11/5/2004	TITLE	CYGNUS C MAIN	SAMSUNG ELECTRONICS
CHECK	BIN, KK	DEV. STEP	PR	CARDBUS / 1394		
APPROVAL	KIM, DW	REV	1.0	November 5, 2004 8:27:10 PM		PART NO. BA41-00451A
MODULE CODE		LAST EDIT		PAGE 27 OF 49		

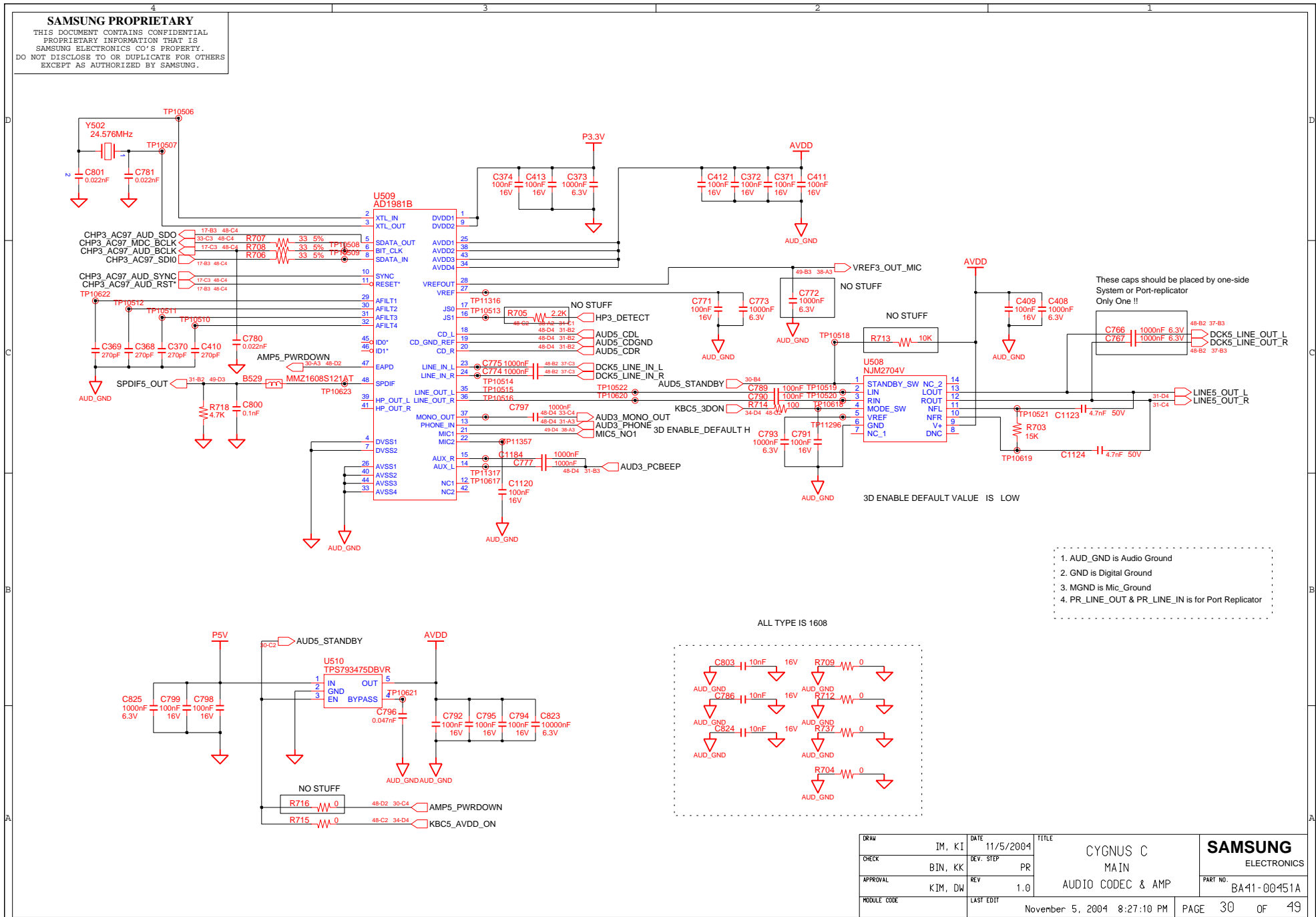
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DRAW	IM, KI	DATE	11/5/2004	TITLE	CYGNUS C MAIN MINI PCI	SAMSUNG ELECTRONICS
CHECK	BIN, KK	DEV. STEP	PR			
APPROVAL	KIM, DW	REV	1.0			PART NO. BA41-00451A
MODULE CODE		LAST EDIT	November 5, 2004 8:27:10 PM	PAGE	29	OF 49

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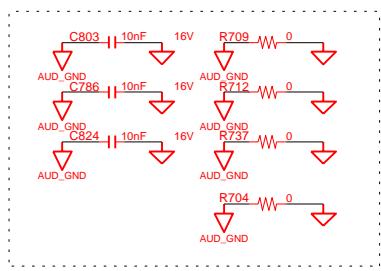
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These caps should be placed by one-side System or Port-replicator Only One !!

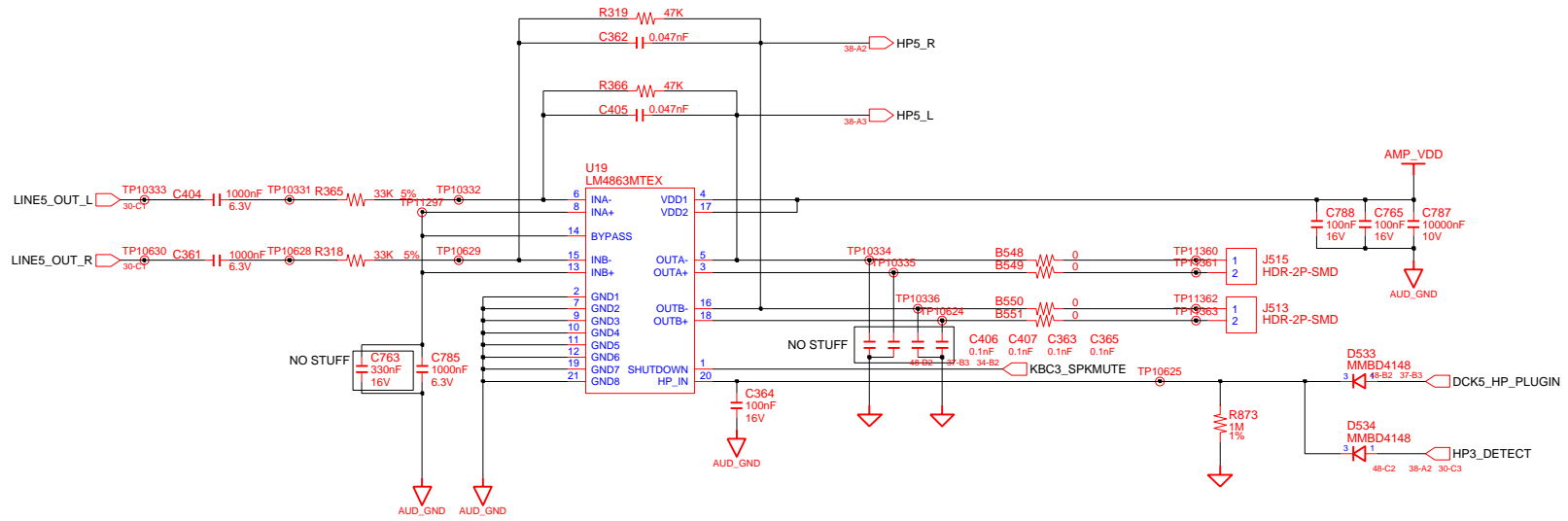
- 1. AUD_GND is Audio Ground
- 2. GND is Digital Ground
- 3. MGN is Mic_Ground
- 4. PR_LINE_OUT & PR_LINE_IN is for Port Replicator

ALL TYPE IS 1608

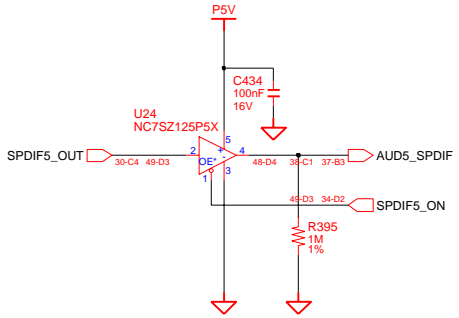
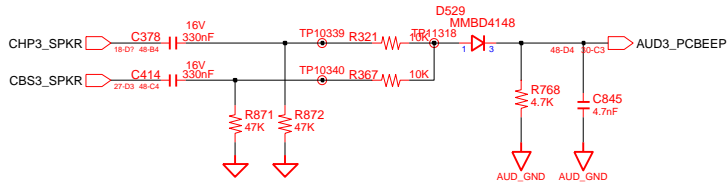
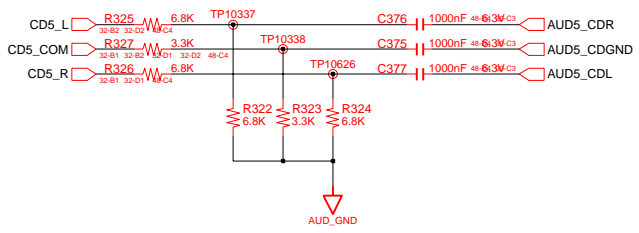
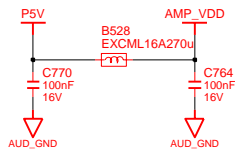


DRAW	IM, KI	DATE	11/5/2004	TITLE	CYGNUS C	SAMSUNG ELECTRONICS
CHECK	BIN, KK	DEV. STEP	PR		MAIN	
APPROVAL	KIM, DW	REV	1.0		AUDIO CODEC & AMP	PART NO.
MODULE CODE		LAST EDIT				BA41-00451A
				November 5, 2004 8:27:10 PM	PAGE	30 OF 49

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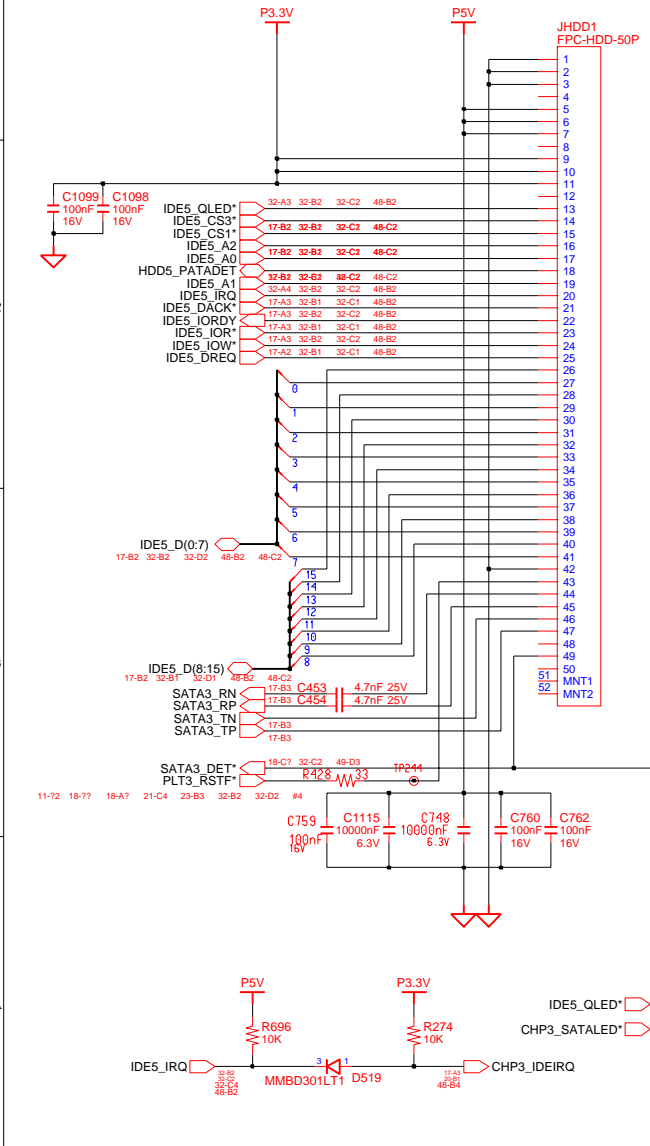
1. HP_IN SHOULD BE USED FOR PORT_REPLICATOR JACK SENSE AND SPDIF_JACK SENSE
 2. PR_JS SHOULD BE IN MAIN B'D
 PR_JS SHOULD HAVE 100kohm RESISTOR WITH Pull_Down
 3. PORT_REPLICATOR SHOULD HAVE 10Kohm with Pull_up



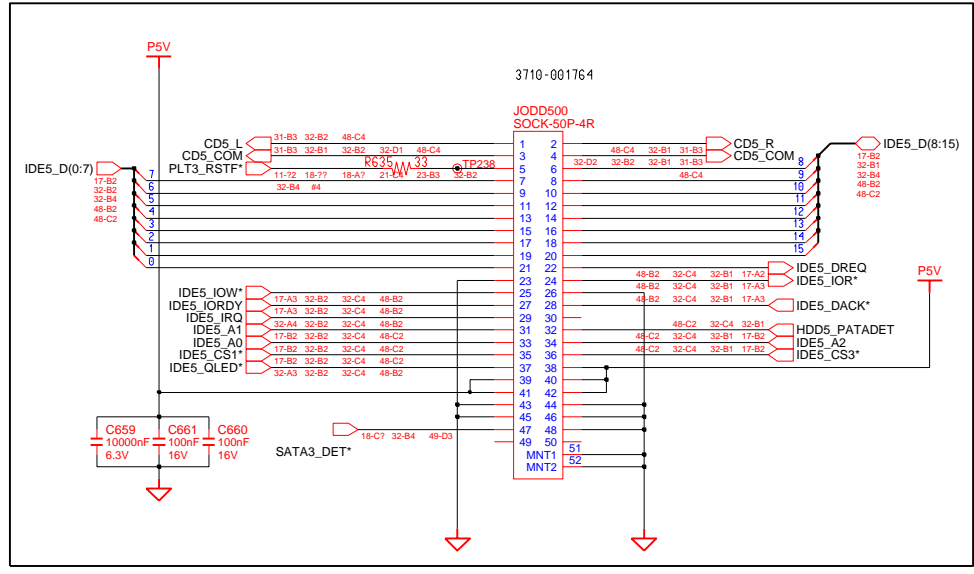
DRAW	IM, KI	DATE	11/5/2004	TITLE	CYGNUS C MAIN AUDIO CODEC & AMP	SAMSUNG ELECTRONICS
CHECK	BIN, KK	DEV. STEP	PR		PART NO.	
APPROVAL	KIM, DW	REV	1.0		BA41-00451A	
MODULE CODE		LAST EDIT	November 5, 2004 8:27:10 PM	PAGE	31	OF 49

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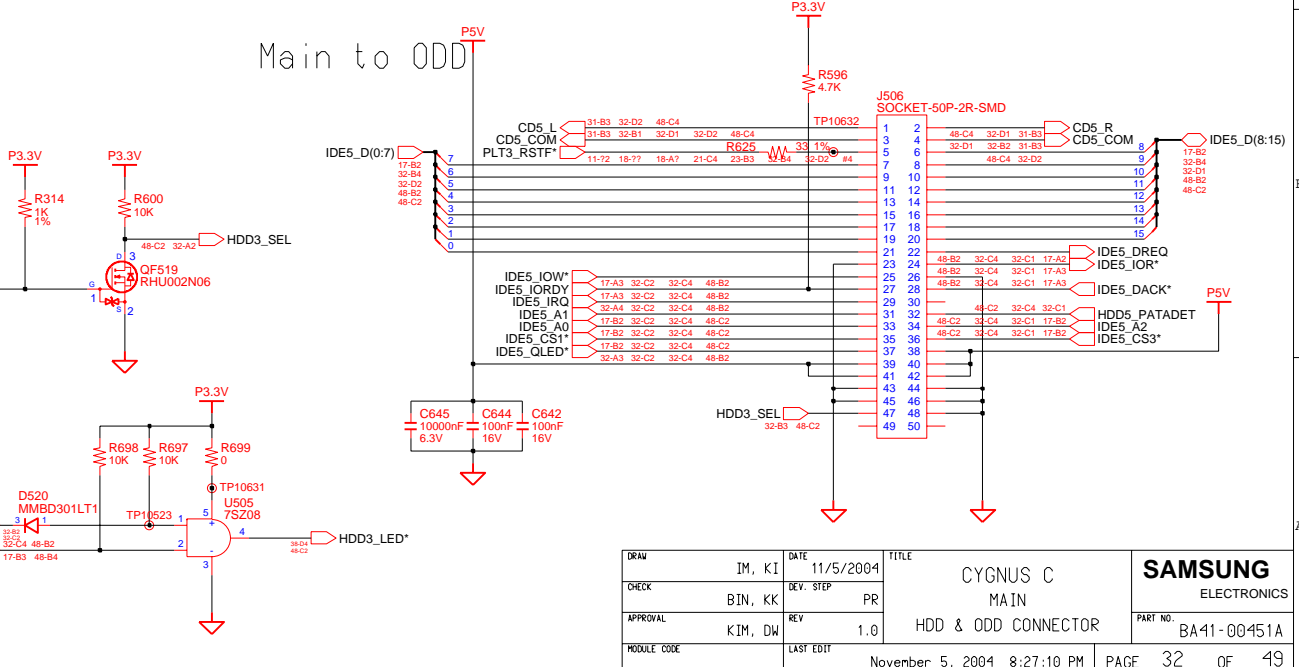
Main to HDD



NO STUFF



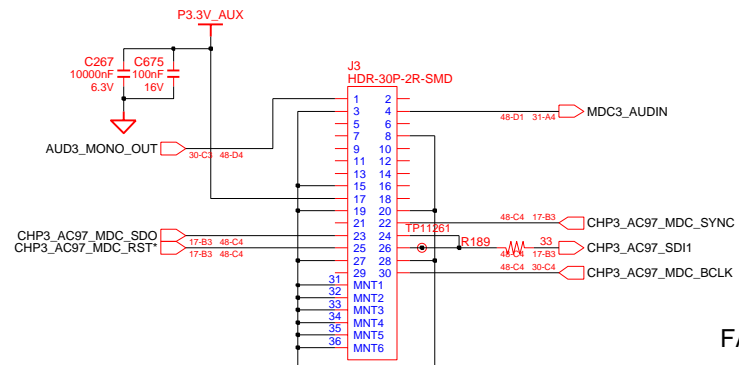
Main to ODD



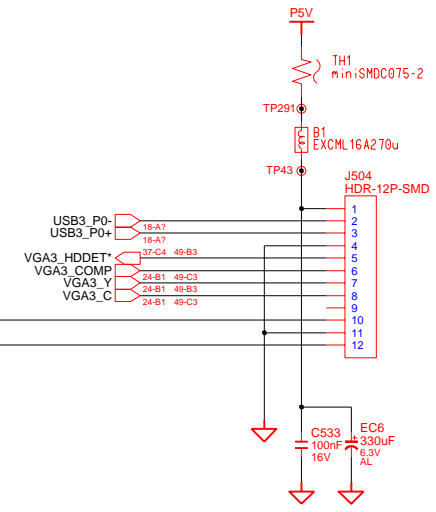
DRAW	IM, KI	DATE	11/5/2004	TITLE	CYGNUS C MAIN HDD & ODD CONNECTOR	SAMSUNG ELECTRONICS PART NO. BA41-00451A
CHECK	BIN, KK	DEV. STEP	PR			
APPROVAL	KIM, DW	REV	1.0			
MODULE CODE		LAST EDIT	November 5, 2004 8:27:10 PM			
					PAGE 32 OF 49	

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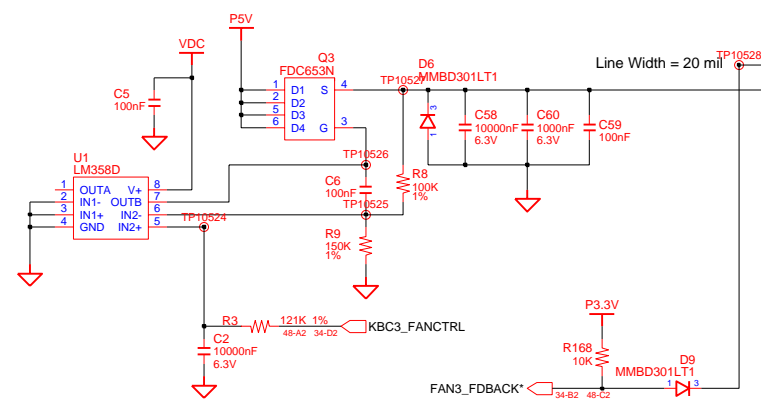
MDC Connector



TV-OUT(S-VHS)



FAN Control Logic

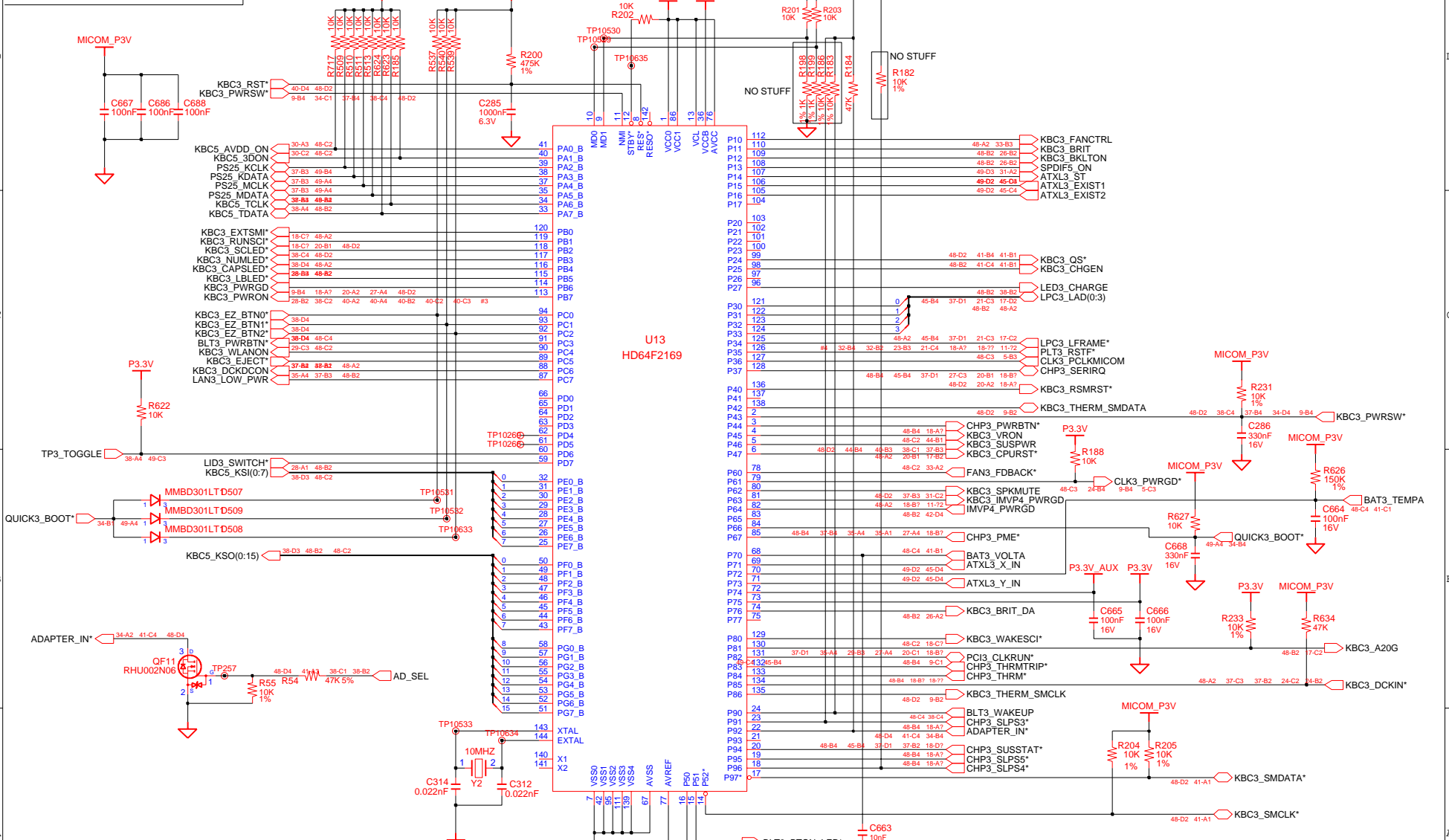


M1 HEAD DIA LENGTH

DRAW	IM, KI	DATE	11/5/2004	TITLE	CYGNUS C	SAMSUNG ELECTRONICS
CHECK	BIN, KK	DEV. STEP	PR		MAIN	
APPROVAL	KIM, DW	REV	1.0	MDC MODEM / TV-OUT(SVHS)		PART NO. BA41-00451A
MODULE CODE		LAST EDIT	November 5, 2004 8:27:10 PM	PAGE	33	OF 49

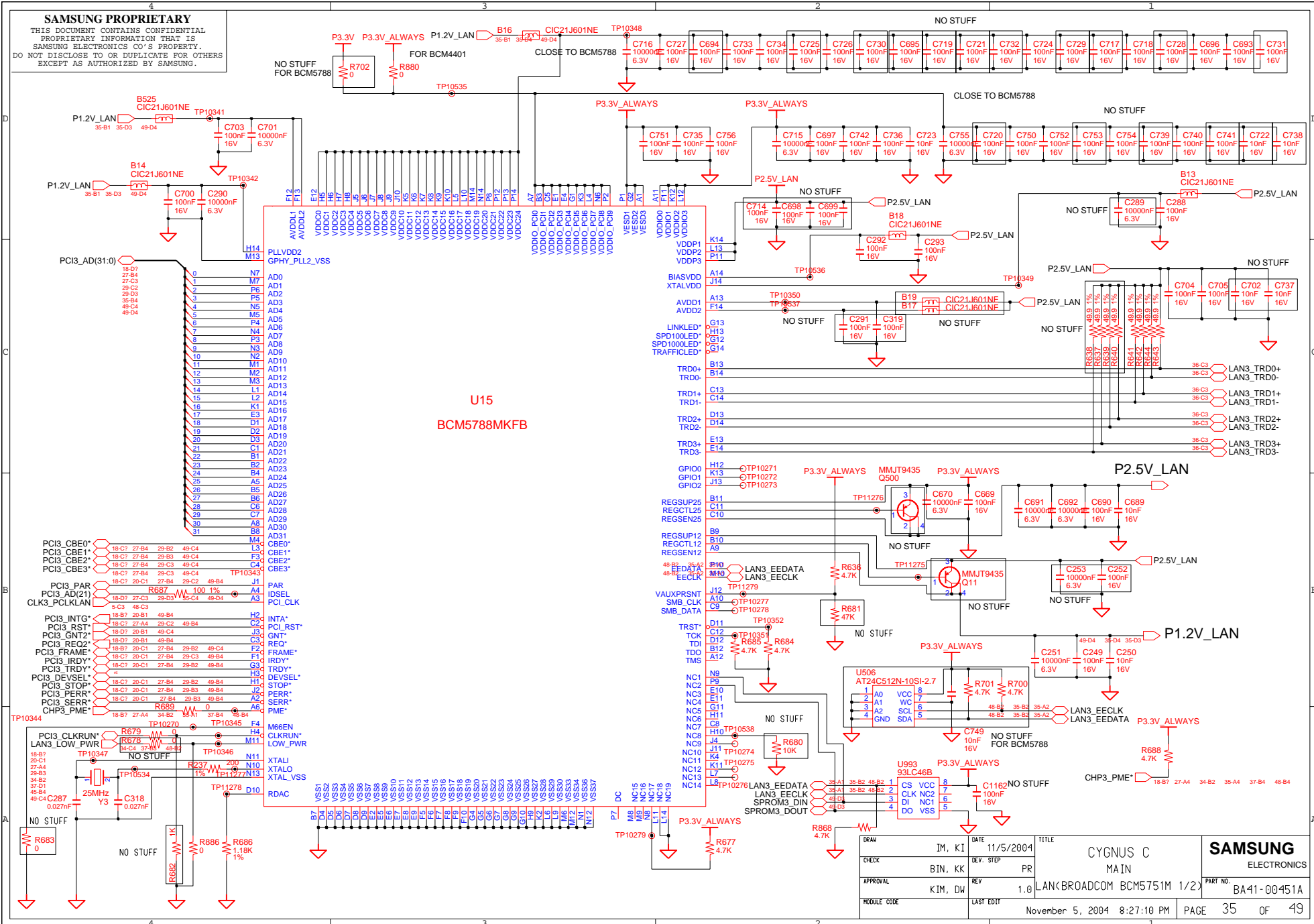
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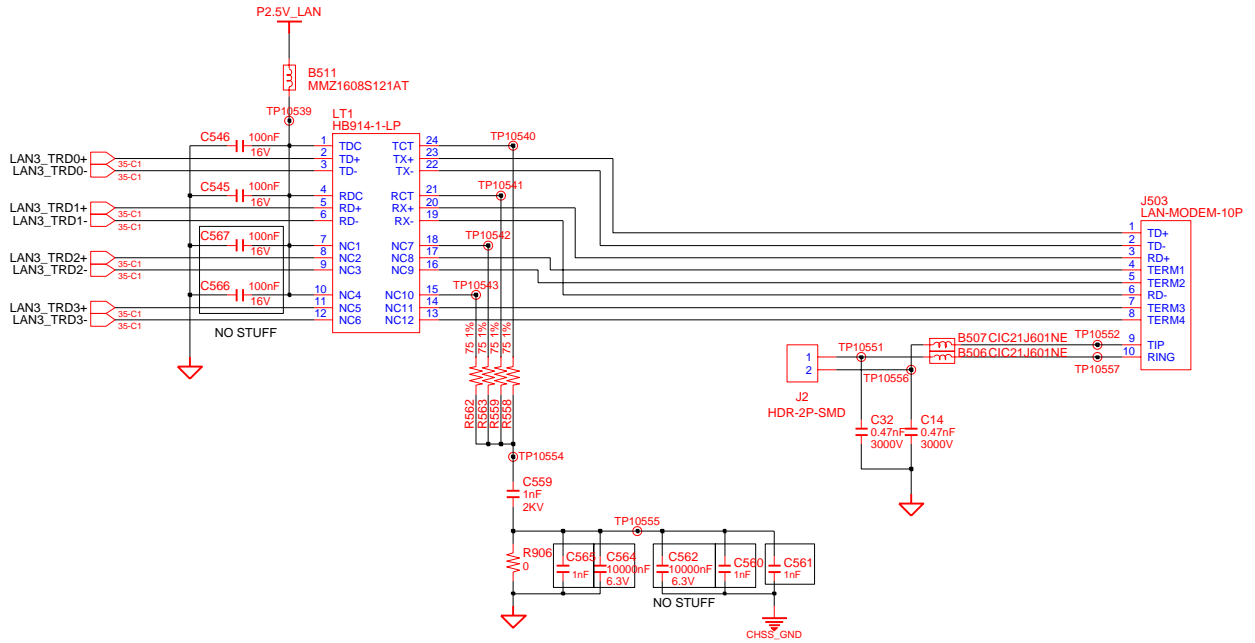
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CHECK	BIN, KK	DEV. STEP	PR		MAIN	
APPROVAL	KIM, DW	REV	1.0		MICOM	PART NO.
MODULE CODE		LAST EDIT	November 5, 2004 8:27:10 PM	PAGE	34	OF 49

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DRAW	IM, KI	DATE	11/5/2004	TITLE	CYGNUS C	SAMSUNG ELECTRONICS
CHECK	BIN, KK	DEV. STEP	PR	CYGNUS C MAIN		
APPROVAL	KIM, DW	REV	1.0	LAN(BROADCOM BCM5751M 1/2)		PART NO.
MODULE CODE		LAST EDIT	November 5, 2004 8:27:10 PM	PAGE	35	OF 49

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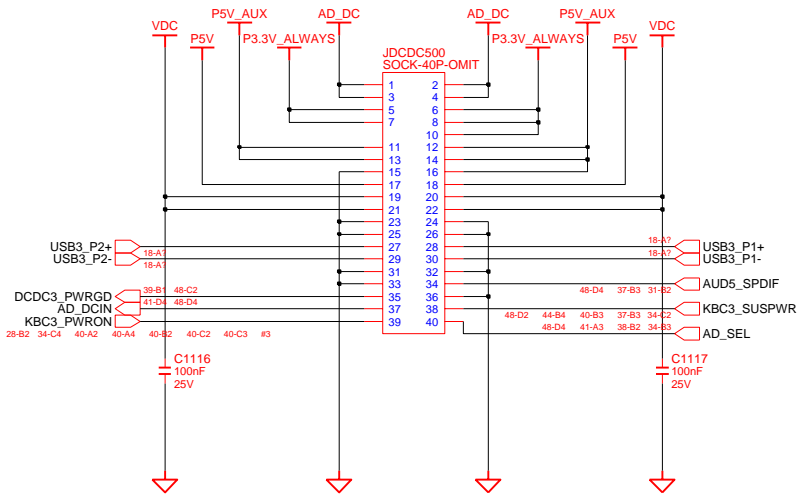
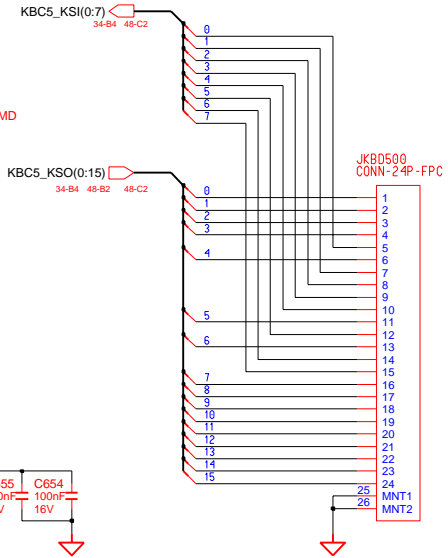
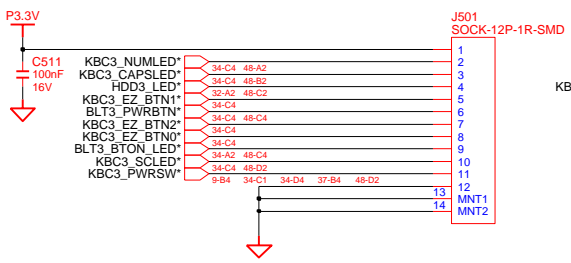
DRAW	IM, KI	DATE	11/5/2004	TITLE	CYGNUS C	PART NO.	SAMSUNG ELECTRONICS
CHECK	BIN, KK	DEV. STEP	PR	MAIN	LAN(BROADCOM BCM5751M 2/2)		
APPROVAL	KIM, DW	REV	1.0			BA41-00451A	
MODULE CODE		LAST EDIT	November 5, 2004 8:27:10 PM	PAGE	36	OF	49

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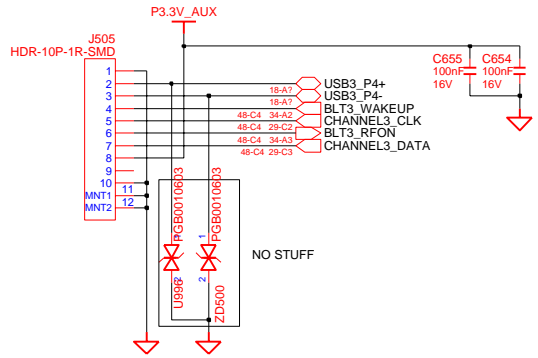
KEYBOARD

Main to DC/DC BOARD

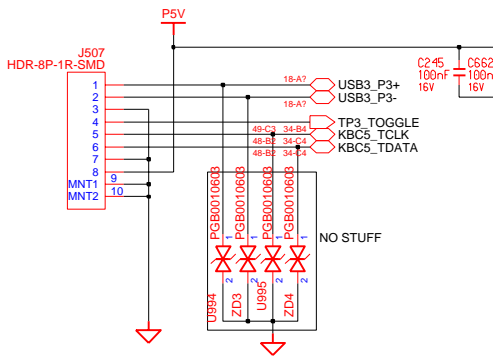
MAIN TO ON-TOP



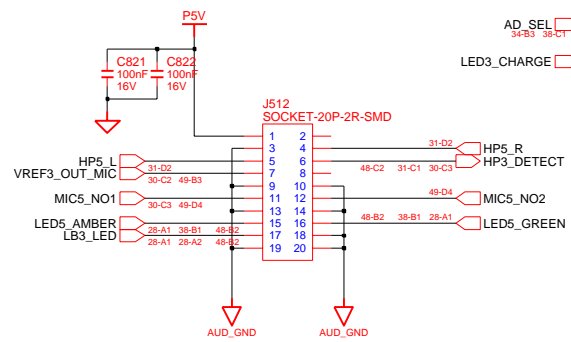
BLUETOOTH CONNECTOR



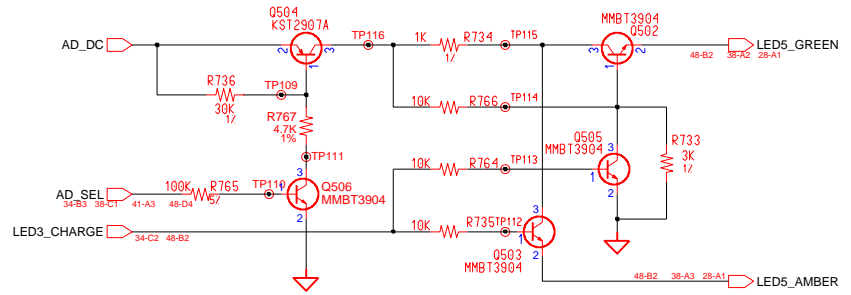
TOUCHPAD CONNECTOR



AUDIO CONNECTOR



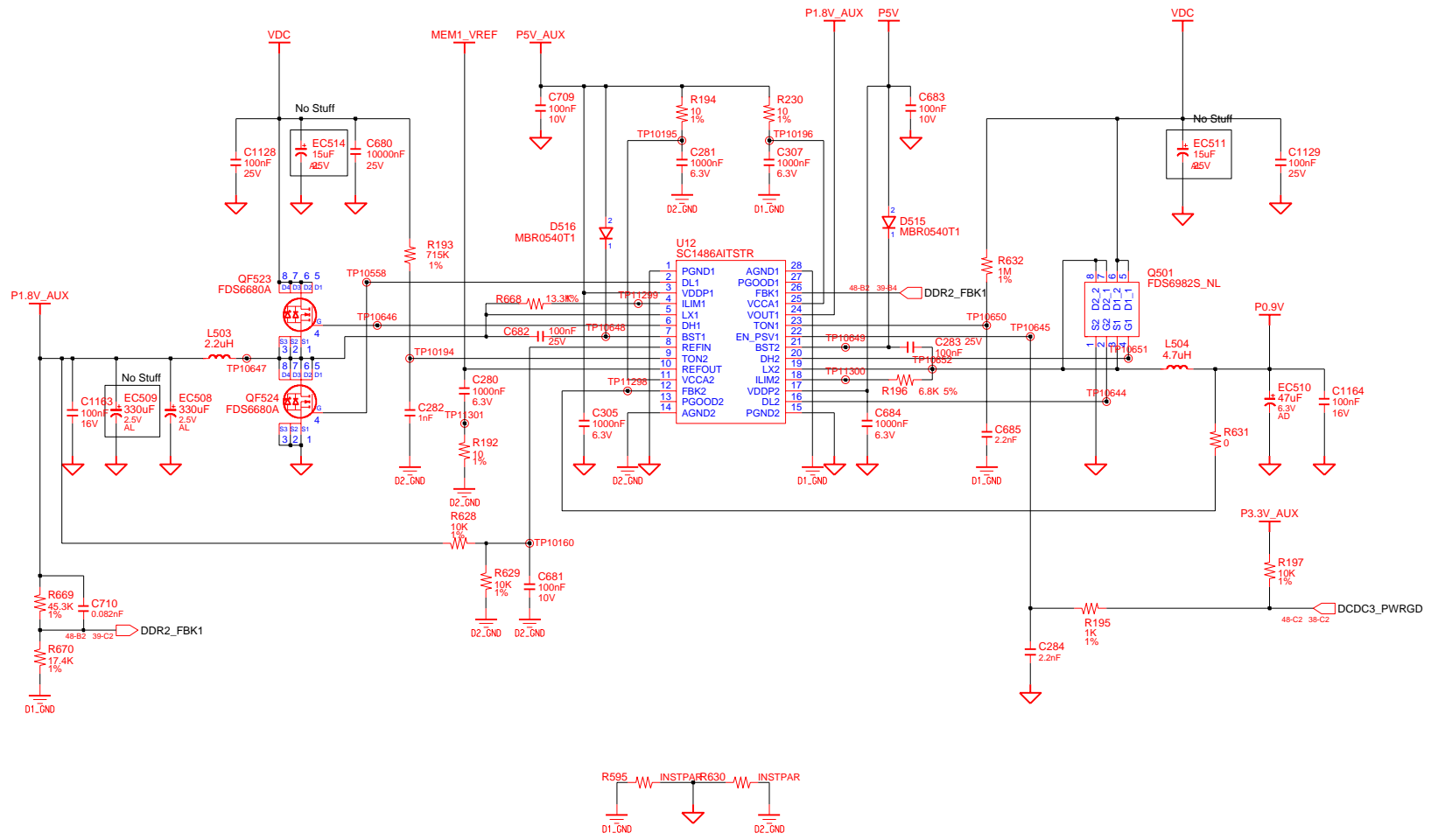
ADAPTERIN/CHARGING LED



DRAW	IM, KI	DATE	11/5/2004	TITLE	CYGNUS C	SAMSUNG ELECTRONICS
CHECK	BIN, KK	DEV. STEP	PR	MAIN		
APPROVAL	KIM, DW	REV	1.0	B'D TO B'D CONNECTOR		PART NO.
MODULE CODE		LAST EDIT	November 5, 2004 8:27:10 PM	PAGE	38	OF 49

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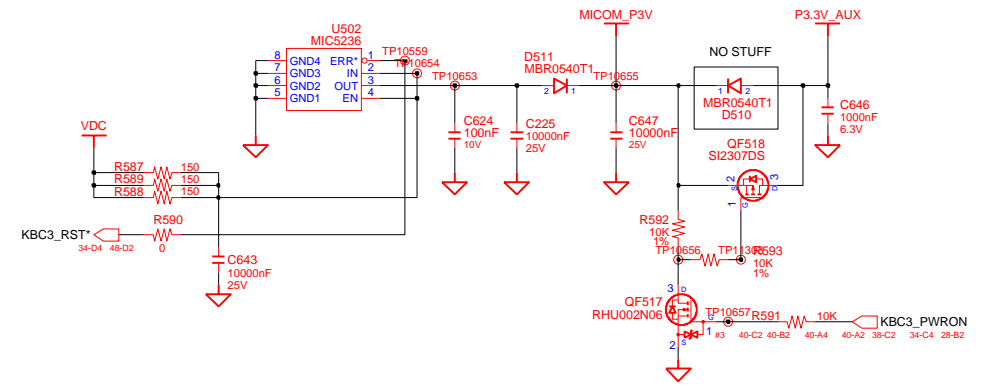
DDR Power



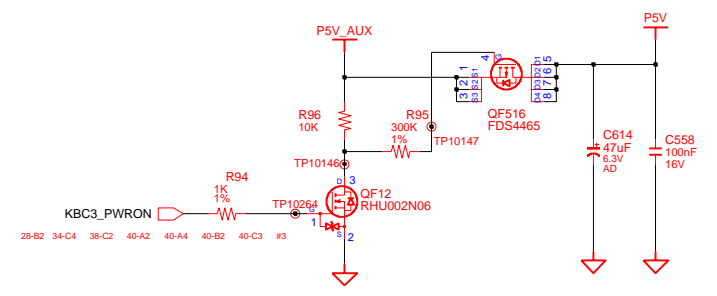
DRAW	IM, KI	DATE	11/5/2004	TITLE	CYGNUS C MAIN DDR POWER	SAMSUNG ELECTRONICS	
CHECK	BIN, KK	DEV. STEP	PR	PART NO.			BA41-00451A
APPROVAL	KIM, DW	REV	1.0	LAST EDIT			November 5, 2004 8:27:10 PM
MODULE CODE				PAGE			39 OF 49

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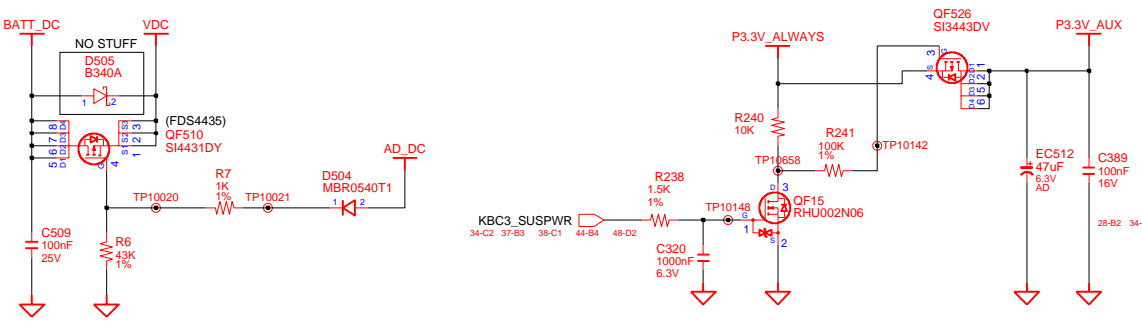
MICOM_P3V Power



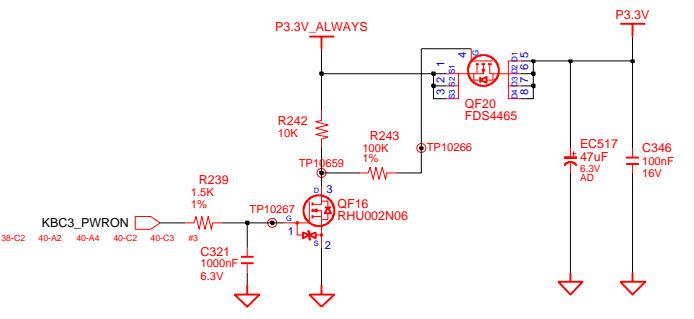
Switched Power On (P5V)



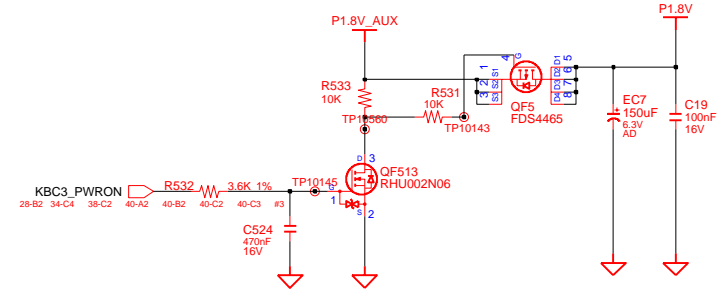
Switched Power On (P3.3V_AUX)



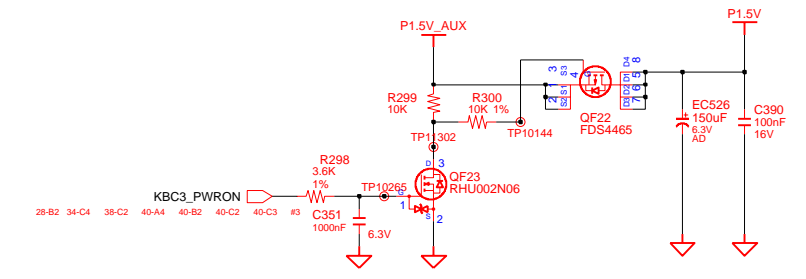
Switched Power On (P3.3V)



Switched Power On (P1.8V)

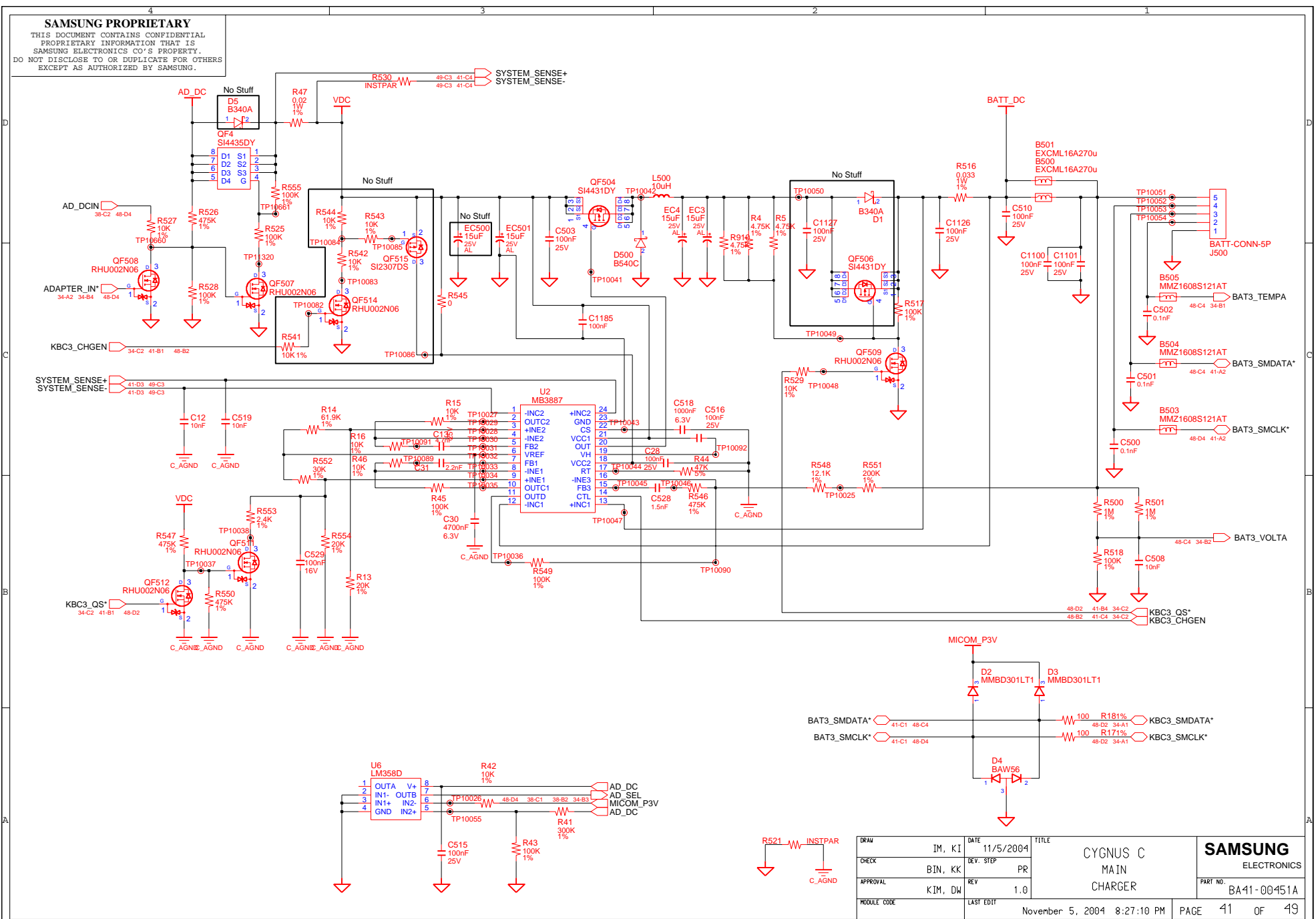


Switched Power On (P1.5V)



DRAW	IM, KI	DATE	11/5/2004	TITLE	CYGNUS C	SAMSUNG ELECTRONICS
CHECK	BIN, KK	DEV. STEP	PR	MAIN		
APPROVAL	KIM, DW	REV	1.0	MICOM & SWITCHED POWER		PART NO. BA41-00451A
MODULE CODE		LAST EDIT	November 5, 2004 8:27:10 PM	PAGE	40	OF 49

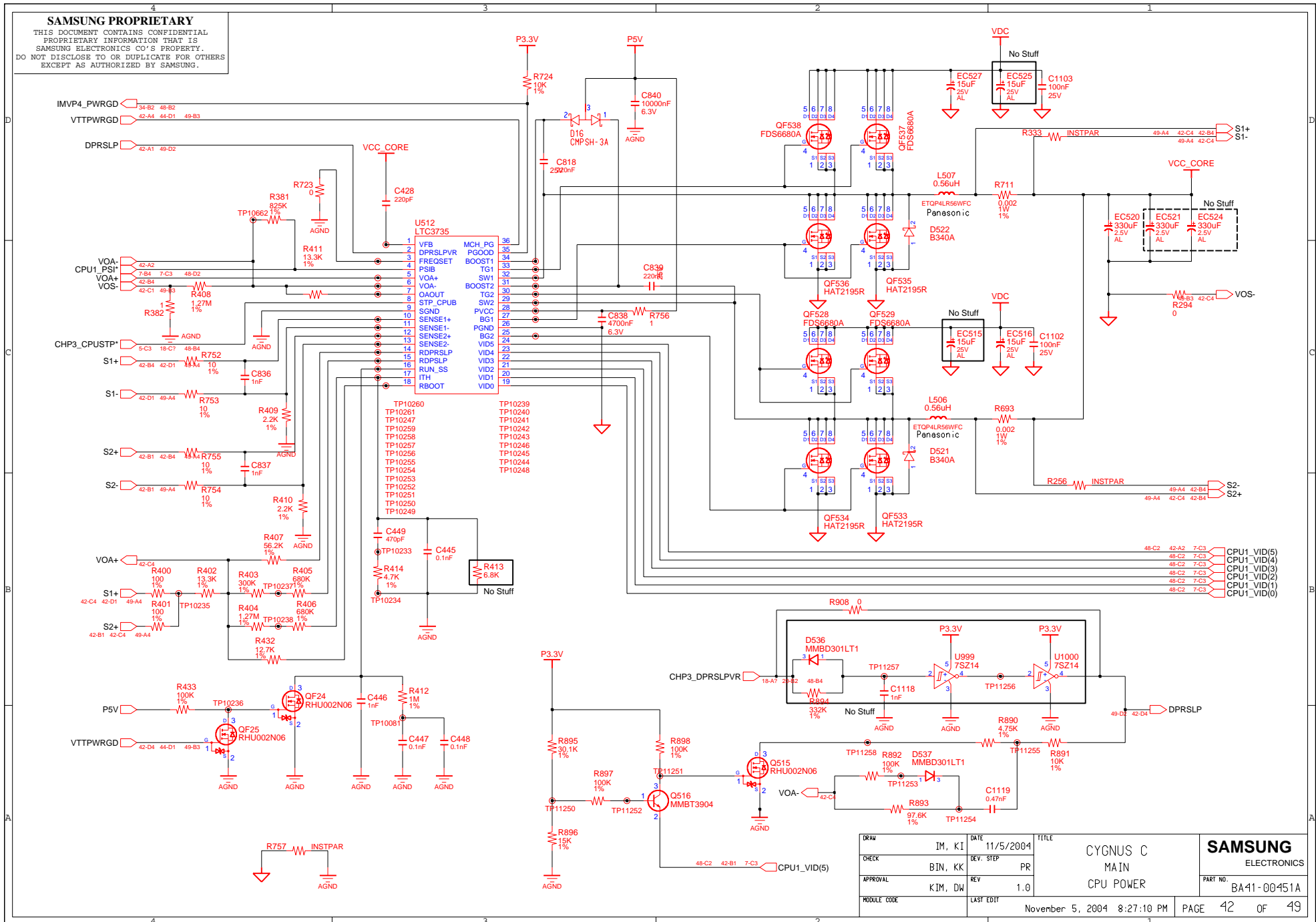
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DRAW	IM, KI	DATE	11/5/2004	TITLE	CYGNUS C MAIN CHARGER	SAMSUNG ELECTRONICS PART NO. BA41-00451A
CHECK	BIN, KK	DEV. STEP	PR			
APPROVAL	KIM, DW	REV	1.0			
MODULE CODE		LAST EDIT	November 5, 2004 8:27:10 PM	PAGE	41 OF 49	

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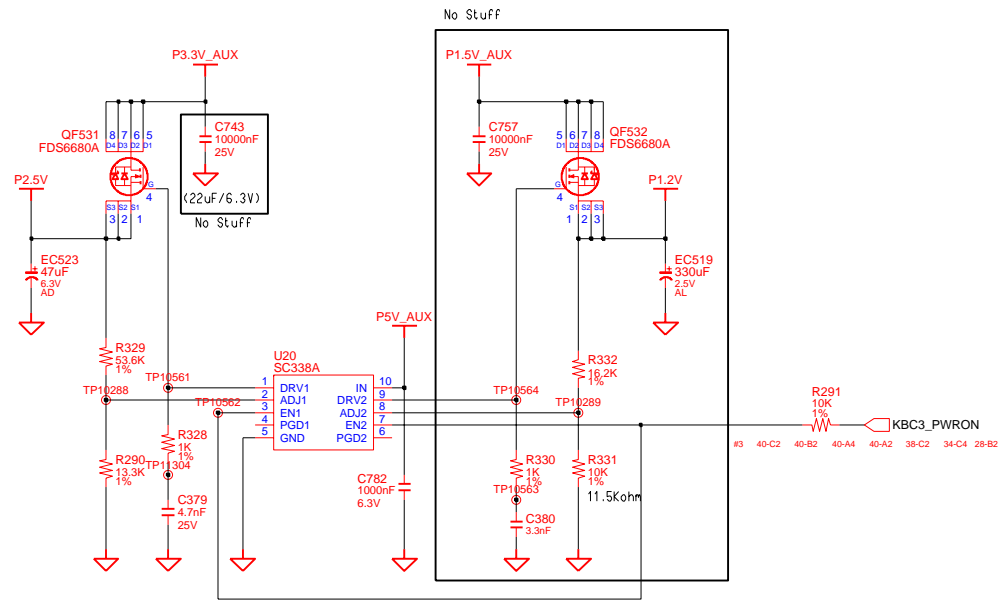
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DRAW	IM, KI	DATE	11/5/2004	TITLE	CYGNUS C MAIN CPU POWER	SAMSUNG ELECTRONICS
CHECK	BIN, KK	DEV. STEP	PR	REV	1.0	
APPROVAL	KIM, DW	LAST EDIT	November 5, 2004 8:27:10 PM	PAGE	42	PART NO. BA41-00-0451A
MODULE CODE					OF	

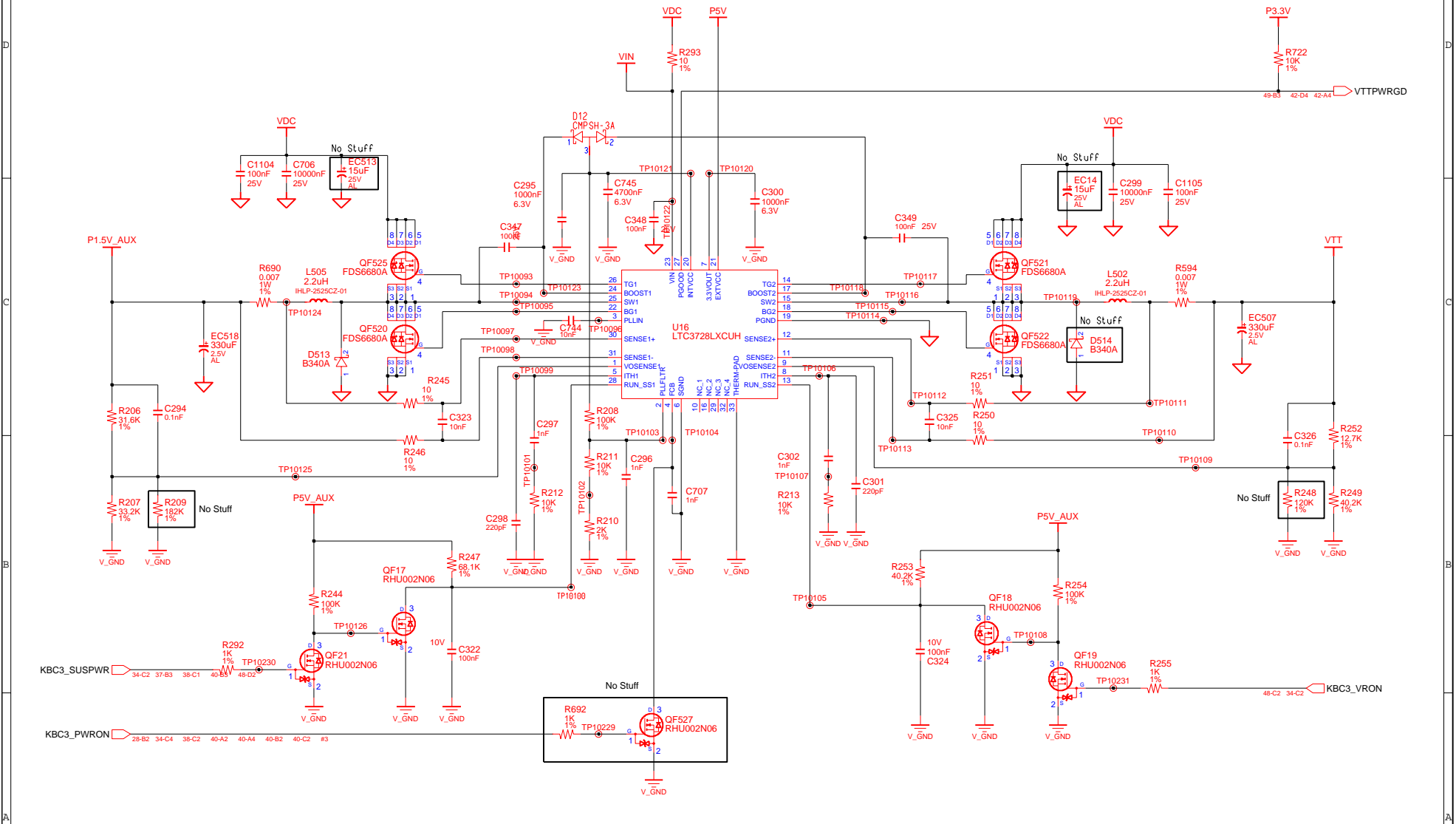
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P2.5V&P1.2V



DRAW	IM, KI	DATE	11/5/2004	TITLE	CYGNUS C MAIN P2.5V & P1.2V	SAMSUNG ELECTRONICS	
CHECK	BIN, KK	DEV. STEP	PR	PART NO.			BA41-00451A
APPROVAL	KIM, DW	REV	1.0	PAGE			43 OF 49
MODULE CODE		LAST EDIT	November 5, 2004 8:27:10 PM				

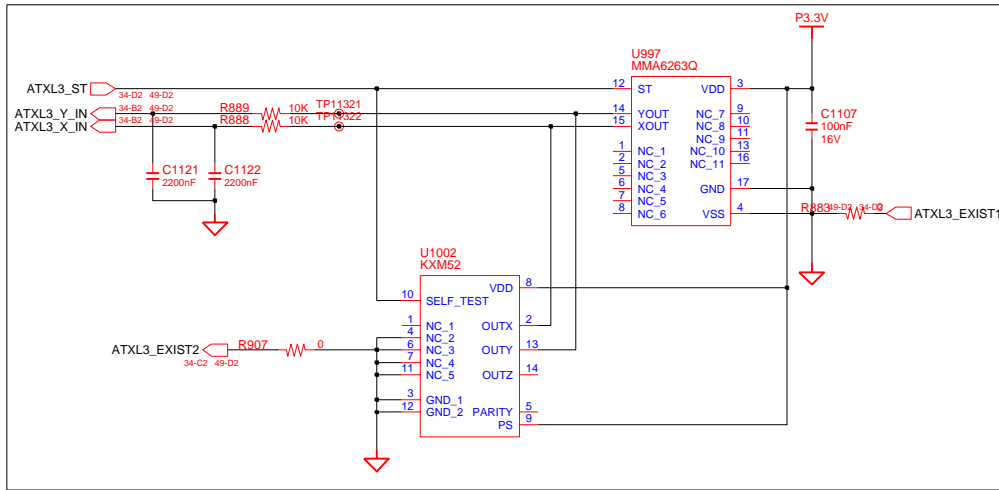
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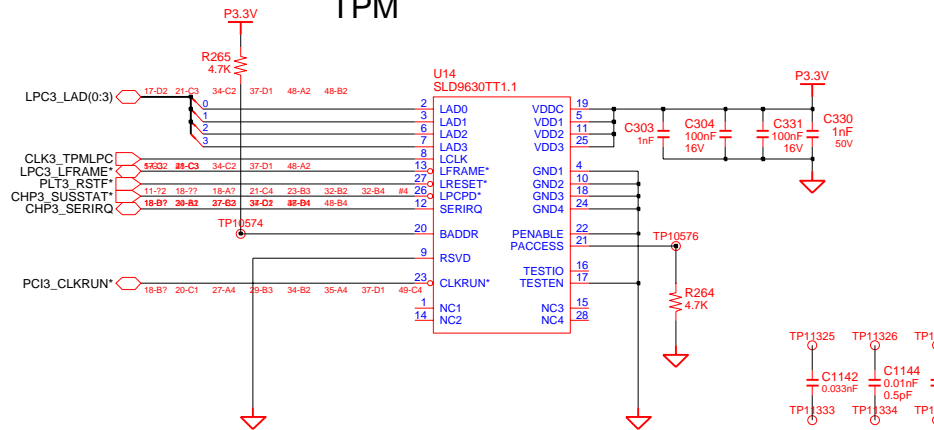
DRAW	IM, KI	DATE	11/5/2004	TITLE	CYGNUS C MAIN P1.5V_AUX & VTT	SAMSUNG ELECTRONICS
CHECK	BIN, KK	DEV. STEP	PR			
APPROVAL	KIM, DW	REV	1.0			PART NO. BA41-00451A
MODULE CODE		LAST EDIT	November 5, 2004 8:27:10 PM	PAGE	44	OF 49

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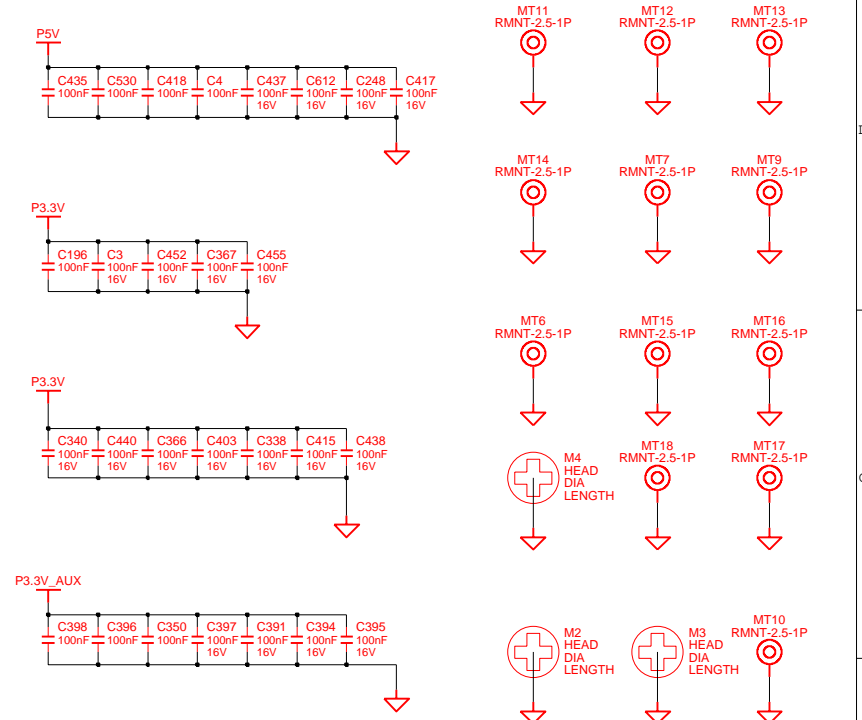
AIRBAG



TPM



PCB REVISION CONTROL (ICT)				
NO	CONNECTION	DATE(Y/M/DD)	REVISION	STEP
1	N.C.			
2	1-2			
3	2-3			
4	3-1			
5	1-2-3			
6	N.C.			
7	1-2			
8	2-3			
9	3-1			
10	1-2-3			



DRAW	IM, KI	DATE	11/5/2004	TITLE	CYGNUS C MAINBD AIRBAG & TPM	SAMSUNG ELECTRONICS PART NO. BA41-00451A
CHECK	BIN, KK	DEV. STEP	PR			
APPROVAL	KIM, DW	REV	1.0			
MODULE CODE		LAST EDIT	November 5, 2004 8:27:10 PM	PAGE	45 OF 49	

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
Cardbus	AD25	0	A,B,C
	AD21	3	
MiniPCI SLOT1	AD23	2	D,E
USB	AD29(internal)	-	USB2.0 #0 : A USB2.0 #1 : D USB2.0 #2 : C
Hub to PCI	AD30(internal)	-	-
LPC bridge/IDE/AC97/SMBUS	AD31(internal)	-	B
	-	-	A,B
Internal MAC	AD24(internal)	-	E
AC Link	-	-	B

Voltage Rails

VDC	Primary DC system power supply (7 to 21V)
VCC_CORE	Core voltage for DOTHAN (1.308-1.068V)
VTT	DOTHAN/ALVISO Processor System Bus(PSB) Termination (1.05V) MCH-M Core Voltage
P0.9V	0.9V switched power rail (off in S3-S5)
P1.2V	1.2V switched power rail (off in S3-S5)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.5V_AUX	1.5V power rail (off in S4-S5)
P1.8V	1.8V switched power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail(off in S4-S5)
P2.5V	2.5V switched power rail (off in S3-S5)
MICOM_P3V	3.3V always on power rail for MICOM
P3.3V	3.3V switched power rail (off in S3-S5)
P3.3V_AUX	3.3V power rail (off in S4-S5)
P5V	5.0V switched power rail (off in S3-S5)
P5V_AUX	5.0V power rail (off in S4-S5)

CPU Core Voltage Table

VID5	VID4	VID3	VID2	VID1	VID0	Voltage	VID5	VID4	VID3	VID2	VID1	VID0	Voltage	
0	0	0	0	0	0	1.708 V	1	0	0	0	0	0	1.196 V	Northwood-B (Interposer B'd)
0	0	0	0	0	1	1.692 V	1	0	0	0	0	1	1.180 V	
0	0	0	0	1	0	1.676 V	1	0	0	0	1	0	1.164 V	
0	0	0	1	1	0	1.660 V	1	0	0	0	1	1	1.148 V	
0	0	0	1	0	0	1.644 V	1	0	0	1	0	0	1.132 V	
0	0	0	1	0	1	1.628 V	1	0	0	1	0	1	1.116 V	
0	0	0	1	1	0	1.612 V	1	0	0	1	1	0	1.100 V	
0	0	1	1	1	1	1.596 V	1	0	0	1	1	1	1.084 V	
0	0	1	0	0	0	1.580 V	1	0	1	0	0	0	1.068 V	
0	0	1	0	0	1	1.564 V	1	0	1	0	0	1	1.052 V	
0	0	1	0	1	0	1.548 V	1	0	1	0	1	0	1.036 V	
0	0	1	0	1	1	1.532 V	1	0	1	0	1	1	1.020 V	
0	0	1	1	0	0	1.516 V	1	0	1	1	0	0	1.004 V	
0	0	1	1	0	1	1.500 V	1	0	1	1	0	1	0.988 V	
0	0	1	1	1	0	1.484 V	1	0	1	1	1	0	0.972 V	
0	0	1	1	1	1	1.468 V	1	0	1	1	1	1	0.956 V	
0	1	0	0	0	0	1.452 V	1	1	0	0	0	0	0.940 V	
0	1	0	0	0	1	1.436 V	1	1	0	0	0	1	0.924 V	
0	1	0	0	1	0	1.420 V	1	1	0	0	1	0	0.908 V	
0	1	0	0	1	1	1.404 V	1	1	0	0	1	1	0.892 V	
0	1	0	1	0	0	1.388 V	1	1	0	1	0	0	0.876 V	
0	1	0	1	0	1	1.372 V	1	1	0	1	0	1	0.860 V	
Highest Freq.	0	1	0	1	1	1.356 V	1	1	0	1	1	0	0.844 V	Lowest Freq.
	0	1	0	1	1	1.340 V	1	1	0	1	1	1	0.828 V	
	0	1	1	0	0	1.324 V	1	1	1	0	0	0	0.812 V	
	0	1	1	0	0	1.308 V	1	1	1	0	0	1	0.796 V	
	0	1	1	0	1	1.292 V	1	1	1	0	1	0	0.780 V	
	0	1	1	0	1	1.276 V	1	1	1	0	1	1	0.764 V	
	0	1	1	1	0	1.260 V	1	1	1	1	0	0	0.748 V	Deeper Sleep
	0	1	1	1	0	1.244 V	1	1	1	0	1	0	0.732 V	
	0	1	1	1	1	1.228 V	1	1	1	1	1	0	0.716 V	
	0	1	1	1	1	1.212 V	1	1	1	1	1	1	0.700 V	

IC / SMB Address

Devices	Address	Hex	Bus
ICH6	Master	-	SMBUS Master
EMC6N300(CPU Thermal Sensor)	1001 110X	9Ch	Thermal Sensor
SODIMM0	1010 0000	A0h	-
SODIMM1	1010 001X	A2h	-
CK-408 (Clock Generator)	1101 001X	D2h	Clock, Unused Clock Output Disable

USB PORT Assign

PORT NUMBER	ASSIGNED TO
0	SYSTEM PORT A
1,2	SYSTEM PORT B
3	BLUETOOTH
4	FINGER PRINT OPTION OPTION

System Power States

- CHP3_SLP1S* S1, Powered-On-Suspend(POS) : In this state, all clocks(except the 32.768KHz clock) are stopped. The system context is maintained in system DRAM. Power is maintained to PCI, the CPU, memory controller, memory, and all other critical subsystems. Note that this state does not preclude power being removed from non-essential devices, such as disk drives. During this state, CPU can be selected for either Deep Sleep or Deeper Sleep.
- In Deeper Sleep, CPU voltage reduced in this state to reduce the leakage power.
- CHP3_SLP3S* S3, Suspend-To-RAM(STR) : The system context is maintained in system DRAM, but power is shut off to non-critical circuits. Memory is retained, and refreshes continue. All clocks stop except RTC clock.
- CHP3_SLP4S* S4, Suspend-To-Disk(STD) : The Context of the system is maintained on the disk. All power is then shut off to the system except for the logic required to resume. Externally appears same as S5, but may have different wake events.
- CHP3_SLP5S* S5, Soft Off(SOFF) : System context is not maintained. All power is shut off except for the logic required to restart. A full boot is required when waking.

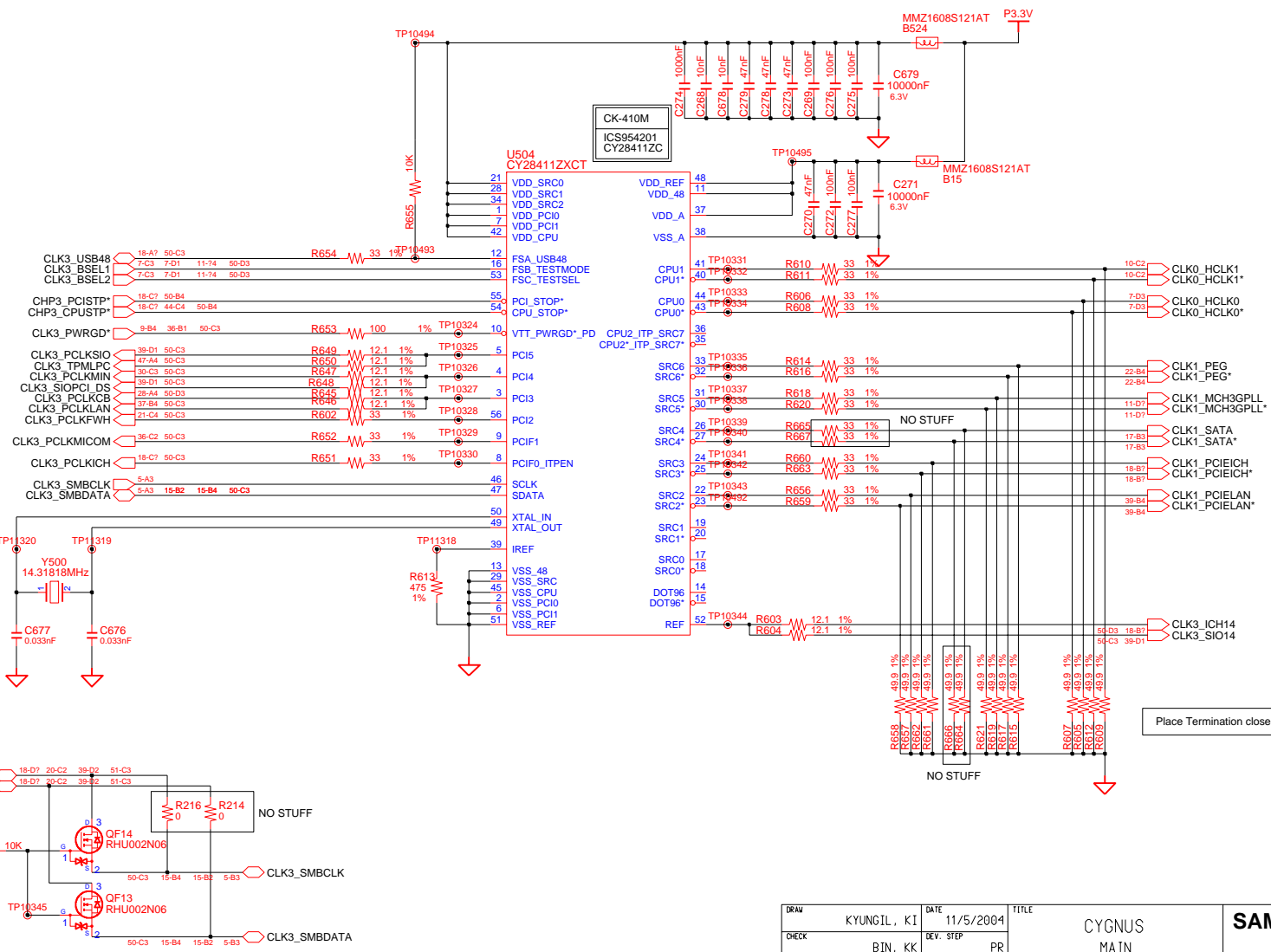
REVISION HISTORY

See rev notes in the changes file for more information.

DRAW	KYUNGIL, KI	DATE	11/5/2004	TITLE	CYGNUS MAIN BOARD INFORMATION	SAMSUNG ELECTRONICS	
CHECK	BIN, KK	DEV. STEP	PR	PART NO.			BA41-00450A
APPROVAL	KIM, DW	REV	1.0	PAGE			4 OF 51
MODULE CODE		LAST EDIT	November 5, 2004 8:10:03 PM				

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FSA	FSB	FSC	HOST CLK
BSEL2	BSEL1	BSEL0	
0	0	0	266 MHz
0	0	1	333 MHz
0	1	0	200 MHz
0	1	1	400 MHz
1	0	0	133 MHz
1	0	1	100 MHz
1	1	0	166 MHz
1	1	1	RSVD

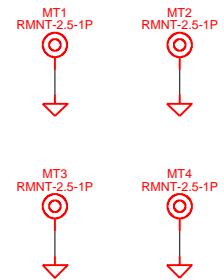
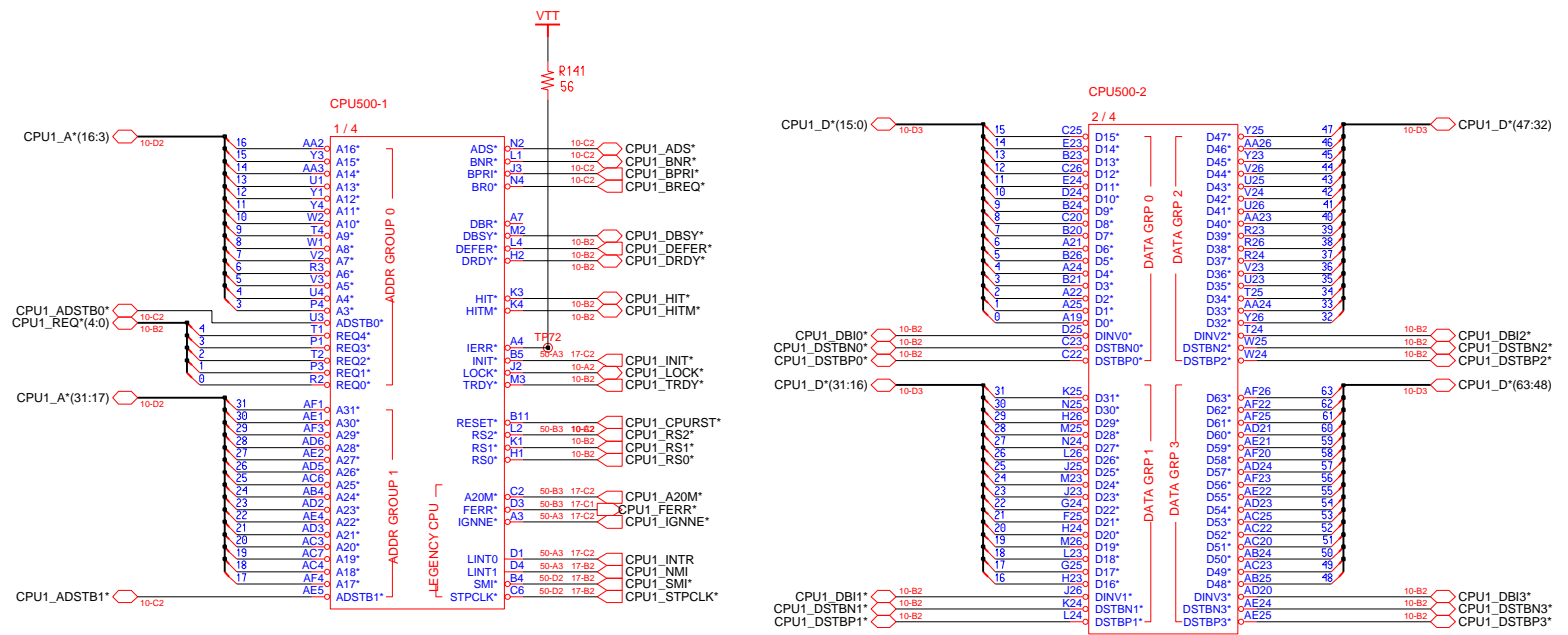


Place 14.318MHz within 500mils of CK-410M

Place Termination close to CK-410M

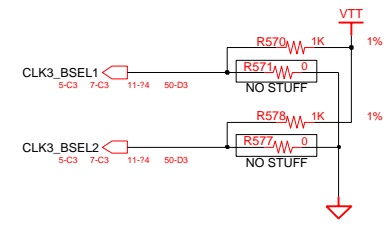
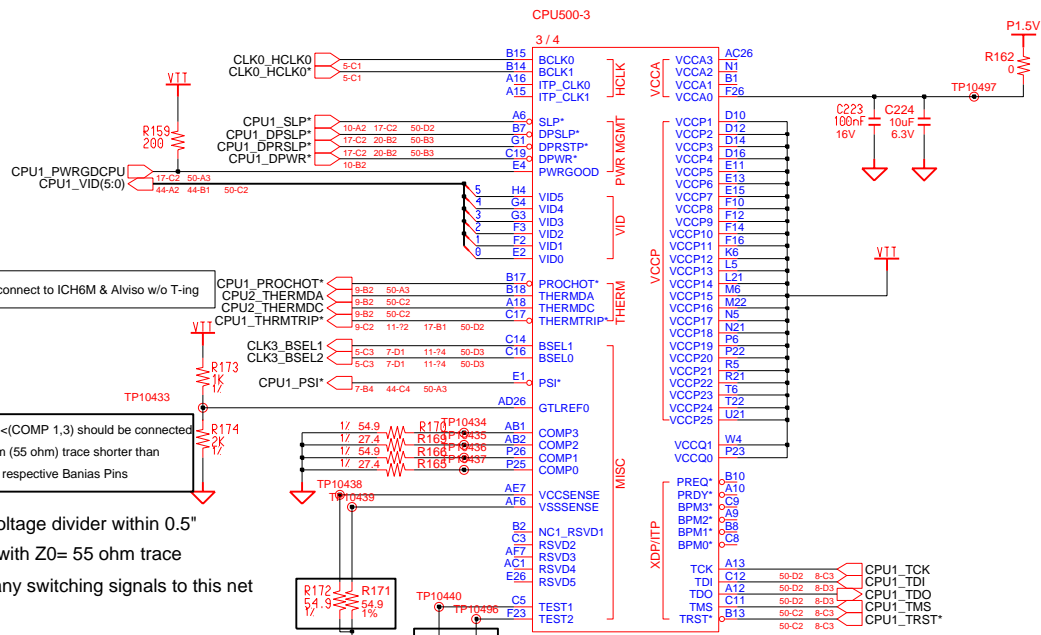
DRAW	KYUNGIL, KI	DATE	11/5/2004	TITLE	CYGNUS MAIN	SAMSUNG ELECTRONICS
CHECK	BIN, KK	DEV. STEP	PR			
APPROVAL	KIM, DW	REV	1.0		CLOCK GENERATOR	PART NO. BA41-00450A
MODULE CODE		LAST EDIT	November 5, 2004 8:10:03 PM	PAGE	5	OF 51

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CHECK	BIN, KK	DEV. STEP	PR			
APPROVAL	KIM, DW	REV	1.0			
MODULE CODE		LAST EDIT				
			November 5, 2004 8:10:03 PM	PAGE 6 OF 51		

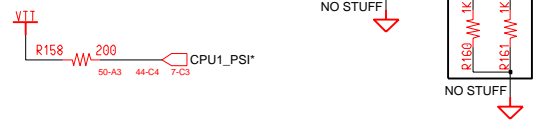
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	STUFF			NO STUFF		
Dothan400 A-Step	R575 R582	R578 R579	R577 R580	R574 R576	R581 R583	
Dothan533 A-Step	R576 R582	R578 R579	R577 R580	R574 R575	R581 R583	
FutureDothan(B-Step*)	R574 R577	R581 R580	R578 R579	R575 R583	R576 R582	

COMP 0, 2 <(COMP 1,3) should be connected
 Z0=27.4 ohm (55 ohm) trace shorter than
 1/2 " to their respective Banias Pins

GTLREF : Keep the Voltage divider within 0.5"
 of the First GTLREF0 with Z0= 55 ohm trace
 Minimize coupling of any switching signals to this net



CPU Core Voltage Table

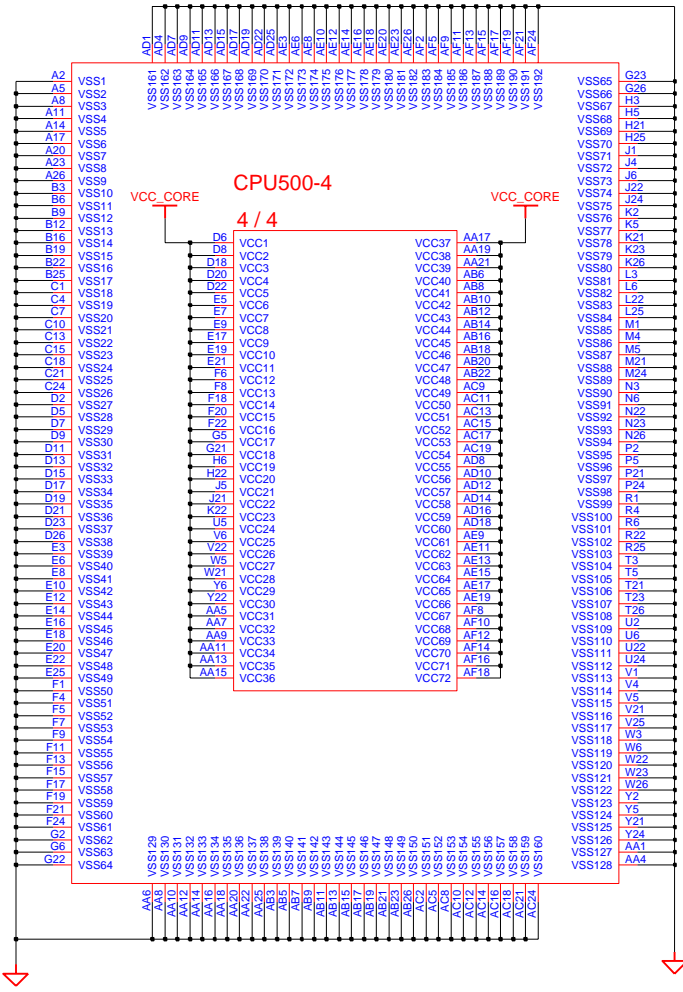
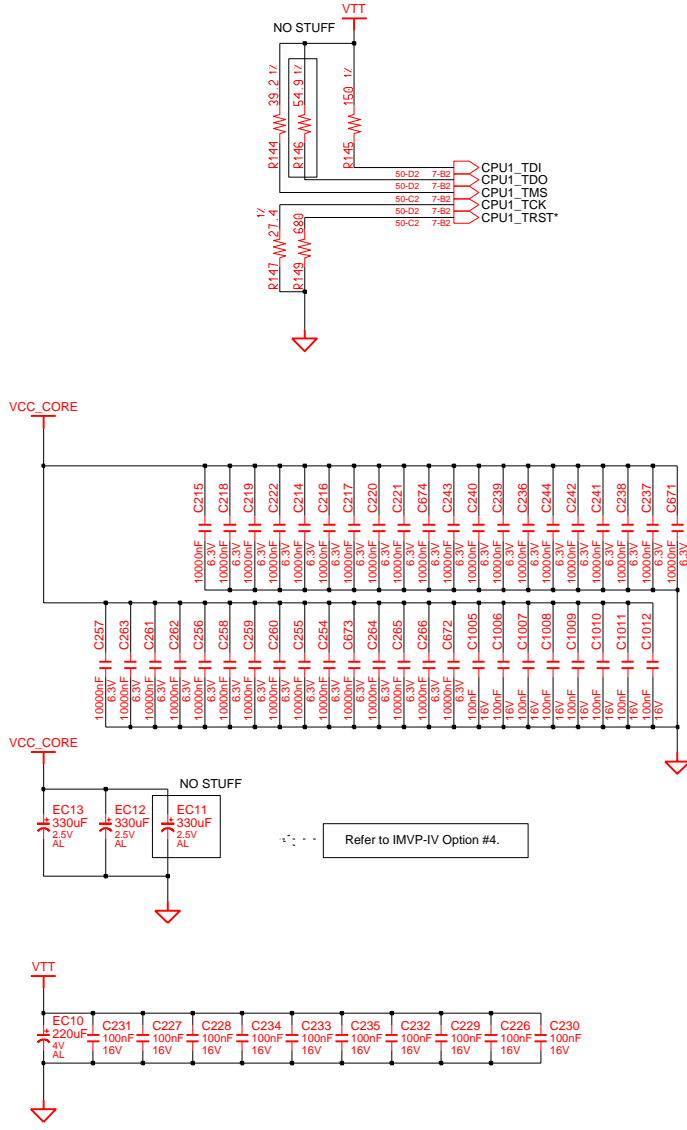
VID(5:0)	Voltage	VID(5:0)	Voltage
0 0 0 0 0 0	1.708 V	1 0 0 0 0 0	1.196 V
0 0 0 0 0 1	1.692 V	1 0 0 0 0 1	1.180 V
0 0 0 0 1 0	1.676 V	1 0 0 0 1 0	1.164 V
0 0 0 0 1 1	1.660 V	1 0 0 0 1 1	1.148 V
0 0 0 1 0 0	1.644 V	1 0 0 1 0 0	1.132 V
0 0 0 1 0 1	1.628 V	1 0 0 1 0 1	1.116 V
0 0 0 1 1 0	1.612 V	1 0 0 1 1 0	1.100 V
0 0 0 1 1 1	1.596 V	1 0 0 1 1 1	1.084 V
0 0 1 0 0 0	1.580 V	1 0 1 0 0 0	1.068 V
0 0 1 0 0 1	1.564 V	1 0 1 0 0 1	1.052 V
0 0 1 0 1 0	1.548 V	1 0 1 0 1 0	1.036 V
0 0 1 0 1 1	1.532 V	1 0 1 0 1 1	1.020 V
0 0 1 1 0 0	1.516 V	1 0 1 1 0 0	1.004 V
0 0 1 1 0 1	1.500 V	1 0 1 1 0 1	0.988 V
0 0 1 1 1 0	1.484 V	1 0 1 1 1 0	0.972 V
0 0 1 1 1 1	1.468 V	1 0 1 1 1 1	0.956 V
0 1 0 0 0 0	1.452 V	1 1 0 0 0 0	0.940 V
0 1 0 0 0 1	1.436 V	1 1 0 0 0 1	0.924 V
0 1 0 0 1 0	1.420 V	1 1 0 0 1 0	0.908 V
0 1 0 0 1 1	1.404 V	1 1 0 0 1 1	0.892 V
0 1 0 1 0 0	1.388 V	1 1 0 1 0 0	0.876 V
0 1 0 1 0 1	1.372 V	1 1 0 1 0 1	0.860 V
0 1 0 1 1 0	1.356 V	1 1 0 1 1 0	0.844 V
0 1 0 1 1 1	1.340 V	1 1 0 1 1 1	0.828 V
0 1 1 0 0 0	1.324 V	1 1 1 0 0 0	0.812 V
0 1 1 0 0 1	1.308 V	1 1 1 0 0 1	0.796 V
0 1 1 0 1 0	1.292 V	1 1 1 0 1 0	0.780 V
0 1 1 0 1 1	1.276 V	1 1 1 0 1 1	0.764 V
0 1 1 1 0 0	1.260 V	1 1 1 1 0 0	0.748 V
0 1 1 1 0 1	1.244 V	1 1 1 1 0 1	0.732 V
0 1 1 1 1 0	1.228 V	1 1 1 1 1 0	0.716 V
0 1 1 1 1 1	1.212 V	1 1 1 1 1 1	0.700 V

Highest Freq. of Dothan400(1.8GHz)
 * Highest Freq. of Dothan533(?? GHz : TBD)

DRAW	KYUNGIL, KI	DATE	11/5/2004	TITLE	CYGNUS MAIN	SAMSUNG ELECTRONICS
CHECK	BIN, KK	DEV. STEP	PR			
APPROVAL	KIM, DW	REV	1.0		DOTHAN CPU(2/3)	PART NO. BA41-00450A
MODULE CODE		LAST EDIT	November 5, 2004 8:10:03 PM	PAGE	7	OF 51

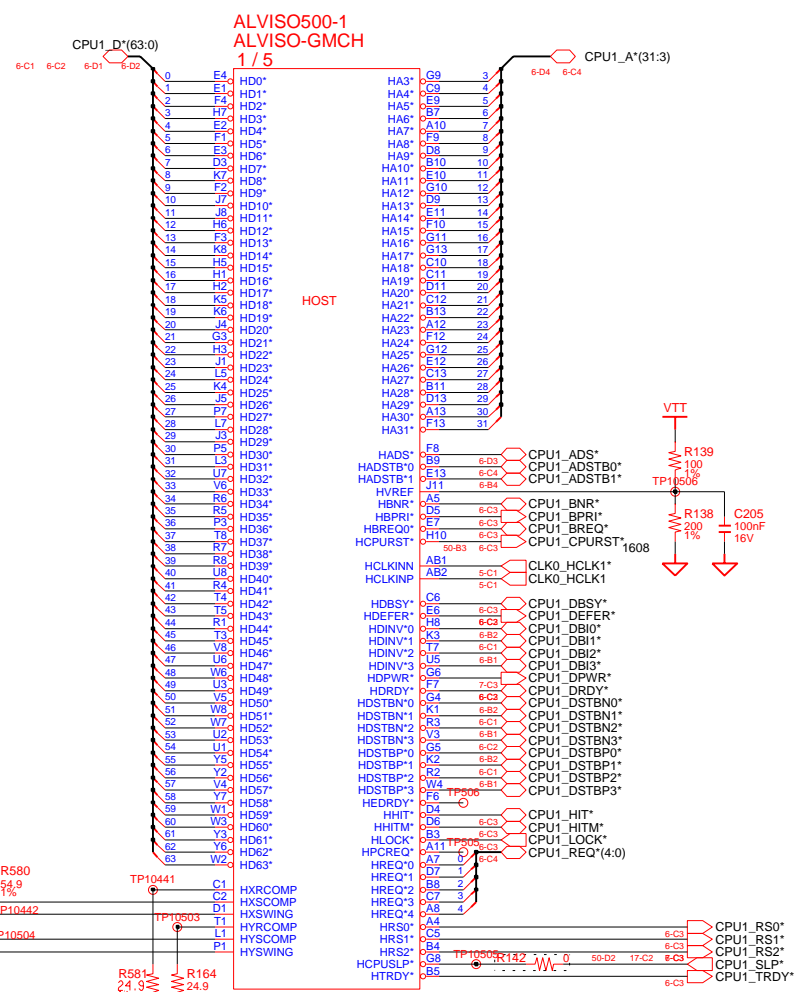
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Refer to Sonoma Platform Design Guide(4.6.1.4)



DRAW	KYUNGIL, KI	DATE	11/5/2004	TITLE	CYGNUS MAIN	SAMSUNG ELECTRONICS
CHECK	BIN, KK	DEV. STEP	PR	DOTHAN CPU(3/3)		
APPROVAL	KIM, DW	REV	1.0	November 5, 2004 8:10:03 PM		PART NO. BA41-00450A
MODULE CODE		LAST EDIT		PAGE	8	OF 51

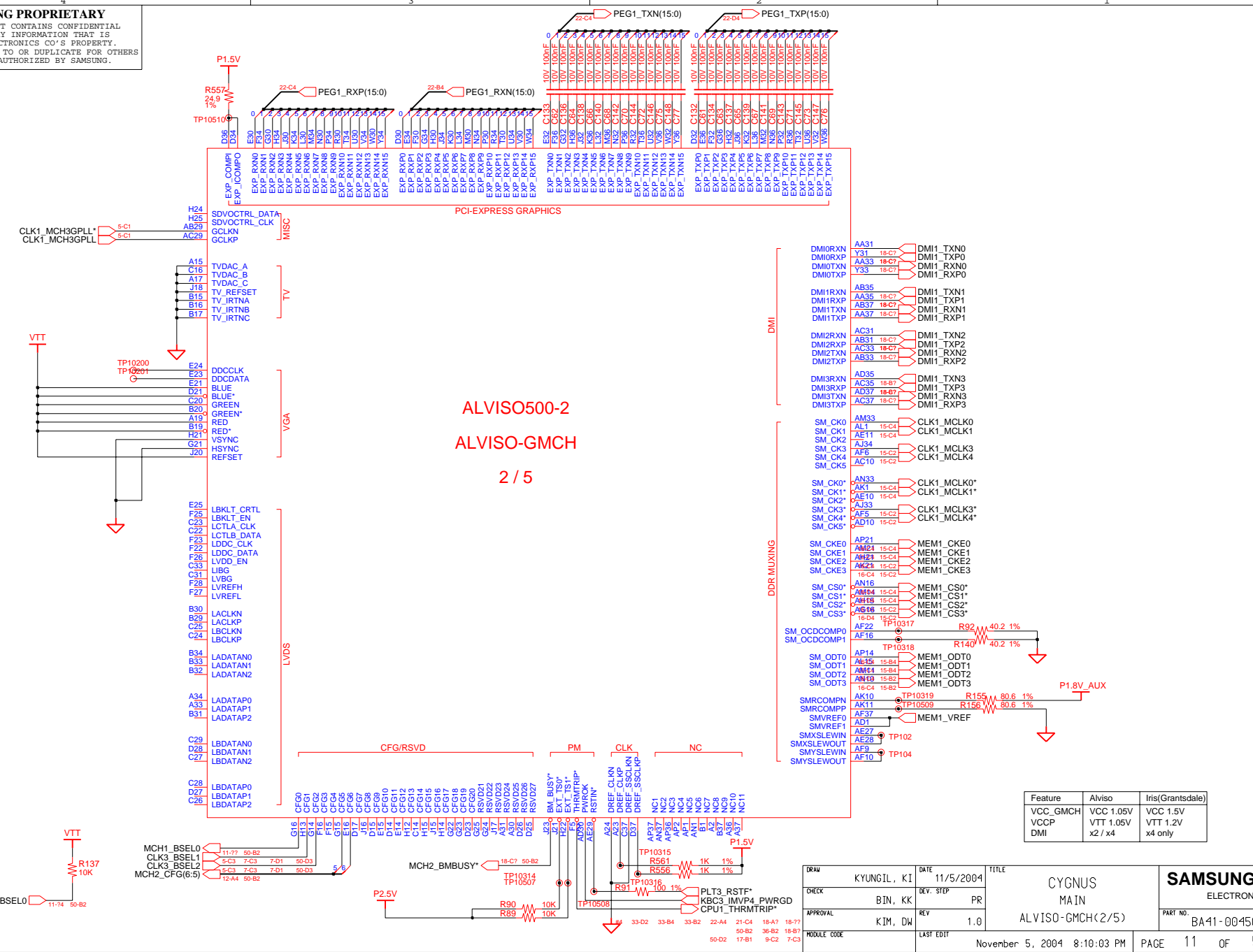
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Dothan A stepping : Stuff resistor on SLP* of ICH6
 Dothan B stepping : Stuff resistor on SLP* of Alviso

DRAW	KYUNGIL, KI	DATE	11/5/2004	TITLE	CYGNUS MAIN ALVISO-GMCH(1/5)	SAMSUNG ELECTRONICS
CHECK	BIN, KK	DEV. STEP	PR	REV	1.0	
APPROVAL	KIM, DW	REV	1.0	LAST EDIT	November 5, 2004 8:10:03 PM	PART NO. BA41-00450A
MODULE CODE		LAST EDIT				PAGE 10 OF 51

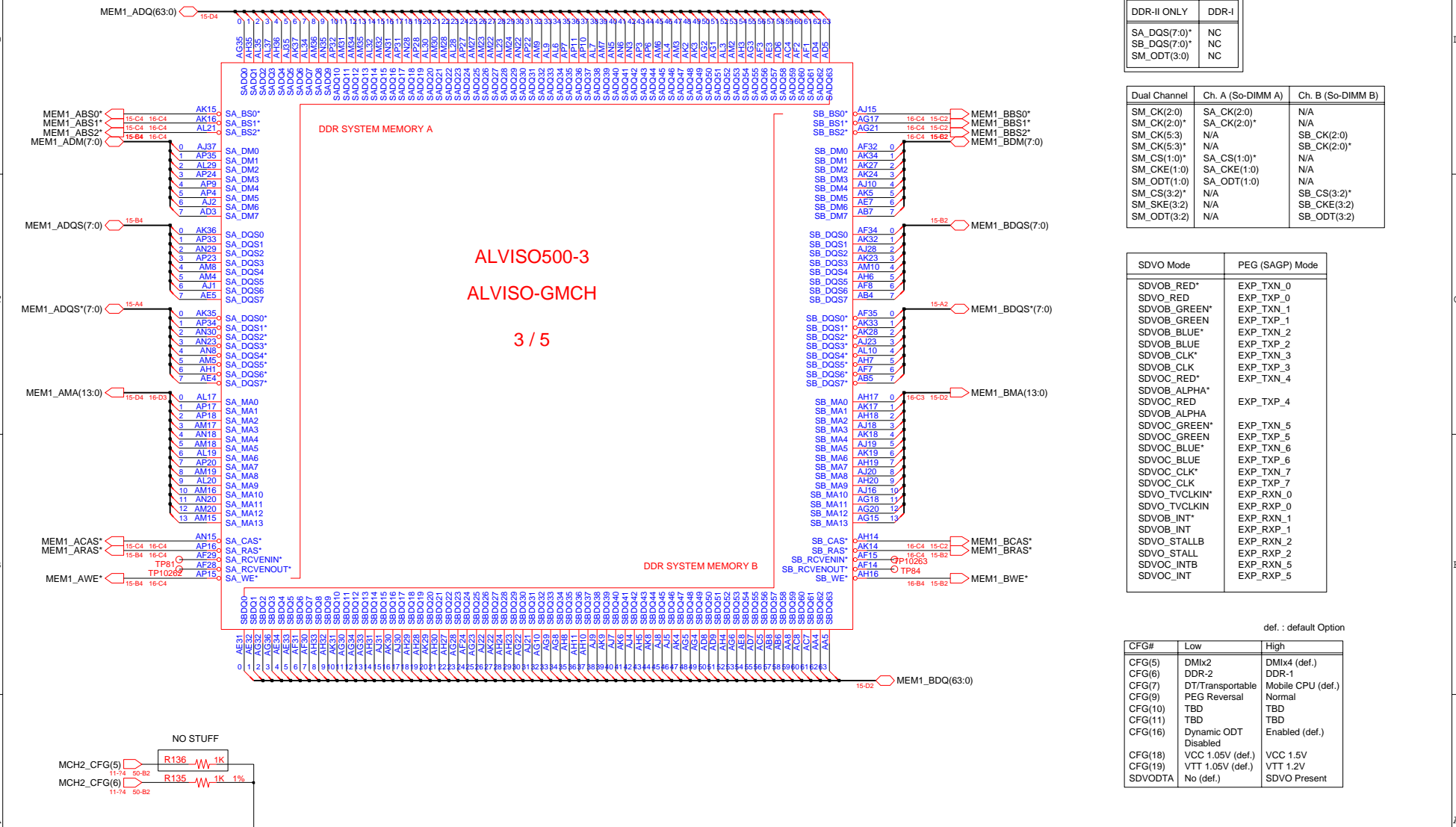
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Feature	Alviso	Iris(Grantsdale)
VCC_GMCH	VCC 1.05V	VCC 1.5V
VCCP	VTT 1.05V	VTT 1.2V
DMI	x2 / x4	x4 only

DRAW	KYUNGIL, KI	DATE	11/5/2004	TITLE	CYGNUS MAIN ALVISO-GMCH(2/5)	SAMSUNG ELECTRONICS PART NO. BA41-00450A
CHECK	BIN, KK	DEV. STEP	PR	REV	1.0	
APPROVAL	KIM, DW	REV	1.0	LAST EDIT	November 5, 2004 8:10:03 PM	
MODULE CODE						

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DDR-II ONLY	DDR-I
SA_DQS(7:0)*	NC
SB_DQS(7:0)*	NC
SM_ODT(3:0)	NC

Dual Channel	Ch. A (So-DIMM A)	Ch. B (So-DIMM B)
SM_CK(2:0)	SA_CK(2:0)	N/A
SM_CK(2:0)*	SA_CK(2:0)*	N/A
SM_CK(5:3)	N/A	SB_CK(2:0)
SM_CK(5:3)*	N/A	SB_CK(2:0)*
SM_CS(1:0)	SA_CS(1:0)*	N/A
SM_CKE(1:0)	SA_CKE(1:0)	N/A
SM_ODT(1:0)	SA_ODT(1:0)	N/A
SM_CS(3:2)*	N/A	SB_CS(3:2)*
SM_SKE(3:2)	N/A	SB_CKE(3:2)
SM_ODT(3:2)	N/A	SB_ODT(3:2)

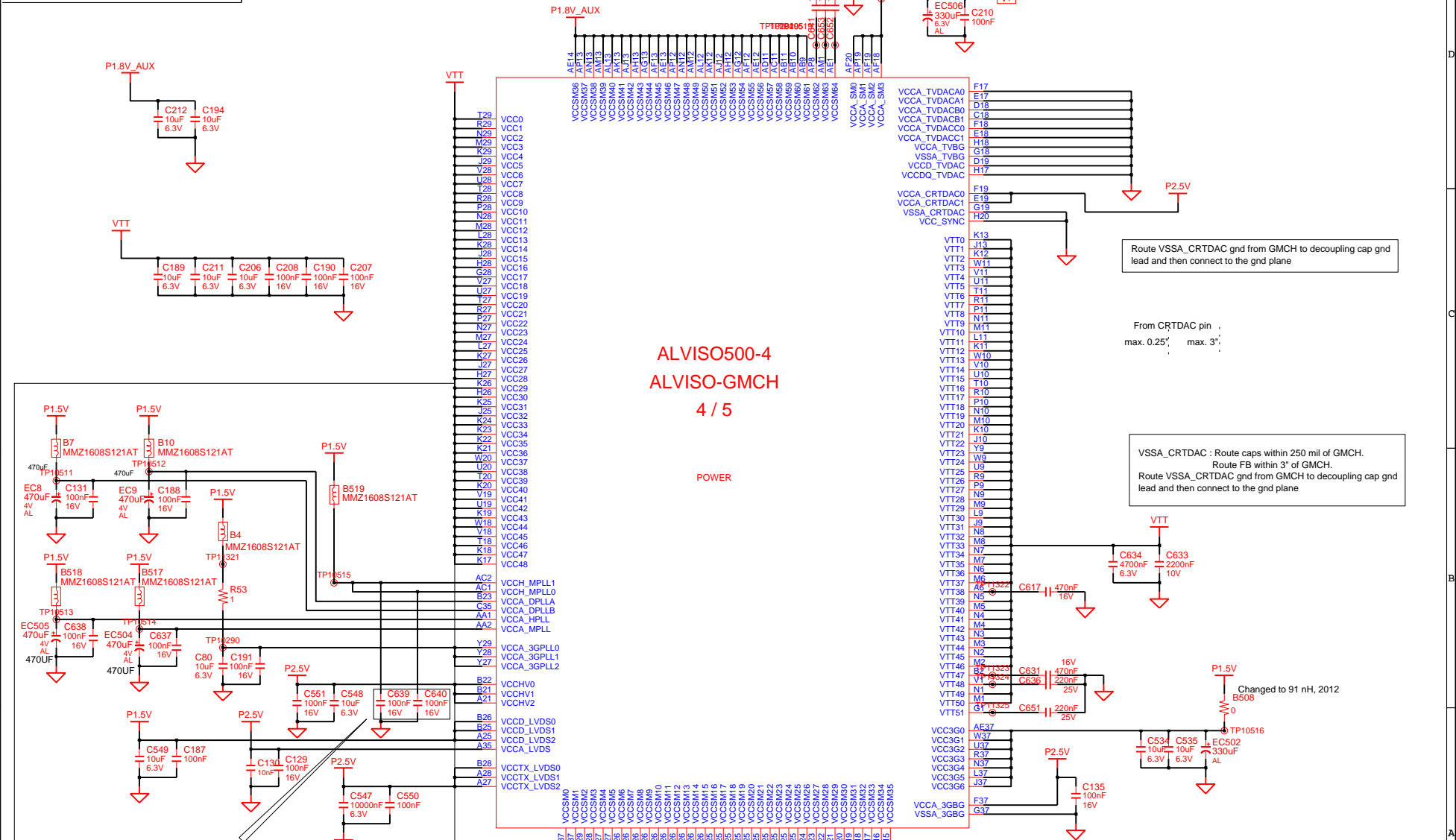
SDVO Mode	PEG (SAGP) Mode
SDVOB_RED*	EXP_TXN_0
SDVO_RED	EXP_TXP_0
SDVOB_GREEN*	EXP_TXN_1
SDVOB_GREEN	EXP_TXP_1
SDVOB_BLUE*	EXP_TXN_2
SDVOB_BLUE	EXP_TXP_2
SDVOB_CLK*	EXP_TXN_3
SDVOB_CLK	EXP_TXP_3
SDVOC_RED*	EXP_TXN_4
SDVOC_ALPHA*	
SDVOC_RED	EXP_TXP_4
SDVOC_ALPHA	
SDVOC_GREEN*	EXP_TXN_5
SDVOC_GREEN	EXP_TXP_5
SDVOC_BLUE*	EXP_TXN_6
SDVOC_BLUE	EXP_TXP_6
SDVOC_CLK*	EXP_TXN_7
SDVOC_CLK	EXP_TXP_7
SDVO_TVCLKIN*	EXP_RXN_0
SDVO_TVCLKIN	EXP_RXP_0
SDVOB_INT*	EXP_RXN_1
SDVOB_INT	EXP_RXP_1
SDVO_STALLB	EXP_RXN_2
SDVO_STALL	EXP_RXP_2
SDVOC_INTB	EXP_RXN_5
SDVOC_INT	EXP_RXP_5

def. : default Option

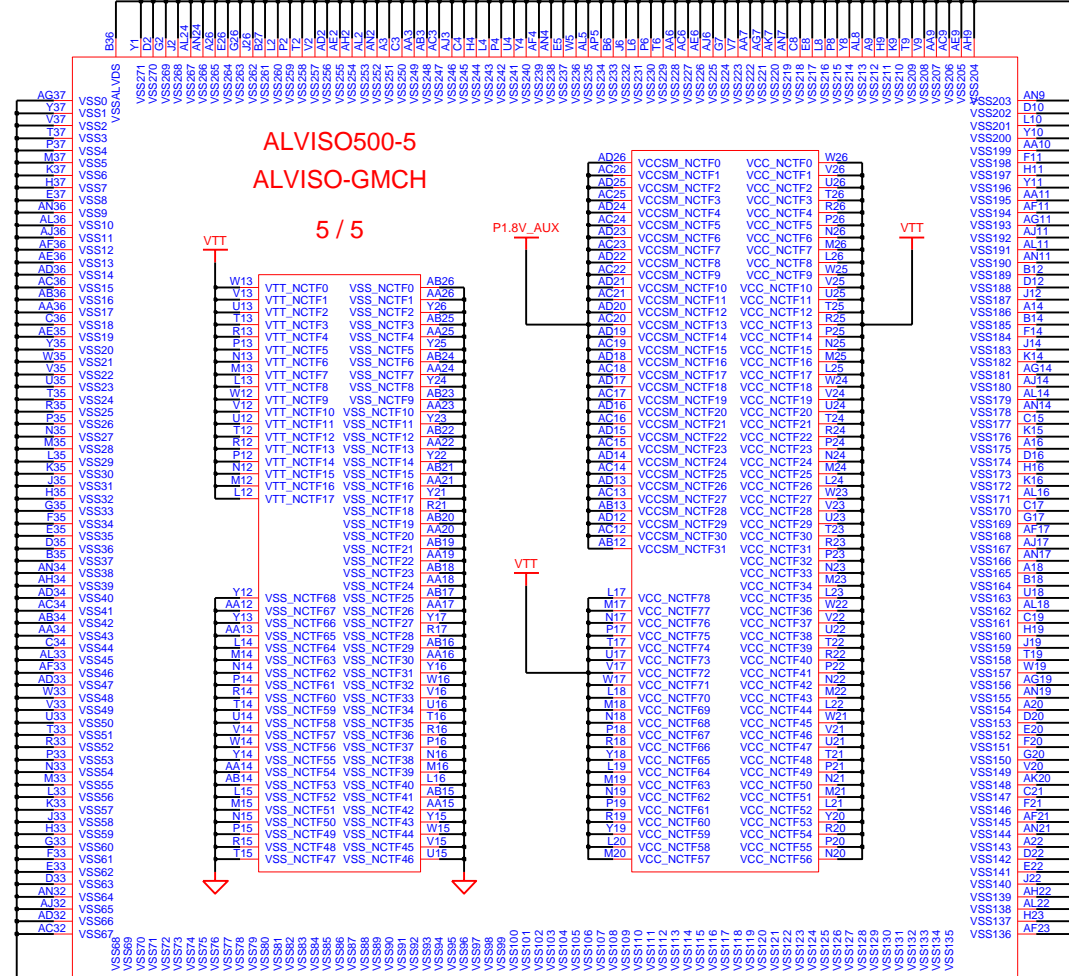
CFG#	Low	High
CFG(5)	DMIM2	DMIM4 (def.)
CFG(6)	DDR-2	DDR-1
CFG(7)	DT/Transportable	Mobile CPU (def.)
CFG(9)	PEG Reversal	Normal
CFG(10)	TBD	TBD
CFG(11)	TBD	TBD
CFG(16)	Dynamic ODT Disabled	Enabled (def.)
CFG(18)	VCC 1.05V (def.)	VCC 1.5V
CFG(19)	VTT 1.05V (def.)	VTT 1.2V
SDVODTA	No (def.)	SDVO Present

DRAW	KYUNGIL, KI	DATE	11/5/2004	TITLE	CYGNUS	SAMSUNG ELECTRONICS
CHECK	BIN, KK	DEV. STEP	PR	MAIN	PART NO.	
APPROVAL	KIM, DW	REV	1.0	ALVISO-GMCH(3/5)	BA41-00450A	
MODULE CODE		LAST EDIT	November 5, 2004 8:10:03 PM	PAGE	12 OF 51	

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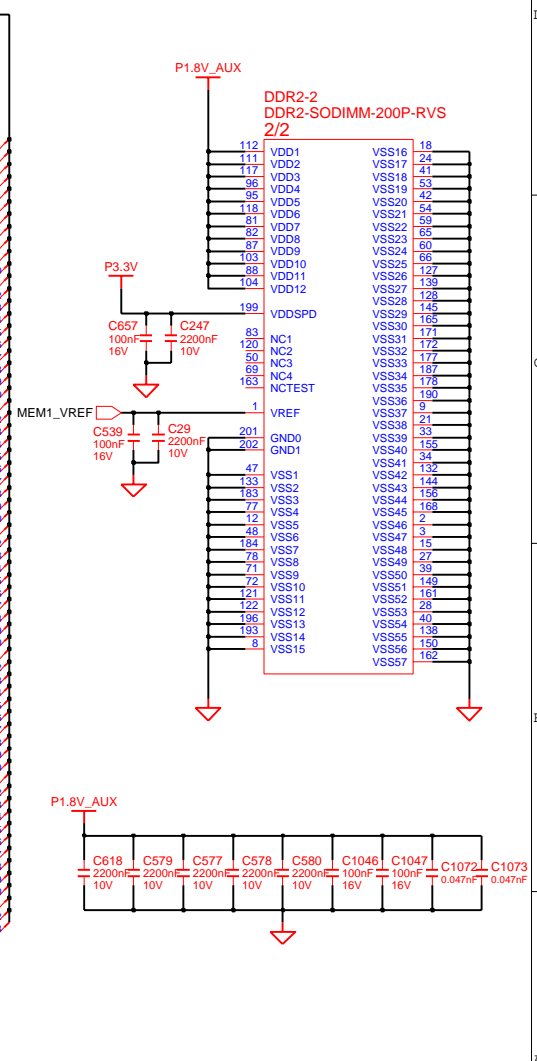
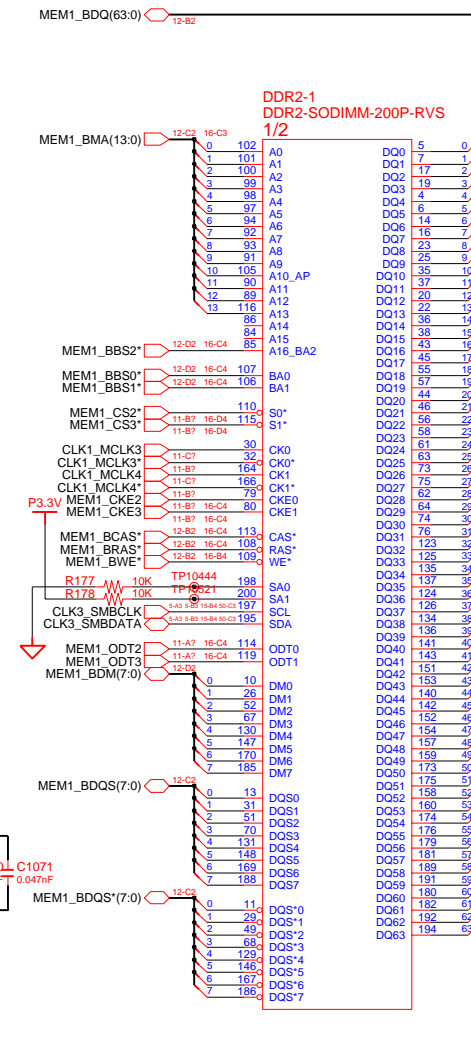
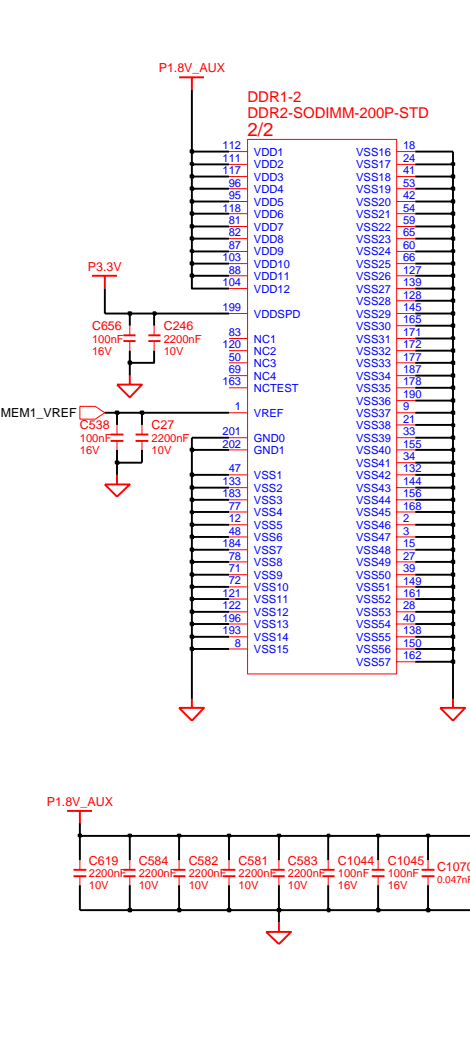
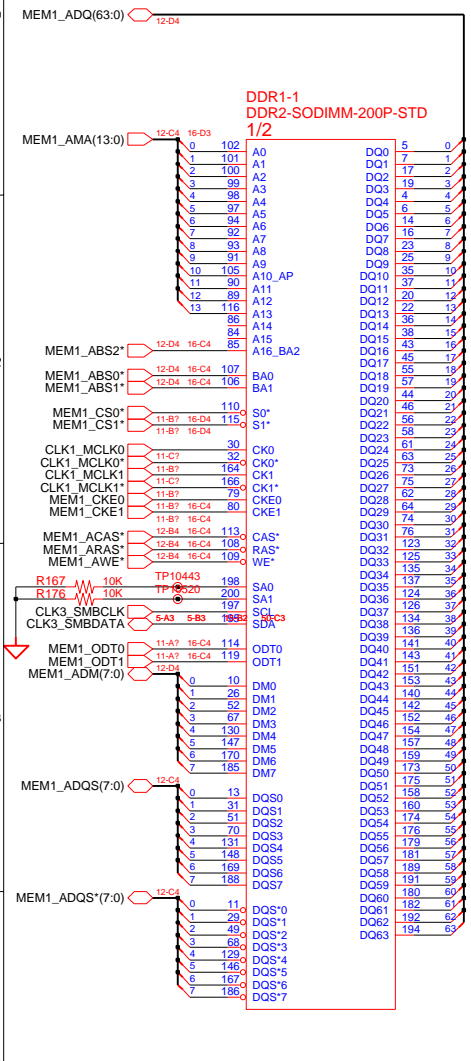


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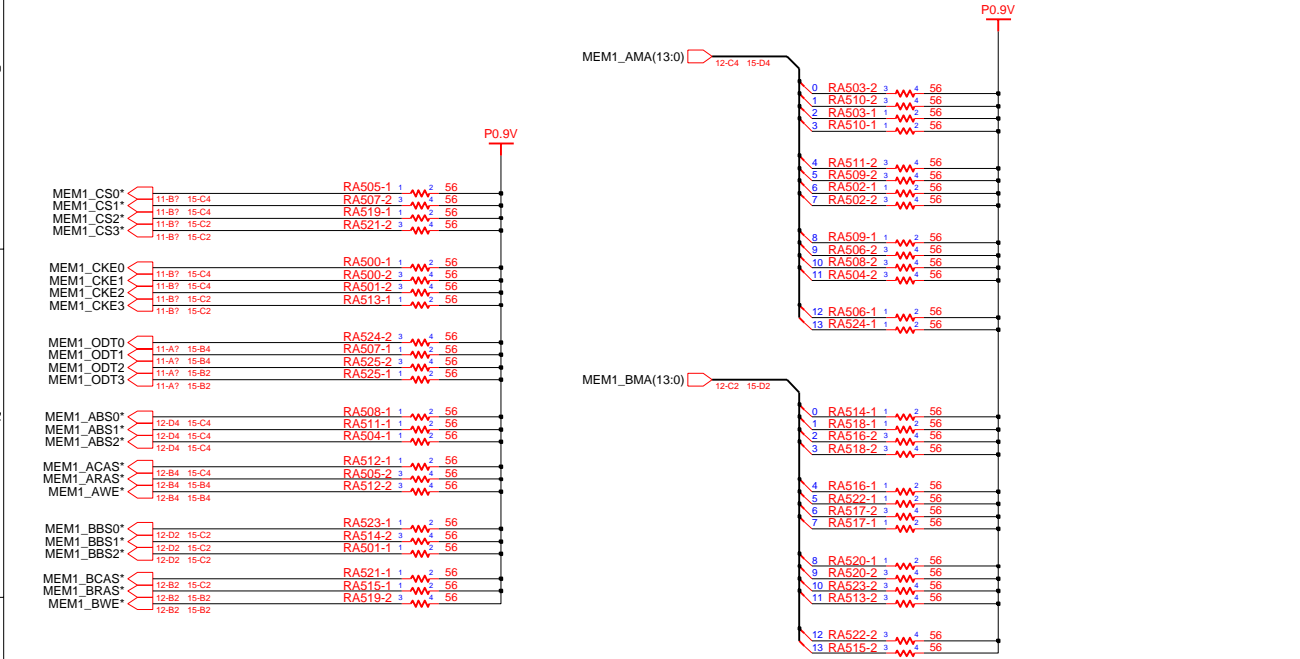
DRAW	KYUNGIL, KI	DATE	11/5/2004	TITLE	CYGNUS MAIN ALVISO-GMCH(5/5)	SAMSUNG ELECTRONICS PART NO. BA41-00450A	
CHECK	BIN, KK	DEV. STEP	PR				
APPROVAL	KIM, DW	REV	1.0				
MODULE CODE		LAST EDIT	November 5, 2004 8:10:03 PM	PAGE			14 OF 51

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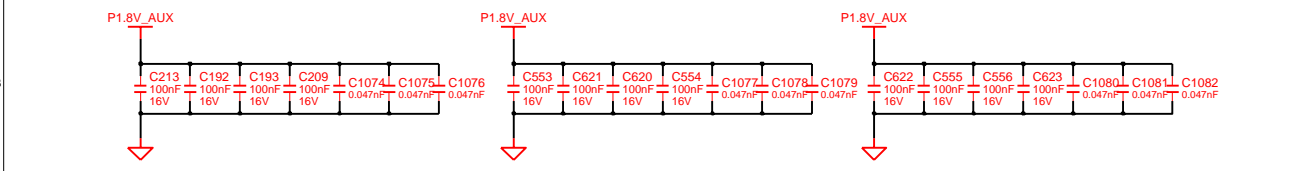
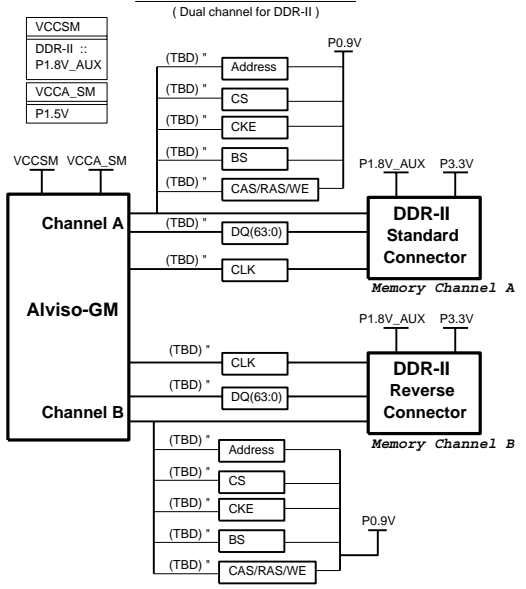


DRAW	KYUNGIL, KI	DATE	11/5/2004	TITLE	CYGNUS	SAMSUNG ELECTRONICS
CHECK	BIN, KK	DEV. STEP	PR	MAIN	PART NO.	
APPROVAL	KIM, DW	REV	1.0	DDR - SODIMM	BA41-00450A	
MODULE CODE		LAST EDIT	November 5, 2004 8:10:03 PM	PAGE	15 OF 51	

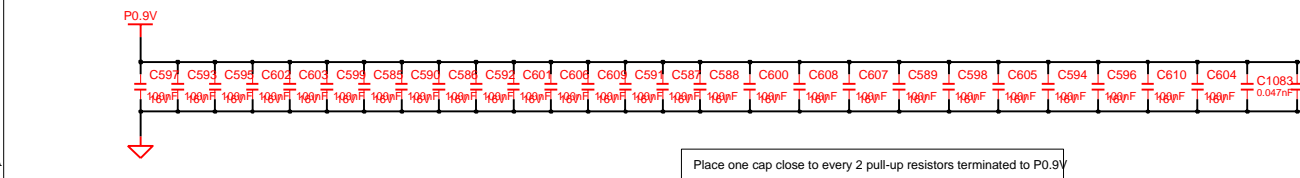
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Memory Topology



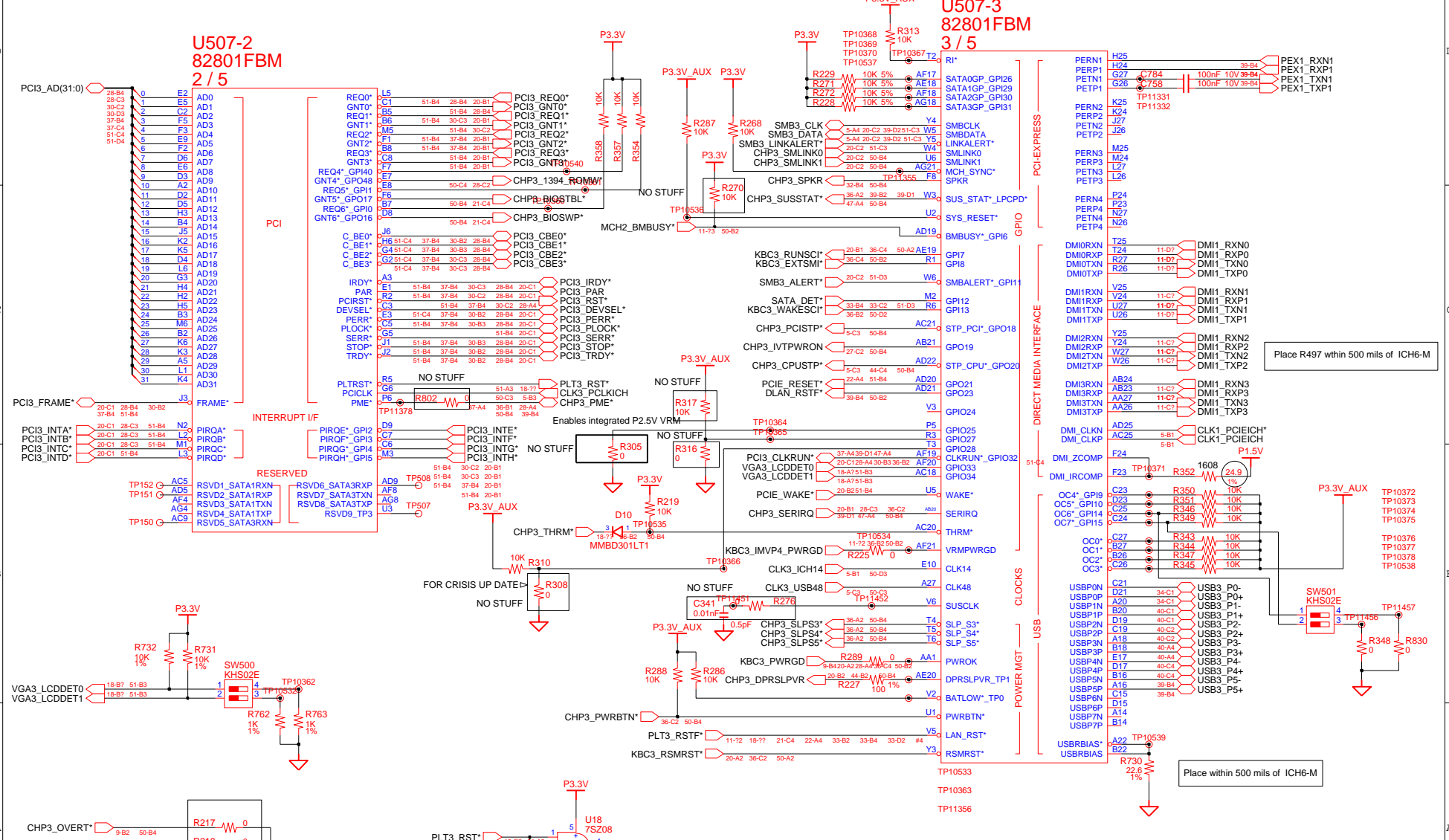
Place near GMCH Place near SO-DIMM0 Place near SO-DIMM1



Place one cap close to every 2 pull-up resistors terminated to P0.9V

DRAW	KYUNGIL, KI	DATE	11/5/2004	TITLE	CYGNUS MAIN	SAMSUNG ELECTRONICS
CHECK	BIN, KK	DEV. STEP	PR	REV	1.0	
APPROVAL	KIM, DW	REV	1.0	DDR - TERMINATION		PART NO. BA41-00450A
MODULE CODE		LAST EDIT	November 5, 2004 8:10:03 PM	PAGE	16	OF 51

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CHECK	BIN, KK	DEV. STEP	PR		MAIN	
APPROVAL	KIM, DW	REV	1.0		ICHG - M(2/4)	PART NO. BA41-00450A
MODULE CODE		LAST EDIT			November 5, 2004 8:10:03 PM	PAGE 18 OF 51

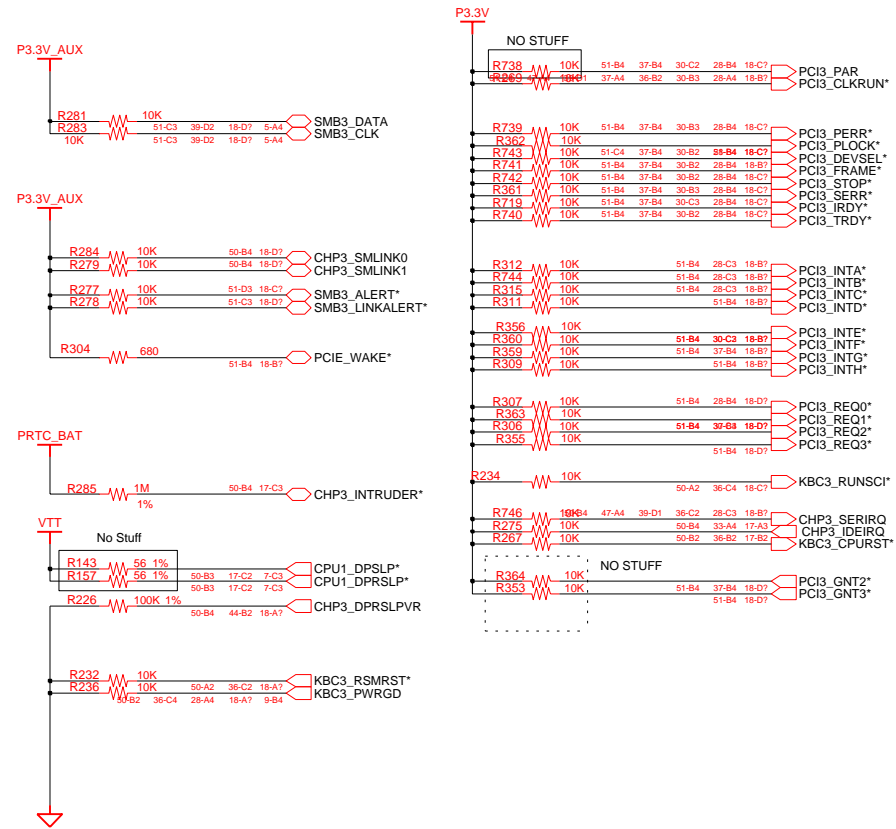
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ICH6-m Strapping Options

	Function	Default
CHP3_SPKR	No Reboot	No Stuff
CHP3_BIOSWP*	Boot BIOS	No Stuff
PC/PCI_GNTA*	A16 swap override	No Stuff
AC97_SDOOUT	Safe Mode	TBD
ECP_DOUT		TBD

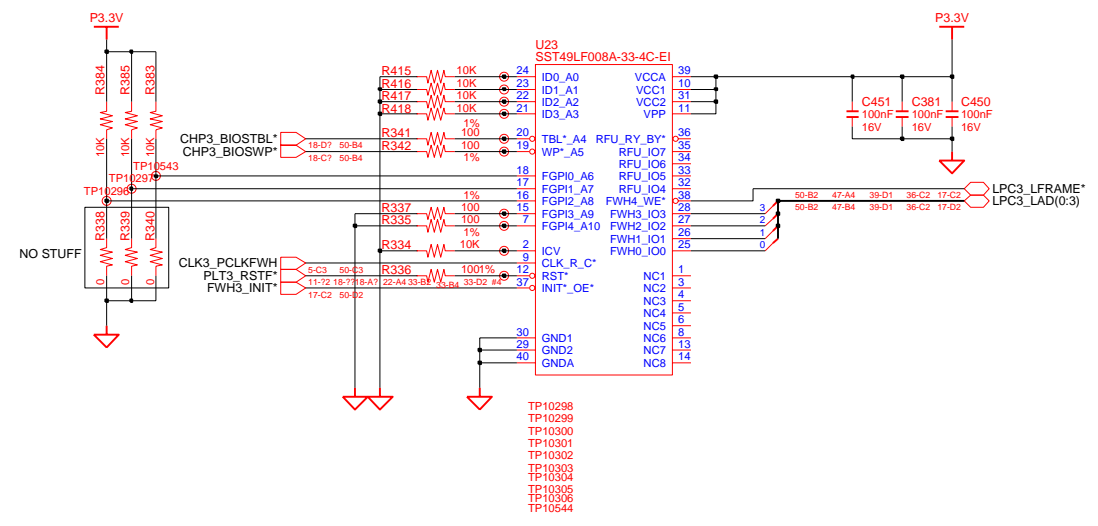
U507-5 82801FBM 5 / 5

AG22	VSS_172	VSS_86	P22
AG20	VSS_171	VSS_85	P16
AG17	VSS_170	VSS_84	P15
AG14	VSS_169	VSS_83	P14
AG12	VSS_168	VSS_82	P13
AG7	VSS_167	VSS_81	P12
AG3	VSS_166	VSS_80	N17
AG1	VSS_165	VSS_79	N16
AF26	VSS_164	VSS_78	N15
AF12	VSS_163	VSS_77	N14
AF10	VSS_162	VSS_76	N13
AF7	VSS_161	VSS_75	N12
AF3	VSS_160	VSS_74	N11
AF1	VSS_159	VSS_73	N7
AE25	VSS_158	VSS_72	N1
AE21	VSS_157	VSS_71	M27
AE11	VSS_156	VSS_70	M26
AE10	VSS_155	VSS_69	M23
AE7	VSS_154	VSS_68	M15
AE6	VSS_153	VSS_67	M14
AE2	VSS_152	VSS_66	M13
AD24	VSS_151	VSS_65	M12
AD18	VSS_150	VSS_64	M4
AD15	VSS_149	VSS_63	L25
AD6	VSS_148	VSS_62	L24
AD2	VSS_147	VSS_61	L15
AD1	VSS_146	VSS_60	L13
AC26	VSS_145	VSS_59	K27
AC23	VSS_144	VSS_58	K26
AC12	VSS_143	VSS_57	K7
AC6	VSS_142	VSS_56	K1
AC2	VSS_141	VSS_55	J25
AC10	VSS_140	VSS_54	J24
AC6	VSS_139	VSS_53	J4
AC3	VSS_138	VSS_52	J23
AB9	VSS_137	VSS_51	J22
AB7	VSS_136	VSS_50	J4
AB2	VSS_135	VSS_49	H27
AB1	VSS_134	VSS_48	H25
AA16	VSS_133	VSS_47	H23
AA13	VSS_132	VSS_46	G21
AA11	VSS_131	VSS_45	G12
AA4	VSS_129	VSS_44	G9
Y27	VSS_128	VSS_43	G7
Y26	VSS_127	VSS_42	G1
Y23	VSS_126	VSS_41	F22
Y6	VSS_125	VSS_40	F19
W25	VSS_124	VSS_39	F17
W24	VSS_123	VSS_38	F4
W1	VSS_122	VSS_37	E27
V27	VSS_121	VSS_36	E25
V26	VSS_120	VSS_35	E18
V23	VSS_119	VSS_34	E15
V21	VSS_118	VSS_33	E14
V16	VSS_117	VSS_32	D22
V15	VSS_116	VSS_31	D20
V14	VSS_115	VSS_30	D19
U24	VSS_114	VSS_29	D14
U23	VSS_113	VSS_28	D13
U15	VSS_112	VSS_27	D10
U13	VSS_111	VSS_26	D10
U11	VSS_110	VSS_25	D1
T27	VSS_109	VSS_24	C21
T26	VSS_108	VSS_23	C20
T23	VSS_107	VSS_22	C22
T16	VSS_106	VSS_21	C12
T15	VSS_105	VSS_20	C14
T14	VSS_104	VSS_19	C4
T13	VSS_103	VSS_18	B25
T12	VSS_102	VSS_17	B24
T11	VSS_101	VSS_16	B23
T7	VSS_100	VSS_15	B21
R25	VSS_99	VSS_14	B19
R24	VSS_98	VSS_13	B15
R23	VSS_97	VSS_12	B14
R17	VSS_96	VSS_11	A26
R16	VSS_95	VSS_10	A23
R15	VSS_94	VSS_9	A21
R14	VSS_93	VSS_8	A19
R13	VSS_92	VSS_7	A15
R12	VSS_91	VSS_6	A12
R11	VSS_90	VSS_5	A9
R4	VSS_89	VSS_4	A7
	VSS_88	VSS_3	A4
	VSS_87	VSS_2	A1



DRAW	KYUNGIL, KI	DATE	11/5/2004	TITLE	CYGNUS MAIN	SAMSUNG ELECTRONICS
CHECK	BIN, KK	DEV. STEP	PR	ICH6 - M(4/4)	PART NO.	
APPROVAL	KIM, DW	REV	1.0	November 5, 2004 8:10:03 PM	PAGE	20 OF 51
MODULE CODE		LAST EDIT				

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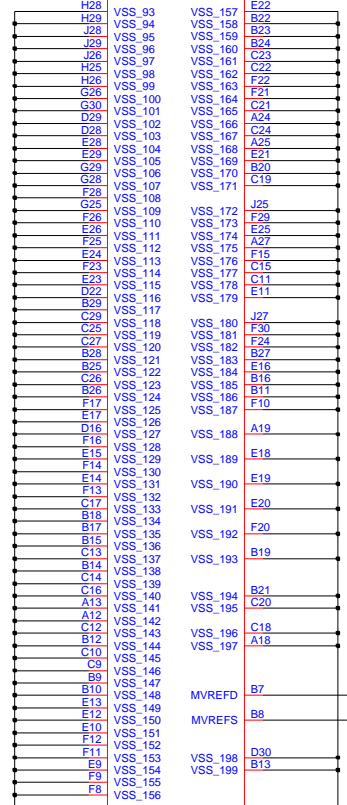


02	VERIFY REAL MODE	66	CONFIGURE ADVANCE CACHE REG.
03	DISABLE NMI	6A	DISPLAY EXTERNAL CACHE SIZE
04	GET CPU TYPE	6C	DISPLAY SHADOW MESSAGE
06	INIT. SYSTEM H/W	6E	DISPLAY NON-DISPOSABLE SEGMENT
08	INIT. CHIPSET REG.	70	DISPLAY ERROR MESSAGE
09	SET IN POST FLAG	72	CHECK FOR CONFIGURATION ERROR
0A	INIT CPU.REG	74	TEST REAL-TIME CLOCK
0B	CPU CACHE ON	76	CHECK FOR KEYBOARD ERROR
0C	INIT.CACHE TO POST	7C	SETUP HARDWARE INTERRUPT VECTOR
0E	INIT. I/O VALUE	7E	TEST COPROCESSER IF PRESENT
0F	ENABLE THE L-BUS IDE	80	DISABLE ON-BOARD I/O PORT
10	INIT. POWER MANAGER	82	DETECT AND INSTALL EXT.RS232C
11	LOAD ALTERNATE REG.	84	DETECT AND INSTALL EXT.PARALLEL
13	PCI BUS MASTER RESET WITH INITIAL POST VALUE	86	RE-INIT. ON-BOARD I/O PORT
14	INIT. KEYBOARD CONTROLLER	88	INIT. BIOS DATA ROM
16	CHECK CHECKSUM	8A	INIT.EXTENDED BIOS DATA AREA
18	8254 TIMER INIT.	8C	INIT. FDD CONTROLLER
1A	8237 DMA CONTROLLER INIT.	9A	SHADOW OPTION ROMS
1C	RESET INTERRUPT CONTROLLER	9C	SETUP POWER MANAGEMENT
20	TEST DRAM REFRESH	9E	ENABLE H/W INTERRUPT
22	TEST 8742 KEYBOARD CONTROLLER	A0	SET TIME OF DAY
24	SET ES SEGMENT REG. TO 4GB	A4	INIT. TYPOMATIC RATE
26	ENABLE A20	A8	ERASE F2 PROMPT
28	AUTO SIZING DRAM	AA	SCAN FOR F2 KEY STROKE
32	COMPUTE THE CPU SPEED	AC	ENTER SETUP
34	TESET CMOS RAM	AE	CLEAR IN POST FLAG
38	SHADOW SYSTEM BIOS ROM	B0	CHECK FOR ERRORS
3A	AUTO SIZING CACHE	B2	POST DONE-PREPARE TO BOOT O/S
3C	CONFIGURE ADVANCED CHIPSET REG.	B4	ONE BEEP
42	INIT. INTERRUPT VECTOR	B6	CHECK PASSWORD (OPTION)
44	INIT. BIOS INTERRUPT	B7	ACPI INIT
46	CHECK ROM COPYRIGHT NOTICE	BA	DMI INIT
47	INIT. I20 SUPPORT IF INSTALLED	BE	CLEAR SCREEN
48	CHECK VIDEO CONFIGURE AGAINST CMOS	C0	TRY BOOT WITH INT19
49	INIT. PCI BUS AND DEVICE	D0	INTERRUPT HANDLER ERROR
4A	INIT. ALL VIDEO BIOS ROM	D2	UNKNOWN INTERRUPT ERROR
4C	SHADOW VIDEO BIOS ROM	D4	PENDING INTERRUPT ERROR
50	DISPLAY CPU TYPE AND SPEED	D6	SHUTDOWN 5
52	TEST KEYBOARD	D8	SHUTDOWN ERROR
54	SET KEYCLICK IF ENABLED	DA	EXTENDED BLOCK MOVE
56	ENABLE KEYBOARD	DC	SHUTDOWN 10
58	TEST FOR UNEXPECTED INTERRUPTS	89	ENABLE NMI
5A	DISPLAY * PRESS SETUP*	90	INIT. HDD CONTROLLER
5C	TEST RAM BETWEEN 512K AND 640K	91	INIT. LOCAL BUS HDD CONTROLLER
60	TEST EXTENDED MEMORY	92	JUMP TO USER PATCH 2
62	TEST EXTENDED MEMORY ADDRESS LINE	94	DISABLE A20 ADDRESS LINE
64	JUMP TO USER PATCH 1	96	CLEAR HUGE ES SEGMENT REG.
		98	SEARCH FOR OPTION ROMS

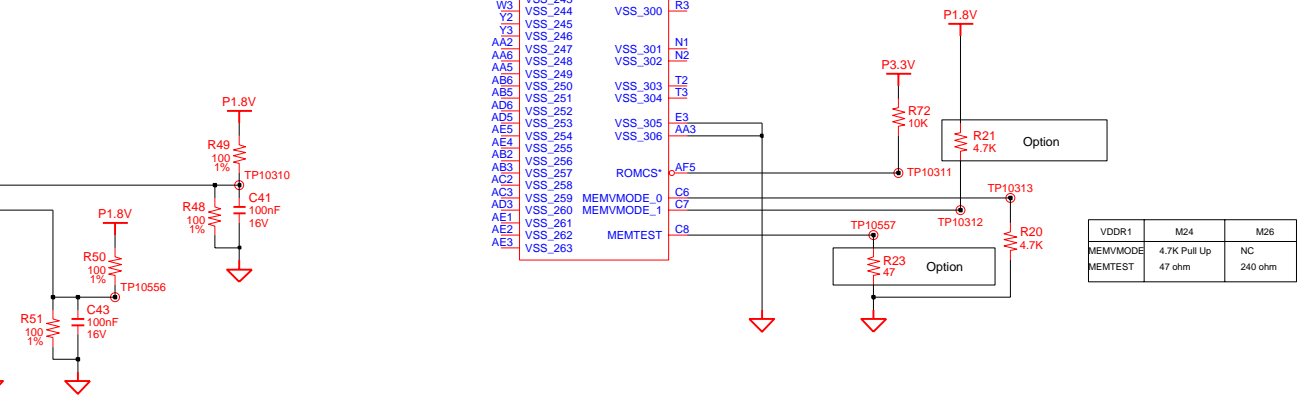
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CHECK	BIN, KK	DEV. STEP	PR			
APPROVAL	KIM, DW	REV	1.0			
MODULE CODE		LAST EDIT	November 5, 2004 8:10:03 PM	PAGE	21 OF 51	

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**GFX500-2
 M24-CSP64
 2 / 5**



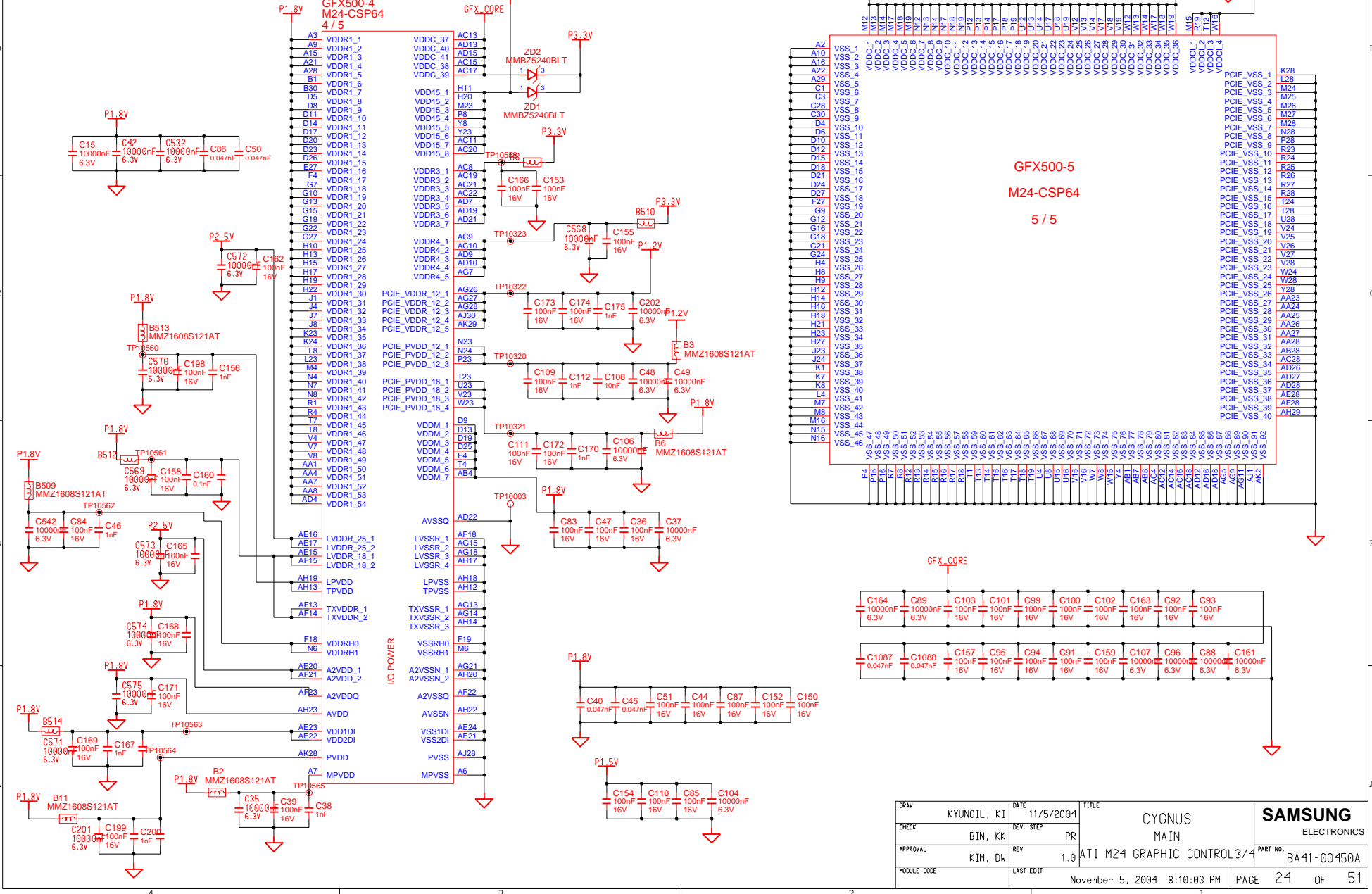
**GFX500-3
 M24-CSP64
 3 / 5**



VDDR1	M24	M26
MEMVMODE	4.7K Pull Up	NC
MEMTEST	47 ohm	240 ohm

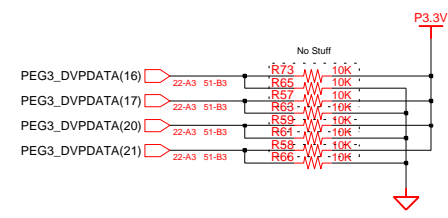
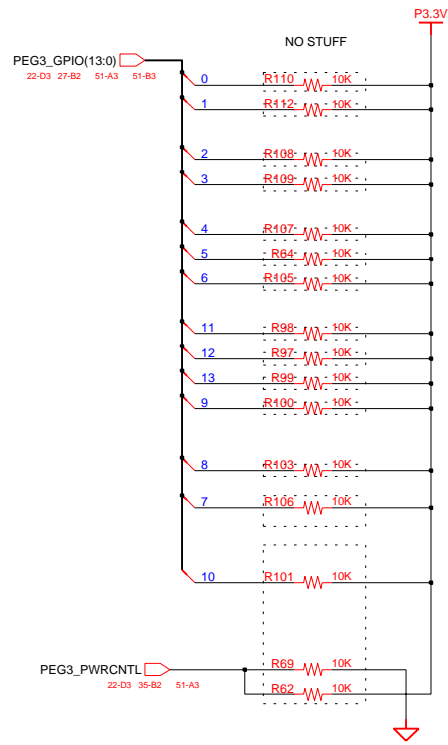
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APPROVAL	KIM, DW	REV	1.0		BA41-00450A	
MODULE CODE		LAST EDIT	November 5, 2004 8:10:03 PM	PAGE	23	OF 51

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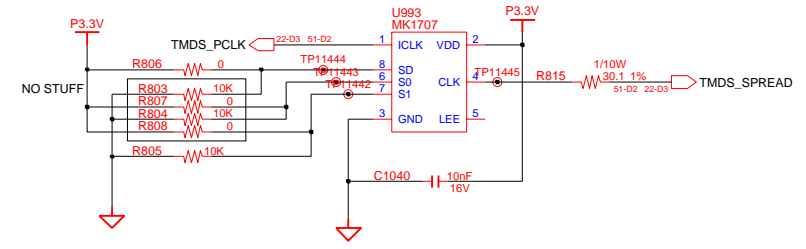


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MODULE CODE		LAST EDIT	November 5, 2004 8:10:03 PM	PAGE	24	OF 51

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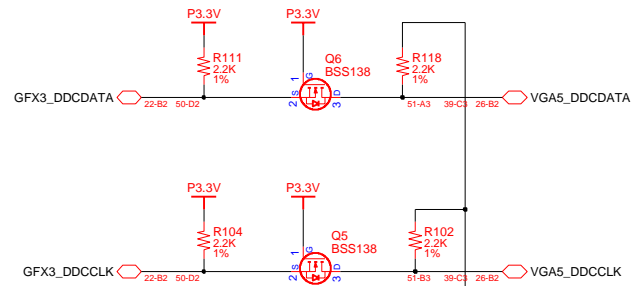
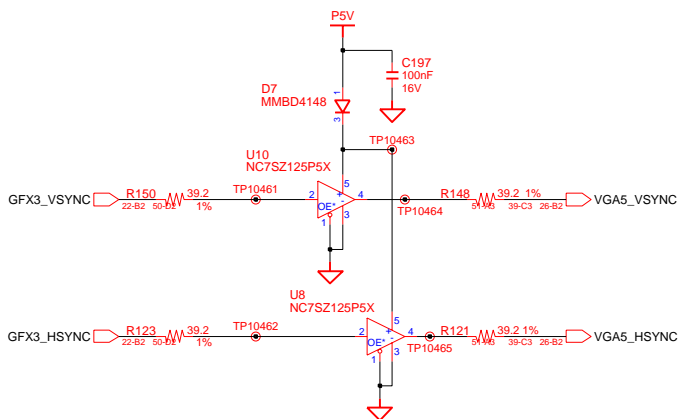


Straps	Pin Number	Descriptions
CAL_BG_BACKUP	GPIO0	PCI-Express Current Calibration Bandgap Backup 0 : use reference voltage from bandgap (Default) 1 : use reference voltage from resistor divider
PLL_CAL_FORCE_EN	GPIO1	PCI-Express PLL Calibration Force Enable 0 : Disable PLL force calibration (Default) 1 : Enable PLL force calibration
PCIE Mode(1:0)	GPIO(3:2)	PCI-Express Mode 00 : PCI Express 1.0A mode (Default) 01 : Reserved 10 : PCI Express 1.0 mode 11 : Reserved
CAL_OFF	GPIO4	Turn-Off PCI-Express Impedance / Strength Calibration 0 : Enable (Default) 1 : Disable Also, used to demux VCOREF / CALREF
BYPASS_PLL	GPIO5	Bypass PCI-Express PLL 0 : - (Default) 1 : -
ICOMP	GPIO6	PCI-Express Transmitter Current Compensation 0 : Normal (Default) 1 : Inject extra current for output buffer switching
ROMIDCFG(3:0)	GPIO(9,13:11)	If no ROM attached, controls chip IDs. 0000 : No ROM, CHG_ID = 0 0001 : No ROM, CHG_ID = 1 0100 : Reserved 0110 : Reserved Others : ROM (Third party vendors)
DEBUG_ACCESS	GPIO8	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible.

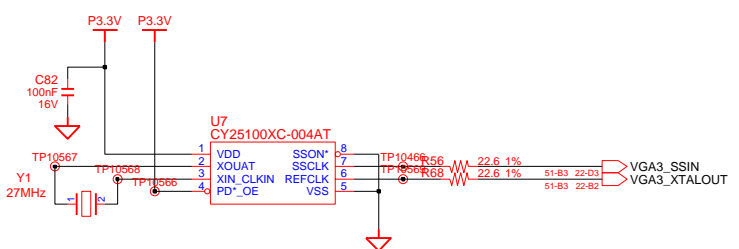
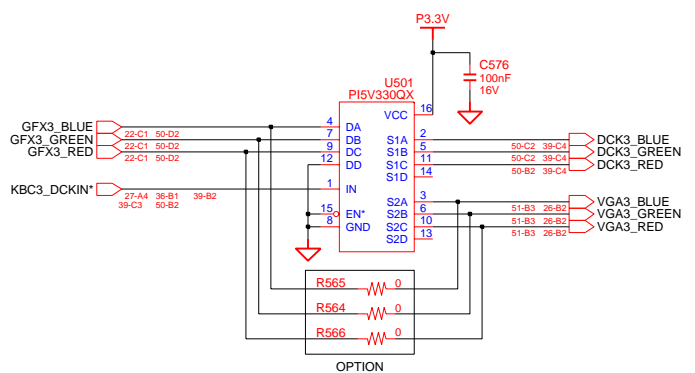
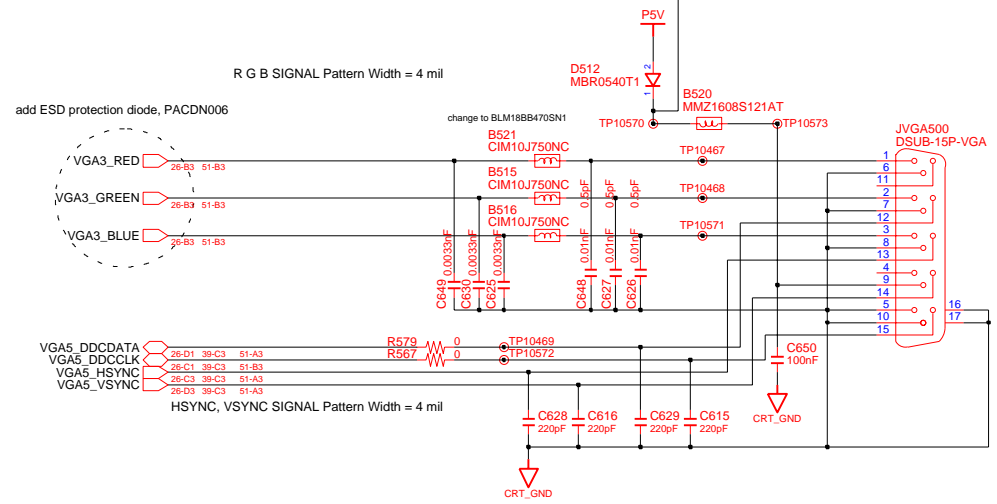


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CHECK	BIN, KK	DEV. STEP	PR	PART NO.		
APPROVAL	KIM, DW	REV	1.0	November 5, 2004 8:10:03 PM		PAGE 25 OF 51
MODULE CODE		LAST EDIT				

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CRT

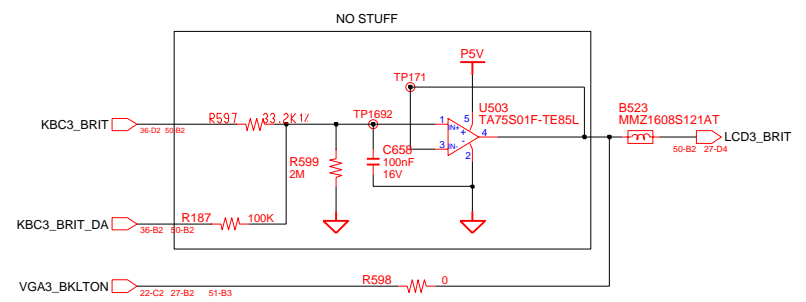
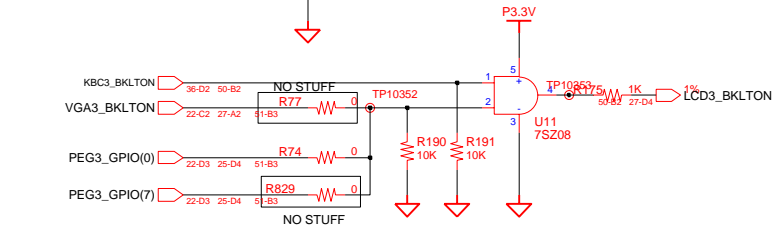
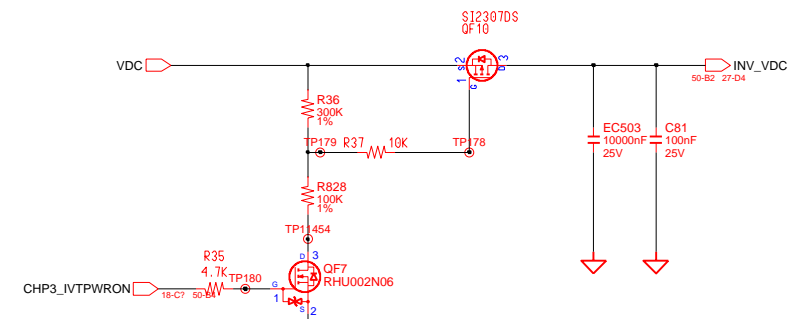
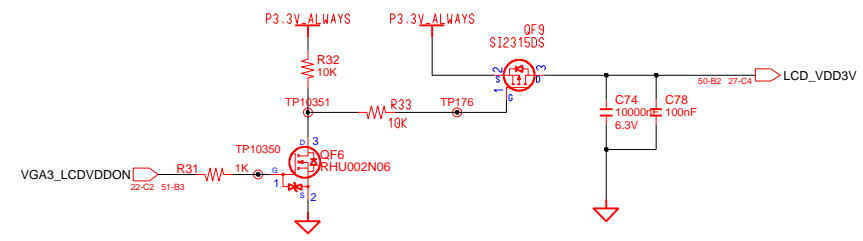
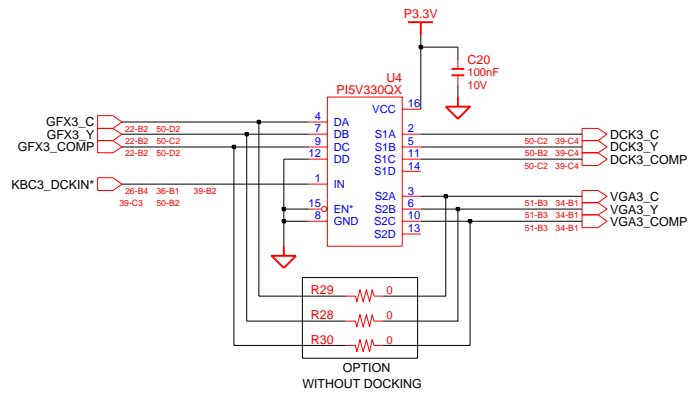
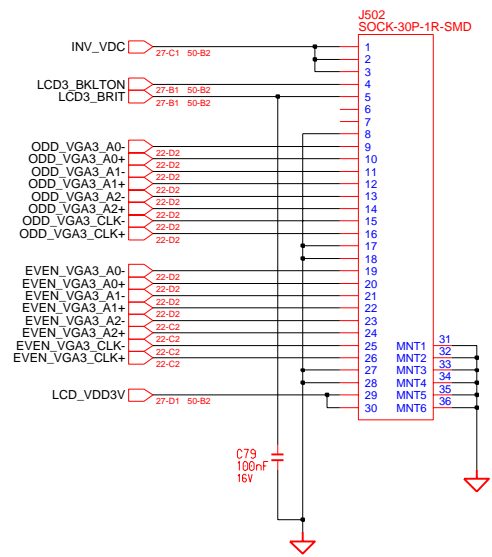


Optional External Thermal Sensor

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CHECK	BIN, KK	DEV. STEP	PR	CRT PORT/SPREAD SPECTRUM		
APPROVAL	KIM, DW	REV	1.0	PART NO. BA41-00450A		PAGE 26 OF 51
MODULE CODE		LAST EDIT	November 5, 2004 8:10:03 PM			

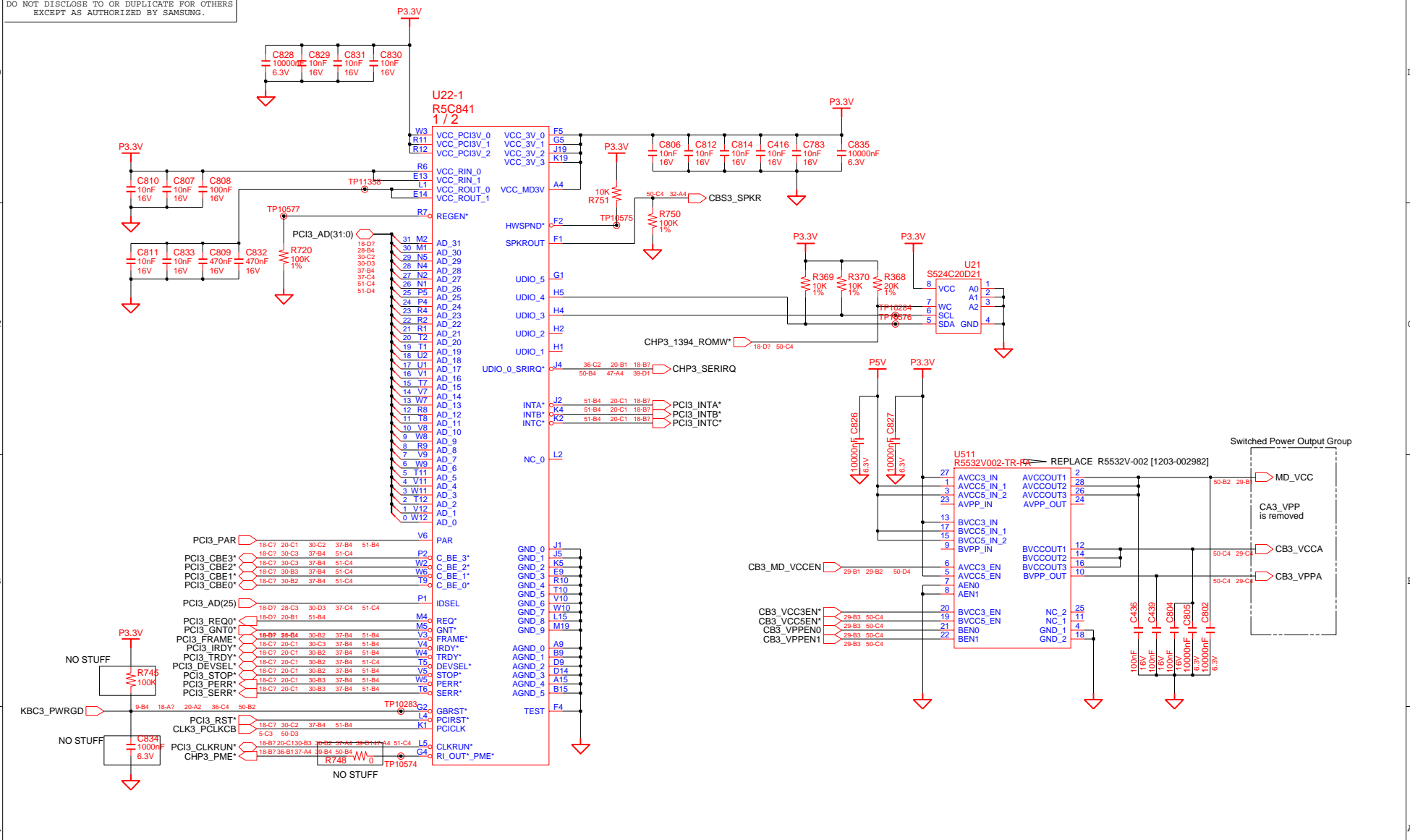
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LCD CONNECTOR



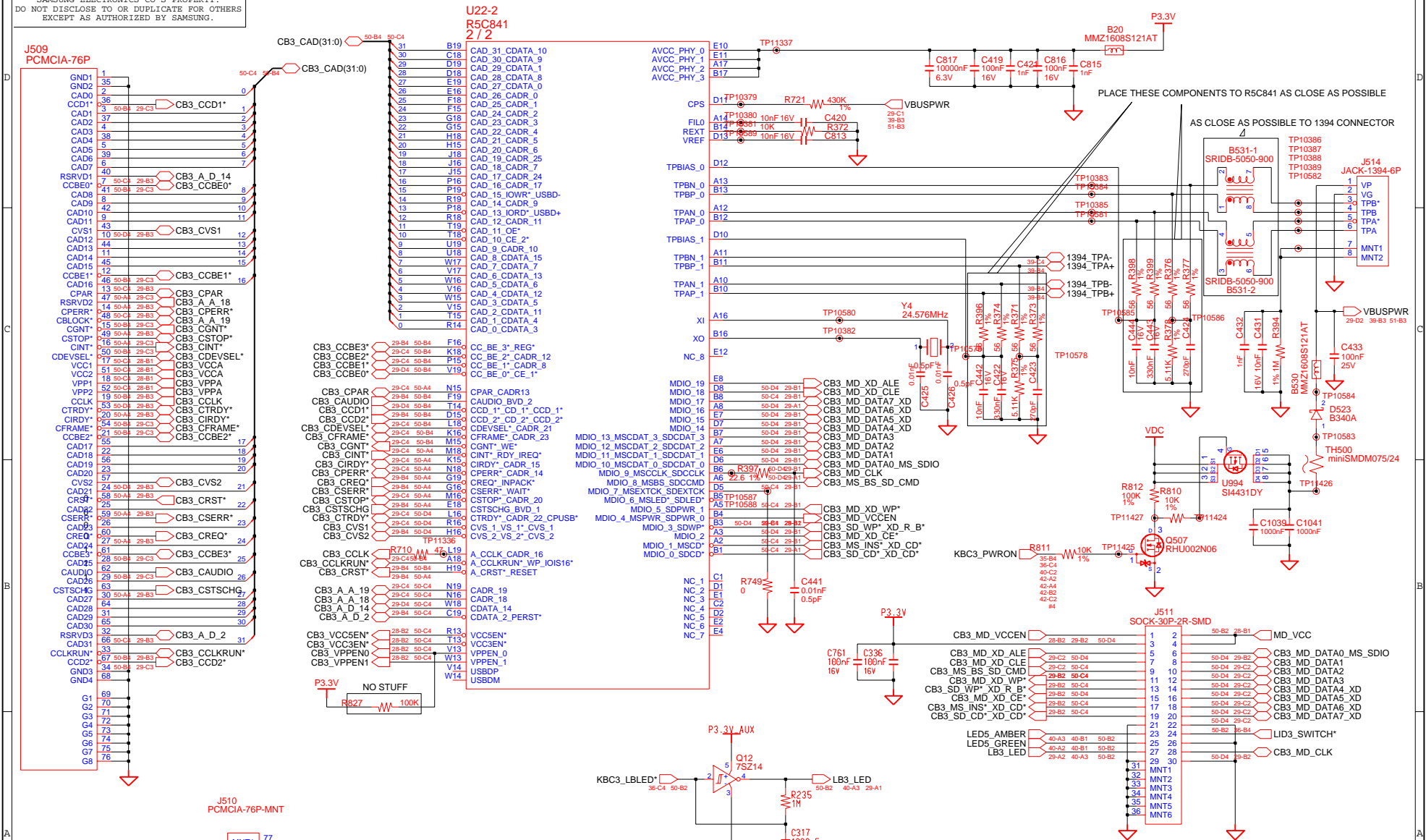
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APPROVAL	KIM, DW	REV	1.0	PART NO. BA41-00450A		PAGE 27 OF 51
MODULE CODE		LAST EDIT	November 5, 2004 8:10:03 PM			

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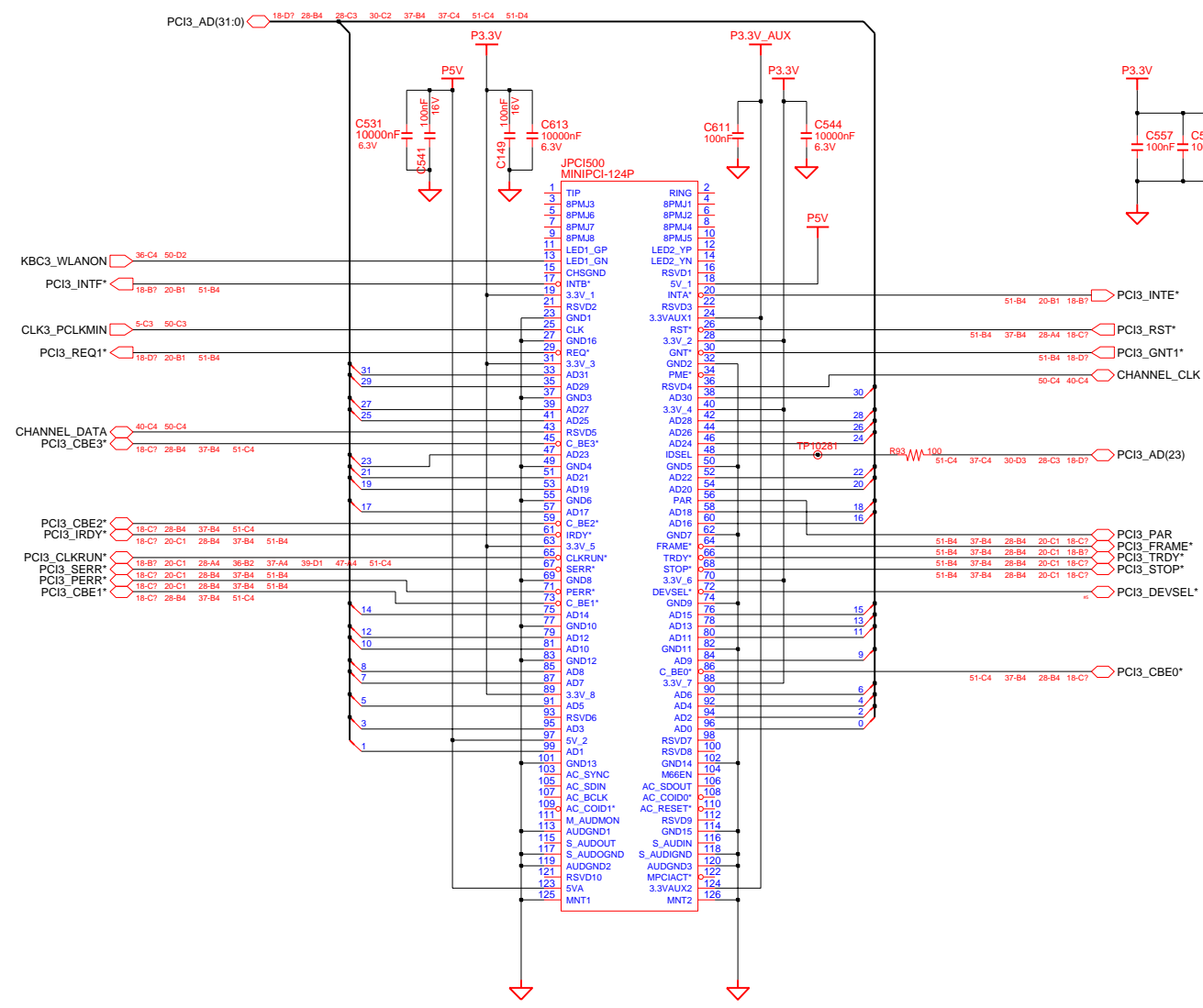


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CHECK	BIN, KK	DEV. STEP	PR			
APPROVAL	KIM, DW	REV	1.0			
MODULE CODE		LAST EDIT	November 5, 2004 8:10:03 PM	PAGE	28 OF 51	

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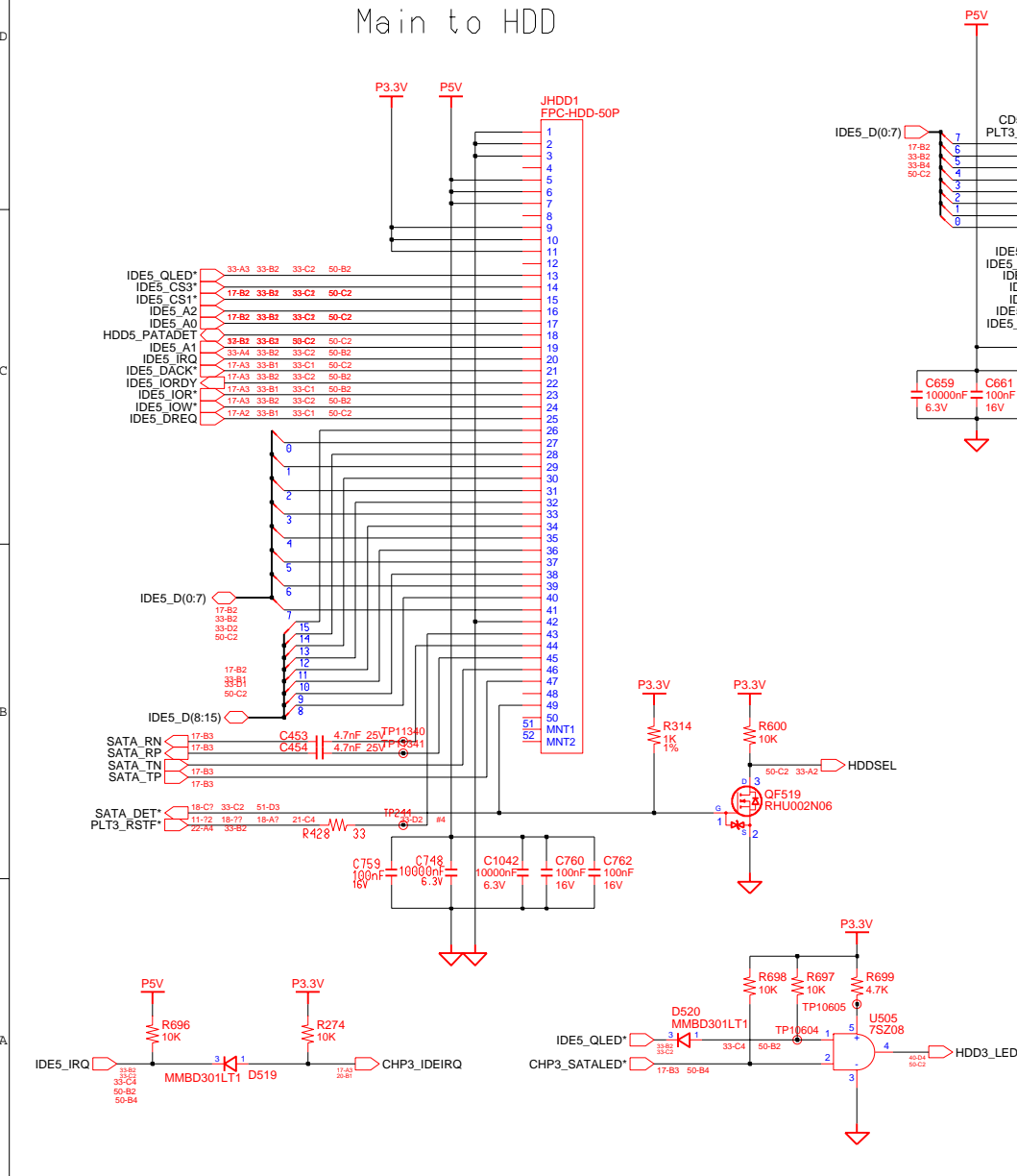
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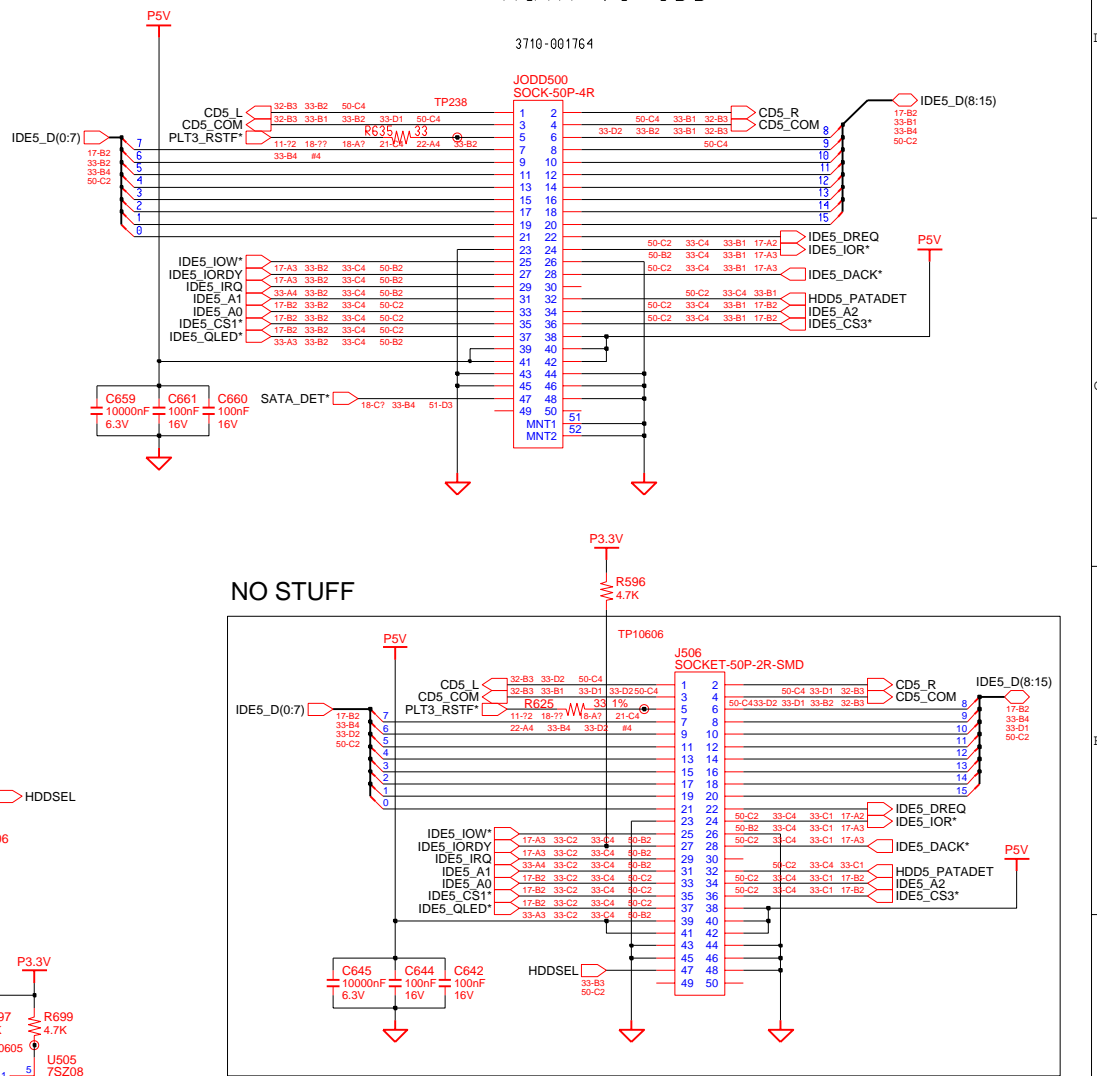
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APPROVAL	KIM, DW	REV	1.0			PART NO. BA41-00450A
MODULE CODE		LAST EDIT	November 5, 2004 8:10:03 PM	PAGE	30	OF 51

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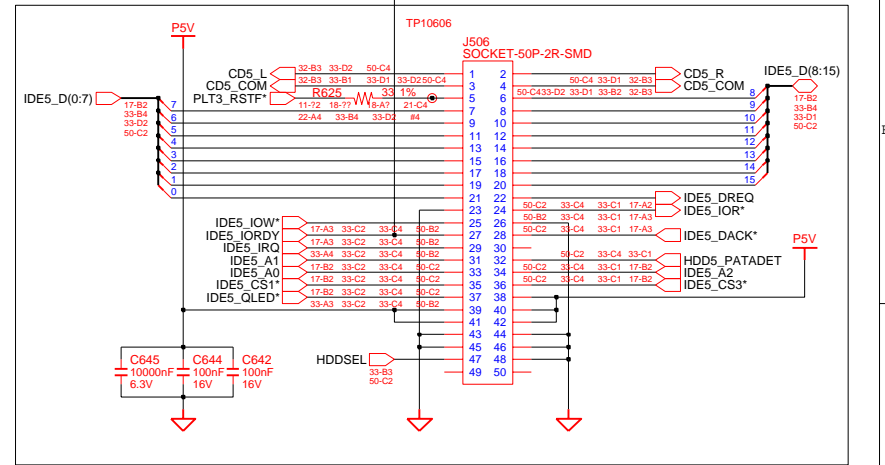
Main to HDD



Main to ODD



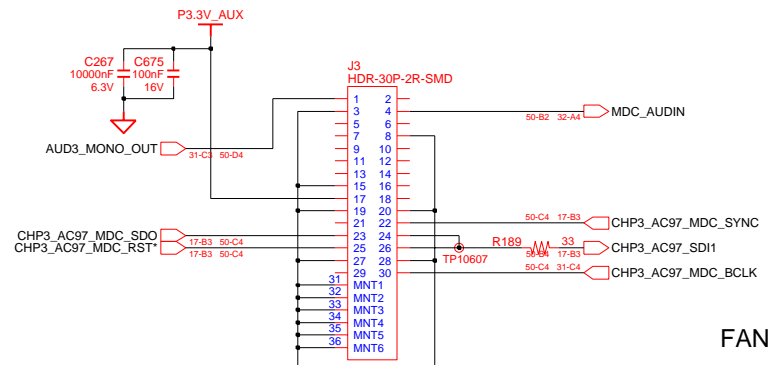
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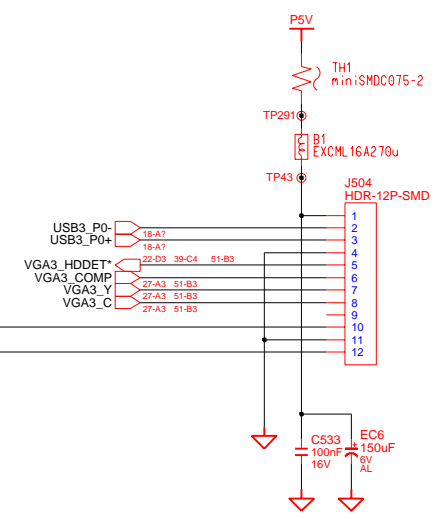
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CHECK	BIN, KK	DEV. STEP	PR			
APPROVAL	KIM, DW	REV	1.0			
MODULE CODE		LAST EDIT	November 5, 2004 8:10:03 PM			
					PAGE 33 OF 51	

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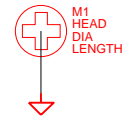
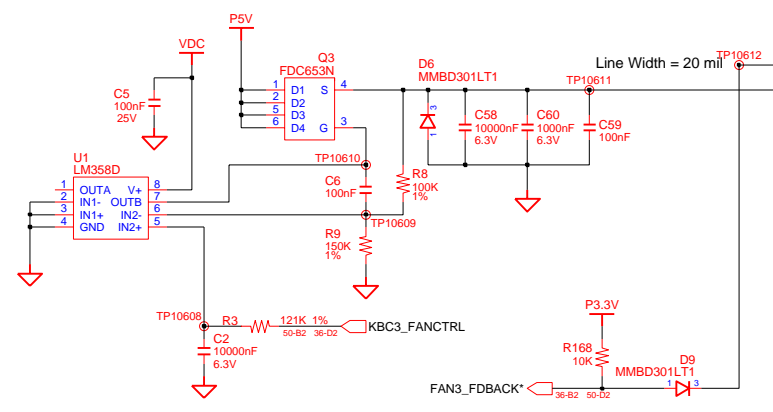
MDC Connector



TV-OUT(S-VHS)



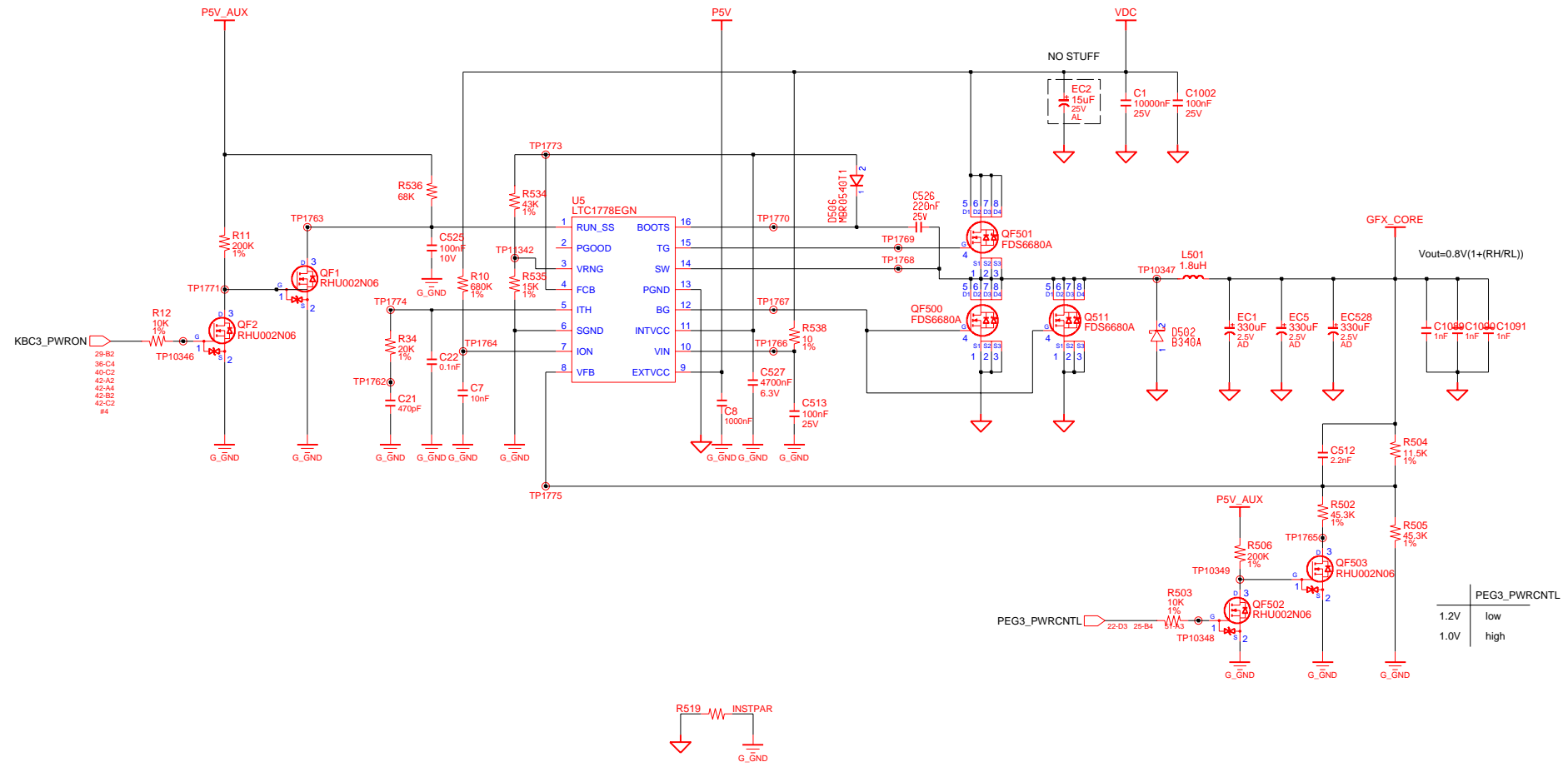
FAN Control Logic



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CHECK	BIN, KK	DEV. STEP	PR	MDC MODEM / TV-OUT(SVHS)	PART NO.	
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MODULE CODE		LAST EDIT				

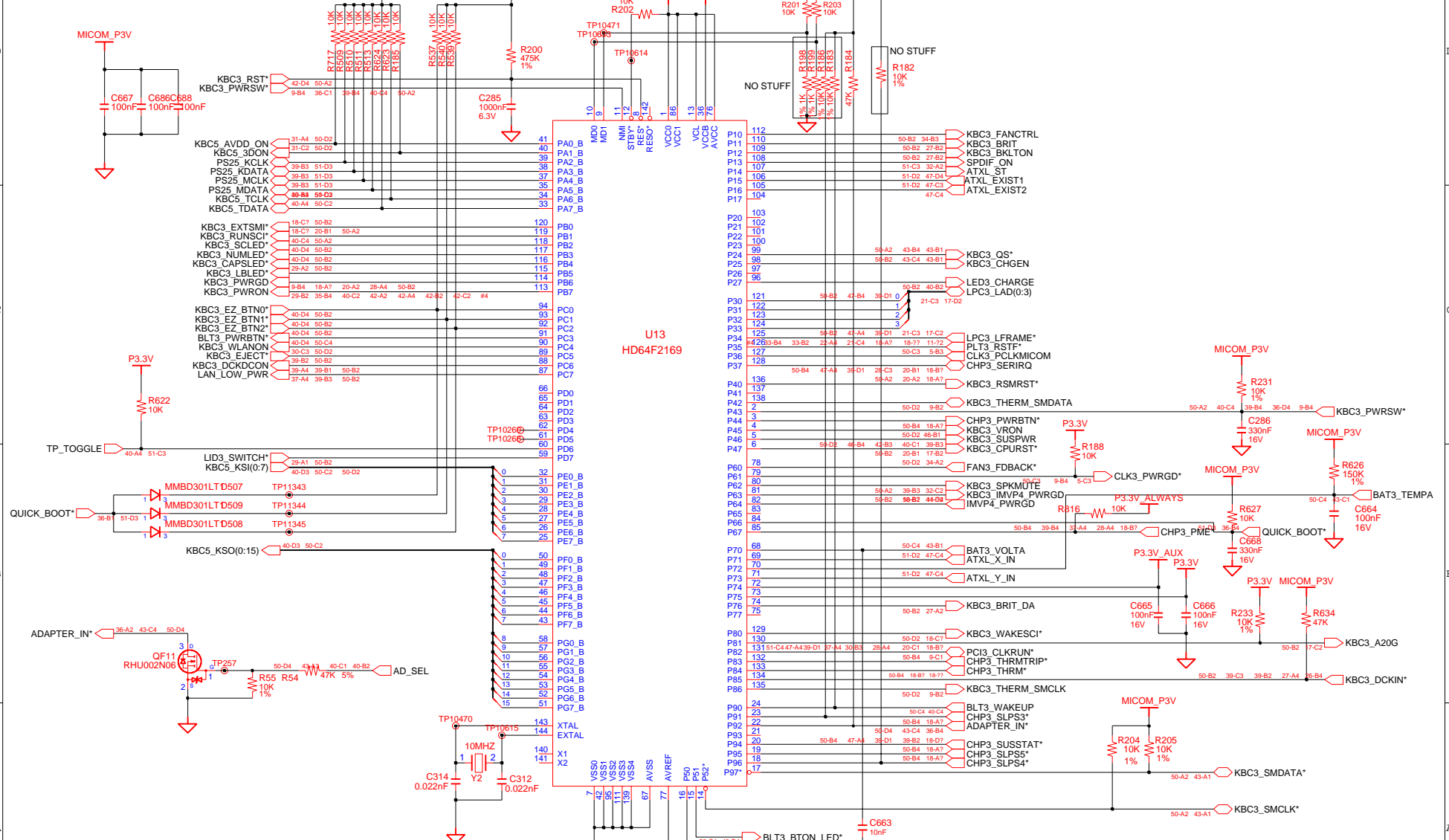
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Graphic Core Power



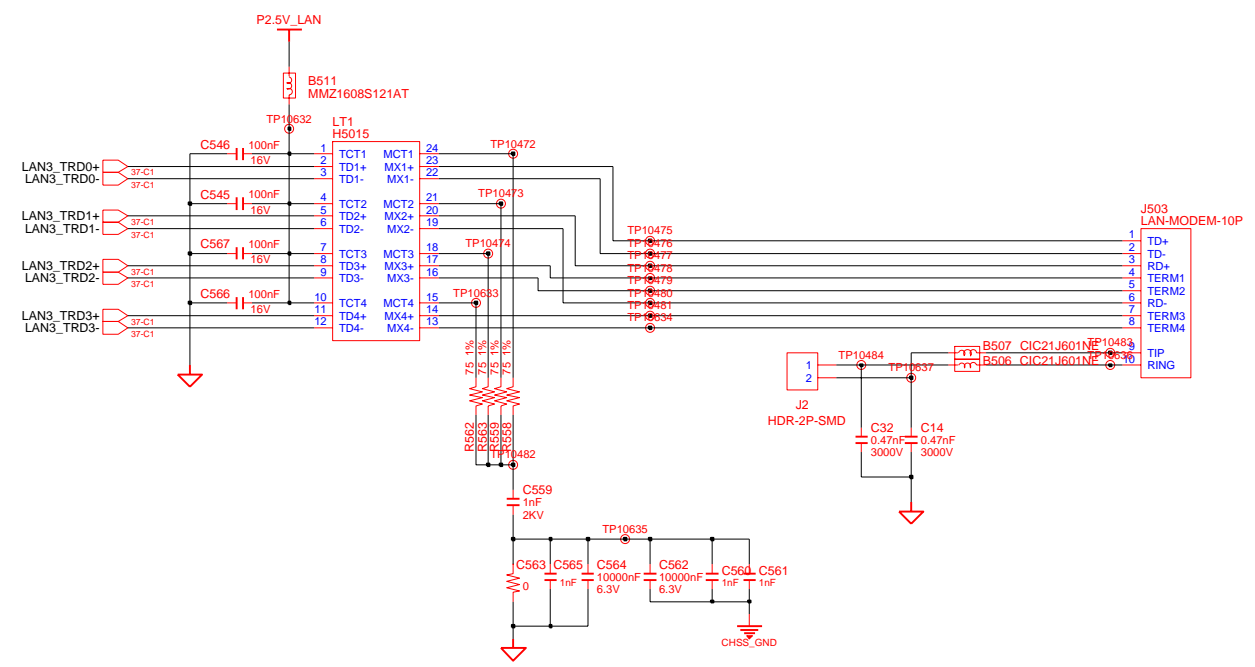
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CHECK	BIN, KK	DEV. STEP	PR	REV	1.0	
APPROVAL	KIM, DW	LAST EDIT	November 5, 2004 8:10:03 PM	PAGE	35	OF 51
MODULE CODE						PART NO. BA41-00450A

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DRAW	KYUNGIL, KI	DATE	11/5/2004	TITLE	CYGNUS MAIN MICOM	SAMSUNG ELECTRONICS PART NO. BA41-00450A
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APPROVAL	KIM, DW	REV	1.0			
MODULE CODE		LAST EDIT	November 5, 2004 8:10:03 PM	PAGE	36 OF 51	

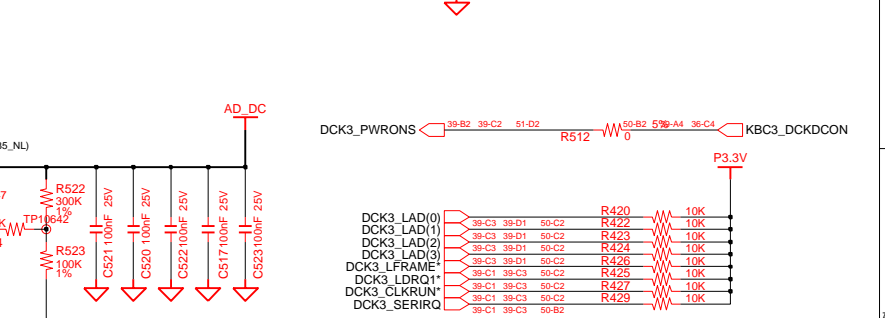
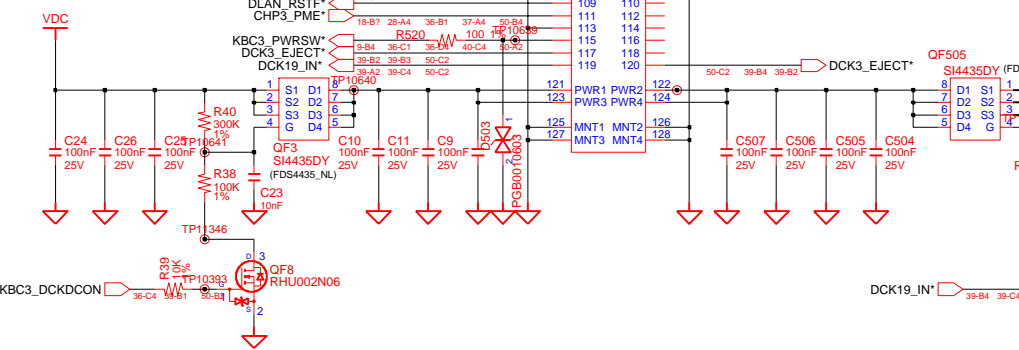
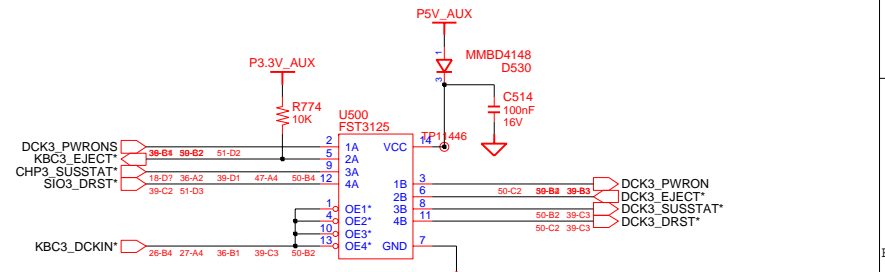
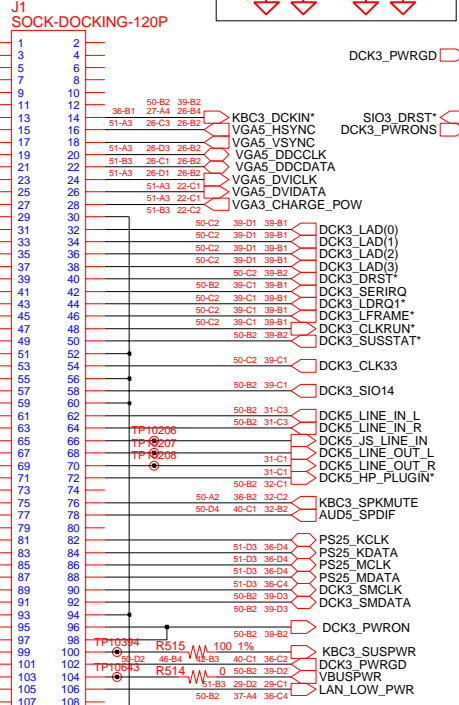
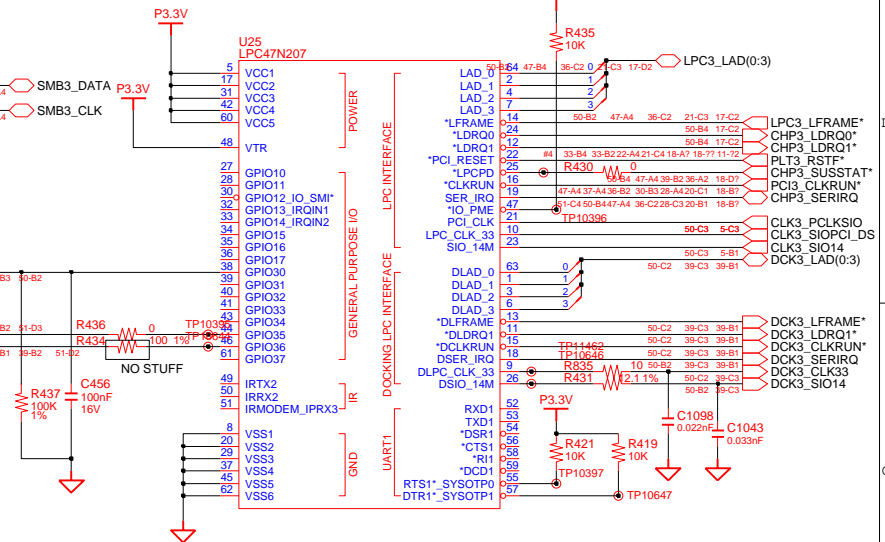
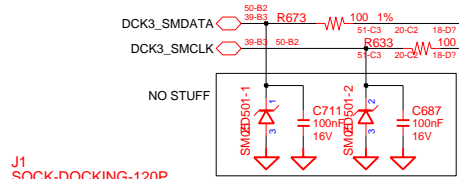
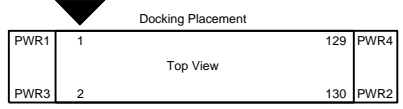
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DRAW	KYUNGIL, KI	DATE	11/5/2004	TITLE	CYGNUS MAIN	SAMSUNG ELECTRONICS
CHECK	BIN, KK	DEV. STEP	PR	LAN(BROADCOM BCM5751M 2/2)		
APPROVAL	KIM, DW	REV	1.0	PART NO.	BA41-00450A	PAGE 38 OF 51
MODULE CODE		LAST EDIT	November 5, 2004 8:10:03 PM			

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DOCKING CONNECTOR (130PIN)



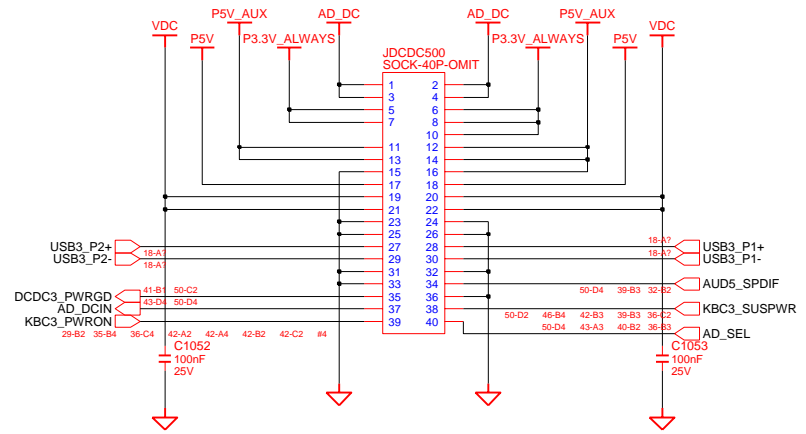
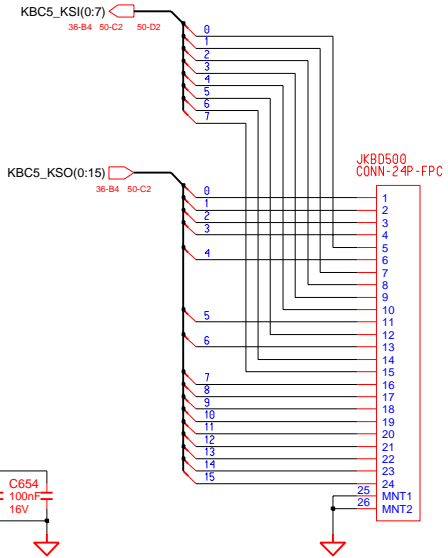
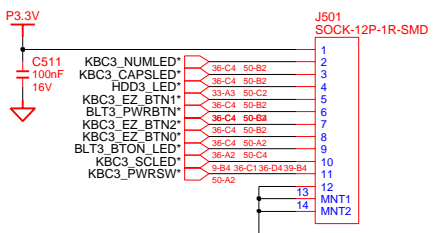
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CHECK	BIN, KK	DEV. STEP	PR			
APPROVAL	KIM, DW	REV	1.0			
MODULE CODE		LAST EDIT	November 5, 2004 8:10:03 PM			
					PAGE 39 OF 51	

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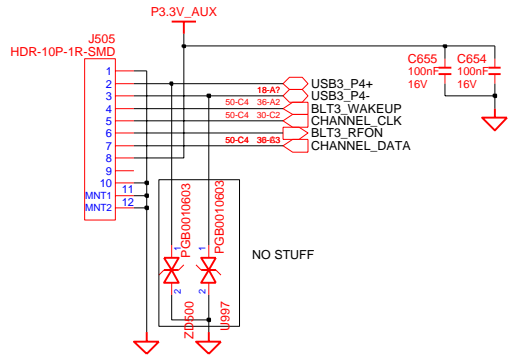
KEYBOARD

Main to DC/DC BOARD

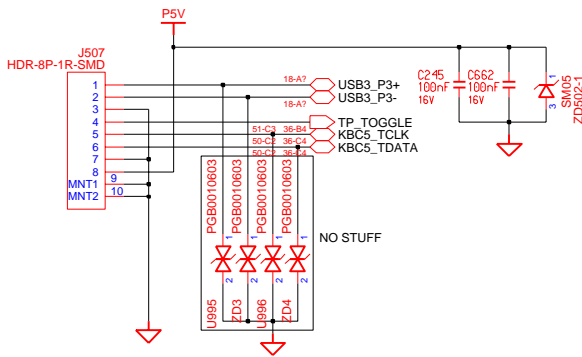
MAIN TO ON-TOP



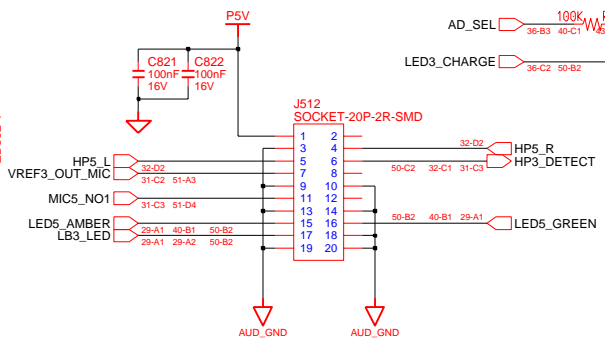
BLUETOOTH CONNECTOR



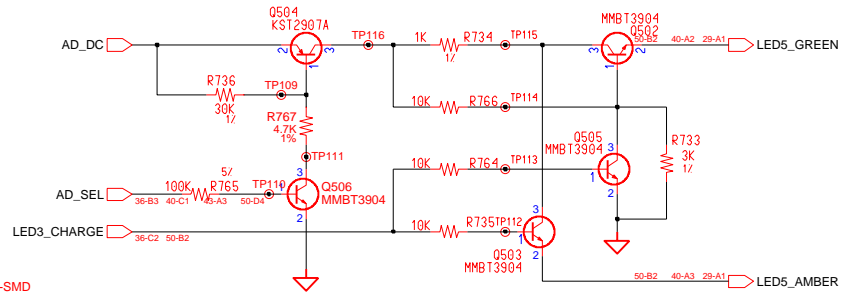
TOUCHPAD CONNECTOR



AUDIO CONNECTOR



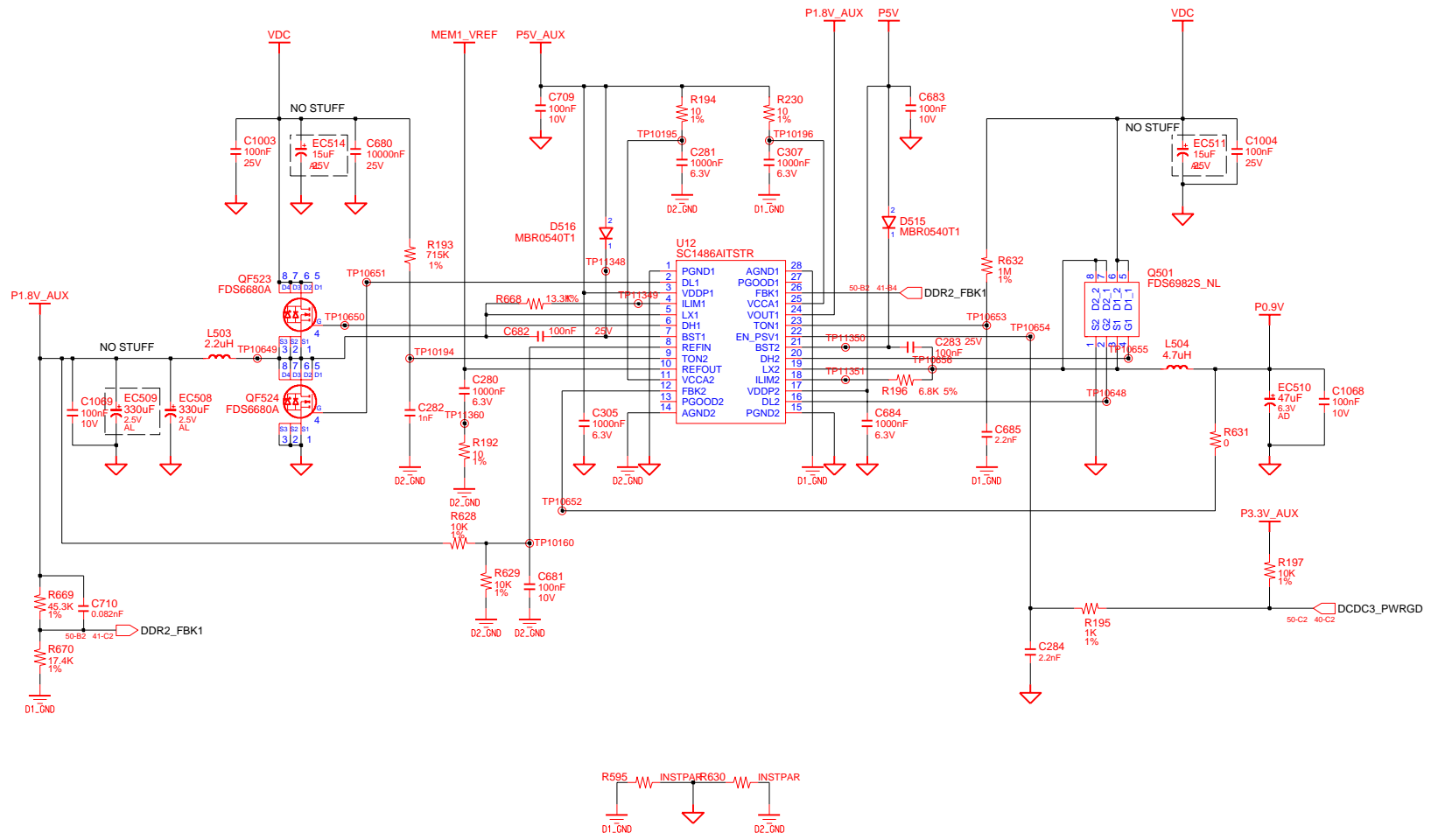
ADAPTER IN/CHARGING LED



DRAW	KYUNGIL, KI	DATE	11/5/2004	TITLE	CYGNUS MAIN B'D TO B'D CONNECTOR	SAMSUNG ELECTRONICS
CHECK	BIN, KK	DEV. STEP	PR		PART NO.	
APPROVAL	KIM, DW	REV	1.0		BA41-00450A	
MODULE CODE		LAST EDIT	November 5, 2004 8:10:03 PM	PAGE	40	OF 51

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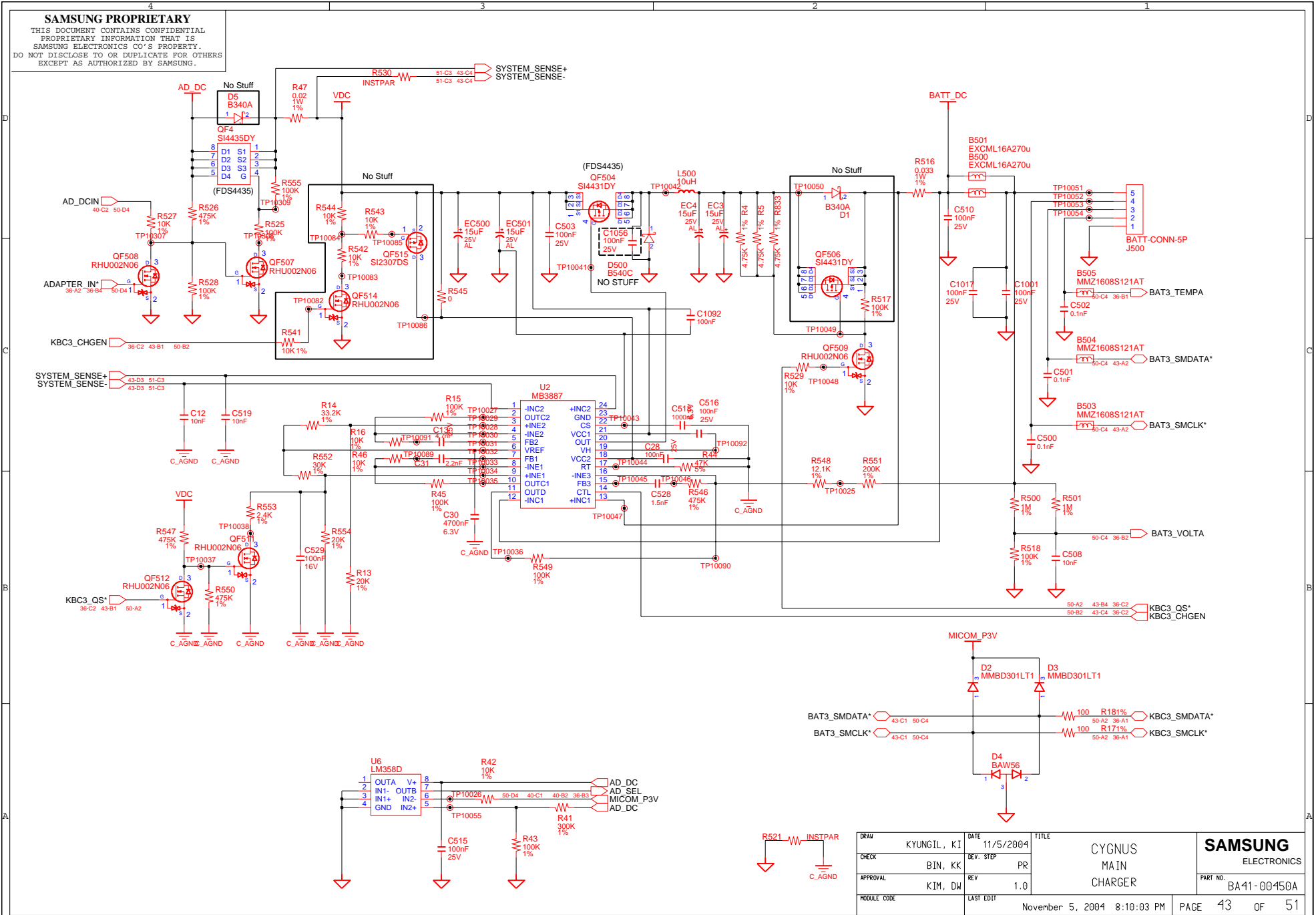
DDR Power



DRAW	KYUNGIL, KI	DATE	11/5/2004	TITLE	CYGNUS MAIN DDR POWER	SAMSUNG ELECTRONICS	
CHECK	BIN, KK	DEV. STEP	PR	PART NO.			BA41-00450A
APPROVAL	KIM, DW	REV	1.0	PAGE			41 OF 51
MODULE CODE		LAST EDIT	November 5, 2004 8:10:03 PM				

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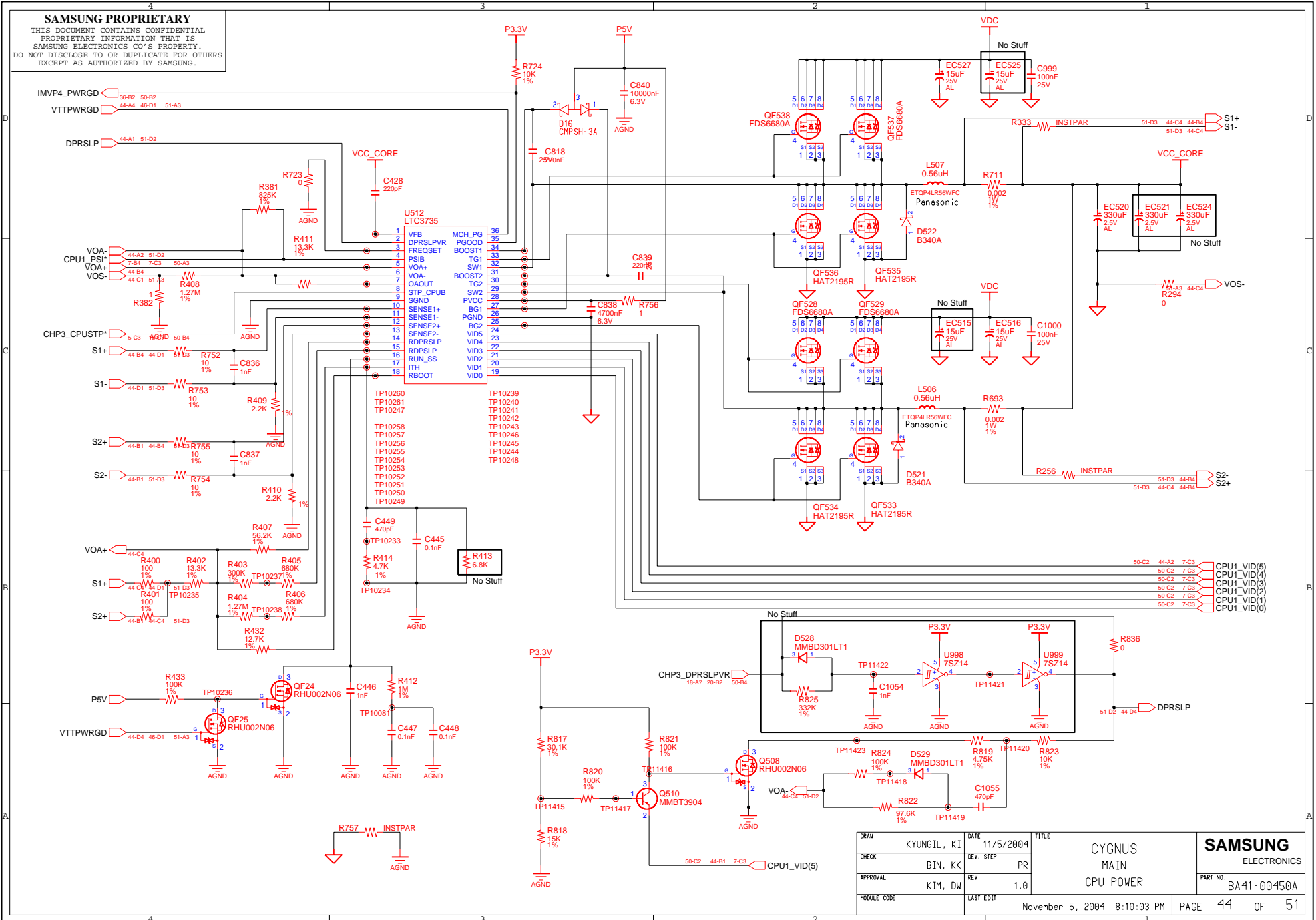
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DRAW	KYUNGIL, KI	DATE	11/5/2004	TITLE	CYGNUS MAIN CHARGER	SAMSUNG ELECTRONICS PART NO. BA41-00450A
CHECK	BIN, KK	DEV. STEP	PR			
APPROVAL	KIM, DW	REV	1.0			
MODULE CODE		LAST EDIT				
			November 5, 2004 8:10:03 PM	PAGE	43 OF 51	

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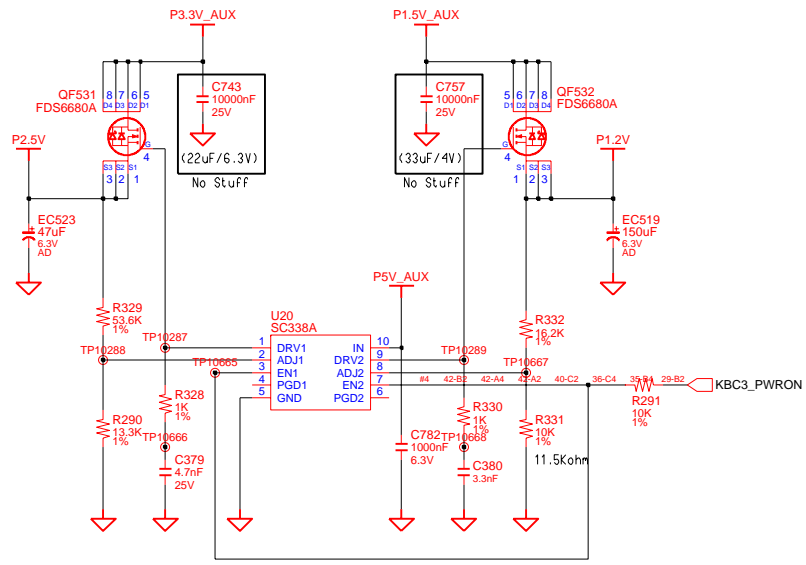
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DRAW	KYUNGIL, KI	DATE	11/5/2004	TITLE	CYGNUS MAIN CPU POWER	SAMSUNG ELECTRONICS PART NO. BA41-00450A
CHECK	BIN, KK	DEV. STEP	PR			
APPROVAL	KIM, DW	REV	1.0			
MODULE CODE		LAST EDIT				
				November 5, 2004 8:10:03 PM	PAGE	44 OF 51

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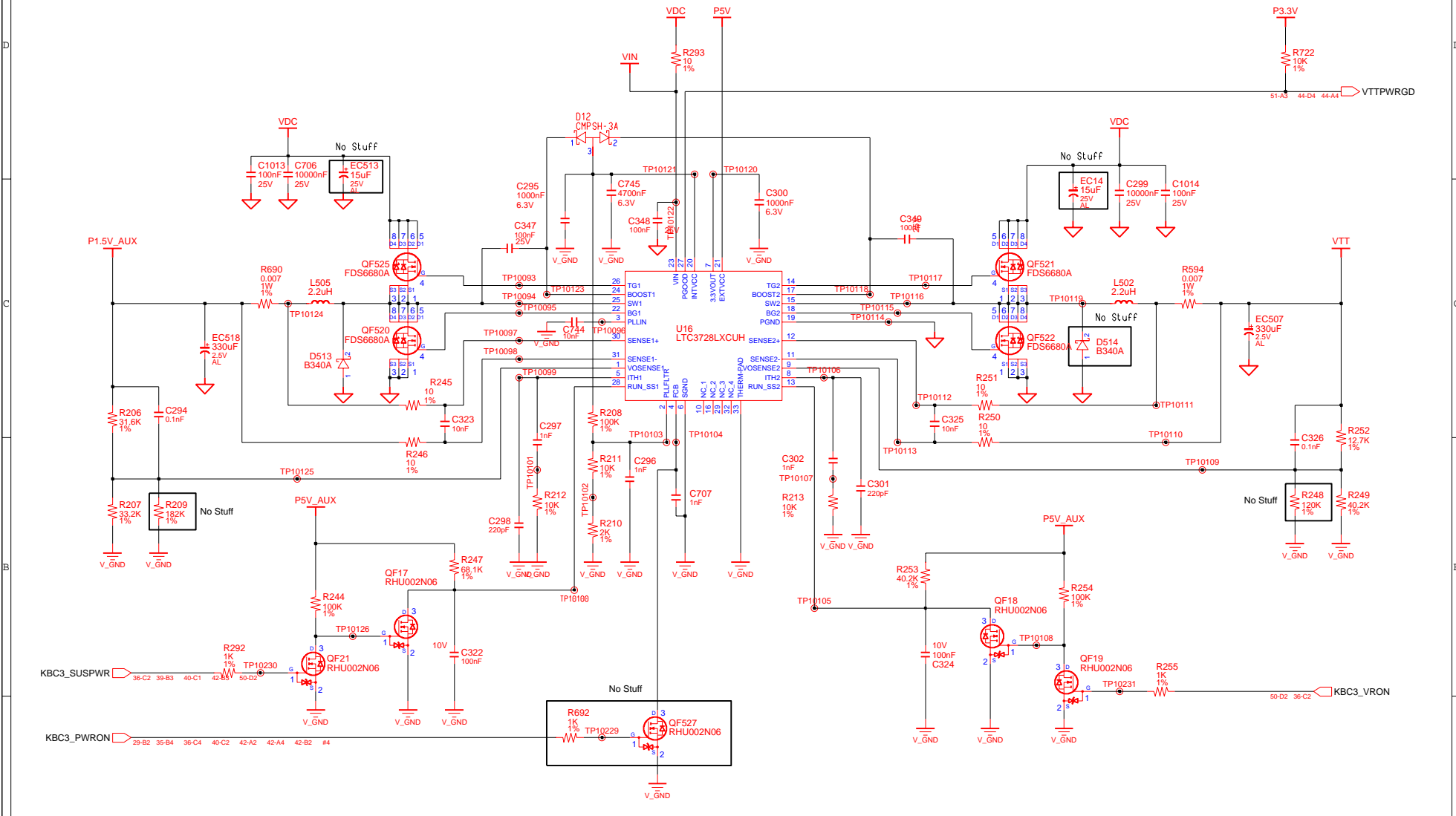
P2.5V&P1.2V



DRAW	KYUNGIL, KI	DATE	11/5/2004	TITLE	CYGNUS MAIN P2.5V & P1.2V	SAMSUNG ELECTRONICS
CHECK	BIN, KK	DEV. STEP	PR	PART NO.		
APPROVAL	KIM, DW	REV	1.0	November 5, 2004 8:10:03 PM		PAGE 45 OF 51
MODULE CODE		LAST EDIT				

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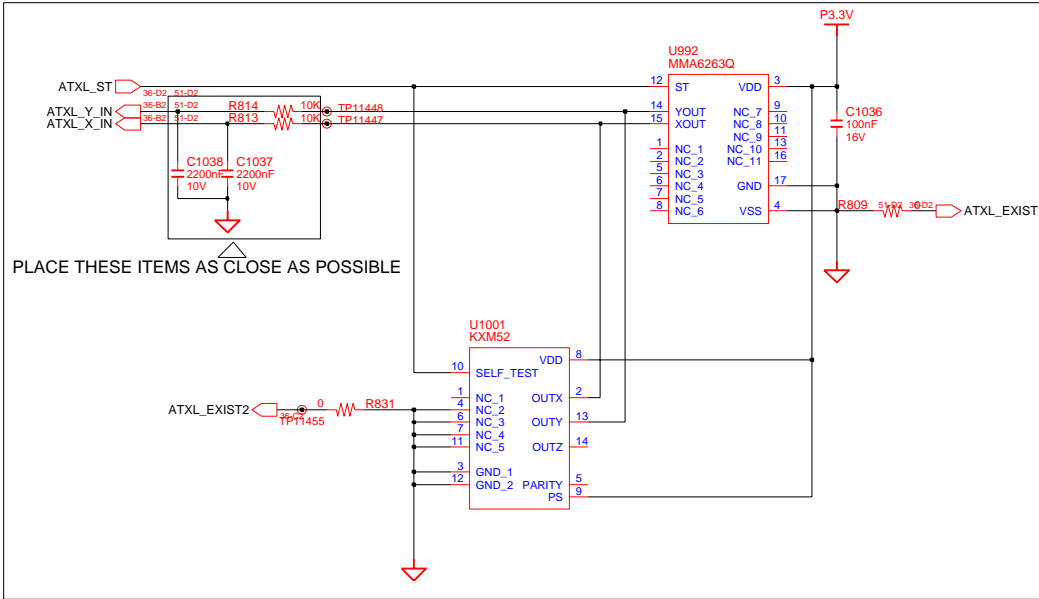
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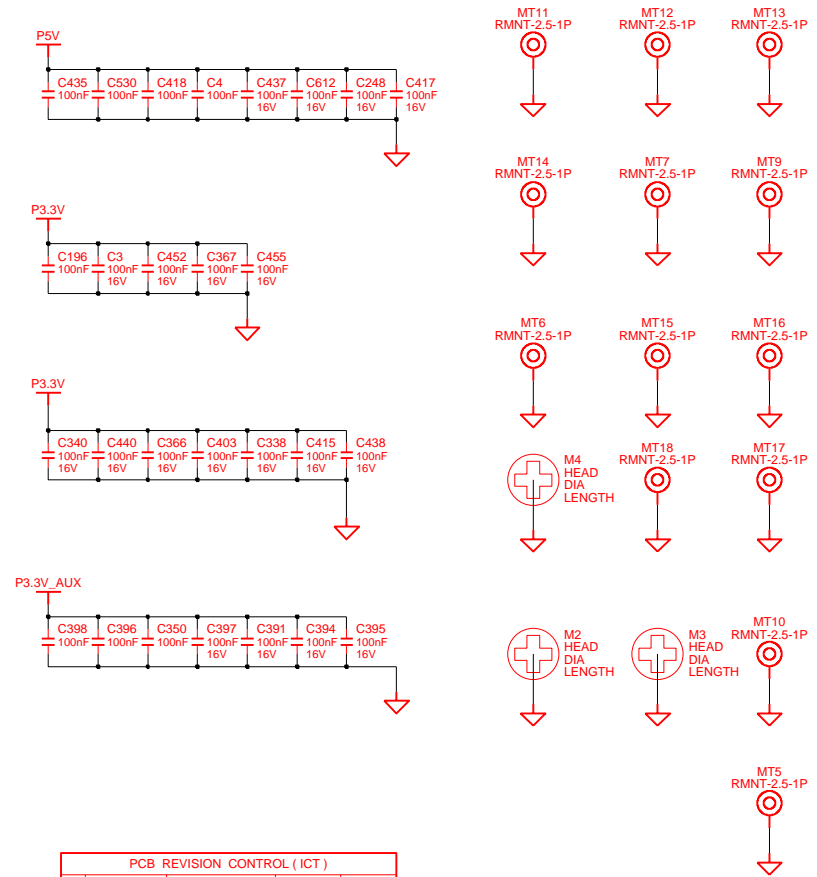
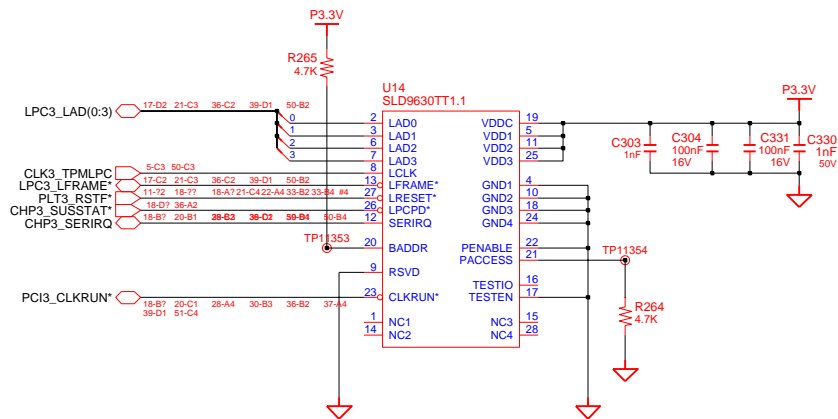
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AIRBAG

NO STUFF



TPM



PCB REVISION CONTROL (ICT)				
NO	CONNECTION	DATE(Y/M/DD)	REVISION	STEP
1	N.C.			
2	1-2			
3	2-3			
4	3-1			
5	1-2-3			
6	N.C.			
7	1-2			
8	2-3			
9	3-1			
10	1-2-3			

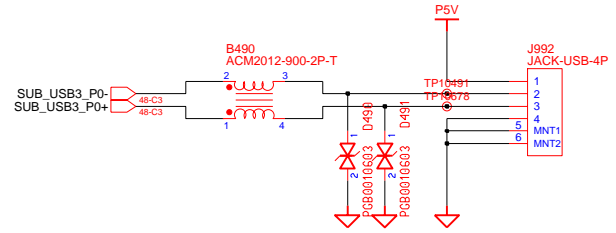
REV1
 1
 2 0 03

DRAW	KYUNGIL, KI	DATE	11/5/2004	TITLE	CYGNUS MAINBD	SAMSUNG ELECTRONICS
CHECK	BIN, KK	DEV. STEP	PR	AIRBAG & TPM		
APPROVAL	KIM, DW	REV	1.0	November 5, 2004 8:10:03 PM		PART NO. BA41-00450A
MODULE CODE		LAST EDIT		PAGE 47 OF 51		

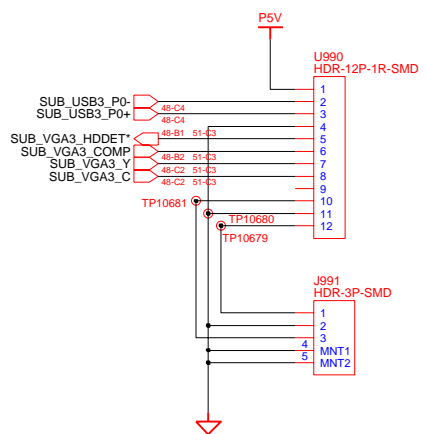
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< USB BOARD >

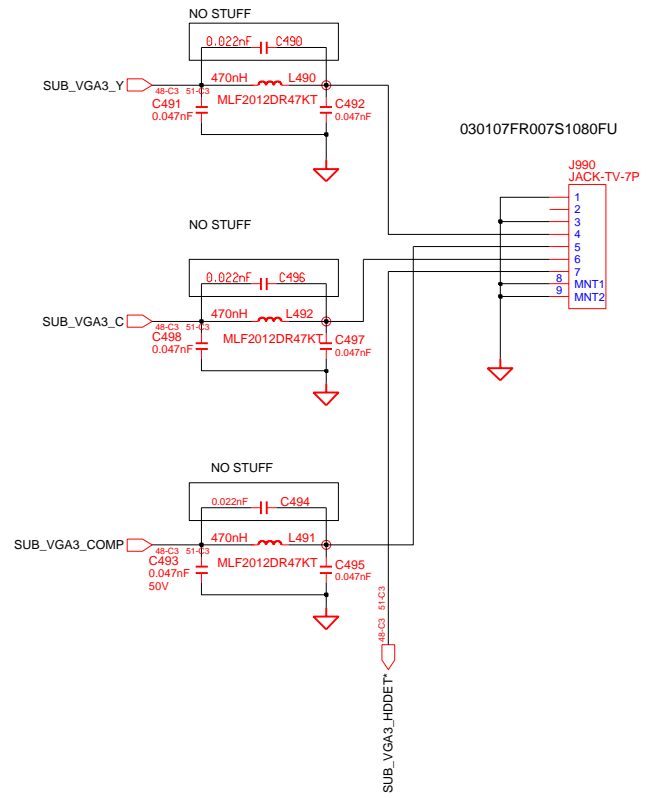
USB Connector



Mother Board I/F



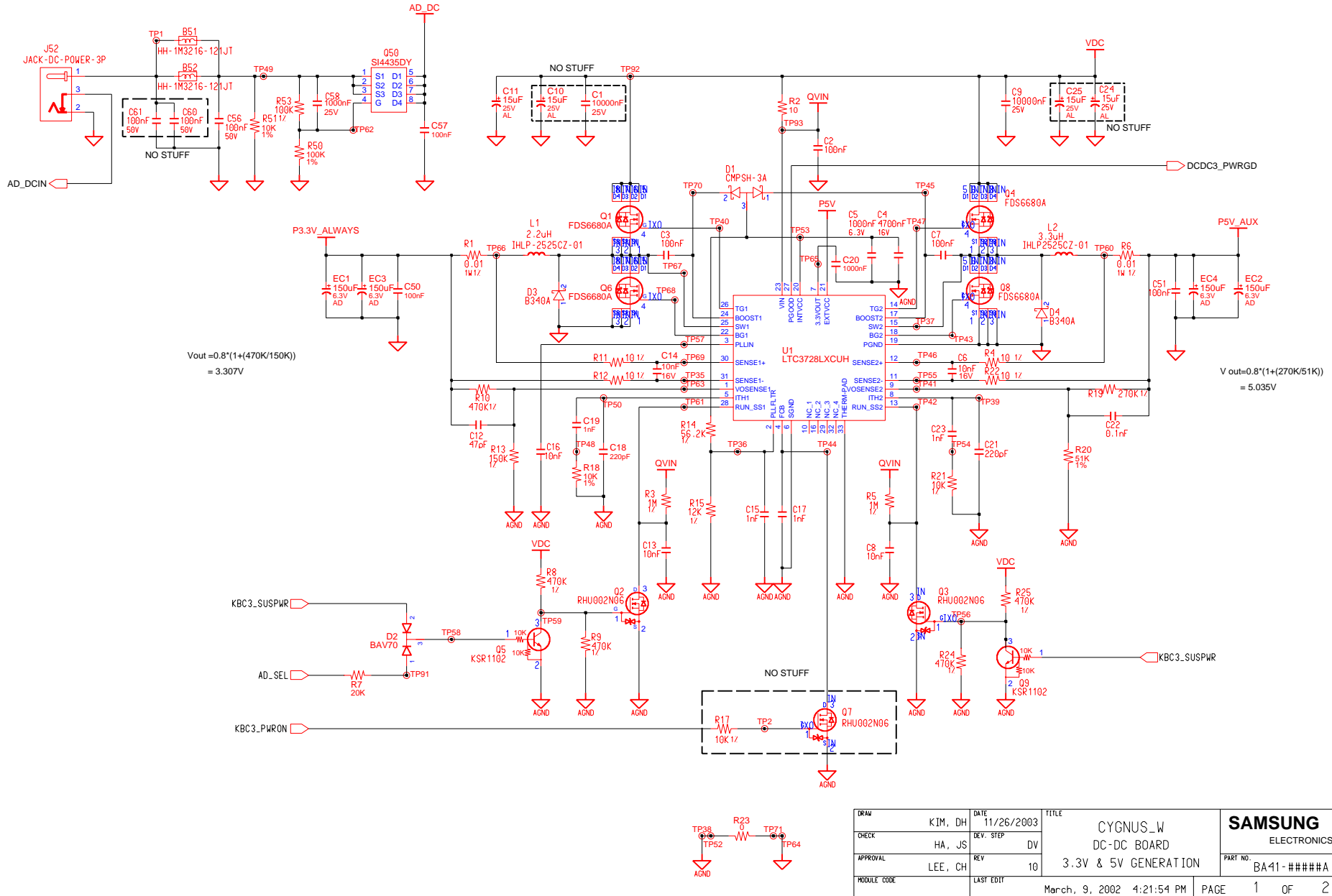
TV OUT JACK



DRAW	KYUNGIL, KI	DATE	11/5/2004	TITLE	CYGNUS MAIN MOUNT HOLE	SAMSUNG ELECTRONICS PART NO. BA41-00450A
CHECK	BIN, KK	DEV. STEP	PR			
APPROVAL	KIM, DW	REV	1.0			
MODULE CODE		LAST EDIT				
			November 5, 2004 8:10:03 PM	PAGE 48 OF 51		

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DATE	11/26/2003	TITLE	CYGNUS_W DC-DC BOARD 3.3V & 5V GENERATION	SAMSUNG ELECTRONICS PART NO. BA41-#####	
DEV. STEP	DV	REV	10		
DATE	March, 9, 2002 4:21:54 PM	PAGE	1	OF	2

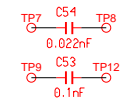
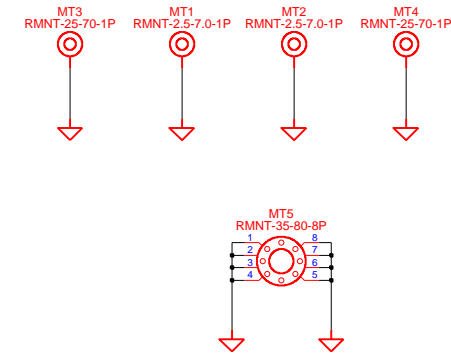
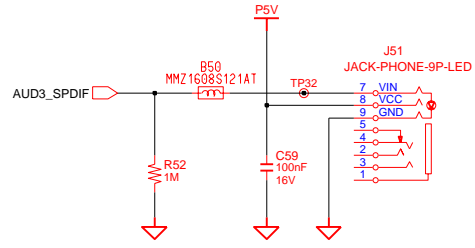
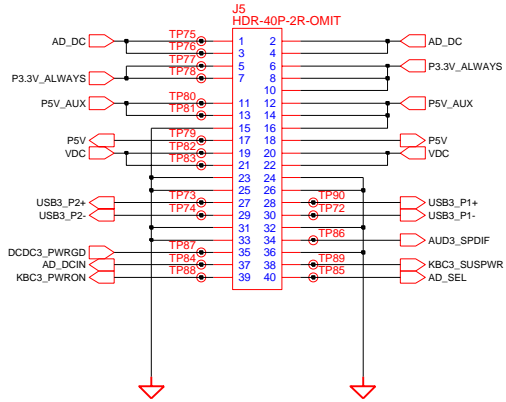
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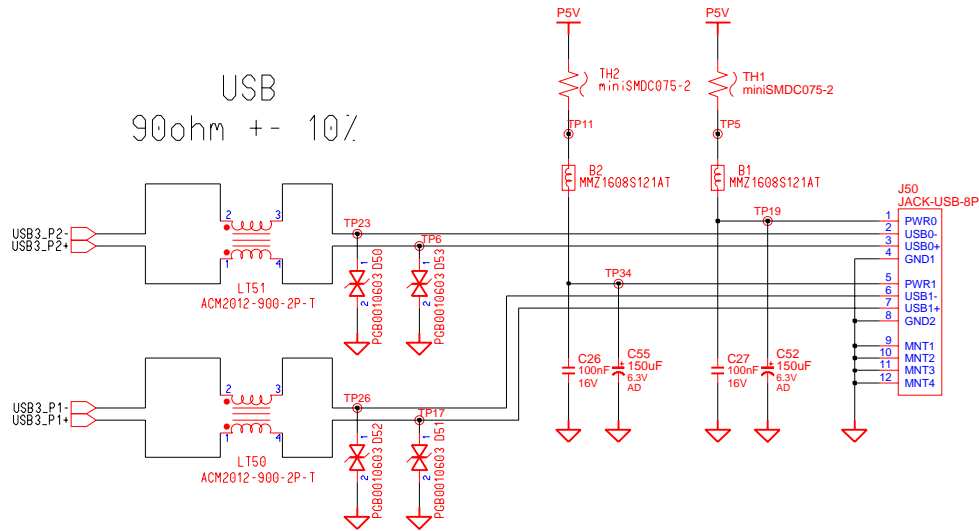
SPDIF OUT

CHANGE THIS CONNECTOR TO HEADER < 12809A-40G5T >

FROM DCDC TO MAIN BOARD



USB
90ohm +- 10%



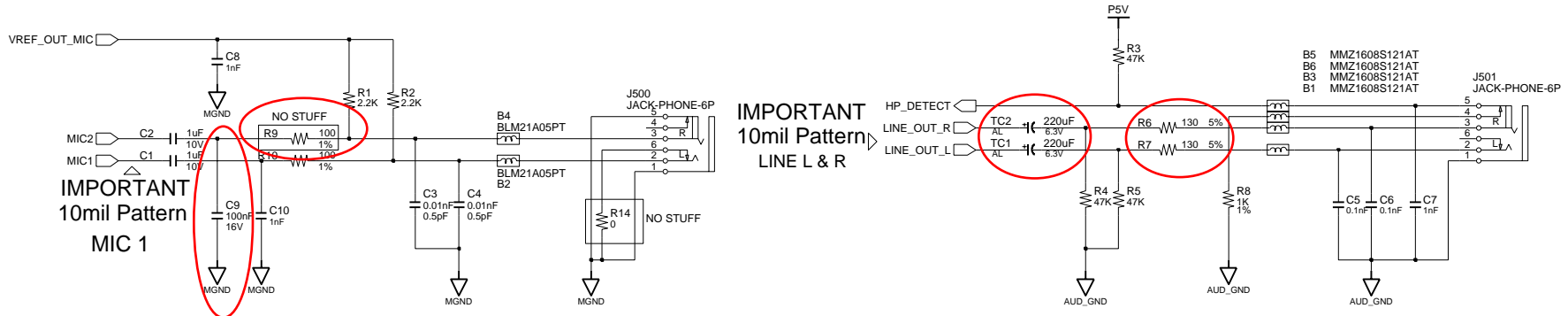
PCB REVISION CONTROL (ICT)				
NO	CONNECTION	DATE(Y/M/D)	REVISION	STEP
1	N.C.			
2	1-2			
3	2-3			
4	3-1			
5	1-2-3			
6	N.C.			
7	1-2			
8	2-3			
9	3-1			
10	1-2-3			

REV1
1 O
2 O 3

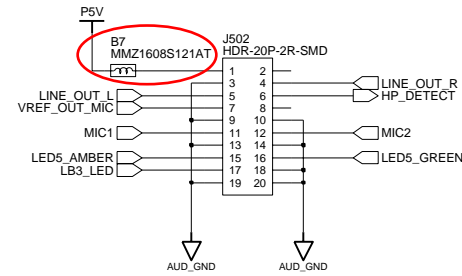
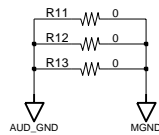
DRAW	KIM, DH	DATE	11/26/2003	TITLE	CYGNUS_W DC-DC BOARD CONNECTOR & PORT	SAMSUNG ELECTRONICS PART NO. BA41-#####A
CHECK	HA, JS	DEV. STEP	DV			
APPROVAL	LEE, CH	REV	10			
MODULE CODE		LAST EDIT	March, 9, 2002 4:23:55 PM	PAGE	2	OF 2

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< AUDIO BOARD >



AQUILA I/F CONNECTOR 3711-0422

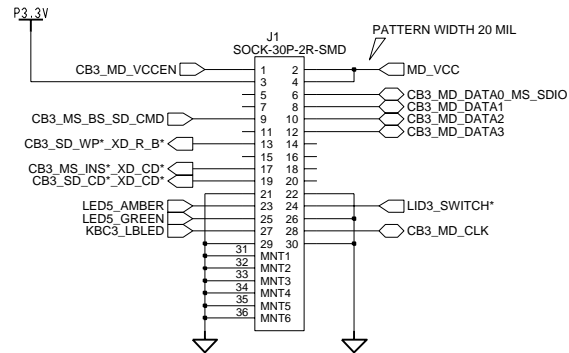


DRAW	DATE	TITLE	SAMSUNG ELECTRONICS
CHECK	DEV. STEP	Cygnus AUDIO JACK	
APPROVAL	REV		PART NO. BA41-
MODULE CODE	LAST EDIT	January, 30, 2004 9:34:17 AM	PAGE 1 OF

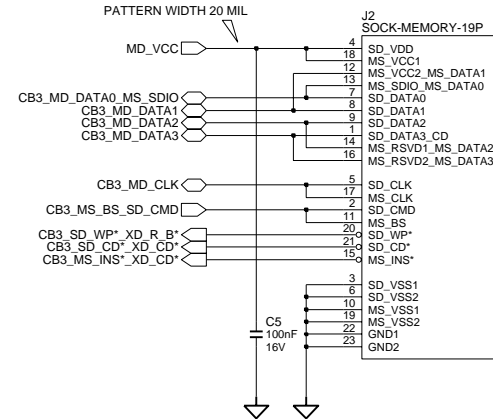
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< 3 IN 1 BOARD >

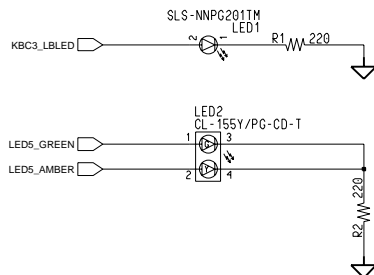
MAIN BOARD I/F CONNECTOR



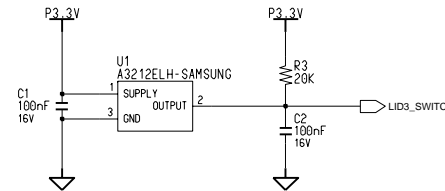
Flash Media Socket



LED



Lid Close Switch

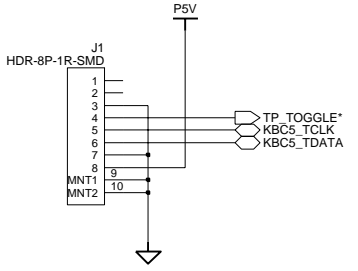


DRAW	DATE	TITLE	SAMSUNG ELECTRONICS PART NO. BA41-
CHECK	DEV. STEP	CYGNUS MEMORY CARD	
APPROVAL	REV		
MODULE CODE	LAST EDIT		
		January, 11, 2004 2:16:04 PM	PAGE 1 OF

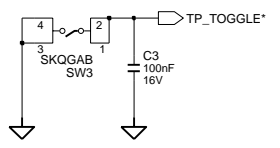
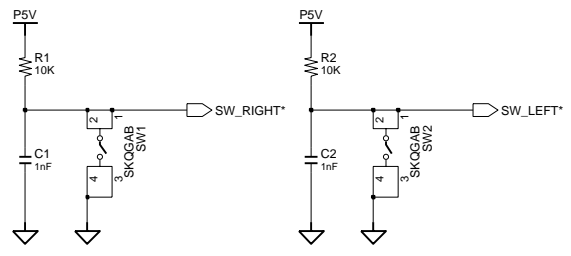
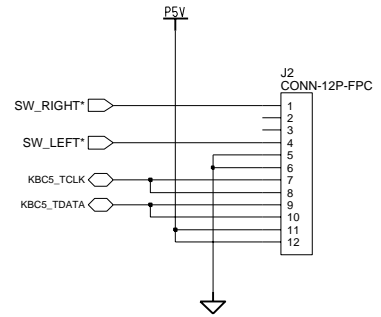
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< TOUCHPAD BOARD >

MotherBoard I/F Connector



TouchPad Connector



DRAW	DATE	TITLE	SAMSUNG ELECTRONICS PART NO. BA41-
CHECK	DEV. STEP	Cygnus TOUCHPAD	
APPROVAL	REV		
MODULE CODE	LAST EDIT		
	undef ined	January, 11, 2004 2:44:31 PM	PAGE 2 OF 3