

LONGBEACH 10/20

LA-2371 REV

1.0 Schematic

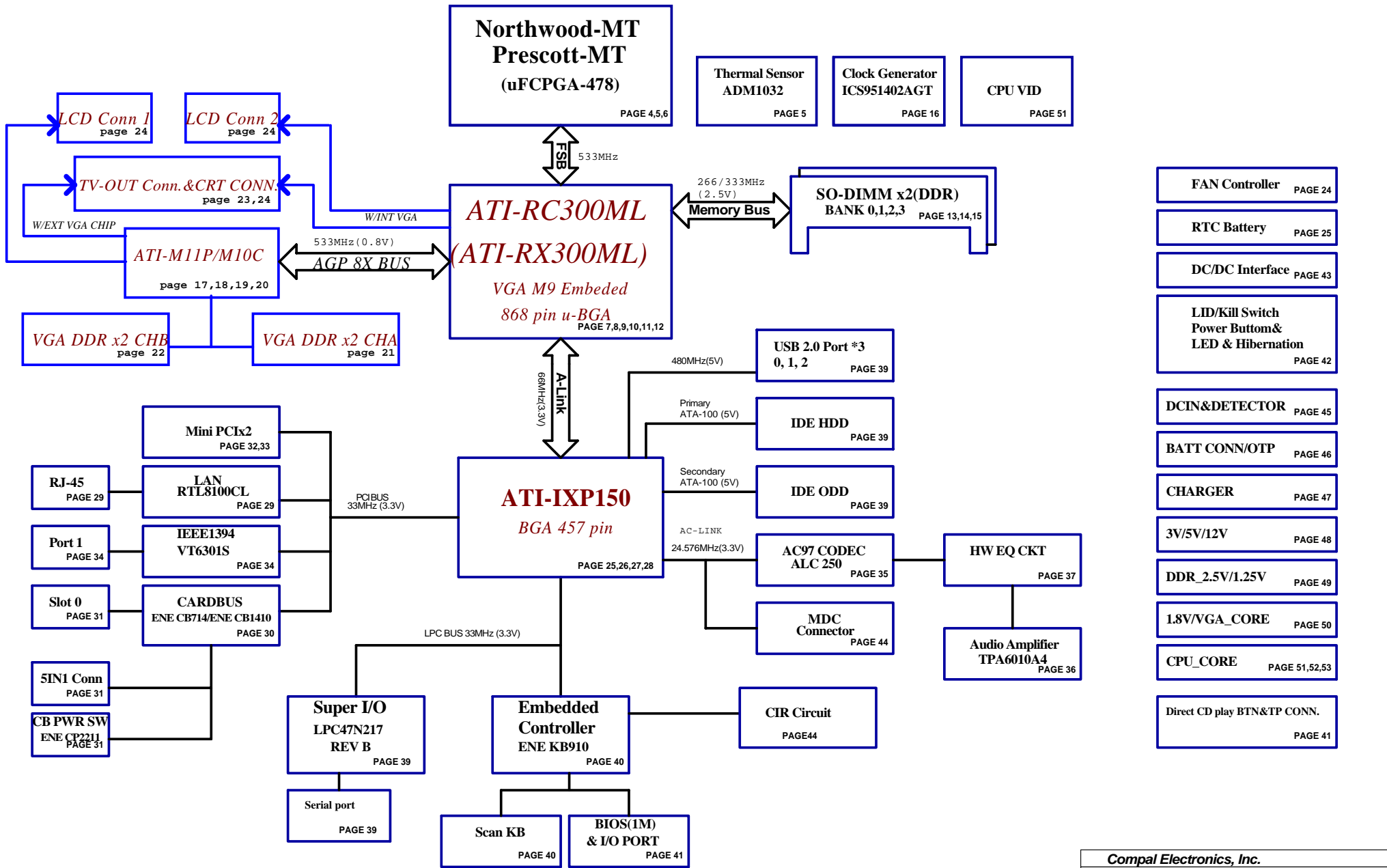
Portability Prescott/Northwood
RC300ML(RX300ML)+IXP150+ATI M11P(128MB VRAM)
2004-07-23

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Title			
Size	Document Number	Rev	
Custom	LA-2371	1.0	
Date:	星期二, 七月 27, 2004	Sheet	1 of 56

BLOCK DIAGRAM

Model Name : EFQ00 & EEQ00
 File Name : LA-2371 Rev: 1.0



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+CPUVID	1.2V switched power rail for CPU AGTL Bus	ON	OFF	OFF
+VGA_CORE	1.0V/1.2V switched power rail for VGA chip	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VS	AGP 4X/8X	ON	OFF	OFF
+1.8VS	1.8VS switched power rail	ON	OFF	OFF
+2.5VALW	2.5V always on power rail	ON	ON	ON*
+2.5V	2.5V power rail	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#GNT#	Interrupts
VGA	AD16		PIRQA
CardBus	AD20	2	PIRQA
LAN	AD19	3	PIRQD
Mini-PCI1	AD18	1(for Wireless Lan)	PIRQC/PIRQD
1394	AD16	0	PIRQA
5IN1	AD20	2	PIRQB
Mini-PCI2	AD22	4(for TV tuner)	PIRQC/PIRQD

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADM1032	1001 110X b
EEPROM(24C16/02) (24C04)	1010 000X b 1011 000Xb		

EC SM Bus2 address

IXP150 SM Bus address

Device	Address
Clock Generator (1CS951402AGT)	1101 001Xb
DDR DIMM0	1010 000Xb
DDR DIMM2	1010 001Xb

STATE	SIGNAL	SLP_S3#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	ON	OFF	OFF	OFF

Board ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra	100K +/- 5%			
Board ID	Rb	V _{AD_BID min}	V _{AD_BID typ}	V _{AD_BID max}
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

SKU ID Table for AD channel

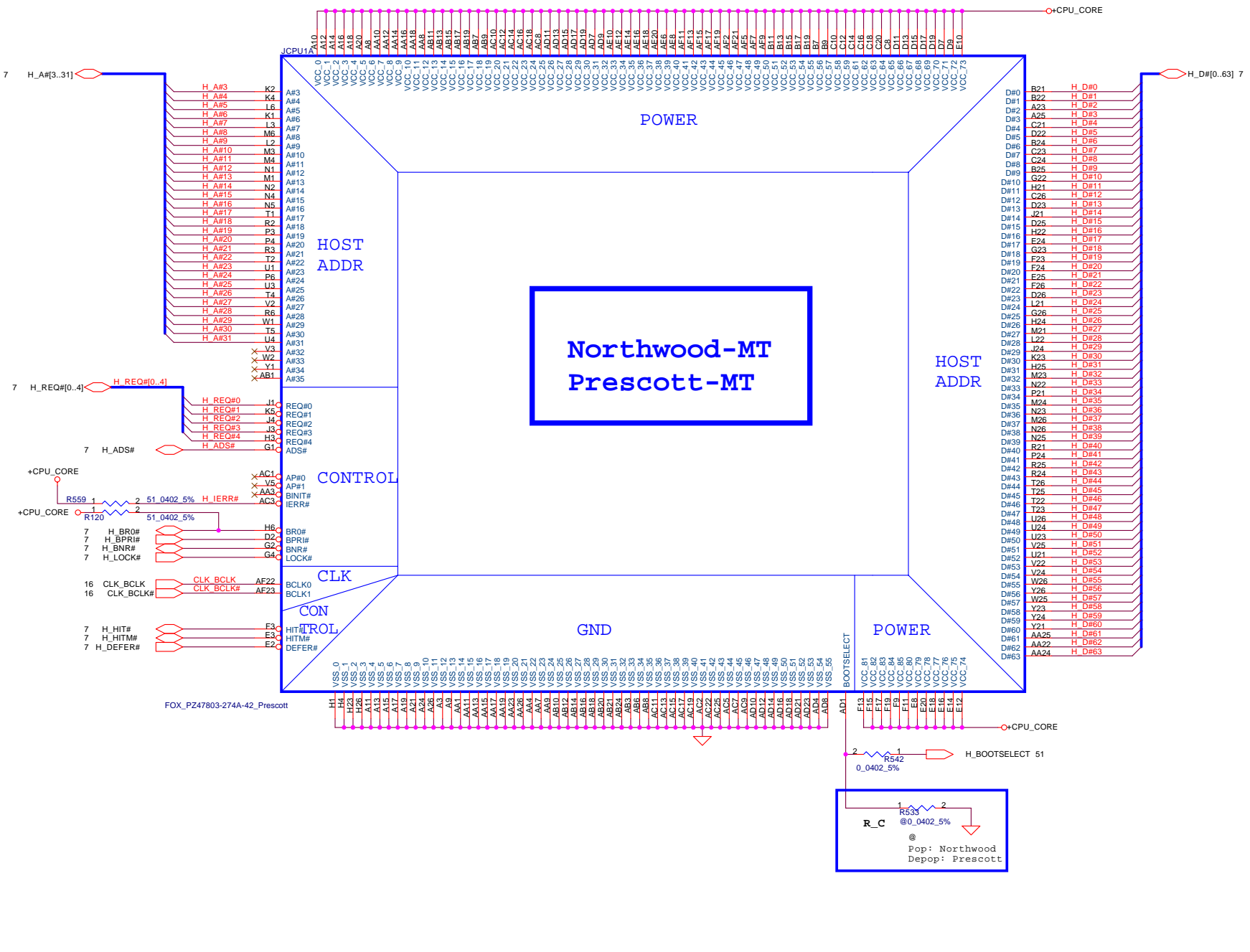
Vcc	3.3V +/- 5%			
Ra	100K +/- 5%			
Board ID	Rb	V _{AD_BID min}	V _{AD_BID typ}	V _{AD_BID max}
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

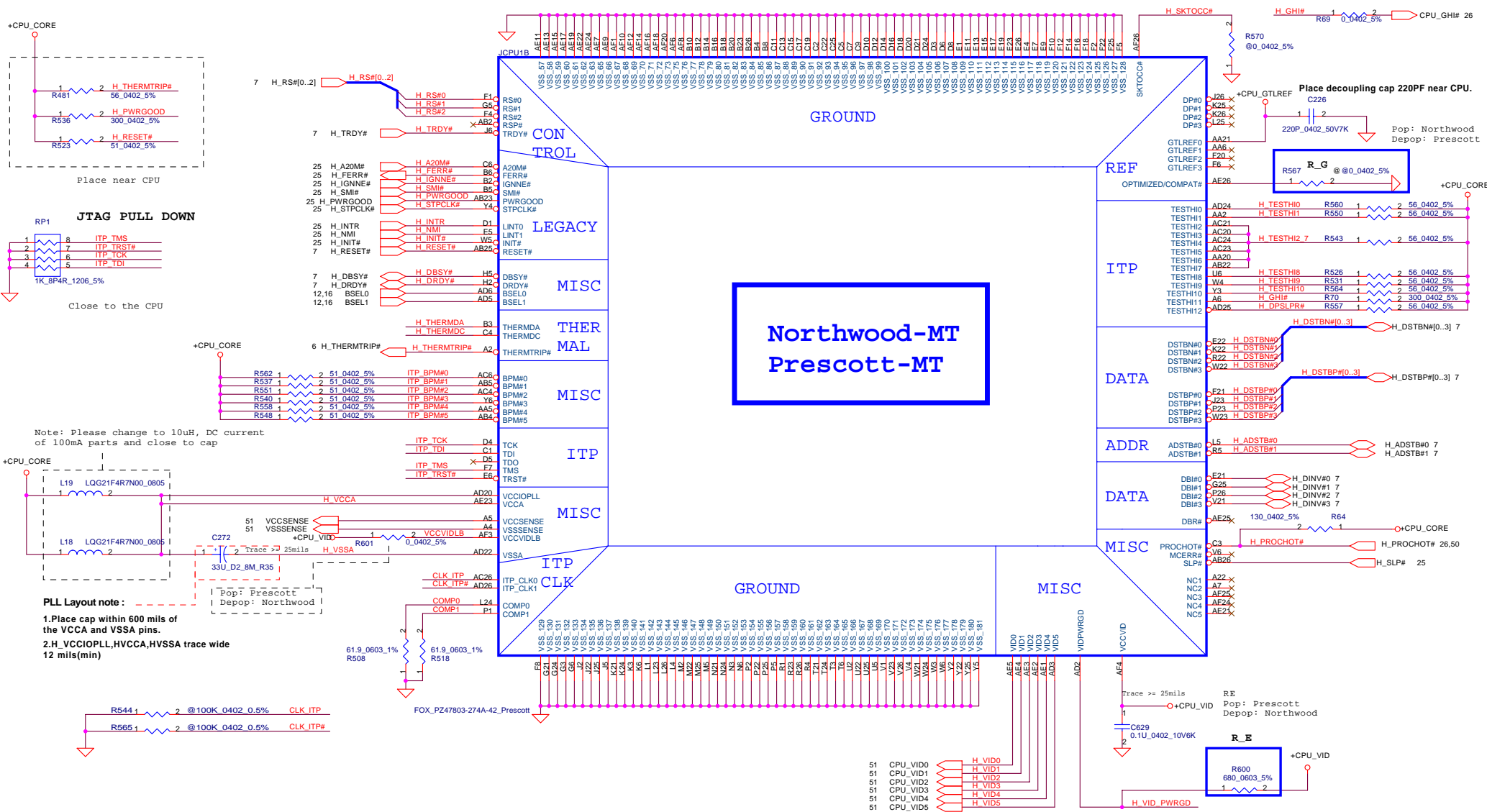
BIOS_ID: H EFW00
L EEW00

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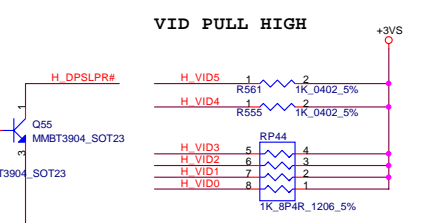
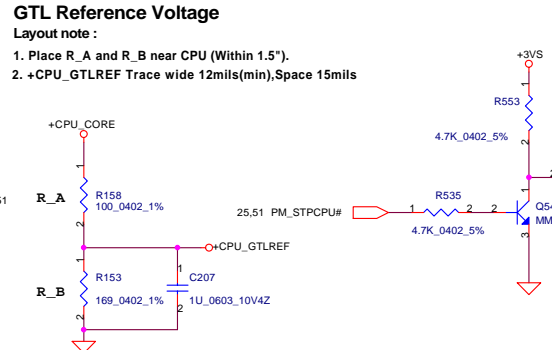
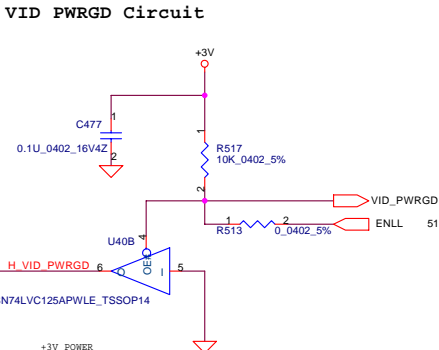
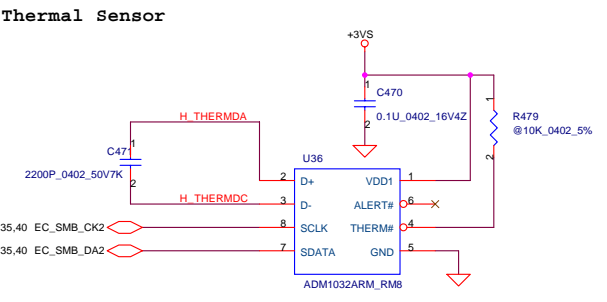
Title		Notes	
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Custom	LA-2371	1.0	
Date:	星期二, 七月 27, 2004	Sheet	3 of 56

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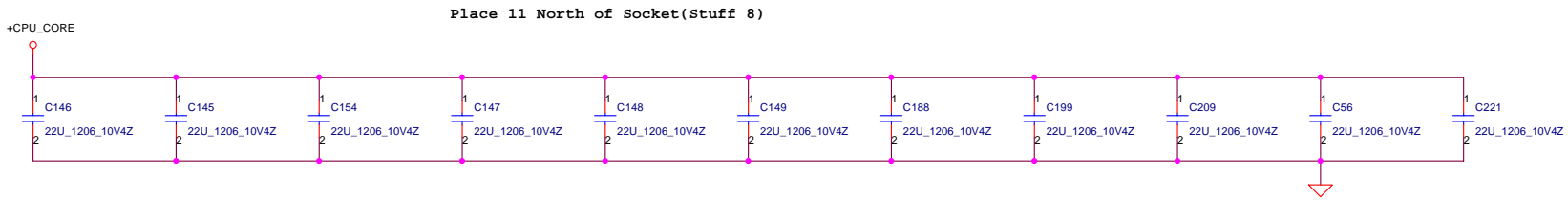




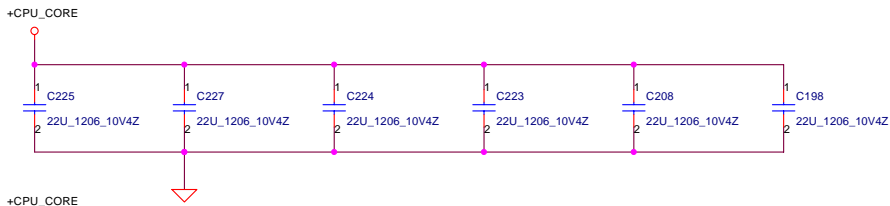
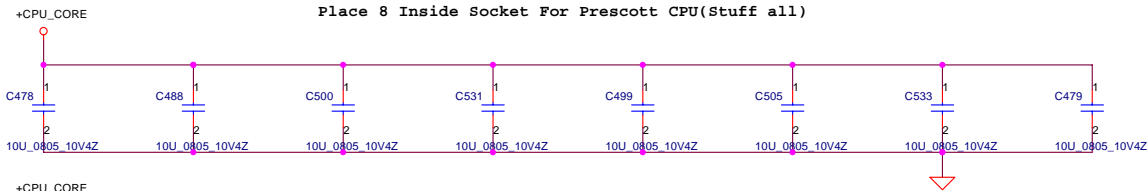
Northwood-MT Prescott-MT



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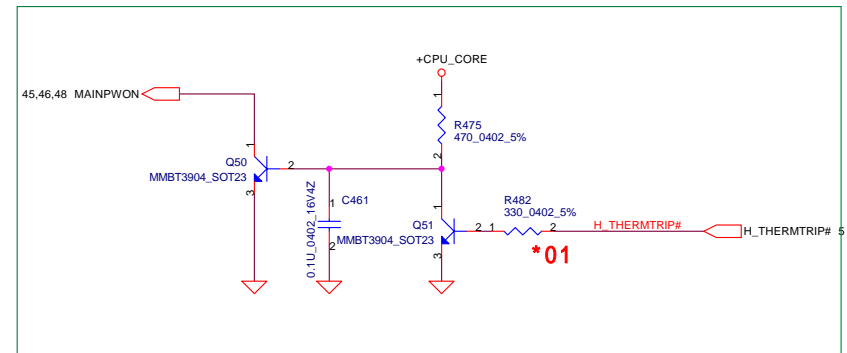
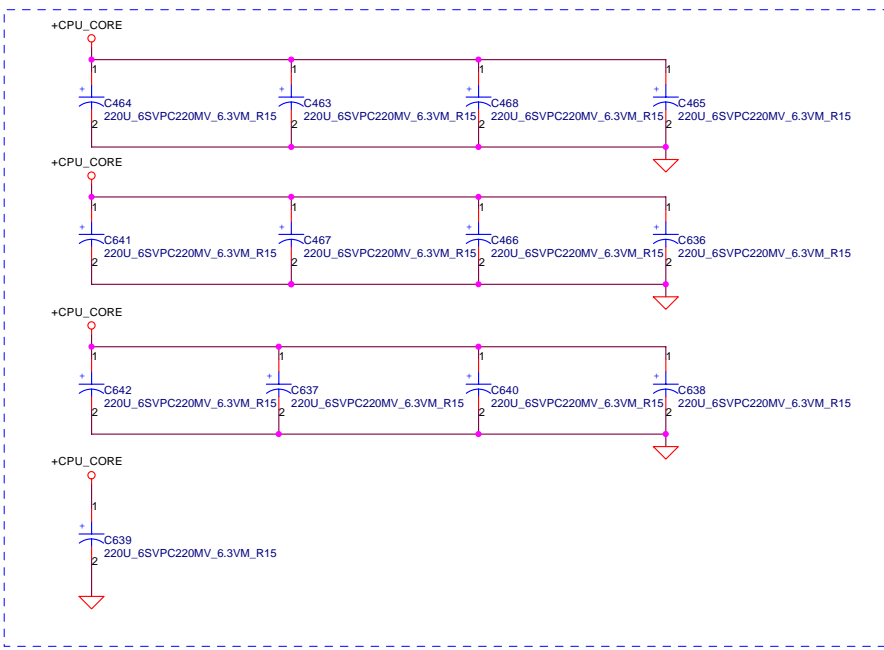
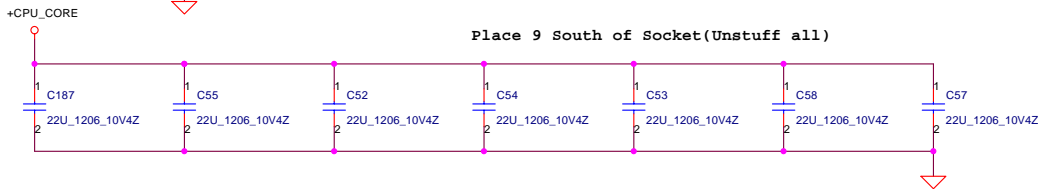


22uF depop reference
Springdale Customer Schematic R1.2 page82



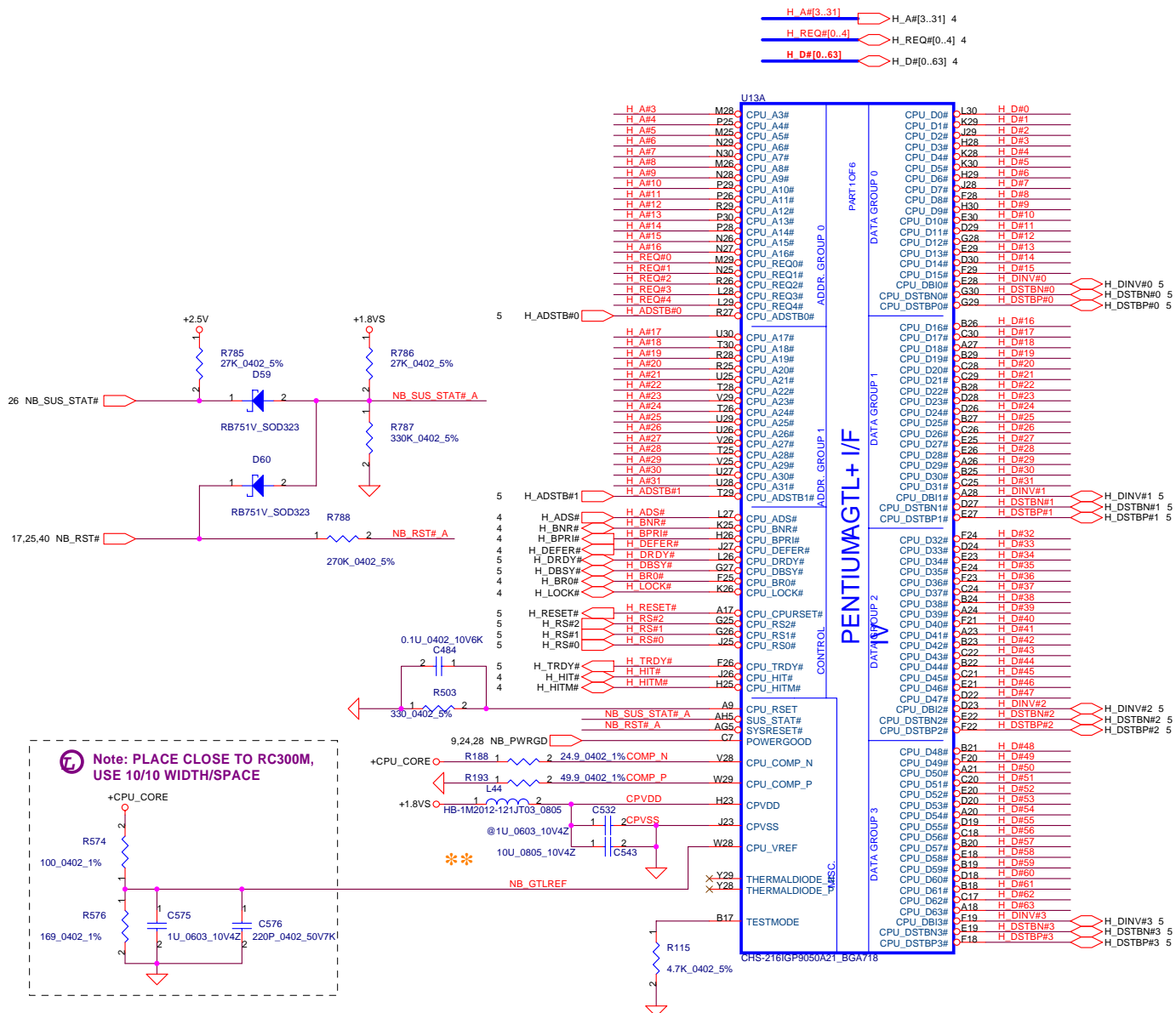
Decoupling Reference Document:
Springdale Chipset Platform Design guide Rev1.11
(12474)page239

Decoupling Reference Requirement:
560uF Polymer, ESR:5m ohm(each) * 10
22uF X5R * 32



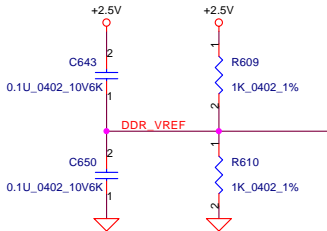
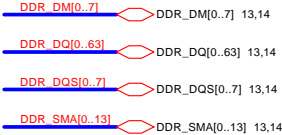
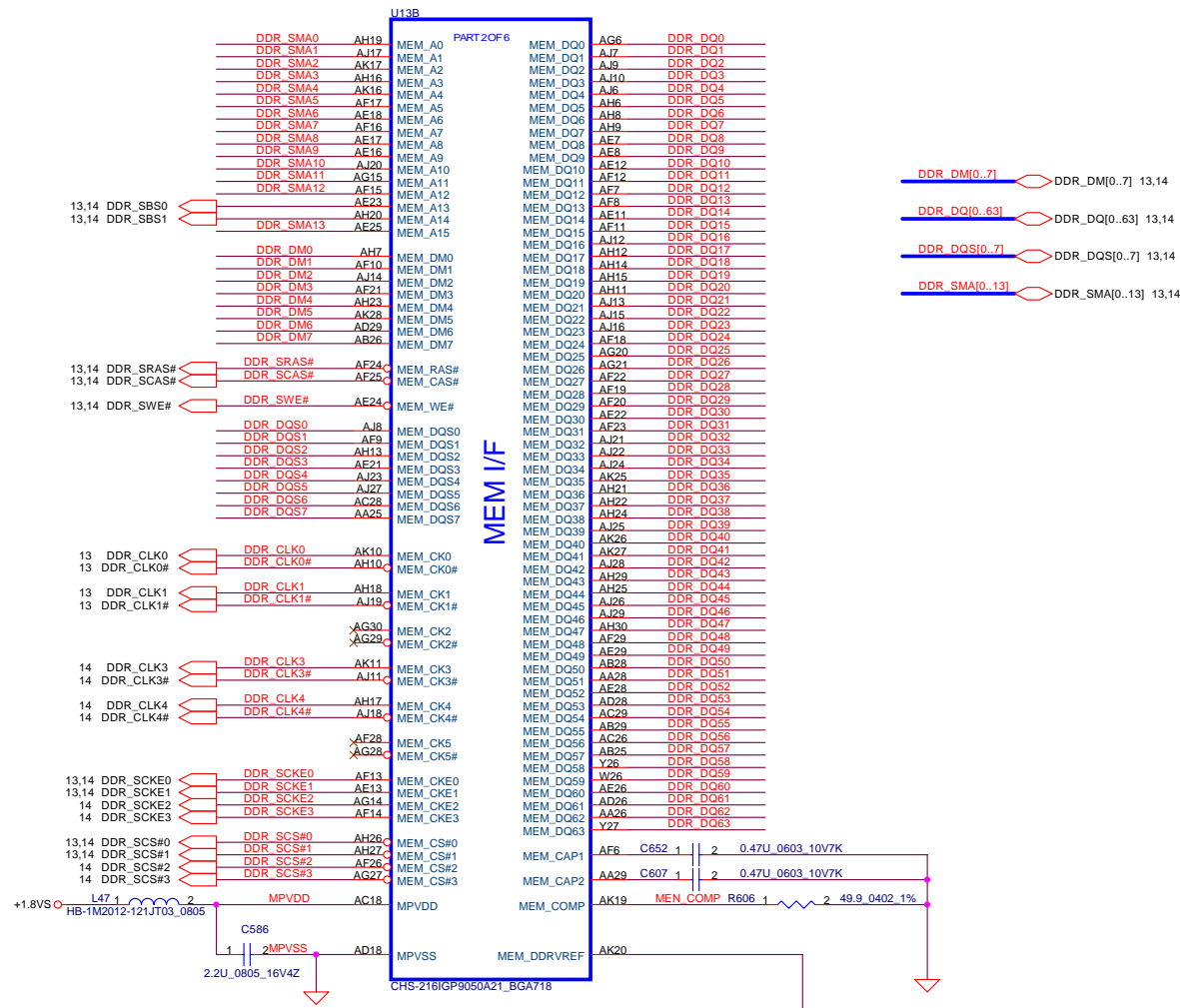
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Title		CPU Decoupling	
Size	Document Number	Rev 1.0	
Customer	LA-2371		
Date:	星期三, 七月 28, 2004	Sheet	6 of 56



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Compal Electronics, Inc.			
Title ATIRC300M-AGTL+			
Size	Document Number	Rev	
	LA-2371	1.0	
Date:	星期三, 七月 28, 2004	Sheet	7 of 56



DDR_VREF trace width of 20mils and space 20mils(min)

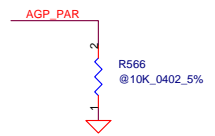
12.25 A_AD[0..31] A_AD0..31
 25 A_CBE#[0..3] A_CBE#0..3

U13C
 A_AD0 AK5 ALINK_AD0
 A_AD1 AJ5 ALINK_AD1
 A_AD2 AJ4 ALINK_AD2
 A_AD3 AH4 ALINK_AD3
 A_AD4 AL3 ALINK_AD4
 A_AD5 AJ2 ALINK_AD5
 A_AD6 AH2 ALINK_AD6
 A_AD7 AH1 ALINK_AD7
 A_AD8 AG2 ALINK_AD8
 A_AD9 AG1 ALINK_AD9
 A_AD10 AG3 ALINK_AD10
 A_AD11 AF3 ALINK_AD11
 A_AD12 AF2 ALINK_AD12
 A_AD13 AF2 ALINK_AD13
 A_AD14 AF4 ALINK_AD14
 A_AD15 AE3 ALINK_AD15
 A_AD16 AE4 ALINK_AD16
 A_AD17 AG2 ALINK_AD17
 A_AD18 AE6 ALINK_AD18
 A_AD19 AC2 ALINK_AD19
 A_AD20 AC4 ALINK_AD20
 A_AD21 AC4 ALINK_AD21
 A_AD22 AB3 ALINK_AD22
 A_AD23 AB2 ALINK_AD23
 A_AD24 AB6 ALINK_AD24
 A_AD25 AA2 ALINK_AD25
 A_AD26 AA4 ALINK_AD26
 A_AD27 AA5 ALINK_AD27
 A_AD28 AA6 ALINK_AD28
 A_AD29 Y3 ALINK_AD29
 A_AD30 Y5 ALINK_AD30
 A_AD31 Y6 ALINK_AD31

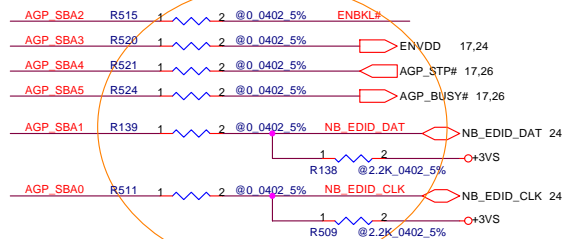
PART 3 OF 6
 PCI Bus 0 / A-Link I/F
 PCI BUS 1 / AGP Bus (GPIO, TMS, ZVPort)

AGP_AD0/TMD2_HSYNC Y2 AGP_AD0
 AGP_AD1/TMD2_VSYNC W3 AGP_AD1
 AGP_AD2/TMD2_D1 W3 AGP_AD2
 AGP_AD3/TMD2_D0 V2 AGP_AD3
 AGP_AD4/TMD2_D2 V1 AGP_AD4
 AGP_AD5/TMD2_D3 U1 AGP_AD5
 AGP_AD6/TMD2_D5 U3 AGP_AD6
 AGP_AD7/TMD2_D4 T2 AGP_AD7
 AGP_AD8/TMD2_D6 R2 AGP_AD8
 AGP_AD9/TMD2_D8 P3 AGP_AD9
 AGP_AD10/TMD2_D8 P2 AGP_AD10
 AGP_AD11/TMD2_D11 P2 AGP_AD11
 AGP_AD12/TMD2_D10 N3 AGP_AD12
 AGP_AD13/TMD2_D10 N2 AGP_AD13
 AGP_AD14 M3 AGP_AD14
 AGP_AD15 M2 AGP_AD15
 AGP_AD16 L1 AGP_AD16
 AGP_AD17/TMD1_VSYNC L2 AGP_AD17
 AGP_AD18/TMD1_HSYNC K3 AGP_AD18
 AGP_AD19/TMD1_DE K2 AGP_AD19
 AGP_AD20/TMD1_D1 J3 AGP_AD20
 AGP_AD21/TMD1_D1 J2 AGP_AD21
 AGP_AD22/TMD1_D2 H1 AGP_AD22
 AGP_AD23/TMD1_D3 H3 AGP_AD23
 AGP_AD24/TMD1_D7 F3 AGP_AD24
 AGP_AD25/TMD1_D6 G2 AGP_AD25
 AGP_AD26/TMD1_D9 F2 AGP_AD26
 AGP_AD27/TMD1_D8 E1 AGP_AD27
 AGP_AD28/TMD1_D11 E2 AGP_AD28
 AGP_AD29/TMD1_D10 E1 AGP_AD29
 AGP_AD30/TMS_HPD D2 AGP_AD30
 AGP_AD31 D1 AGP_AD31

AGP_AD[0..31] AGP_AD[0..31] 17
 AGP_SBA[0..7] AGP_SBA[0..7] 17
 AGP_C/BE#[0..3] AGP_C/BE#[0..3] 17
 AGP_ST[0..2] AGP_ST[0..2] 17



POP For EEQ00
 DEPOP For EFQ00



AGP2_SBSTB/AGP3_SBSTBF/NC/LVDS_BLON E5 AGP_SB_STBF 17
 AGP2_SBSTB/AGP3_SBSTB/NC/ENA_BL E6 AGP_SB_STBS 17
 AGP2_ADSTB0/AGP3_ADSTBF0/TMD2_CLK# T3 AGP_AD_STBF0 17
 AGP2_ADSTB0/AGP3_ADSTB0/TMD2_CLK# G3 AGP_AD_STBS0 17
 AGP2_ADSTB1/AGP3_ADSTBF1/TMD1_CLK# H2 AGP_AD_STBF1 17
 AGP2_ADSTB1/AGP3_ADSTB1/TMD1_CLK# H2 AGP_AD_STBS1 17

AGP2_CBE#0/AGP3_CBE0/TMD2_D7 R3 AGP_C/BE#0 17
 AGP2_CBE#1/AGP3_CBE1/TMD2_DE M1 AGP_C/BE#1 17
 AGP2_CBE#2/AGP3_CBE2 L3 AGP_C/BE#2 17
 AGP2_CBE#3/AGP3_CBE3/TMD1_D5 H1 AGP_C/BE#3 17

AGP2_IRDY#/AGP3_IRDY#/GPIO8/I2C_CLK P5 AGP_IRDY# 17
 AGP2_TRDY#/AGP3_TRDY#/TMS_DVI_CLK R6 AGP_TRDY# 17
 AGP2_STOP#/AGP3_STOP#/GPIO10/DDC_DATA T6 AGP_STOP# 17

AGP2_FRAME#/AGP3_FRAME/TMS_DVI_DATA T5 AGP_FRAME# 17
 AGP2_DEVSEL#/AGP3_DEVSEL#/GPIO9/I2C_DATA R5 AGP_DEVSEL# 17
 AGP2_PIPE#/AGP3_DBI_HI C1 AGP_DBI_HI 17
 AGP2_NC/AGP3_DBI_LO D3 AGP_DBI_LO 17
 AGP2_RBF#/AGP3_RBF N6 AGP_RBF# 17
 AGP2_WBF#/AGP3_WBF N5 AGP_WBF# 17

AGP2_SBA0/AGP3_SBA#0/GPIO0/VDDC_CNTL0 C3 AGP_SBA0
 AGP2_SBA1/AGP3_SBA#1/GPIO1/VDDC_CNTL1 C2 AGP_SBA1
 AGP2_SBA2/AGP3_SBA#2/GPIO2/LVDS_BLON# D4 AGP_SBA2
 AGP2_SBA3/AGP3_SBA#3/GPIO3/LVDS_DIGON E4 AGP_SBA3
 AGP2_SBA4/AGP3_SBA#4/GPIO4/STP_AGP# F6 AGP_SBA4
 AGP2_SBA5/AGP3_SBA#5/GPIO5/AGP_BUSY# F5 AGP_SBA5
 AGP2_SBA6/AGP3_SBA#6/GPIO6/LVDS_SSOUT G6 AGP_SBA6
 AGP2_SBA7/AGP3_SBA#7/GPIO7/LVDS_SSIN G5 AGP_SBA7
 AGP_ST0 L6 AGP_ST0
 AGP_ST1 M6 AGP_ST1
 AGP_ST2 L5 AGP_ST2

A_CBE#0 AG4C ALINK_CBE#0
 A_CBE#1 AE2C ALINK_CBE#1
 A_CBE#2 AC3C ALINK_CBE#2
 A_CBE#3 AA3C ALINK_CBE#3

12.25 A_PAR A_PAR AD5 PCI_PAR/ALINK_NC
 25 A_STROBE# A_STROBE# AC6C PCI_FRAME#/ALINK_STROBE#
 25 A_ACAT# A_ACAT# AC5C PCI_IRDY#/ALINK_ACAT#
 25 A_END# A_END# AD2C PCI_TRDY#/ALINK_END#
 17.25,30,34 PCI_PIRQ# R573 2 0_0402_5% W4 INT#A#
 25 A_DEVSEL# A_DEVSEL# AD3C ALINK_DEVSEL#
 25 A_OFF# A_OFF# AD6C PCI_STOP#/ALINK_OFF#

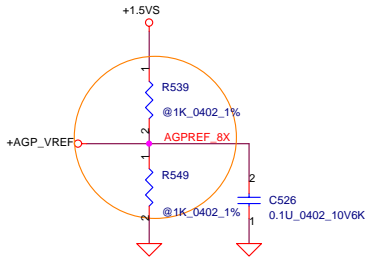
25 A_SBREQ# A_SBREQ# W5C ALINK_SBREQ#
 25 A_SBGNT# A_SBGNT# W6C ALINK_SBGNT#
 +3VS 1 R192 2 V5C PCI_REQ#/ALINK_NC
 8.2k_0402_5% X V6C PCI_GNT#/ALINK_NC

17 AGP_GNT# AGP_GNT# K5C AGP2_GNT#/AGP3_GNT
 17 AGP_REQ# AGP_REQ# K6C AGP2_REQ#/AGP3_REQ
 AGP8X_DET# M5 AGP8X_DET#
 AGPREF_8X J6 AGP_VREF/TMS_VREF

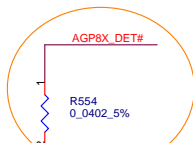


POP For EFQ00
 DEPOP For EEQ00

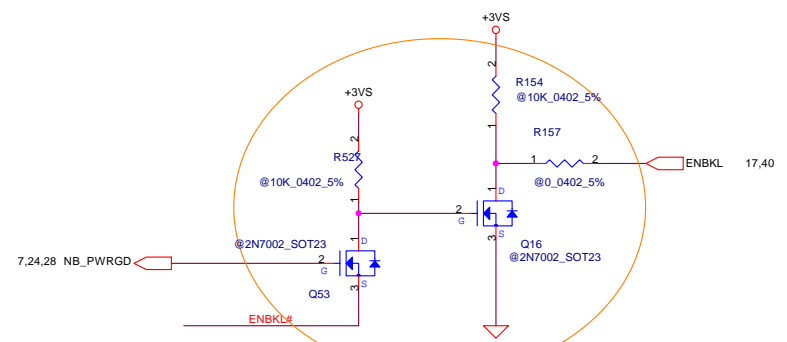
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POP For EEQ00
 DEPOP For EFQ00



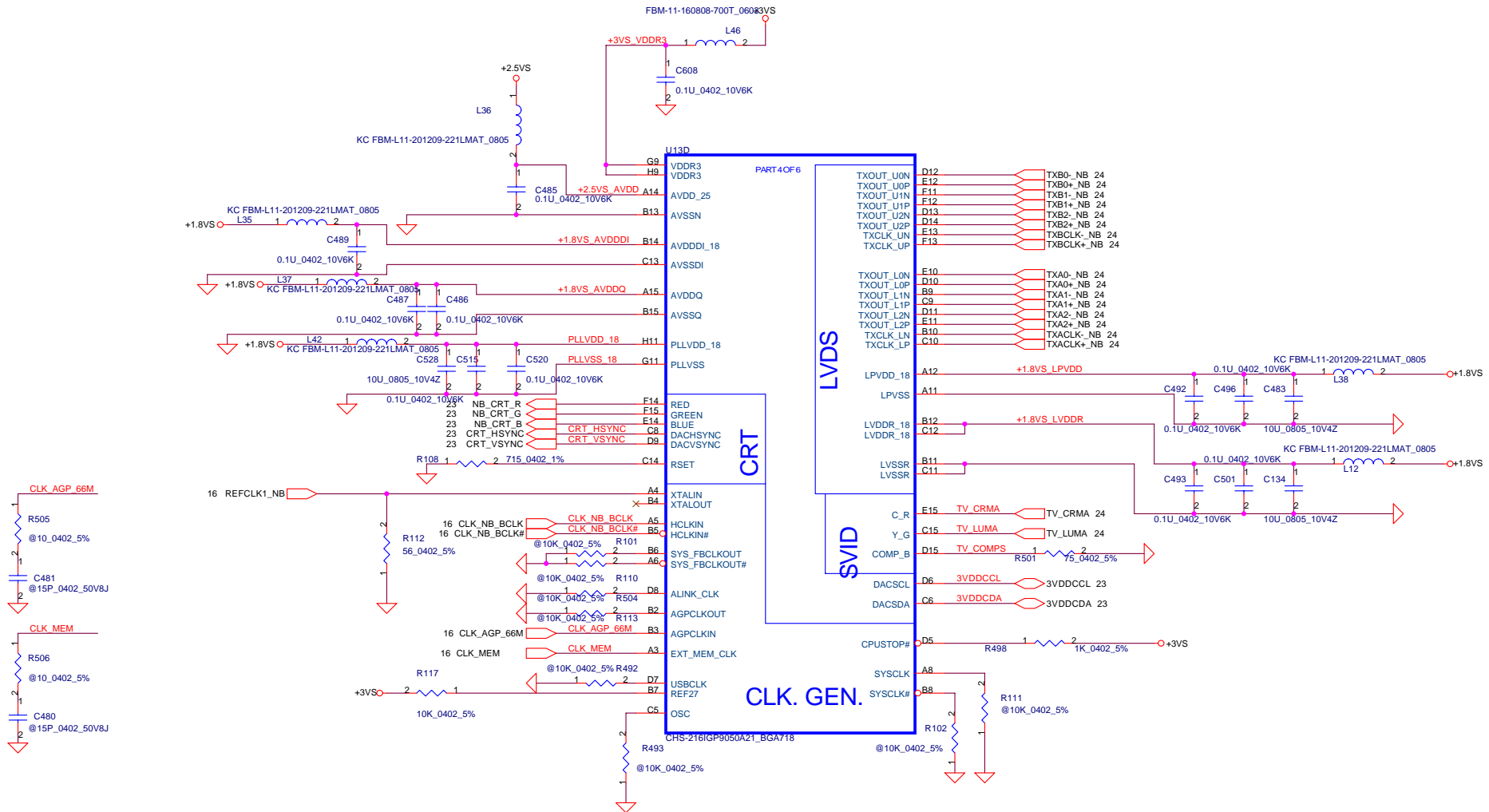
POP For EFQ00
 DEPOP For EEQ00



POP For EEQ00
 DEPOP For EFQ00

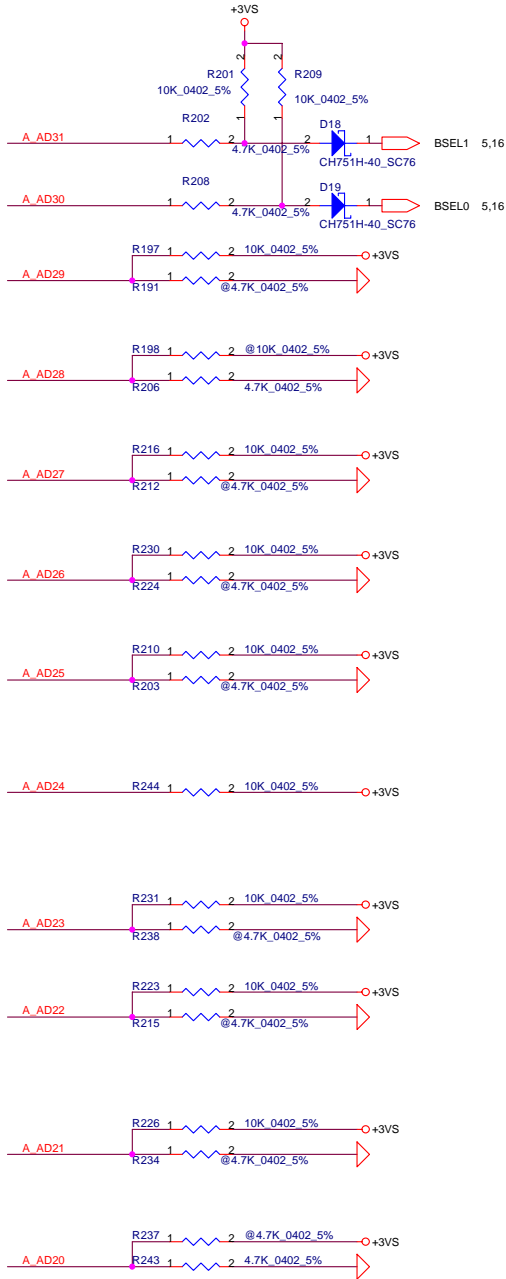
Title			
ATI RC300M-AGP, ALINK BUS			
Size	Document Number	Rev 1.0	
	LA-2371		
Date:	星期三, 七月 28, 2004	Sheet	9 of 56

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9.25 A_AD[0..31] A_AD[0..31]

A_AD[31..30] : FSB CLK SPEED

DEFAULT: 01
 00: 100 MHZ
 01: 133 MHZ
 10: 200MHZ
 11:166 MHZ

A_AD29: STRAP CONFIGURATION

DEFAULT:1
 0:REDUCEDE SET
 1:FULL SET

A_AD28: SPREAD SPECTRUM ENABLE

DEFAULT:0
 0: DISABLE
 1: ENABLE

A_AD27: FrcShortReset#

DEFAULT: 1
 0:TEST MODE
 1:NORMAL MODE

A_AD26 : ENABLE IOQ

DEFAULT: 1
 0: IOQ=1
 1: IOQ=12

A_AD25/A_AD17 : CPU VOLTAGE[1..0]

DEFAULT: 10
 AD25=1 DESTOP CPU
 AD25=0 MOBILE CPU
 AD17--DON'T CARE
 00: 1.05V
 01: 1.35V
 11: 1.75V
 10: 1.45V

A_AD24 : MOBILE CPU SELECT

DEFAULT: 1
 0: BANIAS CPU
 1: OTHER CPU

A_AD23 : CLOCK BYPASS DISABLE

DEFAULT: 1
 0: TEST MODE
 1: NORMAL

A_AD22 : OSC PAD OUTPUT PCICLK

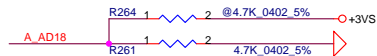
DEFAULT : 1
 0: PCICLK OUT
 1: OSC CLK OUT

A_AD21 : AUTO_CAL ENABLE

DEFAULT : 1
 0: DISABLE
 1: ENABLE

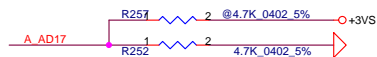
A_AD20 : INTERNAL CLK GEN ENABLE

DEFAULT : 0
 0: DISABLE
 1: ENABLE



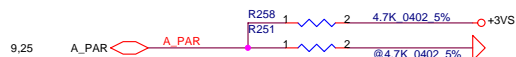
A_AD18 : ENABLE PHASE CALIBRATION

DEFAULT: 0
 0: DISABLE
 1: ENABLE



A_AD25/A_AD17 : CPU VOLTAGE[1..0]

DEFAULT: 0
 00: 1.05V
 01: 1.35V
 11: 1.75V
 10: 1.45V

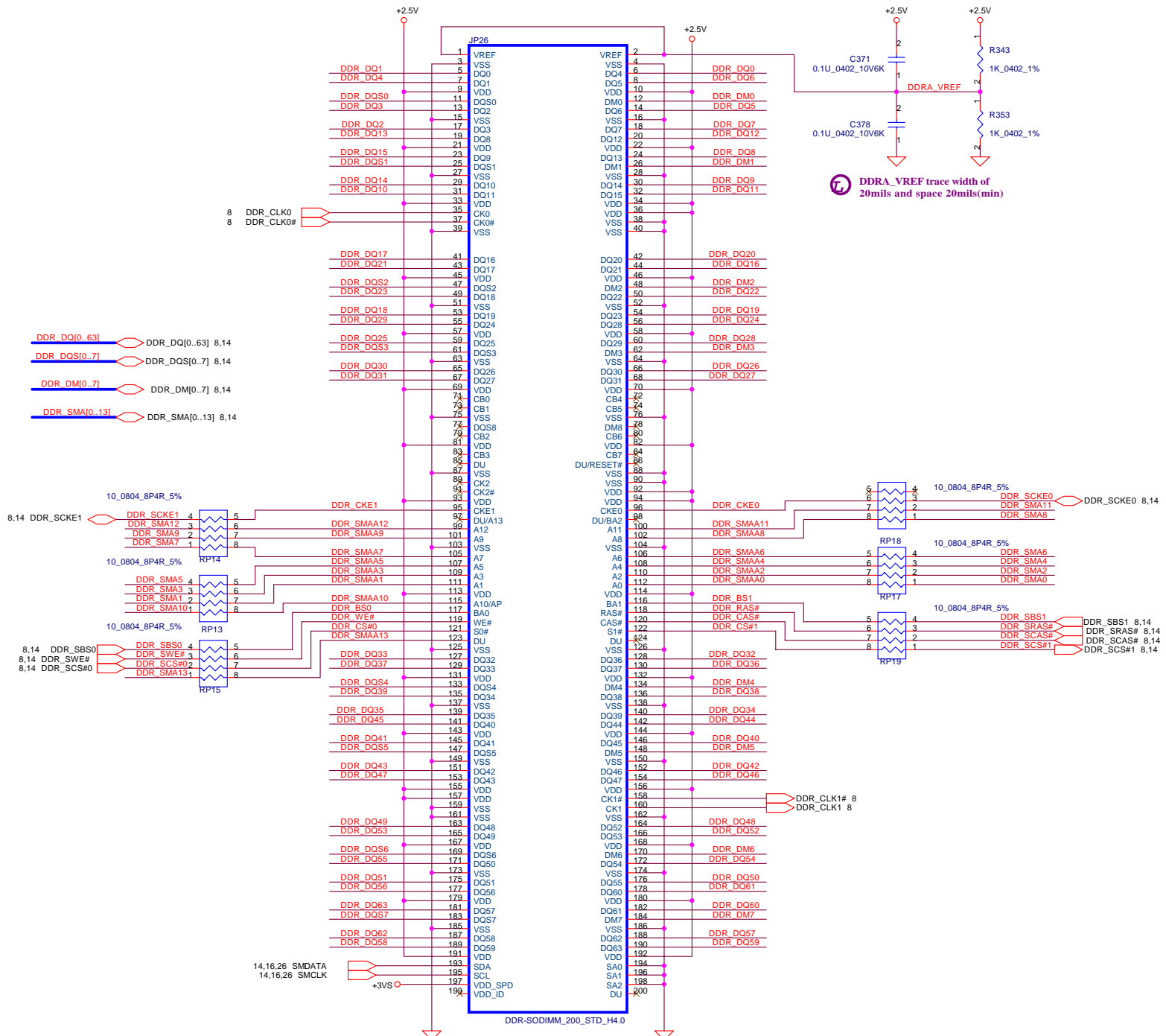


PAR: EXTENDED DEBUG MODE

DEFAULT: 1
 0: DEBUG MODE
 1: NORMAL

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Compal Electronics, Inc.		
ATI RC300M-SYSTEM STRAP		
Size	Document Number	Rev
	LA-2371	1.0
Date:	星期三, 七月 28, 2004	Sheet 12 of 56



DDR_VREF trace width of 20mils and space 20mils(min)

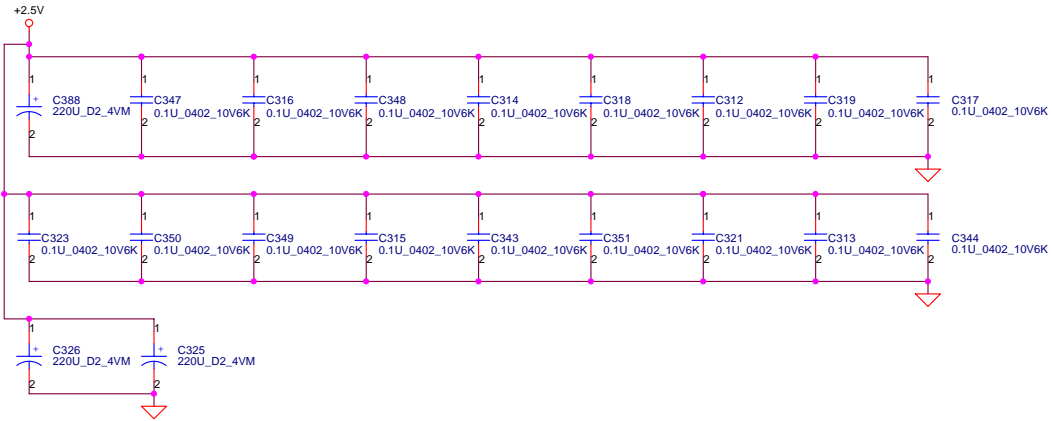
Layout note

Layout note
Place Add/Command resistors
Close to Pin, max L = 300 mils

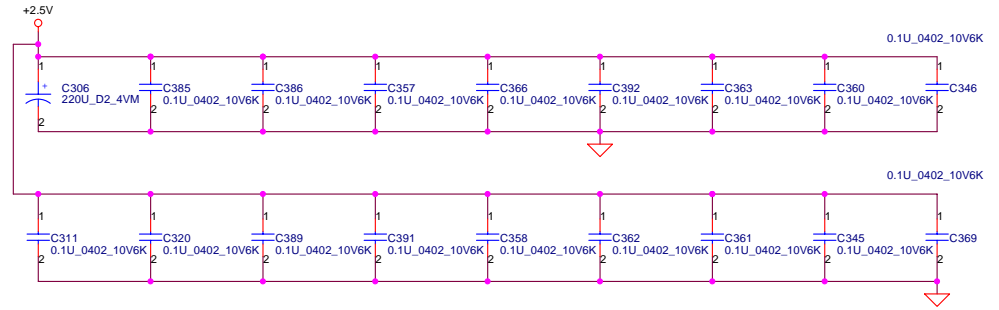
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Title			Compal Electronics, Inc.		
Size			Document Number		
Date:			Rev 1.0		
LA-2371			Rev 1.0		
Date: 星期三, 七月 28, 2004			Sheet 13 of 56		

Layout note :
Distribute as close as possible to DDR-SODIMM0.



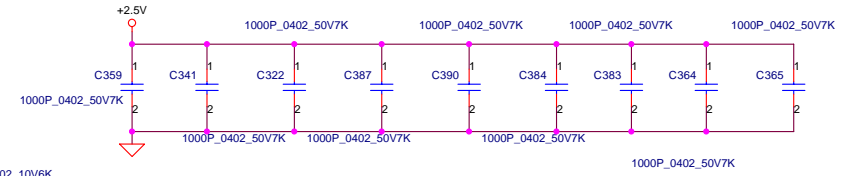
Layout note :
Distribute as close as possible to DDR-SODIMM1.



Layout note :
Place one cap close to every 2 pull up resistors termination to +1.25VS



Layout note :
for EMI solution



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Compal Electronics, Inc.			
DDR SODIMM Decoupling			
Size	Document Number	Rev	
	LA-2371	1.0	
Date:	星期二, 七月 27, 2004	Sheet	15 of 56

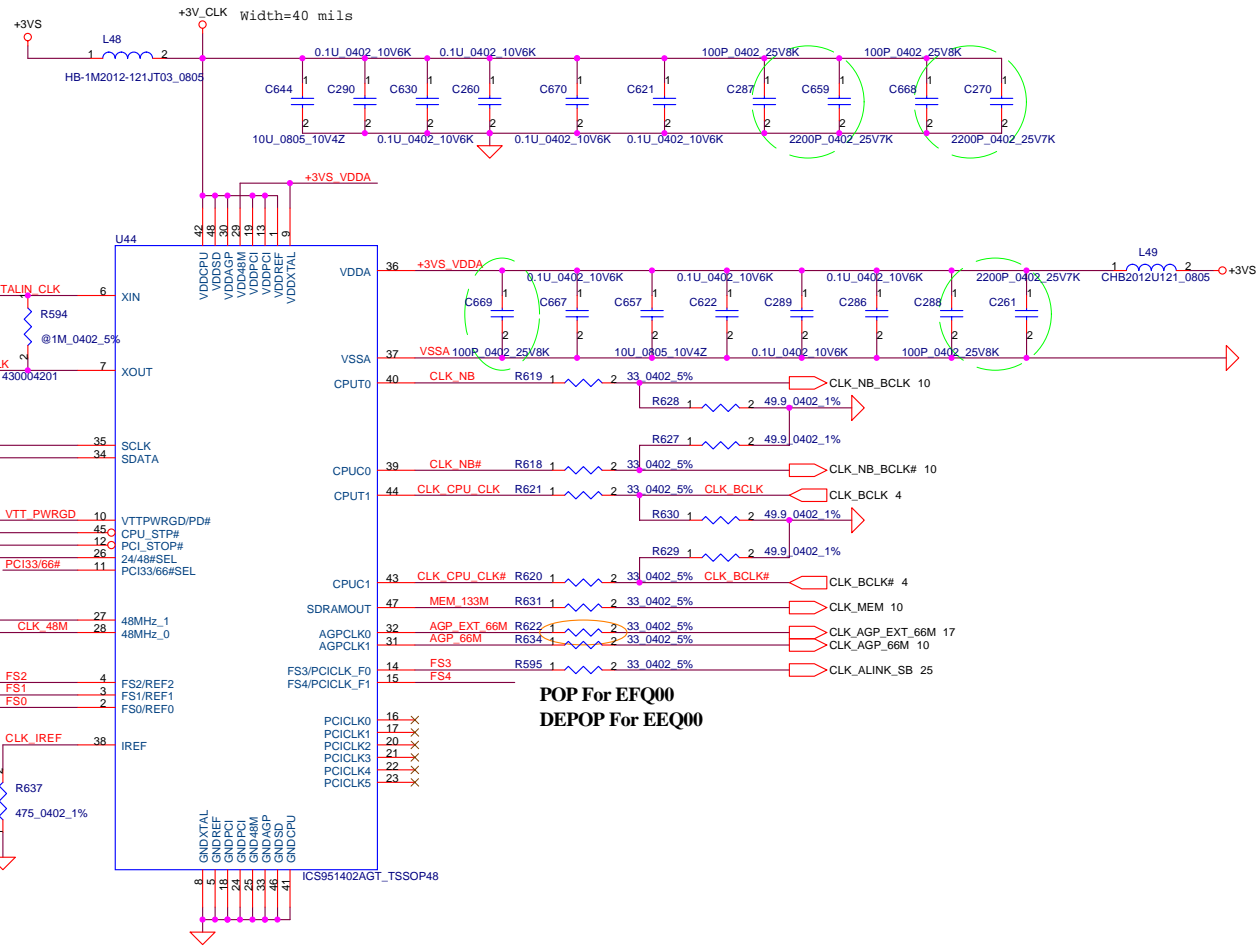
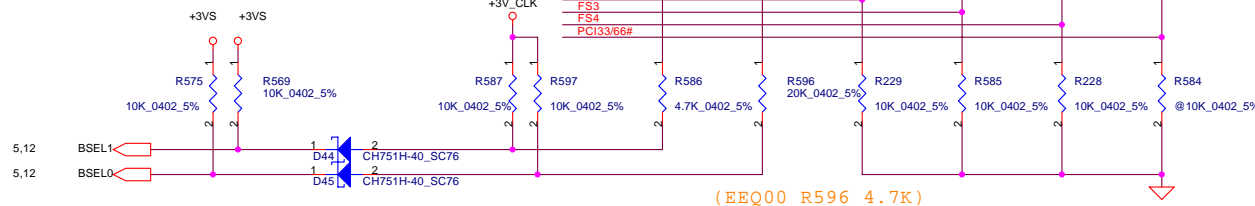
CLOCK FREQUENCY SELECT TABLE

FS4	FS3	FS2	FS1	FS0	CPU	MEM	With Spread Enabled...
0	0	0	1	0	200	200	** Spread OFF OR Center spread +/-0.3%
0	0	0	0	1	133	133	
0	0	0	0	0	100	100	
0	0	0	0	0	100	100	

A-LINK FREQ

** PCI33/66# = HIGH	66MHZ
PCI33/66# = LOW	33MHZ

Note: 0 = PULL LOW
1 = PULL HIGH



POP For EFQ00
DEPOP For EEQ00

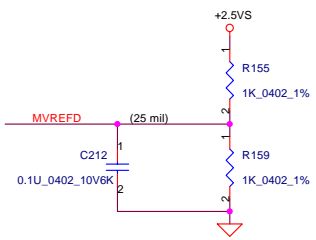
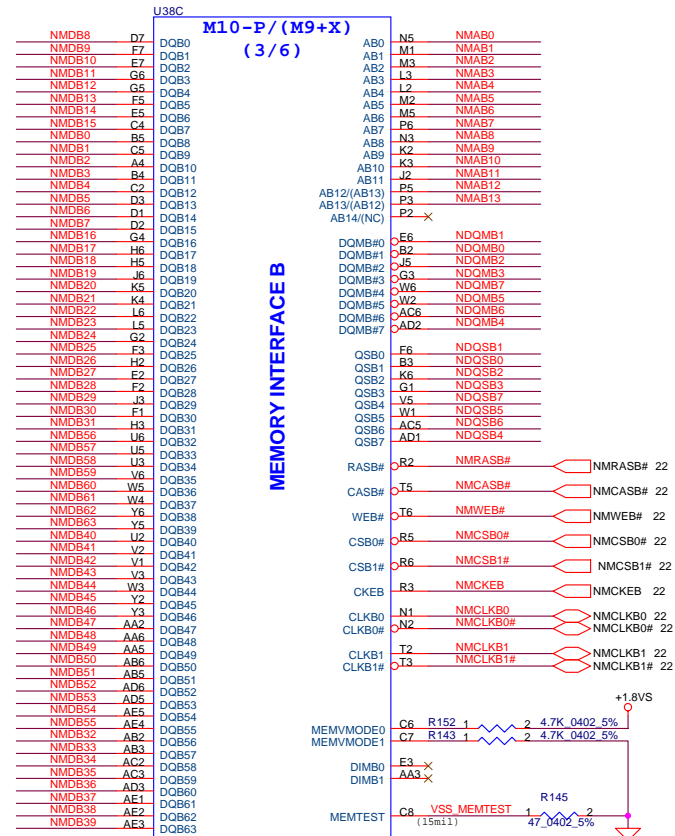
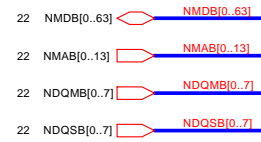
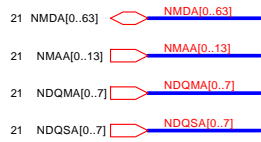
Compal Electronics, Inc.

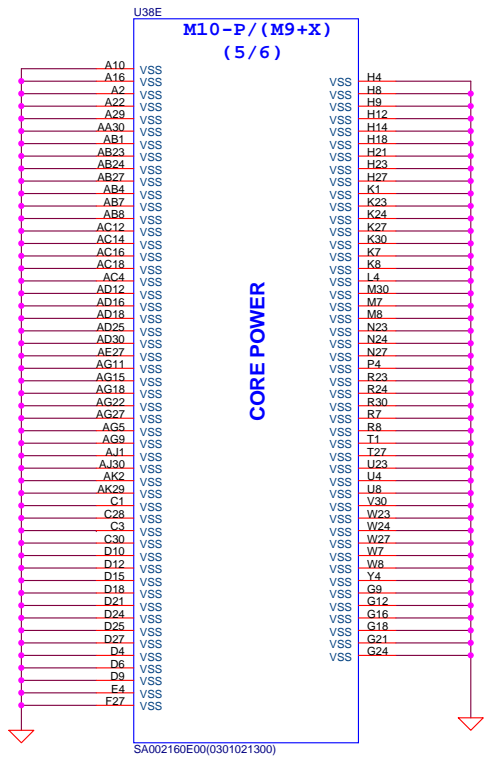
Clock Generator

Title	Clock Generator		Rev	1.0
Size	Document Number	LA-2371		
Date:	星期三, 七月 28, 2004	Sheet	16	of 56

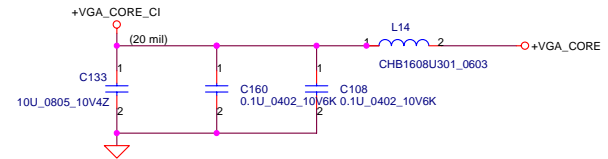
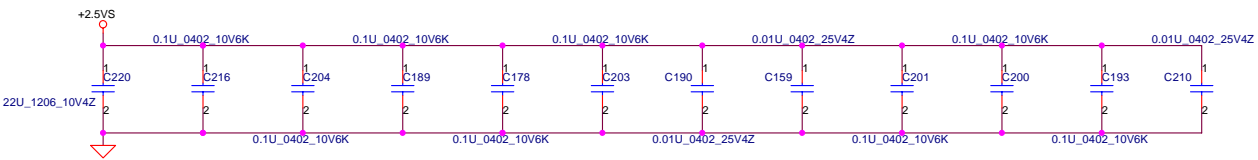
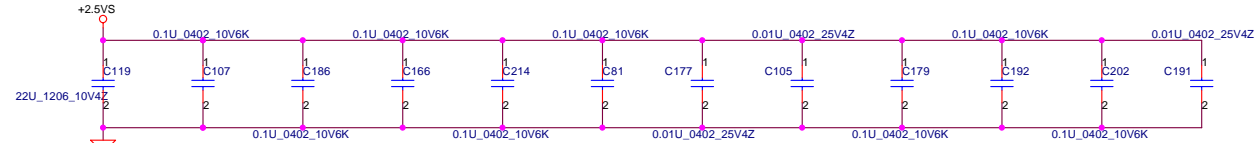
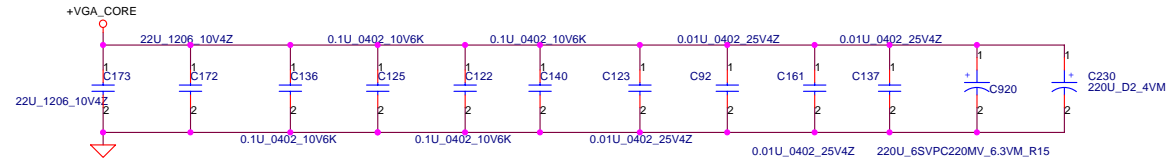
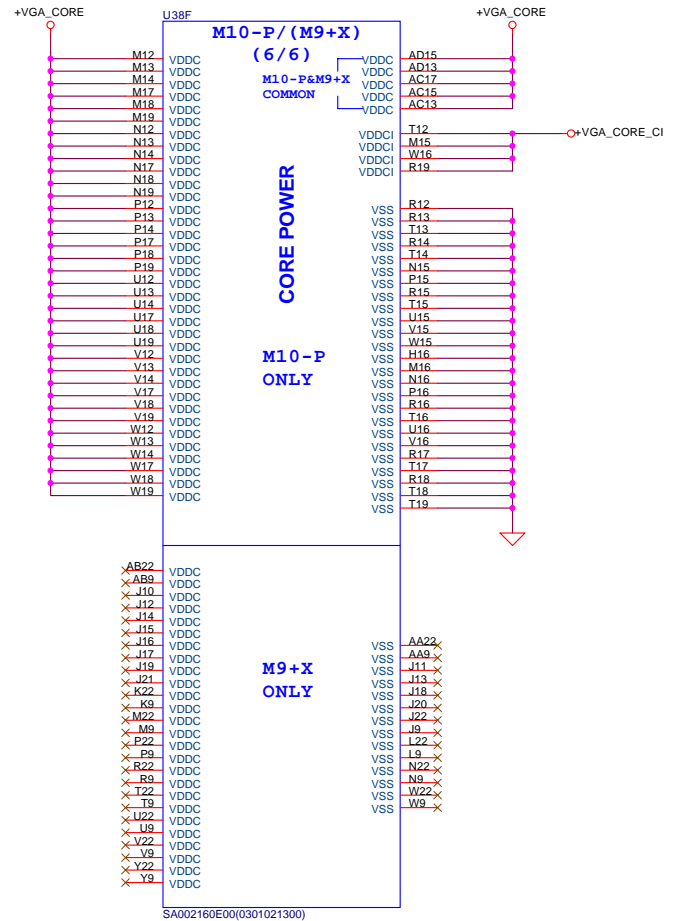
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MEMORY INTERFACE A





POWER INTERFACE



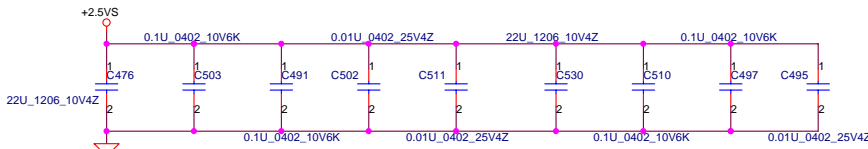
As close as possible to related pin

As close as possible to related pin

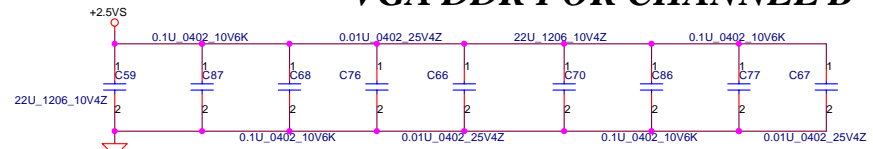
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Compal Electronics, Inc.		
Title ATI M10-P/M9+X POWER-B		
Size	Document Number LA-2371	Rev 1.0
Date: 星期二, 七月 27, 2004	Sheet 20	of 56

VGA DDR FOR CHANNEL B

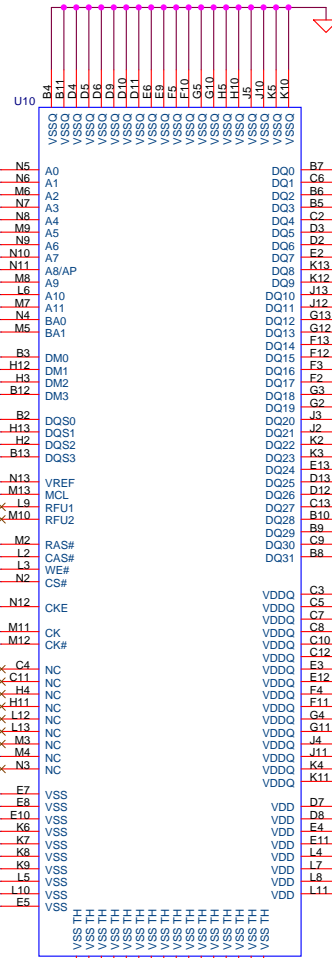


As close as possible to related pin

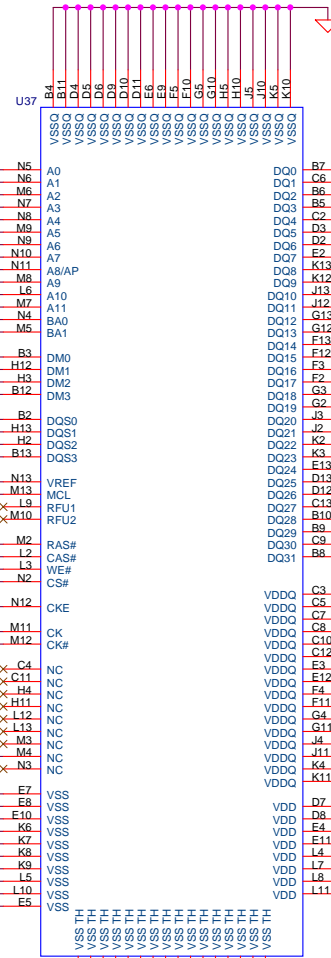


As close as possible to related pin

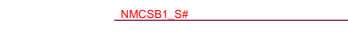
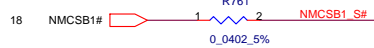
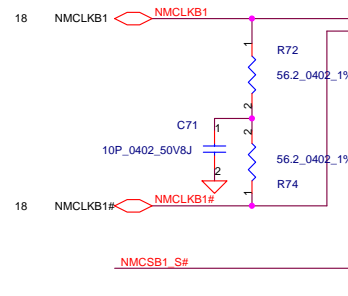
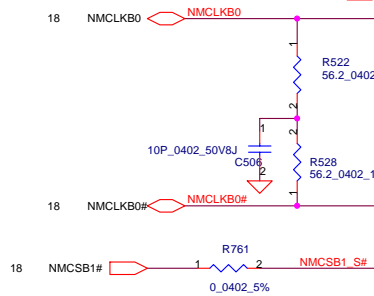
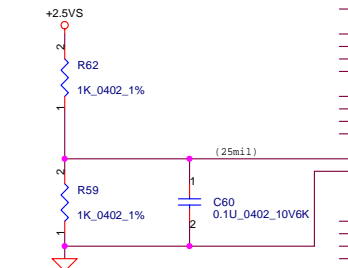
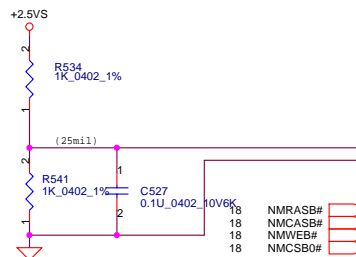
- 18 NMAB[0..13] NMAB[0..13]
- 18 NMDB[0..63] NMDB[0..63]
- 18 NDQMB[0..7] NDQMB[0..7]
- 18 NDQSB[0..7] NDQSB[0..7]



K4D263238A-GC_FBGA144

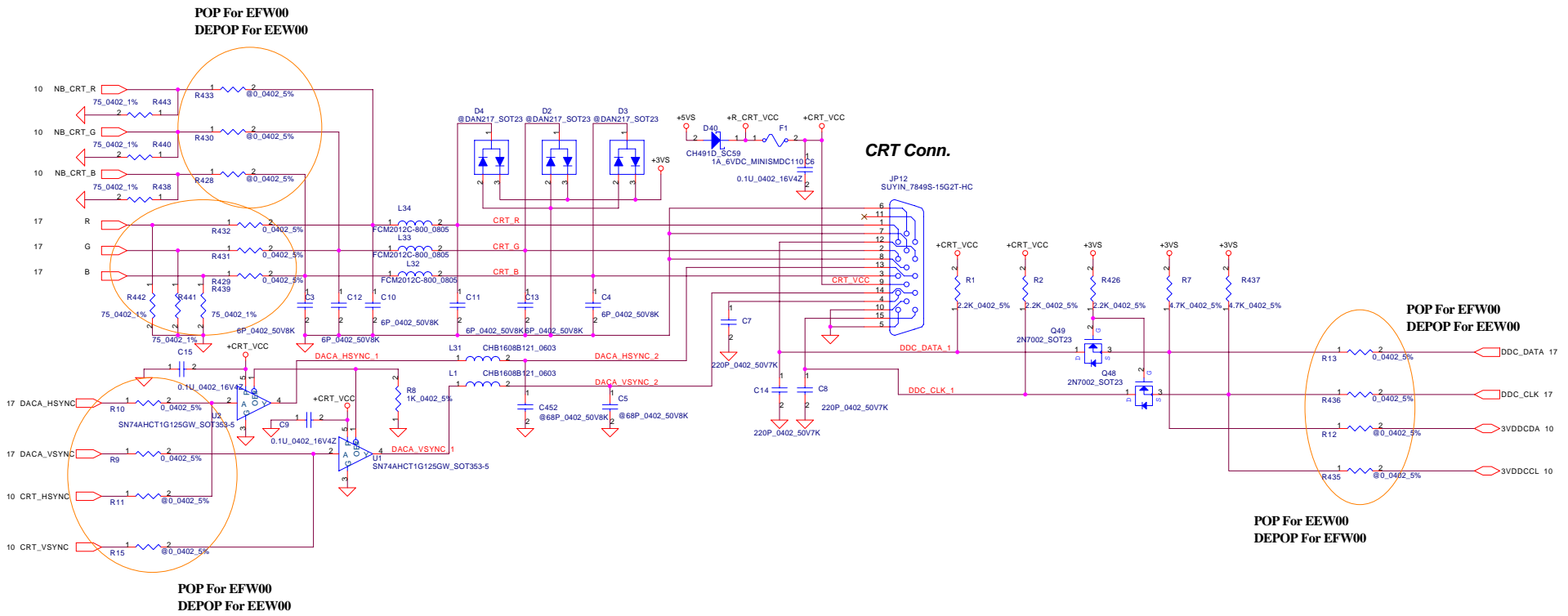


K4D263238A-GC_FBGA144



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VGA DDR FOR CHANNEL B		
Size	Document Number	Rev
	LA-2371	1.0
Date:	星期三, 七月 28, 2004	Sheet 22 of 56

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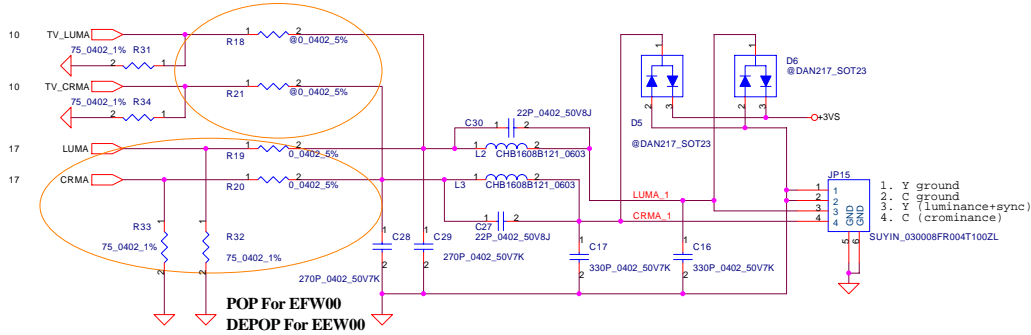


Compal Electronics, Inc.			
Title CRT Connector			
Size C	Document Number LA-2371	Rev 1.0	
Date: 2004年7月28日	Sheet 23	of 56	

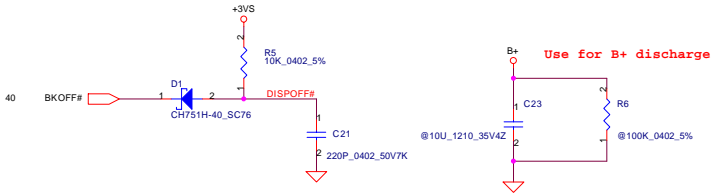
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POP For EEQ00
DEPOP For EFQ00

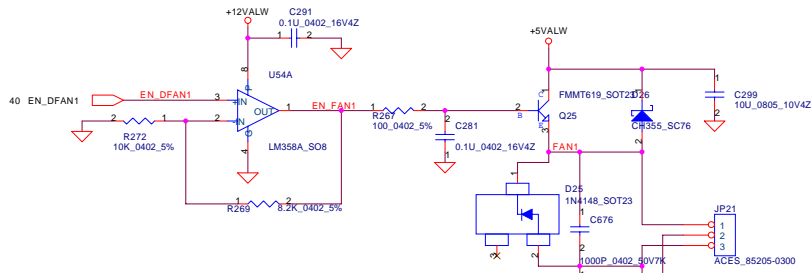
TV-OUT Conn.



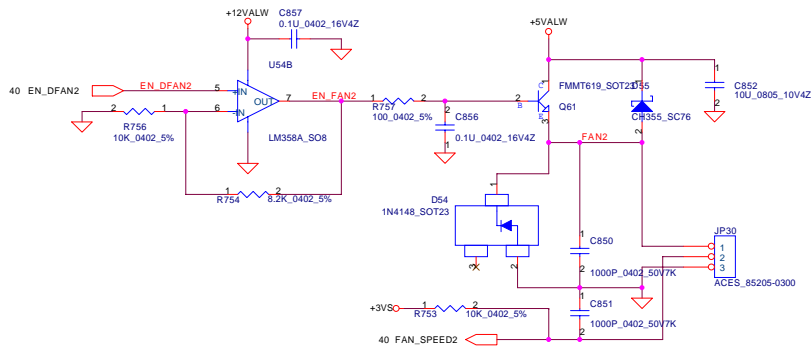
POP For EFW00
DEPOP For EEW00



FAN CONN. 1

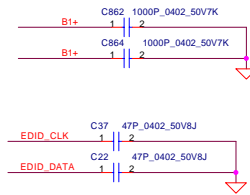
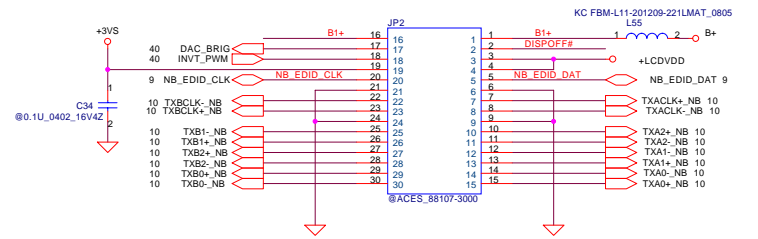


FAN CONN. 2

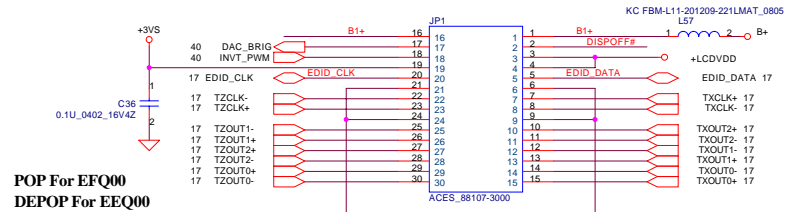


Width: 40mils

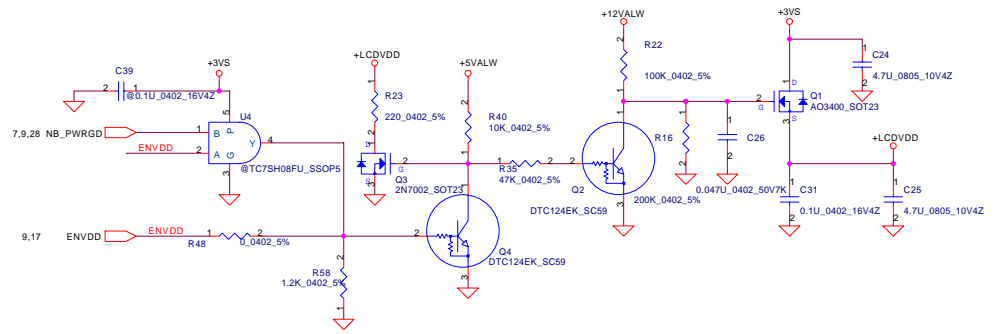
POP For EEQ00
DEPOP For EFQ00



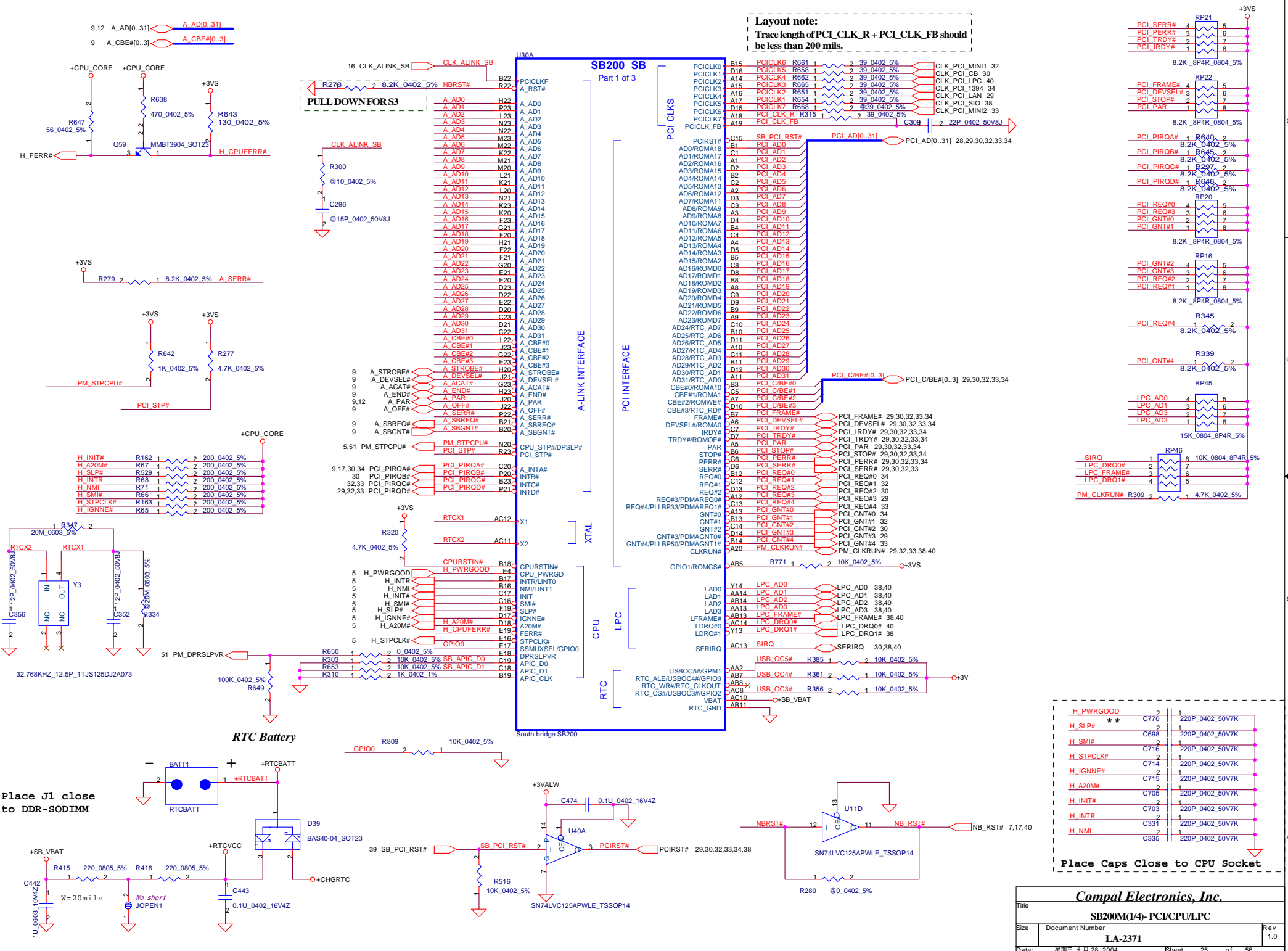
Width: 40mils



POP For EFQ00
DEPOP For EEQ00

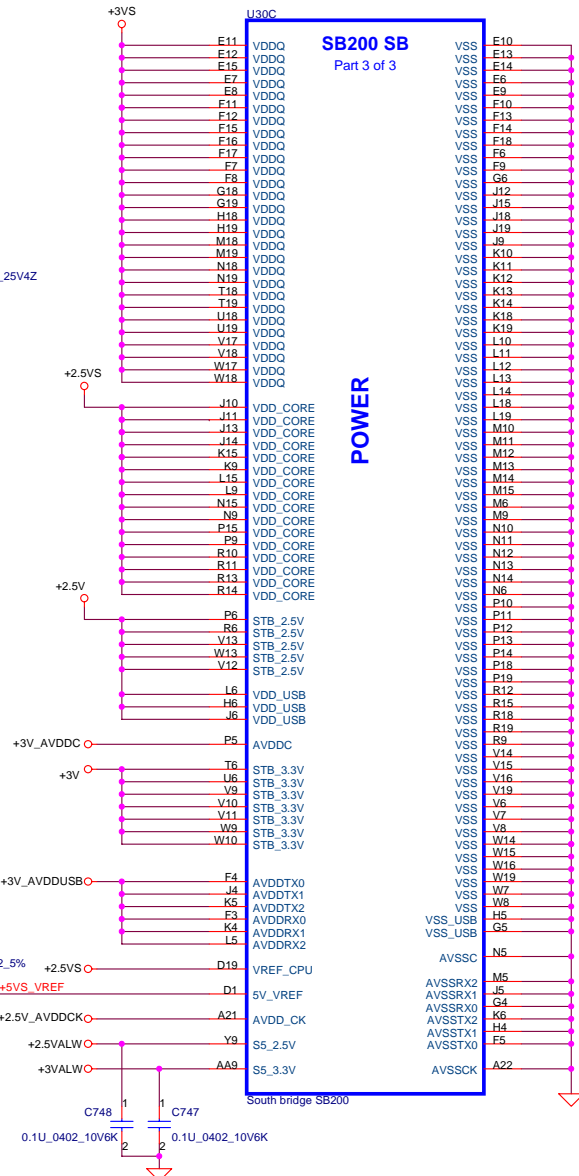
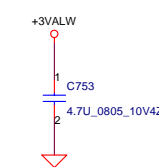
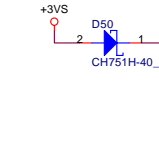
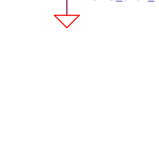
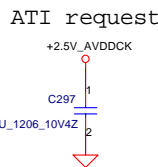
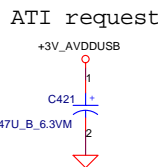
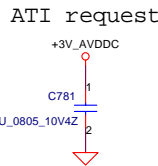
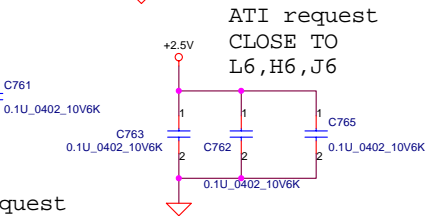
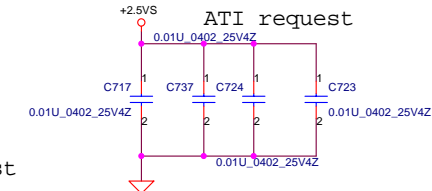
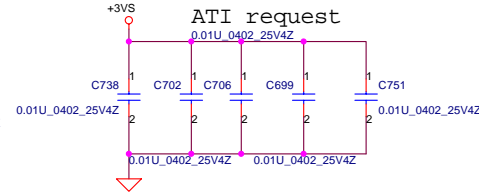
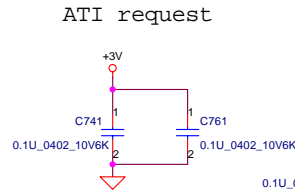
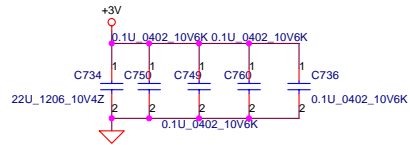
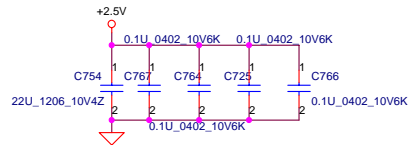
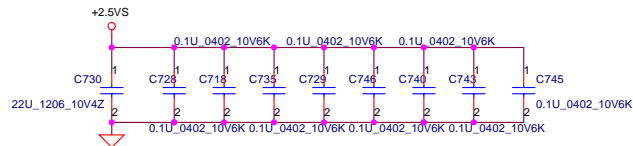
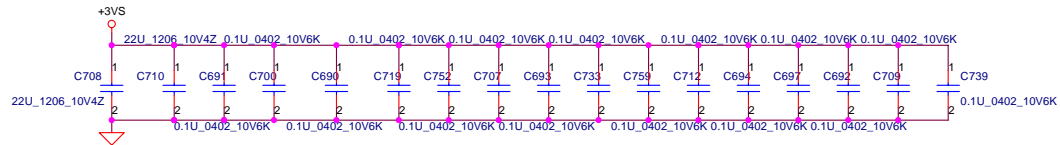


Layout note:
Trace length of PCI_CLK_R + PCI_CLK_FB should be less than 200 mils.

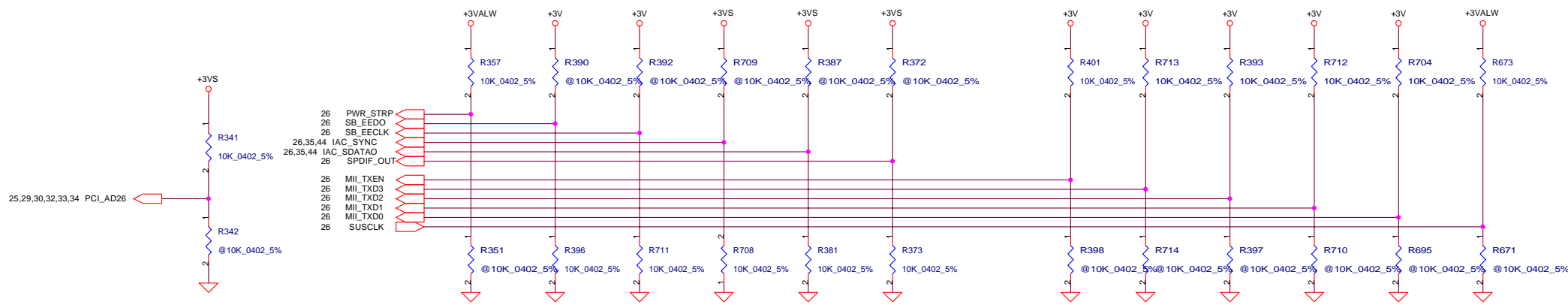


Compal Electronics, Inc.

Title		
SB200M(I/4)-PCI/CPU/LPC		
Size	Document Number	Rev
	LA-2371	1.0
Date:	星期三, 七月 28, 2004	Sheet 25 of 56



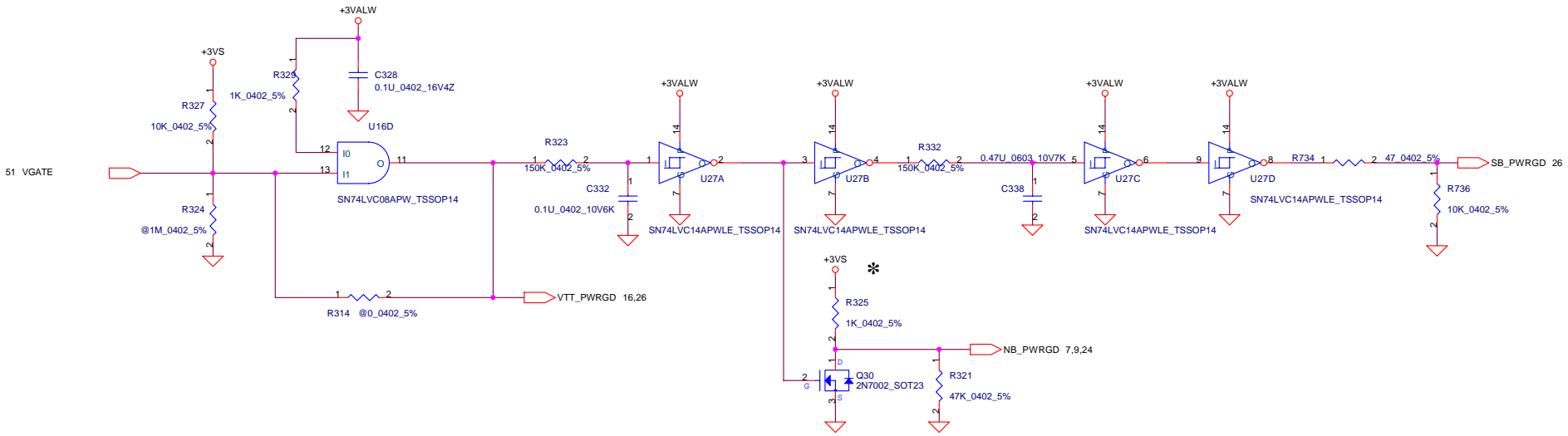
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PCI_AD26 H: ENE910
L: NS87591

REQUIRED SYSTEM STRAPS

	PWR_STRP	IGN DEBUG EEDO	EECK	IAC_SYNC	IAC_SDATA0	SPDIF_OUT	SPEEDSTEP CPU_STP#	FREQLTCH TX_EN	ETHERNET TXD[3:0]	32KHZ_S5
STRAP HIGH	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS	ROM ON PCI BUS DEFAULT	INIT ACTIVE HIGH DEFAULT	33MHz NB BUS DEFAULT	SIO 24MHz DEFAULT	ENABLE SPEED STEP DEFAULT	DISABLE CPU FREQ SETTING DEFAULT	PROCESSOR FREQ MULTIPLIER	32KHZ OUTPUT FROM SB200 (INT RTC) DEFAULT
STRAP LOW	AUTO PWR ON	IGNORE DEBUG STRAPS DEFAULT	ROM ON LPC BUS DEFAULT	INIT ACTIVE LOW (PIII) DEFAULT	HI SPEED A-LINK DEFAULT	SIO 48MHz DEFAULT	DISABLE SPEED STEP DEFAULT	ENABLE CPU FREQ SETTING		32KHZ INPUT TO SB200 (EXT RTC)



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LAN RTL8100C(L)

25,28,30,32,33,34 PCI_AD[0..31]

- PCI_AD0 104 AD0
- PCI_AD1 103 AD1
- PCI_AD2 102 AD2
- PCI_AD3 98 AD3
- PCI_AD4 97 AD4
- PCI_AD5 96 AD5
- PCI_AD6 95 AD6
- PCI_AD7 93 AD7
- PCI_AD8 90 AD8
- PCI_AD9 89 AD9
- PCI_AD10 87 AD10
- PCI_AD11 86 AD11
- PCI_AD12 85 AD12
- PCI_AD13 83 AD13
- PCI_AD14 82 AD14
- PCI_AD15 79 AD15
- PCI_AD16 59 AD16
- PCI_AD17 58 AD17
- PCI_AD18 57 AD18
- PCI_AD19 55 AD19
- PCI_AD20 53 AD20
- PCI_AD21 50 AD21
- PCI_AD22 49 AD22
- PCI_AD23 47 AD23
- PCI_AD24 43 AD24
- PCI_AD25 42 AD25
- PCI_AD26 40 AD26
- PCI_AD27 39 AD27
- PCI_AD28 37 AD28
- PCI_AD29 36 AD29
- PCI_AD30 34 AD30
- PCI_AD31 33 AD31

- PCI_C/BE#0 C/BE#0
- PCI_C/BE#1 C/BE#1
- PCI_C/BE#2 C/BE#2
- PCI_C/BE#3 C/BE#3

- LAN_IDSEL 46 IDSEL
- LAN_PAR 76 PAR
- LAN_FRAME# 61 FRAME#
- LAN_IRDY# 63 IRDY#
- LAN_TRDY# 67 TRDY#
- LAN_DEVSEL# 68 DEVSEL#
- LAN_STOP# 69 STOP#
- LAN_PERR# 70 PERR#
- LAN_SERR# 75 SERR#
- LAN_REQ#3 30 REQ#
- LAN_GNT#3 29 GNT#
- LAN_PIRQD# 25 INTA#
- LAN_PME# 31 PME#
- LAN_PCIRST# 27 PCIRST#
- LAN_CLK_PCI_LAN 28 CLK
- LAN_PM_CLKRUN# 65 PM_CLKRUN#

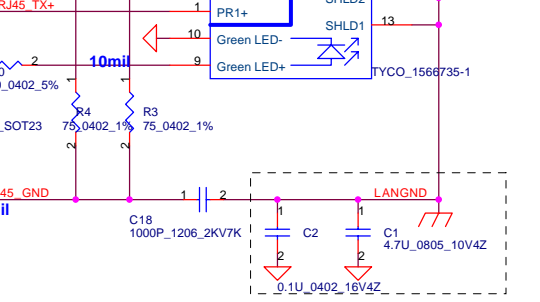
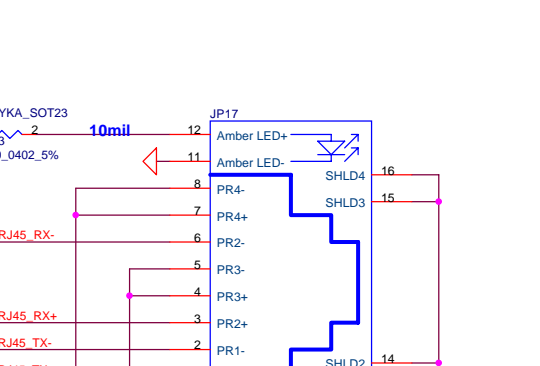
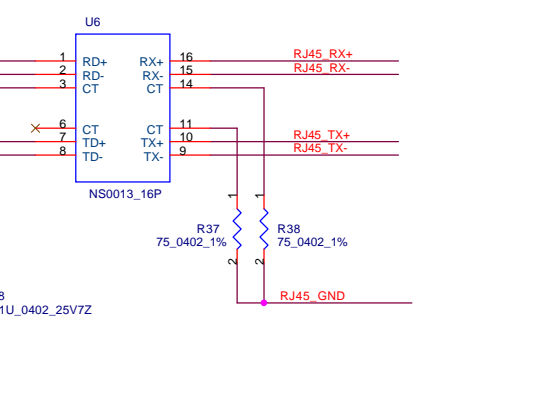
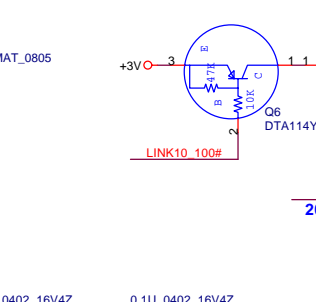
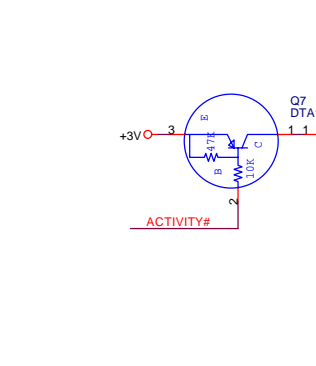
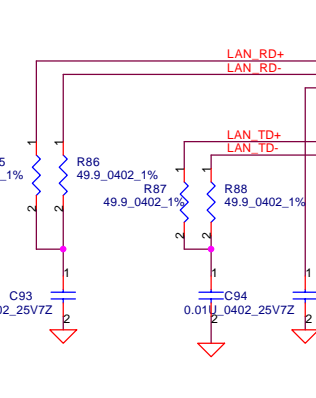
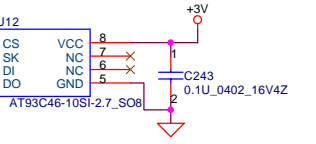
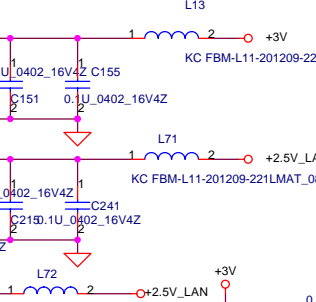
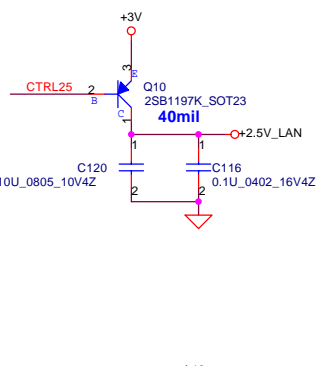
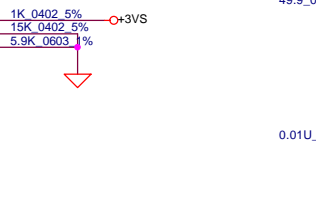
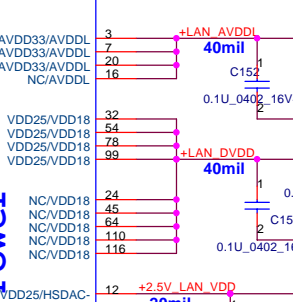
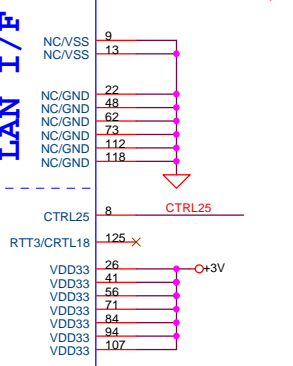
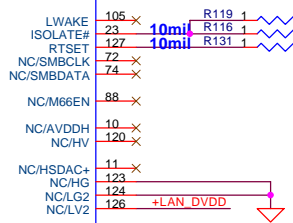
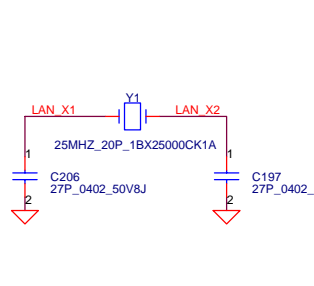
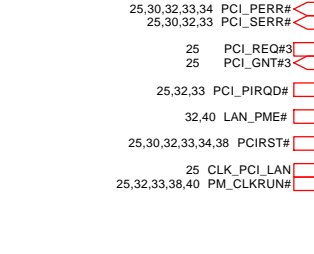
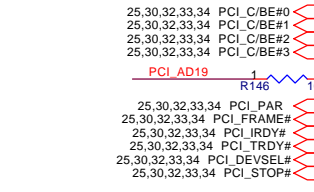
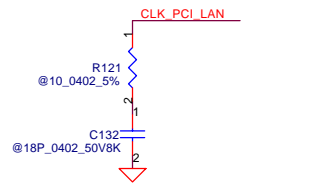
- VDD33 28 VDD33
- VDD33 41 VDD33
- VDD33 56 VDD33
- VDD33 71 VDD33
- VDD33 84 VDD33
- VDD33 94 VDD33
- VDD33 107 VDD33
- GND/VSS 17 GND/VSS
- GND/VSS 128 GND/VSS
- GND/VSSPST 21 GND/VSSPST
- GND/VSSPST 38 GND/VSSPST
- GND/VSSPST 51 GND/VSSPST
- GND/VSSPST 66 GND/VSSPST
- GND/VSSPST 81 GND/VSSPST
- GND/VSSPST 91 GND/VSSPST
- GND/VSSPST 101 GND/VSSPST
- GND/VSSPST 119 GND/VSSPST
- GND 35 GND
- GND 52 GND
- GND 80 GND
- GND 100 GND

- EEDO 108 LAN_EEDO
- AUX/EEDI 109 LAN_EEDI
- EEDI 111 LAN_EECLK
- EESK 106 LAN_EECS
- EESCS 106 LAN_EECS
- LED0 117 ACTIVITY#
- LED1 115 LINK10_100#
- LED2 114
- LED3 113
- NC/LED3 113
- TXD+/MDI0+ 1 LAN_TD+
- TXD-/MDI0- 2 LAN_TD-
- RXIN+/MDI1+ 5 LAN_RD+
- RXIN-/MDI1- 6 LAN_RD-
- NC/MDI2+ 14
- NC/MDI2- 15
- NC/MDI3+ 18
- NC/MDI3- 19
- X1 121 LAN_X1
- X2 122 LAN_X2
- LWAKE 105
- ISOLATE# 23
- RTSET 127
- NC/SMBCLK 74
- NC/SMBDATA 74
- NC/M66EN 88
- NC/AVDDH 10
- NC/HV 120
- NC/HSDAC+ 11
- NC/HG 123
- NC/LG2 124
- NC/LV2 126
- NC/VSS 9
- NC/VSS 13
- NC/GND 22
- NC/GND 48
- NC/GND 62
- NC/GND 73
- NC/GND 112
- NC/GND 118
- CTRL25 8
- RTT3/CRTL18 125
- VDD33 26
- VDD33 41
- VDD33 56
- VDD33 71
- VDD33 84
- VDD33 94
- VDD33 107
- AVDD33/AVDDL 3
- AVDD33/AVDDL 7
- AVDD33/AVDDL 20
- AVDD33/AVDDL 16
- VDD25/VDD18 32
- VDD25/VDD18 54
- VDD25/VDD18 78
- VDD25/VDD18 99
- NC/VDD18 24
- NC/VDD18 45
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- NC/VDD18 110
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- AVDD25/HSDAC- 12

PCI I/F

LAN I/F

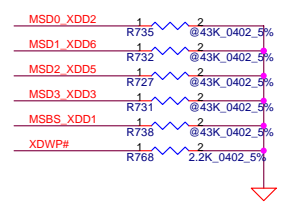
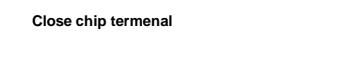
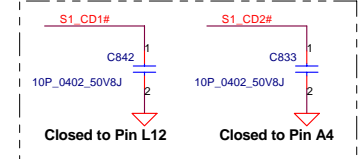
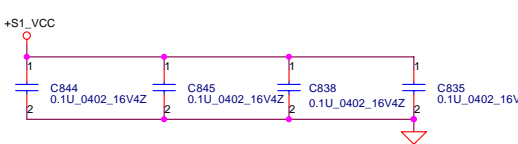
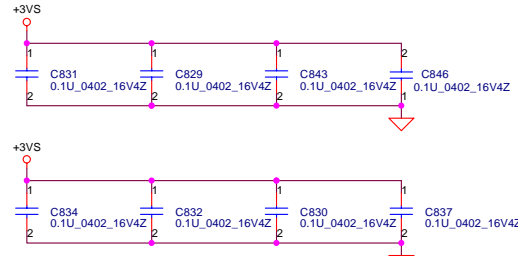
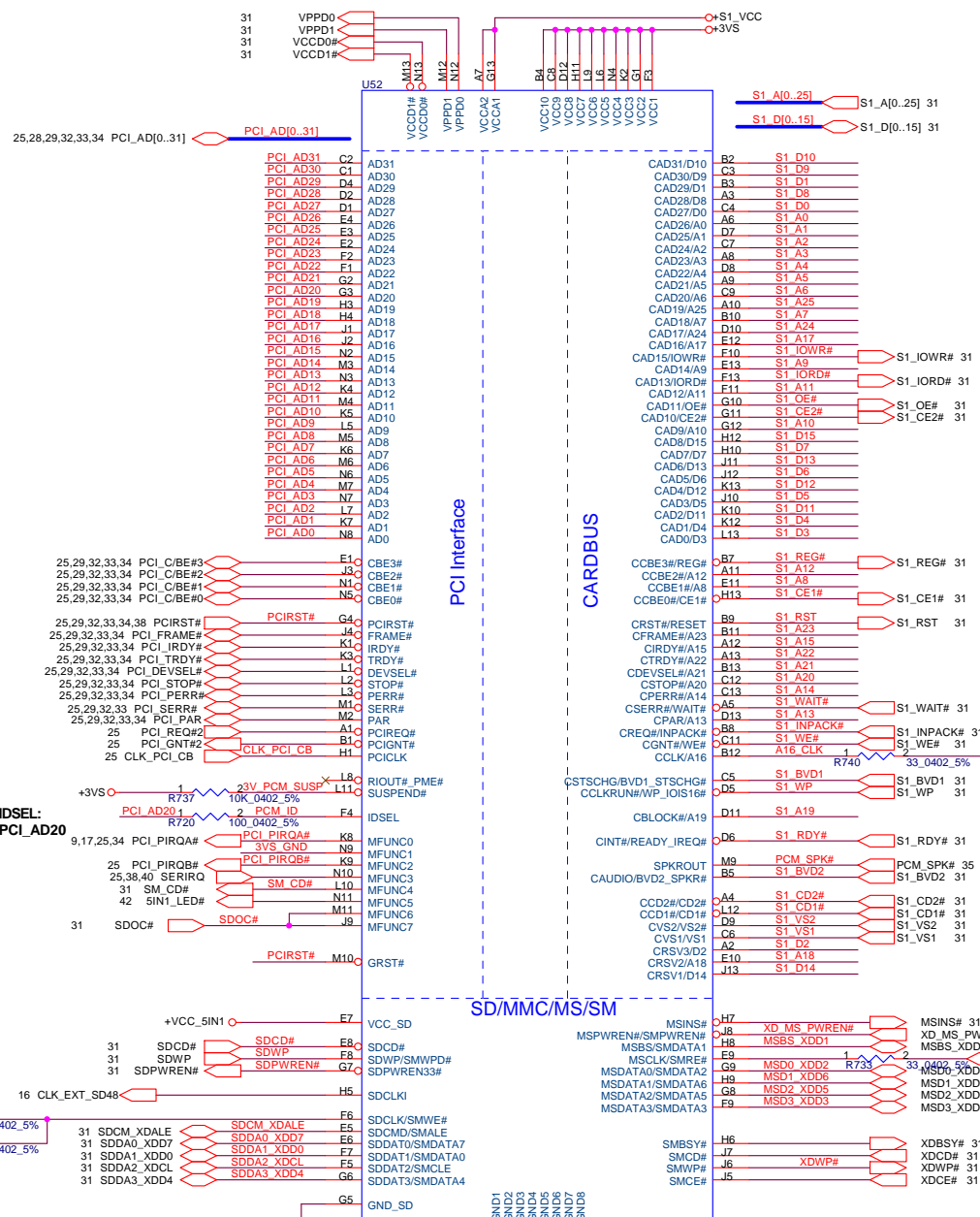
Power



Termination plane should be closed to chassis ground and also depends on safety concern

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Title LAN REALTEK RTL8100CL		
Size	Document Number LA-2371	Rev 1.0
Date:	星期三, 七月 28, 2004	Sheet 29 of 56



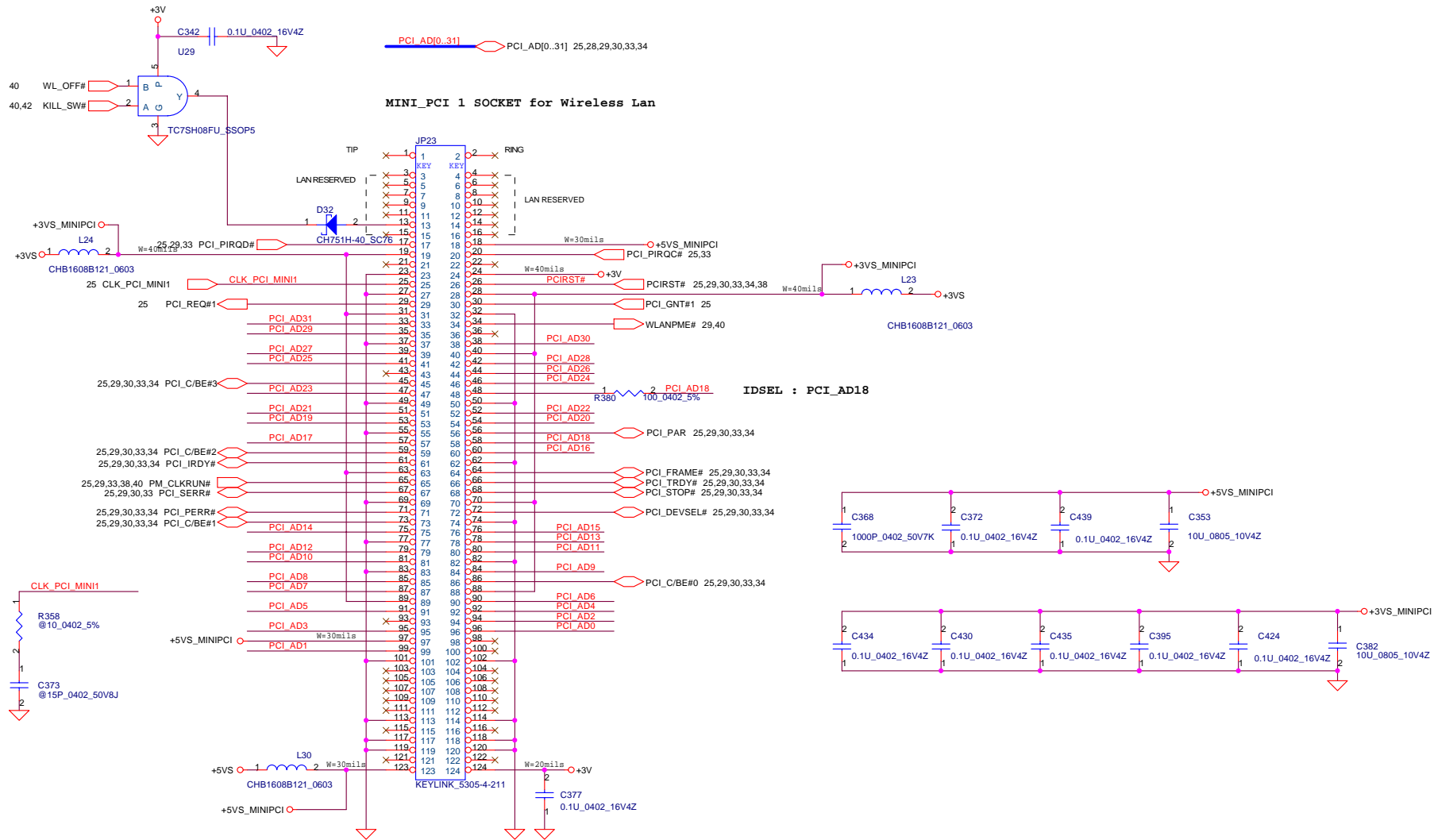
Compal Electronics, Inc.

PCMCIA Controller ENE CB714

Size: Custom Document Number: **LA-2371** Rev: 1.0

Date: 星期四, 七月 29, 2004 Sheet: 30 of 56

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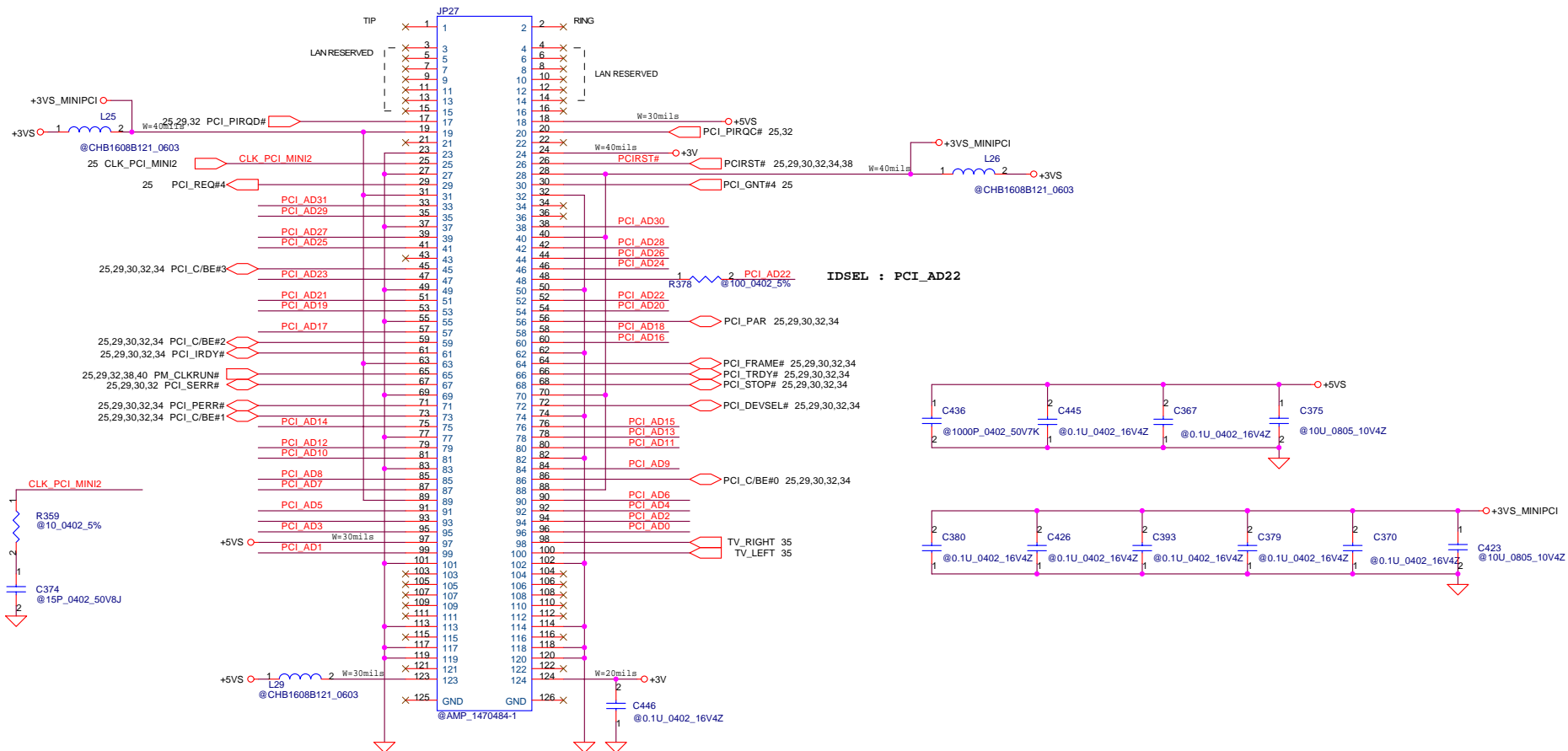


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Compal Electronics, Inc.			
Title: MINI_PCI			
Size: LA-2371	Document Number: LA-2371	Rev: 1.0	
Date: 星期三, 七月 28, 2004	Sheet: 32	of	56

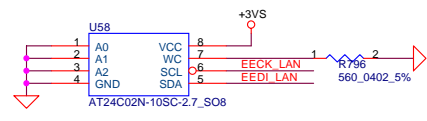
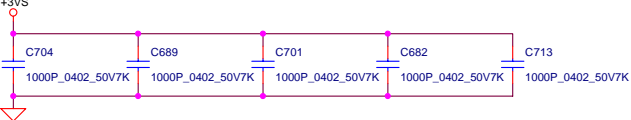
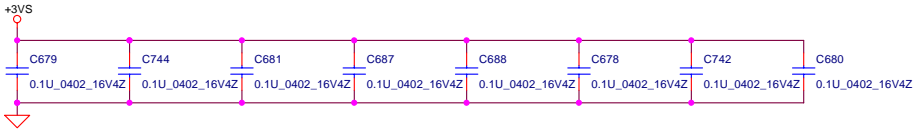
PCI_AD[0..31] PCI_AD[0..31] 25,28,29,30,32,34

MINI_PCI 2 SOCKET for TV turner



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Compal Electronics, Inc.			
Title MINI_PCI (TV TURNER)			
Size	Document Number	Rev	
Custor	LA-2371	1.0	
Date:	星期三, 七月 28, 2004	Sheet	33 of 56



25,28,29,30,32,33 PCI_AD[0..31]

PCI_AD0	25	AD0
PCI_AD1	24	AD1
PCI_AD2	20	AD2
PCI_AD3	19	AD3
PCI_AD4	18	AD4
PCI_AD5	16	AD5
PCI_AD6	15	AD6
PCI_AD7	14	AD7
PCI_AD8	11	AD8
PCI_AD9	10	AD9
PCI_AD10	9	AD10
PCI_AD11	8	AD11
PCI_AD12	7	AD12
PCI_AD13	4	AD13
PCI_AD14	3	AD14
PCI_AD15	2	AD15
PCI_AD16	117	AD16
PCI_AD17	116	AD17
PCI_AD18	115	AD18
PCI_AD19	114	AD19
PCI_AD20	113	AD20
PCI_AD21	109	AD21
PCI_AD22	107	AD22
PCI_AD23	106	AD23
PCI_AD24	103	AD24
PCI_AD25	102	AD25
PCI_AD26	101	AD26
PCI_AD27	98	AD27
PCI_AD28	97	AD28
PCI_AD29	96	AD29
PCI_AD30	95	AD30
PCI_AD31	94	AD31

IDSEL:PCI_AD16

25,29,30,32,33	PCI_C/BE#0	12	CBE0#
25,29,30,32,33	PCI_C/BE#1	1	CBE1#
25,29,30,32,33	PCI_C/BE#2	119	CBE2#
25,29,30,32,33	PCI_C/BE#3	104	CBE3#
25,29,30,32,33	PCI_FRAME#	120	IDSEL FRAME#
25,29,30,32,33	PCI_IRDY#	121	IRDY#
25,29,30,32,33	PCI_TRDY#	123	TRDY#
25,29,30,32,33	PCI_DEVSEL#	124	DEVSEL#
25,29,30,32,33	PCI_STOP#	125	STOP#
25,29,30,32,33	PCI_PERR#	127	PERR#
25,29,30,32,33	PCI_PAR	128	PAR
25	PCI_REQ#0	93	REQ#
25	PCI_GNT#0	92	GNT#
9,17,25,30	PCI_PIRQA#	88	INTA#
25,29,30,32,33,38	PCIRST#	89	PCIRST#
25	CLK_PCI_1394	30	PCICLK

Power

IEEE 1394

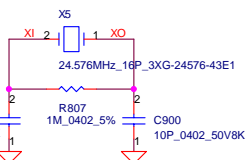
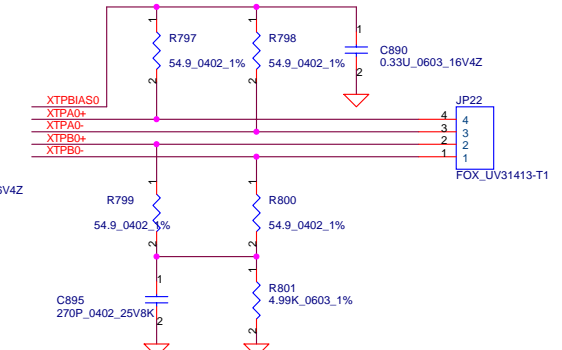
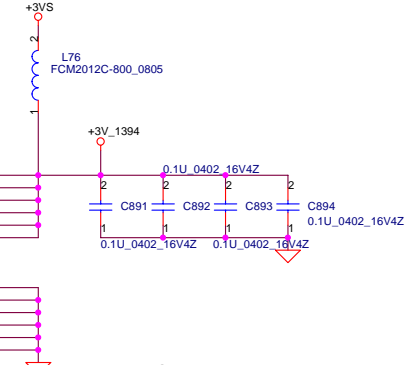
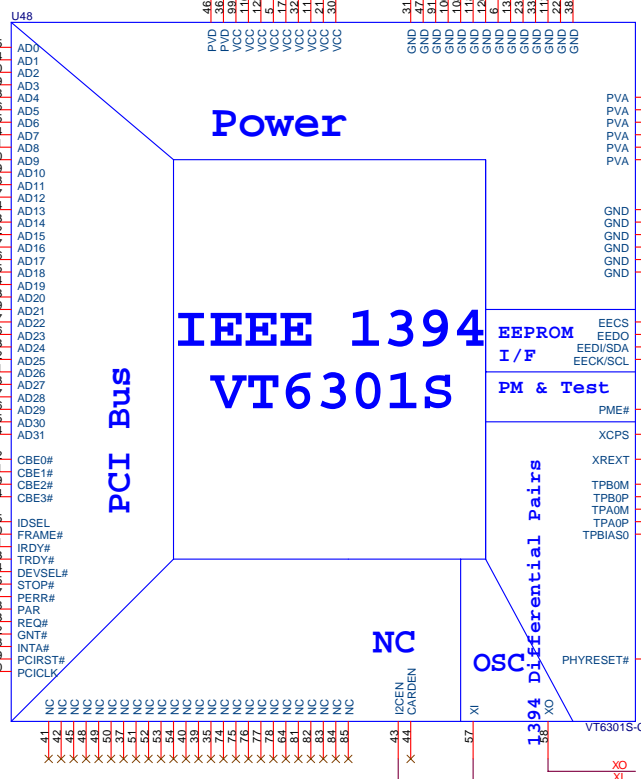
VT6301S

PCI Bus

NC

1394 Differential Pairs

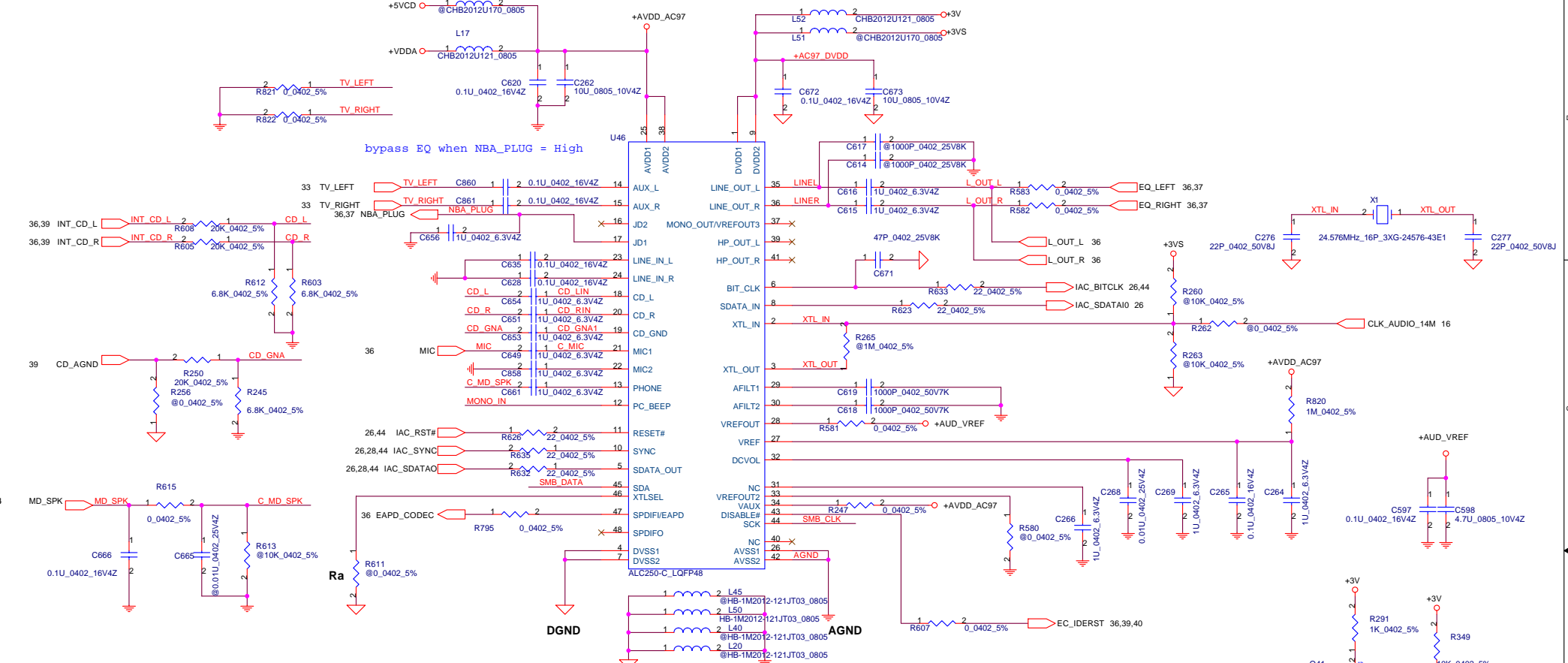
OSC



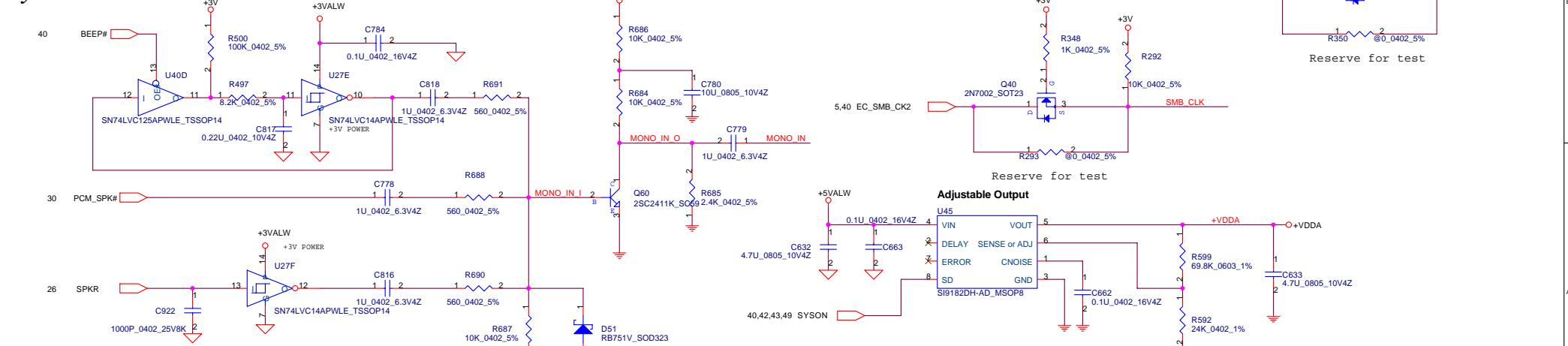
Compal Electronics, Inc.	
Title	1394 Interface
Size	Document Number
Customer	LA-2371
Date	星期三, 七月 28, 2004
Sheet	34 of 56
Rev	1.0

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AC97 Codec



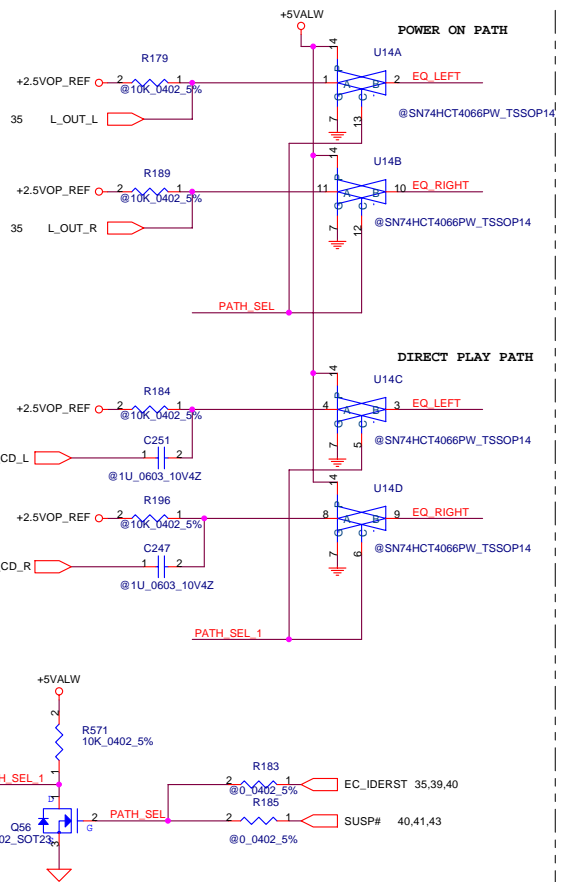
System Sound



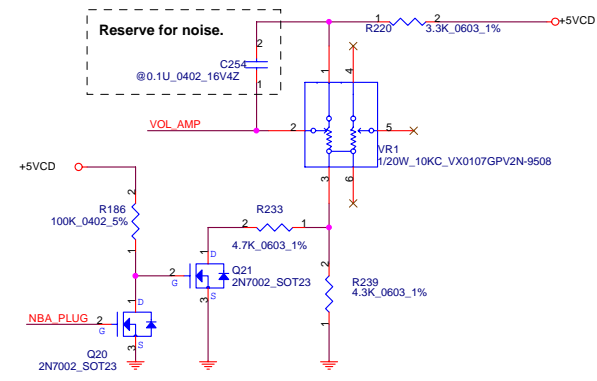
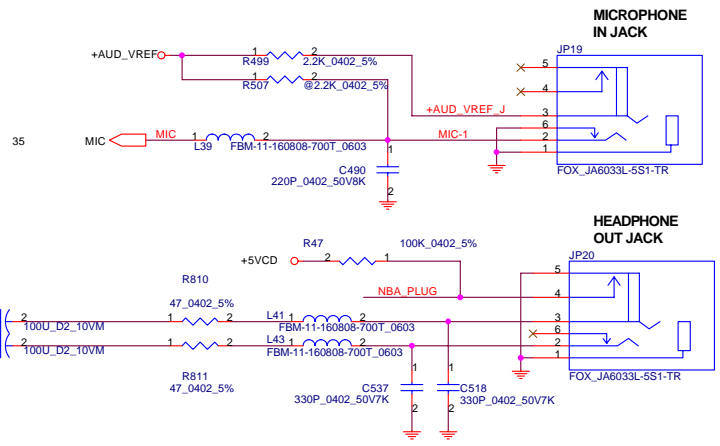
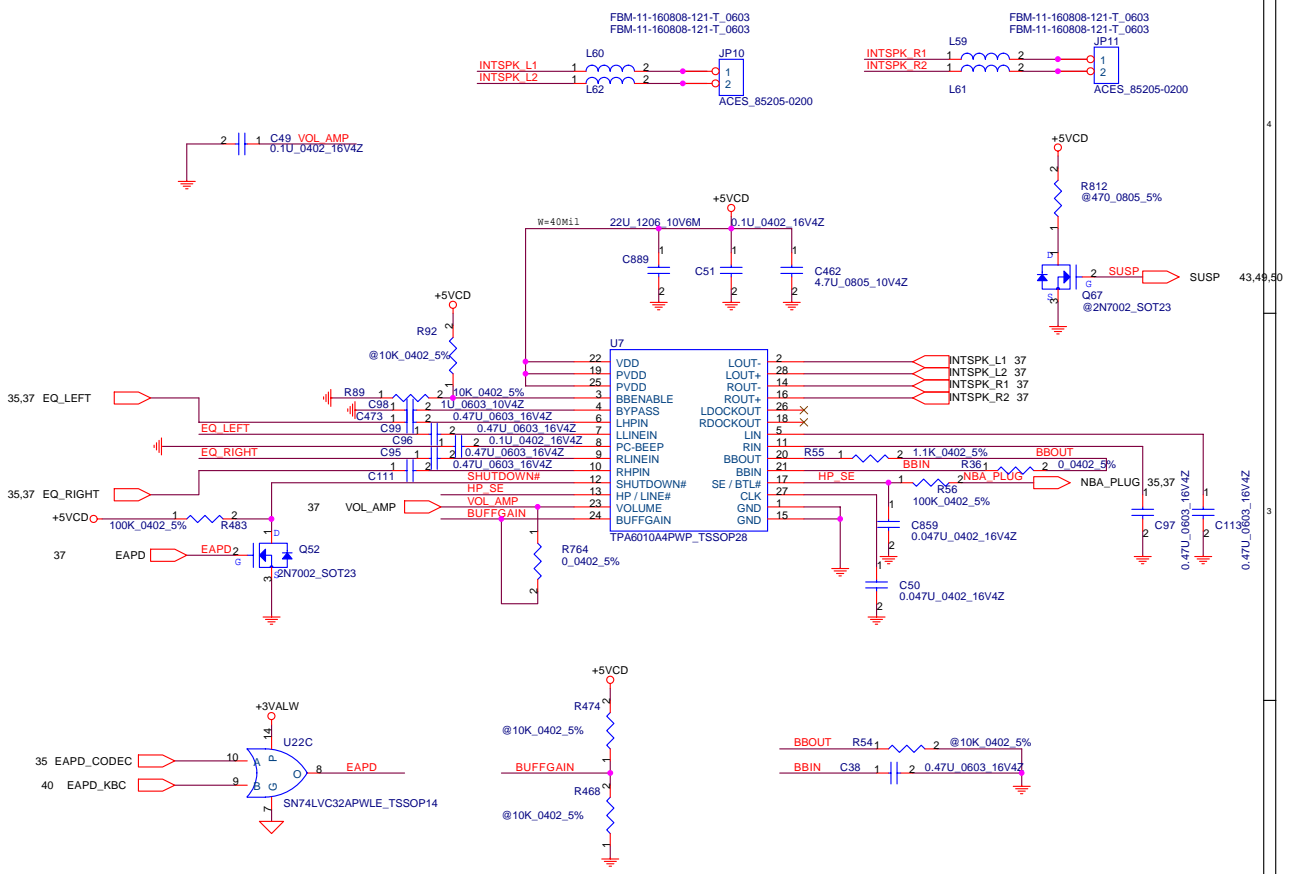
Compal Electronics, Inc.		
AC97 Codec ALC250		
Title	Document Number	Rev
LA-2371	LA-2371	1.0
Date: 星期三, 七月 28, 2004	Sheet 35 of 56	

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Direct CD CTL



Audio AMP



VR - C-Type

R220	3.3K	Bias (Gain)	SPK 22dB
R233	4.7K		
R239	4.3K		HP -4dB

Compal Electronics, Inc.

Audio AMP & JACK

Title: **Audio AMP & JACK**

Size: **LA-2371**

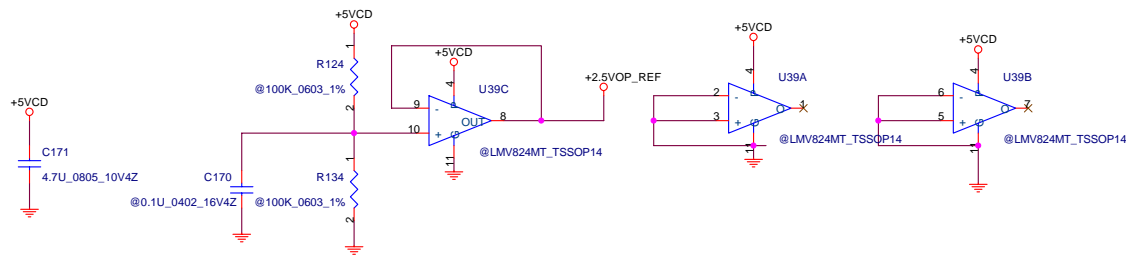
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Date: **星期三, 七月 28, 2004**

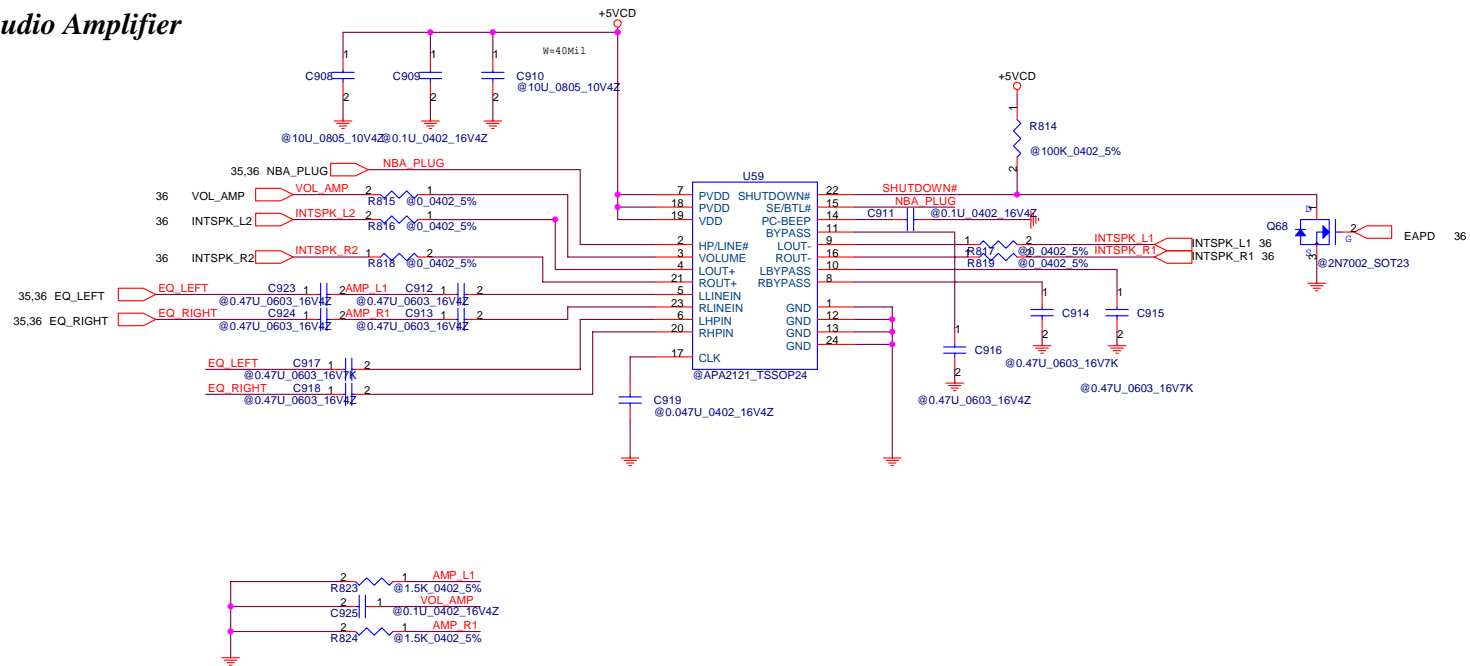
Sheet: **36** of **56**

Rev: **1.0**

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Audio Amplifier

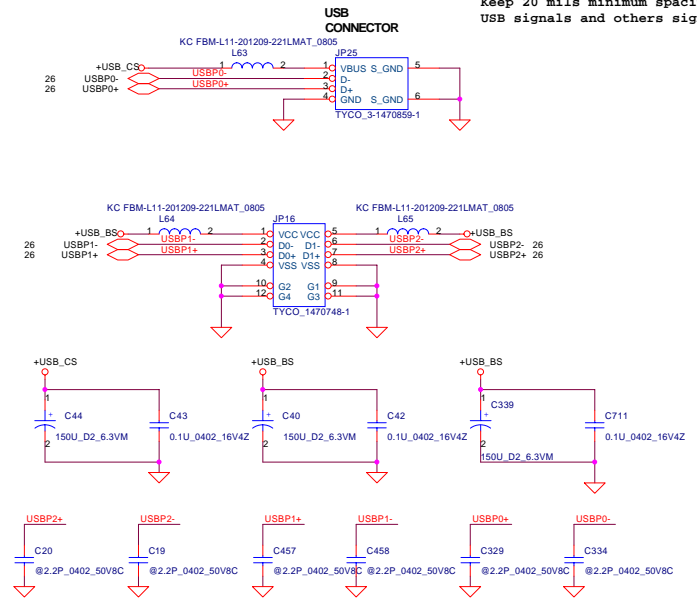
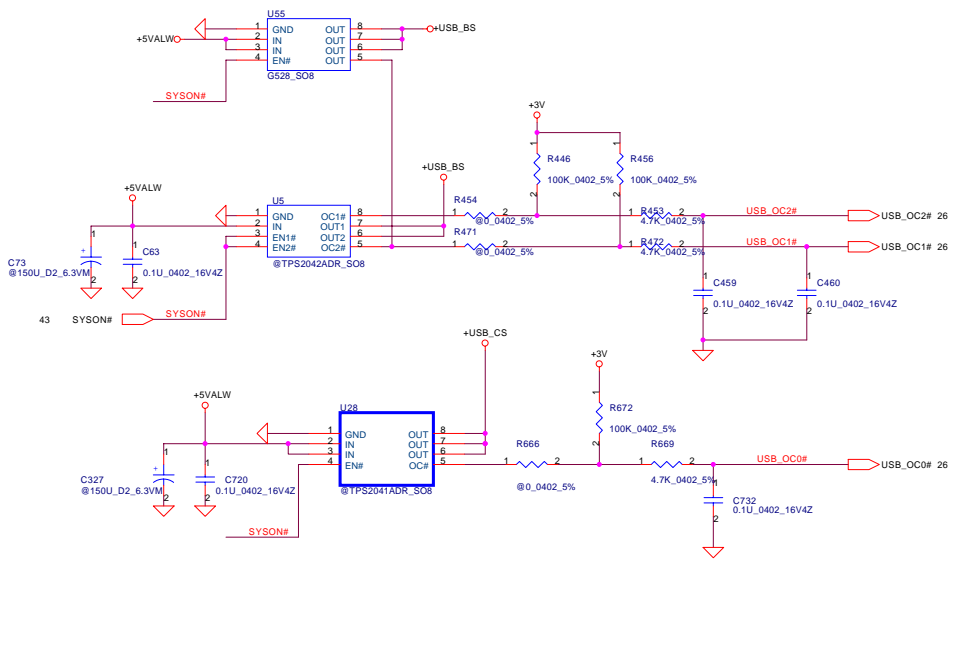


Compal Electronics, Inc.

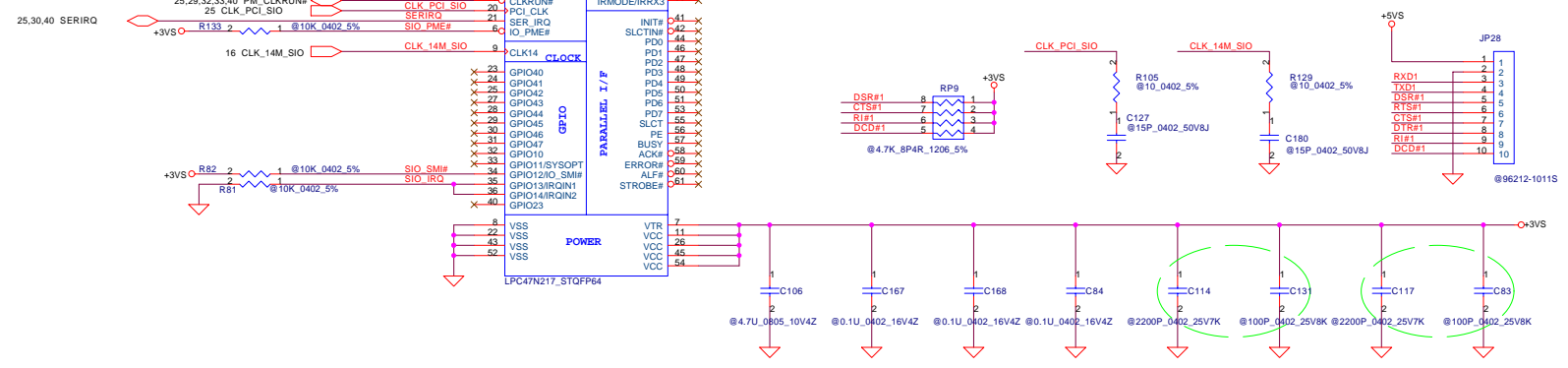
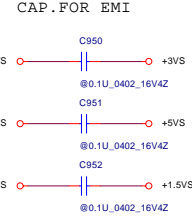
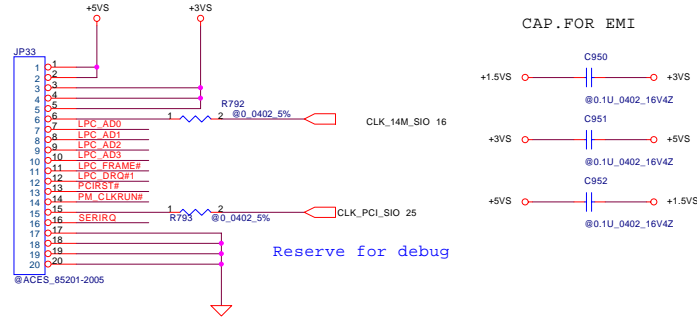
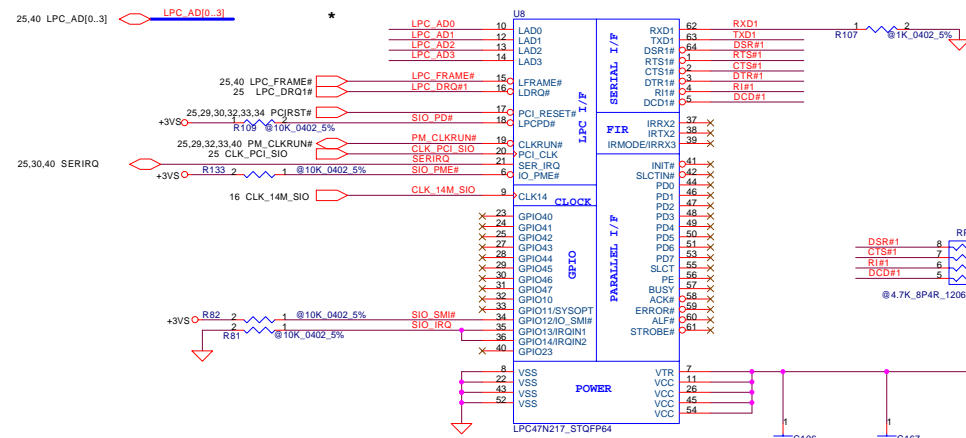
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Size	Document Number	Rev
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Date	星期三, 七月 28, 2004	Sheet 37 of 56

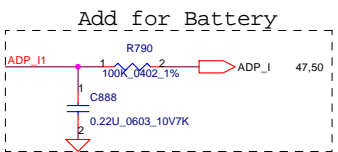
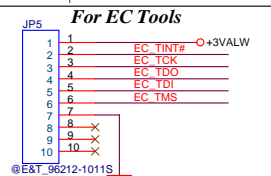
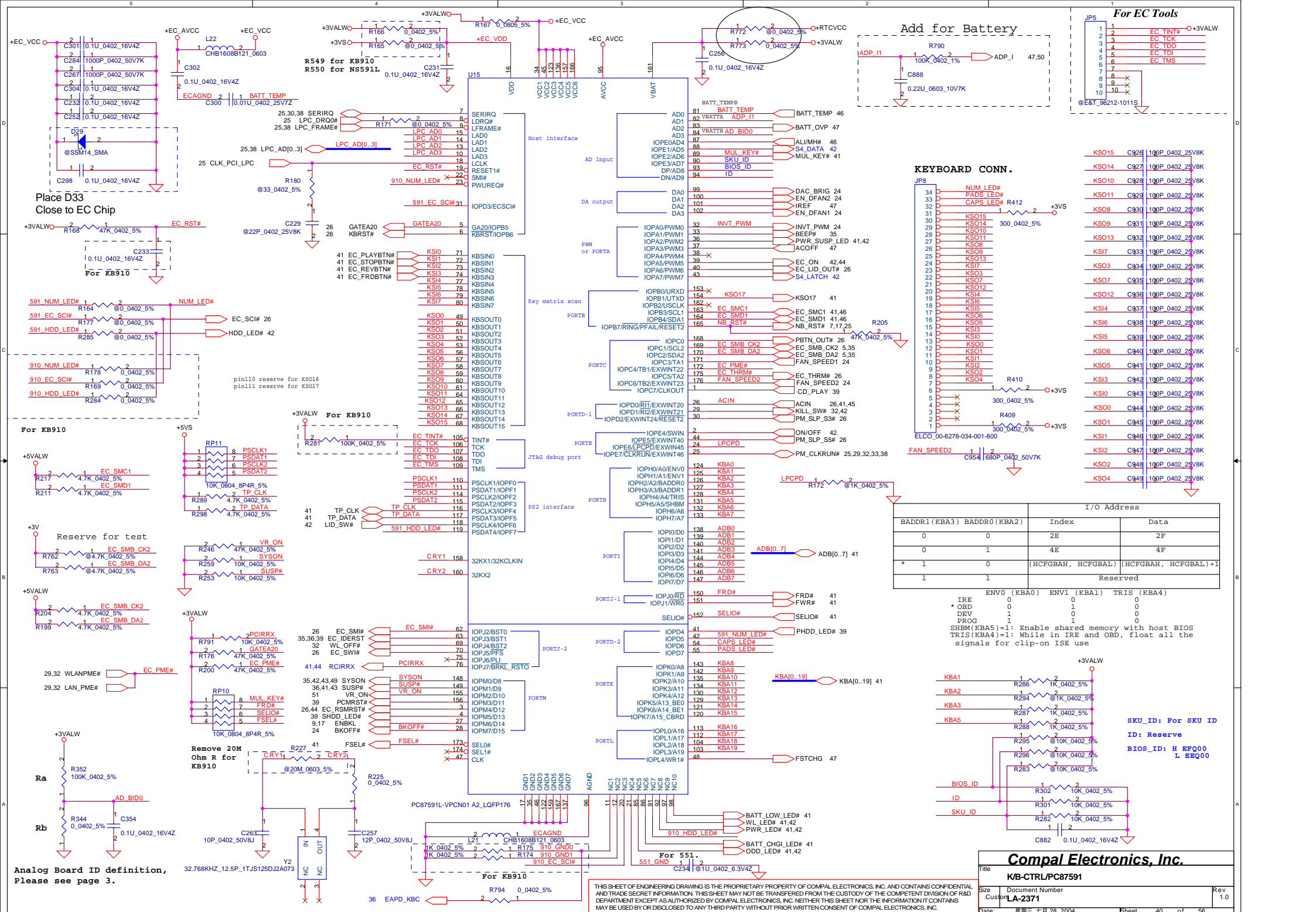
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USB CONNECTOR
 Keep 20 mils minimum spacing between USB signals and others signals

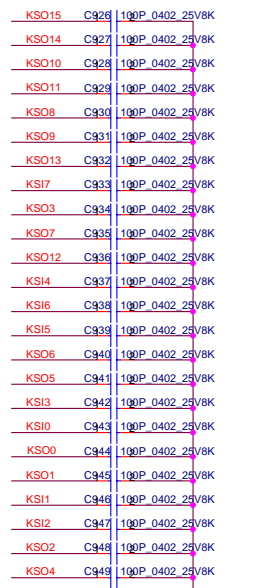
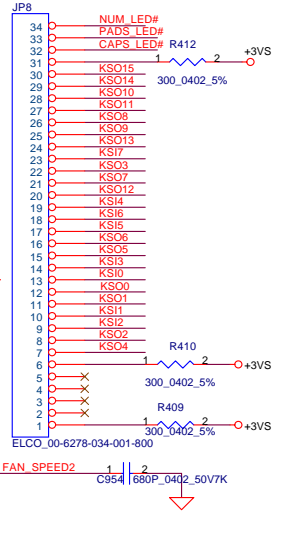


SUPER I/O SMC FDC47N217

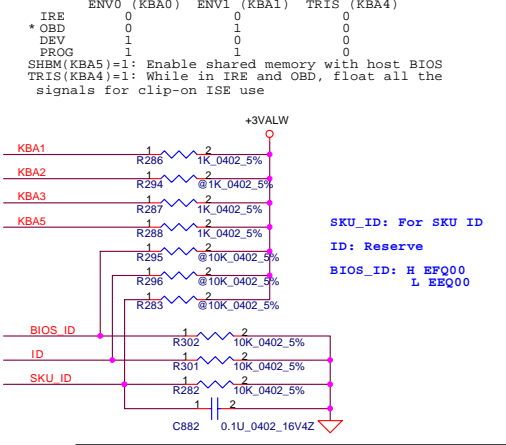




KEYBOARD CONN.



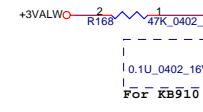
I/O Address			
BADDR1 (KBA3)	BADDR0 (KBA2)	Index	Data
0	0	2E	2F
0	1	4E	4F
*	1	0	(HCFGBAH, HCFGBAL) (HCFGBAH, HCFGBAL)+1
1	1	0	Reserved



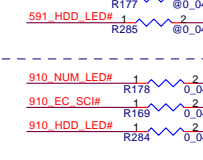
Compal Electronics, Inc.
K/B-CTRL/PC87591

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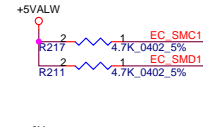
Place D33 Close to EC Chip



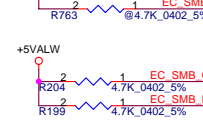
For KB910



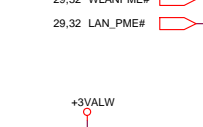
For KB910



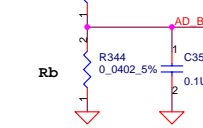
Reserve for test



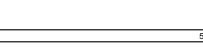
Remove 20M Ohm R for KB910

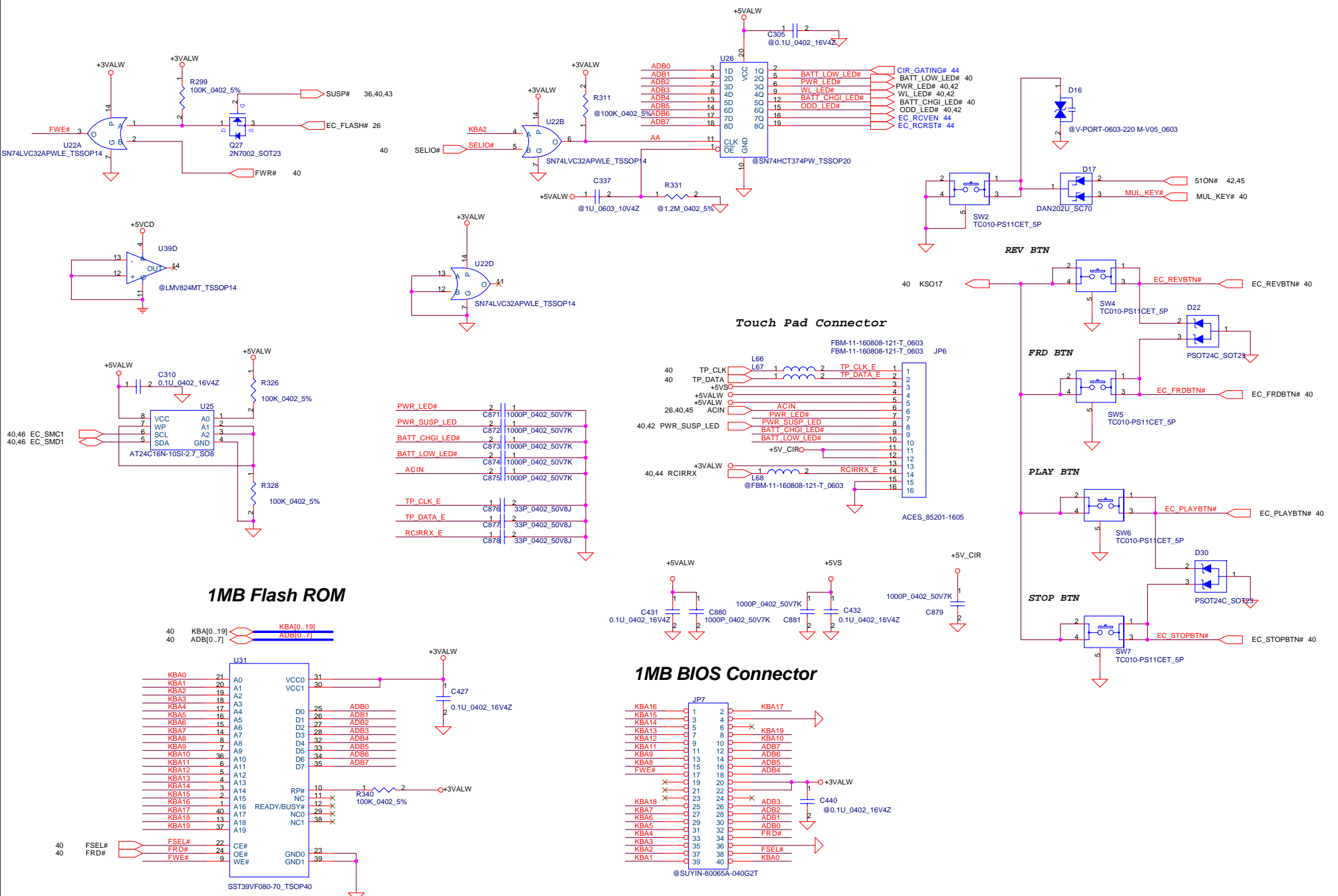


Analog Board ID definition, Please see page 3.



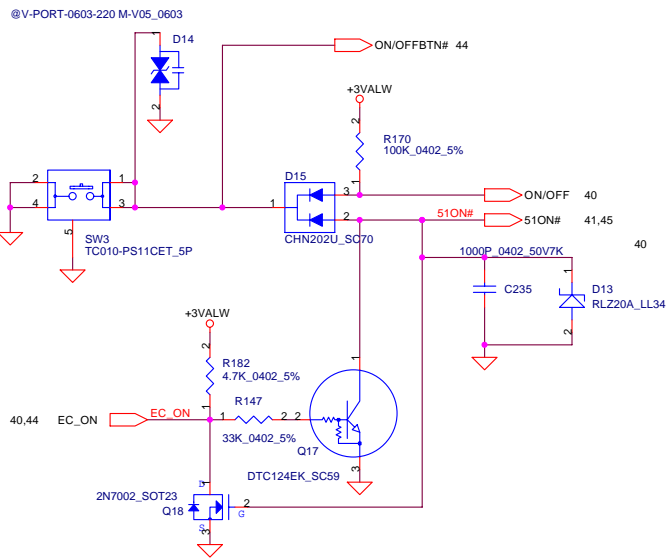
For 551.



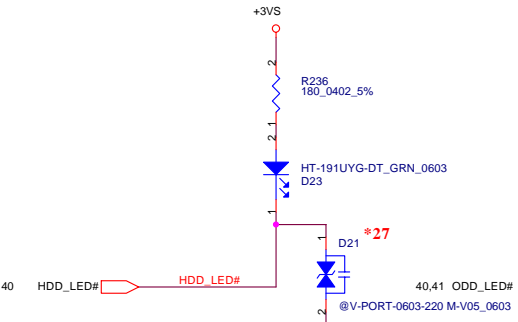


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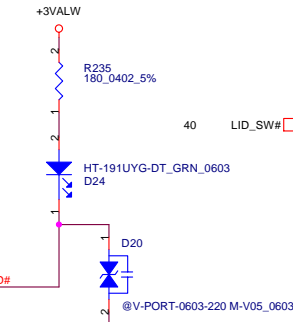
Power Button



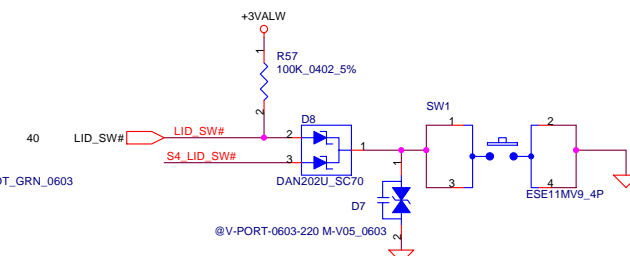
HDD LED



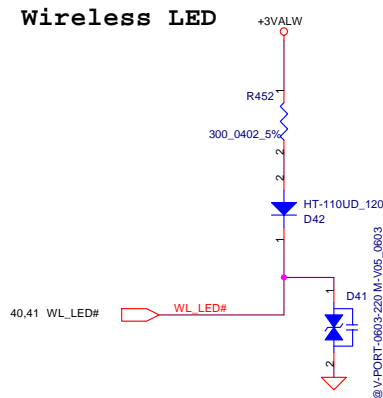
ODD LED



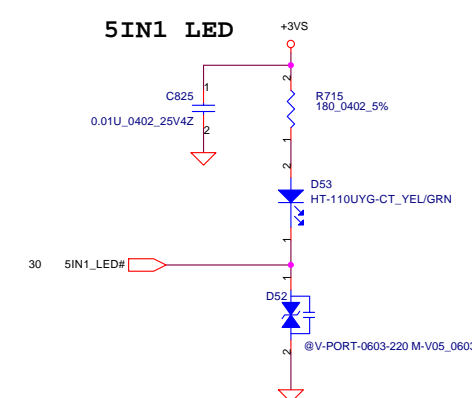
LID Switch



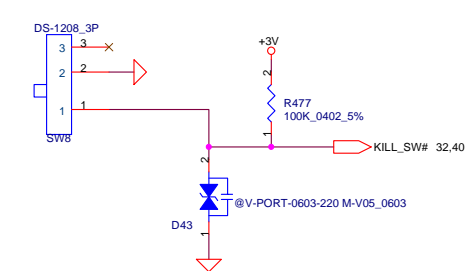
Wireless LED



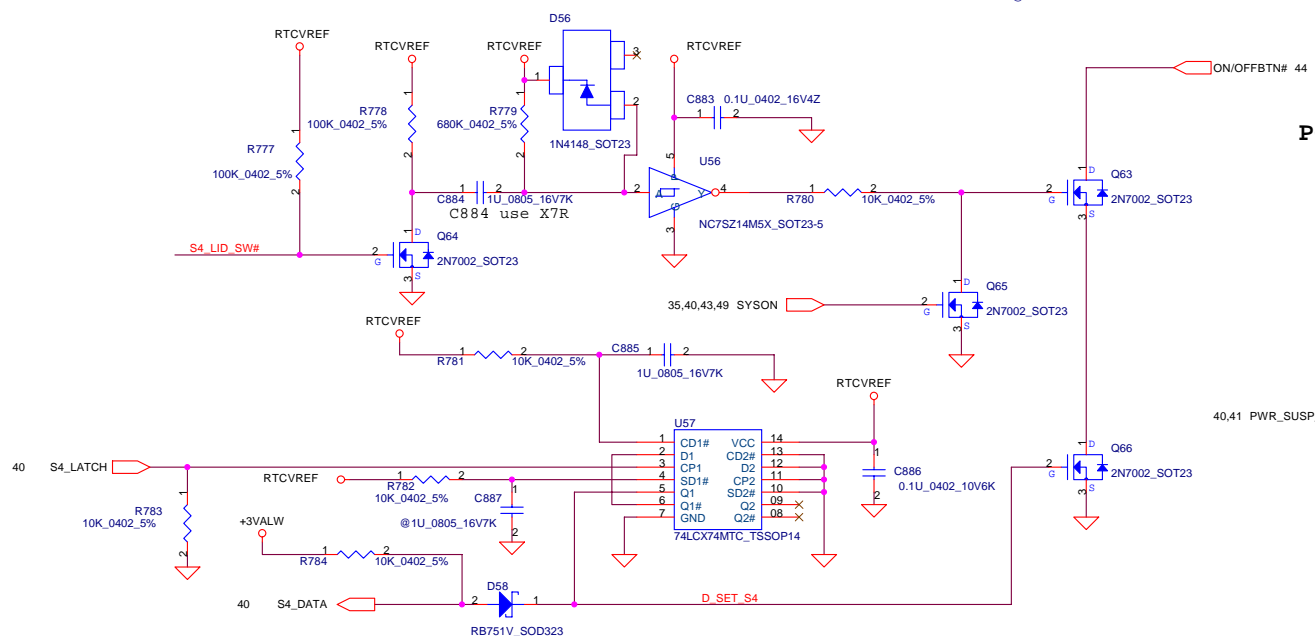
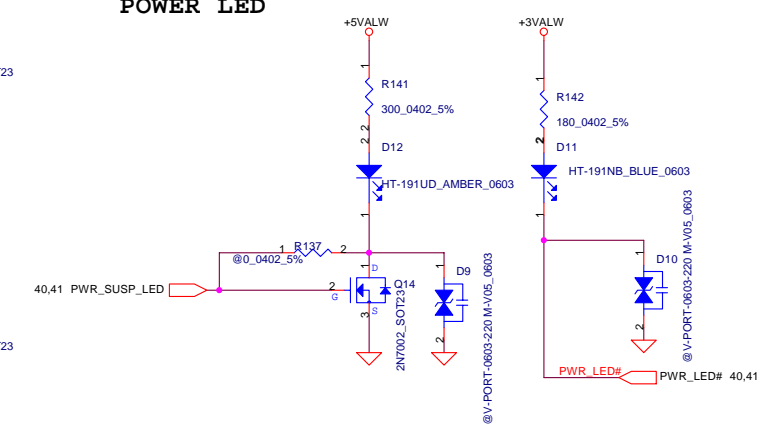
5IN1 LED



Kill SWITCH



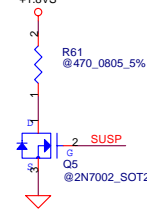
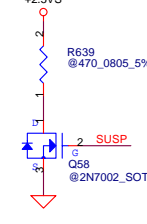
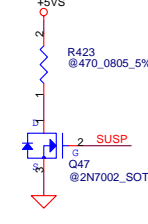
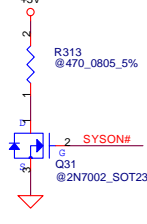
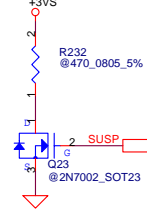
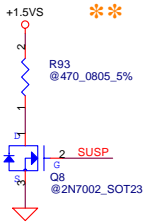
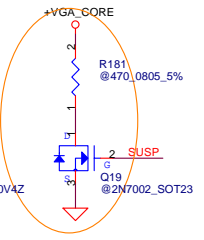
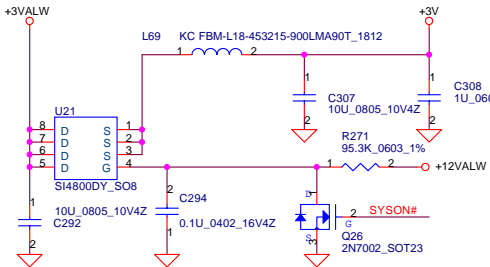
POWER LED



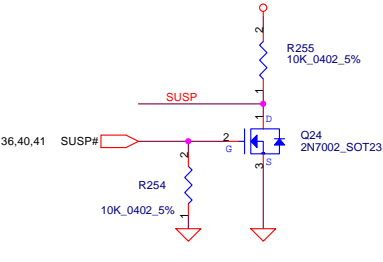
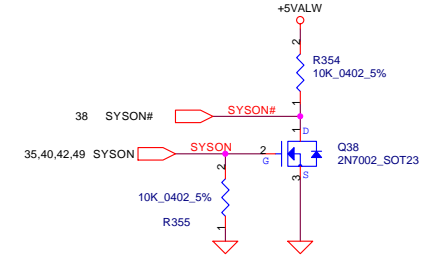
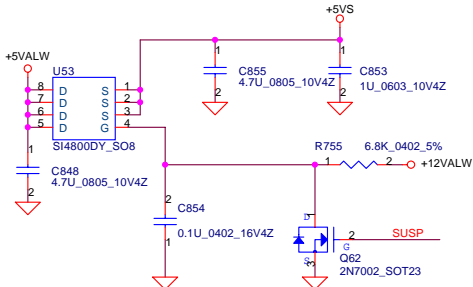
Compal Electronics, Inc.			
Switches & Connectors			
Title	Document Number	Rev 1.0	
Size	LA-2371		
Date	星期三, 七月 28, 2004	Sheet	42 of 56

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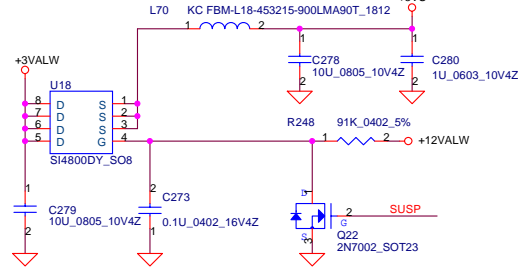
+3VALW TO +3V



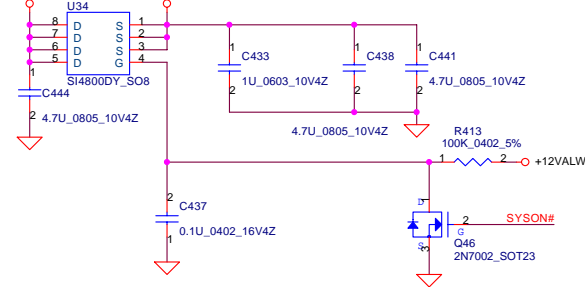
+5VALW TO +5VS



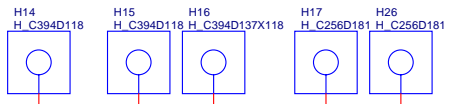
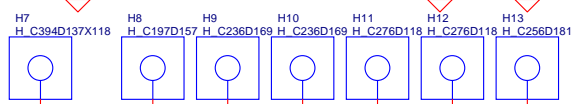
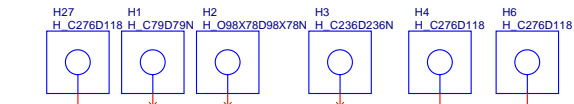
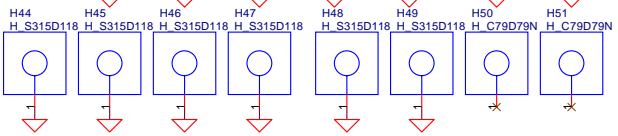
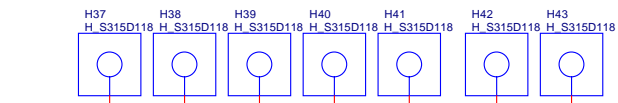
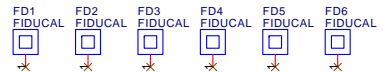
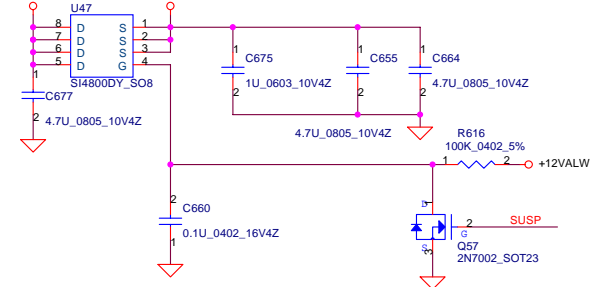
+3VALW TO +3VS



+2.5VALW TO +2.5V

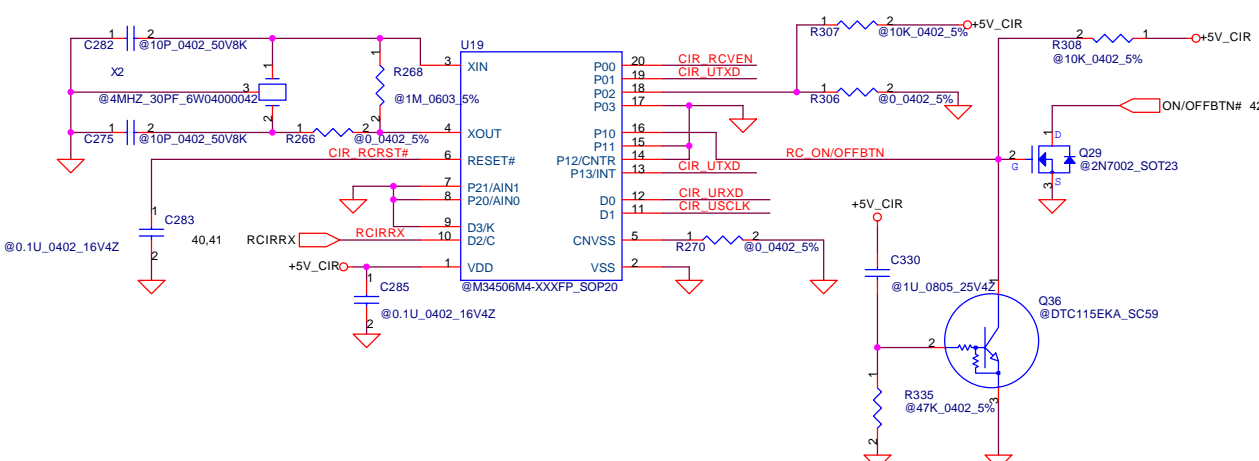
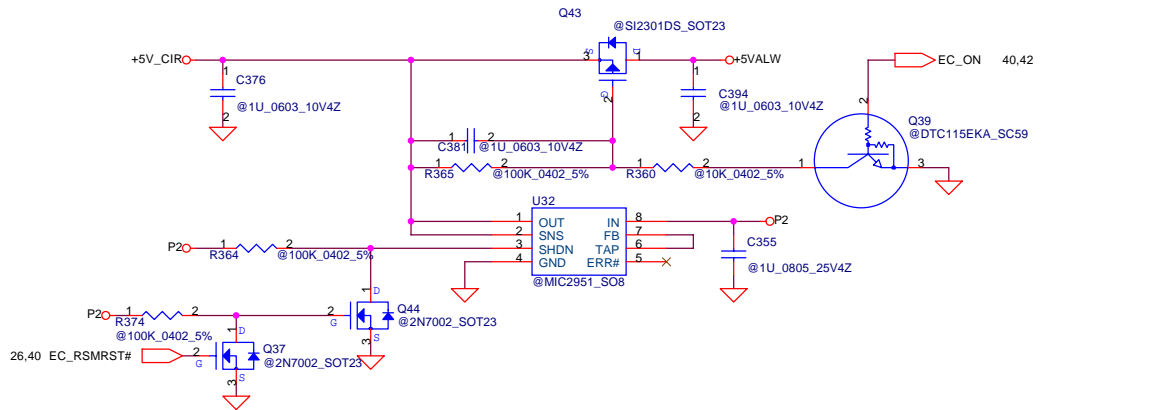
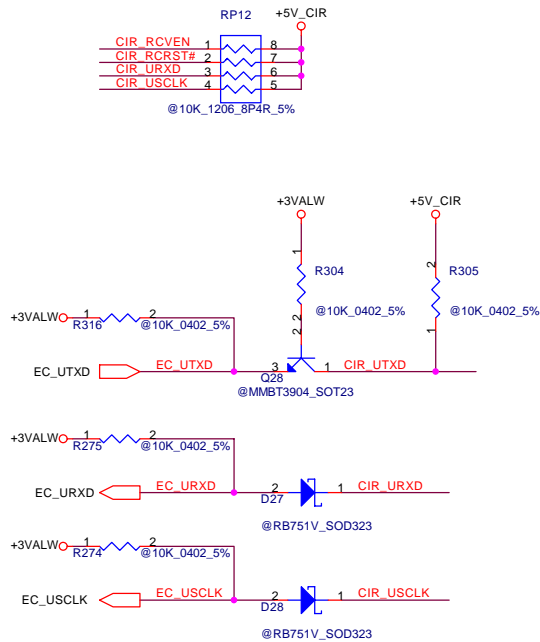


+2.5V TO +2.5VS

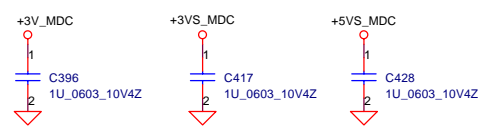
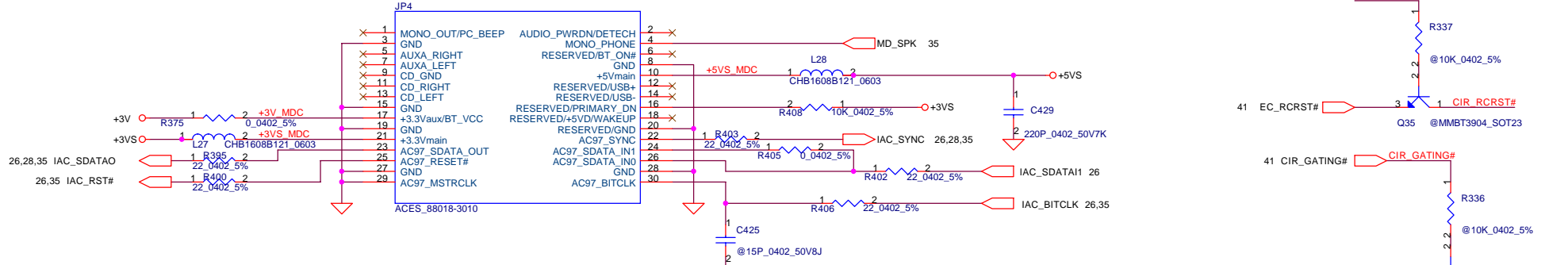


Compal Electronics, Inc.		
Title POWER CONTROL CKT		
Size	Document Number	Rev
Customer	LA-2371	1.0
Date	星期三, 七月 28, 2004	Sheet 43 of 56

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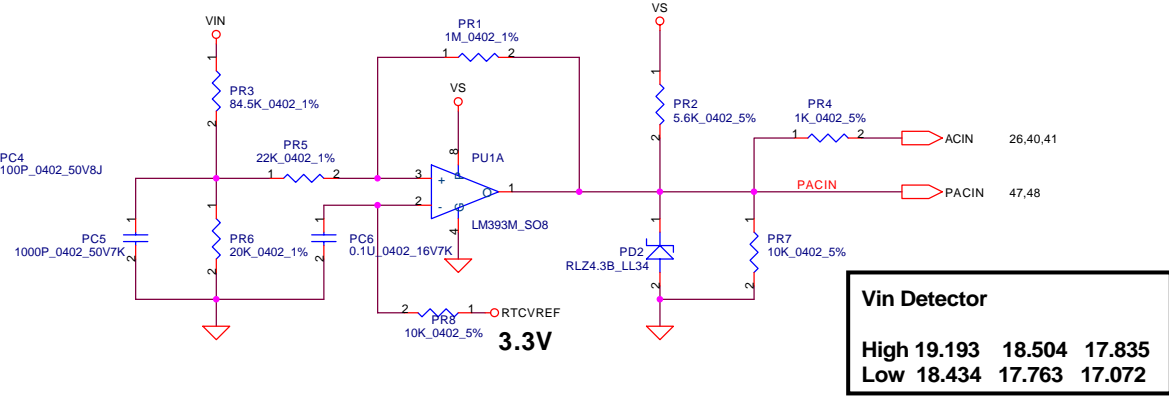
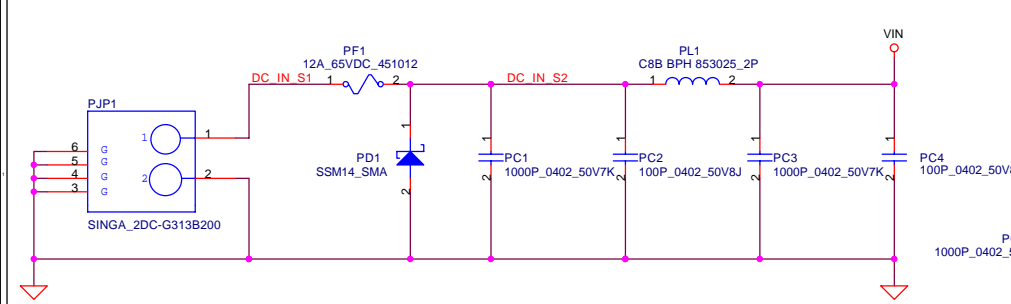


MDC CONN.

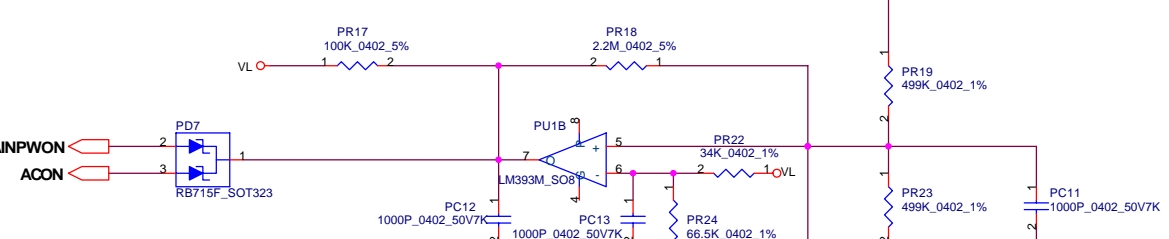
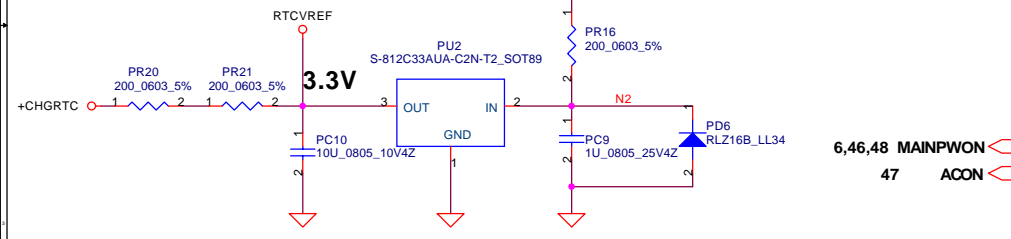
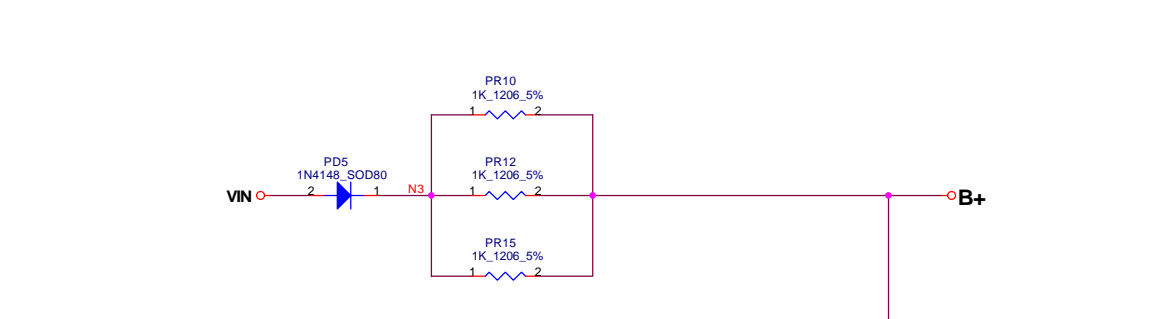
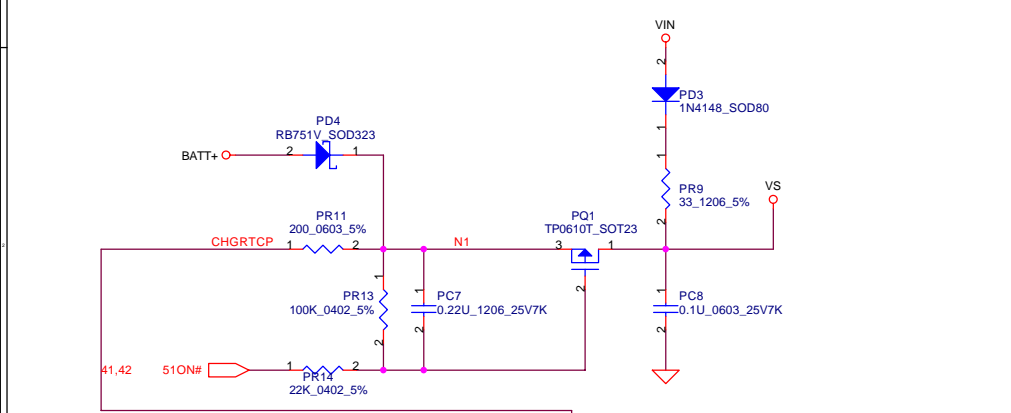


Compal Electronics, Inc.		
Title	CIR & MDC	
Size	Document Number	Rev
B	LA-2371	1.0
Date:	星期三, 七月 28, 2004	Sheet 44 of 56

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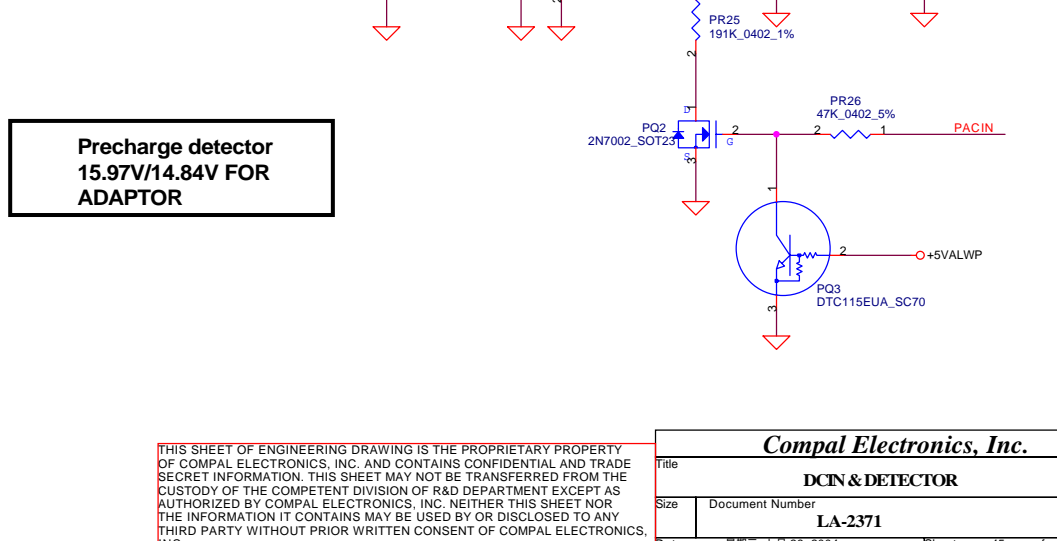
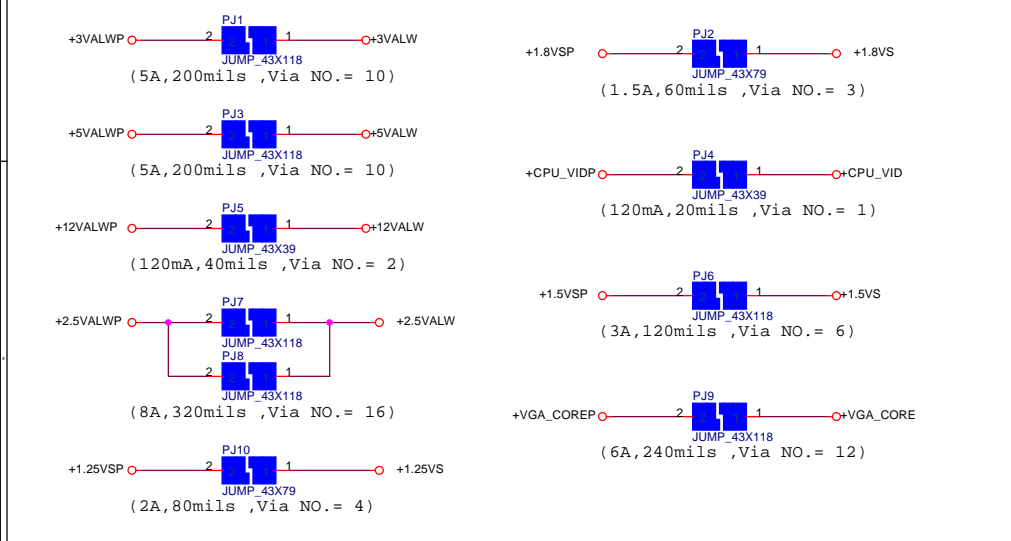


Vin Detector
High 19.193 18.504 17.835
Low 18.434 17.763 17.072



6,46,48 MAINPWON
47 ACIN

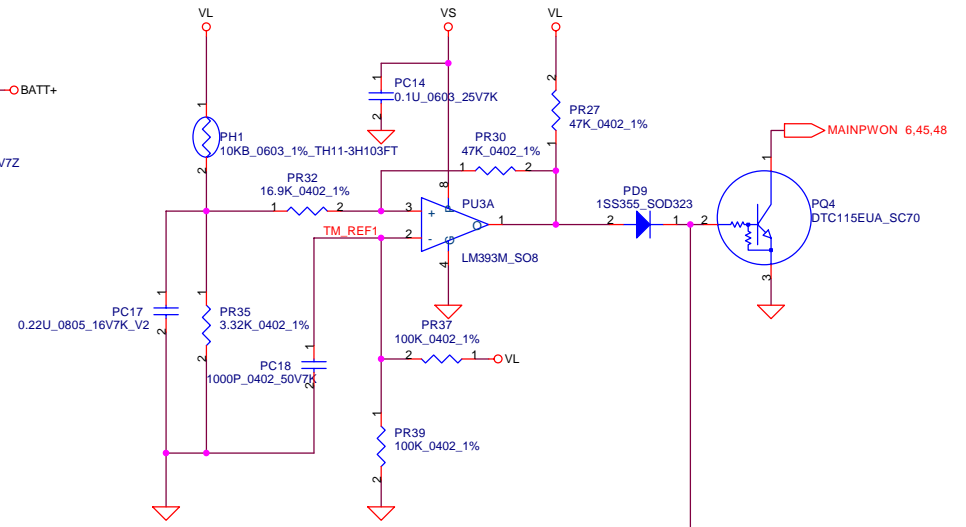
Precharge detector
15.97V/14.84V FOR
ADAPTOR



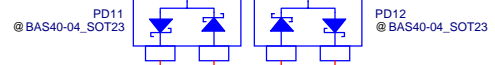
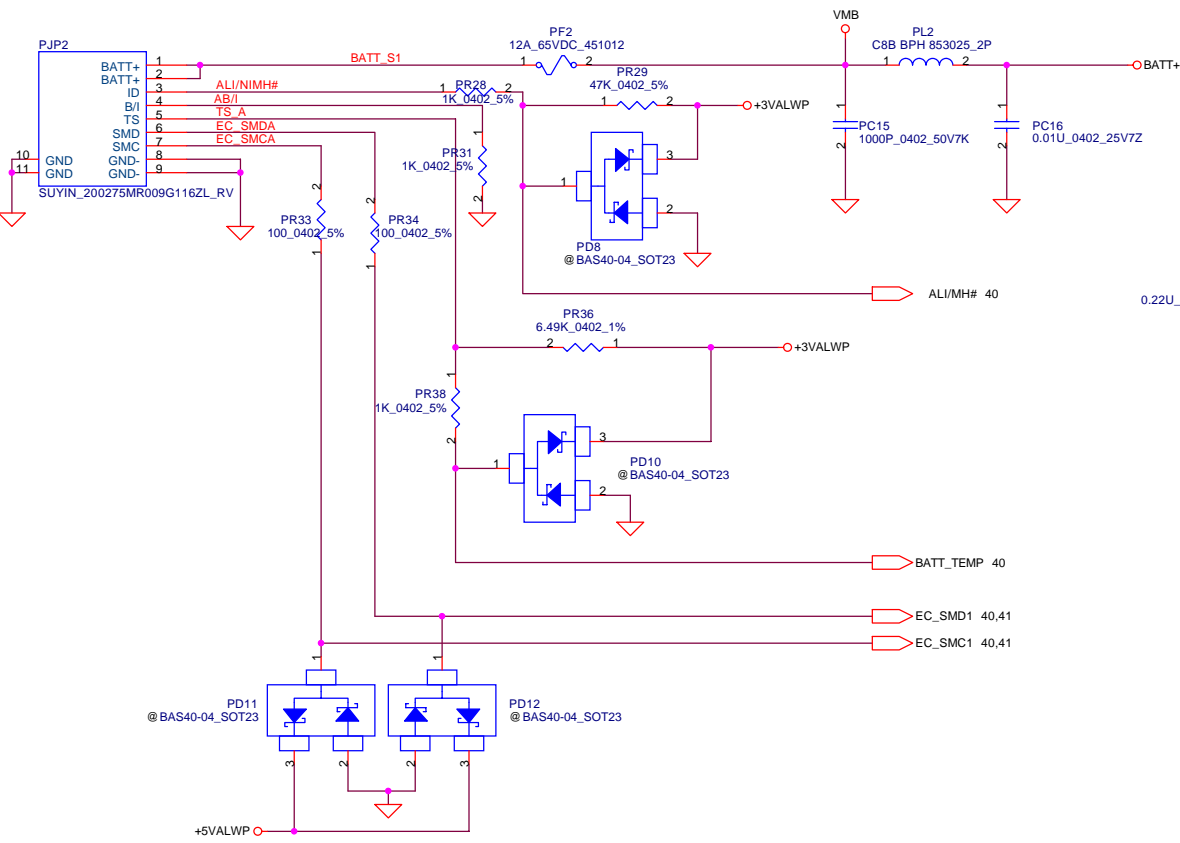
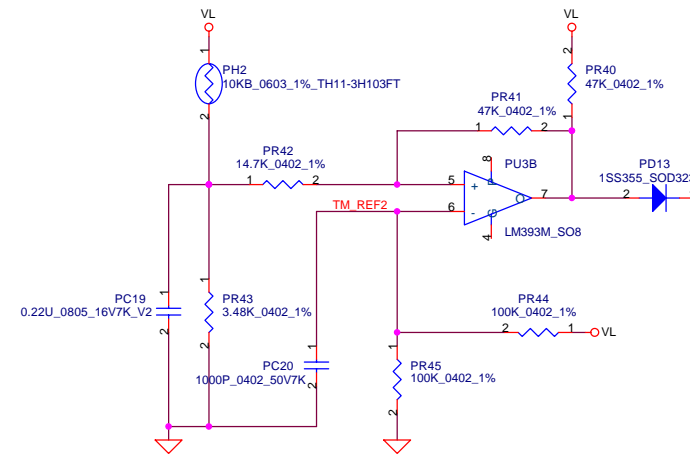
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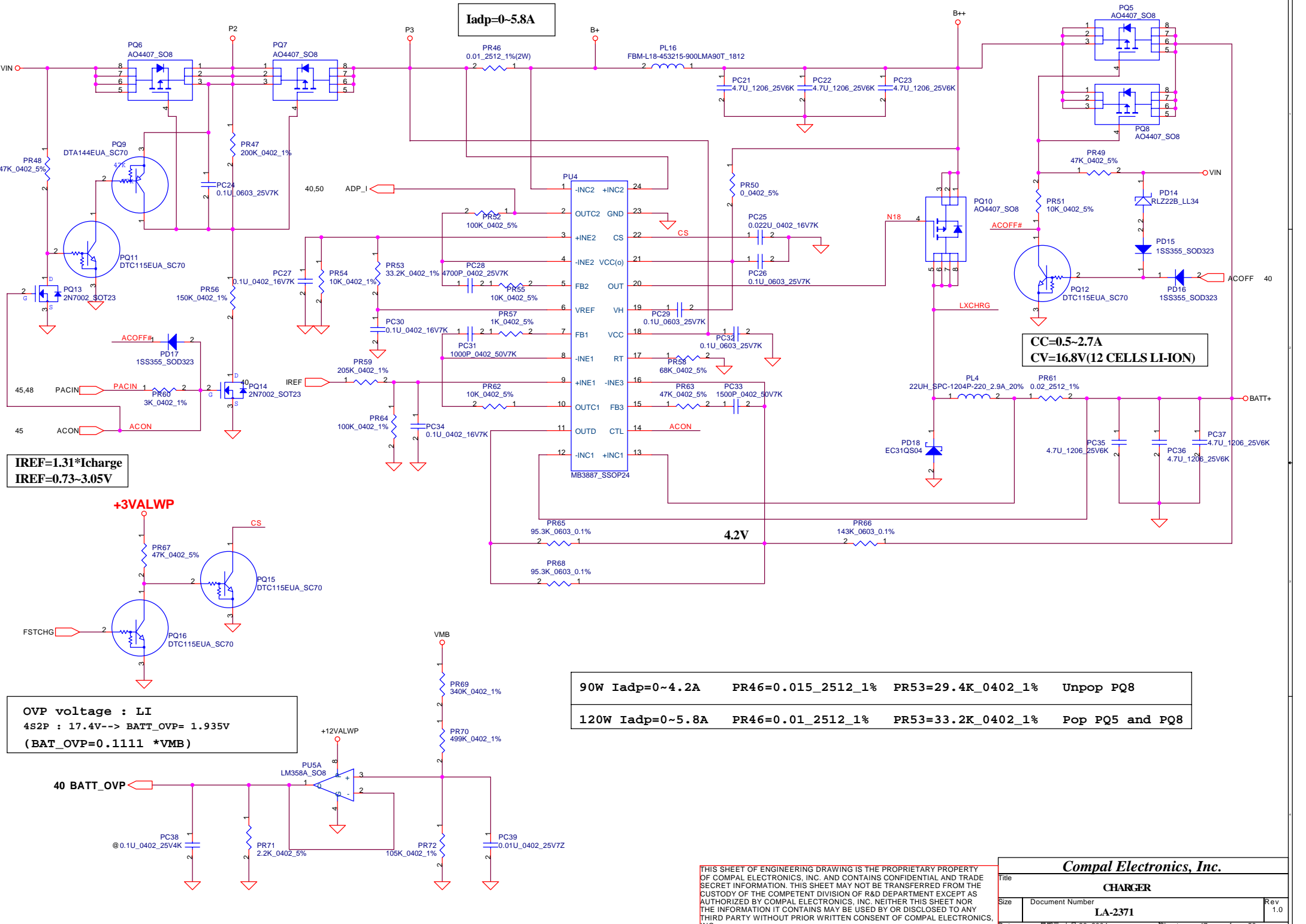
Compal Electronics, Inc.		
DCIN & DETECTOR		
Title	Document Number	Rev
	LA-2371	1.0
Date:	星期三, 七月 28, 2004	Sheet 45 of 56

PH1 under CPU botten side :
 CPU thermal protection at 84 degree C
 Recovery at 45 degree C



PH2 near main Battery CONN :
 BAT. thermal protection at 79 degree C
 Recovery at 45 degree C





I_{adp}=0~5.8A

**CC=0.5~2.7A
CV=16.8V(12 CELLS LI-ION)**

**I_{REF}=1.31*I_{charge}
I_{REF}=0.73~3.05V**

+3VALWP

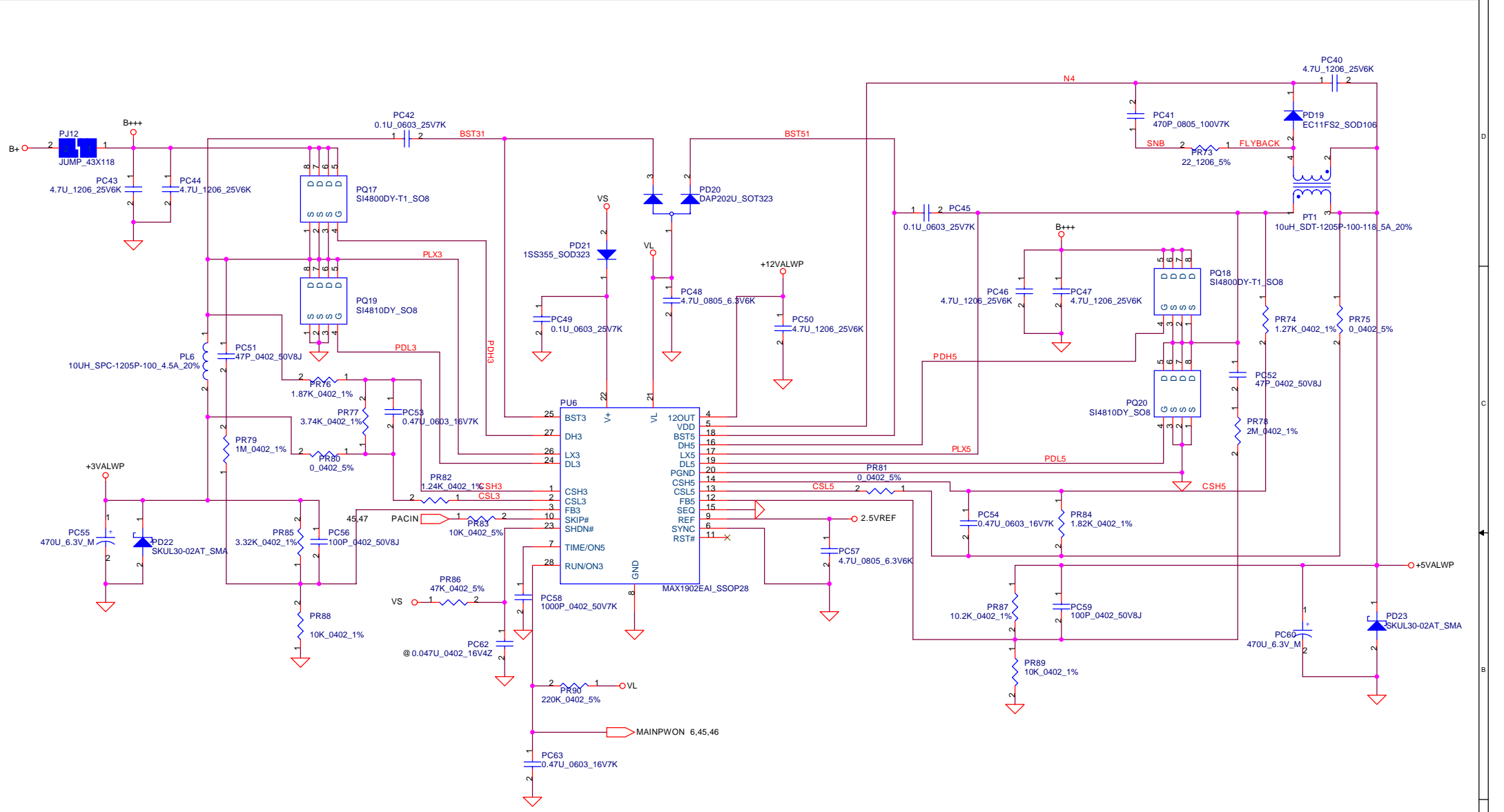
**OVP voltage : LI
4S2P : 17.4V--> BATT_OVP= 1.935V
(BAT_OVP=0.1111 *VMB)**

90W I_{adp}=0~4.2A	PR46=0.015_2512_1%	PR53=29.4K_0402_1%	Unpop PQ8
120W I_{adp}=0~5.8A	PR46=0.01_2512_1%	PR53=33.2K_0402_1%	Pop PQ5 and PQ8

40 BATT_OVP

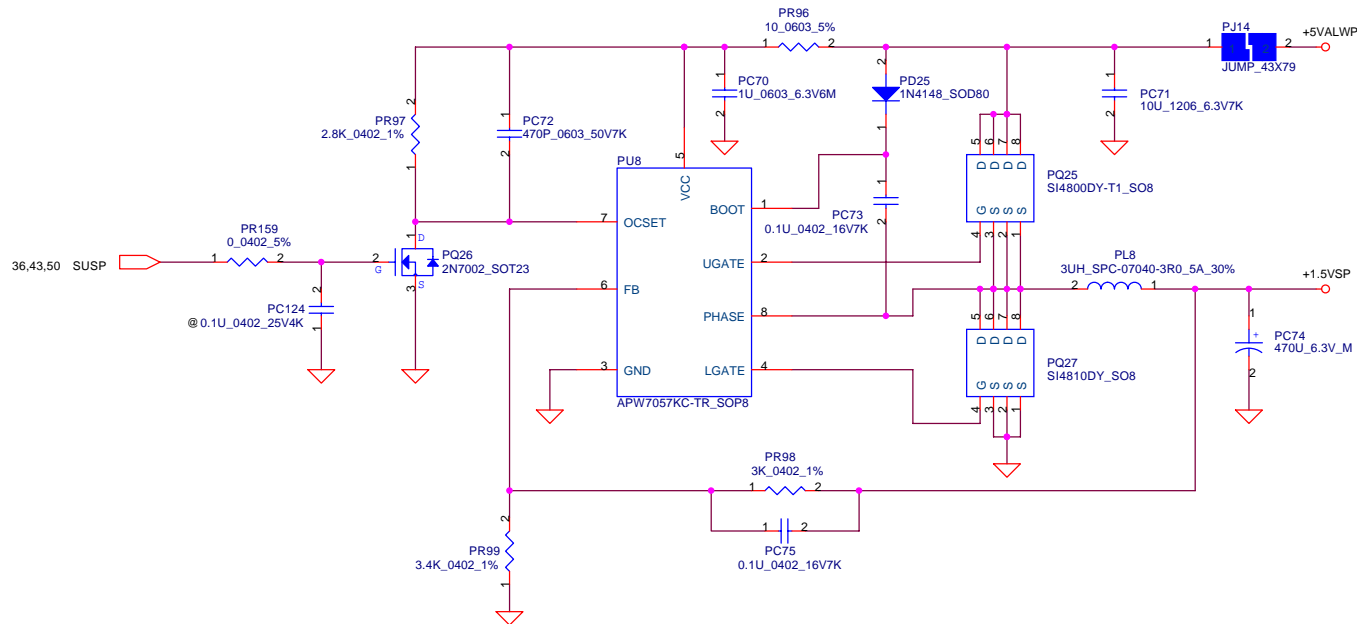
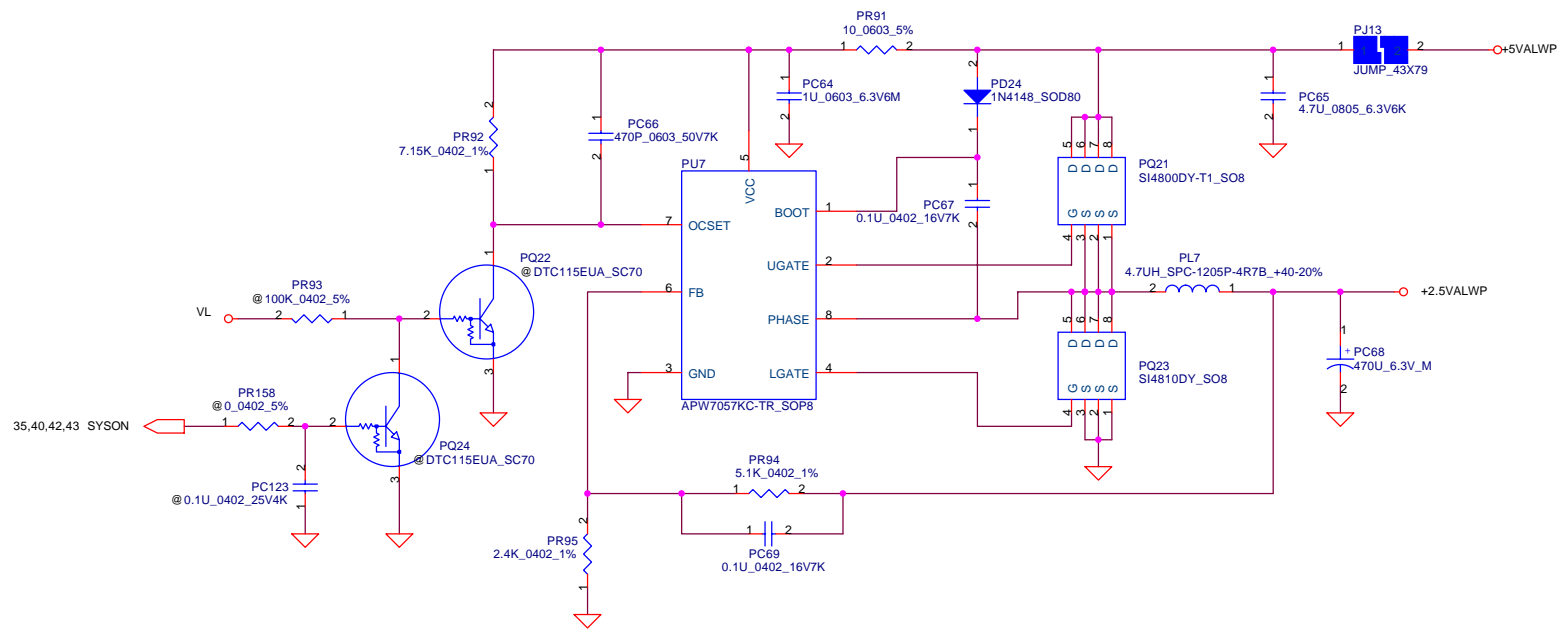
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Compal Electronics, Inc.		
CHARGER		
Size	Document Number	Rev
	LA-2371	1.0
Date:	星期三, 七月 28, 2004	Sheet 47 of 56



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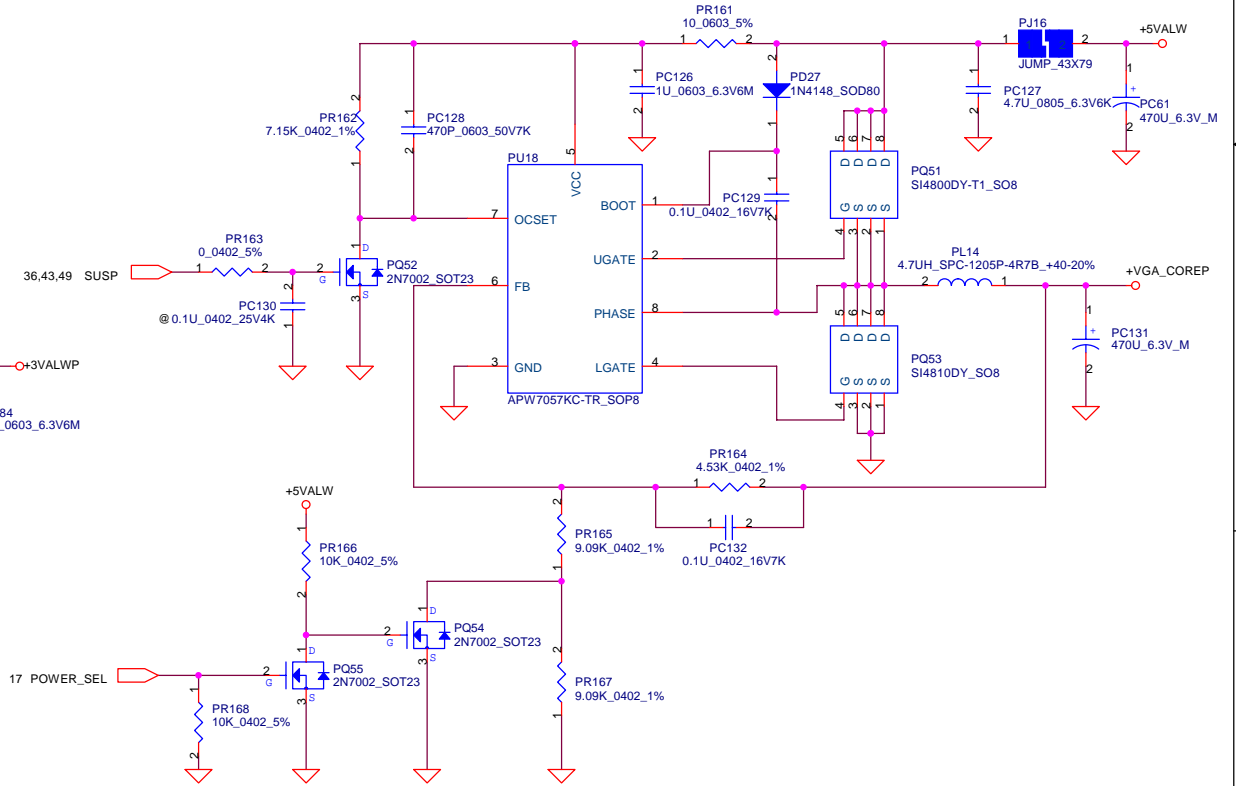
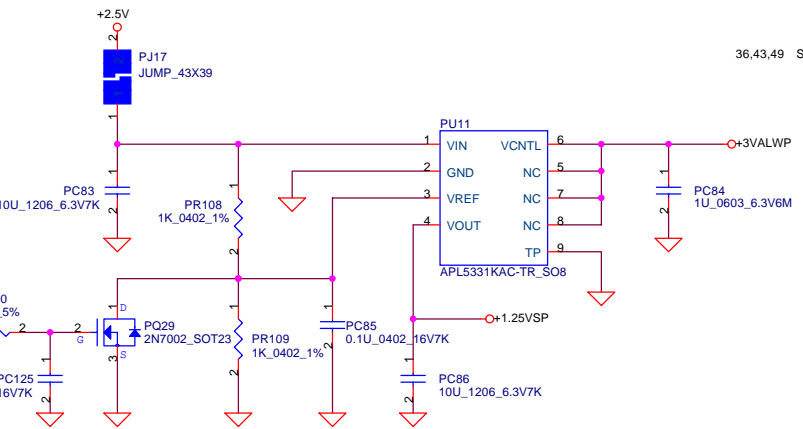
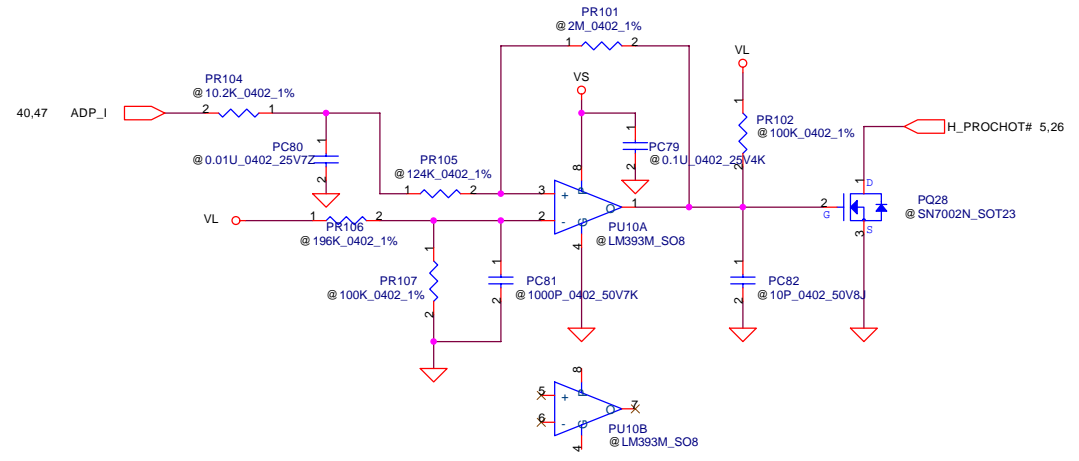
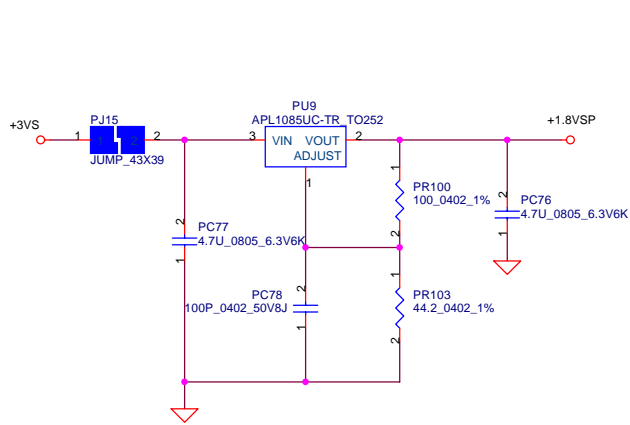
Compal Electronics, Inc.		
Title 5V/3.3V/12V		
Size	Document Number LA-2371	Rev 1.0
Date:	星期三, 七月 28, 2004	Sheet 48 of 56



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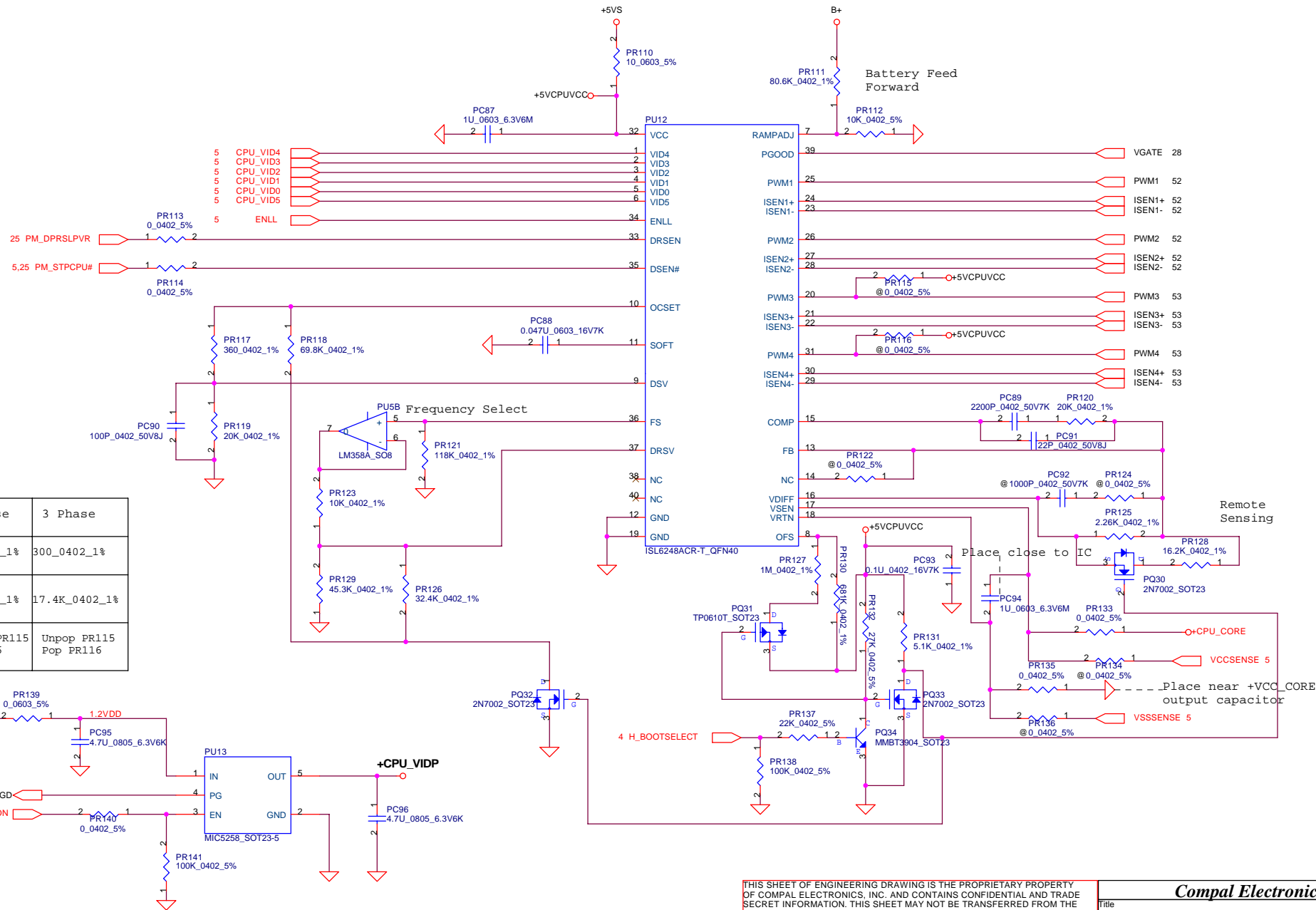
Compal Electronics, Inc.		
Title 2.5V/1.5V		
Size	Document Number LA-2371	Rev 1.0
Date:	星期三, 七月 28, 2004	Sheet 49 of 56

85W THROTTLING
70W RECOVERY

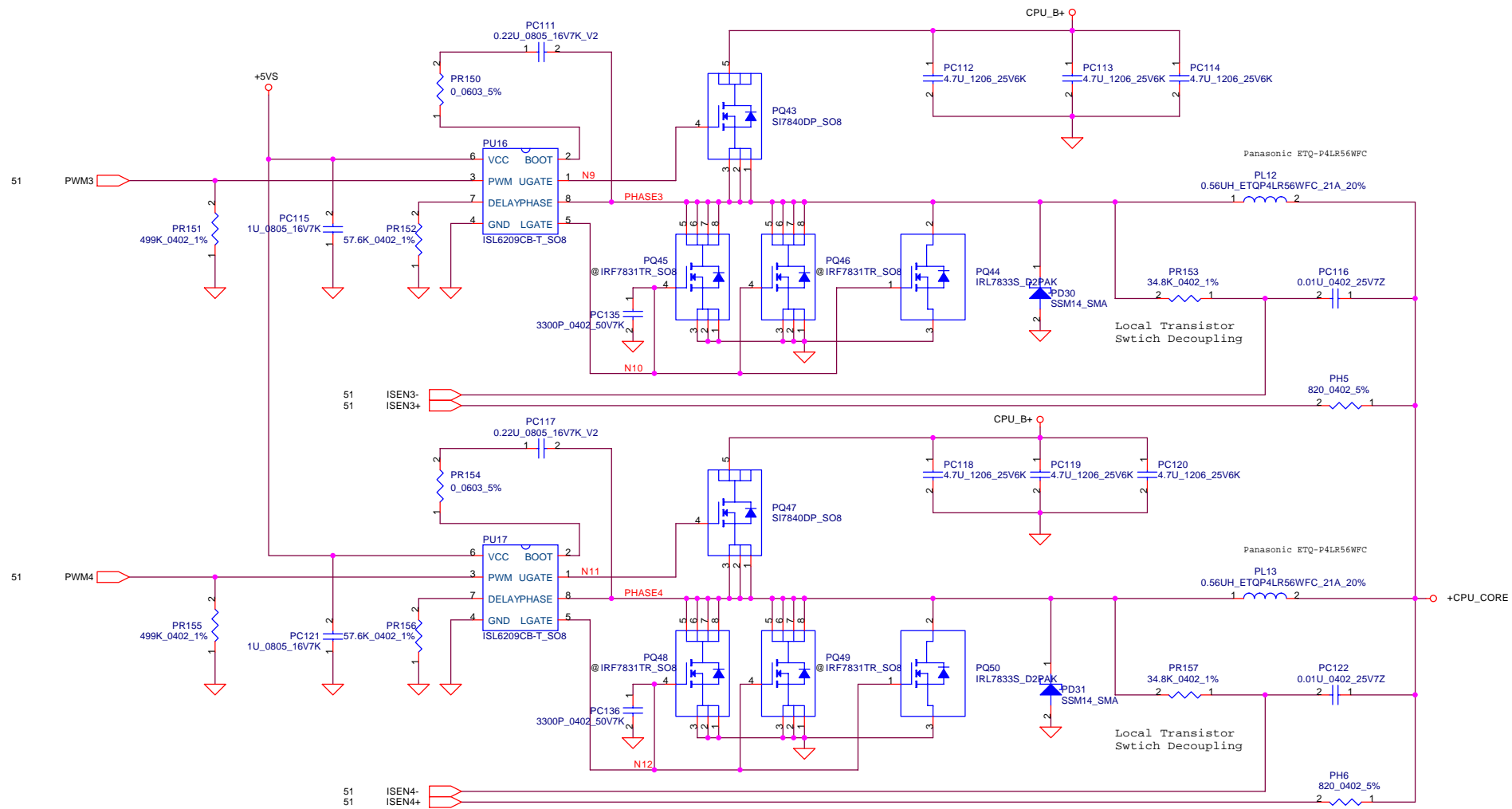


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Compal Electronics, Inc.			
Title 1.8V/PROCHOT/1.25V/VGA			
Size	Document Number	LA-2371	Rev 1.0
Date:	星期三, 七月 28, 2004	Sheet 50 of 56	



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Compal Electronics, Inc.		
Title CPU_CORE (2)		
Size	Document Number LA-2371	Rev 1.0
Date: 星期三, 七月 28, 2004	Sheet 53	of 56

POWER PIR LIST

page	Reason for change	Modify list
DVT 45,46, 49,51	Update BOM	Change PC7 form 0.022u to 0.22u(SE041224K03), PR36 from 25.5K to 6.49K(SD034649100) Change PC17,PC19 form 0.022u to 0.22u(SE030224KT1), PC71 from 4.7u to 10u(SE114106K00) Change PR130 from 340K to 681K(SD034681300) Change PC133,PC134,PC135,PC136 from 3300p to 4700p(SE75472K00)
52	For EMI team request	Add PL15 (FBM-L18-453215-900LMA90T_1812: SM010020700)
52	Solve noise issue	Add PC102(220u; SF22004M200)
PVT	Add 2nd source	Add 2nd source
45,47	For common part with H/W	Change PQ13,PQ14,PQ2,PQ26,PQ29,PQ30,PQ32,PQ33,PQ52,PQ54,PQ55 from SB570020500 to SB7700200T5
48	To decrease 3V/5V negative voltage	Change PD1 from EC10QS04(SC10QS041T4) to SSM14(SCSSSM14000) Change PD18 from RB051L(SC1B051L000) to EC31QS04(SC11QS04000) Change PD22,PD23 from SSM14(SCSSSM14000) to SKUL30-02AT(SCSKUL30000)

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Title		
EFW00 PIR LIST		
Size	Document Number	Rev
B	LA-2371	1.0
Date:	星期二, 七月 27, 2004	Sheet 54 of 56

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NO DATE	PAGE	MODIFICATION LIST	PURPOSE
4/21	P.42	Move R57 to D8.2	Avoid leakage current
	P.36	change footprint of U7	for SMT process
	P.29	change footprint of U9	for SMT process
	P.24	swap JP2 channel A and channel B pin	for LVDS Conn.issue
4/22	P.36	Swap C38 & R54 location	For audio speak DC 2.5V level
	P.36	Pop R55& R36 Depop R54	For Audio noise
	P.36	mirror VR1	For Audio Volume smoothly
	P.35	Del R611	For Audio clock 14.318MHz
4/26	P.25	Add R771 pull high to +3VS	Modify IXP 150 GPIO pin
	P.40	Add R772 & R773	To avoid RTCVCC loss in EC
	P.40	Modify U15.90,U15.93,U15.94	To adjust SKU ID & BIOS ID
4/27	P.31	Swap Jp31.19 and Jp31.25	For XD card issue
	P.31	Change R746,R744,R751 power plane to +VCC_5IN1	
	P.31	Add R775 for Reserve	
	P.30	Add R774 for Reserve	
	P.30	Change R769 power plane to +VCC_5IN1	
	P.31	Add JP32 for Reserve	
	P.36	To change R220=3.3k,R233=4.7k,R239=4.3k	For Speak and HP Gain
	P.36	Add R764,Del R468	For audio Gain adjust
	P.36	To modify U7 CIS LIB	For Speaker can not mute when plug in HP
4/30	P.24	Add L55,L57,C862,C864	for EMI issue
	P.38	Add L63-L65	for EMI issue
	P.26	Add L58,C866	for EMI issue
	P.36	Add L59-L62	for EMI issue
	P.29	Add L71,L72 / Del R97,R106 / Change L13	for EMI issue
	P.25	Change R661,R658,R662,R665,R651,R654,R668,R315	for EMI issue
	P.40	Pop CPL-CP6	for EMI issue
	P.41	Add C871-C881,L66-L68	for EMI issue
	P.43	Add L69,L70	for EMI issue
	P.35	Change U46 CIS to ALC250 ver. C	for direct CD play issue
5/3	P.40	Re-define EC_URXD/EC_UTXD/KS017 pin assignment	for CIR function
	P.40	Add C882	for SKU ID
5/4	P.24	Depop R58,R48/Pop U4,C39	for S3 panel garbage
	P.38	Add U55	for G528 reserve
	P.38	JP16 modify Layout LIB	for reverse type
	P.38	Change Power from +USB_AS to USB_BS	for reverse type
	P.24	Move R58 to Q4.2	for reserve
	P.30	Add R776	for SM_CD# pull high
	P.31	Define 5IN1 CONN. SM_CD# signal	for SM card protect
5/5	P.17	Modify VRAM strap pin, Add R30	for 32MB/64MB/128MB
5/6	P.26	Change R388 to 12K	for USB eyediagram
	P.31	Depop R749/ Change R746,R744,R742 to 10K,Change R751 to 2.2K	for ENE suggestion
	P.30	Depop R749,R735,R732,R727,R731,R738,R768,R741,R719/Pop R770/Change R768 to 2.2K	for ENE suggestion
	P.42	Add Hibernation circuit	for S4 function
	P.24	Change D25,D54 symbol	for 1N4148 Cache LIB
	P.40	Re-define S4_DATA,S4_LATCH	for Hibernation function
5/7	P.33	Change +5VS_miniPCI to +5VS	for Lifeview SPEC.
	P.7	Add R785-R788,D59,D60	For ATI suggestion
	P.35	Add C860,C861	For Analog TV sound
	P.31	Add R789	For 5in1 issue
5/8	P.40	Add R790,C888	for Battery.
	P.23	Add L73-L75	For EMI issue
	P.31	Change R718 to 43K	For 5IN1 function
5/10	P.40	Change RCIRRX to 76 pin	For CIS function
	P.40	Add R791	For RCIRRX pull high +3valw
5/11	P.38	Reserve JP33,R792,R793	for debug
	P.36	Add C889	For Audio noise
	P.26	Del Q32,R317,R312,R318	For ATI suggestion
5/12	P.28	Change R323,R332 to 300K/pop R736 10K	for power on sequence
	P.23	Add Jump from RF GND to Digital GND	for EMI&ESD
5/13	P.40	Reserve R794	for avoid "Po" noise when power on/off
	P.30	Add R795	for "Po" noise test
	P.34	Change IEEE 1394 to VT6301S	for cost down

NO DATE	PAGE	MODIFICATION LIST	PURPOSE
5/17	P.24	Add C862,C864	for EMI issue
	P.43	Add H54	for ME
	P.44	Change R406 to 22ohm	for modem function
	P.23	Change R7,R437 to 4.7kohm	for CRT function
5/18	P.39	Reserve L77 from CD_AGND to Digital GND	for Audio noise test
	P.23	Add R809	for GPIO pin
5/20	P.31	Add Q67,R810,R811,R812	for Audio noise test
5/20	P.31	Add U22C OR gate	for Audio PO sound
=====Rev0.3=====			
6/17		write by Timo Teng	
P.27		Add R813	For S/W DJ Function
P.31		Add C904, C905, C906 C907	For 5 in 1 card transfer noise
P.35		Add R820	For BITCLK smooth
		Add R822, R823, @ in L40	
		del @ in L50	For Audio noise
P.36		Add @10k in R179, R189, R184 and R196	For SWDJ
		Del R95, R98, C112, C110	For Cost down
P.37		Del Hardware EQ circuits	
		Add APA2121 Audio Amplifier circuits	For Cost down
P.40		Add GPIO at pin98, 97,92,85,86 of KB910	For cost down
		Del @ inR773 and Add @ in R772	For RTC power saving
P.41		Add @ in U26, C305, R311, C337 and R331	For cost down
P.42		R235 pull up voltage from +5VS to +5VALW	For SWDJ LED
P.43		H37 connects to GND	
P.43		Add @ in all CIR circuits.	For Del CIR function.
6/21		write by Timo Teng	
P.20		Add C920	
		Change C230 value from 150uF to 220uF	For VGA_CORE stable.
P.42		Change value of R235, R142 and R452 from 300 to 180 ohms	For cost down
6/22		write by Timo Teng	
P.23		Del JP13, JP3, JP14, J1, L73, L74, L75	For take out TV turner
P.31		Add @ into R743 and C847	For some SD Card can't be detected
P.35		Add C922	For decrease Bo sound in Dos Mode
P.36		Add R98, R95, C112, C110	For SWDJ if the SMBUS can't be programed
P.37		Add R823, R824, C923, C924, C925	For SWDJ if the SMBUS can't be programed
P.41		Add @ in L68	For take out CIR function.
		Del C336, U33	For Del 512KB flash ROM
6/23		write by Timo Teng	
P.40		Del CPL-CP6	
		Add C926-C949	For EMI Cost down
6/27		write by Timo Teng	
P.24		Change Value of C26 from 1000P to 0.047U	For SWDJ backlight getting off

NO DATE	PAGE	MODIFICATION LIST	PURPOSE
7/1	P.30	Connect U52.M11 to U52.J9	for follow Fortworth definition
	P.43	Del H52,H53	for layout modify
	P.43	Reserve C950,C951,C952	for EMI test
7/12	P.11	Del C567,C545 and Add C953	for Cost down
=====Rev1.0=====			
7/23		write by Timo Teng	
P.23		Change R443,R440,R438,R442,R441,R439 from 75_0402_5% to 75_0402_1%	
P.25		Change R643 from 330 to 130 ohm	For TPDJ issue
		Add @ in R668	For EMI request
P.26		Change R388 from 12K to 11.5K ohm	For USB2.0 quality
P.34		Add @ in R802	For VIA recomanation
P.36		Del R98, R95,C112, C110	For Harman request
P.37		Add @ in APA2121 circuits	
P.38		Add @ in U5 and Super I/O circuits.	
		Del @ in U55	

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File	PIR LIST-2	
Size	Document Number	Rev
C	LA-2371	1.0
Date:	日期: 七月 27, 2004	Sheet 55 of 56

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P.40 Change R175 and R176 from 0 to 1K ohm
Add @ in R172
P.42 Modify S4 resume circuit

For solve KB910 into test mode
For LPDPC doesn't be used
For solve KB910 into test mode

7/27 Write by Timo Teng

P.24 R31,R34,R32,R33 from 75_0402_5% to 1%
P.31 Add R825

Change 789 from 43K to 10K

For solve power switch ripple

P.36 Change JP10 and JP11 from ACES 85204-0200 to ACES 85205-0200

For ME request

P.40 Add C954 at pin176 of U15

For FAN2 test Fail

7/28 Write by Timo Teng

P.30 Add R826

Change R721 from 33 to 22 ohm

For SD Card Function

P.30 Del R743

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Title	PIR LIST-2	
Size	Document Number	Rev
C	LA-2371	1.0
Date:	星期三, 七月 28, 2004	Sheet 56 of 56