

Compal Confidential

Fortworth Banias EAL20 LA-2461 Schematic

uFC-PGA Dothan / Montara-GM+
M11P-128M VRAM / ICH4-M

2004-07-21

REV: 0.3

Compal Electronics, Inc.

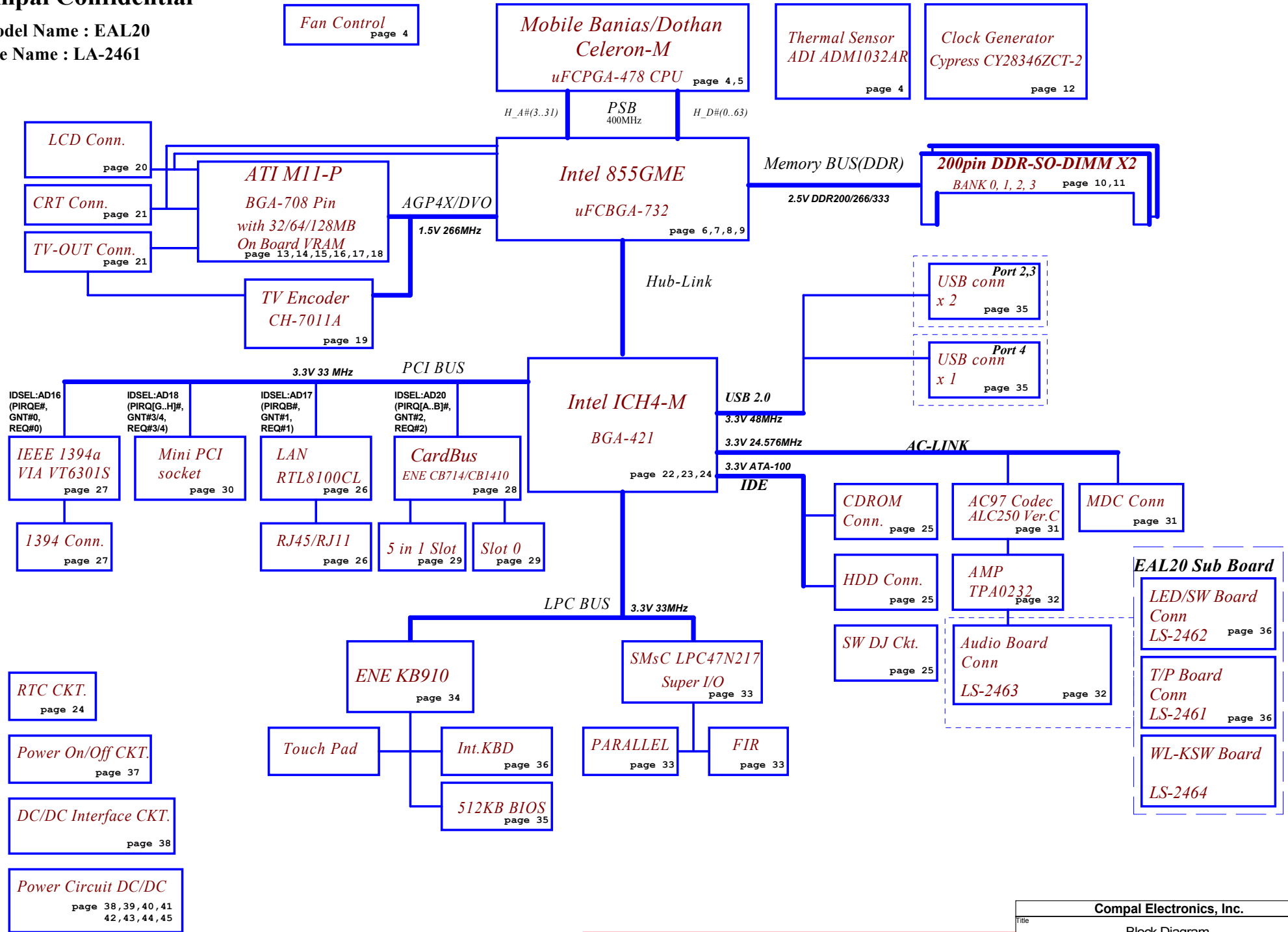
Title		
Cover Sheet		
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	EAL20 LA-2461	0.3
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Model Name : EAL20

File Name : LA-2461



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Block Diagram		
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Voltage Rails

Power Plane	Description	S0-S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VCCP	1.05V rail for Processor I/O	ON	OFF	OFF
+1.25VS	1.25V switched power rail for DDR Vtt	ON	OFF	OFF
+VGA_CORE	1.2V/1.0V switched power rail for VGA core power	ON	OFF	OFF
+1.35VS	1.35V switched power rail for GMCH core power	ON	OFF	OFF
+1.5VALW	1.5V always on power rail	ON	ON	ON*
+1.5VS	1.5V switched power rail for AGP interface	ON	OFF	OFF
+1.8VS	1.8V switched power rail for CPU PLL & Hub-Link	ON	OFF	OFF
+2.5V	2.5V power rail for system DDR	ON	ON	OFF
+2.5VS	2.5V power rail for VGA DDR	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V switched power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

ICH4-M I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 X
DDR SO-DIMM 1	A2	1 0 1 0 0 0 1 X
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 X




KB910 I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
SM1 24C16	A0H	1 0 1 0 0 0 0 X b
SM1 SMART BATTERY	16H	0 0 0 1 0 1 1 X b
SM2 ADM0132 CPU THERMAL MONITOR	98H	1 0 0 1 1 0 0 X b
SM2 ALC250 AUDIO CODEC	00H	0 0 0 0 0 0 0 X b

External PCI Devices

DEVICE	PCI Device ID	IDSEL #	REQ/GNT #	PIRQ
1394	D0	AD16	0	E
LAN	D1	AD17	1	F
CARD BUS	D4	AD20	2	A
SIN1	D4	AD20	2	B
Mini-PCI	D2	AD18	3,4	G,H
AGP BUS	N/A	AGP_DEVSEL#	N/A	A

Symbol note:

-  :means digital ground.
 :means analog ground.
 @ :means reserved.

Fortworth Banias Comparison Table

Item	* Describe	UMA	Page
VGA	ATI M11P	UMA	13 ~ 16
VRAM	128MB/64MB	NA	13 ~ 14
TV Encoder	NA	CH7011A	19

Board ID Table for AD channel

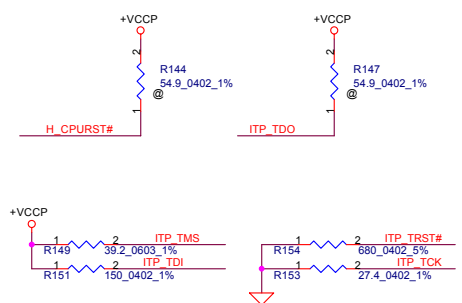
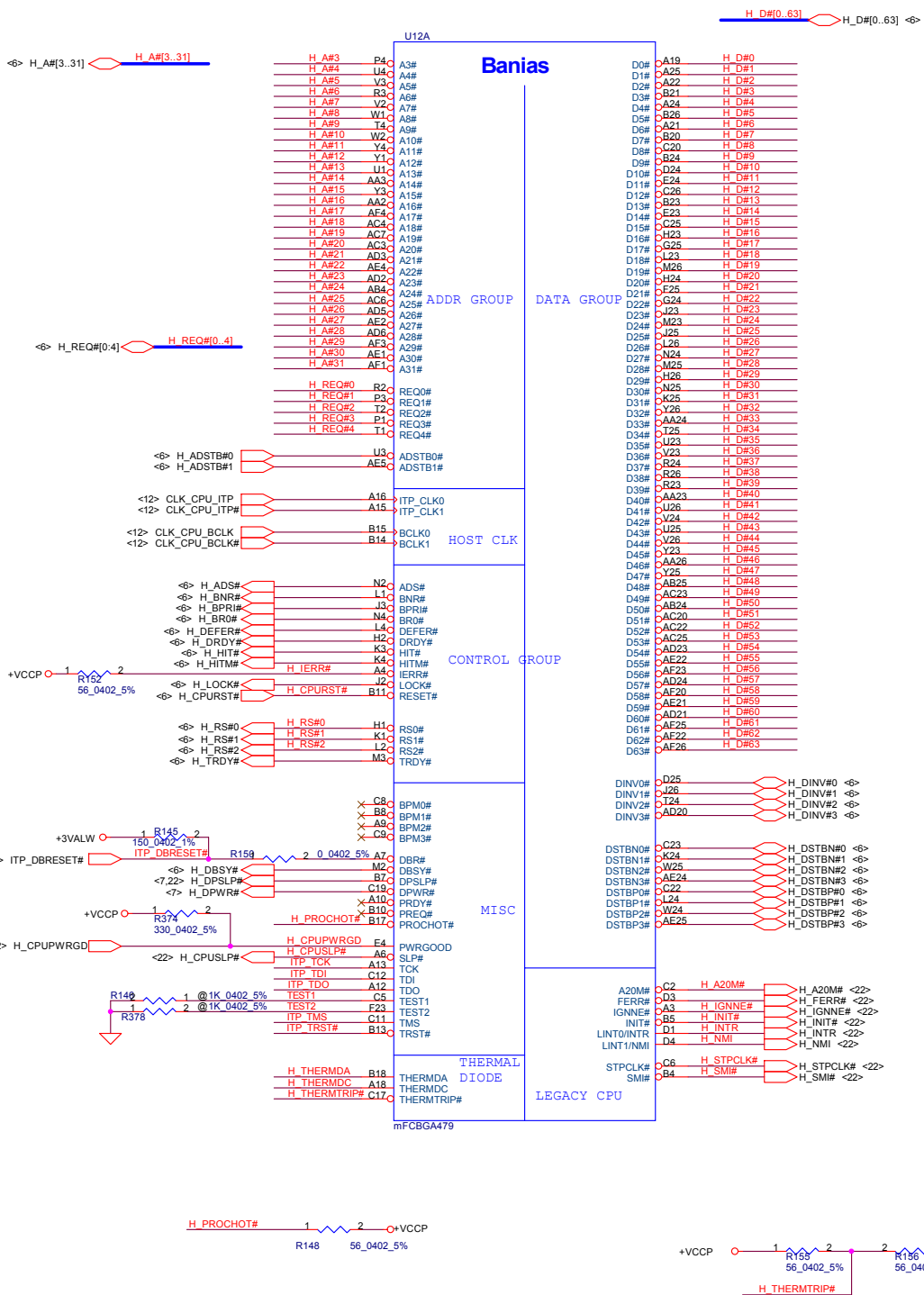
Vcc	3.3V +/- 5%			
Ra	10K +/- 5%			
BID/FID	Rb/Rc	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	1.412 V	1.486 V	1.560 V
2	18K +/- 5%	2.015 V	2.121 V	2.227 V
3	33K +/- 5%	2.406 V	2.533 V	2.659 V
4	56K +/- 5%	2.660 V	2.800 V	2.940 V
5	NC	3.135 V	3.300 V	3.465 V

Board ID	PCB Revision
* 0	0.1
1	0.2
2	0.3
3	0.4
4	0.5
5	
6	
7	

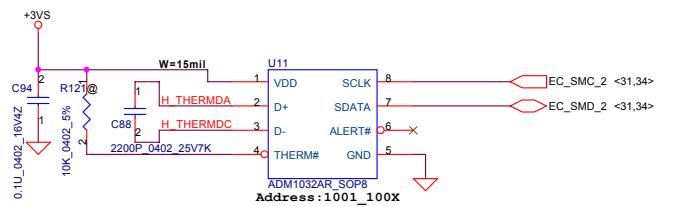
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Notes List		
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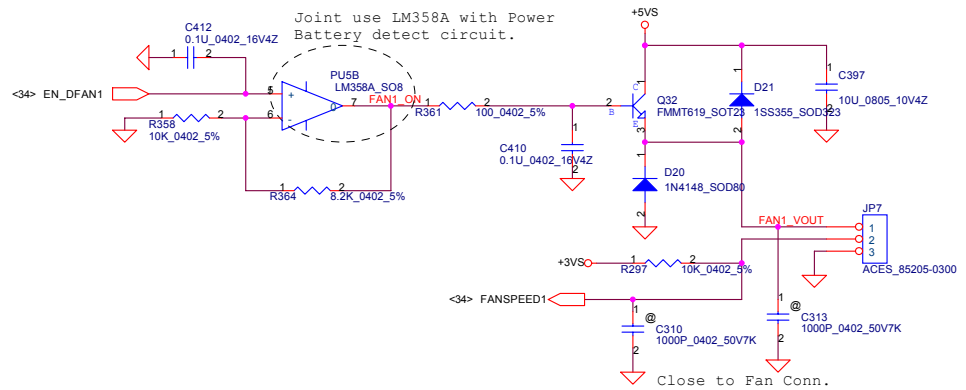
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Thermal Sensor ADI ADM1032AR



Fan Control circuit



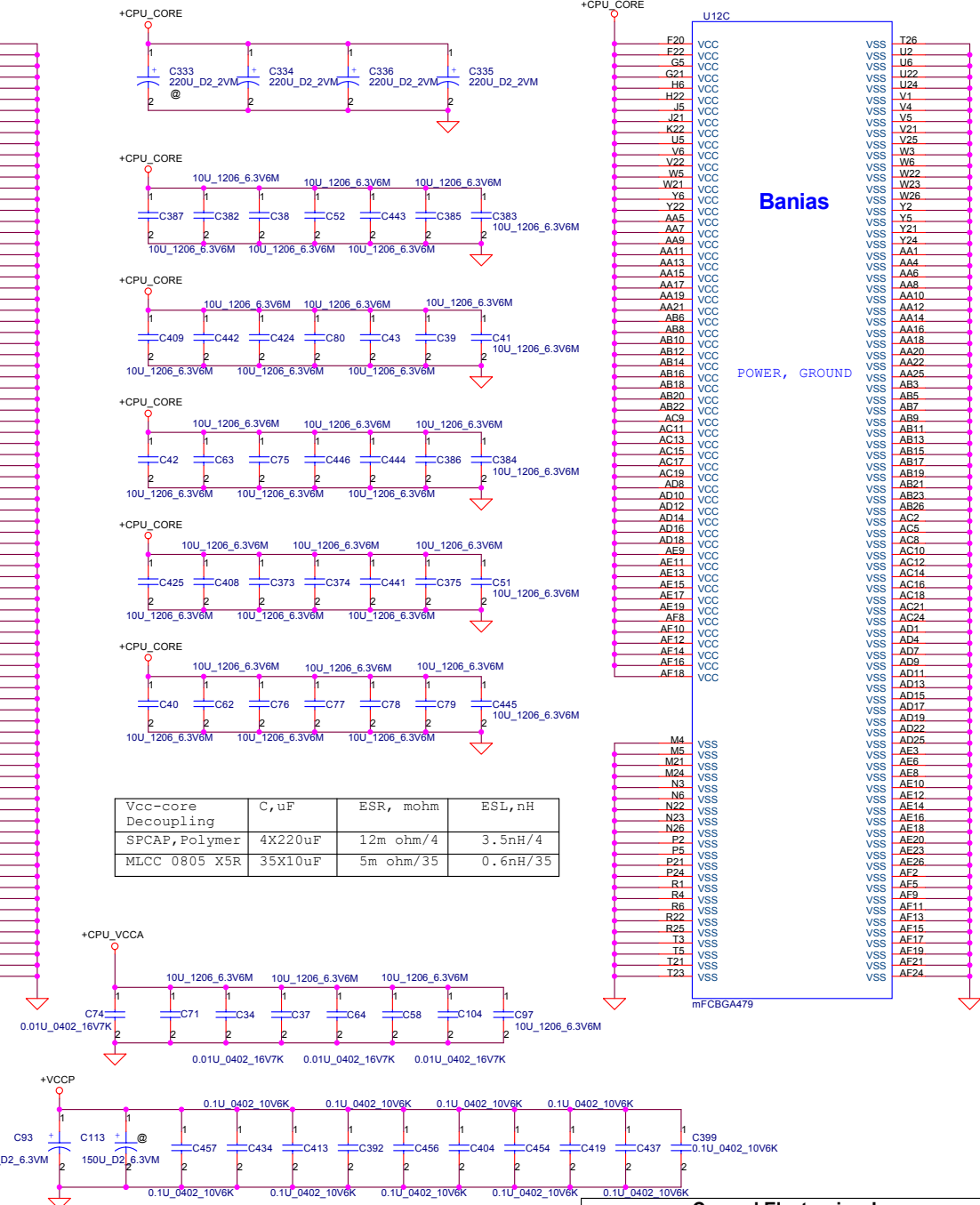
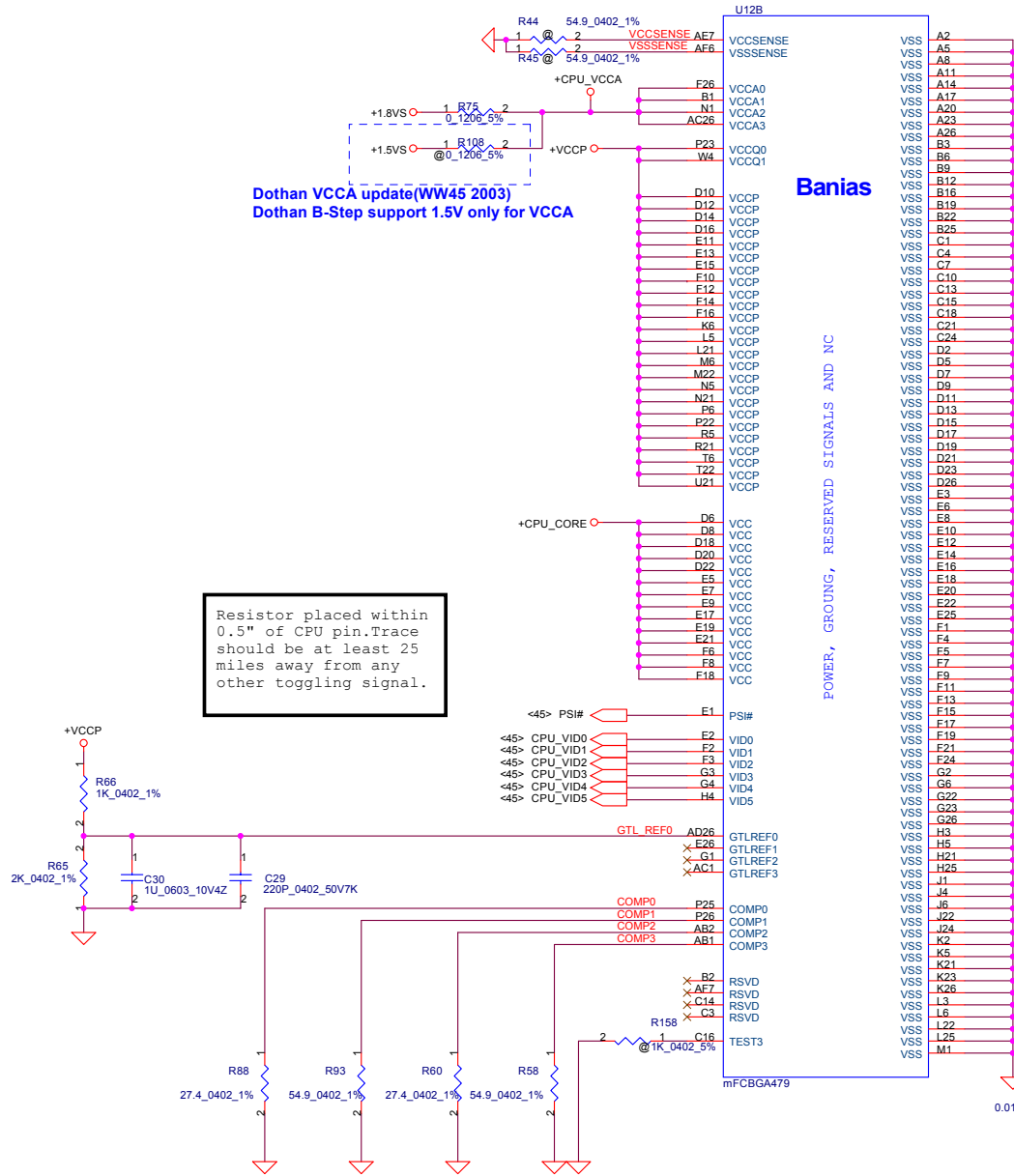
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Title			
INTEL CPU BANIAS (1 of 2)			
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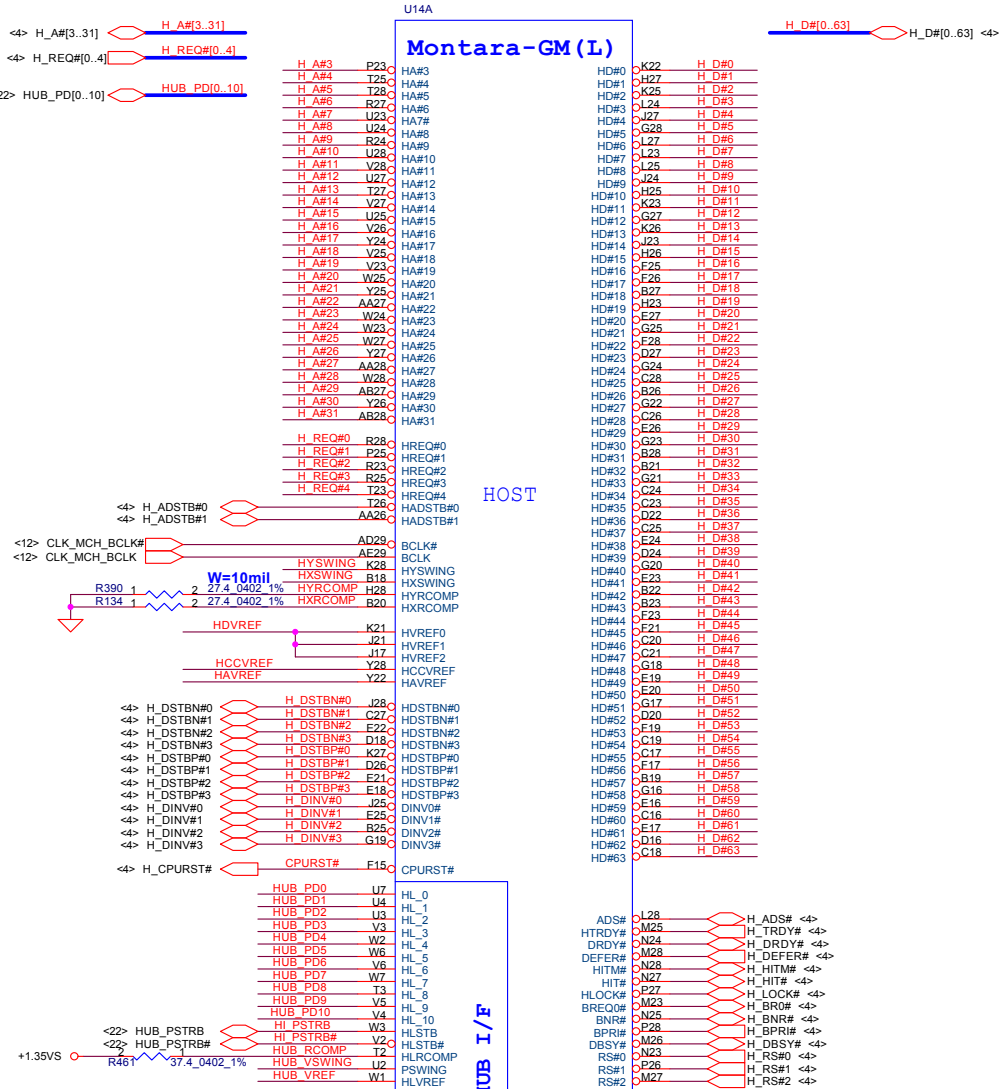
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Dothan VCCA update(WW45 2003)
Dothan B-Step support 1.5V only for VCCA

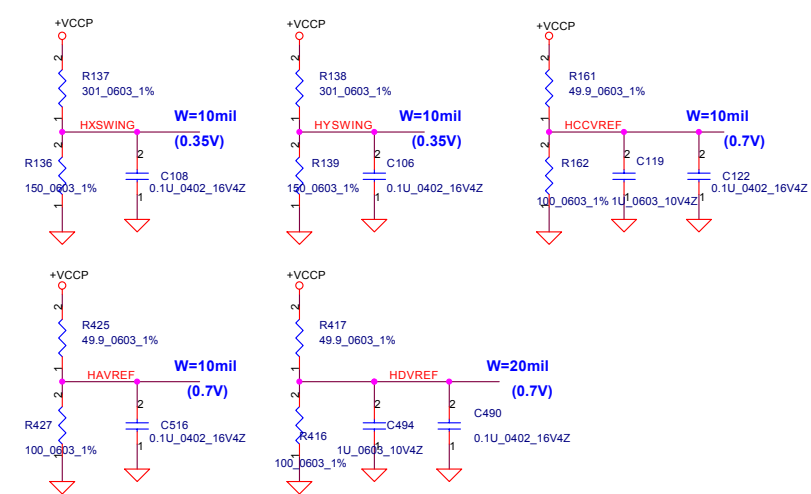
Resistor placed within 0.5" of CPU pin.Trace should be at least 25 miles away from any other toggling signal.

Resistor placed within 0.5" of CPU pin.Trace should be at least 25 miles away from any other toggling signal.

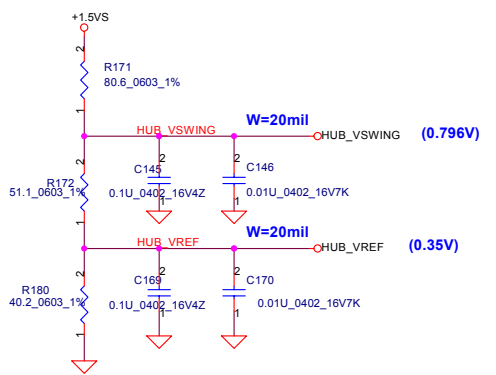




HOST REF VOLTAGE



HUB I/F REF VOLTAGE



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Title INTEL 855GME-HOST(1/4)			
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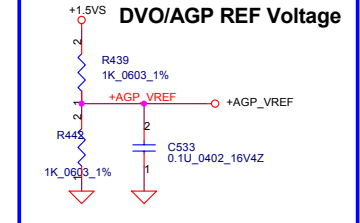
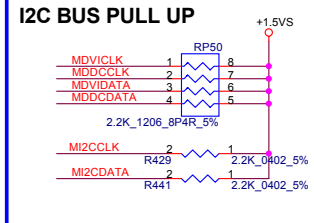
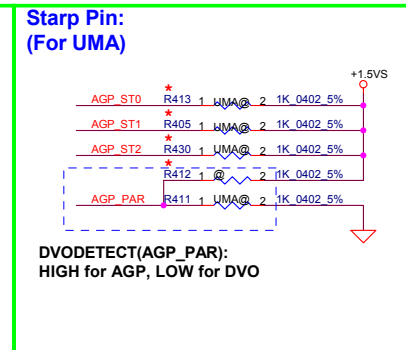
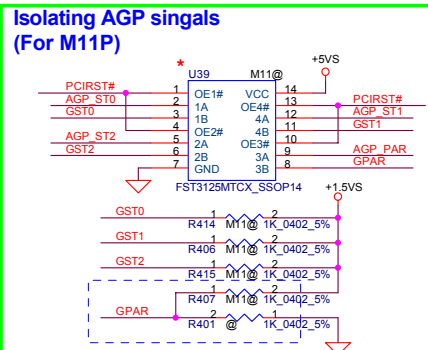
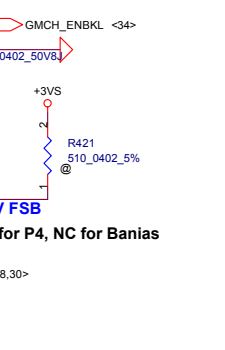
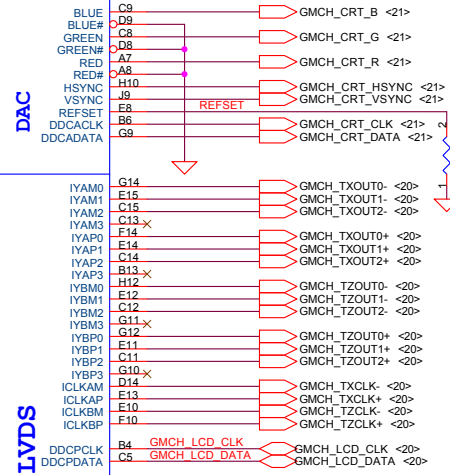
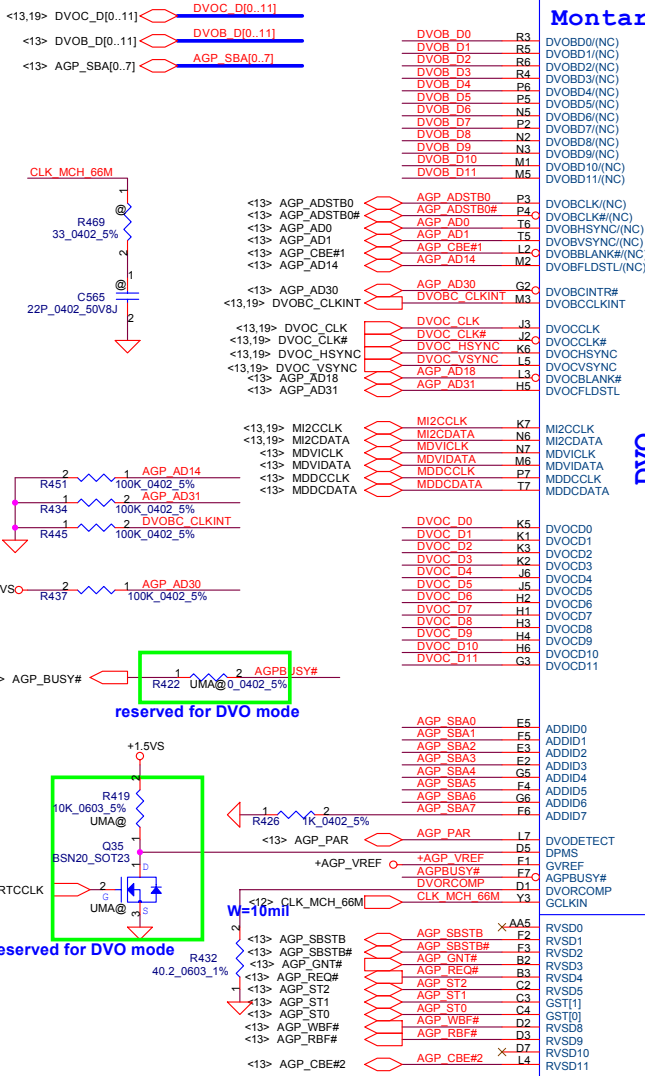
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855GME DVO/AGP Pin Muxing

Ball	DVO Mode	AGP Mode
R3	DVOBD0	GAD3
R5	DVOBD1	GAD2
R6	DVOBD2	GAD5
R4	DVOBD3	GAD4
R7	DVOBD4	GAD7
P5	DVOBD5	GAD6
N8	DVOBD6	GAD8
P2	DVOBD7	GCBE#0
N2	DVOBD8	GAD10
N3	DVOBD9	GAD9
M1	DVOBD10	GAD12
M5	DVOBD11	GAD11
P3	DVOBCLK	GADSTB0
P4	DVOBCLK#	GADSTB0#
T6	DVOBHSYNC	GAD0
T5	DVOBVSNC	GAD1
L2	DVOBLANK	GCBE#1
M2	DVOBFLDSTL	GAD1
M3	DVOBCLINT#	GAD30
J3	DVOCCLK	GAD13
J2	DVOCCLK#	GADSTB1
K6	DVOCHSYNC	GAD11#
L5	DVOCVSYNC	GAD16
L3	DVOCLANK	GAD18
H5	DVOCLDSTL	GAD31
K7	MIZCLK	GIRDY#
N6	MIZDATA1	GDEVSEL#
N7	MDVICLK	GTRDY#
M6	MDVIDATA	GFRAME#
P7	MDDCCLK	GSTO#
T7	MDDCDATA	GAD15
K5	DVOCD0	GAD20
K1	DVOCD1	GAD20
K3	DVOCD2	GAD21
K2	DVOCD3	GAD22
J6	DVOCD4	GAD23
J5	DVOCD5	GCBE#3
H2	DVOCD6	GAD25
H1	DVOCD7	GAD24
H3	DVOCD8	GAD27
H4	DVOCD9	GAD26
H6	DVOCD10	GAD29
G3	DVOCD11	GAD28
E5	ADDID0	GSBA0
F5	ADDID1	GSBA1
E3	ADDID2	GSBA2
E2	ADDID3	GSBA3
G5	ADDID4	GSBA4
F4	ADDID5	GSBA5
F6	ADDID6	GSBA6
F8	ADDID7	GSBA7
L7	DVODETECT	GPAP
D5	DPMS	GPIPE#
F2	RVSD1	GSBSTB
F3	RVSD2	GSBSTB#
B2	RVSD3	GGNT#
B3	RVSD4	GREQ#
C2	RVSD5	GST2
C3	GST1	GST1
C4	GST0	GST0
D2	RVSD8	GWBF#
D3	RVSD9	GRBF#
D4	RVSD10	GCBE#2
L4	RVSD11	

U14B

Montara-GM (L)

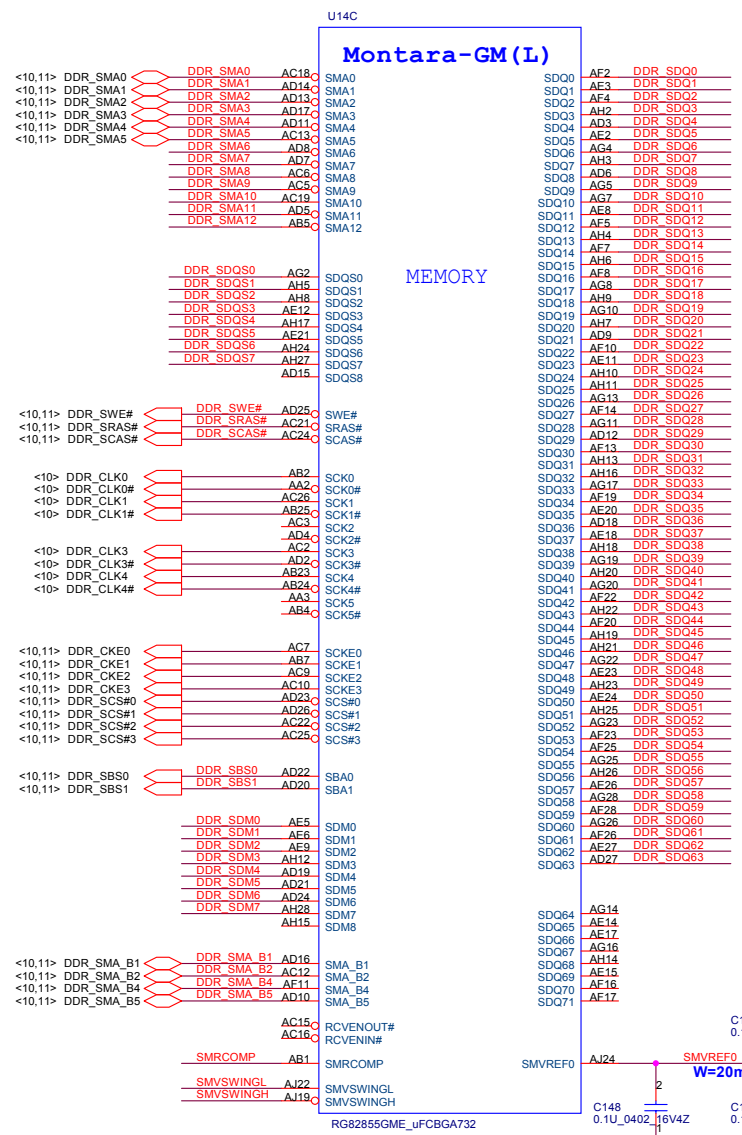


Starp pin list

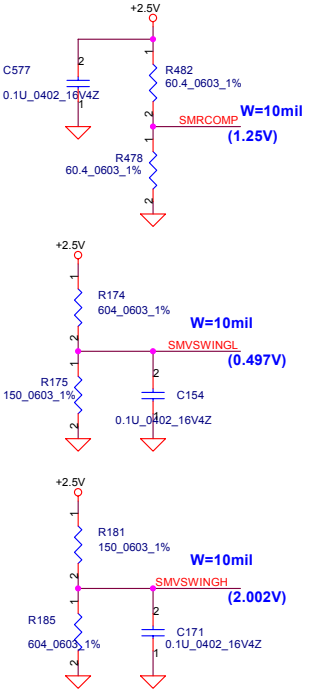
ST2	ST1	ST0	PSB/Mem/GFX
0	0	0	400 / 266 / 200
0	0	1	400 / 200 / 200
0	1	0	400 / 200 / 133
1	1	1	400 / 333 / 250 *

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DDR_SQ0[0..63] <10,11> DDR_SMA[6..12] <10,11>
 DDR_SQ0S[0..7] <10,11> DDR_SDM[0..7] <10,11>

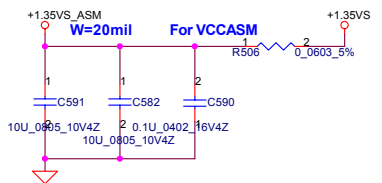
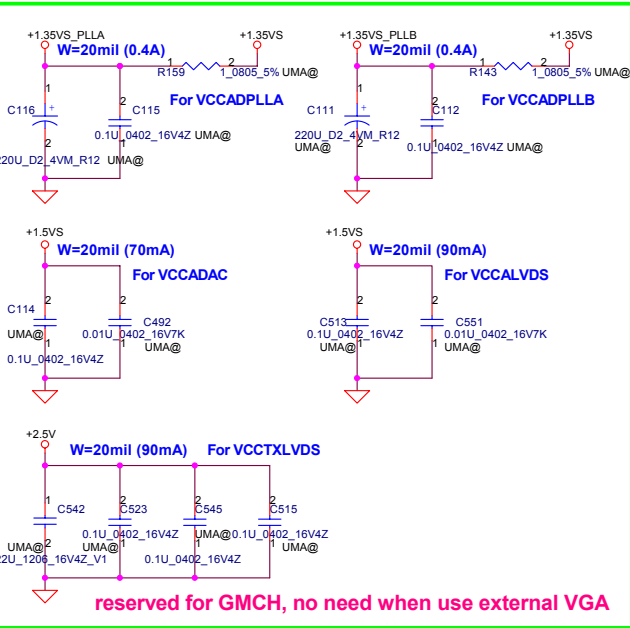
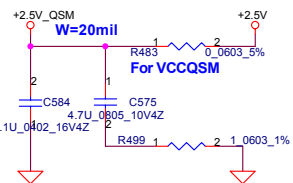
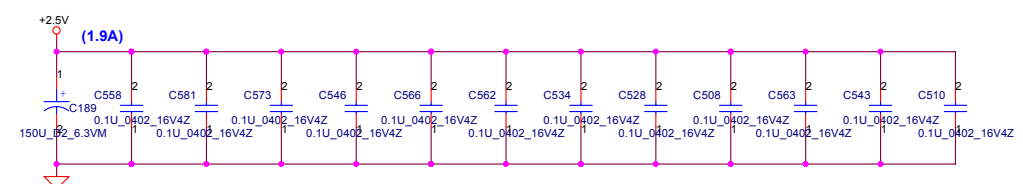
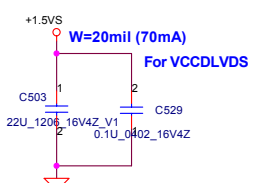
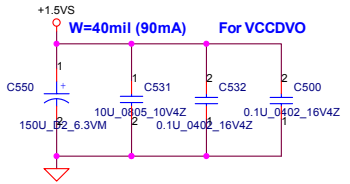
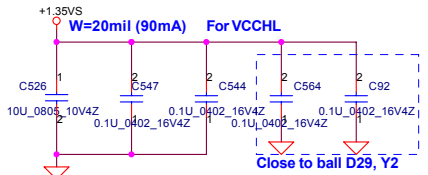
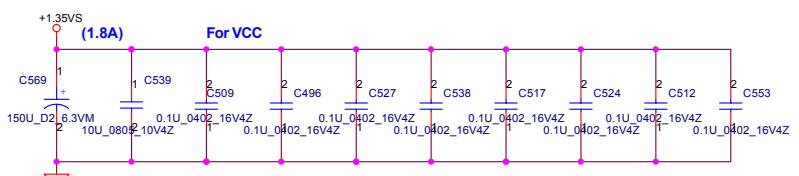
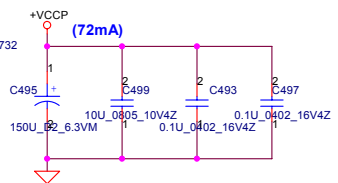
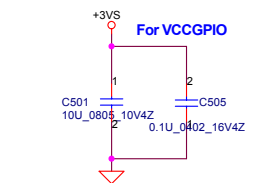
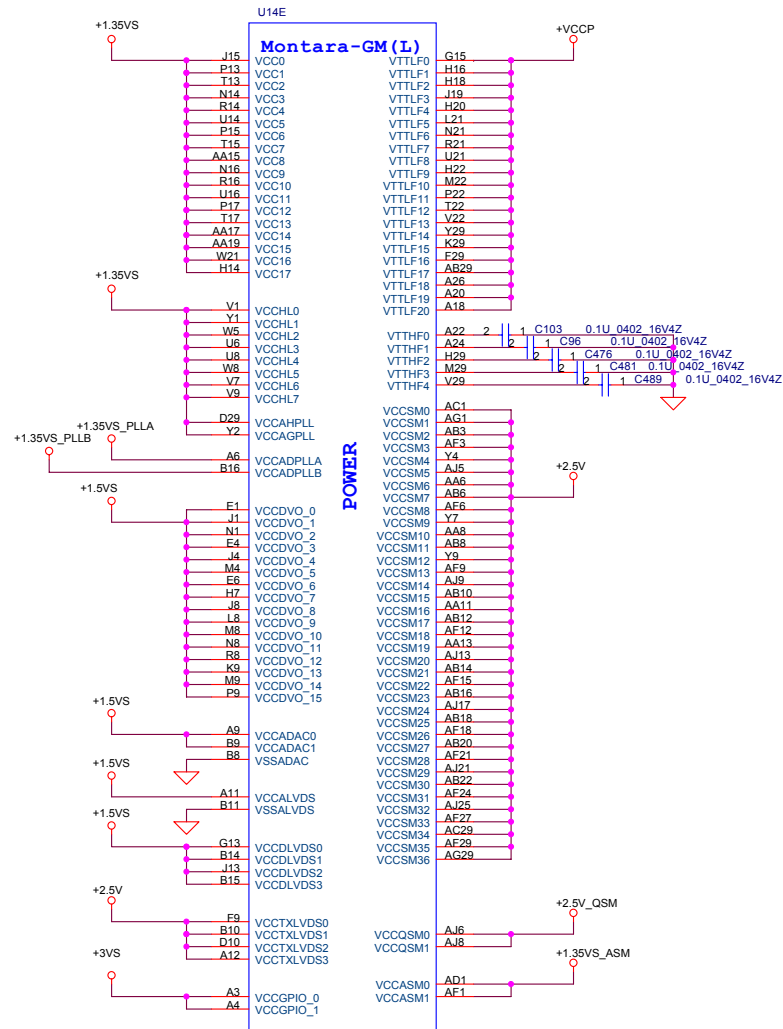


DDR REF & SWING VOLTAGE

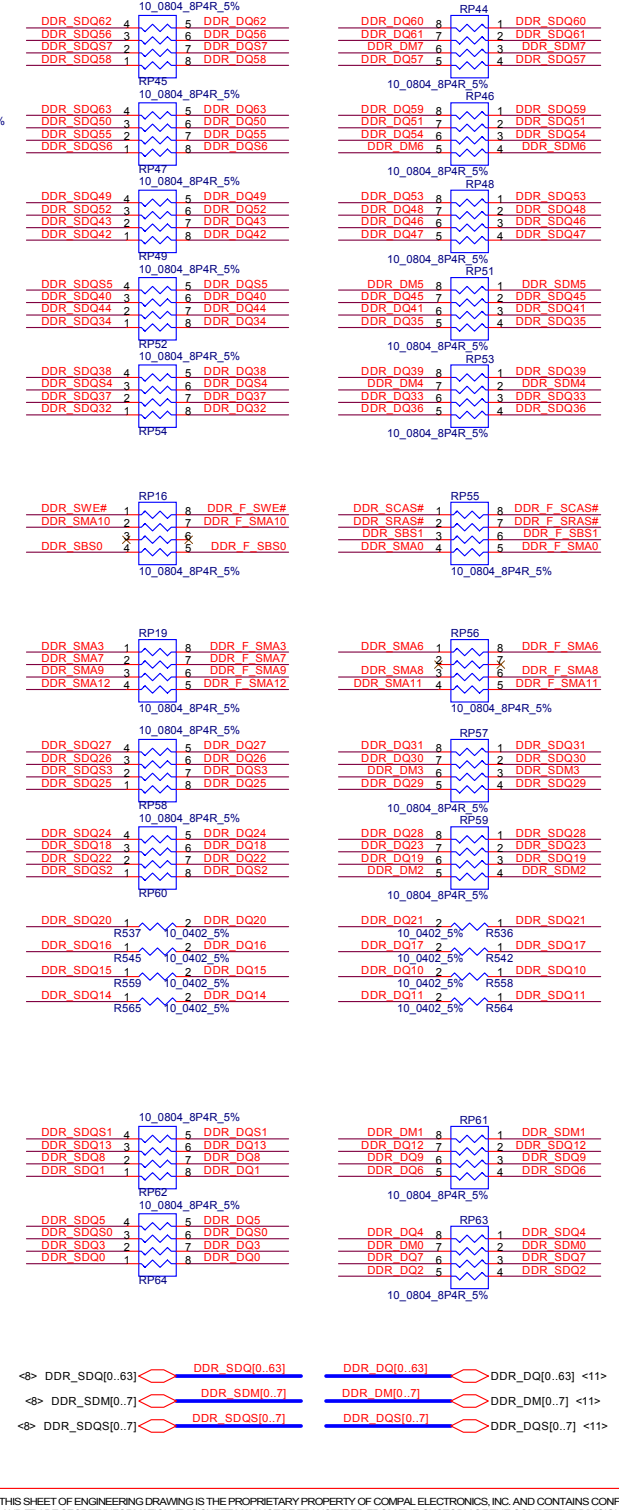
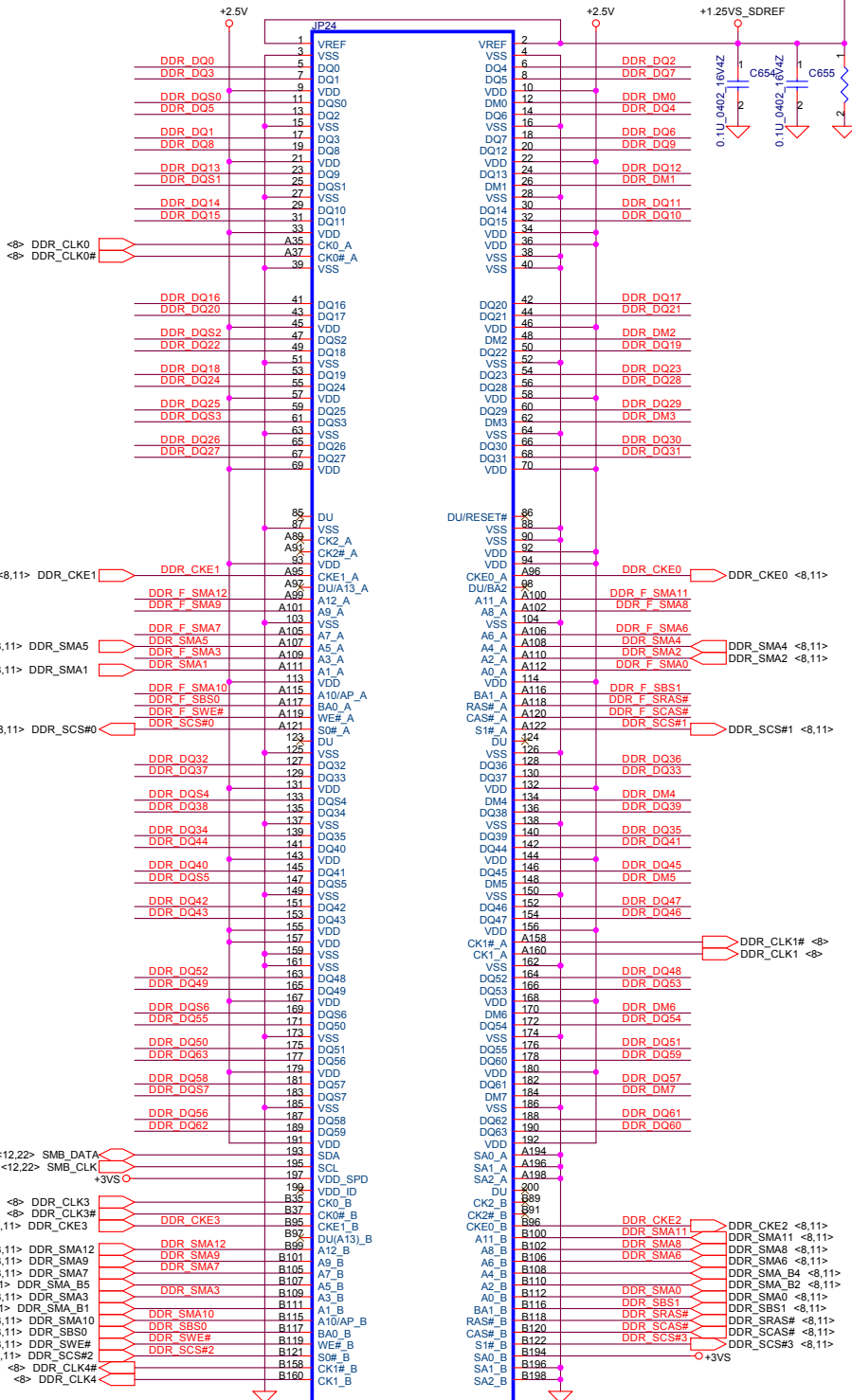
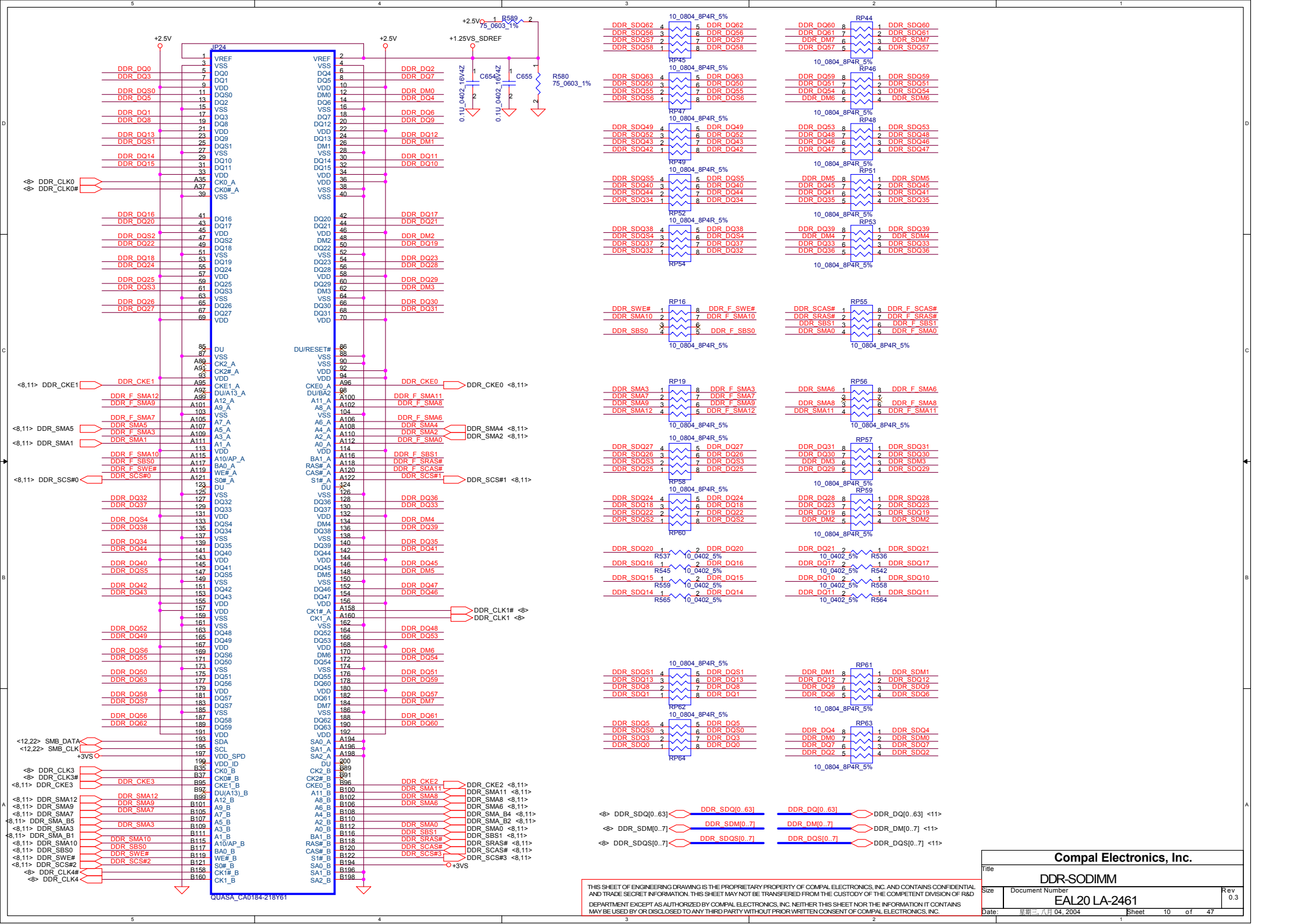


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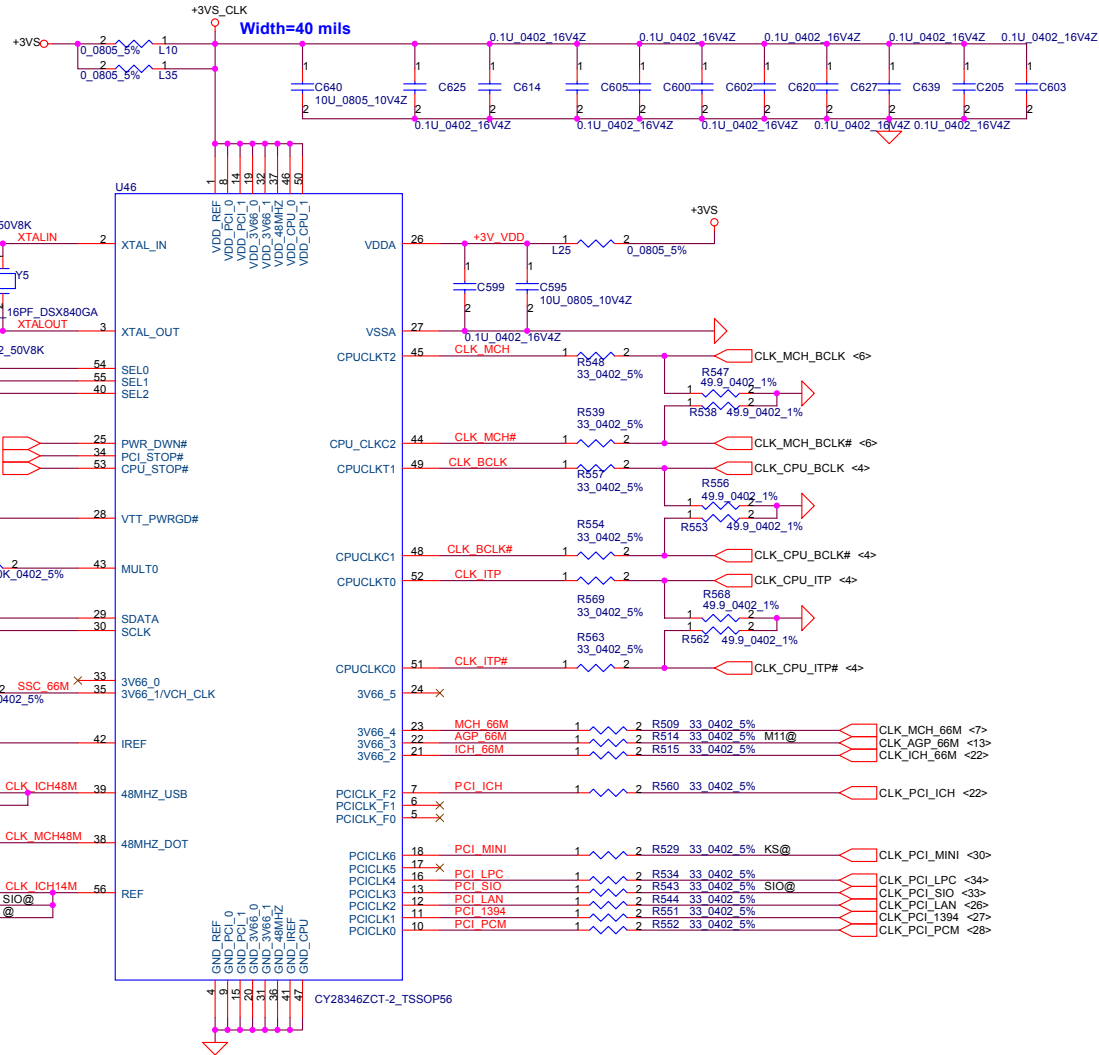


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Clock Generator

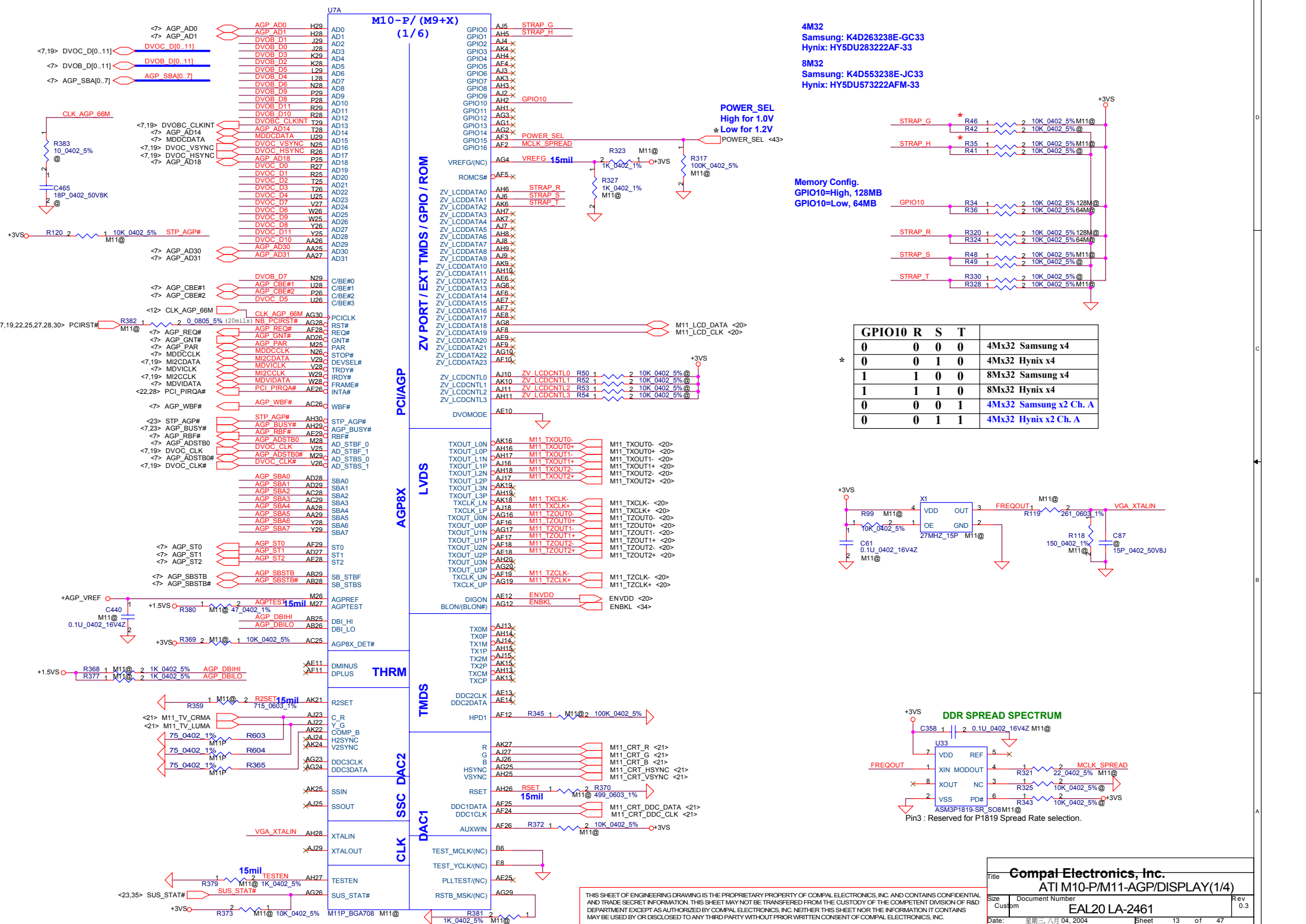
SEL2	SEL1	SEL0	CPUCLK0[0..2]	CPUCLKT[0..2]
0	0	0	166.67	166.67
0	0	1	100.00	100.00 *
0	1	0	200.00	200.00
0	1	1	133.33	133.33



if pull high to +VCCP
Change to DTC124EK

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Clock Generator		
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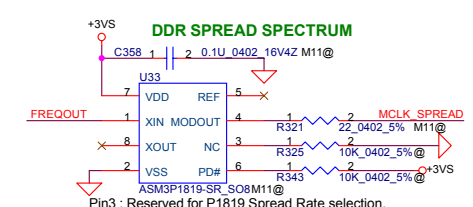
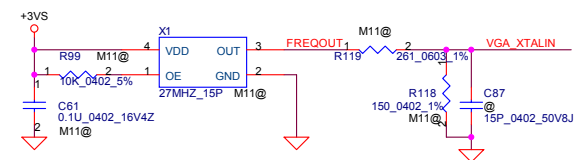


4M32
 Samsung: K4D263238E-GC33
 Hynix: HY5DU283222AF-33





8M32
 Samsung: K4D553238E-JC33
 Hynix: HY5DU73222AFM-33





Memory Config.
 GPIO10=High, 128MB
 GPIO10=Low, 64MB

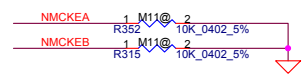
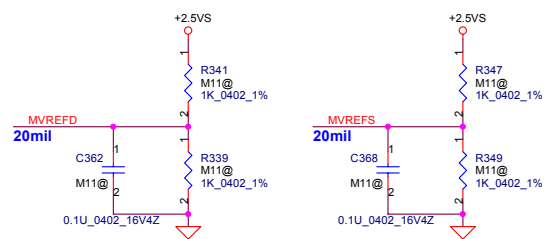
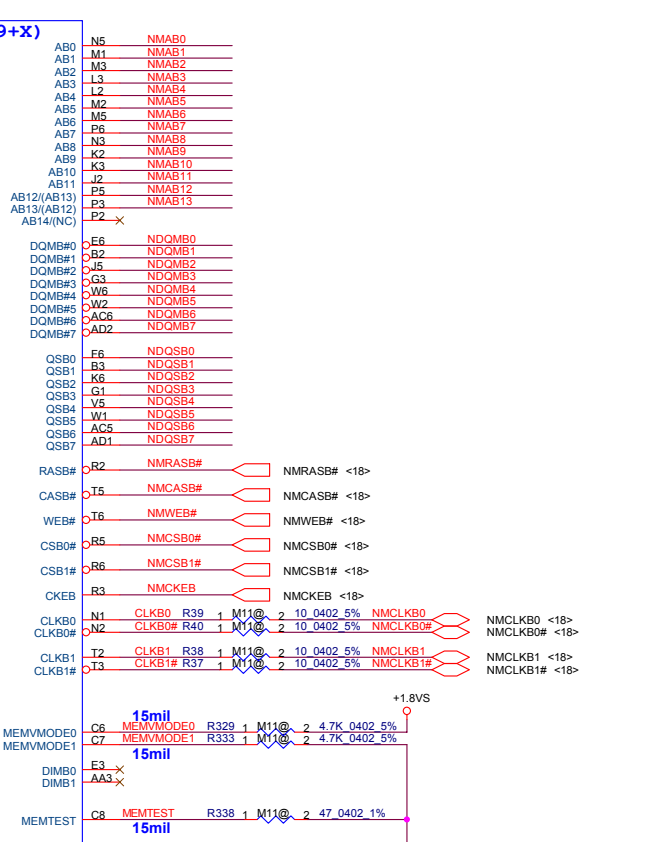
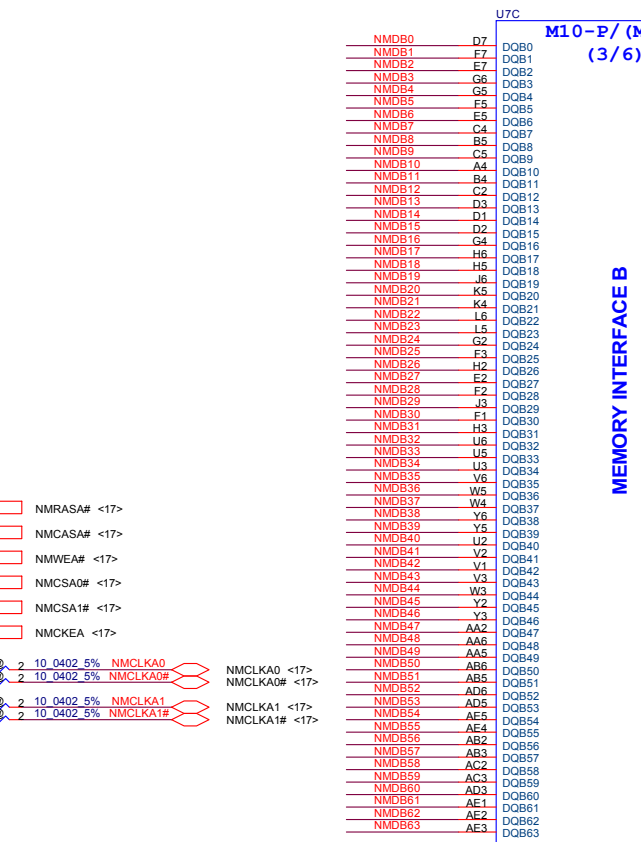
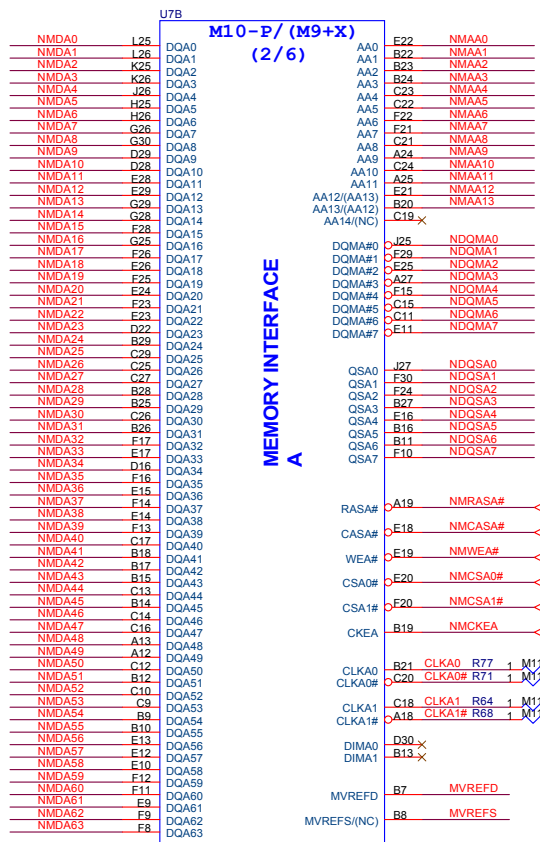
GPIO10	R	S	T	
0	0	0	0	4Mx32 Samsung x4
0	0	1	0	4Mx32 Hynix x4
1	1	0	0	8Mx32 Samsung x4
1	1	1	0	8Mx32 Hynix x4
0	0	0	1	4Mx32 Samsung x2 Ch. A
0	0	1	1	4Mx32 Hynix x2 Ch. A



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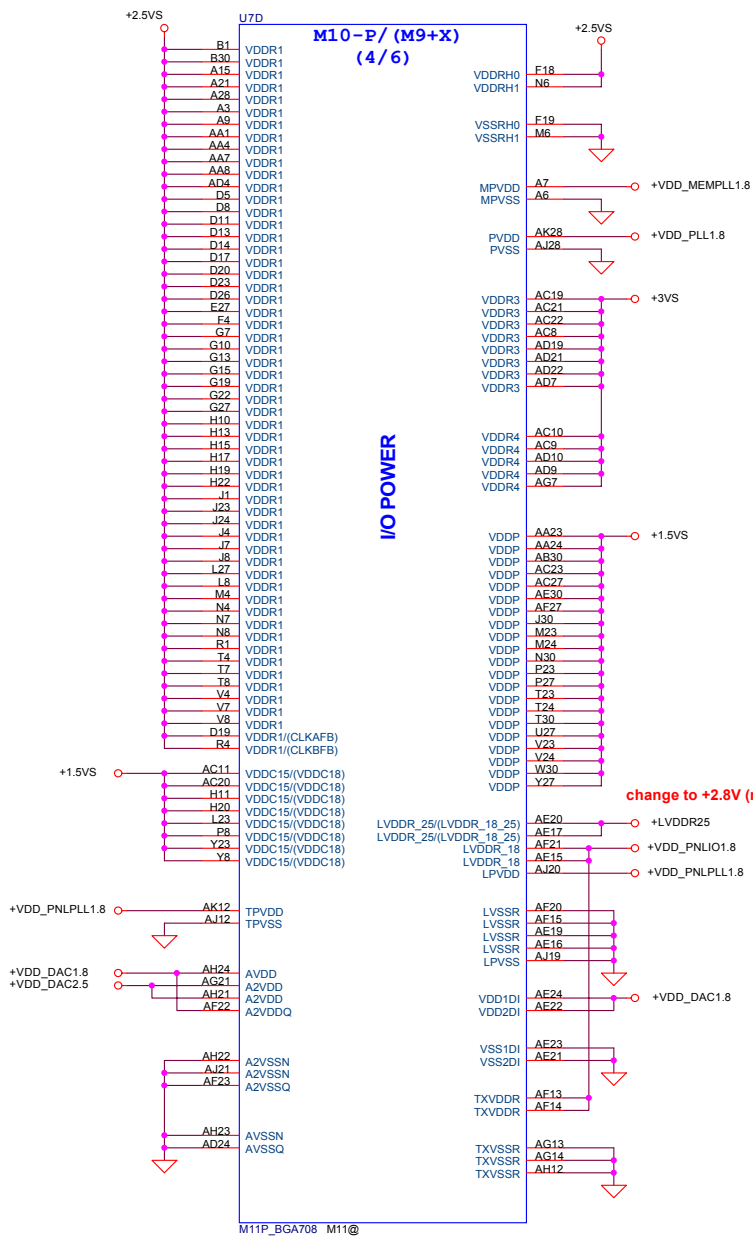


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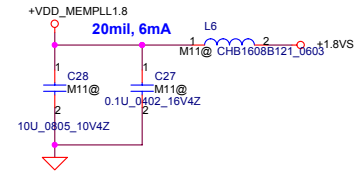
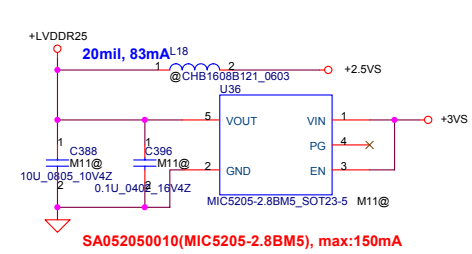
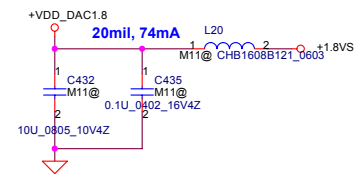
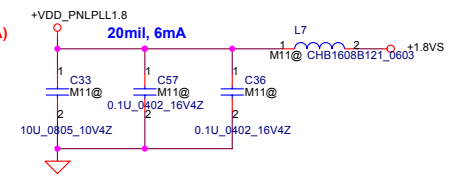
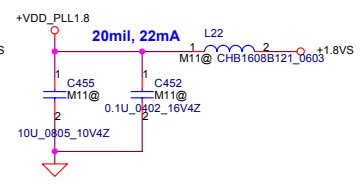
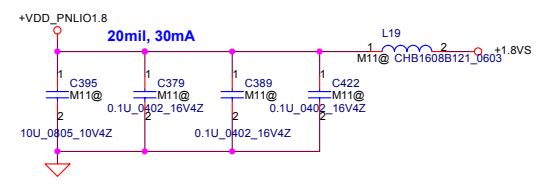
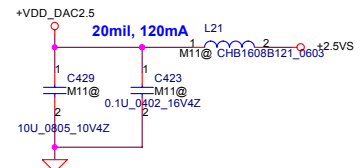
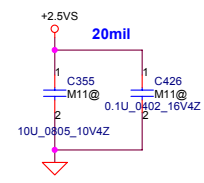
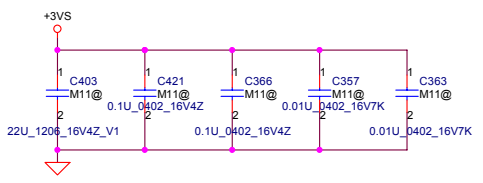
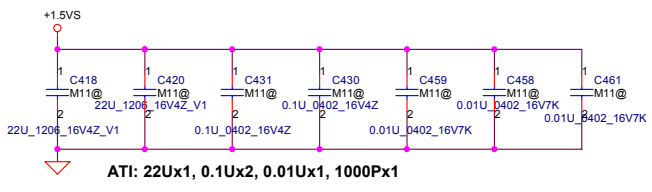
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Date: 星期二, 八月 04, 2004	Sheet: 14	of 47

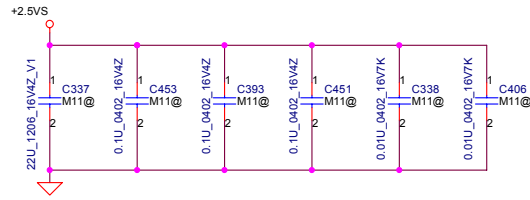
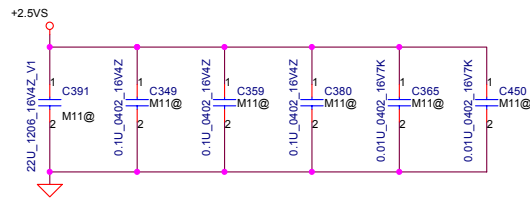
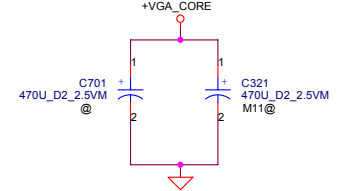
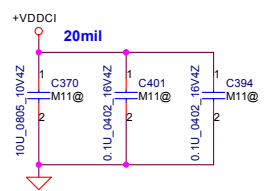
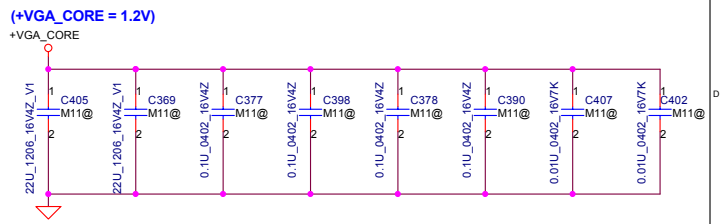
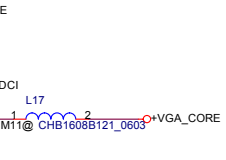
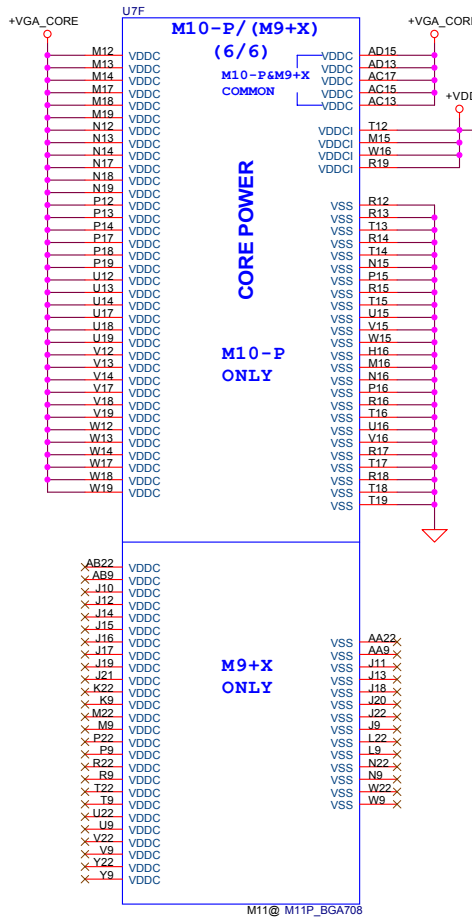
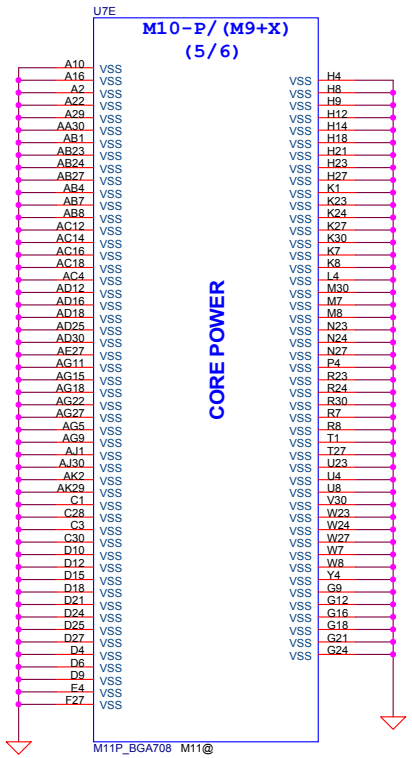
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IO POWER



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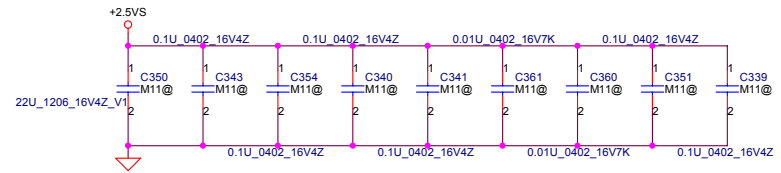
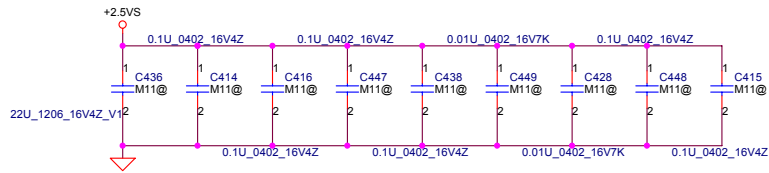
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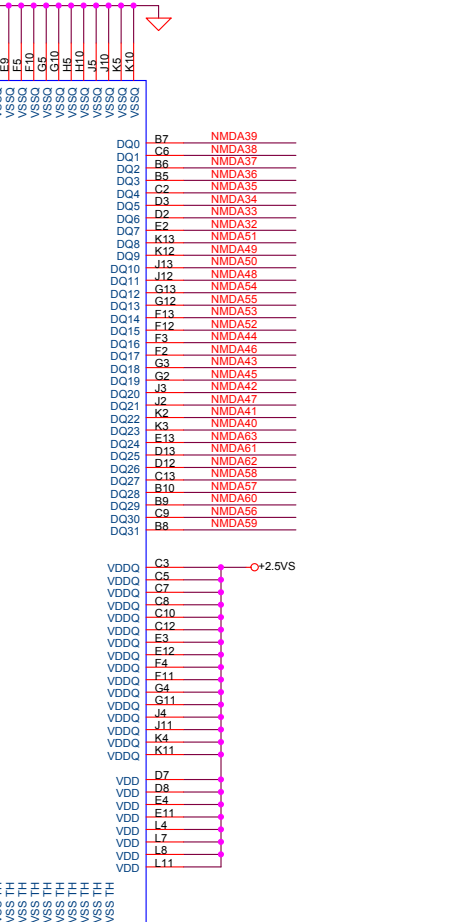
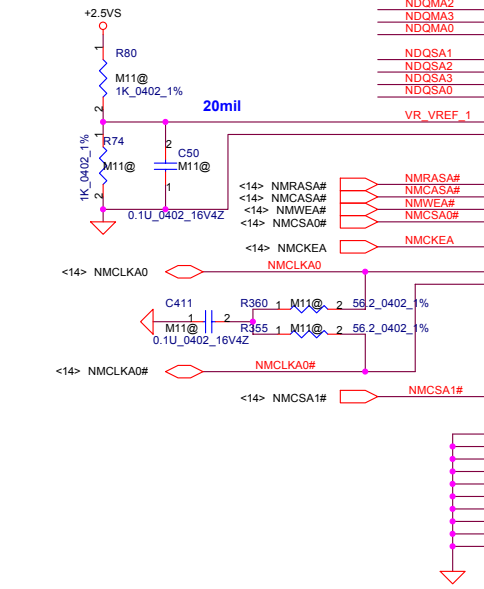
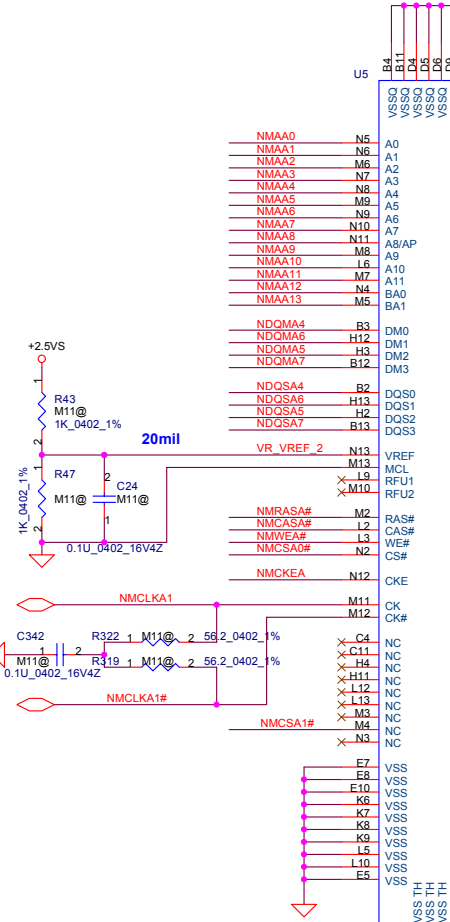
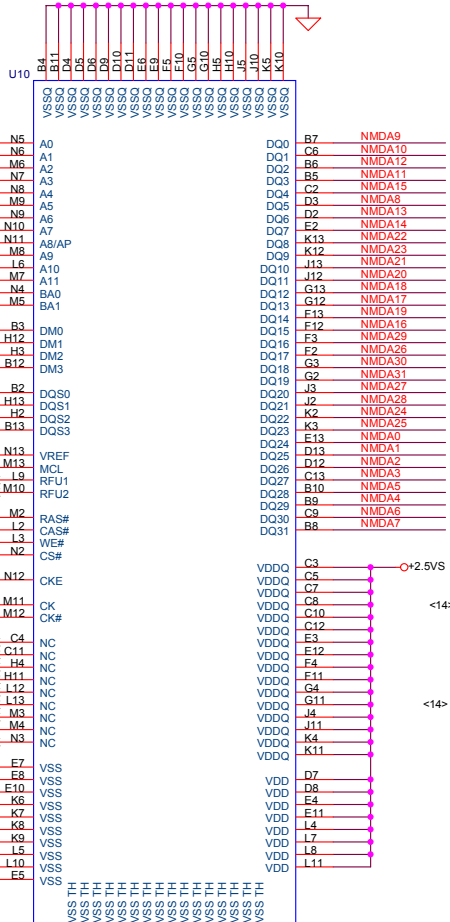
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Date: 星期二, 八月 04, 2004 Sheet: 16 of 47

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- <14> NMDA[0..63] NMDA[0..63]
- <14> NMAA[0..13] NMAA[0..13]
- <14> NDQMA[0..7] NDQMA[0..7]
- <14> NDQSA[0..7] NDQSA[0..7]



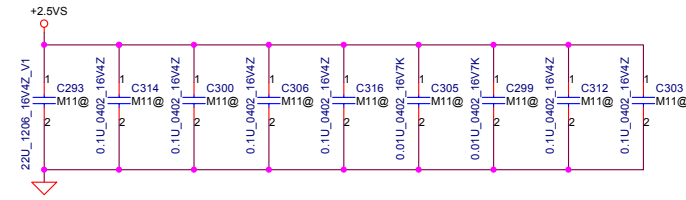
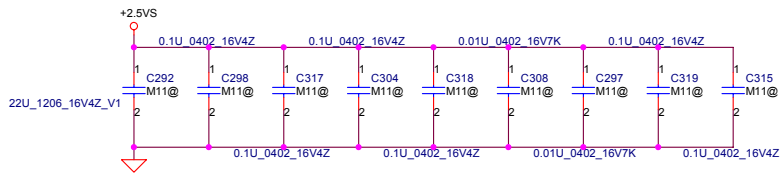
Compal Electronics, Inc.

VGA DDR CHANNEL A

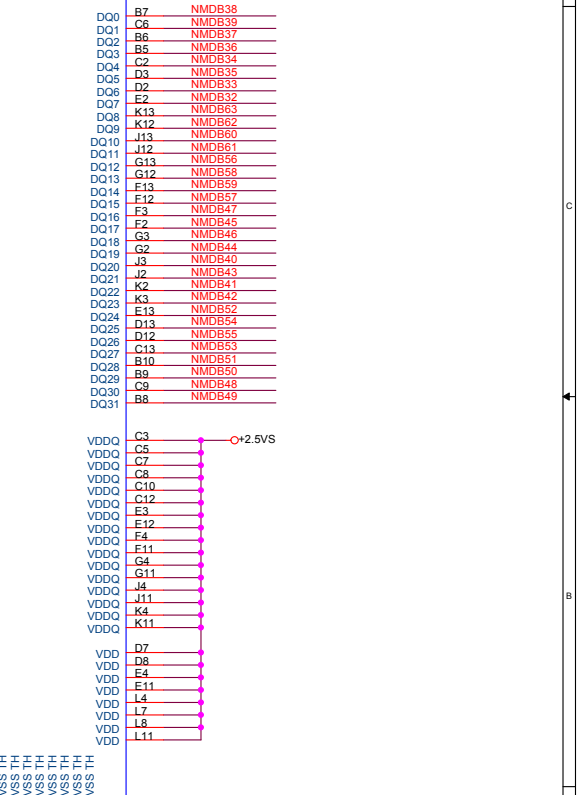
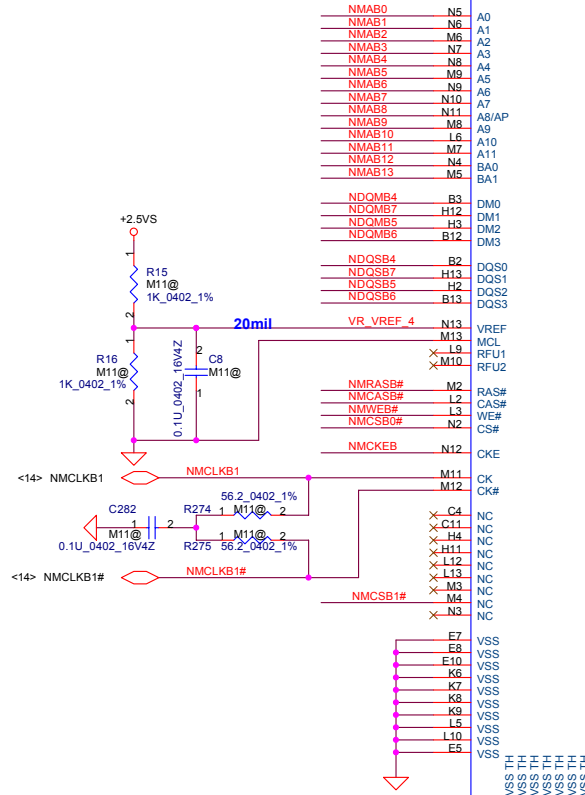
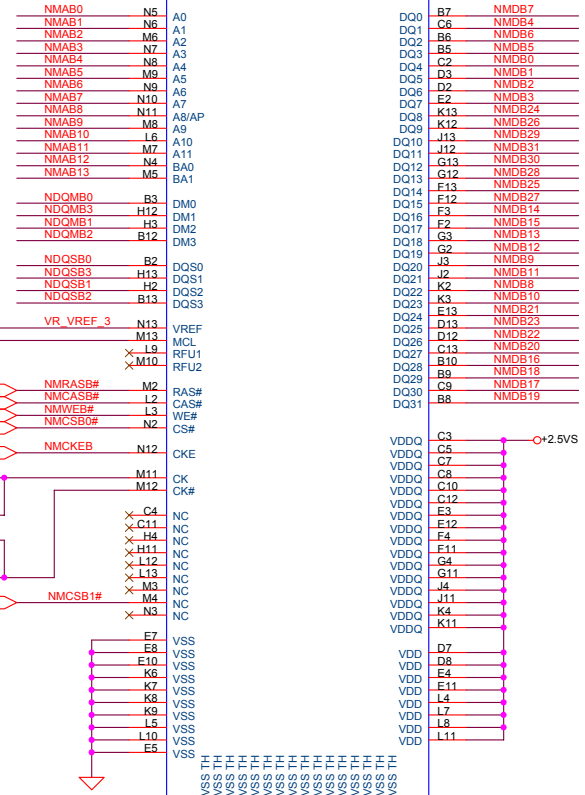
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Date: 星期二, 八月 04, 2004 Sheet: 17 of 47

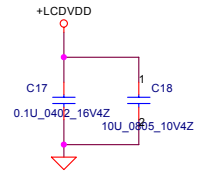
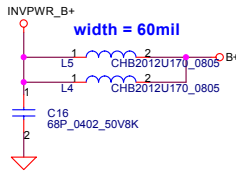
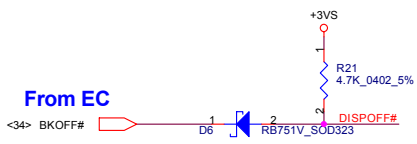
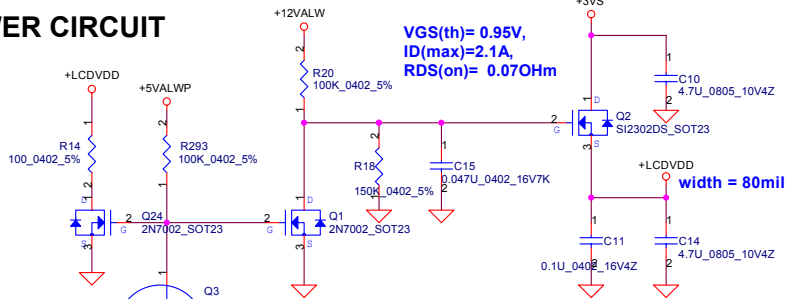
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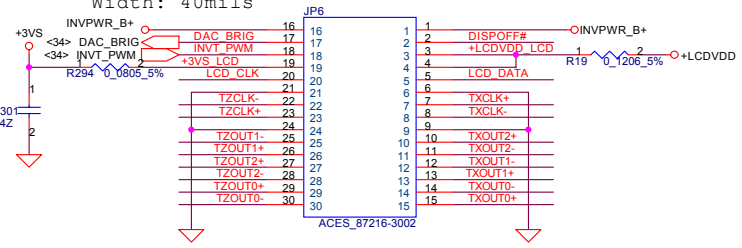


LCD POWER CIRCUIT



LCD CONN.

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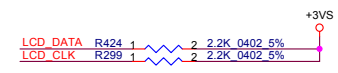


For ATI M11P

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<-13> M11_TZOUT0-	M11_TZOUT0-	R24	1	M11@	2	0	0402	5%	TZOUT0-
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<-13> M11_TZCLK+	M11_TZCLK+	R30	1	M11@	2	0	0402	5%	TZCLK+
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For GMCH

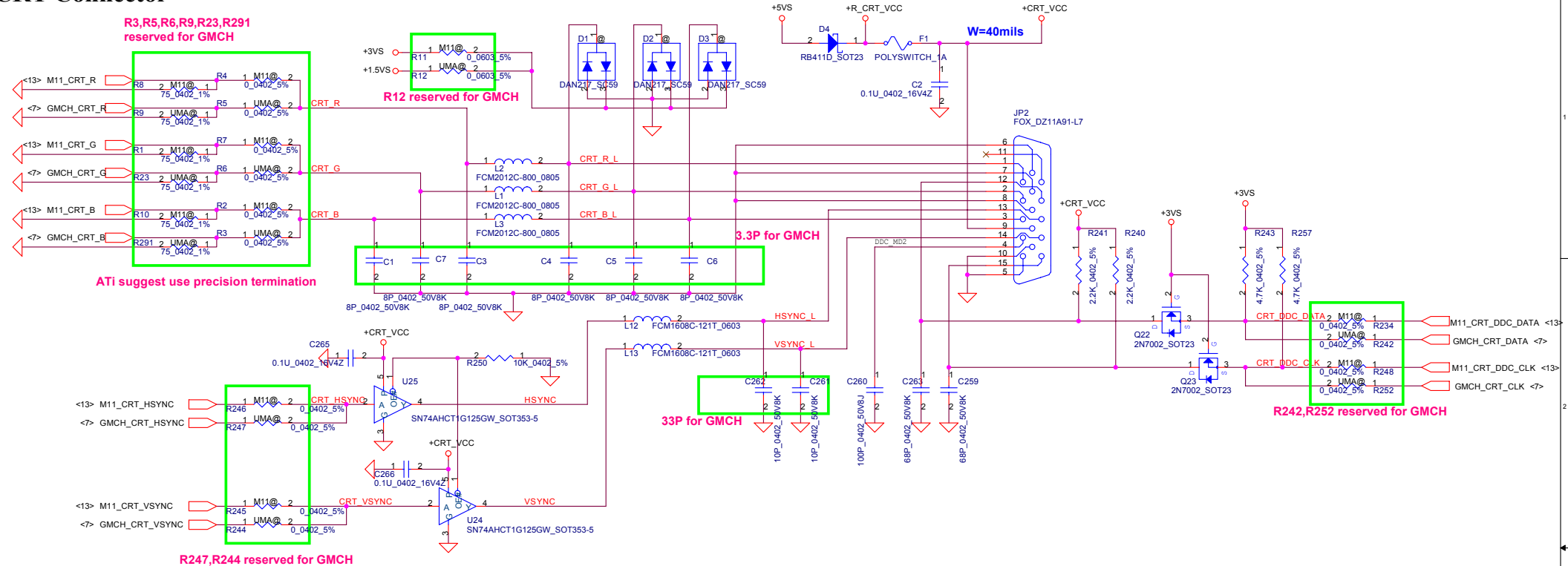
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<-7> GMCH_TXOUT1-	GMCH_TXOUT1-	R287	1	UMA@	2	0	0402	5%	TXOUT1-
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<-7> GMCH_TZCLK-	GMCH_TZCLK-	R302	1	UMA@	2	0	0402	5%	TZCLK-
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<-7> GMCH_LCD_DATA	GMCH_LCD_DATA	R282	1	UMA@	2	0	0402	5%	LCD_DATA
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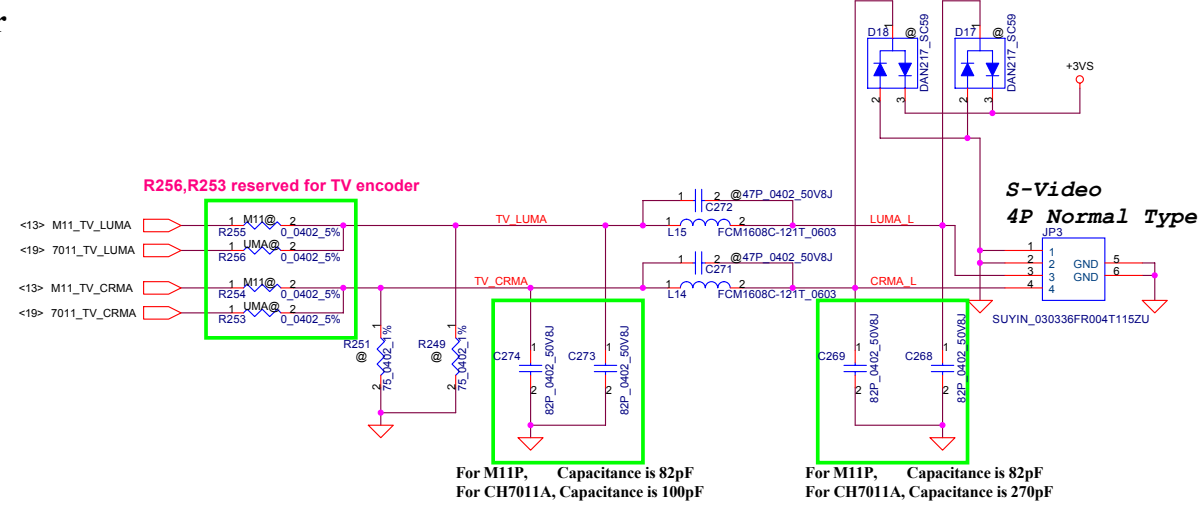
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LCD CONN		
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CRT Connector

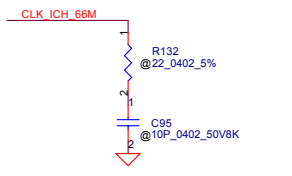
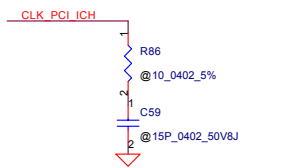


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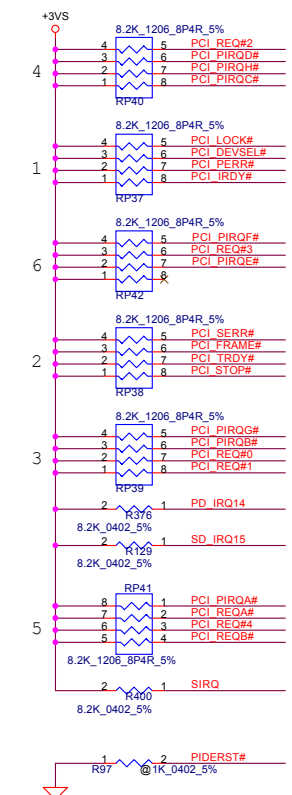


Compal Electronics, Inc.			
Title: CRT & TV-OUT Connector			
Size	Document Number	Rev 0.3	
EAL20 LA-2461		Date:	Rev 0.3
Date: 星期二, 八月 04, 2004		Sheet	21 of 47

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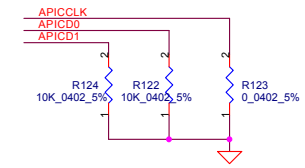
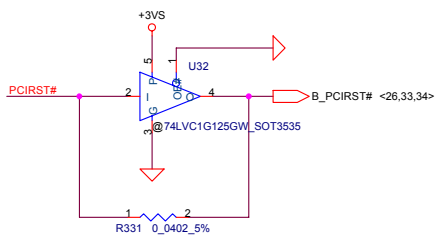
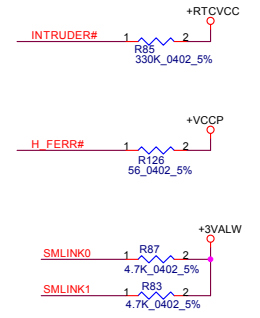
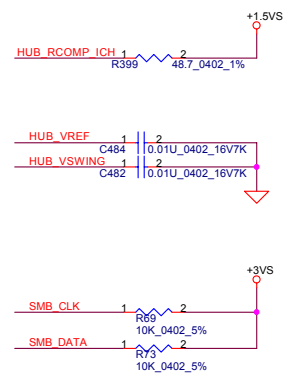
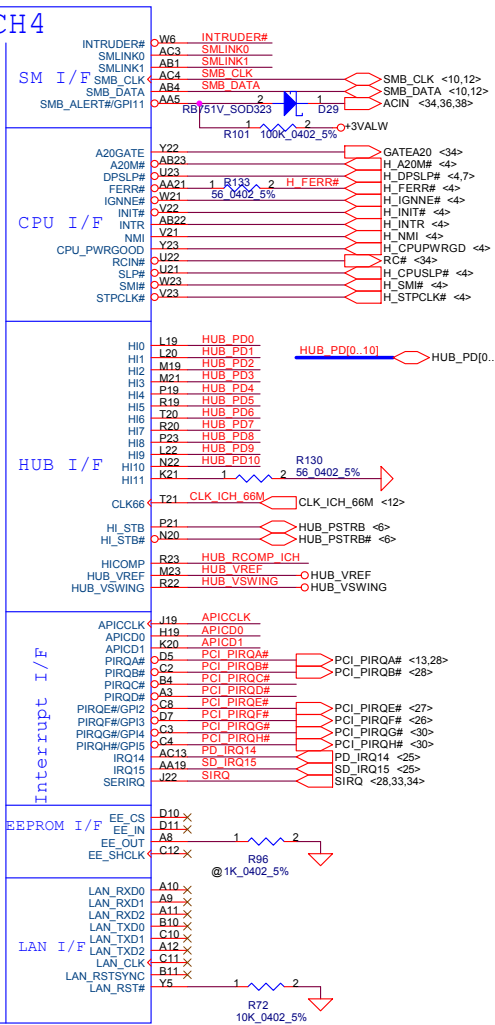
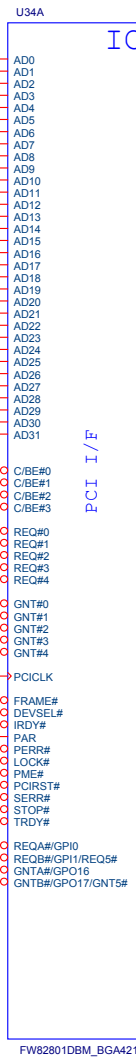
PCI Pullups



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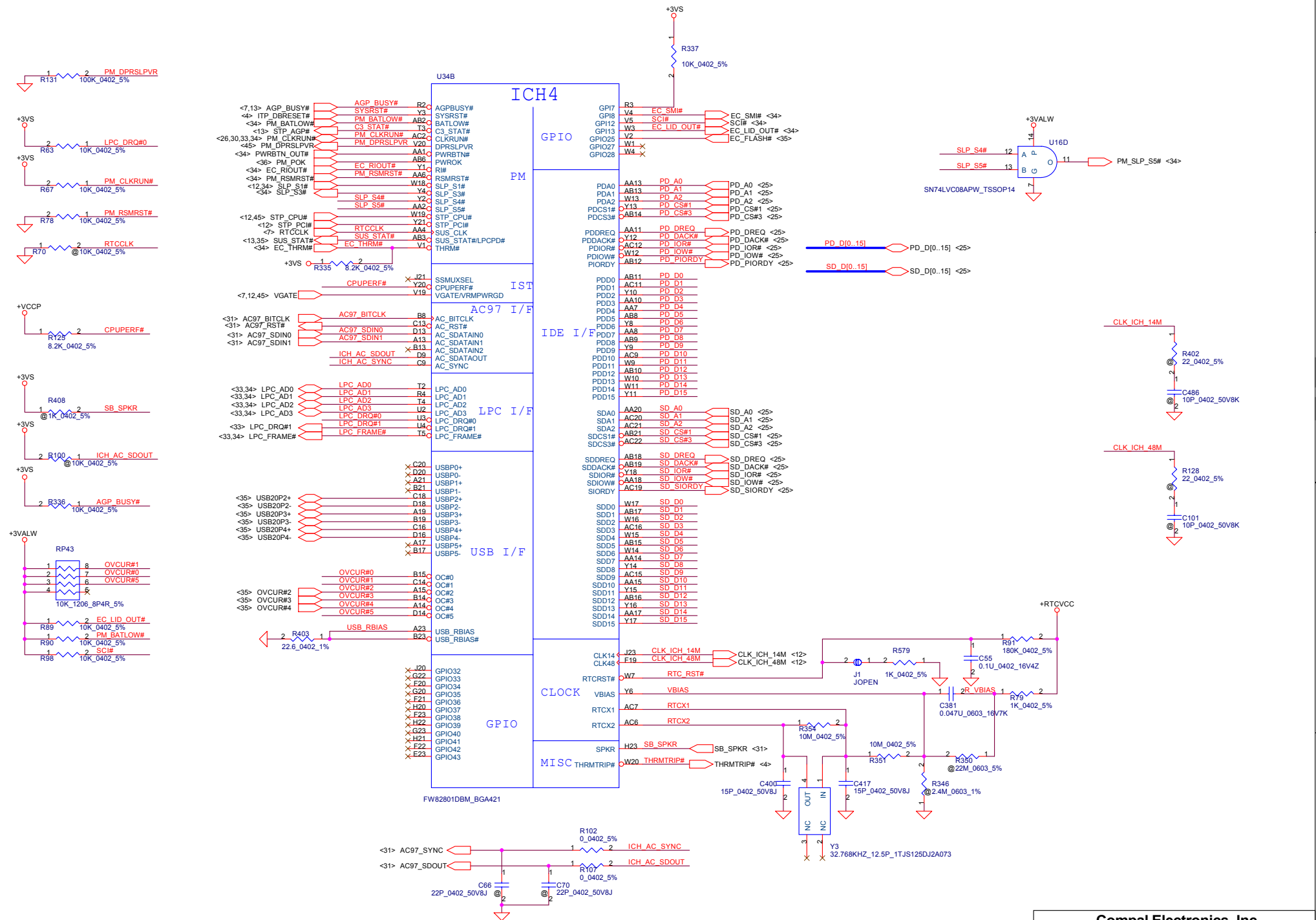
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- PCI_AD1 J3 AD1
- PCI_AD2 H3 AD2
- PCI_AD3 K1 AD3
- PCI_AD4 G5 AD4
- PCI_AD5 H4 AD5
- PCI_AD6 H4 AD6
- PCI_AD7 J5 AD7
- PCI_AD8 K2 AD8
- PCI_AD9 G2 AD9
- PCI_AD10 L1 AD10
- PCI_AD11 G4 AD11
- PCI_AD12 L2 AD12
- PCI_AD13 H2 AD13
- PCI_AD14 L3 AD14
- PCI_AD15 F5 AD14
- PCI_AD16 F4 AD15
- PCI_AD17 N1 AD17
- PCI_AD18 E5 AD18
- PCI_AD19 E5 AD19
- PCI_AD20 E3 AD20
- PCI_AD21 N3 AD21
- PCI_AD22 E4 AD22
- PCI_AD23 M5 AD23
- PCI_AD24 E2 AD24
- PCI_AD25 P1 AD25
- PCI_AD26 L1 AD26
- PCI_AD27 P2 AD27
- PCI_AD28 D3 AD28
- PCI_AD29 R1 AD29
- PCI_AD30 D2 AD30
- PCI_AD31 P4 AD31

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- <26,27,28,30> PCI_CBE#1 PCI_CBE#1 C/BE#1
- <26,27,28,30> PCI_CBE#2 PCI_CBE#2 C/BE#2
- <26,27,28,30> PCI_CBE#3 PCI_CBE#3 C/BE#3
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- <26,27,28,30> PCI_PAR PCI_PAR PAR
- <26,27,28,30> PCI_PERR# PCI_PERR# PERR#
- <26,27,28,30> PCI_LOCK# PCI_LOCK# LOCK#
- <7,13,19,25,27,28,30> PCIRST# PCIRST# PCIRST#
- <26,28,30> PCI_SERR# PCI_SERR# SERR#
- <26,27,28,30> PCI_STOP# PCI_STOP# STOP#
- <26,27,28,30> PCI_TRDY# PCI_TRDY# TRDY#
- PCI_REQA# REQA#/GP10
- PCI_REQB# REQB#/GP11/REQ5#
- <25> PIDERST# PIDERST#
- <25> SIDERST# SIDERST#

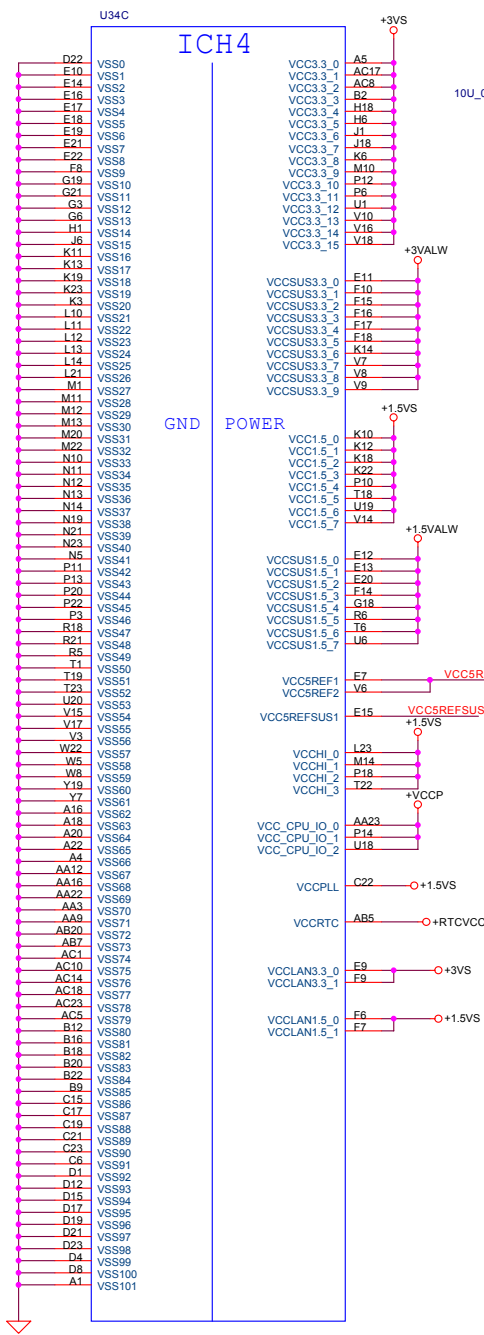


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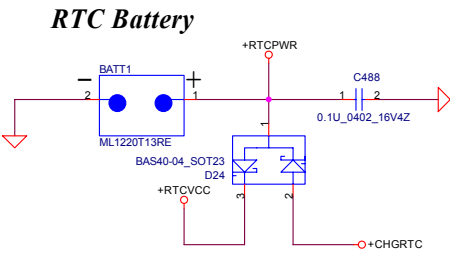
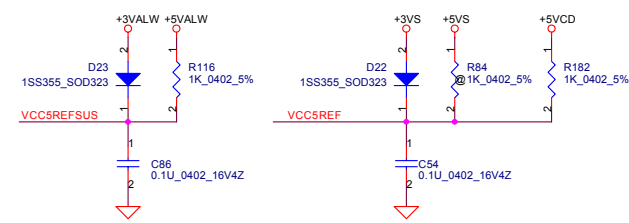
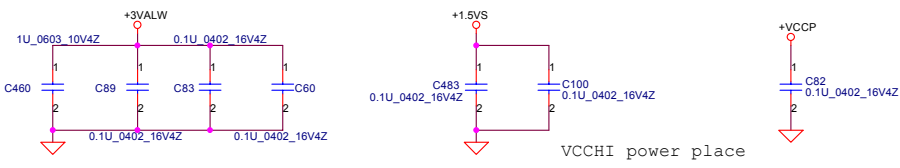
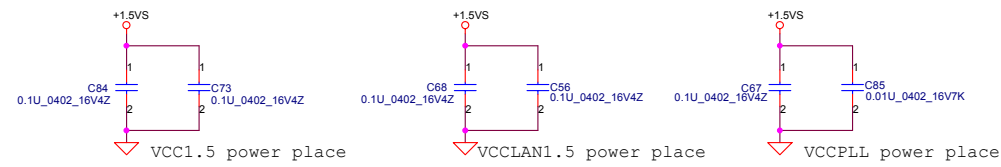
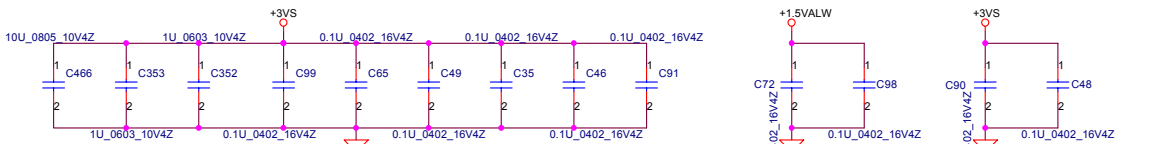
Compal Electronics, Inc.	
Title ICH4-M(1/3) PCI/HUB/CPU/INT	
Size	Document Number
EAL20 LA-2461	
Date: 星期二, 八月 04, 2004	Sheet 22 of 47
Rev 0.3	



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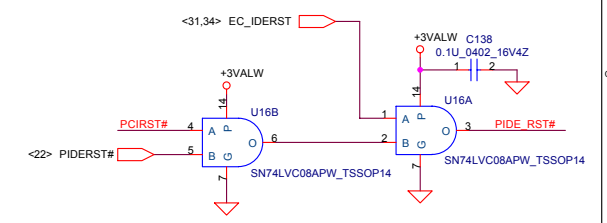
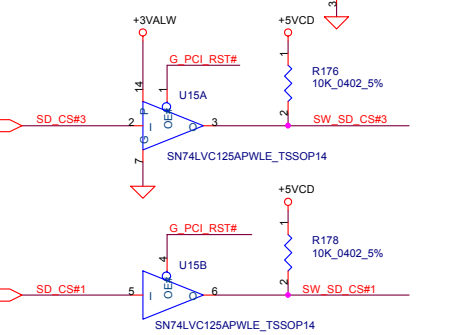
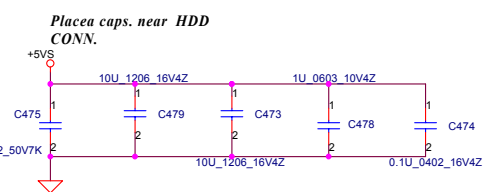
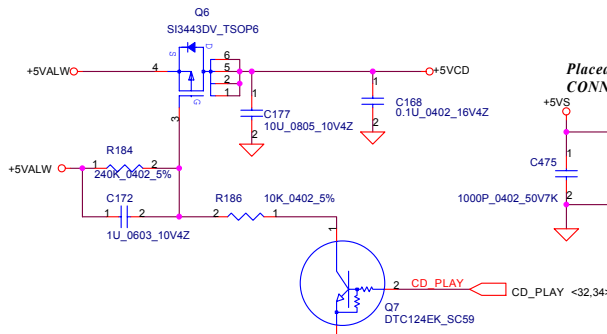
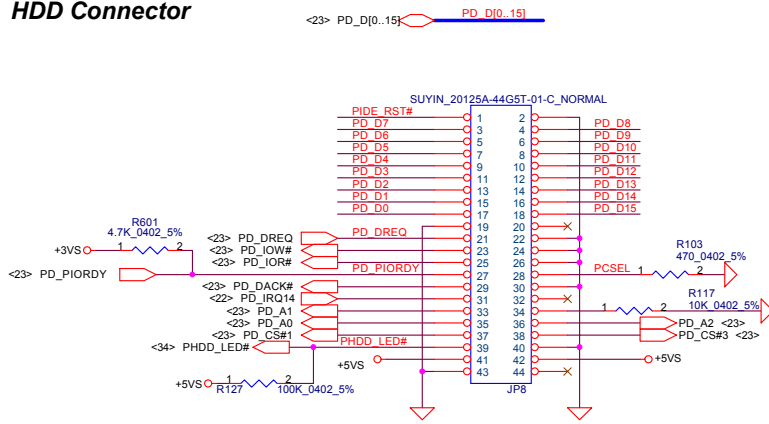
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Compal Electronics, Inc.		
Title ICH4-M(3/3) PWR/GND		
Size	Document Number	Rev
	EAL20 LA-2461	0.3
Date:	星期二, 八月 04, 2004	Sheet 24 of 47

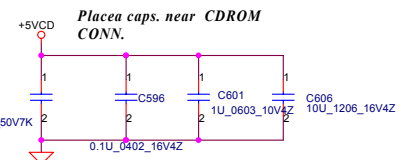
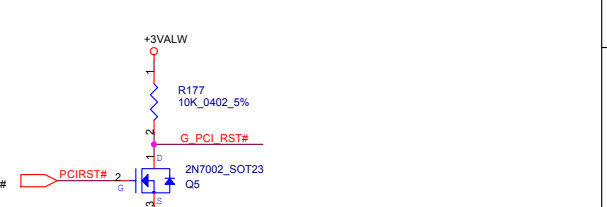
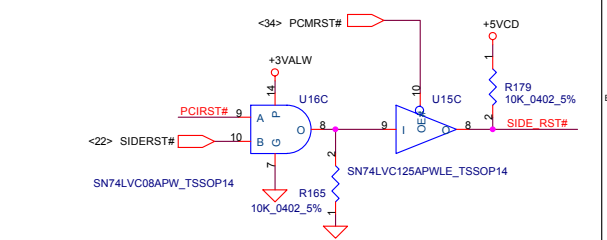
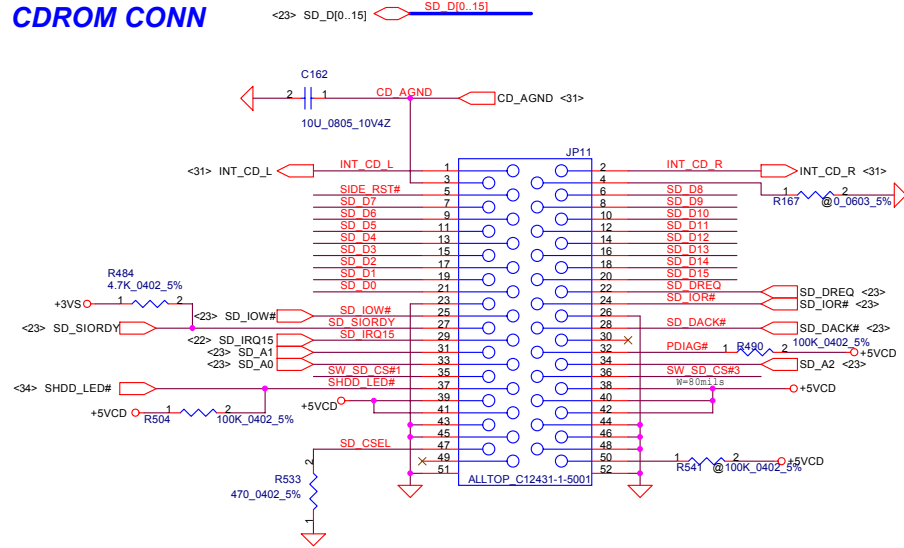
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HDD Connector



This is reverse type conn, PIDE_RST# connect to pin44.
After connector library ready,
correct connection is PIDE_RST# connect to pin1!

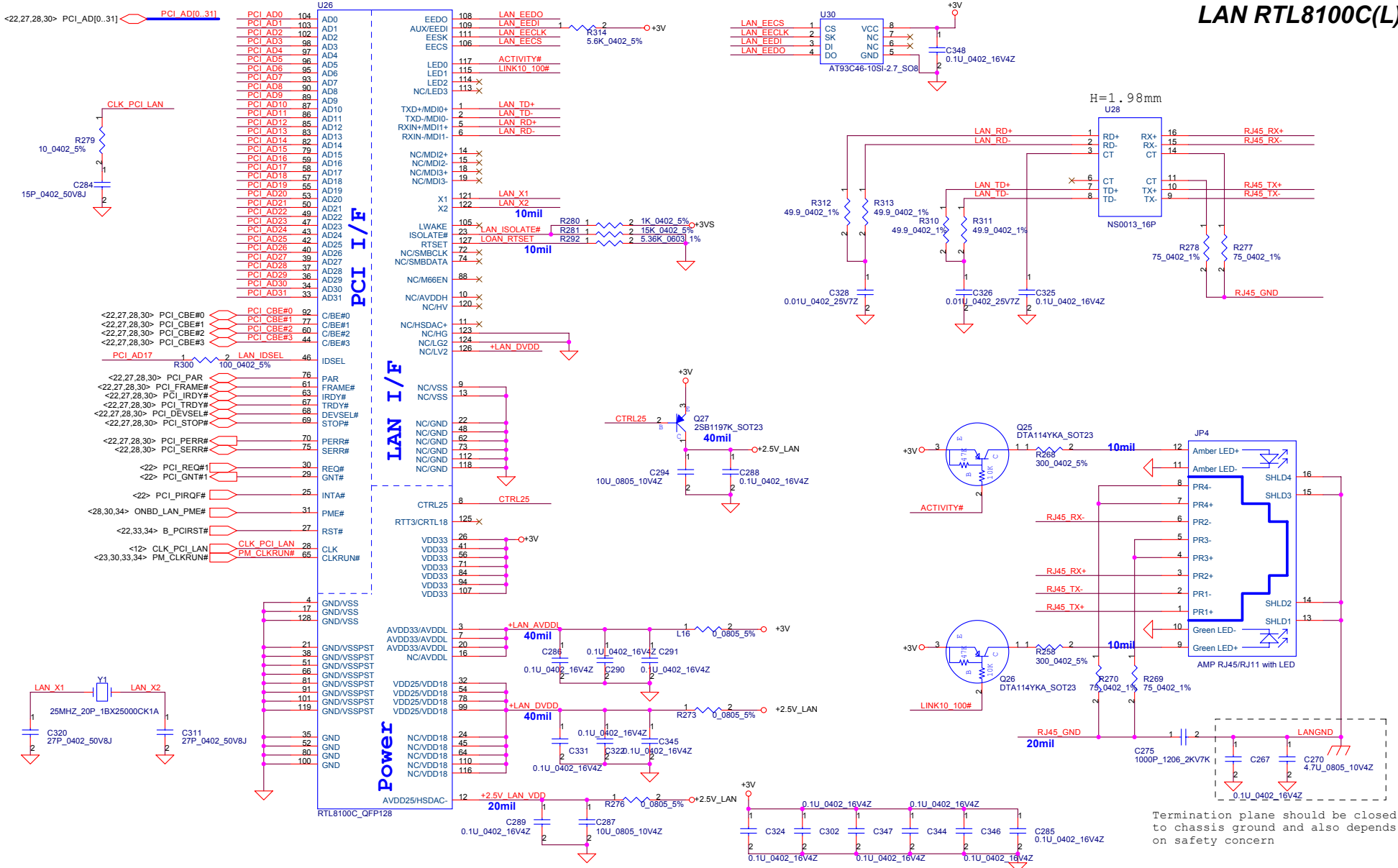
CDROM CONN



Compal Electronics, Inc.		
Title HDD & CDROM Connector & Direct CD		
Size	Document Number EAL20 LA-2461	Rev 0.3
Date:	日期: 八月 04, 2004	Sheet 25 of 47

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LAN RTL8100C(L)

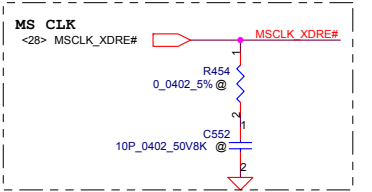
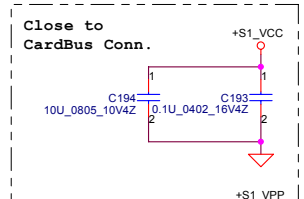
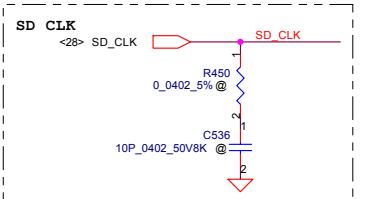
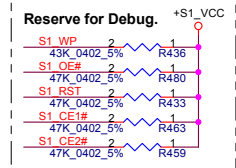
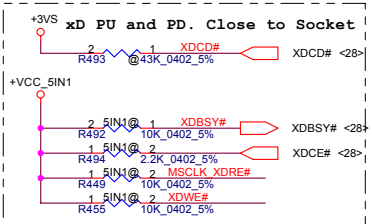
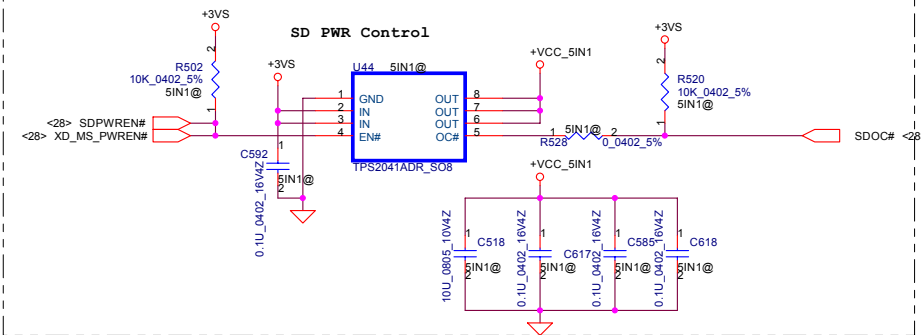
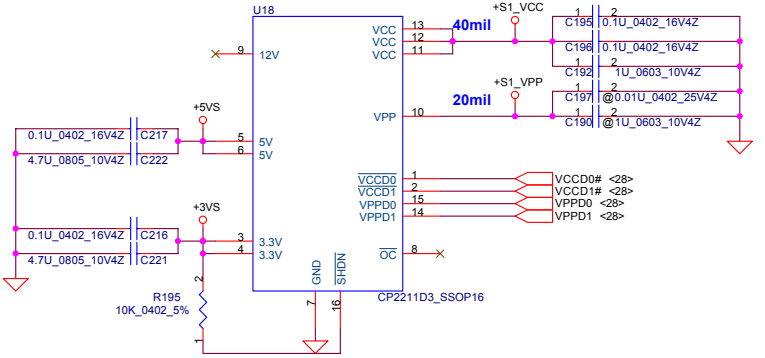


Termination plane should be closed to chassis ground and also depends on safety concern

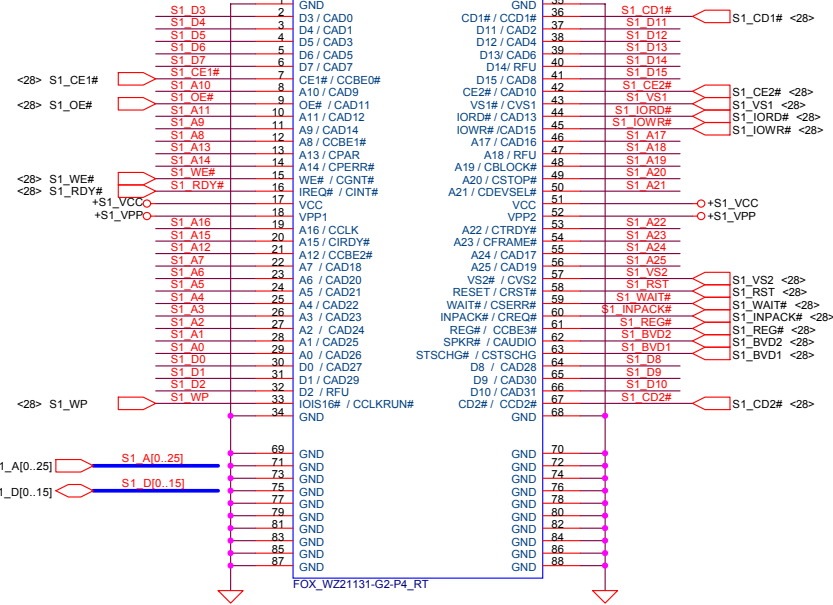
Compal Electronics, Inc.			
Title LAN RTL8100CL			
Size Custom	Document Number EAL20 LA-2461	Rev 0.3	
Date: 星期二, 八月 04, 2004	Sheet 26	of 47	

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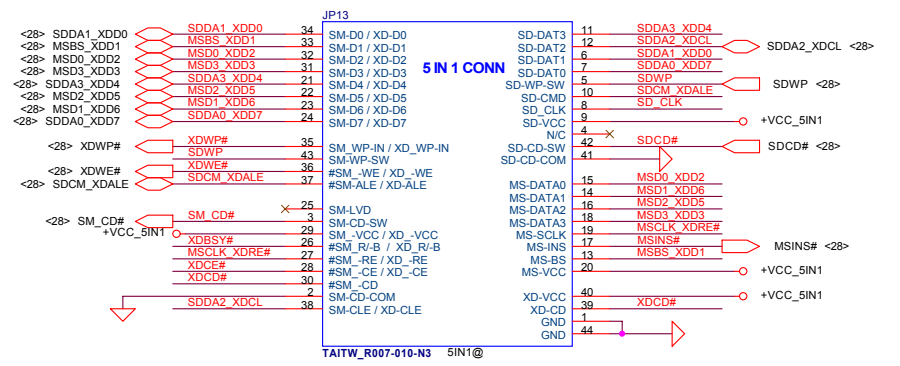
PCMCIA Power Controller



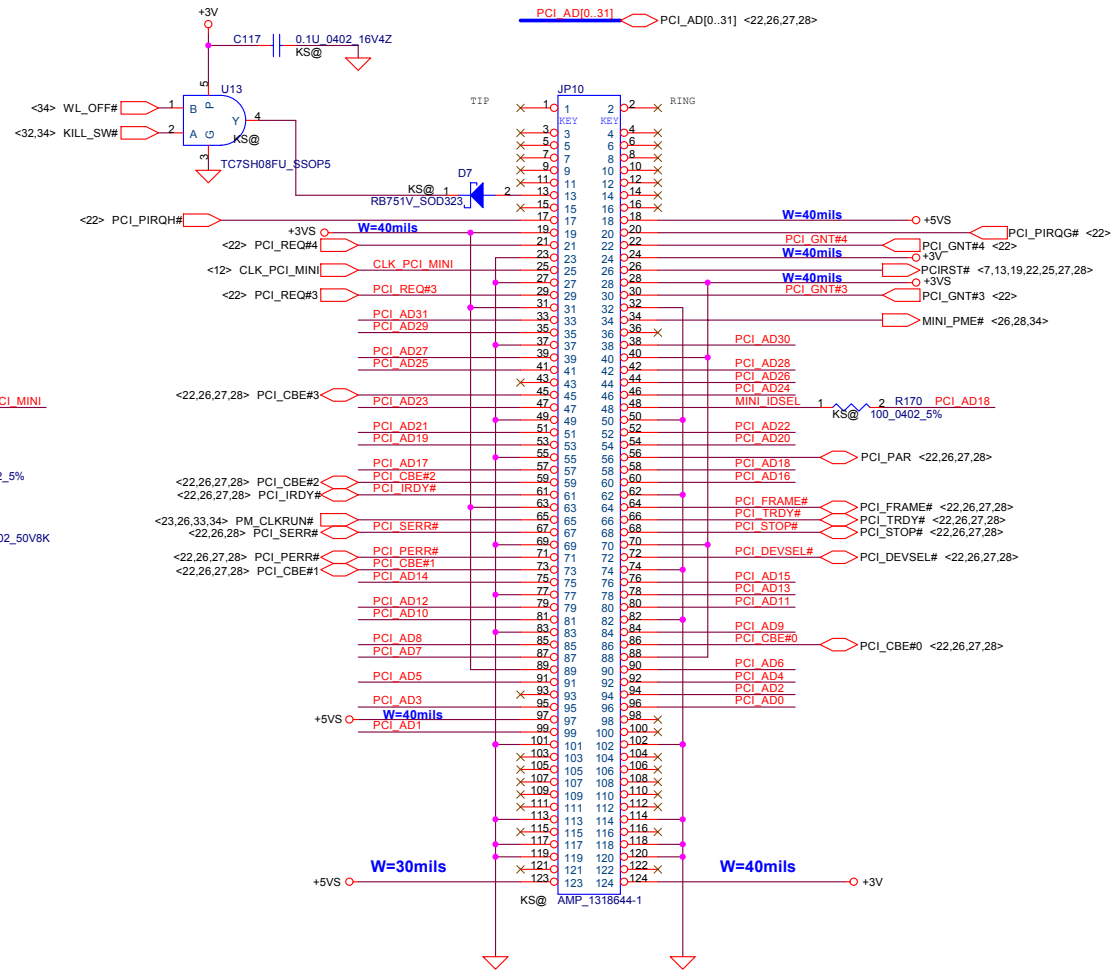
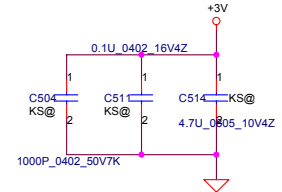
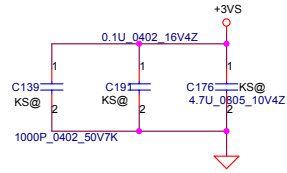
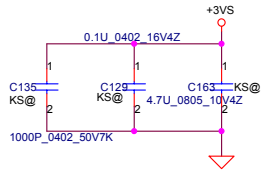
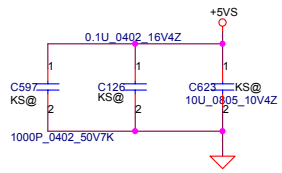
CardBus Socket



5in1 Socket



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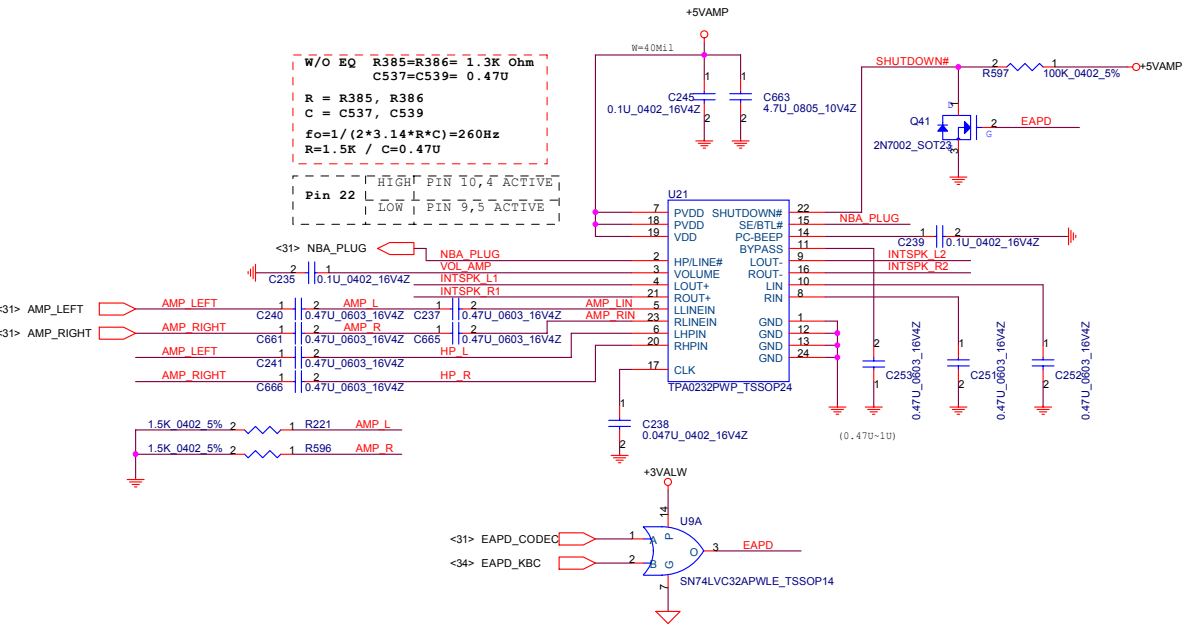
Audio AMP

W/O EQ R385=R386= 1.3K Ohm
C537=C539= 0.47U

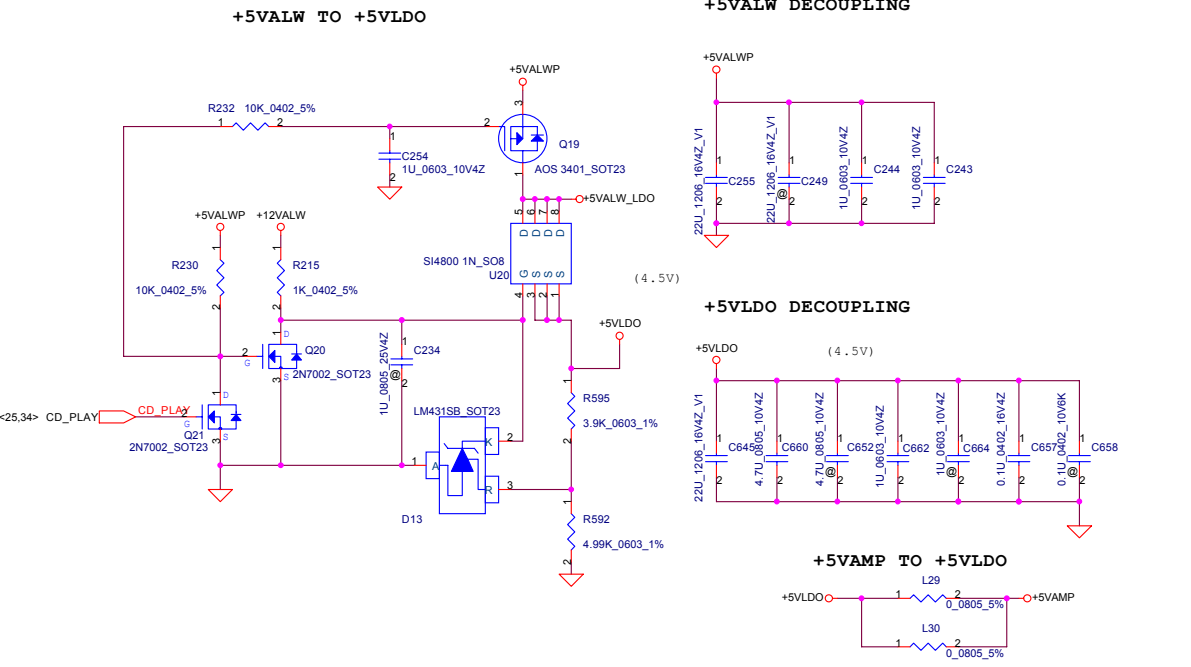
R = R385, R386
C = C537, C539

$f_o = 1 / (2 * \pi * 1.4 * R * C) = 260\text{Hz}$
R=1.5K / C=0.47U

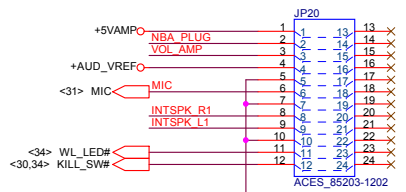
Pin 22 HIGH PIN IO, 4 ACTIVE
Pin 3,5 ACTIVE



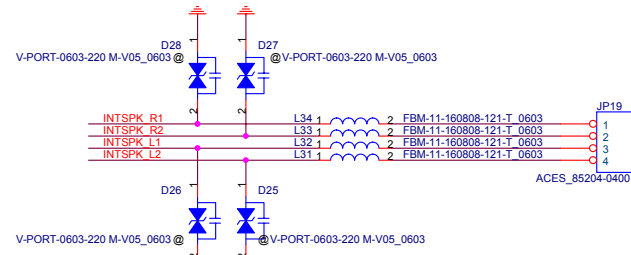
Regulator for AMP



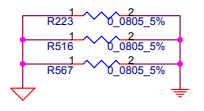
Audio Board Connector



Speaker Connector



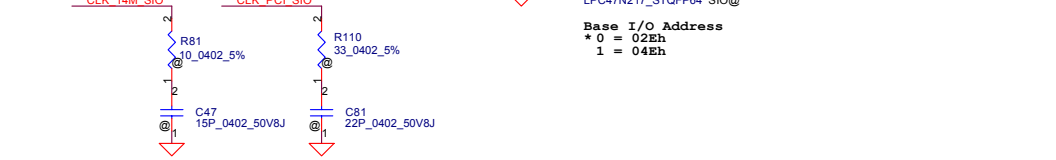
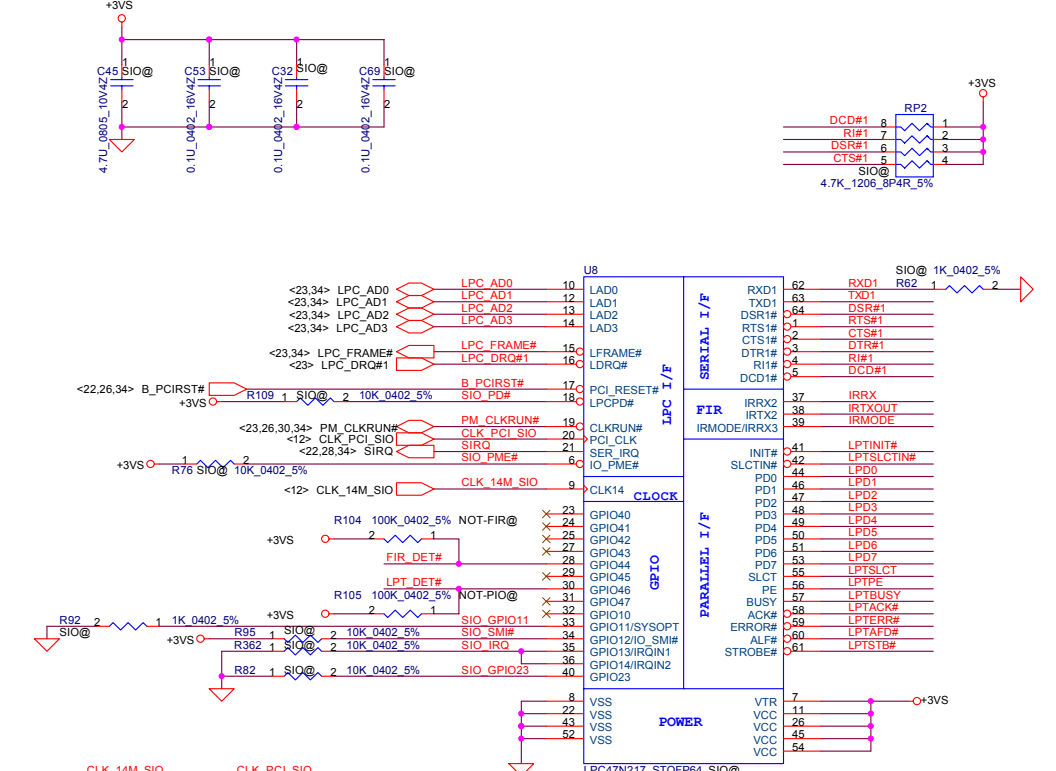
Moad Bridge



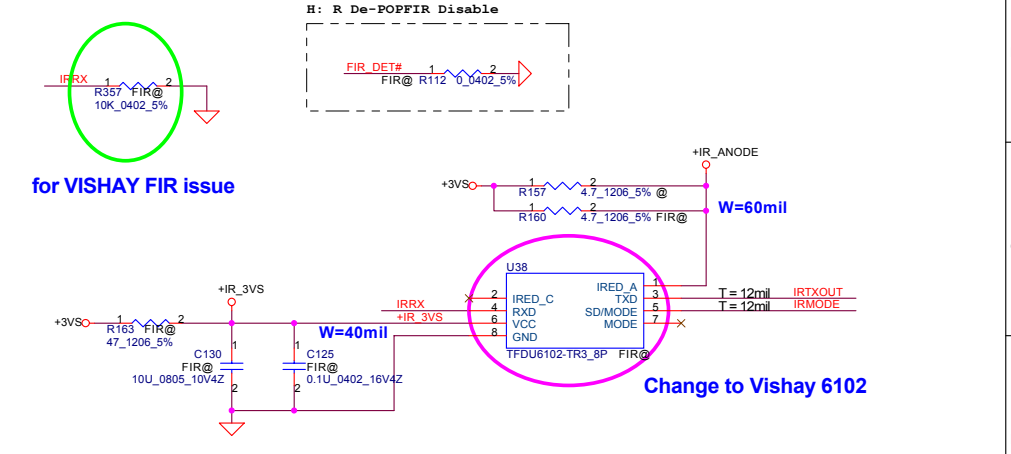
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Compal Electronics, Inc.		
Title AMP & Audio Jack		
Size	Document Number	Rev
	EAL20 LA-2461	0.3
Custom Date:	日期: 八月 04, 2004	Sheet 32 of 47

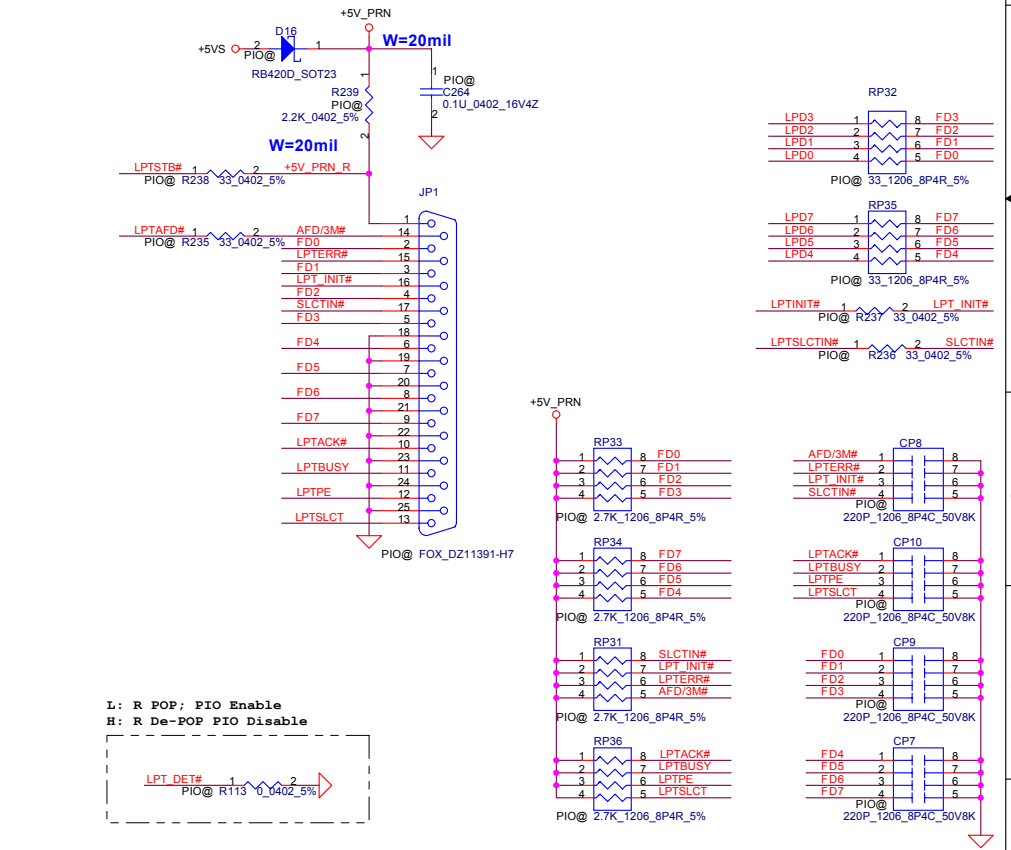
SUPER I/O SMC LPC47N217



FIR Module



Parallel Port

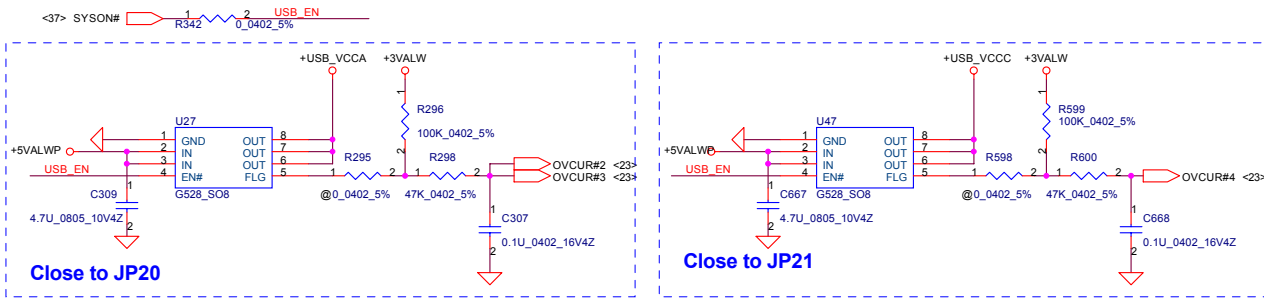


L: R POP; PIO Enable
H: R De-POP PIO Disable

Connections for LPT_DET# (pin 1) and PIO@ (pin 2) are shown.

Title			
SMSC LAP47N217 SIO,PIO,FIR			
Size	Document Number	Rev	
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Date:	星期三, 八月 04, 2004	Sheet	33 of 47

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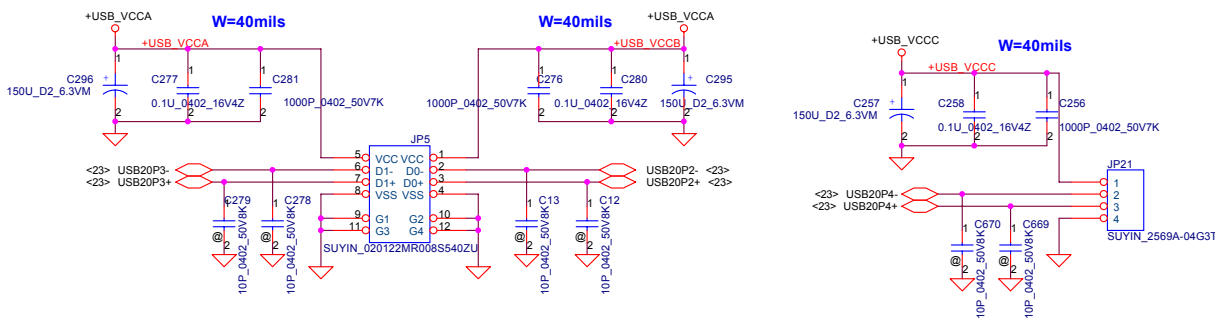
Close to JP20

Close to JP21

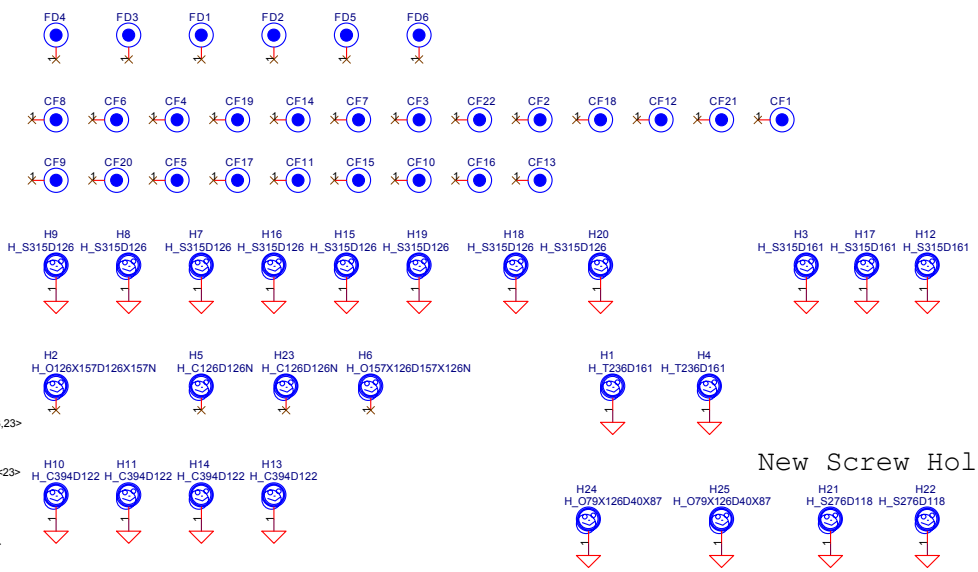
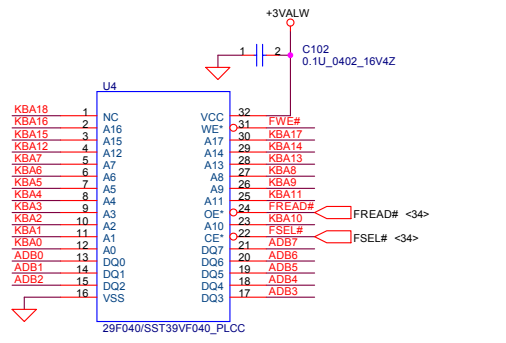
USB CONN. 1

USB CONN. 2

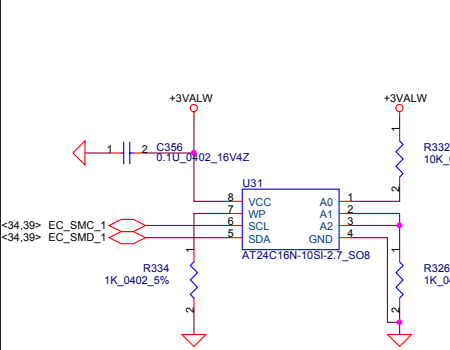
USB CONN. 3



512kB Flash ROM



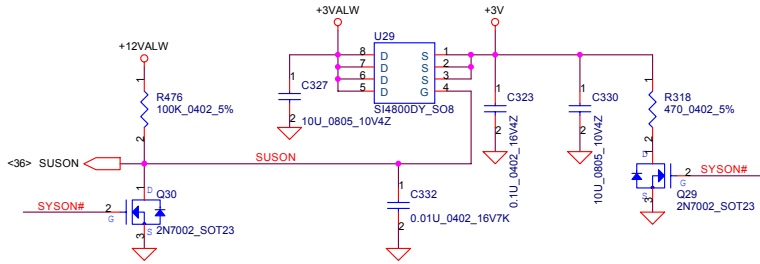
New Screw Hole



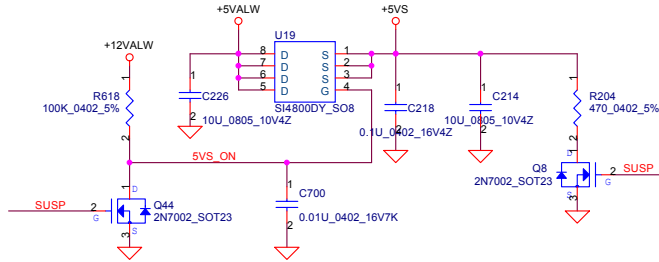
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Compal Electronics, Inc.			
Title: BIOS/WL-SW/Screw Hole/USB			
Size:	Document Number:	EAL20 LA-2461	
Date:	Rev. 0.3	Sheet 35	of 47

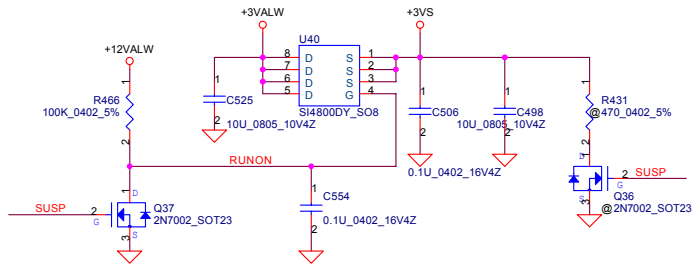
+3VALW to +3V Transfer



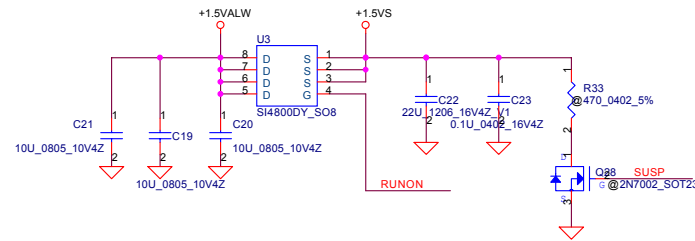
+5VALW to +5VS Transfer



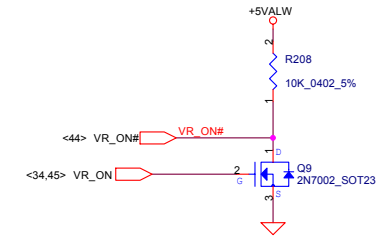
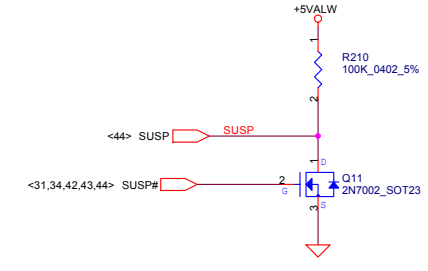
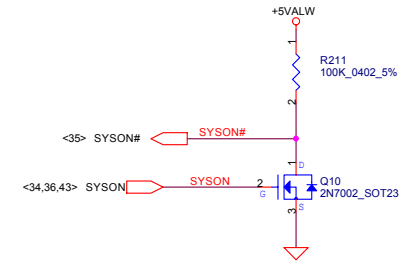
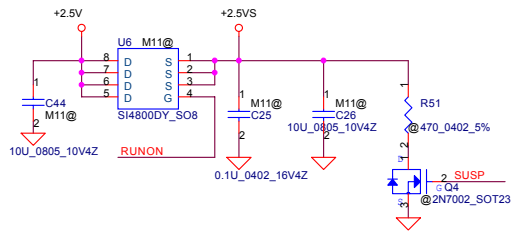
+3VALW to +3VS Transfer



+1.5VALW to +1.5VS Transfer



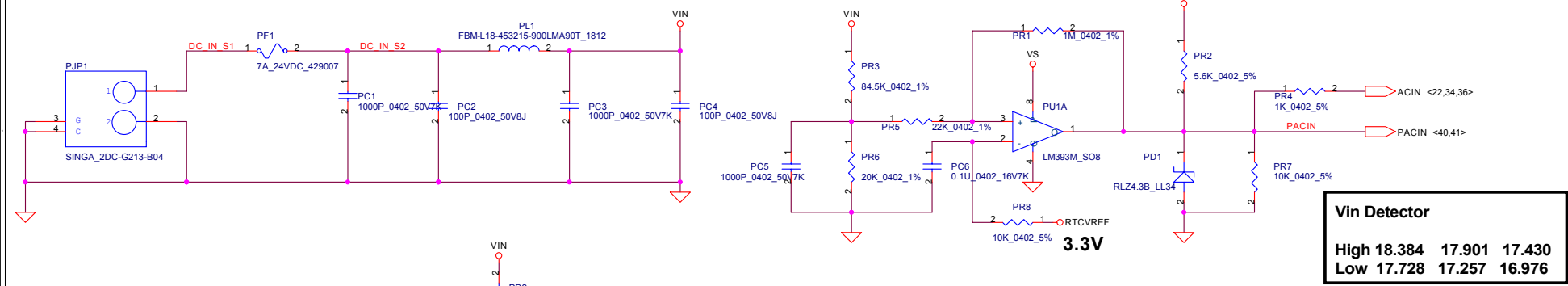
+2.5V to +2.5VS Transfer



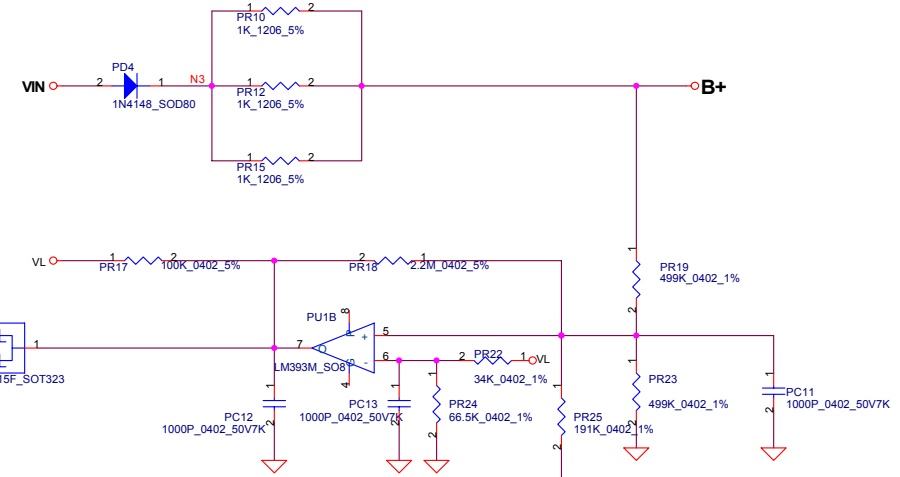
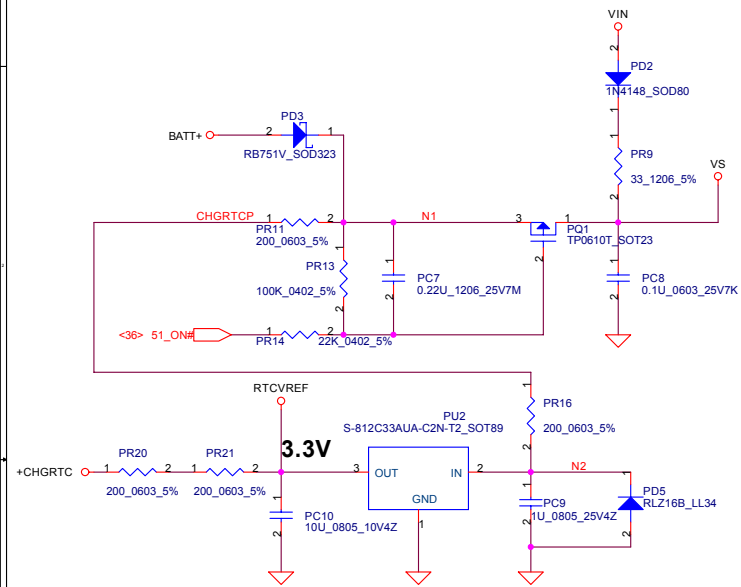
remove on integrated VGA sku

Compal Electronics, Inc.		
Title DC/DC Interface		
Size	Document Number EAL20 LA-2461	Rev 0.3
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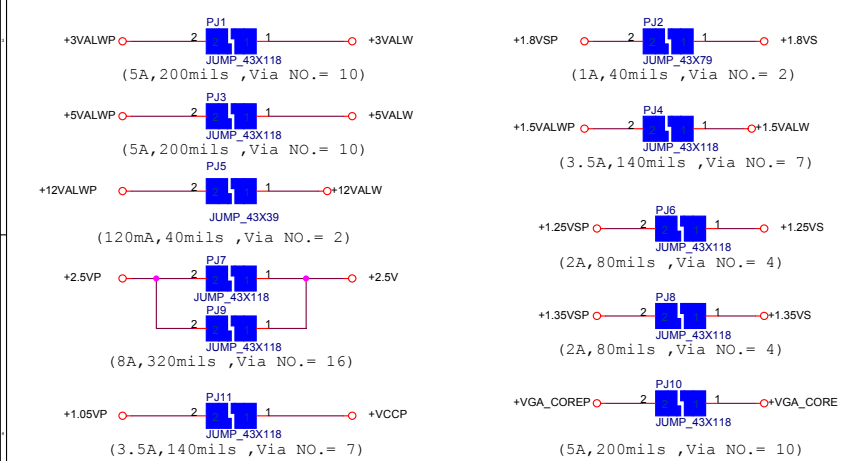
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Vin Detector
 High 18.384 17.901 17.430
 Low 17.728 17.257 16.976



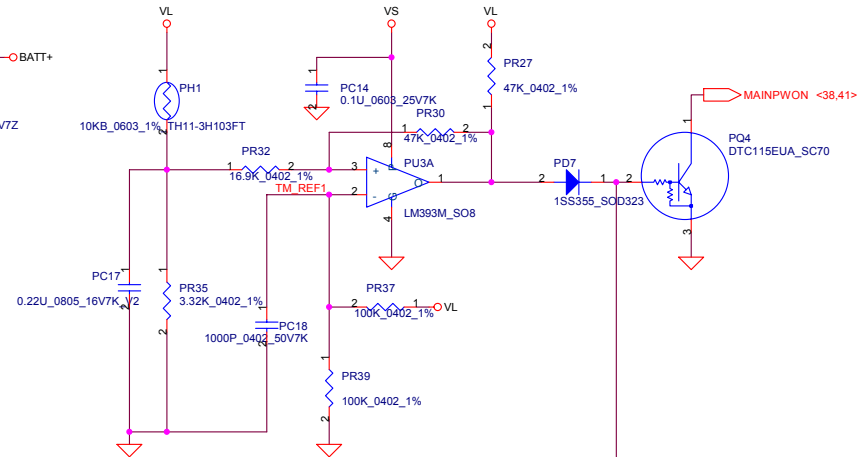
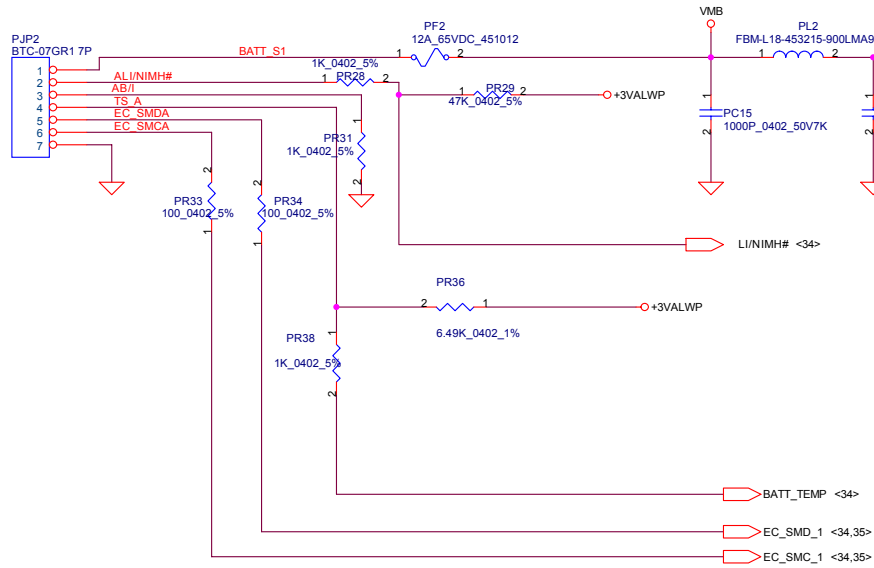
Precharge detector
 15.97V/14.84V FOR
 ADAPTOR



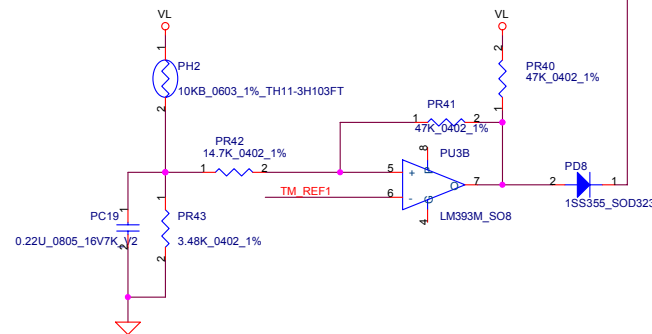
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Compal Electronics, Inc.		
Title DCIN & DETECTOR		
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PH1 under CPU botten side :
 CPU thermal protection at 84 degree C
 Recovery at 45 degree C

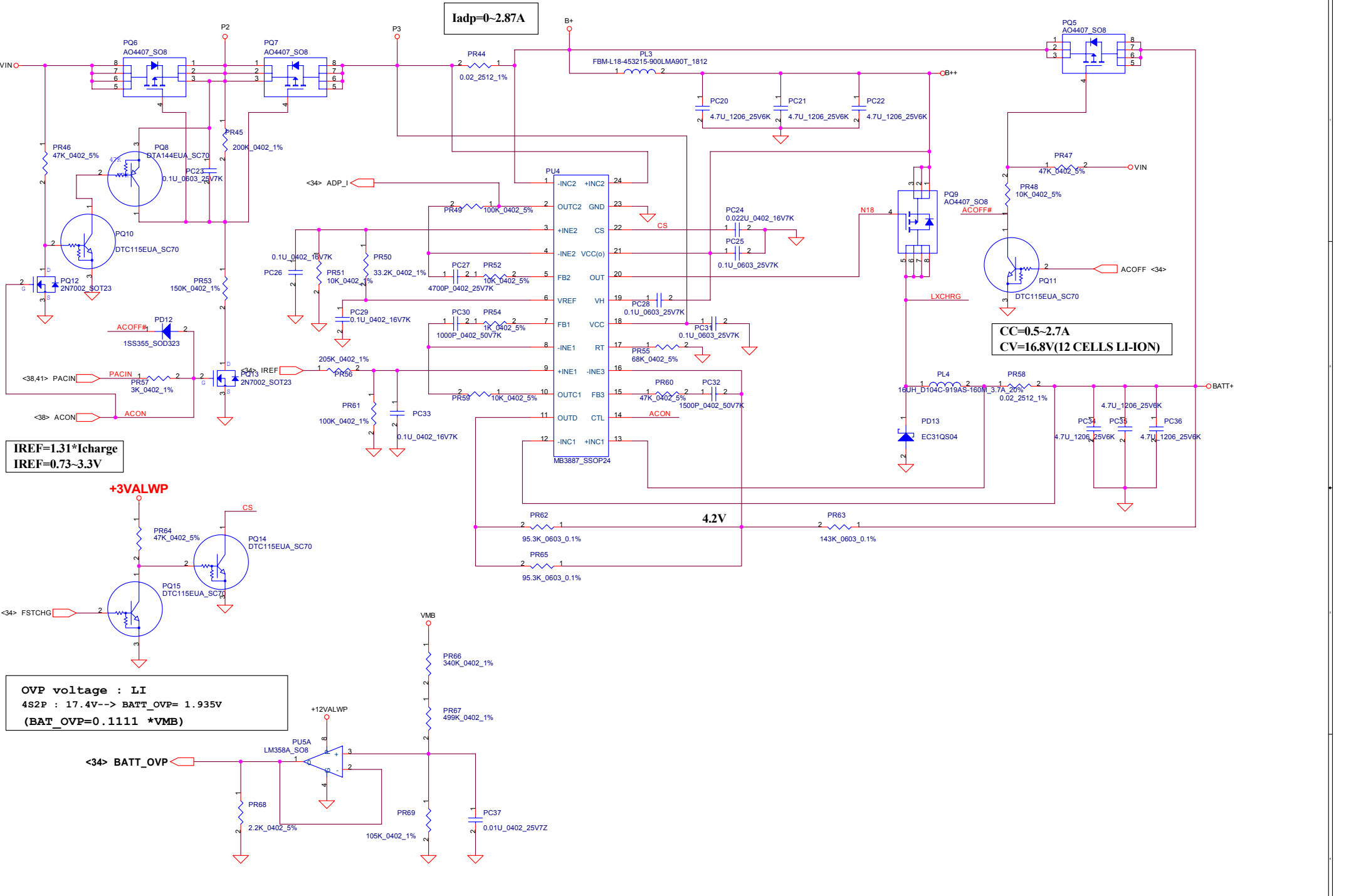


PH2 near main Battery CONN :
 BAT. thermal protection at 79 degree C
 Recovery at 45 degree C



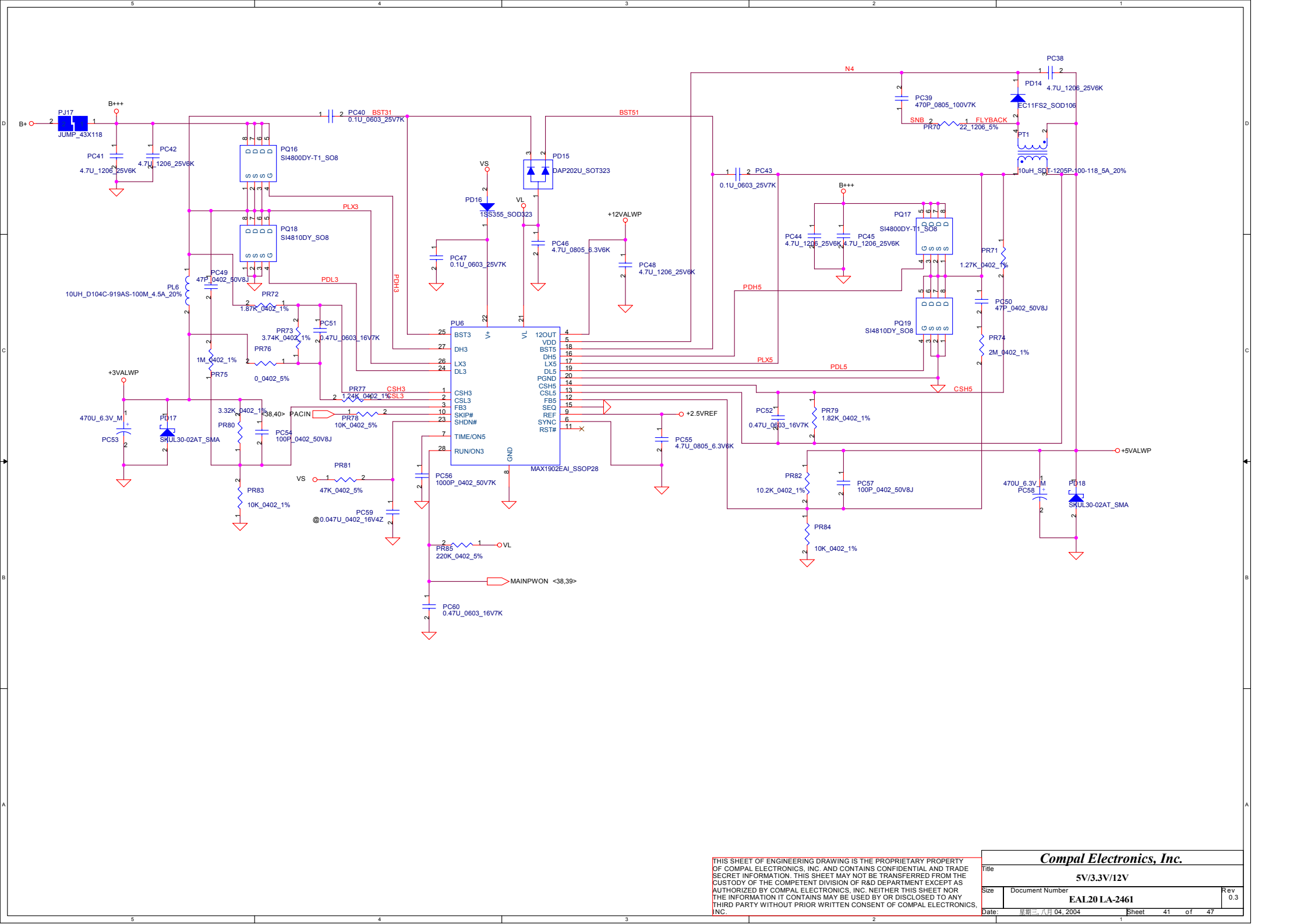
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Title BATTERY CONN / OTP		
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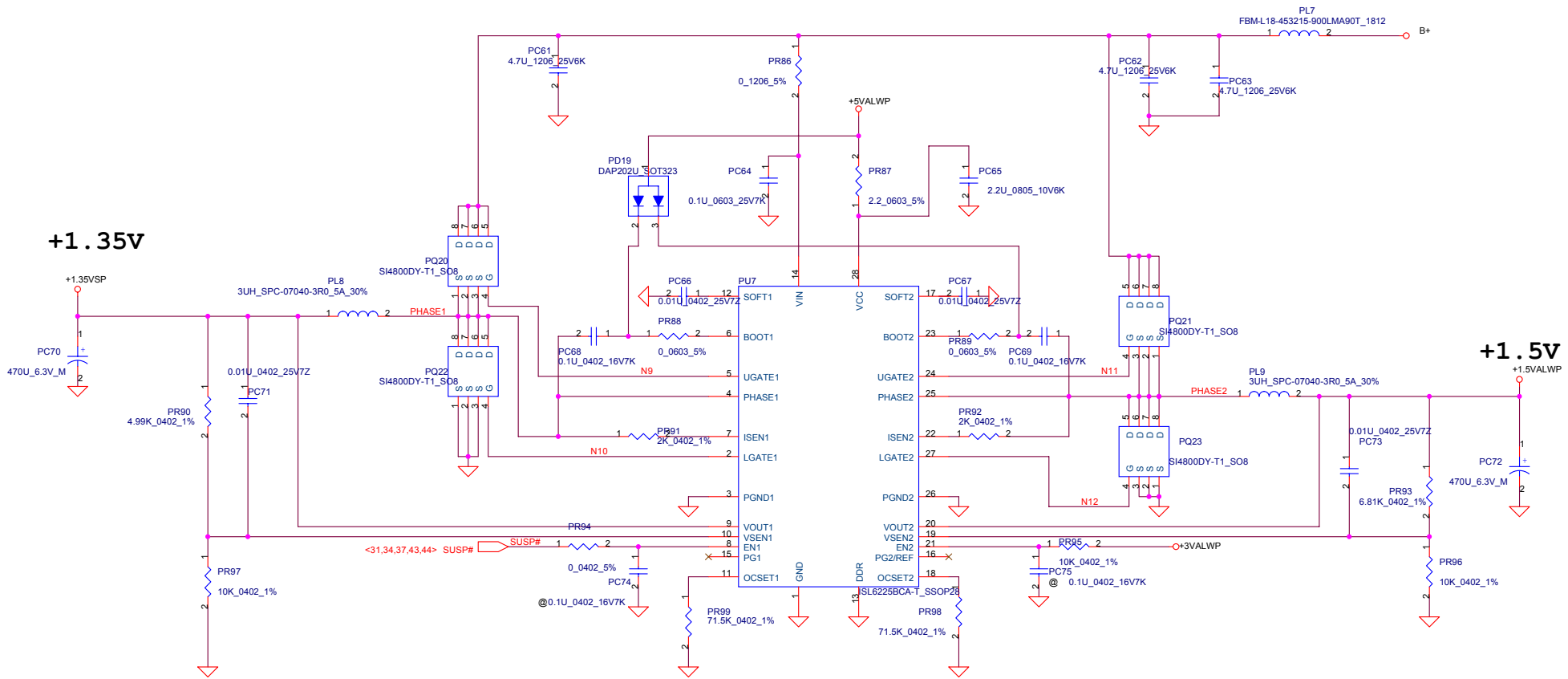
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Title CHARGER		
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Compal Electronics, Inc.		
Title 5V/3.3V/12V		
Size	Document Number EAL20 LA-2461	Rev 0.3
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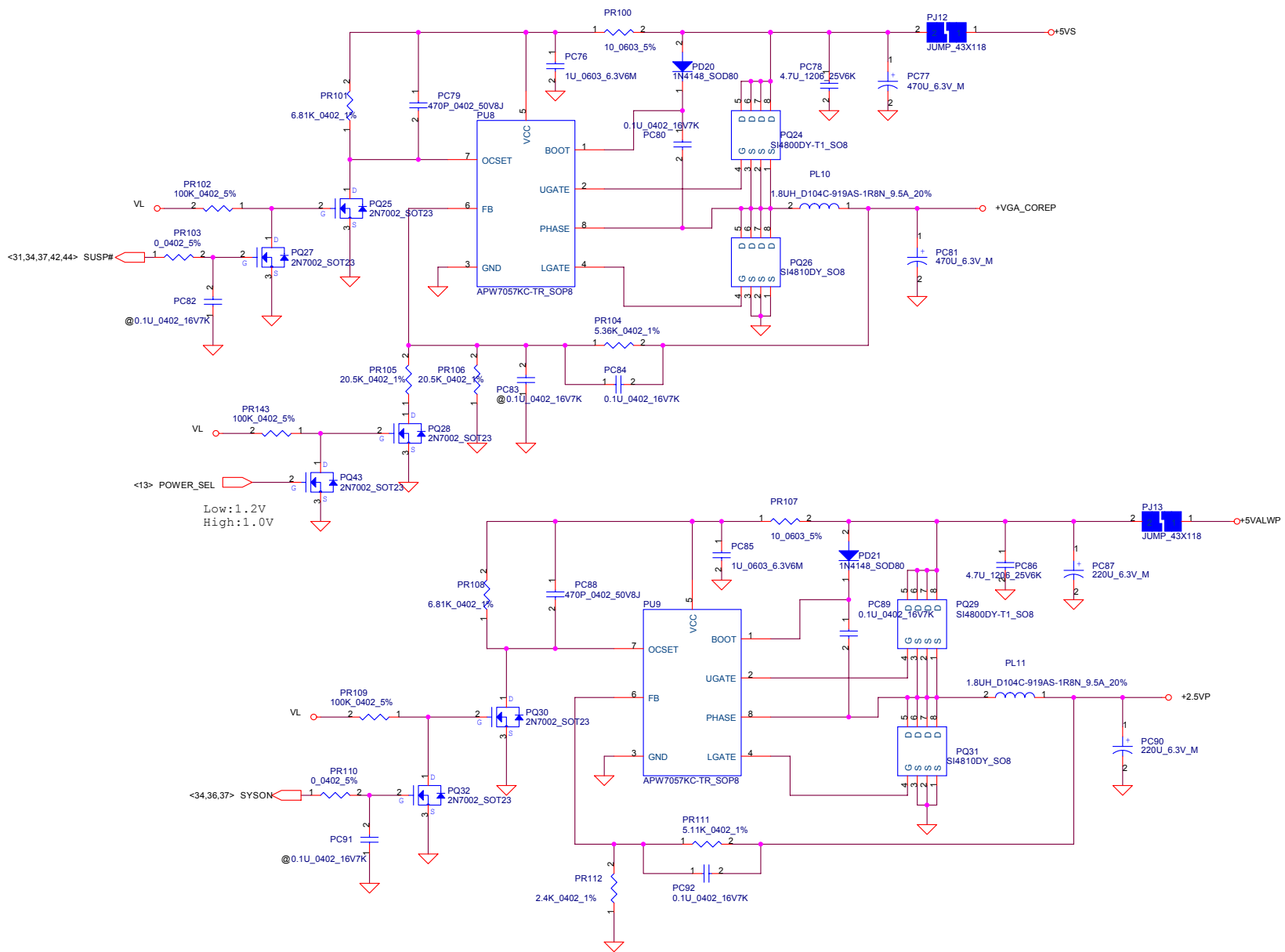


+1.35V

+1.5V

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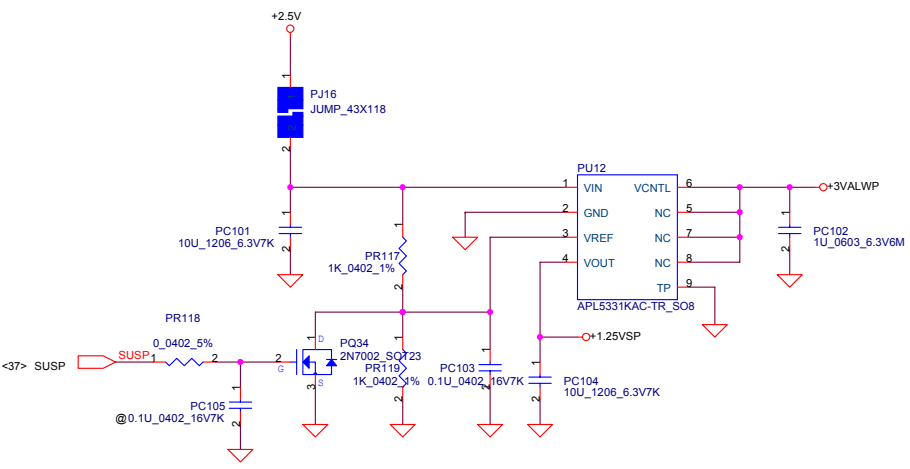
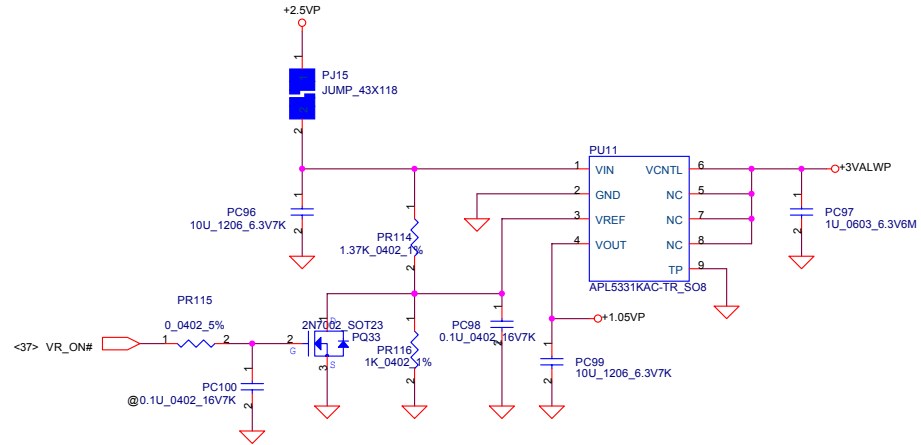
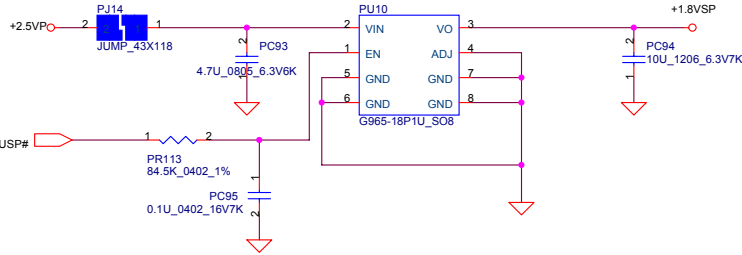
Compal Electronics, Inc.		
Title 1.35V/1.5V		
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Low: 1.2V
High: 1.0V

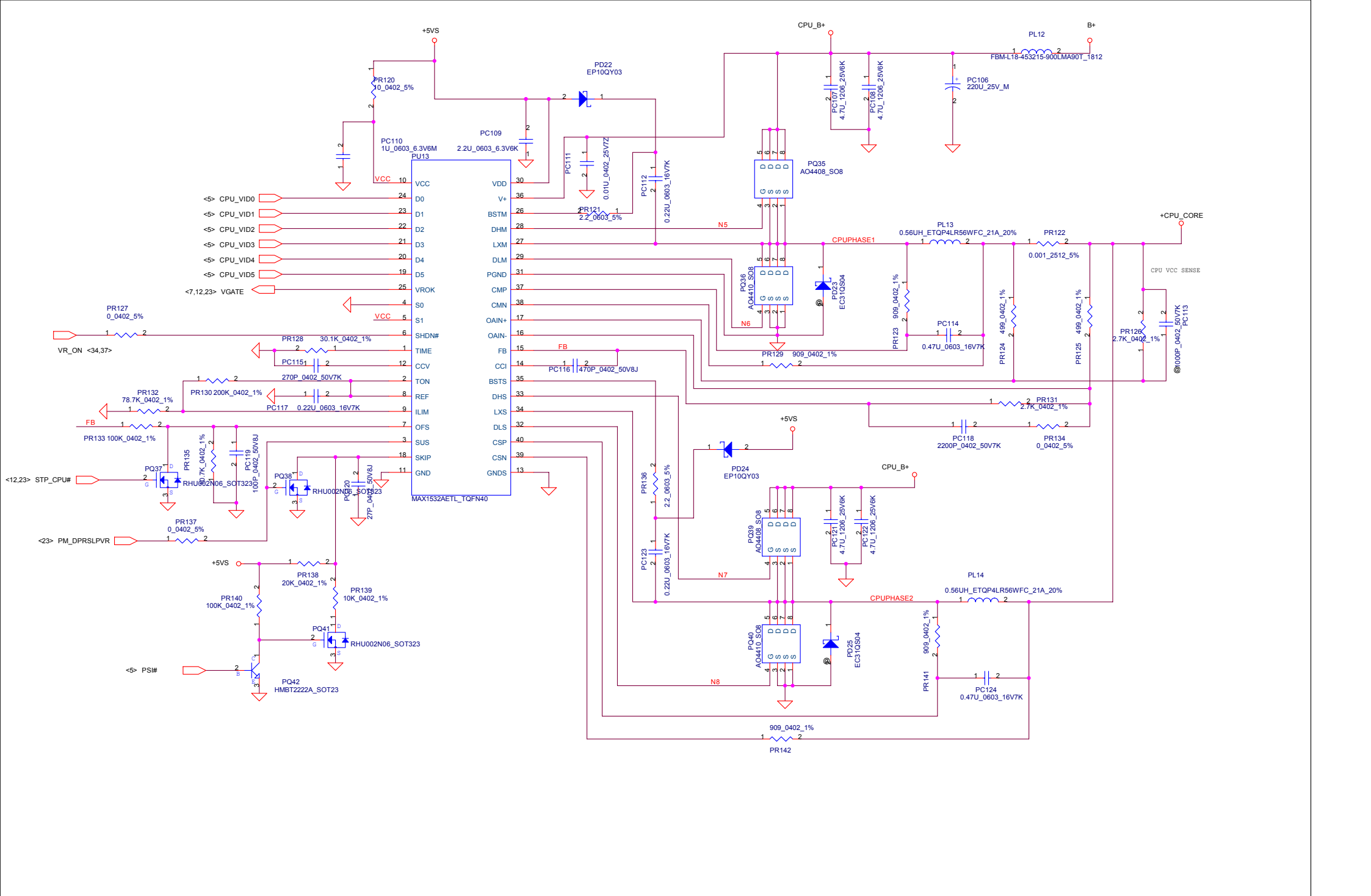
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Compal Electronics, Inc.		
Title 2.5V/VGA_CORE		
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Compal Electronics, Inc.		
Title 1.8V/1.25V/1.05V		
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Compal Electronics, Inc.			
Title CPU_CORE			
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PWR PIR LIST

EVT

page	Reason for change	Modify list
41	Improve design margin	Change PD17,PD18 from SSM14 to SKUL30-02AT
43	Change 2.5V,VGA_CORE OCP to 8A	Change PR101,PR108 from 5.11K to 6.81K
39	Improve design margin	Change PF2 rating from 7A to 12A

DVT

43	Reverse POWER_SEL signal level for HW request	Add PR143(100K),PQ43
41	Adjust 3.3V OCP	Change PR72 from 1.27K to 1.87K_0402_1% Change PR73 from 1.27K to 3.74K_0402_1% Change PR77 from 620 to 1.24K_0402_1%
41	Adjust 5V OCP	Change PR71 from 1.54K to 1.27K_0402_1% Change PR79 from 698 to 1.82K_0402_1%
43	Change choke for design margin	Change PL10,PL11 from 4.7UH to 1.8UH
44	Add 1.8V delay time for HW	Change PR113 from 0 to 84.5K_0402_1% Add 0.1U at PC95
45	For EMI requirement	Change PR121,PR136 from 0 to 2.2_0603_5%
45	Adjust CPU_CORE voltage	Change PR126,PR131 from 3K to 2.7K_0402_1%
42	Modify 1.5V enable signal for HW request	Change PR95 from 0 to 10K_0402_1%

PVT

43	Modify PL10 and PL11 Footprint	
38	Change DC-IN Jack as "SINGA_2DC-G213-B04_4P"	
41	Change PL5 as PJ17	
43	Raise VGA_CORE voltage to 1.21V for HW requirement	Change PR104 from 5.11K_0402_1% to 5.36K_0402_1%
45	Adjust CPU_CORE voltage	Change PC118 from 0.022U to 2200P

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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	6/23	P31	POP R521	CODEC CLOCK SOURCE FROM CLOCK GEN
2	6/23	P35	CHANGE R342.1 CONNECTION FROM SYSON TO SYSON#	CHANGE USB POWER TO LOW ACTIVE
3	6/23	P29	CHANGE R492.2 PULL HIGH FROM +3VS TO +VCC_5I1	CHANGE PULL HIGH POWER
4	6/23	P36	SWAP PIN OF JP16	CHANGE JP16 DIRECTION
5	6/23	P12	RESERVE C671	ADD CAP TO CONTROL VGATE RISING TIME
6	7/05	P12	CHANGE CLK_PCI_1CH CONNECT FROM U49.11 TO U49.7 CHANGE CLK_PCI_1394 CONNECT FROM U49.7 TO U49.11	CHANGE ICH PCI CLK SOURCE TO FREE RUN CLOCK, TO SOLVE SYSTEM CAN NOT SHUTDOWN ISSUE
7	7/05	P29	CHANGE 5I1 CONNECTOR FROM TAI SOL TO TAITWAN	CHANGE CONNECTOR VENDOR
8	7/06	P29	DEL R251, R249	DEL 750HM TERMINATION
		P13	ADD R603, R604	ADD 750HM TERMINATION CLOSE TO CHIP
		P19	RESERVE R605, R606	RESERVE 750HM TERMINATION CLOSE TO CHIP
9	7/06	P22	INSERT D29 BETWEEN GPI11 AND ACIN	PREVENT SB LEAKAGE DURING DC-IN TO SOLVE POWER BOTTON NO FUNCTION ISSUE
10	7/06	P13	ADD R317 100K_0402_5% PULL DOWN POWER_SEL	PREVENT SIGNAL FLOATING
11	7/06	P29	CHANGE R528 CONNECTION	FOR CUSTOMER REQUEST
12	7/06	P36	DEL CP1-CP6, ADD C329, C672-C697	FOR EMI REQUEST
13	7/06	P36	CHANGE Q16.1 CONNECT TO ON/OFF	TO CORRECT LID SW FUNCTION
14	7/06	P20	CHANGE R294 FROM 0603 TO 0805, R19 FROM 0805 TO 1206	TO INCREASE RATING
15	7/07	P31	RESERVE 1M_0402_5% R607-R614, HCT4066 U48 RESERVE 10K_5%_0402 R615, 0_0402_5% R617, RESERVE R616	TO CONTROL POWER ON/OFF AUDIO CD PATH ADD MUX SW CONTROL
16	7/07	P12	ADD L35 BETWEEN +3VS AND +3VS_CLK	FOR CUSTOMER REQUST
17	7/08	P37	CHANGE C554 FROM 0.01U TO 0.1U CHANGE U19.4 NET FROM RUNON TO 5VS_ON ADD R618, Q44, C700, ADD 5VS_ON NET	CHANGE POWER ON SEQUENCE CONTROL +5VS CONTROL GATE
18	7/09	P06	CHANGE R461 FROM 27.4 TO 37.4OHM	CHANGE RESISTANCE FOR 855GME
19	7/09	P26	CHANGE C325 FROM 0.01U TO 0.1U, R292 FROM 5.9K TO 5.36K	CHANGE R.C TO PASS LAN TEST
20	7/09	P29	CHANGE CP2211 U18 FROM C1 TO D3 VERSION	CHANGE FOR MATERIAL EOL

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	7/15	P19	CHANGE R389, R393 BOM STRUCTURE FROM UMA@ TO @	REMOVE IN UMA SKU
2	7/20	P16	RESERVE D2 SIZE CAP C701 ON +VGA_CORE PLANE	ADD ONE MORE BULK CAP FOR VGA CORE
3	7/20	P28	ADD D12, R217, R438, R440, R443, R447, R448, R456, R458, R474, R495, R501 BOM STRUCTURE 5I1@	CHANGE BOM STRUCTURE TO CONTROL BOM
		P29	ADD C518, C585, C592, C617, C618, R449, R455, R492, R494, R502, R520, R528, JP13, U44 BOM STRUCTURE 5I1@	
		P12	ADD R524 BOM STRUCTURE 5I1@	
4	7/20	P31	NEW ADD R619 BETWEEN L_OUT_L AND AMP_LEFT NEW ADD R620 BETWEEN L_OUT_R AND AMP_RIGHT	ADD RES TO BYPASS MUX
5	7/20	P12	CHANGE R574 TO RESERVE	
		P31	CHANGE R527, R521 TO RESERVE	CHANGE AC CODEC CLOCK SOURCE
		P31	CHANGE X3, C610, C619 TO MOUNT	
6	7/20	P31	CHANGE U45.47 NET NAME FROM EAPD TO EAPD_CODEC	USE KBC TO MUTE AMP
		P34	NEW ADD R621 BETWEEN EAPD_KBC AND U35.11	
		P32	ADD U9A, CONNECT U9A.1 TO EAPD_CODEC, U9A.2 TO EAPD_KBC U9A.3 TO EAPD	
7	7/21	P34	RESERVE R622.2, R623.2, R624.2 PULL HIGH TO +3VALW NEW ADD R625.2, R626.2, R627.2 PULL LOW TO GND ADD SKU_ID0 CONNECT BETWEEN U35.93, R622.1, R625.1 ADD SKU_ID1 CONNECT BETWEEN U35.94, R623.1, R626.1 ADD SKU_ID2 CONNECT BETWEEN U35.75, R624.1, R627.1	ADD SKU ID FUNCTION FOR EC RECOGNIZES
8	7/26	P28	Modify "5I1@ " to "5I1@"	
		P29	Modify "5I1@ " to "5I1@"	
		P30	Modify "KS@ " to "KS@"	
		P33	Modify R157 remark from "FIR@" to "@"	
		P21	Modify JP3 footprint from "SUYN 030336FR004T115ZU 4P_EAL20" to "030336FR004T115ZU 4P_EAL20"	
9	7/29	P36	Shift SW/LED Connector signal up one pins, leave JP15.11 as NC.	
		P35	Add 3 screw hole, H23(H_C126D126N), H24 and H25 (H_079X126D40X87) H23 for M/B location Keeping. H24 and H25 for Double USB holding.	
10	7/31	P20	L5 and L4 change as 0_0805_5%	
		P31	L9 and L11 change as 0_0603_5%, L26, L27 and L28 change as 0_0805_5%	
		P32	L29 and L30 change as 0_0805_5%, L26, L31, L32, L33 and L34 change as 0_0603_5%	
		P28	SDCK_XDWE# saperate SD_CLK and XDWE#, add R628 for XDWE#	Some card can't detect because reflection
		P29	R455.2 and JP13.36 SDCK_XDWE# change XDWE#. R450.1 and JP13.8 SDCK_XDWE# change SD_CLK.	
		XXX	Update schematic name from LA2641 to LA2461.	
11	8/02	P20	Add D30 for EMI ESD test fail.	
		P32	L31, L32, L33 and L34 change as Bead.	
		P04	Delete P@ on PU5B.	
		P19	Update R396 and R397 as 75_0402_1%.	
		P13	Update R603, R604 and R365 as 75_0402_1%.	

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