

Boston

LA-2721 Schematics Document

Intel Dothan / Alviso GM(PM) / DDR-1 / ICH6-M

(nVIDIA NV44MV / ATi M24C)

Rev:1.0

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Issued Date	2005/05/06	Deciphered Date	2006/05/06	Title	Cover Sheet
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				Date: 2005/5/6 下午 11:47:55	Sheet 1 of 53
Boston LA-2721					

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+DDRVTT	1.25V switched power rail for DDR terminator	ON	OFF	OFF
+1.5VALW	1.5V always on power rail	ON	ON	ON*
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+DDRVCC	2.5V power rail for DDR	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+5VCD	5V switched power rail for CDROM	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON
+5VAMP	5V switched power rail for amplifier	ON	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus	AD20	2	PIRQA/PIRQB/PIRQC/PIRQD
1394	AD20	2	PIRQA/PIRQB/PIRQC/PIRQD
Card reader	AD20	2	PIRQA/PIRQB/PIRQC/PIRQD
Mini-PCI	AD18	1	PIRQG/PIRQH

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADM1032	1001 110X b
EEPROM(24C16/02)	1010 000X b	2nd Battery	1001 011X b
(24C04)	1011 000Xb	Docking	1010 000X b

EC SM Bus2 address

ICH6M SM Bus address

Device	Address
Clock Generator (ICS 952623)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM1	1001 001Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 1%			
Board ID	Rb / Rd / Rf	V _{AD_BID min}	V _{AD_BID typ}	V _{AD_BID max}
0	0	0 V	0 V	0.100 V
1	8.2K +/- 1%	0.216 V	0.250 V	0.289 V
2	18K +/- 1%	0.436 V	0.503 V	0.538 V
3	33K +/- 1%	0.712 V	0.819 V	0.875 V
4	56K +/- 1%	1.036 V	1.185 V	1.264 V
5	100K +/- 1%	1.453 V	1.650 V	1.759 V
6	200K +/- 1%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

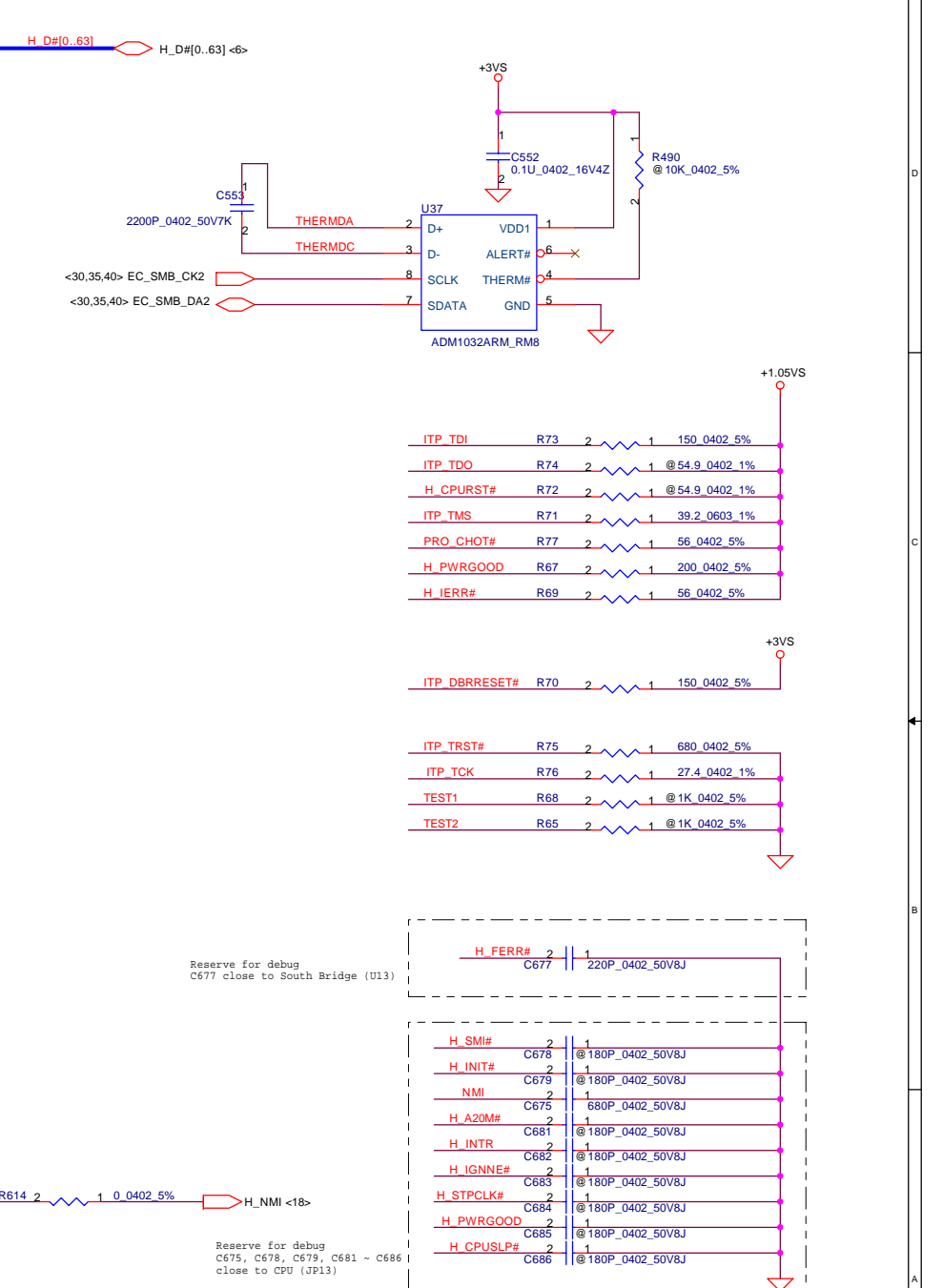
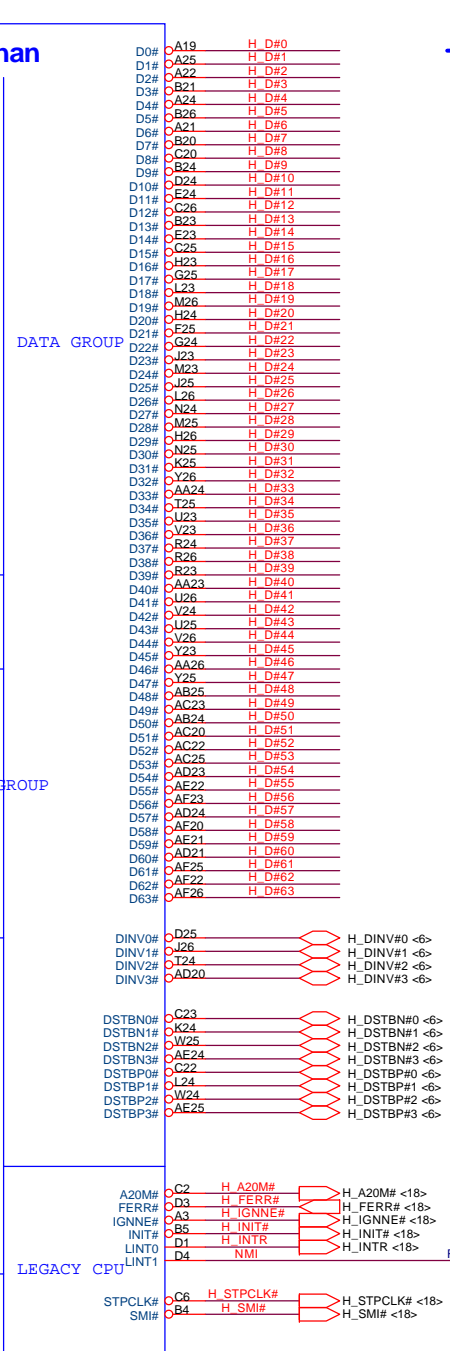
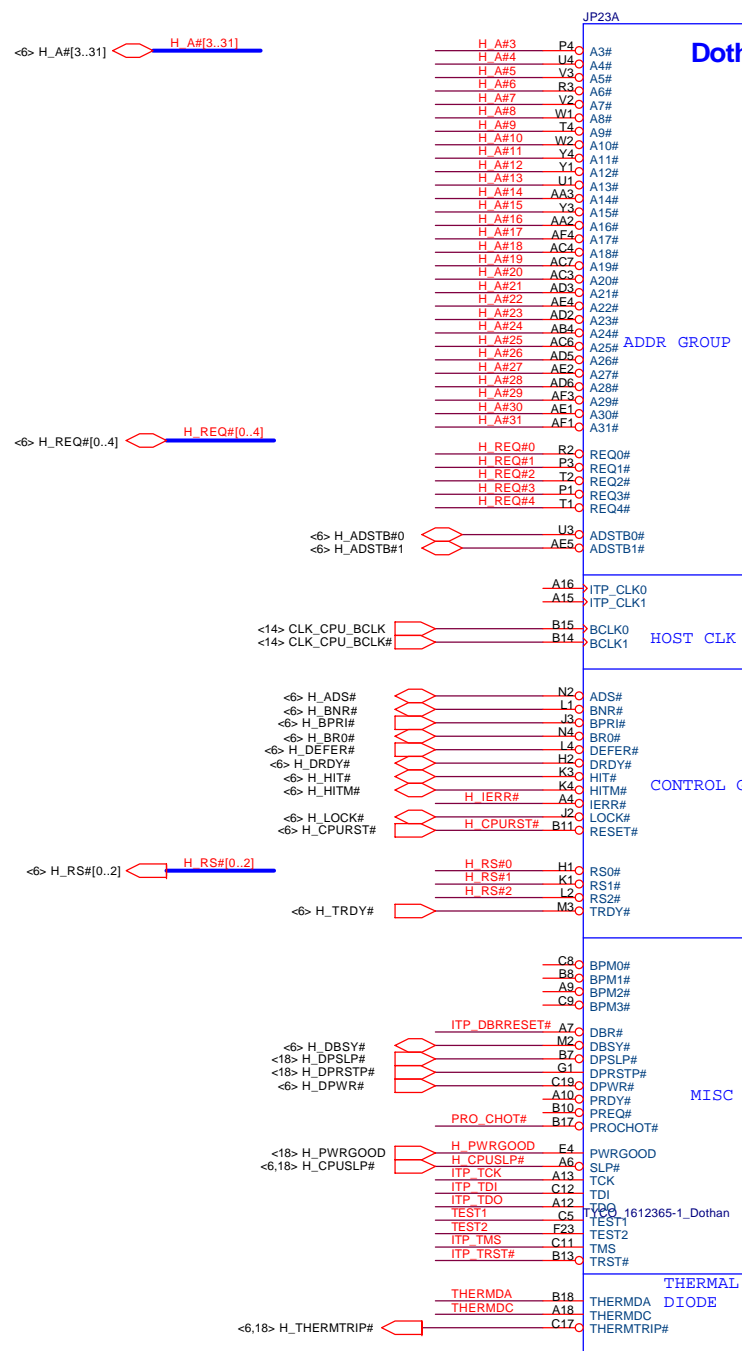
BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

SKU ID Table

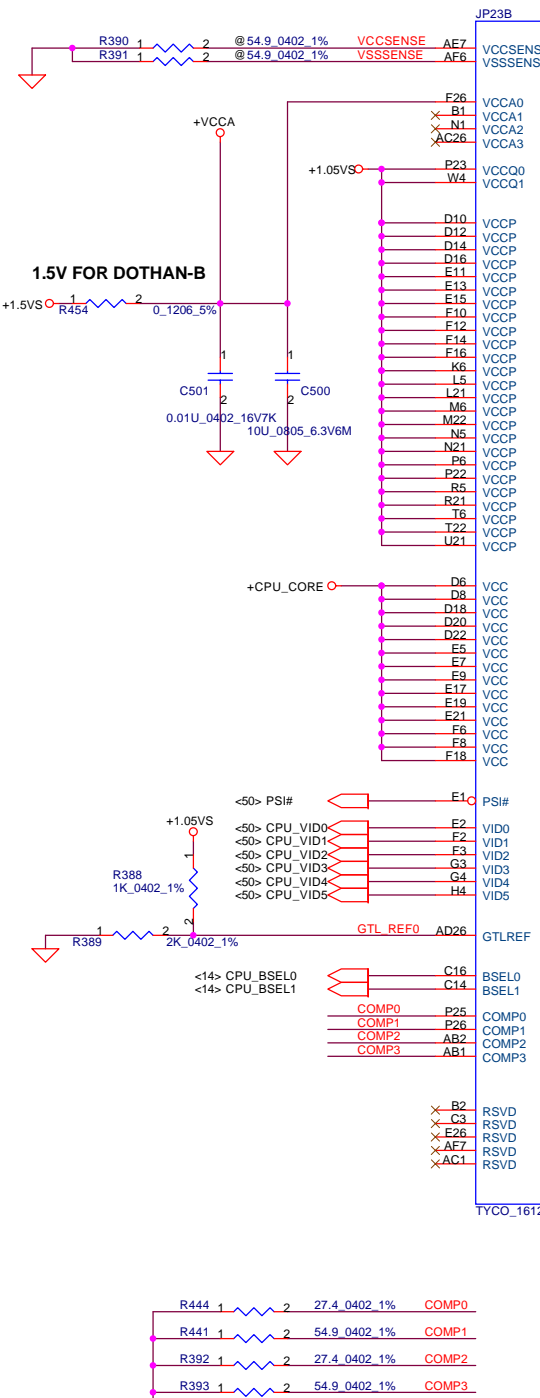
SKU_ID1	1 Button	3 Button	7 Button				
SKU_ID	0	1	2	3	4	5	6
0	10	1	8		0		
1	10C	3	C		2		
2	10G	5	9		4		
3	10GC	7	D		6		
4							
5							
6							
7							

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				Boston LA-2721		
				Date:	2005/5/6 下午 11:47:55	Sheet 3 of 53



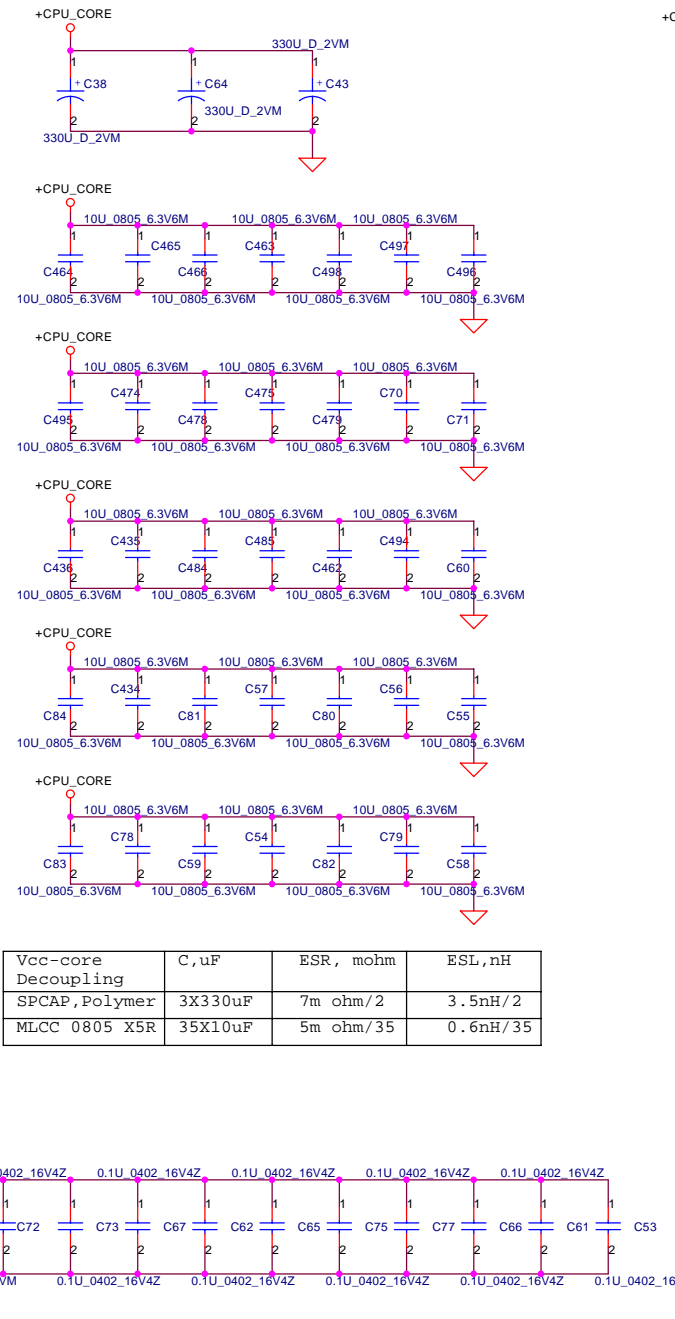
THERMDA & THERMDC Trace / Space = 10 / 10 mil

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Issued Date	2005/05/06	Deciphered Date	2006/05/06	Dothan Processor in mFCPGA479	
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Size	Document Number	Date:		Rev	
	Boston LA-2721	2005/5/6 下午 11:47:59		1.0	
				Sheet	4 of 53



Dothan

POWER, GROUND, RESERVED SIGNALS AND NC



Dothan

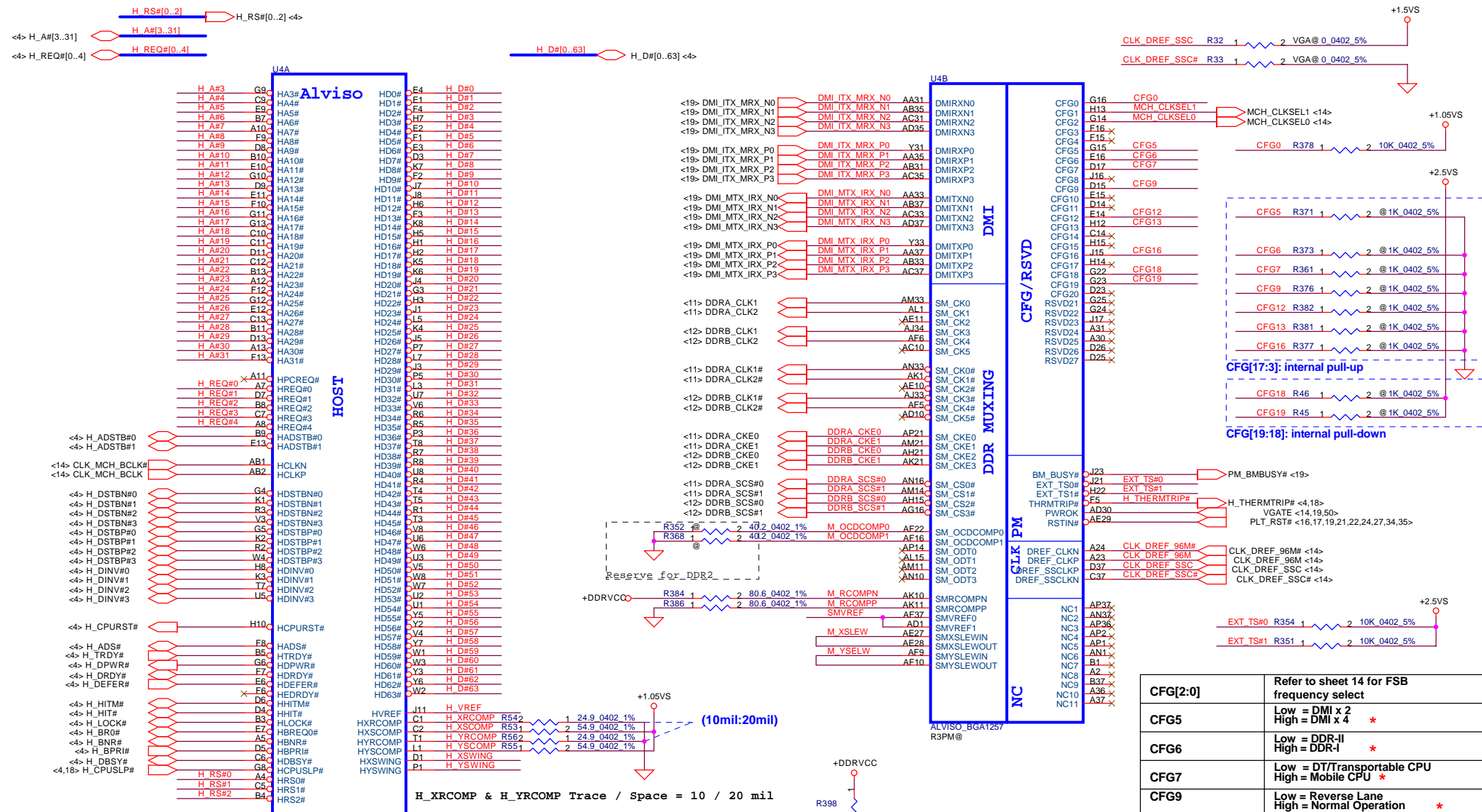
POWER, GROUND

Vcc-core Decoupling	C, uF	ESR, mohm	ESL, nH
SPCAP, Polymer	3X330uF	7m ohm/2	3.5nH/2
MLCC 0805 X5R	35X10uF	5m ohm/35	0.6nH/35

TRACE CLOSELY CPU < 0.5"

COMP0, COMP2 layout : Width 18mils and Space 25mils
 COMP1, COMP3 layout : Space 25mils

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Size	Document Number	Date:		Rev	
	Boston LA-2721	2005/5/6 下午 11:47:54		1.0	
			Sheet	5	of 53



CFG[2:0]	Refer to sheet 14 for FSB frequency select
CFG5	Low = DMI x 2 High = DMI x 4 *
CFG6	Low = DDR-II High = DDR-I *
CFG7	Low = Reverse Lane High = Normal Operation *
CFG9	Low = DT/transportable CPU High = Mobile CPU *
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default) *
CFG16 (FSB Dynamic ODT)	Low = Disabled High = Enabled *
CFG18 (VCC Select)	Low = 1.05V (Default) * High = 1.5V
CFG19 (VTT Select)	Low = 1.05V (Default) * High = 1.2V

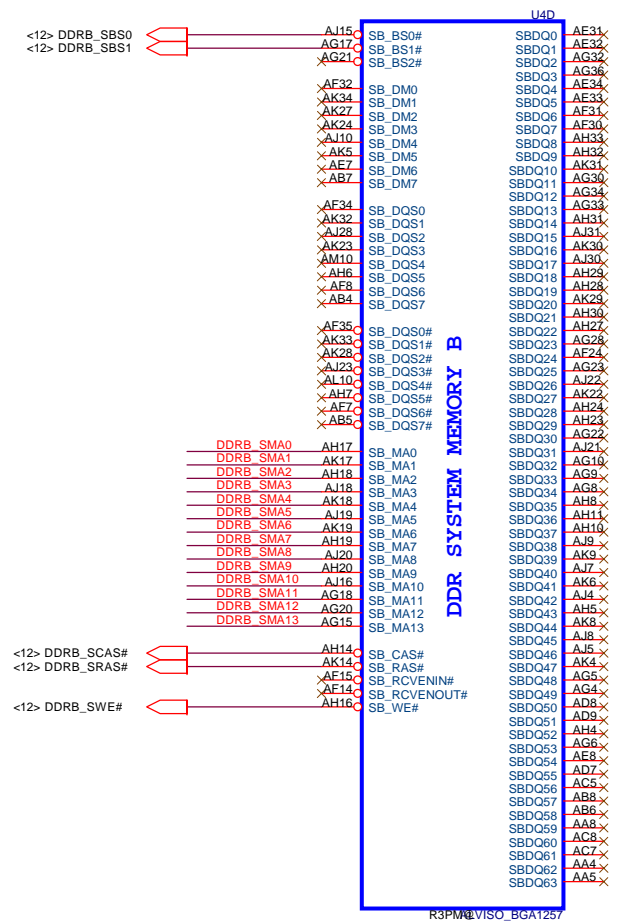
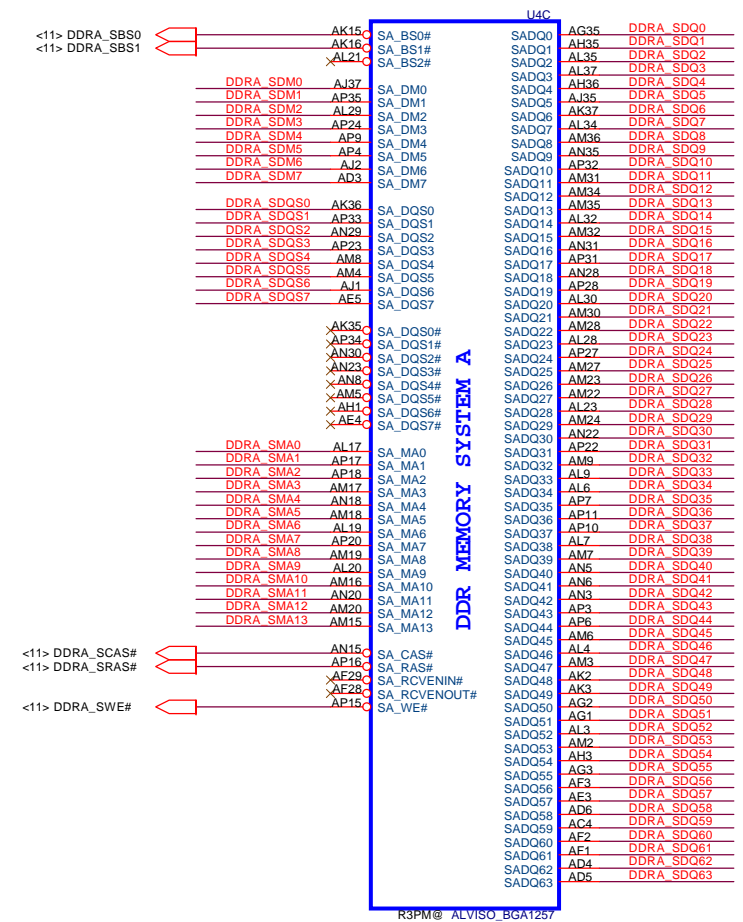
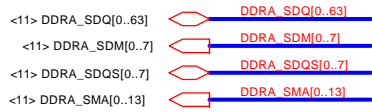
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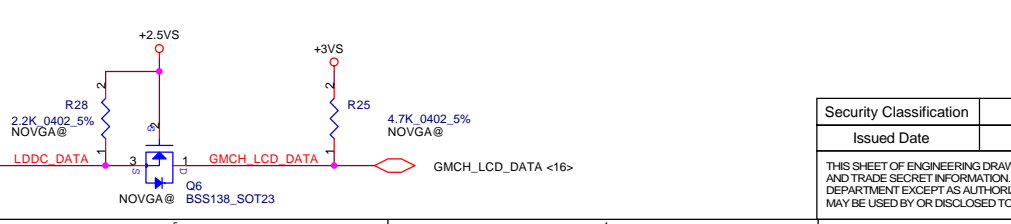
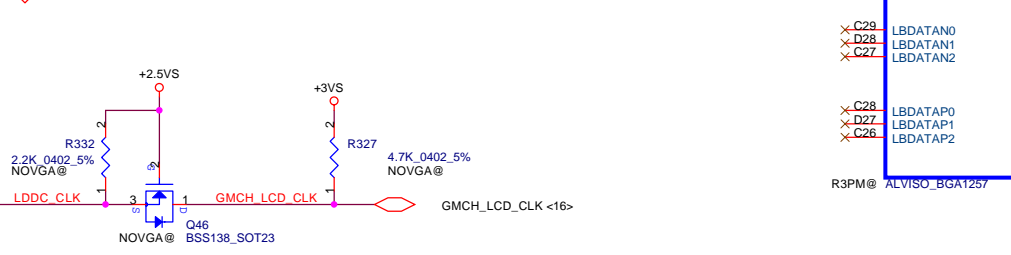
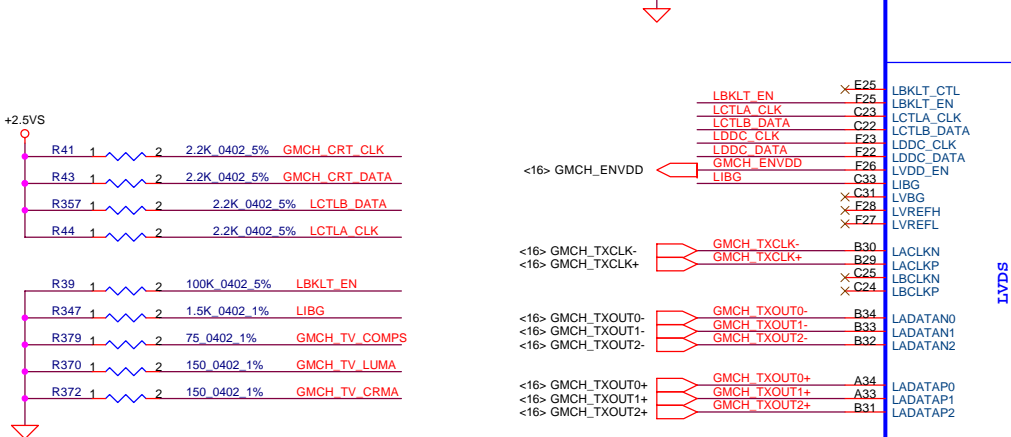
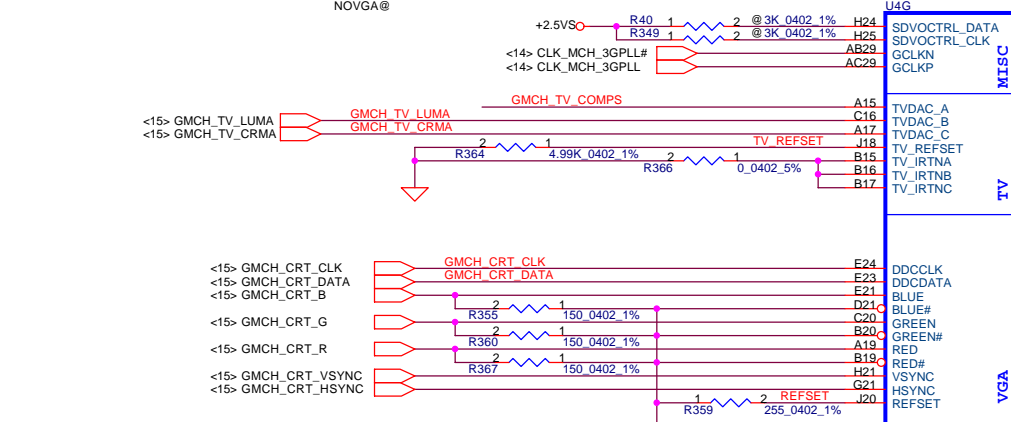
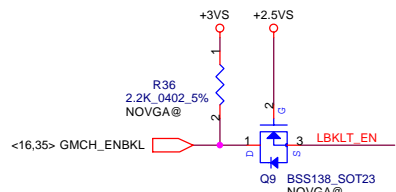
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Alviso HOST(1/5)

Title	Alviso HOST(1/5)	
Size	Document Number	Rev
	Boston LA-2721	
Date:	2005/5/6 下午 11:47:58	Sheet 6 of 53

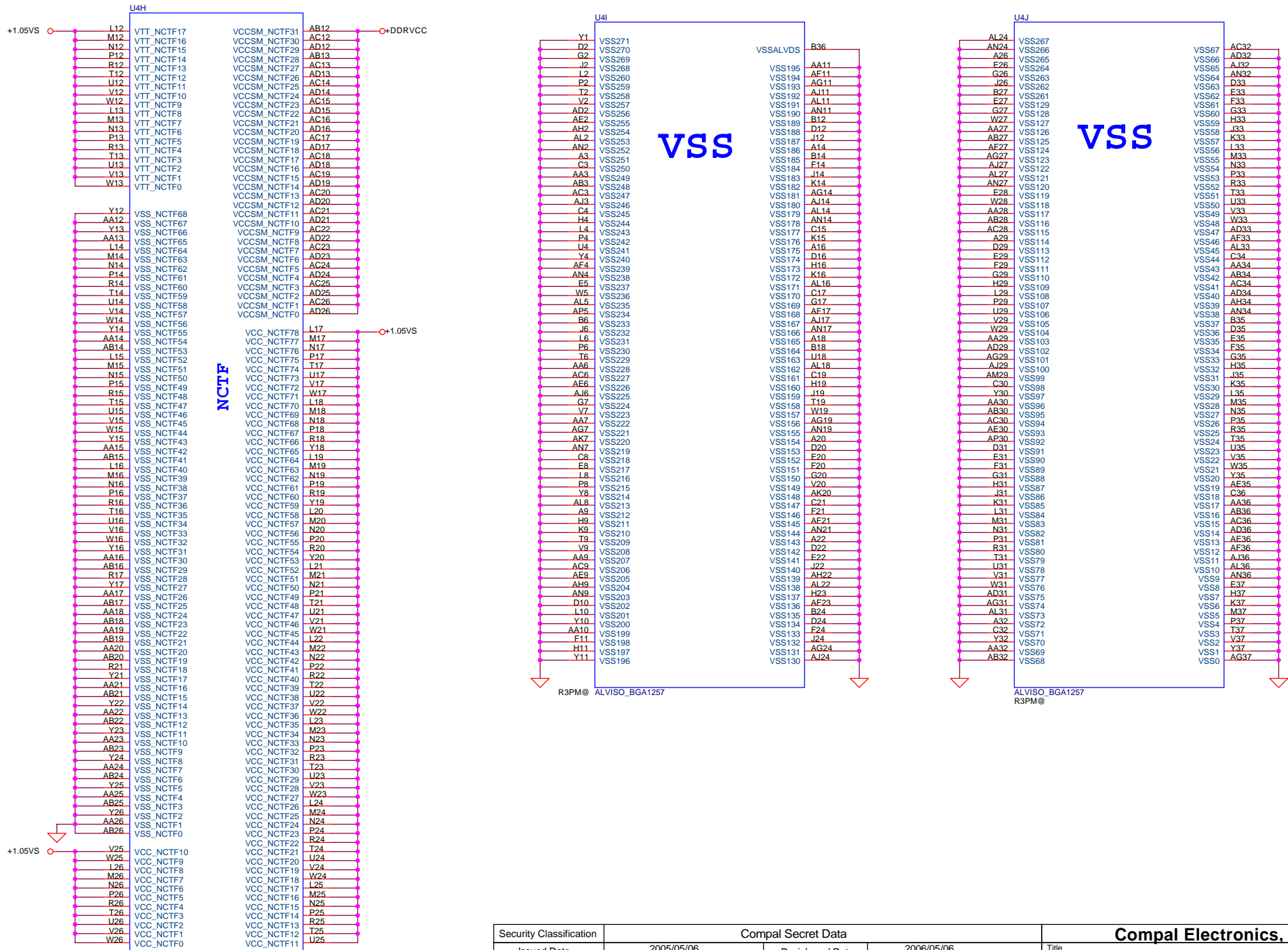


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Date:	2005/5/6 下午 11:47:55	Sheet	7	of	53

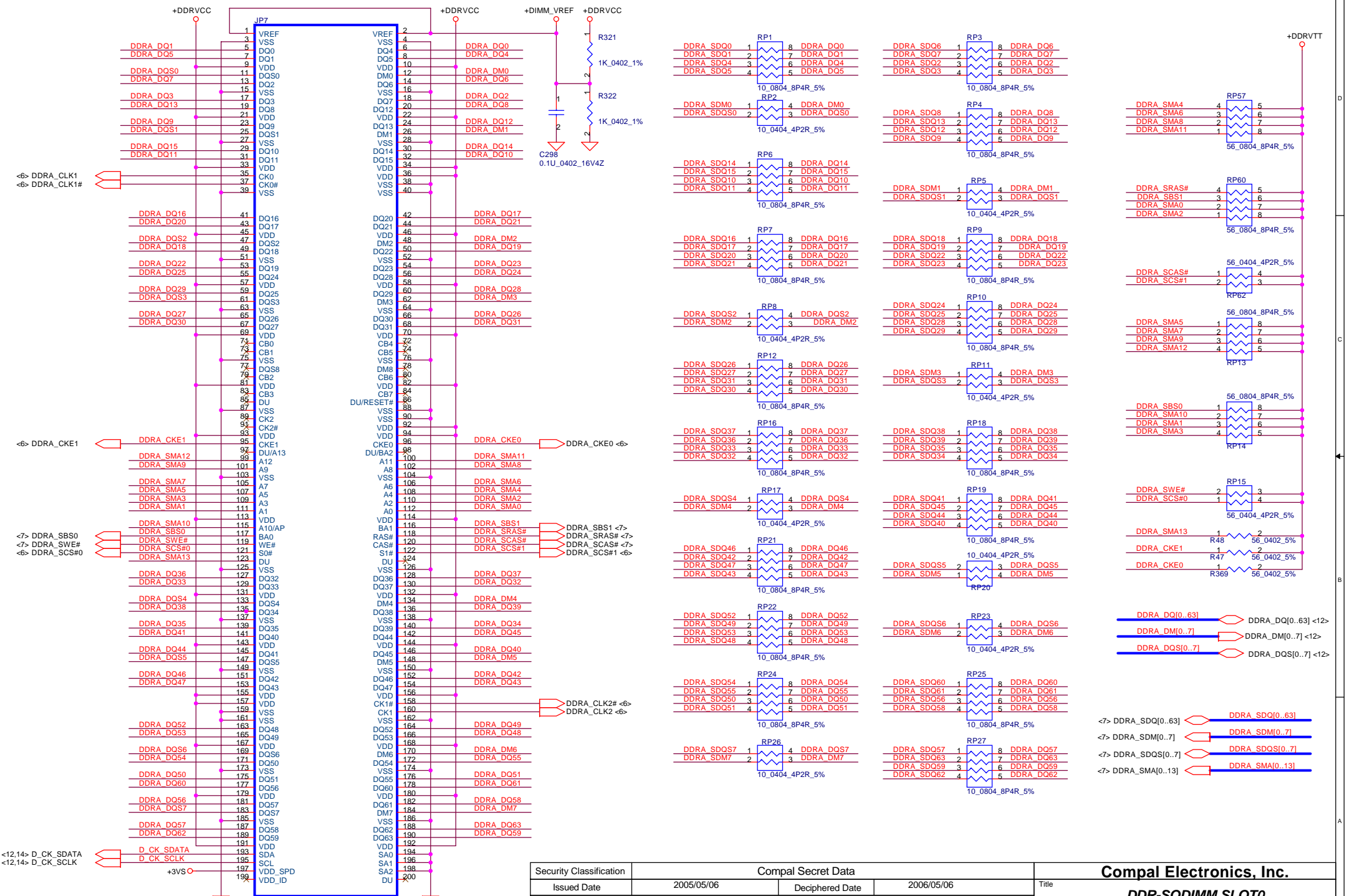


- <16> PCIE_MTX_C_GRX_N[0..15] ← PCIE_MTX_C_GRX_N[0..15]
- <16> PCIE_MTX_C_GRX_P[0..15] ← PCIE_MTX_C_GRX_P[0..15]
- <16> PCEI_GTX_C_MRX_N[0..15] ← PCEI_GTX_C_MRX_N[0..15]
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Size	Document Number			Rev	1.0
Date:	2005/5/6 下午 11:47:55	Sheet	8	of	53



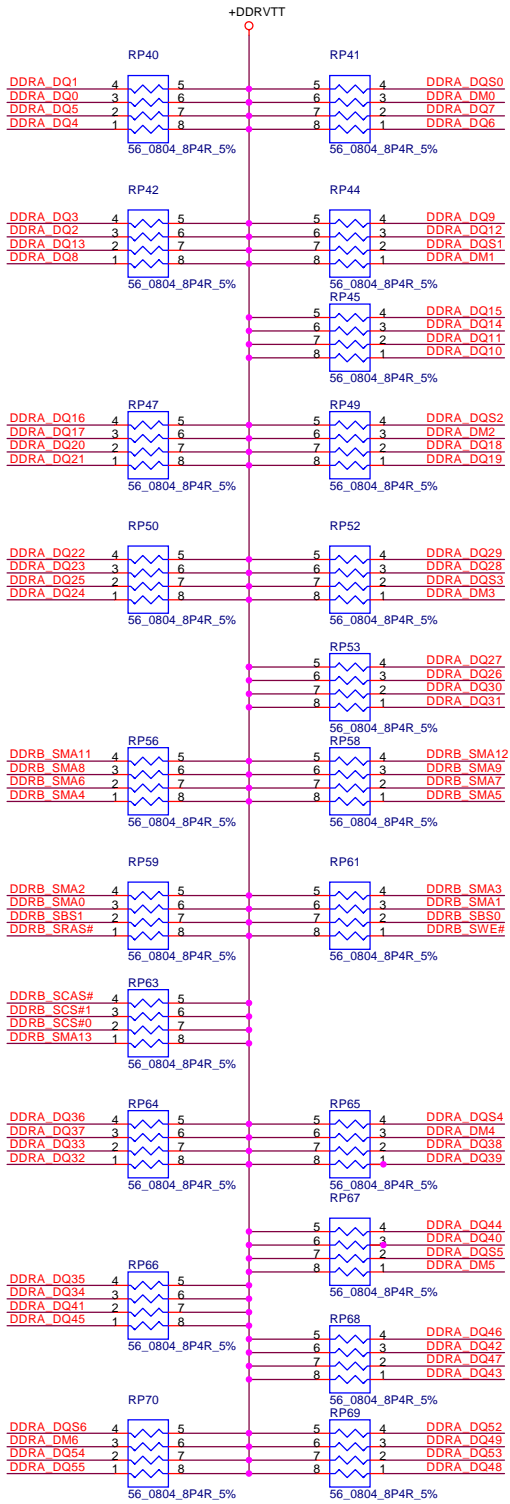
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Date:	2005/5/6 下午 11:47:54	Sheet	10	of	53



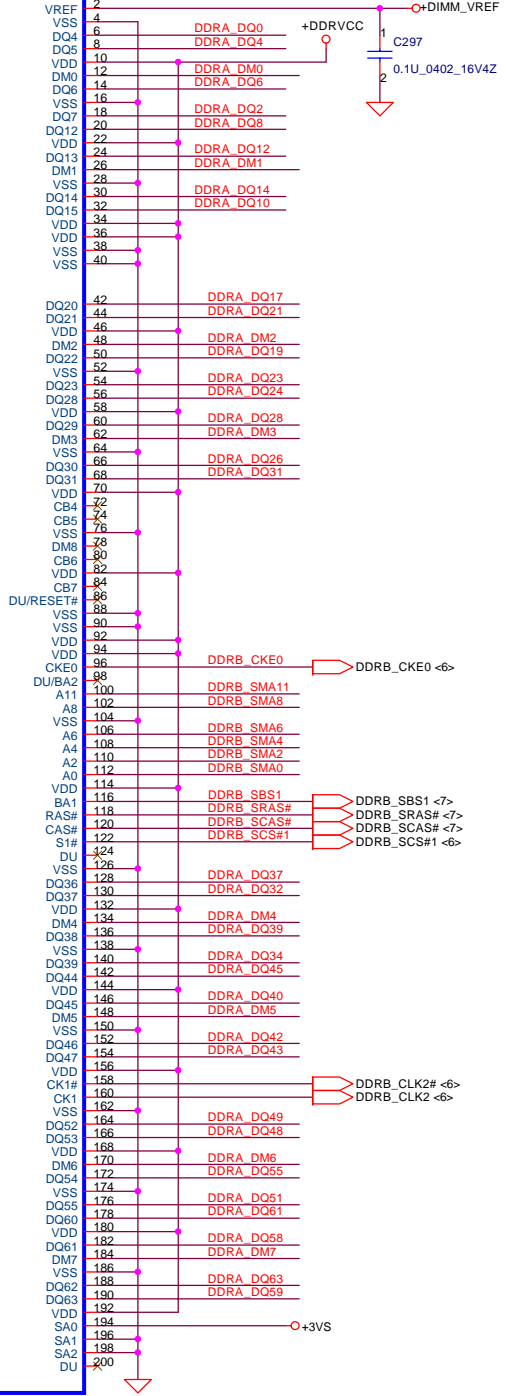
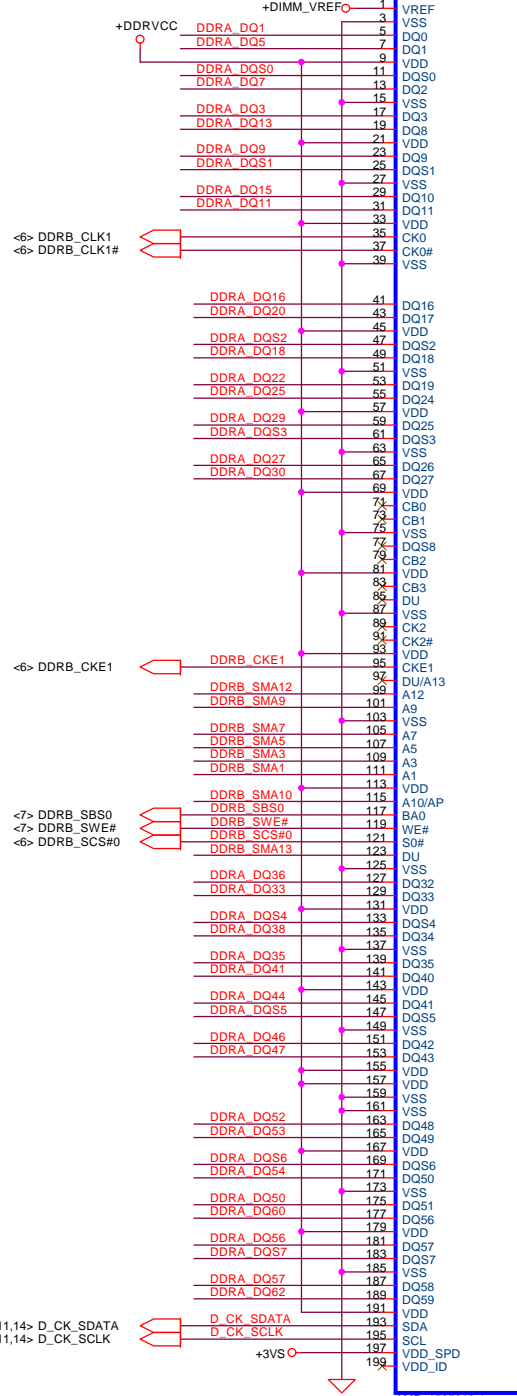
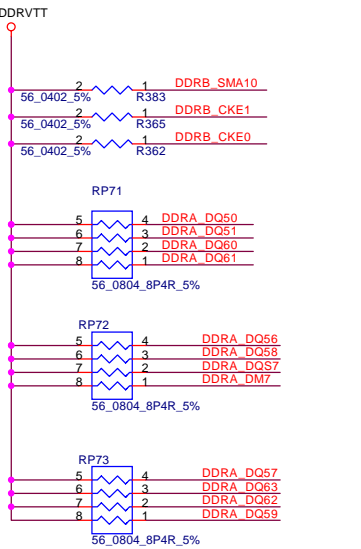
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DDR-SODIMM SLOT0			
Title	Boston LA-2721		
Size	Document Number	Rev 1.0	
Date:	2005/5/6 下午 11:47:58	Sheet	11 of 53



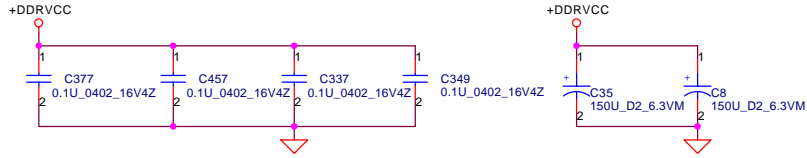
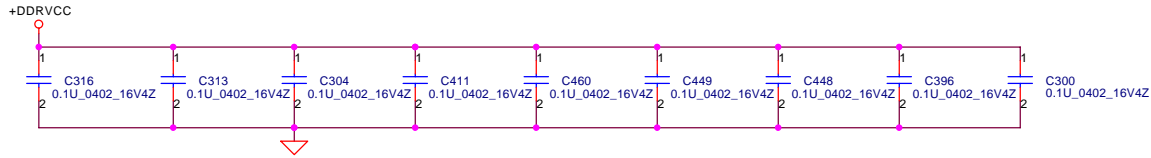
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- <7> DDRB_SMA[0..13] DDRB_SMA[0..13]



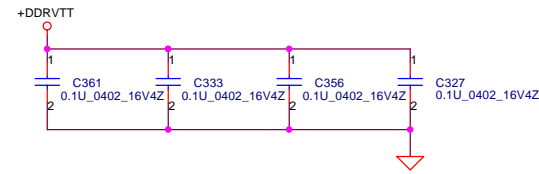
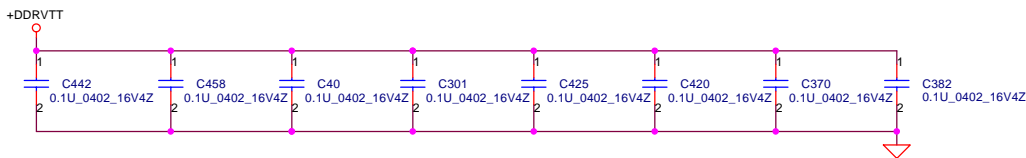
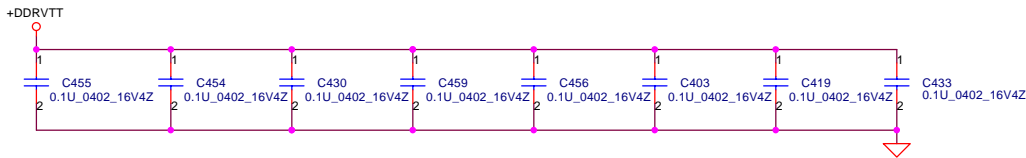
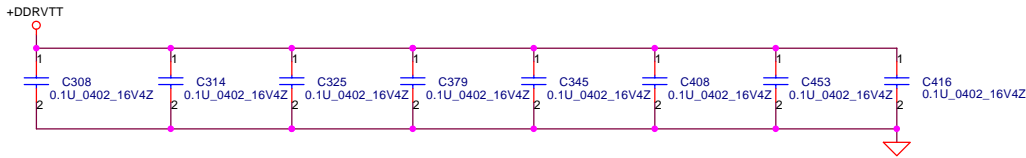
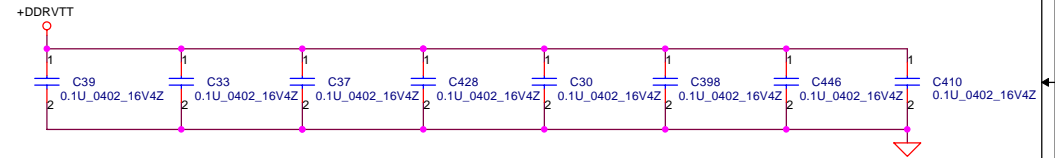
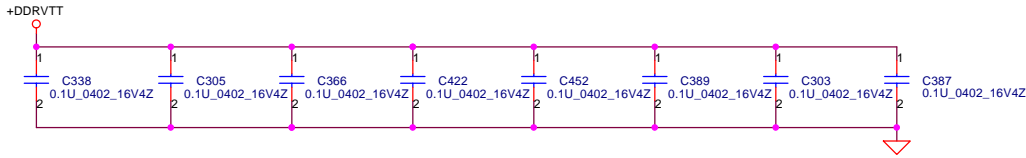
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Size	Document Number	Rev 1.0	
Date: 2005/5/6 下午 11:47:58		Sheet	12 of 53

Layout note :
Distribute as close as possible to DDR-SODIMM.



Layout note :
Place one cap close to every 2 pull up resistors termination to +1.25V

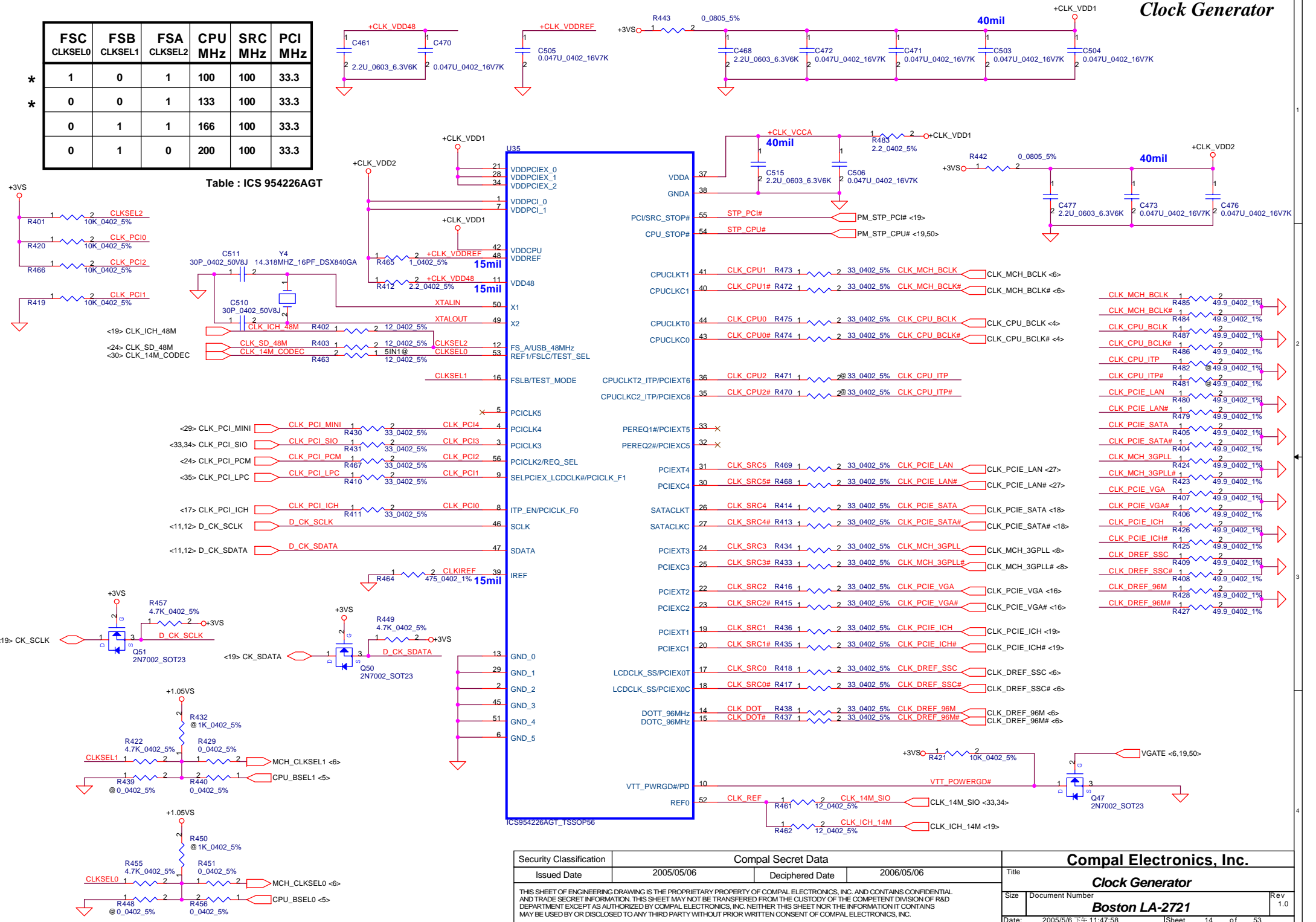


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Date:	2005/5/6 下午 11:47:56	Sheet	13	of	53
Rev 1.0					

Clock Generator

FSC	FSB	FSA	CPU	SRC	PCI
CLKSEL0	CLKSEL1	CLKSEL2	MHz	MHz	MHz
1	0	1	100	100	33.3
0	0	1	133	100	33.3
0	1	1	166	100	33.3
0	1	0	200	100	33.3

Table : ICS 954226AGT



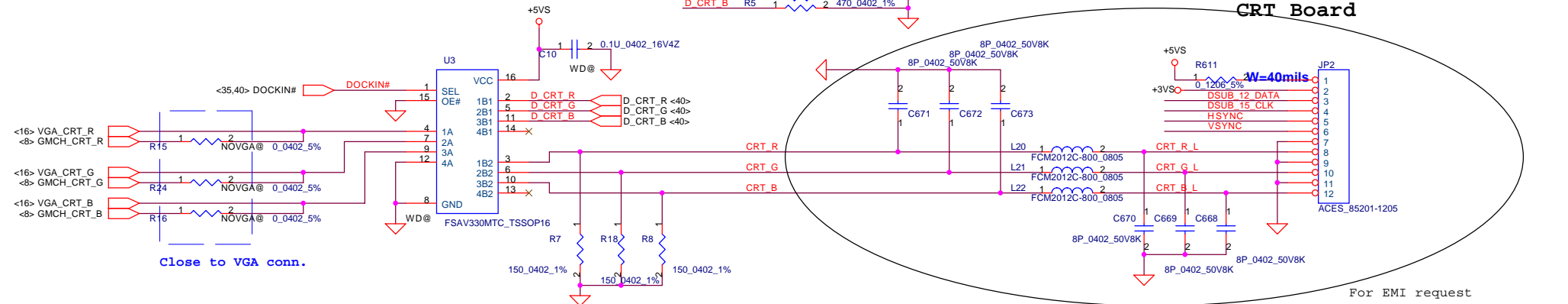
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Compal Electronics, Inc.		
Title Clock Generator		
Size	Document Number Boston LA-2721	Rev 1.0
Date	2005/5/6 下午 11:47:58	Sheet 14 of 53

CRT Connector

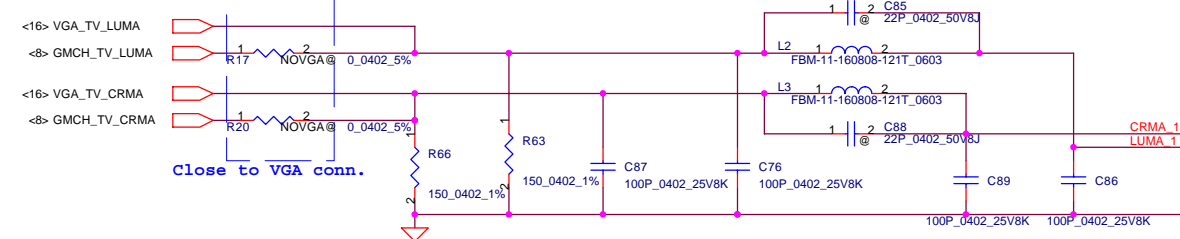
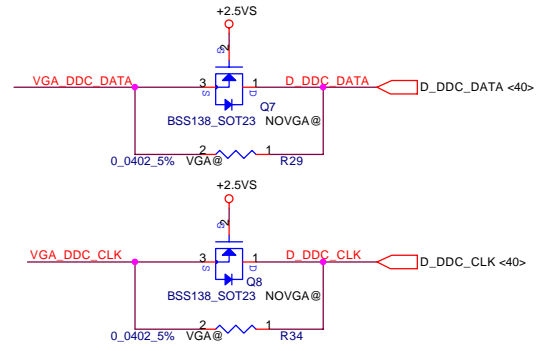
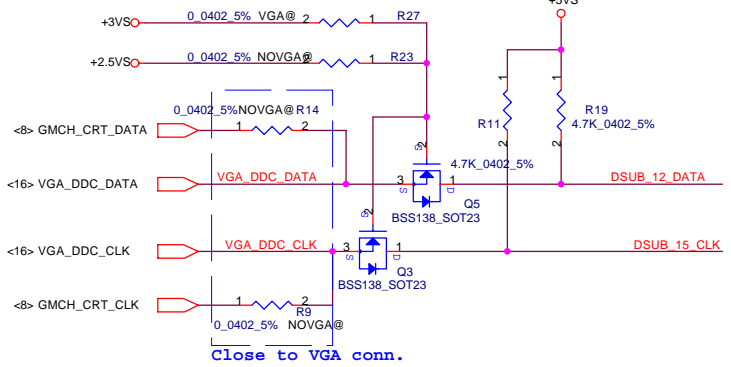
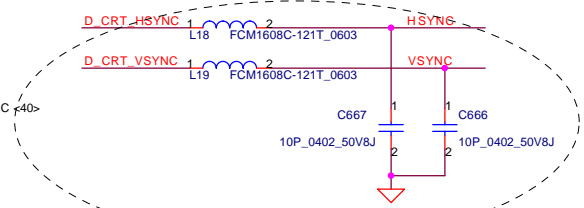
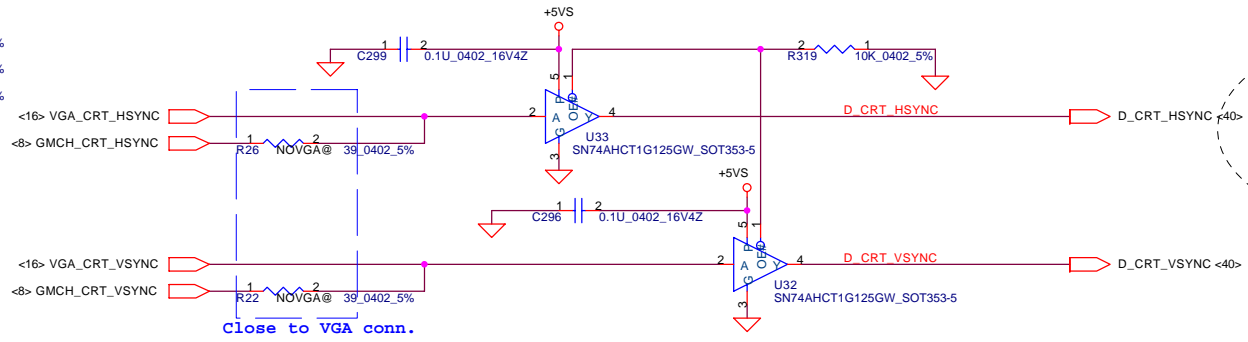
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CRT Board

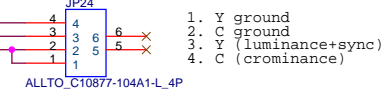


VGA CRT R 1 2 CRT R
 R10 WOD@ 0.0402_5%
 VGA CRT G 1 2 CRT G
 R21 WOD@ 0.0402_5%
 VGA CRT B 1 2 CRT B
 R12 WOD@ 0.0402_5%

Pop with No-Docking



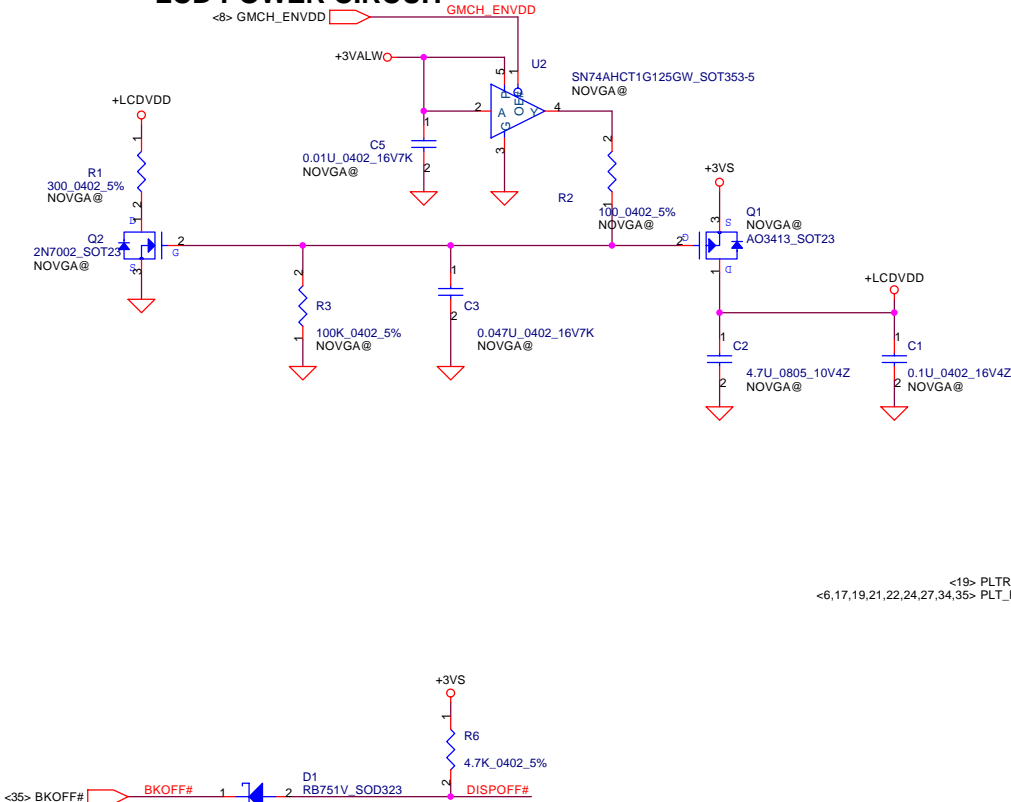
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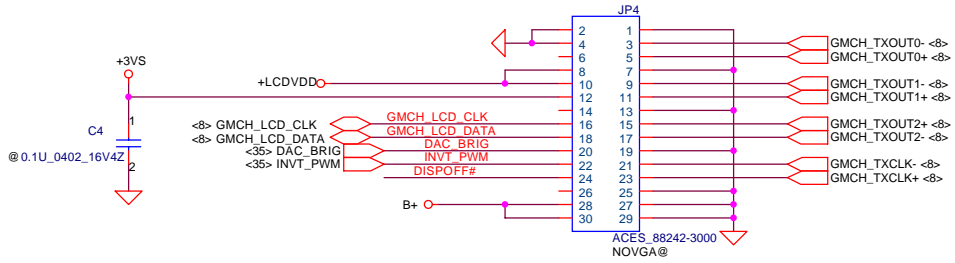
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Compal Electronics, Inc.		
Title		
CRT & TVout Connector		
Size	Document Number	Rev
	Boston LA-2721	1.0
Date:	2005/5/6 下午 11:47:56	Sheet 15 of 53

LCD POWER CIRCUIT

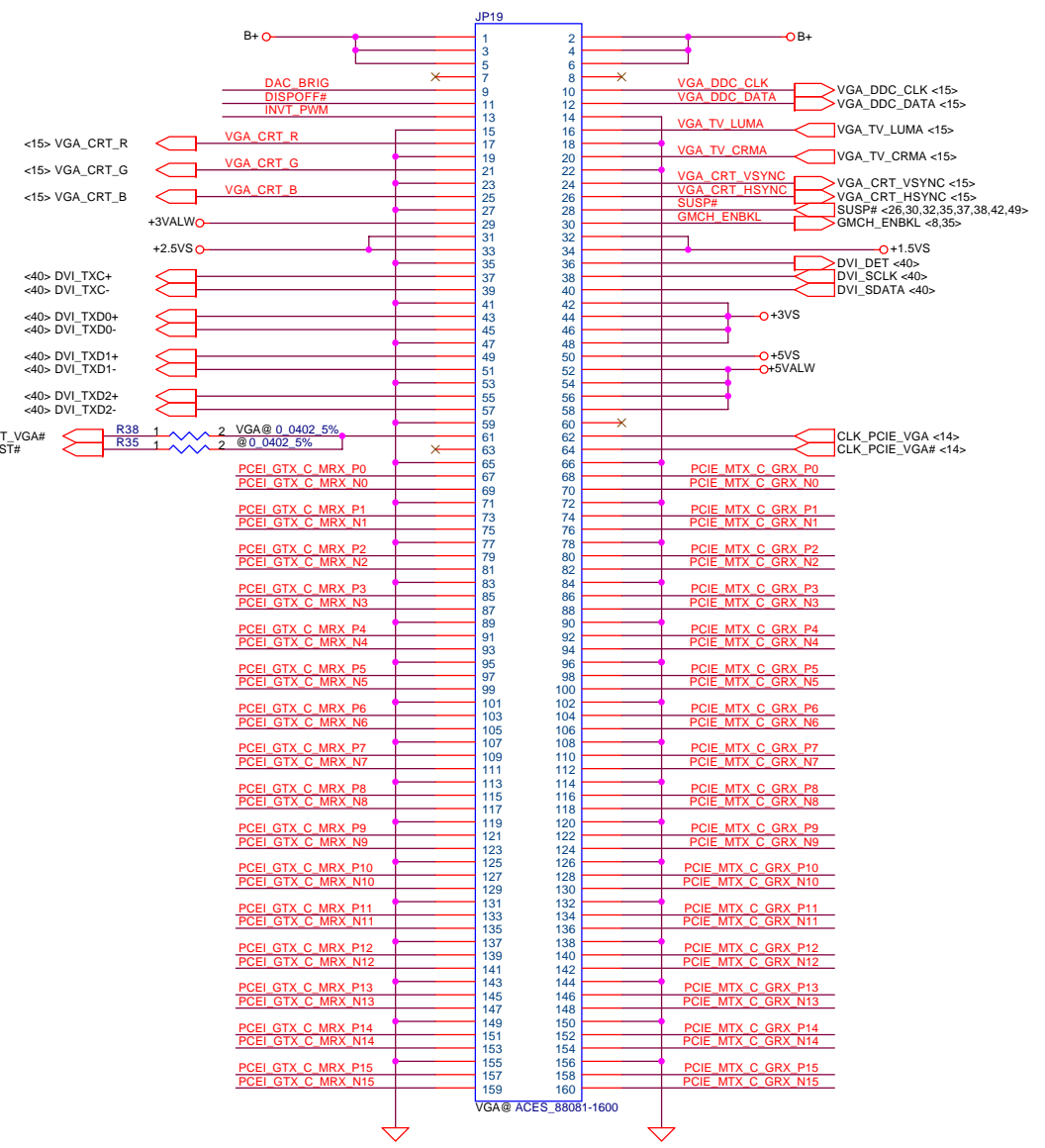


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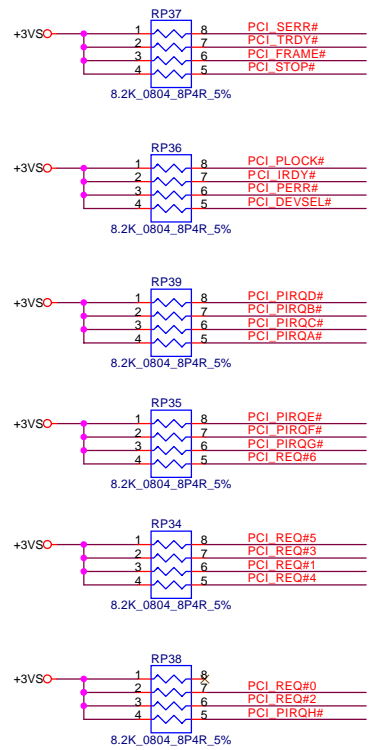


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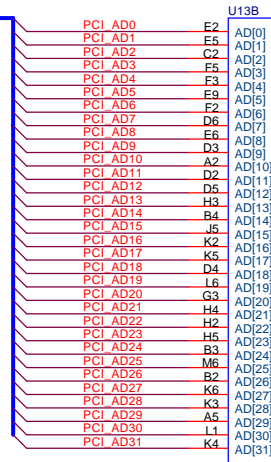
VGA BOARD Conn.



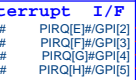
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Size	Document Number	Date:		Rev	
	Boston LA-2721	2005/5/6 下午 11:47:55		1.0	
				Sheet 16 of 53	



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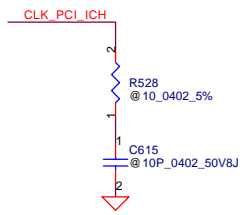
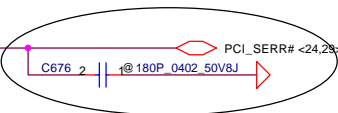
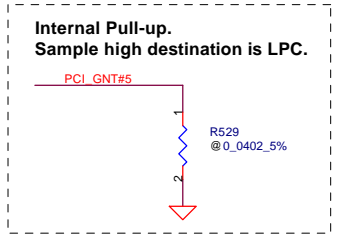
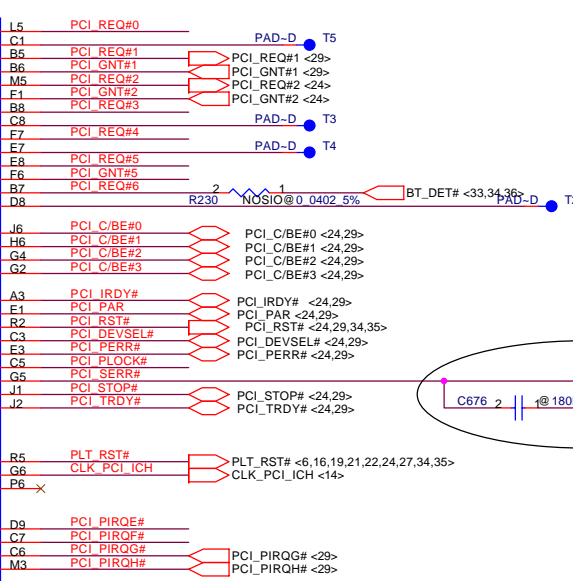
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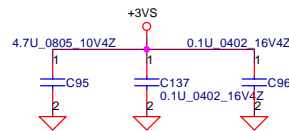
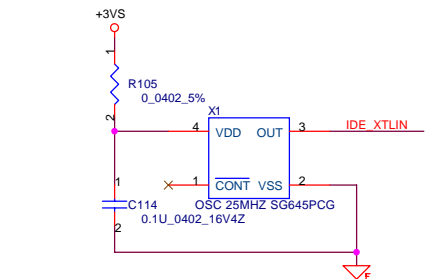
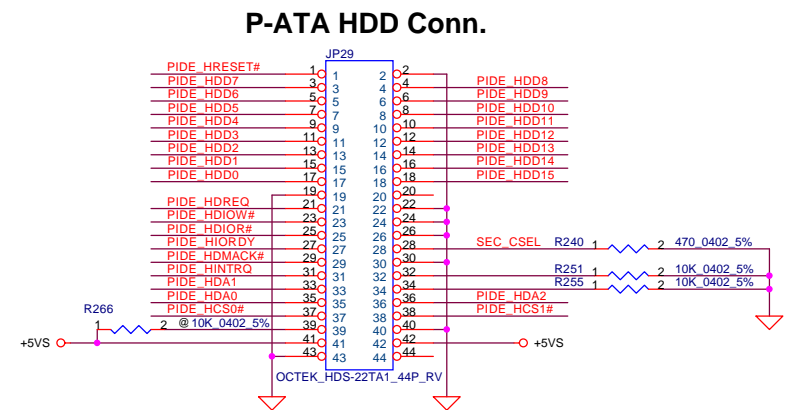
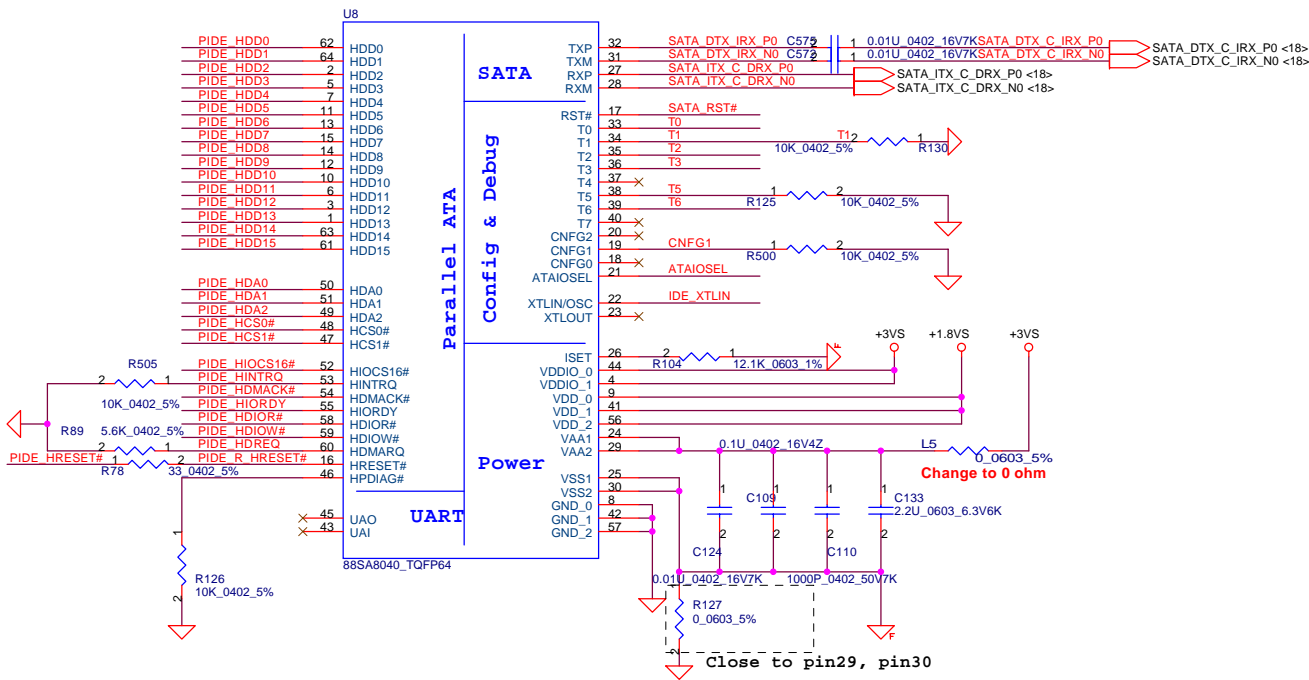
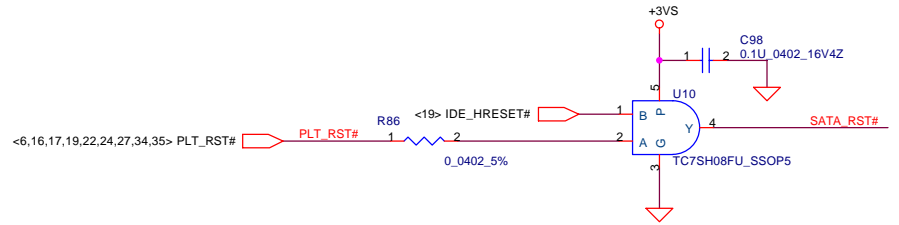
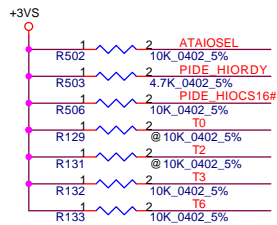
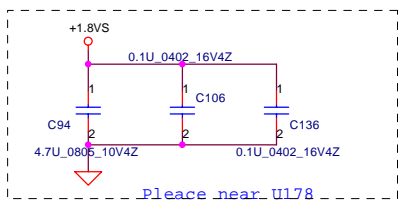
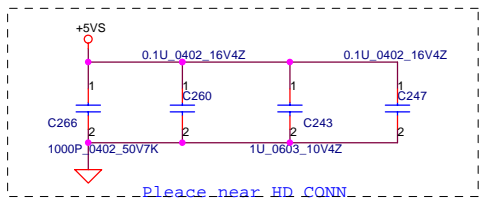
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- × AD5 SATA[1]RXP/RSVD[2]
- × AF4 SATA[1]TXN/RSVD[3]
- × AG4 SATA[1]TXP/RSVD[4]
- × AC9 SATA[3]RXN/RSVD[5]
- × AD9 SATA[3]RXP/RSVD[6]
- × AF8 SATA[3]TXN/RSVD[7]
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- × U3 TP[3]/RSVD[9]

R3S8@ ICH6_BGA609

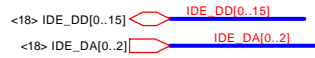
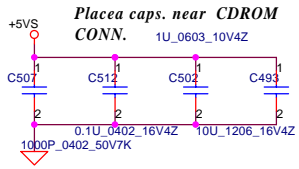


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Date:	2005/5/6 下午 11:47:55	Sheet	17	of	53

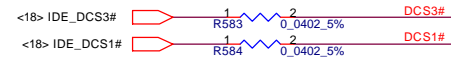
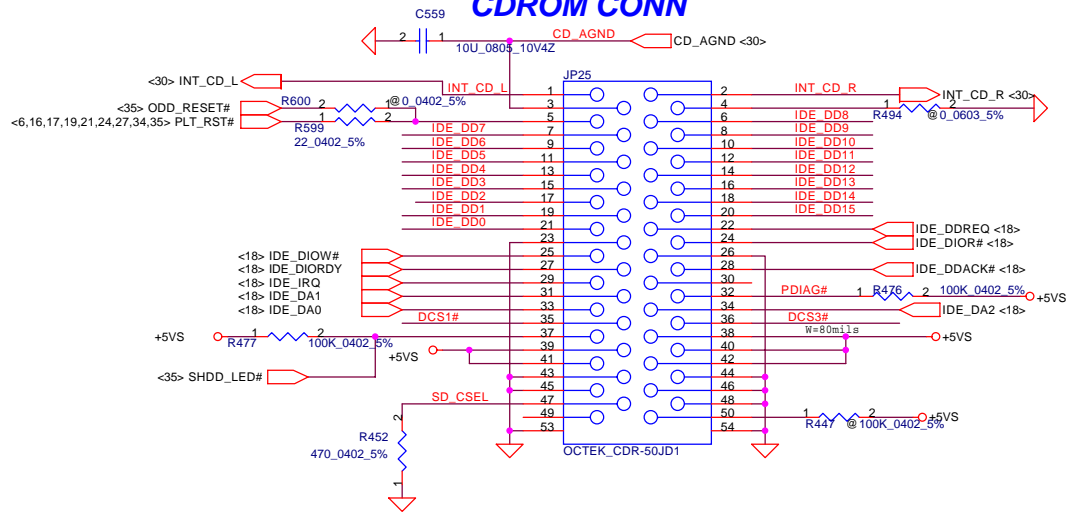


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Date:	2005/5/6 下午 11:47:58	Sheet	21	of	53



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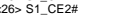




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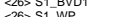

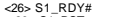
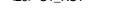
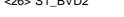
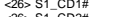
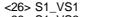

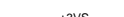



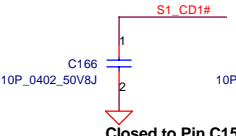
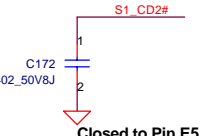
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				Date:	2005/5/6 下午 11:47:54
				Sheet	22 of 53
				Rev	1.0

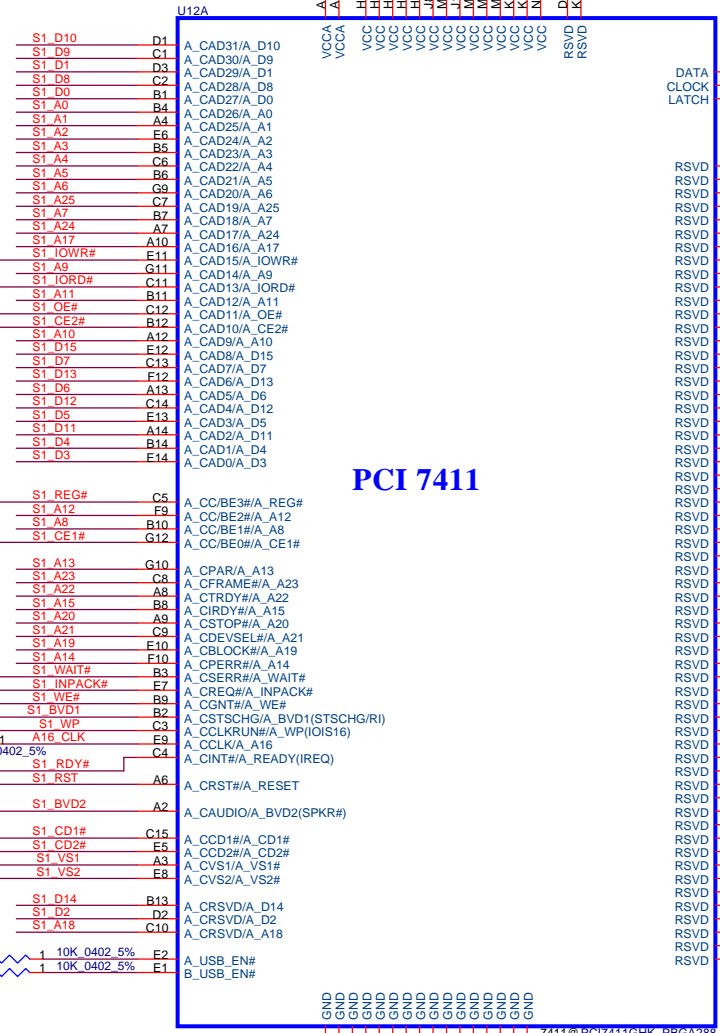
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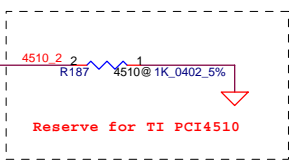
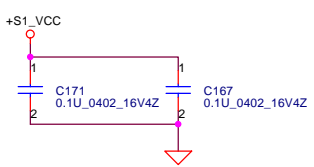
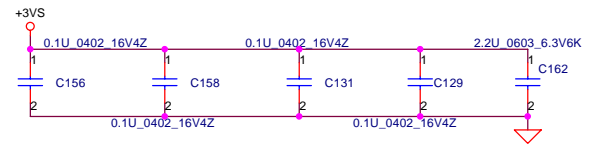
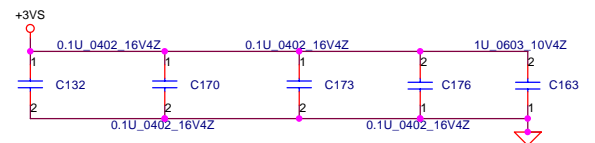





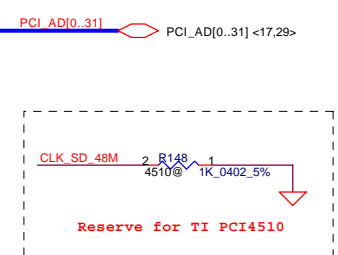
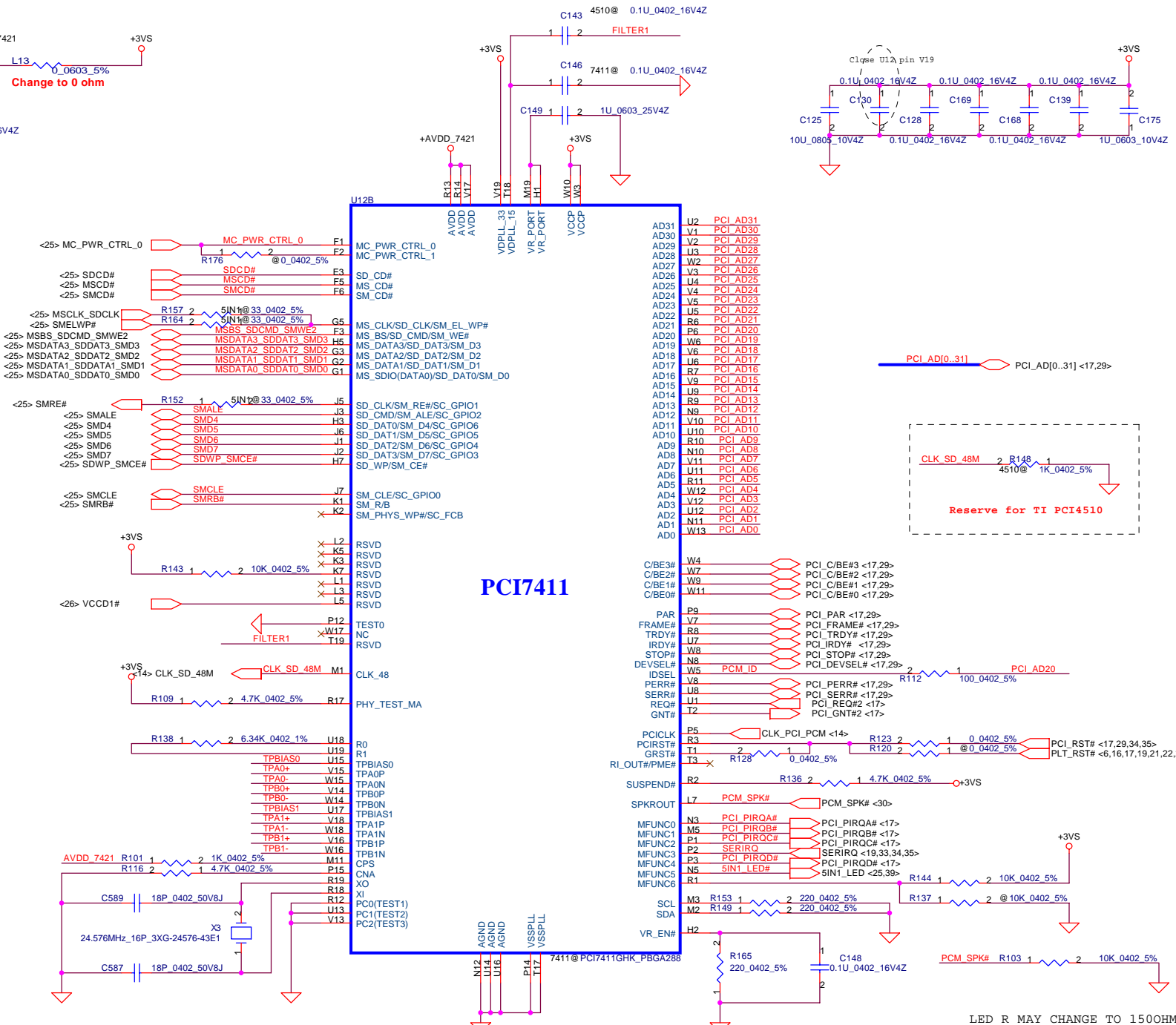
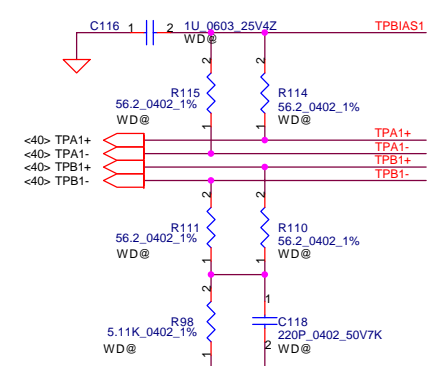
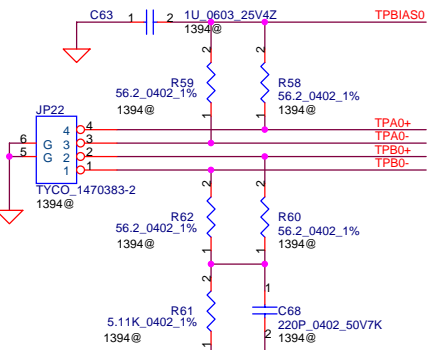
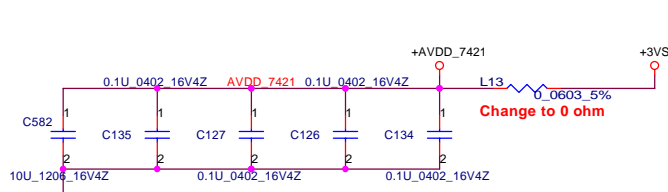
PCI 7411

7411@PCI7411GHK_PBGA288

DATA N1
 CLOCK L6
 LATCH N2
 DATA <26>
 CLOCK <26>
 LATCH <26>



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Date:	2005/5/6 下午 11:47:55	Sheet	23	of	53

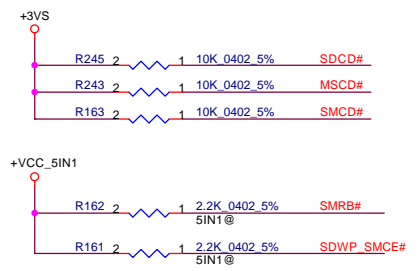
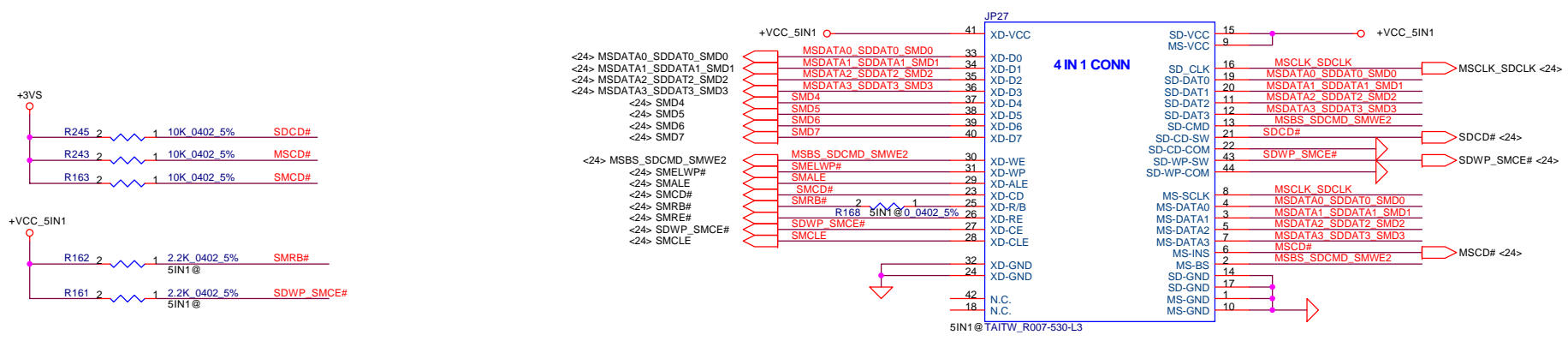


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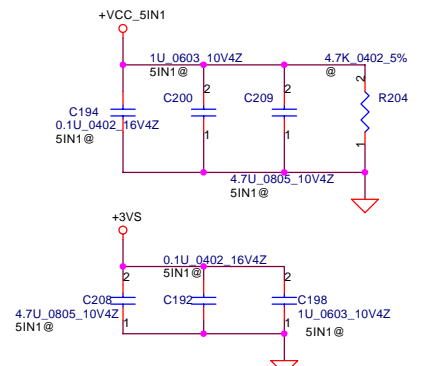
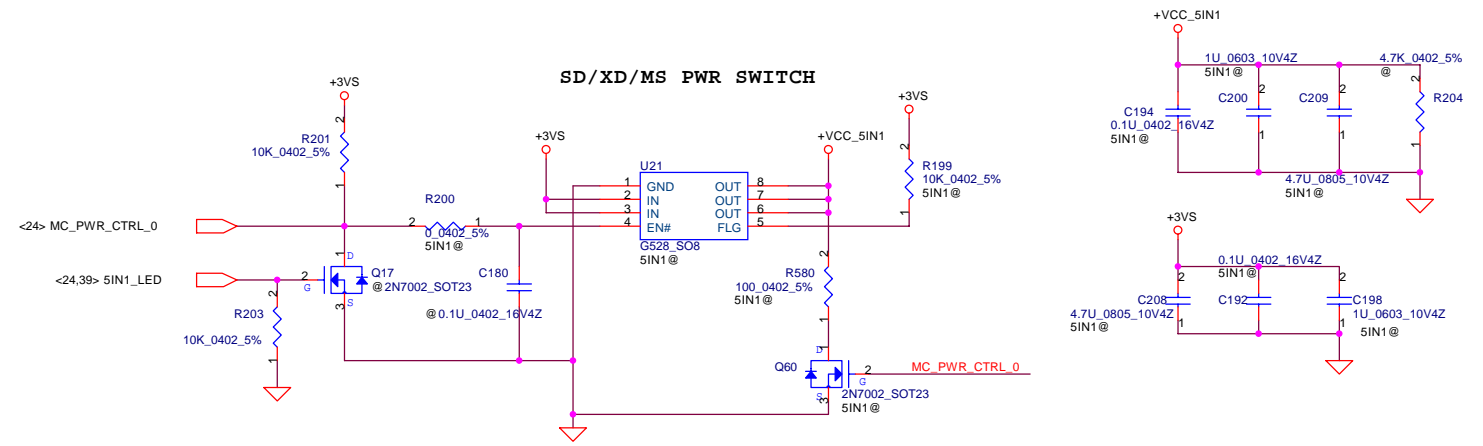
LED R MAY CHANGE TO 150OHM

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Date:	2005/5/6 下午 11:47:54	Sheet	24	of	53

5 in 1 CardReader Conn.



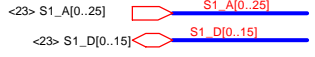
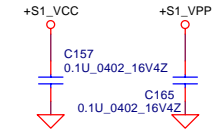
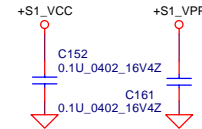
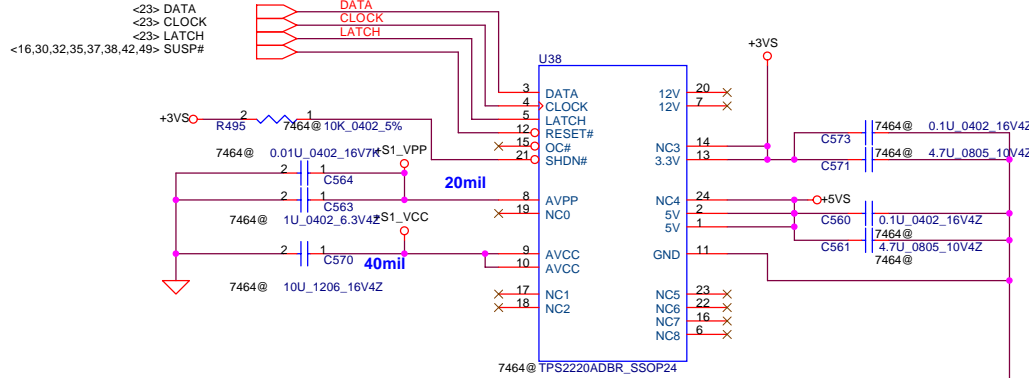
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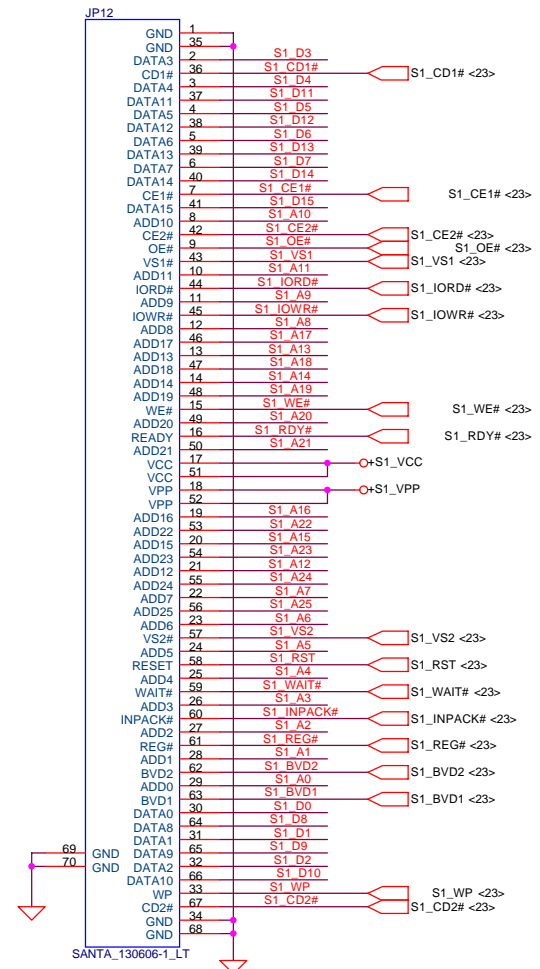
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Size	Document Number			Rev	
	Boston LA-2721			1.0	
Date:	2005/5/6 下午 11:47:58	Sheet	25	of	53

Power Switch for PCMCIA

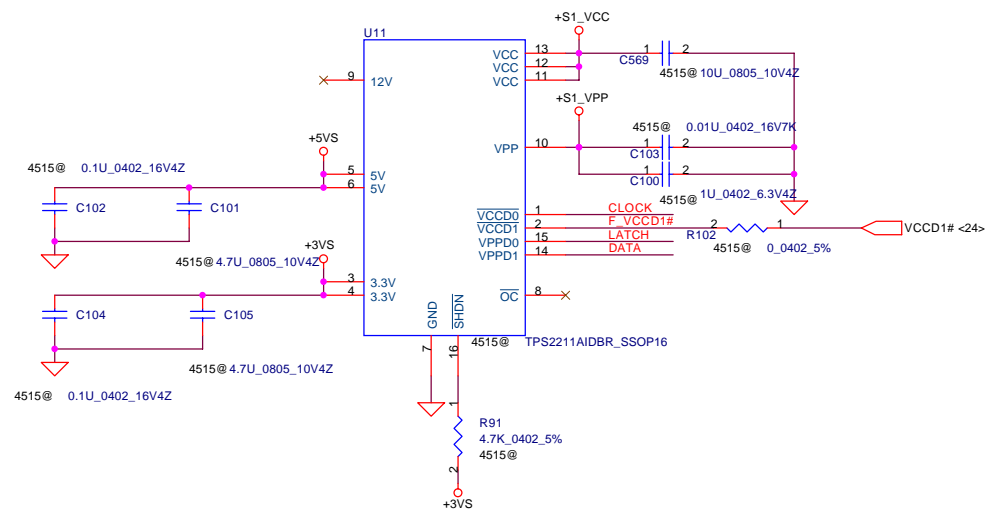
For 7411



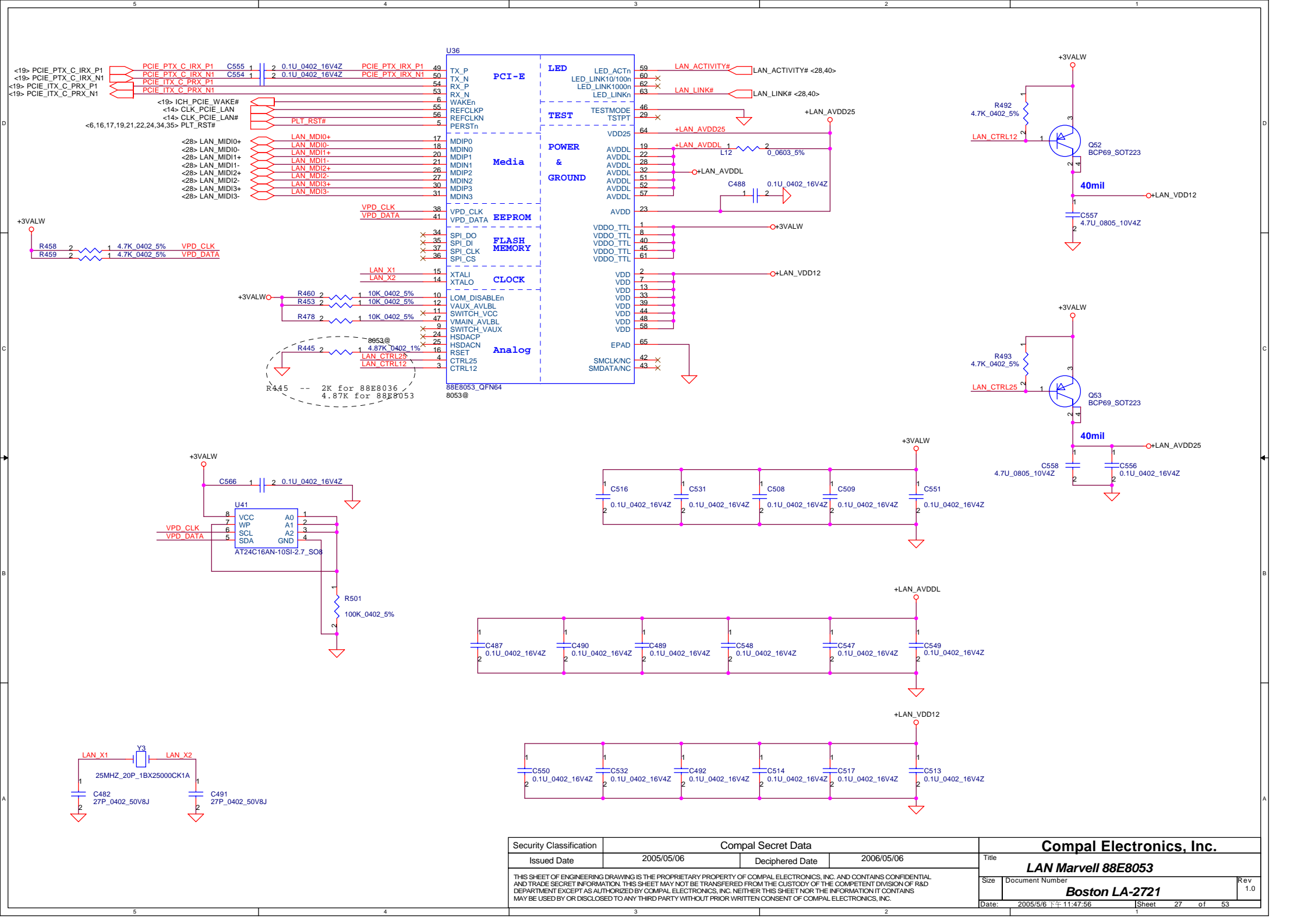
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For 4510

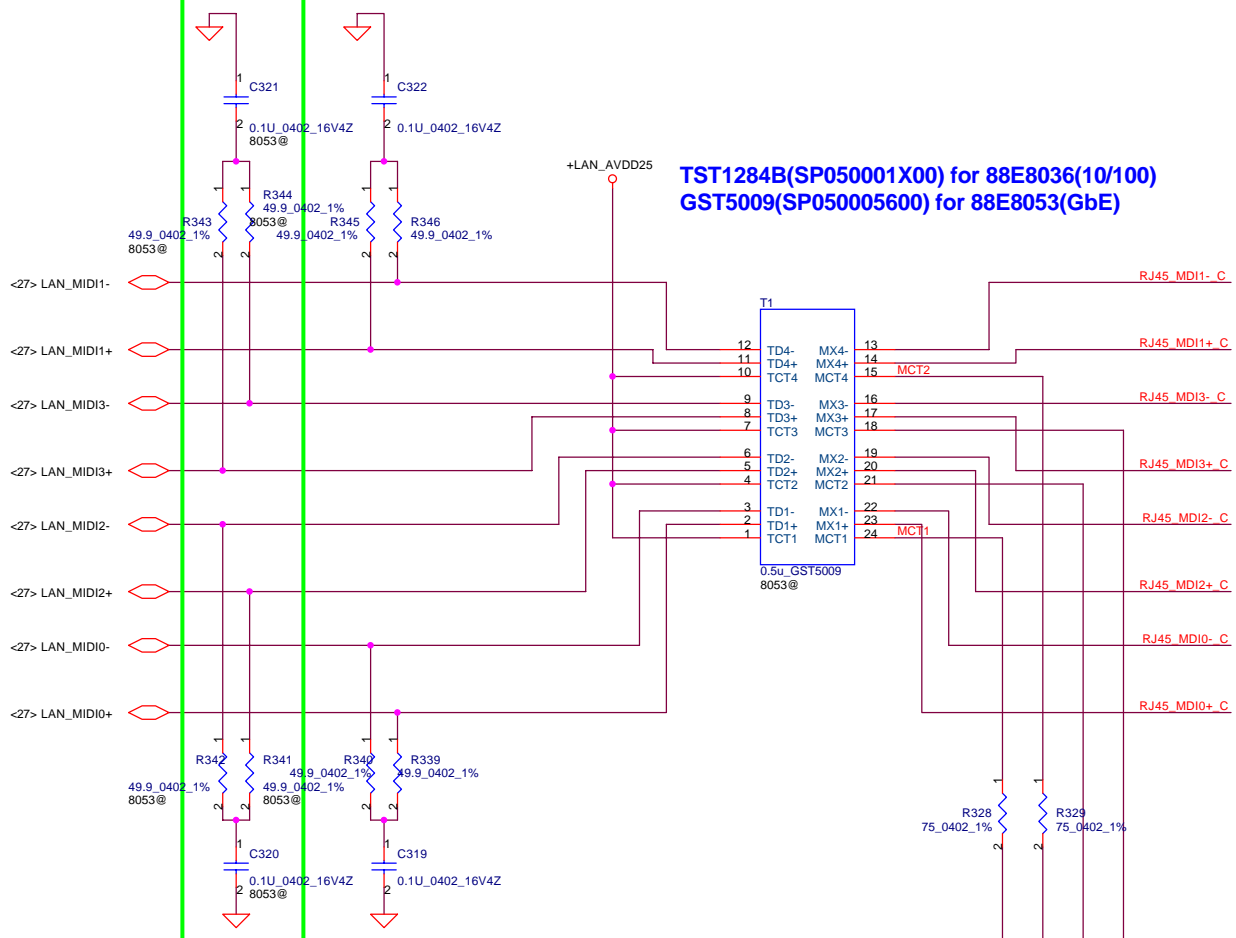


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Date:	2005/5/6	Time:	11:47:54	Sheet 26 of 53

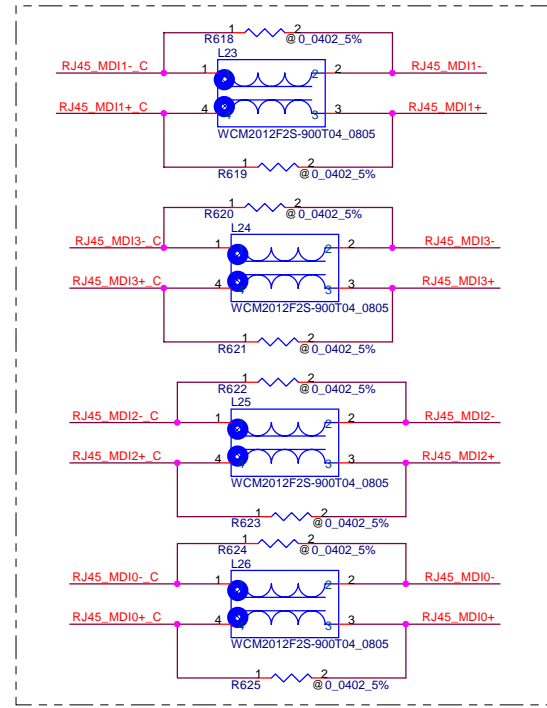
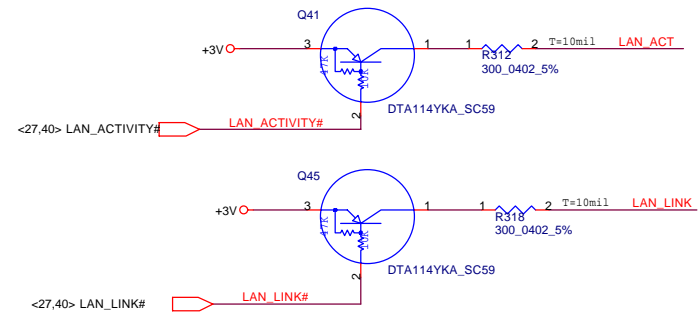
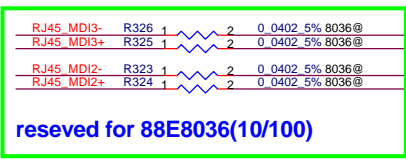


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Date:	2005/5/6 下午 11:47:56	Sheet	27	of	53
Rev	1.0				

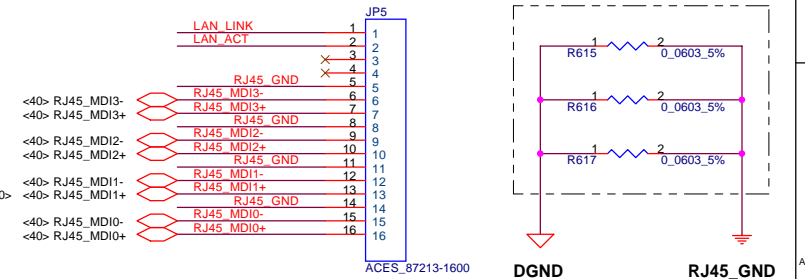
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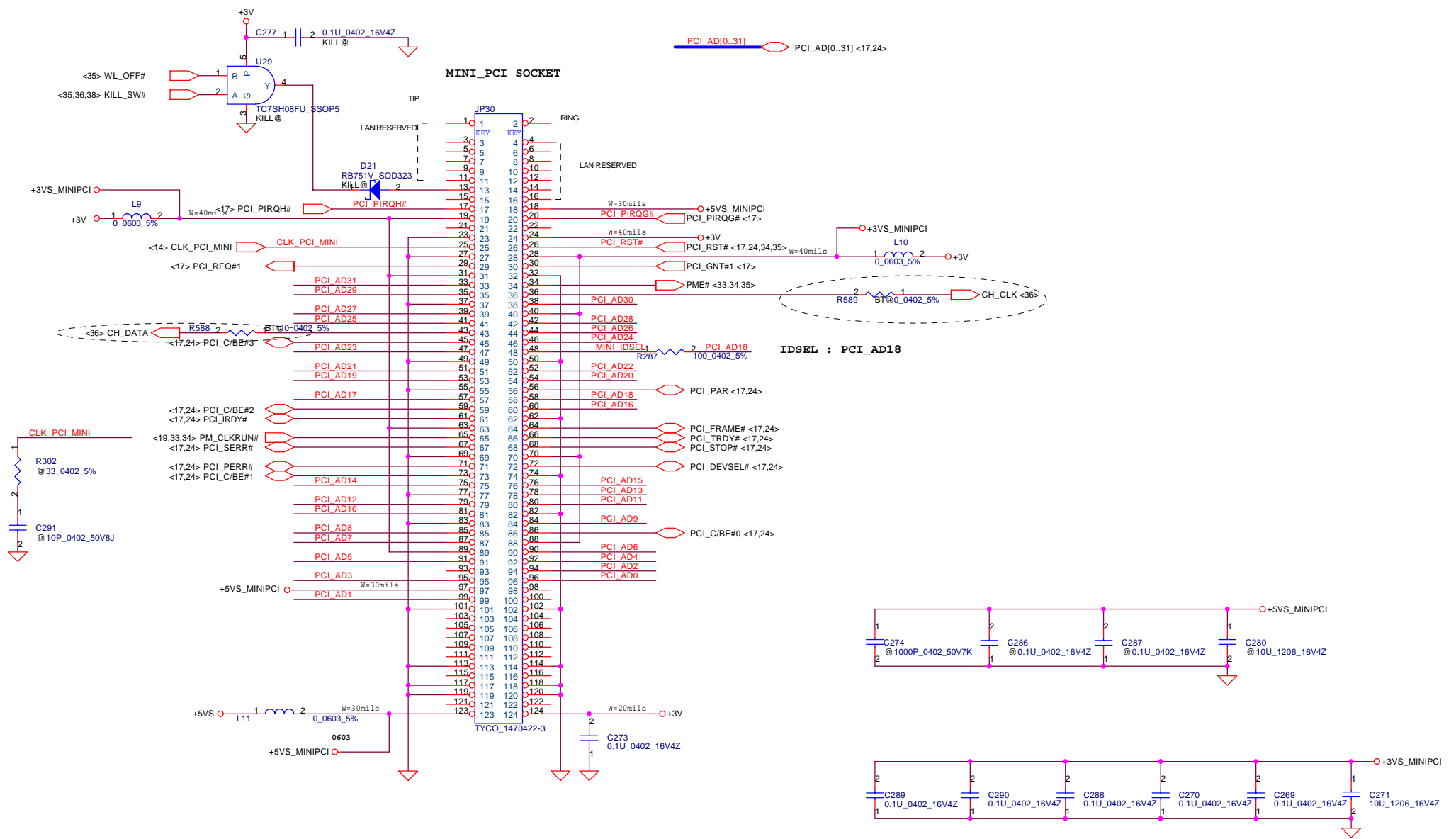
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GST5009(SP050005600) for 88E8053(GbE)



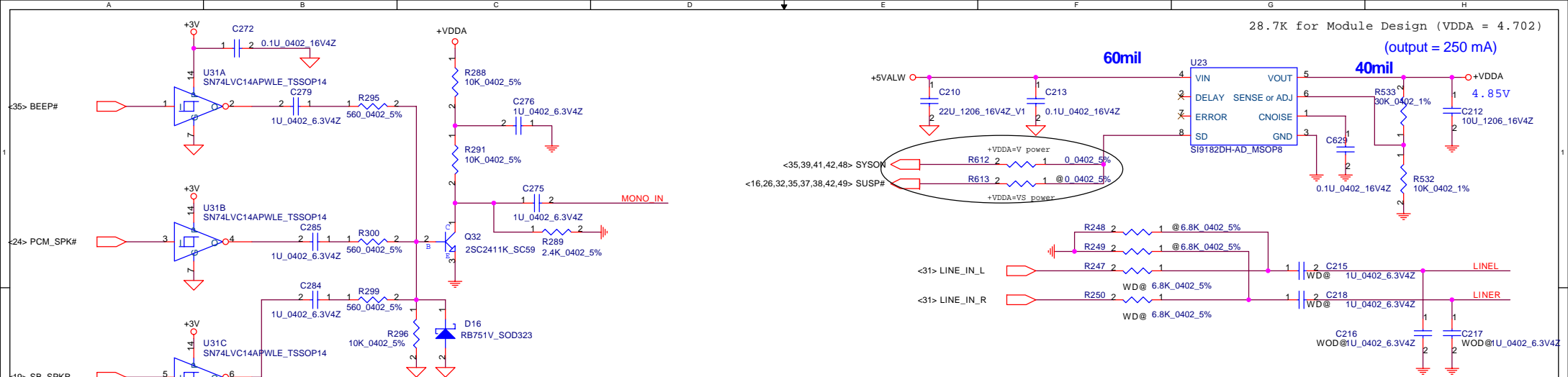
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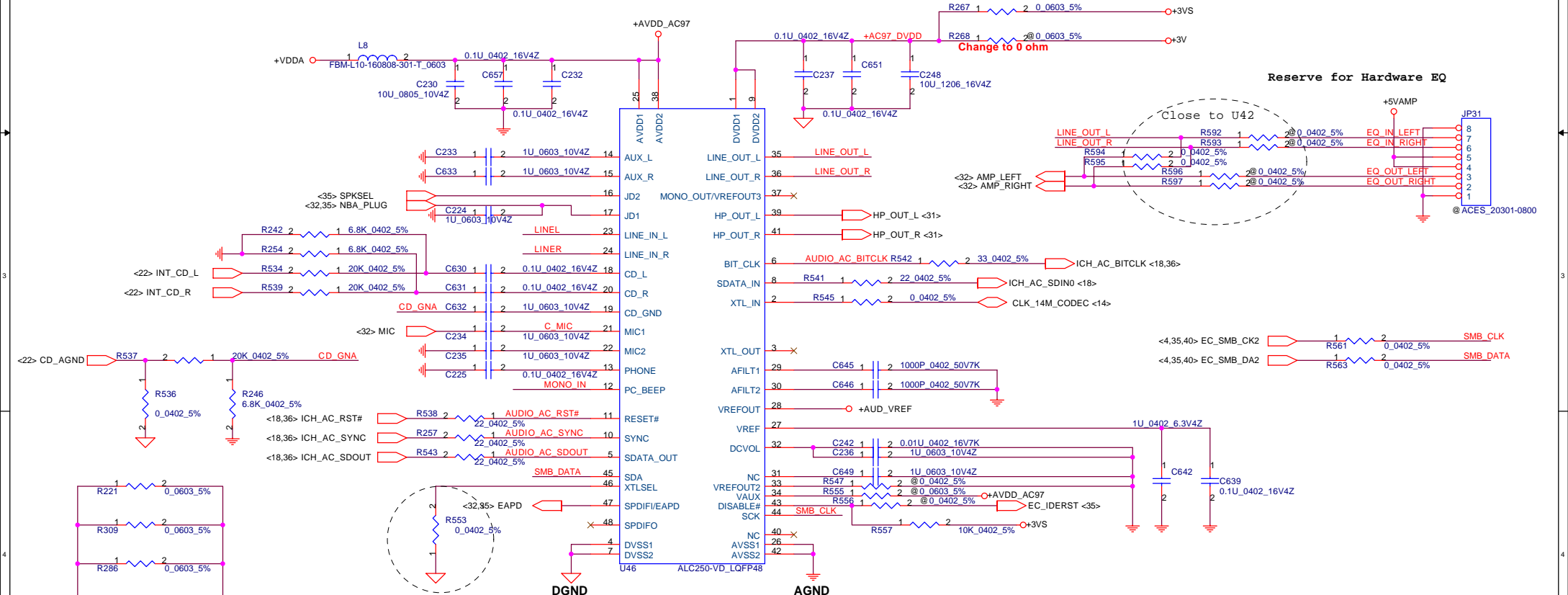
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Date:	2005/5/6 下午 11:47:55	Sheet	28 of 53	Rev	1.0



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Date:	2005/5/6 下午 11:47:56	Sheet	29	of	53
				Rev	1.0



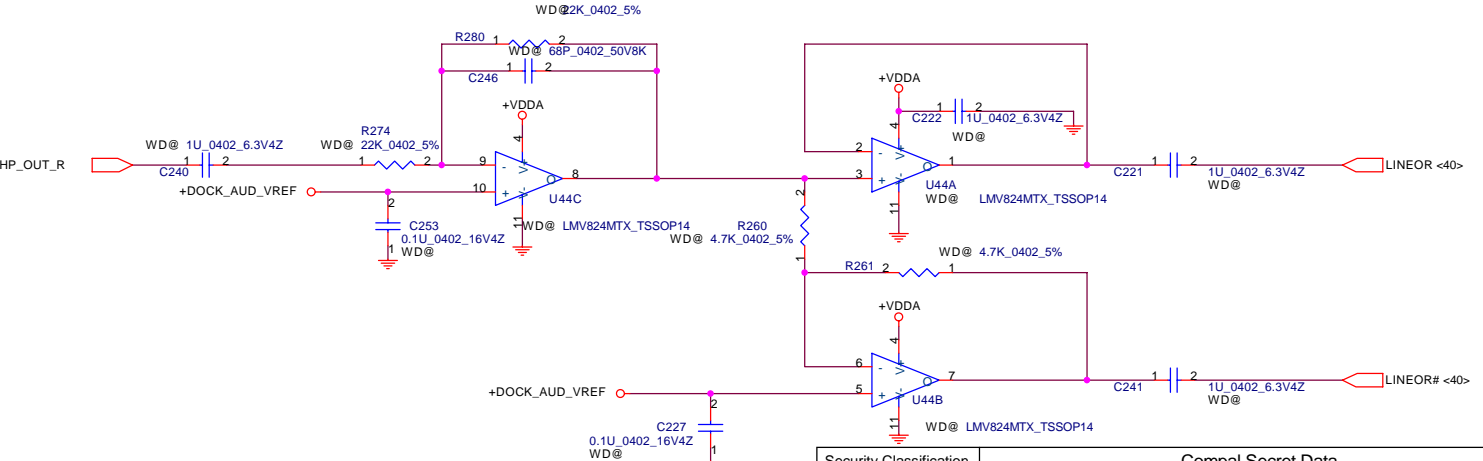
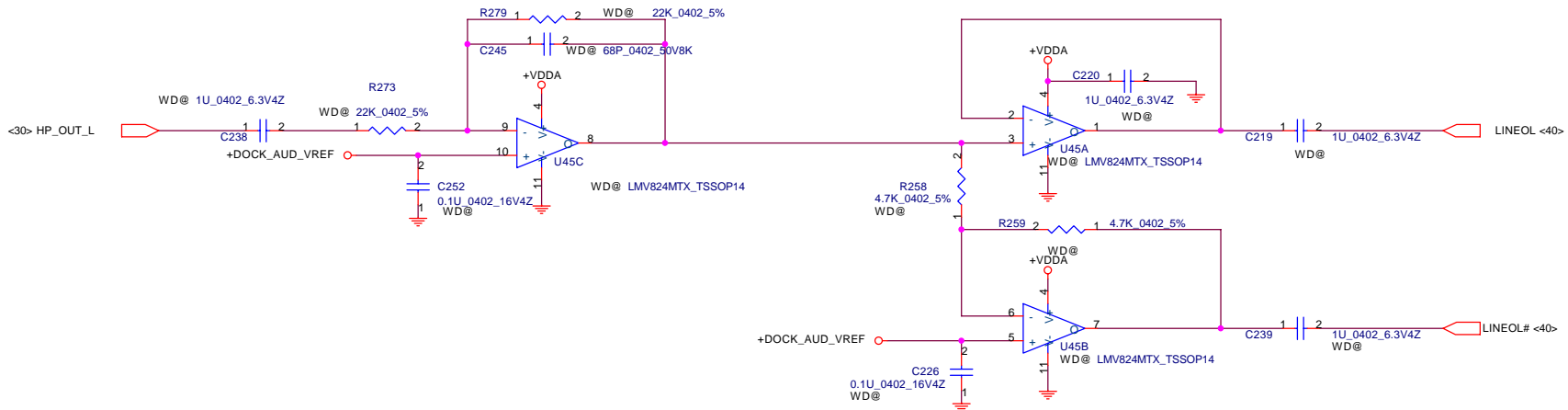
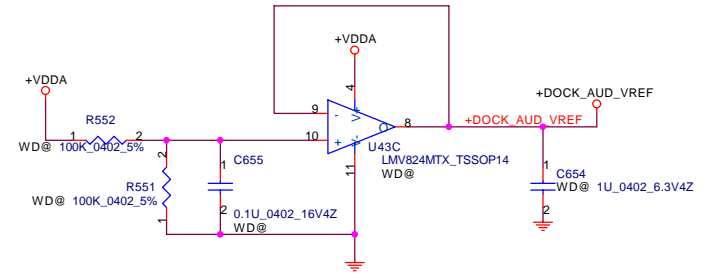
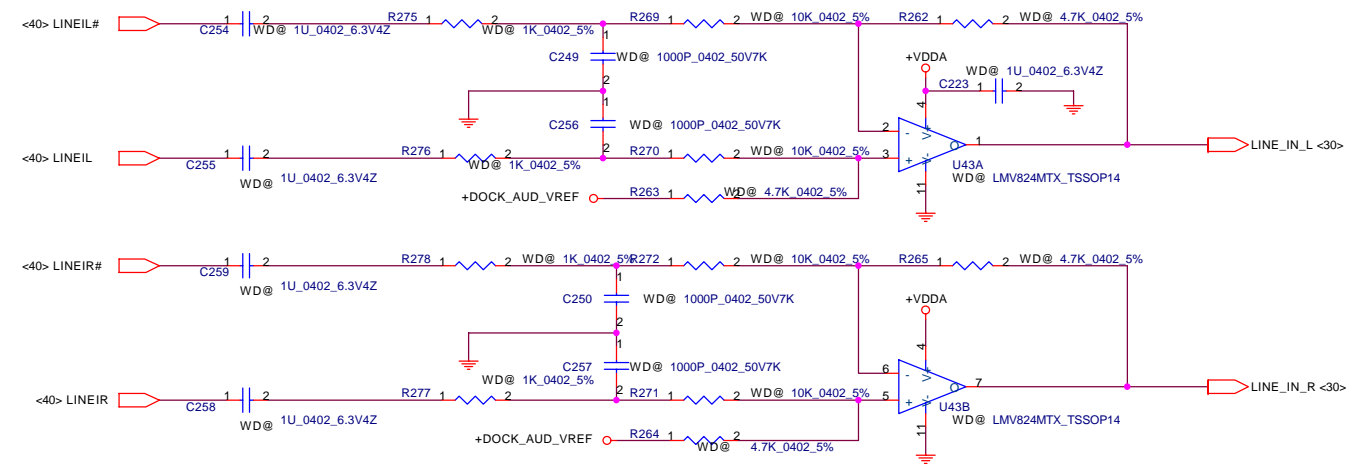
AC97 Codec



With 14.318Mhz : R553 POP
With 24.576Mhz : R553 DEPOP

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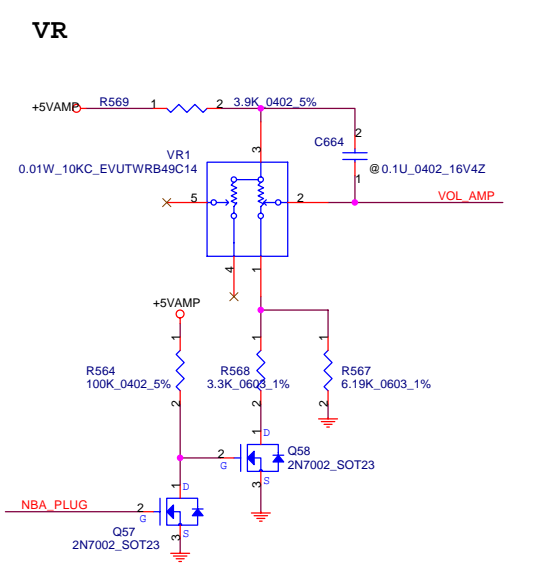
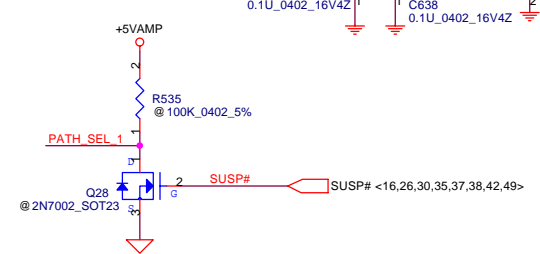
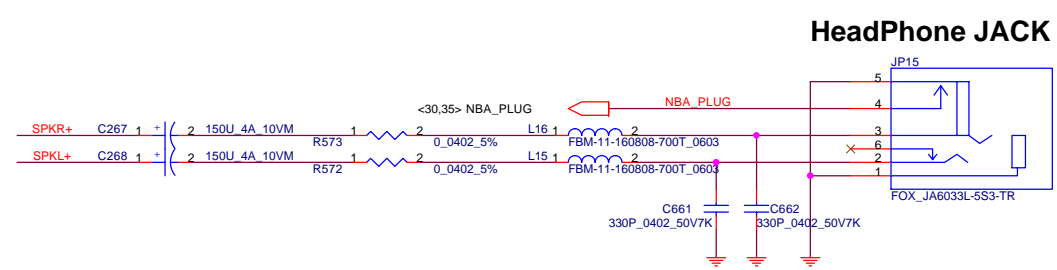
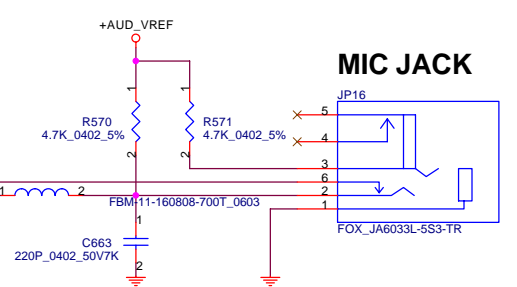
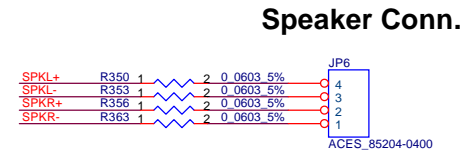
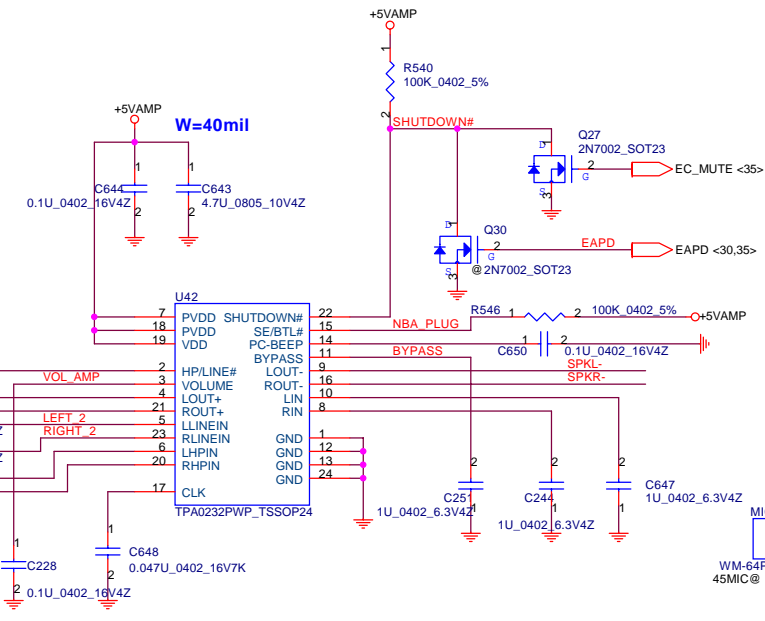
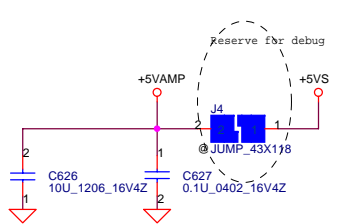
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Title AC97 CODEC			
Size	Document Number	Rev	
	Boston LA-2721	1.0	
Date:	2005/5/6 下午 11:47:55	Sheet	30 of 53



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Compal Electronics, Inc.		
Title Docking Audio		
Size	Document Number Boston LA-2721	Rev 1.0
Date:	2005/5/6 下午 11:47:57	Sheet 31 of 53

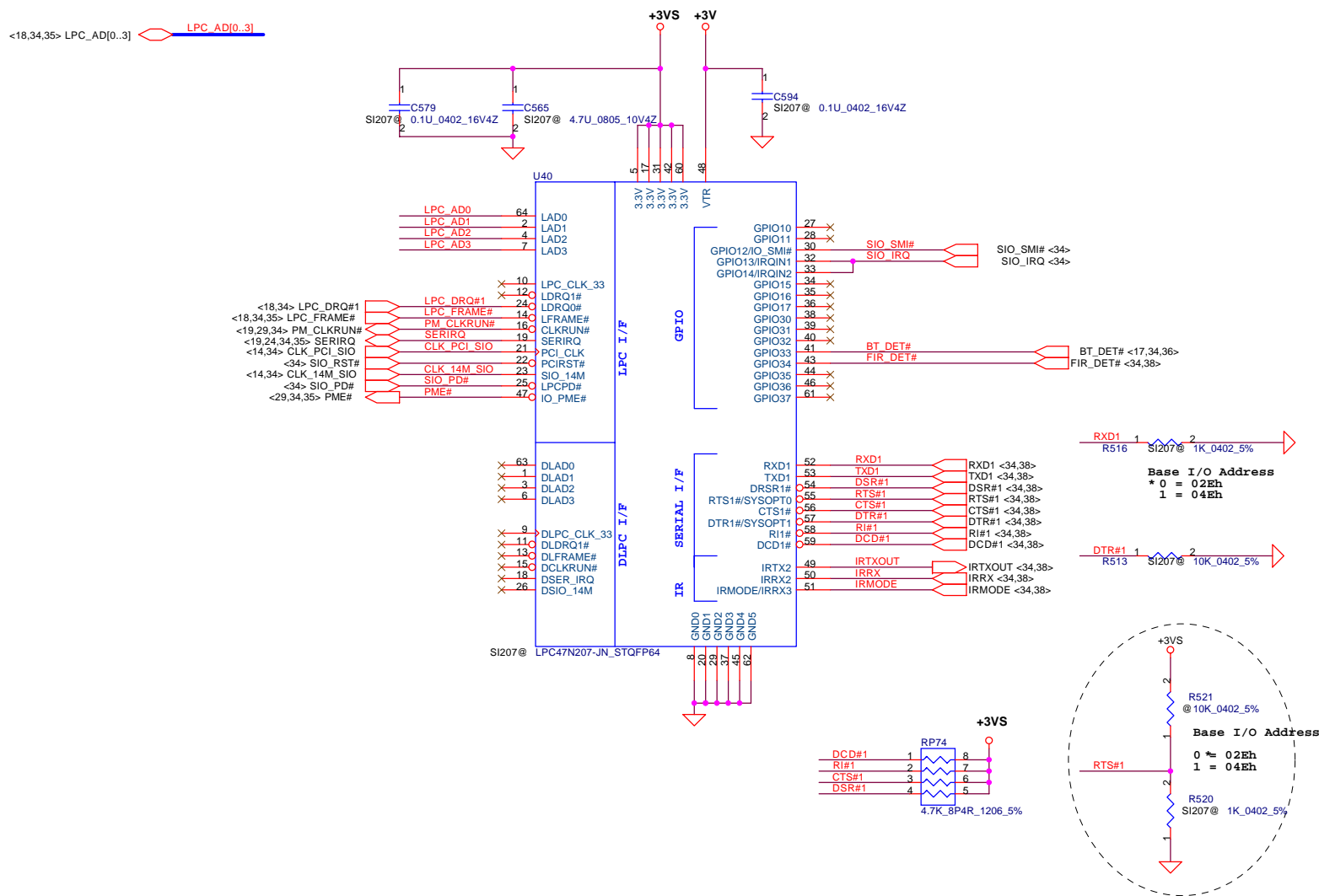
PROPRIETARY NOTE



R569	3.9K
R568	3.3K
R567	6.19K
Bias (Gain)	SPK 0.67 V 10 dB HP 1.54 V -6 dB

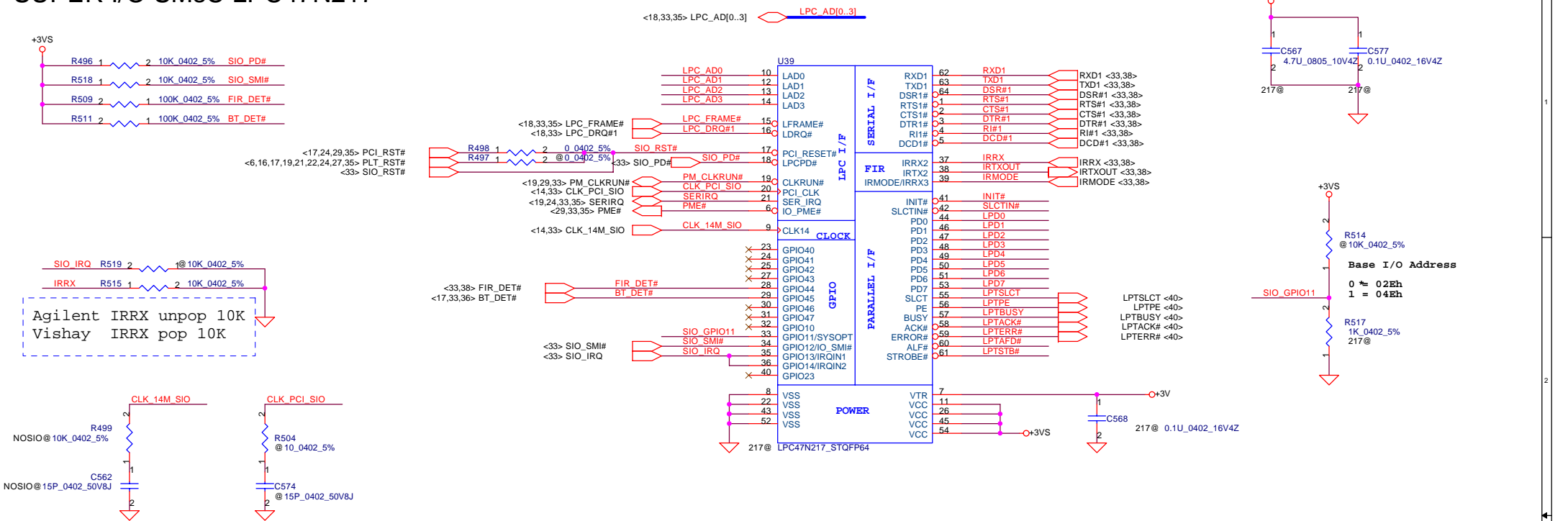
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Issued Date	2005/05/06	Deciphered Date	2006/05/06	Title AMP & Audio Jack	
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Date:	2005/5/6 下午 11:47:54	Sheet	32 of 53	Rev	1.0

SUPER I/O SMC LPC47N207

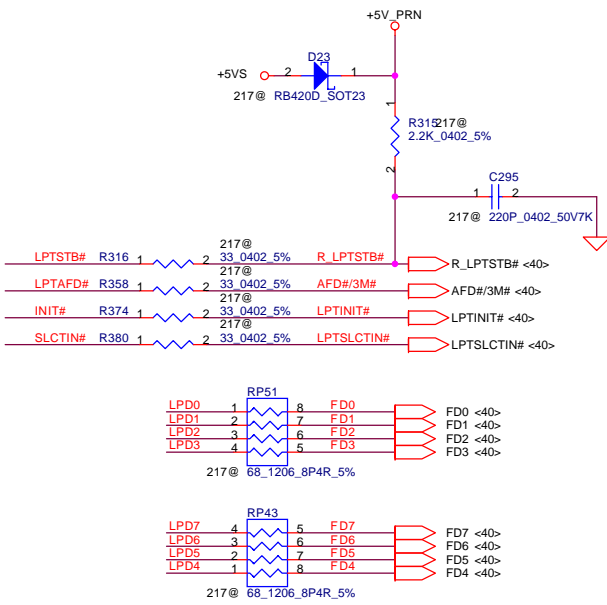


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2005/05/06	Deciphered Date	2006/05/06	Title LPC-Super I/O 207	
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Date:	2005/5/6 下午 11:47:57	Sheet	33 of 53	Rev	1.0

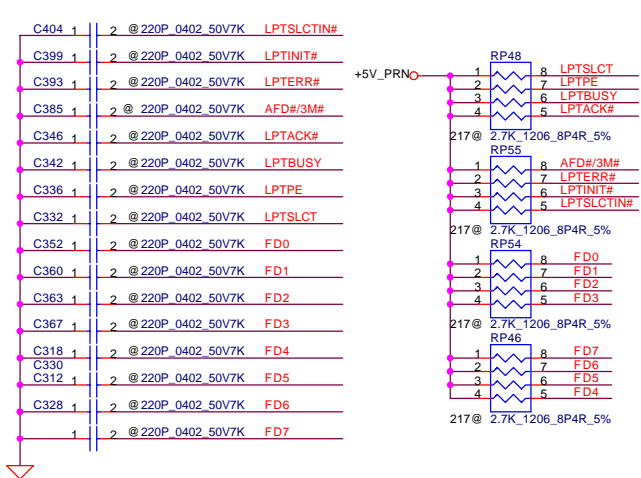
SUPER I/O SMC LPC47N217



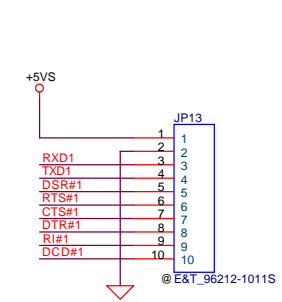
Docking Parallel Port



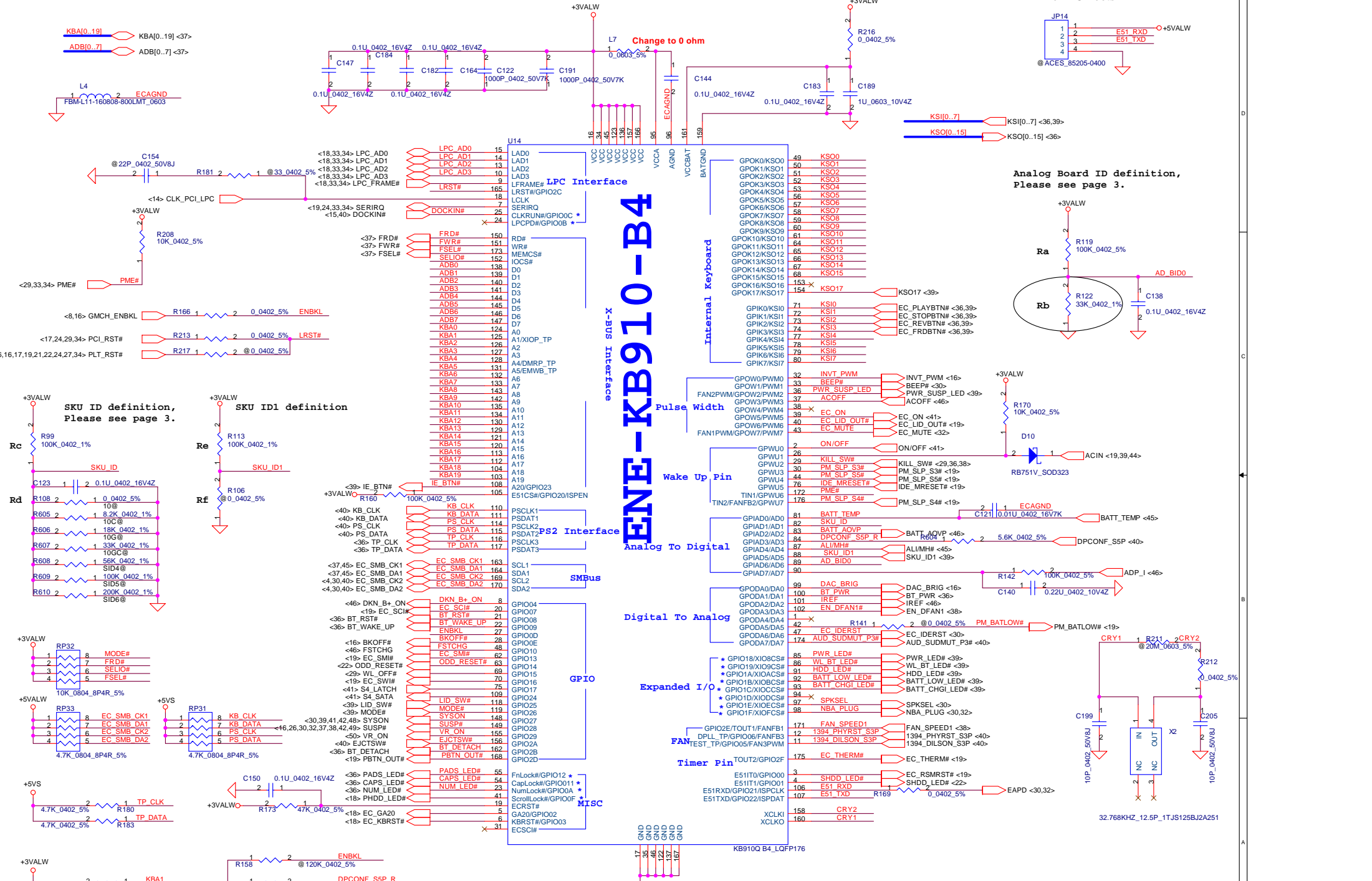
Close to Docking



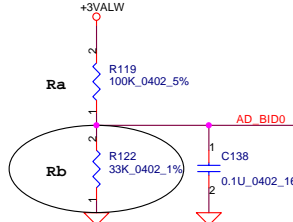
Serial Port for Debug



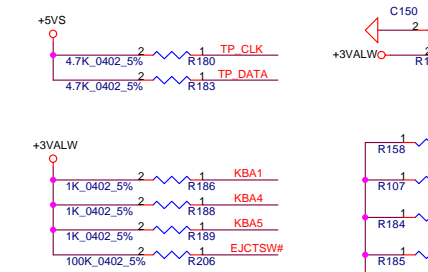
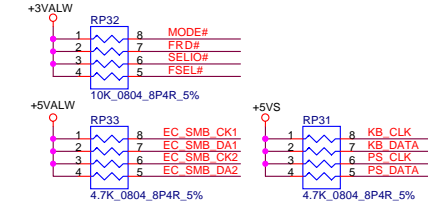
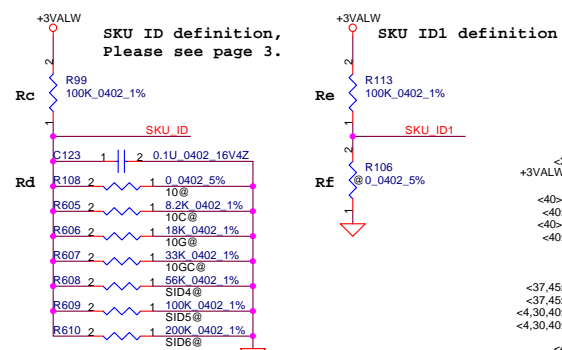
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Size	Document Number	Rev		1.0	
Boston LA-2721		Date:	2005/5/6 下午 11:47:57	Sheet	34 of 53



Analog Board ID definition, Please see page 3.



SKU ID definition, Please see page 3.

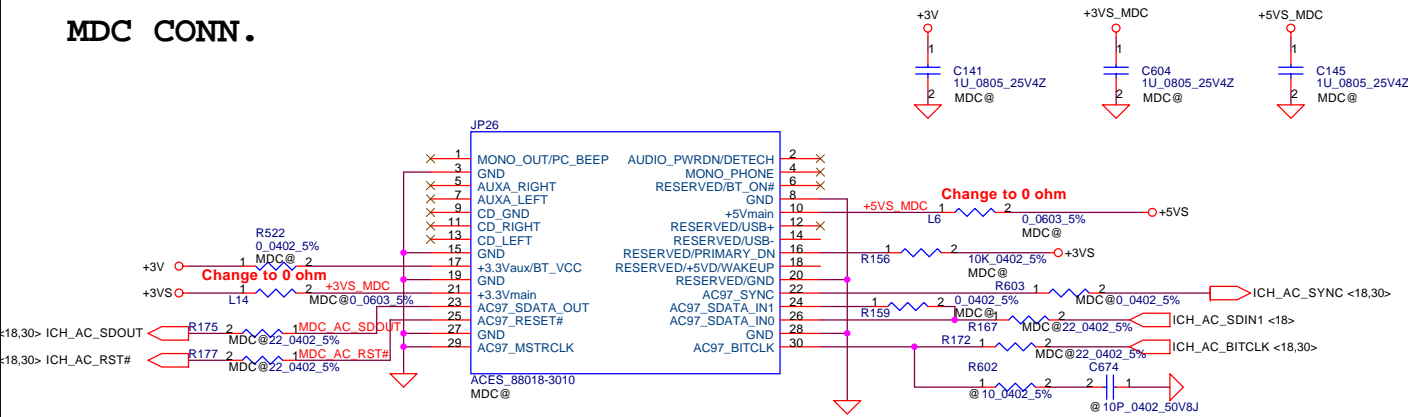


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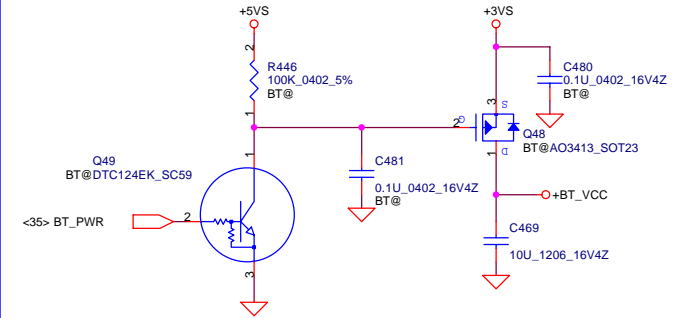
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Compal Electronics, Inc.			
ENE-KB910			
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	Boston LA-2721		1.0
Date:	2005/5/6 下午 11:47:54	Sheet	35 of 53

MDC CONN.

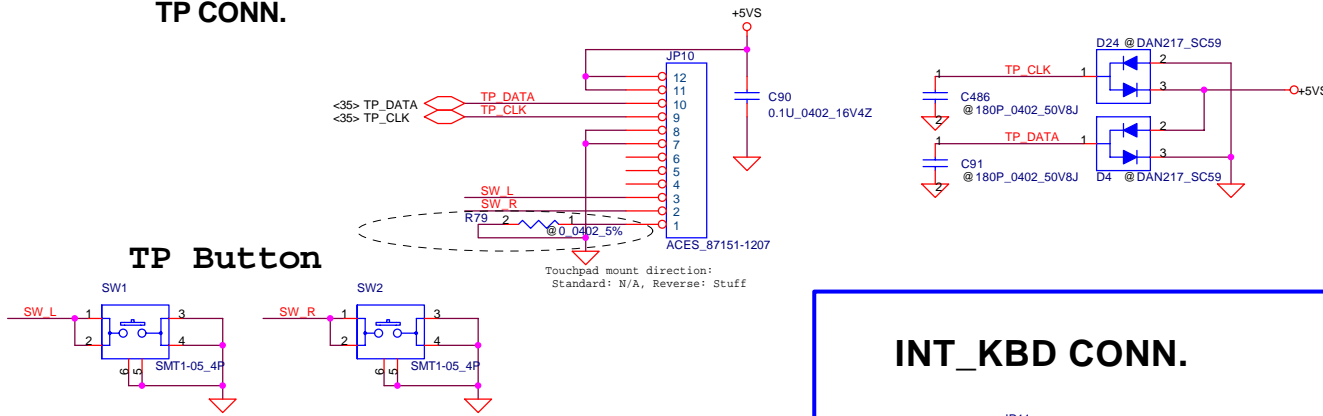


BlueTooth Interface

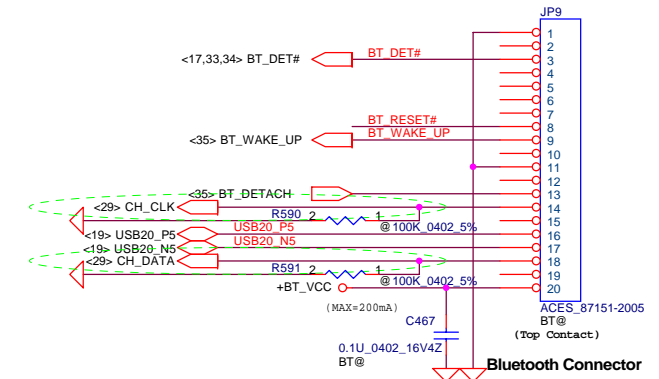
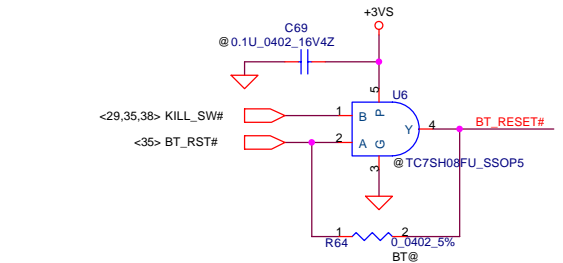
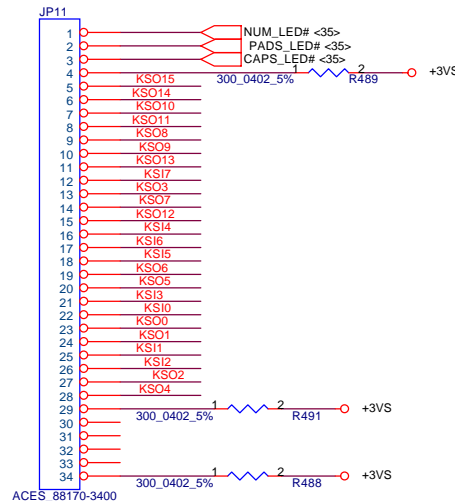
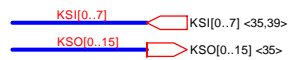


Module ID
Indication for polarity of reset
Reset input High Active --> Low,
Reset input Low Active --> Open

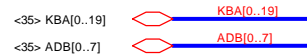
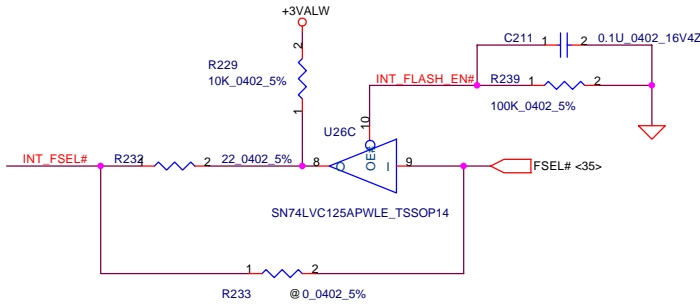
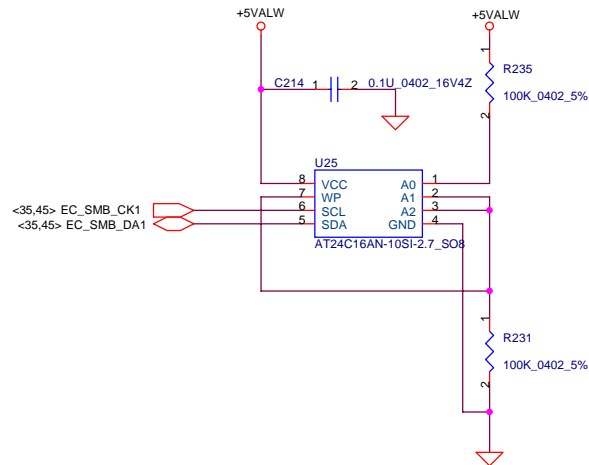
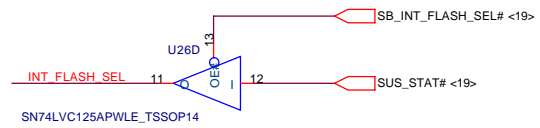
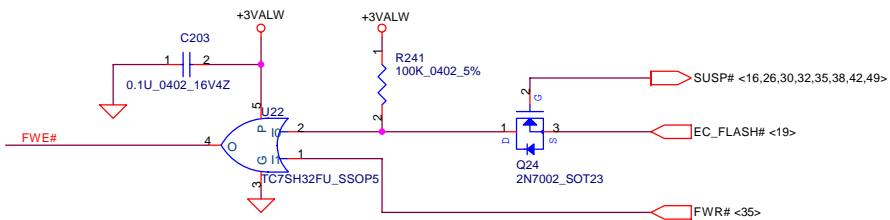
TP CONN.



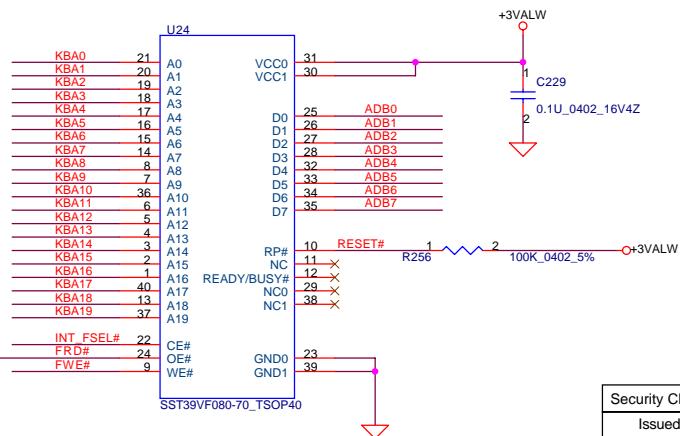
INT_KBD CONN.



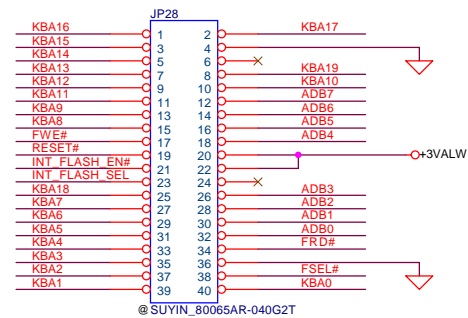
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Size	Document Number	Boston LA-2721		Rev 1.0
Date:	2005/5/6 下午 11:47:58	Sheet	36	of 53



1MB Flash ROM

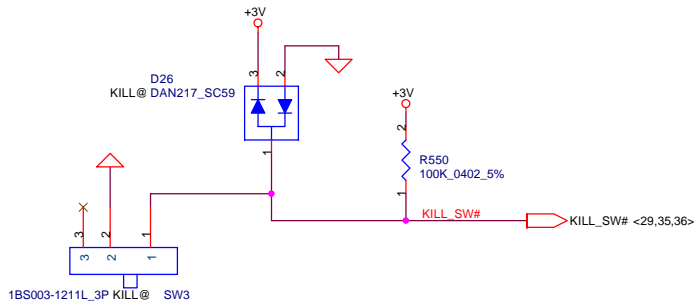


1MB ROM Socket

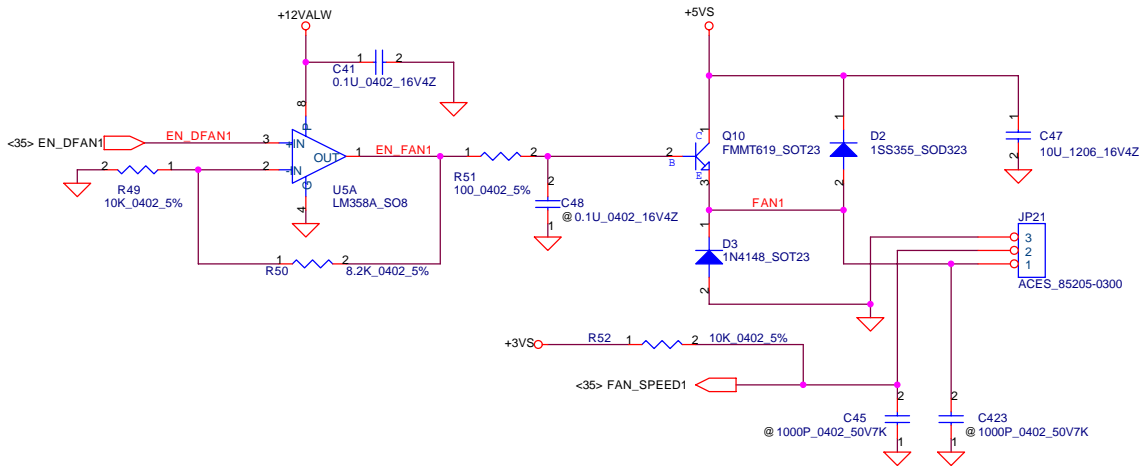


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Size	Document Number	Boston LA-2721		Rev
Date:	2005/5/6 下午 11:47:56	Sheet	37 of 53	1.0

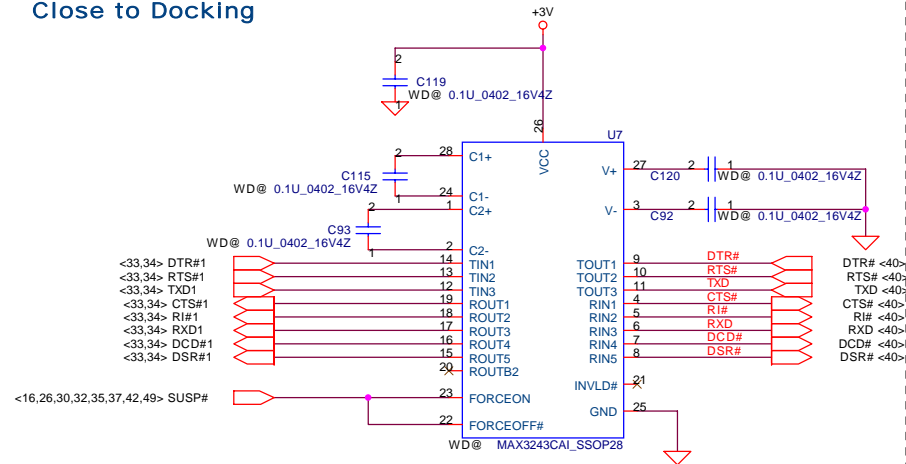
Kill Switch



FAN Conn

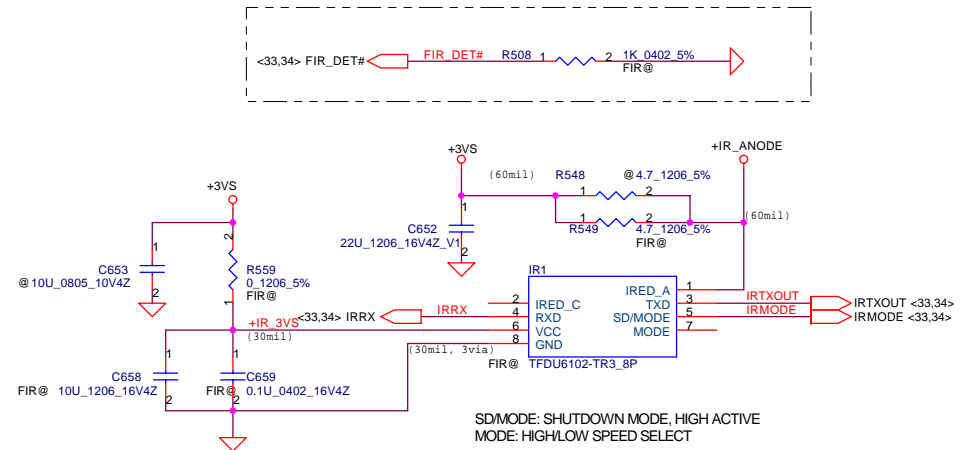


Close to Docking



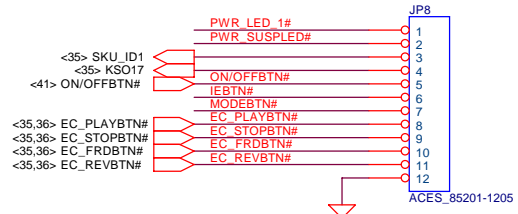
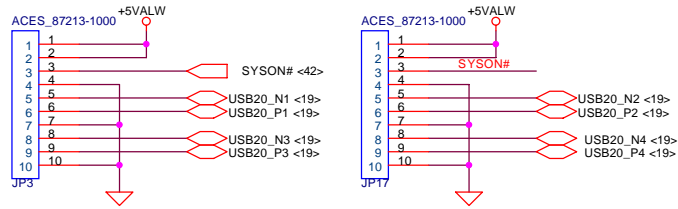
FIR Module

L: R POP; FIR Enable
H: R De-POP/FIR Disable



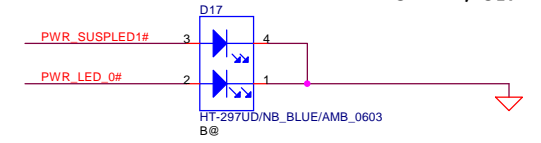
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				Document Number
				Boston LA-2721
				Rev 1.0
				Date: 2005/5/6 下午 11:47:56
				Sheet 38 of 53

USB Board Conn.

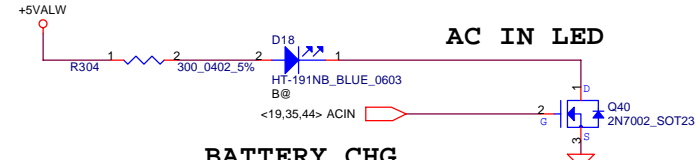


Component	Value	Pin 1	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	Pin 9	Pin 10	Pin 11	Pin 12
KSO17													
ON/OFFBTN#	C432	1	2	220P_0402_50V7K	C441	1	2	220P_0402_50V7K					
PWR_LED 1#					C447	1	2	220P_0402_50V7K					
PWR_SUSPLED#	C444	1	2	220P_0402_50V7K	C429	1	2	220P_0402_50V7K					
IEBTN#					C427	1	2	220P_0402_50V7K					
MODEBTN#	C427	1	2	220P_0402_50V7K	C415	1	2	220P_0402_50V7K					
EC_PLAYBTN#					C417	1	2	220P_0402_50V7K					
EC_STOPBTN#					C424	1	2	220P_0402_50V7K					
EC_FRDBTN#													
EC_REVBTN#	C421	1	2	220P_0402_50V7K									

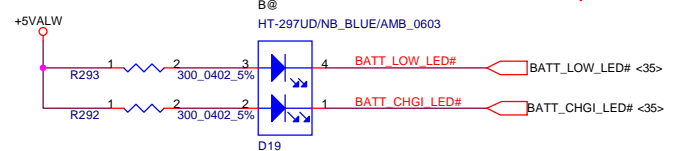
POWER/ON LED



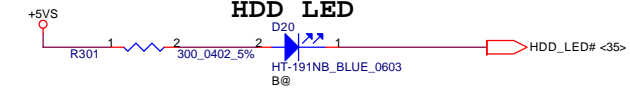
AC IN LED



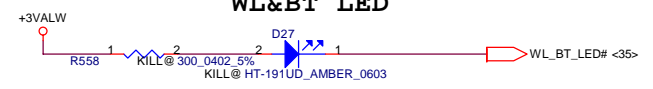
BATTERY CHG



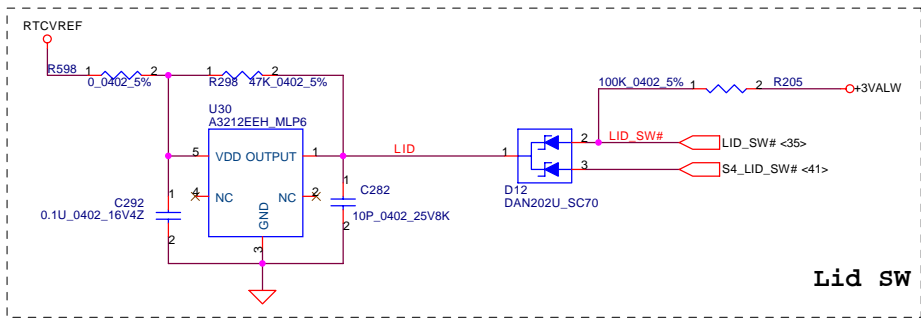
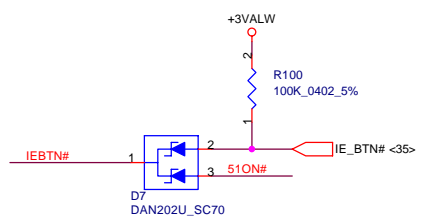
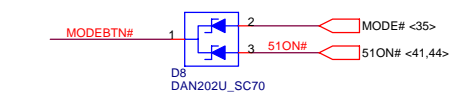
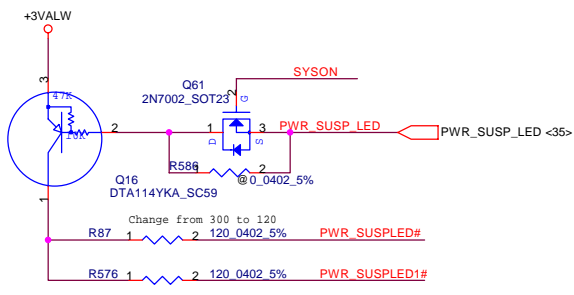
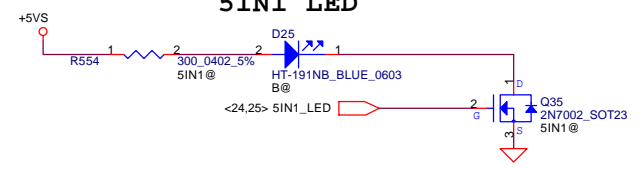
HDD LED



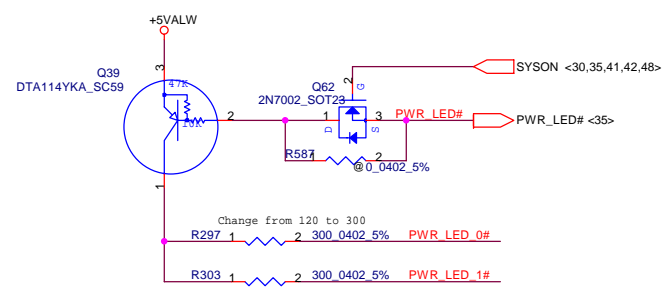
WL&BT LED



SIN1 LED

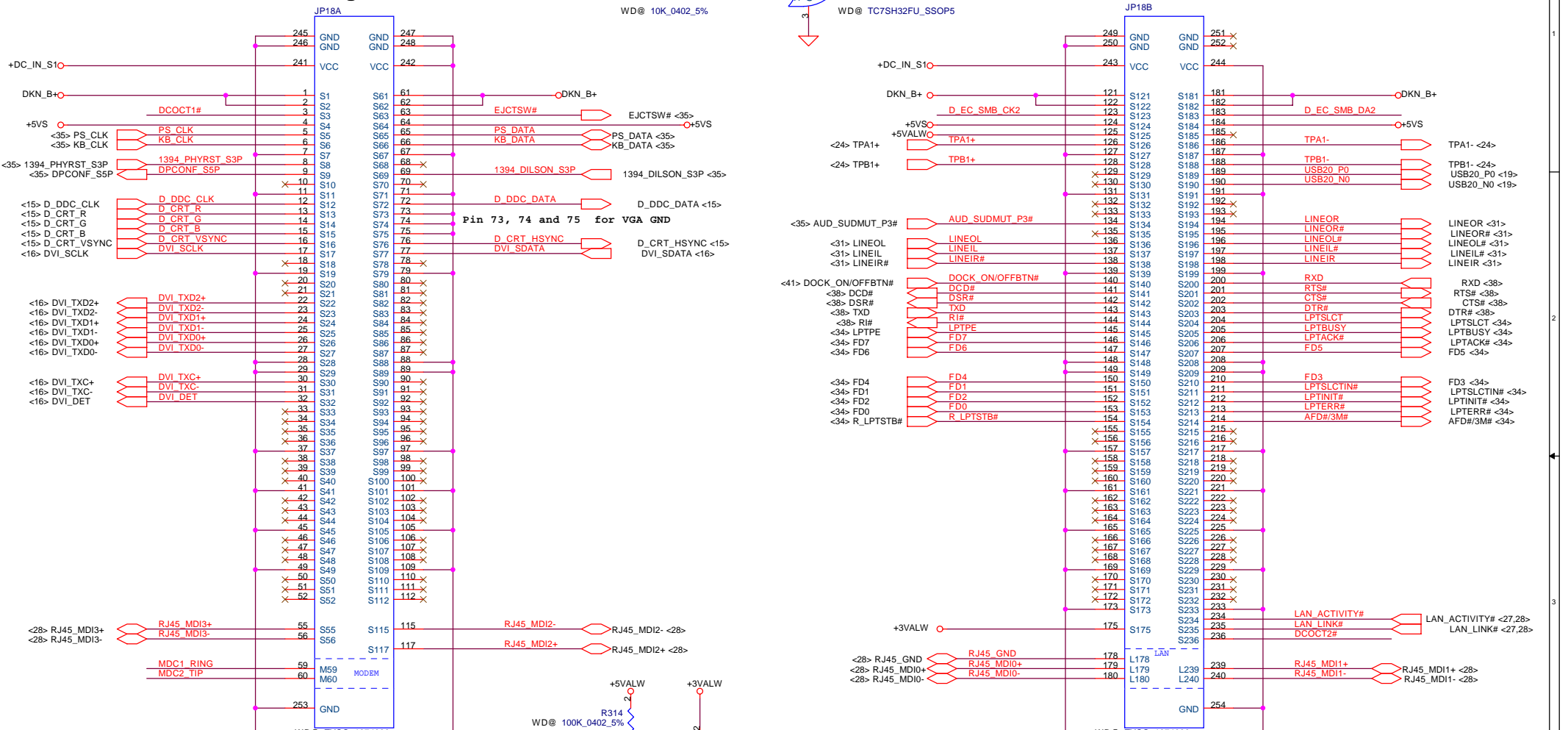


Lid SW

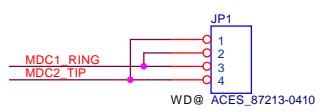


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Size	Document Number	Date: 2005/5/6 下午 11:47:56		Rev 1.0	
				Boston LA-2721	
				Sheet 39 of 53	

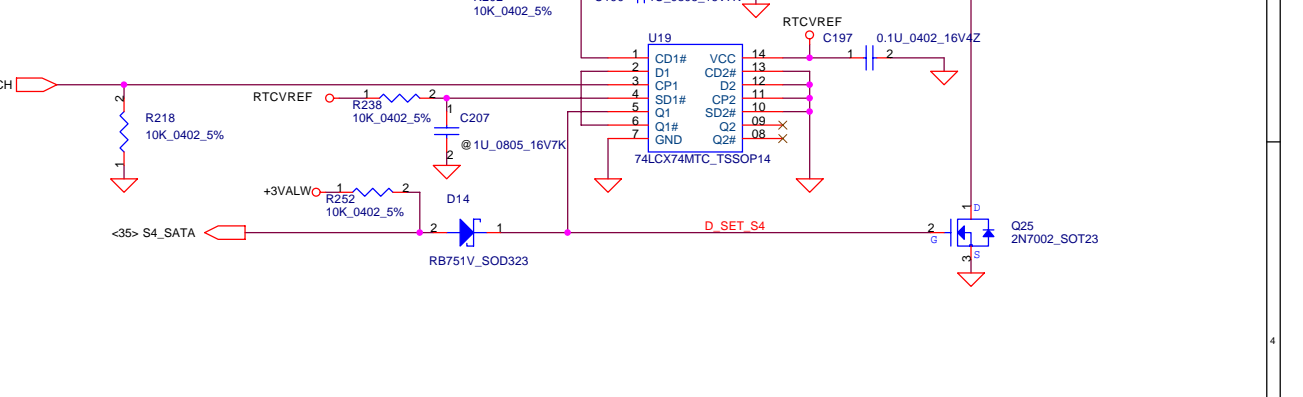
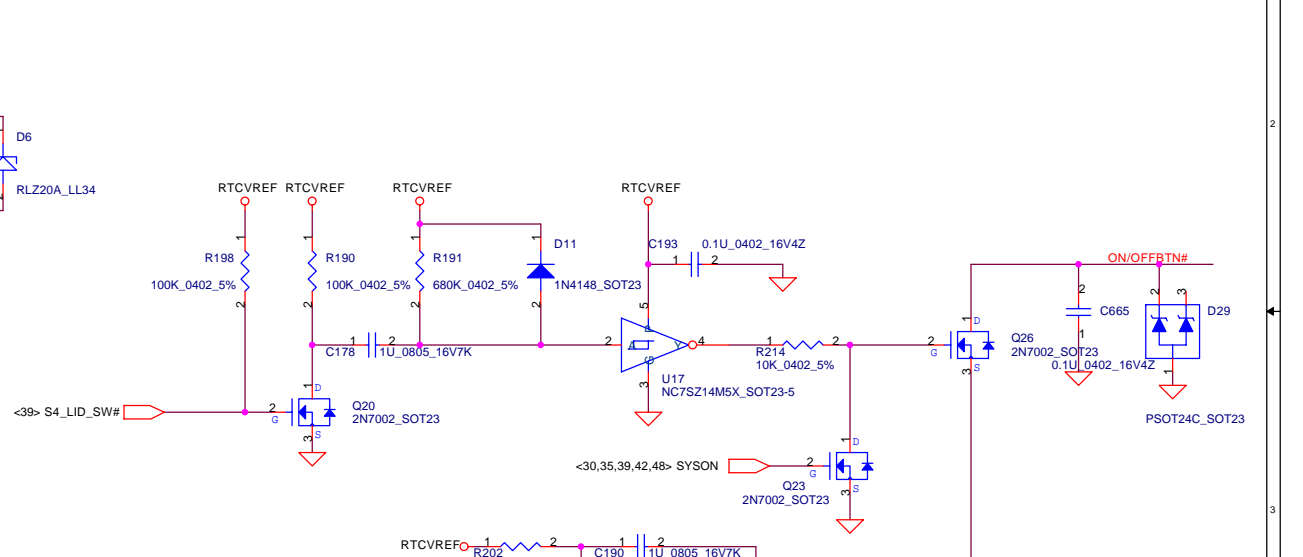
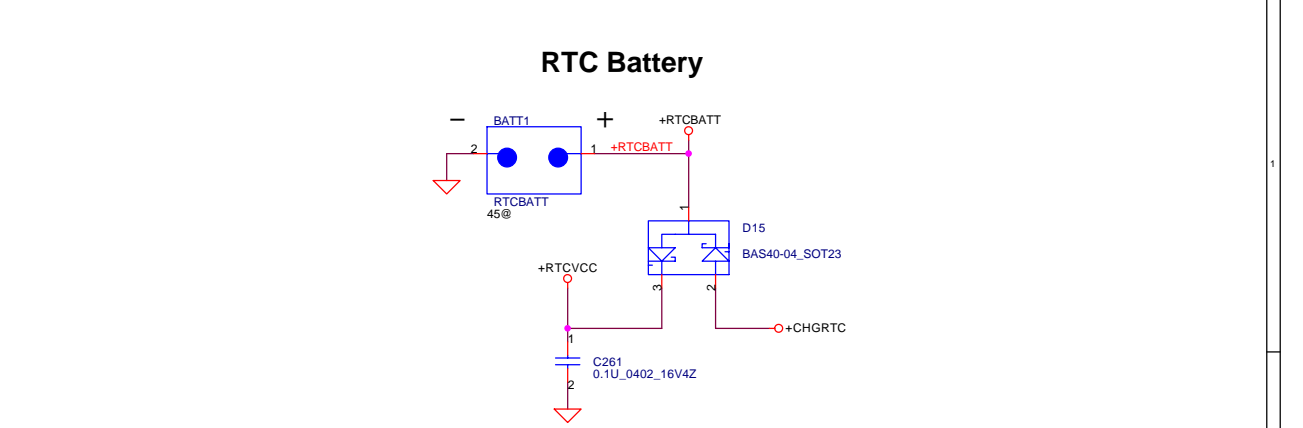
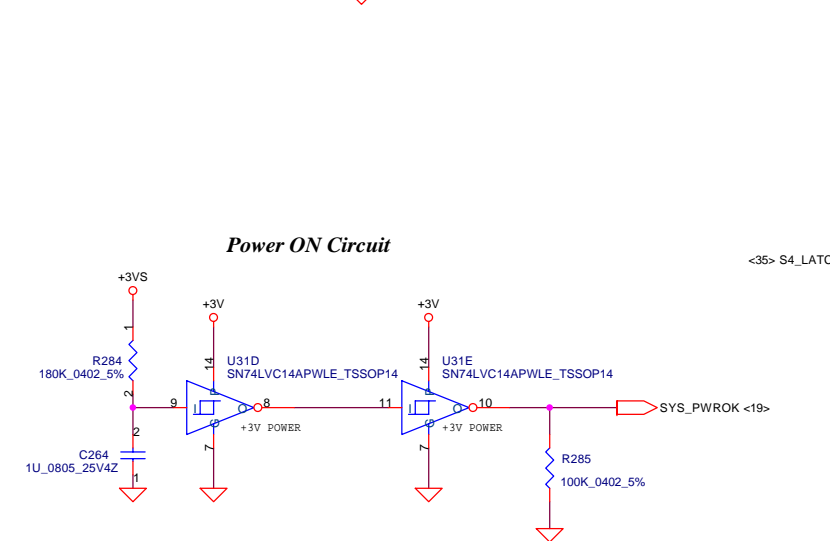
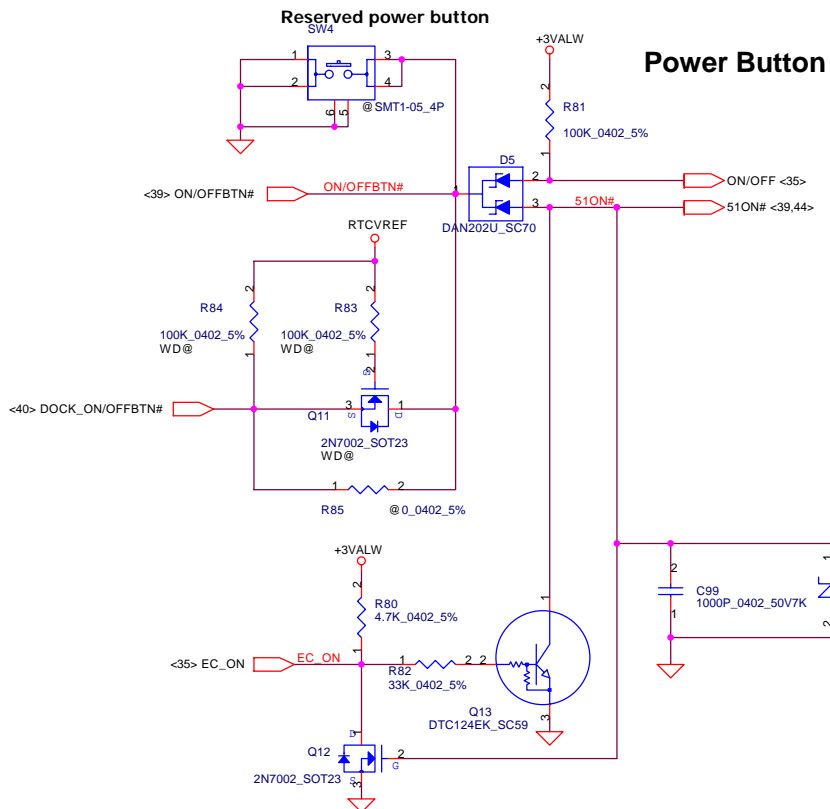
Docking Conn.



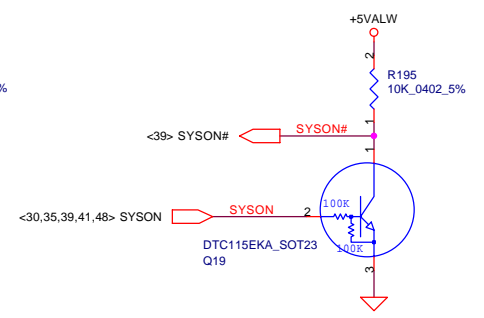
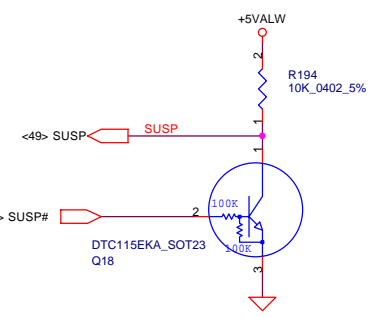
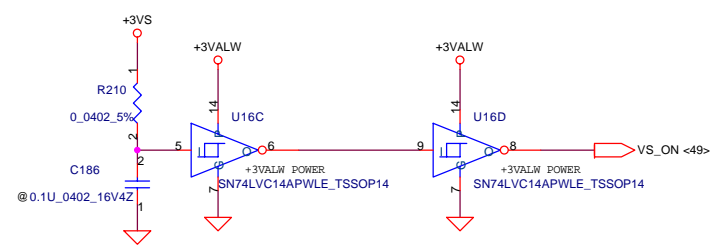
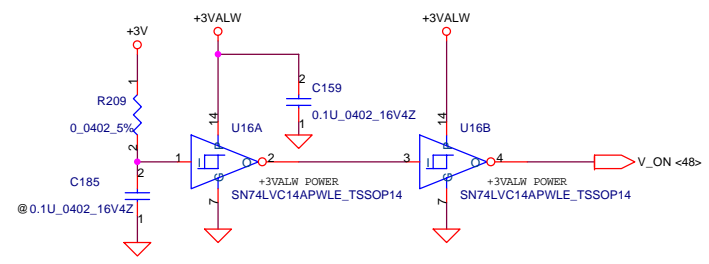
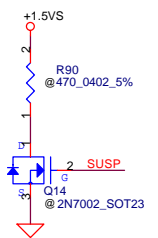
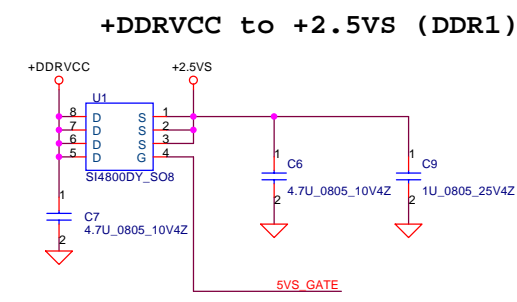
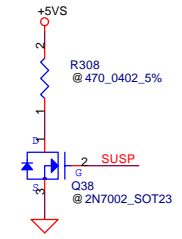
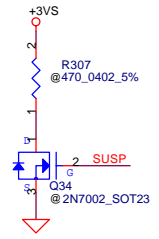
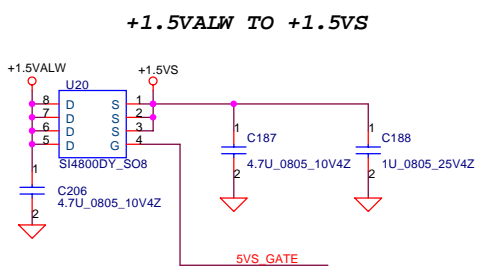
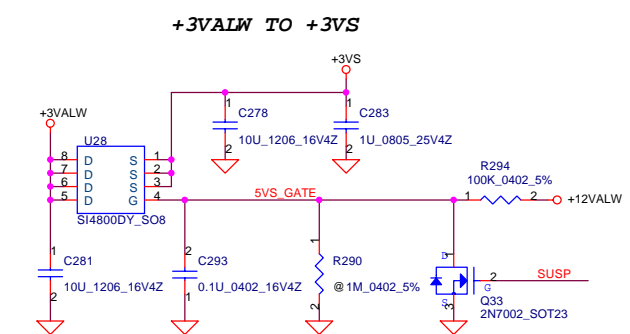
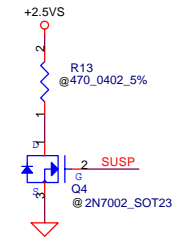
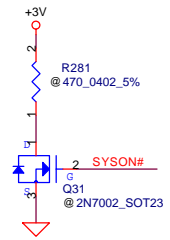
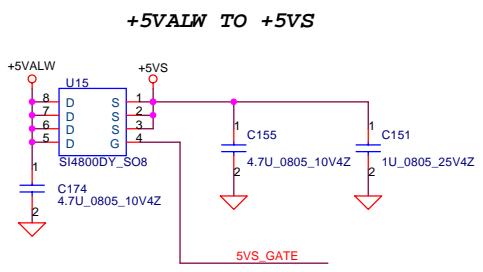
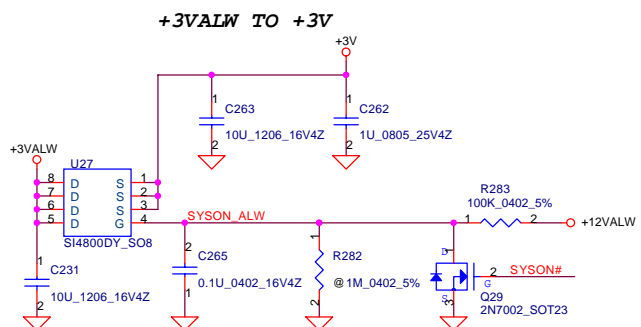
MDC to Docking Conn.



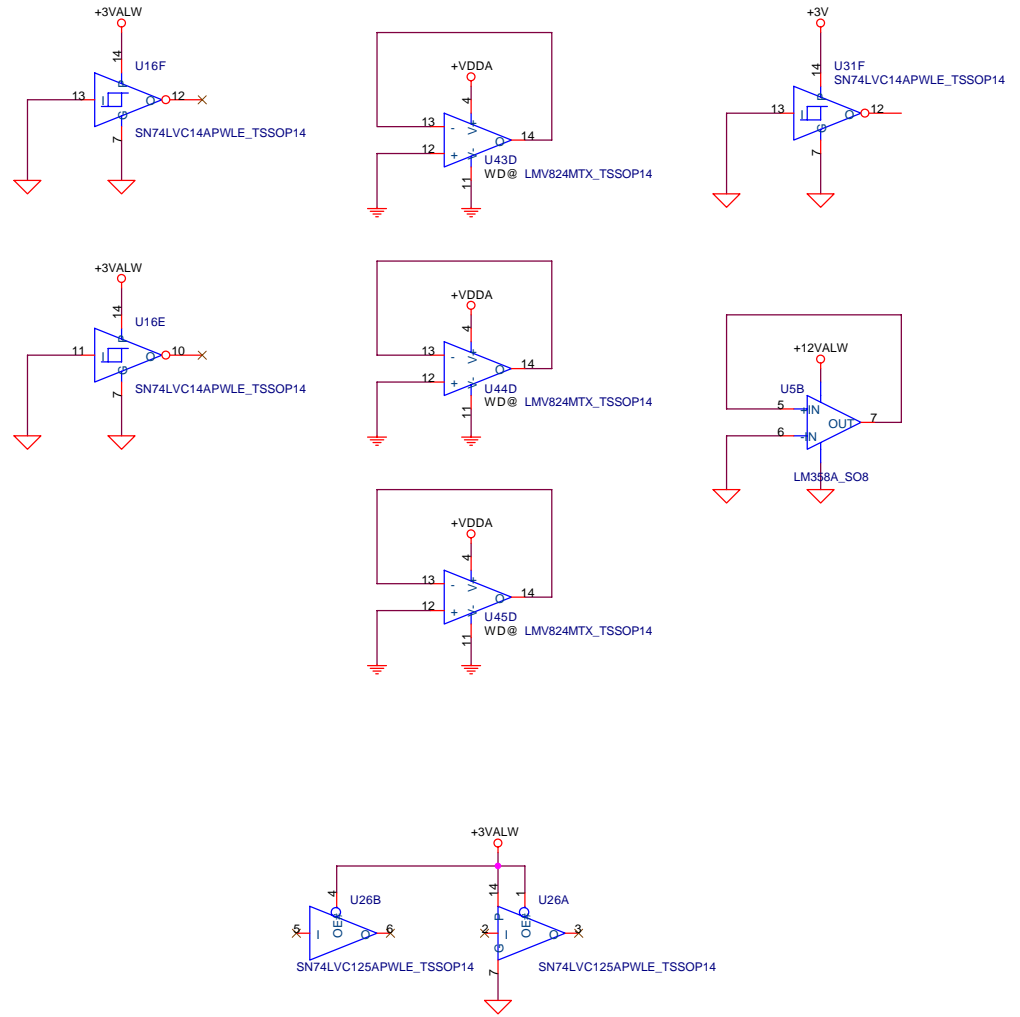
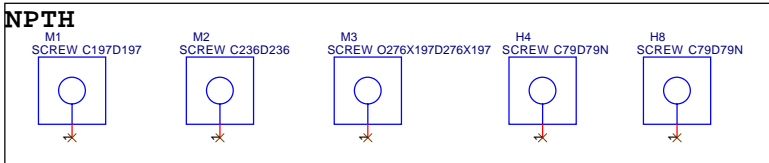
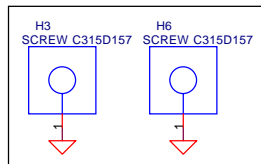
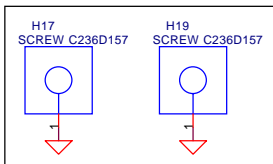
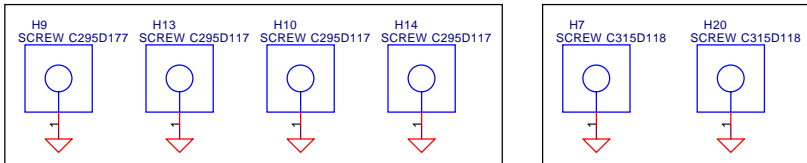
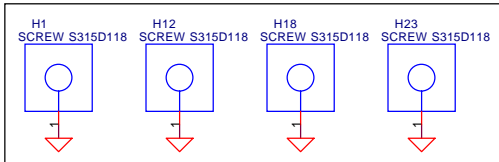
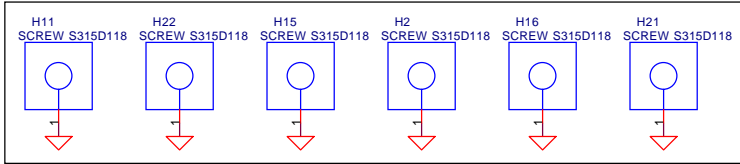
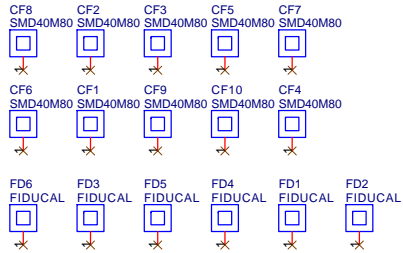
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Size	Document Number			Rev	
				Boston LA-2721	
Date:	2005/5/6 下午 11:47:55			Sheet	40 of 53



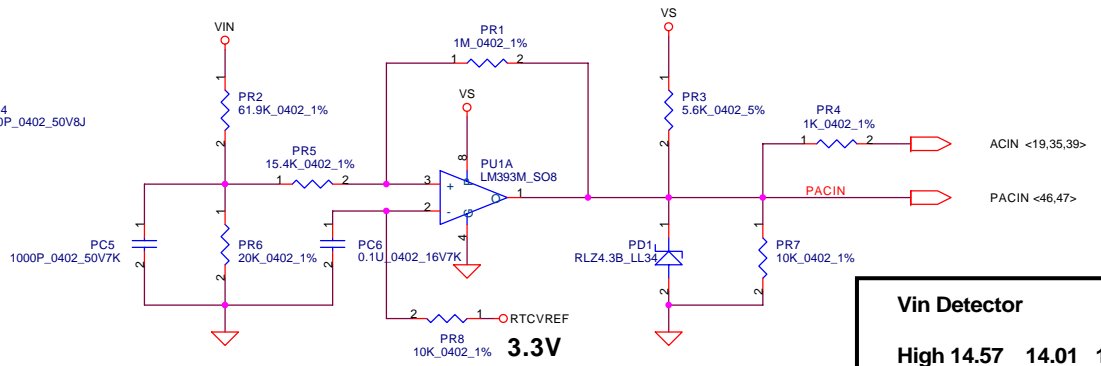
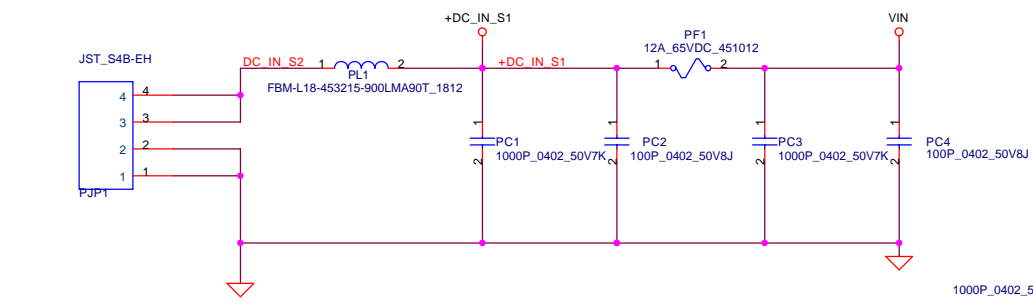
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Size	Document Number			Rev	
				Boston LA-2721	
Date:	2005/5/6 下午 11:47:53	Sheet	41	of	53



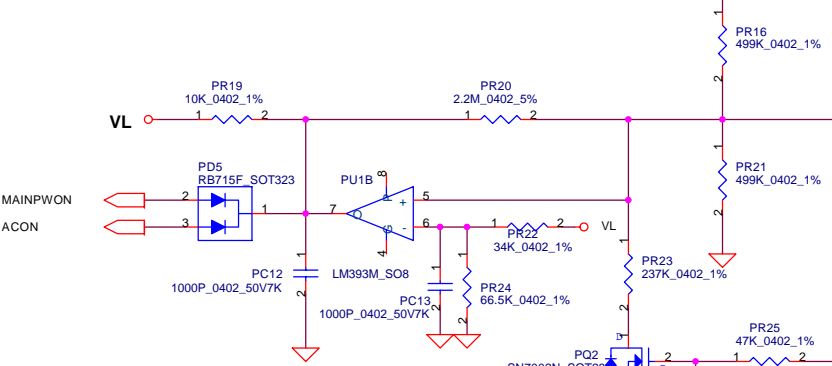
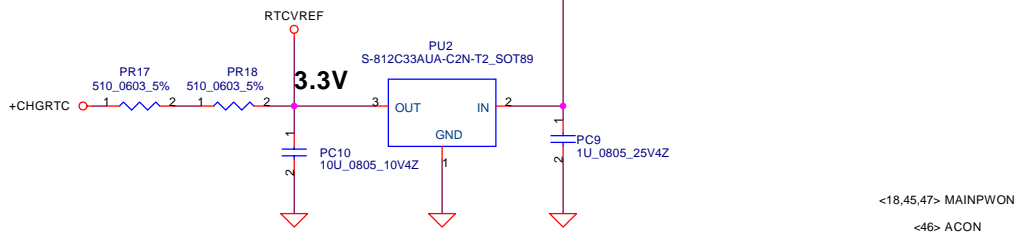
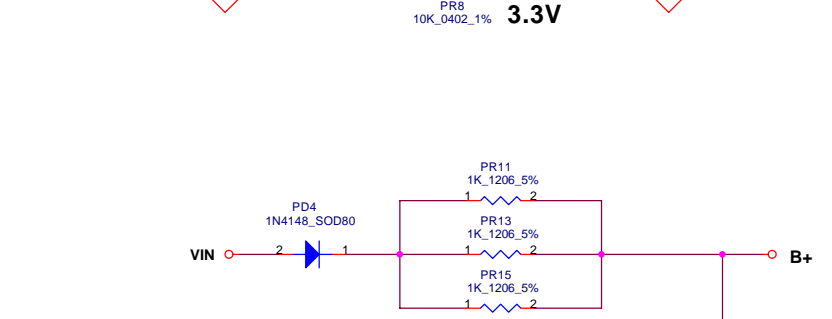
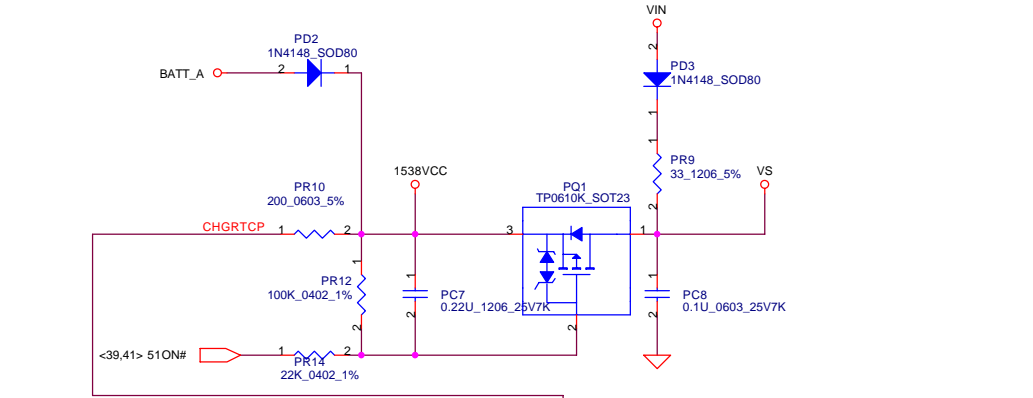
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Size	Document Number			Rev	
				Boston LA-2721	
Date:	2005/5/6 下午 11:47:56	Sheet	42	of	53



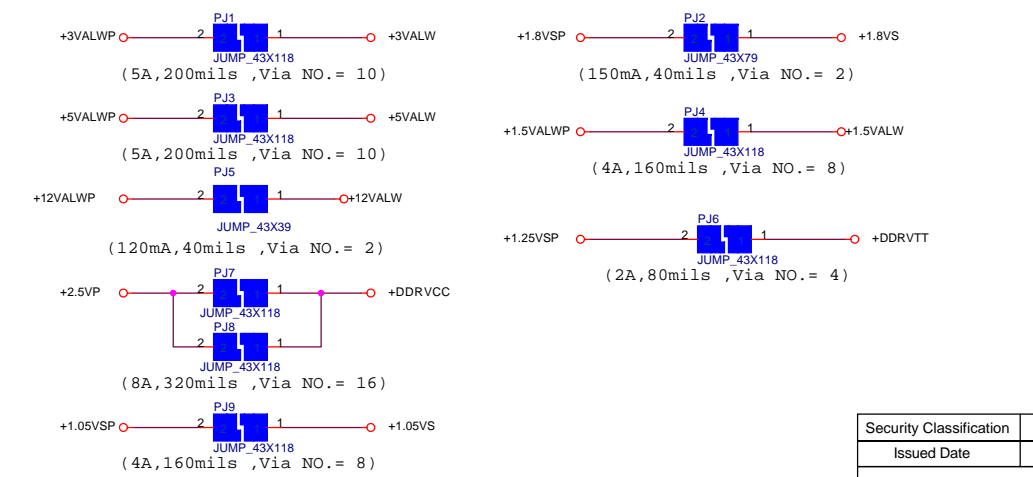
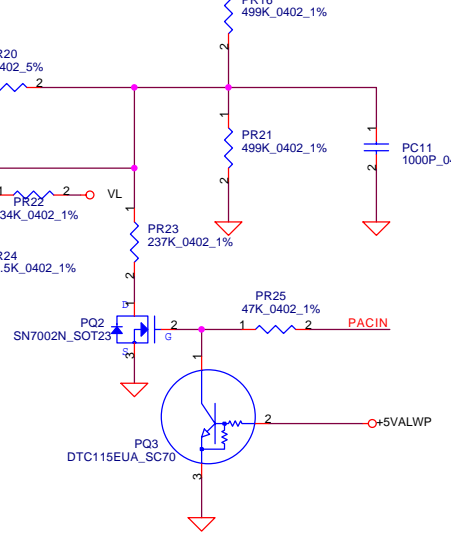
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Date:	2005/5/6 下午 11:47:58	Sheet	43 of 53	Rev	1.0



Vin Detector				
High	14.57	14.01	13.46	
Low	14.06	13.51	12.98	



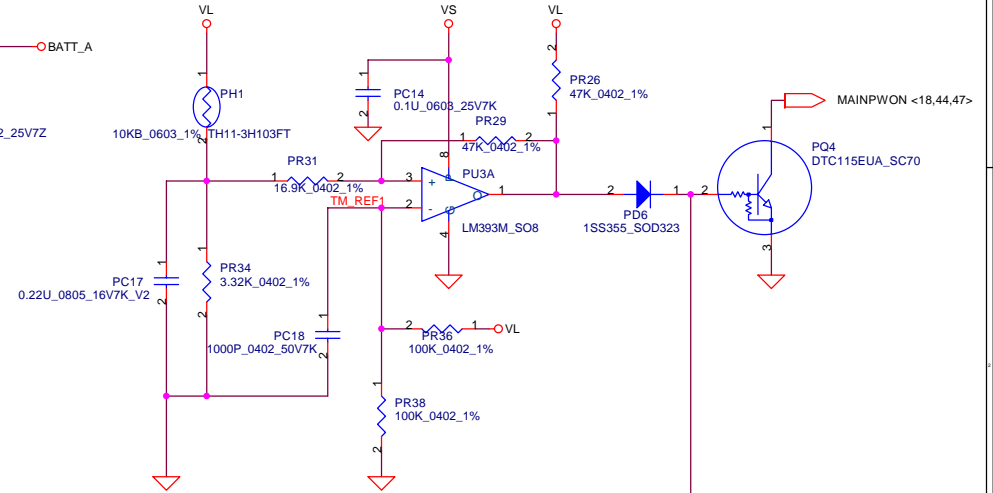
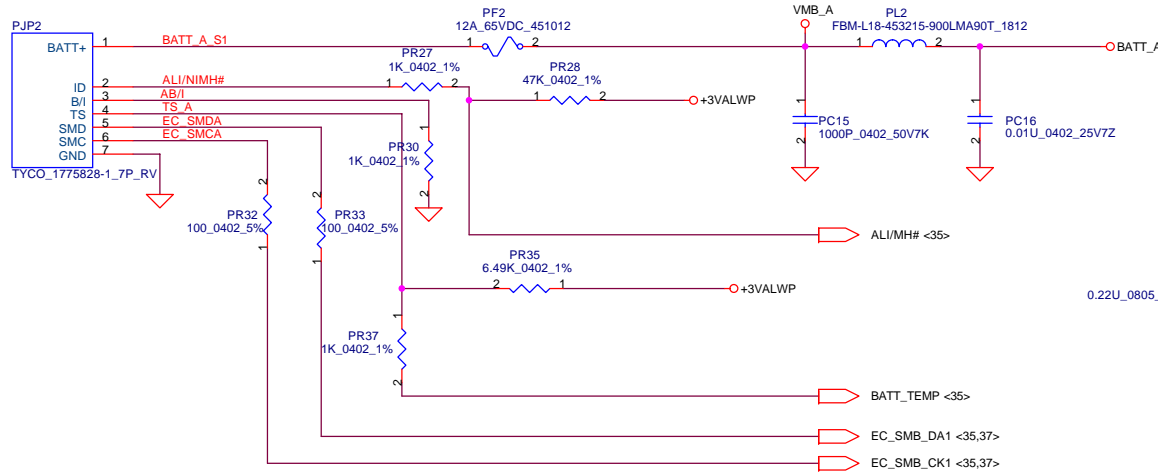
Precharge detector
14.3V/13.18V for adapter



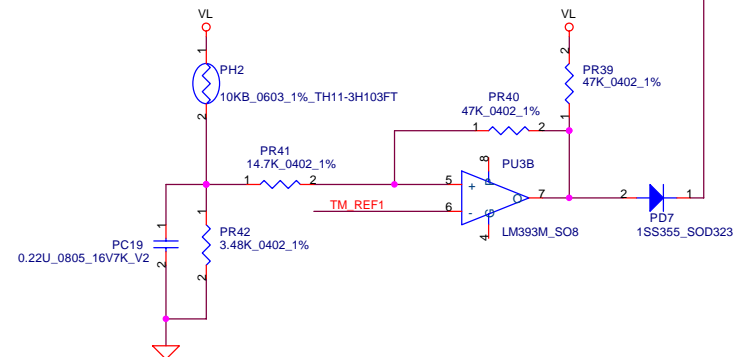
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Issued Date				2005/05/06		Deciphered Date		2006/05/06		Title					
										DCIN & DETECTOR					
										Size		Document Number		Rev	
										Boston LA-2721				1.0	
										Date:		2005/5/6 下午 11:47:57		Sheet 44 of 53	

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PH1 under CPU botten side :
 CPU thermal protection at 84 degree C
 Recovery at 45 degree C



PH2 near main Battery CONN :
 BAT. thermal protection at 79 degree C
 Recovery at 45 degree C



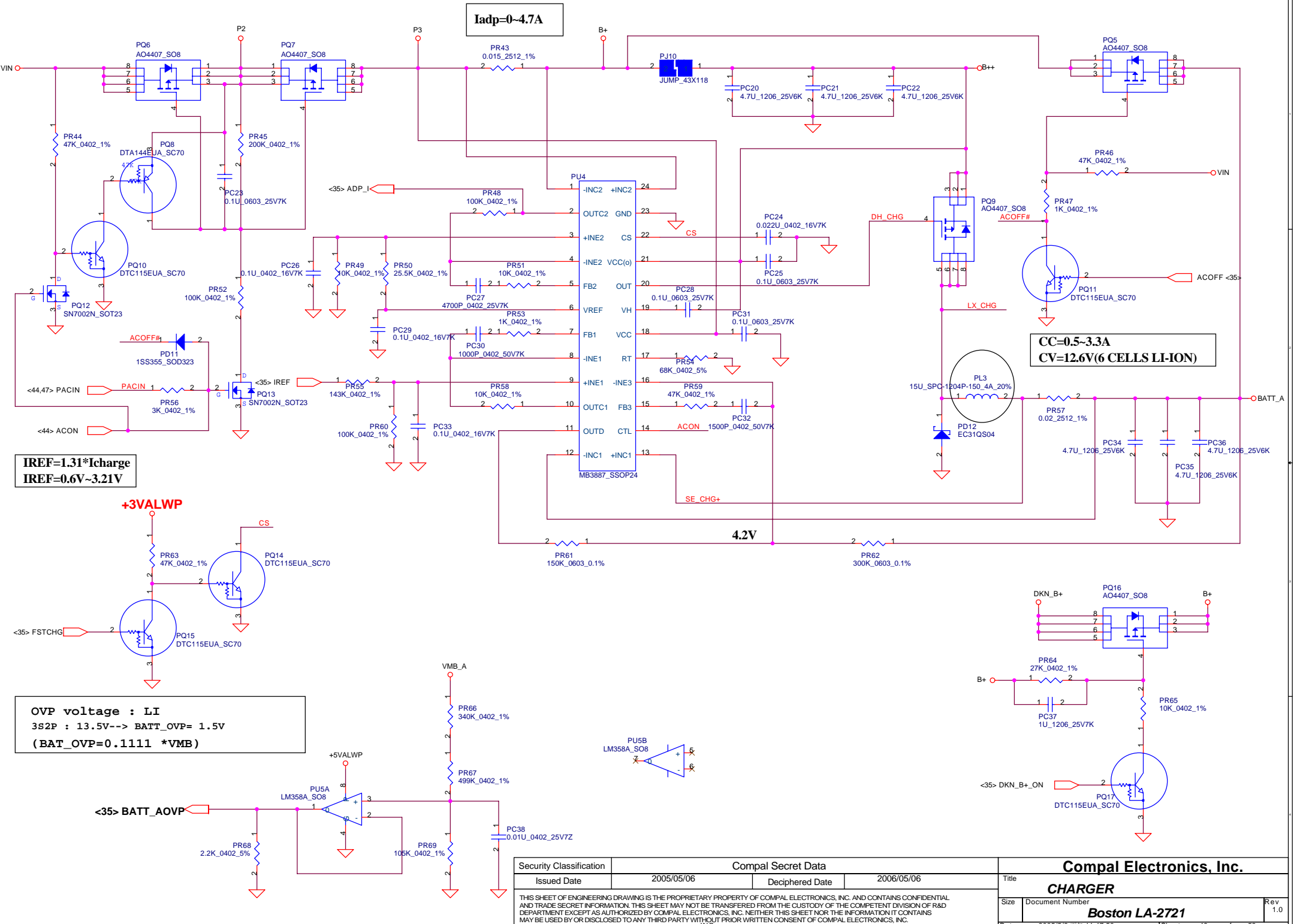
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				Date:	2005/5/6 下午 11:47:56
				Sheet	45 of 53
				Rev	1.0

Iadp=0~4.7A

CC=0.5-3.3A
CV=12.6V(6 CELLS LI-ION)

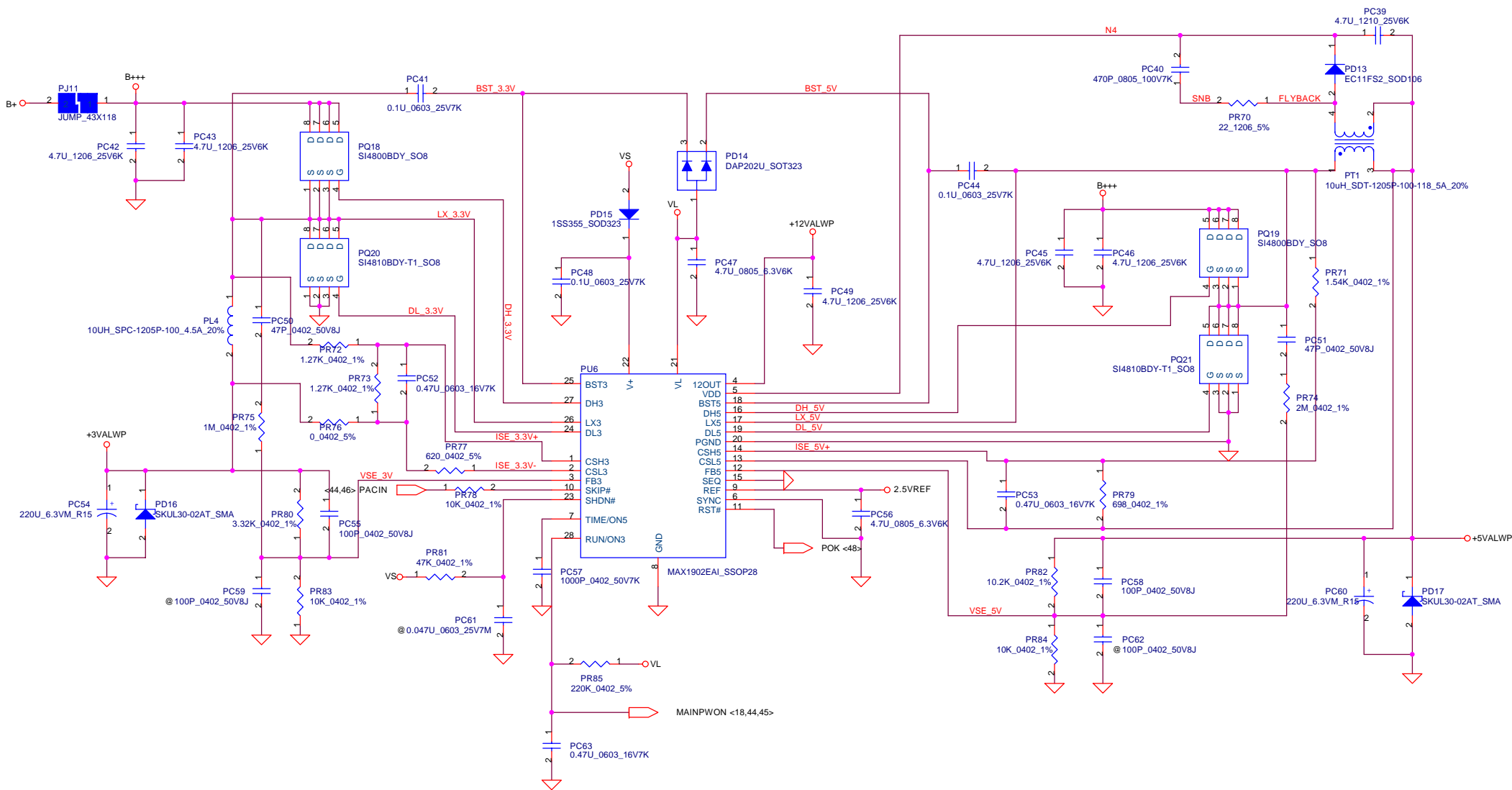
IREF=1.31*Icharge
IREF=0.6V~3.21V

OVP voltage : LI
3S2P : 13.5V--> BATT_OVP= 1.5V
(BAT_OVP=0.1111 *VMB)



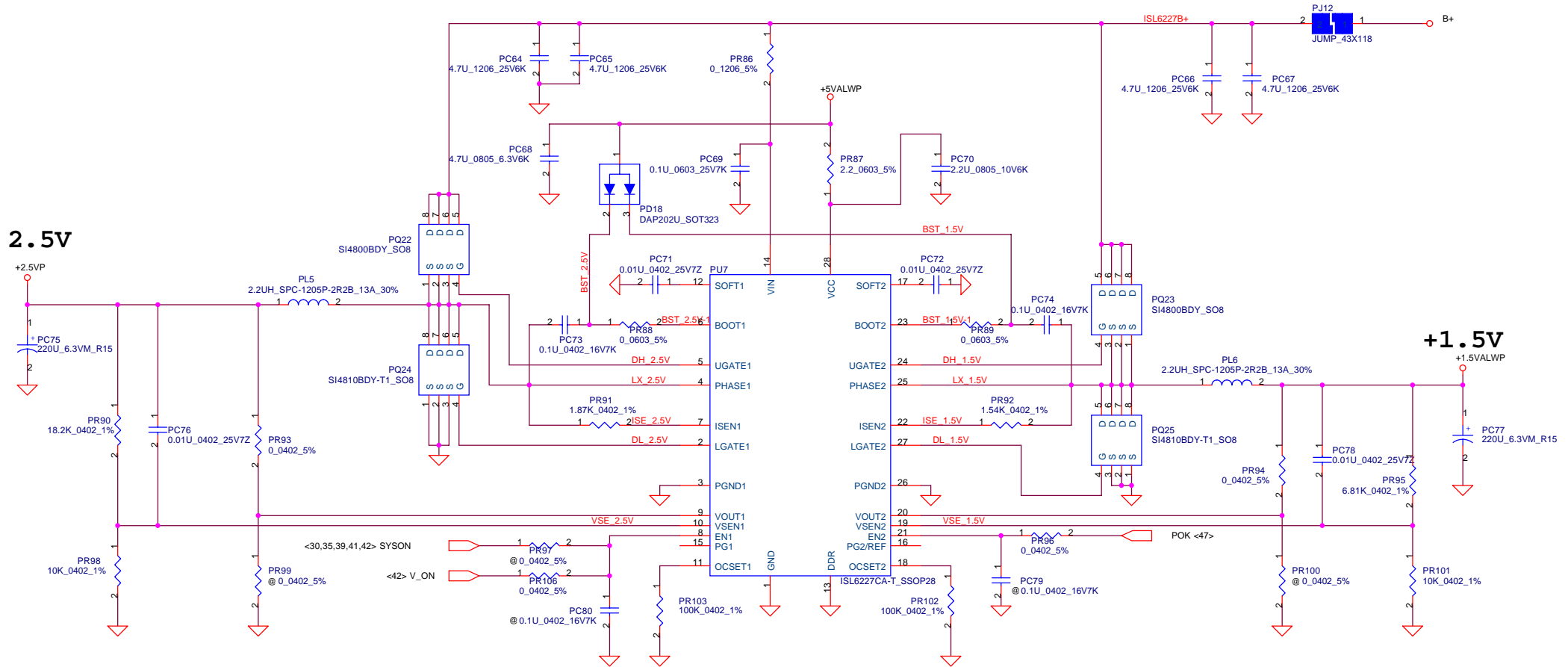
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Title CHARGER			
Size	Document Number	Rev	
	Boston LA-2721	1.0	
Date:	2005/5/6 下午 11:47:58	Sheet	46 of 53

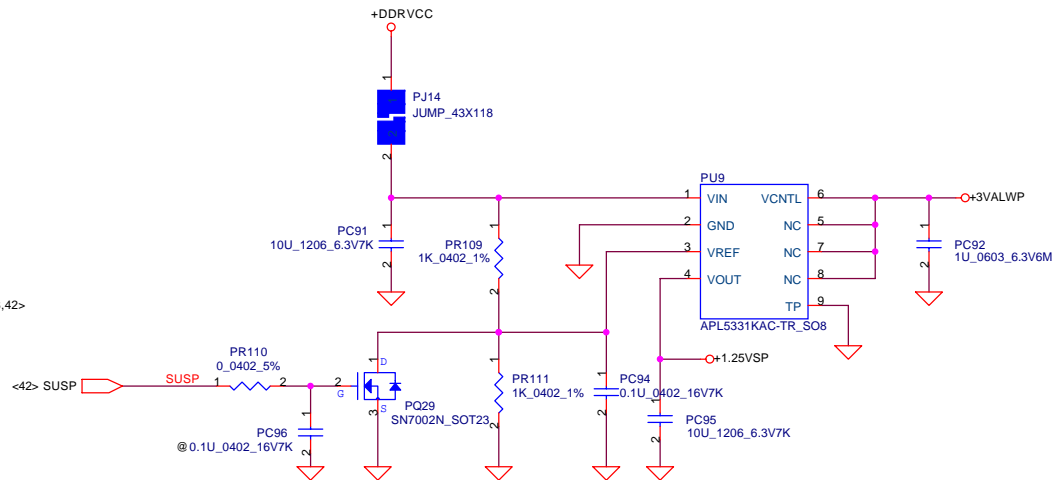
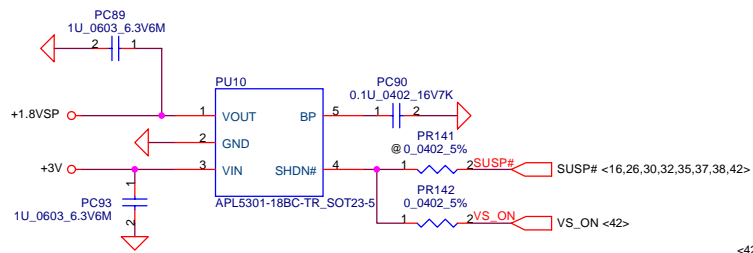
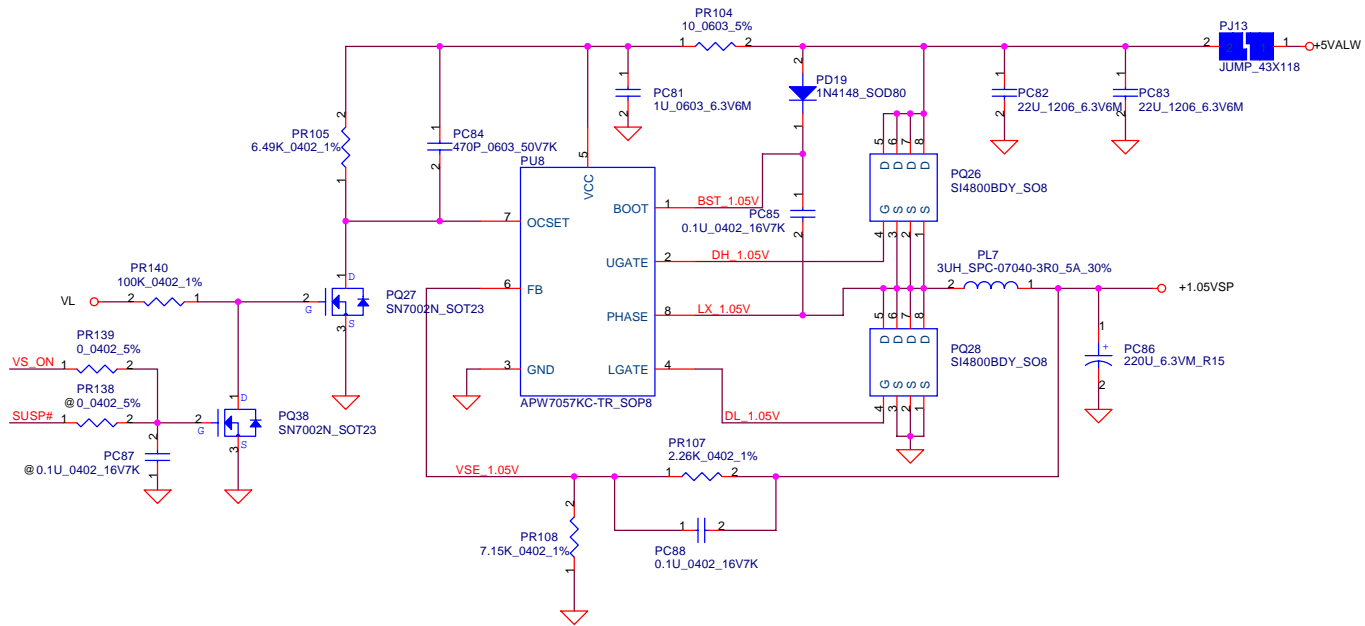


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Date:	2005/5/6 下午 11:47:55	Sheet	47	of	53
				Rev	1.0

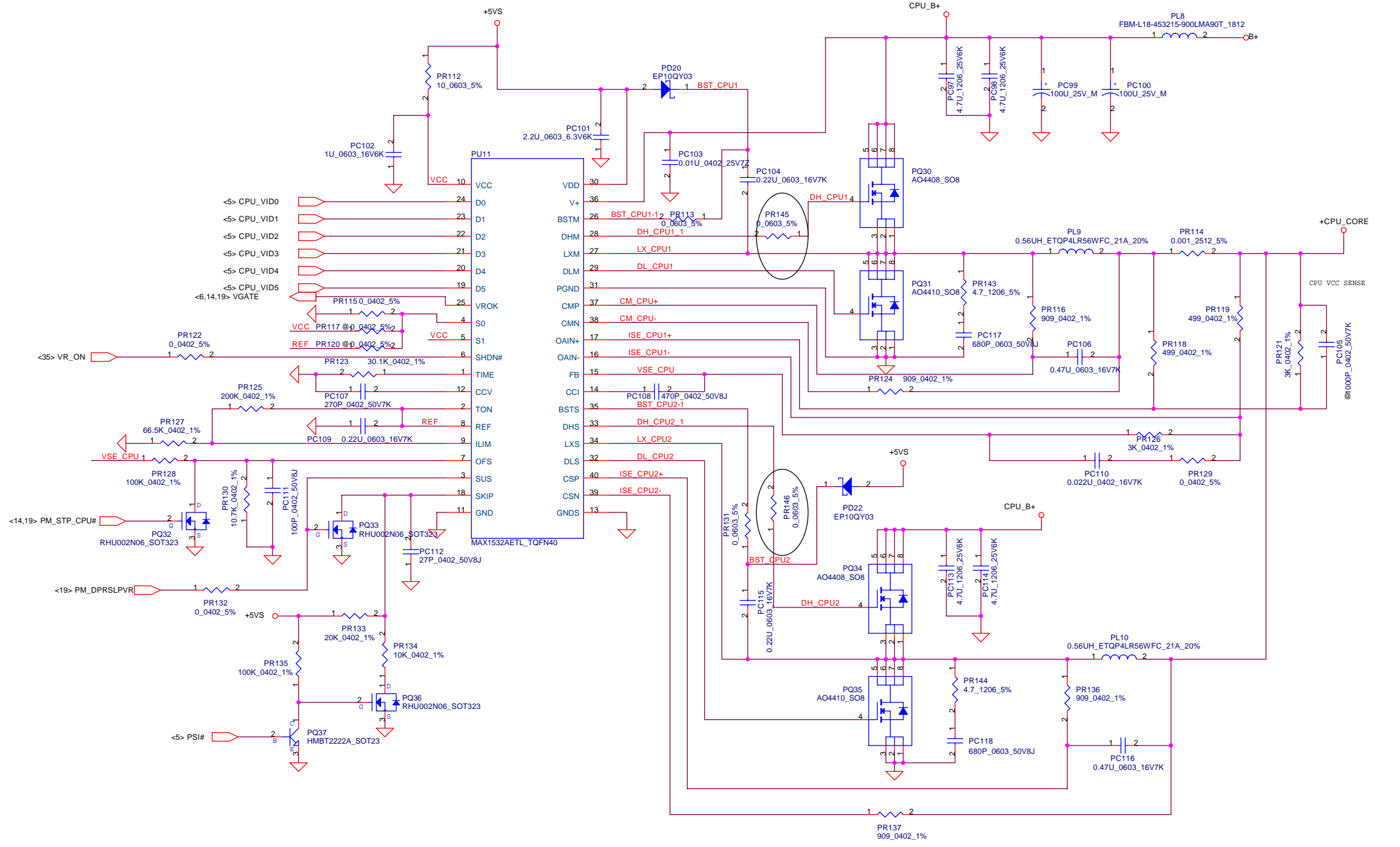
2.5V



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Size	Document Number			Rev	
	Boston LA-2721			1.0	
Date:	2005/5/6 下午 11:47:56		Sheet	48	of 53



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				Boston LA-2721	
				Date:	2005/5/6 下午 11:47:54
				Sheet	49 of 53
				Rev	1.0



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Date:	2005/5/6 下午 11:47:54	Sheet	50 of 53	

ECU00 PIR List

***** From Rev:0.1 to Rev:0.2 PIR List *****

1. Change R30 from 0603 package to 1206 package (Page9)
2. Add filter at CRT signal for EMI request (Page15)
3. Delete F1, D22 and change +CRT_VCC to +5VS (Page15)
4. Delete Software DJ circuit and change +5VCD to +5VS (Page21,22,32)
5. Chnage LAN_LINK and LAN_ACT signal to JP5 pin1,2 (Page28)
6. Add R588, R589, R590, R591 for co-existance function (Page29,36)
7. Add JP31 and R592-R597 for hardware EQ reserve (Page30)
8. Add SKU ID table (Page3,35)
9. Change JP3 and JP17 to 10pin (Page39)
10. Change U30 power from +3VALW to +CHGRTC (Page39)

***** From Rev:0.2 to Rev:0.3 PIR List *****

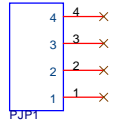
11. Reverse Q41, Q45 pin1, pin3 (Page28)
12. Non-stuff R586, R587 (Page39)
13. Change D27 to Amber LED (Page39)
14. Change U30 power to RTCVREF (Page39)
15. Non-stuff R268, R556 and Stuff R268, R557 (Page30)
16. Remove SATA 88SA8040 crystal reserve (Page21)
17. Change L1 to SM010012500 (Page9)
18. Add R602, C674 for EMI request (Page36)
19. Change ODD reset to PLT_RST# (Page22)
20. Connect Codec pin16, 17 to EC for EQ (Page30, 35)
21. Add D29 (Page41)
22. Add R604 and change R107 to 470ohm (Page35)
23. Change R568 to 3.3kohm (Page32)
24. Add R611 (Page15)

***** From Rev:0.2 to Rev:0.3 PIR List *****

25. Replace JP2 (Page15)
26. Replace R358 for interfer (Page15)
27. Add three while area for ME.
28. JP29 change from OCTEK_HDS-22TA1_44P_RV to OCTEK_HDS-22TA1_44P_RV-S.
29. JP30, update Mini PCI new Foot print form QTC to AMP to update outline.
30. U30. update new Foot print from A3212EEH_MLP6_5P to A3212EEH_MLP6_5P-S.
31. Change PCB PN to Rev1.0.
32. C146 的BOM Structure 7411@ 後有空格, delete.
33. R603 的BOM Structure MDC@ 後有空格, delete.
34. R199 的BOM Structure 7411@ 改為 5IN1@
35. Change Q6 and Q46 from 2N7002 to SB501380009
36. Add C675 680P for H_NMI.
37. Reserve C676 180P for PCI_SERR#
38. Add C677 220P for H_FERR#
39. Reserve C678 ~ C686 180P for H_SMI#, H_INIT#, SERRIRQ, H_A20M#, H_INTR, H_IGNNE#, H_STPCLK#, H_PWRGOOD and H_CPUSLP#.
40. Add R615 ~ R617 00hm for EMI solution link DGND and RJ45_GND.
41. Change R542 from 22 Ohm to 33 Ohm.
42. R527 and C607 change from @ to mount for audio EMI.
43. Add L23 ~ L26 (SM070000H00) and Reserve R618 ~ R625 for EMI
44. Change U2 to SA411250200
45. Change C510 and C511 from 33P to 30P (SE071300J00)

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Rev	1.0				

45@
JST_S4B-EH

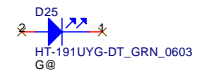
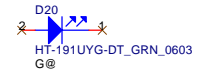
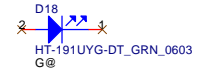


ZZZ
DA800001L10
DAB00001L10
--PCB ZKL LA-2721
REV1 M/B

U4
R3GM@ SA0091500N0
SA0091500N0
--S IC A51 915GM-C1
BGA 1257P GMCH R3

U12
1510@ SA000013200
SA000013200
--S IC PCI1510RGVF PBGA
253P PC CARD CTRL

U36
8036@ SA880360000
SA880360000
--S IC88E88036 10/100
LAN CTRL



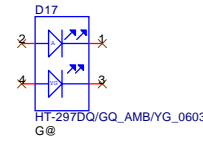
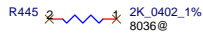
U4
R3GML@ SA0000187A0
SA0000187A0
--S IC A51 910GML-C1
BGA 1257P GMCH R3

U12
4510@ SA045100110
SA045100110
--S IC PCI4510RGVF PBGA
224P PCI-CARD BUS

T1
8036@ SP050001X00
SP050001X00
--TST1284B 10/100
LAN Transformer

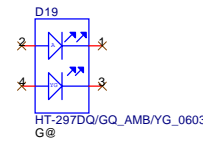
U4
R1GM@ SA0091500M0
SA0091500M0
--S IC A51 915GM-C1
BGA 1257P GMCH R1

U12
6411@ SA064110000
SA064110000
--S IC PCI6411ZHK PBGA-
288 PCI-CARD BUS



U4
R1GML@ SA000018790
SA000018790
--S IC A51 910GML-C1
BGA 1257P GMCH R1

U4
R1PM@ SA0091501J0
SA0091501J0
--S IC 915PM-C1
BGA 1257P GMCH R1



U13
R1SB@ SA8280108B0
SA8280108B0
--S IC A51 FW82801FBM
SL7W6 B2 BGA 609P!

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				Sheet	53 of 53
				Rev	1.0