

945P-A/ 945PL-A

Rev: 3.0

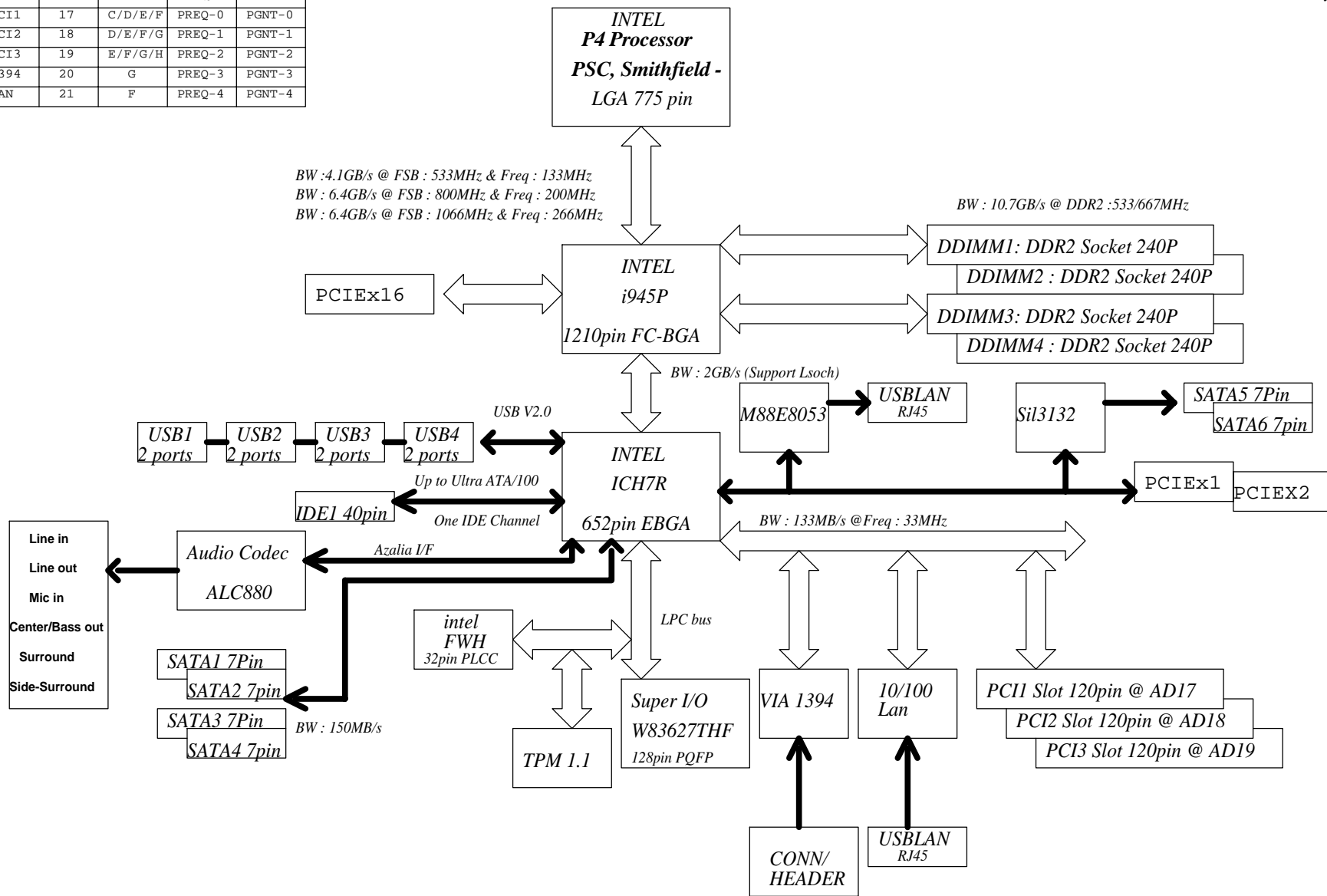
Page Title of Schematic :

Schematics Version History Table :

Circuit Ver.	PCB Ver.	Total Page	Modified Page(s)	Date
A	A	38		01/20/05
B	B	39		03/24/05
1.0	1.0	39		04/18/05
1.1	1.1	39		05/17/05
1.2	1.2	39	ADD R594	02/21/06
3.0	3.0	3 ~ 4 ~ 6 ~ 7 ~ 15 ~ 22 ~ 29	Modify for Support Conroe and PWM RT8802A	06/05/06

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DEVICE	IDSEL	INT#	REQ#	GNT#
PCI1	17	C/D/E/F	PREQ-0	PGNT-0
PCI2	18	D/E/F/G	PREQ-1	PGNT-1
PCI3	19	E/F/G/H	PREQ-2	PGNT-2
1394	20	G	PREQ-3	PGNT-3
LAN	21	F	PREQ-4	PGNT-4

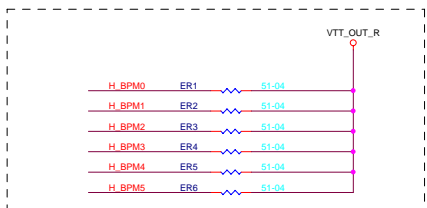
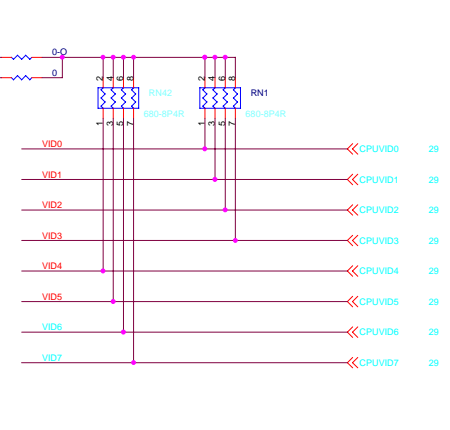
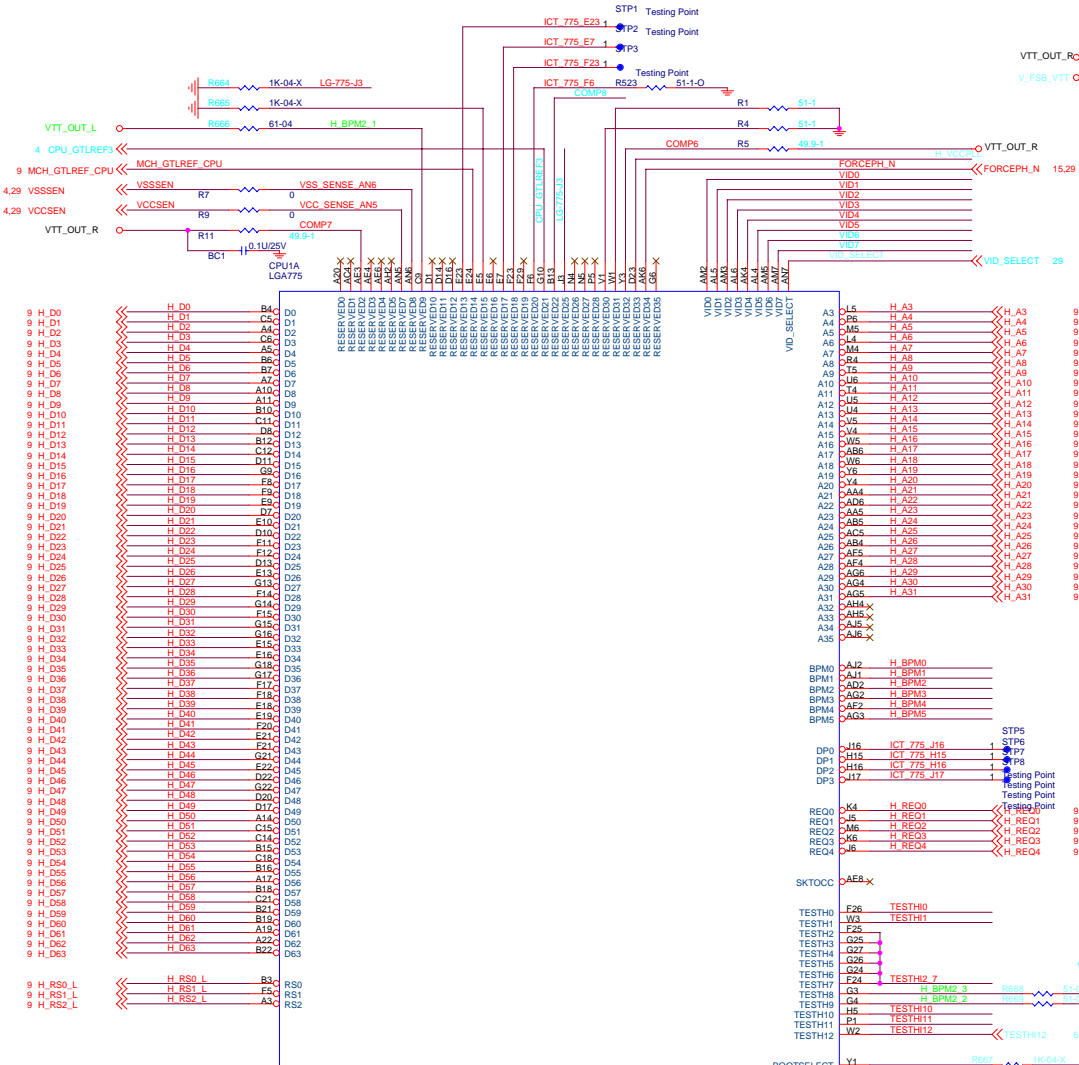


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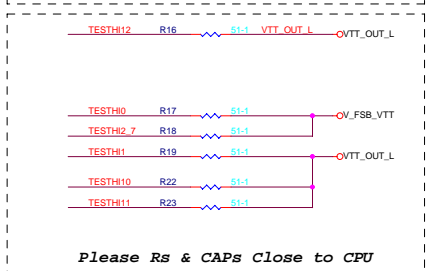
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Size: Custom | Document Number: **945P-A/945PL-A** | Rev: 3.0

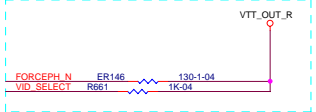
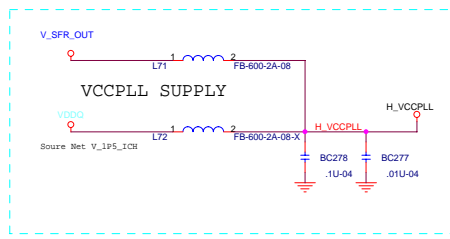
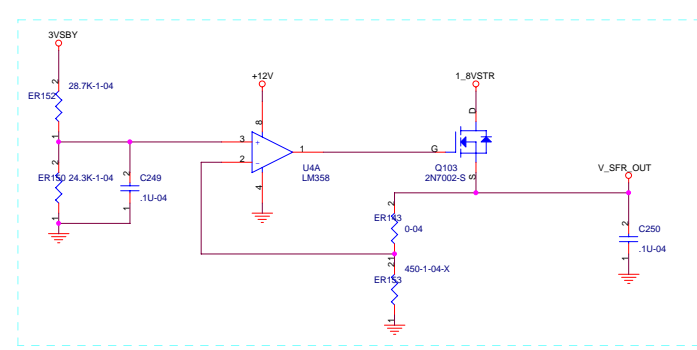
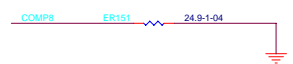
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Please BPM TERMINATION NEAR to CPU



Please Rs & CAPS Close to CPU



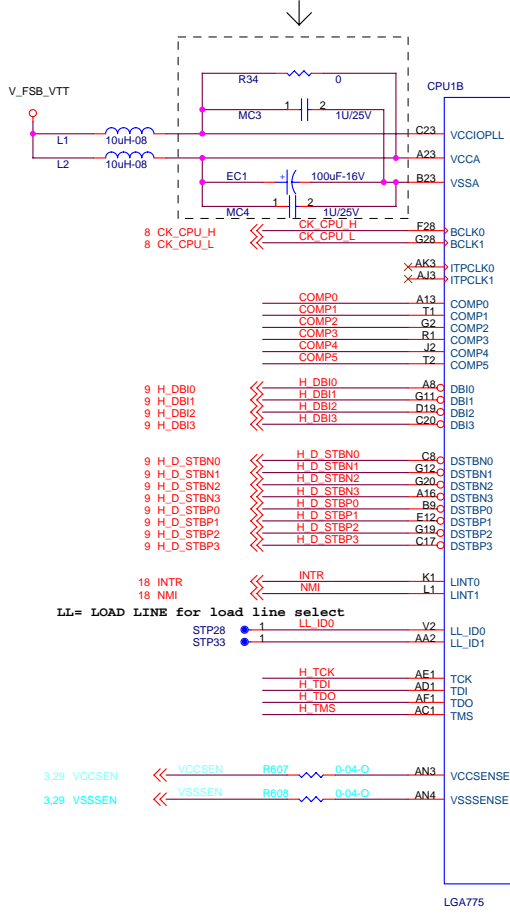
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Title: **P4 LGA775P Part A**

Size: C Document Number: **945P-A/945PL-A** Rev: 3.0

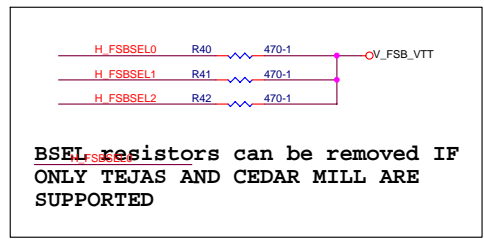
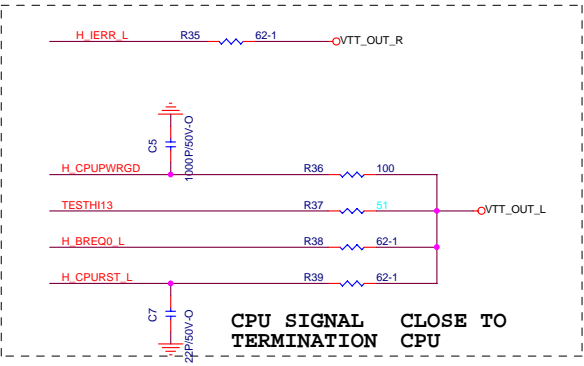
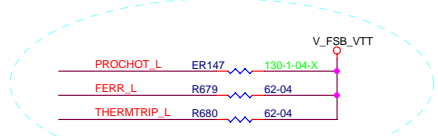
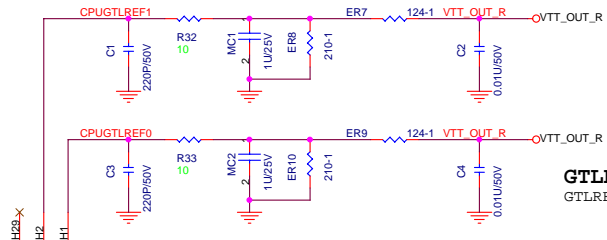
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Place components as close as possible to Processor socket trace width to cap must be no smaller than 12 Milis

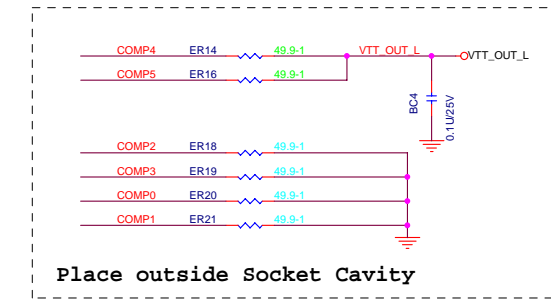
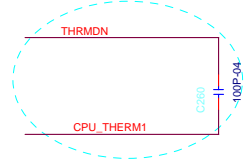


LGA775

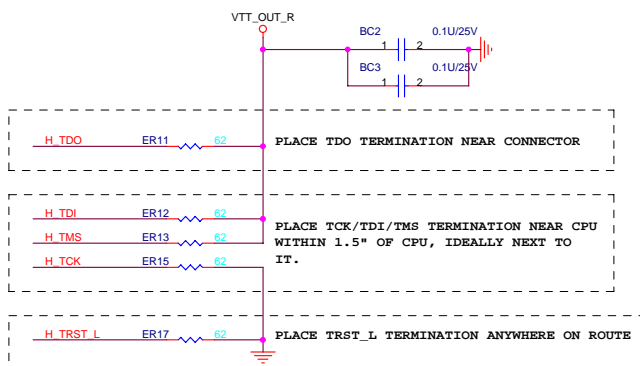
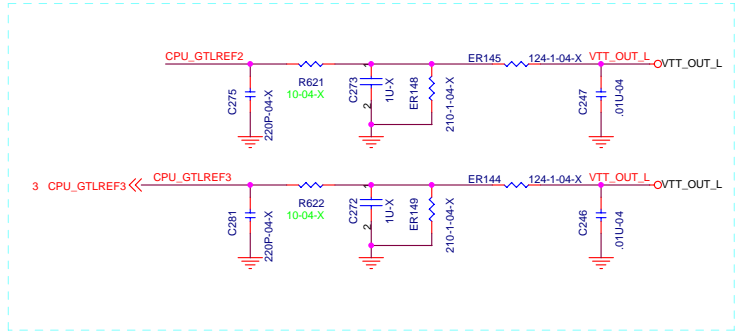
$GTLREF = 0.67 * VTT = 0.8V$
 GTLREF GENERATION CIRCUITS



BSEL resistors can be removed IF ONLY TEJAS AND CEDAR MILL ARE SUPPORTED



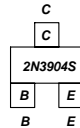
Place outside Socket Cavity



PLACE TDO TERMINATION NEAR CONNECTOR

PLACE TCK/TDI/TMS TERMINATION NEAR CPU WITHIN 1.5" OF CPU, IDEALLY NEXT TO IT.

PLACE TRST_L TERMINATION ANYWHERE ON ROUTE

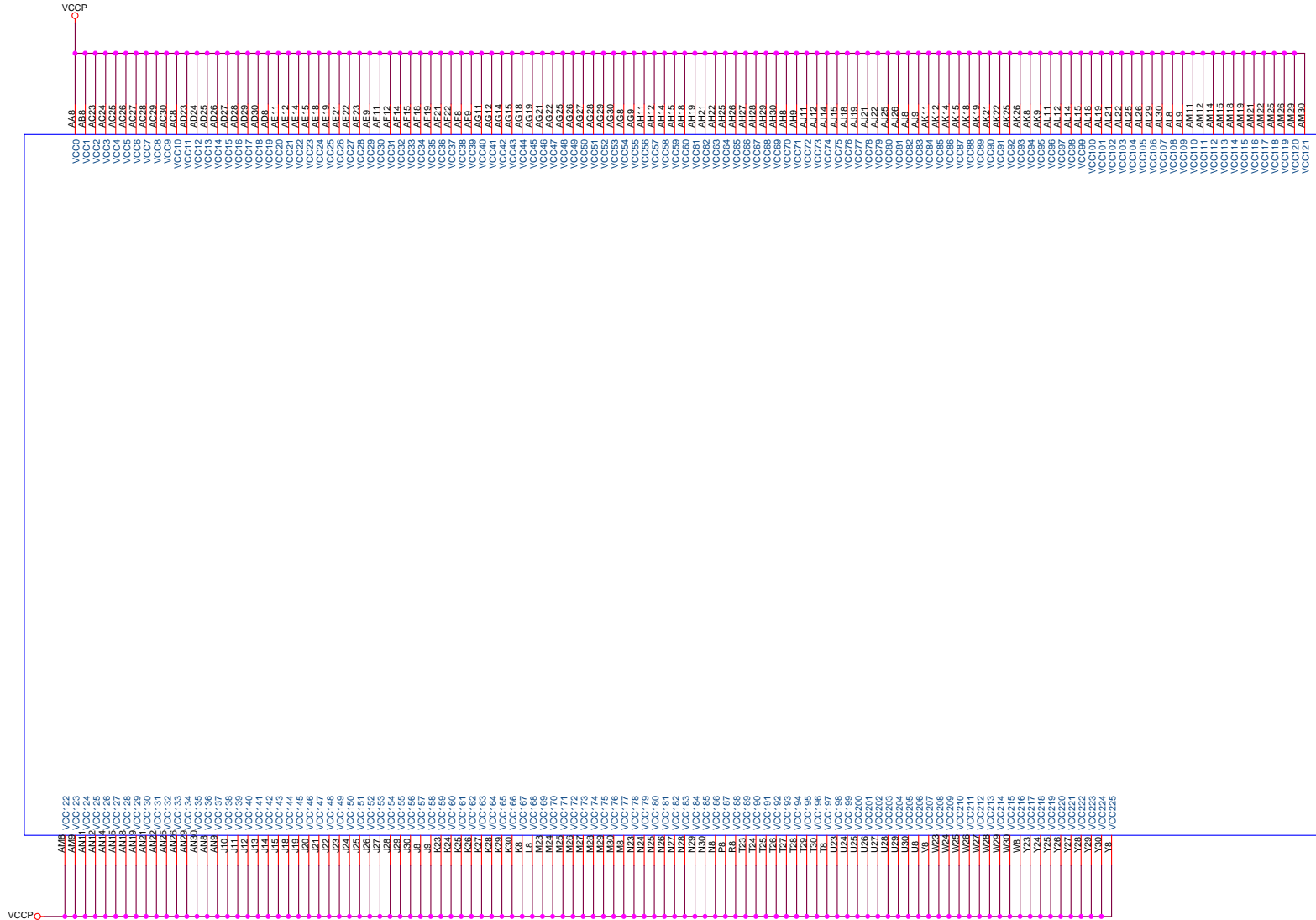


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Title: **P4 LGA775P Part B**

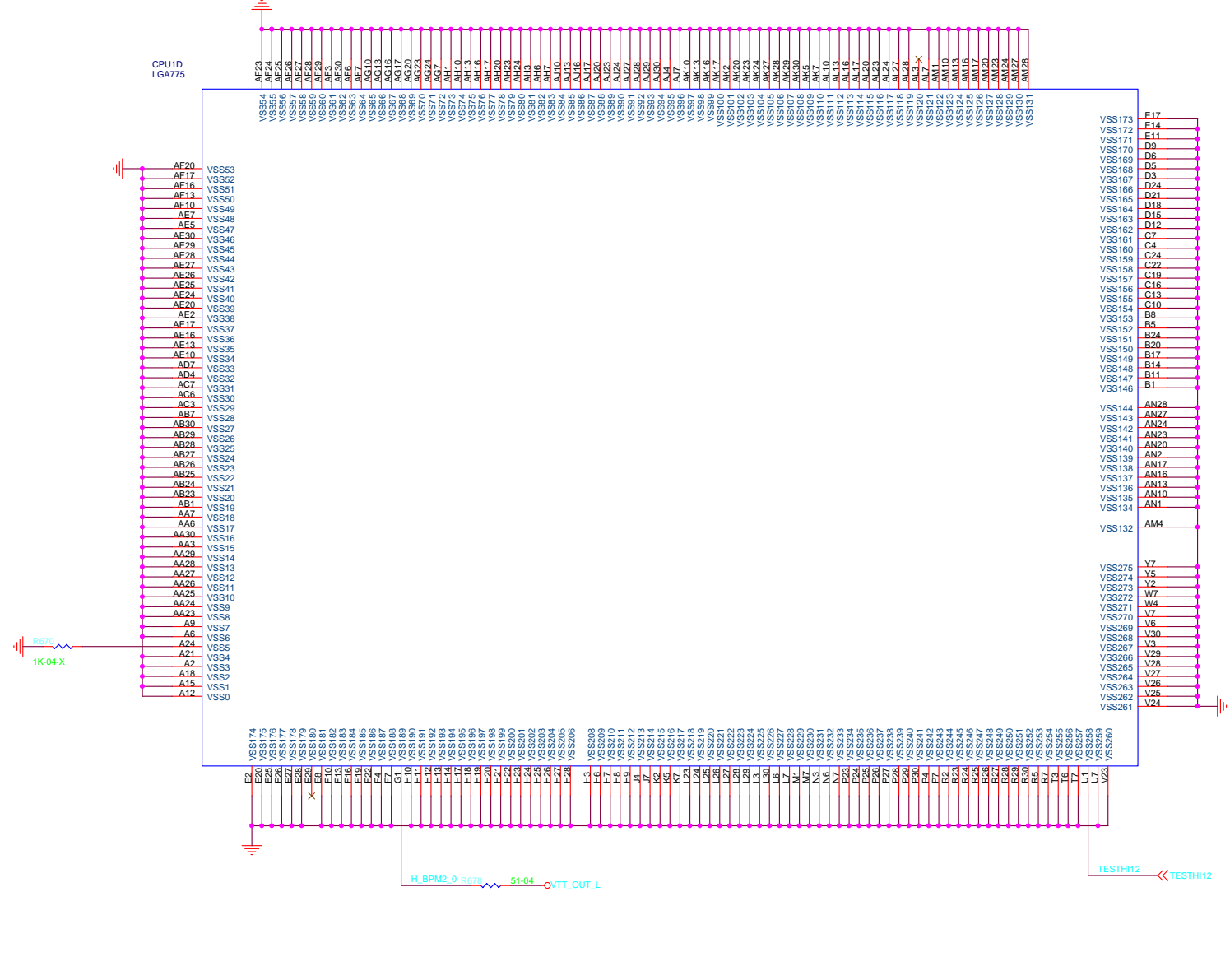
Size: Document Number **945P-A/945PL-A** Rev **3.0**

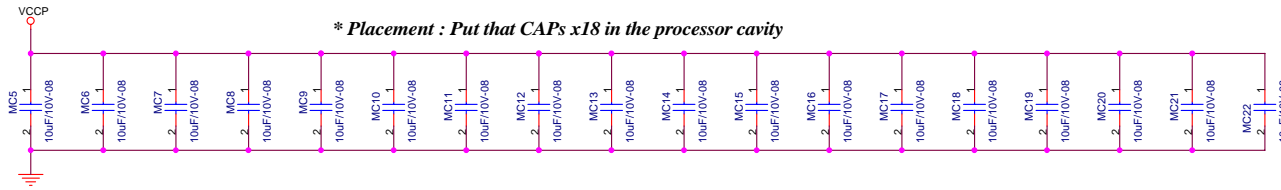
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CPU1C
LGA775

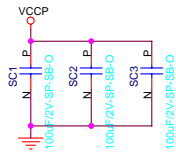
 Elitegroup Computer Systems		
Title		
P4 LGA775P Part C		
Size	Document Number	Rev
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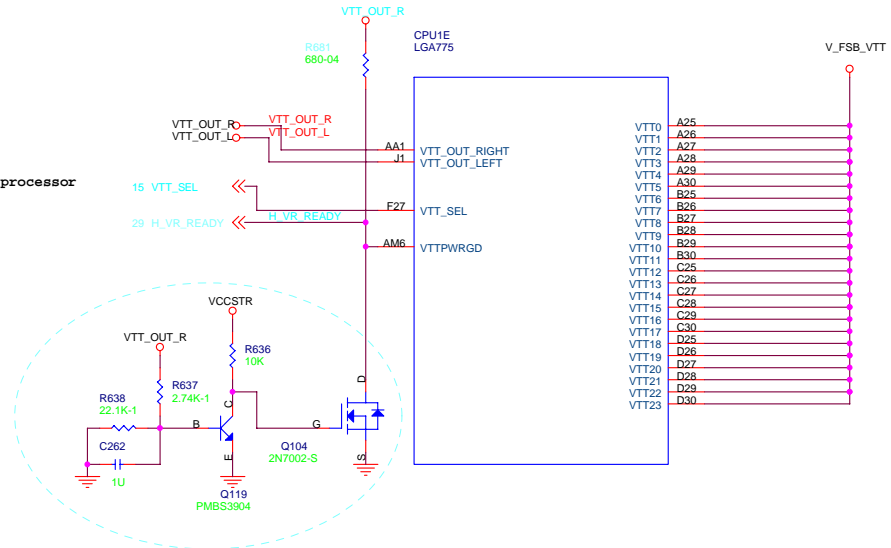


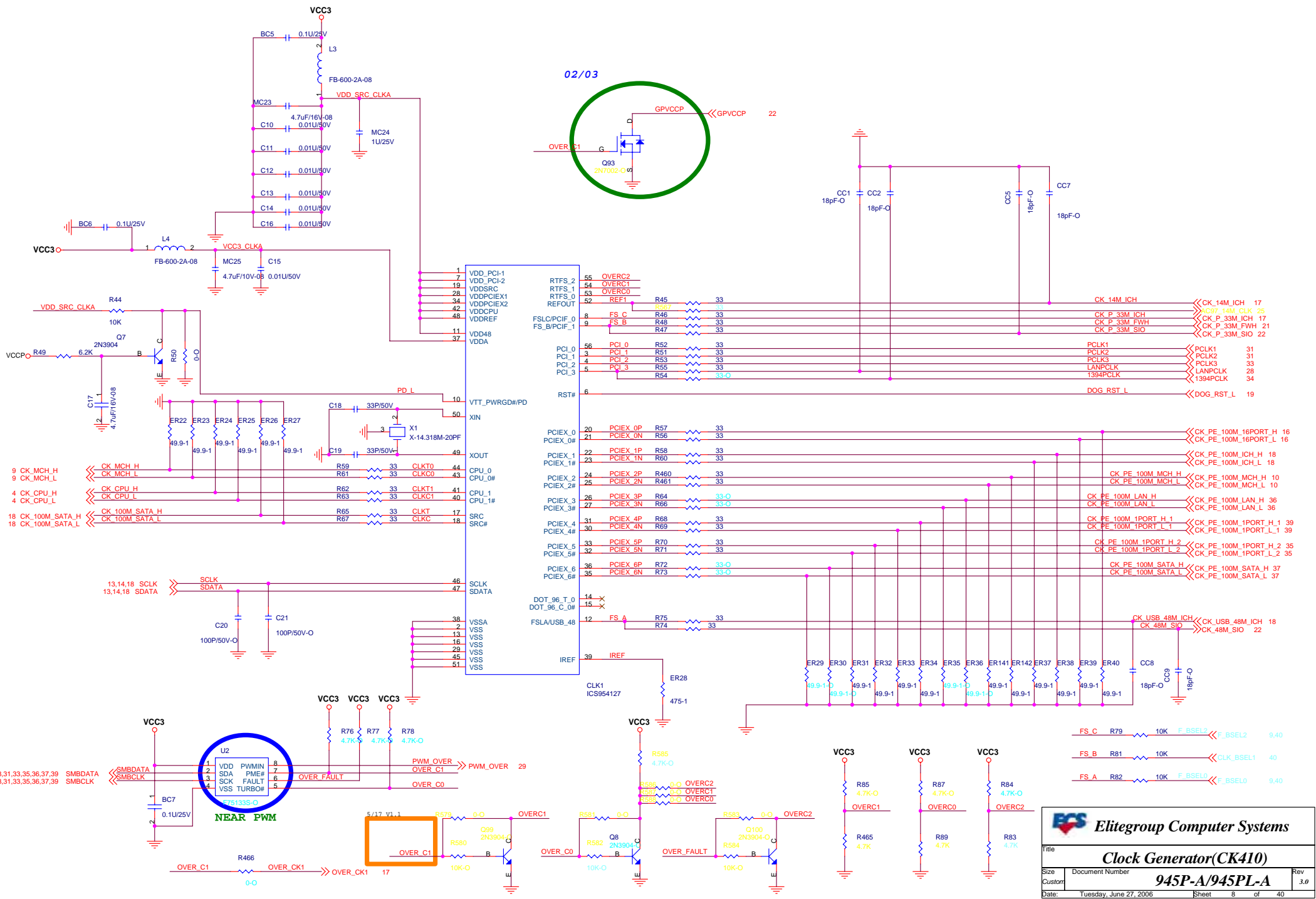
* Placement : Put that CAPs x18 in the processor cavity

* Placement : Put that CAPs x2 on solder side



VTT_SEL=0 for the Tejas processor



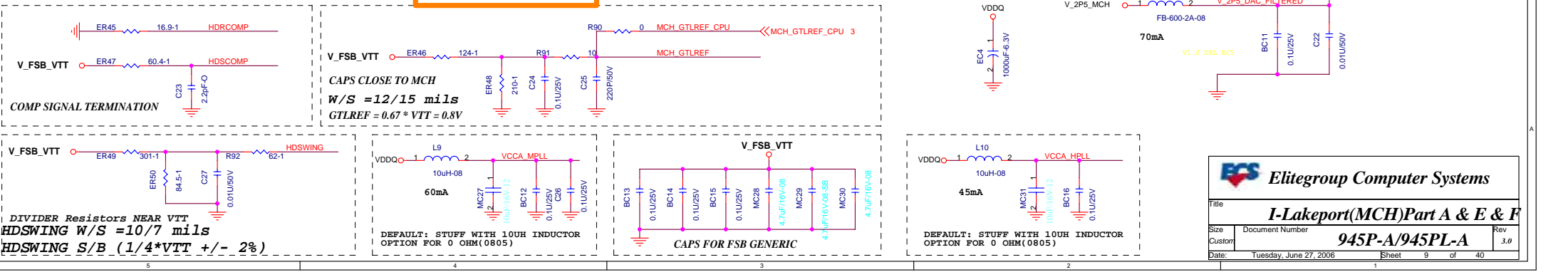
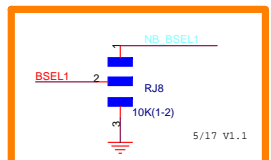
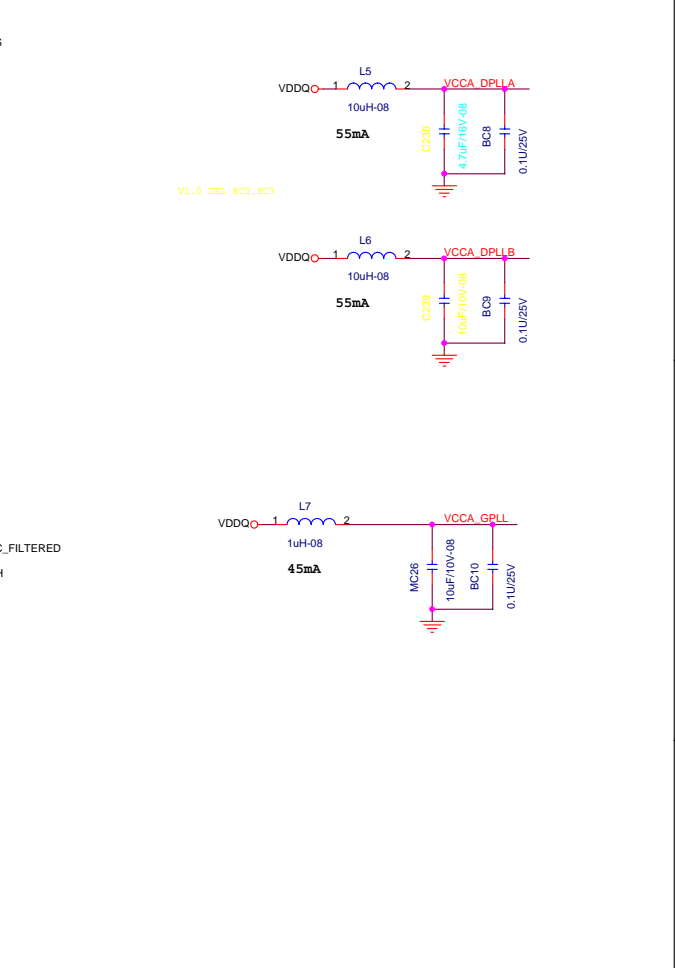
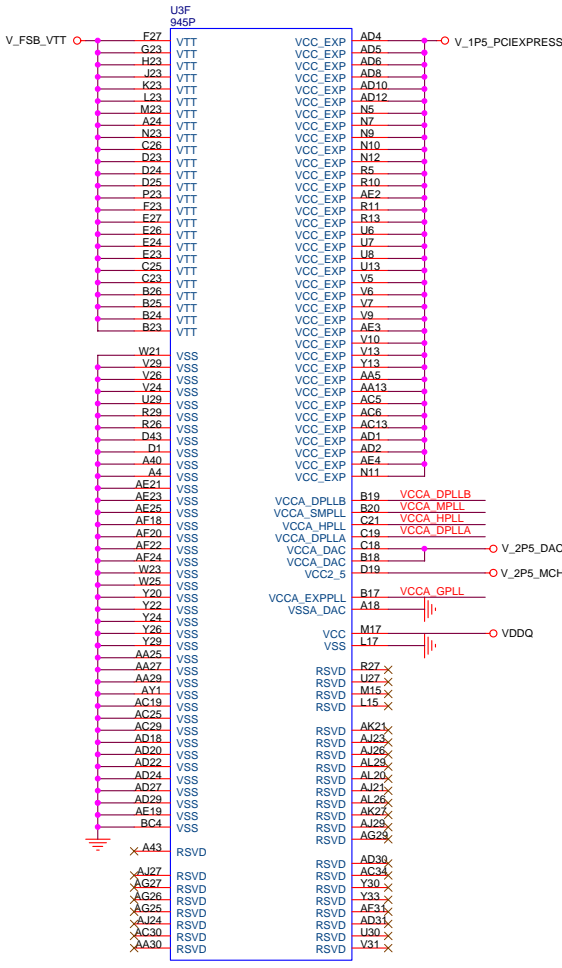


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Title: **Clock Generator(CK410)**

Size	Document Number	Rev
Custom	945P-A/945PL-A	3.0
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U3A 945P				U3F 945P			
3 H_D0	H D0	P41	#HD0	#HA3	H A3	H A3	3
3 H_D1	H D1	M35	#HD1	#HA4	H A4	H A4	3
3 H_D2	H D2	M42	#HD2	#HA5	H A5	H A5	3
3 H_D3	H D3	M42	#HD3	#HA6	H A6	H A6	3
3 H_D4	H D4	M41	#HD4	#HA7	H A7	H A7	3
3 H_D5	H D5	M40	#HD5	#HA8	H A8	H A8	3
3 H_D6	H D6	M40	#HD6	#HA9	H A9	H A9	3
3 H_D7	H D7	M41	#HD7	#HA10	H A10	H A10	3
3 H_D8	H D8	K42	#HD8	#HA11	H A11	H A11	3
3 H_D9	H D9	G34	#HD9	#HA12	H A12	H A12	3
3 H_D10	H D10	G42	#HD10	#HA13	H A13	H A13	3
3 H_D11	H D11	G40	#HD11	#HA14	H A14	H A14	3
3 H_D12	H D12	G40	#HD12	#HA15	H A15	H A15	3
3 H_D13	H D13	G41	#HD13	#HA16	H A16	H A16	3
3 H_D14	H D14	F44	#HD14	#HA17	H A17	H A17	3
3 H_D15	H D15	F44	#HD15	#HA18	H A18	H A18	3
3 H_D16	H D16	F37	#HD16	#HA19	H A19	H A19	3
3 H_D17	H D17	J32	#HD17	#HA20	H A20	H A20	3
3 H_D18	H D18	J32	#HD18	#HA21	H A21	H A21	3
3 H_D19	H D19	D36	#HD19	#HA22	H A22	H A22	3
3 H_D20	H D20	C41	#HD20	#HA23	H A23	H A23	3
3 H_D21	H D21	B39	#HD21	#HA24	H A24	H A24	3
3 H_D22	H D22	B40	#HD22	#HA25	H A25	H A25	3
3 H_D23	H D23	B40	#HD23	#HA26	H A26	H A26	3
3 H_D24	H D24	C37	#HD24	#HA27	H A27	H A27	3
3 H_D25	H D25	J32	#HD25	#HA28	H A28	H A28	3
3 H_D26	H D26	B36	#HD26	#HA29	H A29	H A29	3
3 H_D27	H D27	J32	#HD27	#HA30	H A30	H A30	3
3 H_D28	H D28	B34	#HD28	#HA31	H A31	H A31	3
3 H_D29	H D29	F32	#HD29	RSVD	AA35		3
3 H_D30	H D30	L30	#HD30	RSVD	AA44		3
3 H_D31	H D31	L30	#HD31	RSVD	AA34		3
3 H_D32	H D32	H31	#HD32	RSVD	AA34		3
3 H_D33	H D33	M33	#HD33	RSVD	AA34		3
3 H_D34	H D34	K31	#HD34	#HREQ0	E41	H REQ0	3
3 H_D35	H D35	M26	#HD35	#HREQ1	E41	H REQ1	3
3 H_D36	H D36	K26	#HD36	#HREQ2	E42	H REQ2	3
3 H_D37	H D37	F31	#HD37	#HREQ3	E42	H REQ3	3
3 H_D38	H D38	H29	#HD38	#HREQ4	E42	H REQ4	3
3 H_D39	H D39	F29	#HD39	M36	H A STB0	H A STB0	4
3 H_D40	H D40	L24	#HD40	V35	H A STB1	H A STB1	4
3 H_D41	H D41	M24	#HD41	#HADSTB0			4
3 H_D42	H D42	J26	#HD42	#HADSTB1			4
3 H_D43	H D43	K26	#HD43	HDSTBP0	K41	H D STBP0	4
3 H_D44	H D44	G26	#HD44	#HDSTBN0	K43	H D STBN0	4
3 H_D45	H D45	H24	#HD45	HDSTBN1	K40	H D STBN1	4
3 H_D46	H D46	K24	#HD46	HDSTBP1	F35	H D STBP1	4
3 H_D47	H D47	F24	#HD47	#HDSTBN1	G34	H D STBN1	4
3 H_D48	H D48	E31	#HD48	#HDINV_0	A38	H D STBN1	4
3 H_D49	H D49	A33	#HD49	HDSTBP2	J27	H D STBP2	4
3 H_D50	H D50	E40	#HD50	#HDSTBN2	M26	H D STBN2	4
3 H_D51	H D51	D37	#HD51	HDSTBN3	E29	H D STBN3	4
3 H_D52	H D52	C38	#HD52	#HDINV_3	E34	H D STBP3	4
3 H_D53	H D53	D38	#HD53	HDSTBP3	B37	H D STBN3	4
3 H_D54	H D54	D33	#HD54	#HDINV_3	B32	H DIB3	4
3 H_D55	H D55	C36	#HD55	W42	H ADS L	H ADS L	4
3 H_D56	H D56	D34	#HD56	W40	H TRDY L	H TRDY L	4
3 H_D57	H D57	C34	#HD57	W41	H DRDY L	H DRDY L	4
3 H_D58	H D58	B31	#HD58	P40	H DEFER L	H DEFER L	4
3 H_D59	H D59	C31	#HD59	U41	H HITM L	H HITM L	4
3 H_D60	H D60	C32	#HD60	U41	H HIT L	H HIT L	4
3 H_D61	H D61	D36	#HD61	U40	H LOCK L	H LOCK L	4
3 H_D62	H D62	B30	#HD62	AA41	H BREQ0 L	H BREQ0 L	4
3 H_D63	H D63	D30	#HD63	U39	H BNR L	H BNR L	4
				U38	H BPRI L	H BPRI L	4
				U42	H DBSY L	H DBSY L	4
				T40	H RSO L	H RSO L	3
				T43	H RS2 L	H RS2 L	3
				L43	H RS2 L	H RS2 L	3
				C30	H CPURST L	H CPURST L	4
				F38			4
				Y40			4
				F21	BSEL0	E42	10K
				H21	BSEL1		
				L20	BSEL2		



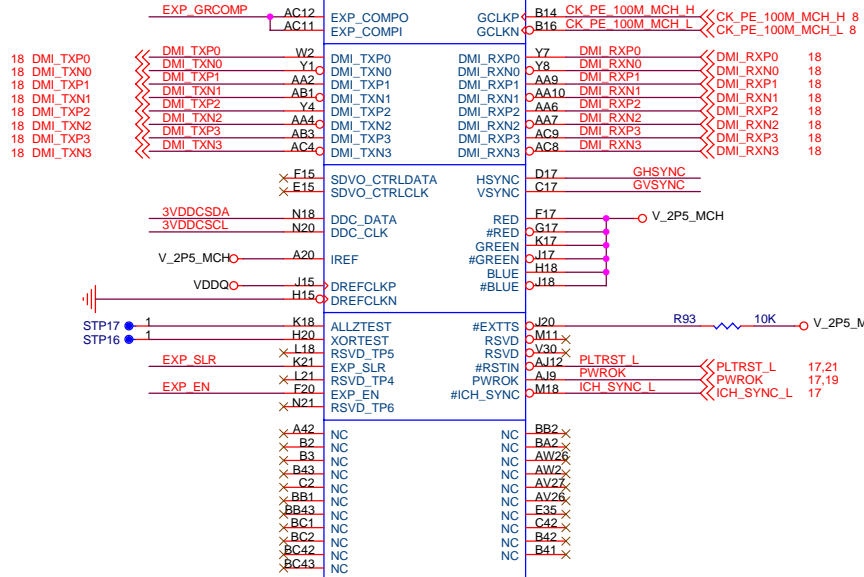
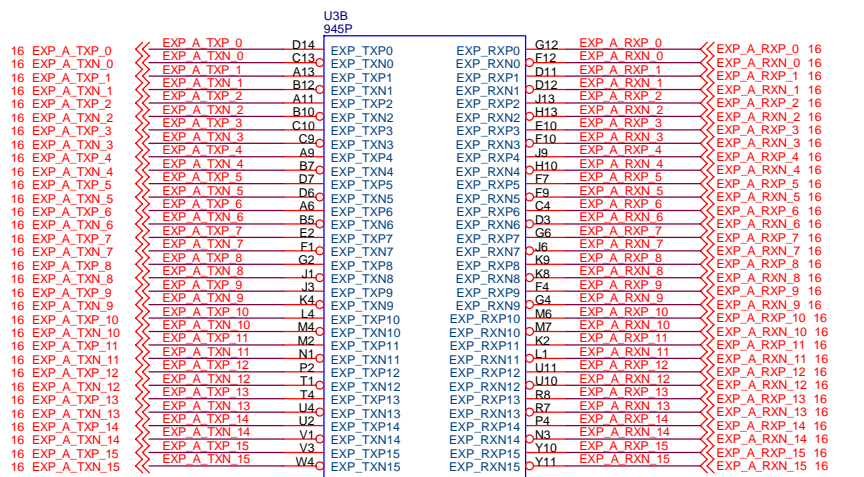
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I-Lakeport(MCH)Part A & E & F

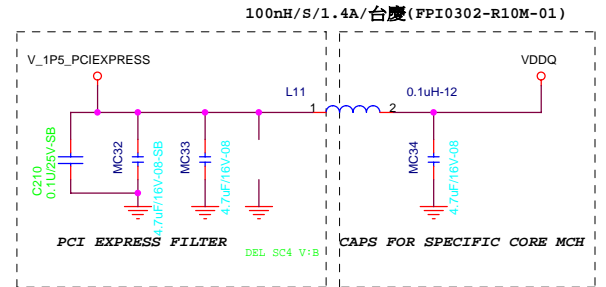
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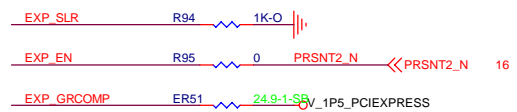
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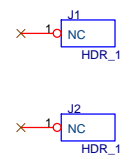
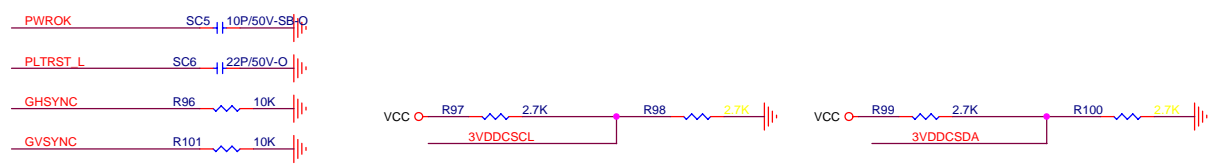
Place close to GMCH 750Mil.



The LC filter is required to source 1.4A of current with less than 30mV of drop across the filter.



COMP SIGNAL TERMINATION

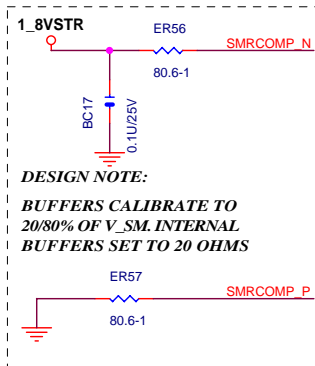
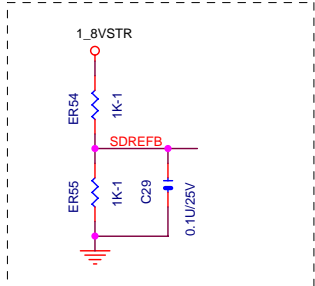
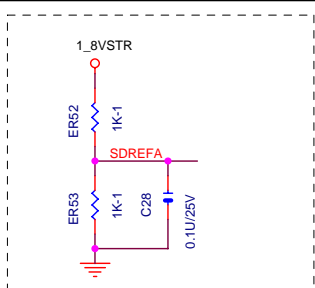


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Title: **I-Lakeport(MCH)Part D**

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DESIGN NOTE:
BUFFERS CALIBRATE TO
20/80% OF V_{SM} INTERNAL
BUFFERS SET TO 20 OHMS

U3C 945P			
DQS_H_A4	AU35	SDQS_A0	AU4
DQS_L_A4	AV35	#SDQS_A0	AR2
MPD_A4	AT34	SDM_A4	AR3
MD_A32	AP32	SDQ_A32	AP3
MD_A33	AV34	SDQ_A33	AP2
MD_A34	AV38	SDQ_A34	AU3
MD_A35	AU39	SDQ_A35	MD_A2
MD_A36	AV32	SDQ_A36	MD_A3
MD_A37	AT32	SDQ_A37	AN1
MD_A38	AR34	SDQ_A38	MD_A4
MD_A39	AU37	SDQ_A39	AP4
DQS_H_A5	AP42	SDQS_A5	AU5
DQS_L_A5	AP40	#SDQS_A5	MD_A6
MPD_A5	AP39	SDM_A5	AU2
MD_A40	AR41	SDQ_A40	MD_A7
MD_A41	AR42	SDQ_A41	BA3
MD_A42	AN43	SDQ_A42	DQS_H_A1
MD_A43	AM40	SDQ_A43	DQS_L_A1
MD_A44	AU41	SDQ_A44	MPD_A1
MD_A45	AU42	SDQ_A45	AW2
MD_A46	AP41	SDQ_A46	MD_A8
MD_A47	AN40	SDQ_A47	AY3
DQS_H_A6	AC42	SDQS_A6	MD_A9
DQS_L_A6	AC41	#SDQS_A6	MD_A10
MPD_A6	AG40	SDM_A6	MD_A11
MD_A48	AL41	SDQ_A48	MD_A12
MD_A49	AL42	SDQ_A49	MD_A13
MD_A50	AF39	SDQ_A50	MD_A14
MD_A51	AE40	SDQ_A51	MD_A15
MD_A52	AM41	SDQ_A52	AY11
MD_A53	AM42	SDQ_A53	DQS_H_A2
MD_A54	AF41	SDQ_A54	DQS_L_A2
MD_A55	AF42	SDQ_A55	MPD_A2
DQS_H_A7	AC42	SDQS_A7	AW7
DQS_L_A7	AC41	#SDQS_A7	MD_A8
MPD_A7	AC40	SDM_A7	MD_A9
MD_A56	AD40	SDQ_A56	MD_A10
MD_A57	AD43	SDQ_A57	MD_A11
MD_A58	AA39	SDQ_A58	MD_A12
MD_A59	AA40	SDQ_A59	MD_A13
MD_A60	AE42	SDQ_A60	MD_A14
MD_A61	AE41	SDQ_A61	MD_A15
MD_A62	AB41	SDQ_A62	AY11
MD_A63	AB42	SDQ_A63	DQS_H_A2
MAAA_0	BA32	SMA_A0	DQS_L_A2
MAAA_1	AW32	SMA_A1	MPD_A2
MAAA_2	BB30	SMA_A2	AW7
MAAA_3	BA30	SMA_A3	MD_A8
MAAA_4	AY30	SMA_A4	MD_A9
MAAA_5	BA27	SMA_A5	MD_A10
MAAA_6	BC28	SMA_A6	MD_A11
MAAA_7	AY27	SMA_A7	MD_A12
MAAA_8	AY28	SMA_A8	MD_A13
MAAA_9	BB27	SMA_A9	MD_A14
MAAA_10	AY33	SMA_A10	MD_A15
MAAA_11	AW27	SMA_A11	AY11
MAAA_12	BB26	SMA_A12	DQS_H_A2
MAAA_13	BC38	SMA_A13	DQS_L_A2
DCLKA_H0	BB32	SCKL_A0	MPD_A2
DCLKA_L0	AY32	#SCKL_A0	AW7
DCLKA_H1	AY5	SCKL_A1	MD_A8
DCLKA_L1	BB5	#SCKL_A1	MD_A9
DCLKA_H2	AK42	SCKL_A2	MD_A10
DCLKA_L2	AK41	#SCKL_A2	MD_A11
DCLKA_H3	BA31	SCKL_A3	MD_A12
DCLKA_L3	BB31	#SCKL_A3	MD_A13
DCLKA_H4	AY6	SCKL_A4	MD_A14
DCLKA_L4	AY6	#SCKL_A4	MD_A15
DCLKA_H5	BA5	SCKL_A5	AY11
DCLKA_L5	AH43	#SCKL_A5	DQS_H_A2
STP21	1	AL17	DQS_L_A2
STP20	1	AK17	MPD_A2
		RSVD_TP1	AW7
		RSVD_TP0	MD_A8
		SVREF0	MD_A9

U3D 945P			
DQS_H_B4	AT29	SDQS_B4	AM8
DQS_L_B4	AV29	#SDQS_B4	DQS_H_B0
MPD_B4	AR29	SDM_B4	AM6
MD_B32	AU27	SDQ_B32	DQS_L_B0
MD_B33	AN29	SDQ_B33	MPD_B0
MD_B34	AR31	SDQ_B34	AL6
MD_B35	AM31	SDQ_B35	MD_B0
MD_B36	AP27	SDQ_B36	AL8
MD_B37	AR27	SDQ_B37	MD_B1
MD_B38	AP31	SDQ_B38	AP9
MD_B39	AU31	SDQ_B39	MD_B2
DQS_H_B5	AP36	SDQS_B5	MD_B3
DQS_L_B5	AM35	#SDQS_B5	AP8
MPD_B5	AR38	SDM_B5	MD_B4
MD_B40	AP35	SDQ_B40	AL11
MD_B41	AP37	SDQ_B41	MD_B5
MD_B42	AN32	SDQ_B42	MD_B6
MD_B43	AL35	SDQ_B43	MD_B7
MD_B44	AR35	SDQ_B44	AV7
MD_B45	AU38	SDQ_B45	DQS_H_B1
MD_B46	AM38	SDQ_B46	DQS_L_B1
MD_B47	AM34	SDQ_B47	MPD_B1
DQS_H_B6	AG34	SDQS_B6	AW7
DQS_L_B6	AG32	#SDQS_B6	MD_B8
MPD_B6	AJ39	SDM_B6	MD_B9
MD_B48	AL34	SDQ_B48	MD_B10
MD_B49	AJ34	SDQ_B49	MD_B11
MD_B50	AF32	SDQ_B50	MD_B12
MD_B51	AF34	SDQ_B51	MD_B13
MD_B52	AL31	SDQ_B52	MD_B14
MD_B53	AJ32	SDQ_B53	MD_B15
MD_B54	AG35	SDQ_B54	AV13
MD_B55	AD32	SDQ_B55	DQS_H_B2
DQS_H_B7	AD36	SDQS_B7	DQS_L_B2
DQS_L_B7	AD38	#SDQS_B7	MPD_B2
MPD_B7	AD39	SDM_B7	AW7
MD_B56	AC32	SDQ_B56	MD_B16
MD_B57	AD34	SDQ_B57	MD_B17
MD_B58	Y32	SDQ_B58	MD_B18
MD_B59	AA32	SDQ_B59	MD_B19
MD_B60	AF35	SDQ_B60	MD_B20
MD_B61	AF37	SDQ_B61	MD_B21
MD_B62	AC33	SDQ_B62	MD_B22
MD_B63	AC35	SDQ_B63	MD_B23
MAAB_0	BB22	SMA_B0	AM15
MAAB_1	BB21	SMA_B1	MD_B16
MAAB_2	BA21	SMA_B2	MD_B17
MAAB_3	AY21	SMA_B3	MD_B18
MAAB_4	BC20	SMA_B4	MD_B19
MAAB_5	AY19	SMA_B5	MD_B20
MAAB_6	AY20	SMA_B6	MD_B21
MAAB_7	BA18	SMA_B7	MD_B22
MAAB_8	BA19	SMA_B8	MD_B23
MAAB_9	BB18	SMA_B9	AV15
MAAB_10	BA22	SMA_B10	MD_B24
MAAB_11	BB17	SMA_B11	MD_B25
MAAB_12	BA17	SMA_B12	MD_B26
MAAB_13	AW42	SMA_B13	MD_B27
DCLKB_H0	AM29	SCKL_B0	MD_B28
DCLKB_L0	AM27	#SCKL_B0	MD_B29
DCLKB_H1	AV9	SCKL_B1	MD_B30
DCLKB_L1	AW9	#SCKL_B1	MD_B31
DCLKB_H2	AL38	SCKL_B2	AM24
DCLKB_L2	AL36	#SCKL_B2	MD_B24
DCLKB_H3	AP26	SCKL_B3	MD_B25
DCLKB_L3	AR26	#SCKL_B3	MD_B26
DCLKB_H4	AU10	SCKL_B4	MD_B27
DCLKB_L4	AT10	#SCKL_B4	MD_B28
DCLKB_H5	AJ38	SCKL_B5	MD_B29
DCLKB_L5	AJ36	#SCKL_B5	MD_B30
STP23	1	AK18	MD_B31
STP22	1	AK23	MD_B32
		RSVD_TP3	BB23
		RSVD_TP2	SWE_L_B
		SVREF1	MD_B24

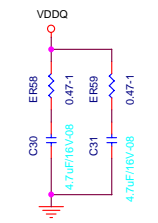
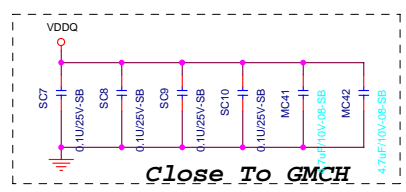
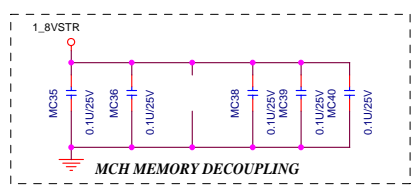
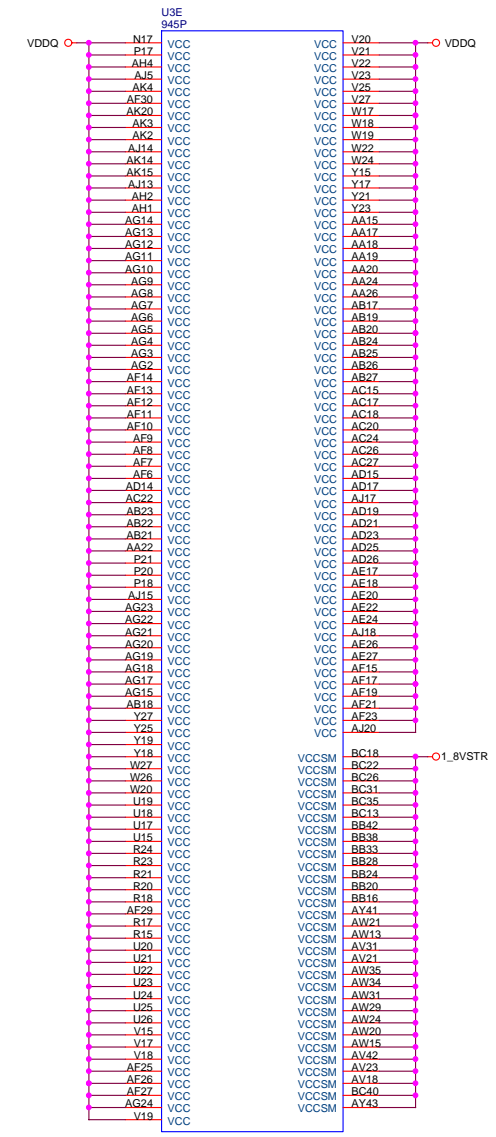
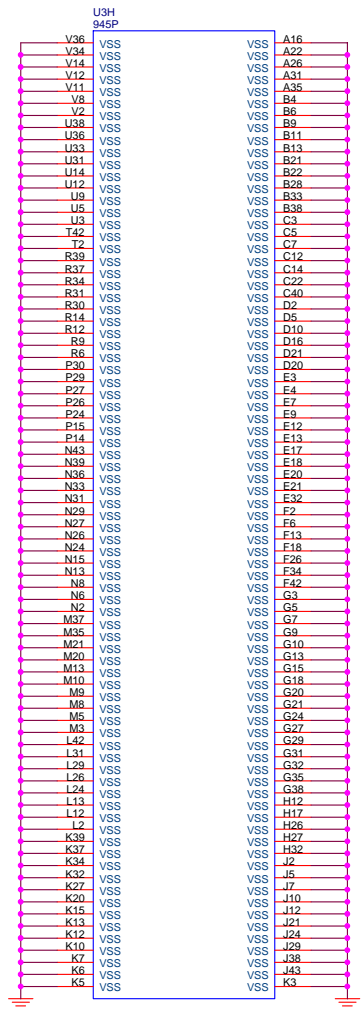
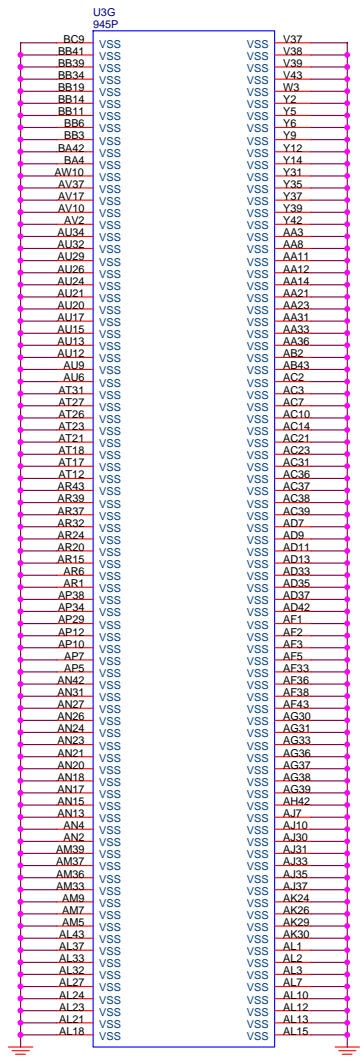
13 MD_A[0..63]	MD A[0..63]
13 DQS_L_A[0..7]	DQS L A[0..7]
13 DQS_H_A[0..7]	DQS H A[0..7]
13 MPD_A[0..7]	MPD A[0..7]
13 MAAA_[0..13]	MAAA [0..13]
13 CSA_L[0..3]	CSA L[0..3]
13 CKEA_[0..3]	CKEA [0..3]
13 DCLKA_L[0..5]	DCLKA L[0..5]
13 DCLKA_H[0..5]	DCLKA H[0..5]
13 ODTA_[0..3]	ODTA [0..3]
13 SBSA_[0..2]	SBSA [0..2]
13 SWE_L_A	SWE L_A
13 SCAS_L_A	SCAS L_A
13 SRAS_L_A	SRAS L_A
14 MD_B[0..63]	MD B[0..63]
14 DQS_L_B[0..7]	DQS L B[0..7]
14 DQS_H_B[0..7]	DQS H B[0..7]
14 MPD_B[0..7]	MPD B[0..7]
14 MAAB_[0..13]	MAAB [0..13]
14 CSB_L[0..3]	CSB L[0..3]
14 CKEB_[0..3]	CKEB [0..3]
14 DCLKB_L[0..5]	DCLKB L[0..5]
14 DCLKB_H[0..5]	DCLKB H[0..5]
14 ODTB_[0..3]	ODTB [0..3]
14 SBSB_[0..2]	SBSB [0..2]
14 SWE_L_B	SWE L_B
14 SCAS_L_B	SCAS L_B
14 SRAS_L_B	SRAS L_B
SOCOMP1	AM3
SOCOMP0	AJ8
SRCOMP1	AJ6
SRCOMP0	AL5
AL39	
AM2	

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Title: **I-Lakeport(MCH)Part B & C**

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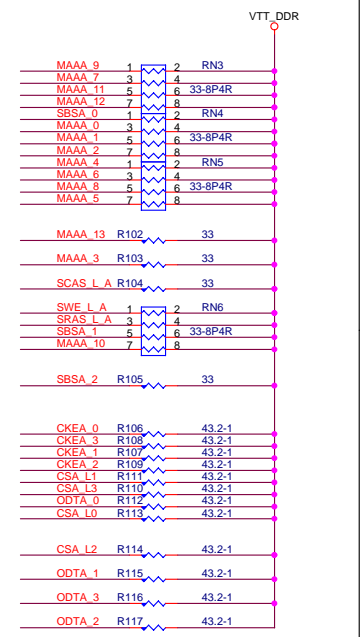
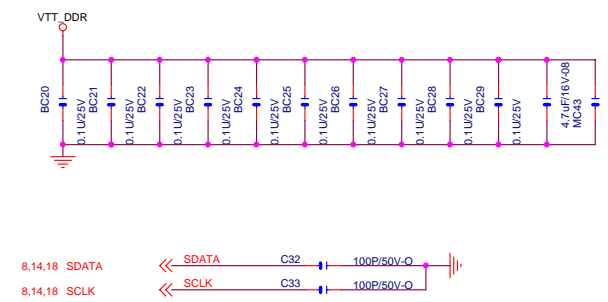
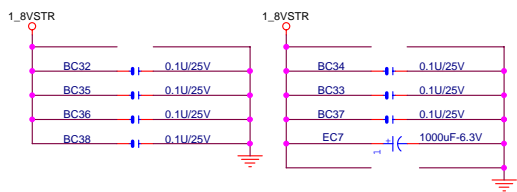
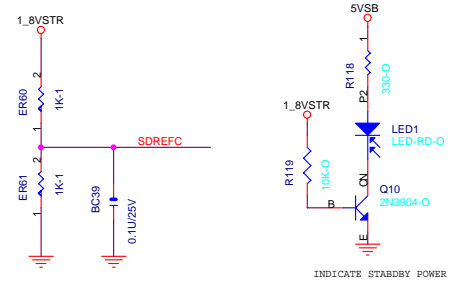
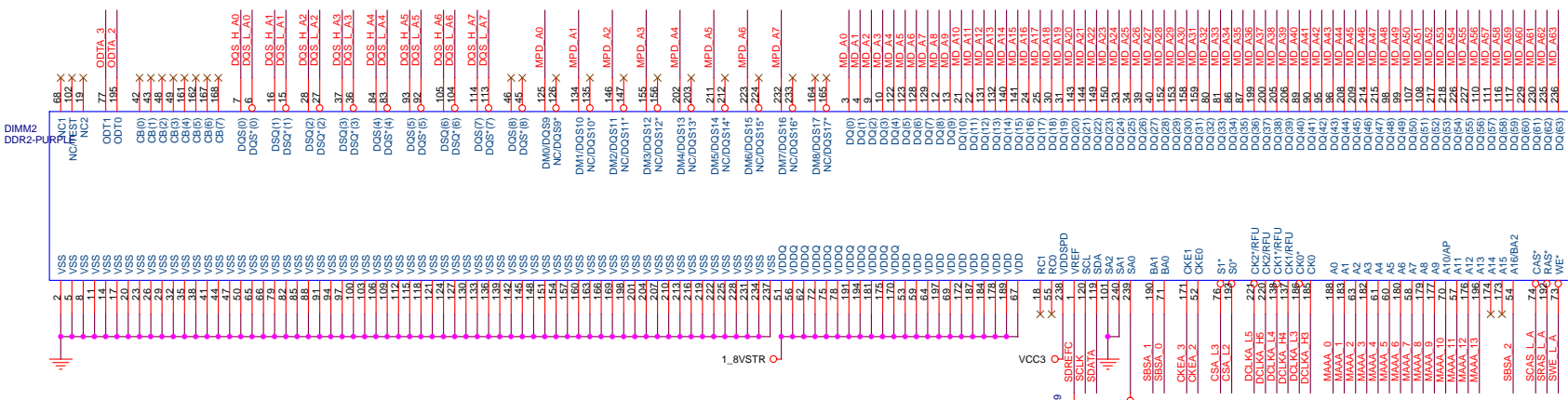
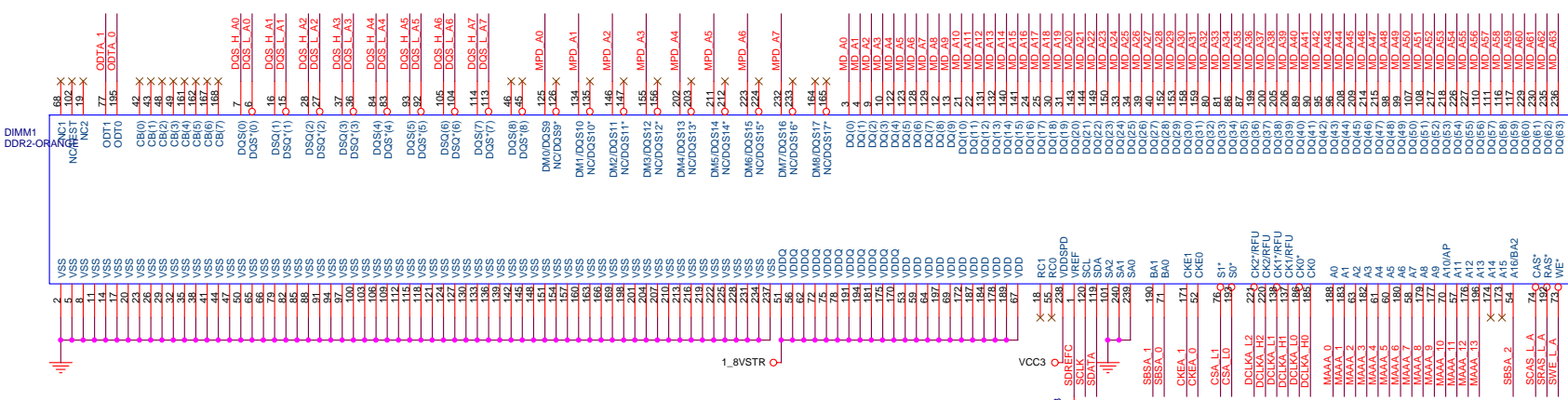
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File: **Schematic Change History**

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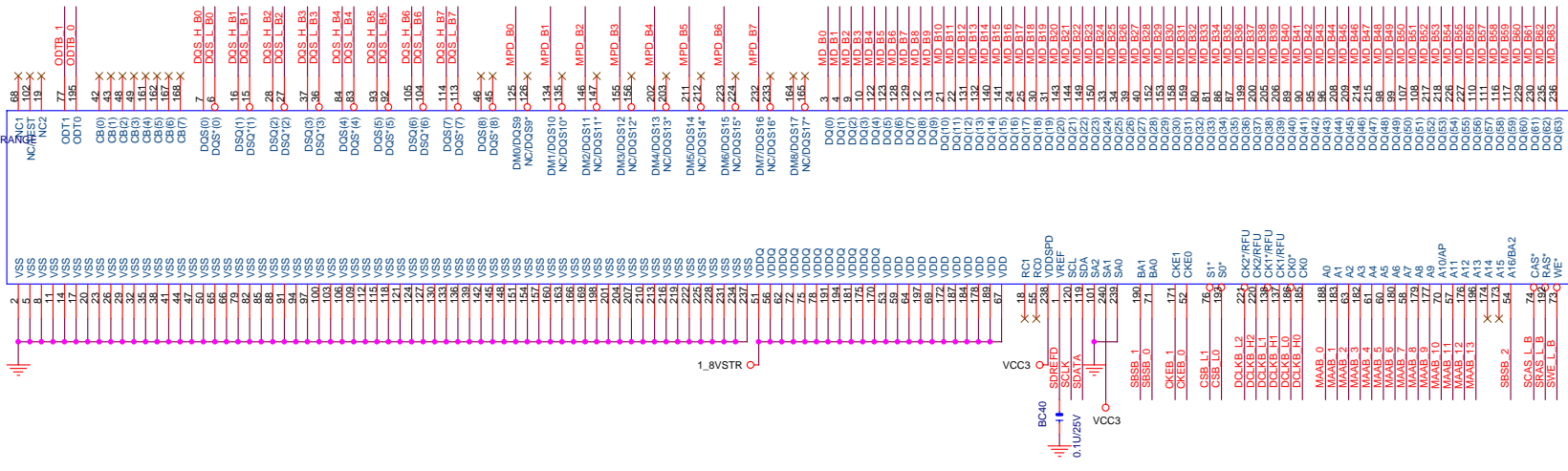
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- 11 DOS_L_A[0..7] <<< DOS_L_A[0..7]
- 11 DOS_H_A[0..7] <<< DOS_H_A[0..7]
- 11 MPD_A[0..7] <<< MPD_A[0..7]
- 11 MAAA_10..13] <<< MAAA_10..13]
- 11 CSA_L[0..3] <<< CSA_L[0..3]
- 11 CKEA_10..3] <<< CKEA_10..3]
- 11 DCLKA_L[0..5] <<< DCLKA_L[0..5]
- 11 DCLKA_H[0..5] <<< DCLKA_H[0..5]
- 11 ODTA_10..3] <<< ODTA_10..3]
- 11 SBSA_10..2] <<< SBSA_10..2]
- 11 SWE_L_A <<< SWE_L_A
- 11 SCAS_L_A <<< SCAS_L_A
- 11 SRAS_L_A <<< SRAS_L_A

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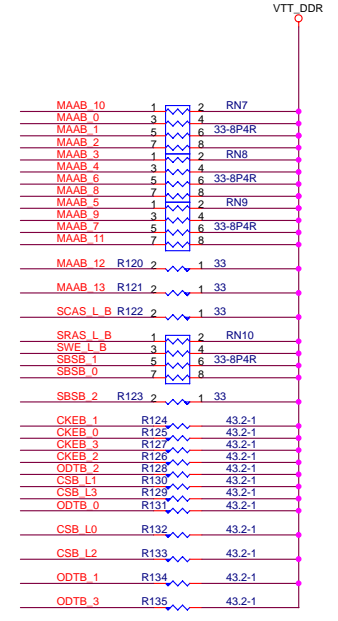
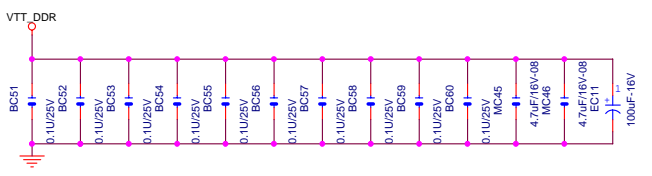
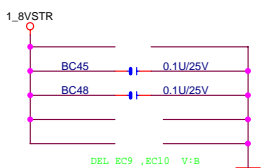
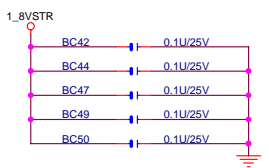
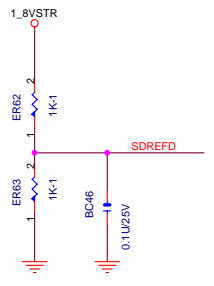
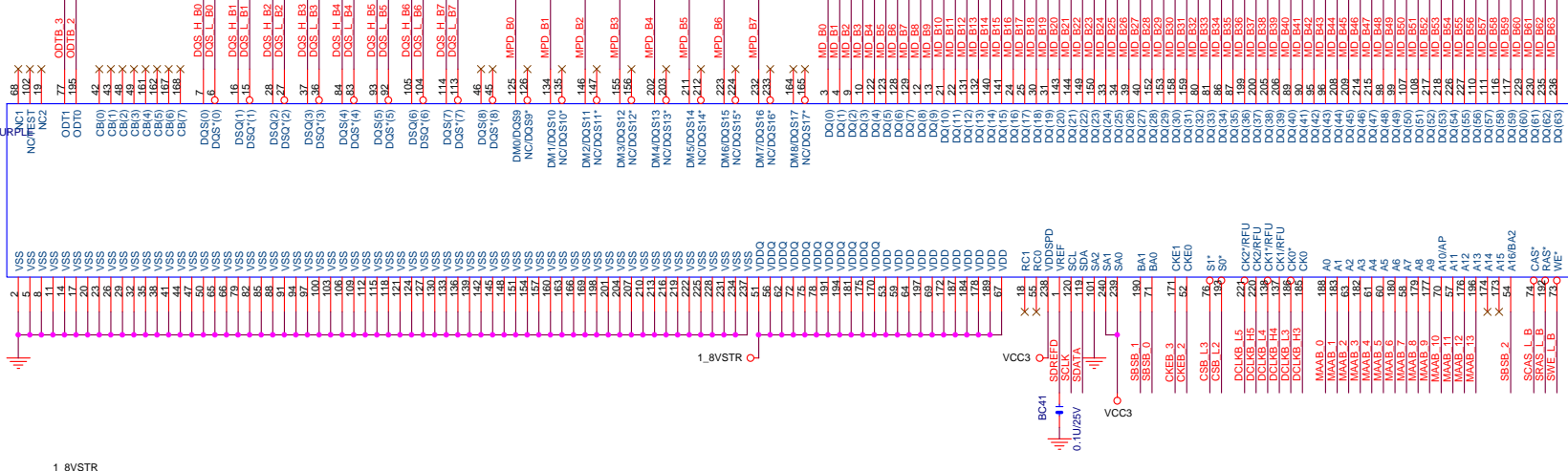
DDIMM 1&2 (DDR SDRAMs)

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DIMM3
DDR2-ORAM



DIMM4
DDR2-PUR



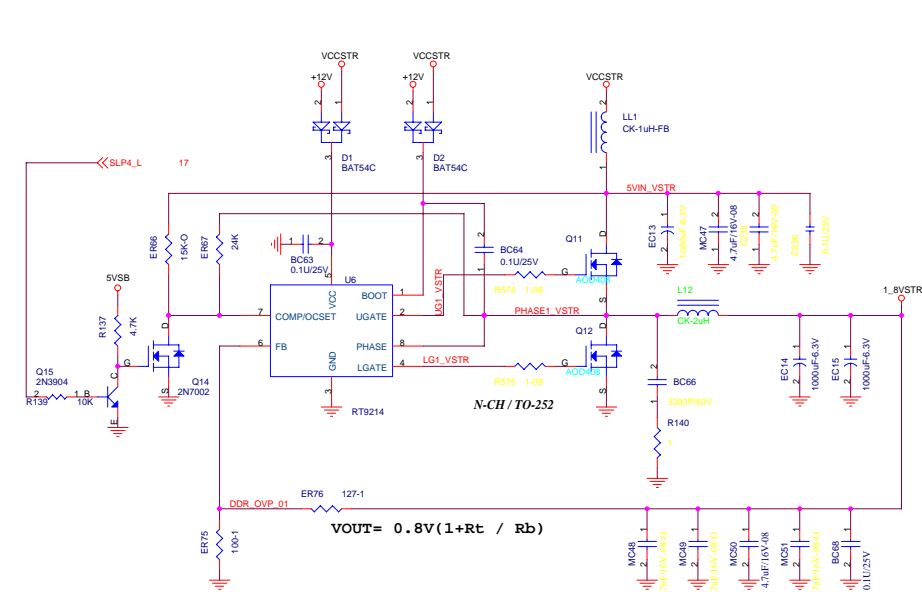
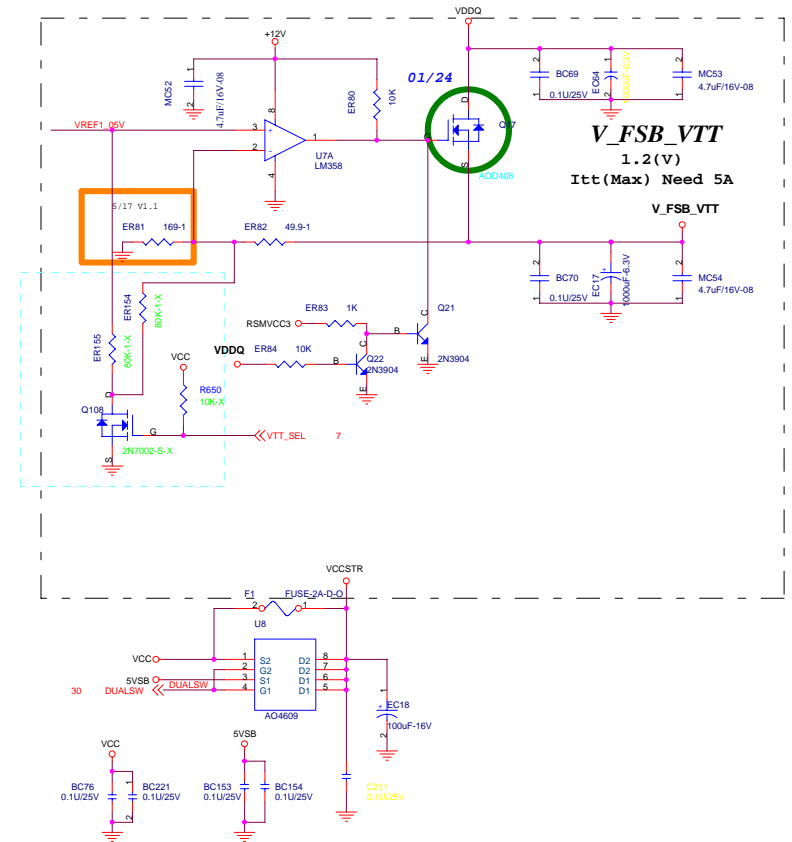
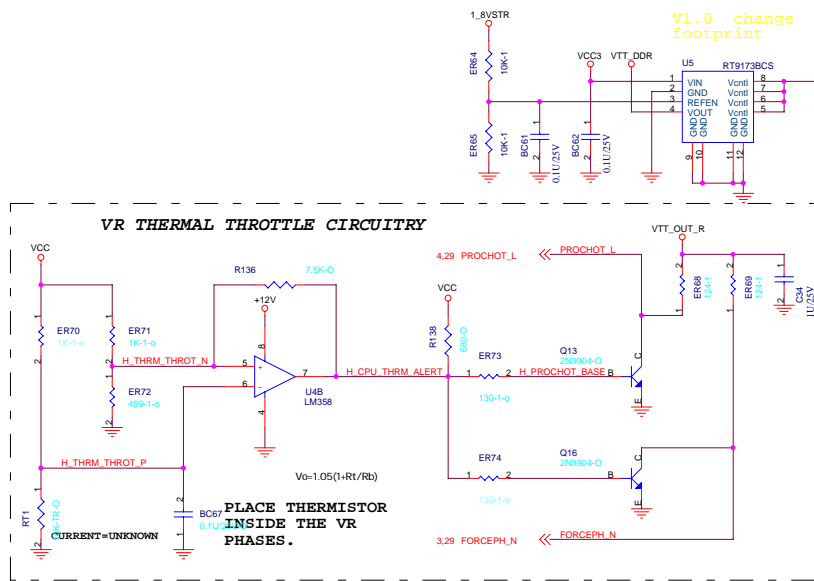
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- 11 DQS_L[0..7] <<< DQS_L_B[0..7]
- 11 DQS_H[0..7] <<< DQS_H_B[0..7]
- 11 MPD_B[0..7] <<< MPD_B[0..7]
- 11 MAAB[0..13] <<< MAAB[0..13]
- 11 CSB_L[0..3] <<< CSB_L[0..3]
- 11 CKEB[0..3] <<< CKEB[0..3]
- 11 DCLKB_L[0..5] <<< DCLKB_L[0..5]
- 11 DCLKB_H[0..5] <<< DCLKB_H[0..5]
- 11 ODTB[0..3] <<< ODTB[0..3]
- 11 SSSB[0..2] <<< SSSB[0..2]
- 11 SWE_L_B <<< SWE_L_B
- 11 SCAS_L_B <<< SCAS_L_B
- 11 SRAS_L_B <<< SRAS_L_B

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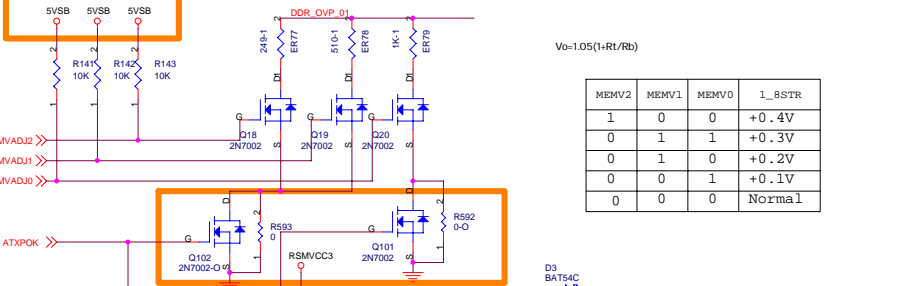
File: **DDIMM 3&4 (DDR SDRAMs)**

Size: Document Number
 Custor: **945P-A/945PL-A** Rev: 3.0

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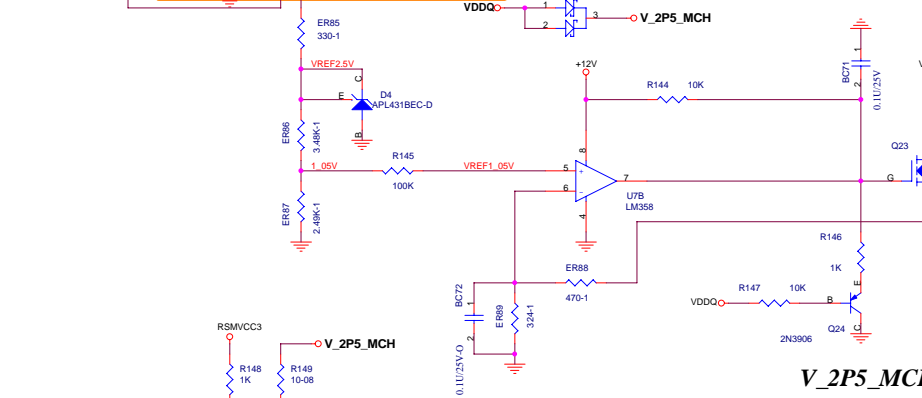


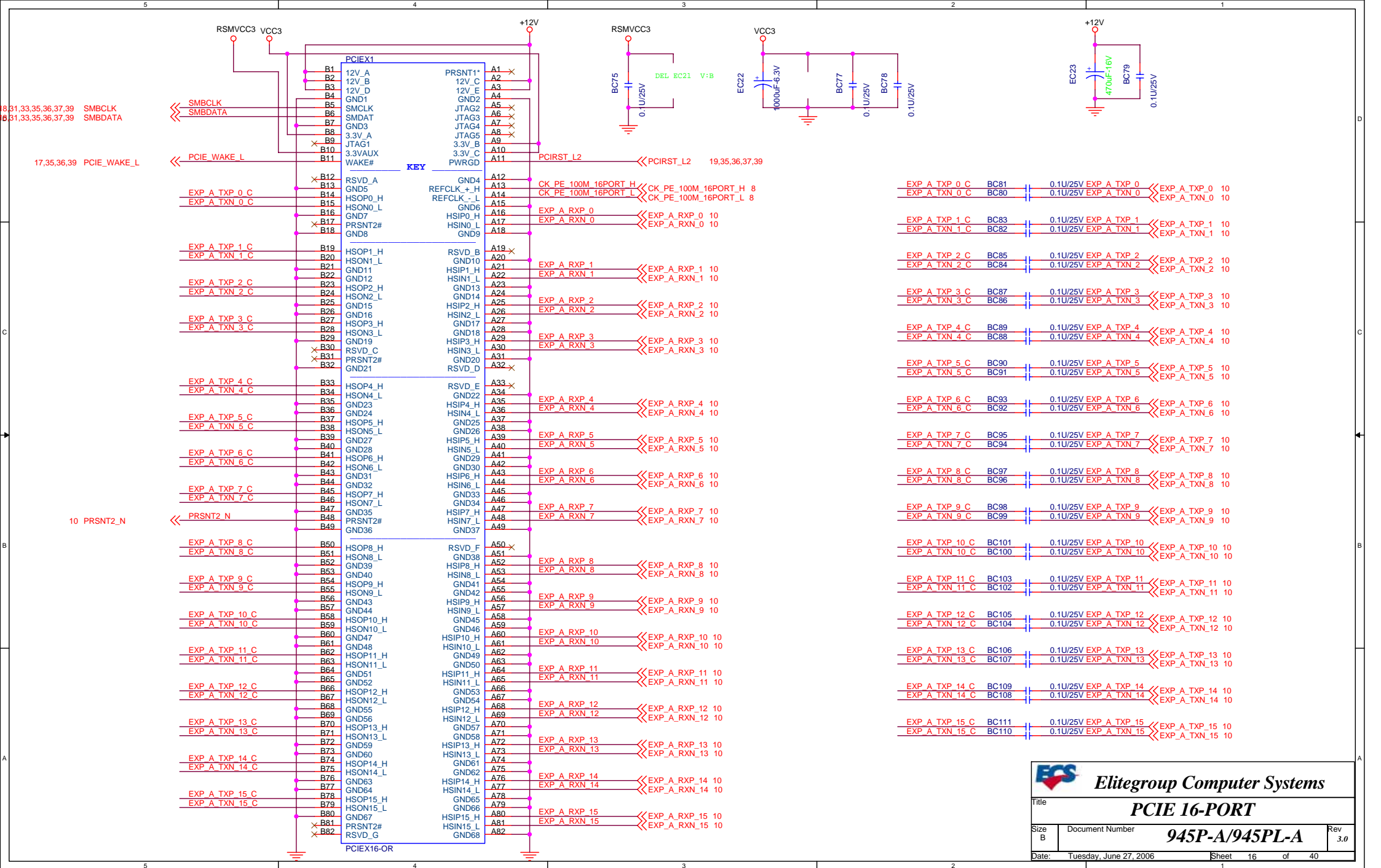
1.8VSTR should be able to support up to 14A



$V_D = 1.05(1 + R_T / R_b)$

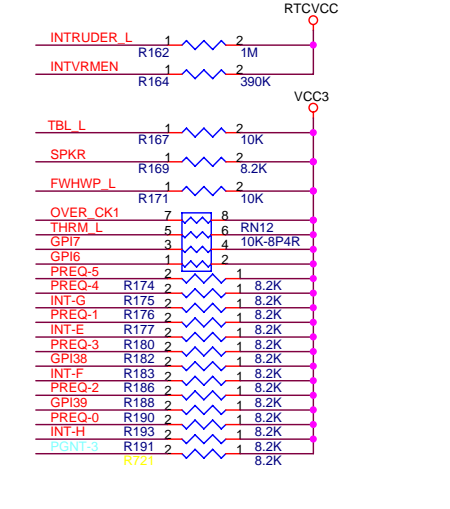
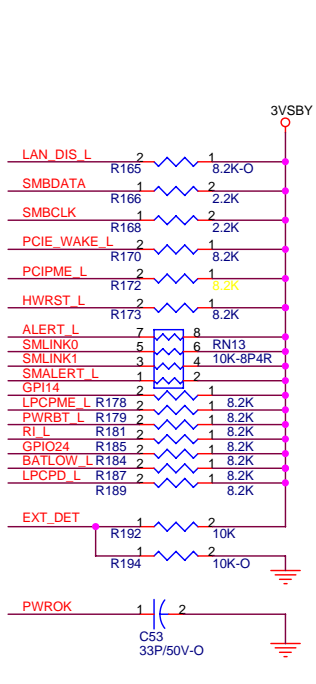
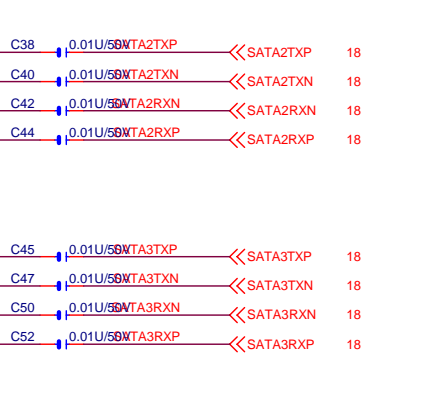
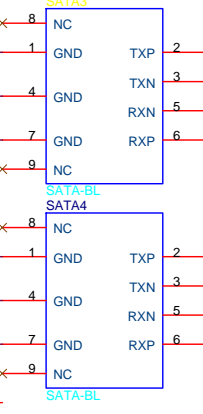
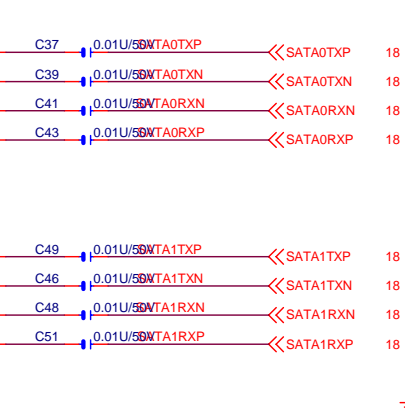
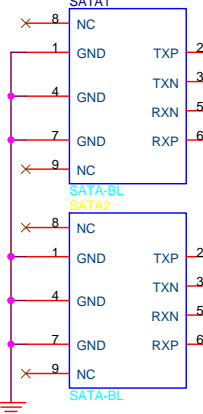
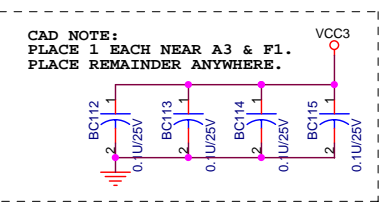
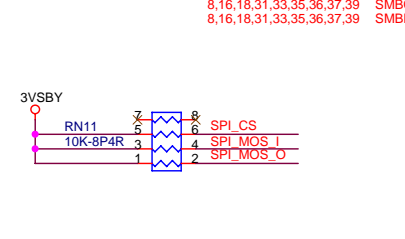
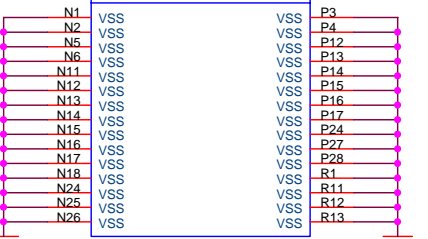
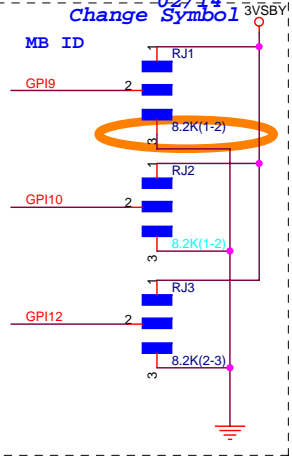
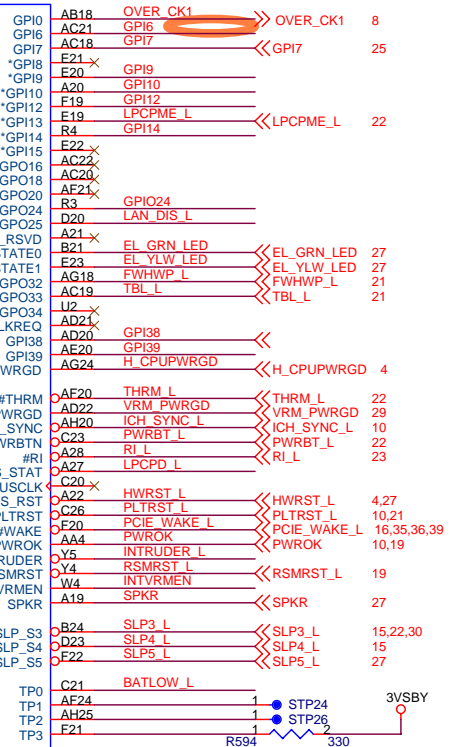
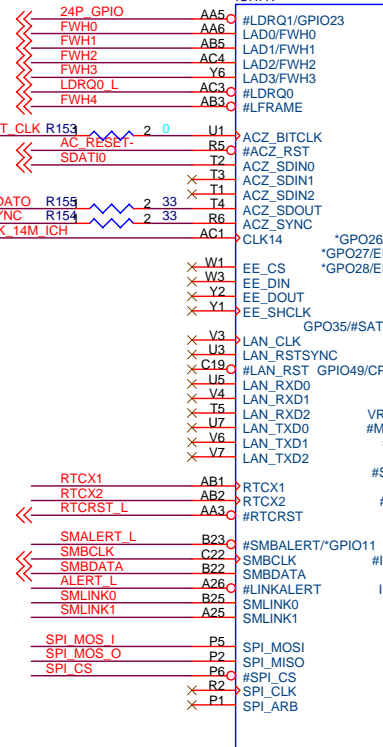
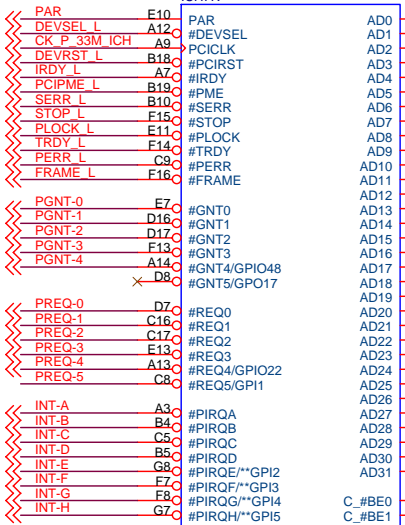
MEMV2	MEMV1	MEMV0	1_8STR
1	0	0	+0.4V
0	1	1	+0.3V
0	1	0	+0.2V
0	0	1	+0.1V
0	0	0	Normal





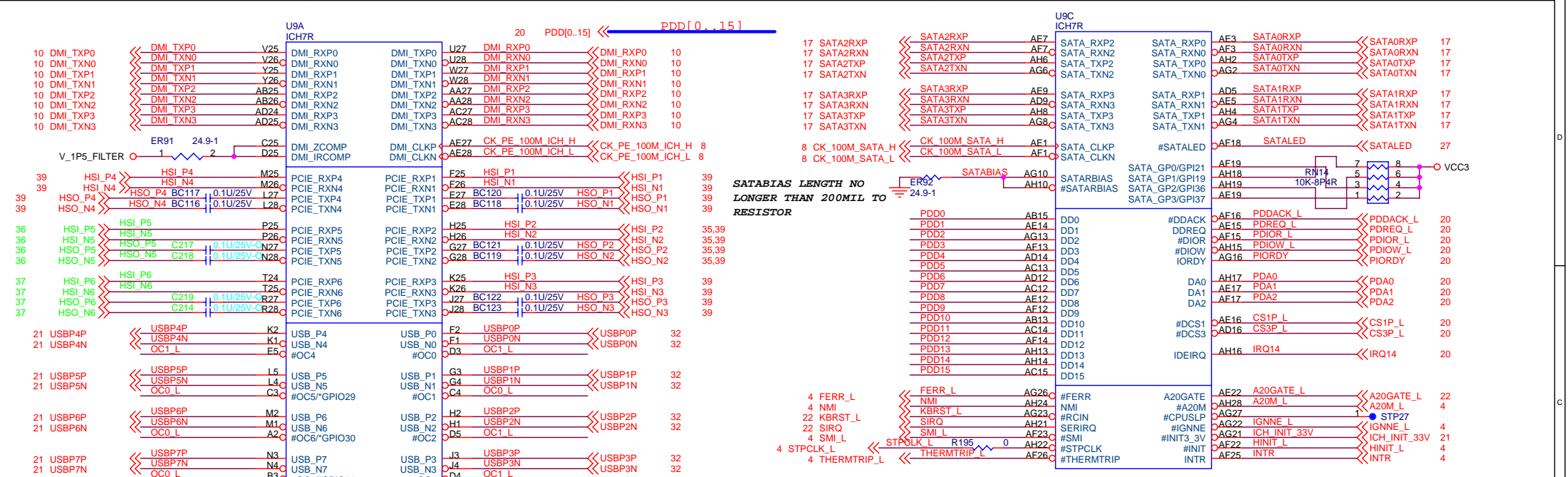
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Size B	Document Number	945P-A/945PL-A	
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28,31,33,34 PAR
28,31,33,34 DEVSEL_L
8 CK_P_33M_ICH
19 DEVRST_L
28,31,33,34 IRDY_L
28,31,33,34 PCIPME_L
28,31,33,34 SERR_L
28,31,33,34 STOP_L
31,33 PLOCK_L
28,31,33,34 TRDY_L
28,31,33,34 PERR_L
28,31,33,34 FRAME_L

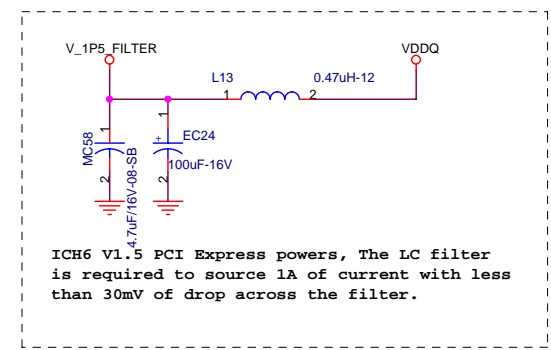


Elitegroup Computer Systems
ICH7 Part A & D

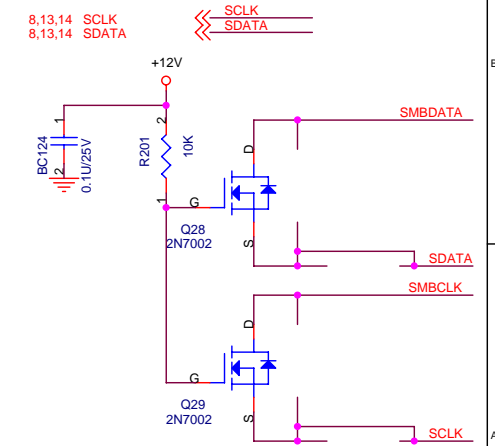
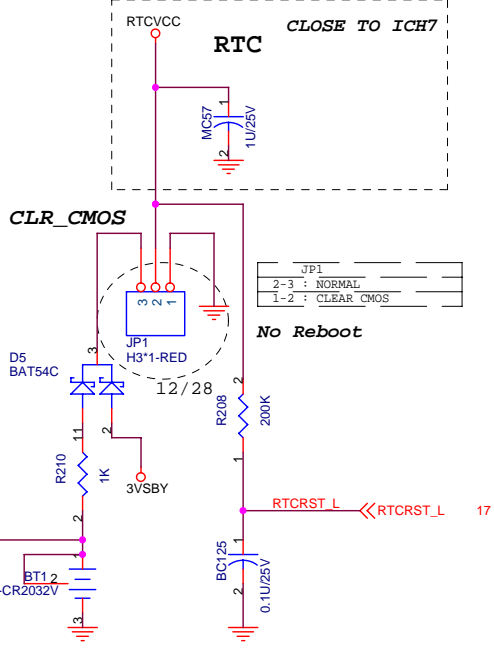
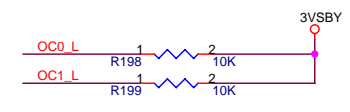
Title	Elitegroup Computer Systems		
Size	Document Number	945P-A/945PL-A	
Custom		Rev	3.0
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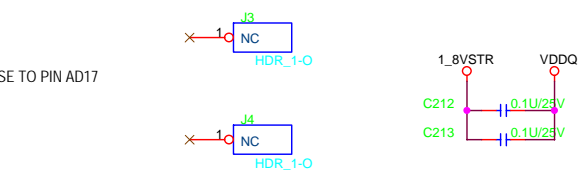
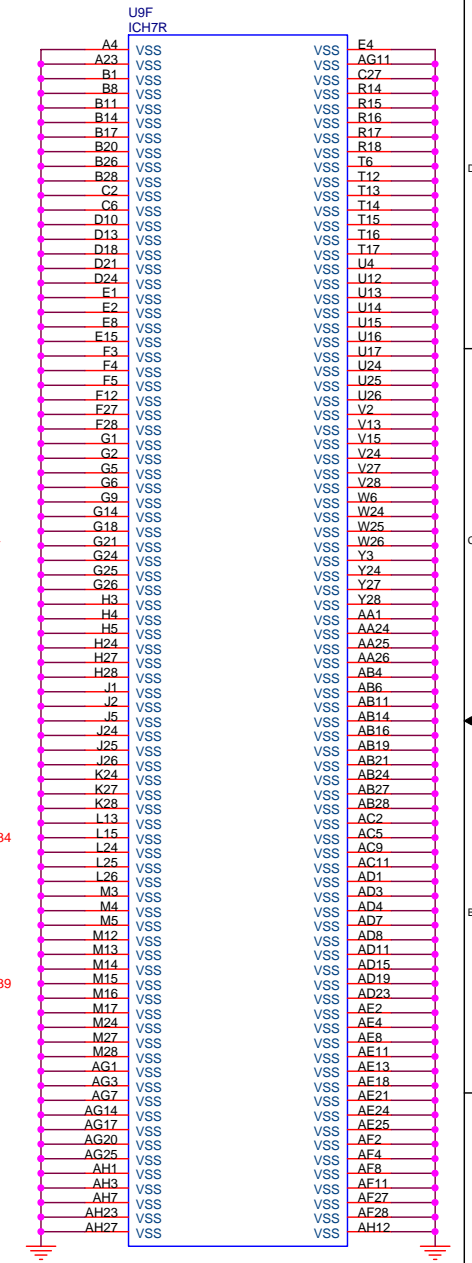
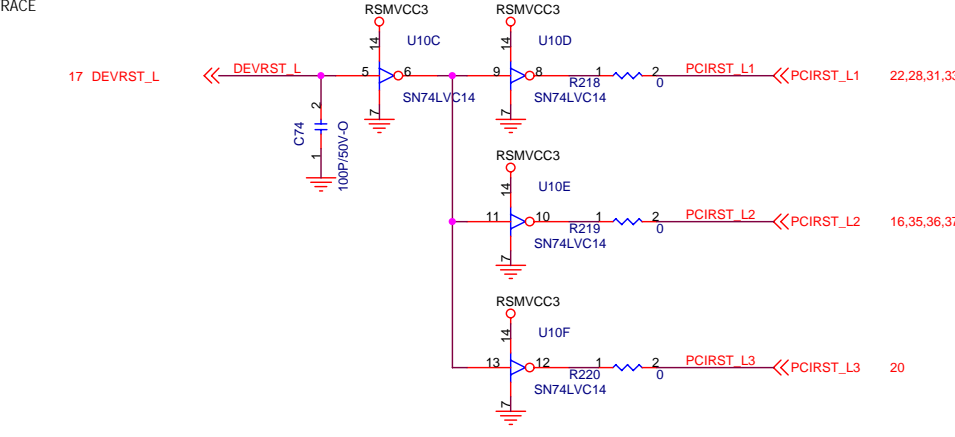
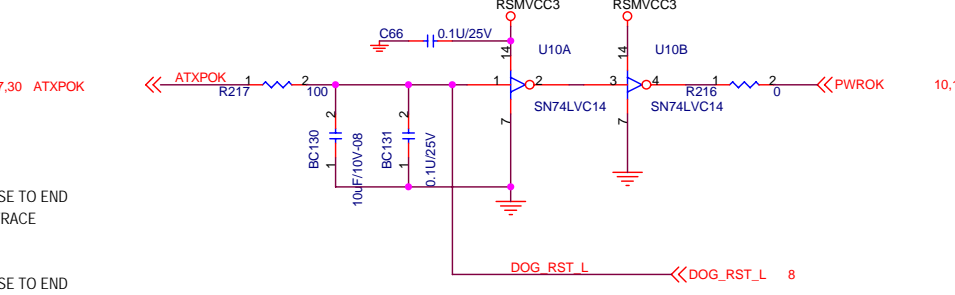
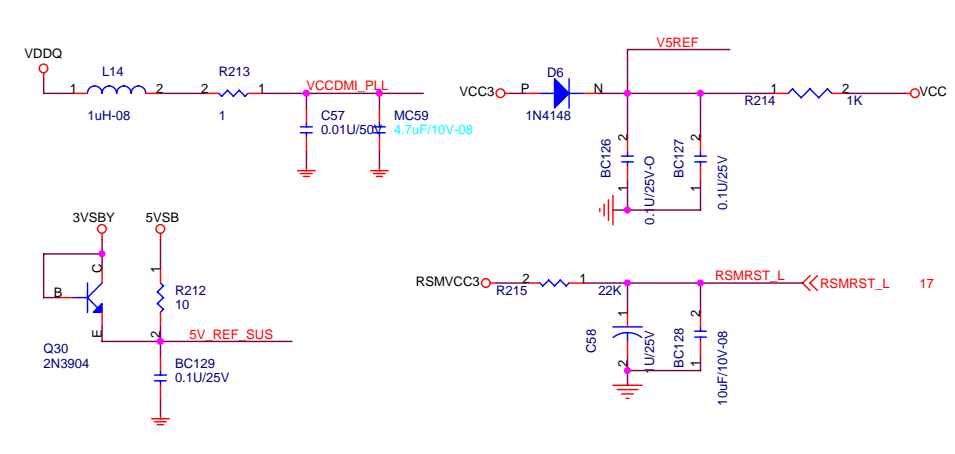
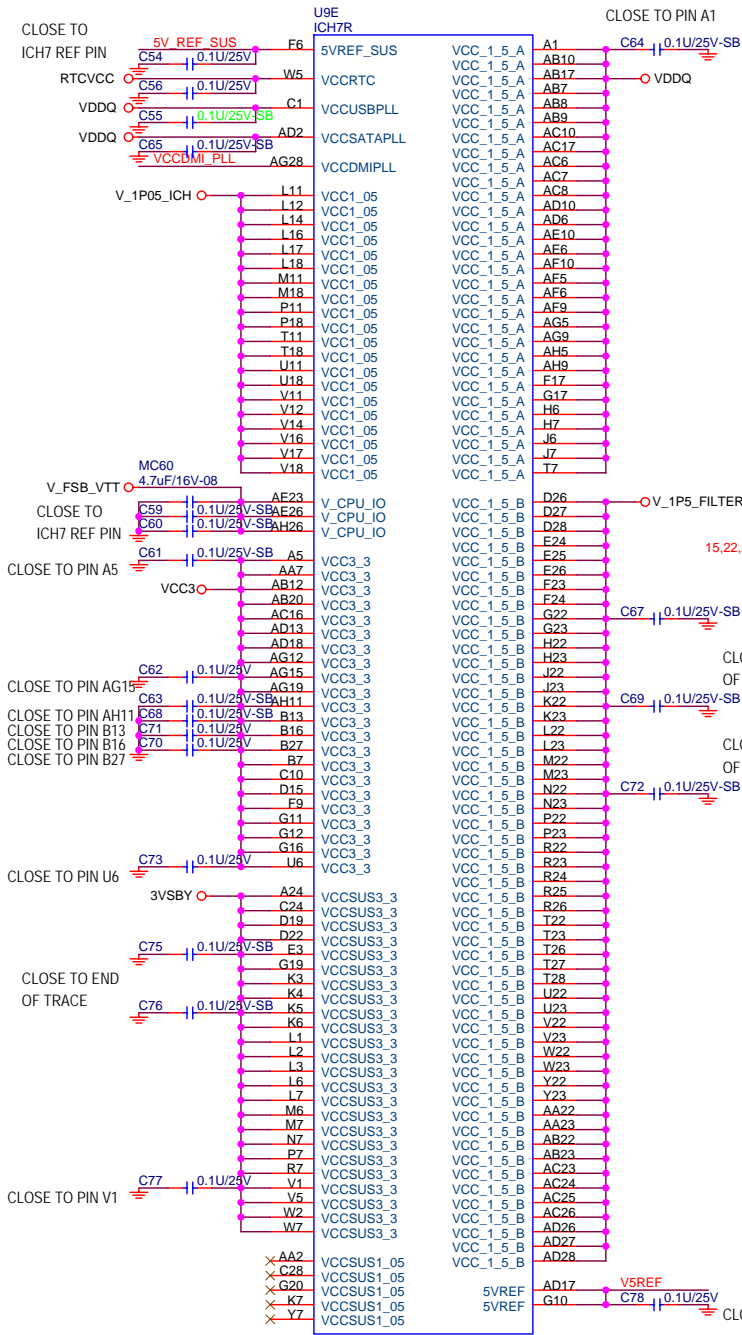



Must routing a trace to 22.6ohm pad, Don't direct connect with USBRBIAS_L. (two trace must < 500 mils)

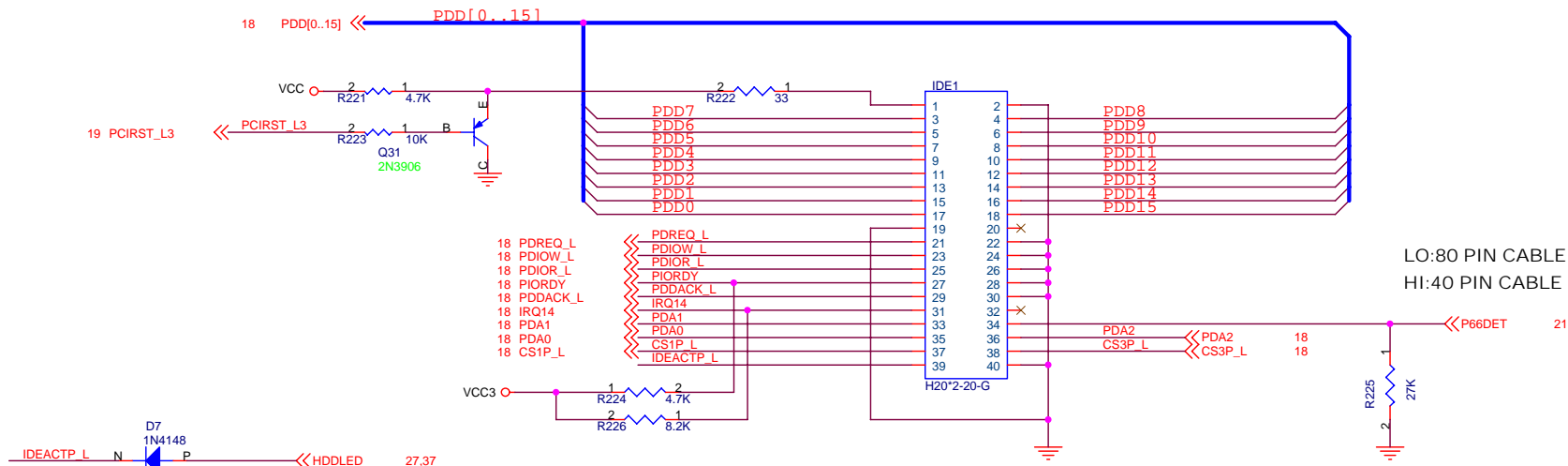


ICH6 V1.5 PCI Express powers, The LC filter is required to source 1A of current with less than 30mV of drop across the filter.



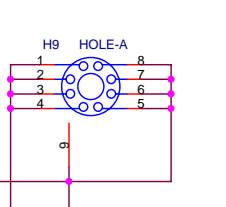
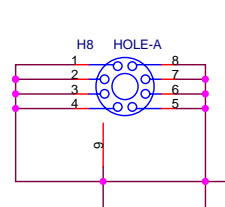
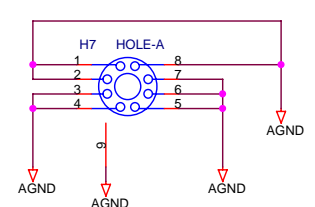
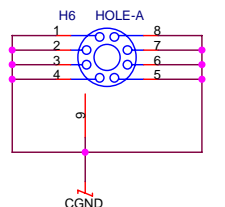
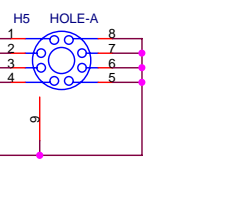
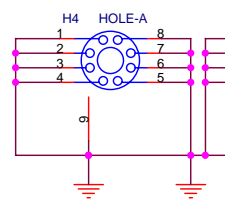
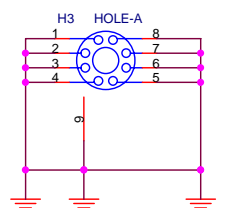
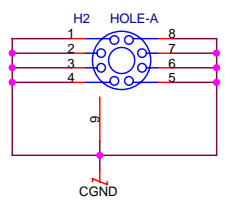
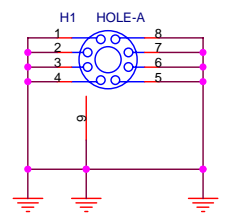


 Elitegroup Computer Systems		Title	
		ICH7 Part E & F	
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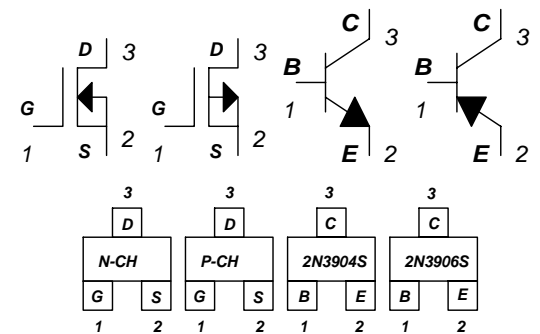


MAX TRACE LENGTH IS 8"

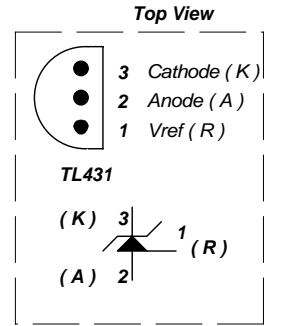
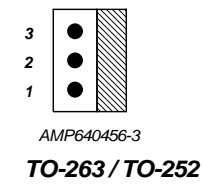
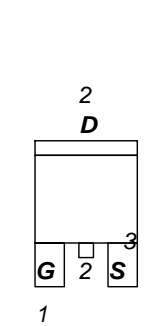
DATA LINES SHOULD BE MATCHED TO STROBES (XDIOR_L , XIORDY_L) WITHIN +/- 250 MIL,
STROBES SHOULD BE MATCHED TO THEIR COMPLEMENT WITHIN +/- 10MIL.



Top View SOT-23

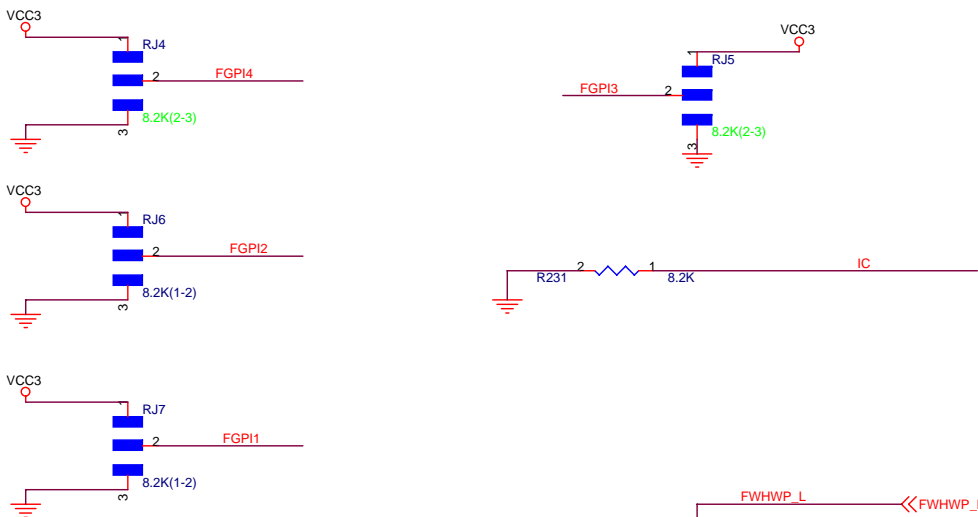
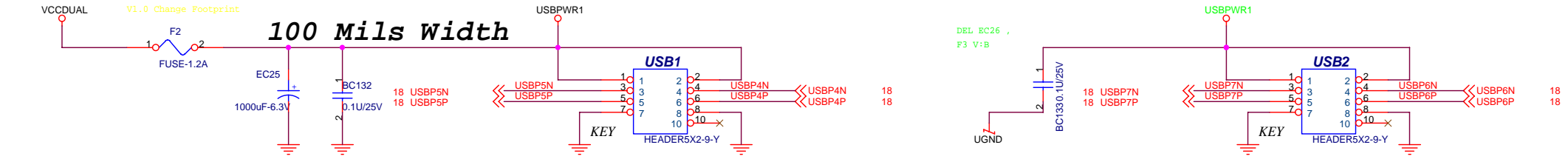


Fan Header



ECS Elitegroup Computer Systems		
IDE Connector		
Title		
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USB PORT INTERFACE



FGPI1:

High : SMART FAN Support
 Low: Not Support SMART Fan

FGPI2:

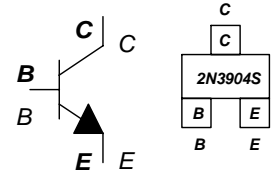
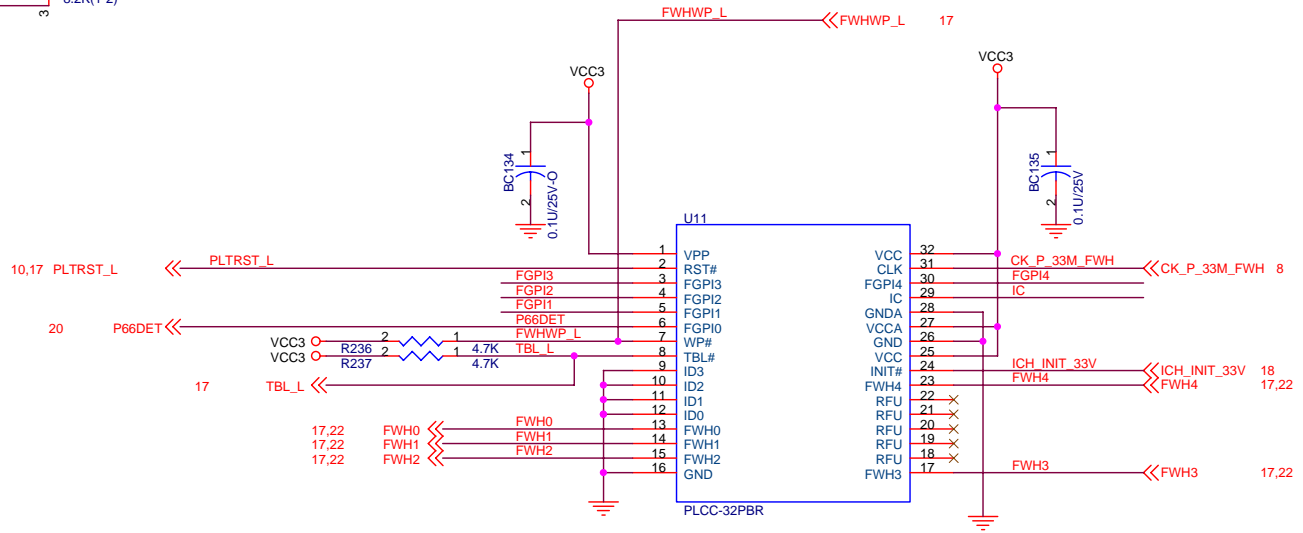
High: Deatect Adjust Voltage
 Low: Not Support ADJ voltage

FGPI3:

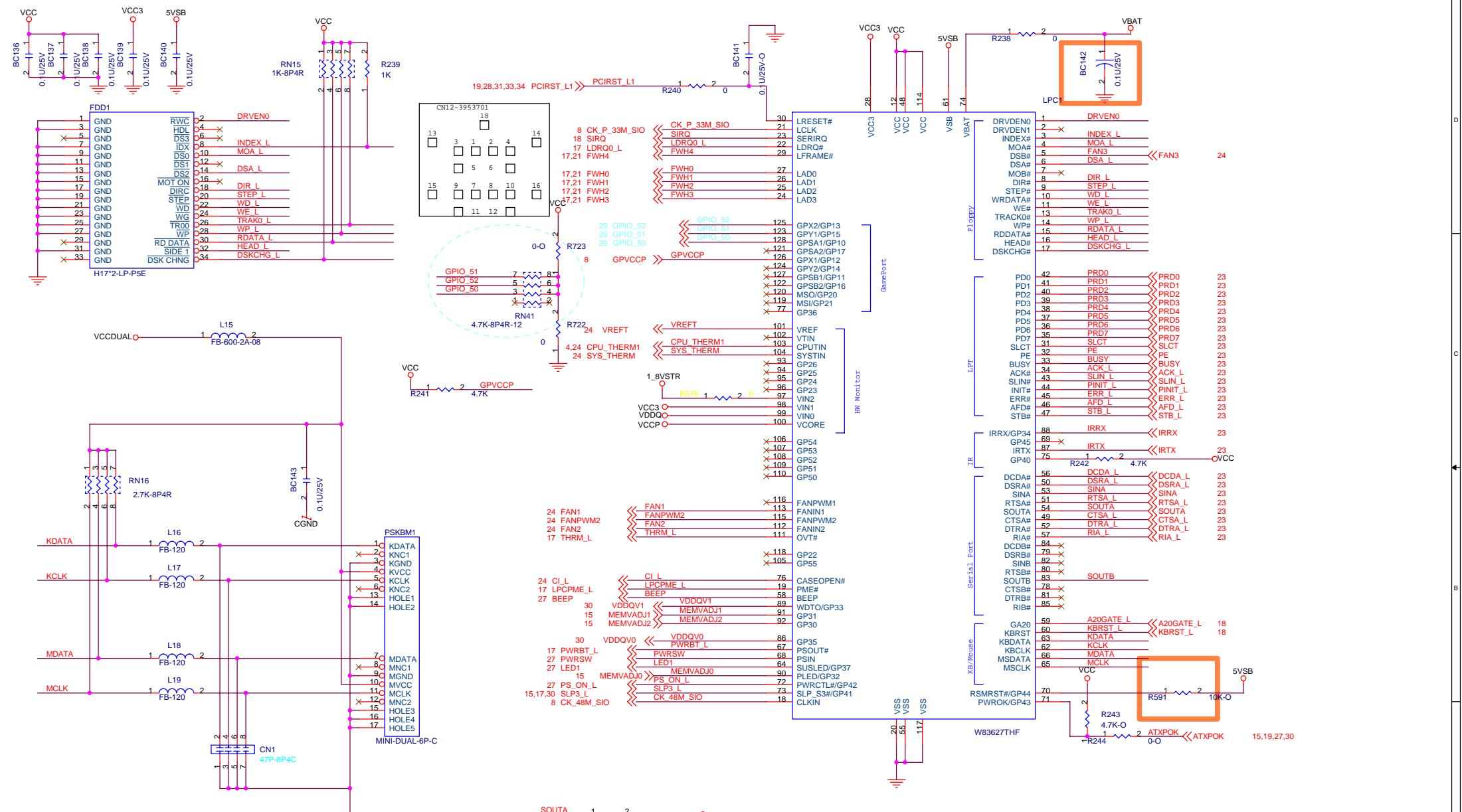
High : Not Support STR
 Low: STR Support

FGPI4:

High: Support COM2
 Low: Not Support COM2



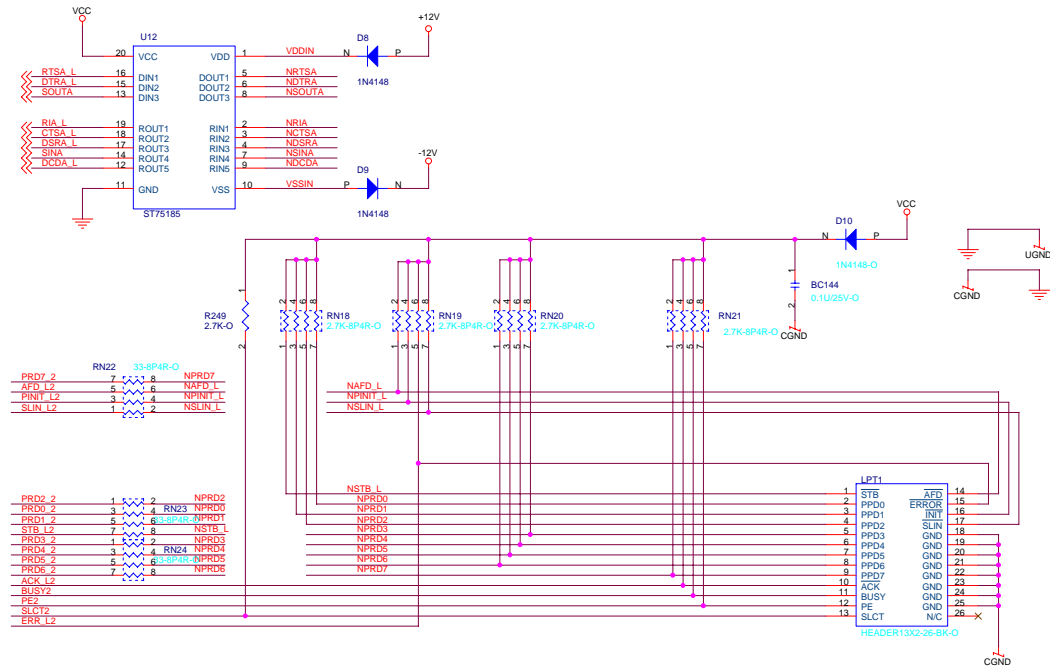
Elitegroup Computer Systems		
USB/FWH		
Size Custom	Document Number	Rev 3.0
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Title LPC_FDD/KB/M		
Size Custpm	Document Number 945P-A/945PL-A	Rev 3.0
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22 RTSA_L
22 DTRA_L
22 SOUTA

22 RIA_L
22 CTSA_L
22 DSRA_L
22 SINA
22 DCDA_L



PRD7_2
AFD_L2
PINIT_L2
SLIN_L2

PRD2_2
PRD3_2
PRD4_2
PRD5_2
PRD6_2
ACK_L2
BUSY2
SLCT2
ERR_L2

AFD_L1
PINIT_L1
SLIN_L1
PRD3_1

STB_L1
PRD0_1
PRD1_1
PRD2_1
PRD7_1
PRD4_1
PRD5_1

ERR_L1
ACK_L1
BUSY1
PE1
SLCT1

22 PRD2
22 PRD1
22 PRD0
22 SLIN_L

22 PRD6
22 PRD5
22 PRD4
22 PRD3

22 PRD7
22 ERR_L
22 AFD_L
22 STB_L

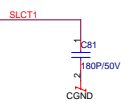
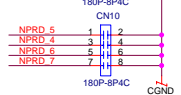
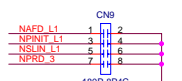
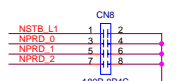
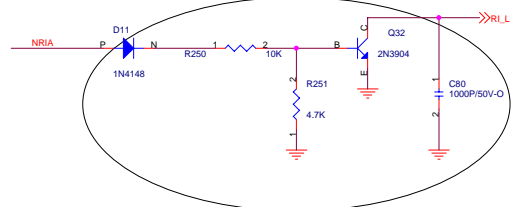
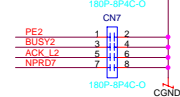
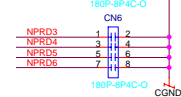
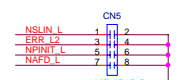
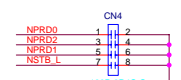
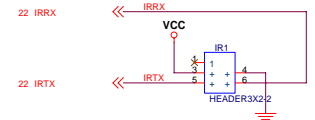
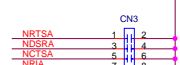
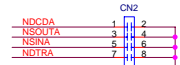
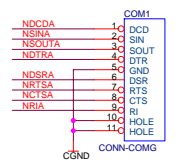
22 PE
22 BUSY
22 ACK_L
22 PRD7
22 SLCT

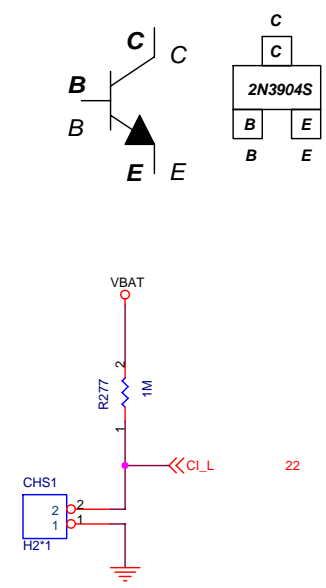
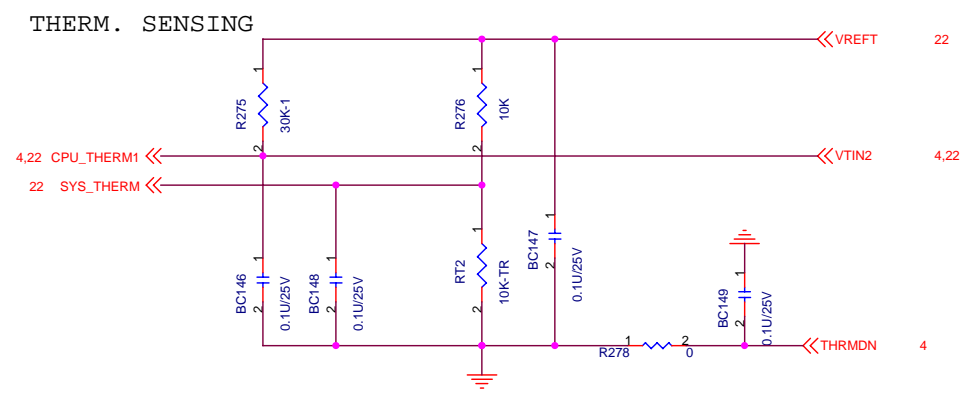
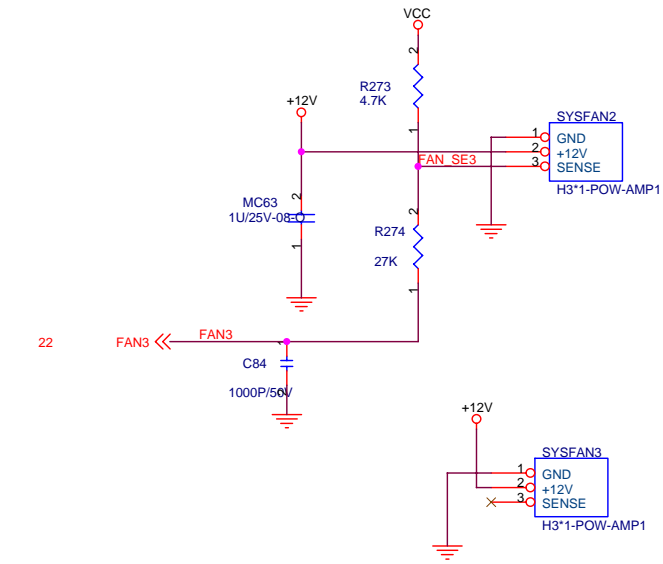
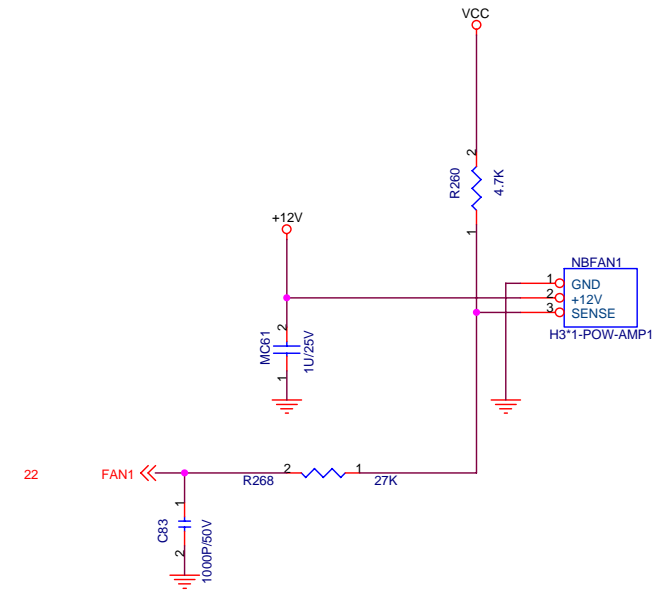
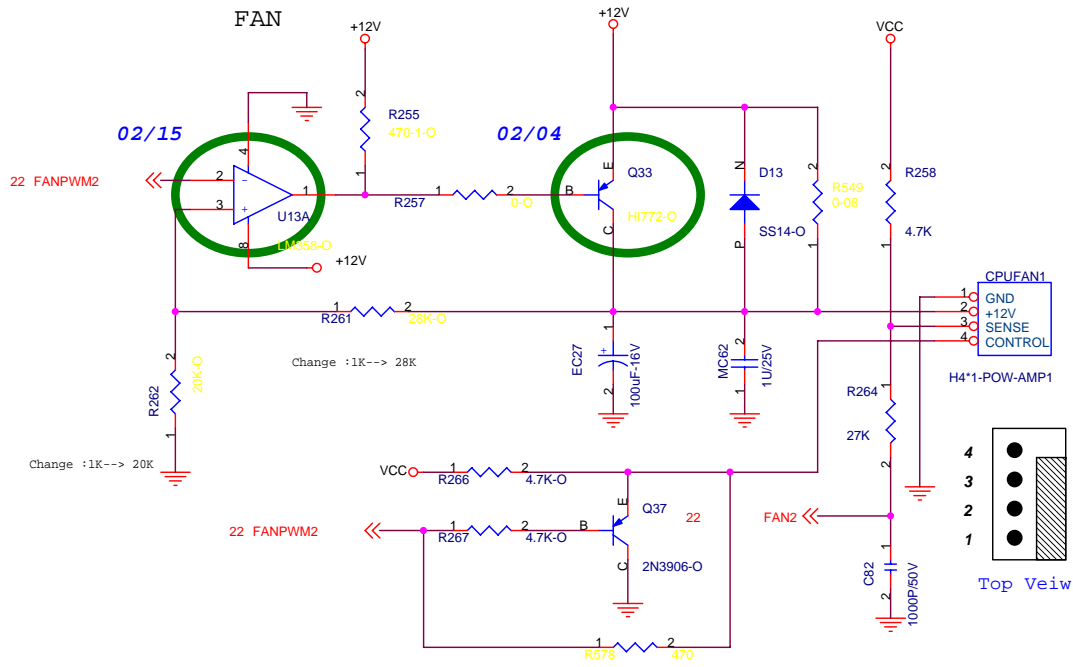
SLIN_L
PRD0
PRD1
PRD2

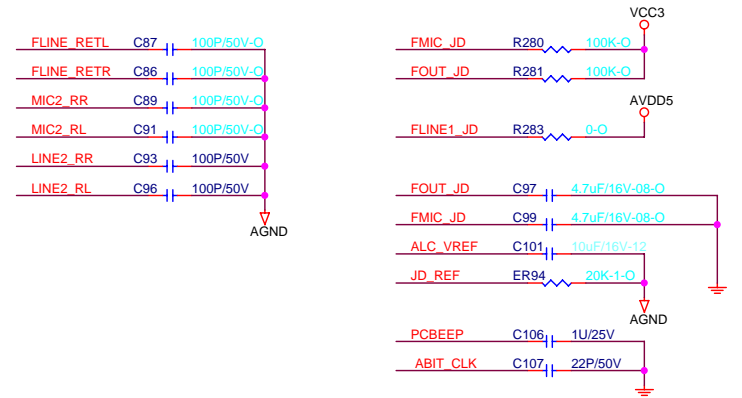
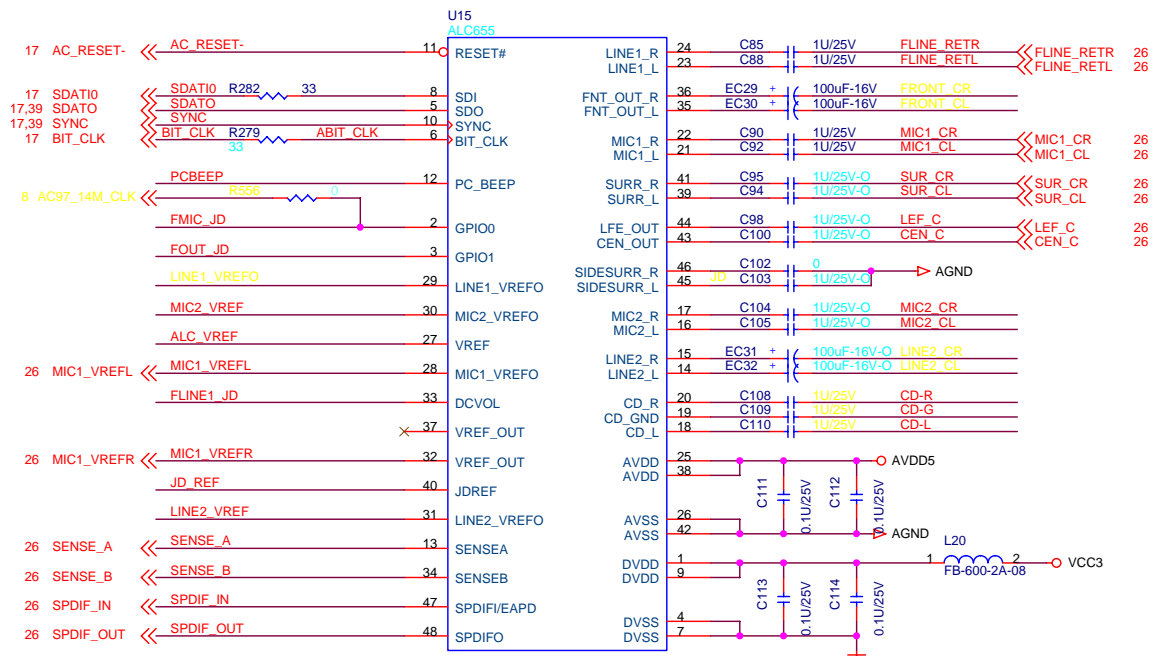
PRD3
PRD4
PRD5
PRD6
PRD7

STB_L
AFD_L
ERR_L
PINIT_L

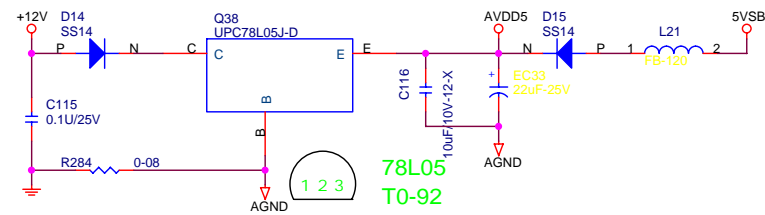
PRD7
ACK_L
BUSY
PE
SLCT



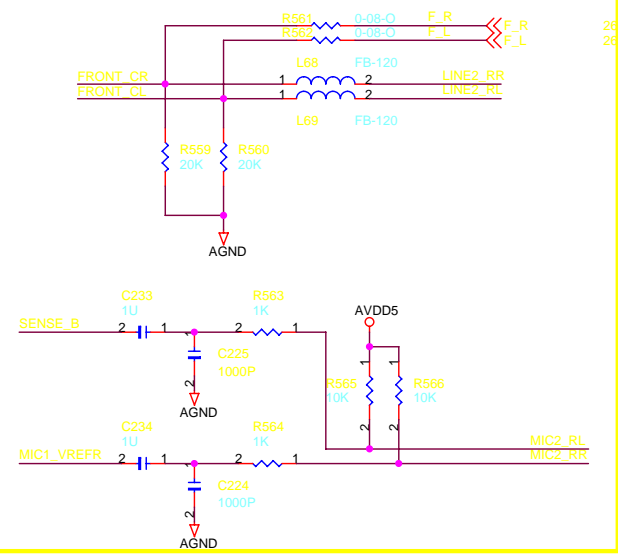
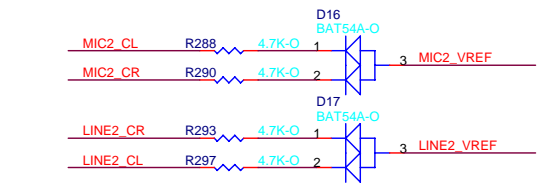
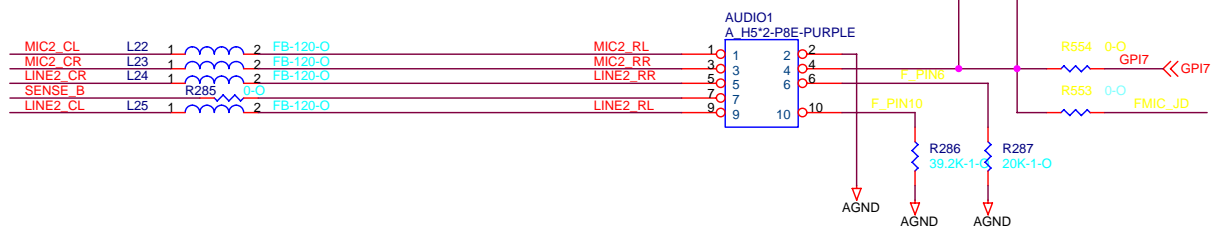




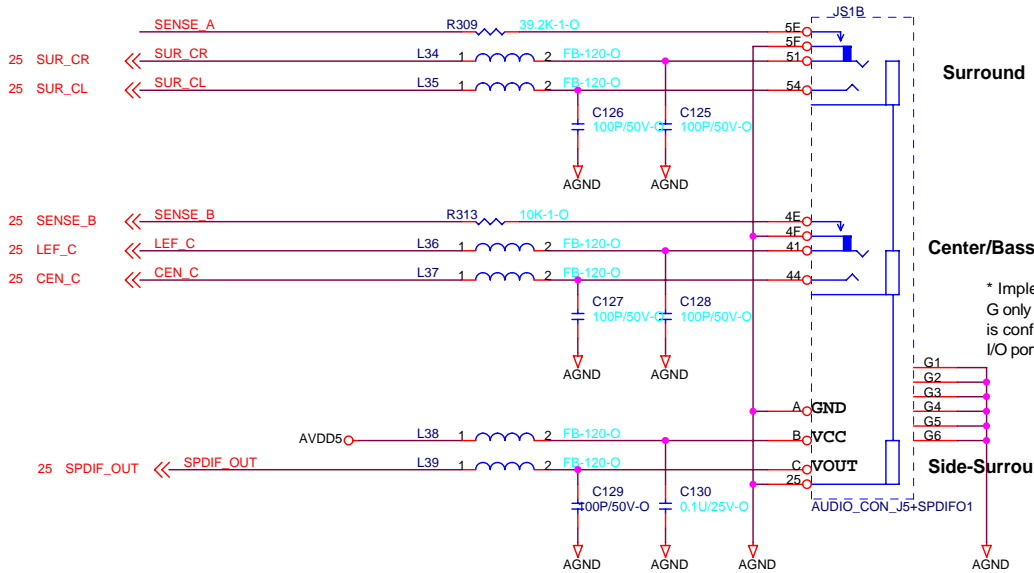
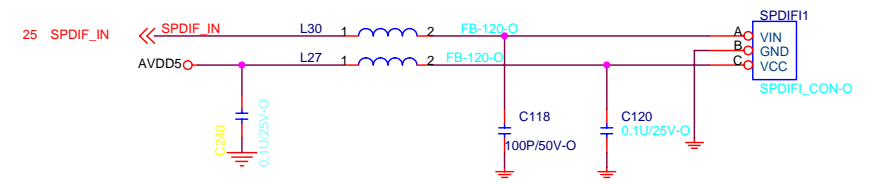
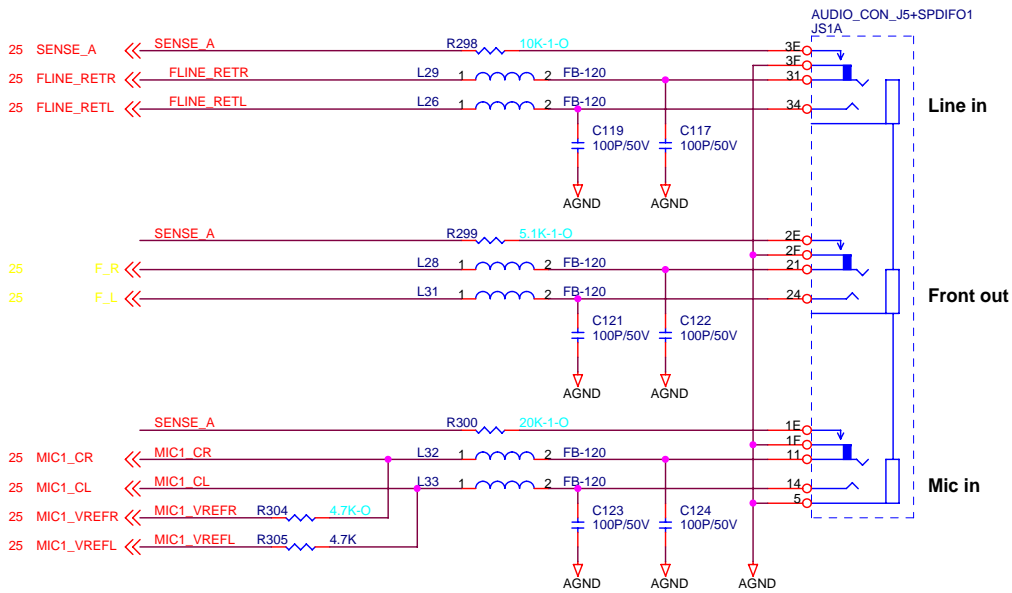
ADD ALC655 SCH



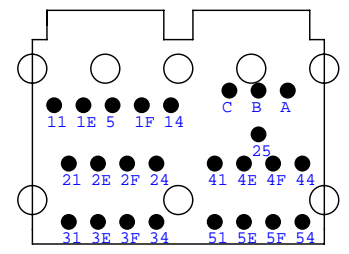
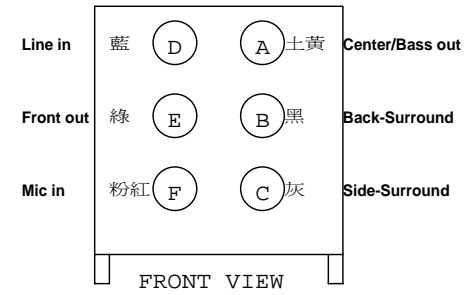
78L05
T0-92



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Audio Codec
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 Size: Custom Document Number: **945P-A/945PL-A** Rev: 3.0
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* Implement Block G only if PORT-G is configured as I/O port
 * Implement Block H only if PORT-H is configured as I/O port

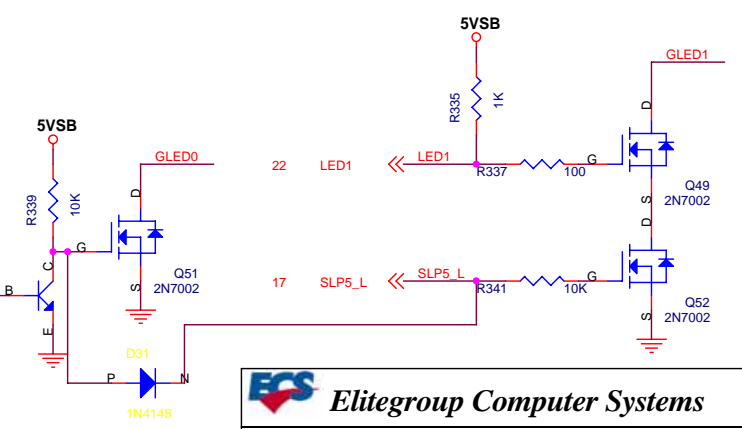
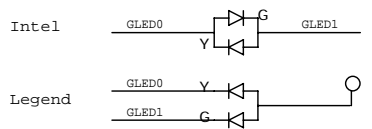
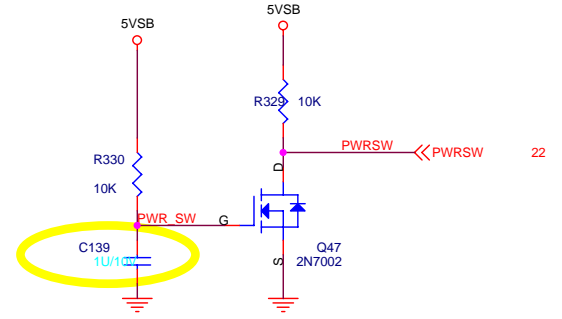
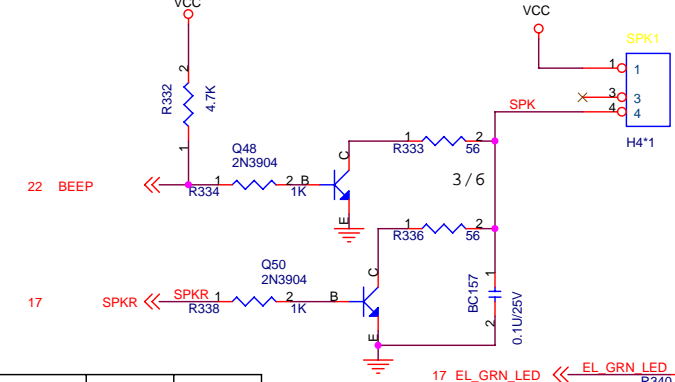
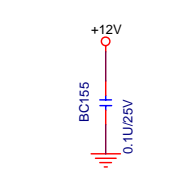
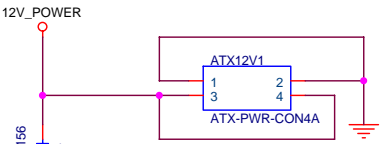
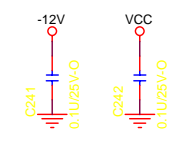
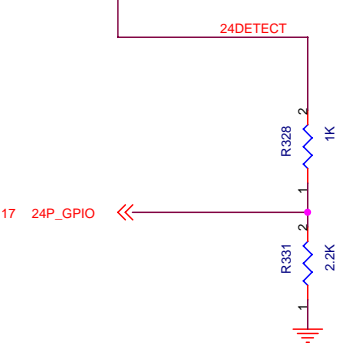
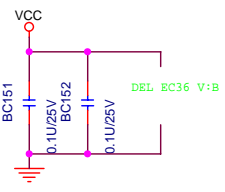
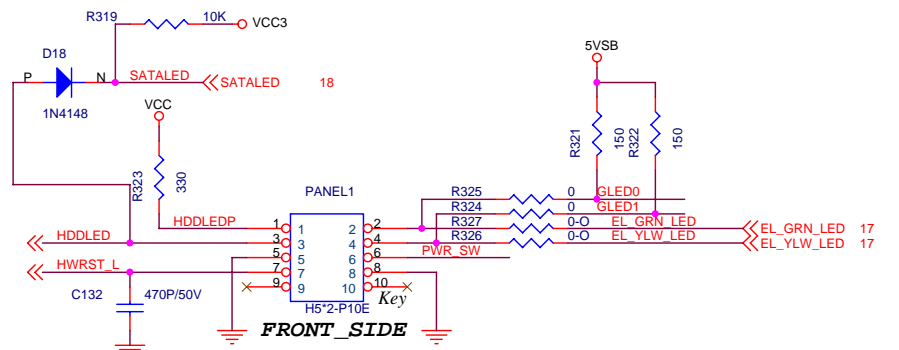
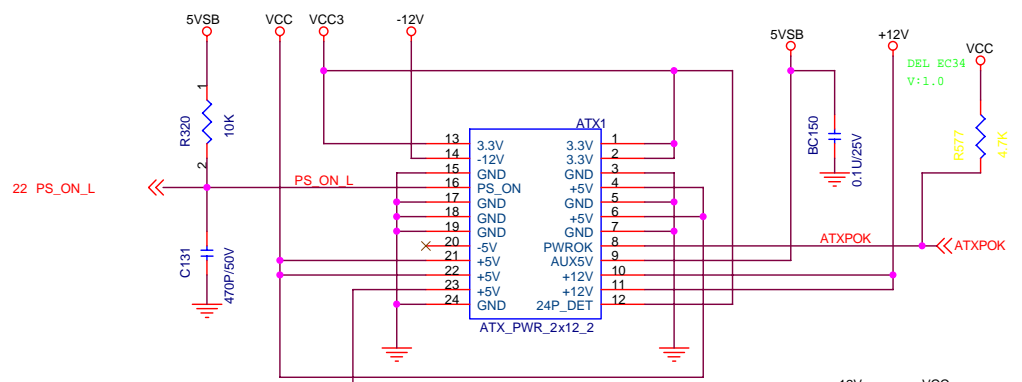


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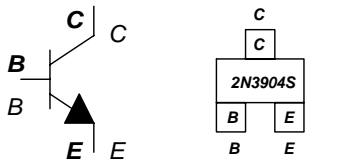
Title: **Audio Interface**

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	S0	S1	S3	S4,S5
PANEL1(4,2)	Green	G-blinking	Y-blinking	Dark
LPANEL1(3,5,7)	Green	G-blinking	G-blinking Yellow	Dark
LSJ1(1,2)	Dark	Dark	Light	Dark
SJ1(1,3)(2,3)	Light	Blinking	Blinking	Dark
GLED0	HIGH	HIGH	LOW	HIGH
GLED1	LOW	SWITCH	SWITCH	HIGH

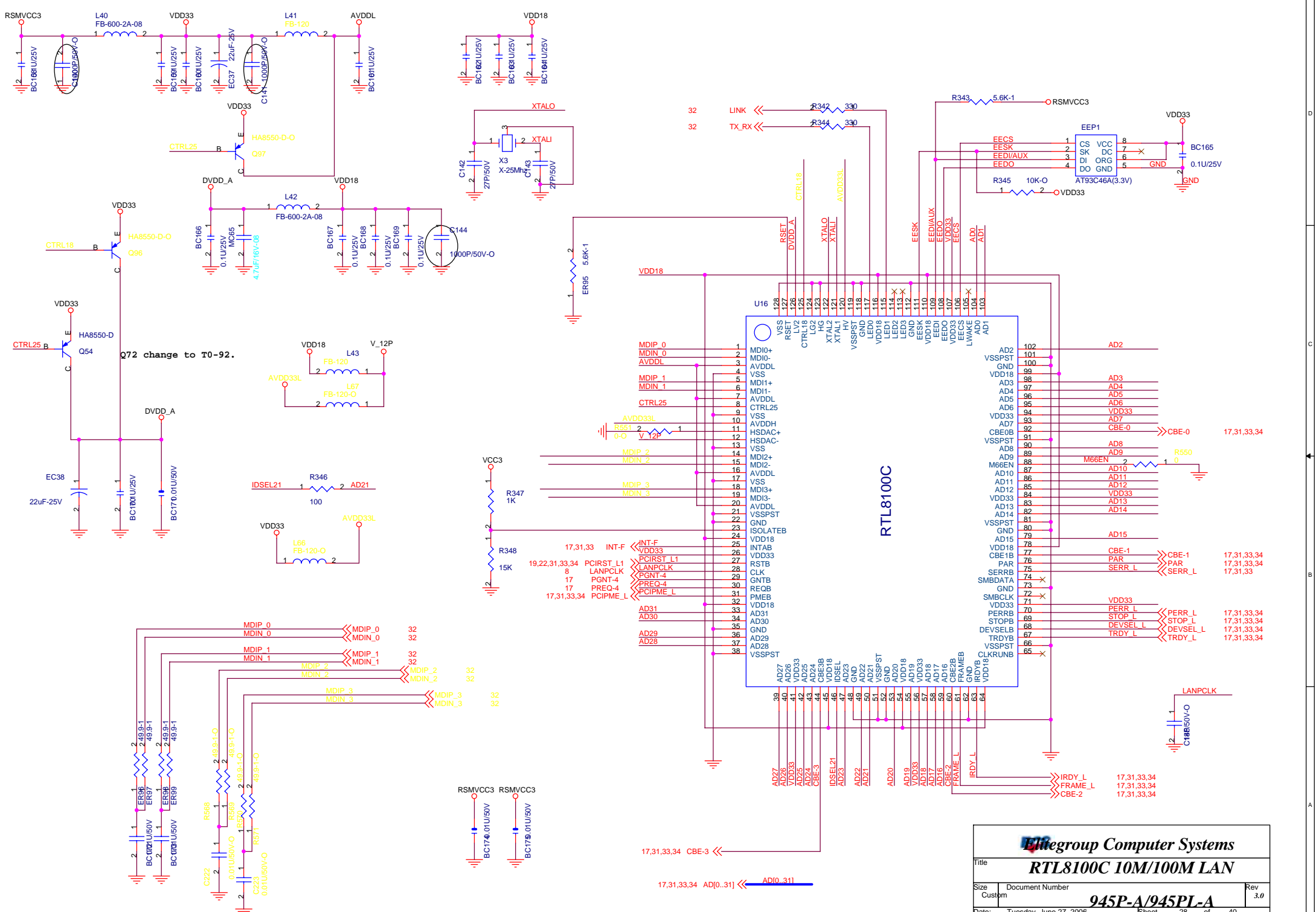


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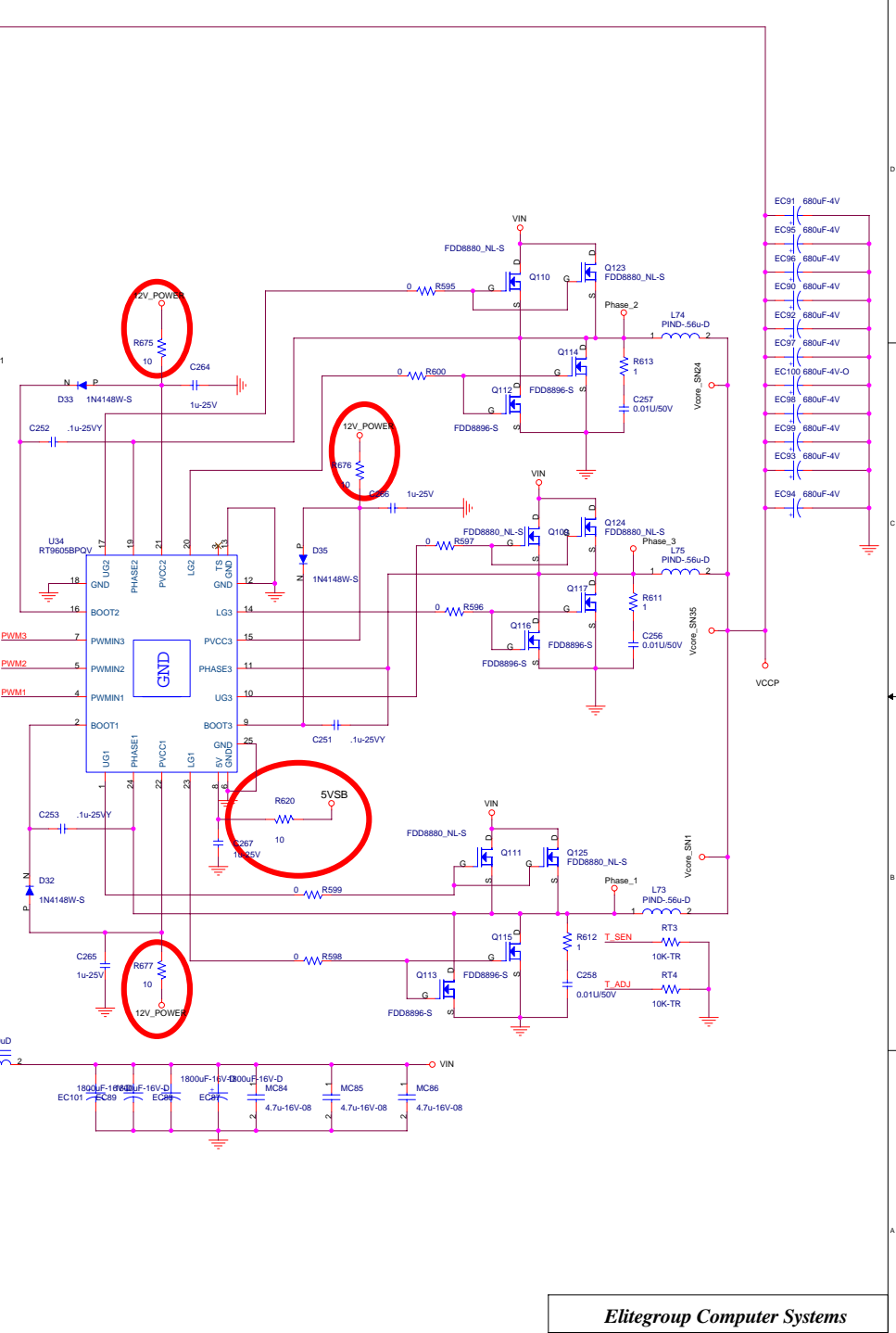
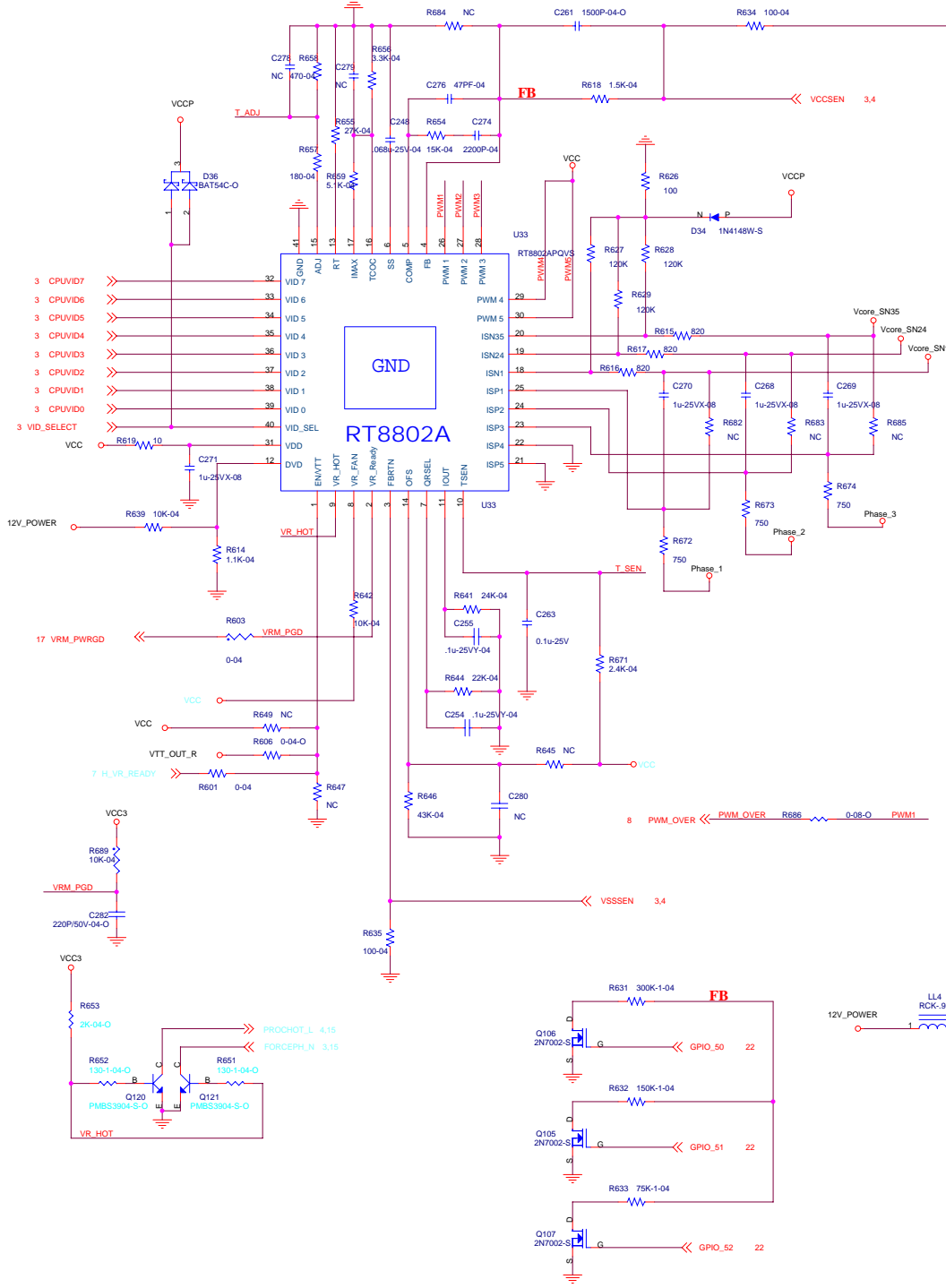
Title: **ATX Power & Front Panel**

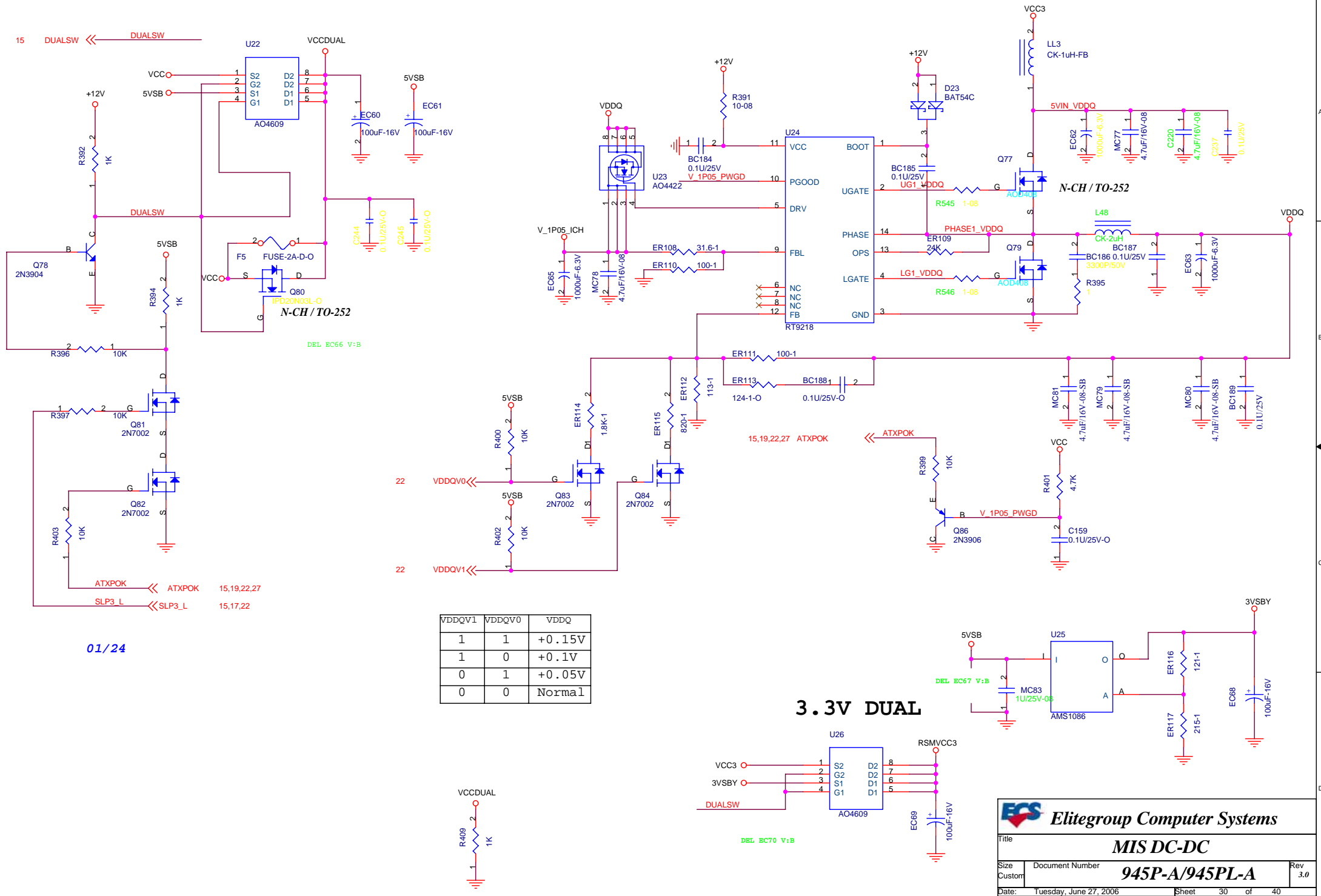
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RTL8100C 10M/100M LAN		
Title		
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DEB EC66 V:B

01/24

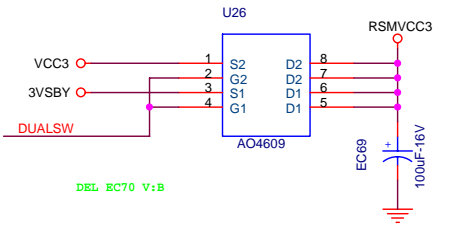
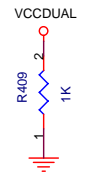
VDDQV1	VDDQV0	VDDQ
1	1	+0.15V
1	0	+0.1V
0	1	+0.05V
0	0	Normal

3.3V DUAL

ECS Elitegroup Computer Systems

Title: **MIS DC-DC**

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ATXP0K << ATXP0K 15,19,22,27
SLP3_L << SLP3_L 15,17,22

15,19,22,27 ATXP0K

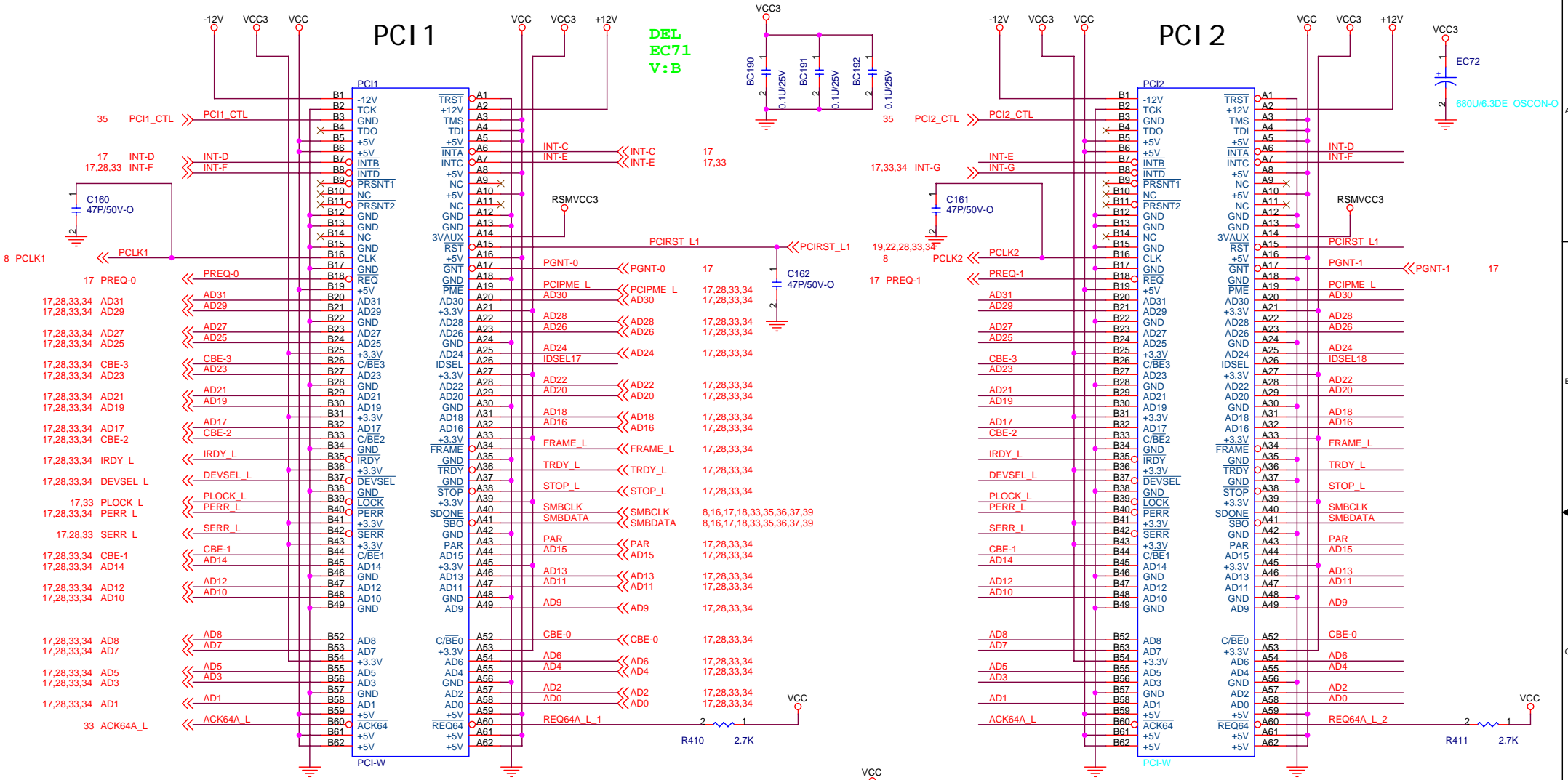
VDDQV0 << VDDQV0
VDDQV1 << VDDQV1

PCI 1

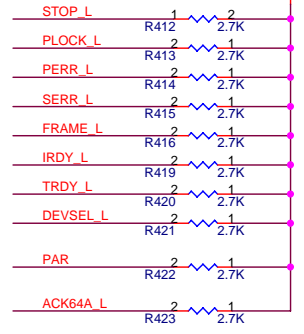
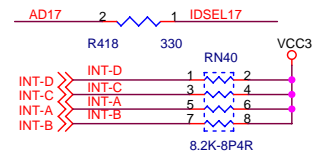
PCI 2

DEL
EC71
V:B

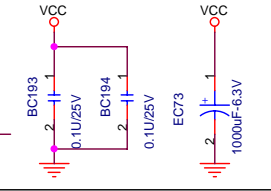
EC72



PCI1-INT : IDSEL=AD17
 INTA:INTC REQ=PREQ0#
 INTB:INTD GNT=PGNT0#
 INTC:INTE
 INTD:INTF



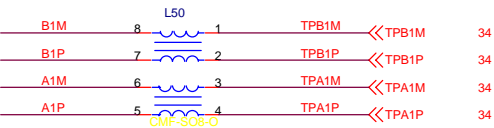
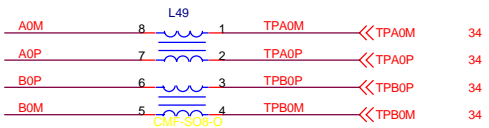
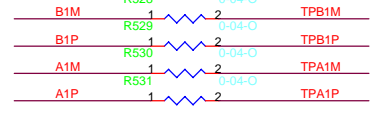
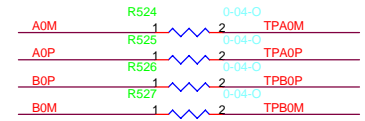
PCI2-INT : IDSEL=AD18
 INTA:INTD REQ=PREQ1#
 INTB:INTE GNT=PGNT1#
 INTC:INTF
 INTD:INTG



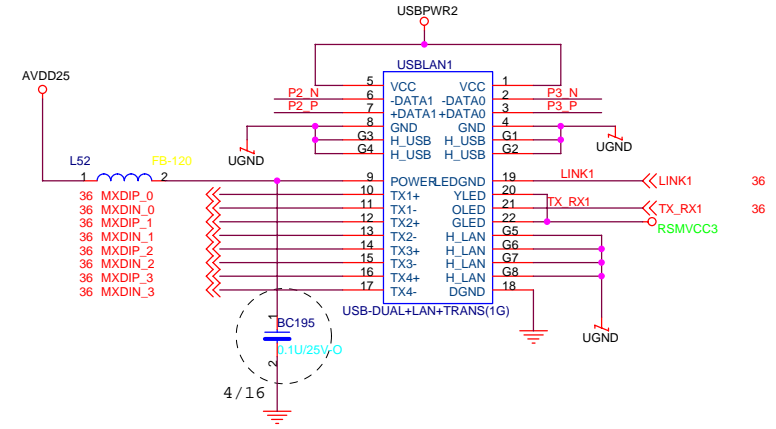
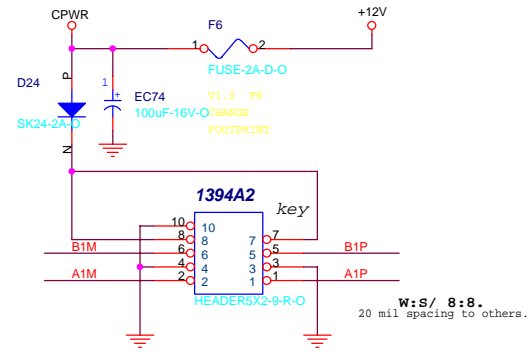
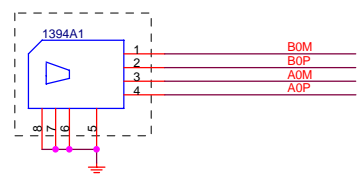
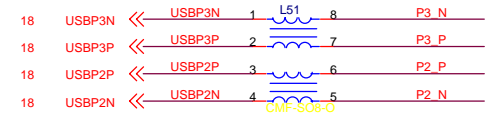
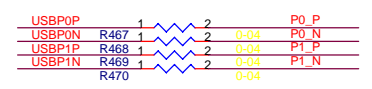
ECS Elitegroup Computer Systems

Title: **PCI Slot 1&2**

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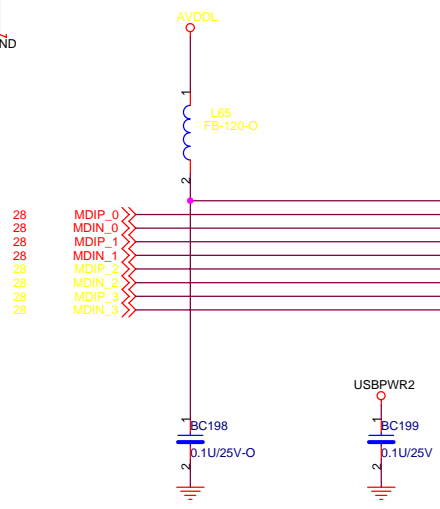
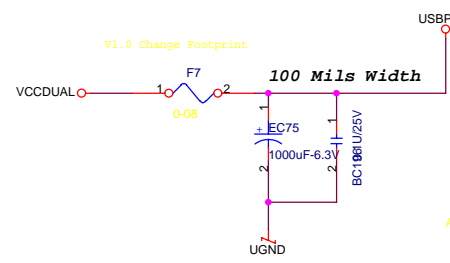
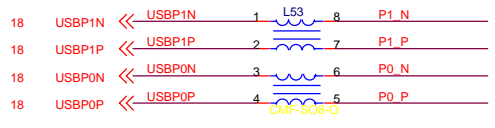
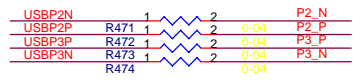


REAR_SIDE

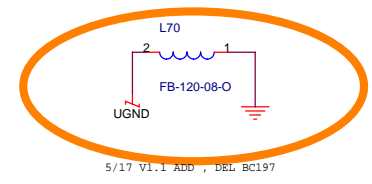


DEL RN42 V:B

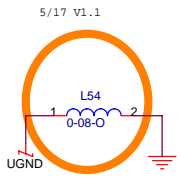
REAR_SIDE



W:S/ 8:8.
20 mil spacing to others.



5/17 V1.1 ADD, DEL BC197



5/17 V1.1

Elitegroup Computer Systems

Title: **Back I/O**

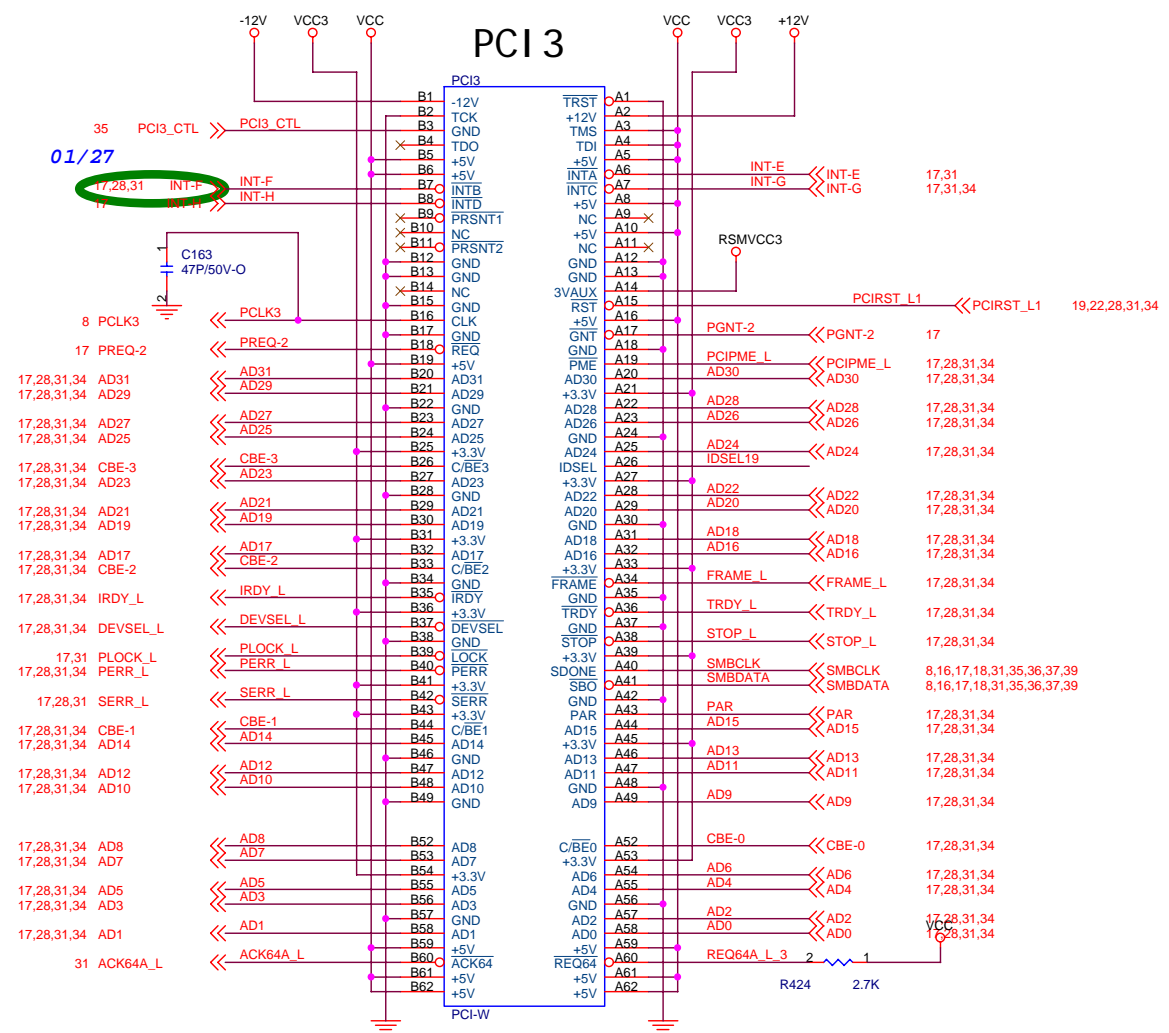
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Part Number: **945P-A/945PL-A**

Date: Tuesday, June 27, 2006

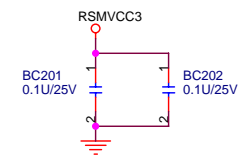
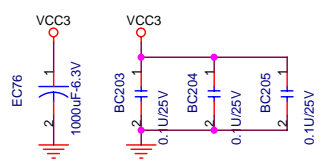
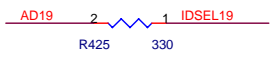
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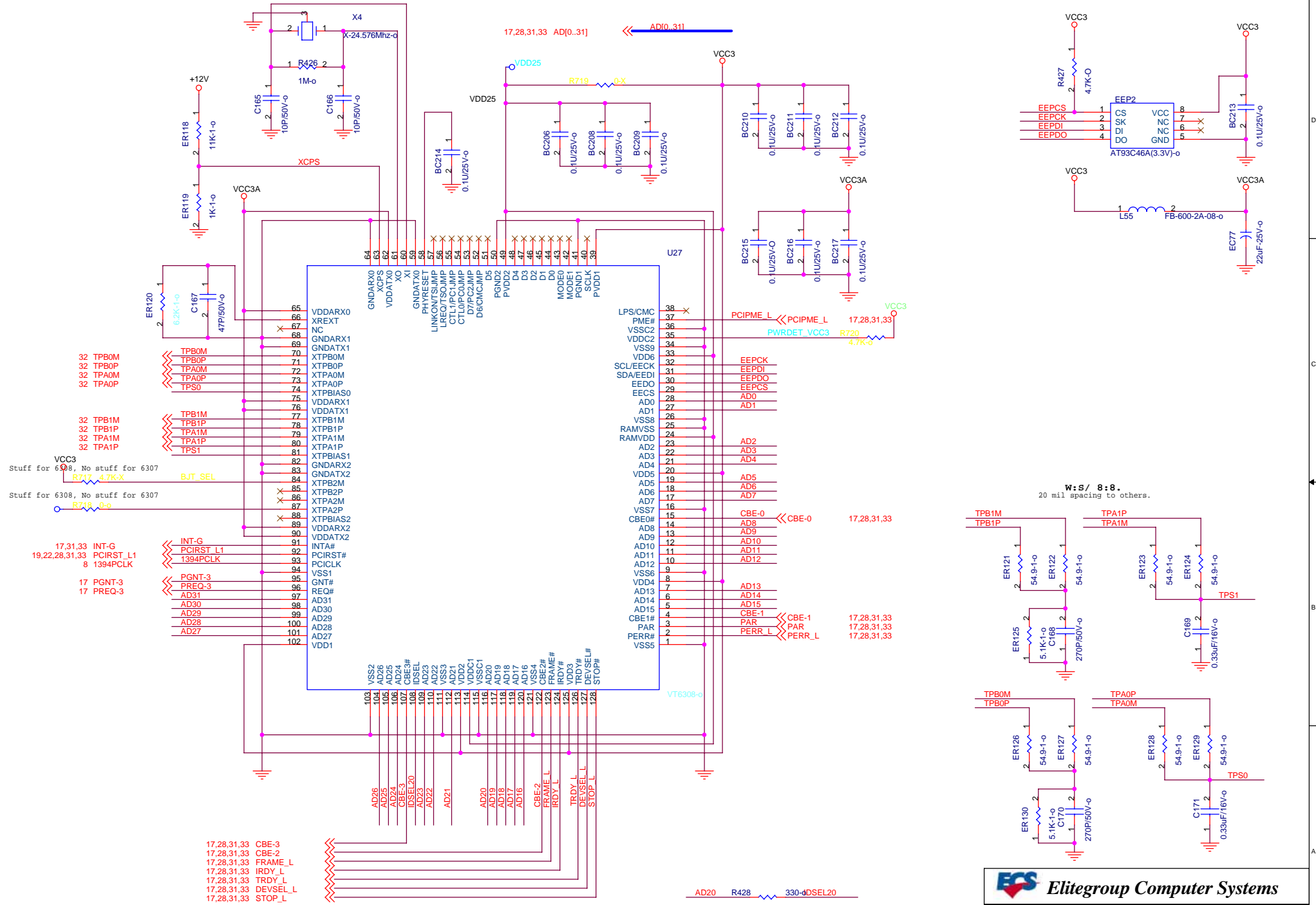


01/27

PCI3-INT: IDSEL=AD19
 INTA: INTE REQ=PREQ2#
 INTB: INTF GNT=PGNT2#
 INTC: INTG
 INTD: INTH



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Title PCI Slot 3		
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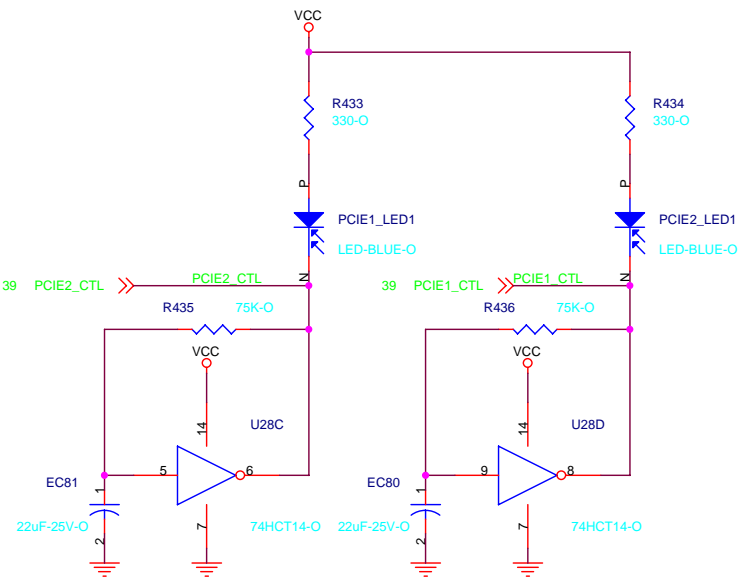
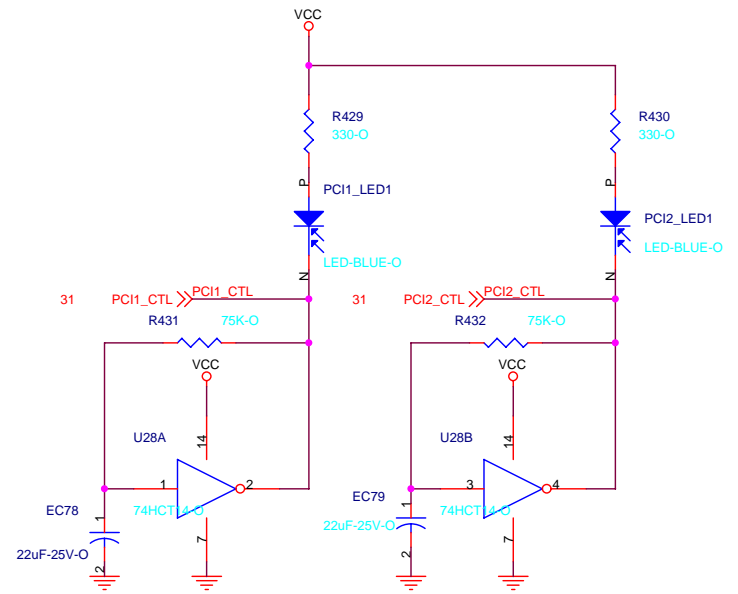
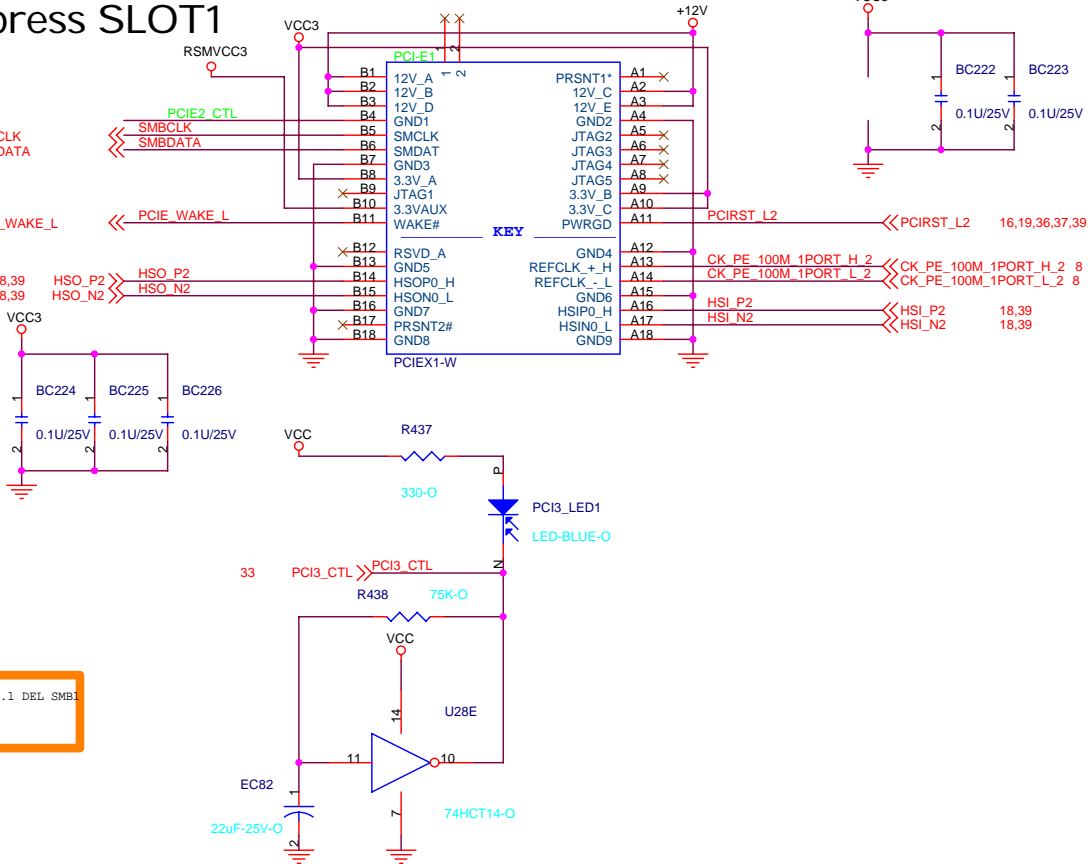
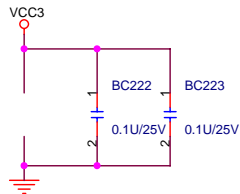
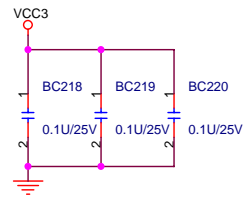
Title: **VT6308(1394)**

Size: Custom Document Number: **945P-A/945PL-A** Rev: 3.0

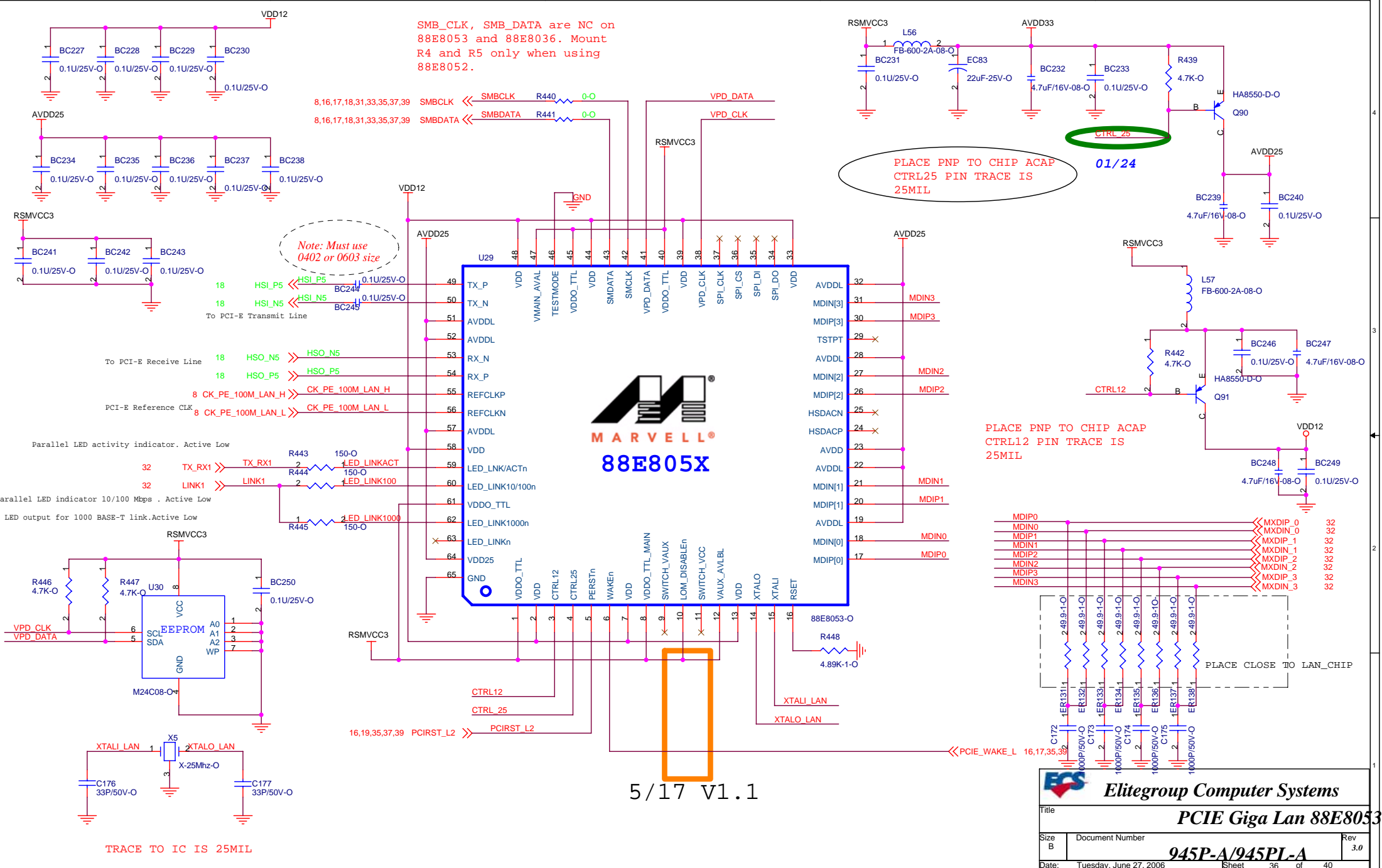
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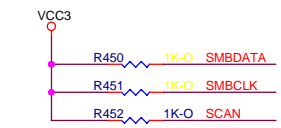
PCI Express SLOT1

DEL
PCI-E2
V:B

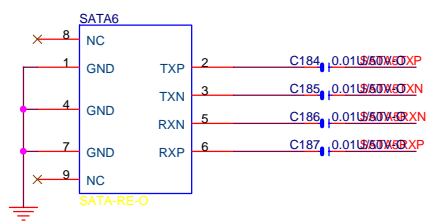
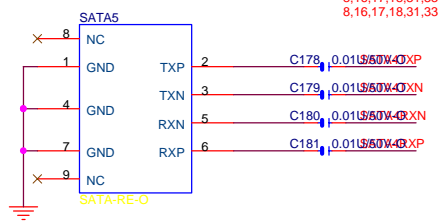


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Title		
PCIe X1		
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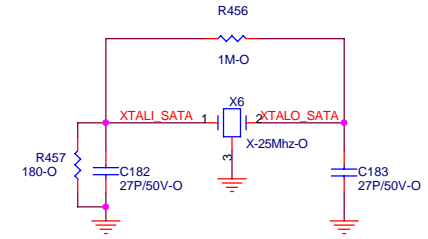
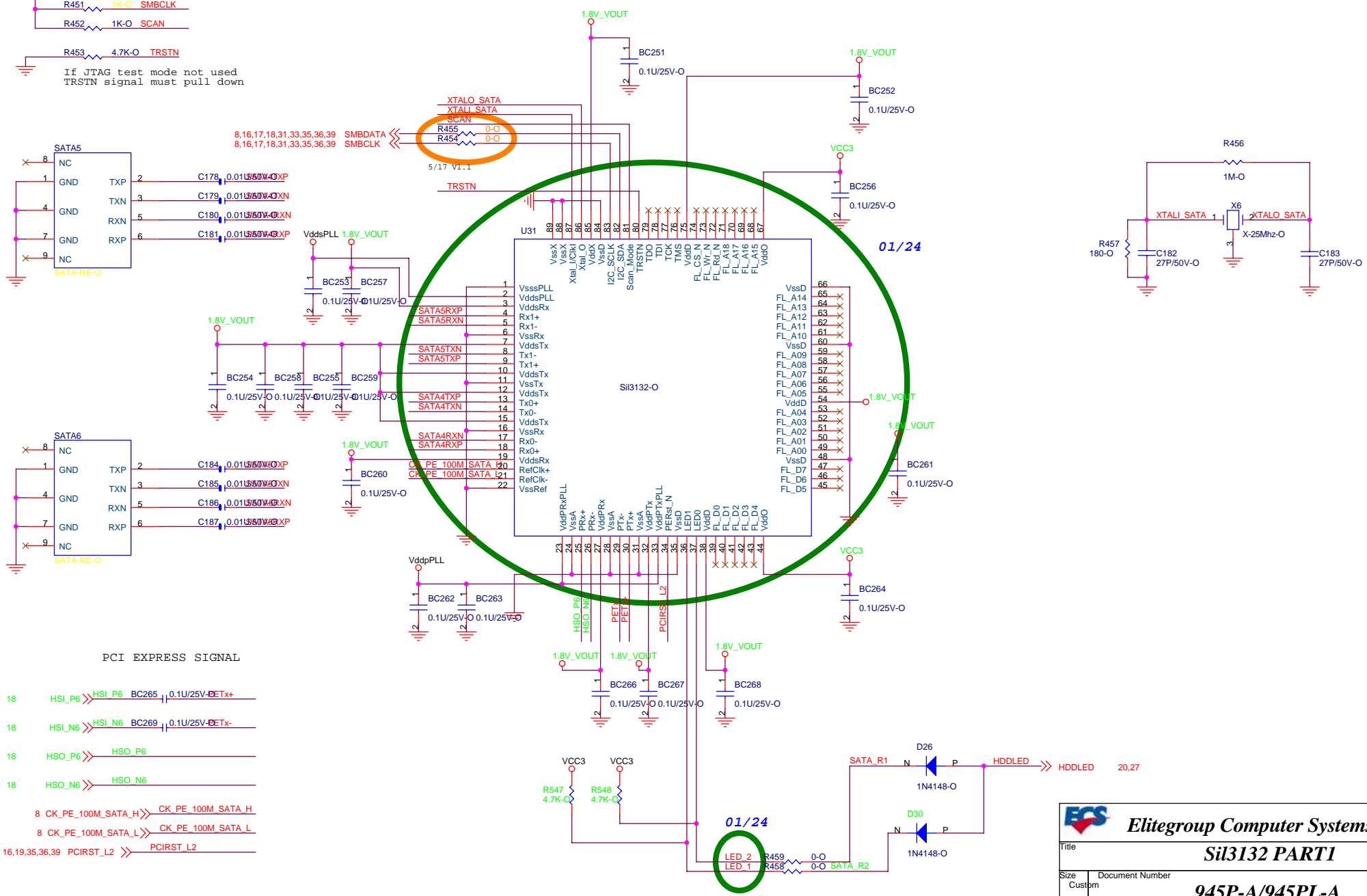


R453 4.7K-O TRSTN
If JTAG test mode not used TRSTN signal must pull down

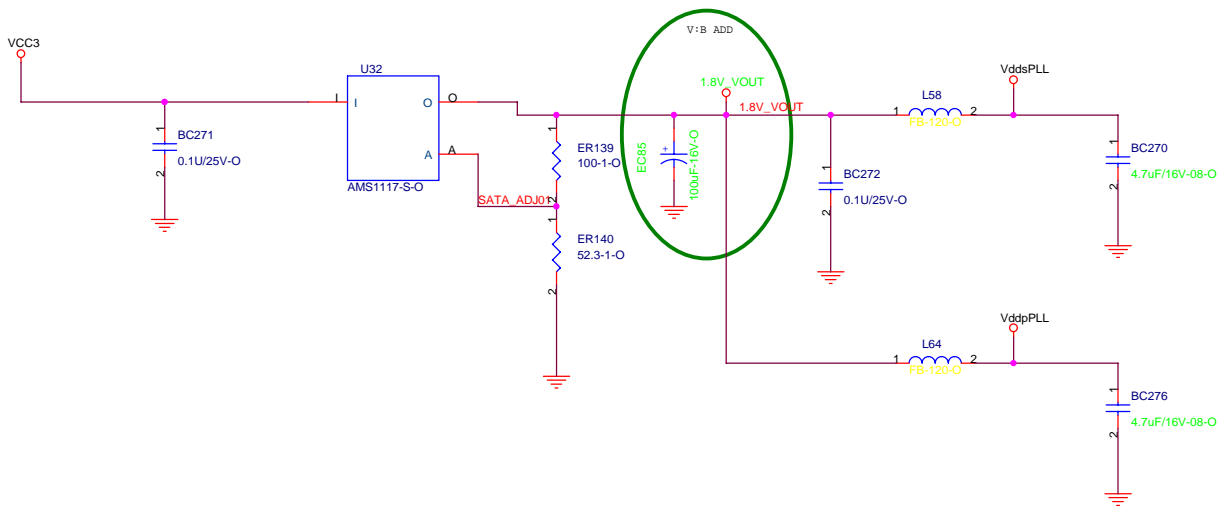



PCI EXPRESS SIGNAL

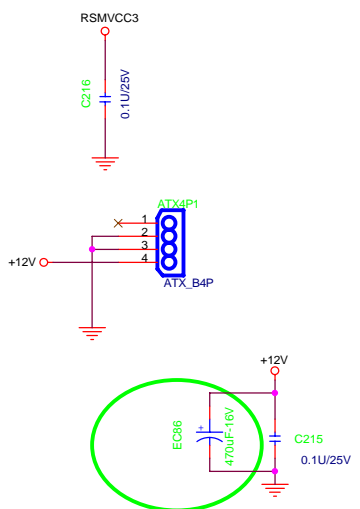
- 18 HSI_P6 >> HSI_P6 BC265 0.1U/25V-0-Tx+
- 18 HSI_N6 >> HSI_N6 BC269 0.1U/25V-0-Tx-
- 18 HSO_P6 >> HSO_P6
- 18 HSO_N6 >> HSO_N6
- 8 CK_PE_100M_SATA_H >> CK_PE_100M_SATA_H
- 8 CK_PE_100M_SATA_L >> CK_PE_100M_SATA_L
- 16,19,35,36,39 PCIRST_L2 >> PCIRST_L2



ECS Elitegroup Computer Systems		
Sil3132 PART1		
Title		
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Title		Sil3132 PART2
Size	Document Number	Rev
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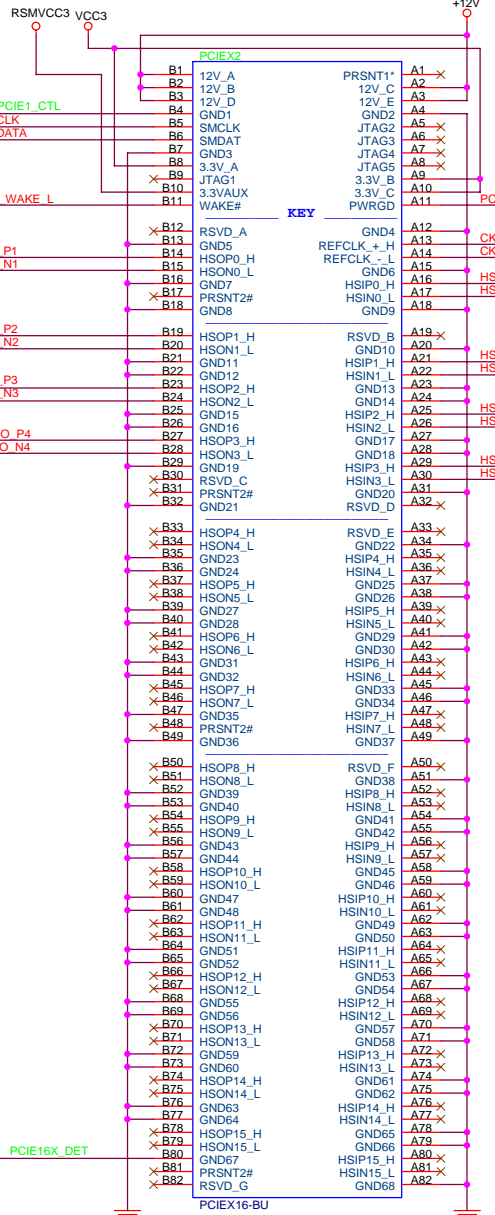
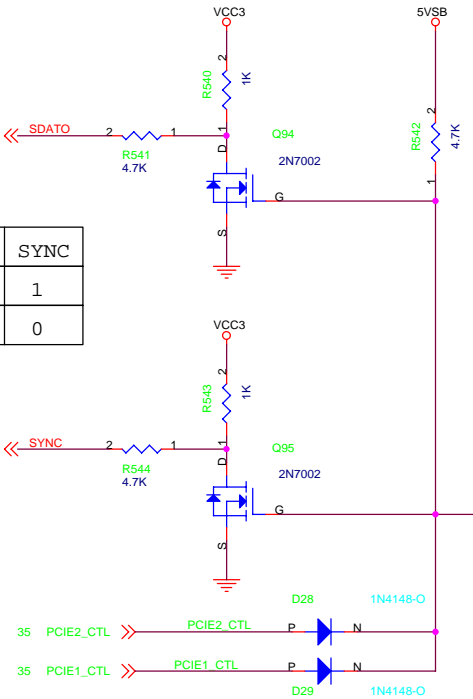
8,16,17,18,31,33,35,36,37 SMBCLK
8,16,17,18,31,33,35,36,37 SMBDATA

16,17,35,36 PCIE_WAKE_L

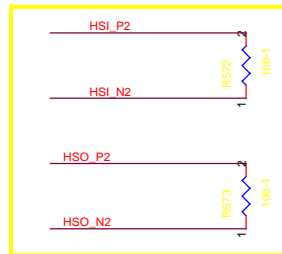
17,25 SDATO

17,25 SYNC

	SDATO	SYNC
4lane x1	1	1
1lane x4	0	0



R572, R573 near
PCIEX2 右側
(Trace 的最尾端)



Elitegroup Computer Systems

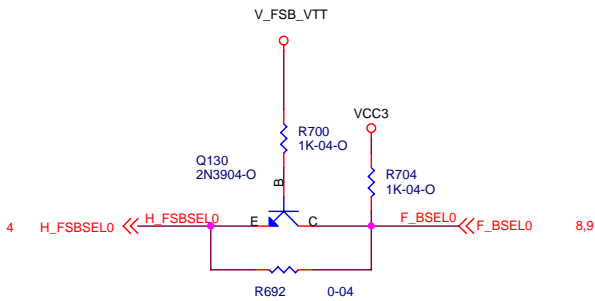
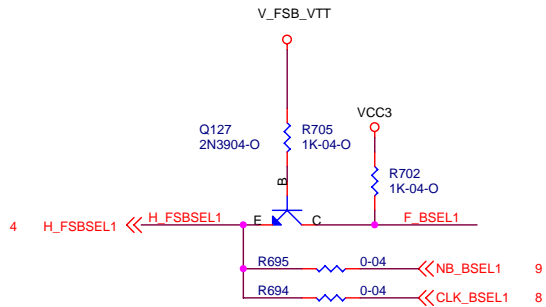
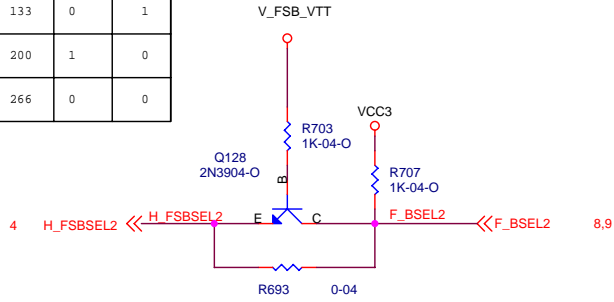
Title: **PCIEX2**

Size: Document Number
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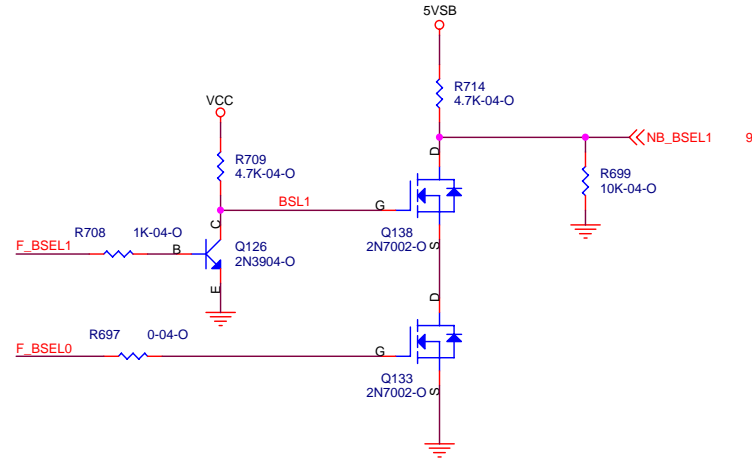
CPU FSB BSEL

CPU	BSEL1	BSEL0
133	0	1
200	1	0
266	0	0

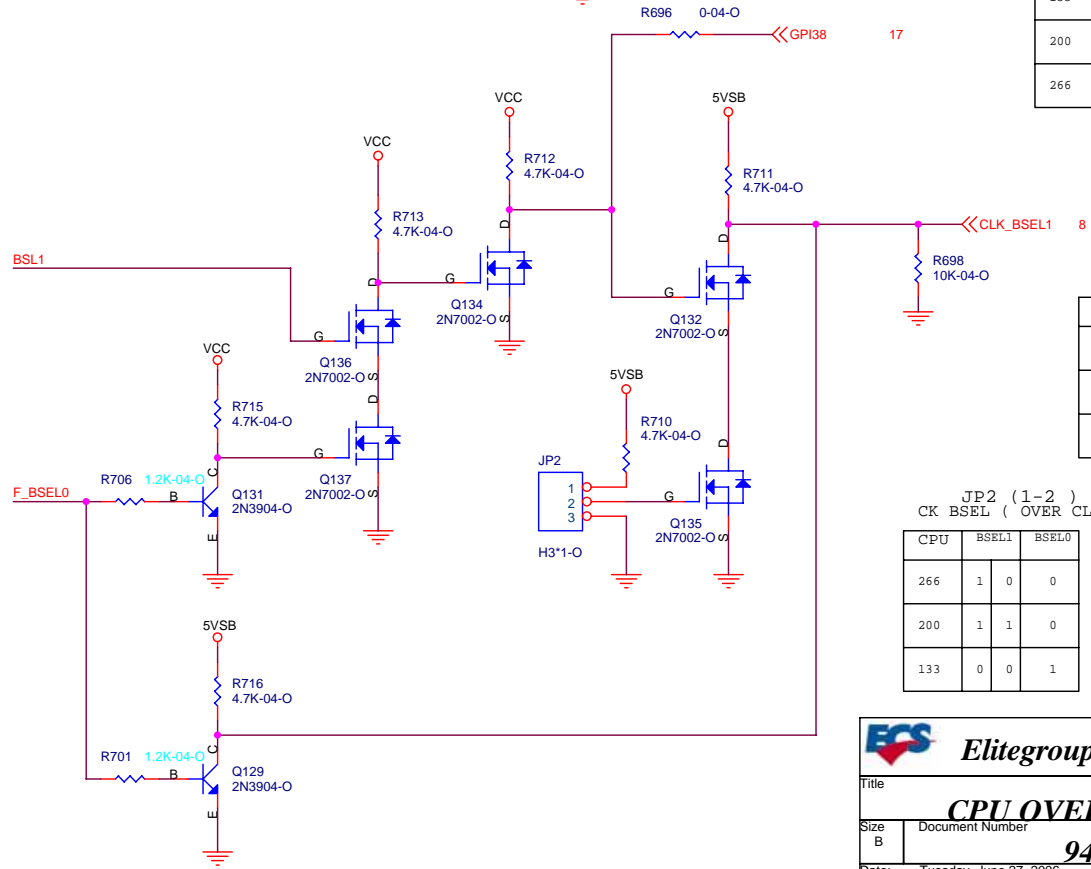


NB BSEL

CPU	BSEL1	BSEL0
133	0	1
200	1	0
266	1	0



CPU	GPI38
133	0
200	0
266	1



JP2

CPU	JP2 (1-2)	JP2 (2-3)
133	133 MHz	133 MHz
200	200 MHz	200 MHz
266	266 MHz	200 MHz

JP2 (1-2)
CK BSEL (OVER CLOCK)

CPU	BSEL1	BSEL0
266	1	0
200	1	1
133	0	0

JP2 (2-3)
CK BSEL (NORMAL)

CPU	BSEL1	BSEL0
266	1	1
200	1	1
133	0	0

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Title: **CPU OVER CLOCKING**
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