

DEVICE	IDSEL	INT#	REQ#	GNT#
PCI1	17	C/D/E/F	PREQ-0	PGNT-0
PCI2	18	D/E/F/G	PREQ-1	PGNT-1
PCI3	19	E/F/G/H	PREQ-2	PGNT-2
1394	20	G	PREQ-3	PGNT-3
LAN	21	F	PREQ-4	PGNT-4

**INTEL
P4 Processor
PSC, Smithfield -
LGA 775 pin**

BW : 6.4GB/s @ FSB : 800MHz & Freq : 200MHz
 BW : 6.4GB/s @ FSB : 1066MHz & Freq : 266MHz

BW : 10.7GB/s @ DDR2 : 533/667/800 MHz

PCIE 16X

**INTEL
BroadWater
1202pin FC-BGA**

DDIMM1: DDR2 Socket 240P
DDIMM2: DDR2 Socket 240P
DDIMM3: DDR2 Socket 240P
DDIMM4: DDR2 Socket 240P

BW : 2GB/s (Support Lsoch)

USB1
2 ports

USB2
2 ports

USB3
2 ports

USB V2.0

**INTEL
ICH8
652pin EBGA**

PCIE 4X

PCIEx1

PCIEx1

**JMicrom
JMB363**

**IDE
CONNECTOR**

**SATA
CONNECTOR**

**SATA
CONNECTOR**

Line in

Line out

Mic in

Center/Bass out

Surround

SPDIFO

**Audio Codec
ALC885
/861**

Azalia I/F

SPI ROM #2

SPI ROM #1

LPC bus

**Intel
82566 Lan PHY**

**USBLAN
RJ45**

SATA1 7Pin

SATA2 7pin

SATA3 7Pin

SATA4 7pin

SATA5 7Pin

SATA6 7pin

BW : 150MB/s

**intel
FWH
32pin PLCC**

**Super I/O
8712F
128pin PQFP**

VIA VT6308

PINHEADER

PINHEADER

RTL8110SC

**USBLAN
RJ45**

PCI1 Slot 120pin @ AD17

PCI2 Slot 120pin @ AD18

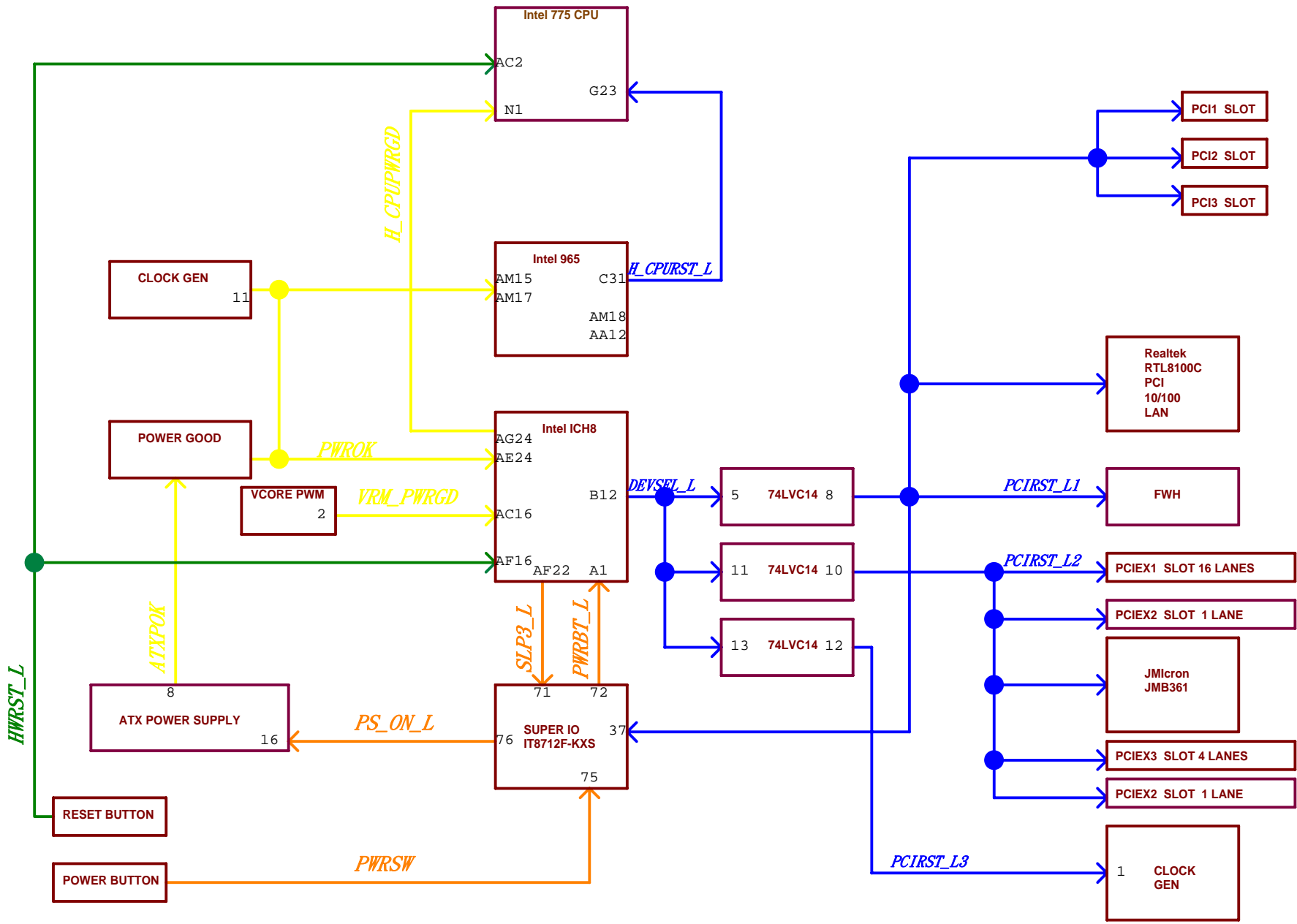
PCI3 Slot 120pin @ AD19

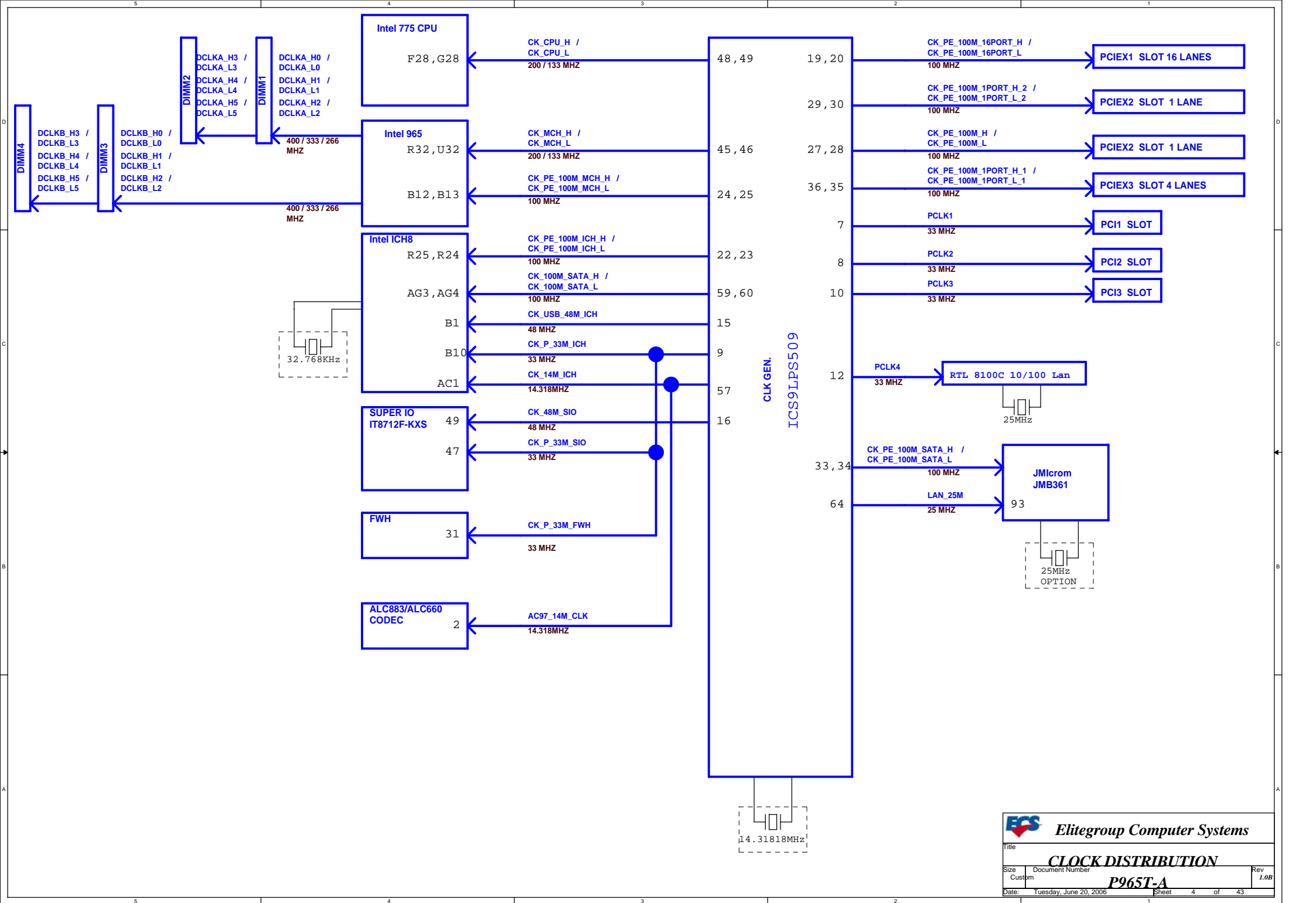
ECS Elitegroup Computer Systems

Title **System Block Diagram**

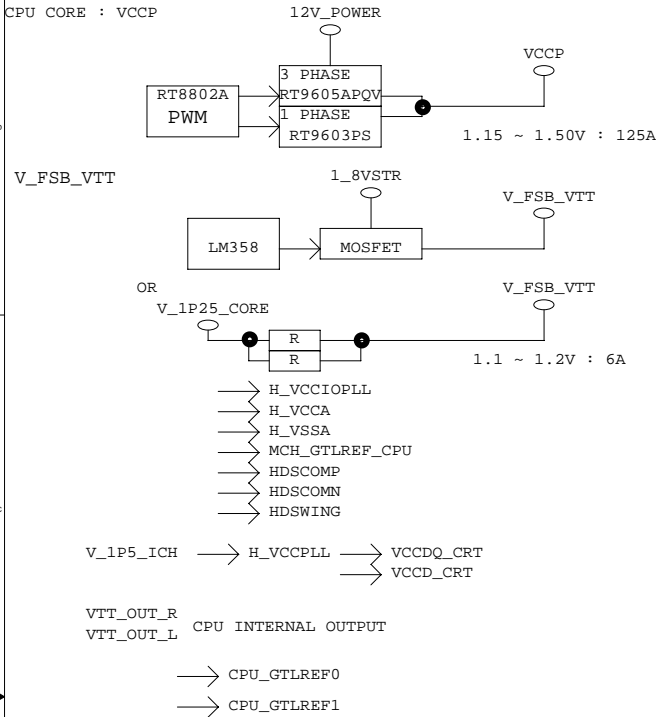
Size Document Number **P965T-A** Rev **1.0B**

Date: Tuesday, June 20, 2006 Sheet 2 of 43

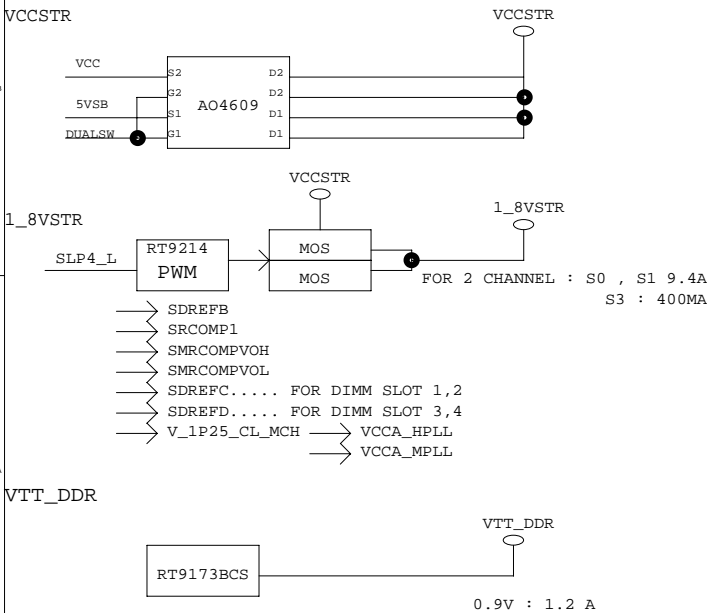




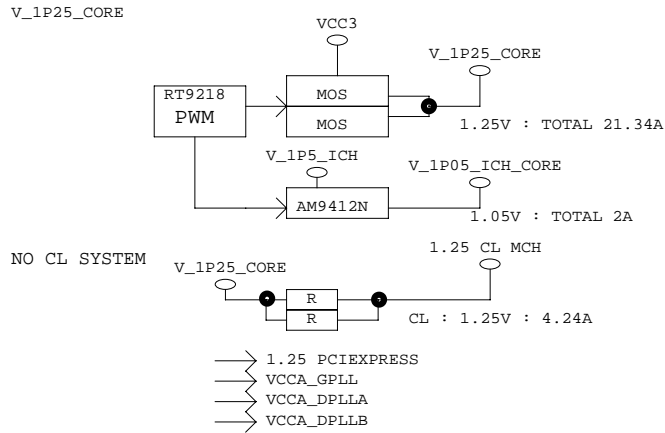
CPU VOLTAGE



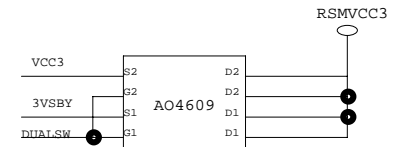
DDR2 VOLTAGE



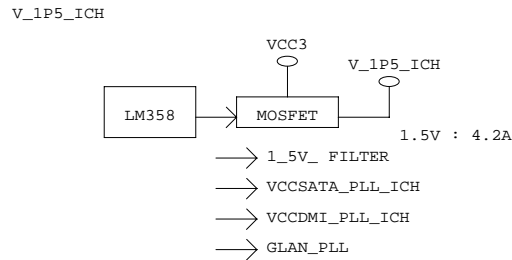
NORTH BRIDGE



3VDUAL



SOUTH BRIDGE

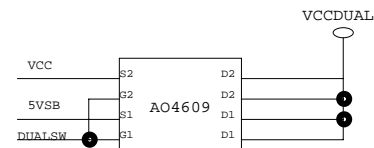


V_1P05_ICH_CORE

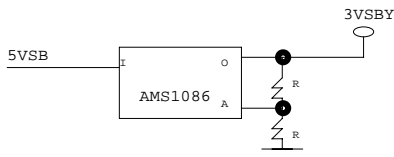
SYSTEM VOLTAGE

+12V
-12V
VCC
5VSB

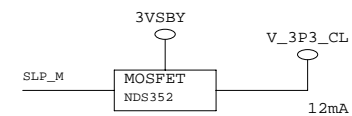
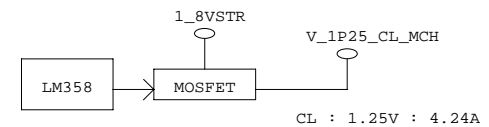
5VDUAL

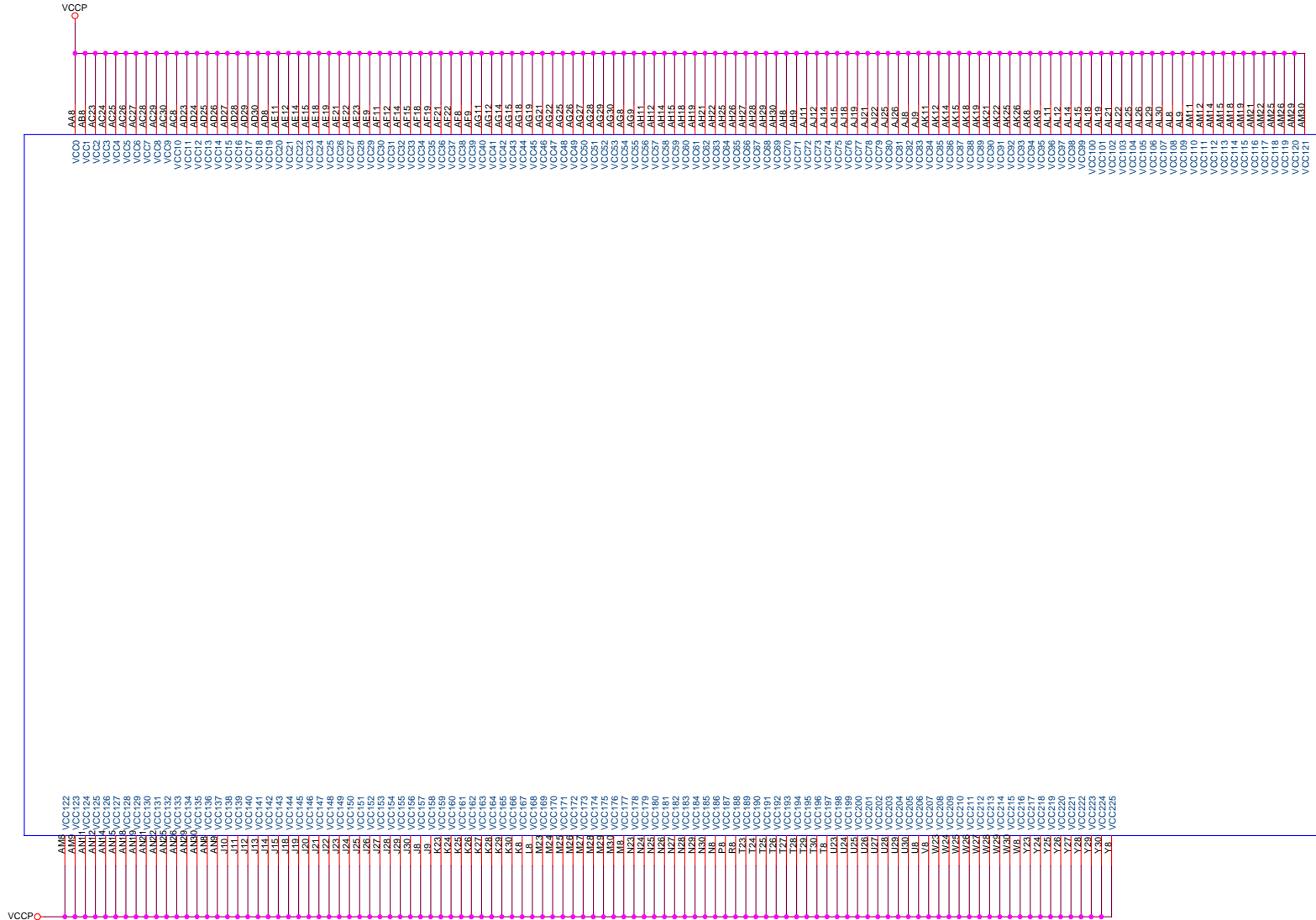


3VSBY




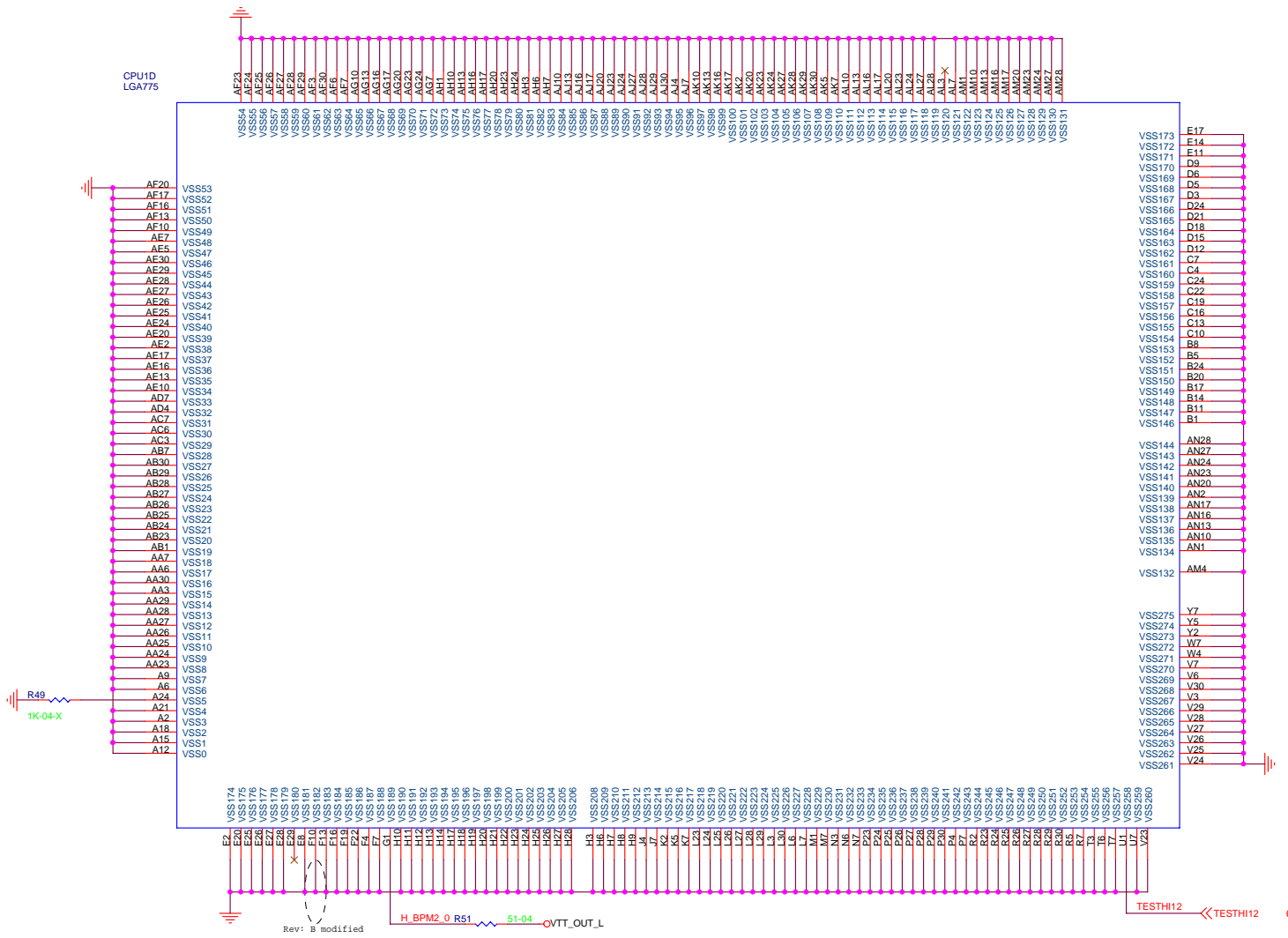
CL SYSTEM :





CPU1C
LGA775

 Elitegroup Computer Systems		
Title		
P4 LGA775P Part C		
Size	Document Number	Rev
Custom:	P965T-A	1.0B
Date:	Tuesday, June 20, 2006	Sheet 8 of 43

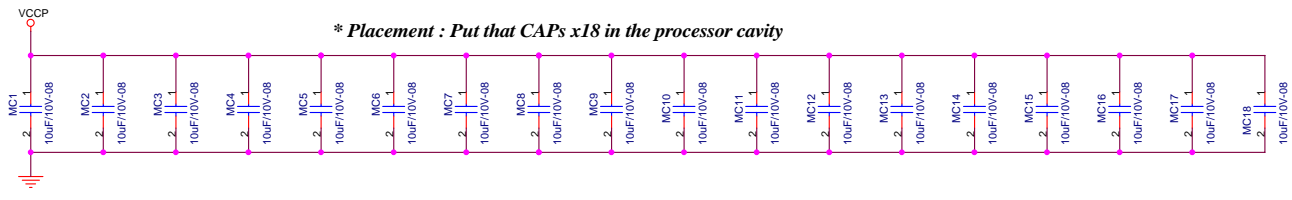


Rev: B modified

H_BPM2_0 R51 51-04 OVTT_OUT_L

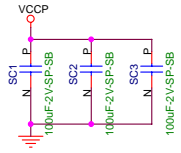
TESTH12 TESTH12 6

Title P4 LGA775P Part D		
Size	Document Number	Rev
Custor	P965T-A	1.0R
Date: Tuesday, June 20, 2006 Sheet 9 of 43		

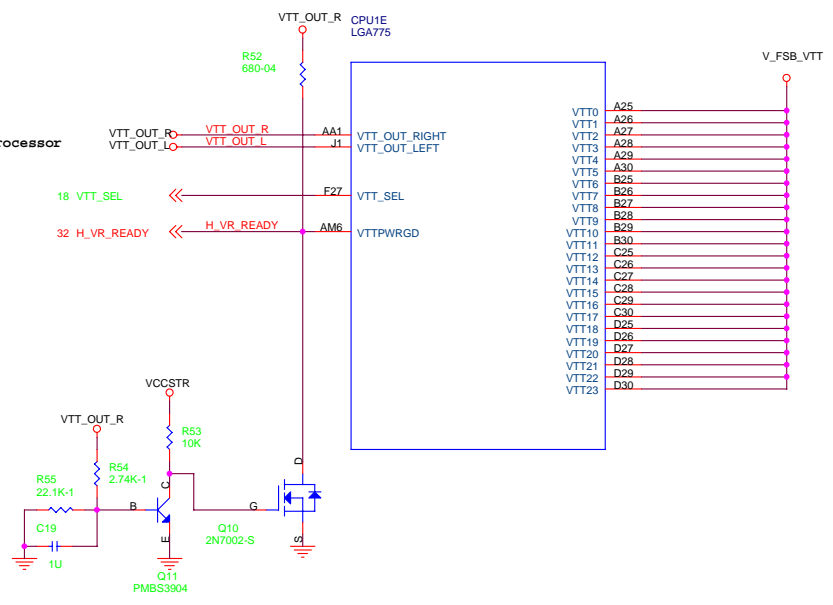


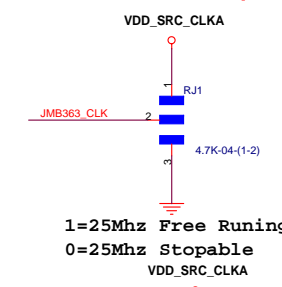
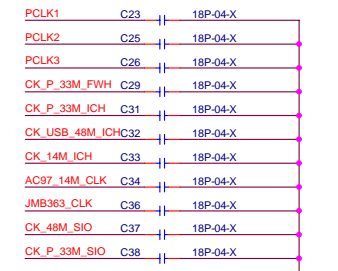
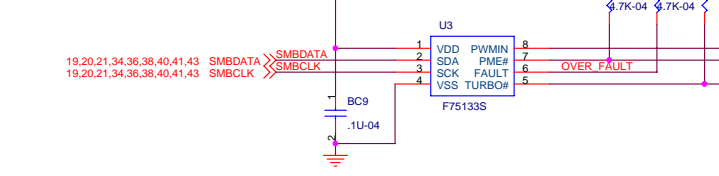
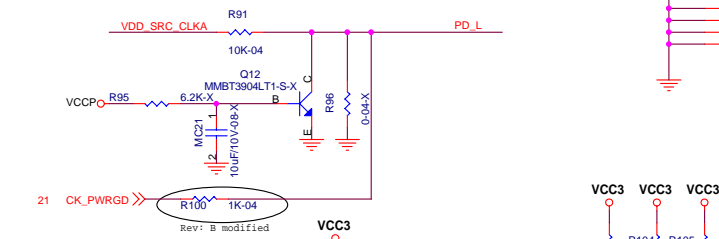
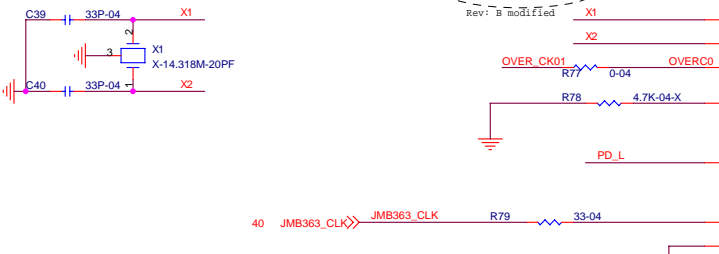
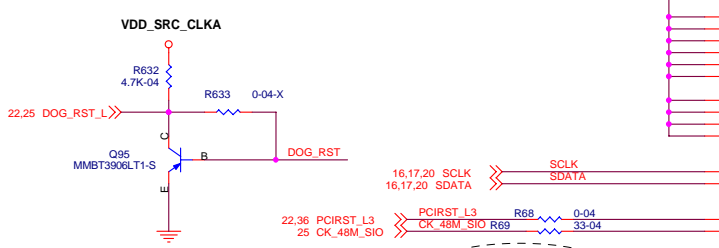
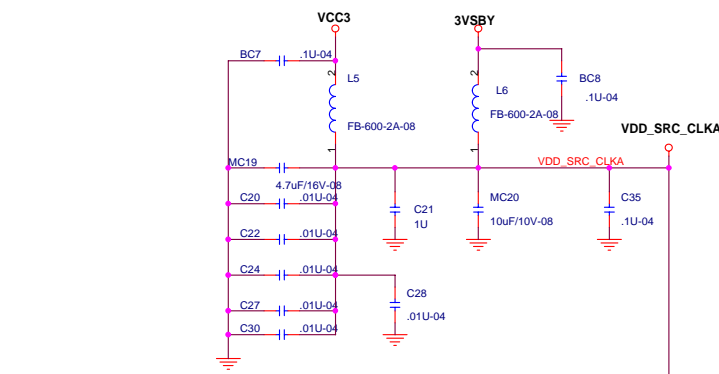
*** Placement : Put that CAPs x18 in the processor cavity**

*** Placement : Put that CAPs x2 on solder side**

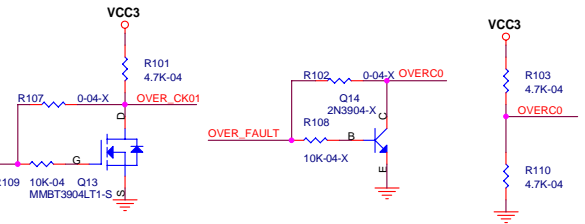
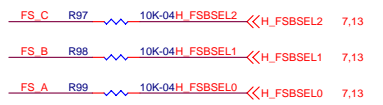
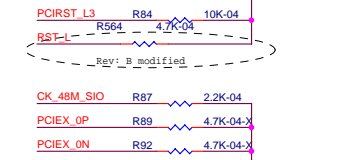


VTT_SEL=0 for the Tejas processor





1=25Mhz Free Running
0=25Mhz Stopable
VDD_SRC_CLKA

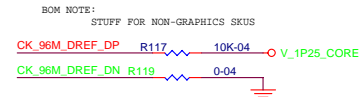
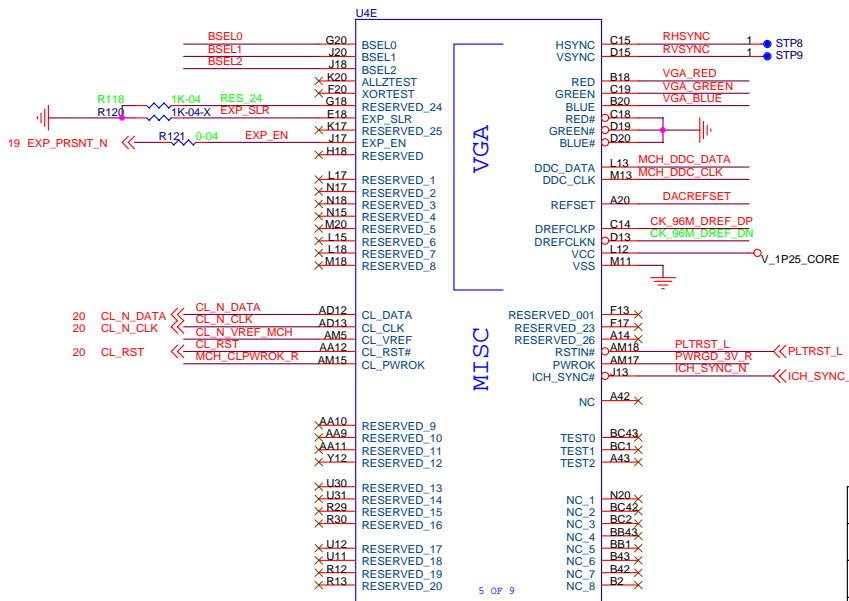


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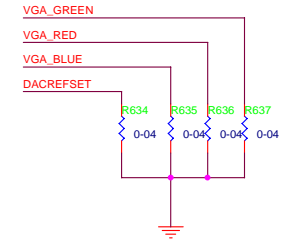
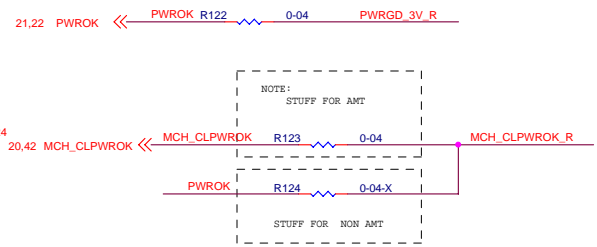
Clock Generator(CK410)

Size: Document Number **P965T-A** Rev: **1.0B**

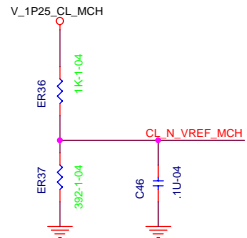
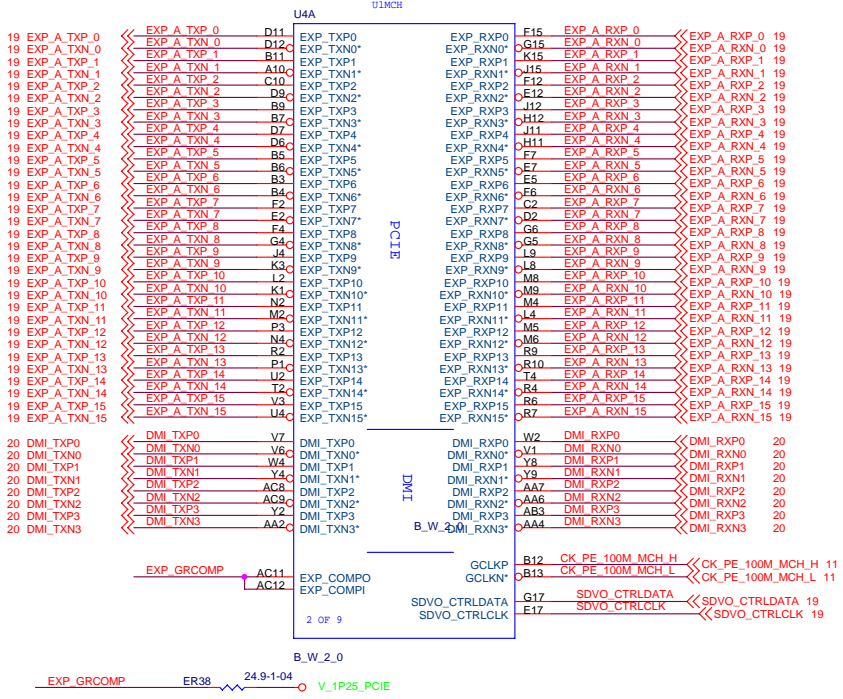
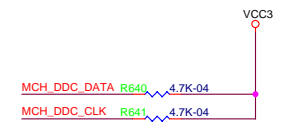
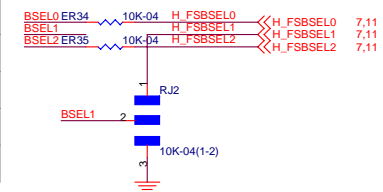
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DDC MCH SIDE TERMINATION
DDC_DATA/DDC_CLK : LOCKTITE PULL-UPS
ANYWHERE ON ROUTE OF TRACE



BSEL TABLE			
2	1	0	PCB FREQUENCY
0	0	0	267 (1067)
0	0	1	133 (533)
0	1	0	200 (800)

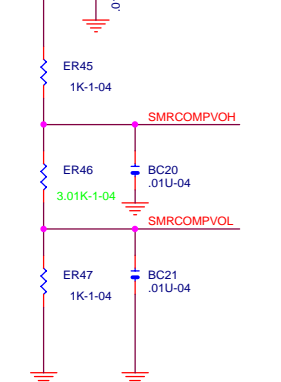
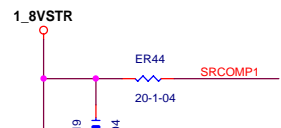
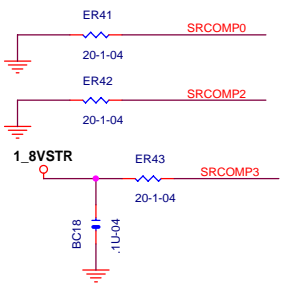
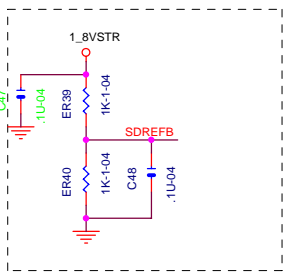


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Title: **BROAD WATER(MCH)Part B**

Size: Custom Document Number: **P965T-A** Rev: 1.0B

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DESIGN NOTE:
 BUFFERS CALIBRATE TO
 20/80% OF V_{SM} INTERNAL
 BUFFERS SET TO 20 OHMS
 SMRCOMPVOH : 0.8 X
 1_8VSTR
 SMRCOMPVOL : 0.2 X
 1_8VSTR

U4C		U1MCH		U4D		U1MCH	
DQS_H A6	AG42	SDQS_A6	SDQS_A0	SDQS_B7	SDQS_B0	SDQS_B0	MD_A[0..63]
DQS_L A6	AG41	SDQS_A6#	SDQS_A0#	DQS_L B7	AC36	AV6	DQS_L A[0..7]
MPD A6	AG40	SDM_A6	SDM_A0	MPD B7	AD38	AU6	DQS_L A[0..7]
MD A48	AH43	SDQ_A48	SDQ_A0	MD B56	AD36	SDM_B7	DQS_H A[0..7]
MD A49	AH44	SDQ_A49	SDQ_A1	MD B57	AC33	SDQ_B0	DQS_H A[0..7]
MD A50	AF39	SDQ_A50	SDQ_A2	MD B58	AA34	SDQ_B1	MPD A[0..7]
MD A51	AE40	SDQ_A51	SDQ_A3	MD B59	AA36	SDQ_B2	MAAA [0..14]
MD A52	AJ42	SDQ_A52	SDQ_A4	MD B60	AD34	SDQ_B3	CSA L[0..3]
MD A53	AF41	SDQ_A53	SDQ_A5	MD B61	AF38	SDQ_B4	CKEA [0..3]
MD A54	AF42	SDQ_A54	SDQ_A6	MD B62	AC34	SDQ_B5	DCLCA_H[0..5]
MD A55	AC42	SDQS_A7	SDQ_A7	MD B63	AA33	SDQ_B6	ODTA [0..3]
DQS_L A7	AC41	SDQS_A7#	SDQ_A8			SDQ_B7	SWE_L A
MPD A7	AC40	SDM_A7	SDQ_A9				SCAS_L A
MD A56	AD43	SDQ_A56	SDQ_A10				SRAS_L A
MD A57	AD43	SDQ_A57	SDQ_A11				
MD A58	AB41	SDQ_A58	SDQ_A12				
MD A59	AA40	SDQ_A59	SDQ_A13				
MD A60	AE42	SDQ_A60	SDQ_A14				
MD A61	AE41	SDQ_A61	SDQ_A15				
MD A62	AC39	SDQ_A62					
MD A63	AB42	SDQ_A63					
MAAA 0	BA31	SMA_A0	SDQS_A2				
MAAA 1	BB25	SMA_A1	SDQS_A2#				
MAAA 2	BA28	SMA_A2	SDM_A2				
MAAA 3	BA25	SMA_A3					
MAAA 4	AY25	SMA_A4					
MAAA 5	BA23	SMA_A5					
MAAA 6	AY24	SMA_A6					
MAAA 7	AY23	SMA_A7					
MAAA 8	BB23	SMA_A8					
MAAA 9	BA22	SMA_A9					
MAAA 10	AY33	SMA_A10					
MAAA 11	BB22	SMA_A11					
MAAA 12	AY38	SMA_A12					
MAAA 13	AY38	SMA_A13					
MAAA 14	BA21	SMA_A14					
SWE_L A	BB34	SWE_A#					
SCAS_L A	AY35	SCAS_A#					
SRAS_L A	BB33	SRAS_A#					
SBSA 0	BA33	SBS_A0					
SBSA 1	AW32	SBS_A1					
SBSA 2	BB21	SBS_A2					
CSA_L0	AW35	SCS_A0#					
CSA_L1	BA35	SCS_A1#					
CSA_L2	BA34	SCS_A2#					
CSA_L3	BB38	SCS_A3#					
CKEA 0	BC20	SCKE_A0					
CKEA 1	AY20	SCKE_A1					
CKEA 2	AY21	SCKE_A2					
CKEA 3	BA19	SCKE_A3					
ODTA 0	AY37	SODT_A0					
ODTA 1	BA38	SODT_A1					
ODTA 2	BB35	SODT_A2					
ODTA 3	BA39	SODT_A3					
DCLKA_H0	AU31	SCLK_A0					
DCLKA_L0	AB31	SCLK_A0#					
DCLKA_H1	AN27	SCLK_A1					
DCLKA_L1	AN27	SCLK_A1#					
DCLKA_H2	AV33	SCLK_A2					
DCLKA_L2	AW33	SCLK_A2#					
DCLKA_H3	AP29	SCLK_A3					
DCLKA_L3	AP29	SCLK_A3#					
DCLKA_H4	AM28	SCLK_A4					
DCLKA_L4	AM27	SCLK_A4#					
DCLKA_H5	AT33	SCLK_A5					
DCLKA_L5	AU33	SCLK_A5#					
AN21	RESERVED						

Channel A

U4C		U1MCH		U4D		U1MCH	
DQS_H B7	AC36	SDQS_B7	SDQS_B0	DQS_H B0	AC36	AV6	DQS_H B0
DQS_L B7	AD38	SDQS_B7#	SDQS_B0#	DQS_L B0	AD38	AU6	DQS_L B0
MPD B7	AD36	SDM_B7	SDM_B0	MPD B0	AD36	SDM_B0	
MD B56	AD36	SDQ_B56	SDQ_B0	MD B0	AD36	SDQ_B0	
MD B57	AC33	SDQ_B57	SDQ_B1	MD B1	AC33	SDQ_B1	
MD B58	AA34	SDQ_B58	SDQ_B2	MD B2	AA34	SDQ_B2	
MD B59	AA36	SDQ_B59	SDQ_B3	MD B3	AA36	SDQ_B3	
MD B60	AD34	SDQ_B60	SDQ_B4	MD B4	AD34	SDQ_B4	
MD B61	AF38	SDQ_B61	SDQ_B5	MD B5	AF38	SDQ_B5	
MD B62	AC34	SDQ_B62	SDQ_B6	MD B6	AC34	SDQ_B6	
MD B63	AA33	SDQ_B63	SDQ_B7	MD B7	AA33	SDQ_B7	
MAAB 0	BB17	SMA_B0	SDQS_B1				
MAAB 1	AY17	SMA_B1	SDQS_B1#				
MAAB 2	BA17	SMA_B2	SDM_B1				
MAAB 3	BC16	SMA_B3	SDM_B1#				
MAAB 4	AW15	SMA_B4	SDQ_B8				
MAAB 5	BA15	SMA_B5	SDQ_B9				
MAAB 6	BA15	SMA_B6	SDQ_B9				
MAAB 7	BA14	SMA_B7	SDQ_B10				
MAAB 8	AY15	SMA_B8	SDQ_B11				
MAAB 9	BB14	SMA_B9	SDQ_B12				
MAAB 10	AW18	SMA_B10	SDQ_B13				
MAAB 11	BB13	SMA_B11	SDQ_B14				
MAAB 12	BA13	SMA_B12	SDQ_B15				
MAAB 13	AY29	SMA_B13	SDQ_B16				
MAAB 14	AY13	SMA_B14	SDQ_B17				
SWE_L B	BA27	SWE_B#	SDQ_B16				
SCAS_L B	AW25	SCAS_B#	SDQ_B17				
SRAS_L B	AW28	SRAS_B#	SDQ_B18				
SBBS 0	AY19	SBS_B0	SDQ_B19				
SBBS 1	BA18	SBS_B1	SDQ_B20				
SBBS 2	BC12	SBS_B2	SDQ_B21				
CSB_L0	BB27	SCS_B0#	SDQ_B22				
CSB_L1	BB30	SCS_B1#	SDQ_B23				
CSB_L2	AY27	SCS_B2#	SDQ_B24				
CSB_L3	AY31	SCS_B3#	SDQ_B25				
CKEB 0	AY12	SCKE_B0	SDQ_B26				
CKEB 1	AW12	SCKE_B1	SDQ_B27				
CKEB 2	BB11	SCKE_B2	SDQ_B28				
CKEB 3	BA11	SCKE_B3	SDQ_B29				
ODTB 0	BA29	SODT_B0	SDQ_B30				
ODTB 1	BA30	SODT_B1	SDQ_B31				
ODTB 2	BB29	SODT_B2	SDQ_B32				
ODTB 3	BB31	SODT_B3	SDQ_B33				
DCLKB_H0	AV31	SCLK_B0	SDQ_B34				
DCLKB_L0	AW31	SCLK_B0#	SDQ_B35				
DCLKB_H1	AU27	SCLK_B1	SDQ_B36				
DCLKB_L1	AT27	SCLK_B1#	SDQ_B37				
DCLKB_H2	AV32	SCLK_B2	SDQ_B38				
DCLKB_L2	AT32	SCLK_B2#	SDQ_B39				
DCLKB_H3	AU29	SCLK_B3	SDQ_B40				
DCLKB_L3	AP29	SCLK_B3#	SDQ_B41				
DCLKB_H4	AV29	SCLK_B4	SDQ_B42				
DCLKB_L4	AW29	SCLK_B4#	SDQ_B43				
DCLKB_H5	AN33	SCLK_B5	SDQ_B44				
DCLKB_L5	AP32	SCLK_B5#	SDQ_B45				
RESERVED_1	BB2	RESERVED_1	SDQ_B46				
RESERVED_2	AW42	RESERVED_2	SDQ_B47				
RESERVED_3	AN32	RESERVED_3	SDQ_B48				
RESERVED_4	AM31	RESERVED_4	SDQ_B49				
RESERVED_5	AG32	RESERVED_5	SDQ_B50				
RESERVED_6	AF32	RESERVED_6	SDQ_B51				
RESERVED_7	AP21	RESERVED_7	SDQ_B52				
RESERVED_8	AA39	RESERVED_8	SDQ_B53				
RESERVED_9	AM21	RESERVED_9	SDQ_B54				
RESERVED_10	AM21	RESERVED_10	SDQ_B55				
SDREFB	AM6	SDREFB					
SRCOMP0	AN2	SRCOMP0					
SRCOMP1	AN5	SRCOMP1					
SRCOMP2	BB40	SRCOMP2					
SRCOMP3	BA40	SRCOMP3					
SMRCOMPVOL	AM8	SMRCOMPVOL					
SMRCOMPVOH	AM10	SMRCOMPVOH					
RESERVED	BB19	RESERVED					

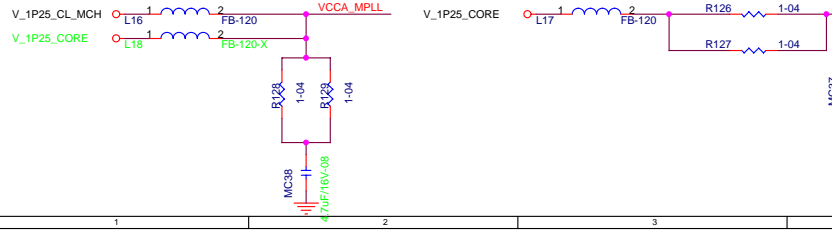
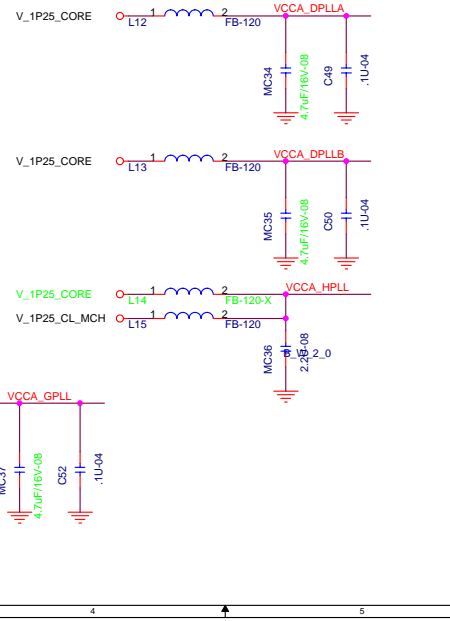
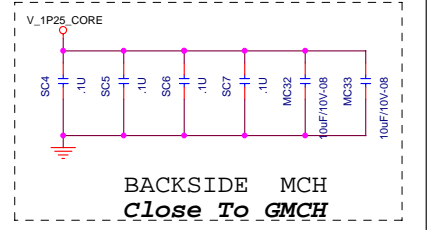
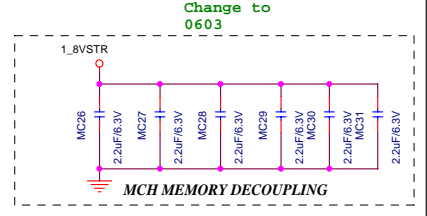
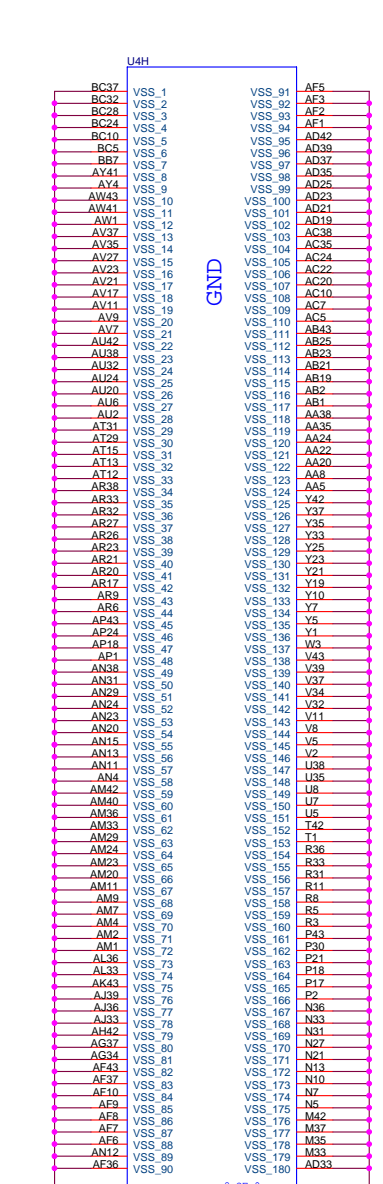
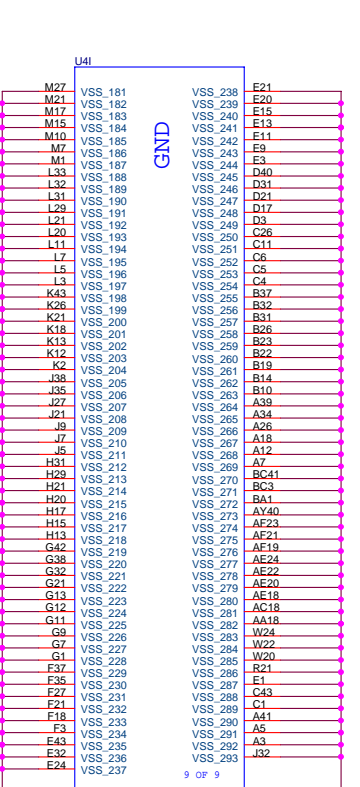
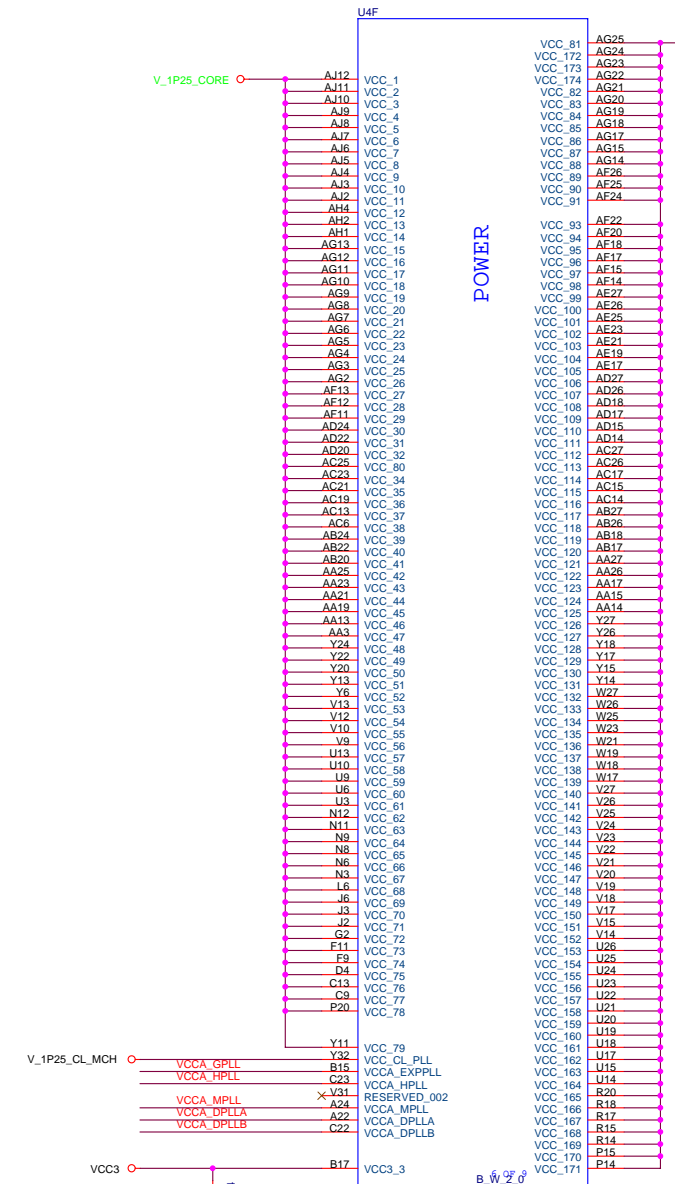
Channel B

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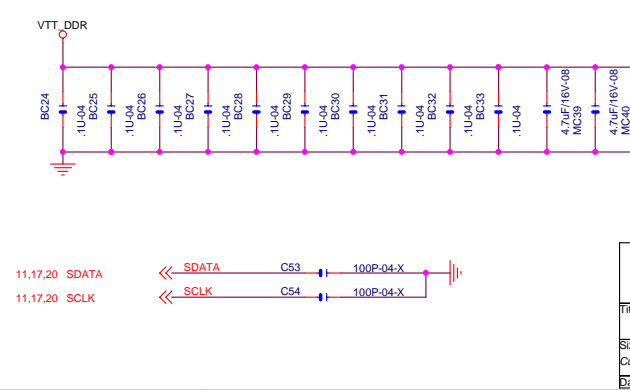
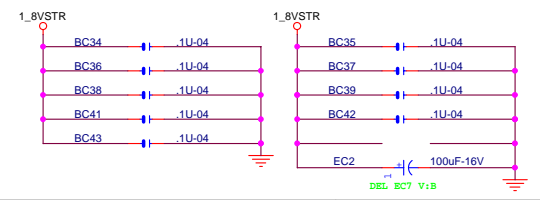
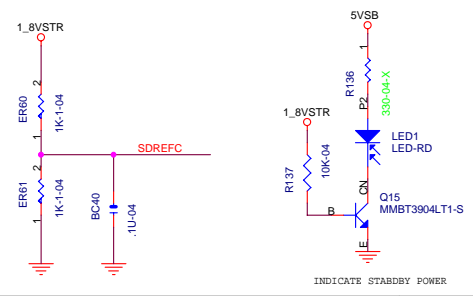
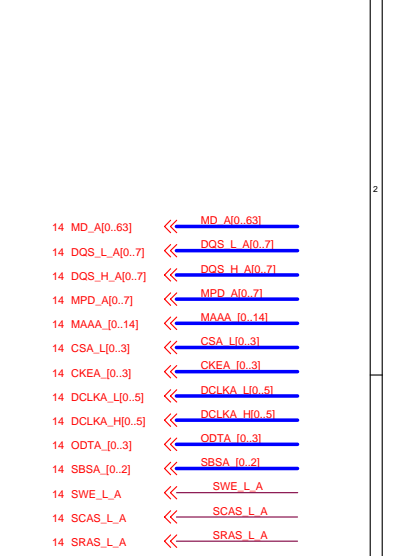
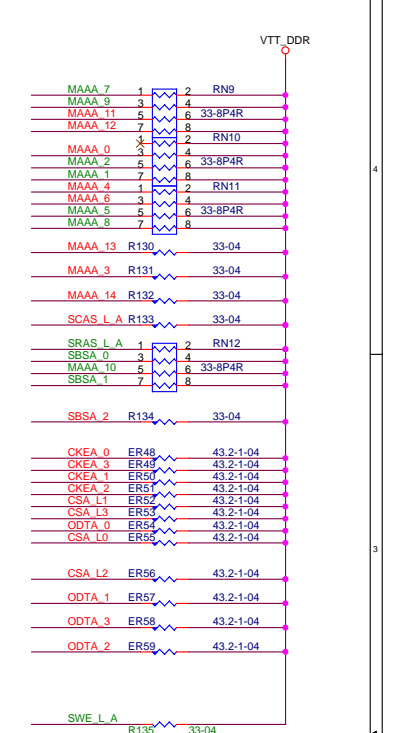
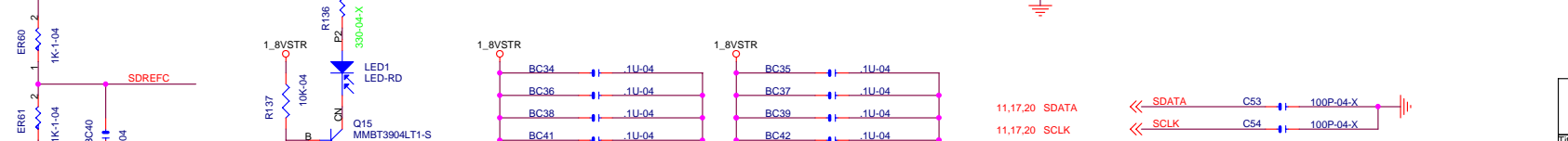
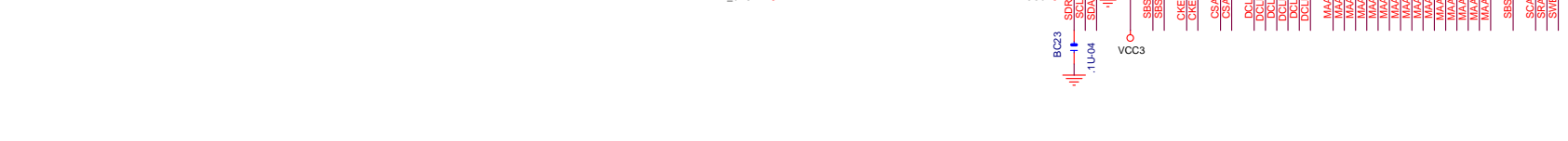
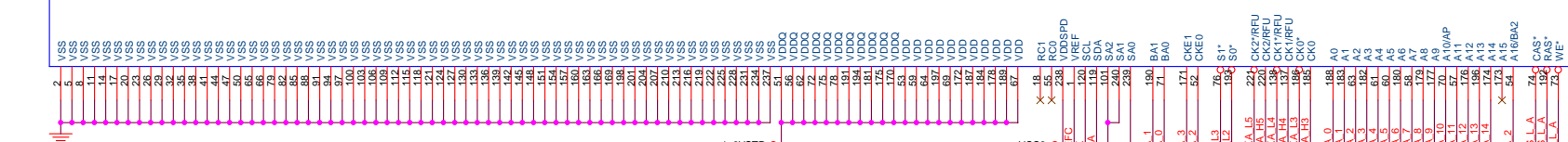
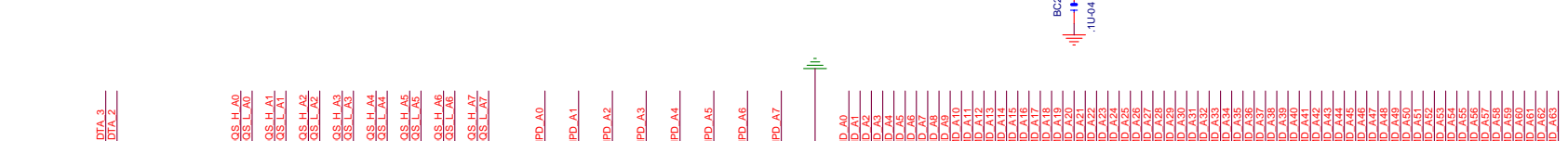
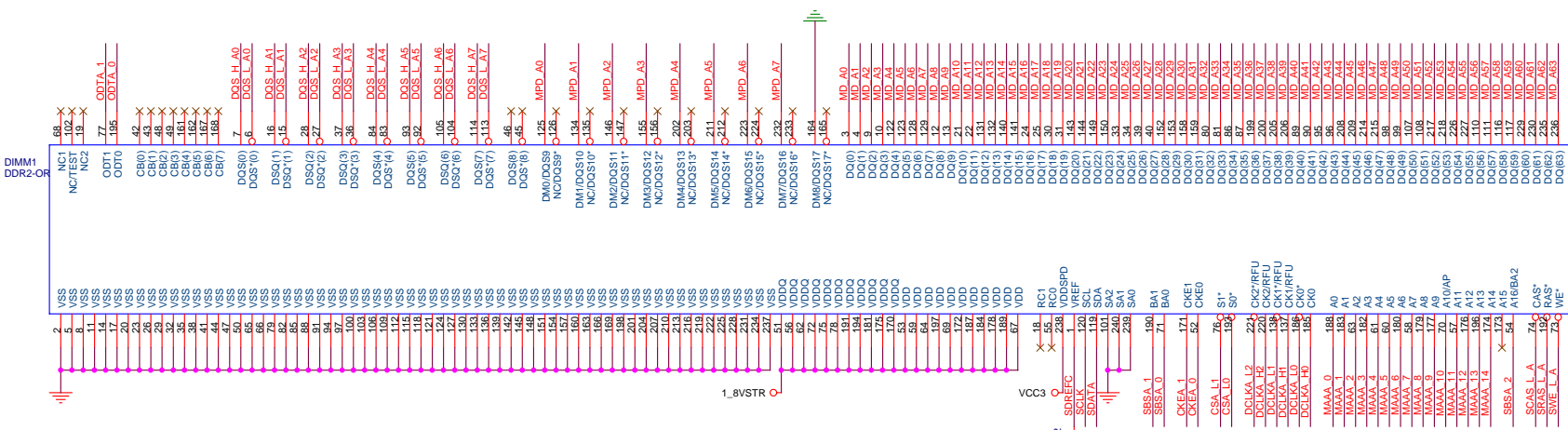
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Size: Document Number **P965T-A** Rev: **1.0B**

Date: Tuesday, June 20, 2006 Sheet: 14 of 43



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 Title: **BROAD WATER(MCH)Part E & G & H**
 Size: Document Number **P965T-A** Rev **1.0B**
 Date: Tuesday, June 20, 2006 Sheet 15 of 43



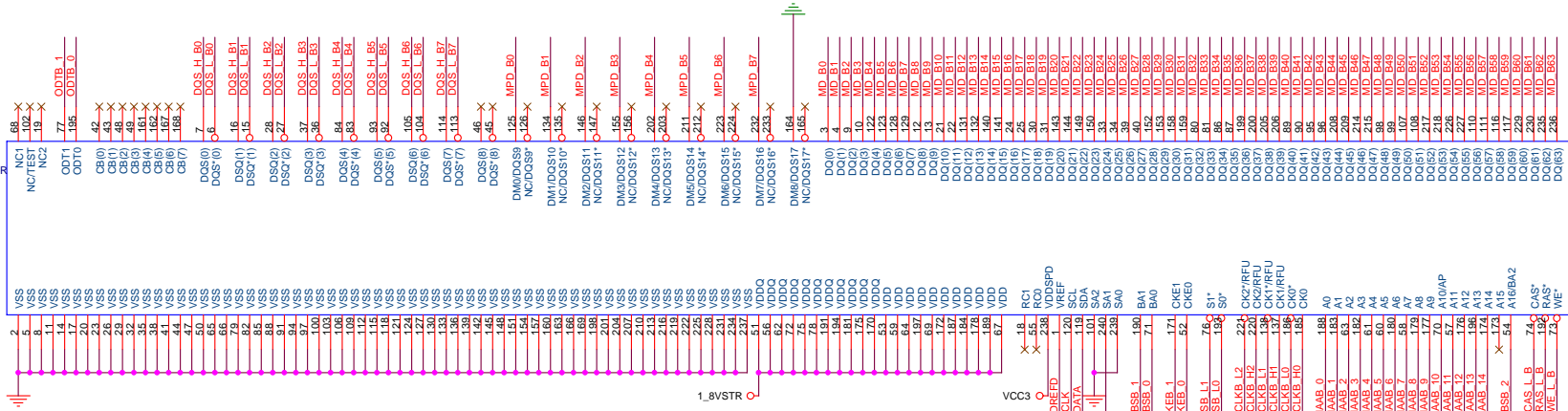
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Title: **DDIMM 1&2 (DDR SDRAMs)**

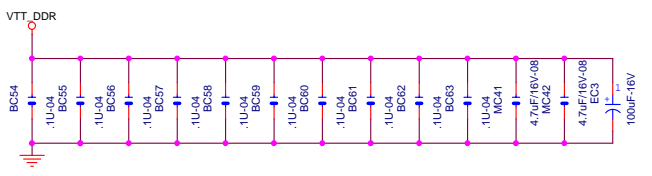
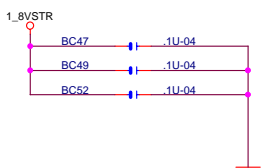
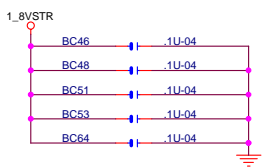
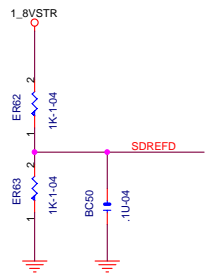
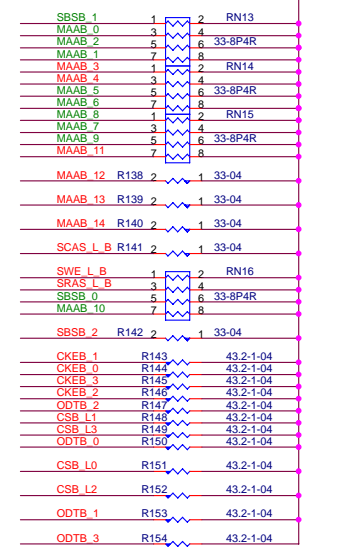
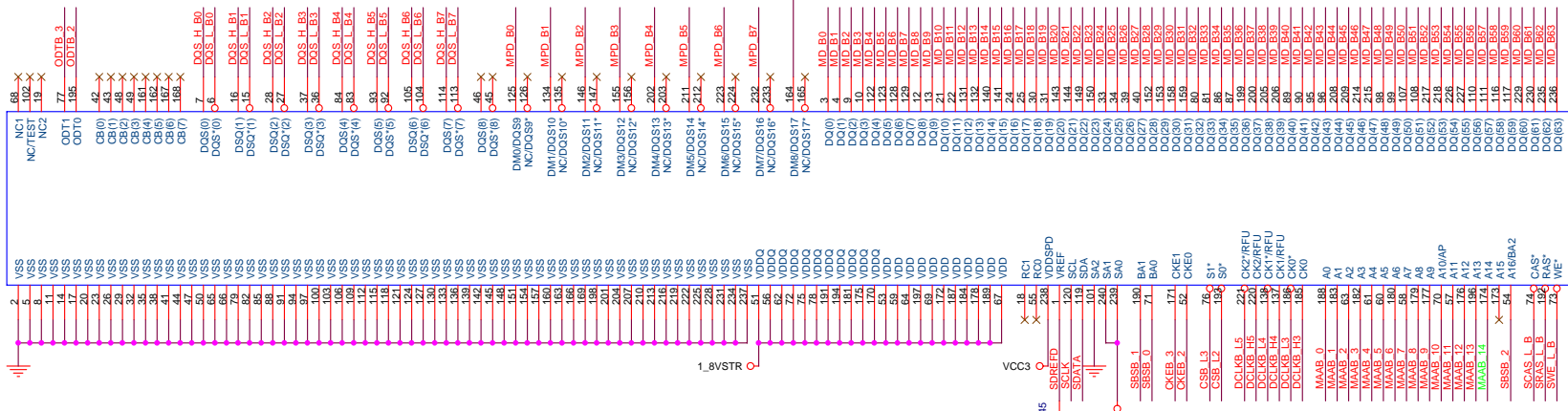
Size: Document Number **P965T-A** Rev: 1.0B

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DIMM3
DDR2-O



DIMM4
DDR2-PU

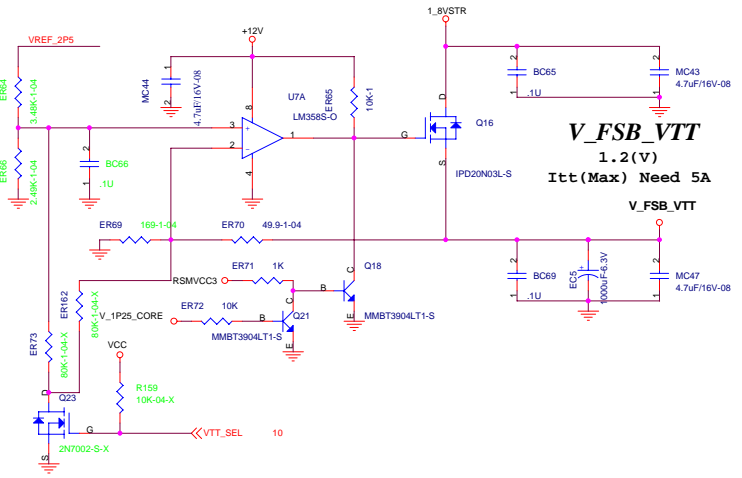


- 14 MD_B[0..63] <<< MD_B[0..63]
- 14 DQS_L[0..7] <<< DQS_L[BIO_7]
- 14 DQS_H[0..7] <<< MPD_B[0..7]
- 14 MPD_B[0..7] <<< MAAB [0..14]
- 14 MAAB [0..14] <<< CSB_L [0..3]
- 14 CSB_L [0..3] <<< CKEB [0..3]
- 14 CKEB [0..3] <<< DCLKB_L [0..5]
- 14 DCLKB_L [0..5] <<< DCLKB_H [0..5]
- 14 DCLKB_H [0..5] <<< ODTB [0..3]
- 14 ODTB [0..3] <<< SBSS [0..2]
- 14 SBSS [0..2] <<< SWE_L_B
- 14 SWE_L_B <<< SCAS_L_B
- 14 SCAS_L_B <<< SRAS_L_B
- 14 SRAS_L_B <<< SDATA
- 11,16,20 SCLK <<< SCLK

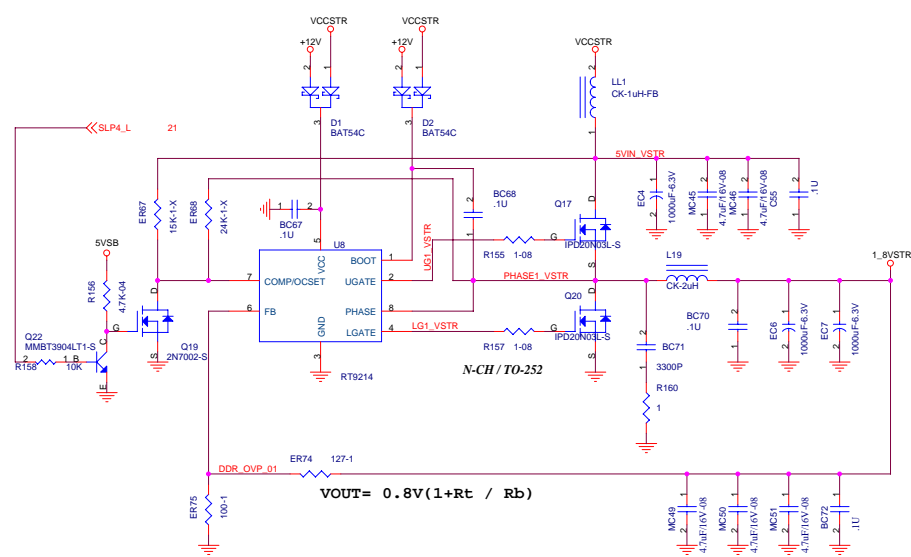
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Title: **DDIMM 3&4 (DDR SDRAMs)**

Size: Document Number
 Custor: **P965T-A**
 Date: Tuesday, June 20, 2006 Sheet 17 of 43

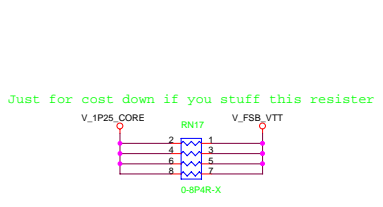


V_FSB_VTT
1.2(V)
Itt(Max) Need 5A
V_FSB_VTT

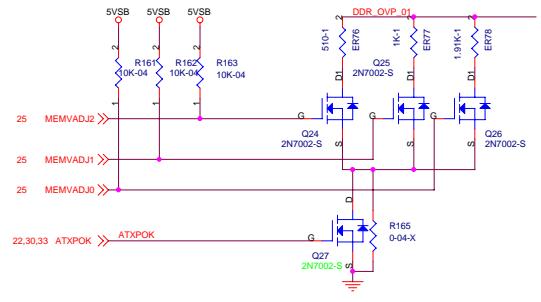
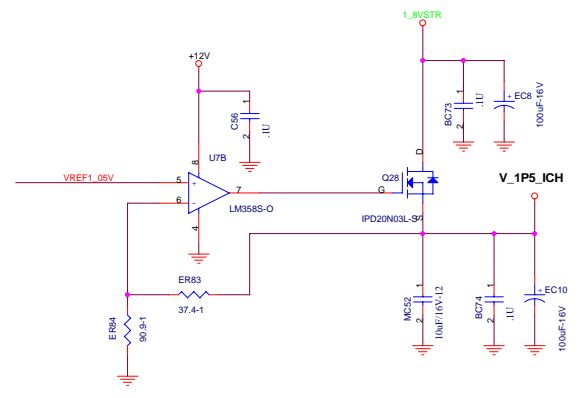
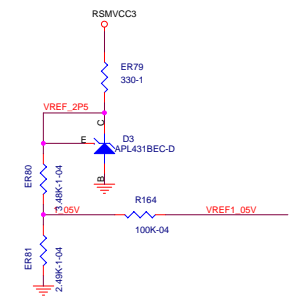


$$V_{OUT} = 0.8V(1+R_t / R_b)$$

1.8VSTR should be able to support up to 14A

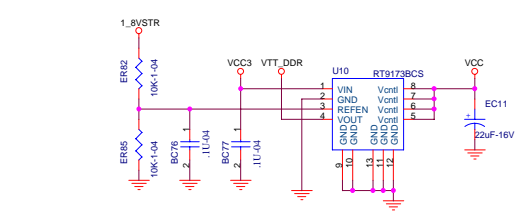
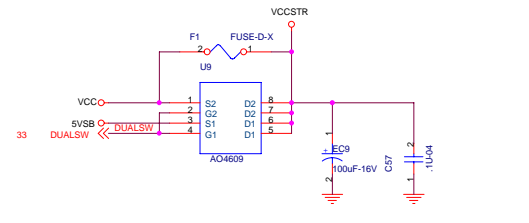


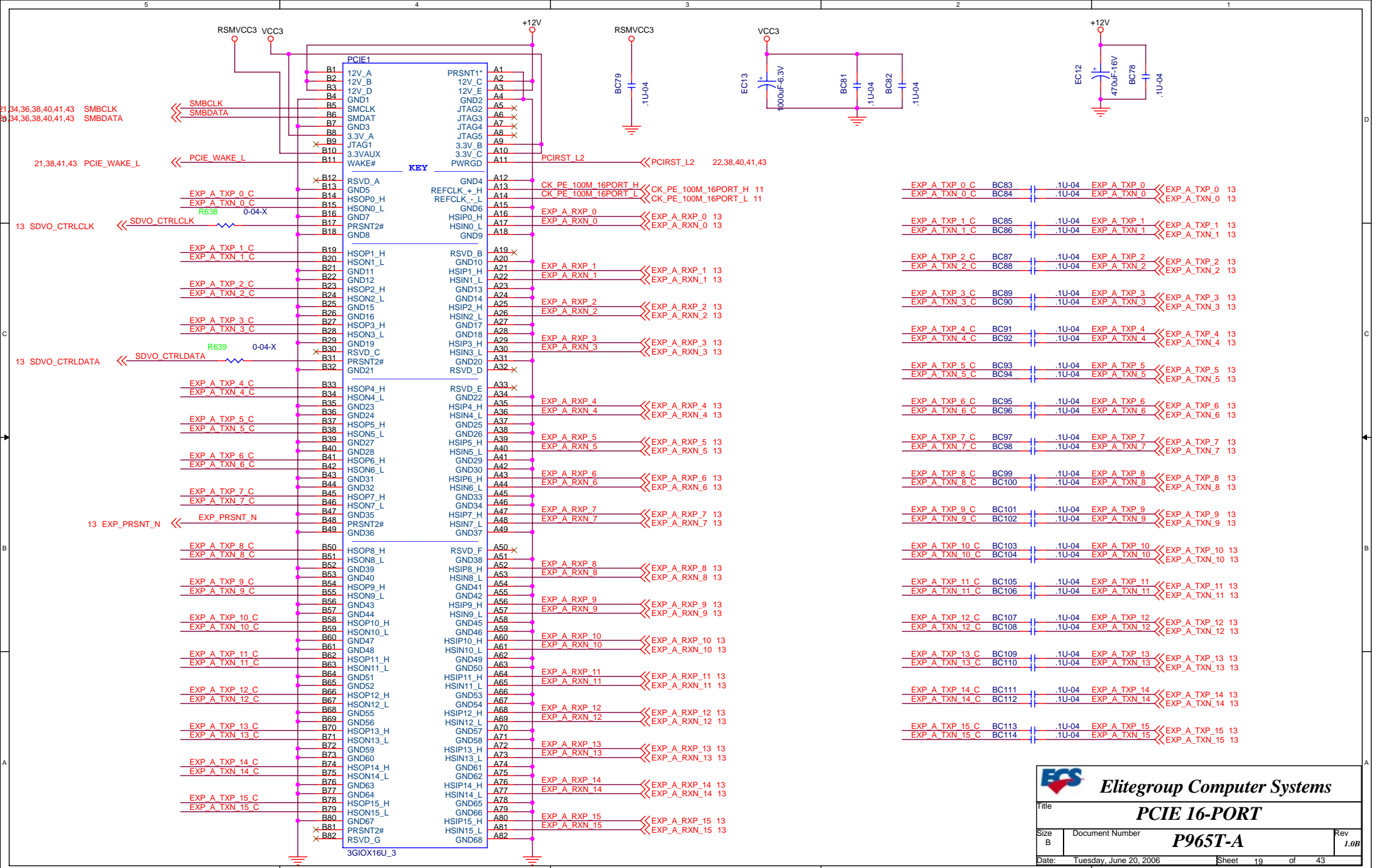
Just for cost down if you stuff this resistor



$$V_o = 1.05(1+R_t/R_b)$$

MEMV2	MEMV1	MEMV0	1_8STR
1	0	0	+0.4V
0	1	1	+0.3V
0	1	0	+0.2V
0	0	1	+0.1V
0	0	0	Normal





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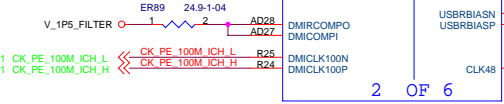
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Size B Document Number **P965T-A** Rev 1.0B

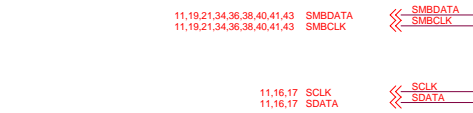
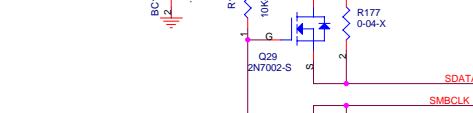
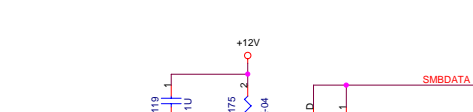
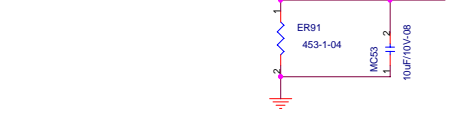
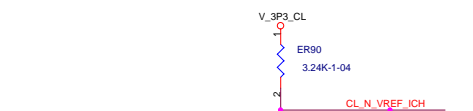
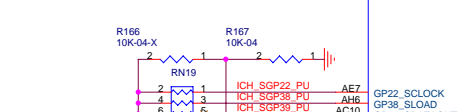
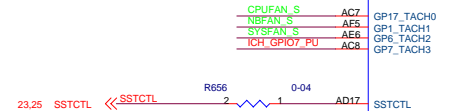
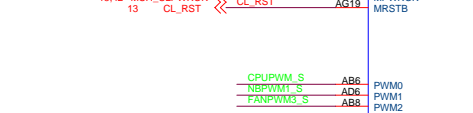
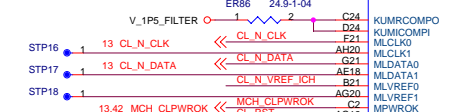
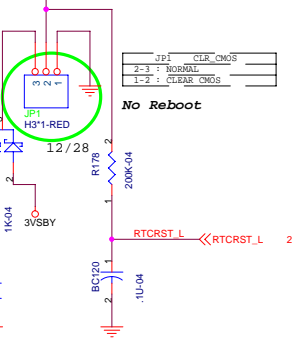
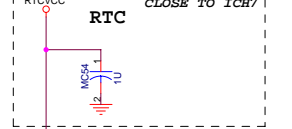
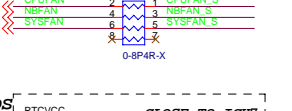
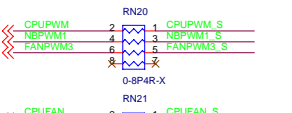
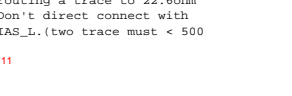
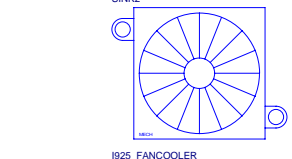
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13	DMI_TXN0	DMI_TXN0	U26	DMI0RXN	USBP0N	G2	USBP0N	USBP0N	35
13	DMI_TXP0	DMI_TXP0	U26	DMI0RXP	USBP0P	G3	USBP0P	USBP0P	35
13	DMI_RXN0	DMI_RXN0	T28	DMI0TXN	USBP1N	H4	USBP1N	USBP1N	35
13	DMI_RXP0	DMI_RXP0	T27	DMI0TXP	USBP1P	H1	USBP1P	USBP1P	35
13	DMI_TXN1	DMI_TXN1	U26	DMI1RXN	USBP2N	H2	USBP2N	USBP2N	35
13	DMI_TXP1	DMI_TXP1	U26	DMI1RXP	USBP2P	J3	USBP2P	USBP2P	35
13	DMI_RXN1	DMI_RXN1	V28	DMI1TXN	USBP3N	J2	USBP3N	USBP3N	35
13	DMI_RXP1	DMI_RXP1	V27	DMI1TXP	USBP3P	J3	USBP3P	USBP3P	35
13	DMI_TXN2	DMI_TXN2	AA25	DMI2RXN	USBP4N	K5	USBP4N	USBP4N	24
13	DMI_TXP2	DMI_TXP2	AA24	DMI2RXP	USBP4P	K4	USBP4P	USBP4P	24
13	DMI_RXN2	DMI_RXN2	Y28	DMI2TXN	USBP5N	K1	USBP5N	USBP5N	24
13	DMI_RXP2	DMI_RXP2	Y27	DMI2TXP	USBP5P	K2	USBP5P	USBP5P	24
13	DMI_TXN3	DMI_TXN3	AC26	DMI3RXN	USBP6N	L3	USBP6N	USBP6N	24
13	DMI_TXP3	DMI_TXP3	AC25	DMI3RXP	USBP6P	L2	USBP6P	USBP6P	24
13	DMI_RXN3	DMI_RXN3	AB28	DMI3TXN	USBP7N	J5	USBP7N	USBP7N	24
13	DMI_RXP3	DMI_RXP3	AB27	DMI3TXP	USBP7P	M4	USBP7P	USBP7P	24
					USBP8N	J2	USBP8N	USBP8N	24
					USBP8P	M1	USBP8P	USBP8P	24
					USBP9N	N2	USBP9N	USBP9N	24
					USBP9P	N3	USBP9P	USBP9P	24

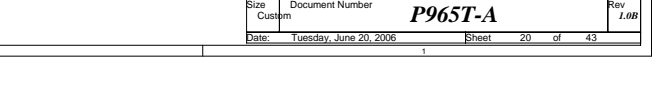
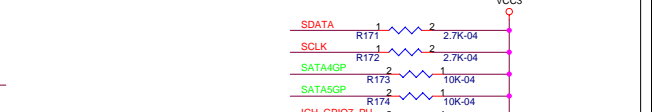
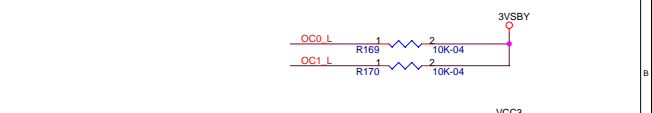
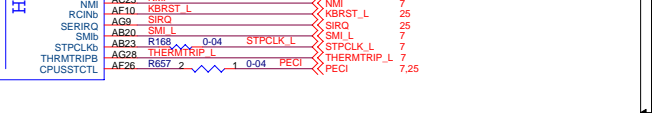
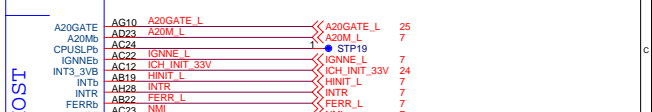
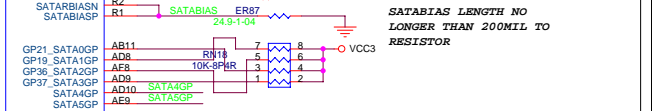
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39	HSO_N6	HSO_P6	BC116	PER6N_KUM_PETN	OC2B	GP41		
39	HSO_P6	HSO_P6	BC116	PER6N_KUM_PETP	OC3B	GP42		
41	HSL_N1	HSL_P1	N24	PER1N	OC4B	GP43		
41	HSL_P1	HSL_P1	N24	PER1P	OC5B	GP29		
41	HSL_N1	HSL_P1	BC117	PET1N	OC6B	GP30		
41	HSL_P1	HSL_P1	BC118	PET1P	OC7B	GP31		
38,41	HSL_N2	HSL_P2	L26	PER2N	OC8B	GP9B		
38,41	HSL_P2	HSL_P2	L26	PER2P				
38,41	HSO_N2	HSO_P2	C58	PET2N				
38,41	HSO_P2	HSO_P2	C59	PET2P				
41,43	HSL_N3	HSL_P3	J26	PER3N				
41,43	HSL_P3	HSL_P3	J26	PER3P				
41,43	HSO_N3	HSO_P3	C61	PET3N				
41,43	HSO_P3	HSO_P3	C61	PET3P				
41	HSL_N4	HSL_P4	G26	PER4N				
41	HSL_P4	HSL_P4	G26	PER4P				
41	HSO_N4	HSO_P4	C62	PET4N				
41	HSO_P4	HSO_P4	C63	PET4P				
40	HSL_N5	HSL_P5	E26	PER5N				
40	HSL_P5	HSL_P5	E26	PER5P				
40	HSO_N5	HSO_P5	C64	PET5N				
40	HSO_P5	HSO_P5	C65	PET5P				



35	USBP0N	G2	USBP0N	USBP0N	35
35	USBP0P	G3	USBP0P	USBP0P	35
35	USBP1N	H4	USBP1N	USBP1N	35
35	USBP1P	H1	USBP1P	USBP1P	35
35	USBP2N	H2	USBP2N	USBP2N	35
35	USBP2P	J3	USBP2P	USBP2P	35
35	USBP3N	J2	USBP3N	USBP3N	35
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24	USBP4N	K5	USBP4N	USBP4N	24
24	USBP4P	K4	USBP4P	USBP4P	24
24	USBP5N	K1	USBP5N	USBP5N	24
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24	USBP8P	M1	USBP8P	USBP8P	24
24	USBP9N	N2	USBP9N	USBP9N	24
24	USBP9P	N3	USBP9P	USBP9P	24



21	SATA0RXN	AC5	SATA0RXN	SATA0RXN	21
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21	SATA0TXN	AE4	SATA0TXN	SATA0TXN	21
21	SATA0TXP	AE3	SATA0TXP	SATA0TXP	21
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21	SATA1RXP	AH2	SATA1RXP	SATA1RXP	21
21	SATA1TXN	AH1	SATA1TXN	SATA1TXN	21
21	SATA1TXP	LW4	SATA1TXP	SATA1TXP	21
21	SATA2RXN	LW5	SATA2RXN	SATA2RXN	21
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21	SATA2TXN	AA4	SATA2TXN	SATA2TXN	21
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21	SATA5RXN	V1	SATA5RXN	SATA5RXN	21
21	SATA5RXP	V2	SATA5RXP	SATA5RXP	21
21	SATA5TXN	V1	SATA5TXN	SATA5TXN	21
21	SATA5TXP	V1	SATA5TXP	SATA5TXP	21
21	SATA6RXN	AG3	CK_100M_SATA_L	CK_100M_SATA_L	11
21	SATA6RXP	AG4	CK_100M_SATA_H	CK_100M_SATA_H	11
21	SATA6TXN				
21	SATA6TXP				



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File: _____

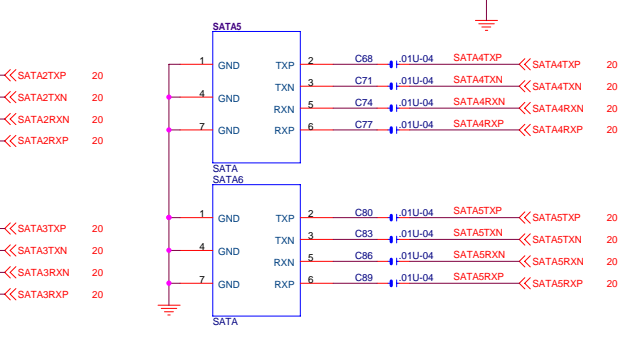
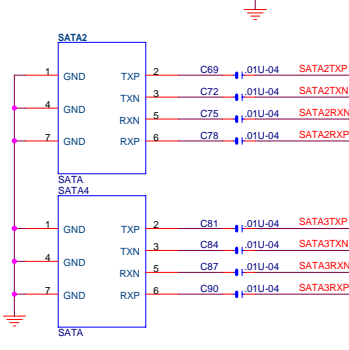
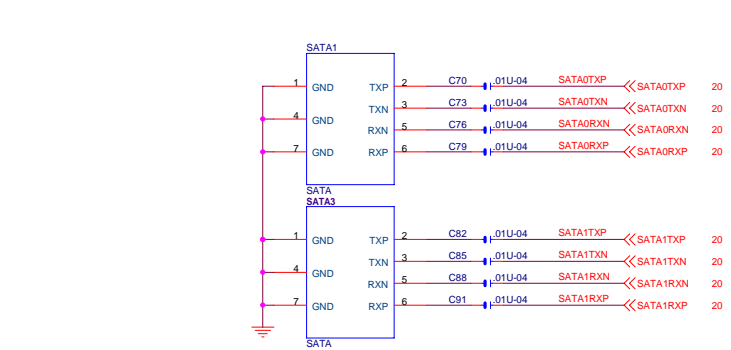
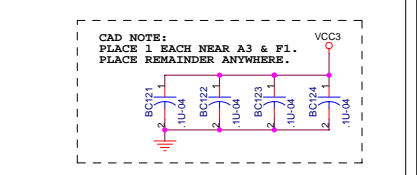
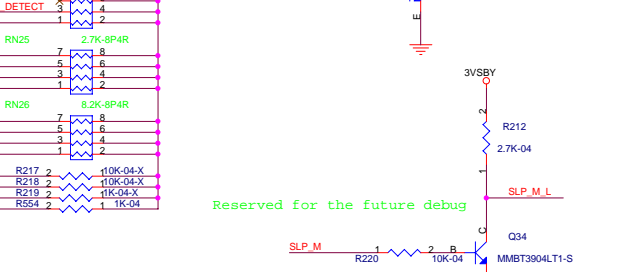
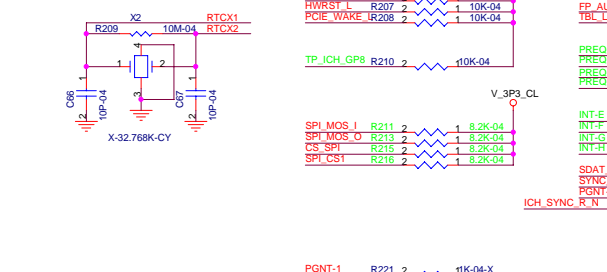
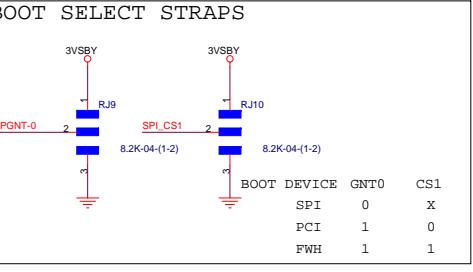
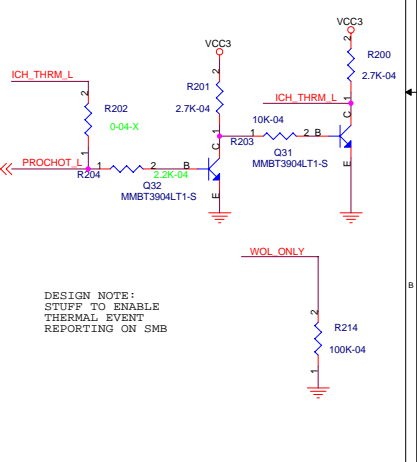
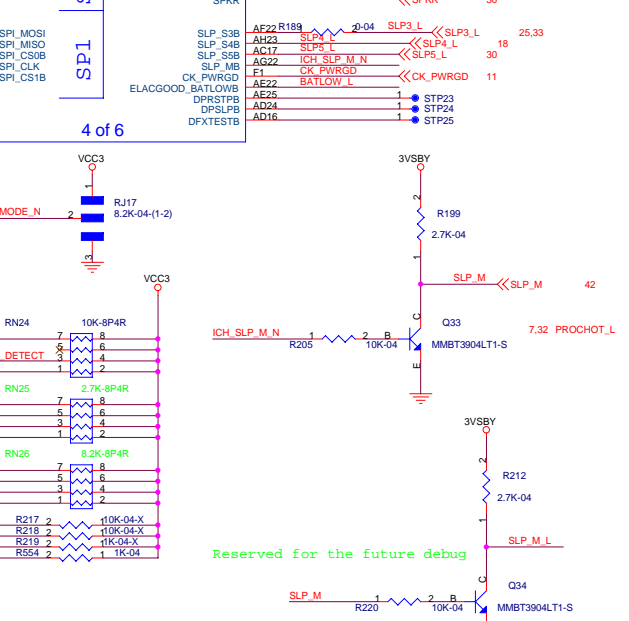
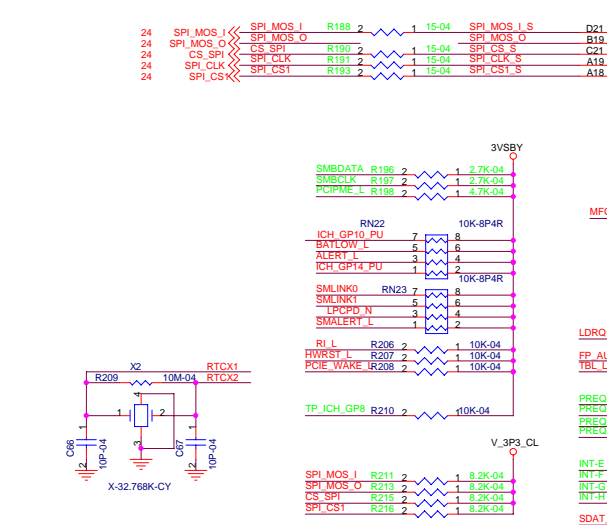
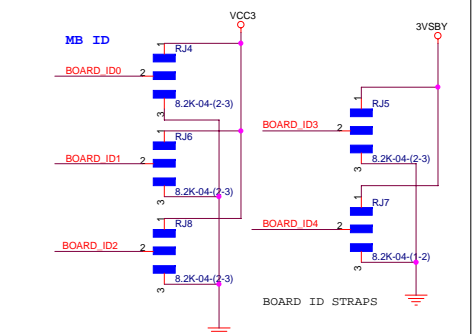
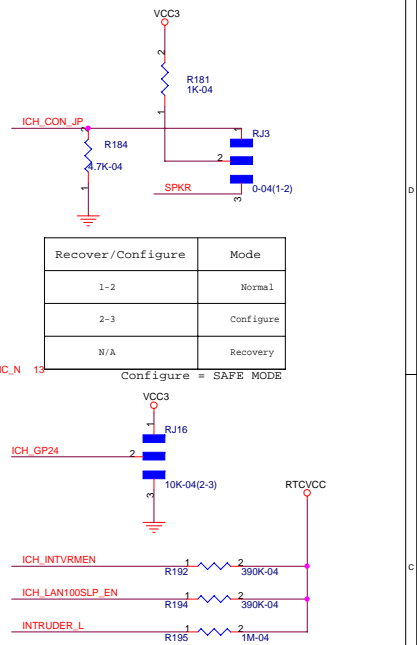
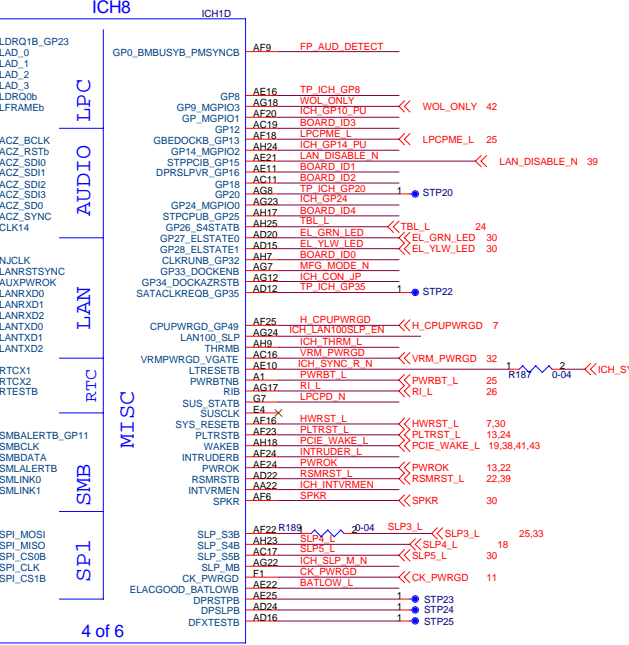
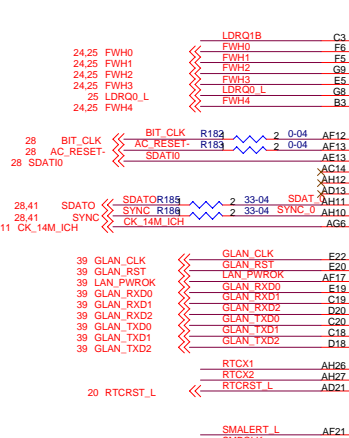
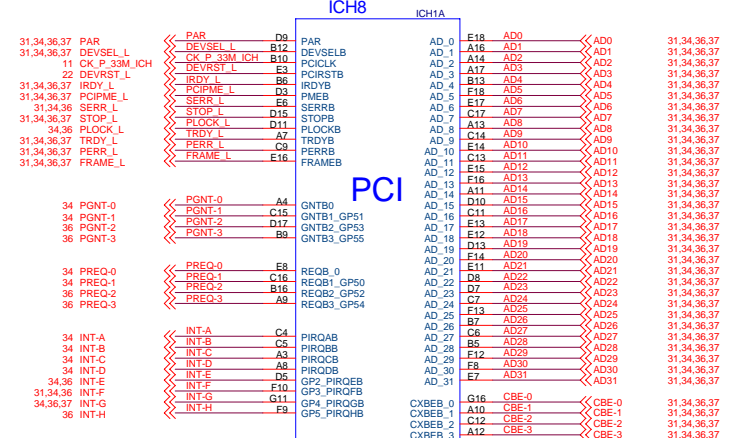
Size: Custom

Date: Tuesday, June 20, 2006

Document Number: **ICH8 Part B & C**

Rev: **L.08**

Sheet: 20 of 43



CAD NOTE:
PLACE 1 EACH NEAR A3 & F1.
PLACE REMAINDER ANYWHERE.

Elitegroup Computer Systems

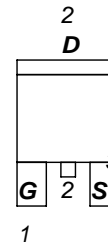
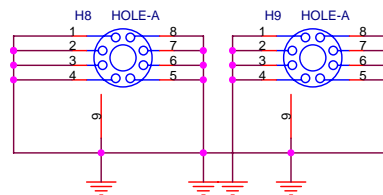
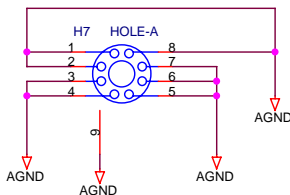
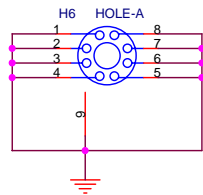
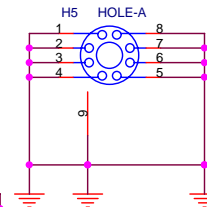
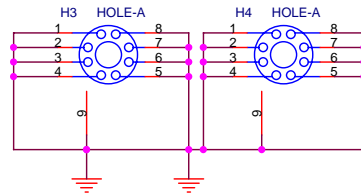
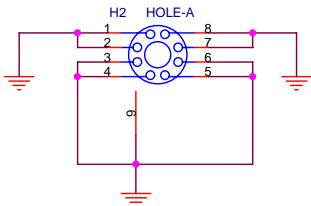
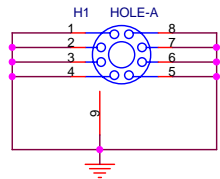
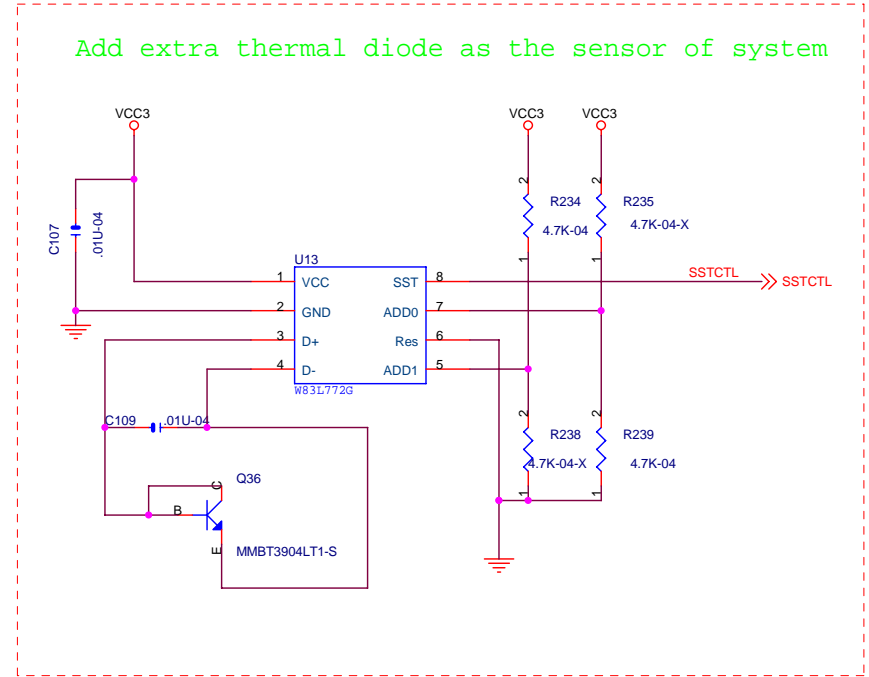
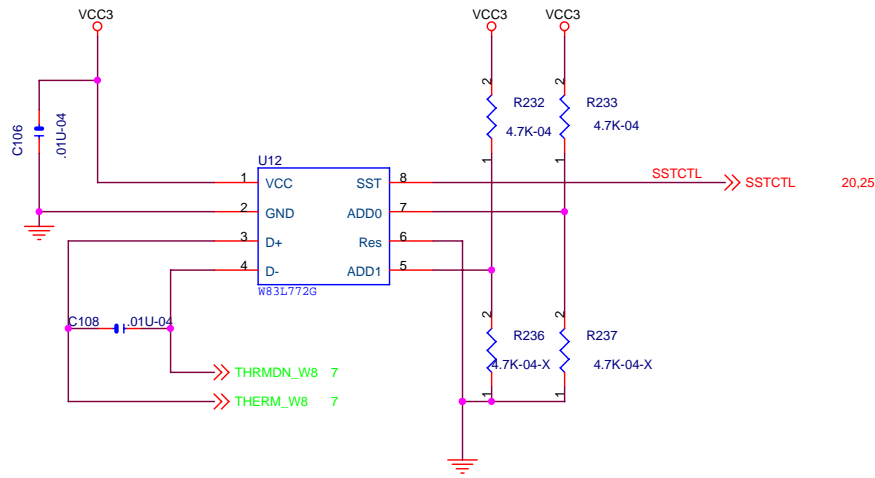
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Size: Custom Document Number: P965T-A Rev: 1.0B

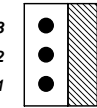
Date: Tuesday, June 20, 2006 Sheet: 21 of 43

R1,R2,R3,R4 depend on the address selection.

ADD0	ADD1	ADDRESS
GND	GND	0x48
OPEN	GND	0x49
VCC	GND	0x4A
GND	OPEN	0x4B
OPEN	OPEN	0x4C
VCC	OPEN	0x4D
GND	VCC	0x4E
OPEN	VCC	0x4F
VCC	VCC	0x50

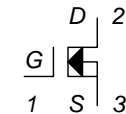


Fan Header

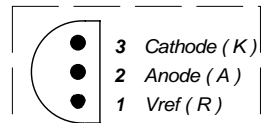


AMP640456-3

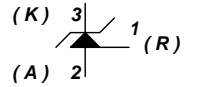
TO-263 / TO-252



Top View



TL431



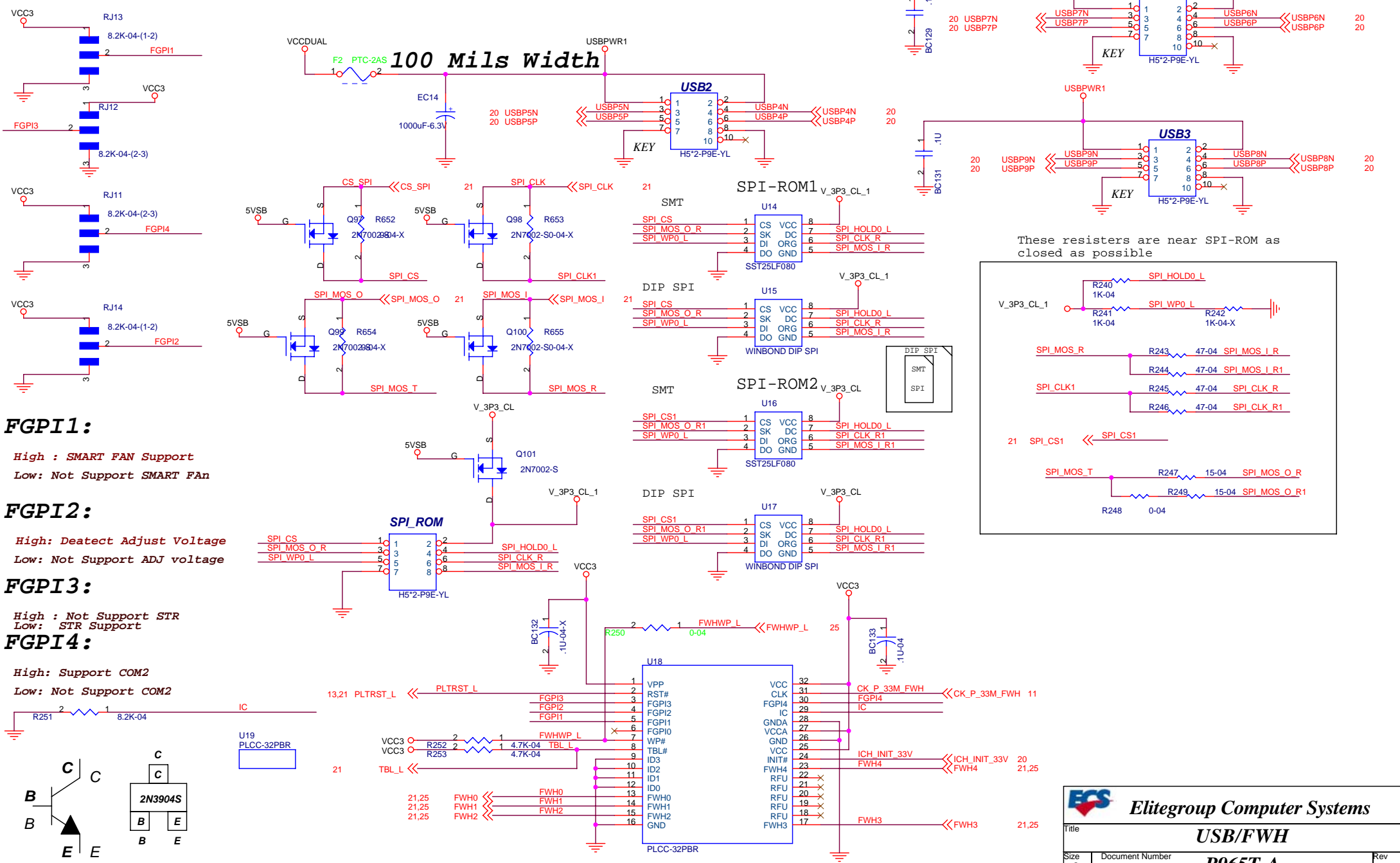
Elitegroup Computer Systems

Title SST W83L772G

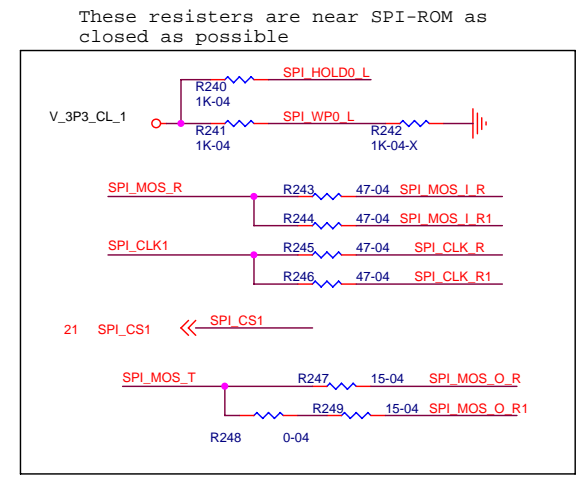
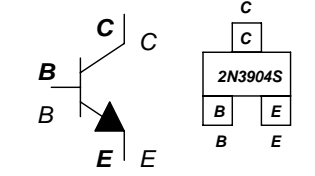
Size Custom Document Number P965T-A Rev 1.0B

Date: Tuesday, June 20, 2006 Sheet 23 of 43

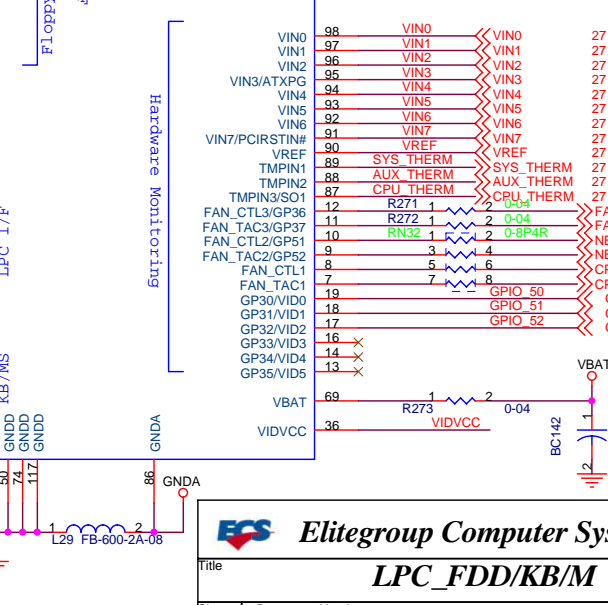
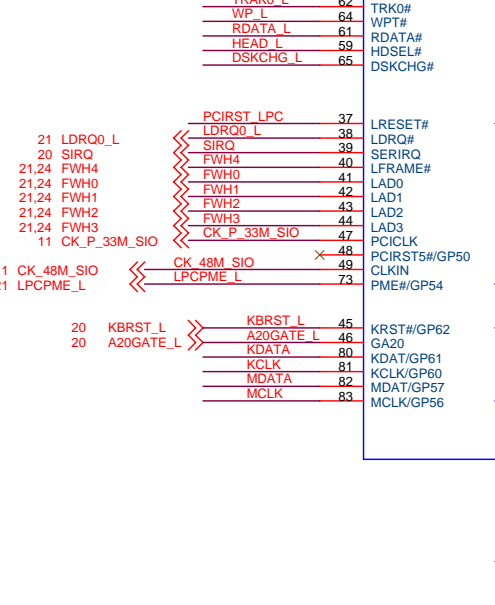
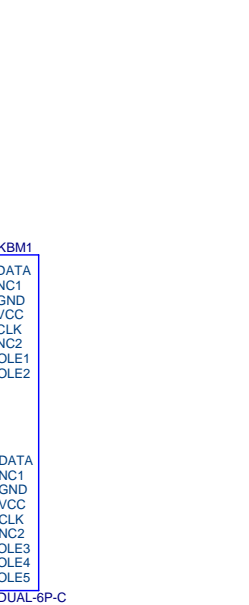
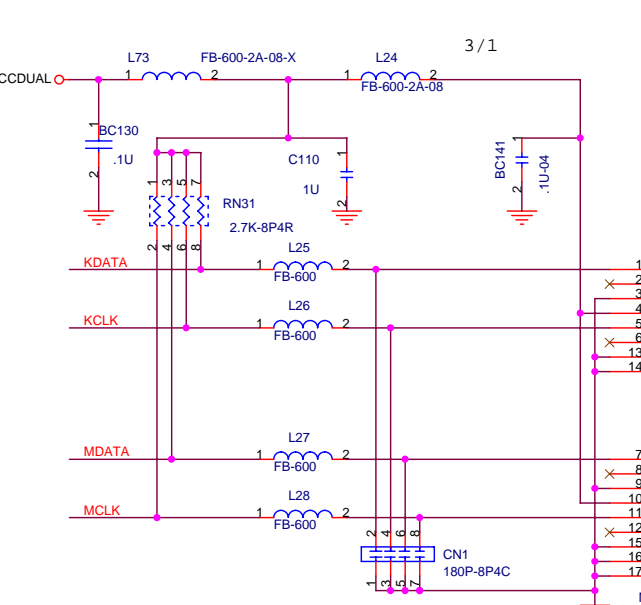
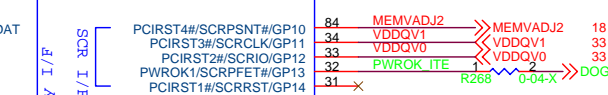
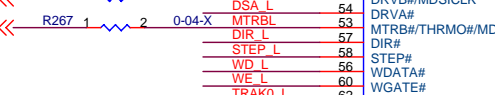
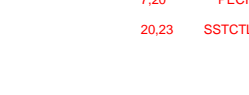
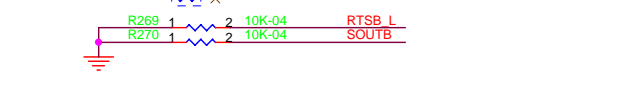
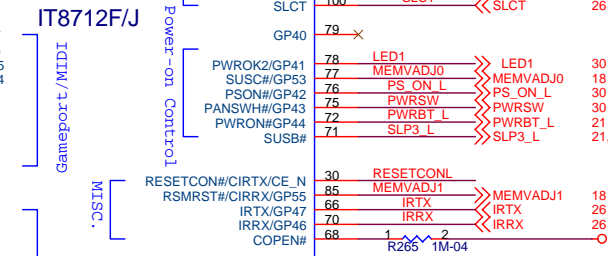
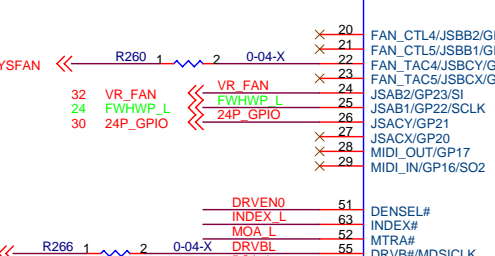
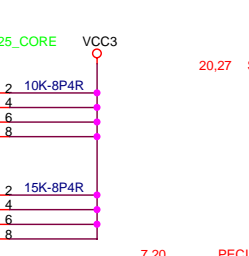
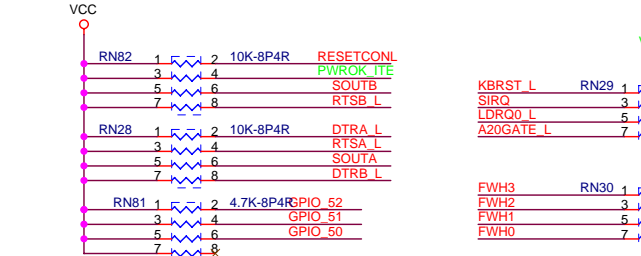
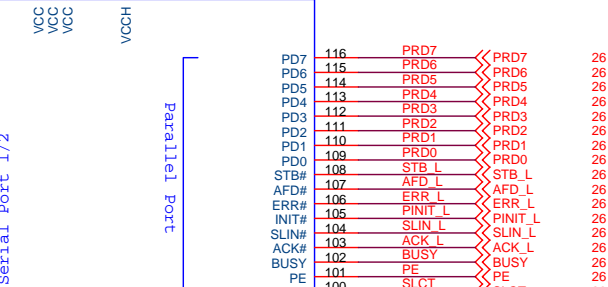
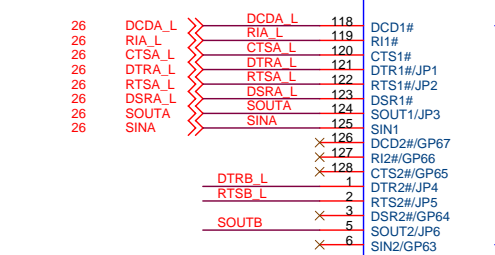
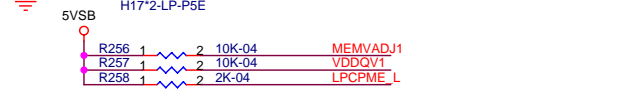
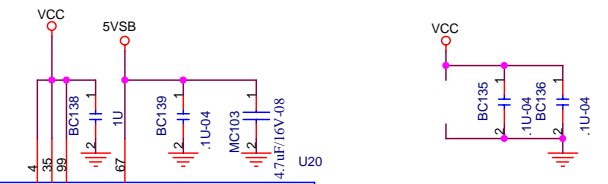
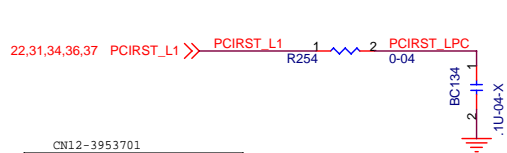
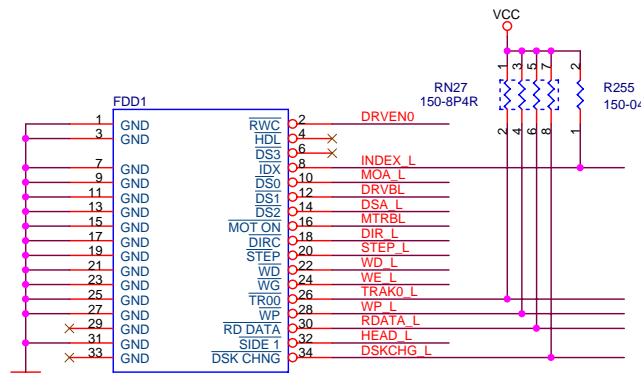
USB PORT INTERFACE



- FGPI1:**
High : SMART FAN Support
Low: Not Support SMART FAN
- FGPI2:**
High: Deatetect Adjust Voltage
Low: Not Support ADJ voltage
- FGPI3:**
High : Not Support STR
Low: STR Support
- FGPI4:**
High: Support COM2
Low: Not Support COM2



USB/FWH		
Title Custom	Document Number P965T-A	Rev 1.0B
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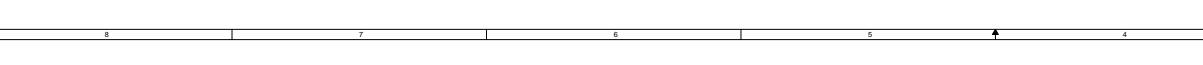
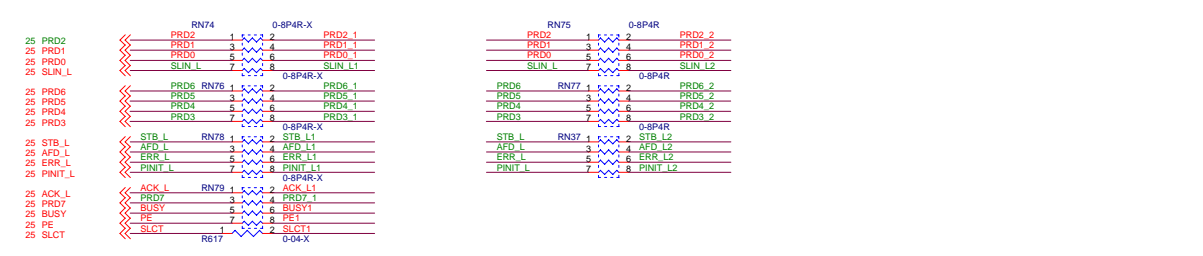
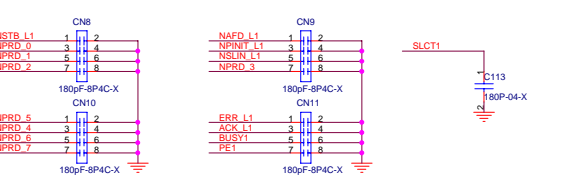
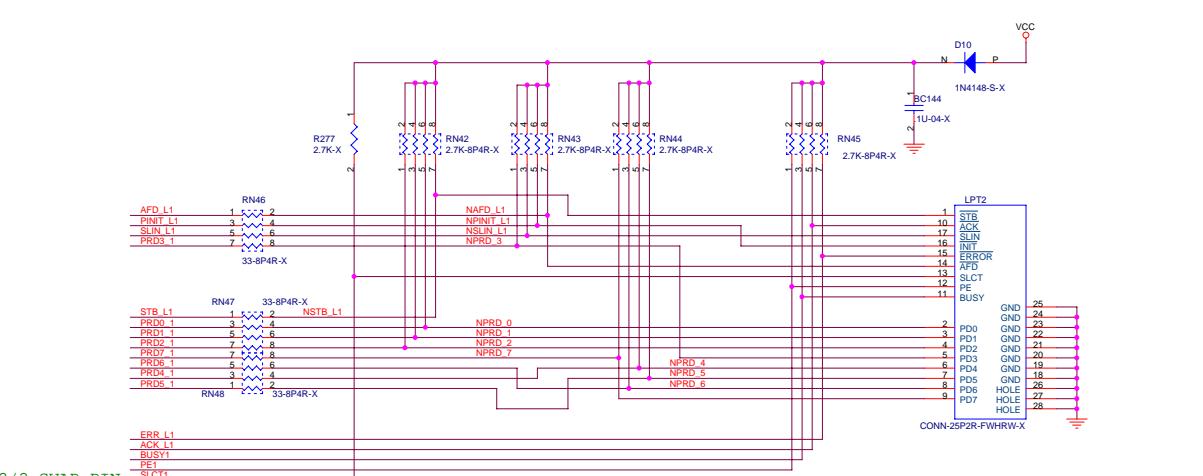
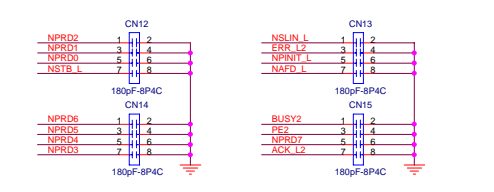
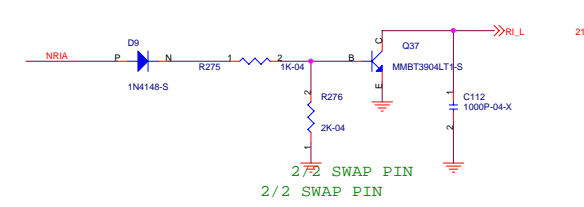
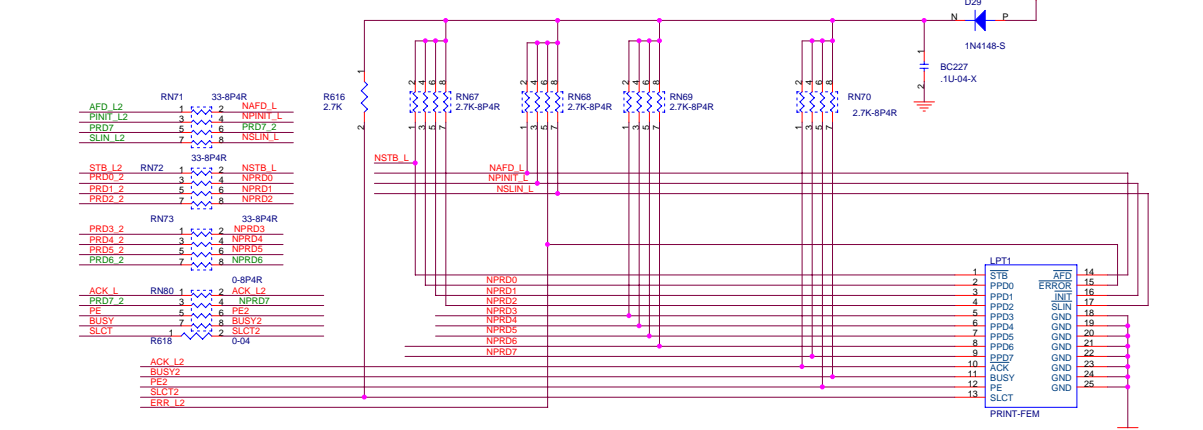
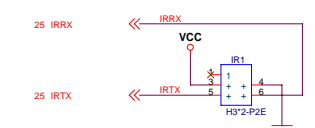
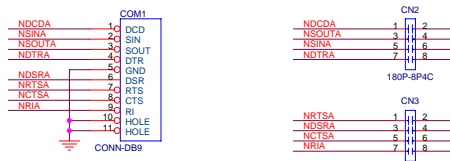
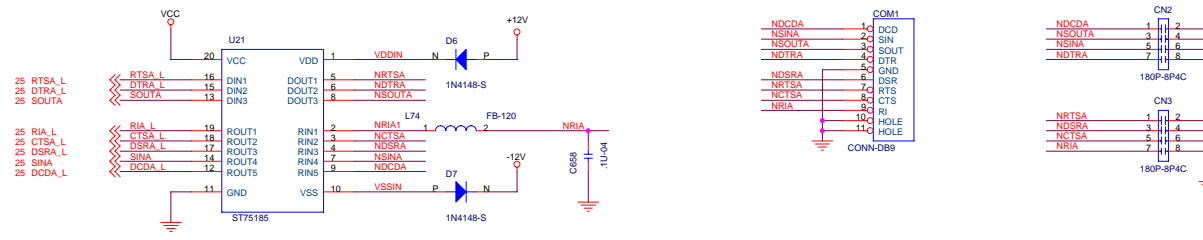


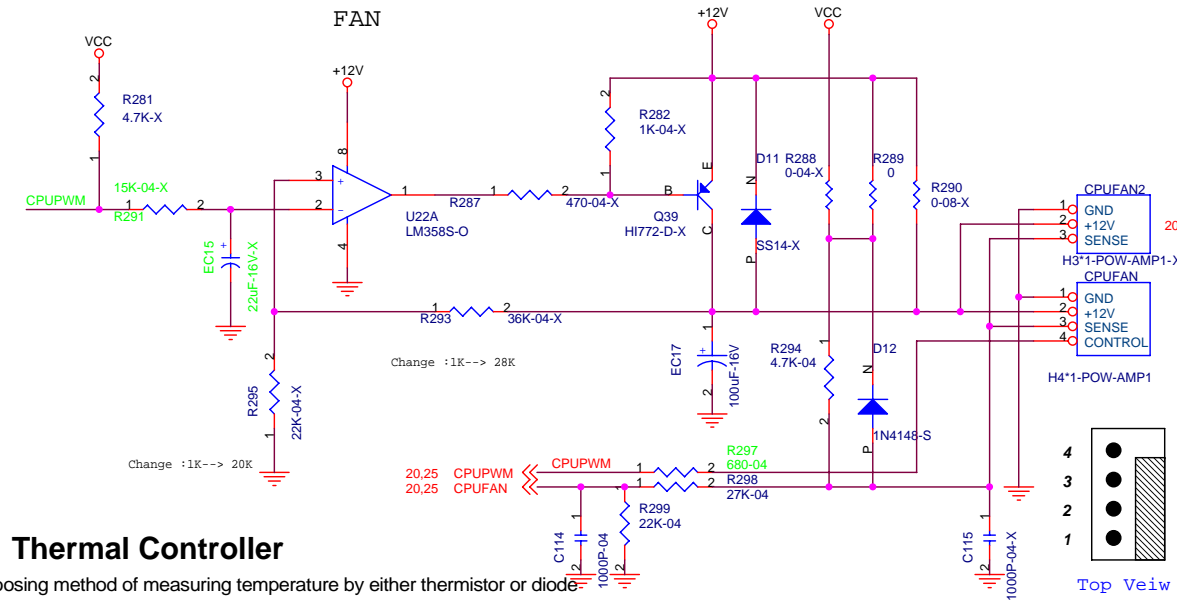
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File: **LPC_FDD/KB/M**

Size: Custom Document Number: **P965T-A** Rev: 1.0B

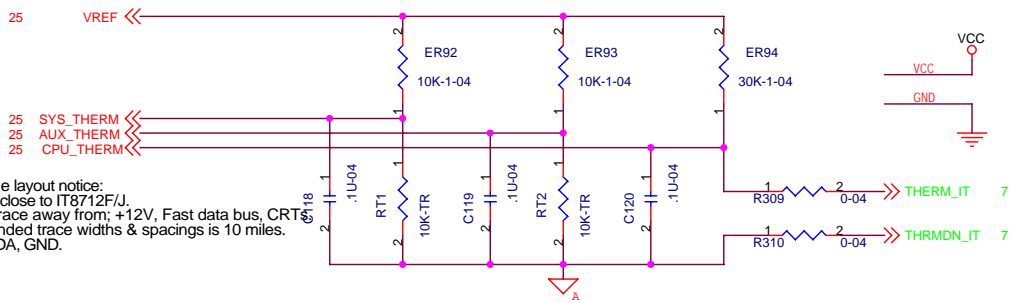
Date: Tuesday, June 20, 2006 Sheet: 25 of 43





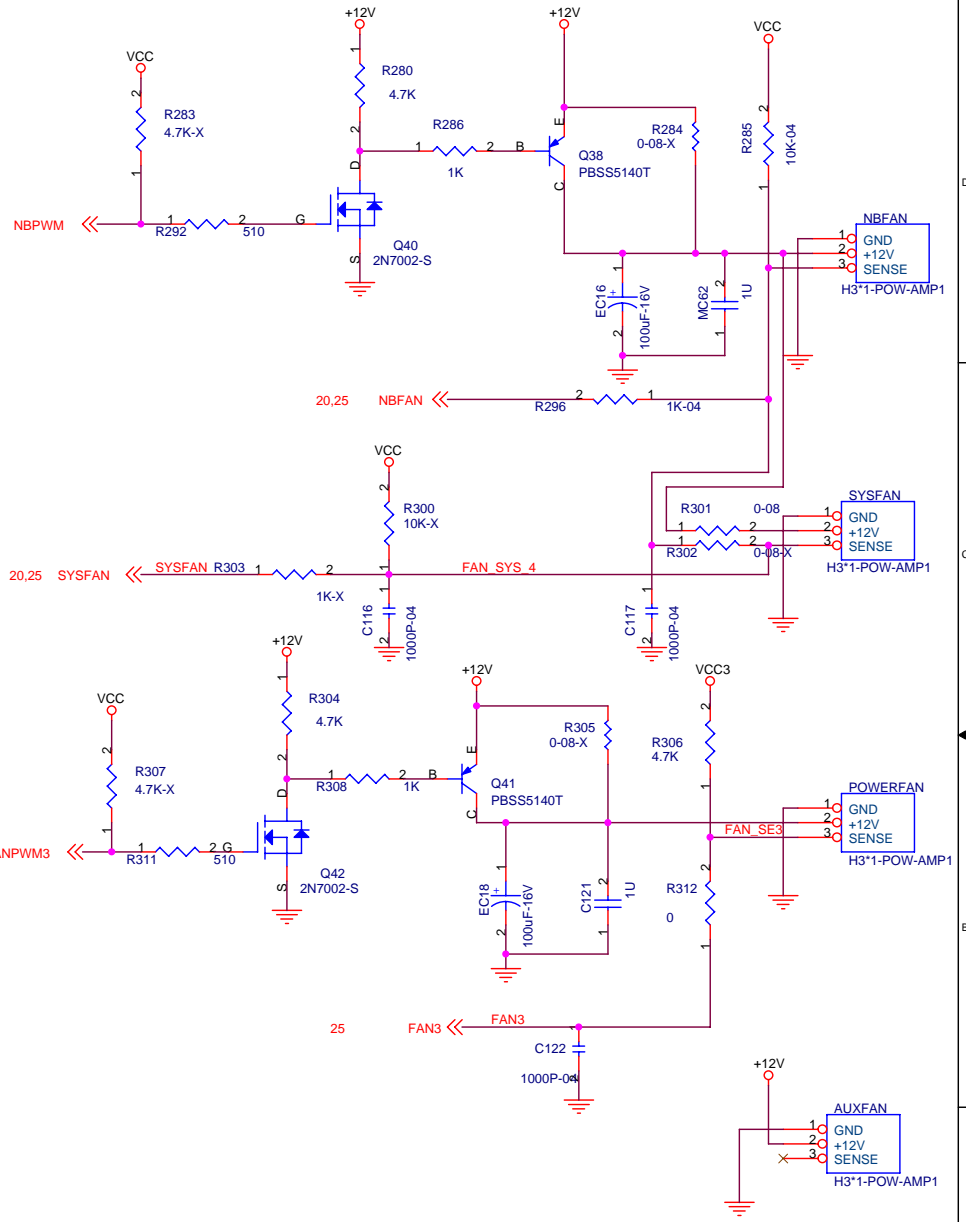
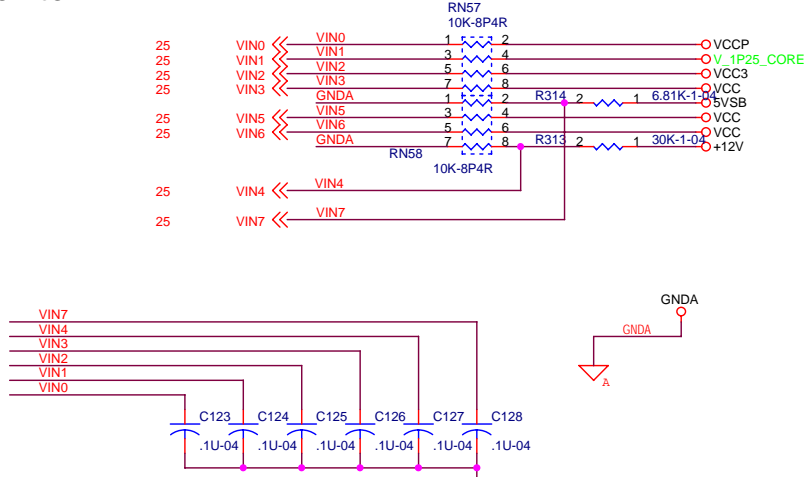
Thermal Controller

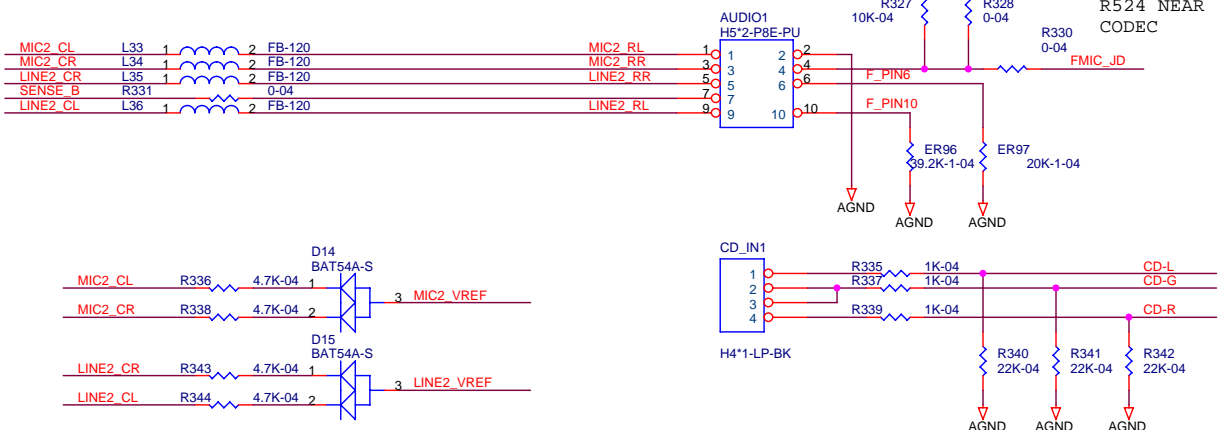
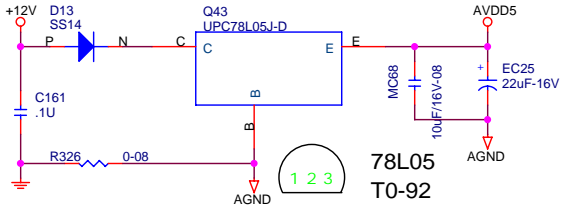
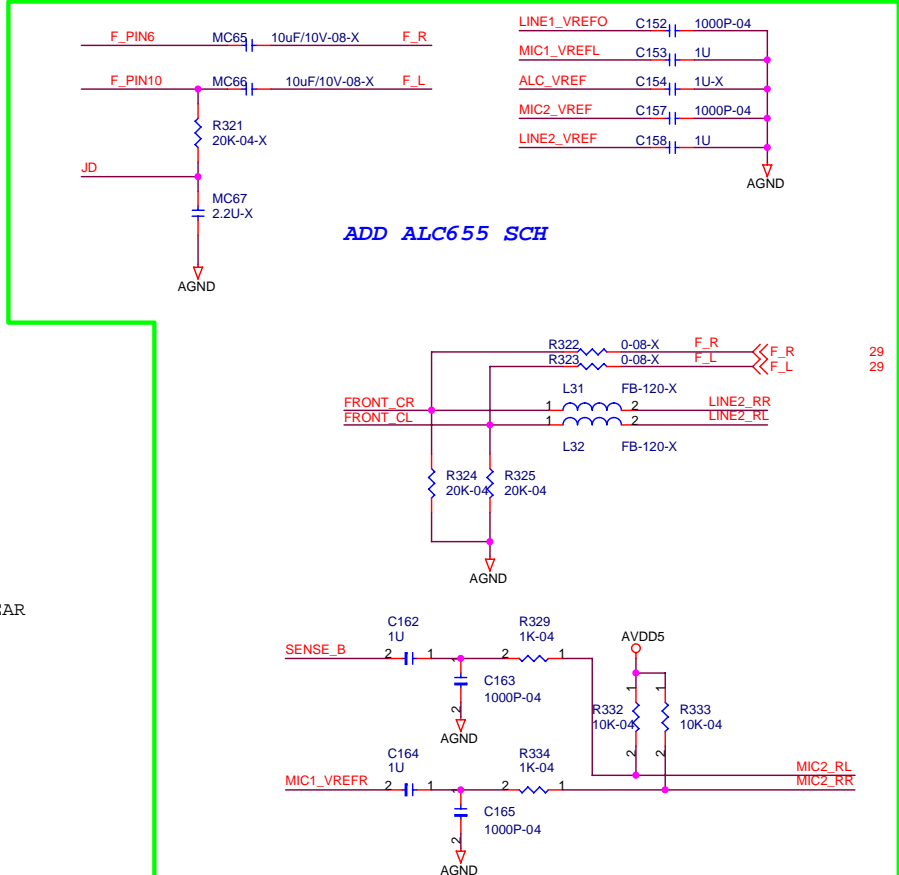
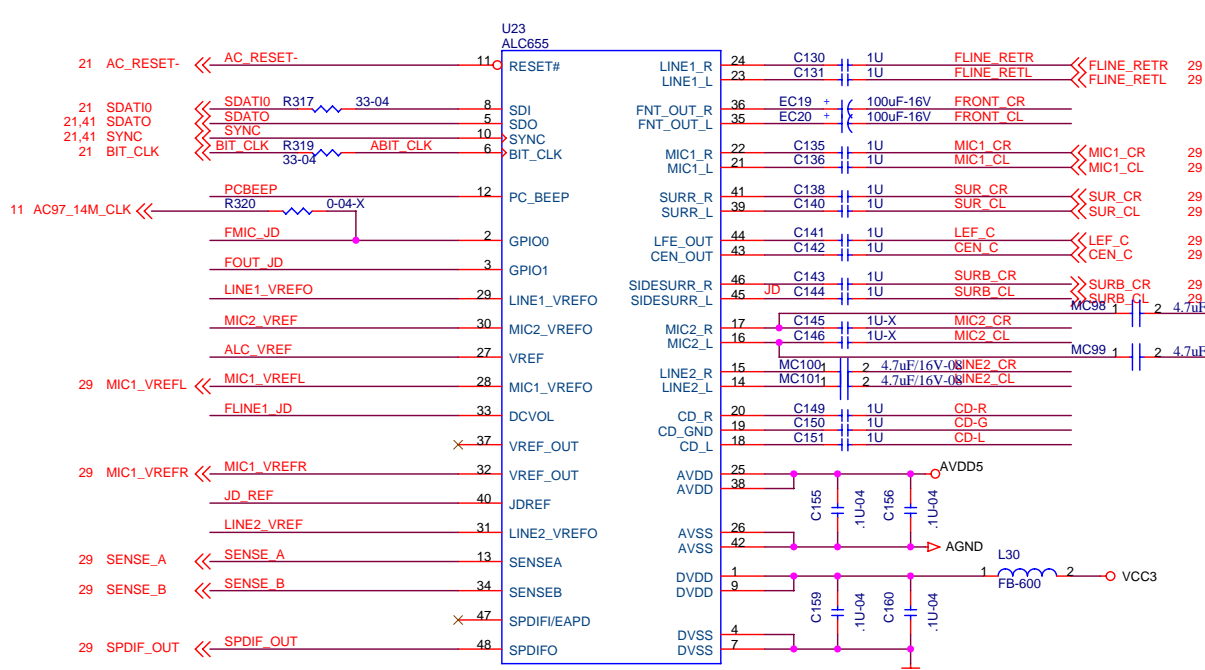
Choosing method of measuring temperature by either thermistor or diode

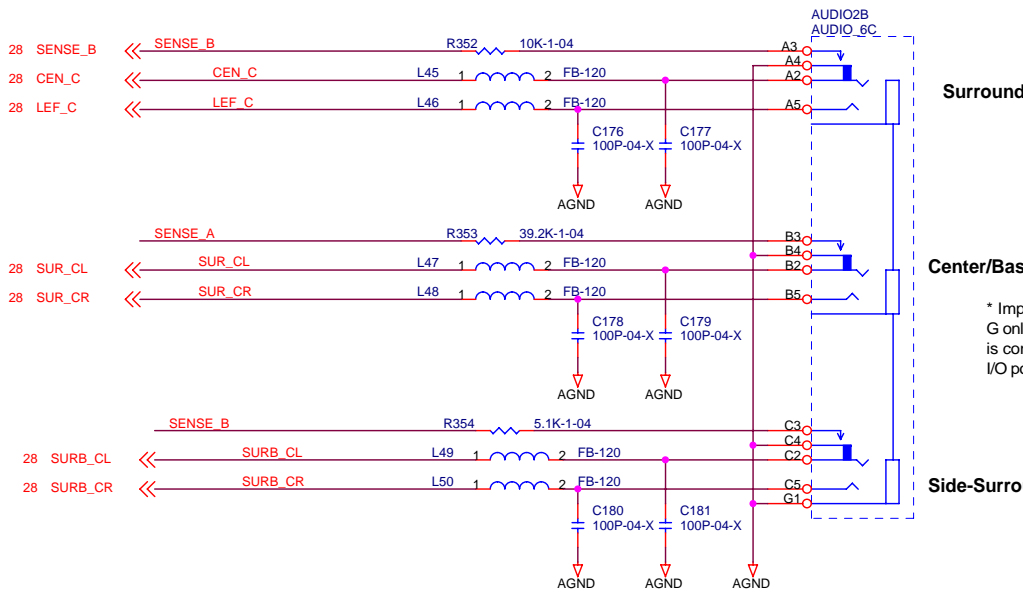
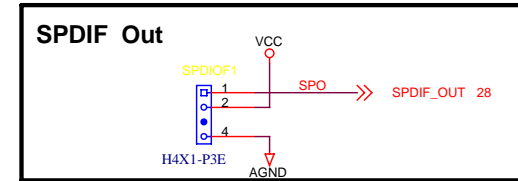
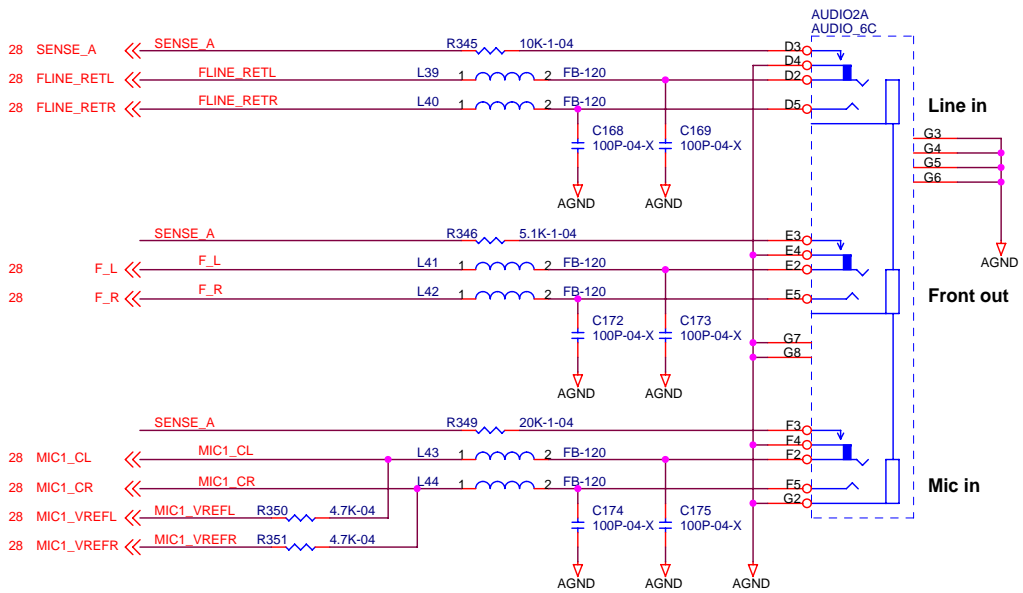


Thermal Diode layout notice:
 a. Place T.D. close to IT6712F/J.
 b. Keep the trace away from: +12V, Fast data bus, CRT.
 c. Recommended trace widths & spacings is 10 miles.
 d. Isolate GNDA, GND.

Voltage Monitor

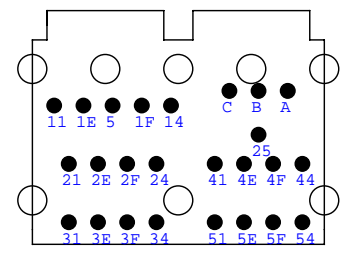
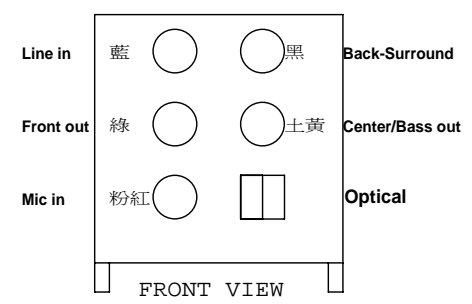






* Implement Block G only if PORT-G is configured as I/O port

* Implement Block H only if PORT-H is configured as I/O port

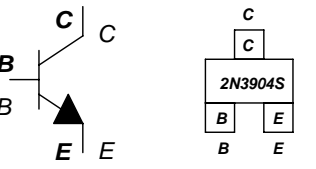
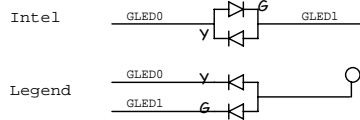
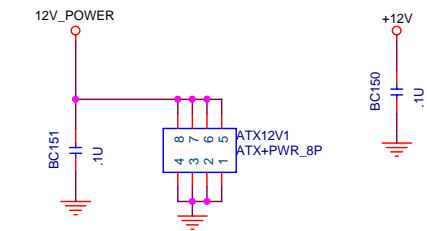
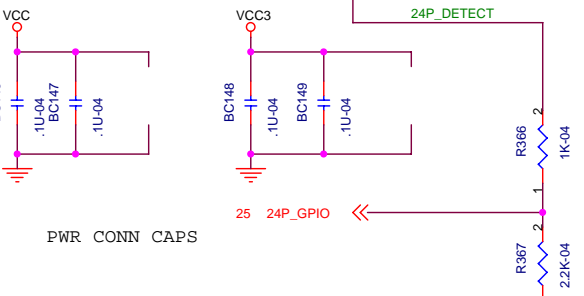
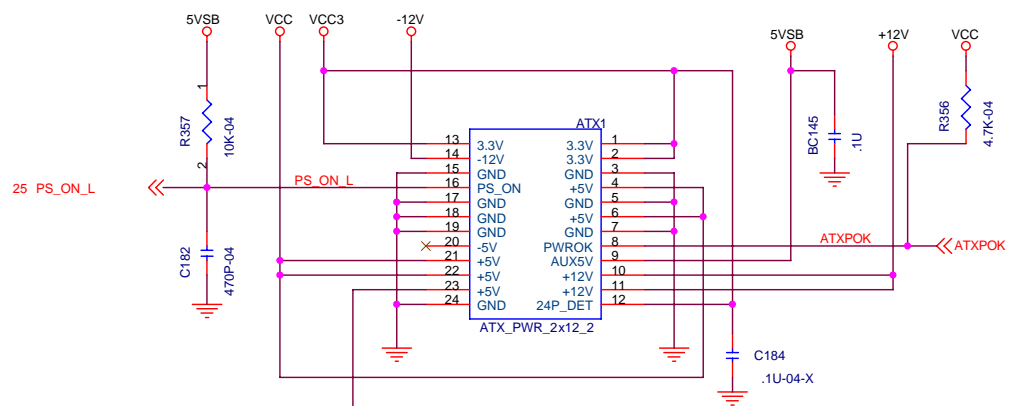


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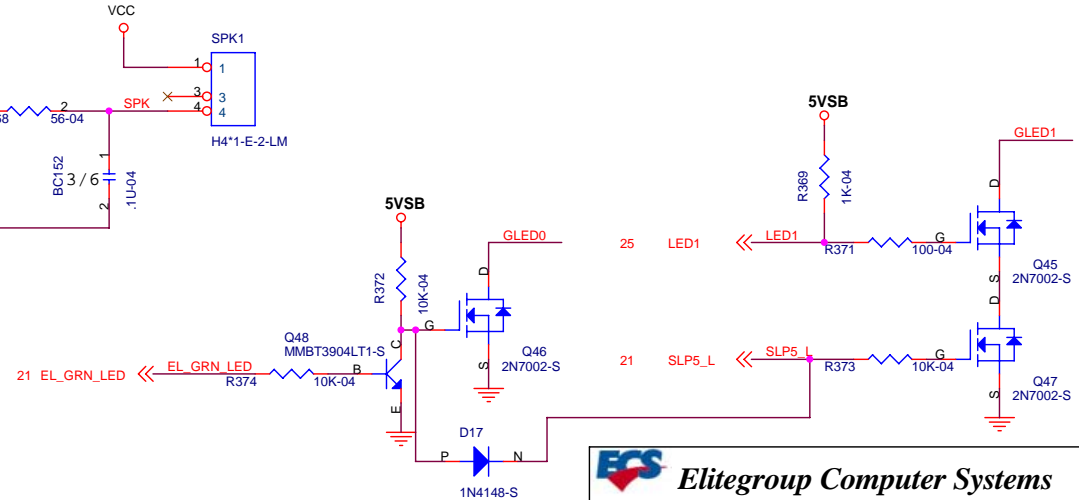
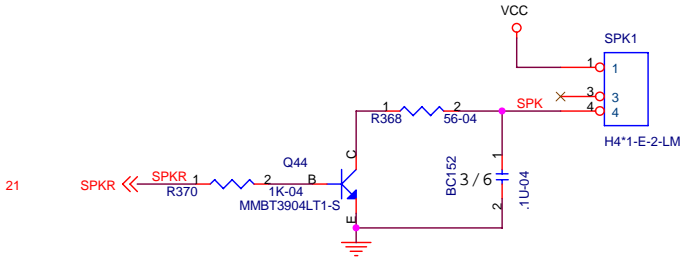
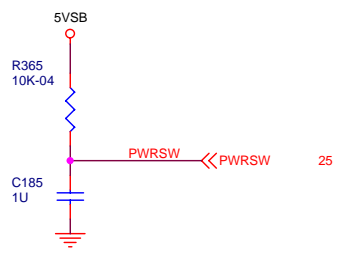
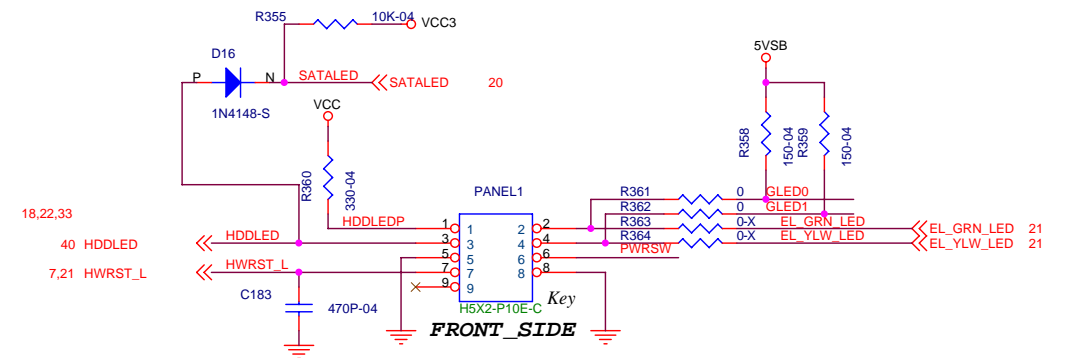
Title: **Audio Connector**

Size: Custom | Document Number: **P965T-A** | Rev: 1.0B

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	S0	S1	S3	S4,S5
PANEL1(4,2)	Green	G-blinking	Y-blinking	Dark
LPANEL1(3,5,7)	Green	G-blinking	G-blinking Yellow	Dark
LSJ1(1,2)	Dark	Dark	Light	Dark
SJ1(1,3)(2,3)	Light	Blinking	Blinking	Dark
GLED0	HIGH	HIGH	LOW	HIGH
GLED1	LOW	SWITCH	SWITCH	HIGH

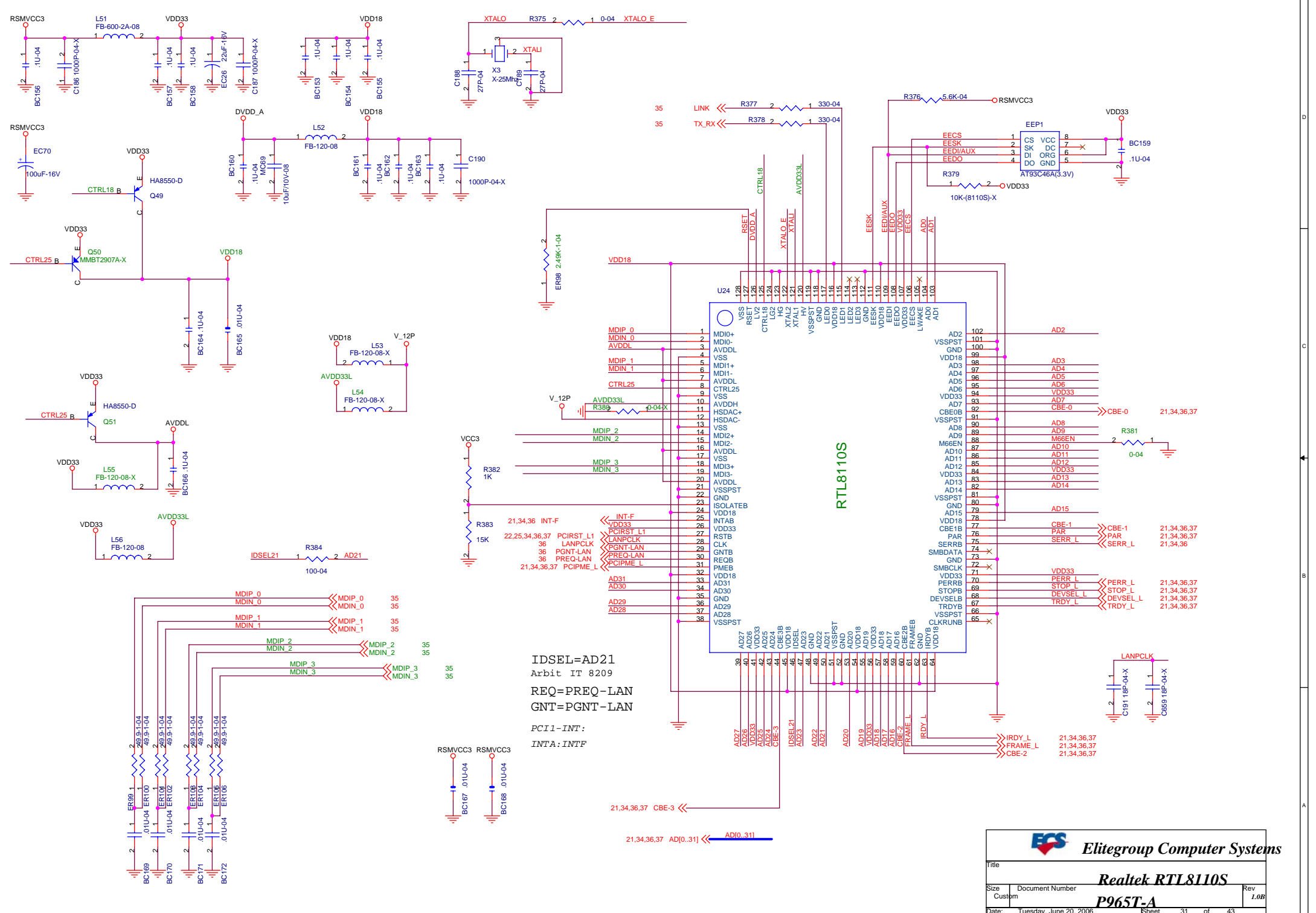


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Title: **ATX Power & Front Panel**

Size B | Document Number: **P965T-A** | Rev: **1.0B**

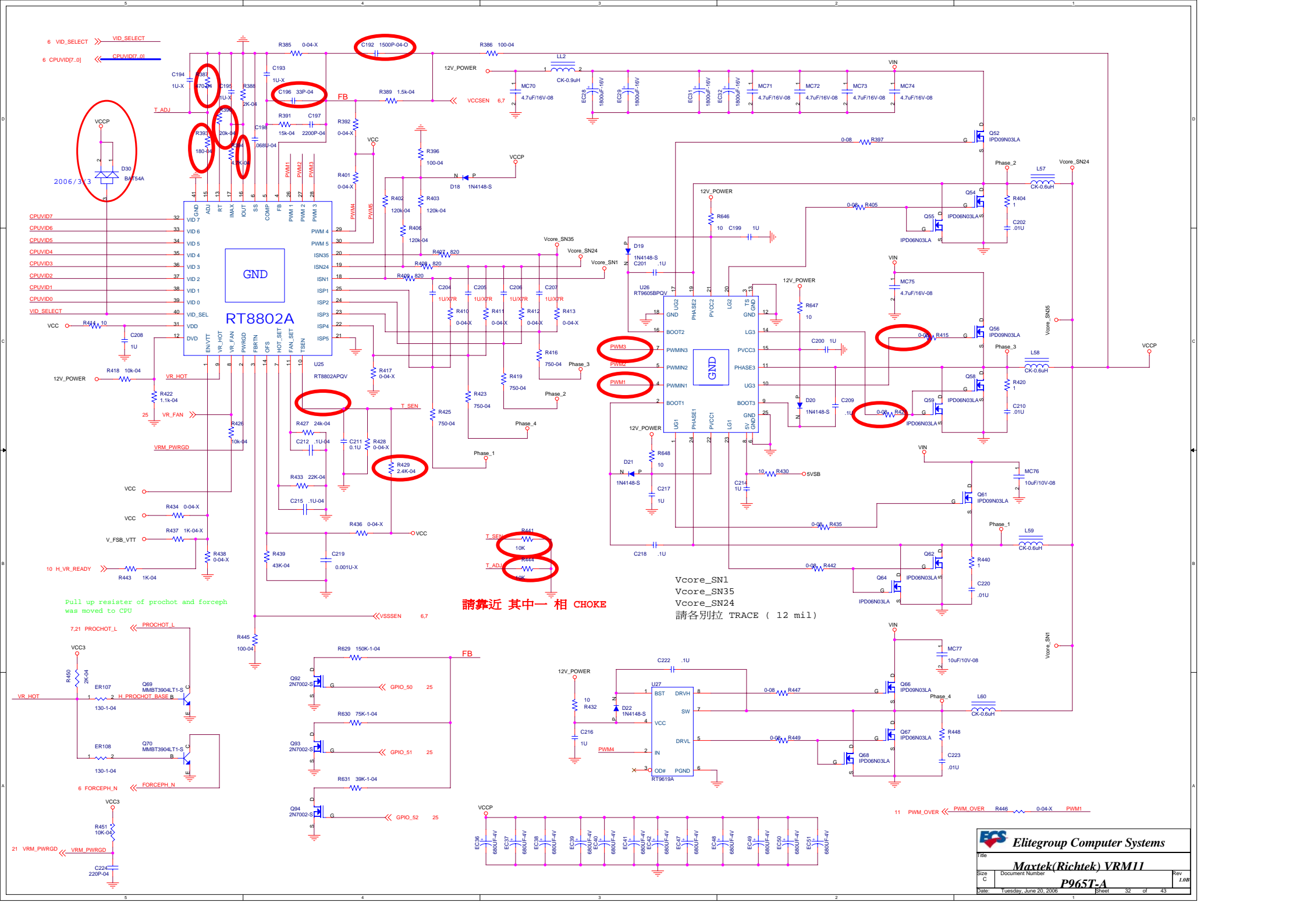
Date: Tuesday, June 20, 2006 | Sheet: 30 of 43



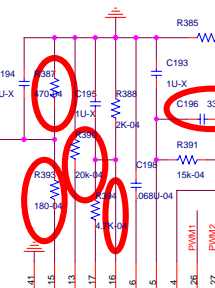
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 Arbit IT 8209
 REQ=PREQ-LAN
 GNT=PGNT-LAN

PCI1-INT:
 INTA:INTF

Realtek RTL8110S		
P965T-A		
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6 VID_SELECT >> VID_SELECT
6 CPUVID7..0 << CPUVID7..0



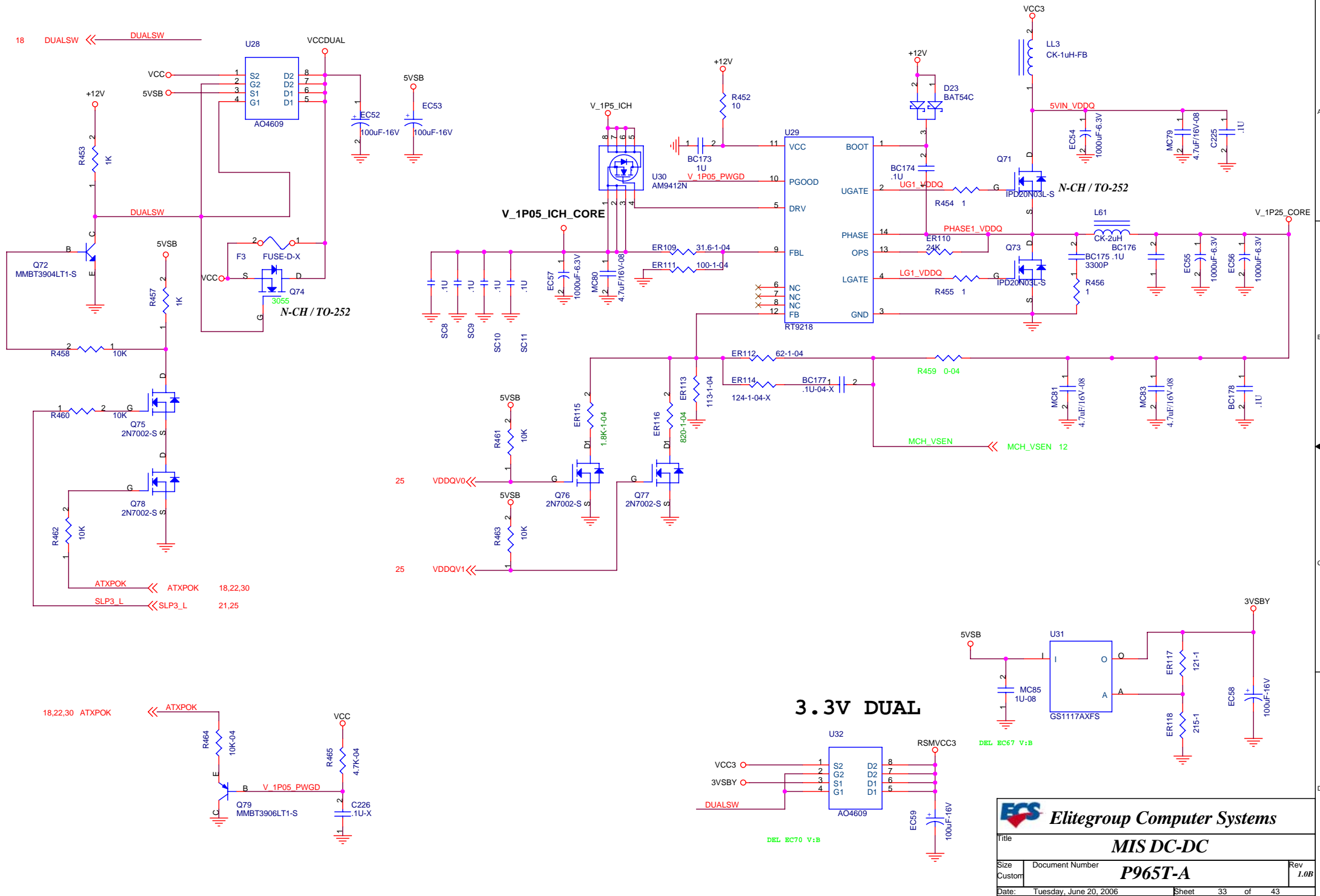
GND

RT8802A

RT8802APQV

請靠近 其中一相 CHOKE

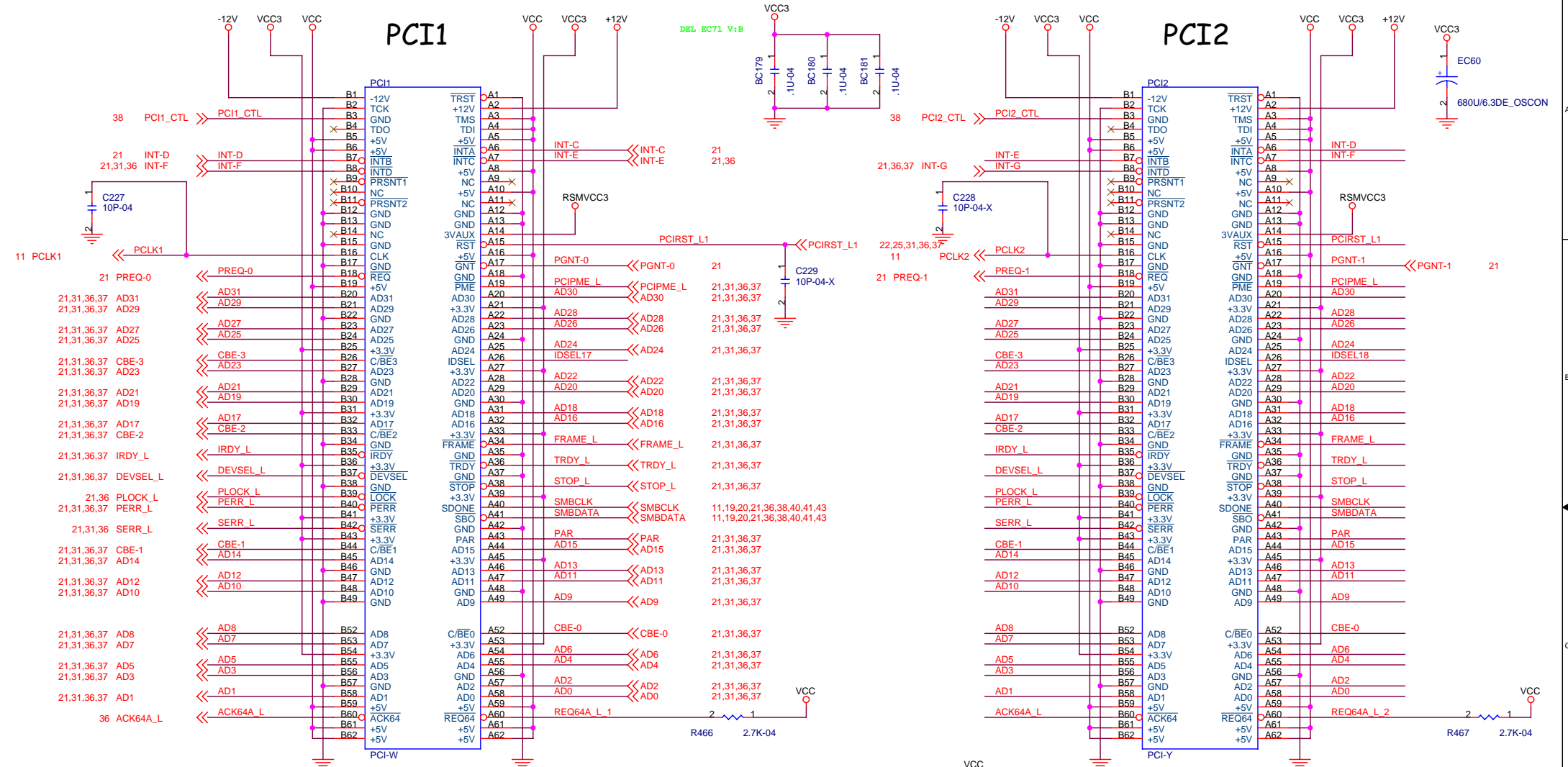
Vcore_SN1
Vcore_SN35
Vcore_SN24
請各別拉 TRACE (12 mil)



ECS Elitegroup Computer Systems

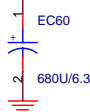
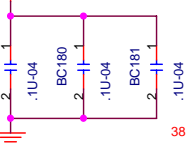
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Size: Custom	Document Number: P965T-A	Rev: 1.0B
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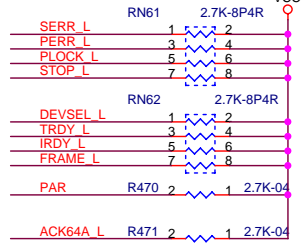
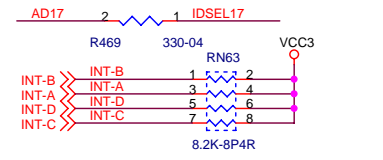


DEL EC71 V:B

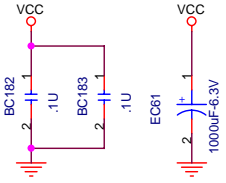
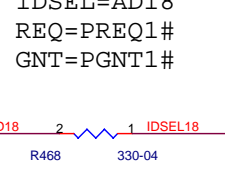
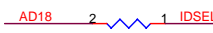
R466 2.7K-04



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 INTA: INT-C
 INTB: INT-D
 INTC: INT-E
 INTD: INT-F



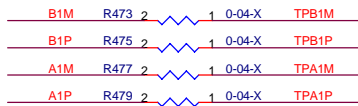
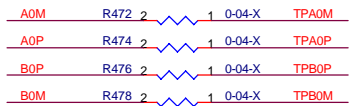
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 INTB: INT-E
 INTC: INT-F
 INTD: INT-G



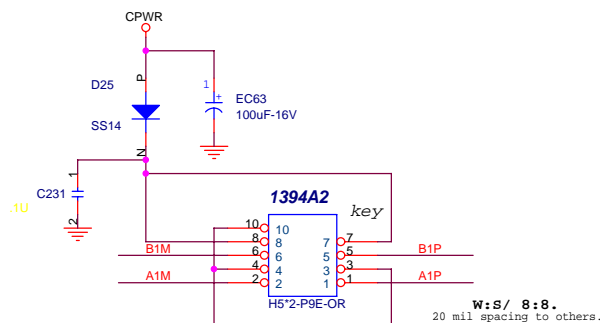
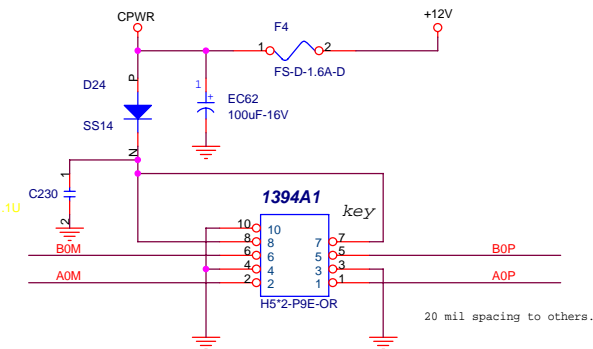
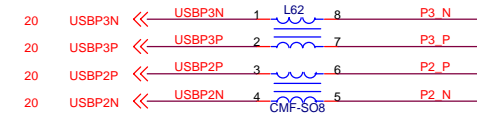
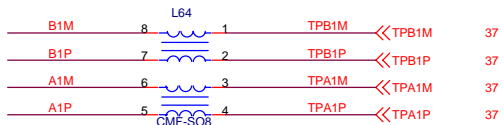
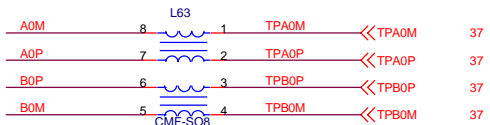
Elitegroup Computer Systems

Title: **PCI Slot 1&2**

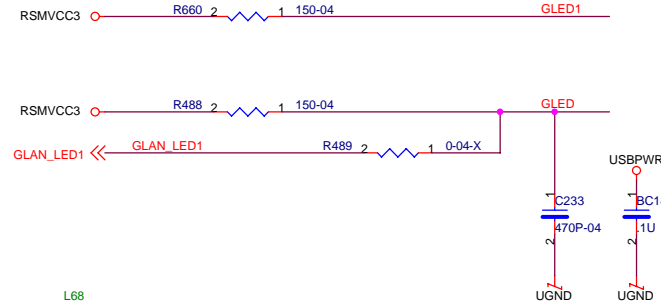
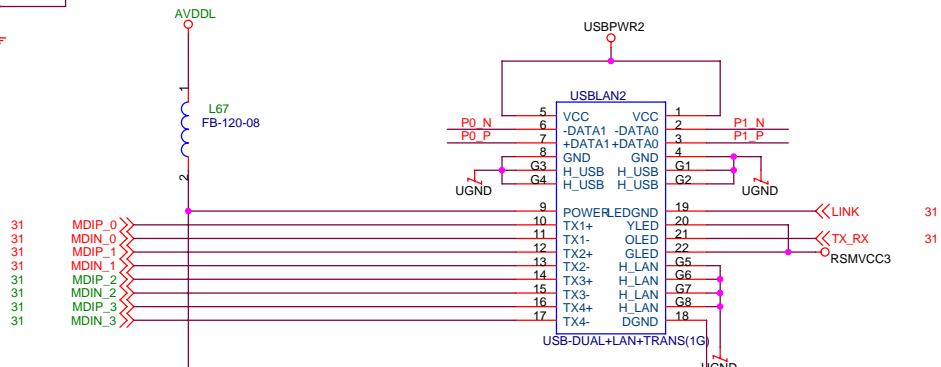
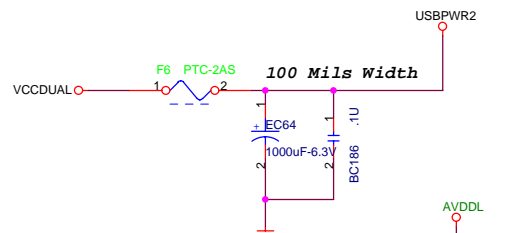
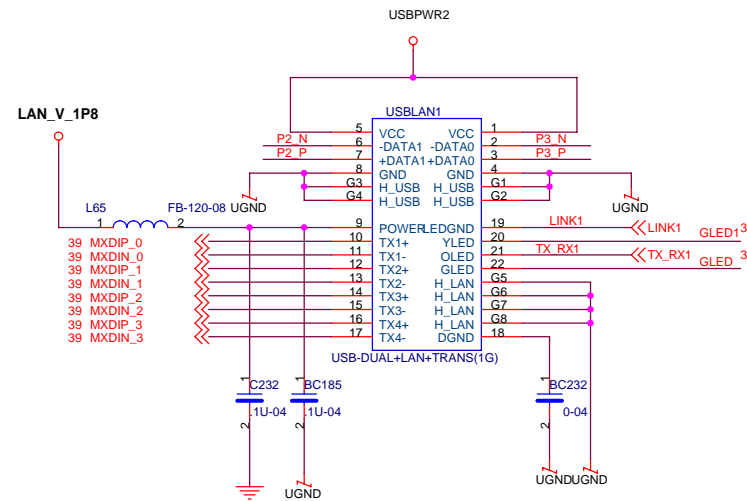
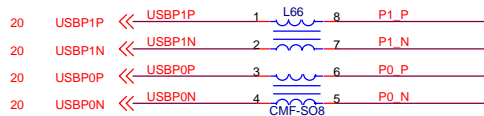
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REAR_SIDE



REAR_SIDE



Elitegroup Computer Systems

Title: **Back I/O**

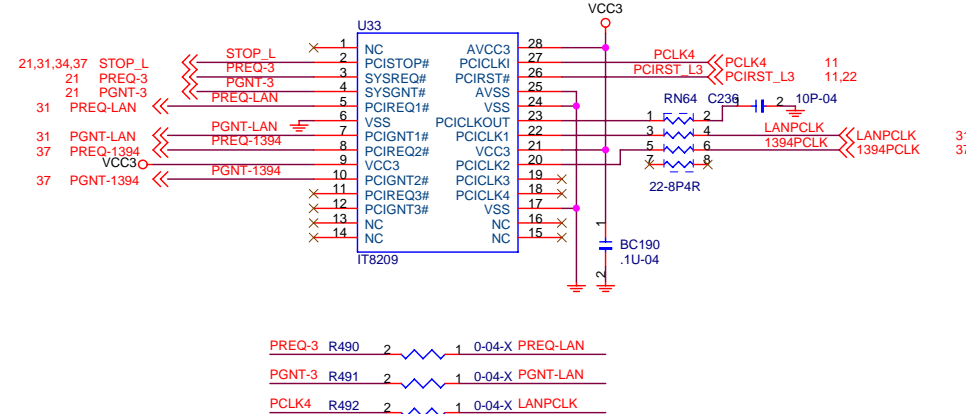
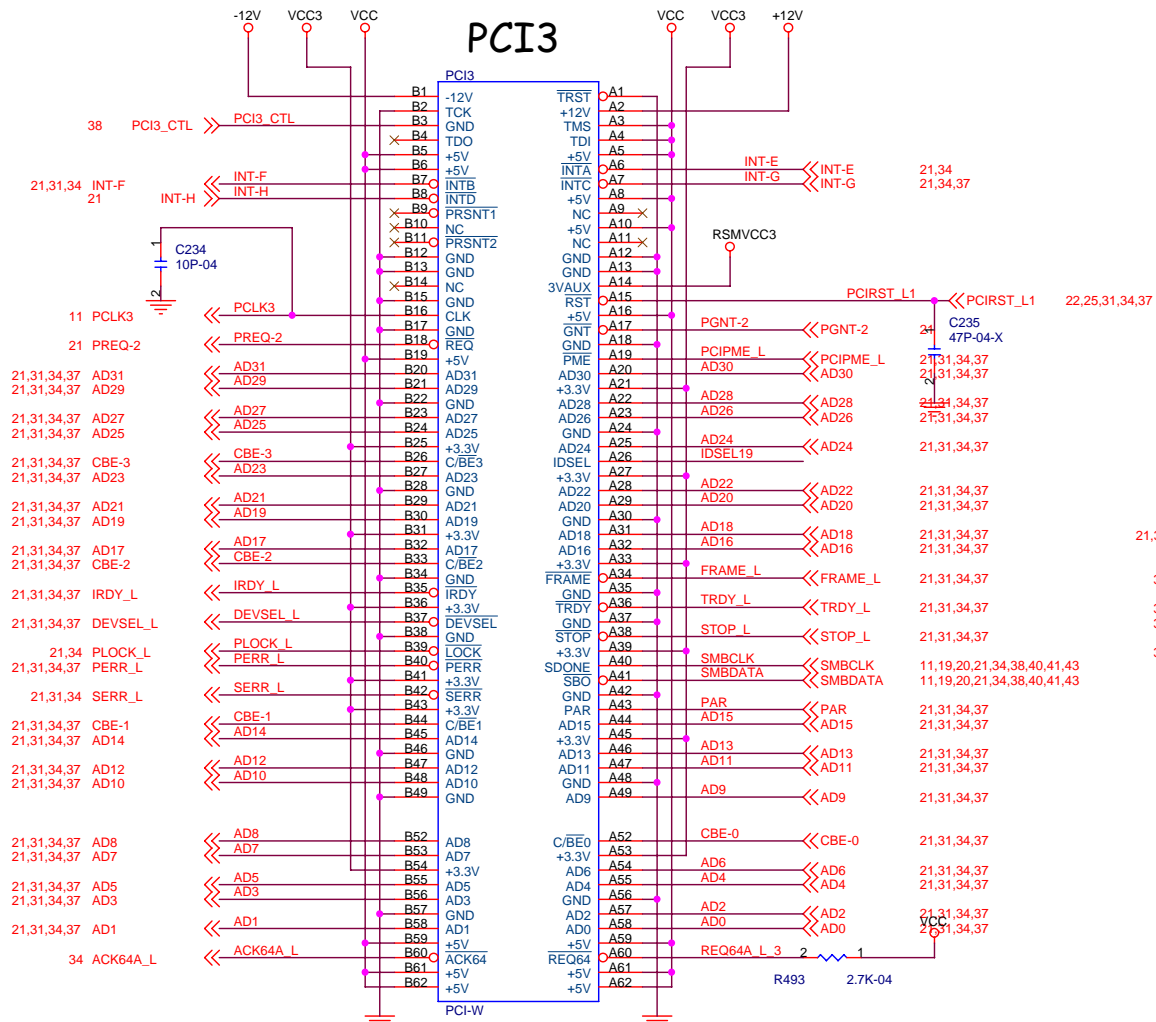
Size: Custom Document Number

Date: Tuesday, June 20, 2006

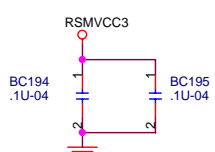
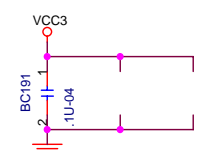
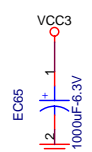
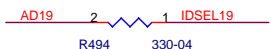
Sheet: 35 of 43

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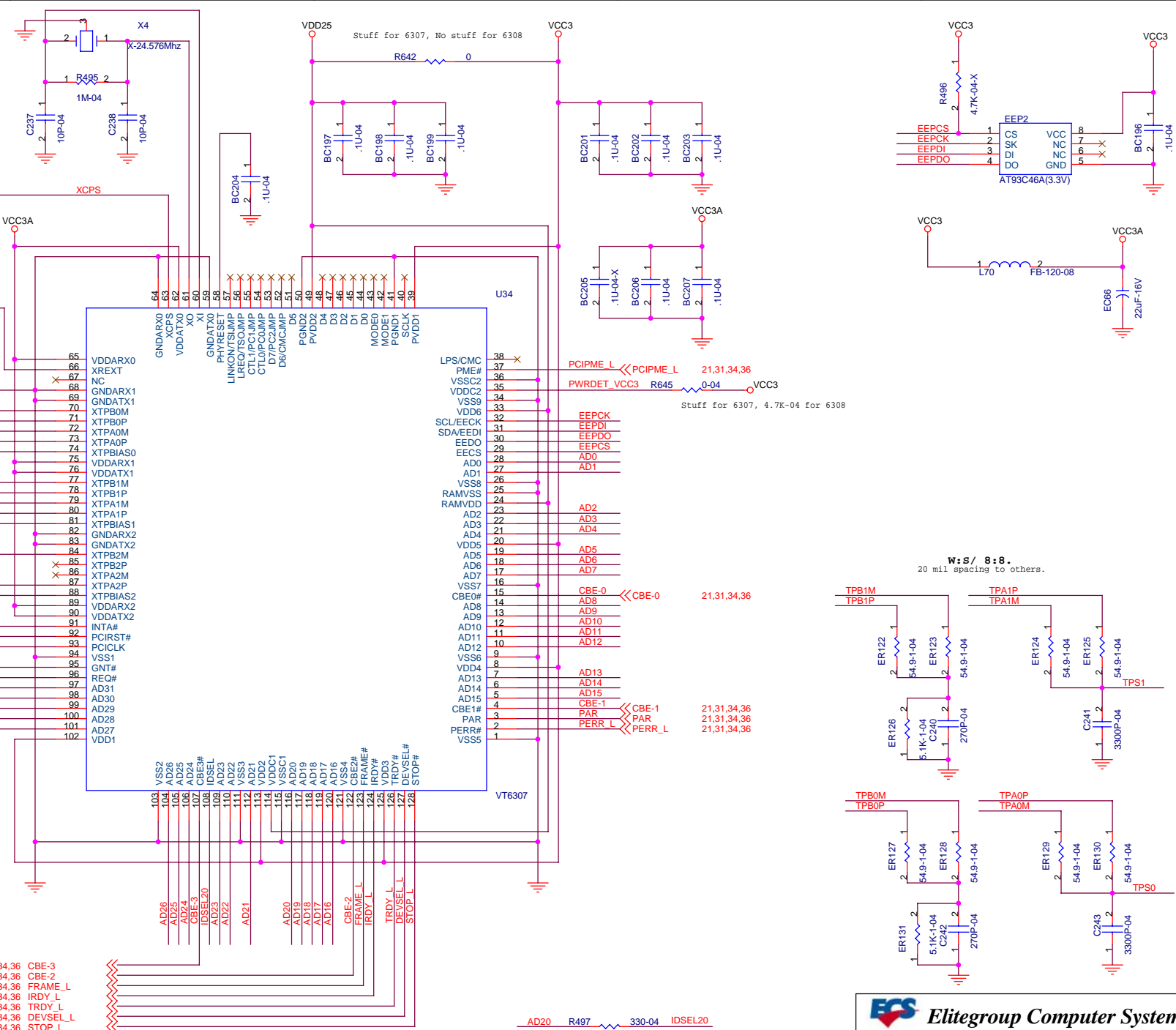
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 INTA: INTE REQ=PREQ2#
 INTB: INTF GNT=PGNT2#
 INTC: INTG
 INTD: INTH



ECS		Elitegroup Computer Systems	
Title PCI Slot 3			
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21,31,34,36 AD[0..31]

AD[0..31]



35 TPB0M
35 TPB0P
35 TPA0M
35 TPA0P

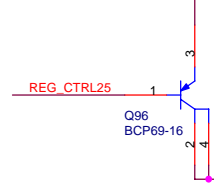
35 TPB1M
35 TPB1P
35 TPA1M
35 TPA1P

Stuff for 6308, No stuff for 6307
VCC3 R643 4.7K-04-X BJT_SEL
Stuff for 6308, No stuff for 6307
VDD25 R644 0-04-X REG_CTRL25

21,34,36 INT-G
22,25,31,34,36 PCIRST_L1
36 1394PCLK
36 PGNT-1394
36 PREQ-1394

IDSEL=AD20
Arbit IT 8209
REQ=PREQ-1394
GNT=PGNT-1394

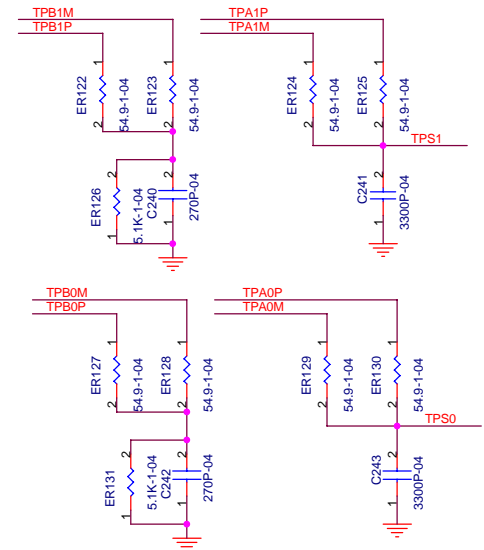
PCI1-INT:
INTA:INTG



21,31,34,36 CBE-3
21,31,34,36 CBE-2
21,31,34,36 FRAME_L
21,31,34,36 IRDY_L
21,31,34,36 TRDY_L
21,31,34,36 DEVSEL_L
21,31,34,36 STOP_L

AD20 R497 330-04 IDSEL20

W:5/ 8:8.
20 mil spacing to others.



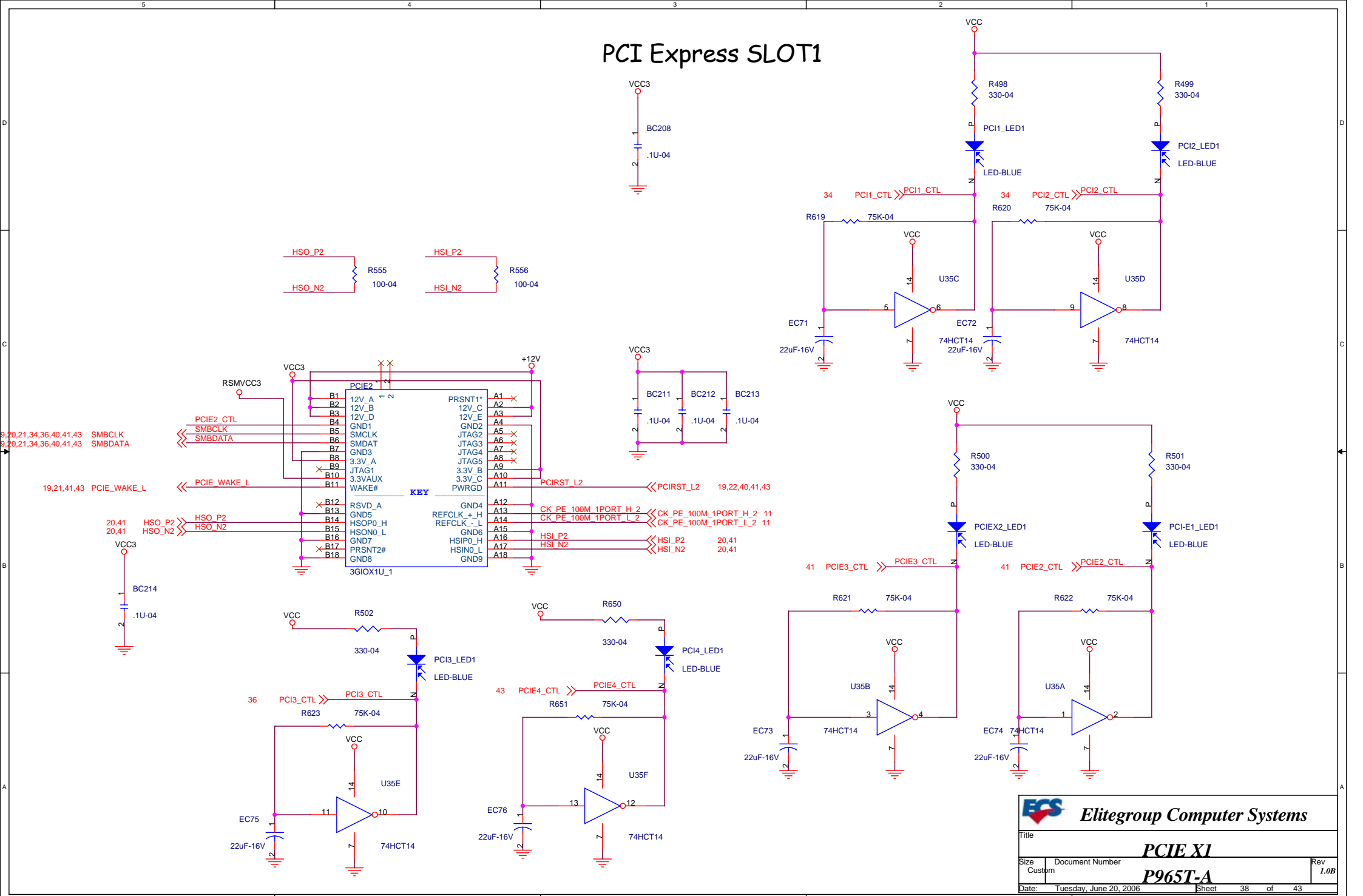
ECS Elitegroup Computer Systems

Title: **VT6307(1394)**

Size: Custom	Document Number: P965T-A	Rev: 1.0B
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Date: Tuesday, June 20, 2006 Sheet 37 of 43

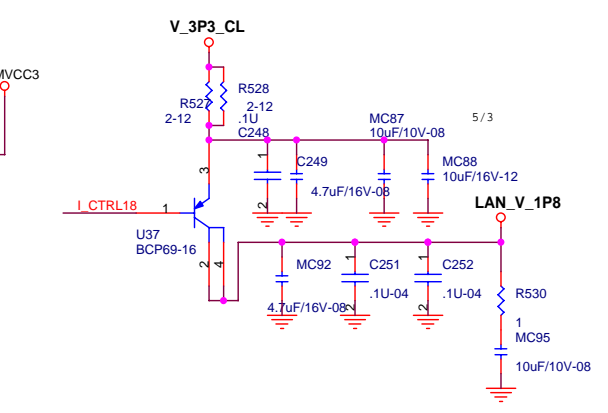
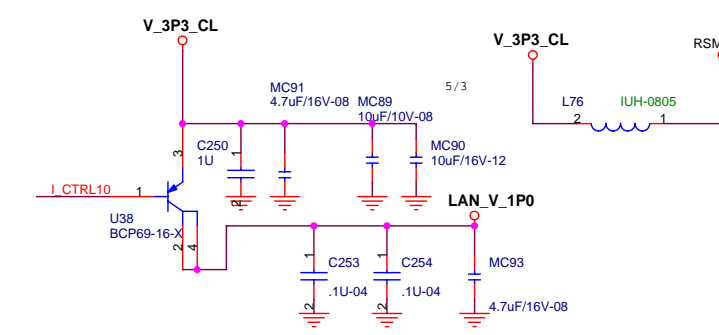
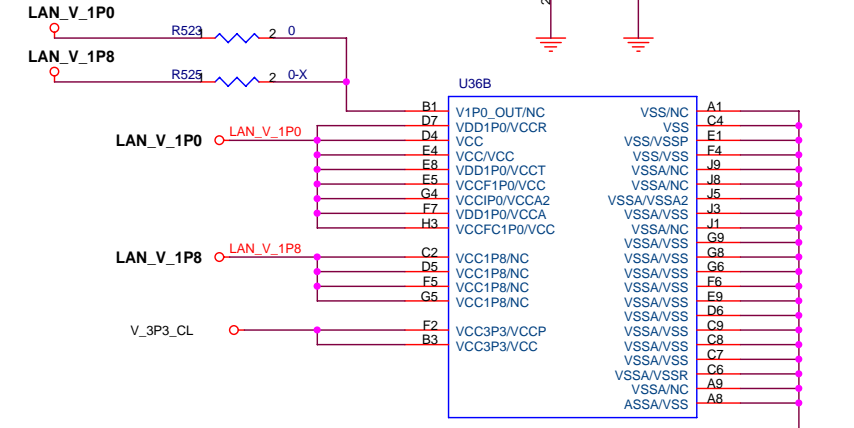
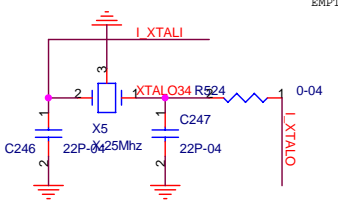
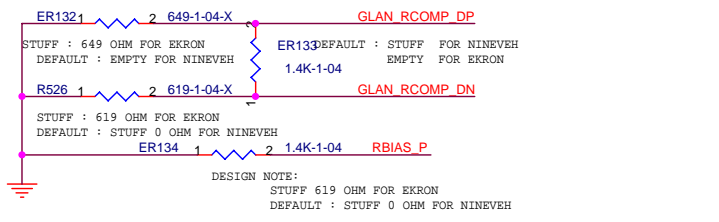
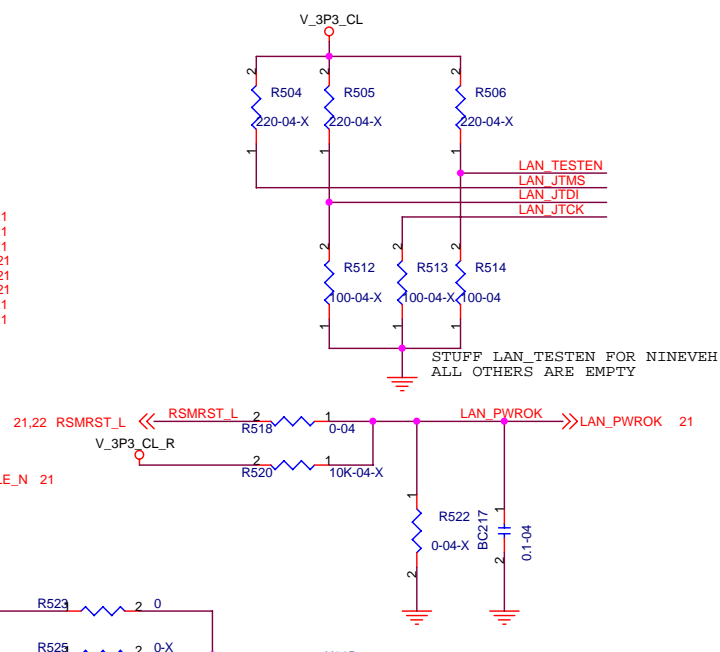
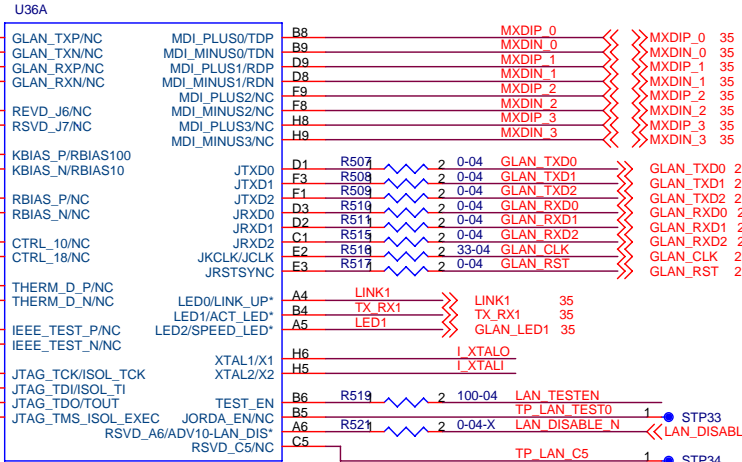
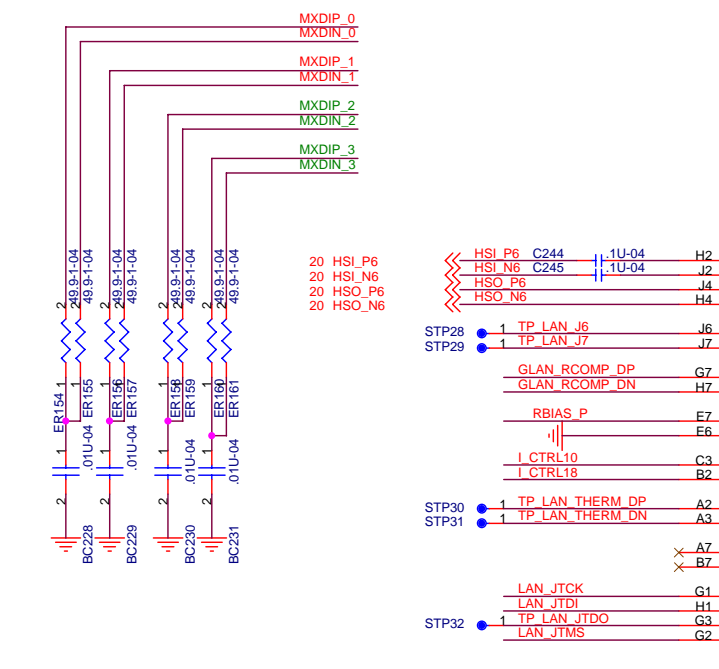
PCI Express SLOT1



Title		
PCIE X1		
Size	Document Number	Rev
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EKRON MODE SELECT OPTIONS: FOLLOW BELOW FOR RESISTOR STUFFING CONFIGURATION

	MODE 0	MODE 1	MODE 2
LAN_TESTEN	NOT SUPPORTED	0 (EXTERNAL)	1 (EXTERNAL)
LAN_JTCK	NOT SUPPORTED	0 (INTERNAL)	0 (EXTERNAL)
LAN_JTDI	NOT SUPPORTED	1 (EXTERNAL)	0 (EXTERNAL)
LAN_JTMS	NOT SUPPORTED	1 (EXTERNAL)	1 (EXTERNAL)

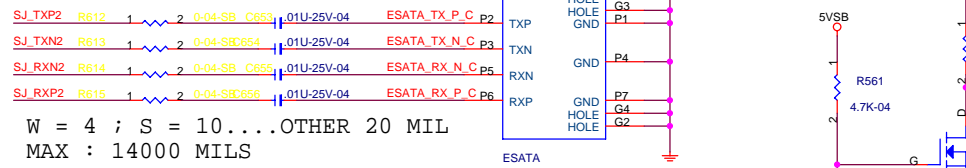


Elitegroup Computer Systems

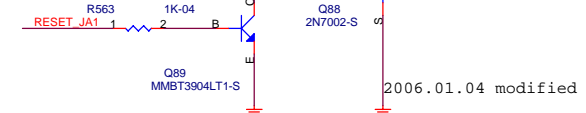
INTEL GLAN PHY

P965T-A

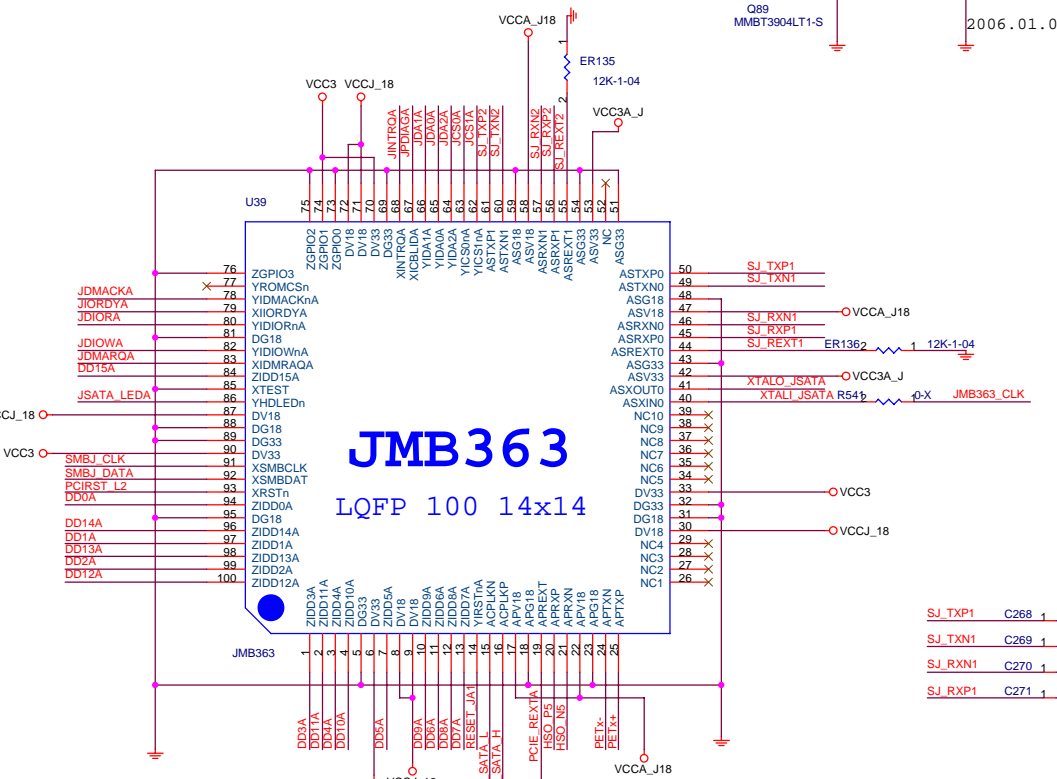
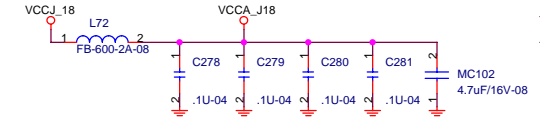
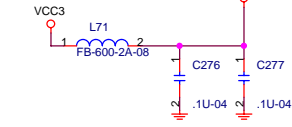
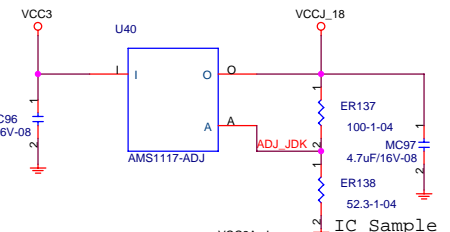
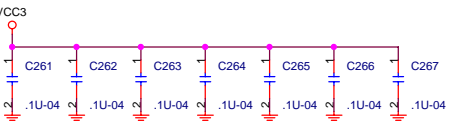
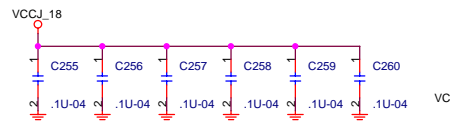
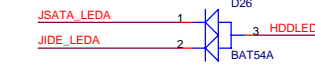
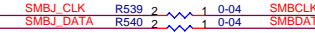
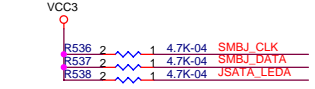
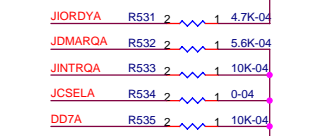
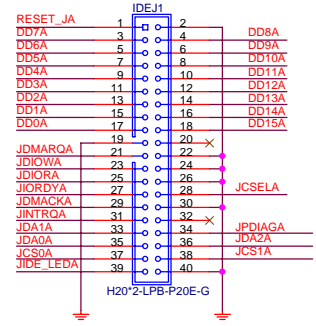
Title: INTEL GLAN PHY
Size: B Document Number: P965T-A Rev: 1.0P
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W = 4 ; S = 10...OTHER 20 MIL
MAX : 14000 MILS



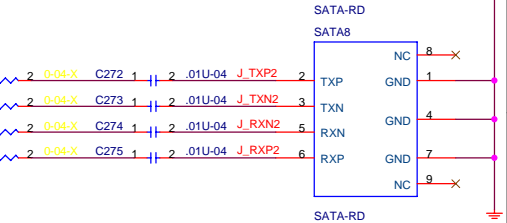
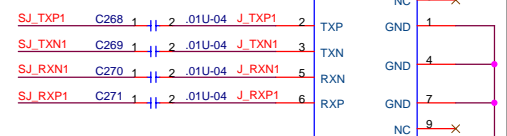
2006.01.04 modified



JMB363

LQFP 100 14x14

阻抗 : 110 ~ 120 Ohm



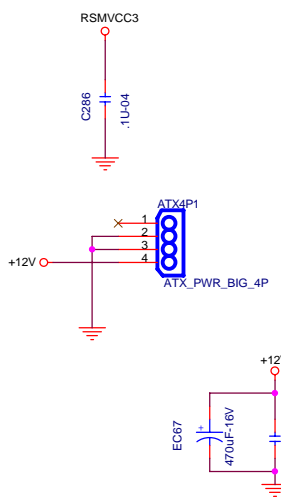
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- SMBCLK << SMBCLK 11,19,20,21,34,36,38,41,43
- SMBDATA << SMBDATA 11,19,20,21,34,36,38,41,43
- PCIRST_L2 << PCIRST_L2 19,22,38,41,43
- HDDLLED << HDDLLED 30
- HSI_P5 << HSI_P5 20
- HSI_N5 << HSI_N5 20
- HSI_P5 C284 << .1U-04 PETX+ 20
- HSI_N5 C285 << .1U-04 PETX- 20
- HSD_P5 << HSD_P5 20
- HSD_N5 << HSD_N5 20
- CK_PE_100M_SATA_H << CK_PE_100M_SATA_H 11
- CK_PE_100M_SATA_L << CK_PE_100M_SATA_L 11

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Title: **JMB363 SATA RAID_PATA**

Size: Custom Document Number: **P965T-A** Rev: 1.0B

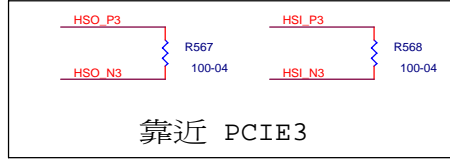
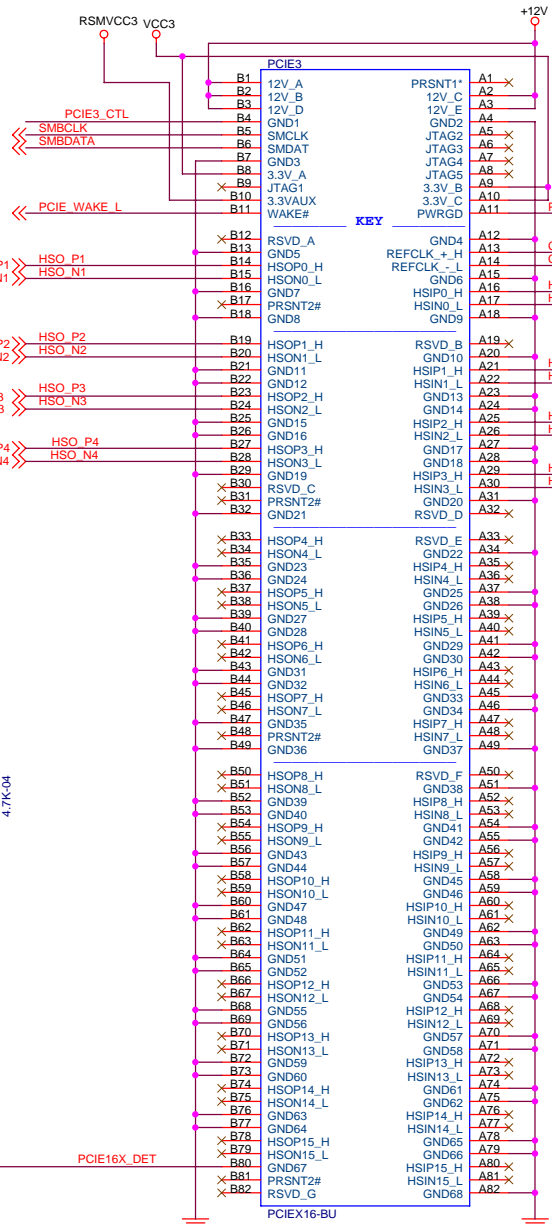
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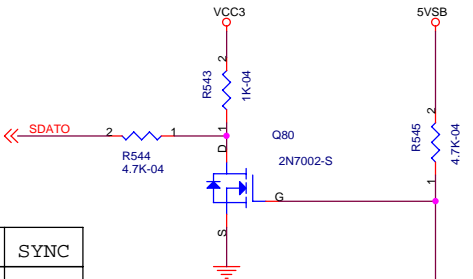
11,19,20,21,34,36,38,40,43 SMBCLK
11,19,20,21,34,36,38,40,43 SMBDATA

19,21,38,43 PCIE_WAKE_L

20 HSO_P1 HSO_N1
20 HSO_P2 HSO_N2
20,38 HSO_P2 HSO_N2
20,38 HSO_P2 HSO_N2
20,43 HSO_P3 HSO_N3
20,43 HSO_P3 HSO_N3
20 HSO_P4 HSO_N4
20 HSO_P4 HSO_N4

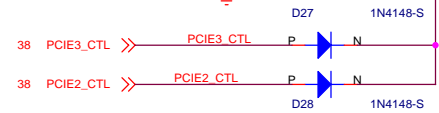
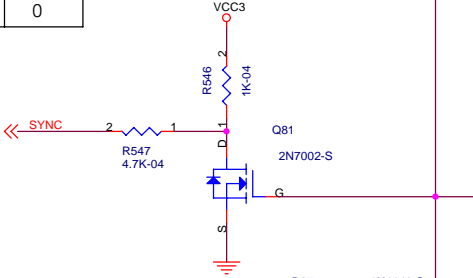


21,28 SDATO



	SDATO	SYNC
4lane x1	1	1
1lane x4	0	0

21,28 SYNC

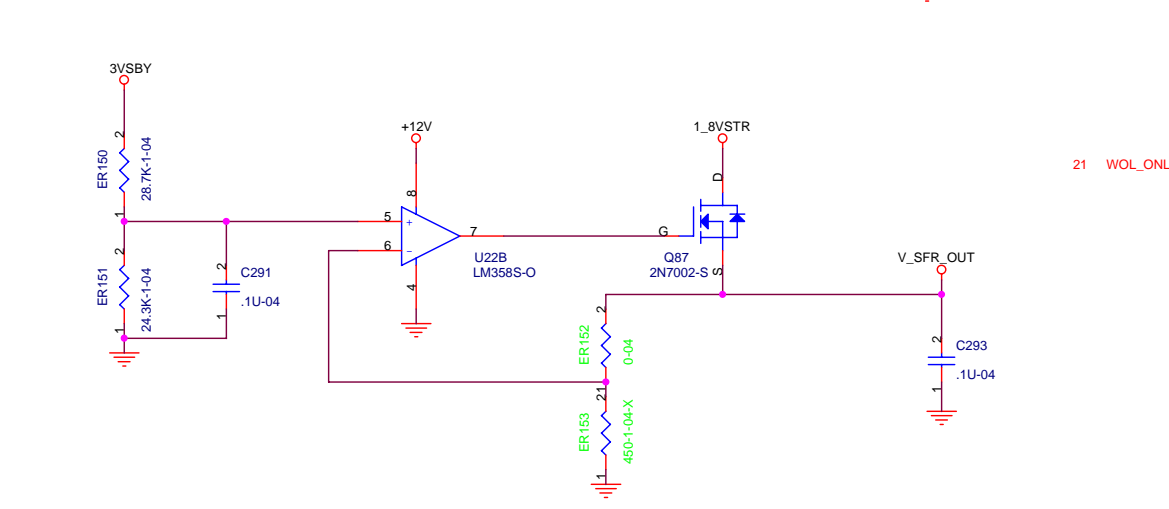
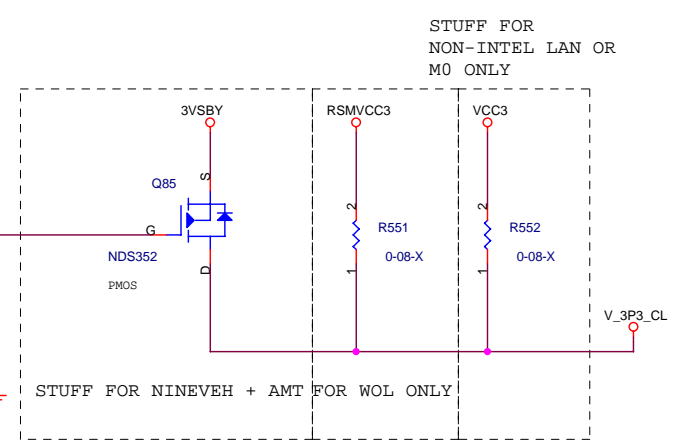
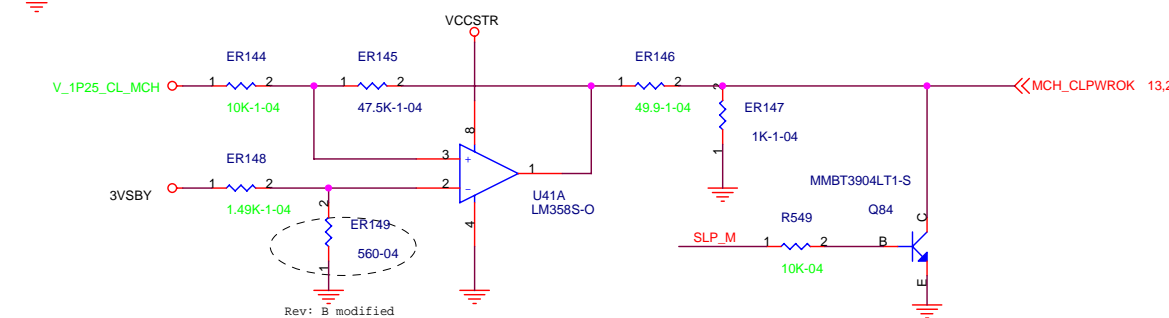
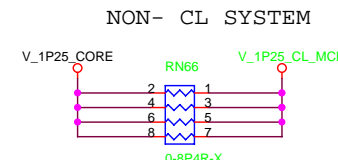
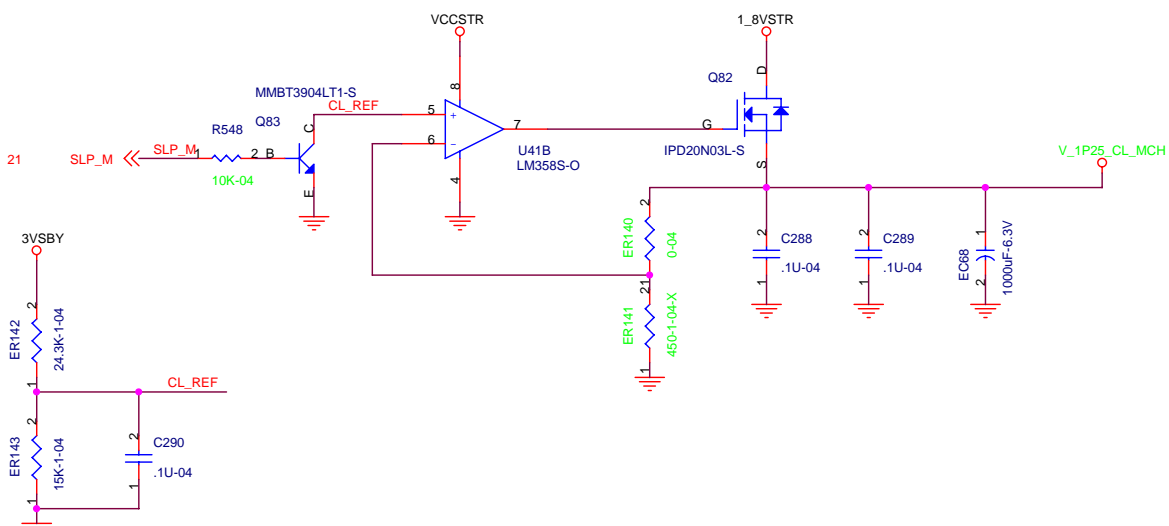


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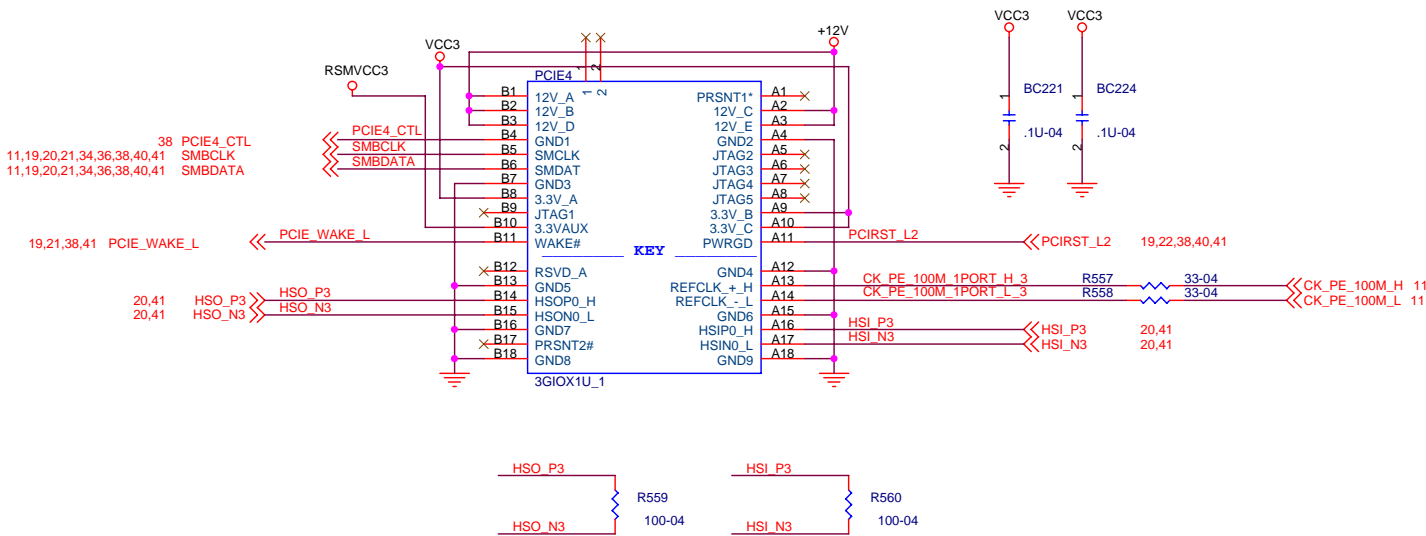
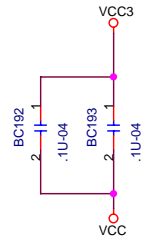
Title: **PCIEX2**


Size: Document Number **P965T-A** Rev: **1.0P**

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PCI Express SLOT1



 Elitegroup Computer Systems		
Title		
PCIE_1X		
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