

# Foxconn Precision Co. Inc.

## 865A01

Ver 1.1

Date: 2003/08/21

### 1. REVISION LIST:

REVISION	TOTAL PAGES	MODIFIED PAGES	ERRATA NO.	DATE
A				
B				
C				
D (Ver1.0)				
E				

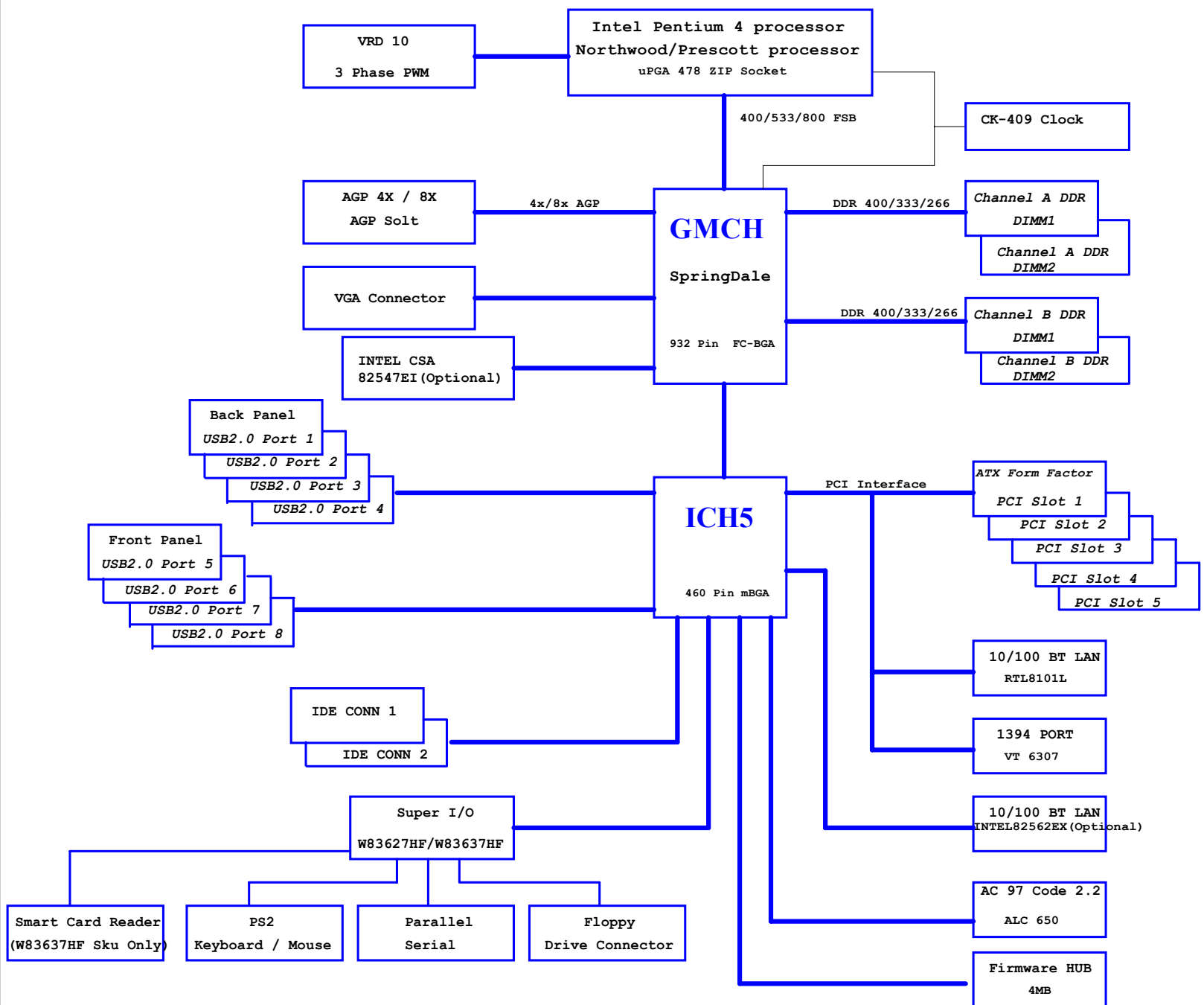
### 2. PAGE INDEX

01. Index Page	22. ICH5-1
02. Topology	23. ICH5-2
03. Rest Map	24. ICH5-3
04. Clock Distribution	25. 1394_VT6307
05. Power Delivery Map	26. LAN RTL8101L
06. ClockGen Cypress CY28405	27. CSA
07. Voltage Regulator Down 10	28. LAN CON & USB3,4
08. 2.5V Power	29. ITP
09. 1.5V Power	30. FWH
10. 1.25V Power	31. USB Connectors
11. Socket478 -1	32. AC'97 Codec
12. Socket478 -2	33. Power/MISC Connectors
13. Springdale-GMCH-1	34. PCI Slots 1,2
14. Springdale-GMCH-2	35. PCI Slots 3,4
15. Springdale-GMCH-3	36. PCI Slot 5
16. DDR Channel A DIMM's	37. Super IO W83627NHF
17. DDR Channel A Termination	38. Keyboard/Mouse/FAN
18. DDR Channel B DIMM's	39. Serial/Print Ports
19. DDR Channel B Termination	40. GPIO Summary
20. AGP Connector	41. Jumper Setting Summary
21. VGA Connector	42. For EMI Caps
	43. CNR

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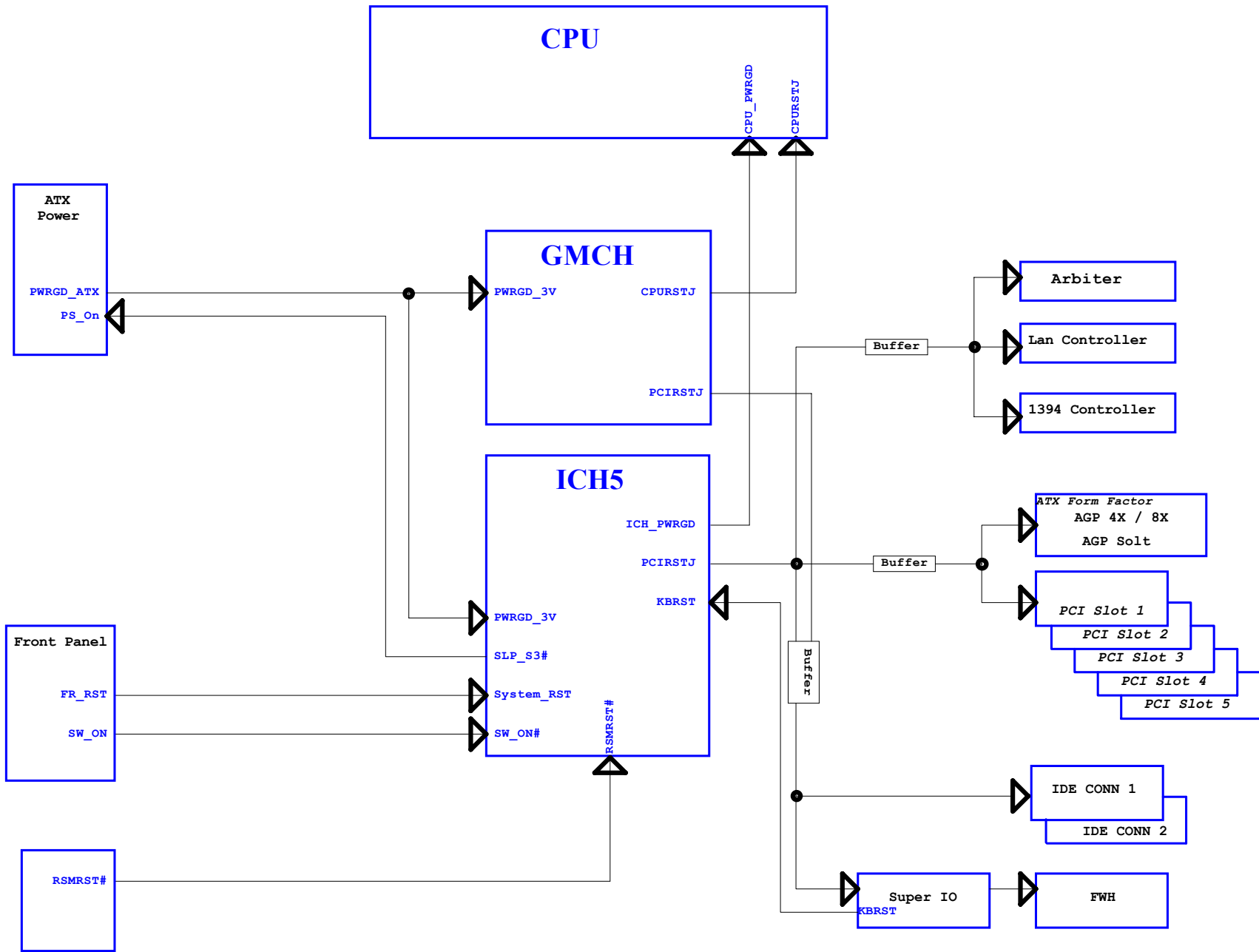
Title Index Page		
Size C	Document Number 865A01	Rev E
Date: Sunday, August 24, 2003	Sheet 1	of 44



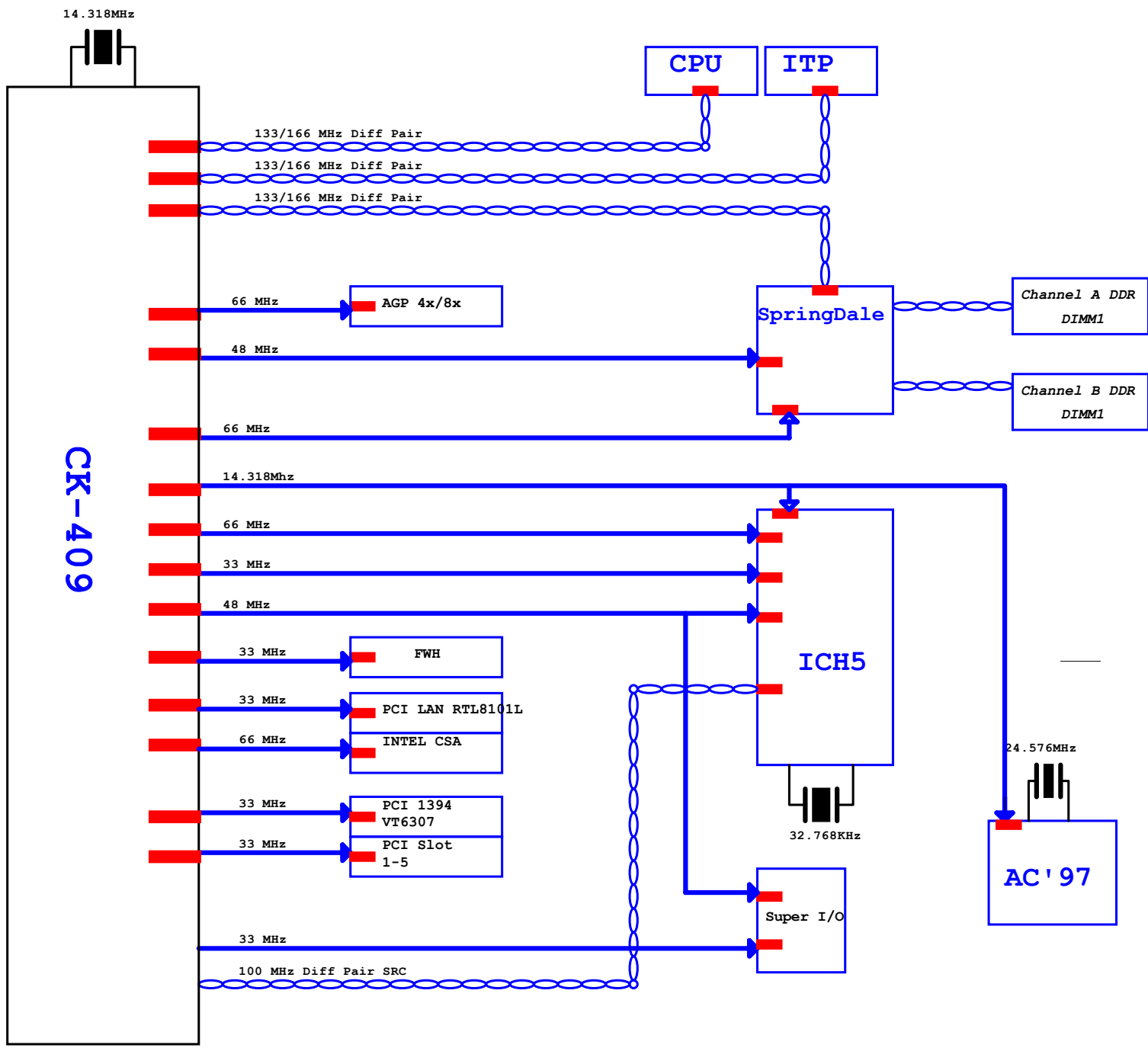
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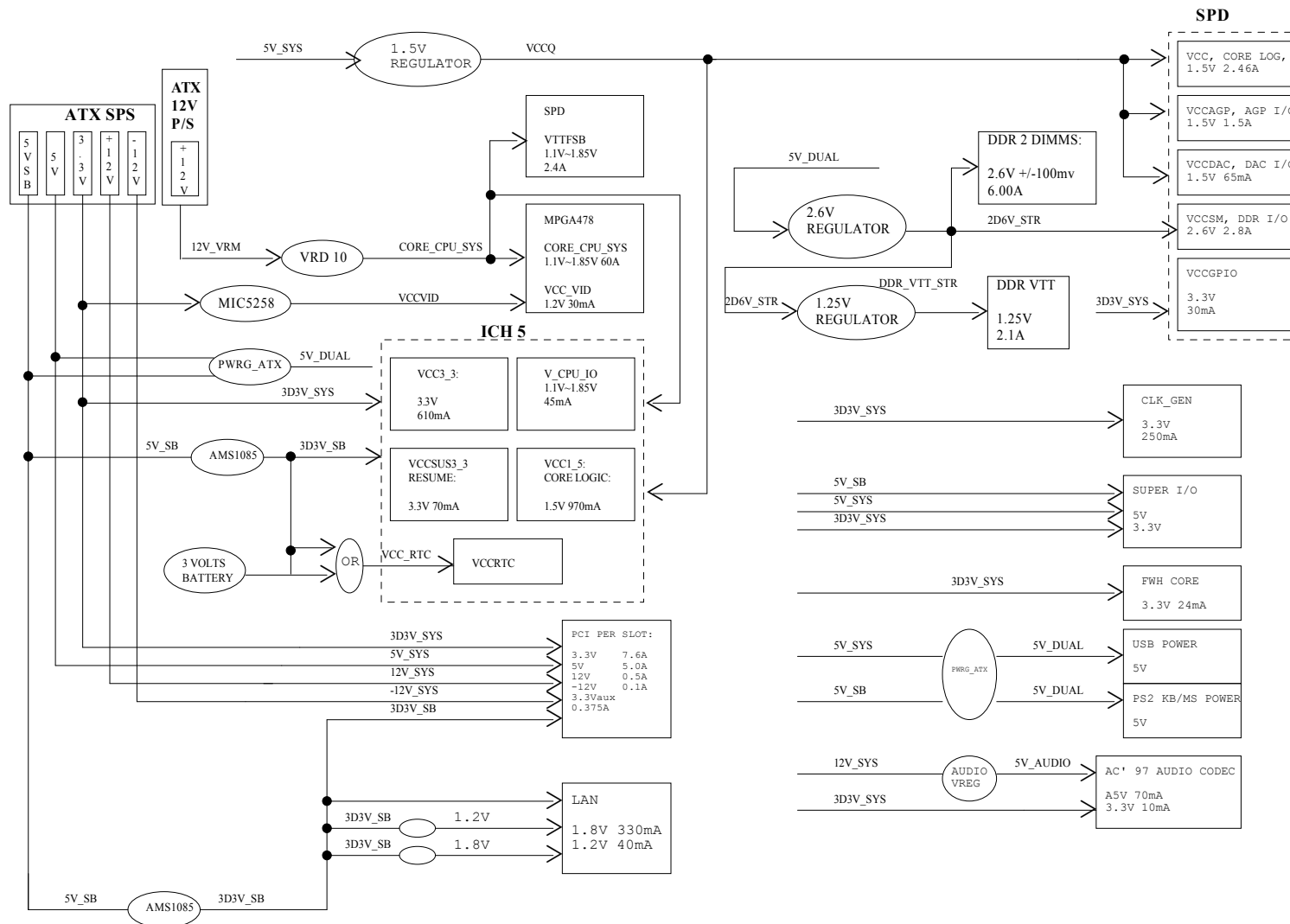
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Size	Document Number	865A01	
C	Date	Sunday, August 24, 2003	Sheet 2 of 44
Rev	E		



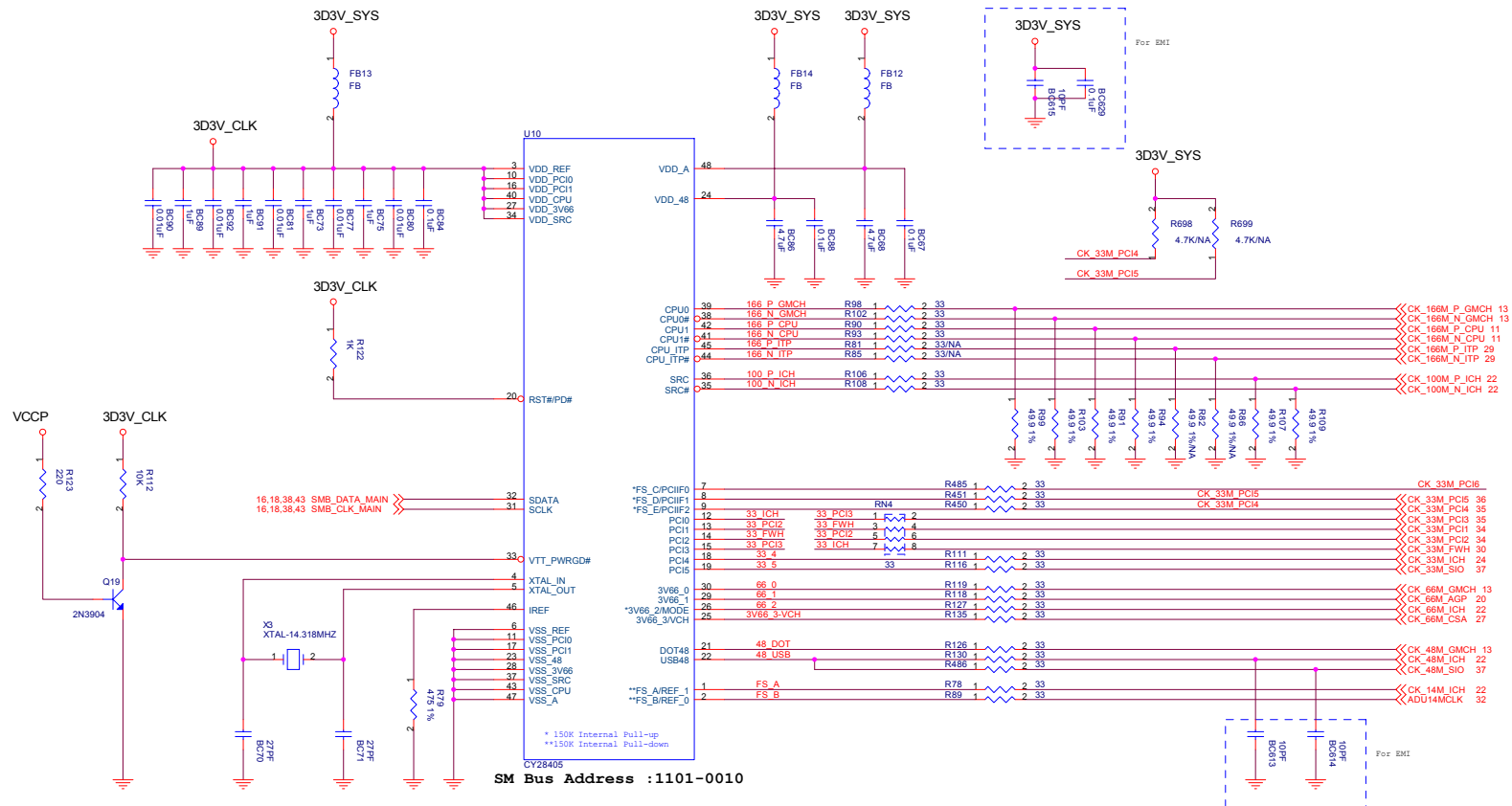
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PCI Arbiter



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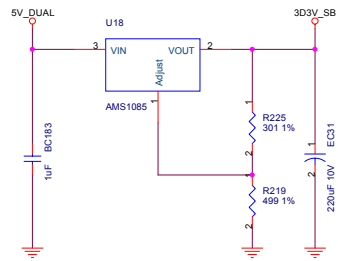
Title: **Clock Generator CK-409**

Size: C Document Number: **865A01** Rev: E

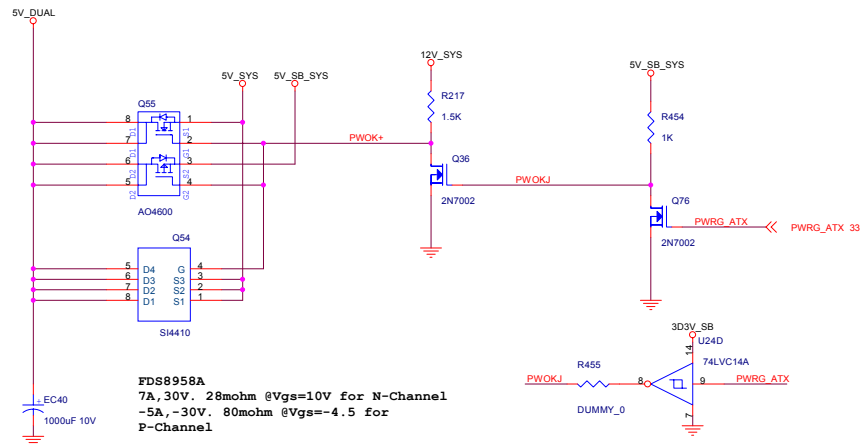
Date: Sunday, August 24, 2003 Sheet: 6 of 44

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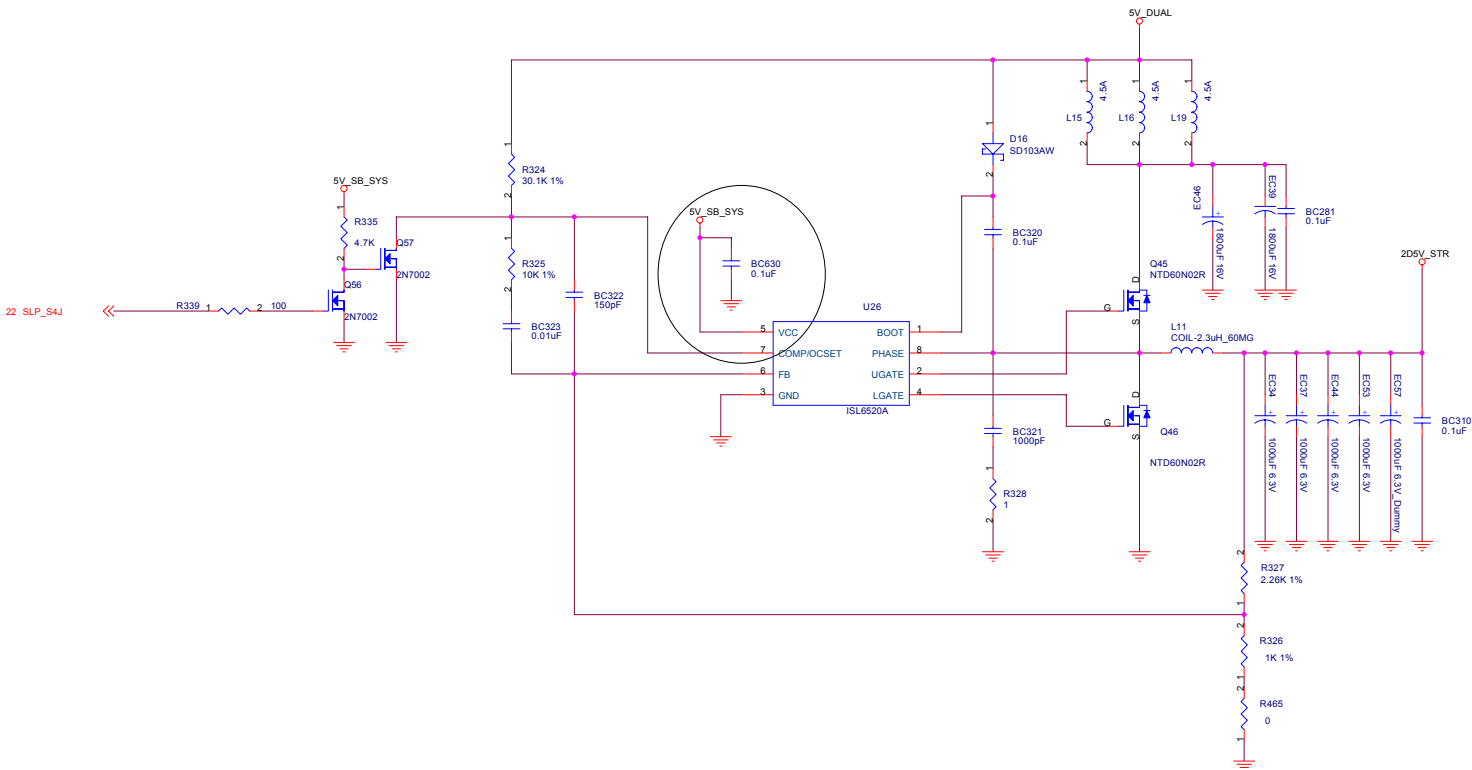




$V_{out} = V_{ref}(1 + R_2/R_1) + I_{adj}R_2$   
 $R_1$  is Up Resister.  
 $I_{adj} = 50\mu A$   
 $V_{ref} = 1.25V$



**FDS8958A**  
**7A, 30V, 28mohm @Vgs=10V for N-Channel**  
**-5A, -30V, 80mohm @Vgs=-4.5 for P-Channel**

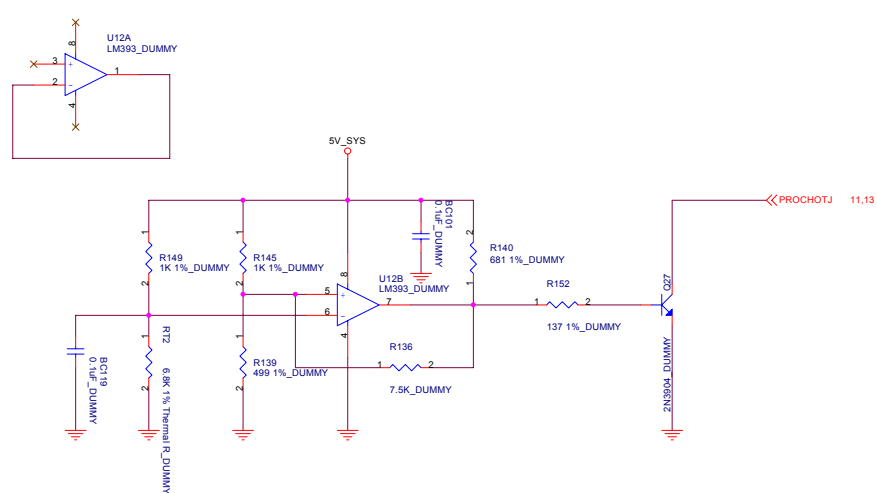
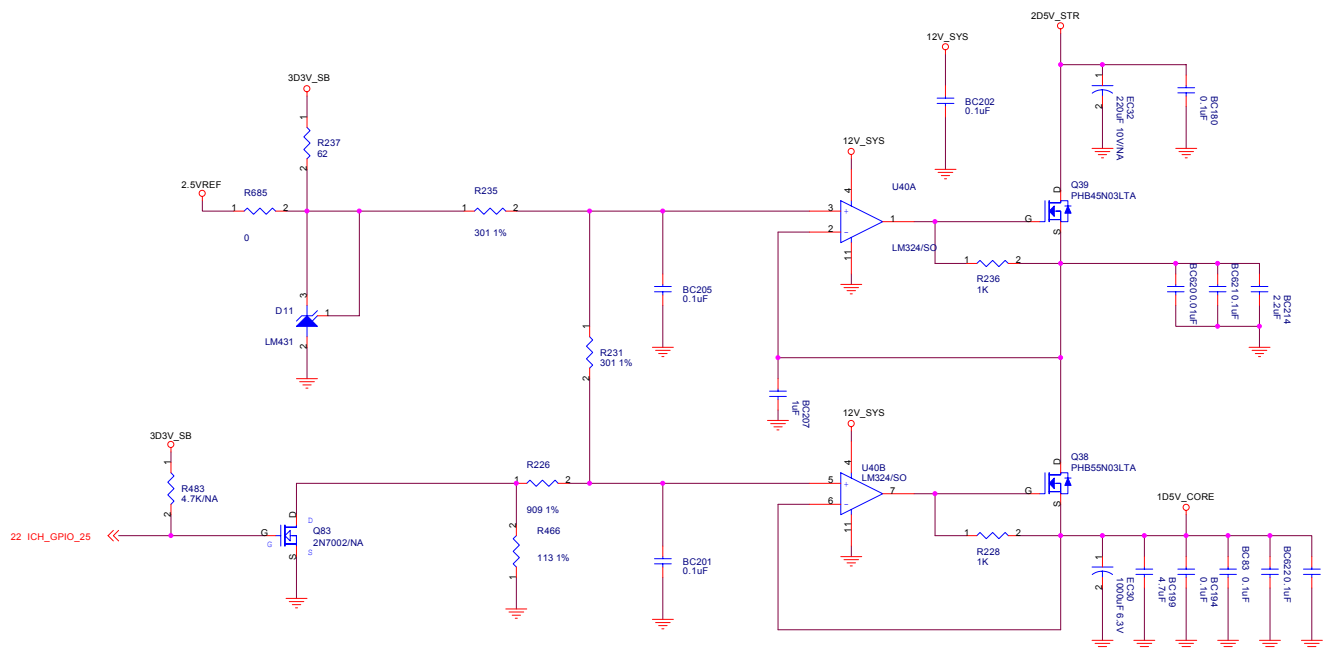


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Title		Power 2.5V-5VDUAL-3.3SB	
Size	Document Number	865A01	
C	Date	Sunday, August 24, 2003	Sheet 8 of 44
	Rev	E	



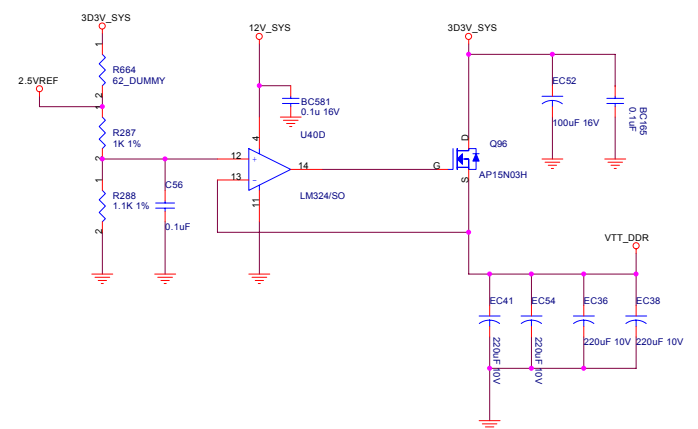
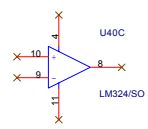
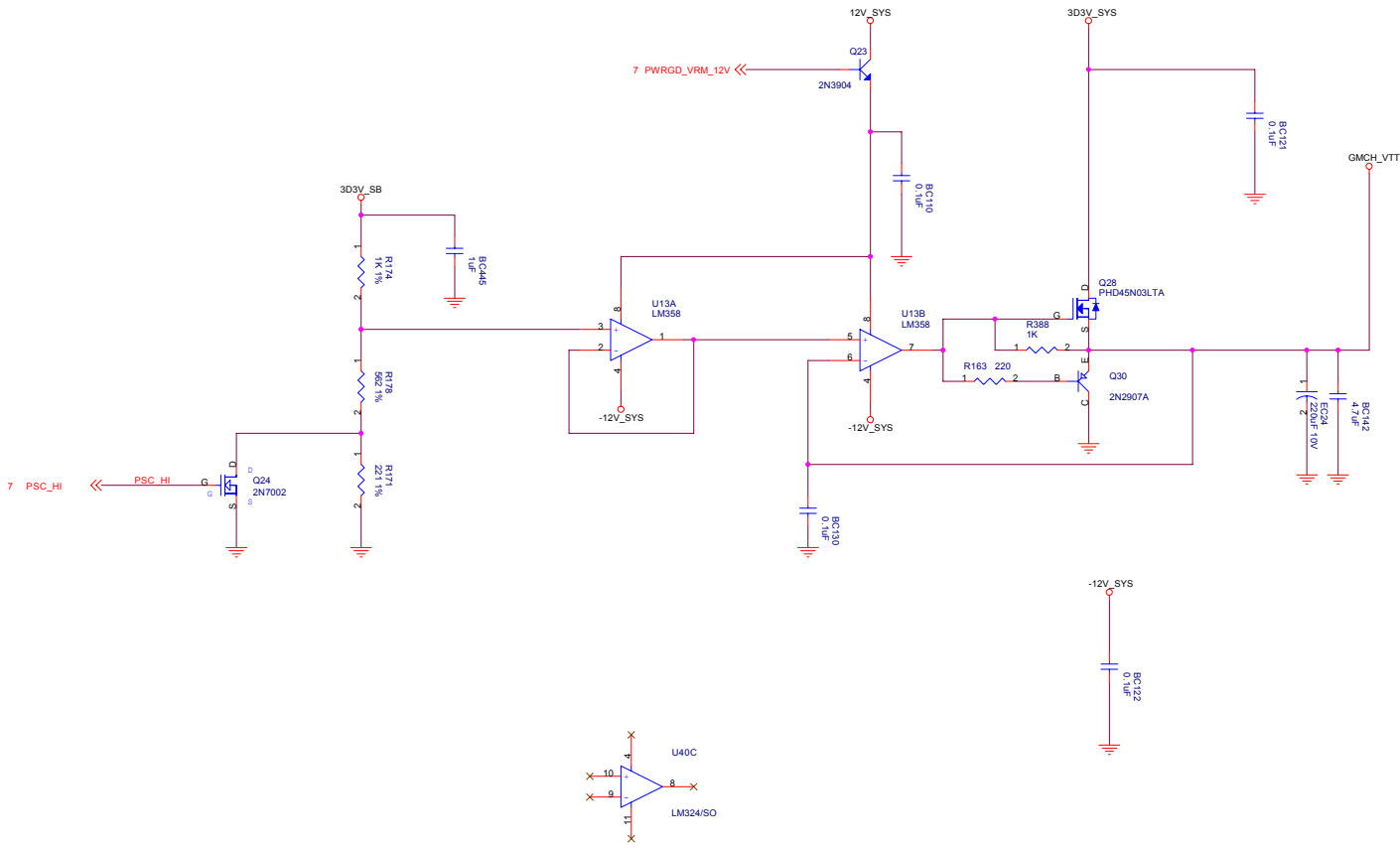


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Title		Power 1.5V
Size	Document Number	865A01
Date:	Sunday, August 24, 2003	Sheet 9 of 44

NWD=1.45V  
PSC=1.2V  
GMCH\_VTT Source 1.6A and Sink 600mA



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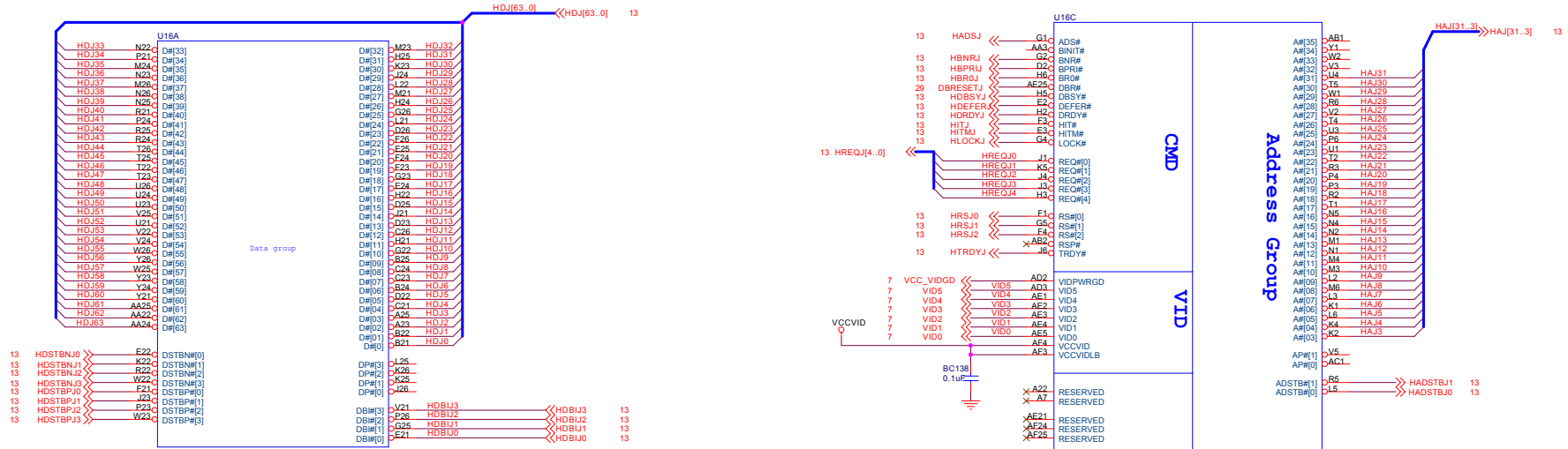
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FOXCONN PCEG

Title: Power 1.25V-GMCH VTT  
Size: Custom  
Date: Sunday, August 24, 2003  
Sheet: 10 of 44

Document Number: **865A01**  
Rev: E

HOST BUS

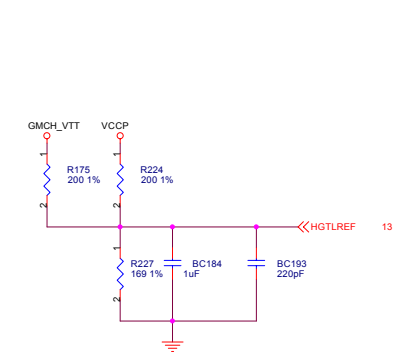
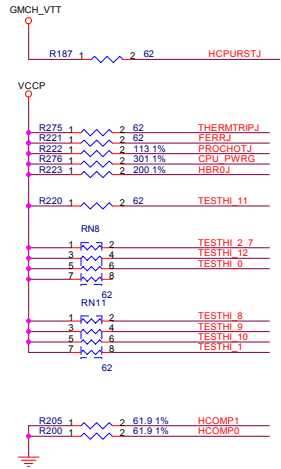
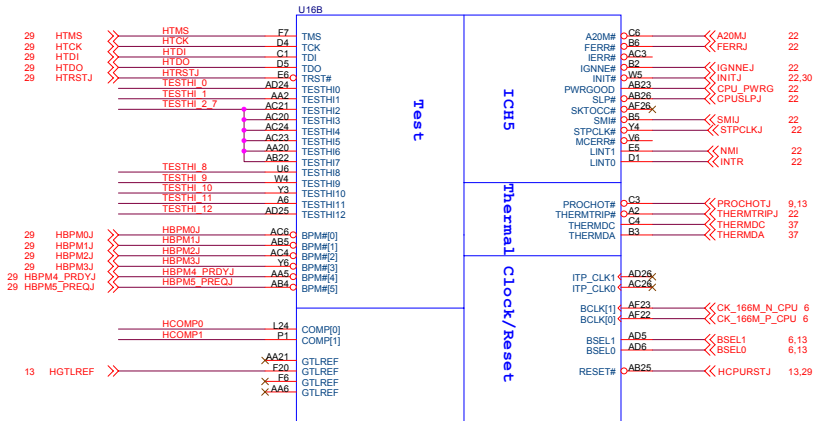
CMD ADDRESS & VID



TEST, ICH5, CLK & THERMAL

PULL UP CIRCUIT

HOST GTLREF

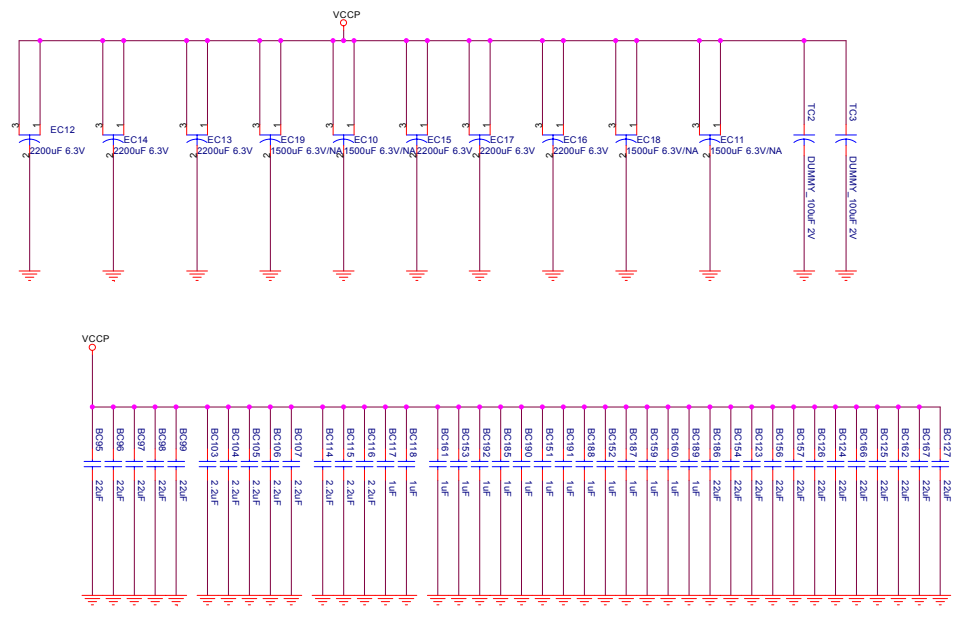
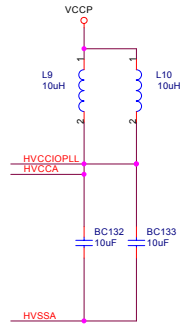


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Title: Socket 478-1

Size: C	Document Number: 865A01	Rev: E
Date: Sunday, August 24, 2003	Sheet: 11	of: 44



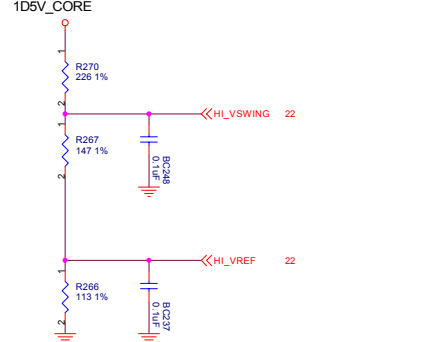
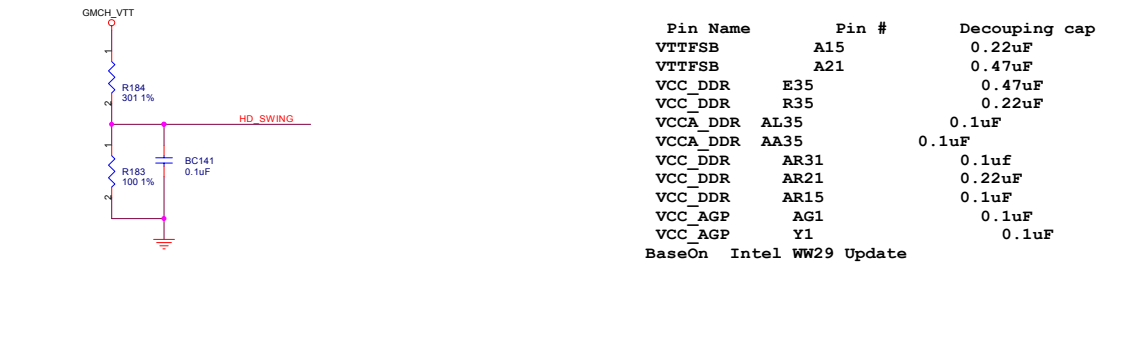
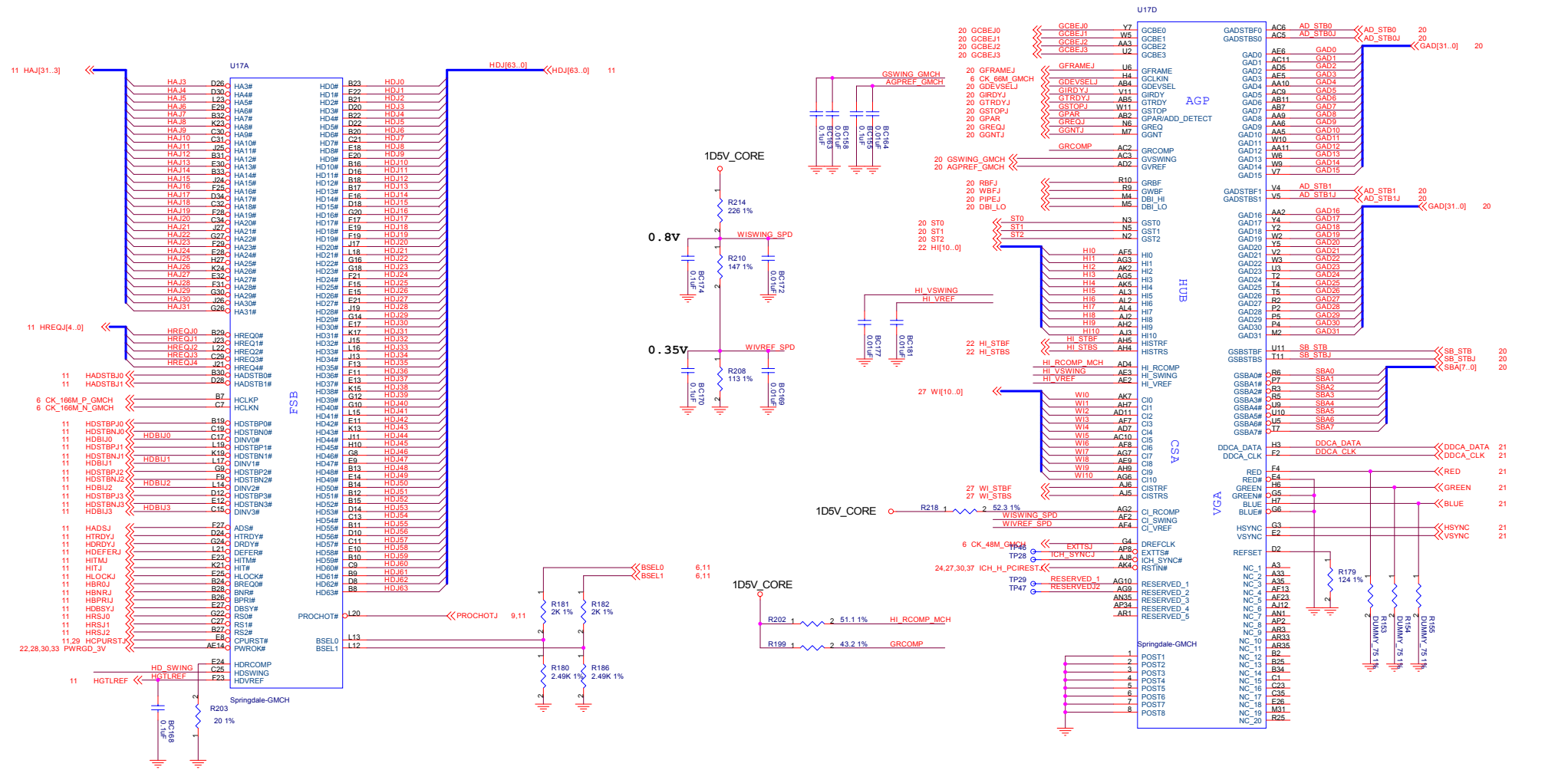
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Title: Socket 478-2

Size: C    Document Number: **865A01**    Rev: E

Date: Sunday, August 24, 2003    Sheet: 12 of 44

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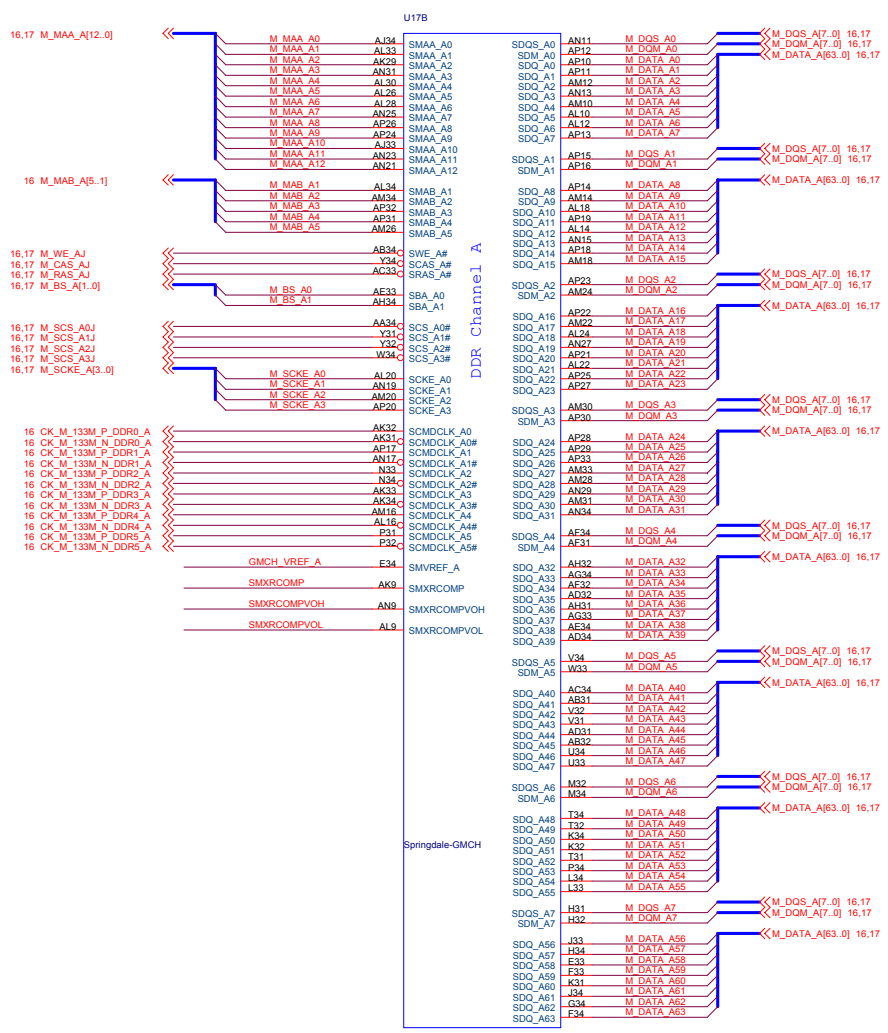
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Title: **GMCH-1**

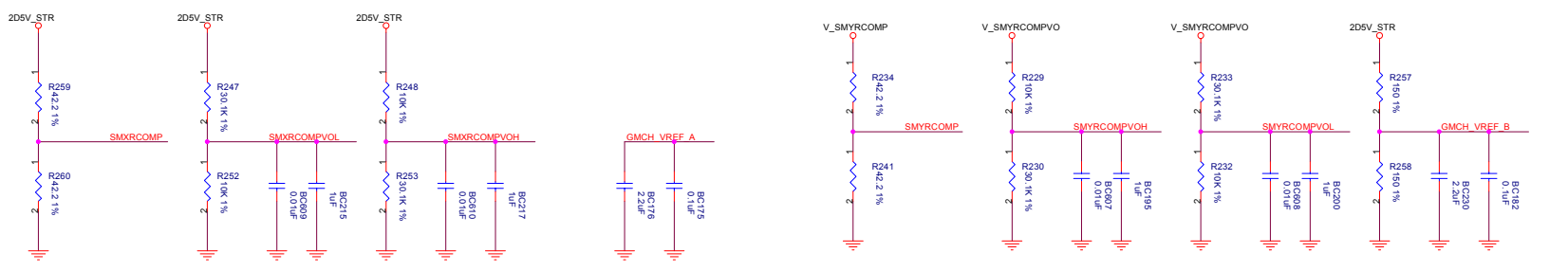
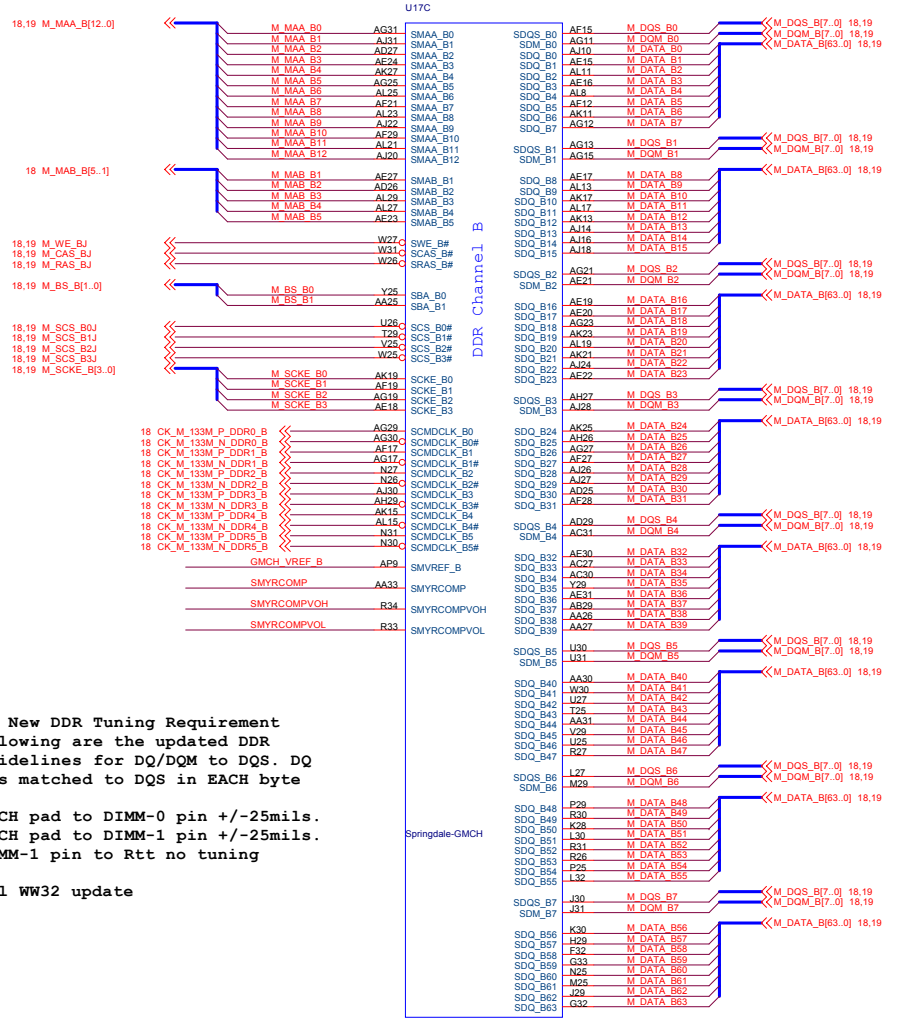
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Date: Sunday, August 24, 2003 Sheet: 13 of 44

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**Subject: New DDR Tuning Requirement**  
 > The following are the updated DDR tuning guidelines for DQ/DQM to DQS. DQ > & DQM is matched to DQS in EACH byte lane:  
 > From GMCH pad to DIMM-0 pin +/-25mils.  
 > From GMCH pad to DIMM-1 pin +/-25mils.  
 > From DIMM-1 pin to Rtt no tuning required.  
 Form Intel WW32 update

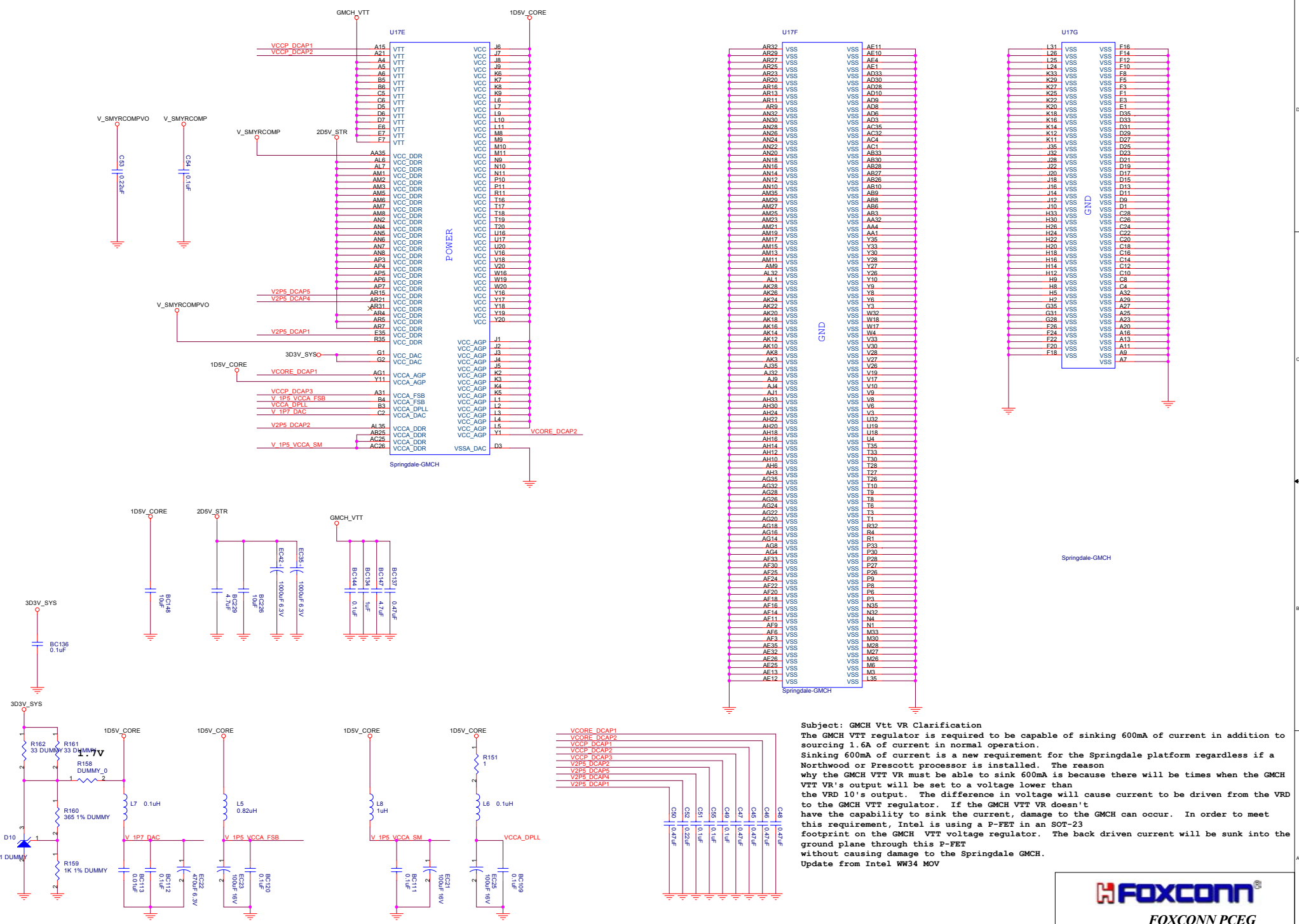


**GMCH-2**

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Title			Rev
Size	Document Number	865A01	E
Date:	Sunday, August 24, 2003	Sheet	14 of 44



**Subject: GMCH Vtt VR Clarification**

The GMCH VTT regulator is required to be capable of sinking 600mA of current in addition to sourcing 1.6A of current in normal operation. Sinking 600mA of current is a new requirement for the Springdale platform regardless if a Northwood or Prescott processor is installed. The reason why the GMCH VTT VR must be able to sink 600mA is because there will be times when the GMCH VTT VR's output will be set to a voltage lower than the VRD 10's output. The difference in voltage will cause current to be driven from the VRD to the GMCH VTT regulator. If the GMCH VTT VR doesn't have the capability to sink the current, damage to the GMCH can occur. In order to meet this requirement, Intel is using a P-FET in an SOT-23 footprint on the GMCH VTT voltage regulator. The back driven current will be sunk into the ground plane through this P-FET without causing damage to the Springdale GMCH.

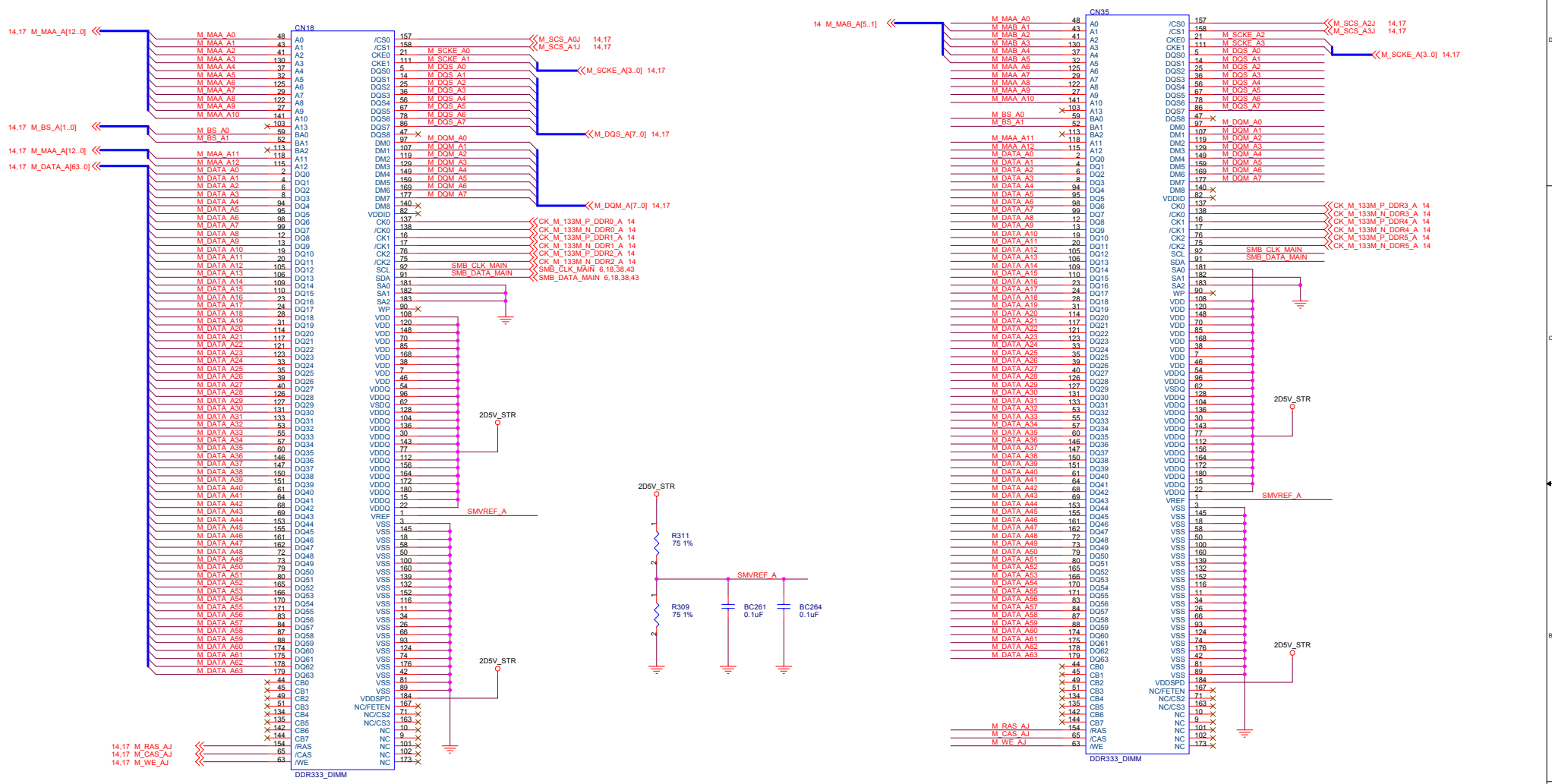
Update from Intel W34 MOV

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Title: Springdale-GMCH-3

Size: C Document Number: 865A01 Rev: E

Date: Sunday, August 24, 2003 Sheet: 15 of 44



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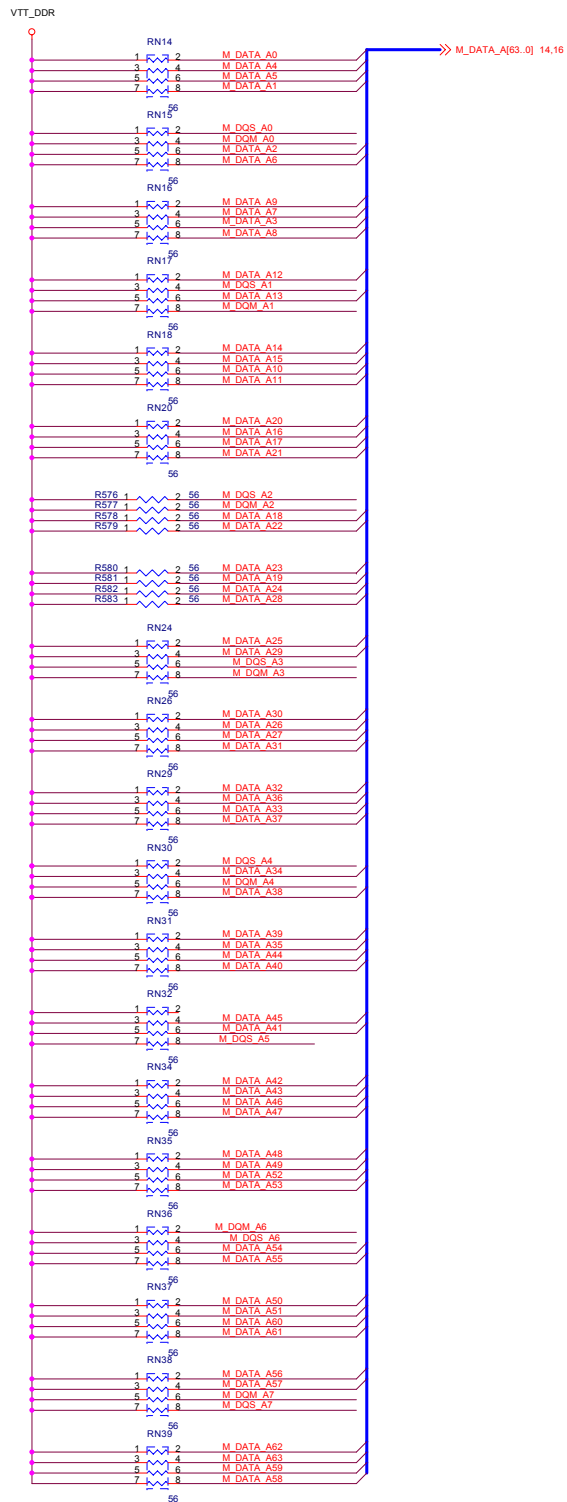
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Title: **DDR Channel A DIMM's**

Size: Document Number **865A01** Rev: E

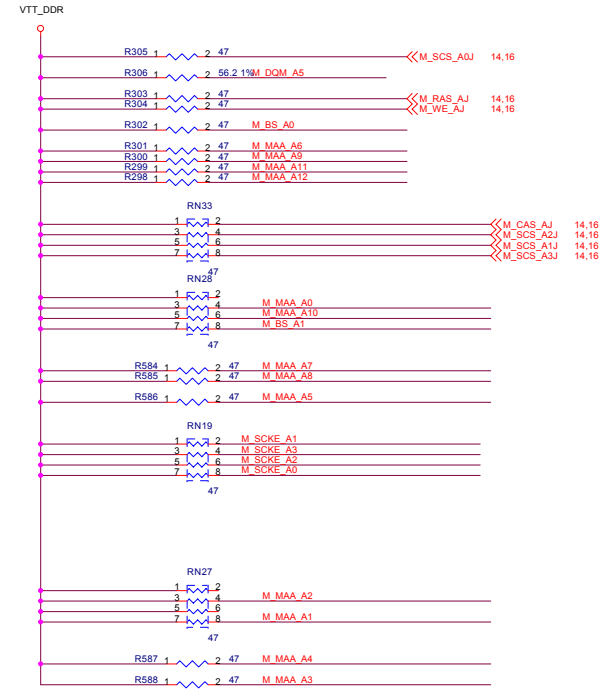
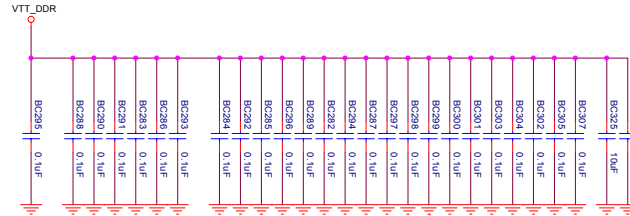
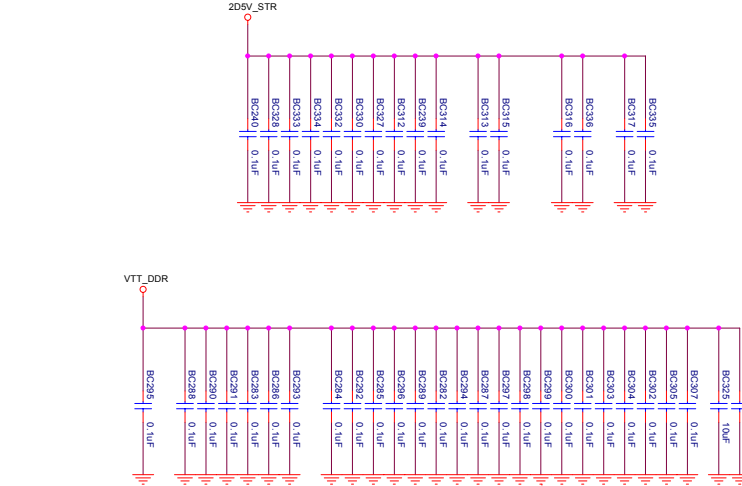
Date: Sunday, August 24, 2003 Sheet 16 of 44

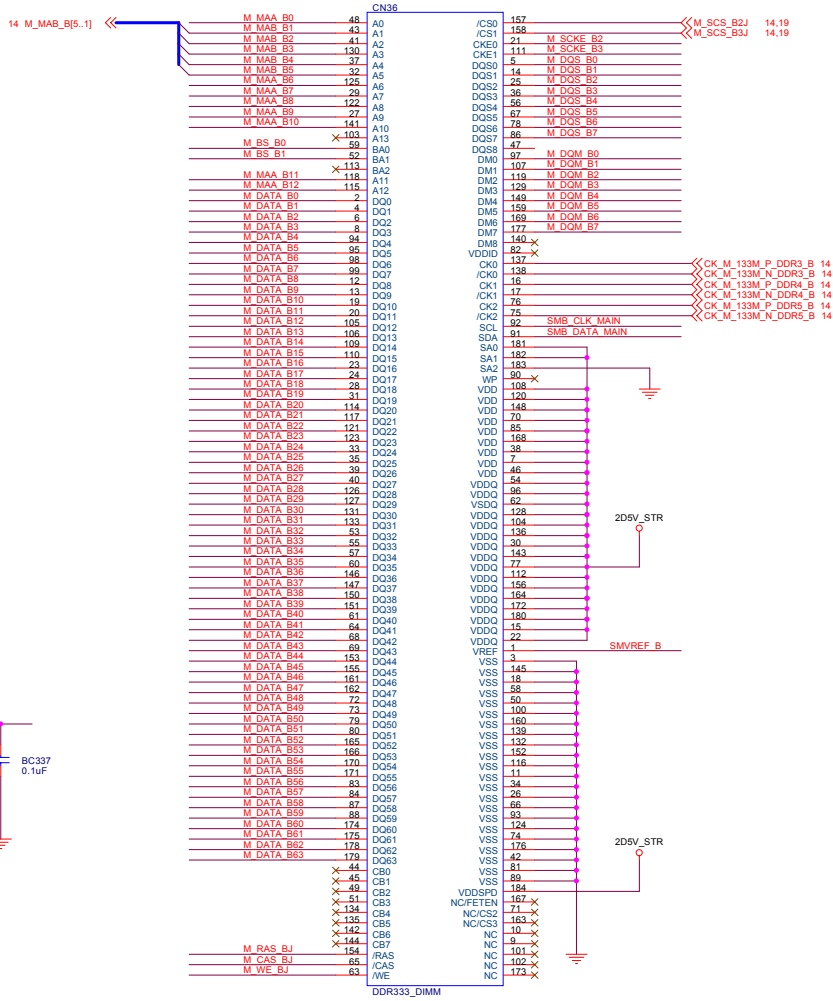
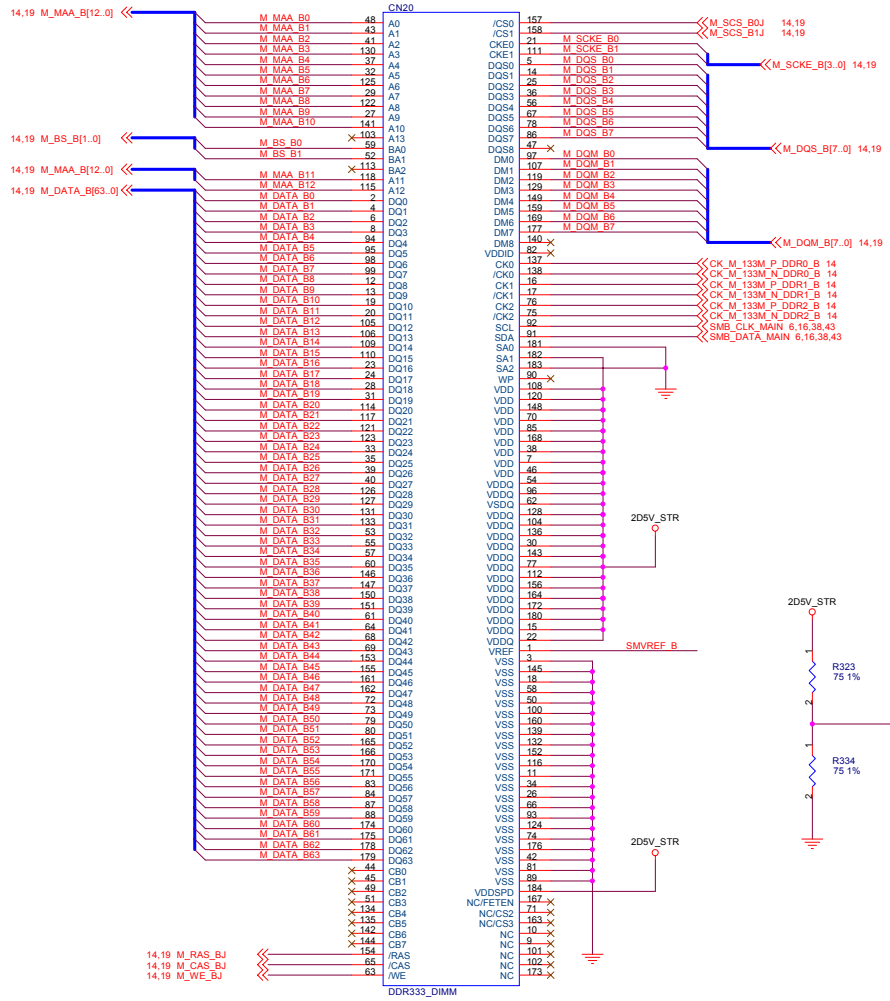




Updated DDR Termination Resistor (Rtt) Values  
 The recommended termination resistor (Rtt) value for DQ/DQM/DQS is changed to 56 ohms. The previous recommendation was 110 ohms.  
 Form Intel FAE WW32

- M\_MAA\_A[12..0] 14,16
- M\_BS\_A[1..0] 14,16
- M\_SCKE\_A[3..0] 14,16
- M\_DOM\_A[7..0] 14,16
- M\_DQS\_A[7..0] 14,16





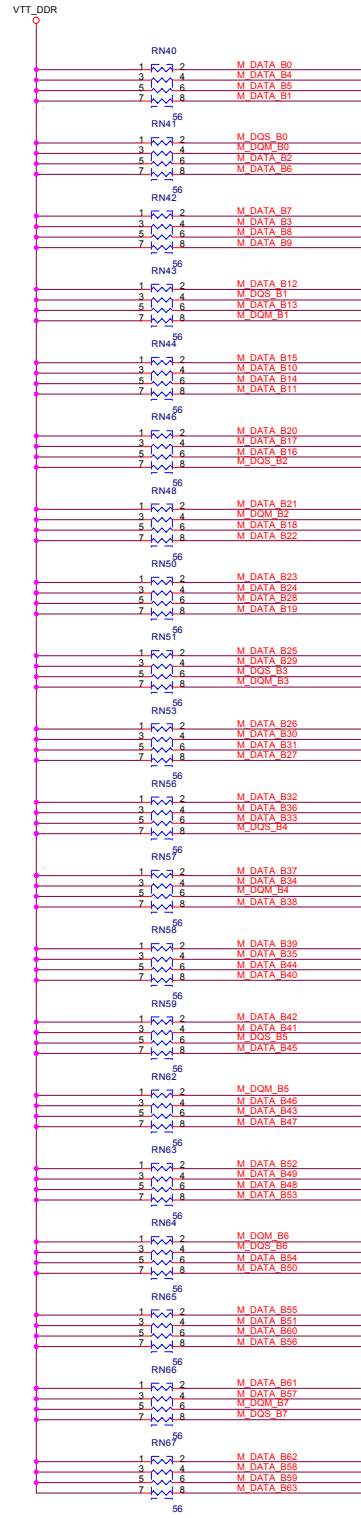
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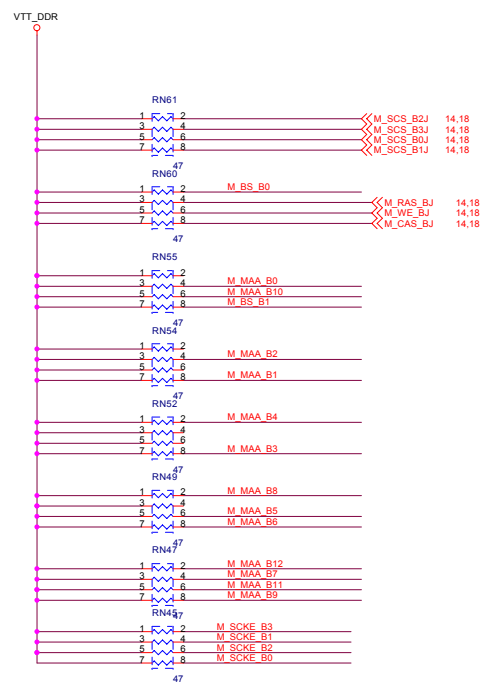
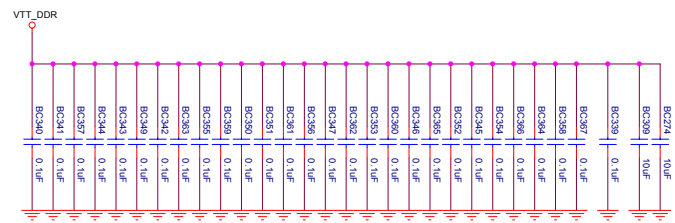
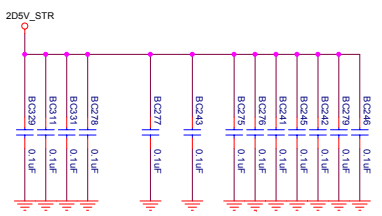
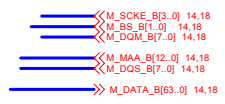
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Size: Custom Document Number **865A01** Rev: E

Date: Sunday, August 24, 2003 Sheet 18 of 44



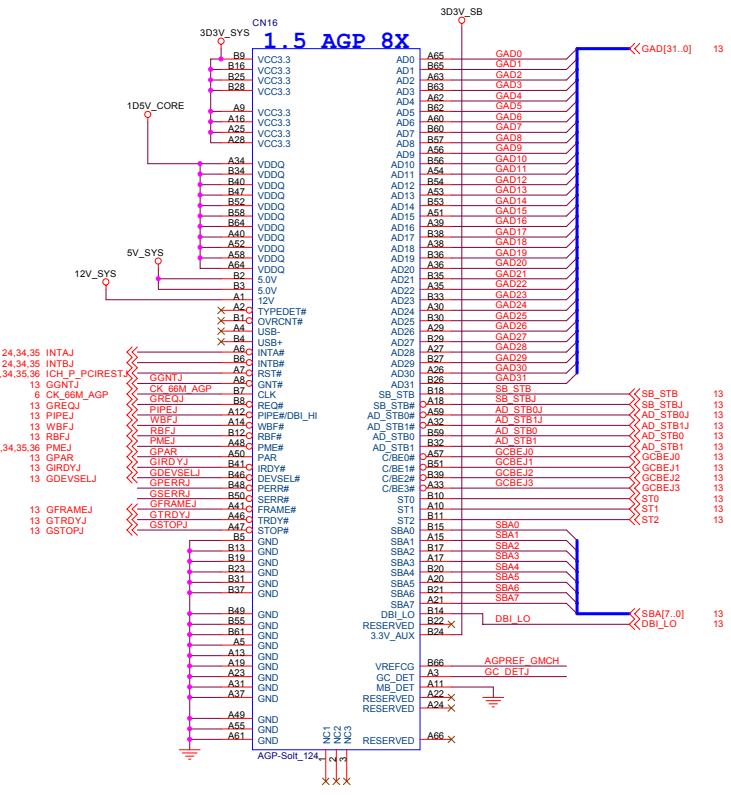
Updated DDR Termination Resistor (Rtt) Values  
 The recommended termination resistor (Rtt) value for DQ/DQM/DQS is changed to 56 ohms. The previous recommendation was 110 ohms.  
 Form Intel FAE WW32



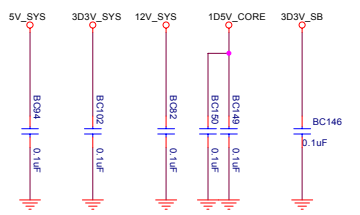
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 FOXCONN PCEG

Title: **DDR Channel B Termination**

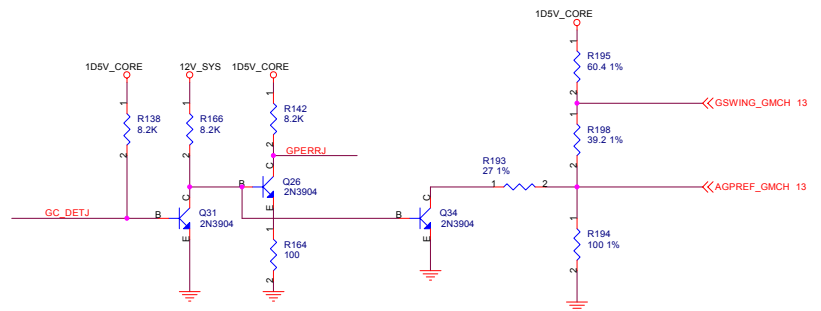
Size	Document Number	Rev
C	<b>865A01</b>	E
Date:	Sunday, August 24, 2003	Sheet 19 of 44



### DECUBLE CAP.

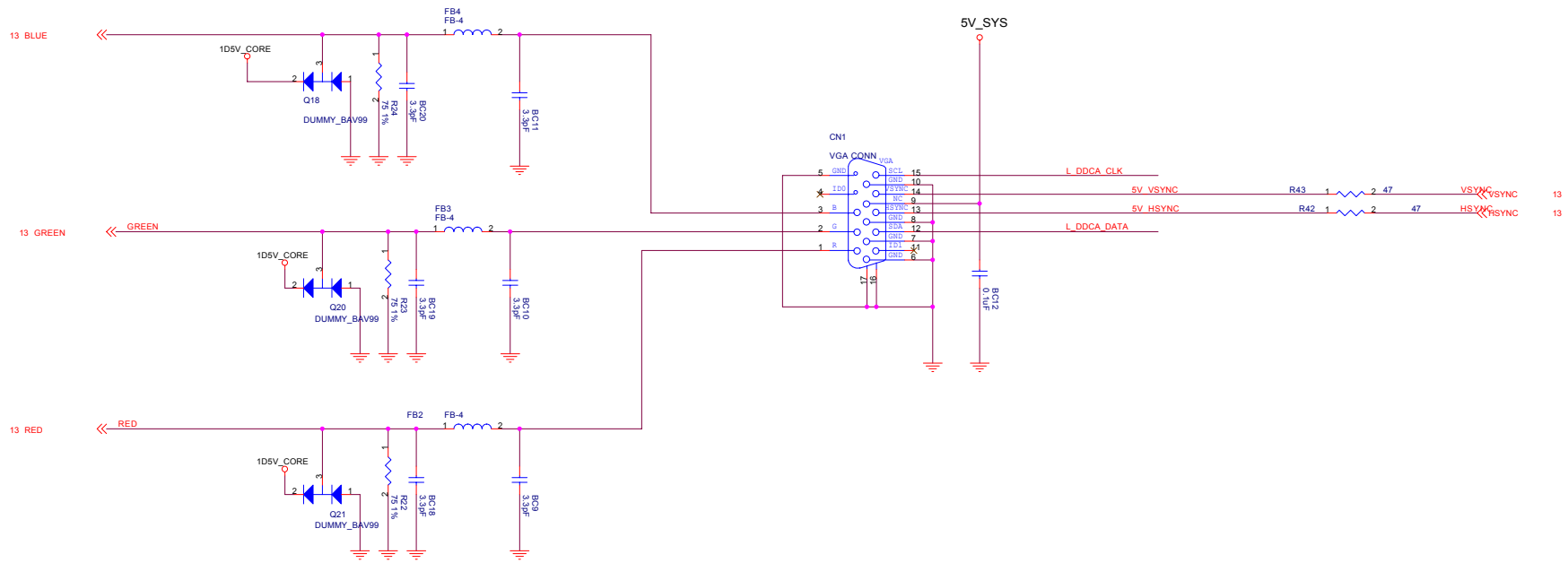


### AGPREF & AGPSWING CIRCUIT

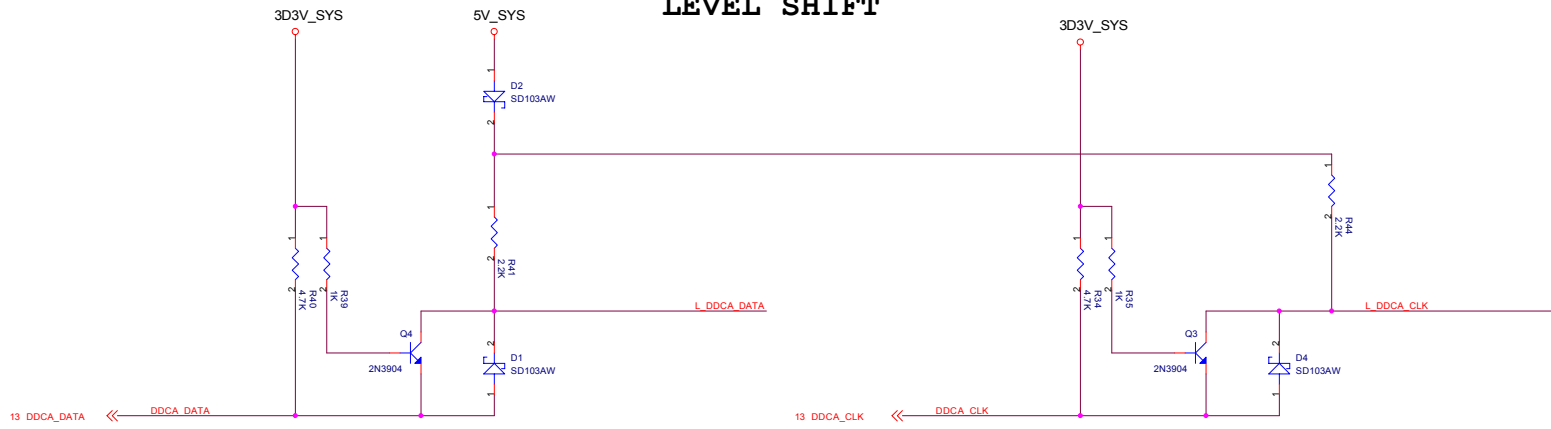


Title <b>AGP Connector</b>		
Size C	Document Number <b>865A01</b>	Rev E
Date: Sunday, August 24, 2003	Sheet 20	of 44

# VGA CONN.

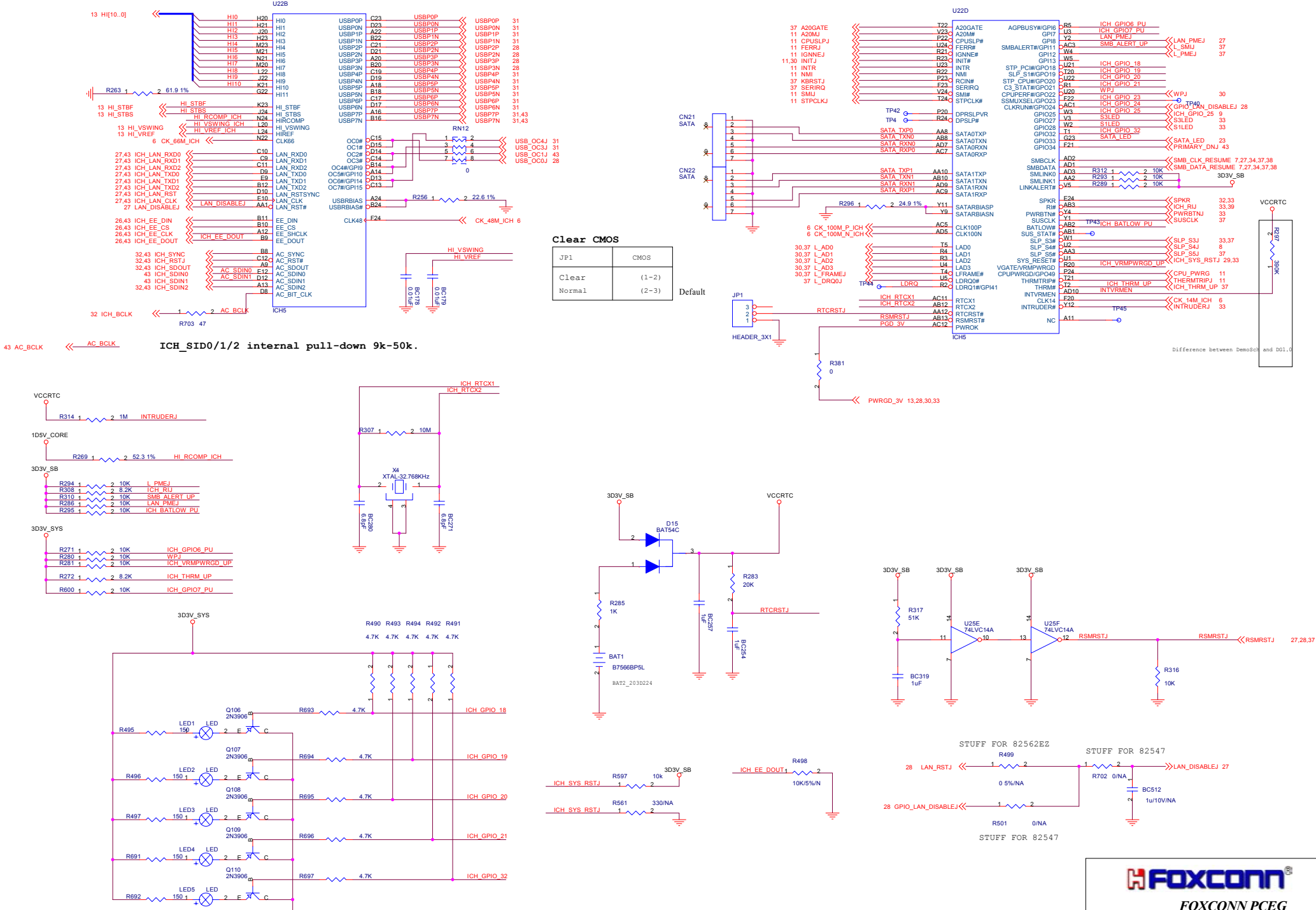


# LEVEL SHIFT




Title			VGA Connector
Size	Document Number	865A01	
C	Date	Sunday, August 24, 2003	Sheet 21 of 44
			Rev E

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**Clear CMOS**

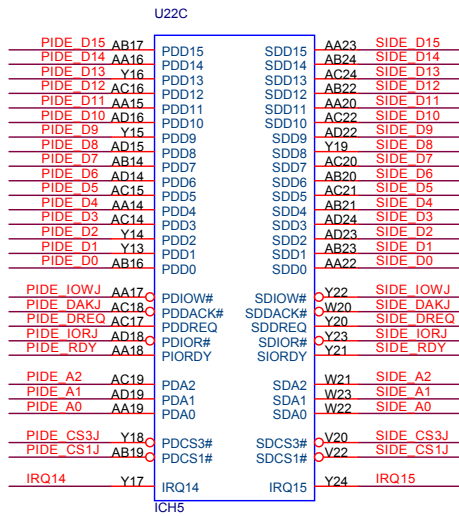
JP1	CMOS	Default
Clear	(1-2)	
Normal	(2-3)	

  
**FOXCONN PCEG**

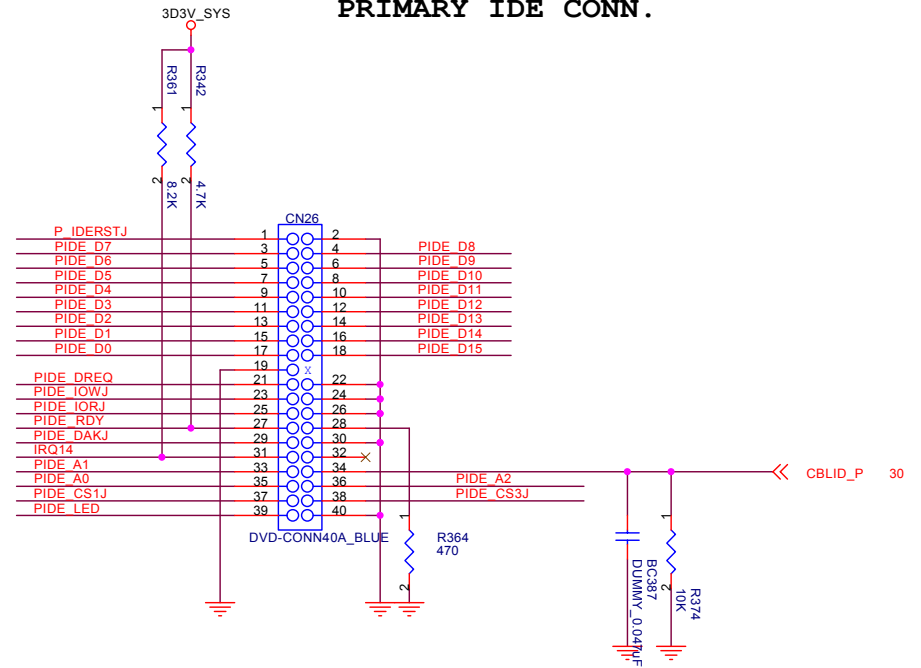
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 Size: C Document Number: **865A01** Rev: E  
 Date: Sunday, August 24, 2003 Sheet: 22 of 44

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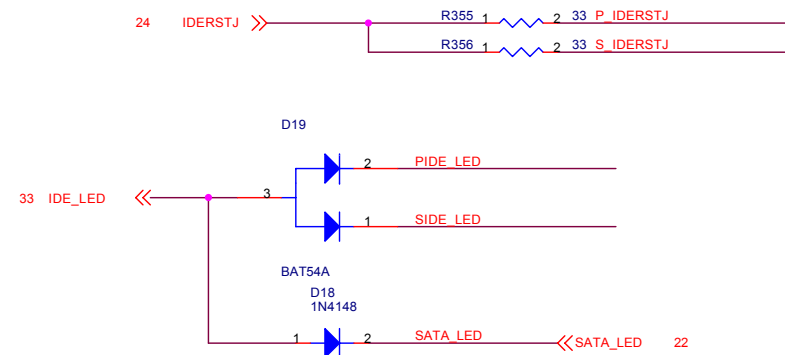
# ICH5 IDE INTERFACE



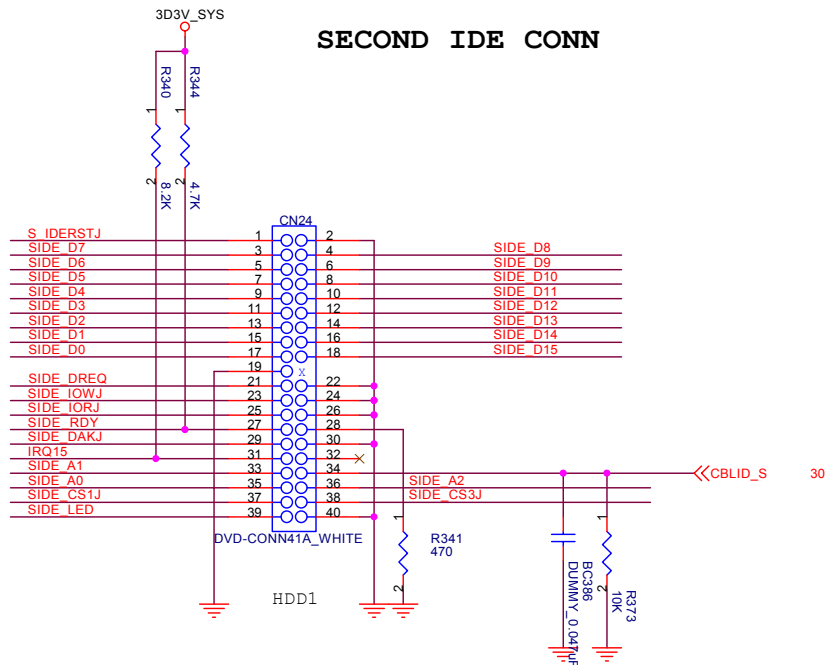
# PRIMARY IDE CONN.



# IDE LED & IDE RST



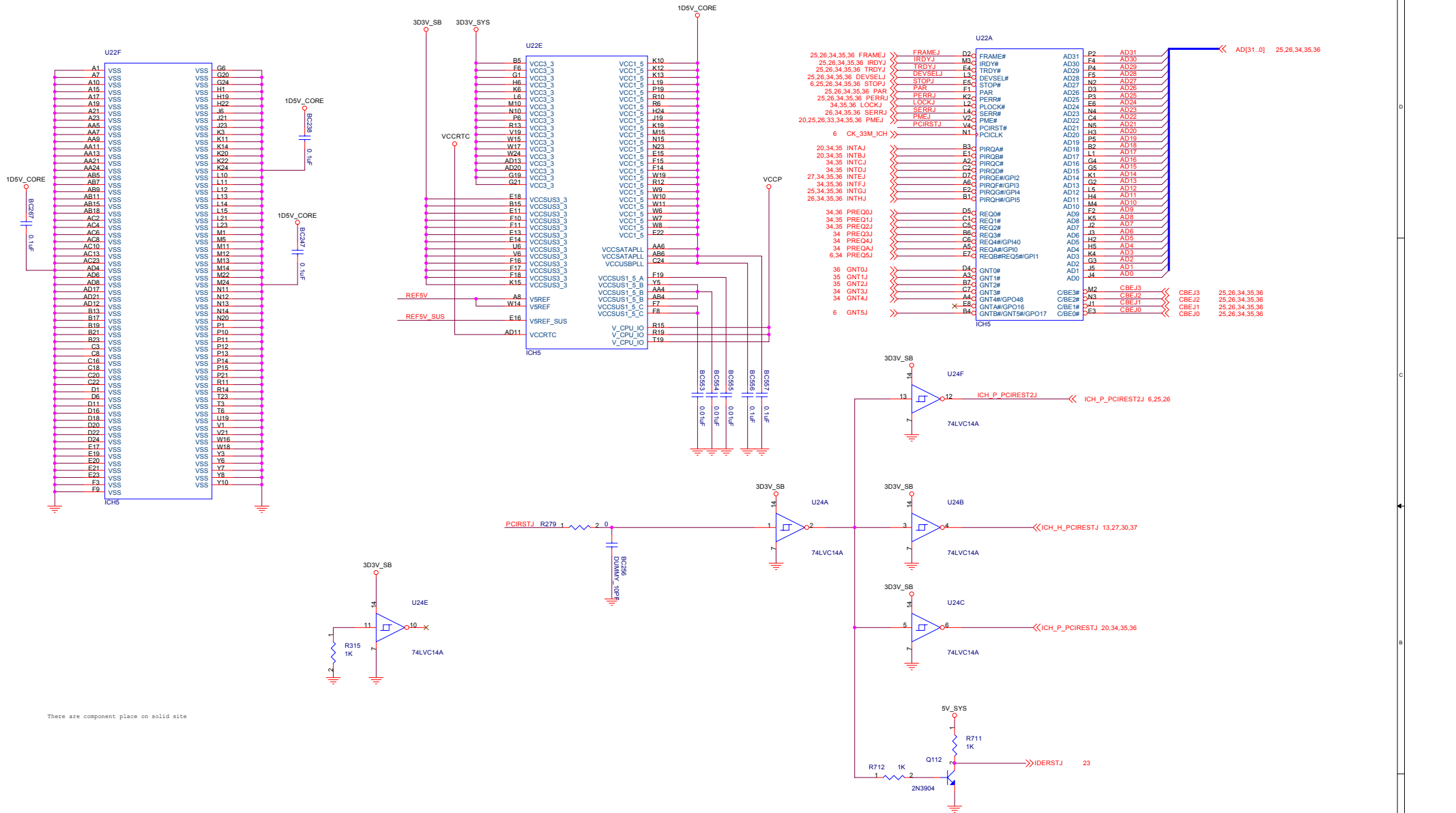
# SECOND IDE CONN



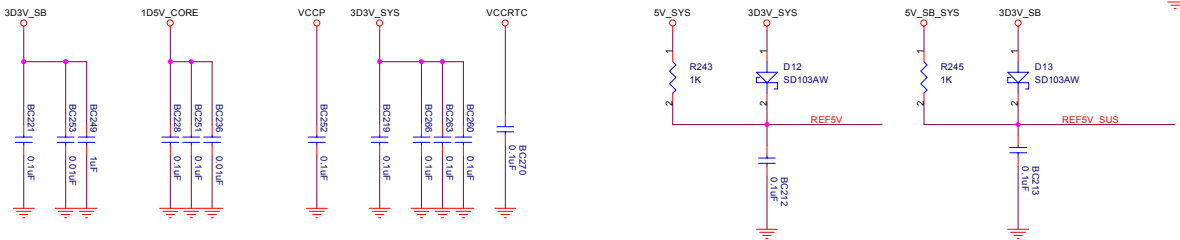
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Title		
ICH5-2 IDE Connectors		
Size	Document Number	Rev
Custom	865A01	E
Date:	Sunday, August 24, 2003	Sheet 23 of 44



There are component place on solid site



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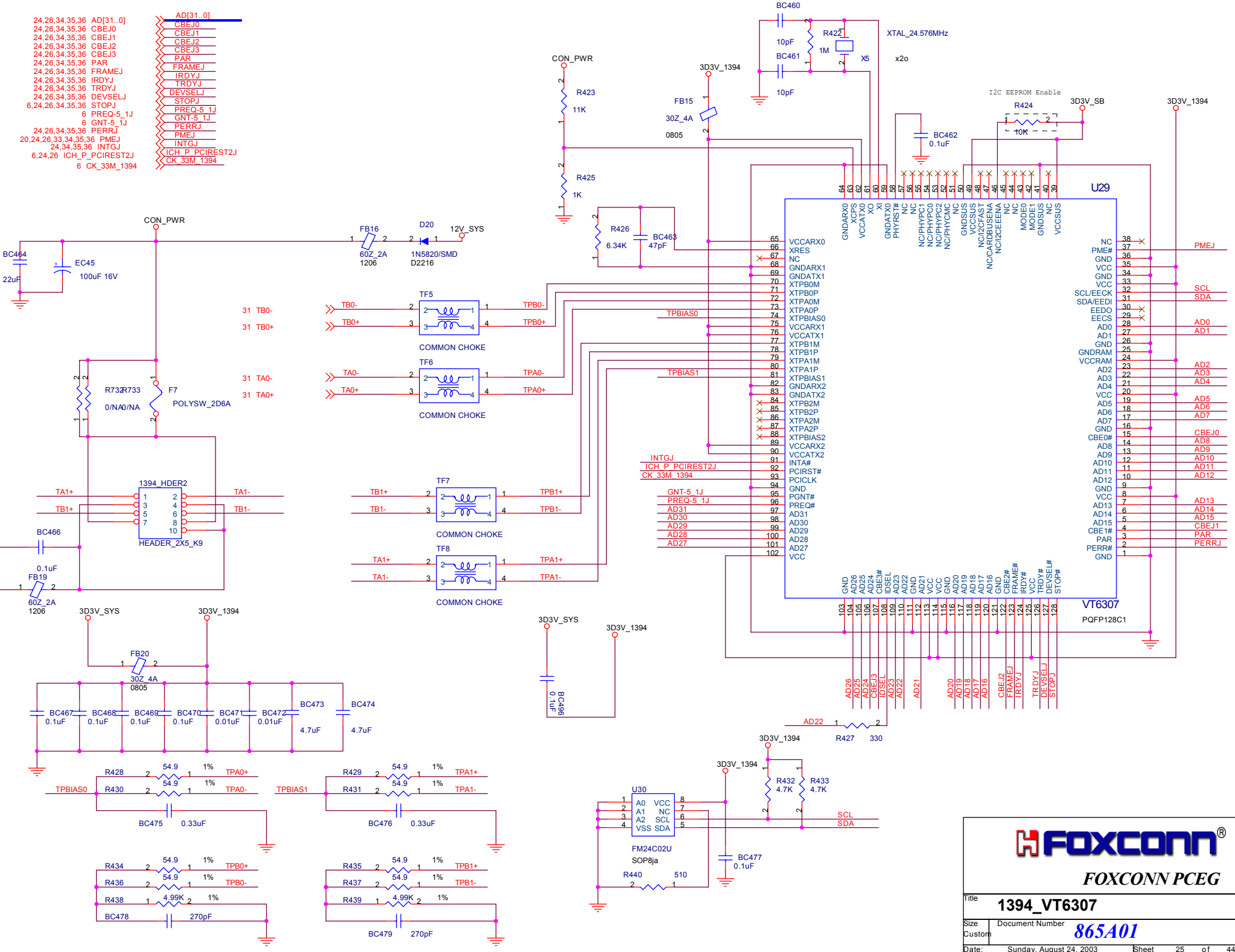
Title: ICH5-3		
Size: C	Document Number: 865A01	Rev: E
Date: Sunday, August 24, 2003	Sheet: 24	of: 44


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- 24,26,34,35,36 AD[31..0]
- 24,26,34,35,36 CBEJ0
- 24,26,34,35,36 CBEJ1
- 24,26,34,35,36 CBEJ2
- 24,26,34,35,36 CBEJ3
- 24,26,34,35,36 PAR
- 24,26,34,35,36 FRAMEJ
- 24,26,34,35,36 IRDYJ
- 24,26,34,35,36 TRDYJ
- 24,26,34,35,36 DEVSELJ
- 24,26,34,35,36 STOPJ
- 6,24,26,34,35,36 PREQ-5\_1J
- 6 GNT-5\_1J
- 24,26,34,35,36 PERRJ
- 20,24,26,33,34,35,36 PMEJ
- 24,34,35,36 INTGJ
- 6,24,26 ICH\_P\_PCIREST2J
- 6 CK\_33M\_1394

- AD[31..0]
- CBEJ0
- CBEJ1
- CBEJ2
- CBEJ3
- PAR
- FRAMEJ
- IRDYJ
- TRDYJ
- DEVSELJ
- STOPJ
- PREQ-5\_1J
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- PMEJ
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- ICH\_P\_PCIREST2J
- CK\_33M\_1394



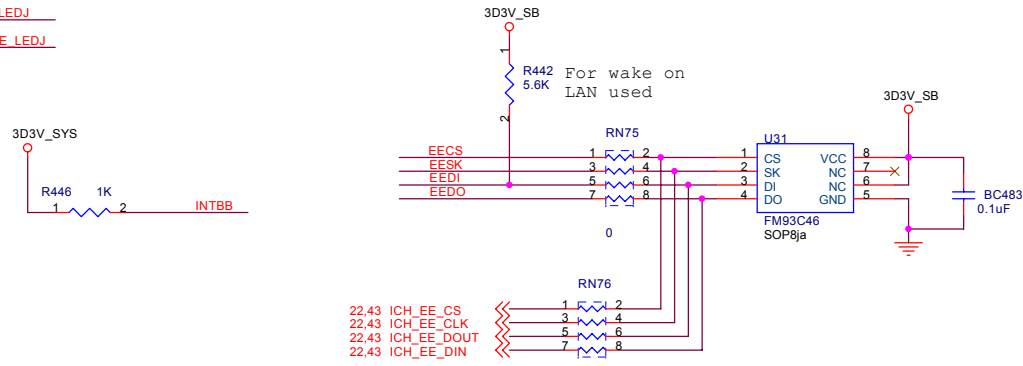
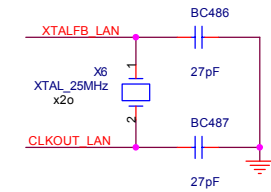
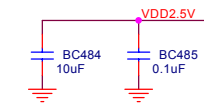
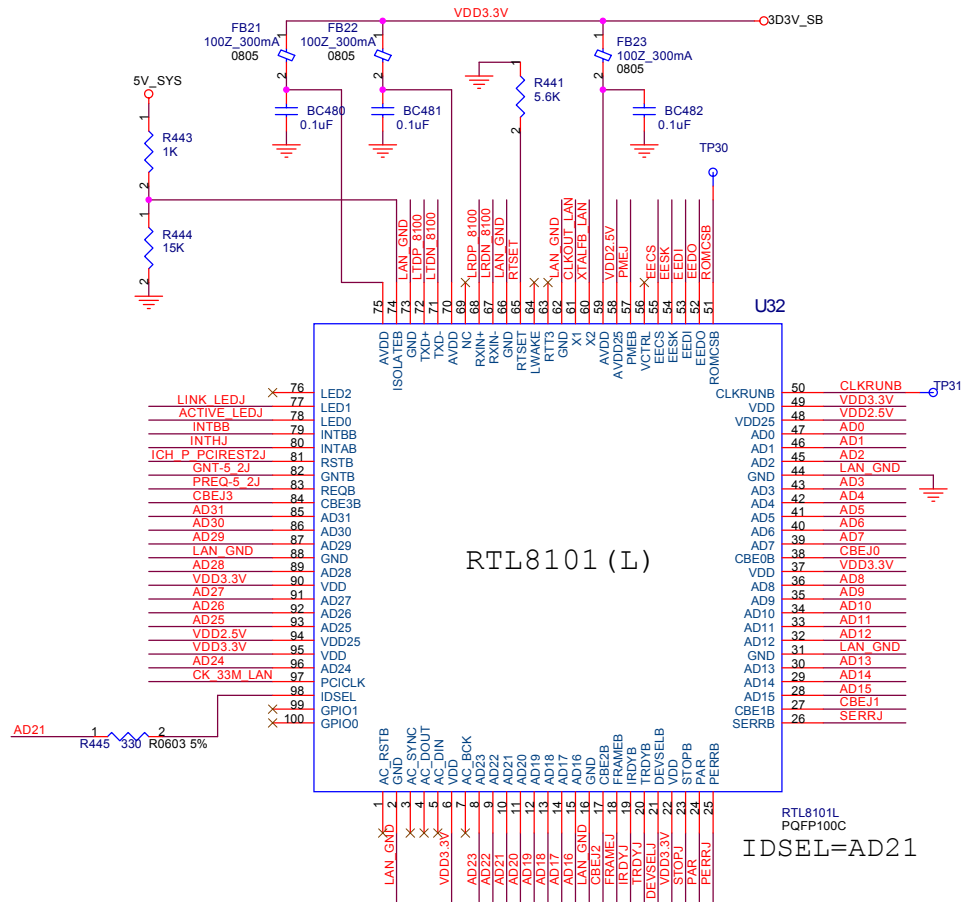


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Title		
<b>1394_VT6307</b>		
Size	Document Number	Rev
Custom	<b>865A01</b>	E
Date:	Sunday, August 24, 2003	Sheet 25 of 44

6,24,25 ICH\_P\_PCIEST2J >> ICH\_P\_PCIEST2J  
 24,25,34,35,36 AD[31..0] >> AD[31..0]  
 24,25,34,35,36 CBEJ0 >> CBEJ0  
 24,25,34,35,36 CBEJ1 >> CBEJ1  
 24,25,34,35,36 CBEJ2 >> CBEJ2  
 24,25,34,35,36 CBEJ3 >> CBEJ3  
 24,25,34,35,36 PAR >> PAR  
 24,34,35,36 SERRJ >> SERRJ  
 24,25,34,35,36 PERRJ >> PERRJ  
 6,24,25,34,35,36 STOPJ >> STOPJ  
 24,25,34,35,36 DEVSELJ >> DEVSELJ  
 24,25,34,35,36 TRDYJ >> TRDYJ  
 24,25,34,35,36 IRDYJ >> IRDYJ  
 24,25,34,35,36 FRAMEJ >> FRAMEJ  
 6 CK\_33M\_LAN >> CK\_33M\_LAN  
 24,34,35,36 INTHJ >> INTHJ  
 6 PREQ-5\_2J >> PREQ-5\_2J  
 6 GNT-5\_2J >> GNT-5\_2J  
 20,24,25,33,34,35,36 PMEJ >> PMEJ

28 LTDP\_8100 >> LTDP\_8100  
 28 LTDN\_8100 >> LTDN\_8100  
 28 LRDP\_8100 >> LRDP\_8100  
 28 LRDN\_8100 >> LRDN\_8100  
 28 LINK\_LEDJ >> LINK\_LEDJ  
 28 ACTIVE\_LEDJ >> ACTIVE\_LEDJ

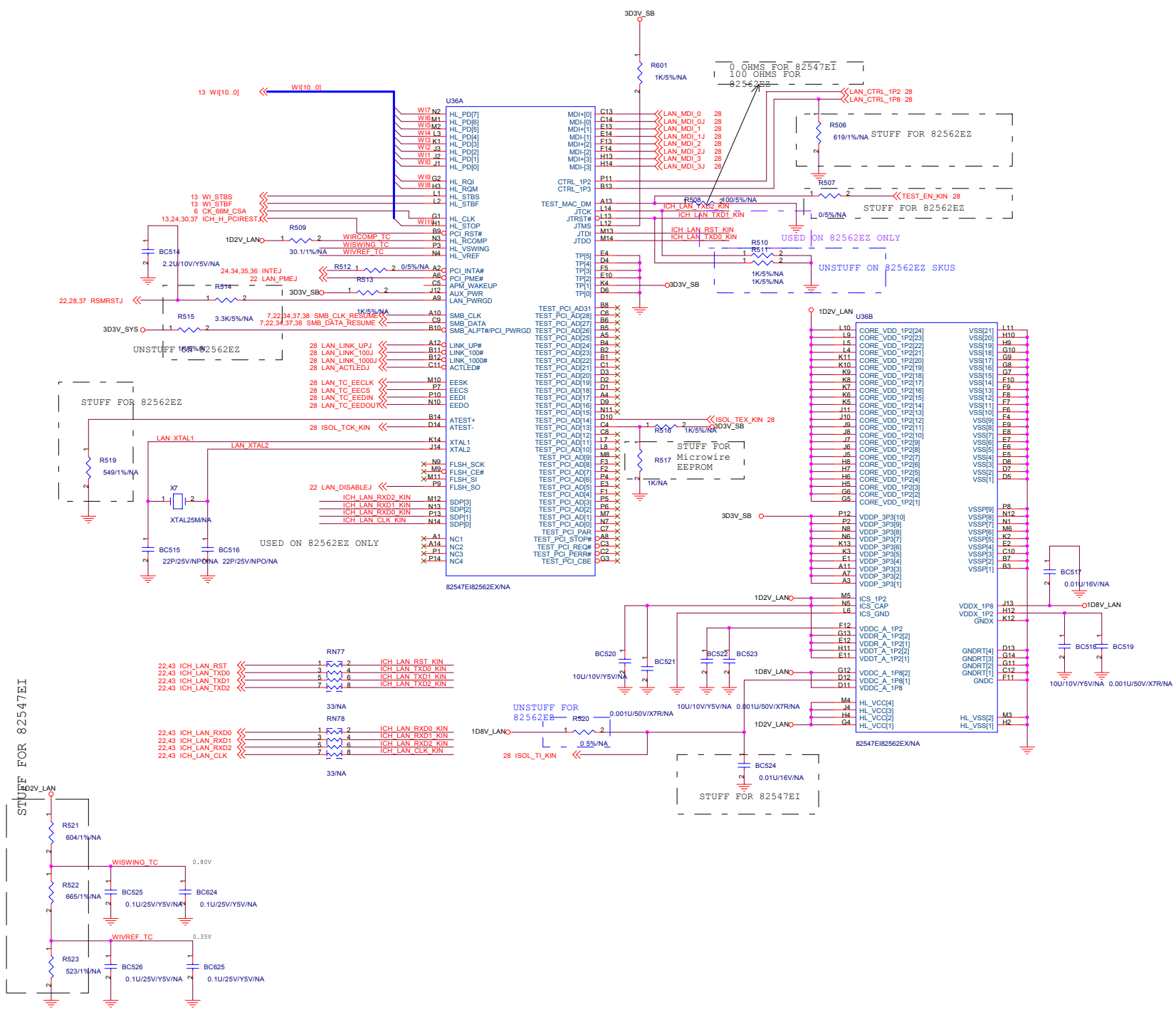


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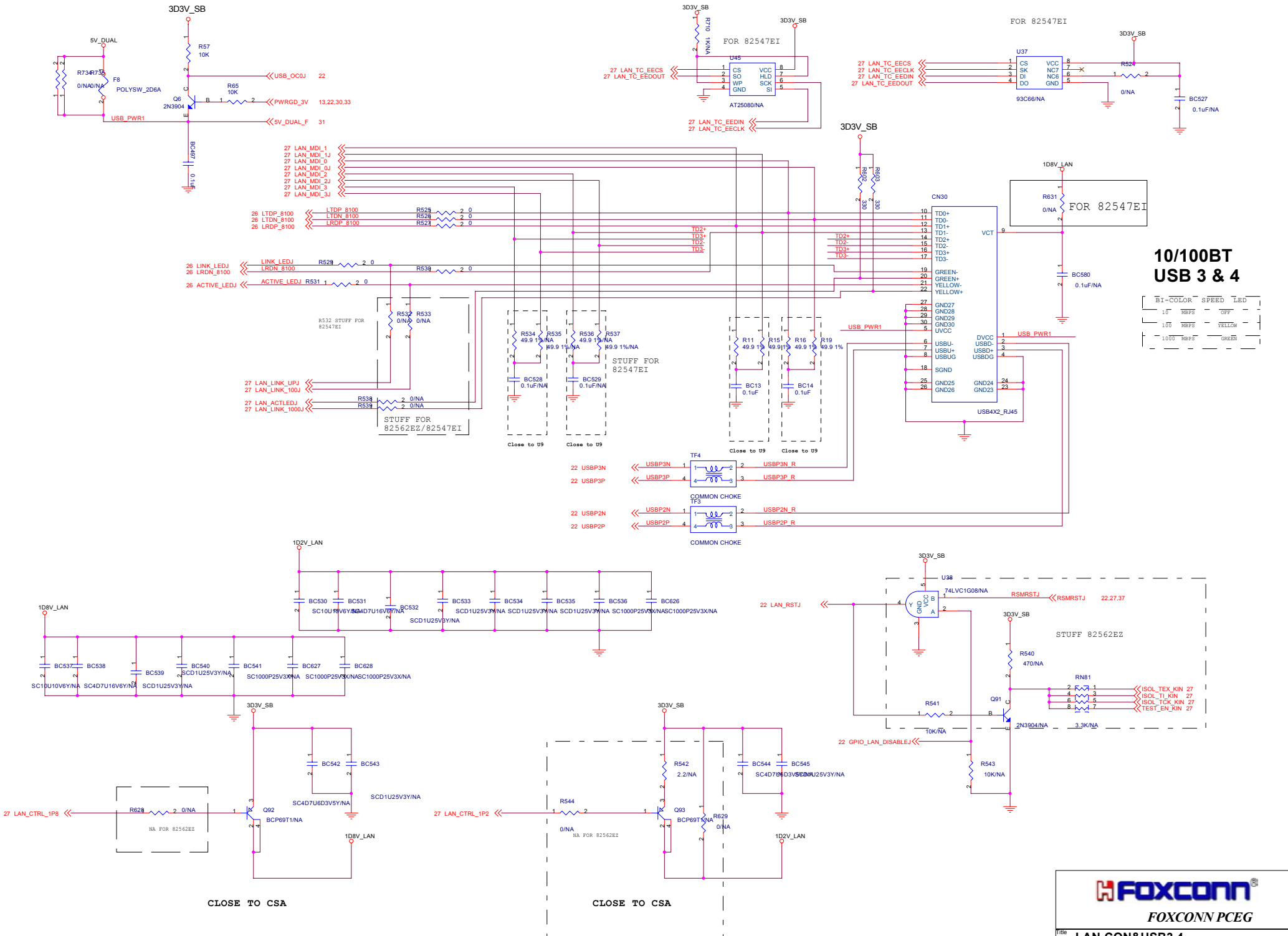
Title: LAN\_RTL8101L

Size: Custom Document Number: 865A01 Rev: E

Date: Sunday, August 24, 2003 Sheet: 26 of 44



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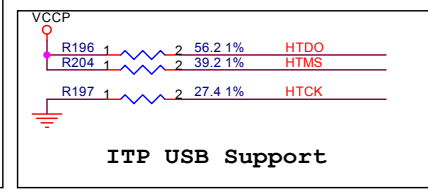
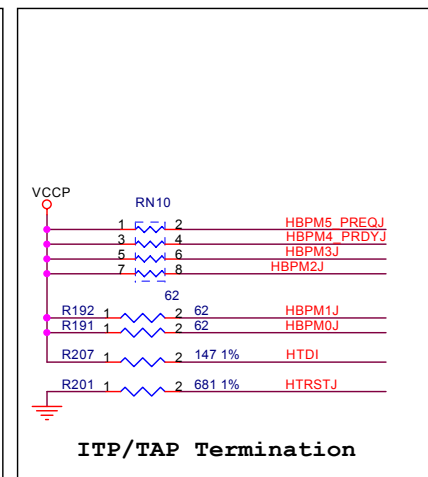
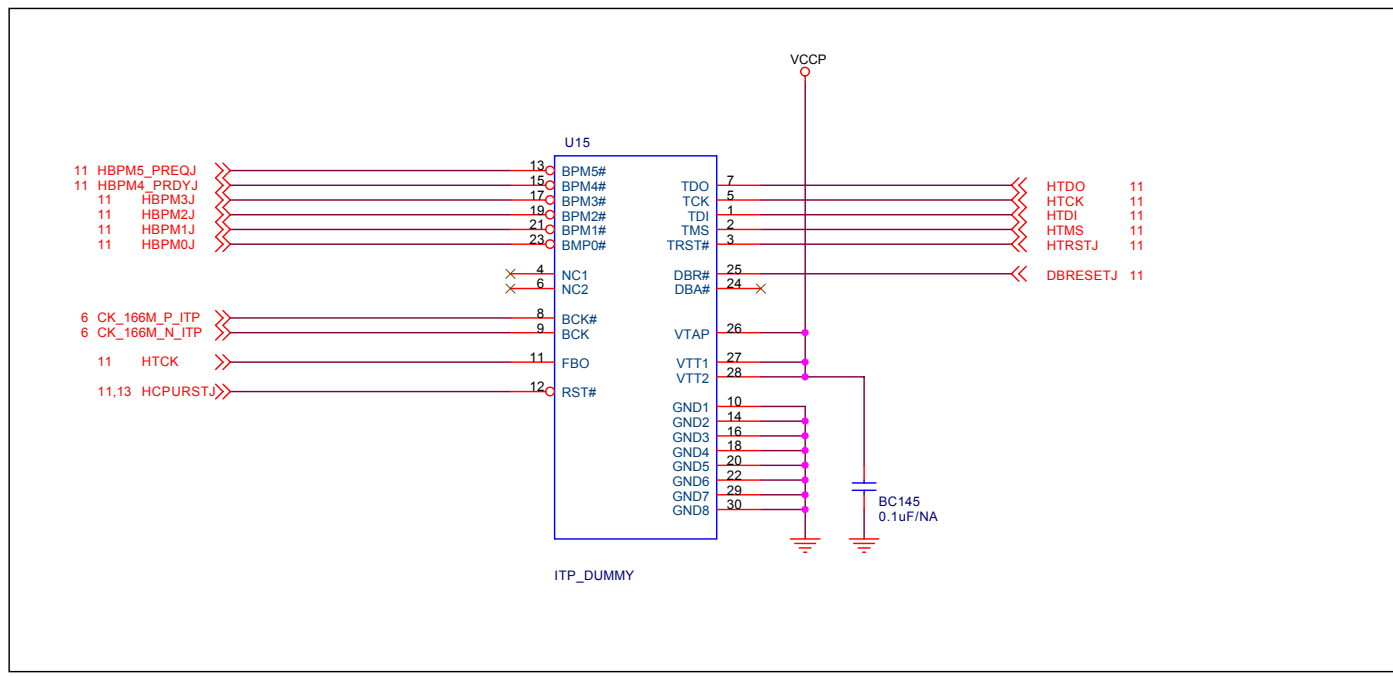
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Title: LAN CON&USB3,4

Size: Cusom Document Number: 865A01 Rev E

Date: Sunday, August 24, 2003 Sheet 28 of 44

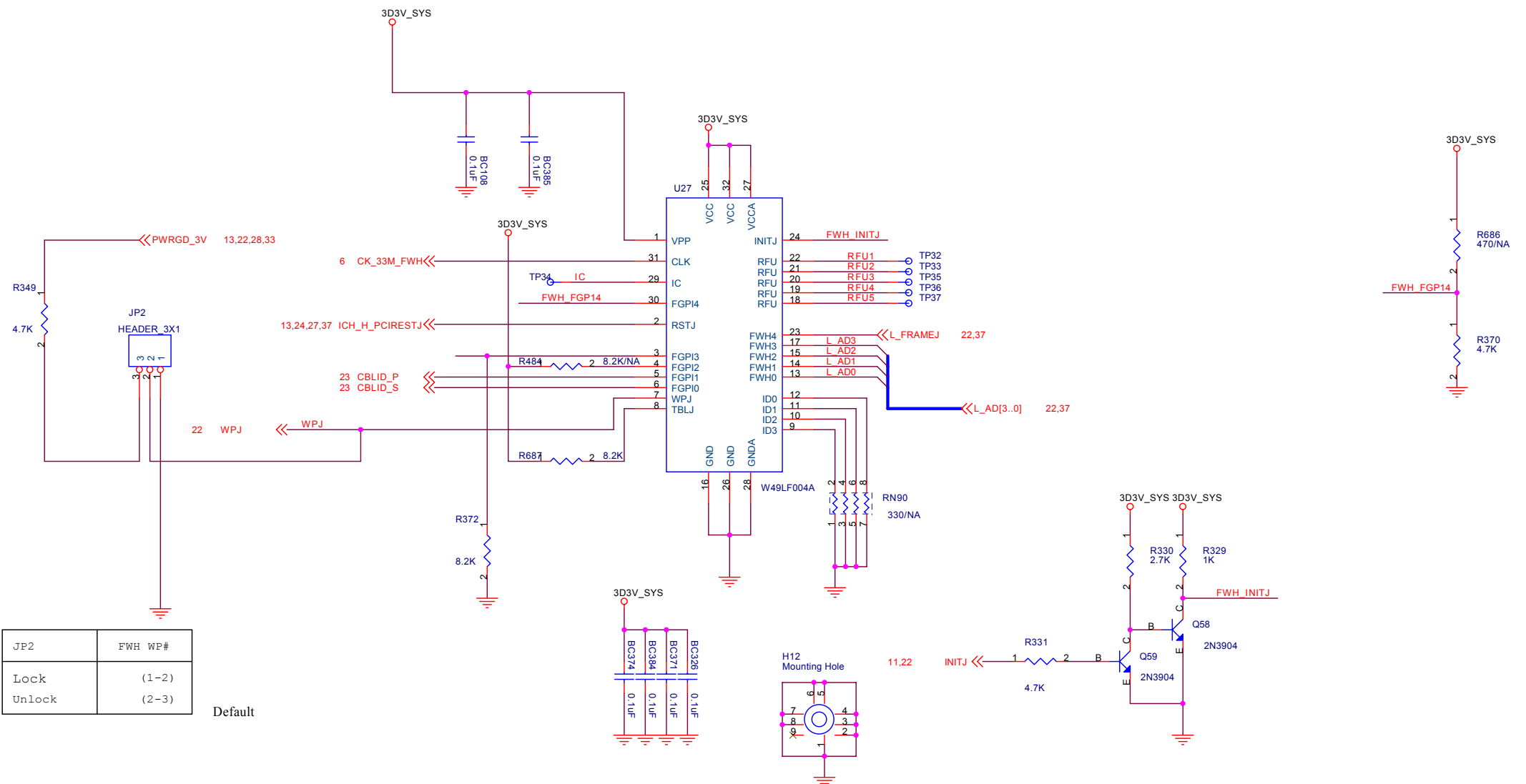
22,33 ICH\_SYS\_RSTJ >> R189 1 2 0/NA DBRESETJ



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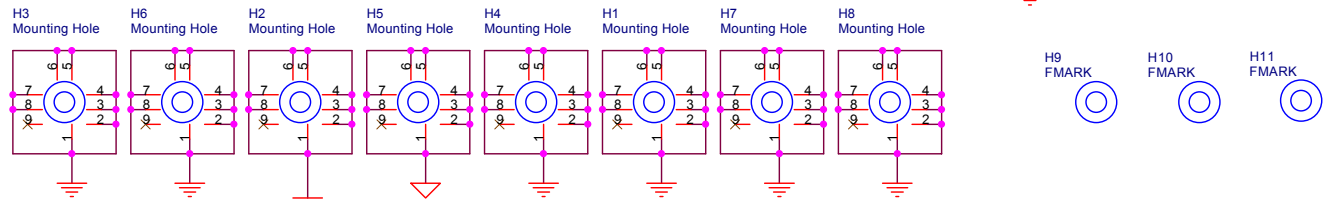
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Title		<b>ITP</b>	
Size	Document Number	<b>865A01</b>	
Date:	Sunday, August 24, 2003	Sheet	29 of 44




JP2	FWH WP#
Lock	(1-2)
Unlock	(2-3)

Default



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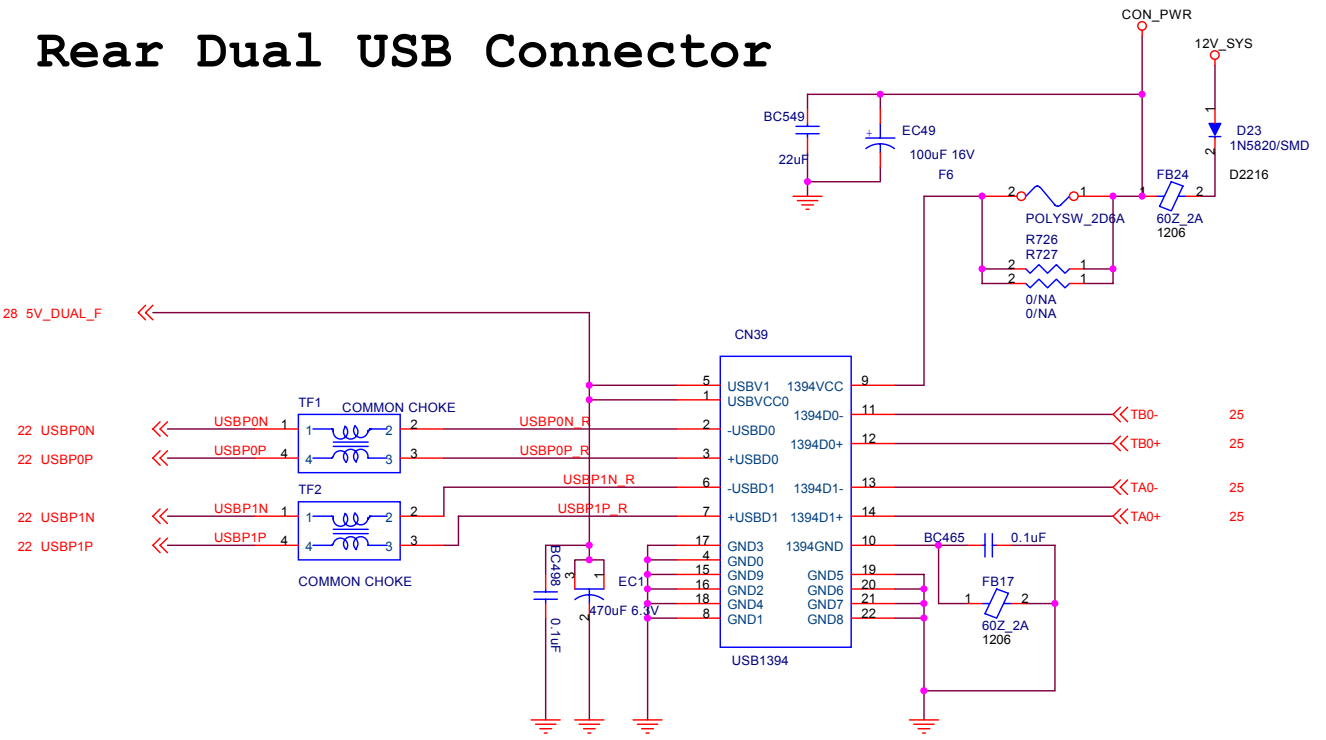
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Title <b>FWH</b>	
Size B	Document Number <b>865A01</b>
Date: Sunday, August 24, 2003	Sheet 30 of 44

# Rear Dual USB Connector

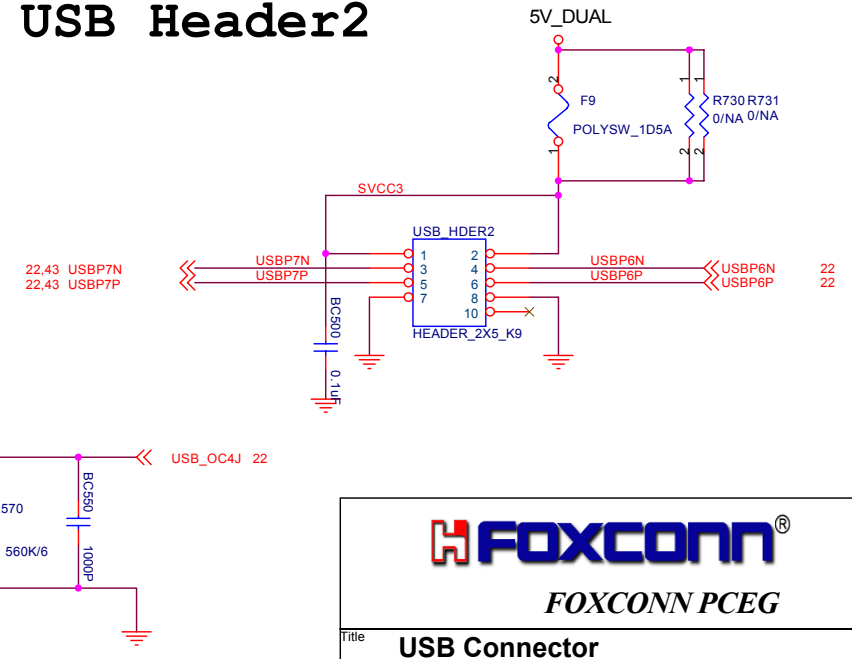
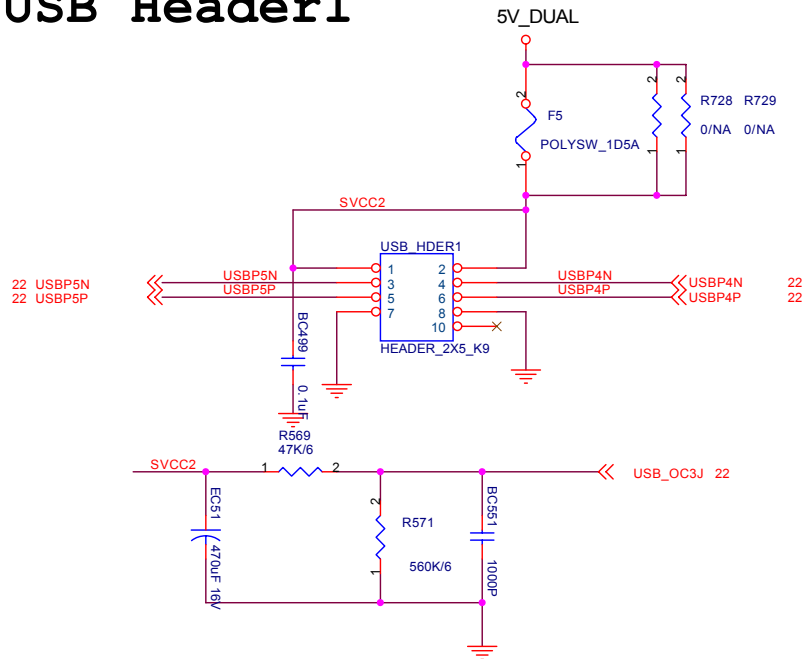
# Rear USB CONN Power

REMOVE TO FAB B



# USB Header1

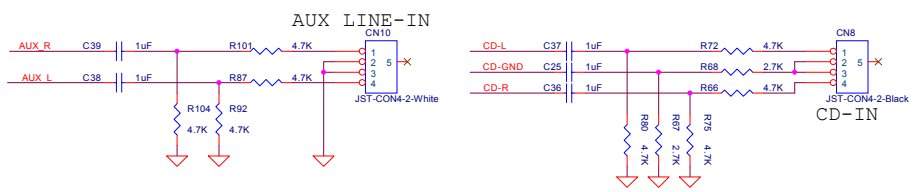
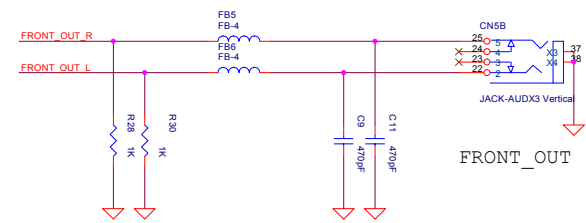
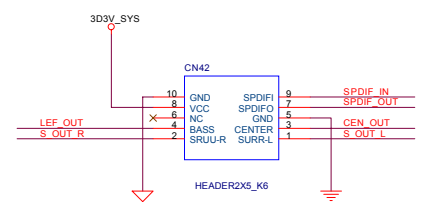
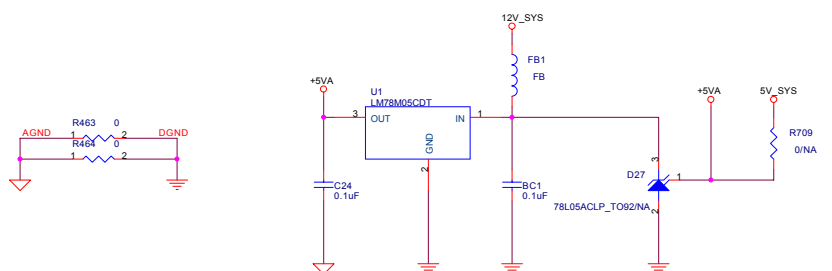
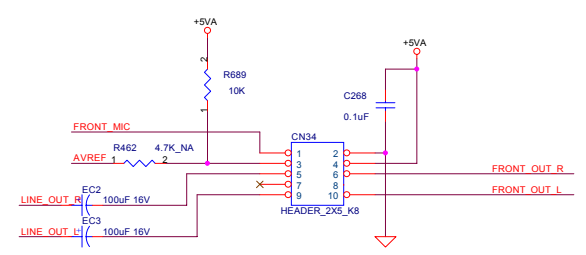
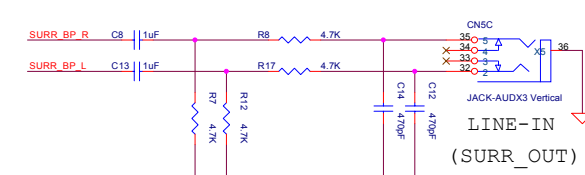
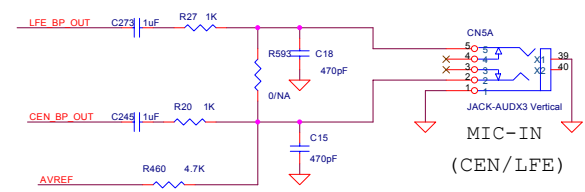
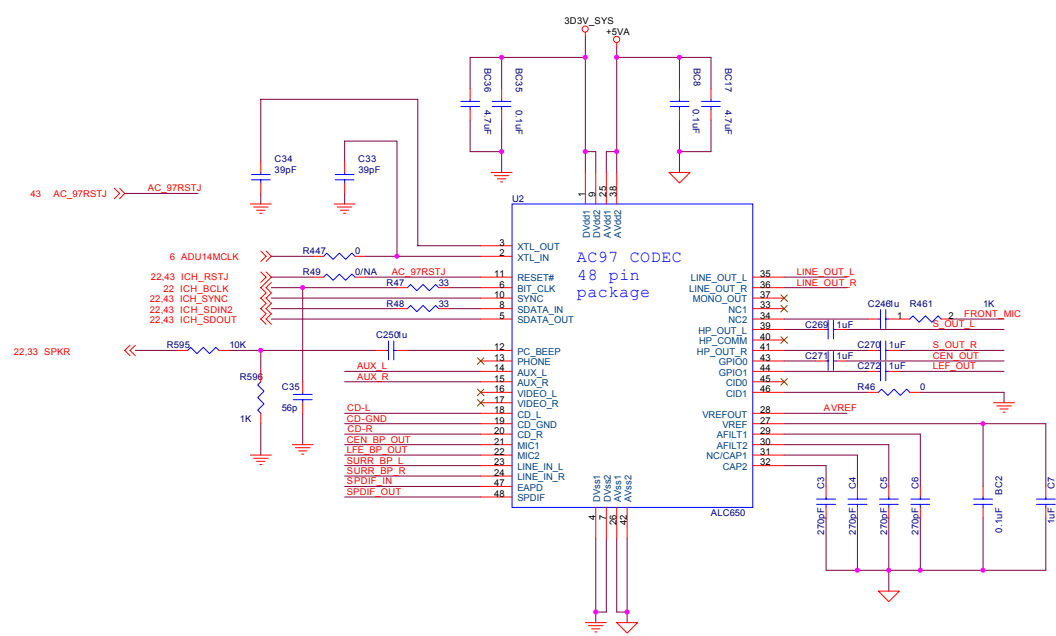
# USB Header2



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Size Custom	Document Number <b>865A01</b>	Rev E
Date: Sunday, August 24, 2003	Sheet 31	of 44



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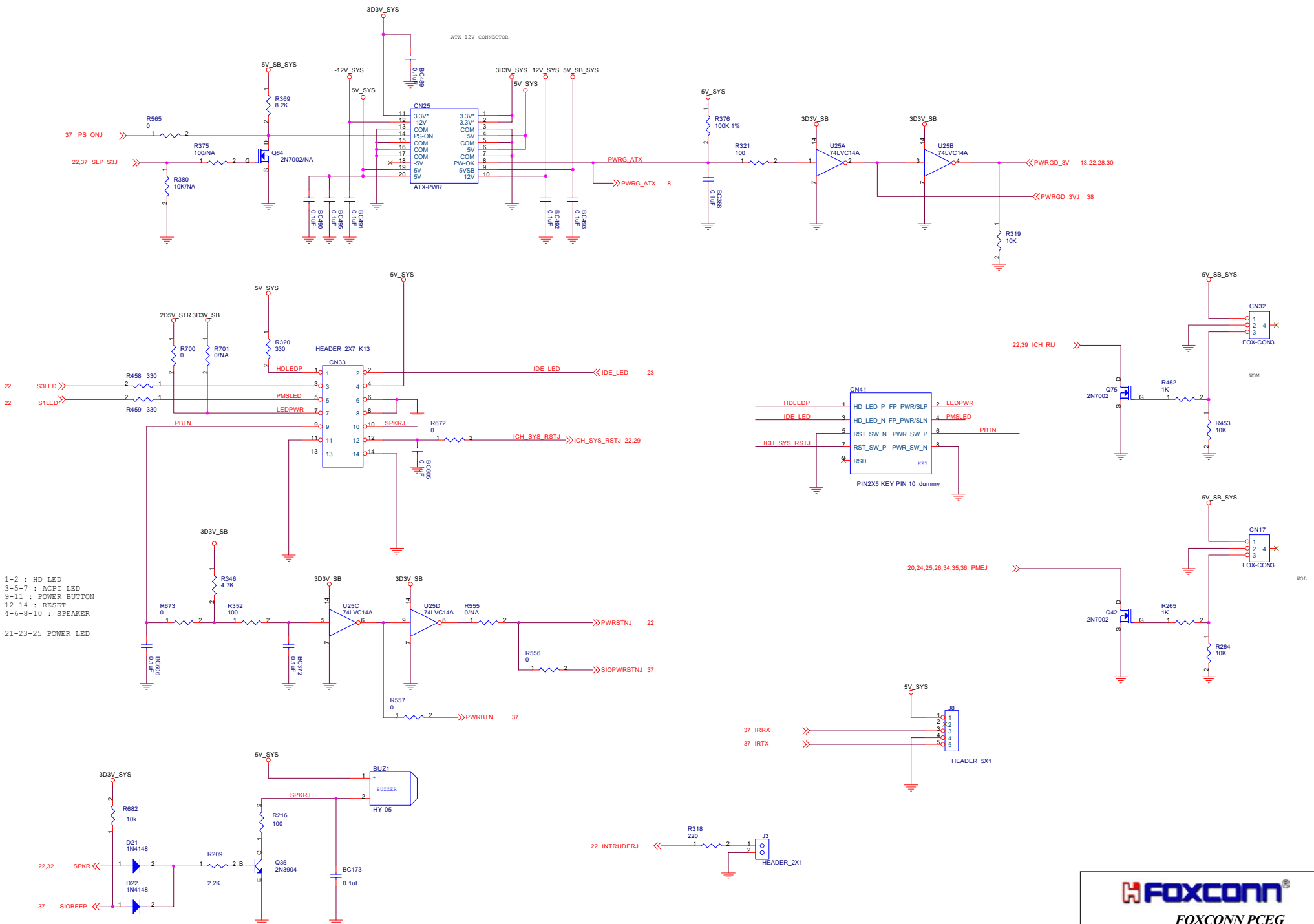
Title: **AC97 Codec**

Size: C Document Number: **865A01** Rev: E

Date: Sunday, August 24, 2003 Sheet: 32 of 44

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1-2 : HD LED  
 3-5-7 : ACPI LED  
 9-11 : POWER BUTTON  
 12-14 : RESET  
 4-6-8-10 : SPEAKER  
 21-23-25 POWER LED

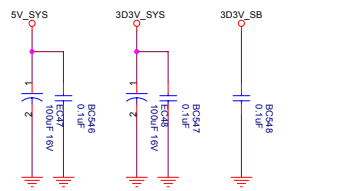
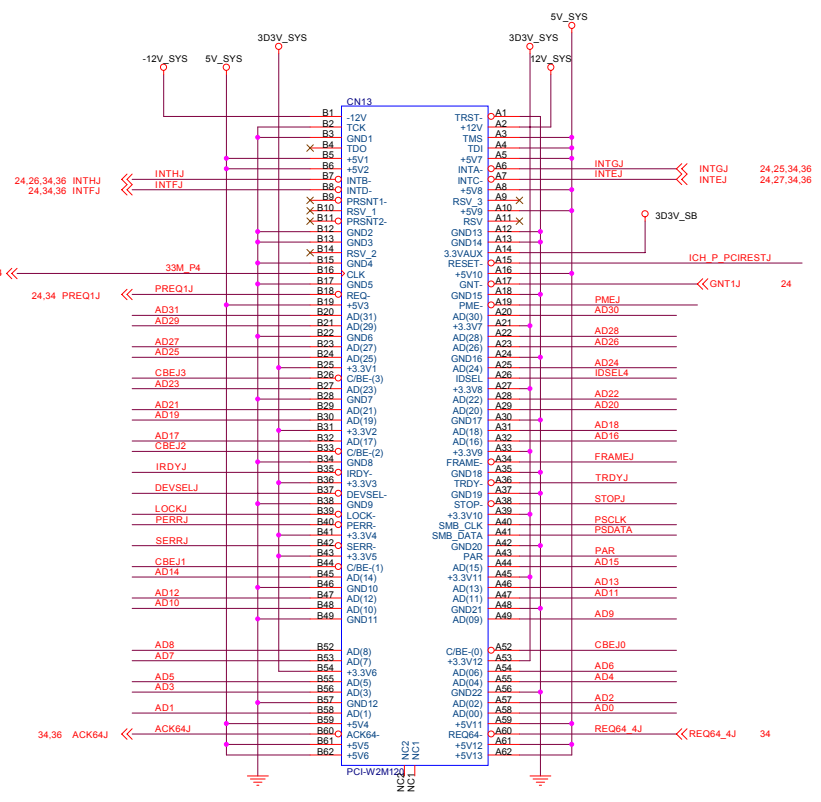
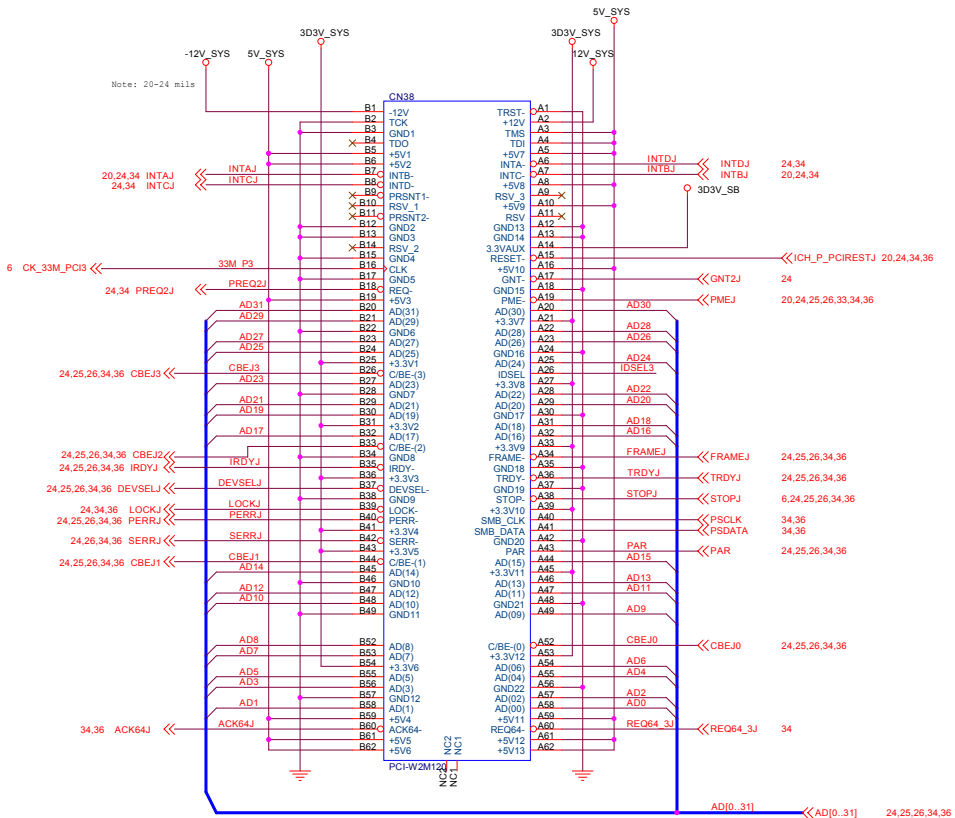
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Title: MISC Connector / ATX Power Connector

Size: C	Document Number: <b>865A01</b>	Rev: E
Date: Sunday, August 24, 2003	Sheet: 33	of: 44





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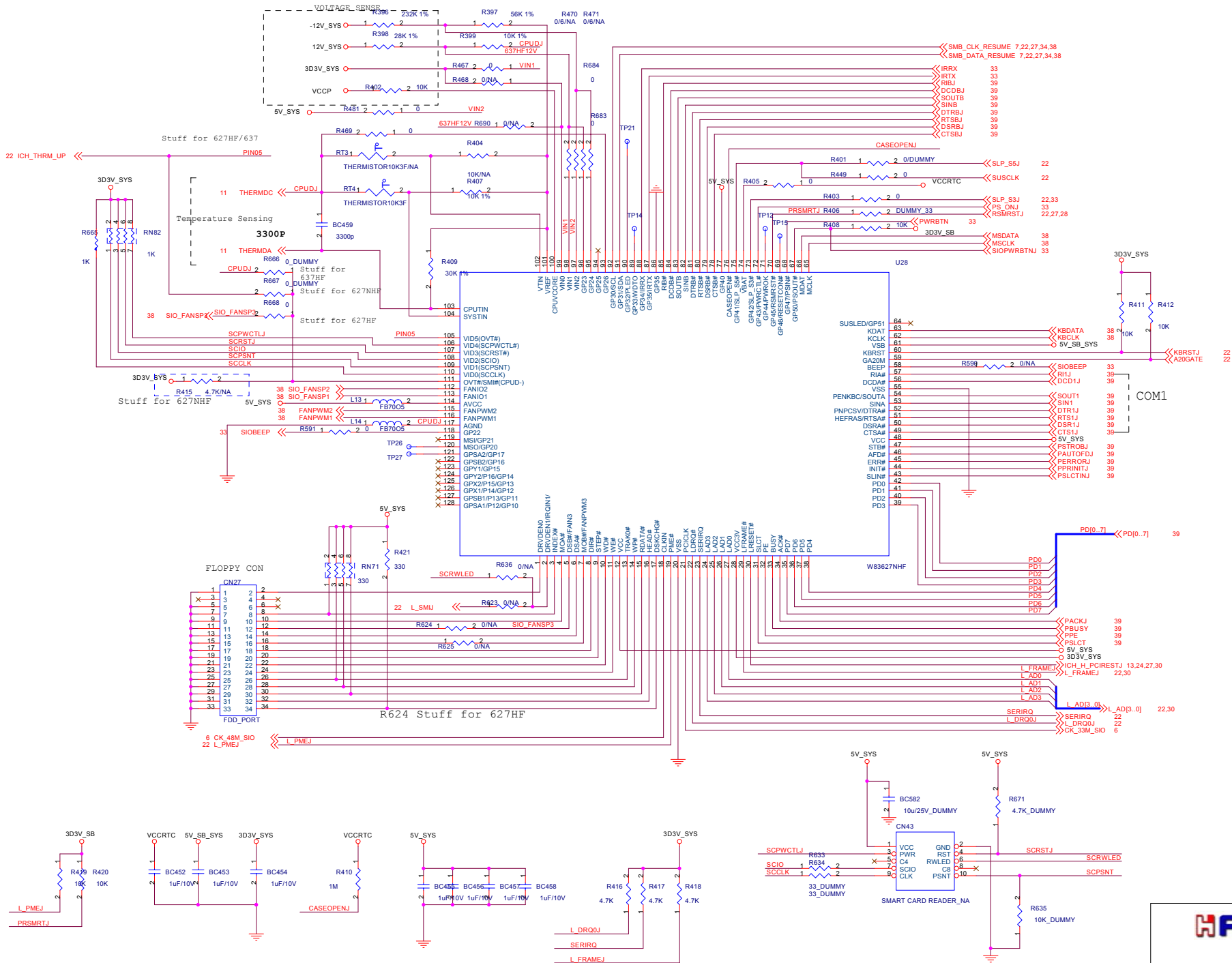
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Title: PCI SLOT 3,4

Size: Document Number 865A01

Date: Sunday, August 24, 2003 Sheet 35 of 44

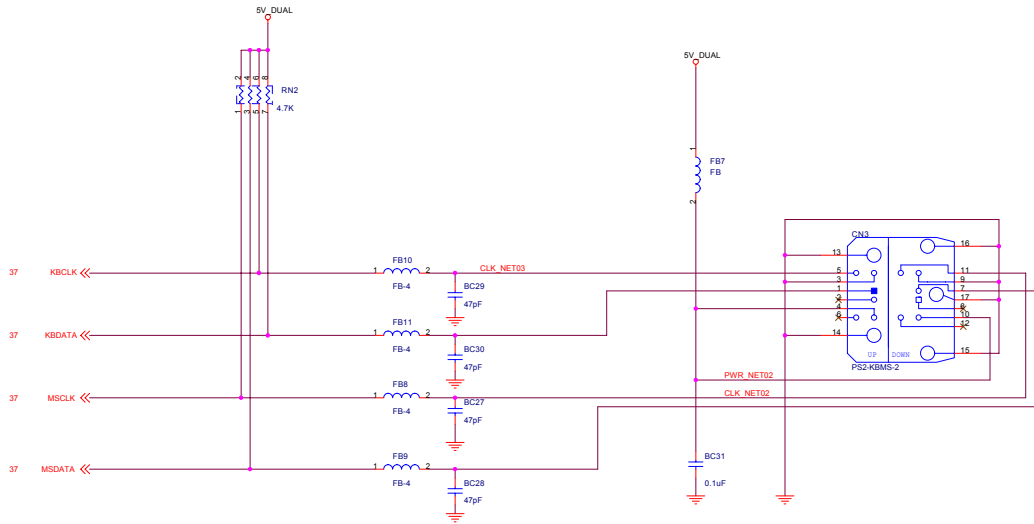
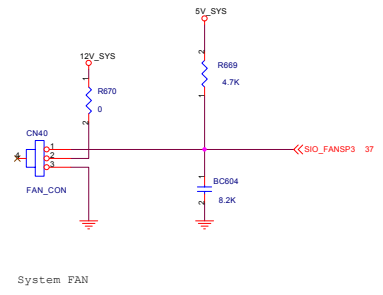
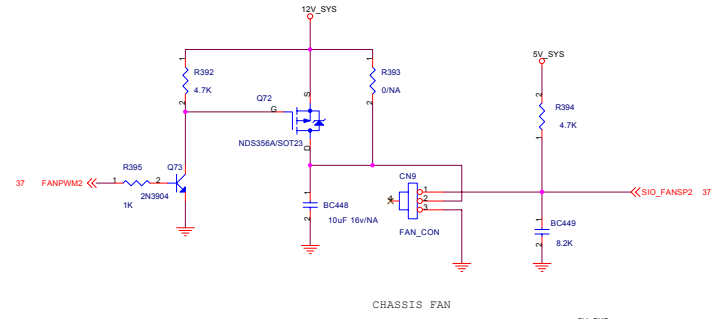
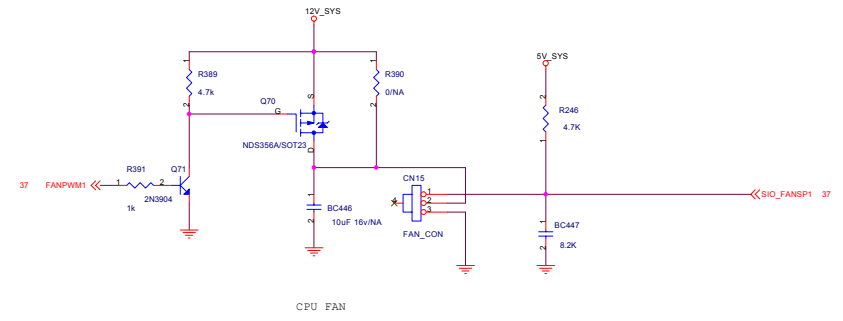
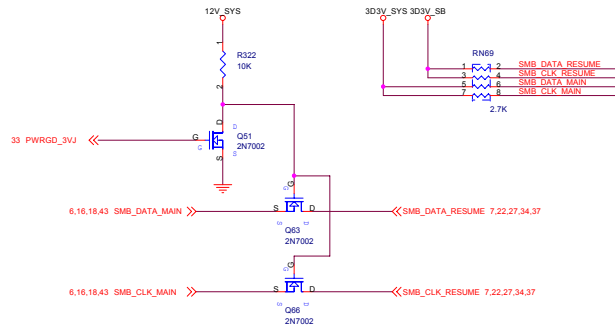




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Title		<b>SIO W83627HF</b>	
Size	Document Number	<b>885401</b>	
Date:	Sunday, August 24, 2003	Sheet	37 of 44

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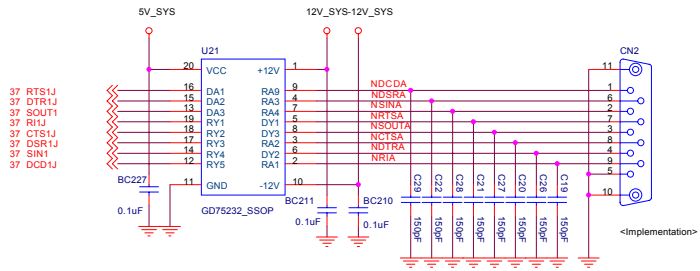
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KEYBOARD/Mouse/Fan

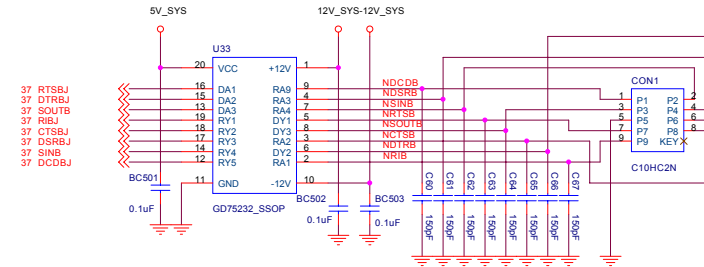
Size: Custom Document Number: 865A01 Rev: E

Date: Sunday, August 24, 2003 Sheet: 38 of 44

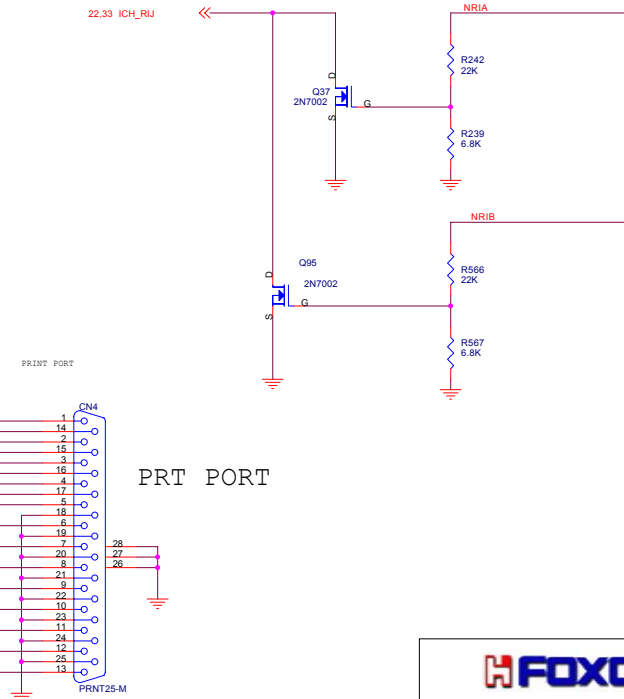
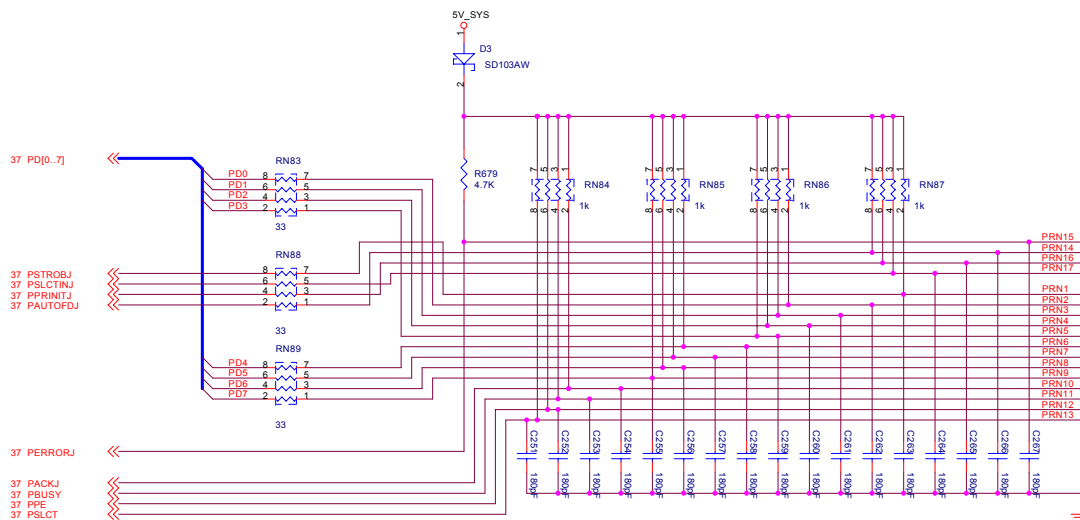
## SERIAL PORT I



## SERIAL PORT II



## PRINT PORT



# ICH5 GPIO Summary

Name	Power Plane	Type	Description
GPIO0	Main	I	REQA#
GPIO1	Main	I	REQ5#
GPIO2	Main	I	PIRQE#
GPIO3	Main	I	PIRQF#
GPIO4	Main	I	PIRQG#
GPIO5	Main	I	PIRQH#
GPIO6	Main	I	Pull_up resistor 10K(Non-use)
GPIO7	Main	I	Pull_up resistor 10K(Non-use)
GPIO8	Resume	I	LAN PME#
GPIO9	Resume	I	OC4#
GPIO10	Resume	I	OC5#
GPIO11	Resume	I	L SMIJ
GPIO12	Resume	I	LPC PME#
GPIO13	Resume	I	SLEEPJ
GPIO14	Resume	I	OC6#
GPIO15	Resume	I	OC7#
GPIO16	Main	O	GNTA#
GPIO17	Main	O	GNT5#
GPIO18	Main	O	GP018 (Debug Led)
GPIO19	Main	O	GP019 (Debug Led)
GPIO20	Main	O	GP020 (Debug Led)
GPIO21	Main	O	GP021 (Debug Led)
GPIO22	Main	OD	WPJ
GPIO23	Main	O	GP023 (Debug Led)
GPIO24	Resume	I/O	GPIO24
GPIO25	Resume	I/O	GPIO25
GPIO26			Not Implement
GPIO27	Resume	I/O	S3LED
GPIO28	Resume	I/O	S1LED
GPIO29			Not Implement
GPIO30			Not Implement
GPIO31			Not Implement
GPIO32	Main	I/O	Board ID0
GPIO33	Main	I/O	SATA LED
GPIO34	Main	I/O	Board ID1
GPIO35	N/A		Not Implement
GPIO36	N/A		Not Implement
GPIO37	N/A		Not Implement
GPIO38	N/A		Not Implement
GPIO39	N/A		Not Implement
GPIO40	Main	I	REQ4#
GPIO41	Main	I	LDRQ1#
GPIO42	N/A		Not Implement
GPIO43	N/A		Not Implement
GPIO44	N/A		Not Implement
GPIO45	N/A		Not Implement
GPIO46	N/A		Not Implement
GPIO47	N/A		Not Implement
GPIO48	Main	O	GNT4#
GPIO49	Main	OD	CPUPWRGD

# Super I/O GPIO Summary

Name	Power Plane	Type	Description
GPIO23	Main	I/OD	12V_SYS
GPIO24	Main	I/OD	-12V_SYS
GPIO30	Main	I/OD	SDA
GPIO31	Main	I/OD	SCL
GPIO34	Main	I/OD	IRRX
GPIO35	Main	I/OD	IRTX
GPIO41	Resume	I/OD	SUSCLK
GPIO42	Resume	I/OD	SLP_S3#
GPIO43	Resume	I/OD	PWRCTL#
GPIO45	Resume	I/OD	RSMRST#
GPIO47	Resume	I/OD	PSIN#
GPIO50	Resume	I/O	PSOUT#
GPIO51	Resume	I/O	SUSLED

# FWH GPIO Summary

Name	Power Plane	Type	Description
FGPIO	Main	I	IDE2 Detect 33/66/100
FGPI1	Main	I	IDE1 Detect 33/66/100
FGPI2	Main	I	Unused
FGPI3	Main	I	Unused

# PCI Routing Summary

	AGP	PCI1	PCI2	PCI3	PCI4	PCI5	CSA LAN
INTA#	A	D	C	B			
INTB#	B	A	D	C			
INTC#		B	A	D			
INTD#		C	B	A			
INTE#					C	D	
INTF#					D	A	
INTG#					A	B	
INTH#					B	C	
REG#/GNT#		4	3	2	1	0	
IDSEL		20	19	18	17	16	

PCI Dev	Interrupt	Req/Gnt	ID Select
PCI1	BCDA	4	AD20
PCI2	CDBA	3	AD19
PCI3	DABC	2	AD18
PCI4	GHEF	1	AD17
PCI5	FGHE	0	AD16



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Title: <b>GPIO / IRQ / IDESEL Map</b>		
Size: C	Document Number: <b>865A01</b>	Rev: E
Date: Sunday, August 24, 2003	Sheet: 40	of 44



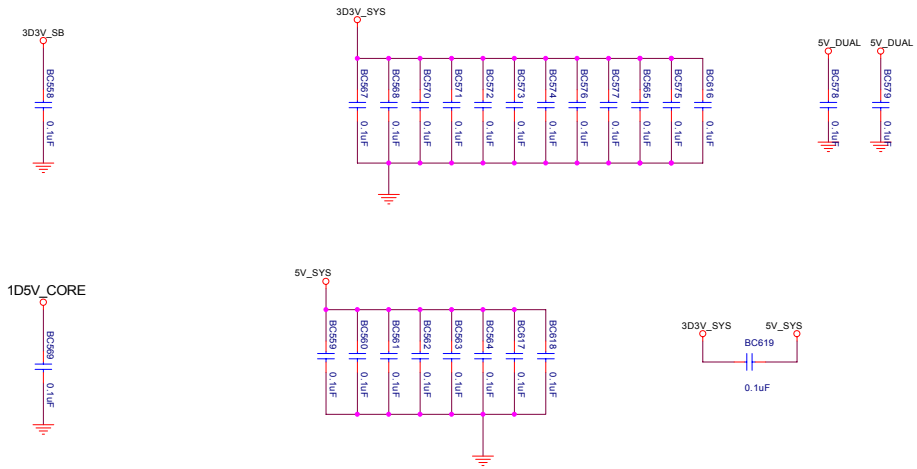
# Jumper Setting Summary

JP5	BIOS Recovery 1-2 : Normal (Default) 2-3 : Safe Mode Open: BIOS Recovery
JP3	Clear CMOS 1-2 : Normal (Default) 2-3 : Clear CMOS
CN18	Chassis Intruder 1 : Intruder 2 : GND
CN21	Wake On LAN 1 : 5V Standby Power 2 : GND 3 : Detect
CN20	Front Plane Header ( 2X9 Key14 ) 1-3 : HDD LED 2-4 : Power LED 5-7 : Reset Switch 6-8 : Power Switch 10 : Chassis ID0 17 : Chassis ID1

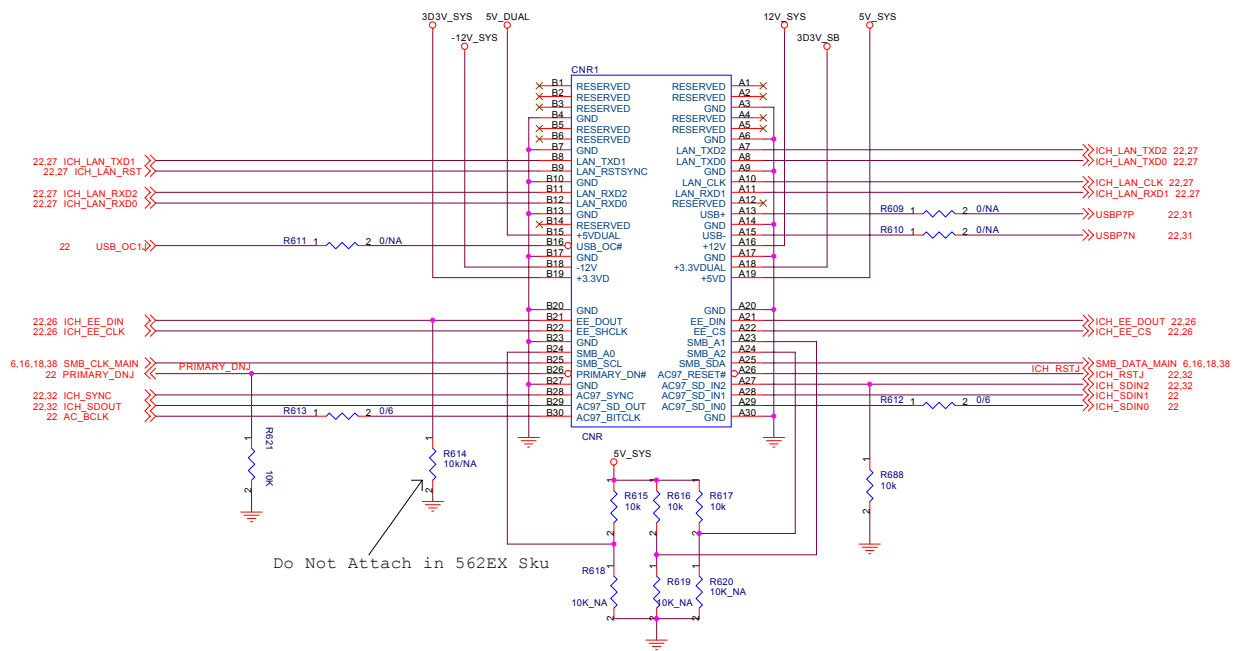
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Title: Jumper Setting		
Size: C	Document Number: 865A01	Rev: E
Date: Sunday, August 24, 2003 Sheet 41 of 44		

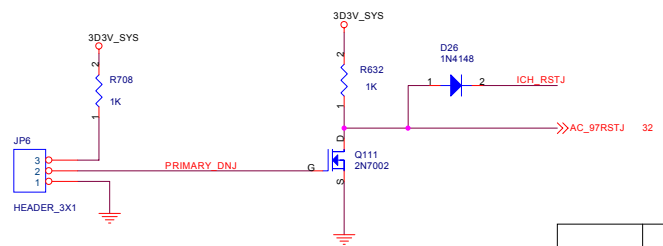
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Title <b>Modify List</b>		
Size C	Document Number <b>865A01</b>	Rev E
Date: Sunday, August 24, 2003	Sheet 42 of 44	



CNR




2-3	enable CNR audio
1-2	enable PRIMARY audio

ON\_BOARD\_AC97\_DISABLE\_CIRCUITRY



File		CNR	
Size	Custom	Document Number	865A01
Date:	Sunday, August 24, 2003	Sheet	43 of 44

8/21 Change VCCVID\_GD pull-up voltage to VCCVID.  
NA R661,R646.

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Title		
Size	Document Number	Rev
C	<b>865A01</b>	E
Date: Sunday, August 24, 2003 Sheet 44 of 44		

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