

Foxconn Precision Co. Inc.

865A05 Schematic

Fab B

Date: 2003/08/025

1. REVISION LIST:

REVISION	TOTAL PAGES	MODIFIED PAGES	ERRATA NO.	DATE
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B				
C				
D				

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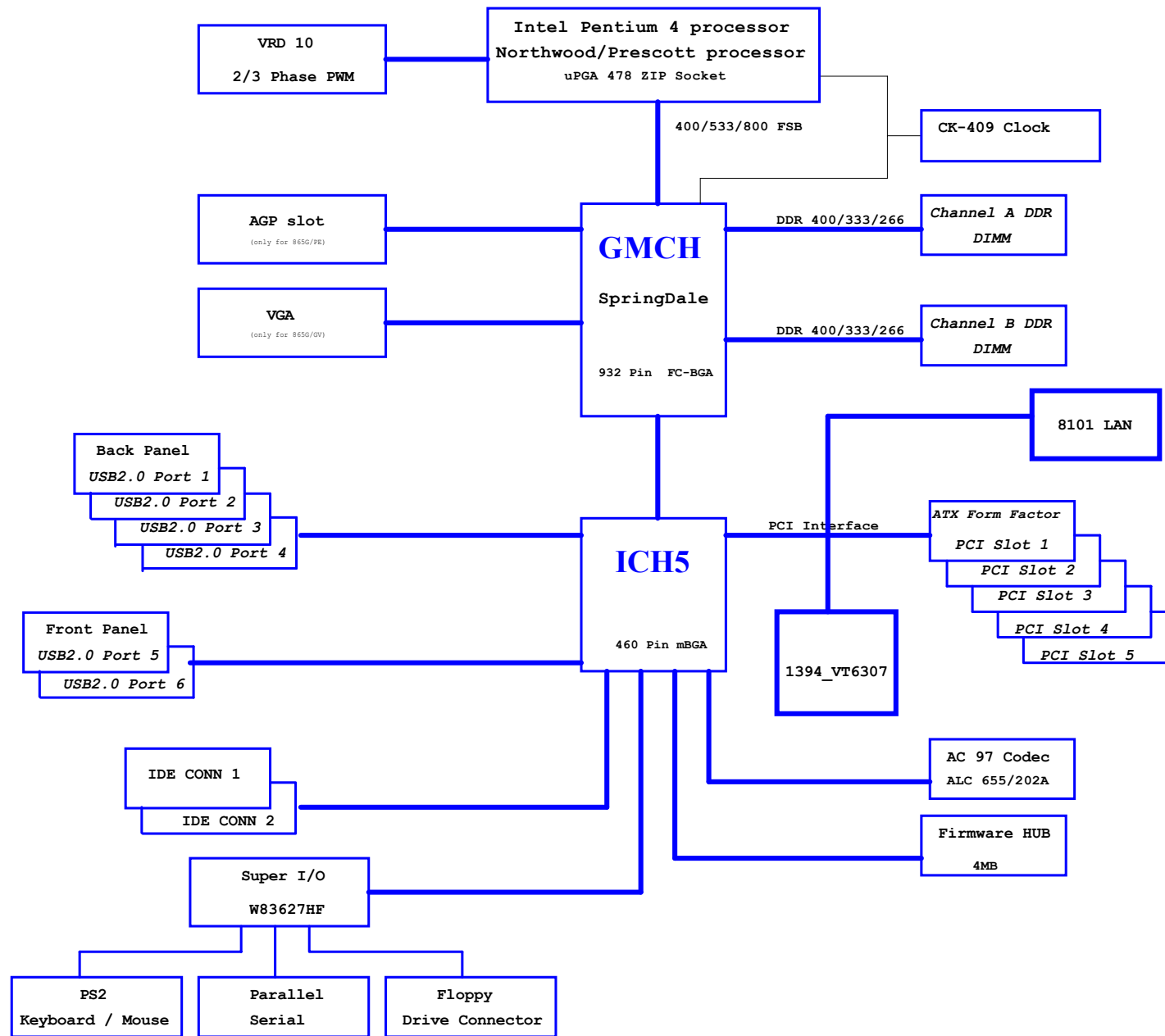
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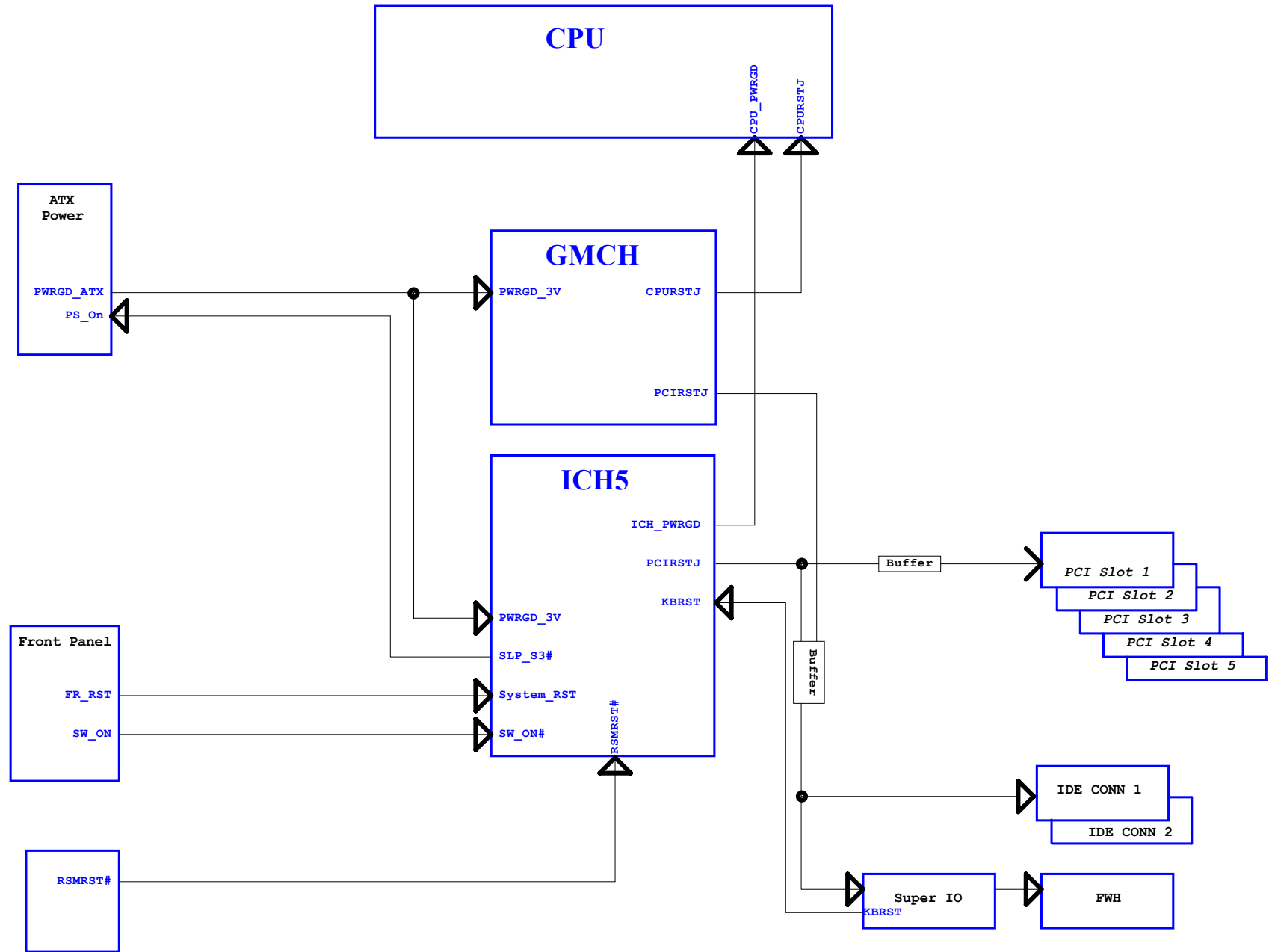
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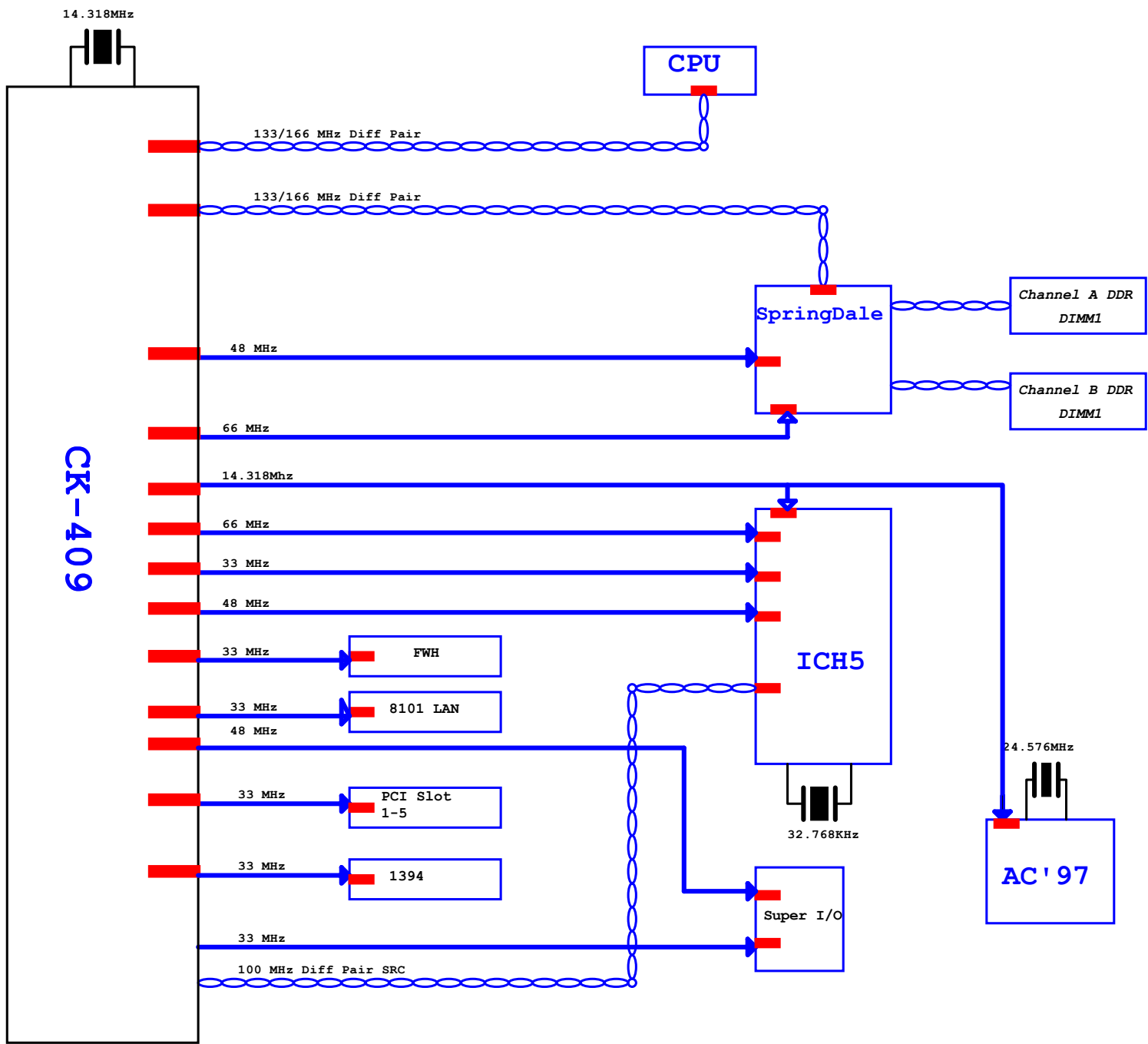
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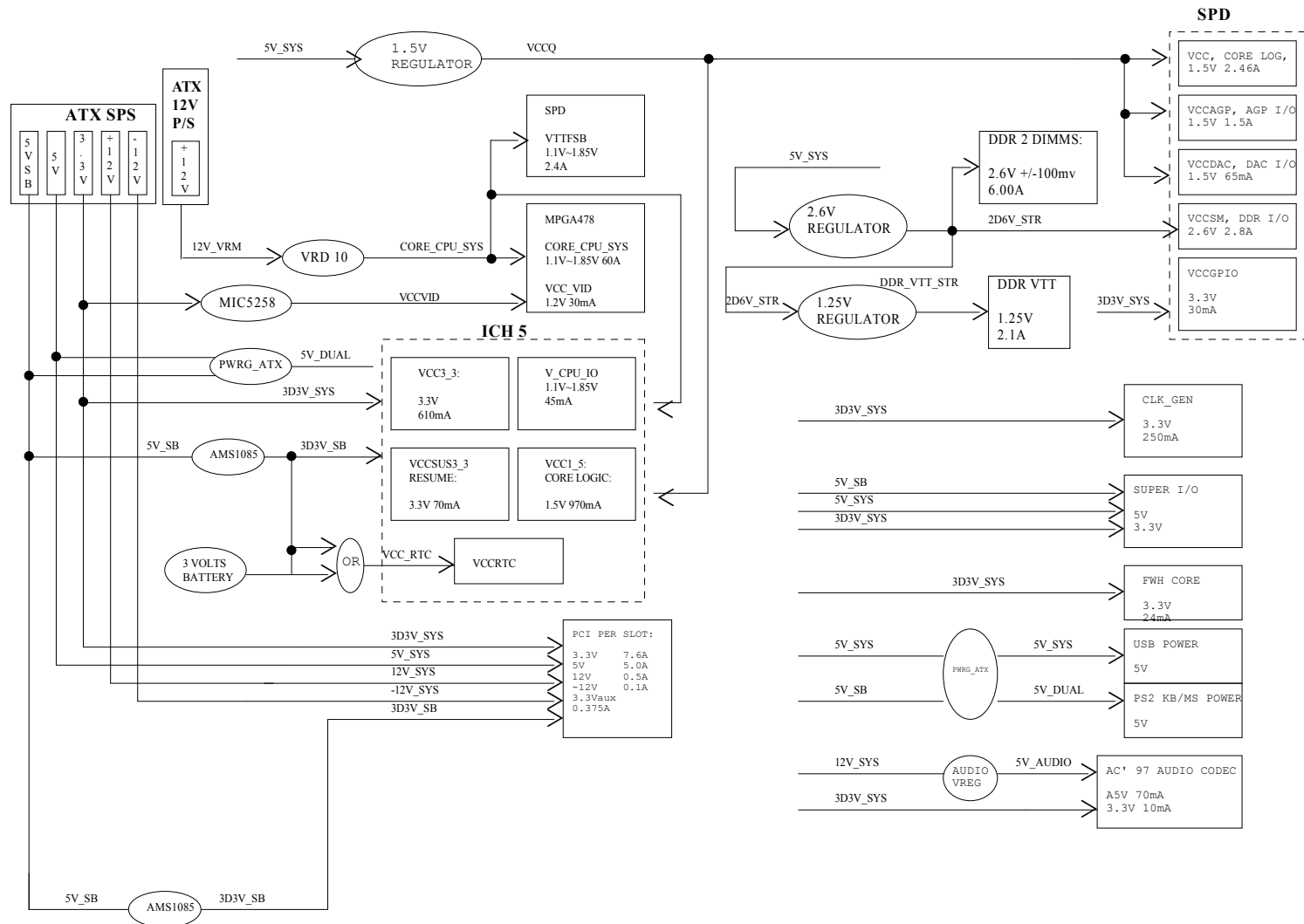
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Title: Power Delivery Map	
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3D3V_SYS

FB, 300ohm@100MHz, L0805, P-TYPE, RDC<0.3.ohm, IDC>=1A

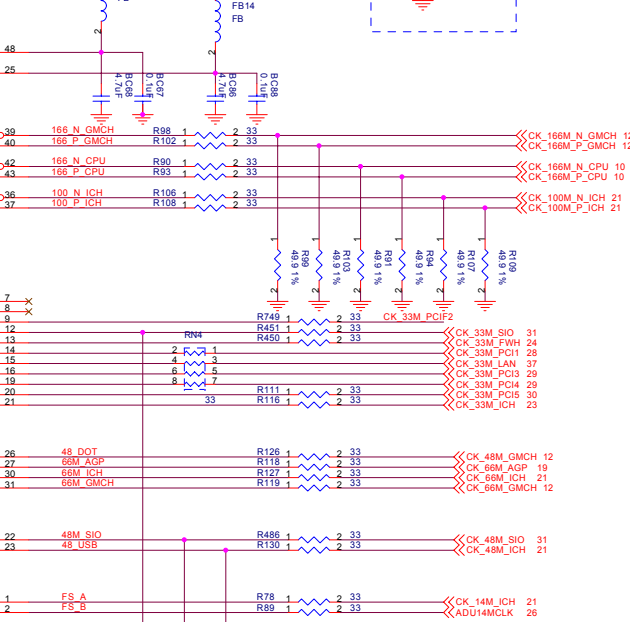
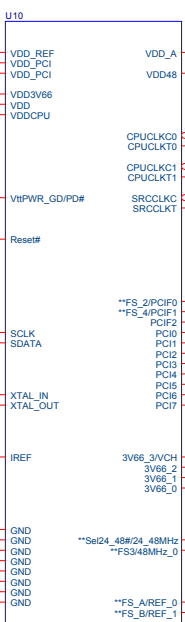
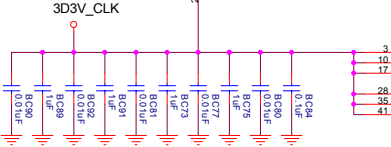
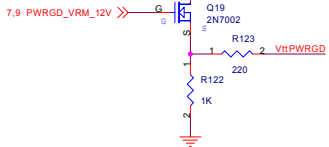
3D3V_CLK

3D3V_SYS

3D3V_SYS

3D3V_SYS

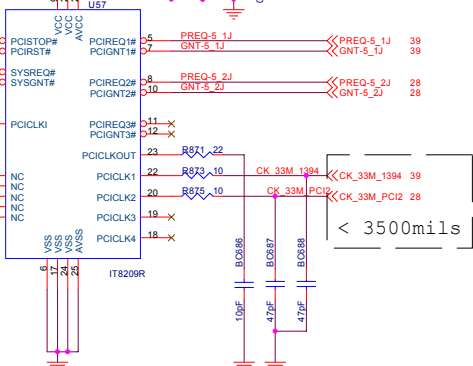
For BHI



3D3V_SYS

PCI Arbiter

12,19,23,24,28,29,30,31,37,39 ICH_H_PCIE_RST#



23,28 PREQ5J GNT5J

23,28 PREQ5J GNT5J

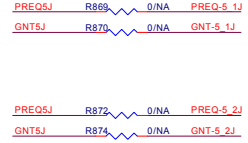
< 16inch

< 7500mils

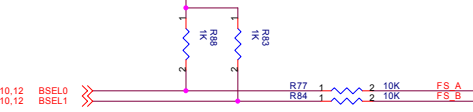
CK_33M_PCIE2

CK_33M_PCIE2 R876 0/NA CK_33M_1394 R877 0/NA CK_33M_PCIE2

CK_33M_PCIE2 R876 0/NA CK_33M_1394 R877 0/NA CK_33M_PCIE2



3D3V_CLK

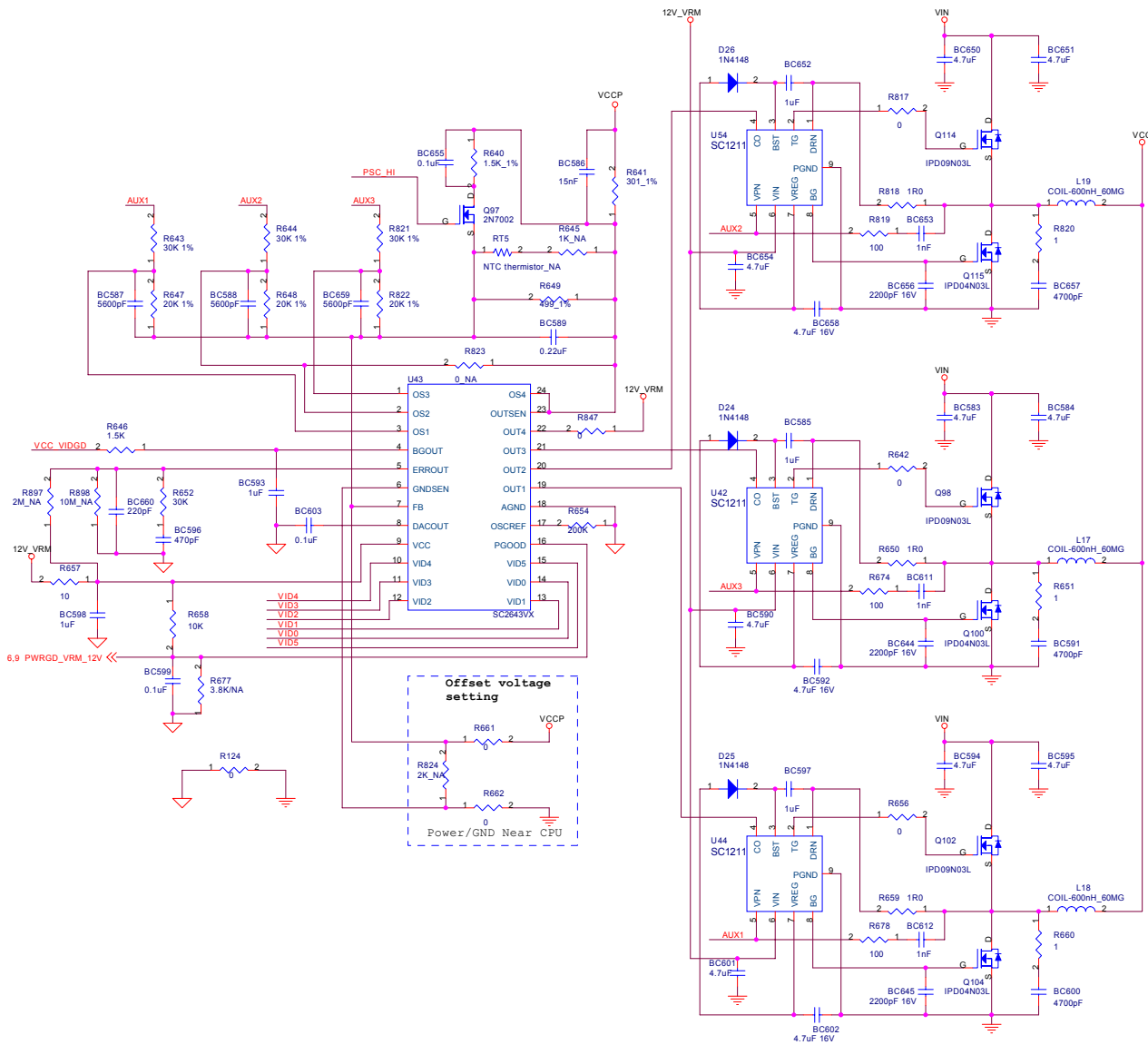


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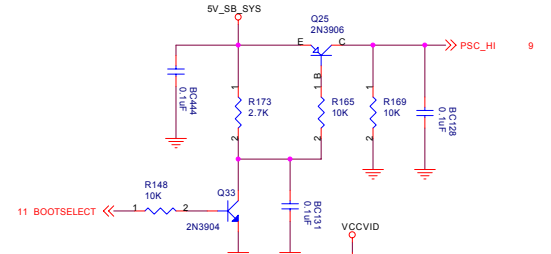
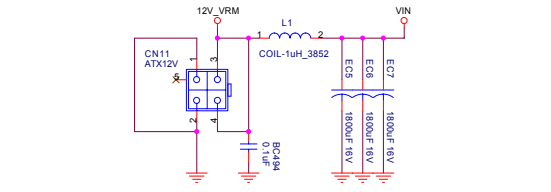


Title		Clock Generator CK-409	
Size	Document Number	865A05	
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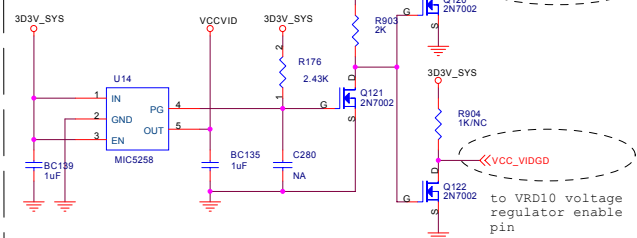
Semtech PWM for Intel P4 VRM10 Power



ATX12V_POWER_CONNECTOR

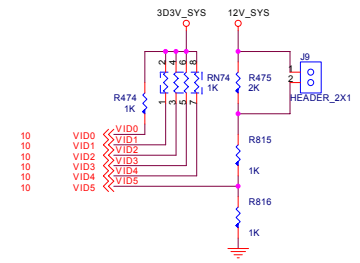


VCC_VID & VIDGD



VRD9/VRD10/VRD10.1 Select

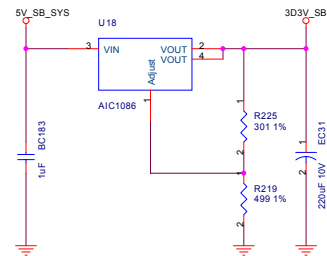
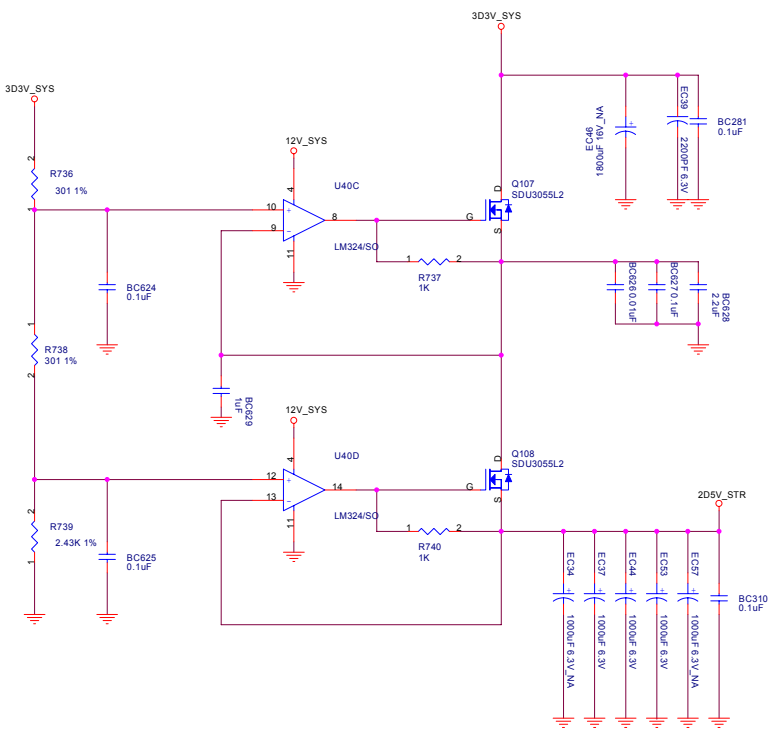
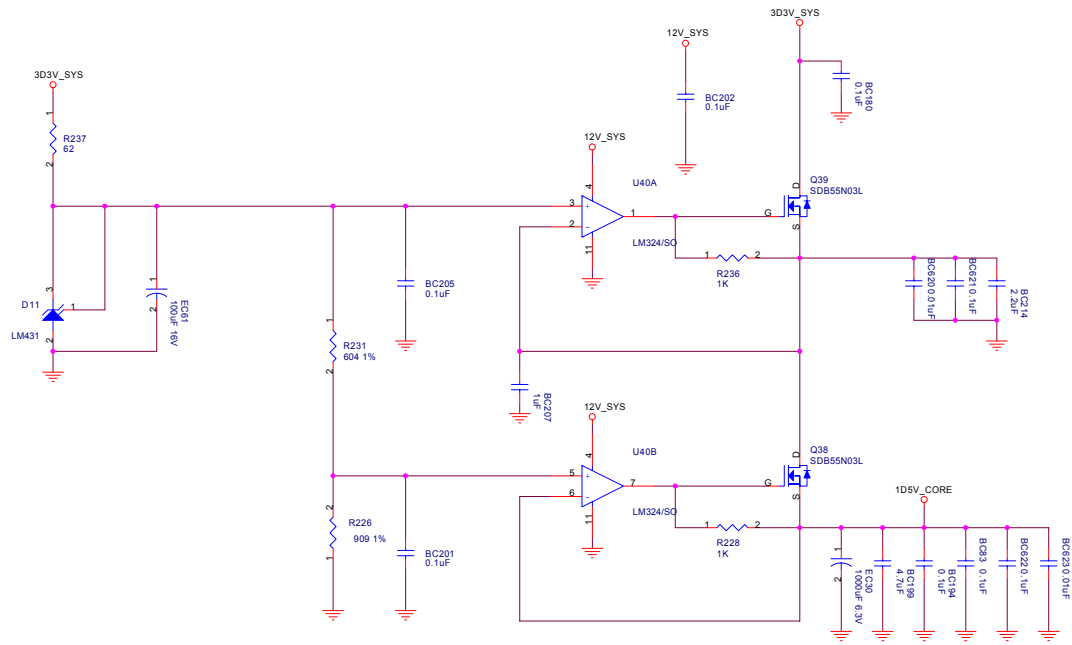
VID5	
0-4V for VR10	J9 open VRM10/VRD10.1
4-7V for VR9	J9 short VRM9



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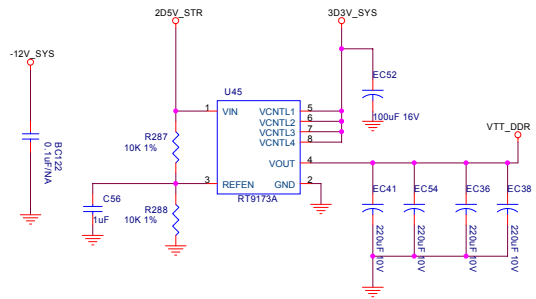
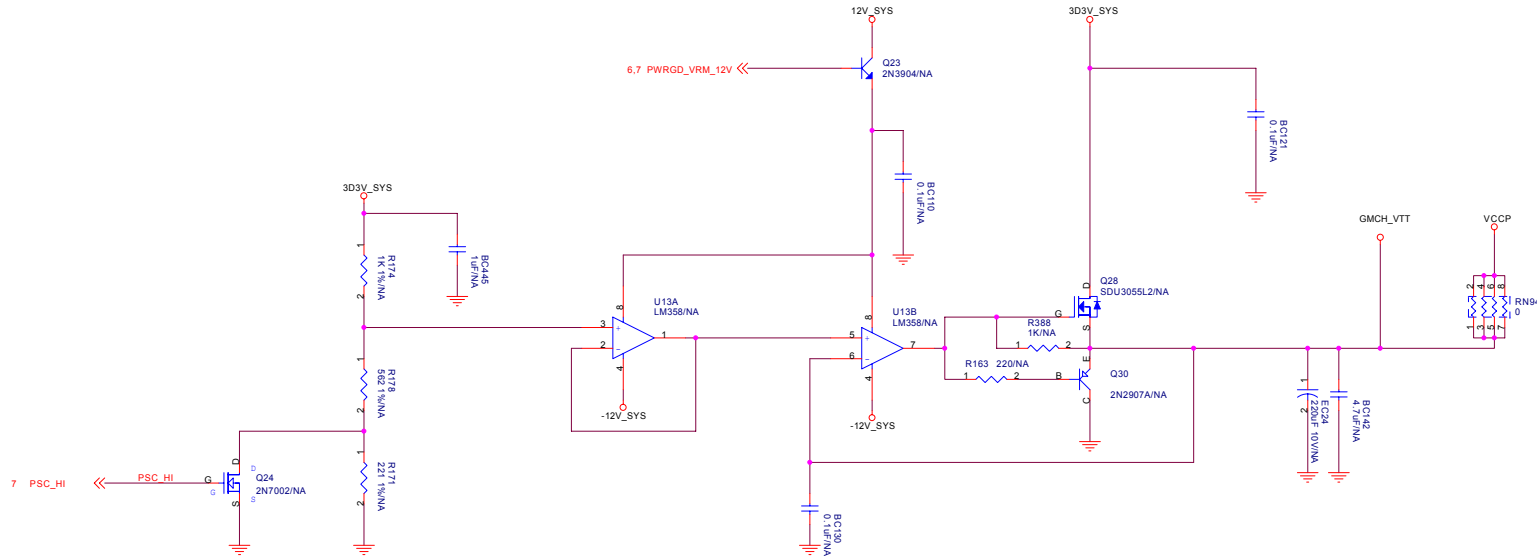
$V_{out} = V_{ref} (1 + R2/R1) + I_{adj} R2$
 R1 is Up Resistor.
 $I_{adj} = 50\mu A$
 $V_{ref} = 1.25V$

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Title	Power 2.5V-1.5V-3.3SB		
Size	Document Number	865A05	Rev 3
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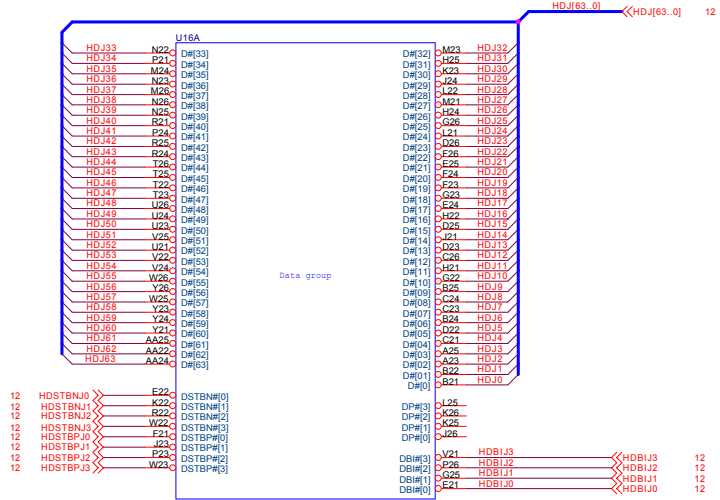
NWD=1.45V
PSC=1.2V
GMCH VTT Source 1.6A and Sink 600mA



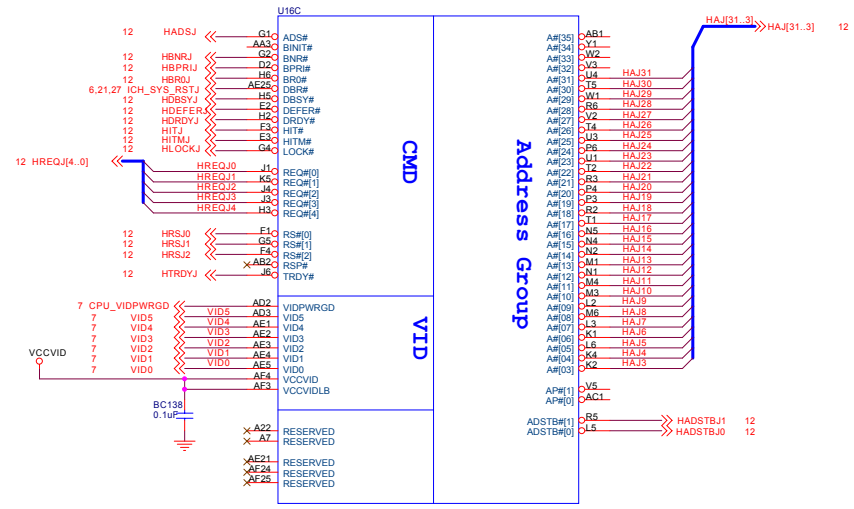
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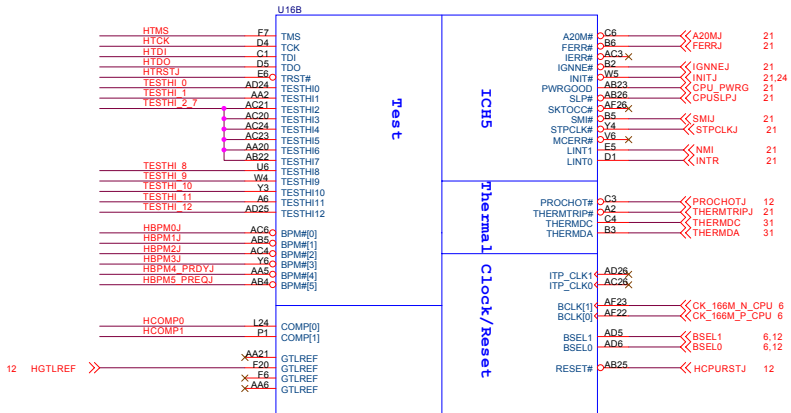
HOST BUS



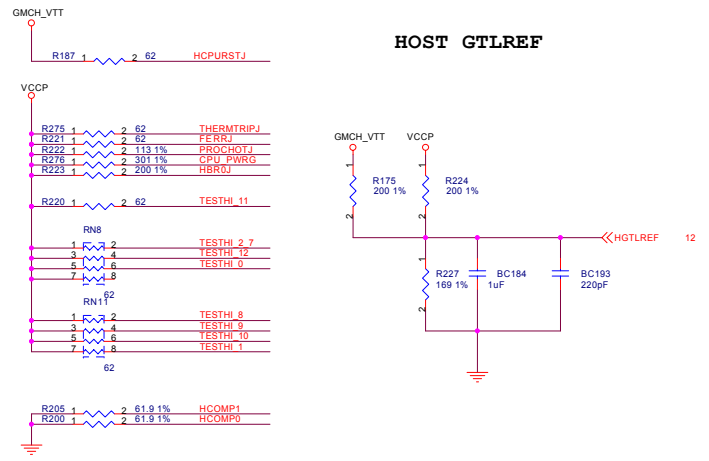
CMD ADDRESS & VID



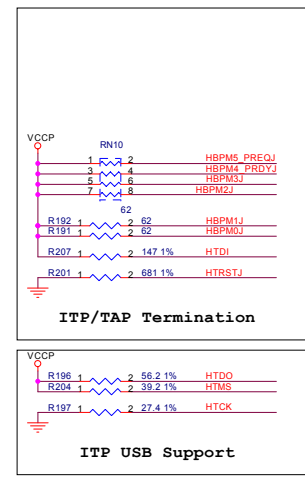
TEST, ICH5, CLK & THERMAL



PULL UP CIRCUIT

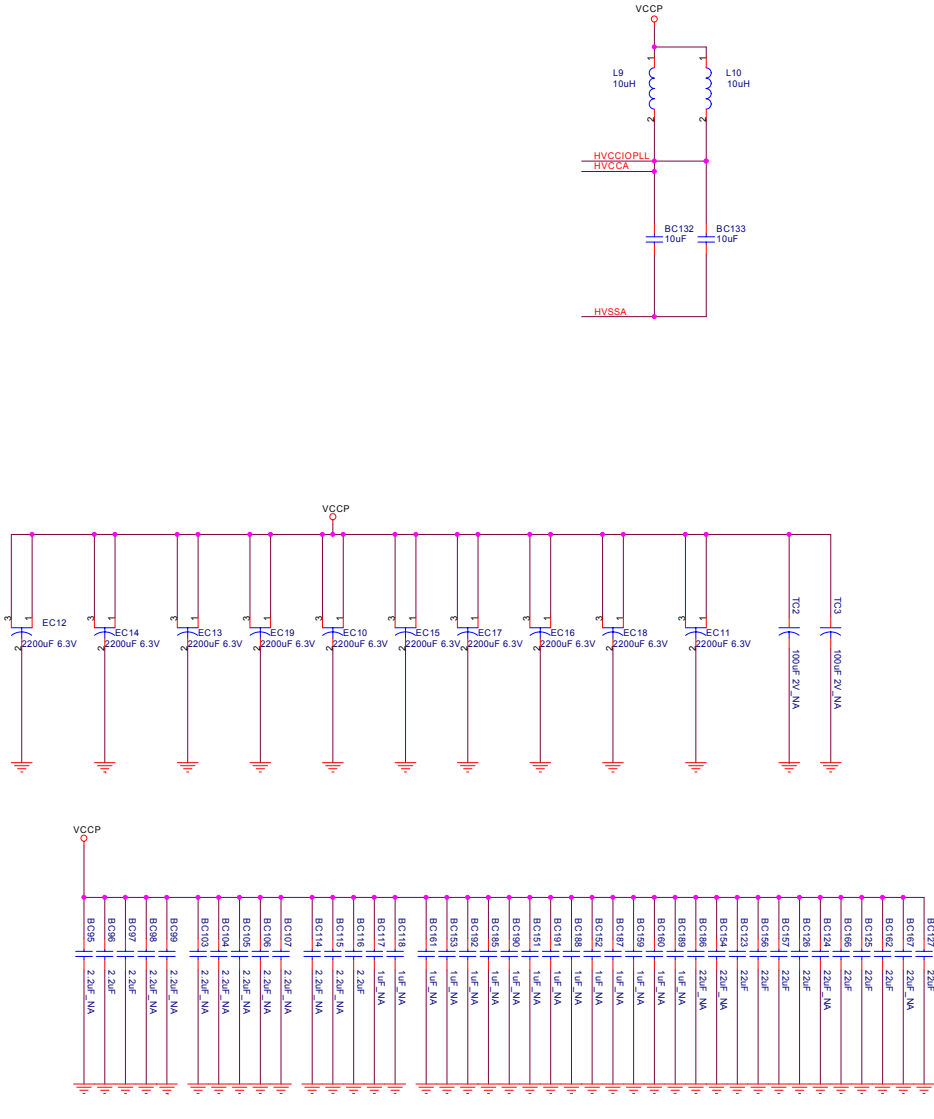


HOST GTLREF



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Title: Socket 478-1
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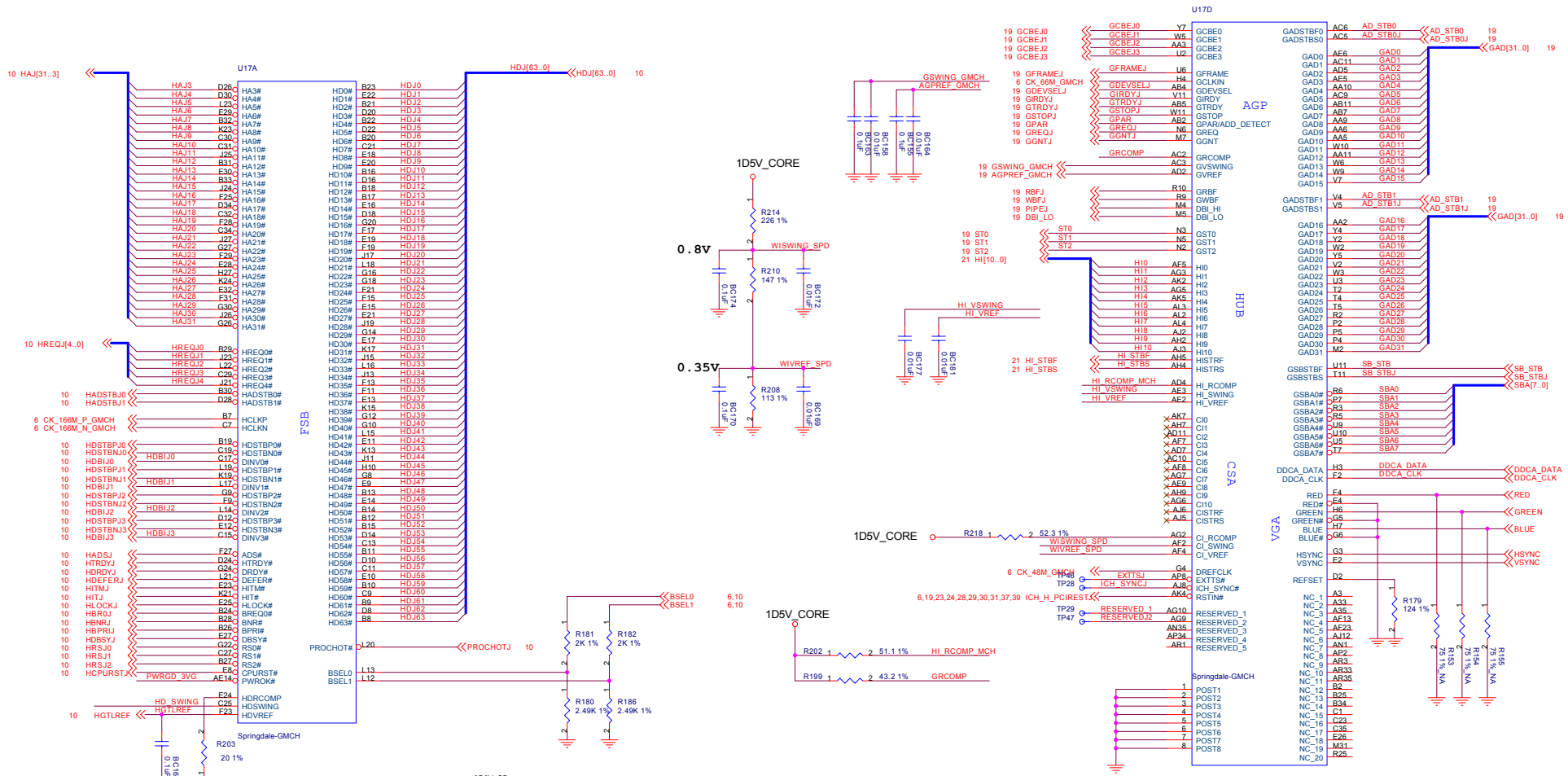
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Title: **Socket 478-2**

Size C: Document Number **865A05** Rev 8

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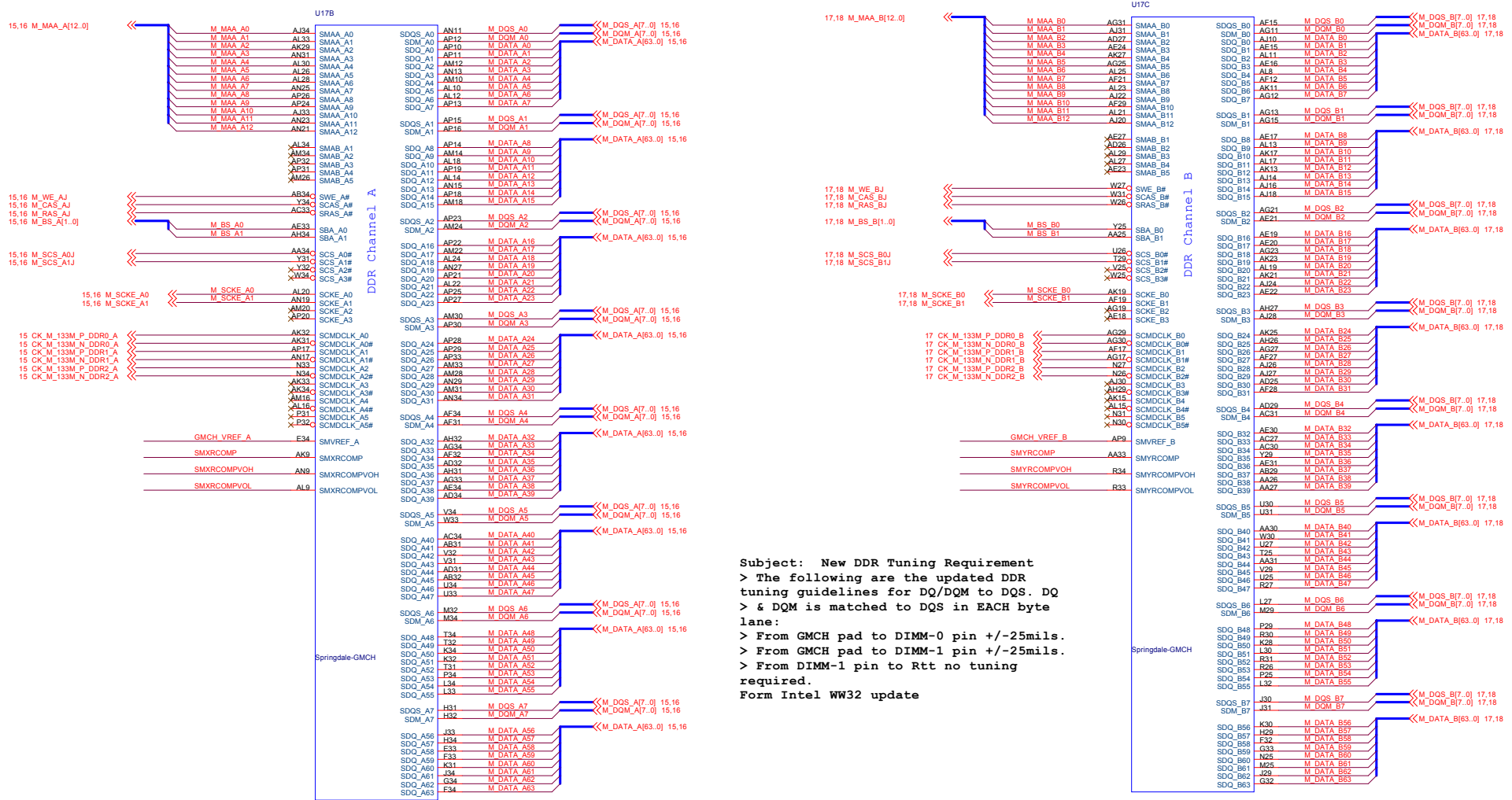
Pin Name	Pin #	Decoupling cap
VTTF5B	A15	0.22uF
VTTF5B	A21	0.47uF
VCC_DDR	E35	0.47uF
VCC_DDR	R35	0.22uF
VCCA_DDR	AL35	0.1uF
VCCA_DDR	AA35	0.1uF
VCC_DDR	AR31	0.1uF
VCC_DDR	AR21	0.22uF
VCC_DDR	AR15	0.1uF
VCC_AGP	AG1	0.1uF
VCC_AGP	Y1	0.1uF

BaseOn Intel WW29 Update

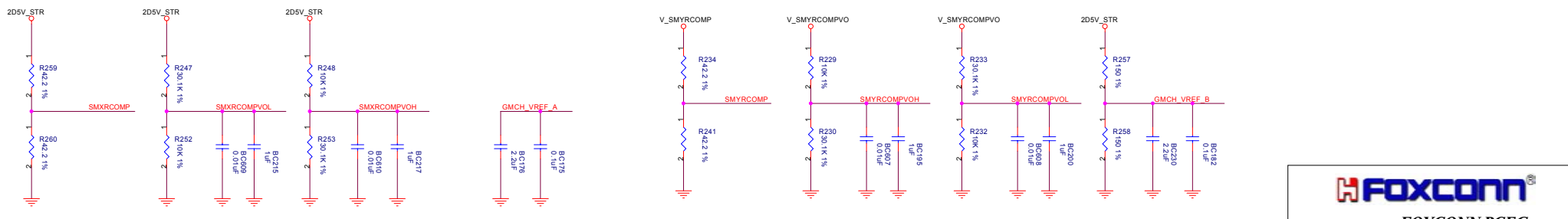


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Title		GMCH-1
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Subject: New DDR Tuning Requirement
 > The following are the updated DDR tuning guidelines for DQ/DQM to DQS. DQ > & DQM is matched to DQS in EACH byte lane:
 > From GMCH pad to DIMM-0 pin +/-25mils.
 > From GMCH pad to DIMM-1 pin +/-25mils.
 > From DIMM-1 pin to Rtt no tuning required.
 Form Intel WW32 update

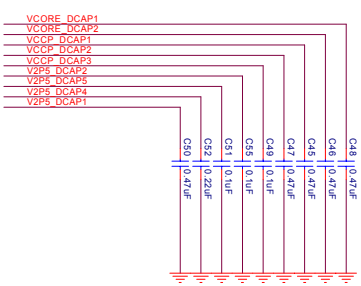
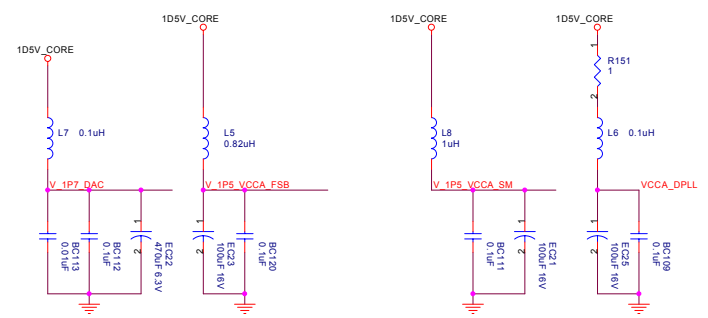
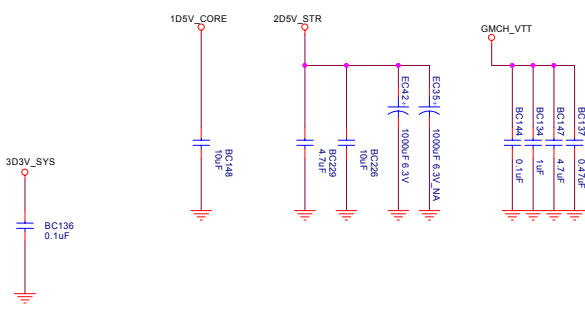


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Title: **GMCH-2**

Size C Document Number: **865A05** Rev A

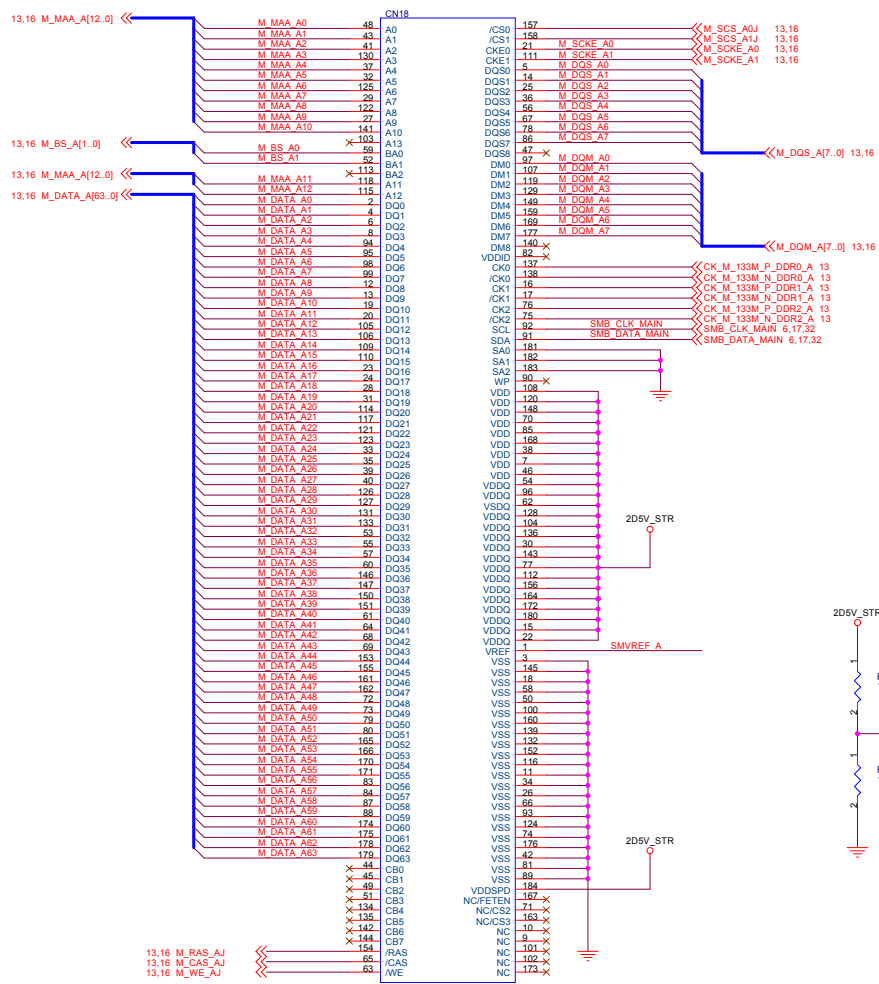
Date: Monday, February 10, 2003 Sheet 13 of 39

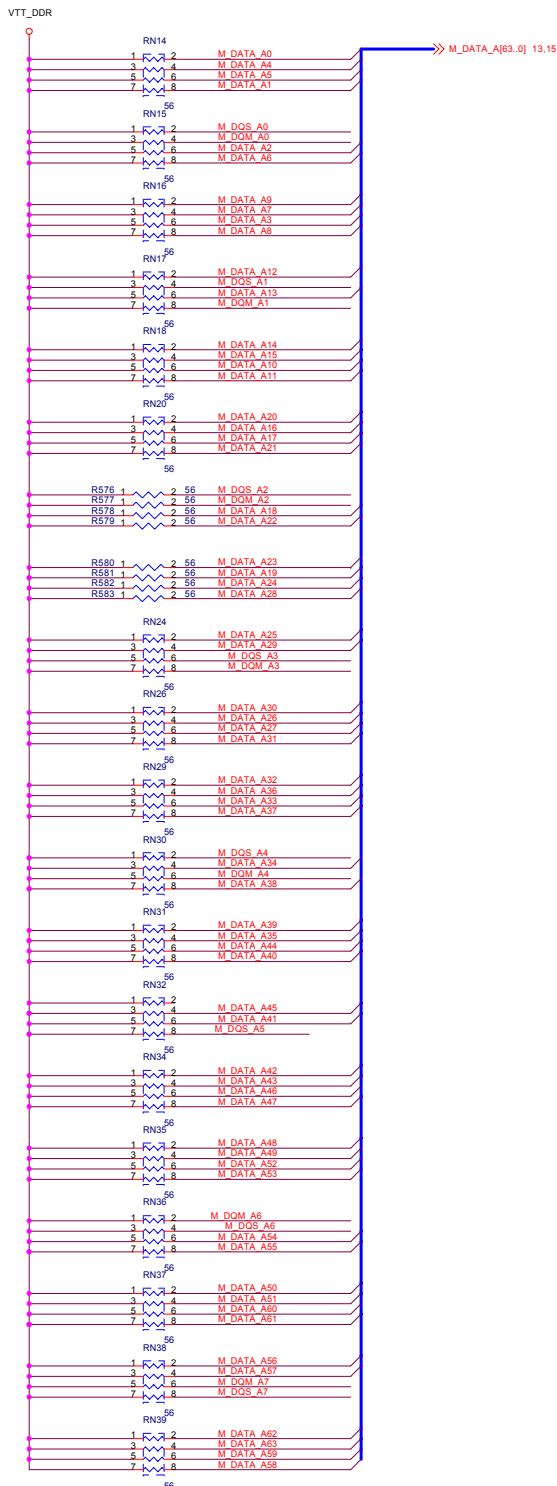


Subject: GMCH Vtt VR Clarification
 The GMCH VTT regulator is required to be capable of sinking 600mA of current in addition to sourcing 1.6A of current in normal operation. Sinking 600mA of current is a new requirement for the Springdale platform regardless if a Northwood or Prescott processor is installed. The reason why the GMCH VTT VR must be able to sink 600mA is because there will be times when the GMCH VTT VR's output will be set to a voltage lower than the VRD 10's output. The difference in voltage will cause current to be driven from the VRD to the GMCH VTT regulator. If the GMCH VTT VR doesn't have the capability to sink the current, damage to the GMCH can occur. In order to meet this requirement, Intel is using a P-FET in an SOT-23 footprint on the GMCH VTT voltage regulator. The back driven current will be sunk into the ground plane through this P-FET without causing damage to the Springdale GMCH.
 Update from Intel WW34 MOV

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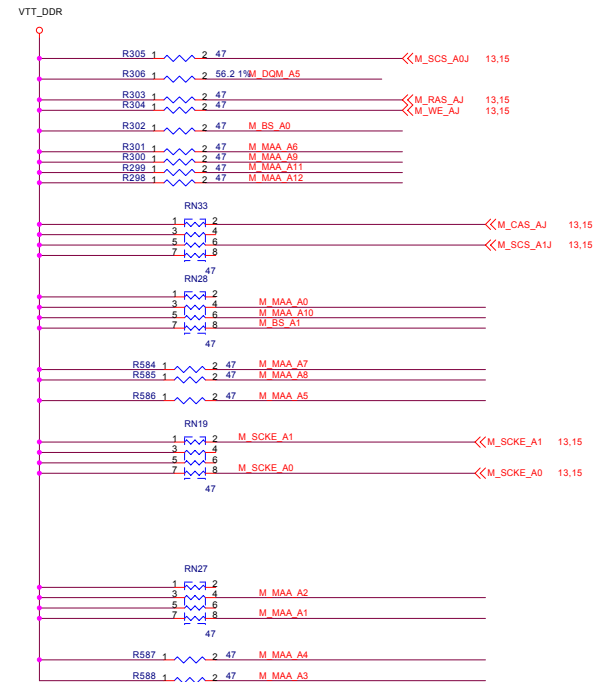
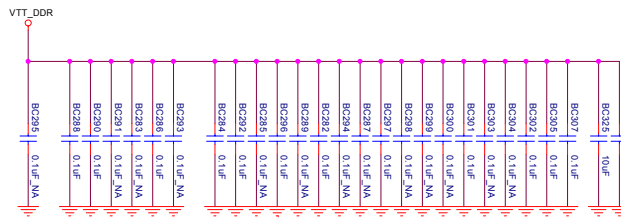
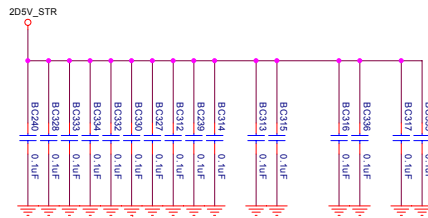
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 Size: C Document Number: 865A05 Rev: 8
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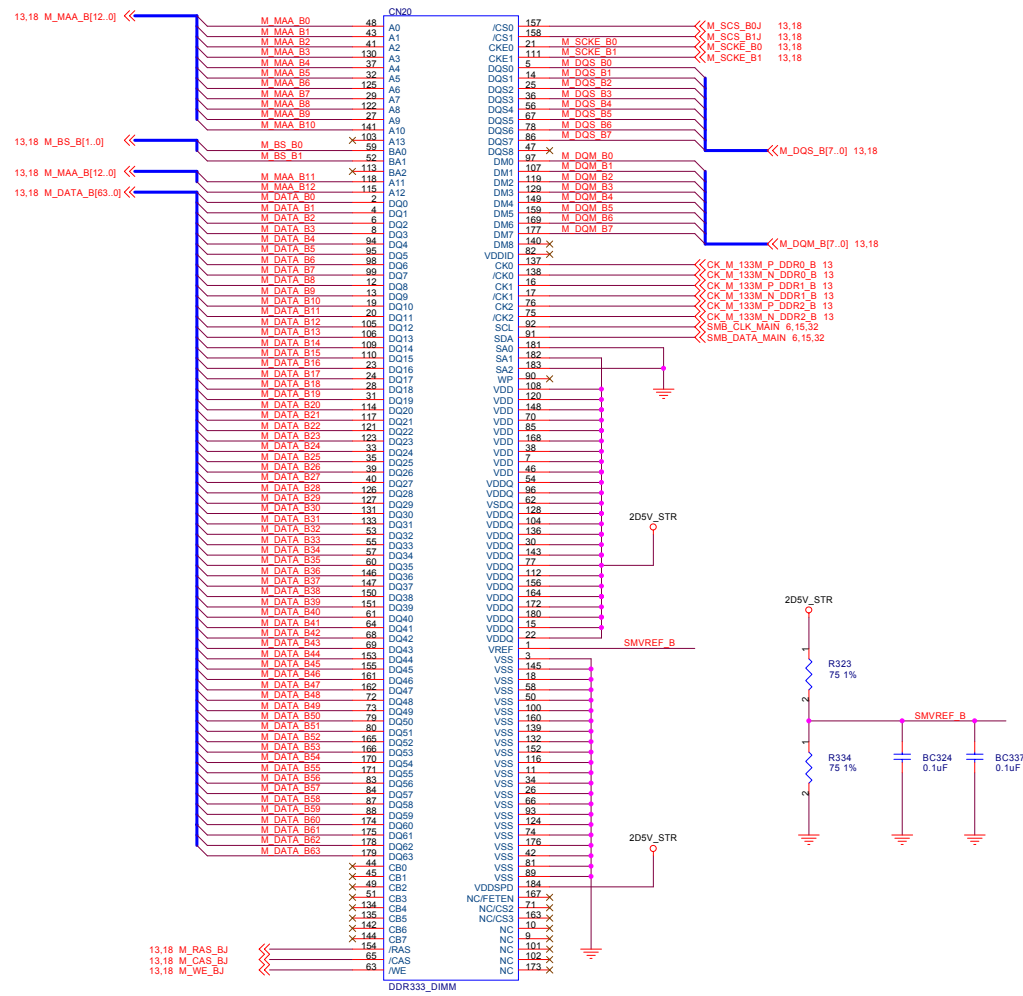




Updated DDR Termination Resistor (Rtt) Values
The recommended termination resistor (Rtt) value for DQ/DQM/DQS is changed to 56 ohms. The previous recommendation was 110 ohms.
Form Intel FAE WW32

\ll M_MAA_A[12..0] 13,15
 \ll M_BS_A[1..0] 13,15
 \ll M_DQM_A[7..0] 13,15
 \ll M_DQS_A[7..0] 13,15





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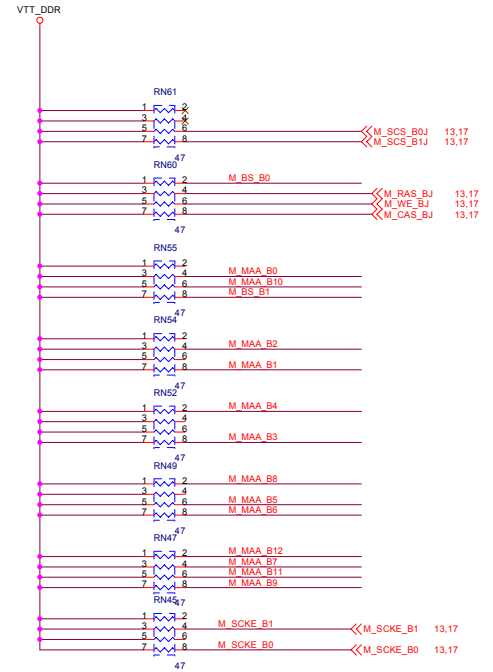
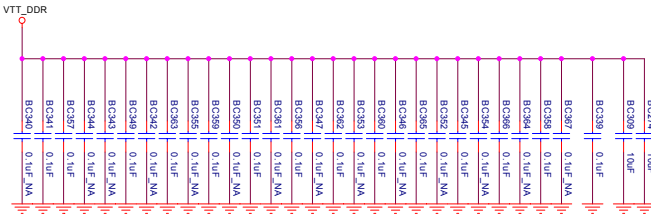
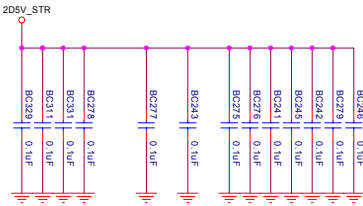
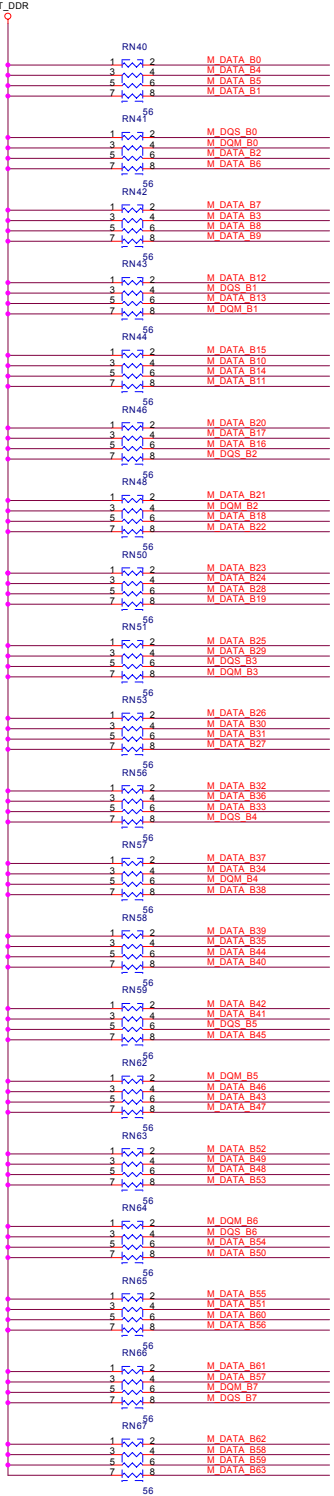
Title: **DDR Channel B DIMM**

Size: Custom Document Number: **865A05** Rev: 8

Date: Monday, February 10, 2003 Sheet: 17 of 39

Updated DDR Termination Resistor (Rtt) Values
 The recommended termination resistor (Rtt) value for DQ/DQM/DQS is changed to 56 ohms. The previous recommendation was 110 ohms.
 Form Intel FAE WW32

- M_BS_B[1..0] 13,17
- M_DQM_B[7..0] 13,17
- M_MAA_B[12..0] 13,17
- M_DQS_B[7..0] 13,17
- M_DATA_B[63..0] 13,17

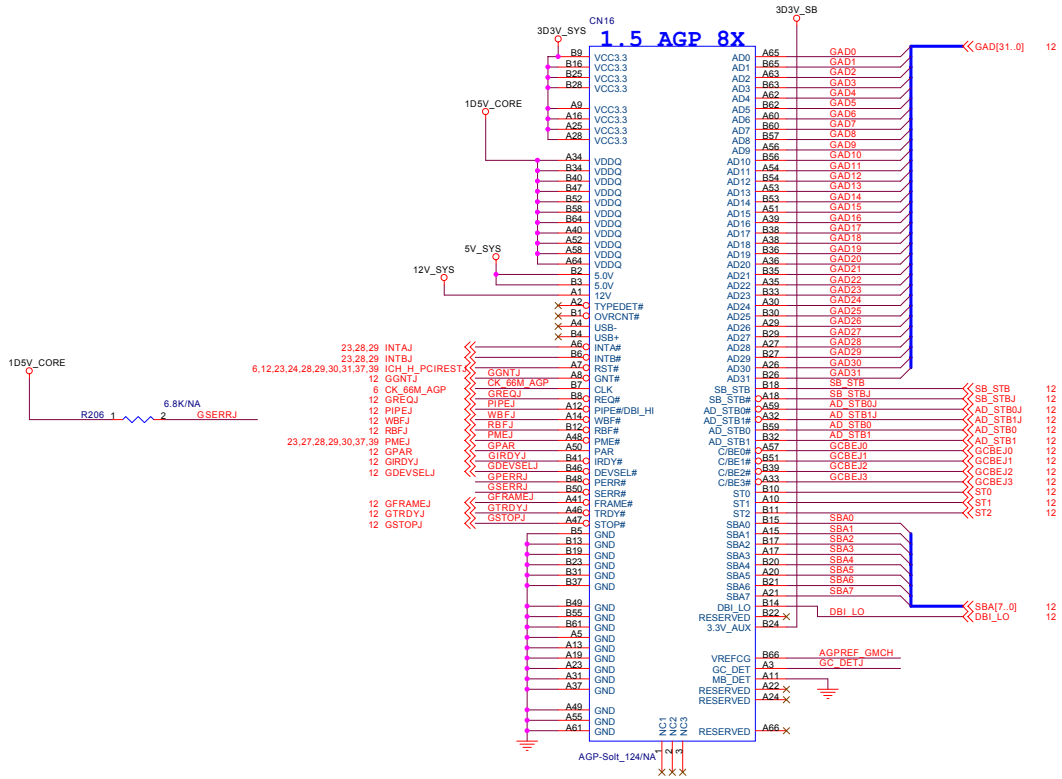


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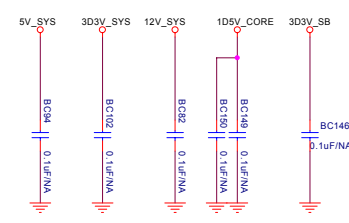
Title: **DDR Channel B Termination**

Size: C Document Number: **865A05** Rev: B

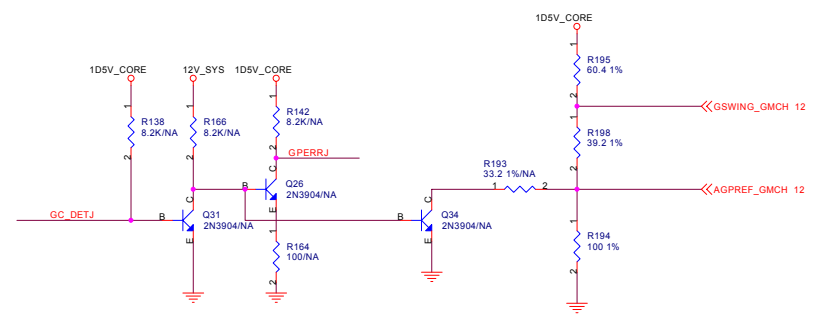
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DECUBLE CAP.



AGPREF & AGPSWING CIRCUIT

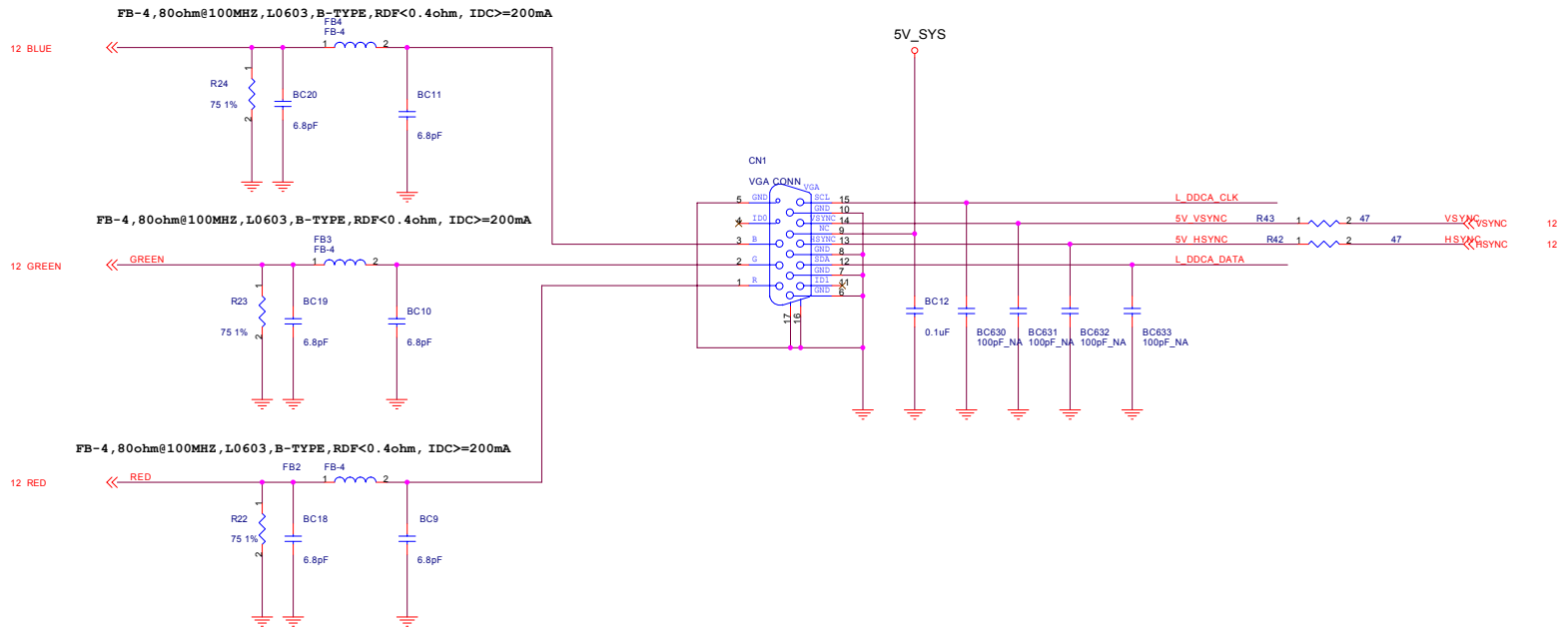


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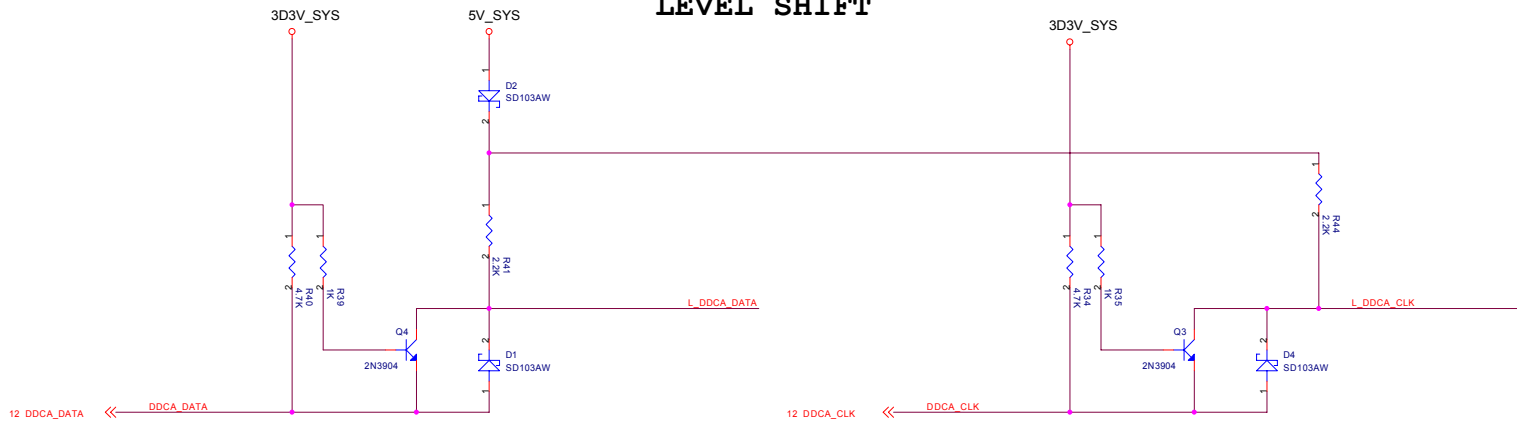
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Title AGP Connector	
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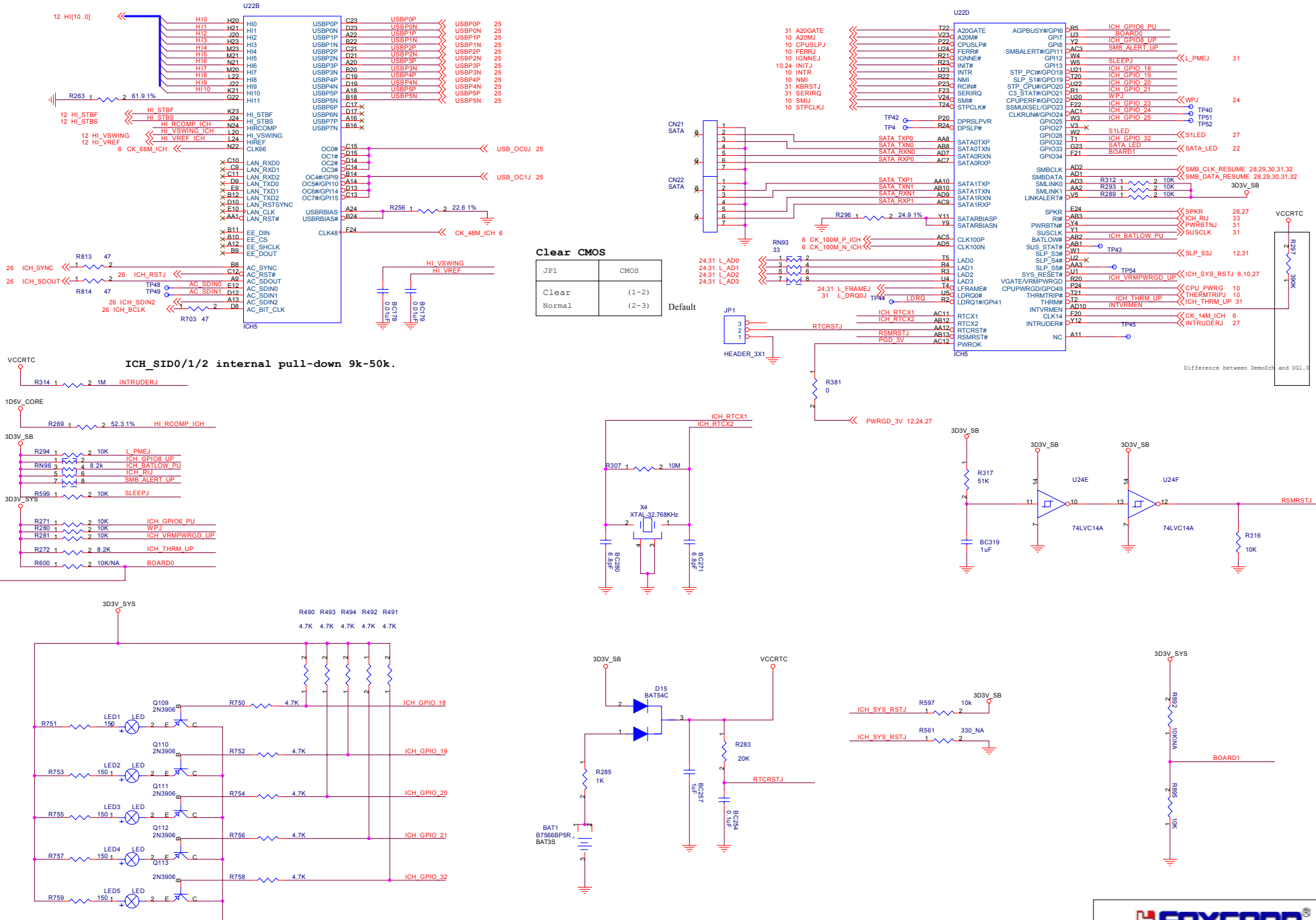
VGA CONN.



LEVEL SHIFT



Title		VGA Connector
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Clear CMOS

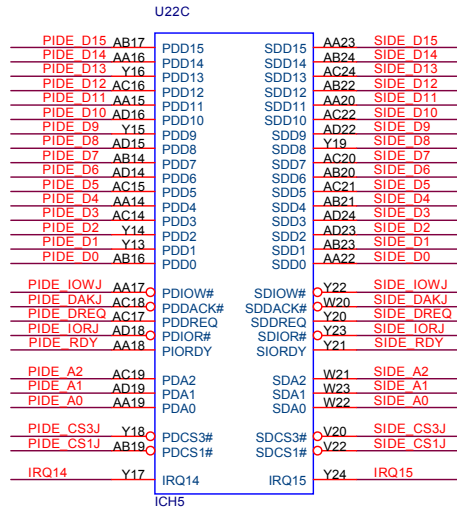
JP1	CMOS
Clear	(1-2)
Normal	(2-3)

Default

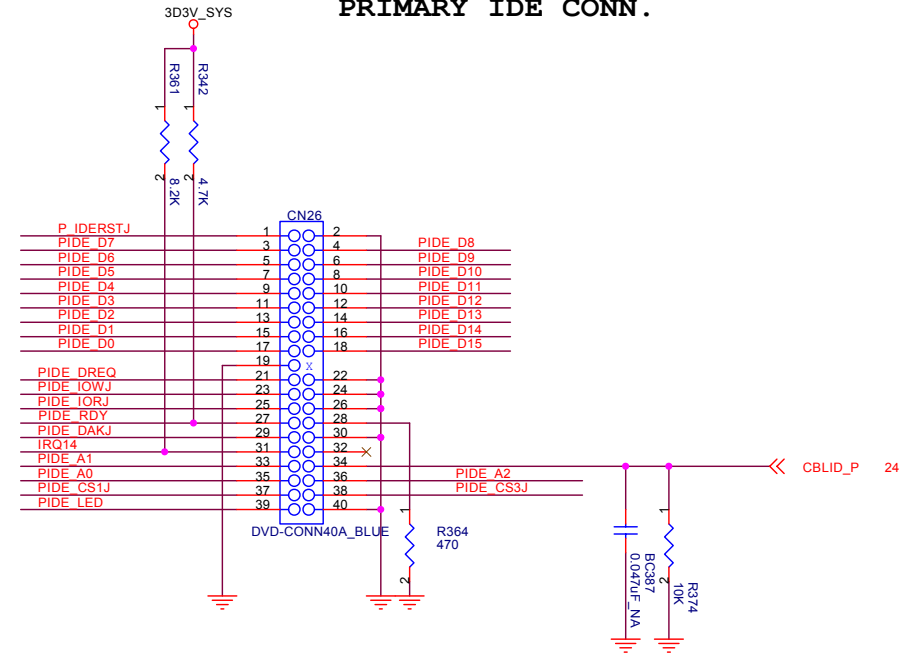
ICH_SID0/1/2 internal pull-down 9k-50k.

Difference between Demo and D01.

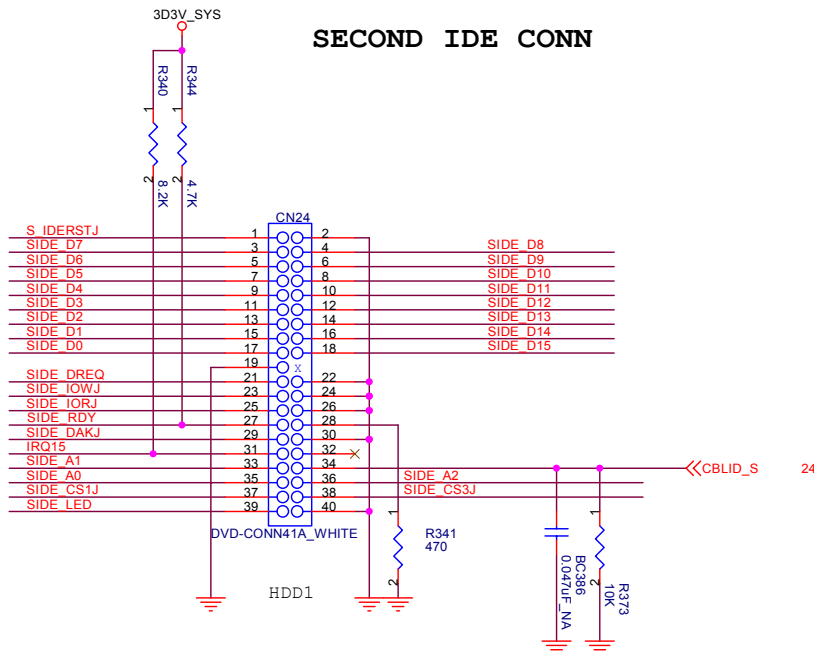
ICH5 IDE INTERFACE



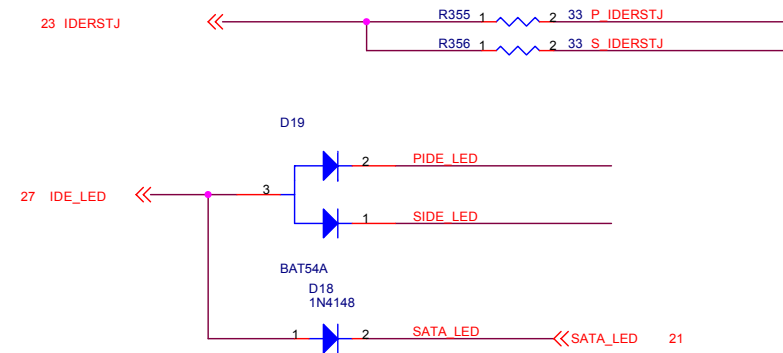
PRIMARY IDE CONN.



SECOND IDE CONN



IDE LED & IDE RST



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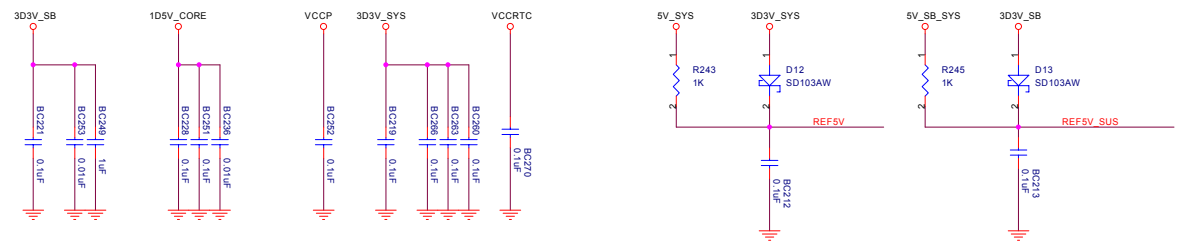
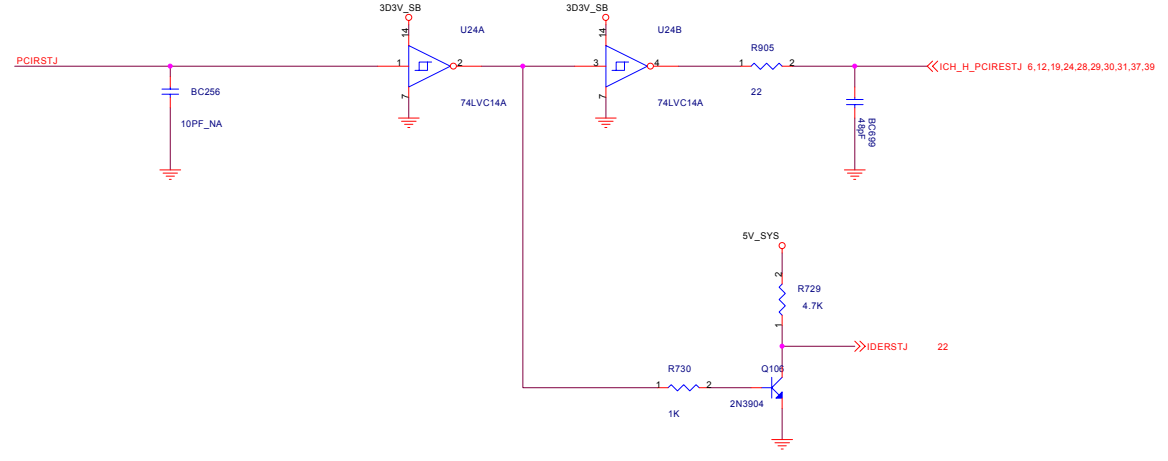
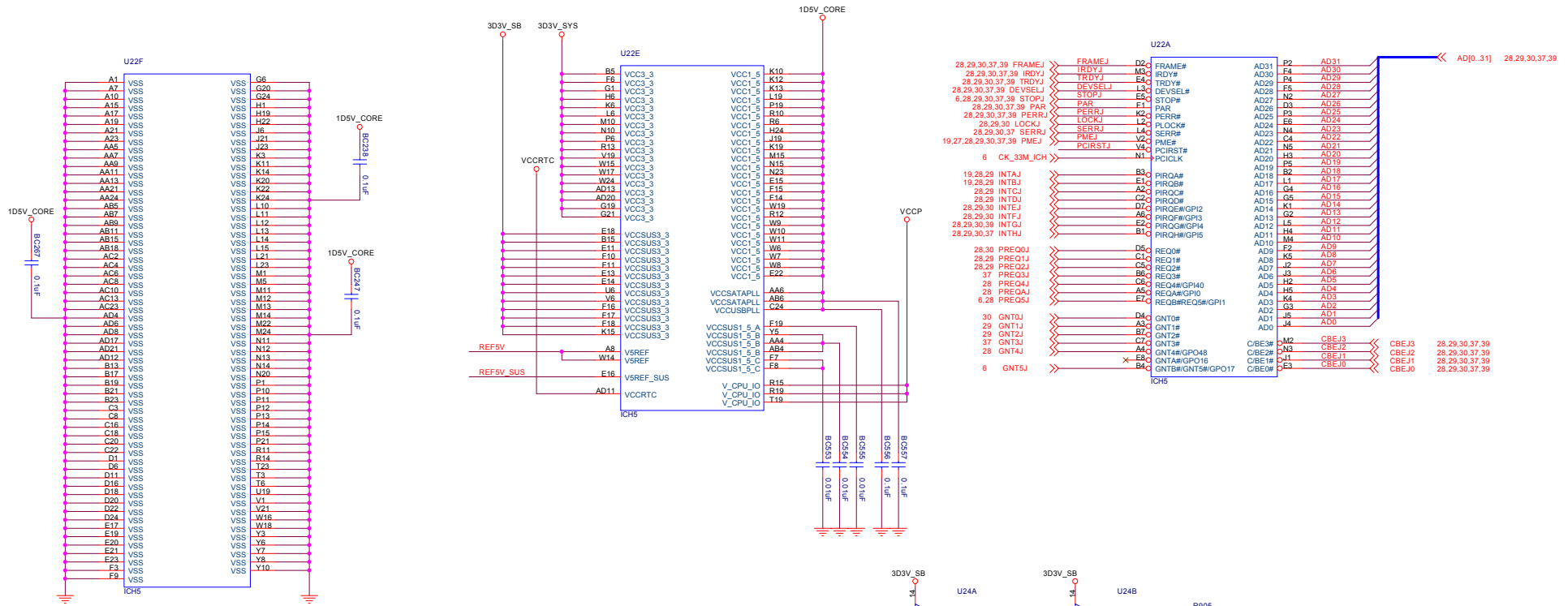
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Title ICH5-2 IDE Connectors

Size Custom Document Number 865A05

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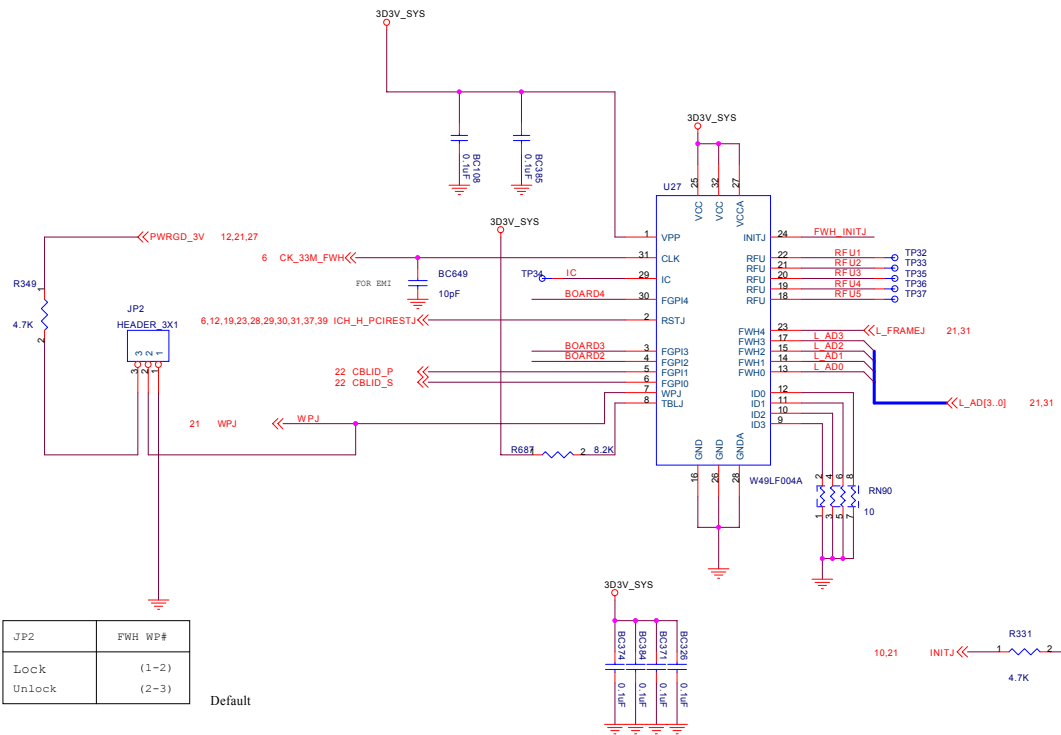


There are component place on solid site

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Title: ICH5-3
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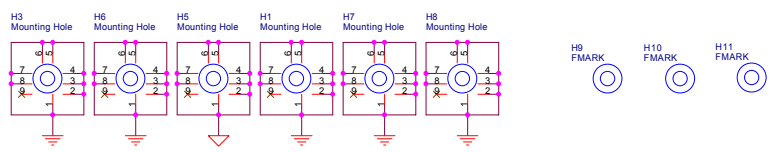
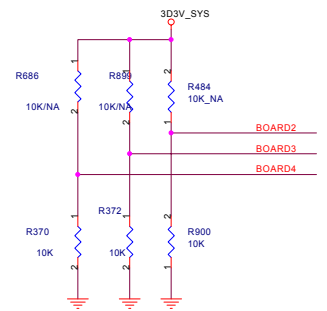


JUMPER: JP7	MODE
CONFIG	(1-2)
NORMAL	(2-3)
RECOVERY	OPEN

Safe Speed
Default

JP2	FWH WP#
Lock	(1-2)
Unlock	(2-3)

Default

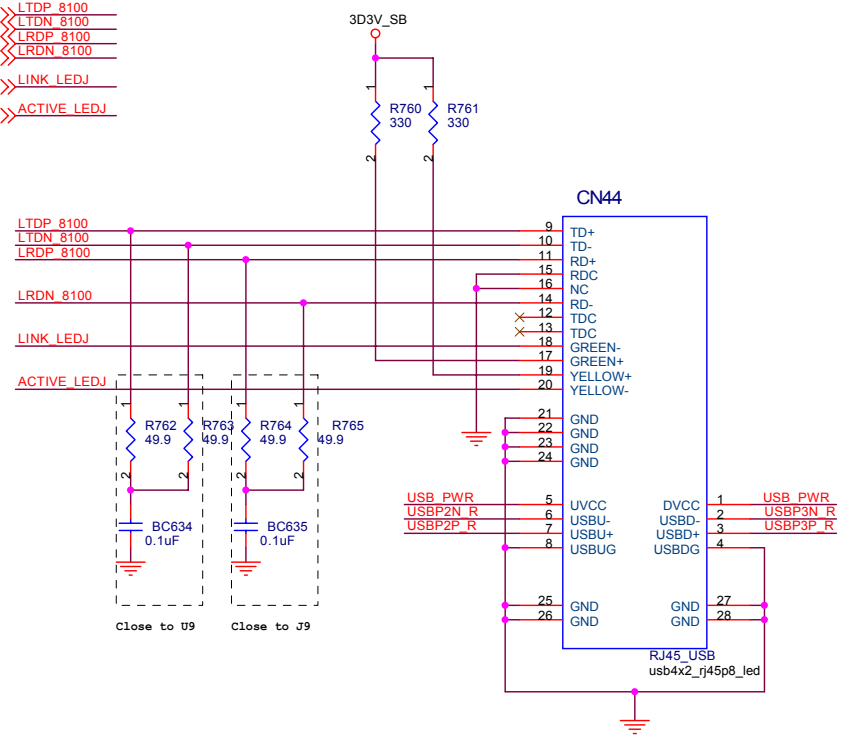
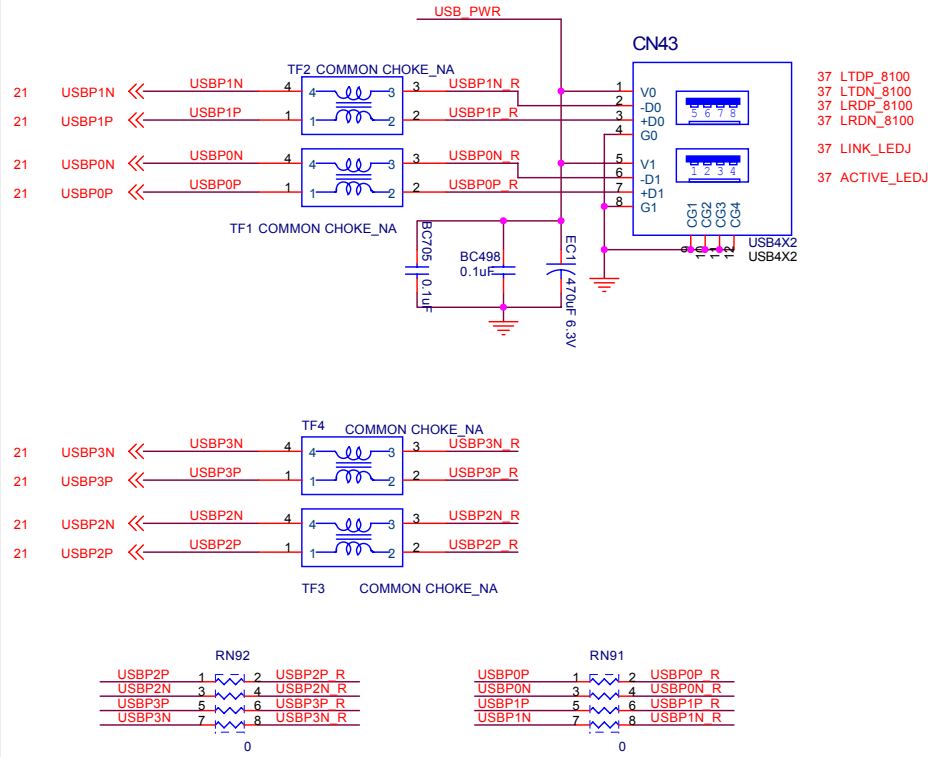


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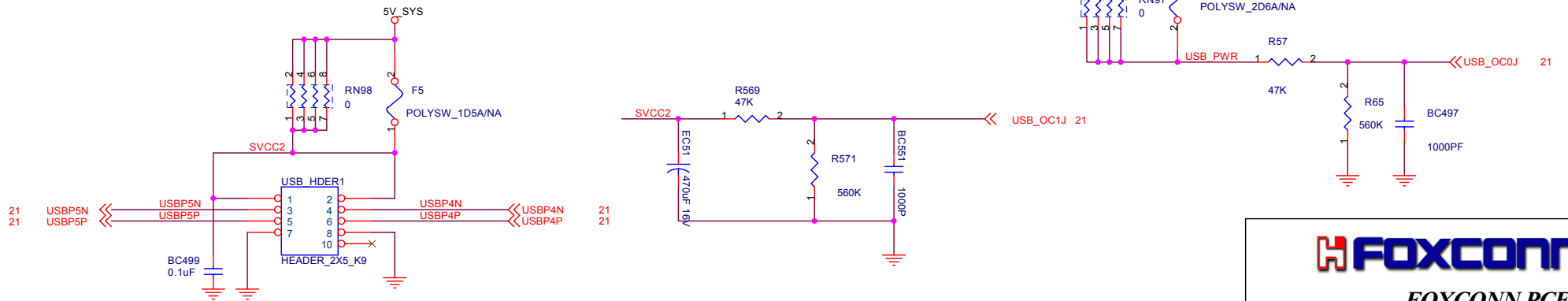
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Title	FWH	
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Rear Dual USB Connector



USB Header1



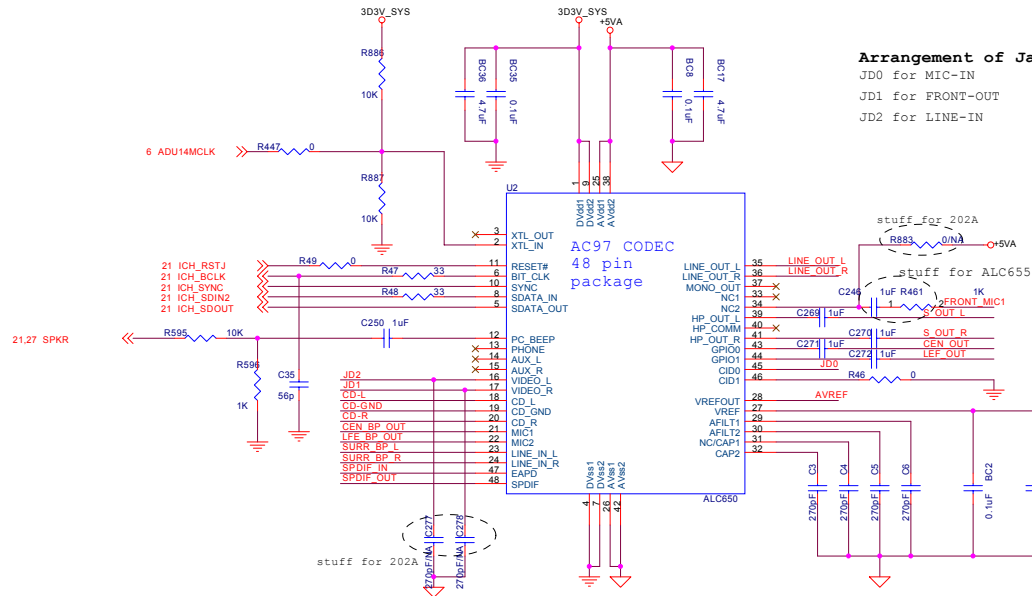
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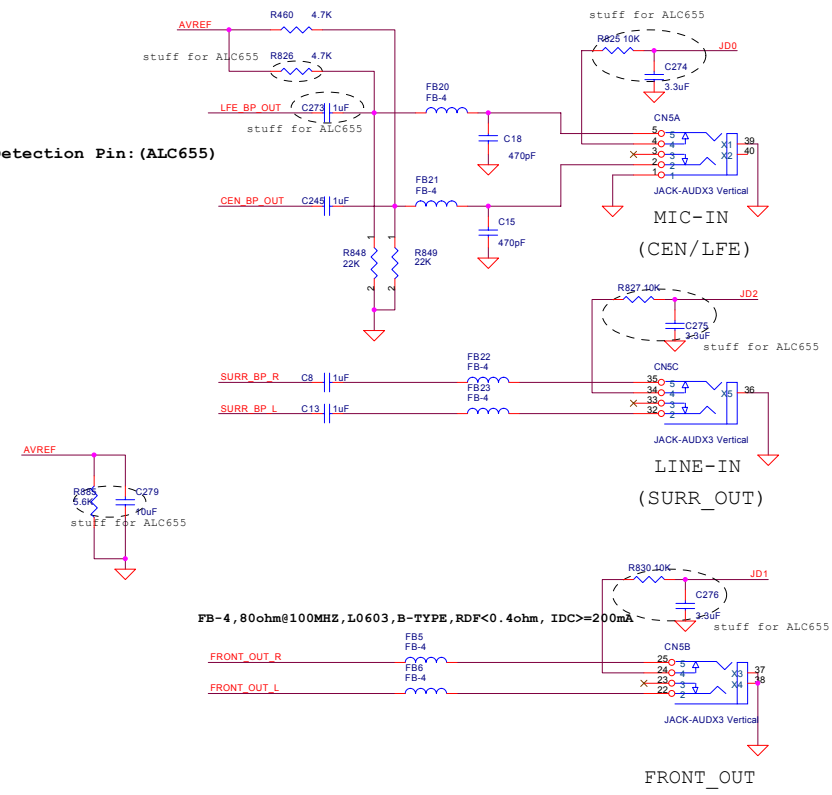
Title **LAN_USB Connector**

Size Custom Document Number **865A05** Rev B

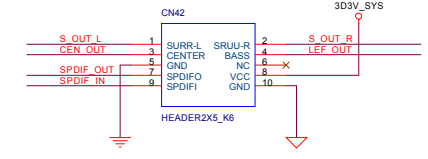
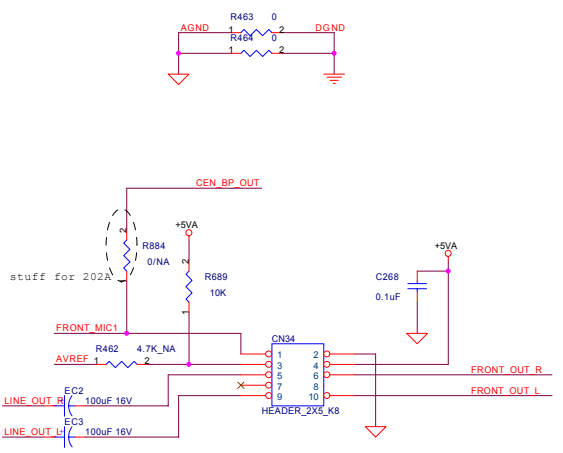
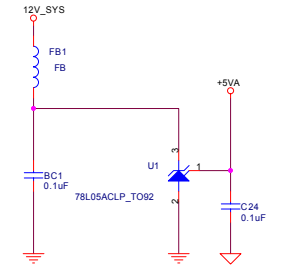
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Arrangement of Jack Detection Pin: (ALC655)
 JD0 for MIC-IN
 JD1 for FRONT-OUT
 JD2 for LINE-IN



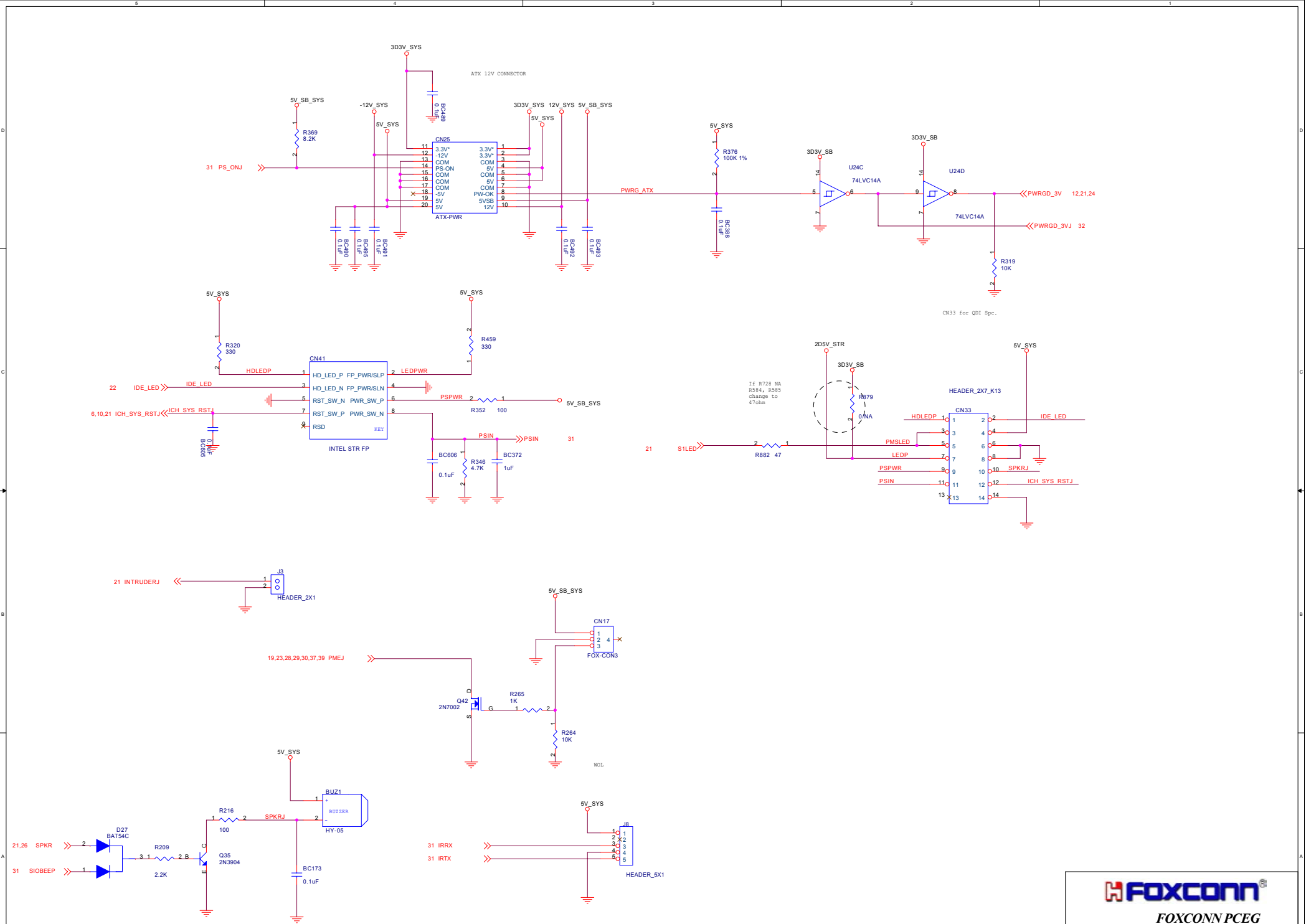
FB, 300ohm@100MHz, L0805, P-TYPE, RDC<03.ohm, IDC=>=1A



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Title: **AC97 Codec**
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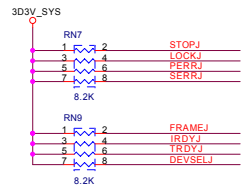
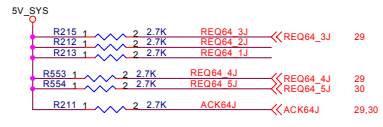
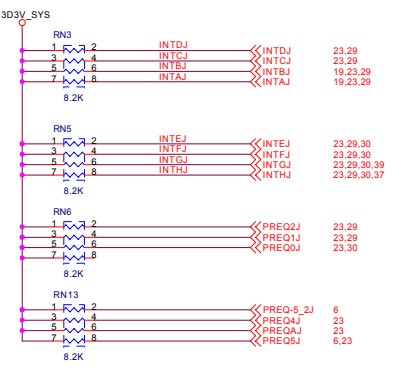
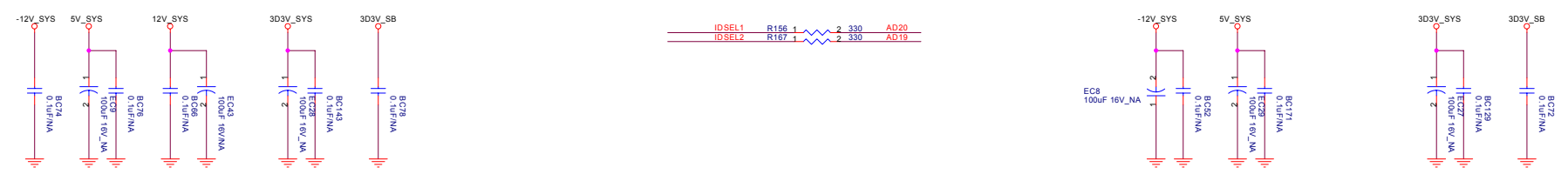
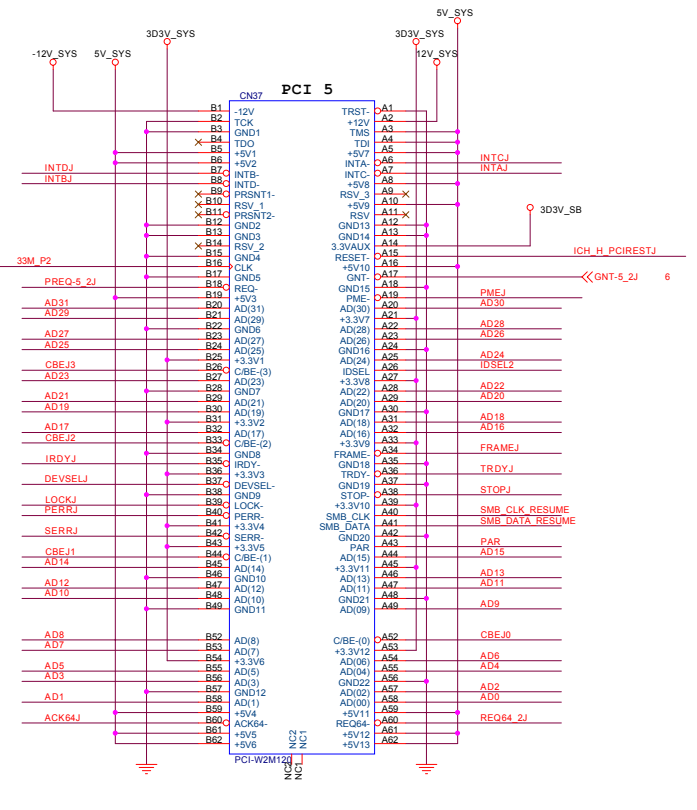
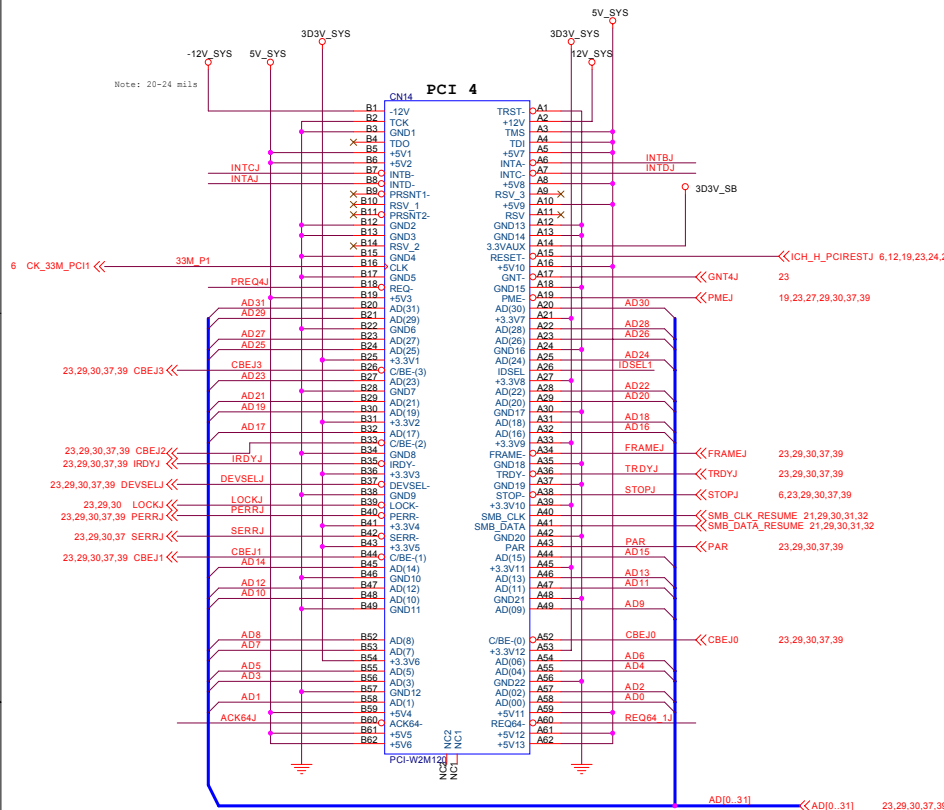


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Title MISC Connector / ATX Power Connector

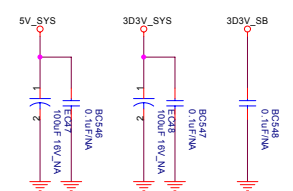
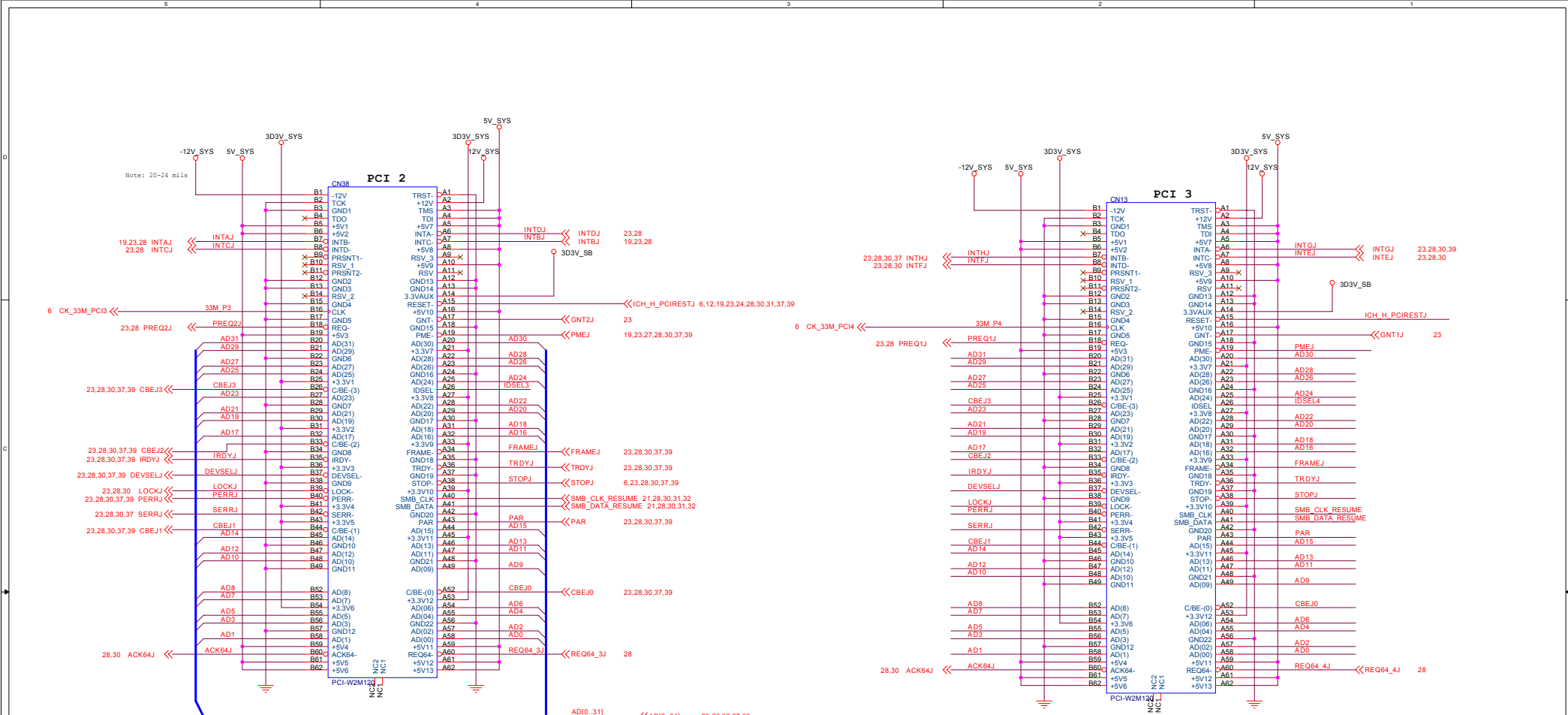
Size C Document Number 865A05 Rev B

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Title		PCI Connectors 1,2	
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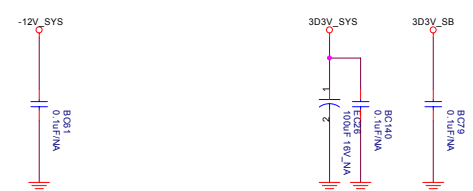
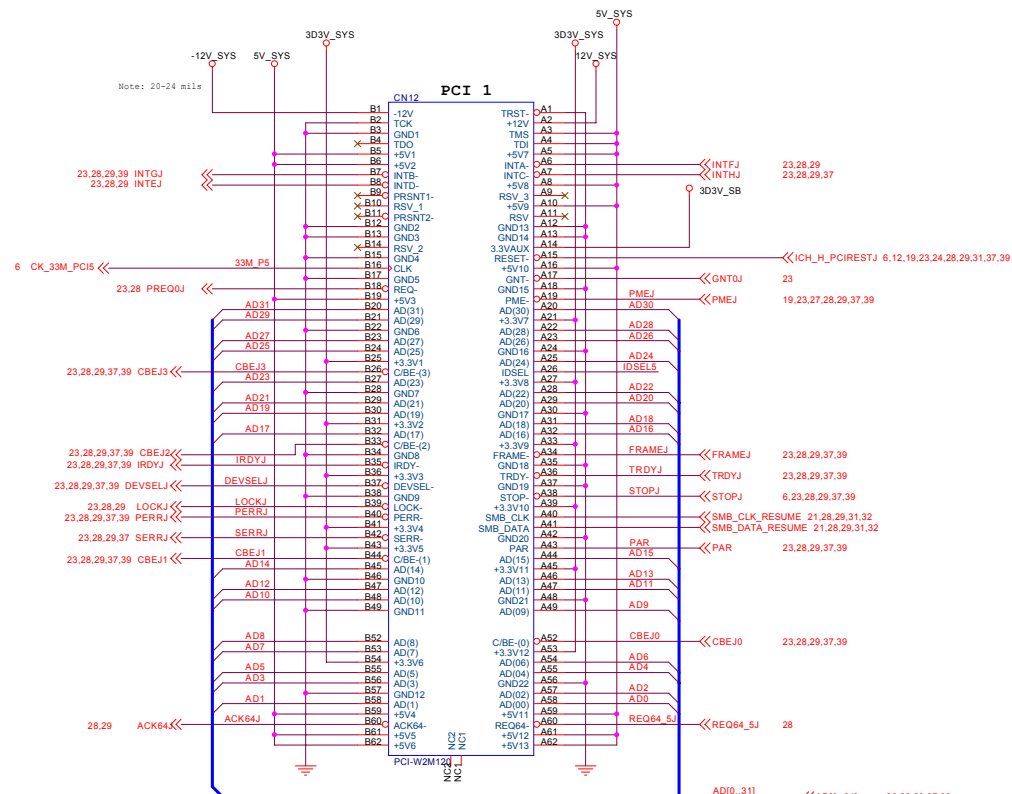
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Title: **PCI SLOT 3,4**

Size: Custom Document Number: **865A05** Rev: 8

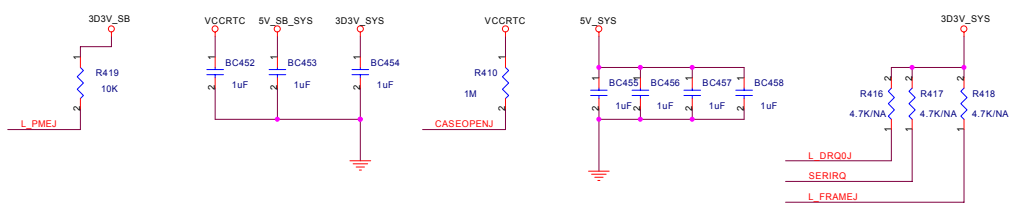
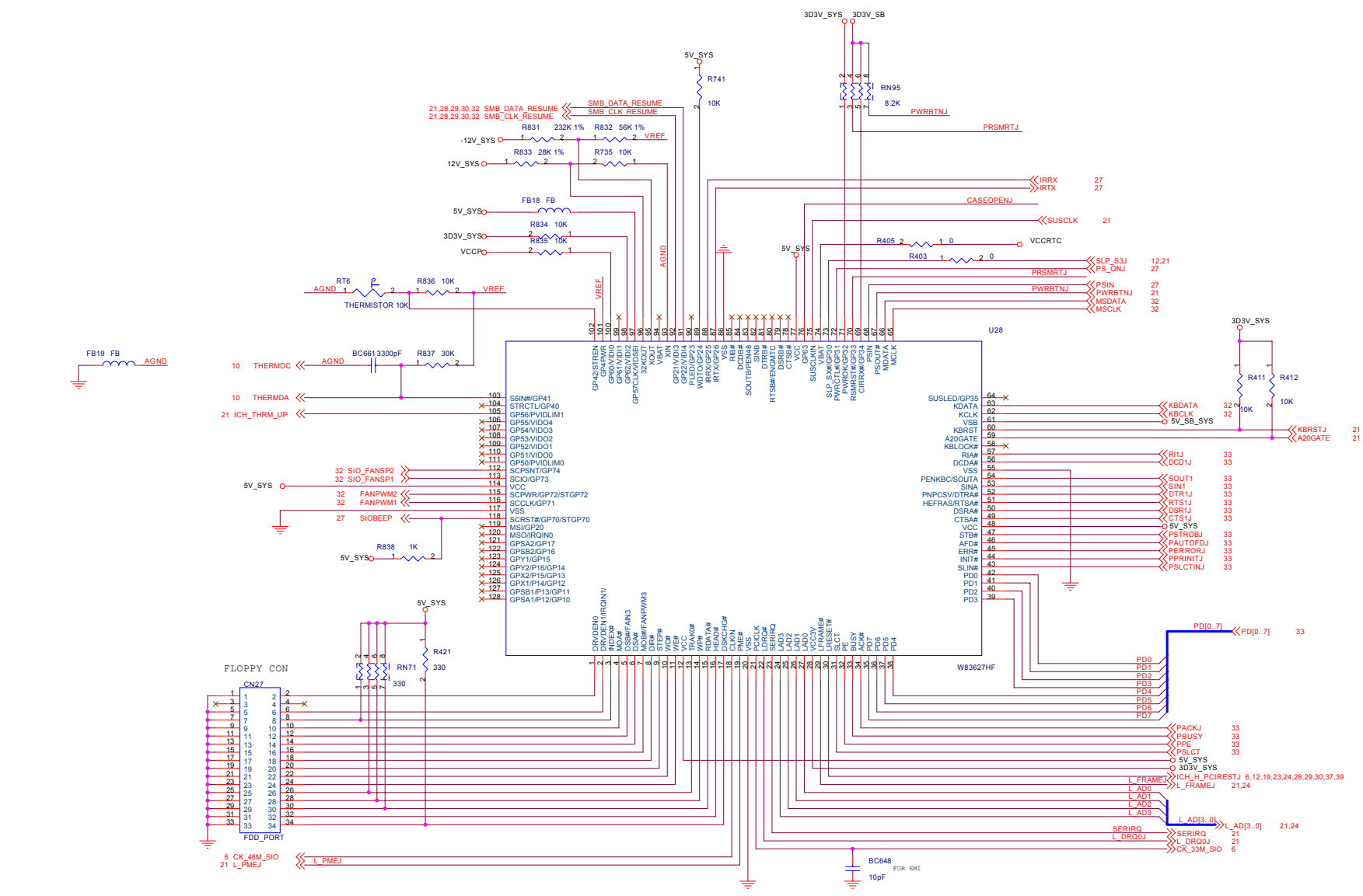
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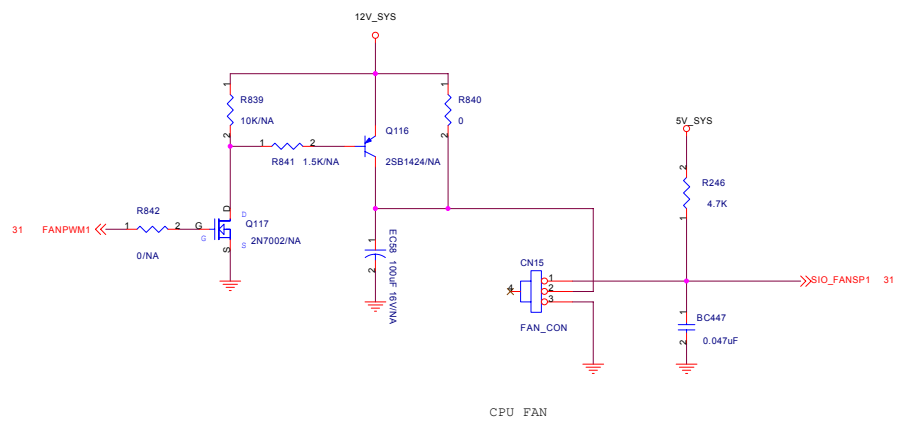
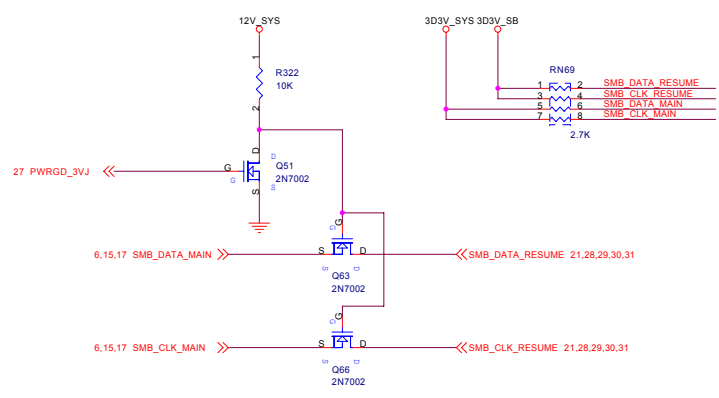
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Title		PCI Connector 5
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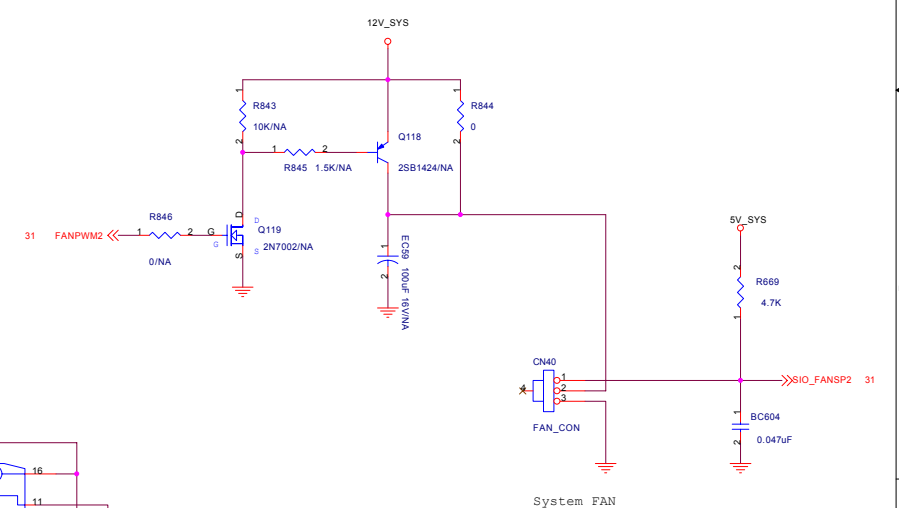
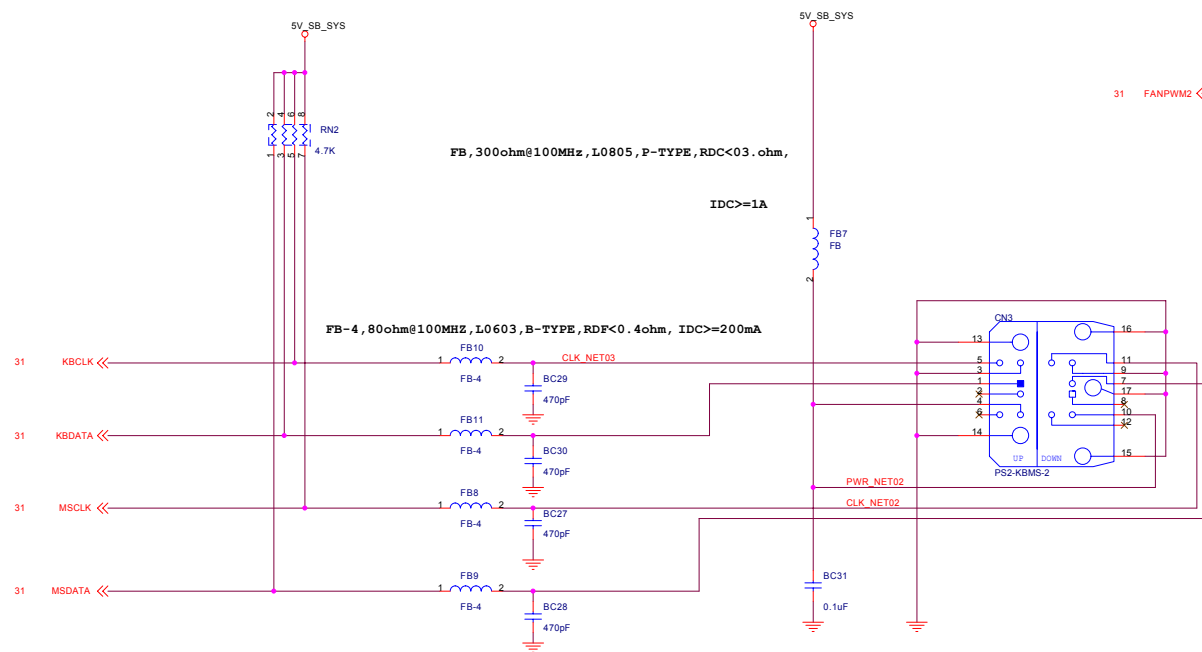


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CPU FAN



System FAN

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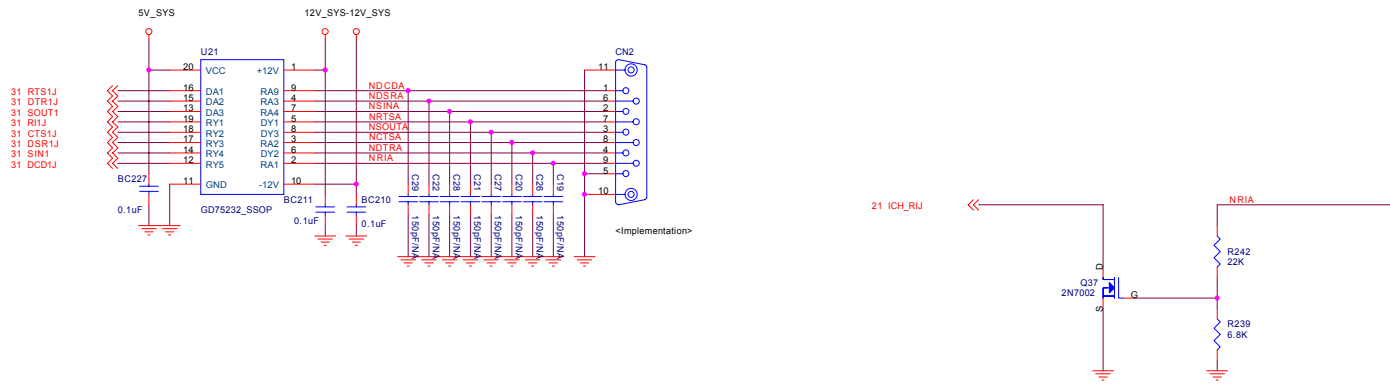
Title: **KEYBOARD/Mouse/Fan**

Size C Document Number: **865A05** Rev S

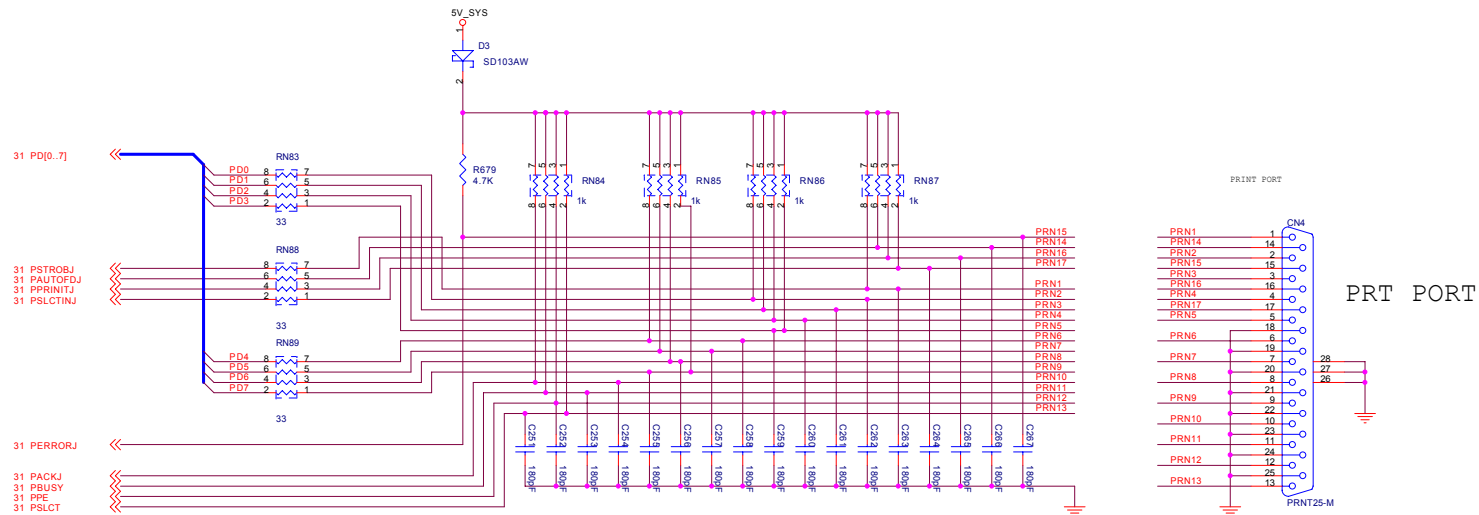
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SERIAL PORT1



PRINT PORT



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ICH5 GPIO Summary

Name	Power Plane	Type	Description
GPIO0	Main	I	REQA#
GPIO1	Main	I	REQ5#
GPIO2	Main	I	PIRQE#
GPIO3	Main	I	PIRQF#
GPIO4	Main	I	PIRQG#
GPIO5	Main	I	PIRQH#
GPIO6	Main	I	Pull_up resistor 10K (Non-use)
GPIO7	Main	I	Pull_up resistor 10K (Non-use)
GPIO8	Resume	I	Not Implement
GPIO9	Resume	I	OC4#
GPIO10	Resume	I	OC5#
GPIO11	Resume	I	Not Implement
GPIO12	Resume	I	LPC PME#
GPIO13	Resume	I	SLEEPJ
GPIO14	Resume	I	OC6#
GPIO15	Resume	I	OC7#
GPIO16	Main	O	GNTA#
GPIO17	Main	O	GNT5#
GPIO18	Main	O	Not Implement
GPIO19	Main	O	Not Implement
GPIO20	Main	O	Not Implement
GPIO21	Main	O	Not Implement
GPIO22	Main	OD	WPJ
GPIO23	Main	O	GP023 (Debug Led)
GPIO24	Resume	I/O	GPIO24
GPIO25	Resume	I/O	GPIO25
GPIO26			Not Implement
GPIO27	Resume	I/O	S3LED
GPIO28	Resume	I/O	S1LED
GPIO29			Not Implement
GPIO30			Not Implement
GPIO31			Not Implement
GPIO32	Main	I/O	Not Implement
GPIO33	Main	I/O	SATA_LED
GPIO34	Main	I/O	Not Implement
GPIO35	N/A		Not Implement
GPIO36	N/A		Not Implement
GPIO37	N/A		Not Implement
GPIO38	N/A		Not Implement
GPIO39	N/A		Not Implement
GPIO40	Main	I	REQ4#
GPIO41	Main	I	LDRQ1#
GPIO42	N/A		Not Implement
GPIO43	N/A		Not Implement
GPIO44	N/A		Not Implement
GPIO45	N/A		Not Implement
GPIO46	N/A		Not Implement
GPIO47	N/A		Not Implement
GPIO48	Main	O	GNT4#
GPIO49	Main	OD	CPUPWRGD

Super I/O GPIO Summary

Name	Power Plane	Type	Description
GPIO50	Main	I/OD	JACX
GPIO51	Main	I/OD	JACY
GPIO52	Main	I/OD	JBCX
GPIO53	Main	I/OD	JBCY
GPIO54	Main	I/OD	JAB1
GPIO55	Main	I/OD	JAB2
GPIO56	Main	I/OD	JBB1
GPIO57	Main	I/OD	JBB2

FWH GPIO Summary

Name	Power Plane	Type	Description
FGPIO	Main	I	IDE2 Detect 33/66/100
FGPI1	Main	I	IDE1 Detect 33/66/100
FGPI2	Main	I	Unused
FGPI3	Main	I	Unused

PCI Routing Summary

	AGP	PCI1	PCI2	PCI3	PCI4	PCI5
INTA#	A		B		D	D
INTB#	B		C		A	C
INTC#			D		B	A
INTD#			A		C	B
INTE#		D		C		
INTF#		A		D		
INTG#		B		A		
INTH#		C		B		
REG#/GNT#		0	2	1	4	3
IDSEL		16	18	17	20	19

PCI Dev	Interrupt	Req/Gnt	ID Select
PCI1	FGHE	0	AD16
PCI2	DABC	2	AD18
PCI3	GHEF	1	AD17
PCI4	BCDA	4	AD20
PCI5	CDBA	3	AD19

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Title: GPIO / IRQ / IDESEL Map

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Jumper Setting Summary

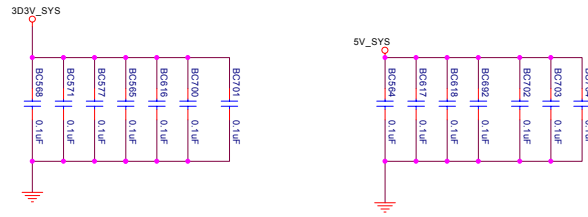
JP3	Clear CMOS 1-2 : Normal (Default) 2-3 : Clear CMOS
CN18	Chassis Intruder 1 : Intruder 2 : GND
CN21	Wake On LAN 1 : 5V Standy Power 2 : GND 3 : Detect
CN20	Front Plane Header (2X9 Key14) 1-3 : HDD LED 2-4 : Power LED 5-7 : Reset Switch 6-8 : Power Switch 10 : Chassis ID0 17 : Chassis ID1

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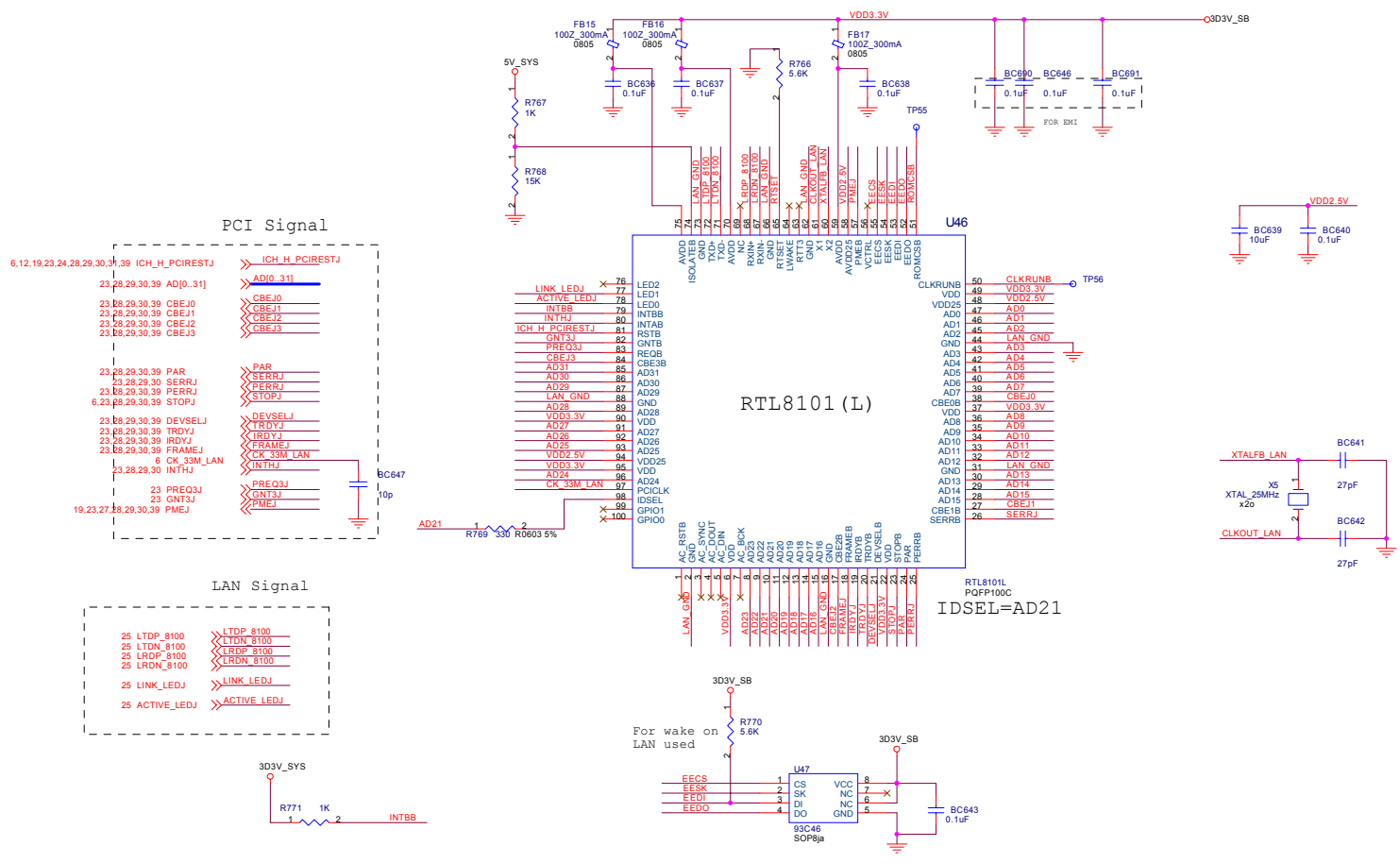
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To mogran hill:NA R193,Q34,R142,Q26,R164,R166,Q31,R138
NA CN16,R206,BC94,BC102,BC82,BC150,BC149,BC146

655 audio:add R828 0,R829 0,R826 4.7K,R825 10K,C274 1uF,R827 10K,C275 1uF,R830 10K,C276 1uF.

add C279.del R80,R67,R75,R72,R68,R66,C33,C34

change PWM from 2 phase to 3 phase:

change R652 68K to 30K,BC596 1200PF to 470PF.

add BC660 220PF, R821 30K 1%,R822 20K 1%,BC659 5600PF.change R640 250 to 1.5k 1%.

add BC655 0.1uF.change R649 499 5% to 1%.add D26 1N4148,BC652 1uF,R817 0,U54 SC1211,BC654 4.7uF,R818 1,R819 100,BC653 1nF,
BC656 2200pF,BC658 4.7uF,Q115 IPD04N03L,Q114 IPD09N03L,BC650 4.7uF,BC651 4.7uF,L19 coil-600nh-60mg,R820 1,BC657 4700pF.

del Q105 06N03L,Q101 06N03L.change R475 from 1k to 2k,R815 from 470 to 1k,R816 from 470 to 1k.
NA EC56

add R847 0

change SIO to 83627HF

add FB19,BC661,R837,RT6,R836,R835,R834,FB18,R833,R831,R832,R669,R246,BC447,BC604,D27,R838,R840,R844

1394: add page 39

PCI arbiter:add u57,bc682,bc683,bc684,bc685,r871,r873,r875,bc686,bc687,bc688

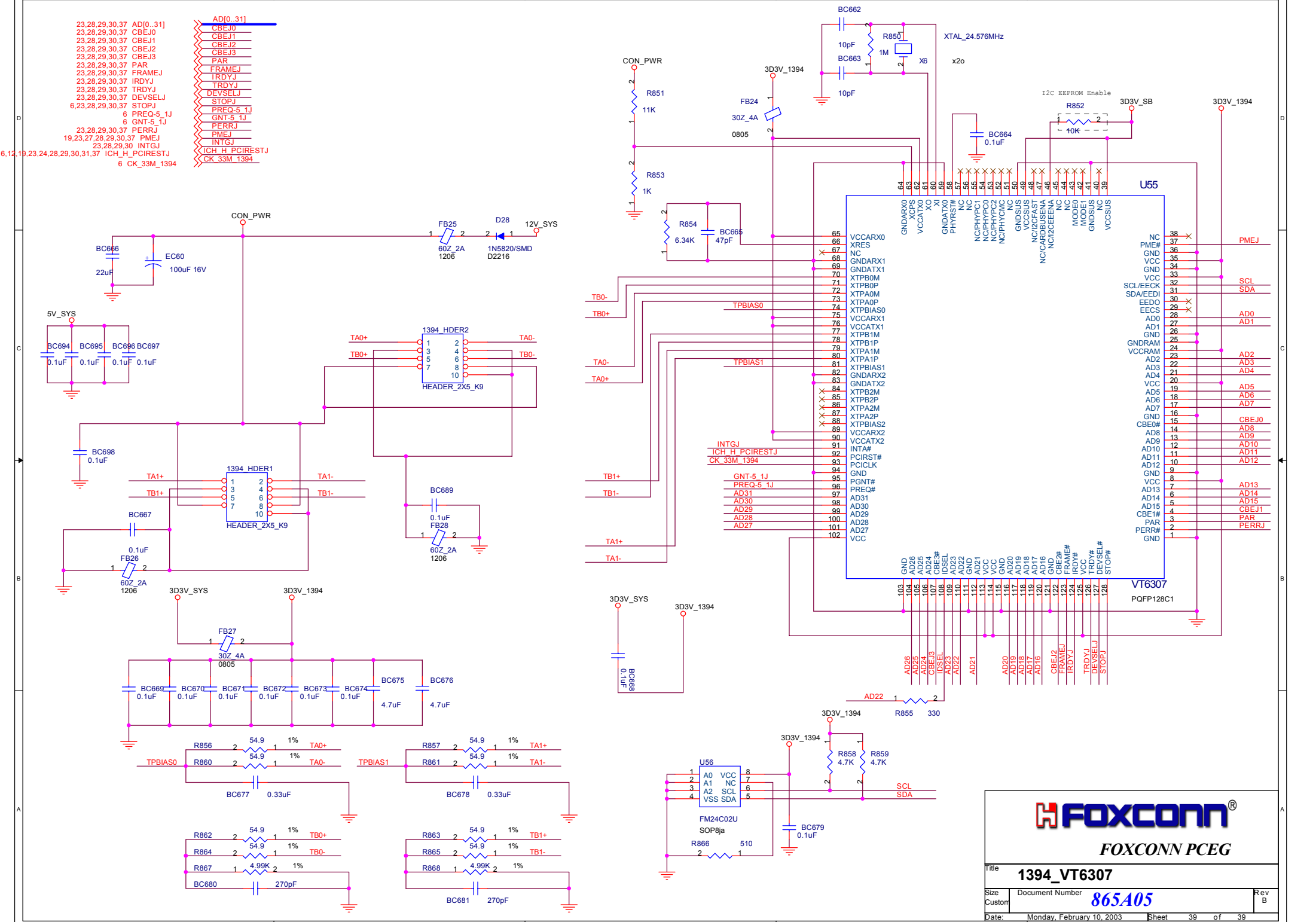
add F10,1394 Header2,BC689,FB28

Front header: add R879,R880,R881,R882

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- 23,28,29,30,37 AD[0..31]
- 23,28,29,30,37 CBEJ0
- 23,28,29,30,37 CBEJ1
- 23,28,29,30,37 CBEJ2
- 23,28,29,30,37 CBEJ3
- 23,28,29,30,37 PAR
- 23,28,29,30,37 FRAMEJ
- 23,28,29,30,37 IRDYJ
- 23,28,29,30,37 TRDYJ
- 23,28,29,30,37 DEVSELJ
- 23,28,29,30,37 STOPJ
- 6,23,28,29,30,37 PREQ-5_1J
- 6 GNT-5_1J
- 23,28,29,30,37 PERRJ
- 19,23,27,28,29,30,37 PMEJ
- 23,28,29,30 INTGJ
- 6,12,19,23,24,28,29,30,31,37 ICH_H_PCIRESTJ
- 6 CK_33M_1394

- AD[0..31]
- CBEJ0
- CBEJ1
- CBEJ2
- CBEJ3
- PAR
- FRAMEJ
- IRDYJ
- TRDYJ
- DEVSELJ
- STOPJ
- PREQ-5_1J
- GNT-5_1J
- PERRJ
- PMEJ
- INTGJ
- ICH_H_PCIRESTJ
- CK_33M_1394

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Title: **1394_VT6307**

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