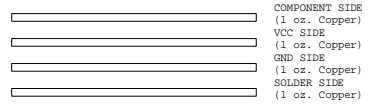


# GIGABYTE GA-8I848E-L Schematics

Revision  
1.01

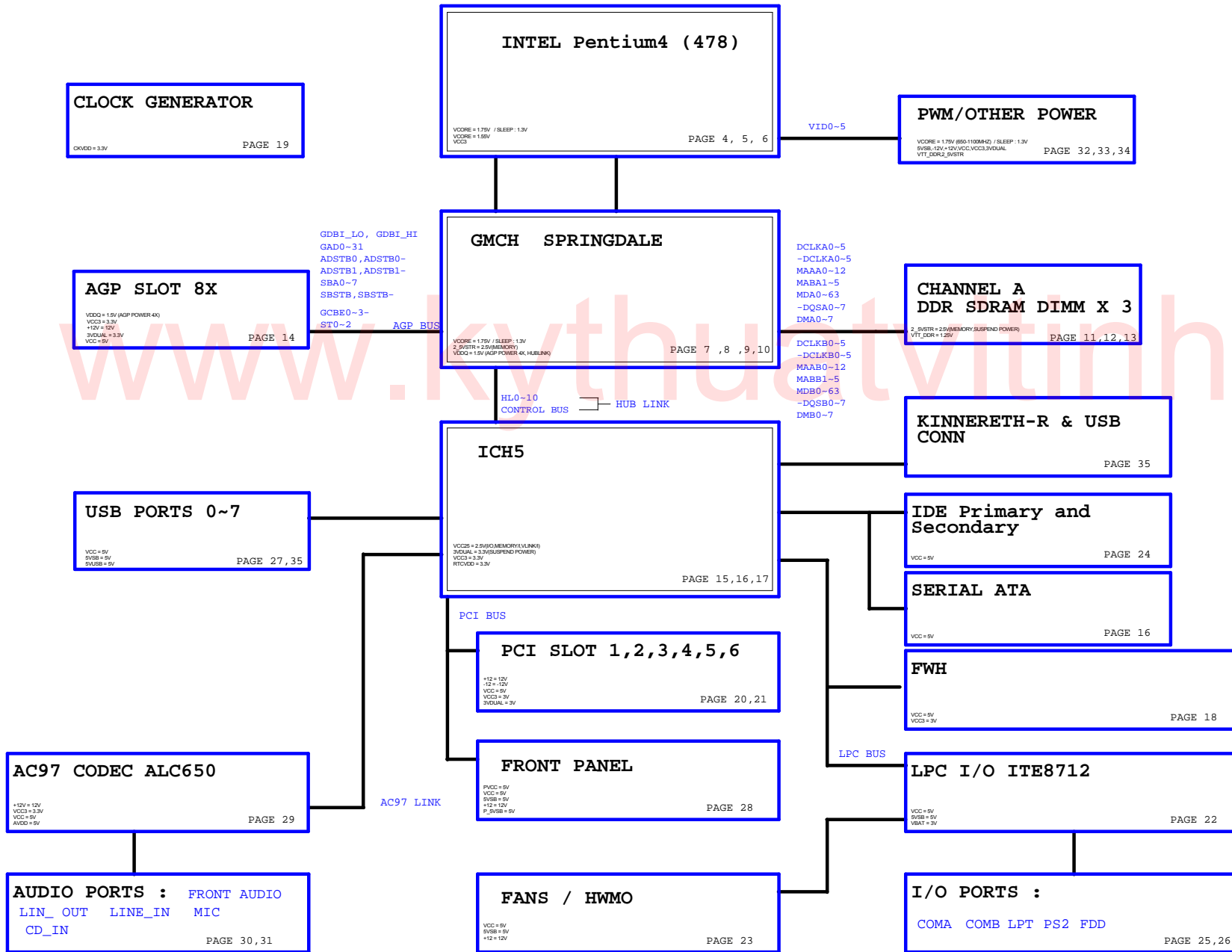
SHEET	TITLE
01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	P4_478A
05	P4_478B
06	P4_478C
07	SPRINGDALE HOST
08	SPRINGDALE DDR
09	SPRINGDALE AGP, HUB, CSA, VGA
10	SPRINGDALE PWR
11	DDR1,2 CHANNEL A
12	DDR3 CHANNEL A
13	DDR TERMINATION
14	AGP
15	ICH5 PCI, USB, HUB, LAN
16	ICH5 IDE, GPIO, SATA, CTRL
17	ICH5 VCC, GND
18	FWH
19	ICS952603 CLOCK GEN
20	PCI1_2
21	PCI3_4
22	PCI5_6

SHEET	TITLE
23	CODEC
24	AUDIO JACK, L_OUT, F_AUDIO
25	ITE 8712
26	COM_LPT
27	IDE
28	FAN/HWMO
29	KB_PS2
30	FPANEL
31	USB CONN
32	DDR POWER
33	VCORE POWER
34	ATX, OTHERS POWER
35	KINNERETH-R LNA(CSA-1)
36	KINNERETH-R LNA(CSA-2)
37	KINNERETH-R LNA(CSA-3)

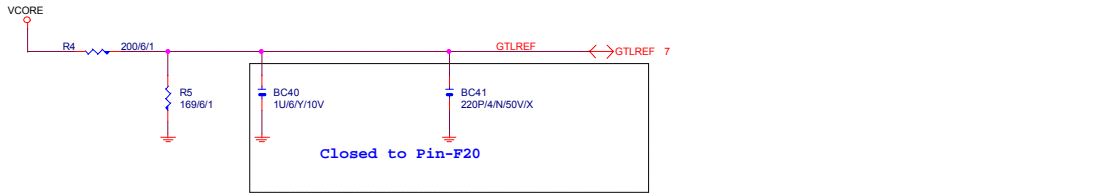
	
<b>GIGABYTE CORP.</b>	
Title: COVER SHEET	
Size: Custom	Document Number: GA-8I848E-L
Date:	Rev: 1.01
Sheet 1 of 38	



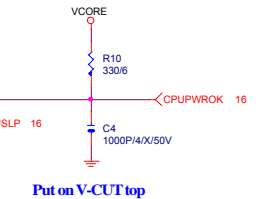
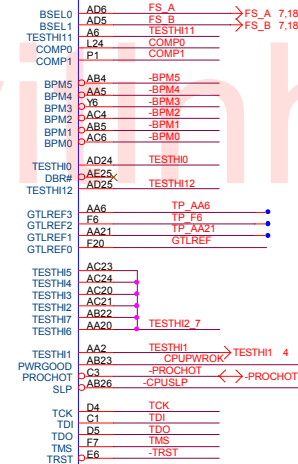
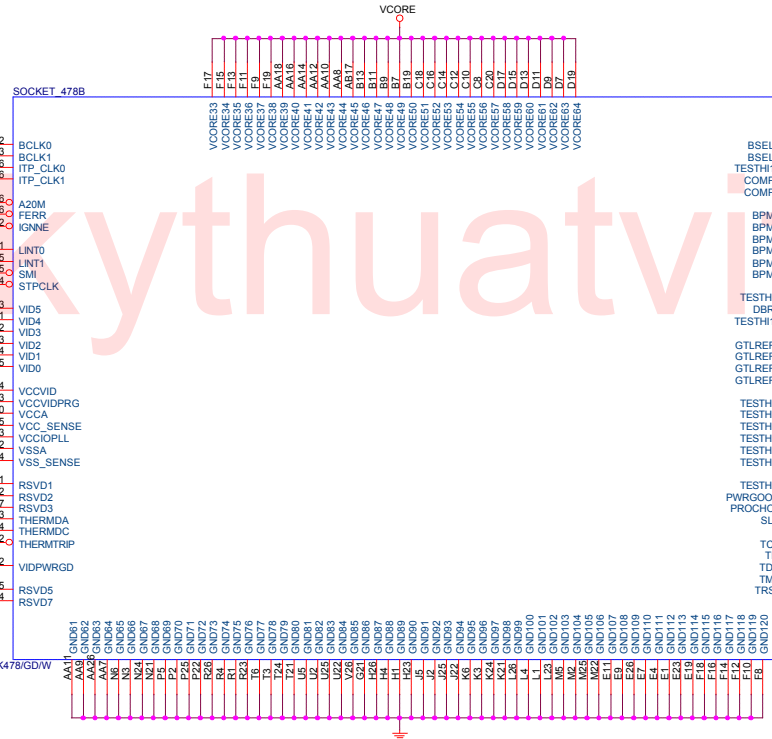
# BLOCK DIAGRAM





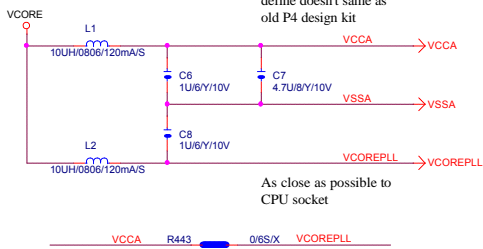


Place outside of CPU socket



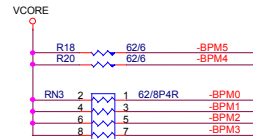
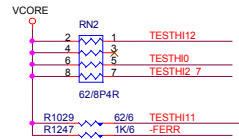
Put on V-CUT top

**Note:**  
VCCA & VCOREPLL  
define doesn't same as  
old P4 design kit

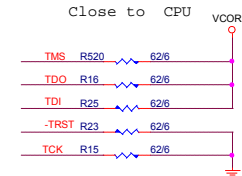


As close as possible to CPU socket

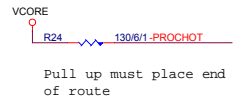
Trace width doesn't less than 12 Mil



Close to CPU

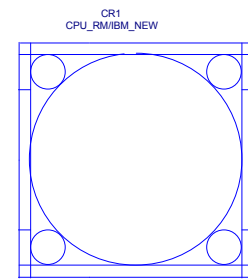
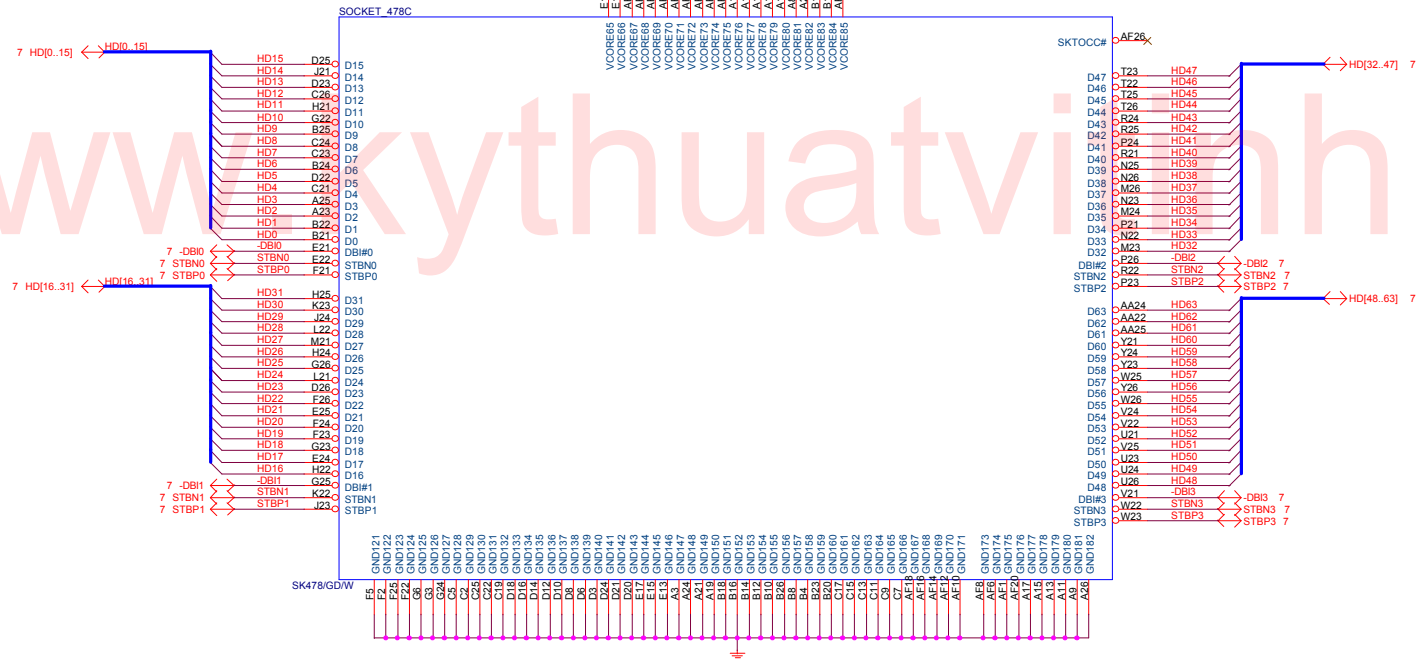
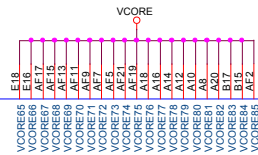
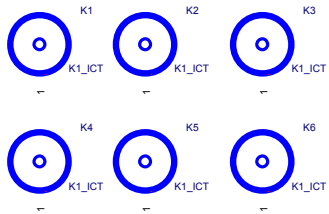


Close to CPU

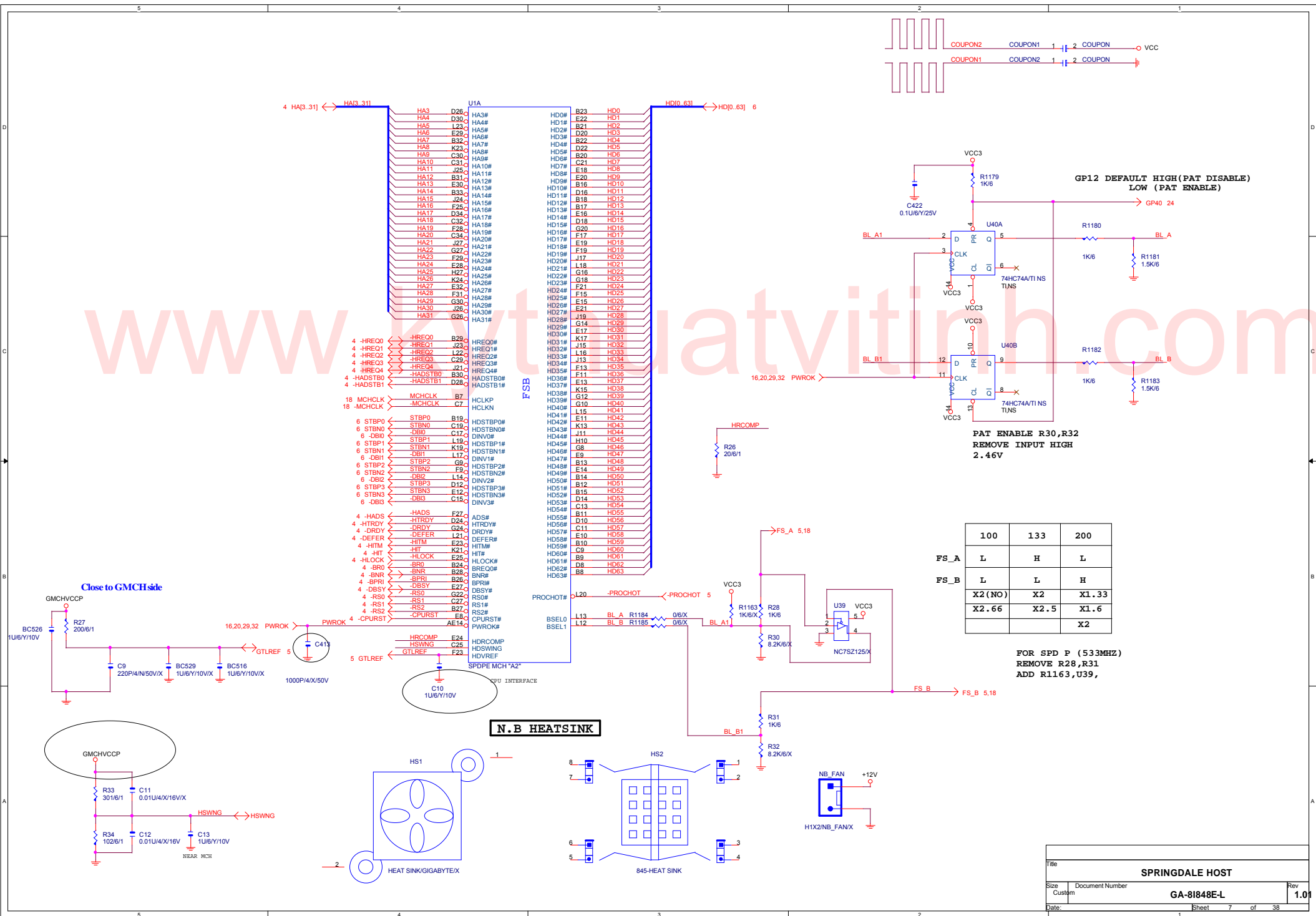


Pull up must place end of route

Title			P4 478B		
Size	Document Number			Rev	
Custom	GA-81848E-L			1.01	
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Title			P4 478C		
Size	Document Number				Rev
Custom	GA-81848E-L				1.01
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	100	133	200
FS_A	L	H	L
FS_B	L	L	H
X2 (NO)	X2	X2	X1.33
X2.66	X2.5	X2.5	X1.6
			X2

FOR SPD P (533MHZ)  
REMOVE R28,R31  
ADD R1163,U39,

11,12,13 MAAA[0..12] ↔ MAAA0\_121  
 11,12 MABA[1..5] ↔ MABA1\_51  
 11,12,13 DMA[0..7] ↔ DMA0\_71  
 11,12,13 MDA[0..63] ↔ MDA0\_631  
 11,12,13 DQSA[0..7] ↔ DQSA0\_71

**U1B**

MAAA0 AJ34 SMAA\_A0  
 MAAA1 AL33 SMAA\_A1  
 MAAA2 AK29 SMAA\_A2  
 MAAA3 AN31 SMAA\_A3  
 MAAA4 AL30 SMAA\_A4  
 MAAA5 AL28 SMAA\_A5  
 MAAA6 AL28 SMAA\_A6  
 MAAA7 AN25 SMAA\_A7  
 MAAA8 AP26 SMAA\_A8  
 MAAA9 AP24 SMAA\_A9  
 MAAA10 AJ33 SMAA\_A10  
 MAAA11 AN23 SMAA\_A11  
 MAAA12 AN21 SMAA\_A12

MABA1 AL34 SMAB\_A1  
 MABA2 AM34 SMAB\_A2  
 MABA3 AP32 SMAB\_A3  
 MABA4 AP31 SMAB\_A4  
 MABA5 AM26 SMAB\_A5

SWEA AB34 SWE\_A#  
 SCASA Y34 SCAS\_A#  
 SRASA AC33 SRAS\_A#

SBA0 AE33 SBA\_A0  
 SBA1 AH34 SBA\_A1

CSA0 AA34 SCS\_A0#  
 CSA1 Y21 SCS\_A1#  
 CSA2 Y32 SCS\_A2#  
 CSA3 W34 SCS\_A3#

CKEA0 AL20 SCKE\_A0  
 CKEA1 AN19 SCKE\_A1  
 CKEA2 AM20 SCKE\_A2  
 CKEA3 AP20 SCKE\_A3

DCLKA0 AK32 SCMDCLK\_A0#  
 DCLKA1 AP17 SCMDCLK\_A1#  
 DCLKA2 N33 SCMDCLK\_A2#  
 DCLKA2 N34 SCMDCLK\_A2#  
 DCLKA3 AK33 SCMDCLK\_A3#  
 DCLKA4 AM16 SCMDCLK\_A4#  
 DCLKA4 AL16 SCMDCLK\_A4#  
 DCLKA5 P31 SCMDCLK\_A5#  
 DCLKA5 P32 SCMDCLK\_A5#

DDRVRIFA E34 SMVREF\_A  
 SMXRCOMP AK9 SMXRCOMP  
 SMXRCOMPVOH AN9 SMXRCOMPVOH  
 SMXRCOMPVOL AL9 SMXRCOMPVOL

**SDQS\_A0** AN11 DQSA0  
 SDQ\_A0 AP10 MDA0  
 SDQ\_A1 AP11 MDA1  
 SDQ\_A2 AM12 MDA2  
 SDQ\_A3 AN13 MDA3  
 SDQ\_A4 AM10 MDA4  
 SDQ\_A5 AL10 MDA5  
 SDQ\_A6 AL12 MDA6  
 SDQ\_A7 AP13 MDA7

SDQS\_A1 AP15 DQSA1  
 SDQ\_A8 AP14 MDA8  
 SDQ\_A9 AM14 MDA9  
 SDQ\_A10 AL18 MDA10  
 SDQ\_A11 AL14 MDA11  
 SDQ\_A12 AL14 MDA12  
 SDQ\_A13 AN15 MDA13  
 SDQ\_A14 AP18 MDA14  
 SDQ\_A15 AM18 MDA15

SDQS\_A2 AP23 DQSA2  
 SDQ\_A16 AP22 MDA16  
 SDQ\_A17 AM22 MDA17  
 SDQ\_A18 AL24 MDA18  
 SDQ\_A19 AN27 MDA19  
 SDQ\_A20 AP21 MDA20  
 SDQ\_A21 AL22 MDA21  
 SDQ\_A22 AP25 MDA22  
 SDQ\_A23 AP27 MDA23

SDQS\_A3 AM30 DQSA3  
 SDQ\_A24 AP28 MDA24  
 SDQ\_A25 AP25 MDA25  
 SDQ\_A26 AP33 MDA26  
 SDQ\_A27 AM33 MDA27  
 SDQ\_A28 AM28 MDA28  
 SDQ\_A29 AN29 MDA29  
 SDQ\_A30 AM31 MDA30  
 SDQ\_A31 AN34 MDA31

SDQS\_A4 AF34 DQSA4  
 SDQ\_A32 AH32 MDA32  
 SDQ\_A33 AF34 MDA33  
 SDQ\_A34 AF32 MDA34  
 SDQ\_A35 AD32 MDA35  
 SDQ\_A36 AH31 MDA36  
 SDQ\_A37 AG33 MDA37  
 SDQ\_A38 AE34 MDA38  
 SDQ\_A39 AD34 MDA39

SDQS\_A5 V34 DQSA5  
 SDQ\_A40 AC34 MDA40  
 SDQ\_A41 AB31 MDA41  
 SDQ\_A42 V32 MDA42  
 SDQ\_A43 V31 MDA43  
 SDQ\_A44 AD31 MDA44  
 SDQ\_A45 AB32 MDA45  
 SDQ\_A46 U34 MDA46  
 SDQ\_A47 U33 MDA47

SDQS\_A6 M32 DQSA6  
 SDQ\_A48 T34 MDA48  
 SDQ\_A49 T32 MDA49  
 SDQ\_A50 K34 MDA50  
 SDQ\_A51 K32 MDA51  
 SDQ\_A52 T31 MDA52  
 SDQ\_A53 P34 MDA53  
 SDQ\_A54 L34 MDA54  
 SDQ\_A55 L33 MDA55

SDQS\_A7 H31 DQSA7  
 SDQ\_A56 J33 MDA56  
 SDQ\_A57 H34 MDA57  
 SDQ\_A58 E33 MDA58  
 SDQ\_A59 F32 MDA59  
 SDQ\_A60 K31 MDA60  
 SDQ\_A61 J34 MDA61  
 SDQ\_A62 G34 MDA62  
 SDQ\_A63 F34 MDA63

**U1C**

SMAA\_B0 AP12 MDA0  
 SMAA\_B1 AP10 MDA0  
 SMAA\_B2 AP11 MDA1  
 SMAA\_B3 AM12 MDA2  
 SMAA\_B4 AN13 MDA3  
 SMAA\_B5 AM10 MDA4  
 SMAA\_B6 AL10 MDA5  
 SMAA\_B7 AL12 MDA6  
 SMAA\_B8 AP13 MDA7

SMAA\_B9 AP15 MDA8  
 SMAA\_B10 AP14 MDA8  
 SMAA\_B11 AM14 MDA9  
 SMAA\_B12 AL18 MDA10

SMAB\_B1 AL18 MDA11  
 SMAB\_B2 AL14 MDA12  
 SMAB\_B3 AN15 MDA13  
 SMAB\_B4 AP18 MDA14  
 SMAB\_B5 AM18 MDA15

SWE\_B# W27 SWE\_B#  
 SCAS\_B# W31 SCAS\_B#  
 SRAS\_B# W26 SRAS\_B#

SBA\_B0 Y25 SBA\_B0  
 SBA\_B1 Y25 SBA\_B1

SCS\_B0# U26 SCS\_B0#  
 SCS\_B1# U29 SCS\_B1#  
 SCS\_B2# Y25 SCS\_B2#  
 SCS\_B3# W26 SCS\_B3#

SCKE\_B0 AK19 SCKE\_B0  
 SCKE\_B1 AF19 SCKE\_B1  
 SCKE\_B2 AG19 SCKE\_B2  
 SCKE\_B3 AE19 SCKE\_B3

SCMDCLK\_B0 AG29 SCMDCLK\_B0#  
 SCMDCLK\_B0# AG30 SCMDCLK\_B0#  
 SCMDCLK\_B1 AE17 SCMDCLK\_B1#  
 SCMDCLK\_B1# AG17 SCMDCLK\_B1#  
 SCMDCLK\_B2 N27 SCMDCLK\_B2#  
 SCMDCLK\_B2# N27 SCMDCLK\_B2#  
 SCMDCLK\_B3 X26 SCMDCLK\_B3#  
 SCMDCLK\_B3# X26 SCMDCLK\_B3#  
 SCMDCLK\_B4 AH29 SCMDCLK\_B4#  
 SCMDCLK\_B4# AK15 SCMDCLK\_B4#  
 SCMDCLK\_B5 AL15 SCMDCLK\_B5#  
 SCMDCLK\_B5# N30 SCMDCLK\_B5#

SMVREF\_B AP9 SMVREF\_B  
 SMYRCOMP AA33 SMYRCOMP  
 SMYRCOMPVOH R34 SMYRCOMPVOH  
 SMYRCOMPVOL R33 SMYRCOMPVOL

SDQS\_B0 AP12 MDA0  
 SDQ\_B0 AP10 MDA0  
 SDQ\_B1 AP11 MDA1  
 SDQ\_B2 AM12 MDA2  
 SDQ\_B3 AN13 MDA3  
 SDQ\_B4 AM10 MDA4  
 SDQ\_B5 AL10 MDA5  
 SDQ\_B6 AL12 MDA6  
 SDQ\_B7 AP13 MDA7

SDQS\_B1 AP15 MDA8  
 SDQ\_B8 AP14 MDA8  
 SDQ\_B9 AM14 MDA9  
 SDQ\_B10 AL18 MDA10  
 SDQ\_B11 AL14 MDA11  
 SDQ\_B12 AL14 MDA12  
 SDQ\_B13 AN15 MDA13  
 SDQ\_B14 AP18 MDA14  
 SDQ\_B15 AM18 MDA15

SDQS\_B2 AG21 DQSA2  
 SDQ\_B16 AP22 MDA16  
 SDQ\_B17 AM22 MDA17  
 SDQ\_B18 AL24 MDA18  
 SDQ\_B19 AN27 MDA19  
 SDQ\_B20 AP21 MDA20  
 SDQ\_B21 AL22 MDA21  
 SDQ\_B22 AP25 MDA22  
 SDQ\_B23 AP27 MDA23

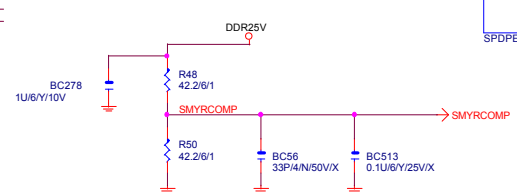
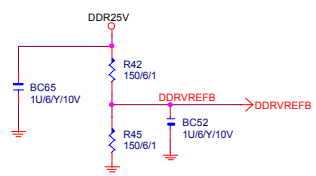
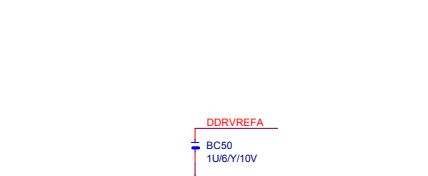
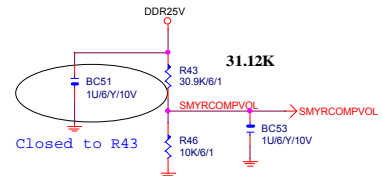
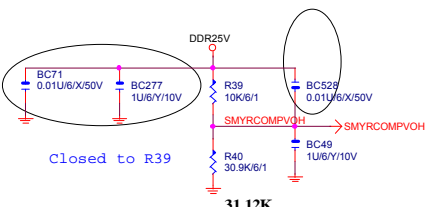
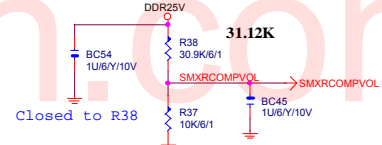
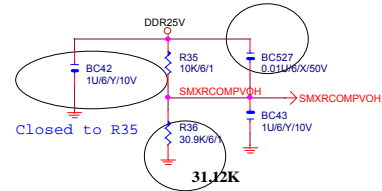
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 SDQ\_B24 AP28 MDA24  
 SDQ\_B25 AP25 MDA25  
 SDQ\_B26 AP33 MDA26  
 SDQ\_B27 AM33 MDA27  
 SDQ\_B28 AM28 MDA28  
 SDQ\_B29 AN29 MDA29  
 SDQ\_B30 AM31 MDA30  
 SDQ\_B31 AN34 MDA31

SDQS\_B4 AF34 DQSA4  
 SDQ\_B32 AH32 MDA32  
 SDQ\_B33 AF34 MDA33  
 SDQ\_B34 AF32 MDA34  
 SDQ\_B35 AD32 MDA35  
 SDQ\_B36 AH31 MDA36  
 SDQ\_B37 AG33 MDA37  
 SDQ\_B38 AE34 MDA38  
 SDQ\_B39 AD34 MDA39

SDQS\_B5 V34 DQSA5  
 SDQ\_B40 AC34 MDA40  
 SDQ\_B41 AB31 MDA41  
 SDQ\_B42 V32 MDA42  
 SDQ\_B43 V31 MDA43  
 SDQ\_B44 AD31 MDA44  
 SDQ\_B45 AB32 MDA45  
 SDQ\_B46 U34 MDA46  
 SDQ\_B47 U33 MDA47

SDQS\_B6 M32 DQSA6  
 SDQ\_B48 T34 MDA48  
 SDQ\_B49 T32 MDA49  
 SDQ\_B50 K34 MDA50  
 SDQ\_B51 K32 MDA51  
 SDQ\_B52 T31 MDA52  
 SDQ\_B53 P34 MDA53  
 SDQ\_B54 L34 MDA54  
 SDQ\_B55 L33 MDA55

SDQS\_B7 H31 DQSA7  
 SDQ\_B56 J33 MDA56  
 SDQ\_B57 H34 MDA57  
 SDQ\_B58 E33 MDA58  
 SDQ\_B59 F32 MDA59  
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 SDQ\_B61 J34 MDA61  
 SDQ\_B62 G34 MDA62  
 SDQ\_B63 F34 MDA63

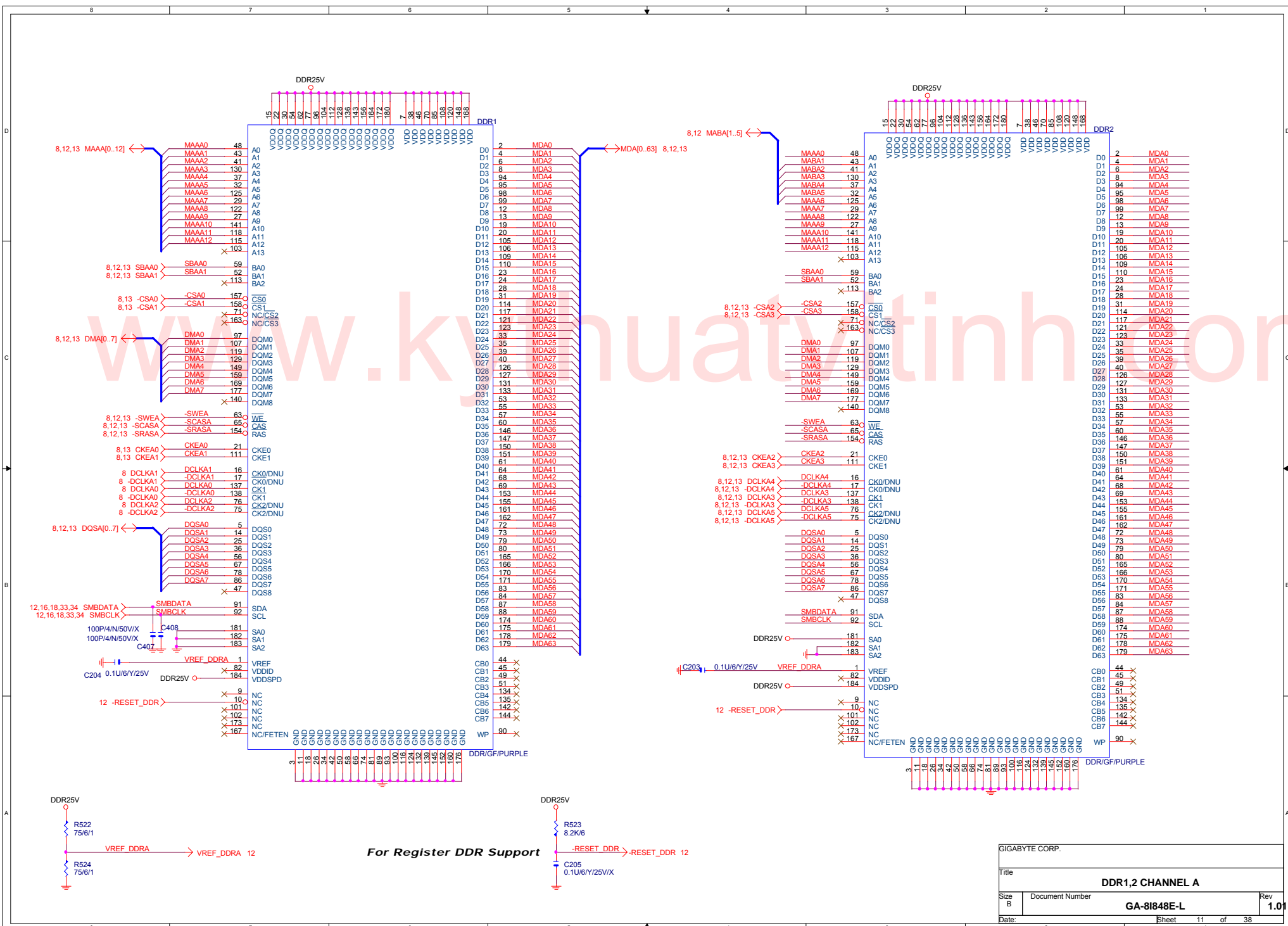


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Size	Document Number	GA-81848E-L	
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Date		Sheet	8 of 38



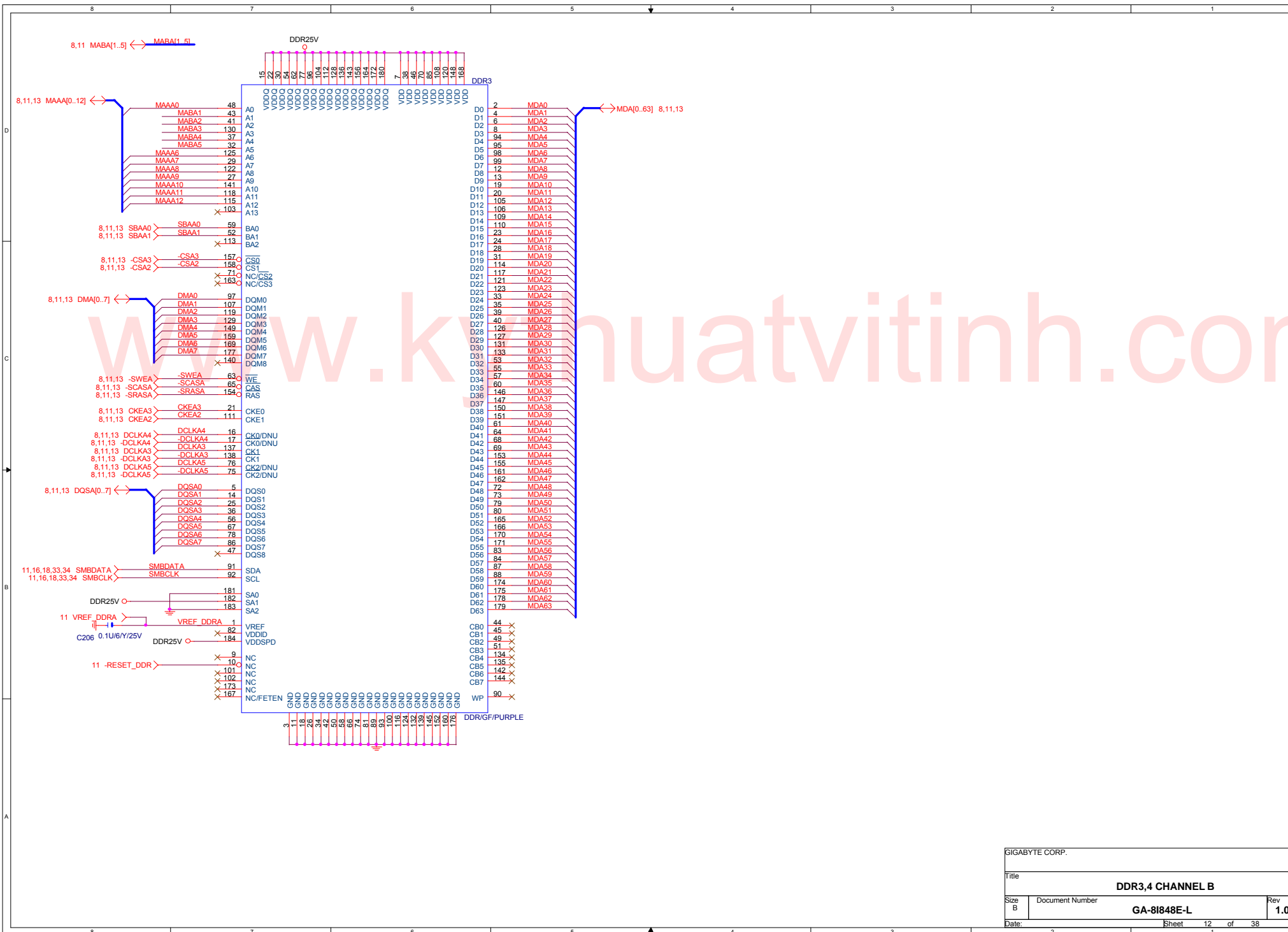






For Register DDR Support

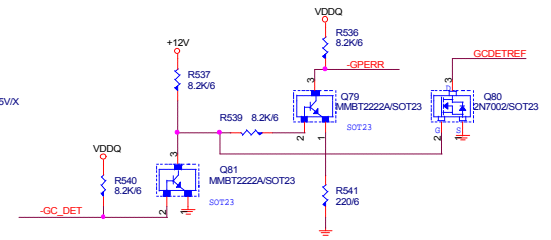
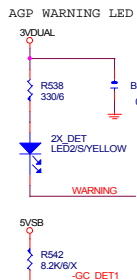
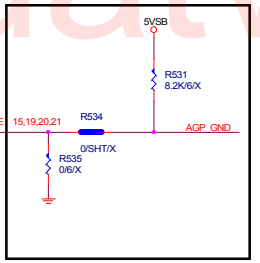
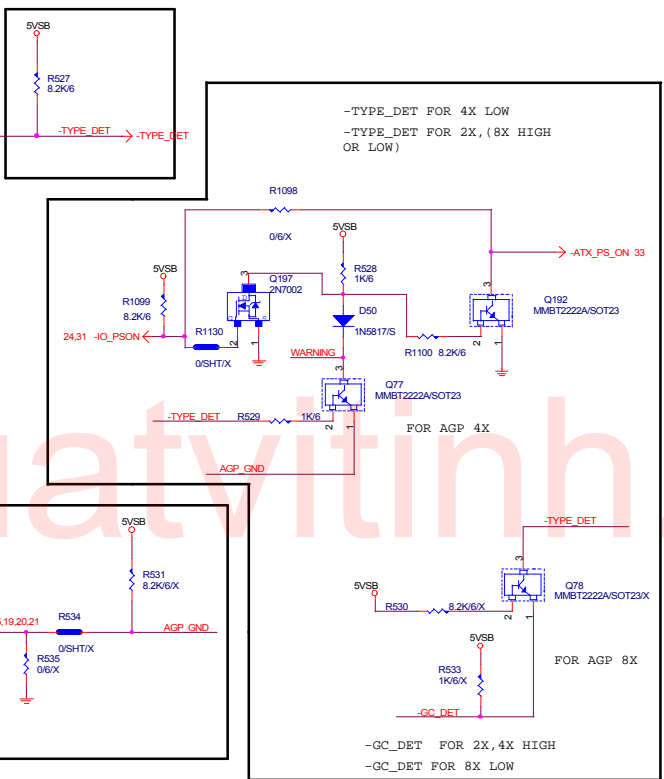
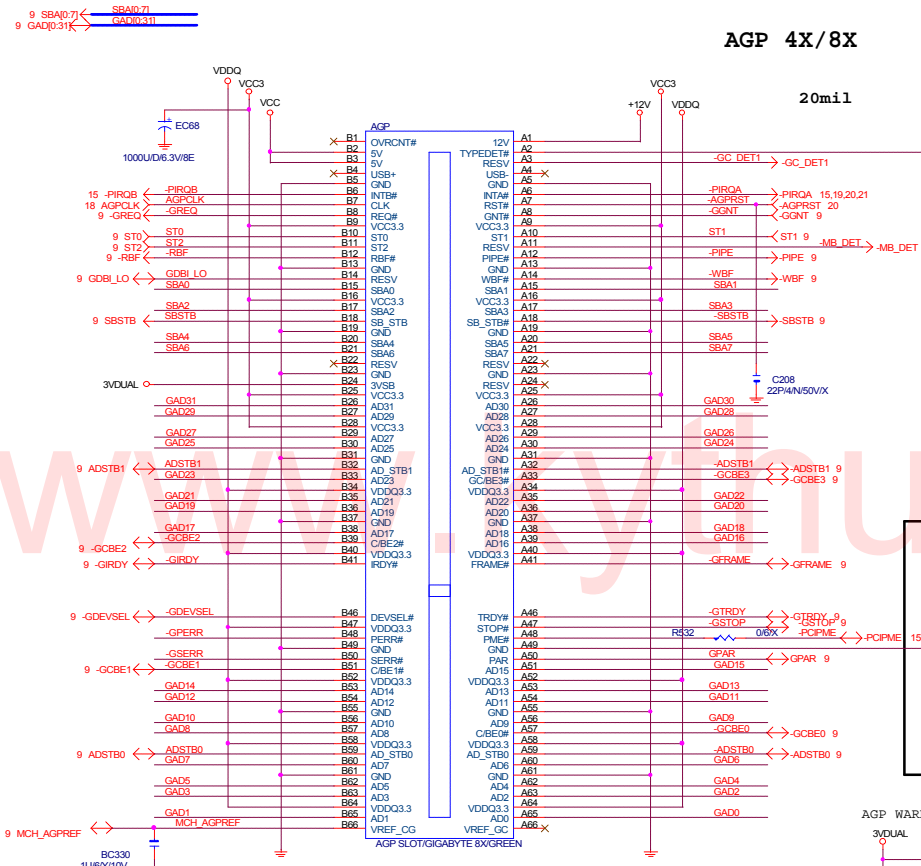
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Title		
<b>DDR1,2 CHANNEL A</b>		
Size	Document Number	Rev
B	<b>GA-8848E-L</b>	<b>1.01</b>
Date:	Sheet 11 of 38	



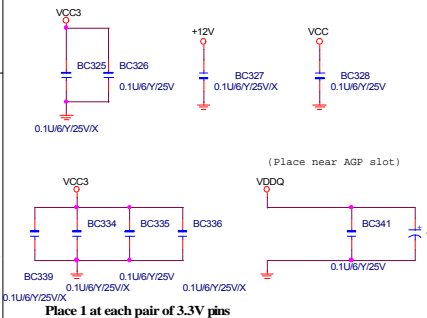


# AGP 4X/8X

20mil

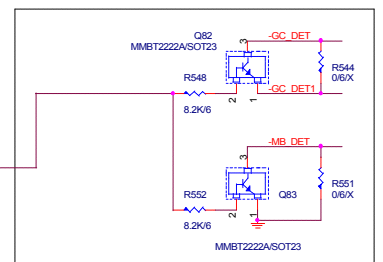


AGP_4X:	
ON	AGP 4X
OFF	AGP 8X



Place 1 at each pair of 3.3V pins

Place 1 at each pair of VDDQ pins  
Place an additional for spread from A14 - A33



Note: 1.GPO pin must power on default High

**GIGABYTE CORP.**

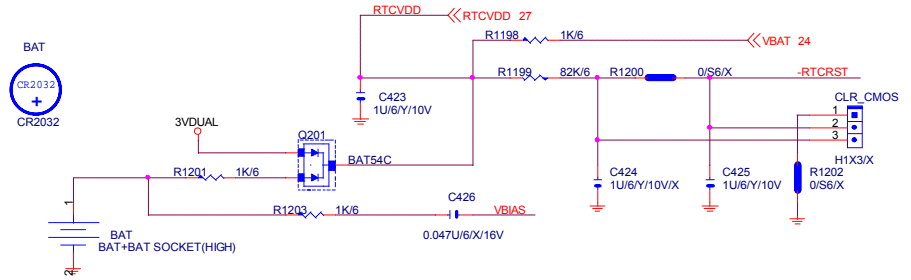
**AGP SLOT**

GA-81848E-L

Rev 1.01

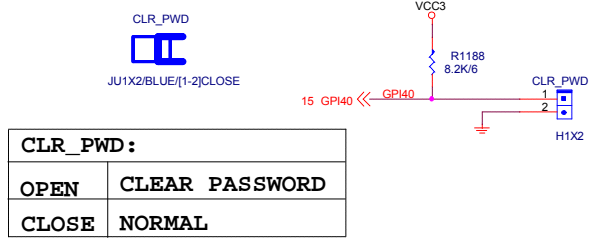
Date: 星期三, 八月 06, 2003 Sheet 14 of 38





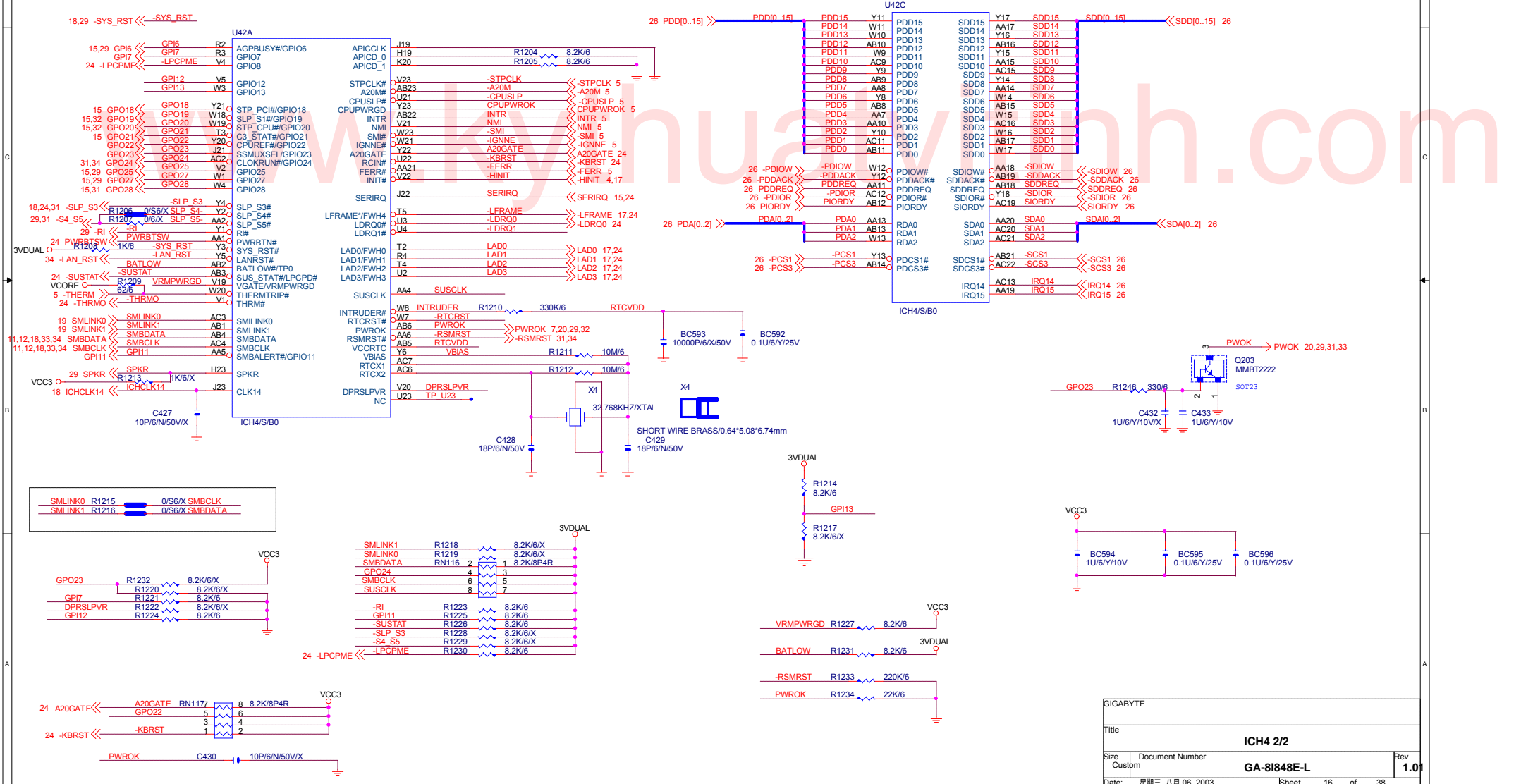
**CLR\_CMOS :**

1-2	CLEAR CMOS
2-3	NORMAL



**CLR\_PWD :**

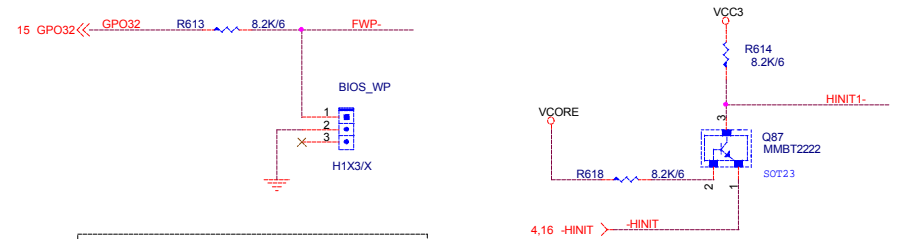
OPEN	CLEAR PASSWORD
CLOSE	NORMAL



GIGABYTE

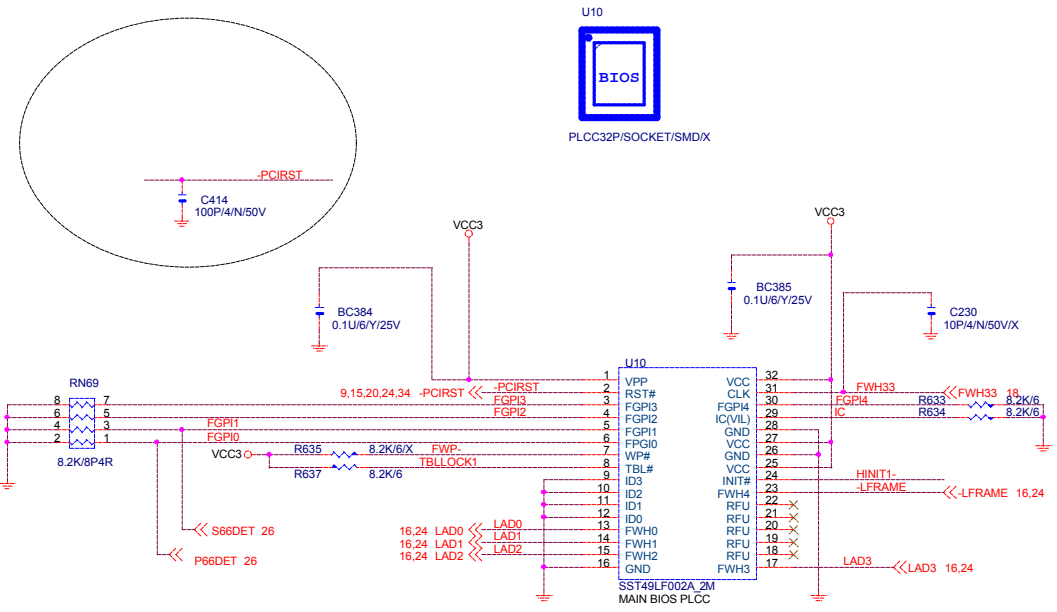
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Size	Document Number	Rev	
Custom	GA-81848E-L	1.01	
Date:	星期三, 八月 06, 2003	Sheet	16 of 38





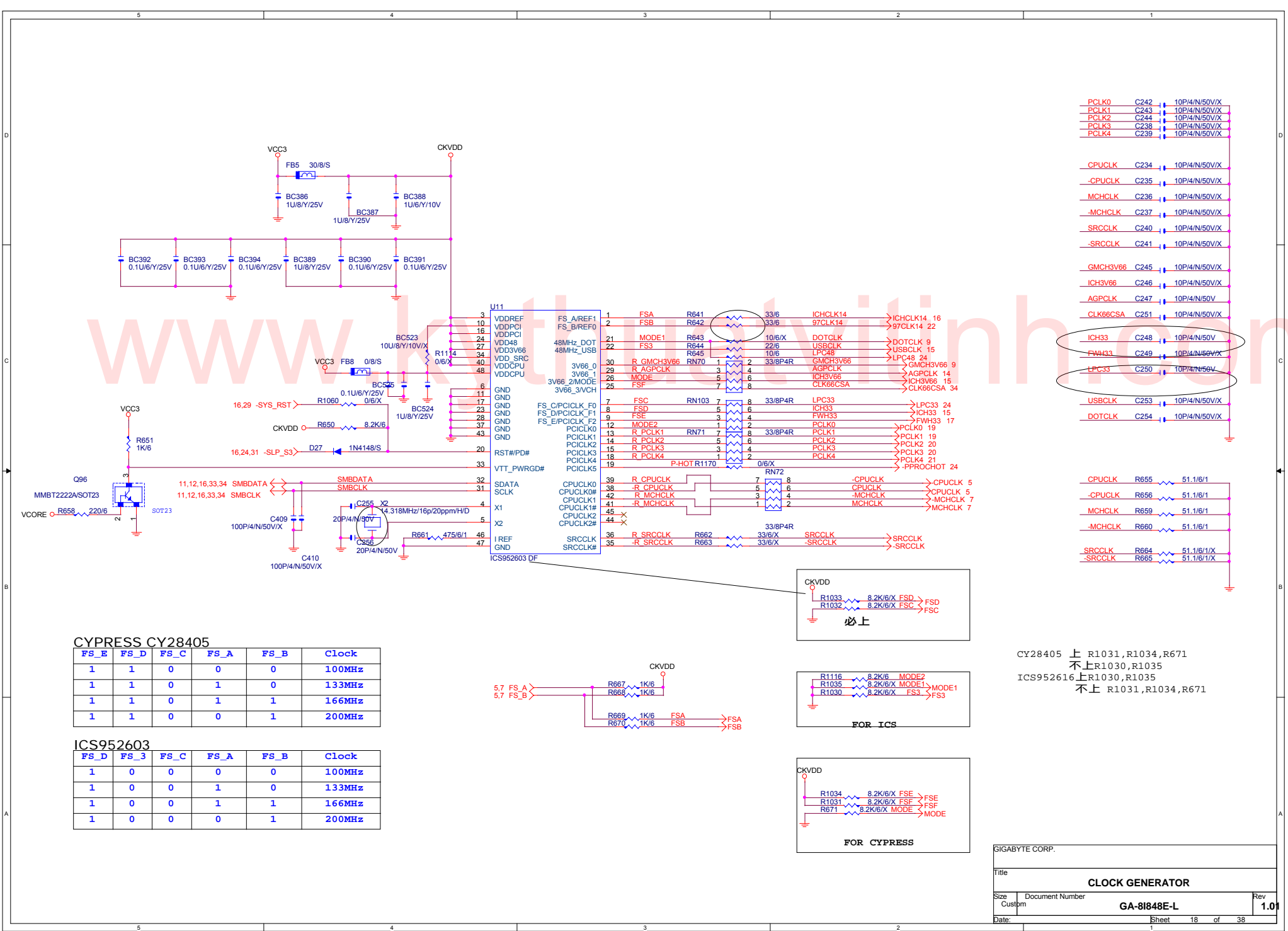
BIOS_WP:	
1-2	WRITE PROTECT
2-3	DISABLE

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ADD WINBOUD FWH SEC. SOURCE

GIGABYTE CORP.		
Title		
FWH		
Size	Document Number	Rev
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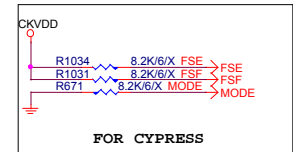
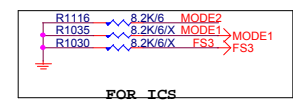
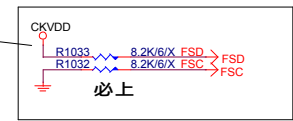
- PCLK0 C242 10P/4/N/50V/X
- PCLK1 C243 10P/4/N/50V/X
- PCLK2 C244 10P/4/N/50V/X
- PCLK3 C238 10P/4/N/50V/X
- PCLK4 C239 10P/4/N/50V/X
- CPUCLK C234 10P/4/N/50V/X
- GPUCLK C235 10P/4/N/50V/X
- MCHCLK C236 10P/4/N/50V/X
- MCHCLK C237 10P/4/N/50V/X
- SRCLK C240 10P/4/N/50V/X
- SRCLK C241 10P/4/N/50V/X
- GMCH3V66 C245 10P/4/N/50V/X
- ICH3V66 C246 10P/4/N/50V/X
- AGPCLK C247 10P/4/N/50V
- CLK66CSA C251 10P/4/N/50V/X
- ICH33 C248 10P/4/N/50V
- FWH33 C249 10P/4/N/50V/X
- LPC33 C250 10P/4/N/50V
- USBCLK C253 10P/4/N/50V/X
- DOTCLK C254 10P/4/N/50V/X
- CPUCLK R655 51.1/6/1
- GPUCLK R656 51.1/6/1
- MCHCLK R659 51.1/6/1
- MCHCLK R660 51.1/6/1
- SRCLK R664 51.1/6/1/X
- SRCLK R665 51.1/6/1/X

**CYPRESS CY28405**

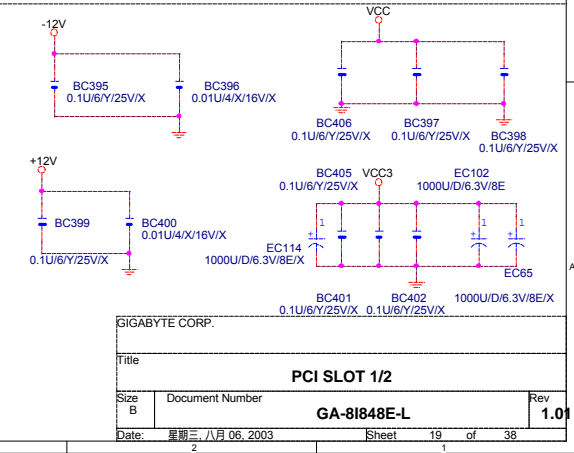
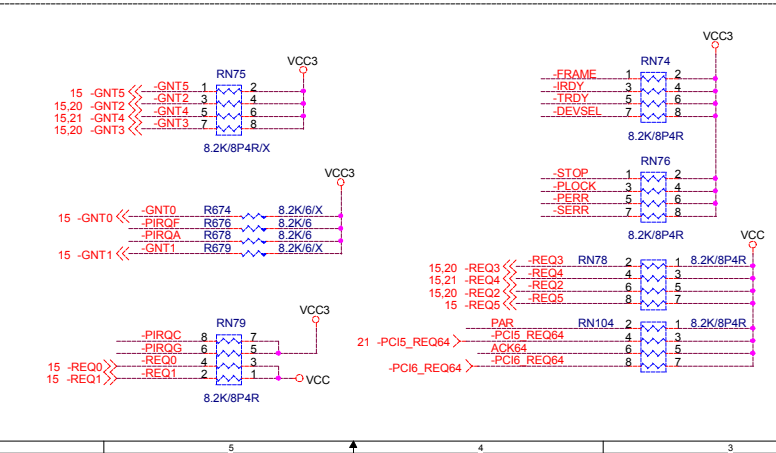
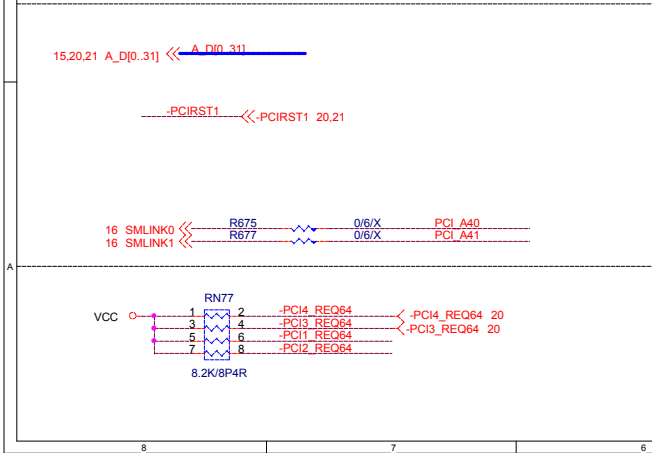
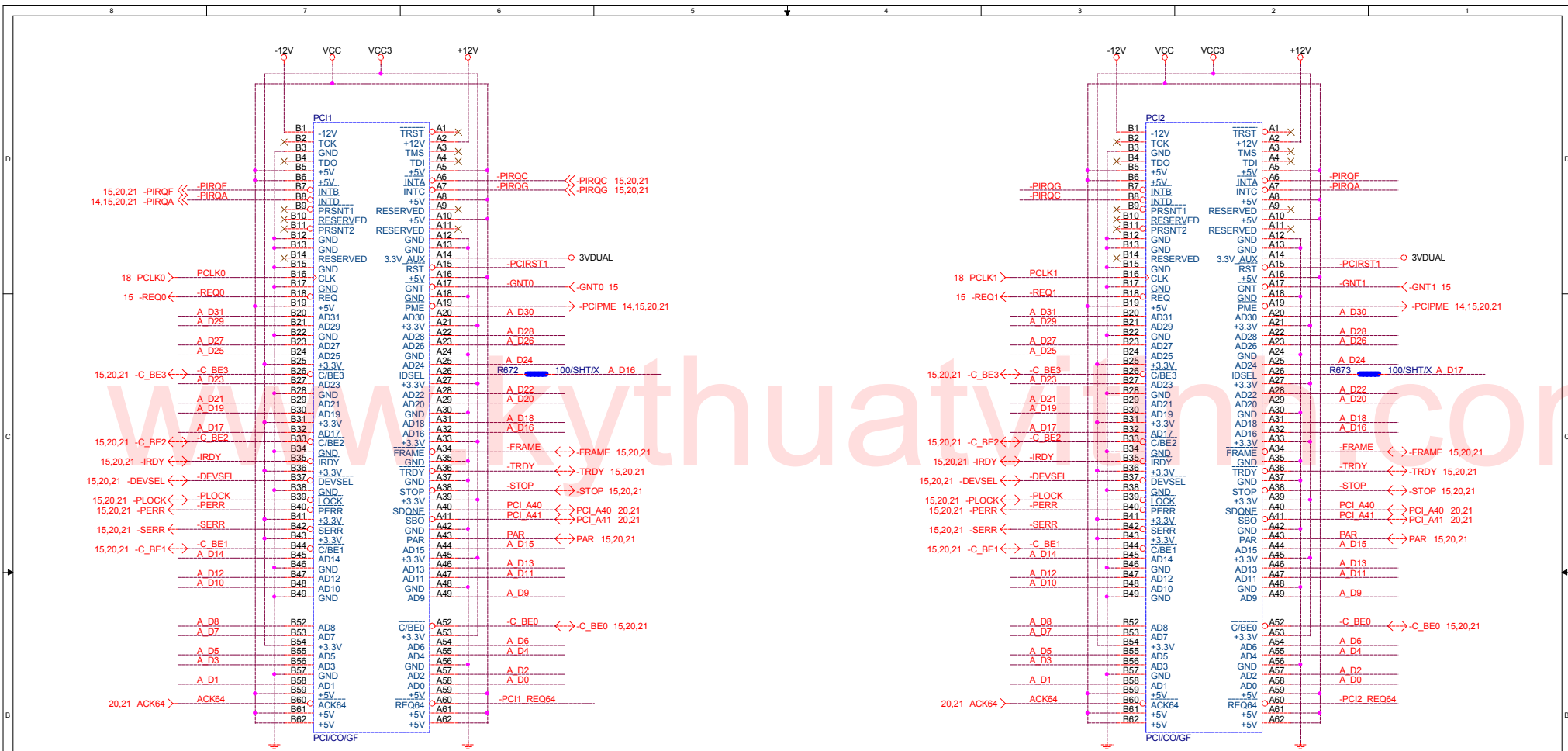
FS_E	FS_D	FS_C	FS_A	FS_B	Clock
1	1	0	0	0	100MHz
1	1	0	1	0	133MHz
1	1	0	1	1	166MHz
1	1	0	0	1	200MHz

**ICS952603**

FS_D	FS_3	FS_C	FS_A	FS_B	Clock
1	0	0	0	0	100MHz
1	0	0	1	0	133MHz
1	0	0	1	1	166MHz
1	0	0	0	1	200MHz

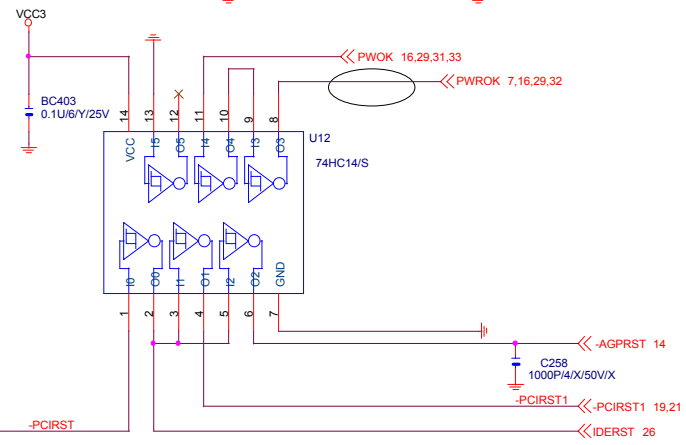
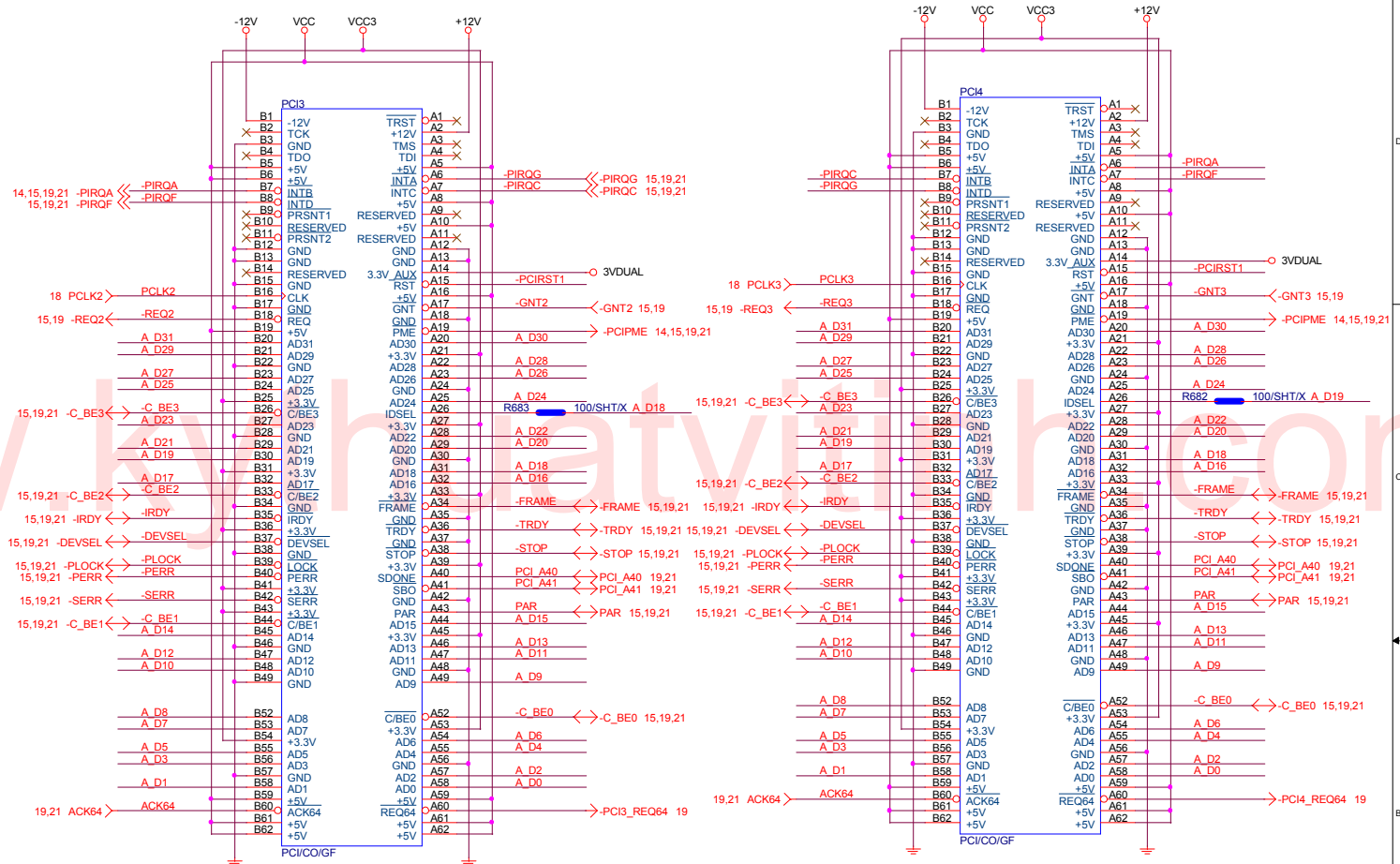


CY28405 上 R1031, R1034, R671  
不上 R1030, R1035  
ICS952616 上 R1030, R1035  
不上 R1031, R1034, R671



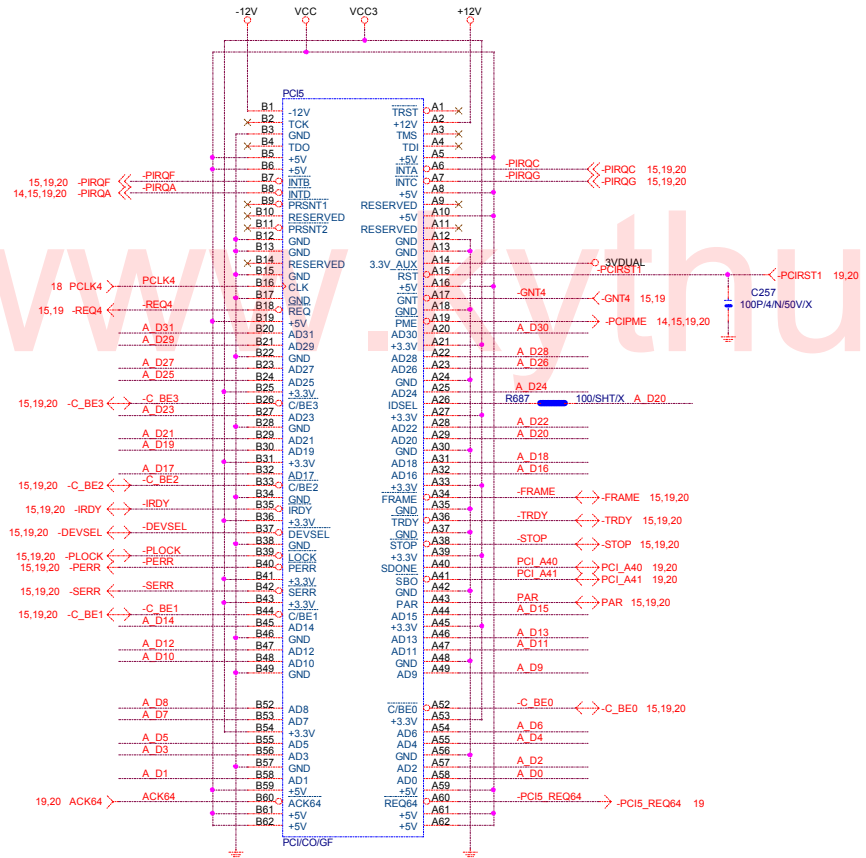
GIGABYTE CORP.		
Title		
<b>PCI SLOT 1/2</b>		
Size	Document Number	Rev
B	<b>GA-81848E-L</b>	<b>1.01</b>
Date:	星期三, 八月 06, 2003	Sheet 19 of 38

15,19,21 A\_D0..31 << A D0..31



GIGABYTE CORP.		
Title <b>PCI SLOT 3/4</b>		
Size B	Document Number <b>GA-81848E-L</b>	Rev <b>1.0</b>
Date: 2003.06.06	Sheet 20	of 38

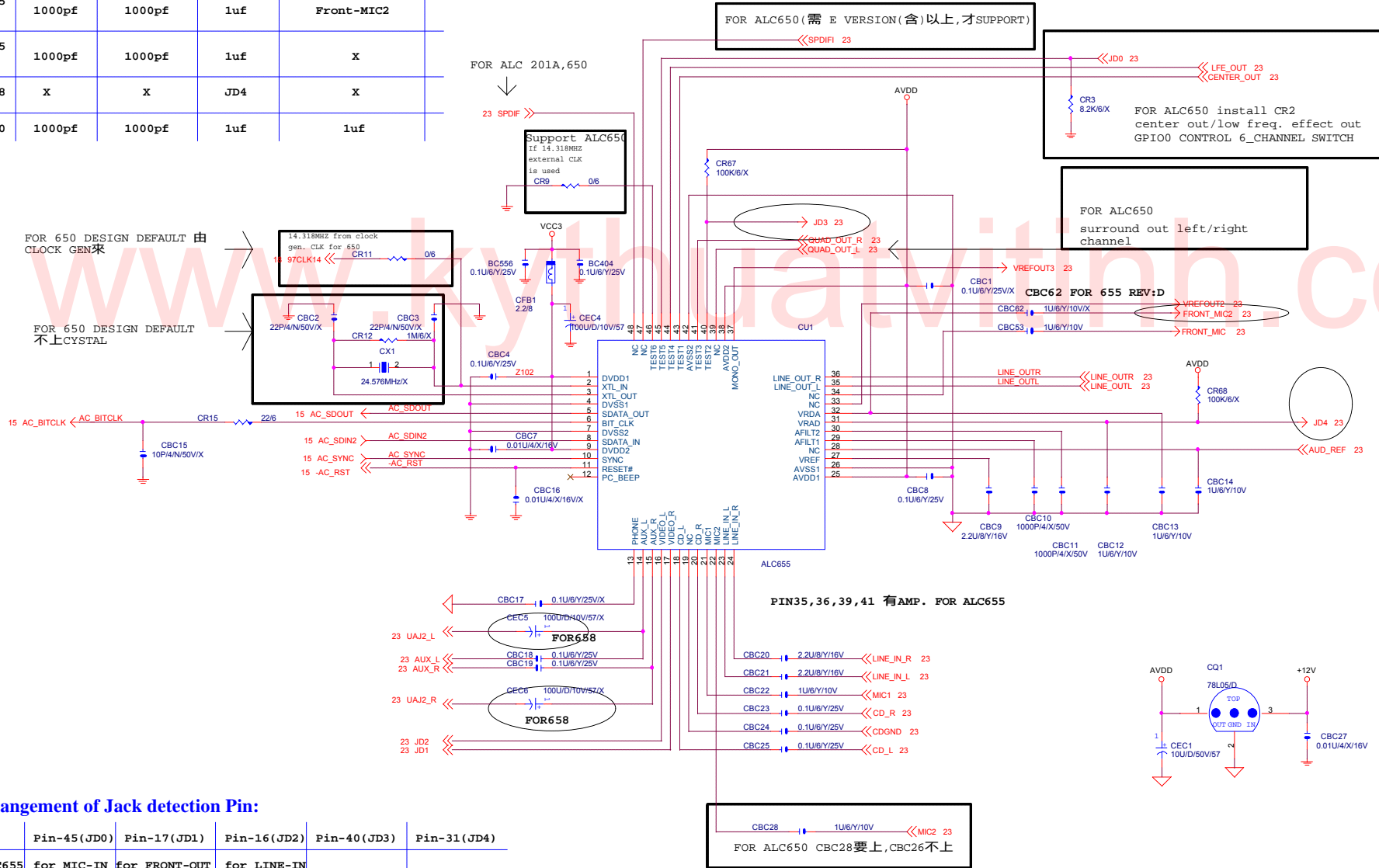
15,19,20 A\_D0..31] << A D0..31]



GIGABYTE CORP.			
Title			
PCI SLOT 5/6			
Size	Document Number	Rev	
Custom	GA-81848E-L	1.01	
Date:	星期二, 八月 06, 2003	Sheet	21 of 38

### Filter Cap design:

	Pin-29	Pin-30	Pin-31	Pin-32
ALC655 Rev D	1000pf	1000pf	1uf	Front-MIC2
ALC655 Rev C	1000pf	1000pf	1uf	X
ALC658	X	X	JD4	X
ALC650	1000pf	1000pf	1uf	1uf

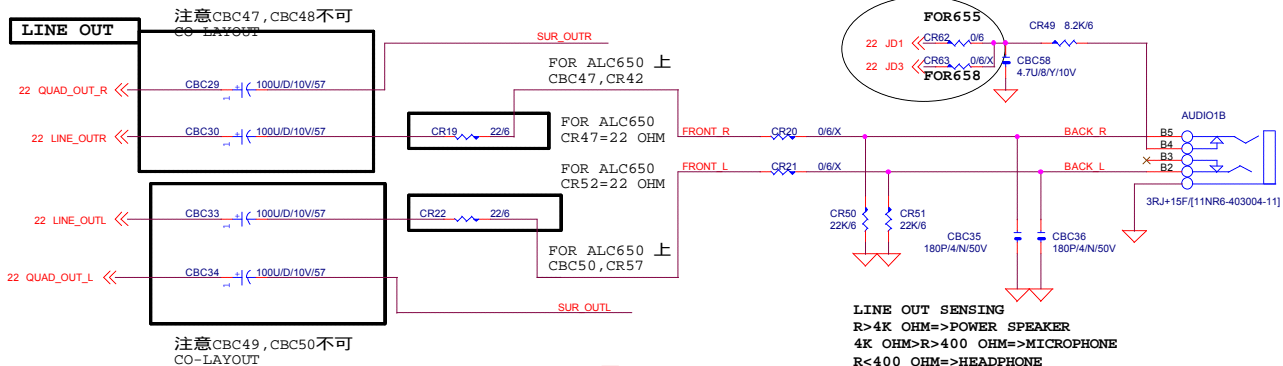


### Arrangement of Jack detection Pin:

	Pin-45(JD0)	Pin-17(JD1)	Pin-16(JD2)	Pin-40(JD3)	Pin-31(JD4)
ALC655	for MIC-IN	for FRONT-OUT	for LINE-IN		
ALC658	for MIC-IN	for UAJ1	for UAJ2	for FRONT-OUT	for LINE-IN External pull high is needed

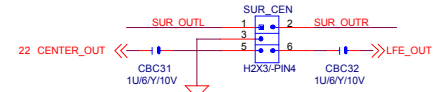
JDO,JD2,GPIO0 為偵測DEVICE INPUT 時由LOW TO HIGH Edge trigger(pop manual)

1/2(3.14)RC=1/2(3.14)8.2K\*4.7U=4.3HZ以上AC 信號全部衰減 TO 0V 不會造成JDO 誤動作(無device 時play wav)



FOR SUPPORT 6 CHANNEL, SURROUND OUT

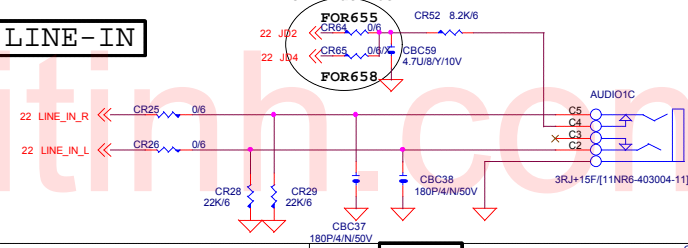
CENTER OUT, LOW FREQUENCY EFFECT OUT



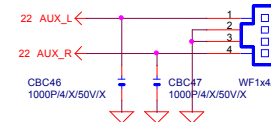
LINE IN SENSING(當OUTPUT)  
R>4K OHM=>POWER SPEAKER  
4K OHM>R>400 OHM=>MICROPHONE  
R<400 OHM=>HEADPHONE

LINE IN SENSING(當INPUT)  
swing of input signal>-40dbv(10mv)===>line in device active  
swing of input signal<-40dbv(10mv)===>unknown line in device

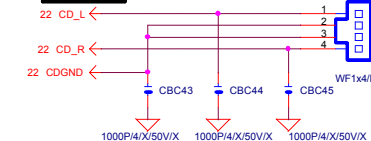
LINE-IN



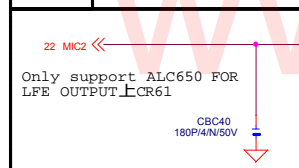
AUX IN DEFAULT NO POP



CD IN



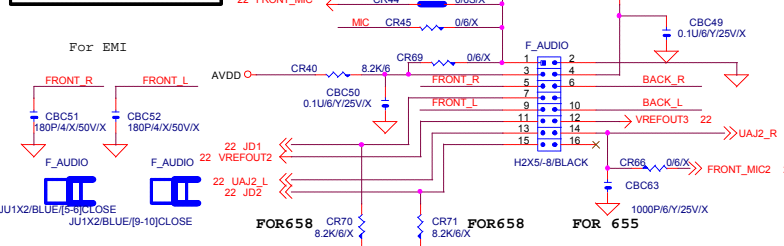
MIC



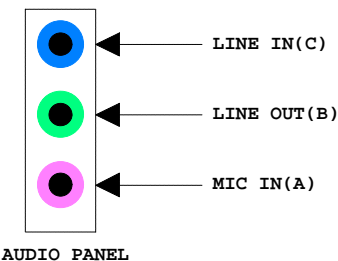
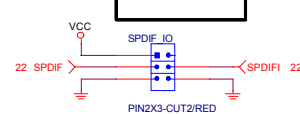
MICROPHONE IN SENSING(當INPUT)(利用vref 偏壓 與CR43,CR32 並聯求出阻抗)  
7.1k ohm>R>2.3k ohm===>microphone in  
R<2.3k ohm or R>7.1k ohm===>unknown device

MICROPHONE IN SENSING(當OUTPUT)  
R>4K OHM=>POWER SPEAKER  
4K OHM>R>400 OHM=>MICROPHONE  
R<400 OHM=>HEADPHONE

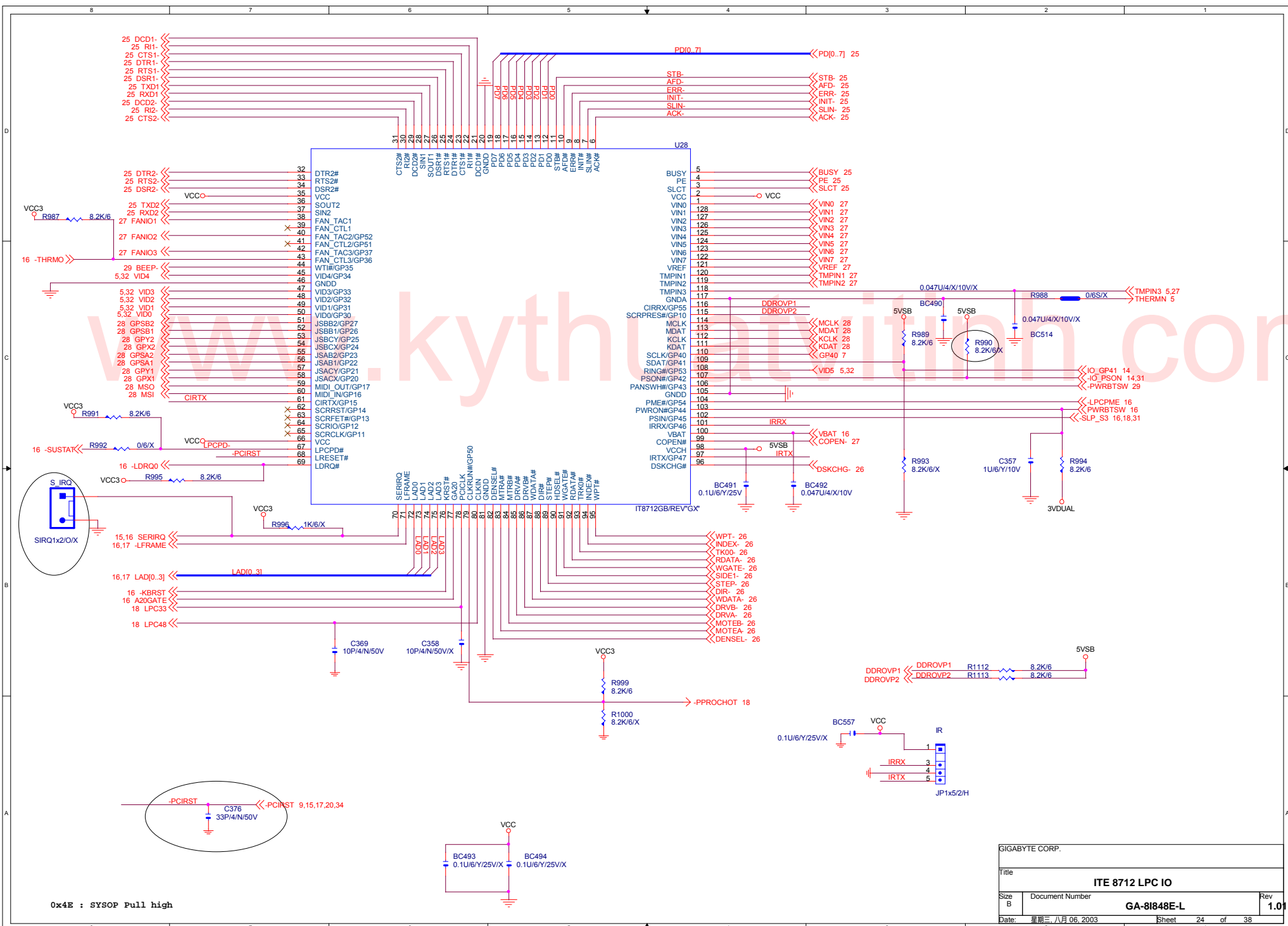
INTEL FRONT AUDIO



SPDIF\_IO

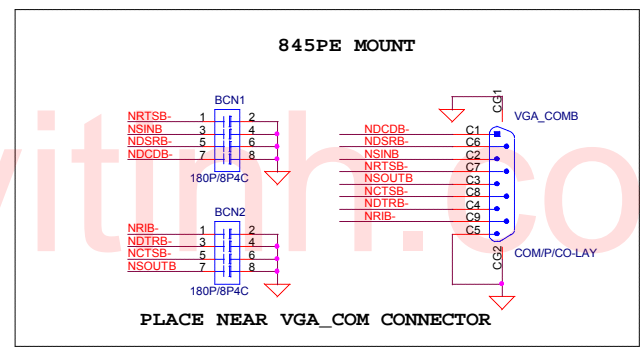
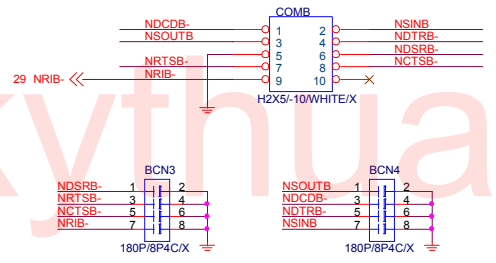
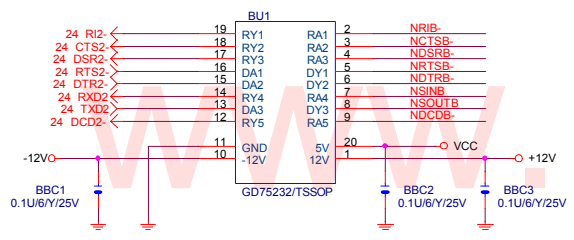
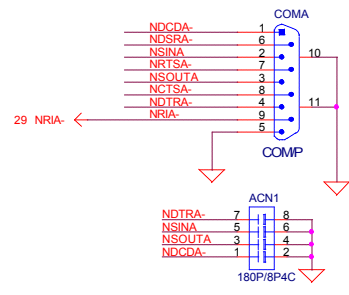
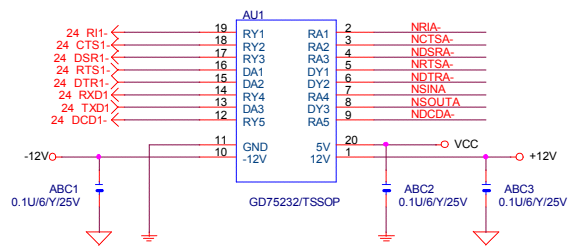


<b>GIGABYTE CORP.</b>			
<b>AUDIO OUTPUT, GAME PORT</b>			
Title	Document Number	Rev	
Size	GA-81848E-L	1.01	
Custom			
Date	星期二, 八月 06, 2003	Sheet	23 of 38

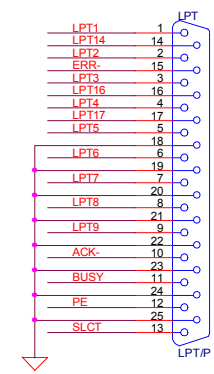
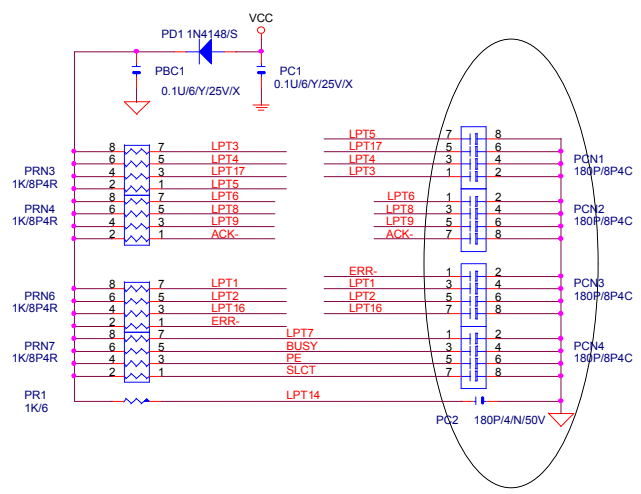
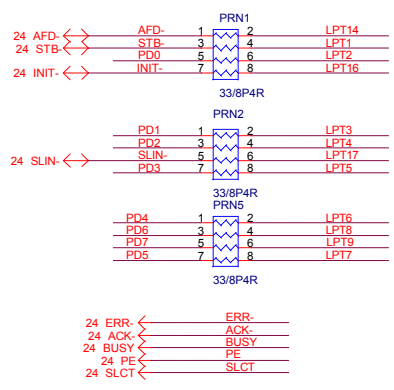


GIGABYTE CORP.		
Title		
<b>ITE 8712 LPC IO</b>		
Size	Document Number	Rev
B	<b>GA-8I848E-L</b>	<b>1.01</b>
Date:	星期三, 八月 06, 2003	Sheet 24 of 38



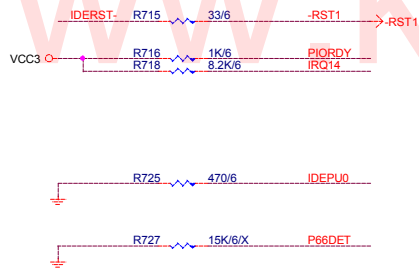
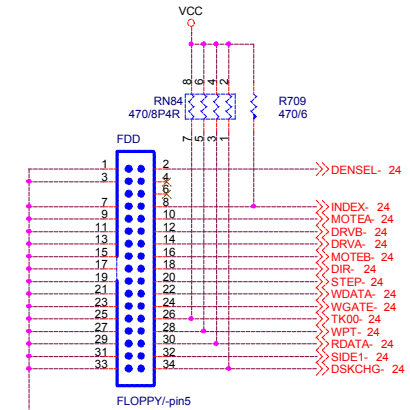
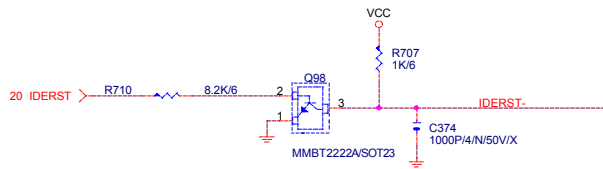


24 PD[0..7] ↔ PD[0..7]

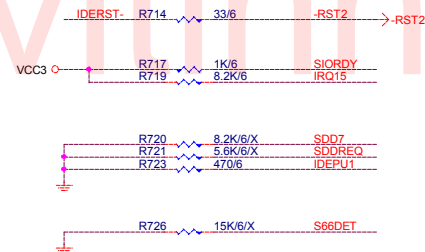


GIGABYTE CORP.

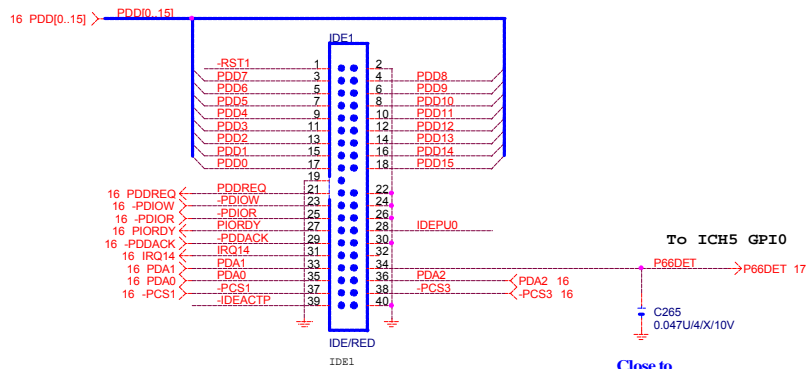
Title		
<b>COM &amp; IR &amp; LPT PORT &amp; FLOOPY</b>		
Size	Document Number	Rev
B	<b>GA-81848E-L</b>	<b>1.01</b>
Date:	星期三, 八月 06, 2003	Sheet 25 of 38



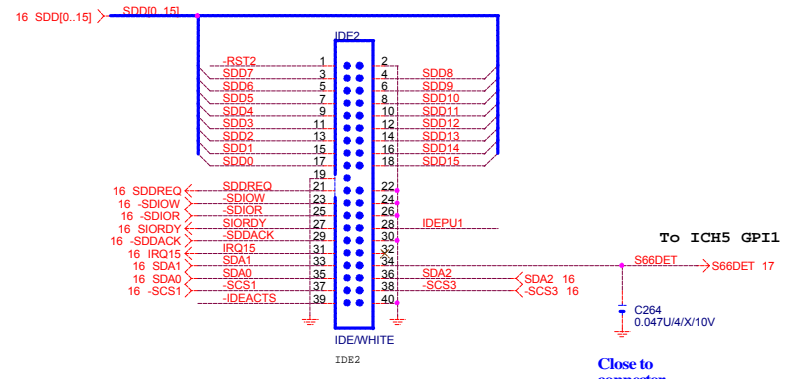
PRIMARY IDE CONNECTOR



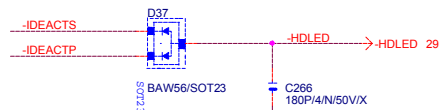
SECONDARY IDE CONNECTOR



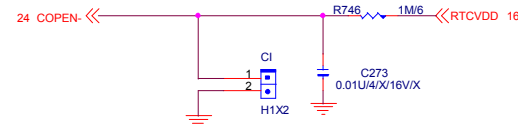
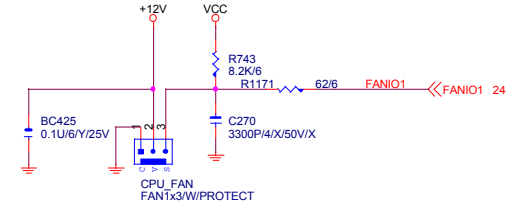
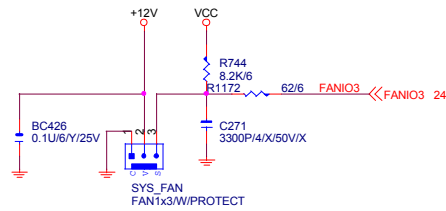
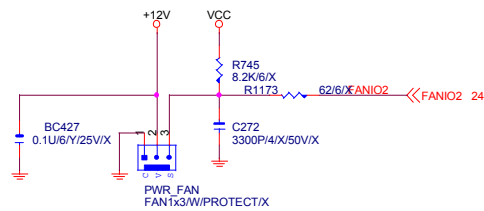
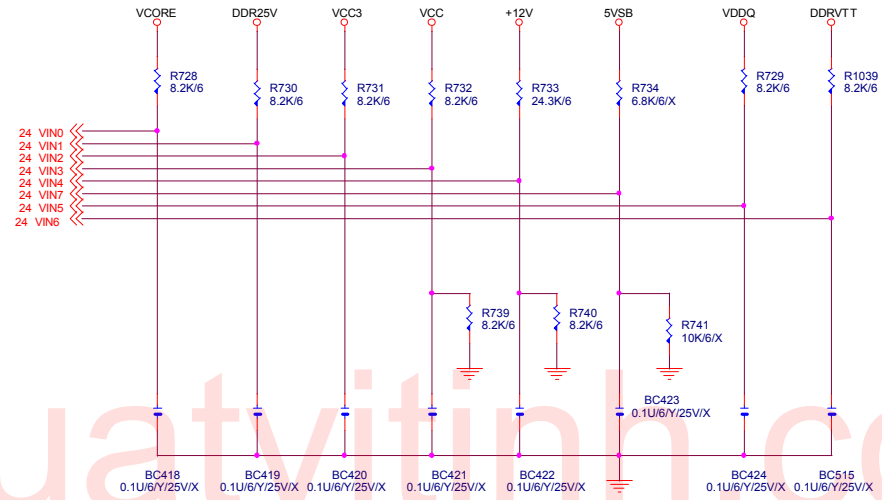
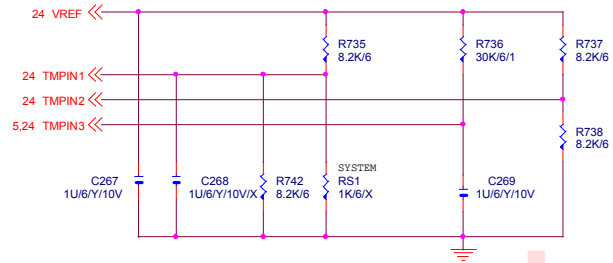
Close to connector



Close to connector

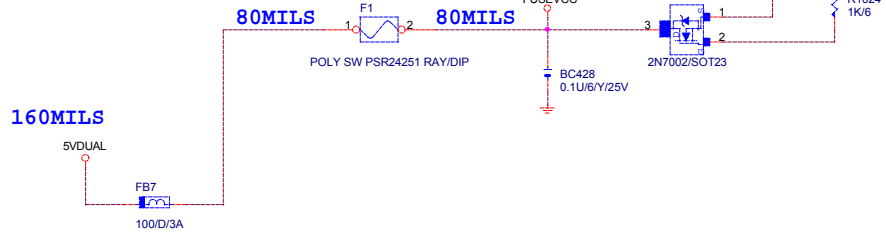
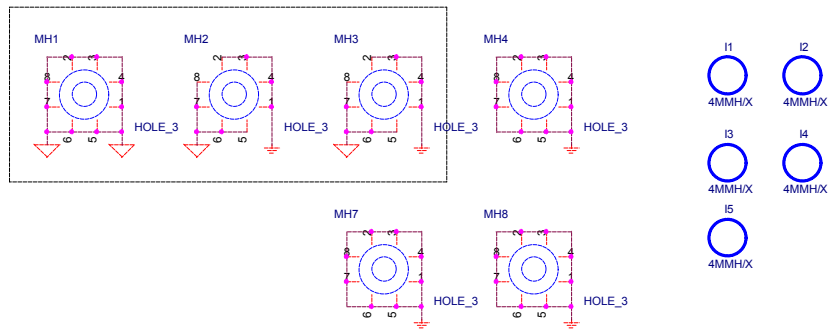


# Hardware Monitor circuits

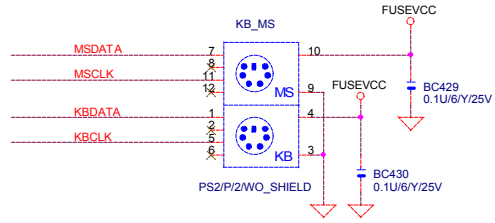
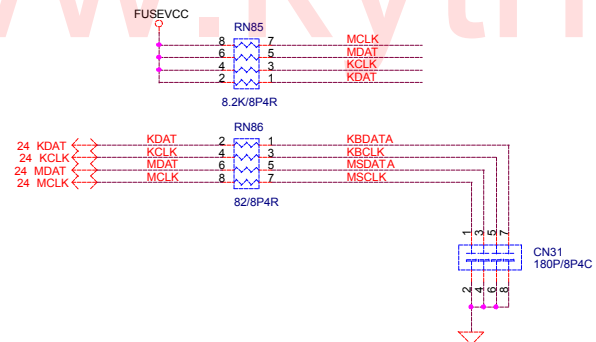


GIGABYTE CORP.		
Title		
<b>FAN/HWMO</b>		
Size	Document Number	Rev
B	<b>GA-8I848E-L</b>	<b>1.01</b>
Date:	星期三, 八月 06, 2003	Sheet 27 of 38

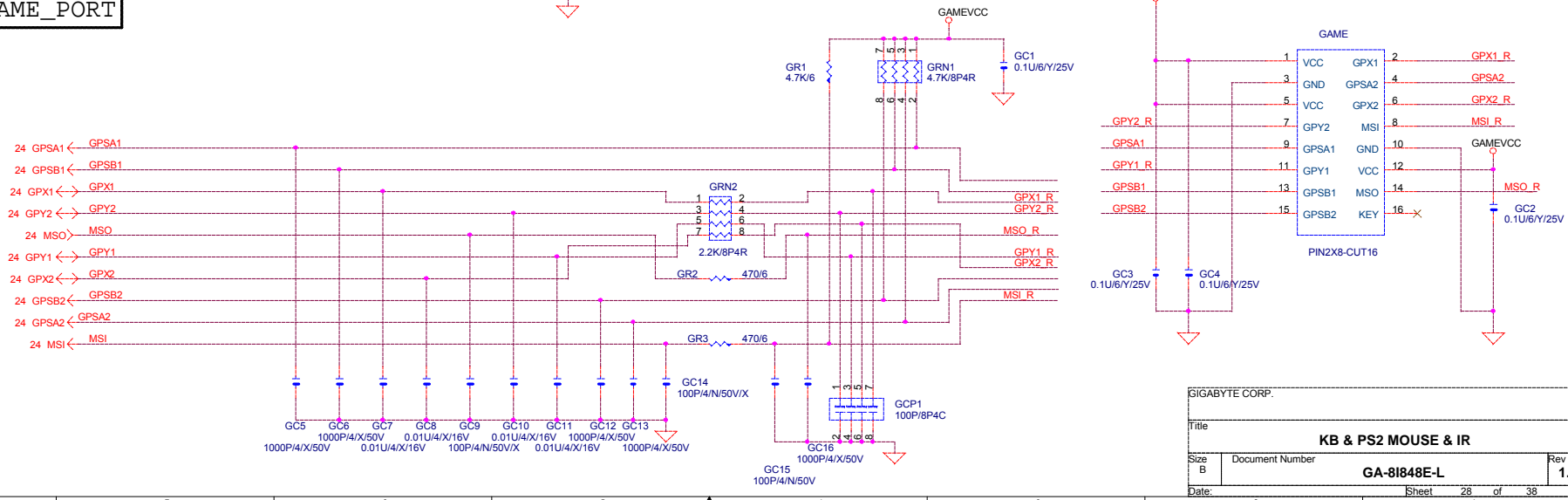
ATX AGND 與 GND 切割必須有三個



www.kvthuatvith.com

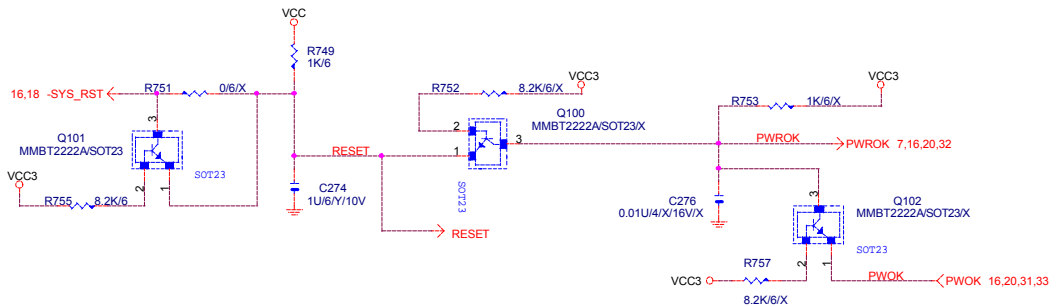
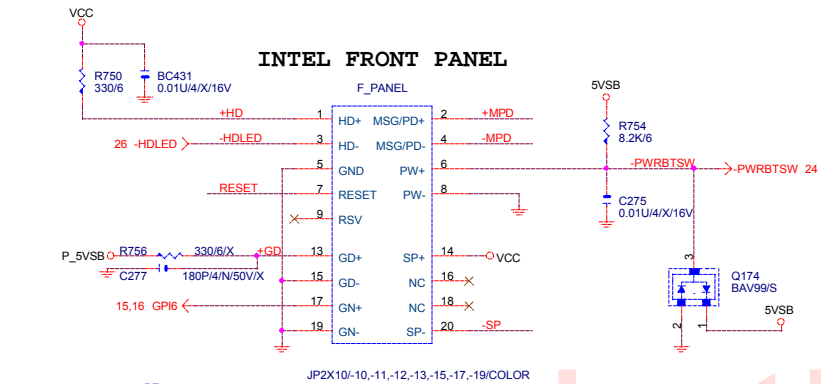


GAME\_PORT

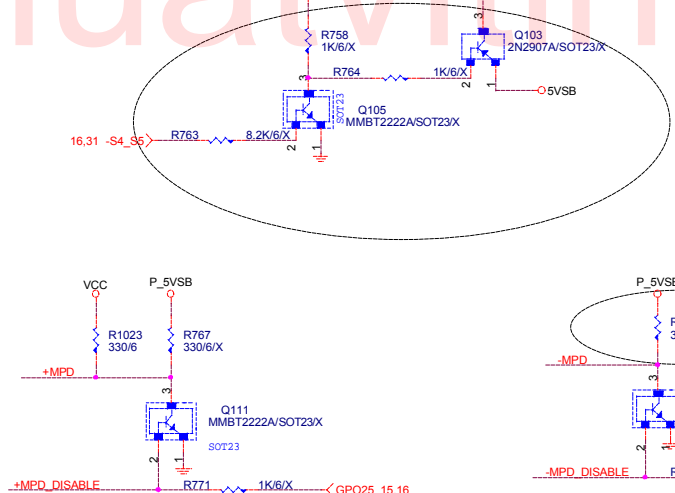
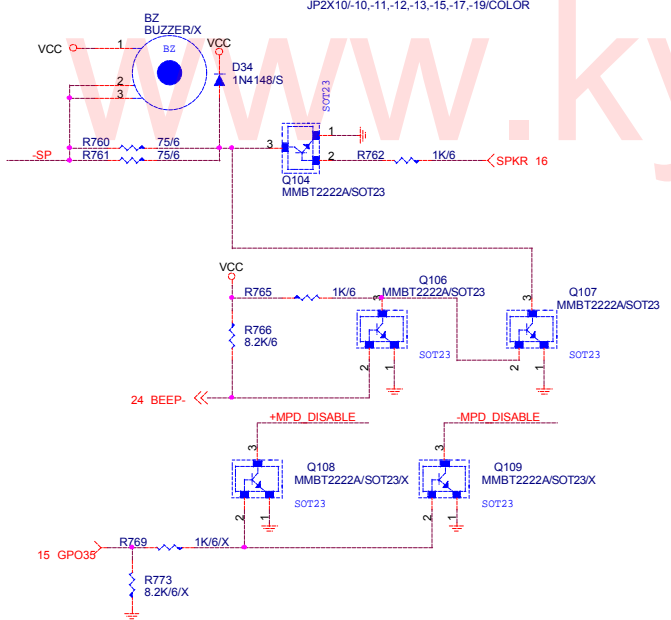
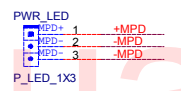


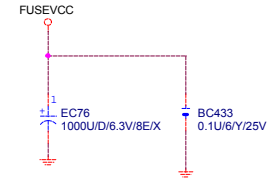
GIGABYTE CORP.		
Title		
<b>KB &amp; PS2 MOUSE &amp; IR</b>		
Size	Document Number	Rev
B	<b>GA-8I848E-L</b>	<b>1.01</b>
Date:	Sheet	of
	28	38

### INTEL FRONT PANEL

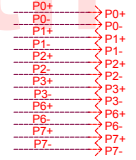
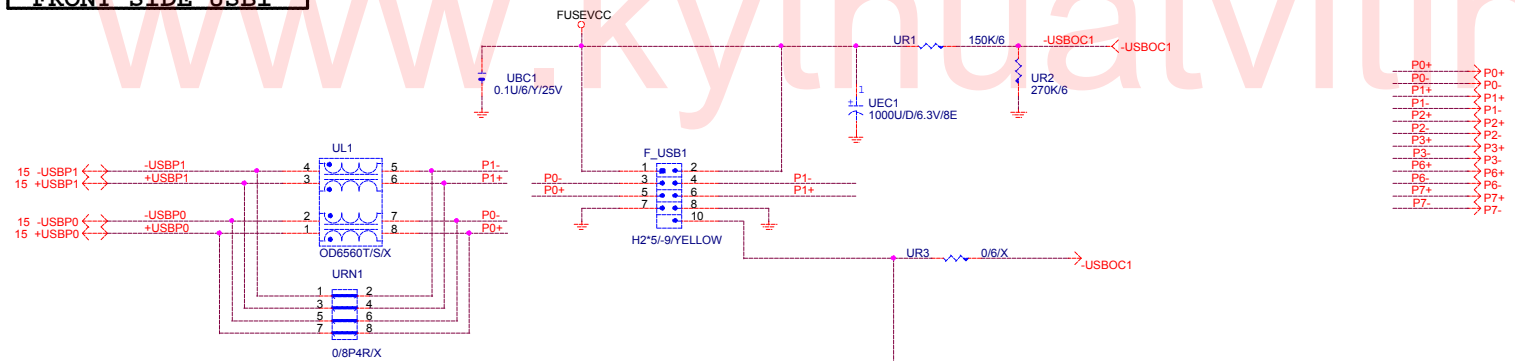


### 3 PIN POWER LED

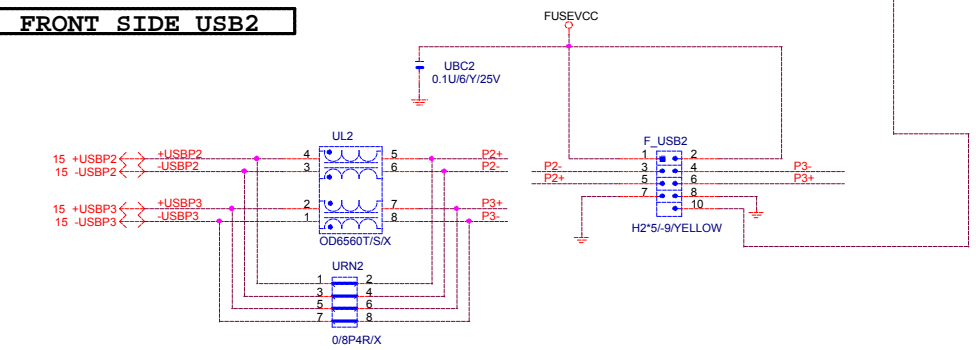




**FRONT SIDE USB1**

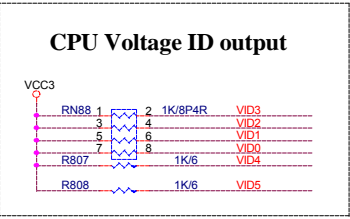
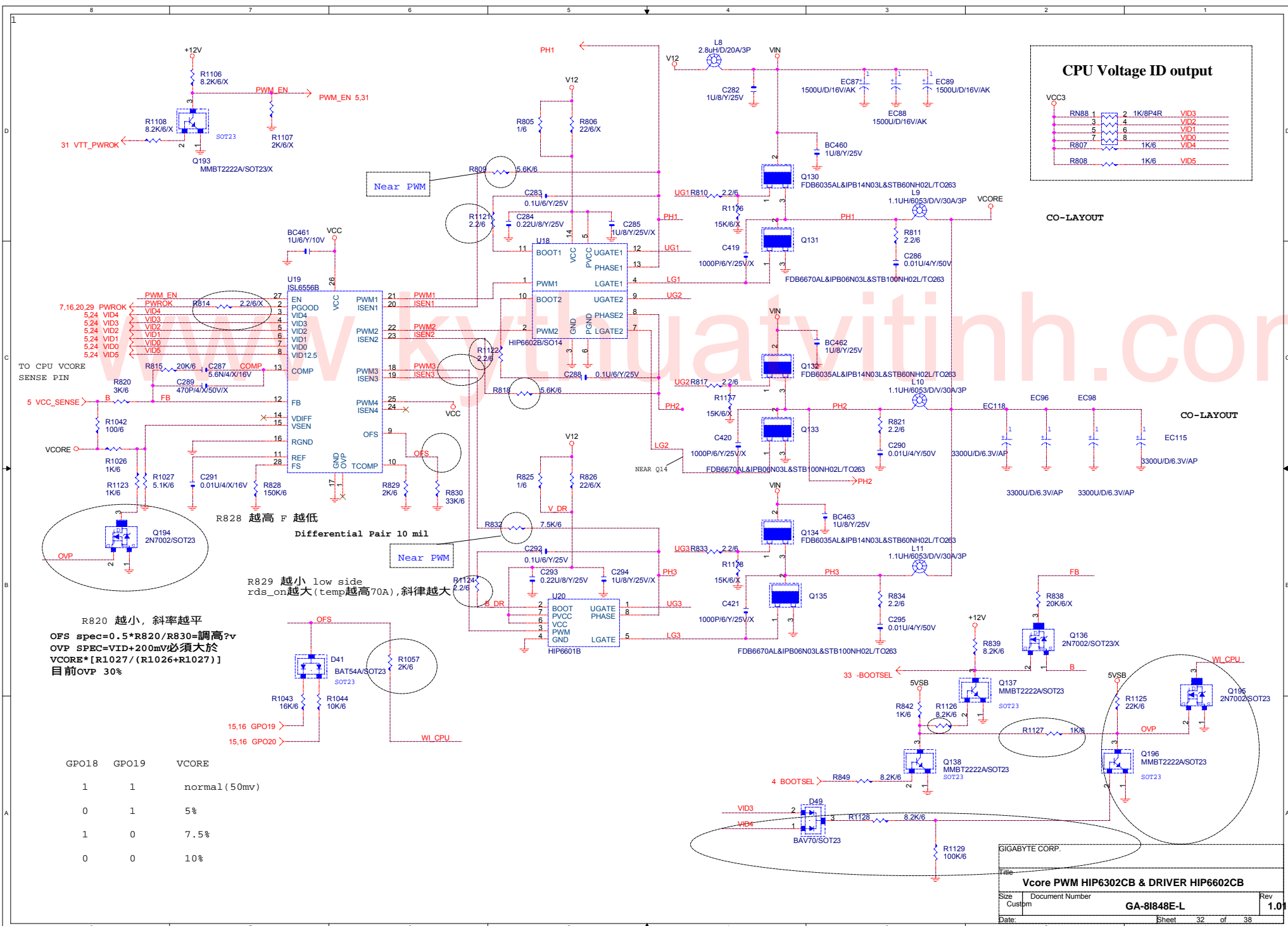


**FRONT SIDE USB2**



GIGABYTE CORP.		
Title		
<b>ICH USB PORT</b>		
Size B	Document Number	Rev
	<b>GA-81848E-L</b>	<b>1.01</b>
Date:	Sheet 30 of 38	





CO-LAYOUT

CO-LAYOUT

R828 越高 F 越低

Differential Pair 10 mil

R829 越小 low side rds\_on 越大 (temp 越高 70A), 斜率越大

R820 越小, 斜率越平

OFS spec =  $0.5 * R820 / R830 = \text{調高?}$   
 OVP SPEC =  $\text{VID} + 200\text{mV}$  必須大於  $\text{VCCORE} * [R1027 / (R1026 + R1027)]$   
 目前 OVP 30%

GPO18	GPO19	VCCORE
1	1	normal (50mv)
0	1	5%
1	0	7.5%
0	0	10%

GIGABYTE CORP.

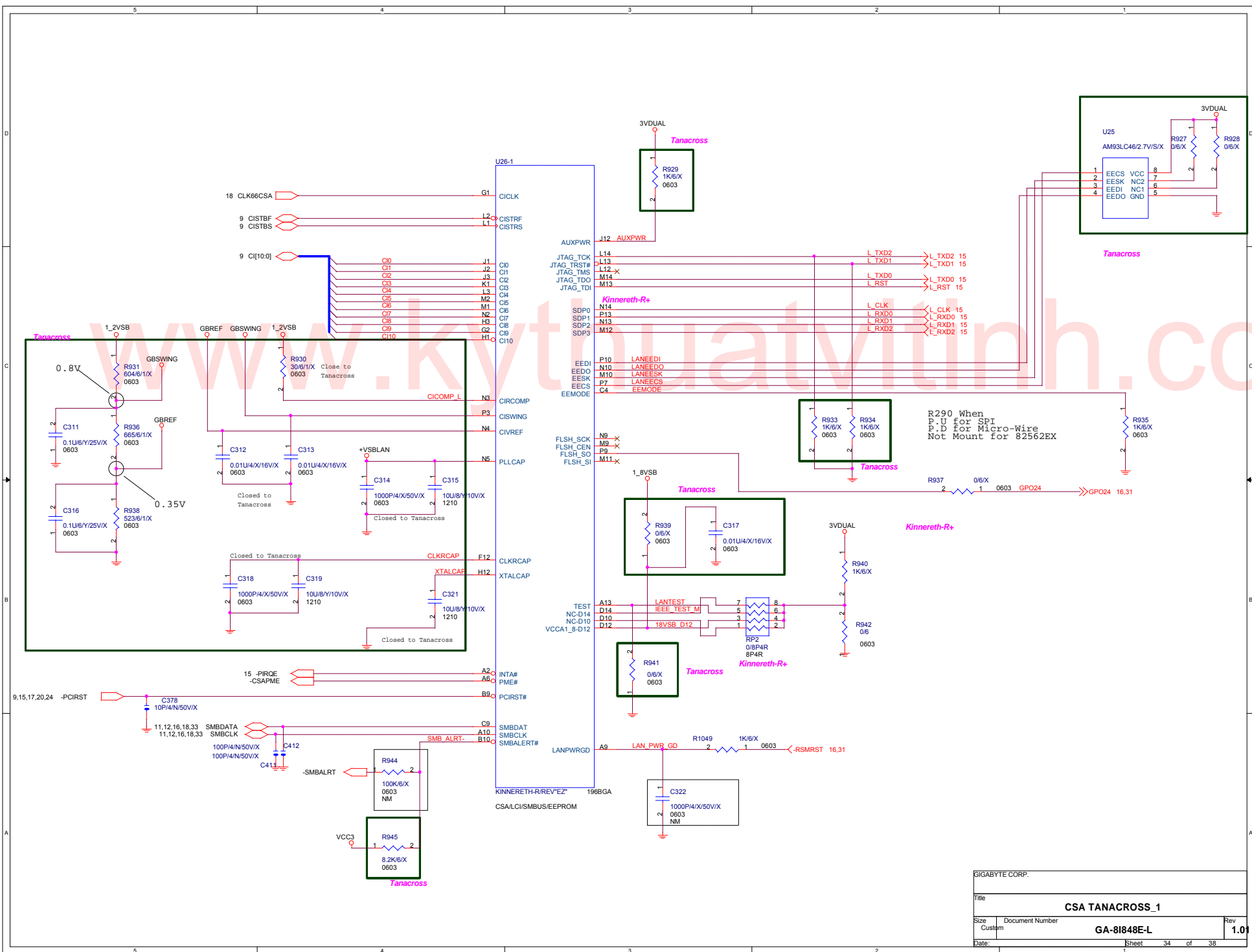
Title: **Vcore PWM HIP6302CB & DRIVER HIP6602CB**

Size	Document Number	Rev
Custom	<b>GA-8I848E-L</b>	<b>1.01</b>

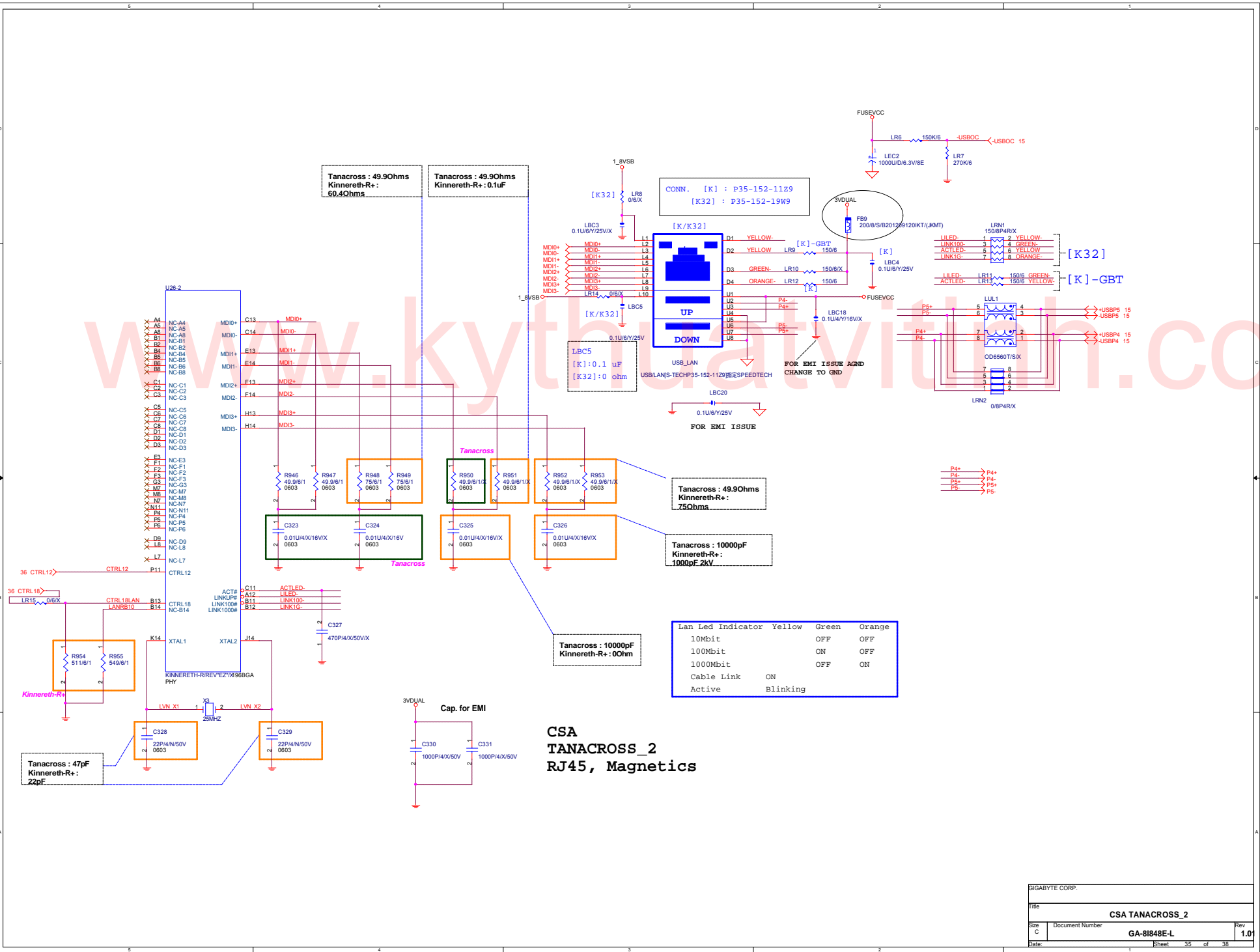
Date: \_\_\_\_\_ Sheet 32 of 38

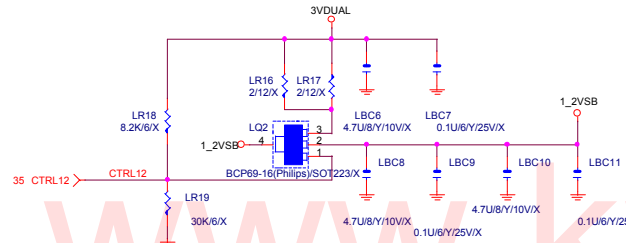




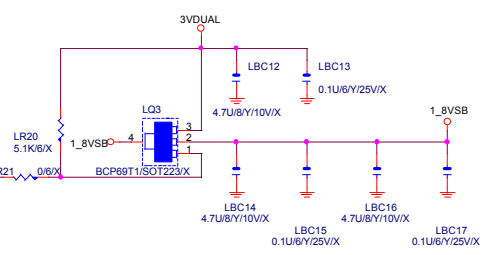


SIGABYTE CORP.			
Title			
<b>CSA TANACROSS_1</b>			
Size	Document Number	Rev	
Custom	<b>GA-81848E-L</b>	<b>1.01</b>	
Date:	Sheet	34	of 38

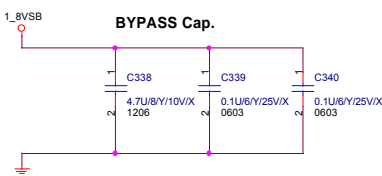
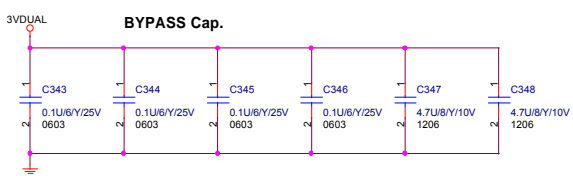
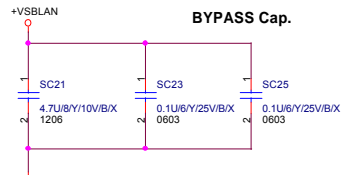
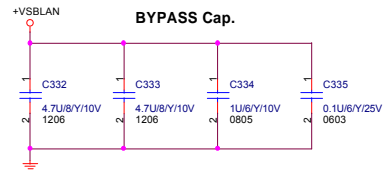
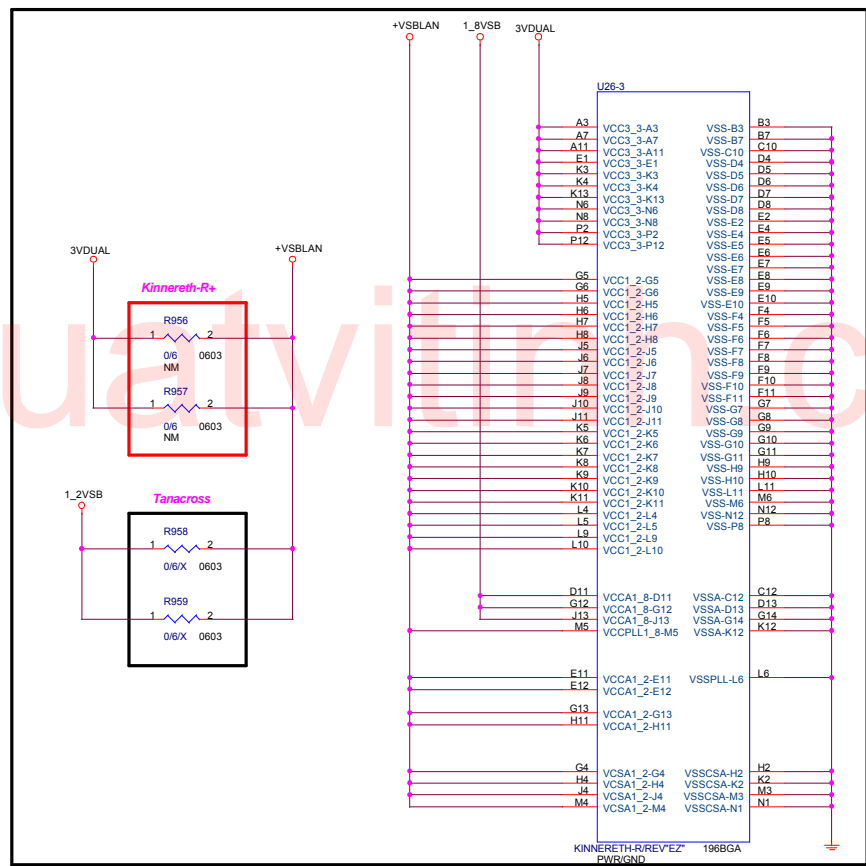




**+1.2VSB**  
**Max800mA**  
**Typ500mA**



**+1.8VSB**  
**Max500mA**  
**Typ250mA**



SIGABYTE CORP.			
Title			
<b>CSA TANACROSS_3</b>			
Size	Document Number		Rev
Custom	<b>GA-81848E-L</b>		<b>1.01</b>
Date:		Sheet	36 of 38

# GIGABYTE GA-8I848E-L PCI ROUNTING LIST

PCI DEVICE	IDSEL	INT	CLOCK	REQ	GNT
PCI SLOT1	16	C,F,G,A	PCLK0	REQ0-	GNT0-
PCI SLOT2	17	F,G,A,C	PCLK1	REQ1-	GNT1-
PCI SLOT3	18	G,A,C,F	PCLK2	REQ2-	GNT2-
PCI SLOT4	19	A,C,F,G	PCLK3	REQ3-	GNT3-
PCI SLOT5	20	C,F,G,A	PCLK4	REQ4-	GNT4-
VIA 1394	21	F	PCICLK1394	REQ5-	GNT5-

**GIGABYTE CORP.**

Title			PCI ROUNT LIST
Size	Document Number	GA-8I848E-L	Rev 1.01
Custom	Date: 星期三, 八月 06, 2003	Sheet 37 of 38	

# GIGABYTE GA-8I848E-L GPIO LIST

SHEET

TITLE

SHEET

TITLE

GPIP	I/O	FUNCTION
GPI0/REQA-	I	PULL HIGH 8.2K to VCC3, SMB connector.
GPI1/REQ5-		PULL HIGH 8.2K to VCC, REQ5-.
GPI2/PIRQE-		PULL HIGH 8.2K to VCC3, PIRQE-.
GPI3/PIRQF-		PULL HIGH 8.2K to VCC3, PIRQF-.
GPI4/PIRQG-		PULL HIGH 8.2K to VCC, PIRQG-.
GPI5/PIRQH-	NA	PULL HIGH 8.2K to VCC
GPI6/AGPBUSY-	I	PULL 8.2K TO VCC3, PANEL GREEN_BUTTON
GPI7	I	DUAL BIOS FIRST BOOT SELECT.
GPI8	I	PULL 8.2K TO 3VDUAL, -CASPMO.
GPI9/OC4-	NA	USB OC4-.
GPI10/OC5-	NA	USB OC5-.
GPI11/-SMBALRT	NA	PULL 8.2K TO 3VDUAL, -SMBALERT.
GPI12	I	PULL 8.2K TO VCC3, M/B REVERSION ID.
GPI13	I	LPC PME.
GPI14/OC6-	NA	USB OC6-.
GPI15/OC7-	NA	USB OC7-.
GPO16/GNTA-	NA	GPO16.
GPO17/GNT5-		GNT5-.
GPO18/STP_PCI-	NA	GPO18.
GPO19/SLP_S1-	O	DUAL BIOS.
GPO20/SLP_CPU-	O	DUAL BIOS.
GPO21/C3_SATA-	O	BLOCK TOP TABLE.
GPO22/CPUPERF-	O	PULL 8.2K TO VCC3, PANEL S3 POWER LED.

GPIP	I/O	FUNCTION
GPO16		PULL 8.2K TO VCC3
GPO17		PULL 8.2K TO VCC3 (GNT5-)
GPO18		PULL 8.2K TO VCC3
GPO19		PULL 8.2K TO VCC3
GPO20		PULL 8.2K TO VCC3
GPO21		PULL 8.2K TO VCC3
GPO22		PULL 8.2K TO VCC3
GPO23		PULL 8.2K TO VCC3
GPO24		PULL 1K TO 3VDUAL (TOP BLOCK)
GPO25		PULL 4.7K TO 3VDUAL, LAN 100/10 DETECT.
GPO26		NOT IMPLEMENTED
GPO27		PULL 8.2K TO 3VDUAL, BIOS WRITE PROTECT.
GPO28		PULL 8.2K TO 3VDUAL