


GIGABYTE GA-8I848P-G Schematics

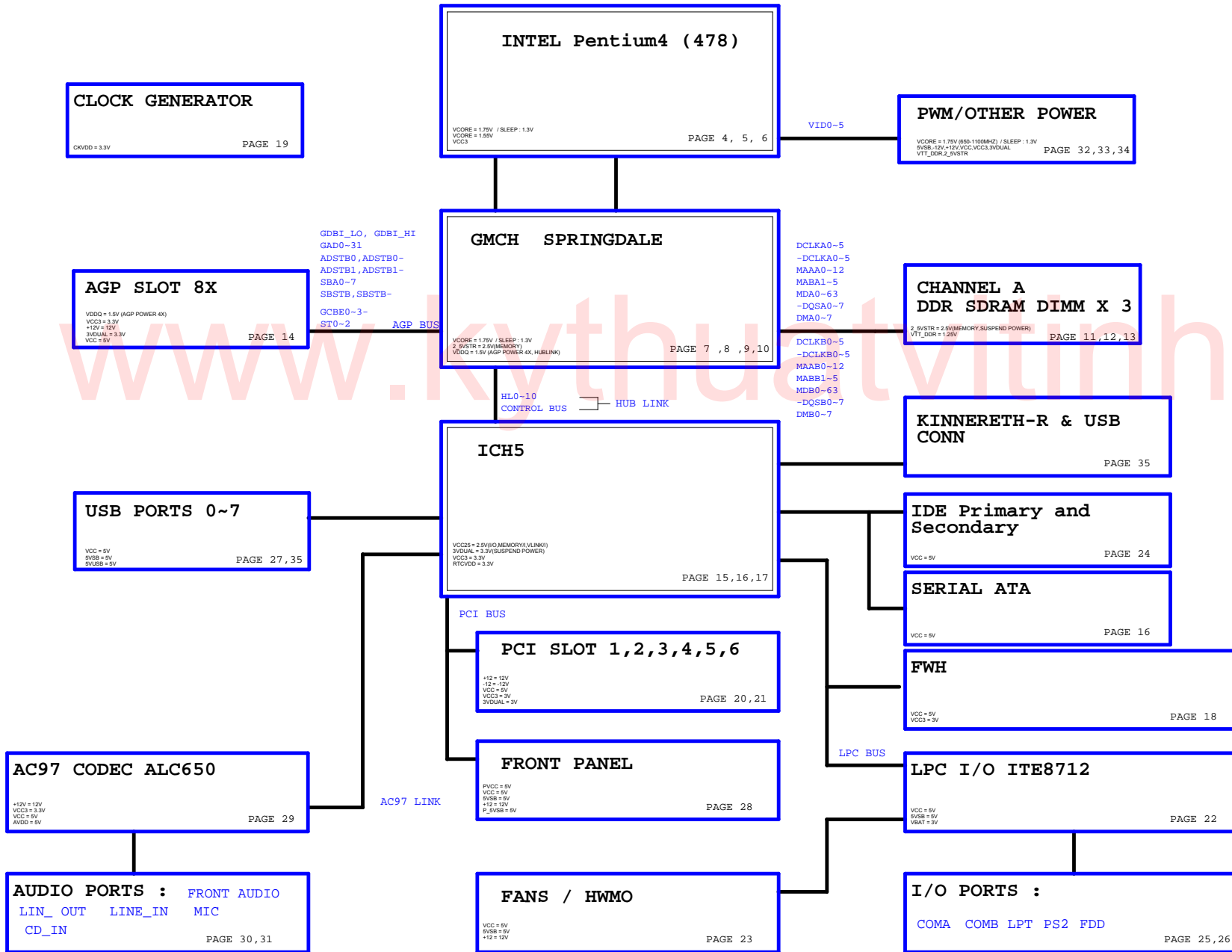
Revision 2.01

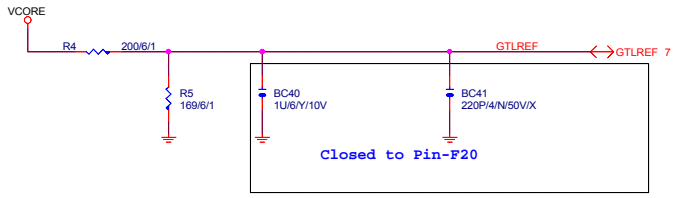
SHEET	TITLE
01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	P4_478A
05	P4_478B
06	P4_478C
07	SPRINGDALE HOST
08	SPRINGDALE DDR
09	SPRINGDALE AGP, HUB, CSA, VGA
10	SPRINGDALE PWR
11	DDR1,2 CHANNEL A
12	DDR3 CHANNEL A
13	DDR TERMINATION
14	AGP
15	ICH5 PCI, USB, HUB, LAN
16	ICH5 IDE, GPIO, SATA, CTRL
17	ICH5 VCC, GND
18	FWH
19	ICS952603 CLOCK GEN
20	PCI1_2
21	PCI3_4
22	PCI5_6

SHEET	TITLE
23	CODEC
24	AUDIO JACK, L_OUT, F_AUDIO
25	ITE 8712
26	COM_LPT
27	IDE
28	FAN/HWMO
29	KB_PS2
30	FPANEL
31	USB CONN
32	DDR POWER
33	VCORE POWER
34	ATX, OTHERS POWER
35	KINNERETH-R LNA(CSA-1)
36	KINNERETH-R LNA(CSA-2)
37	KINNERETH-R LNA(CSA-3)

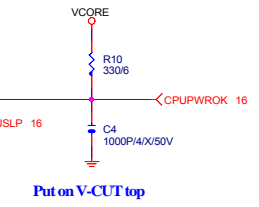
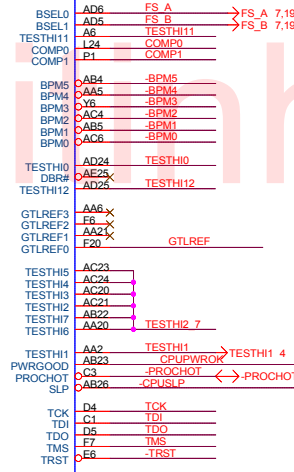
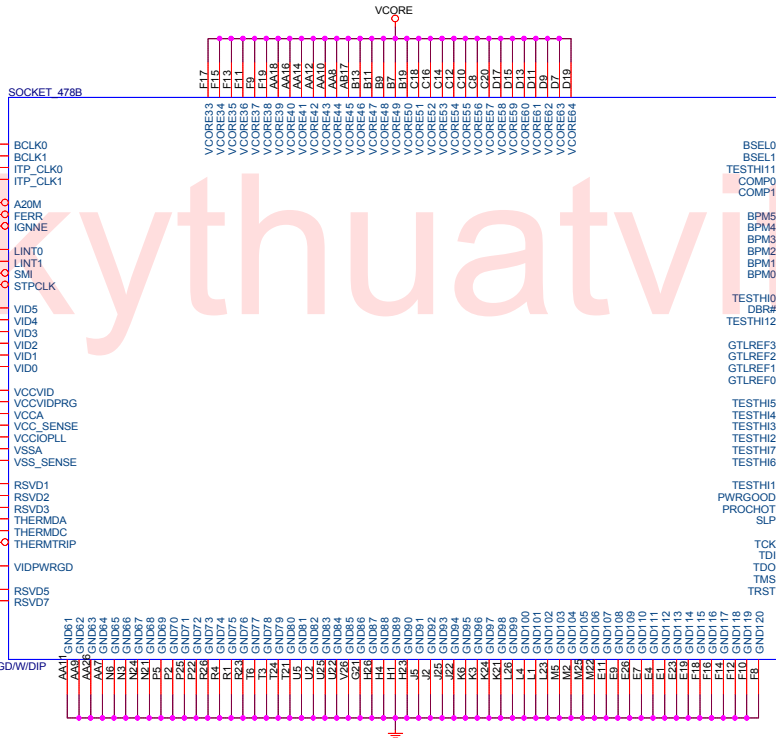
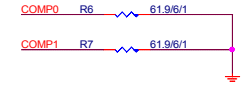
		
GIGABYTE CORP.		
Title COVER SHEET		
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BLOCK DIAGRAM

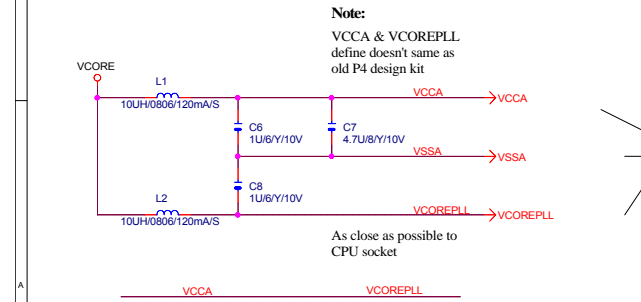
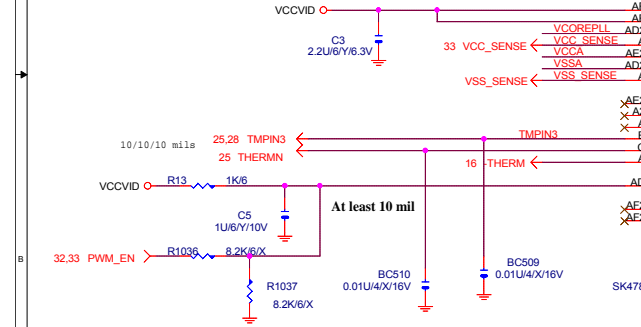




Place outside of CPU socket

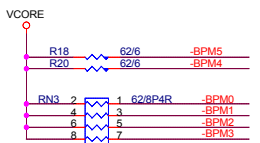
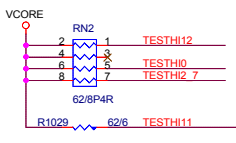


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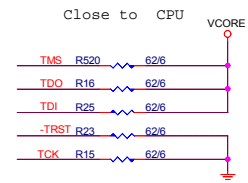


Note:
VCCA & VCCOREPLL
define doesn't same as
old P4 design kit

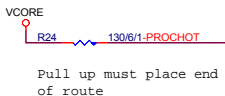
Trace width doesn't
less than 12 Mil



Close to CPU

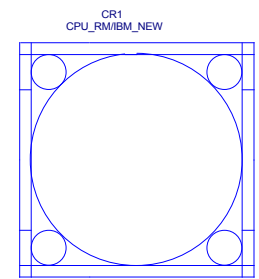
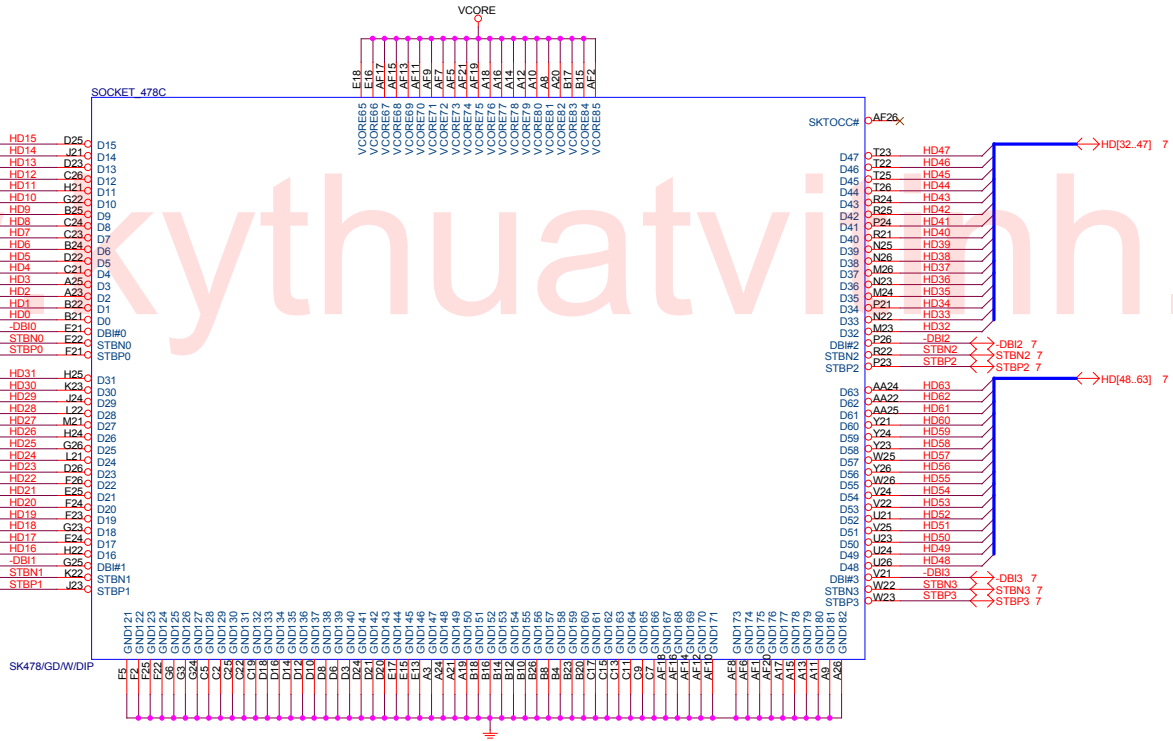
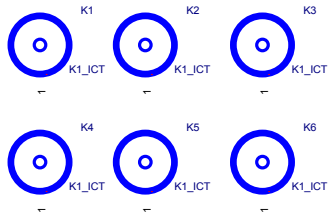


Close to CPU

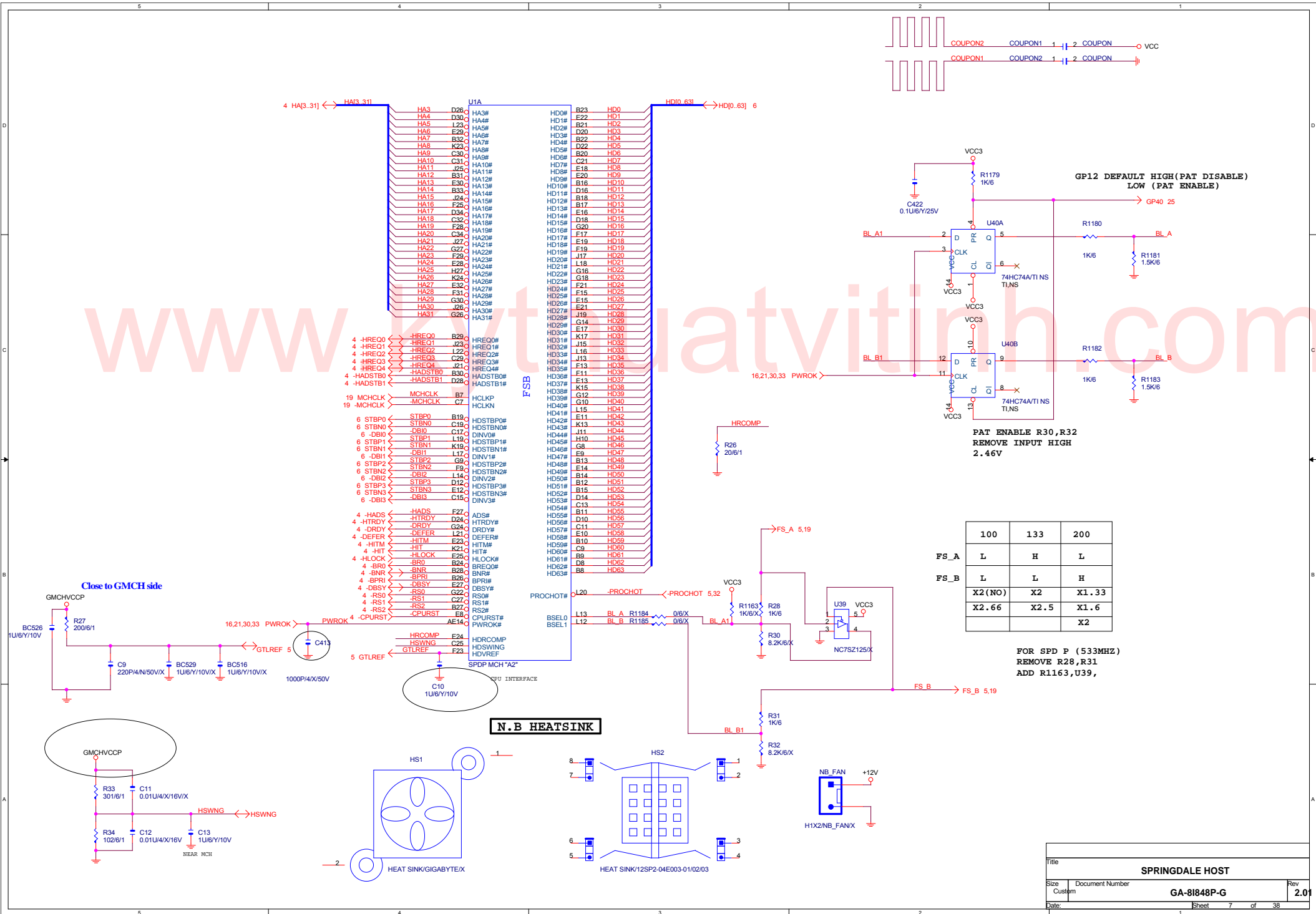


Pull up must place end
of route

Title		
P4 478B		
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Title			P4 478C		
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11.12.13 MAAA[0..12] <-> MAAA0_12I
 11.12.13 MABA[1..5] <-> MABA1_5I
 11.12.13 DMA[0..7] <-> DMA0_7I
 11.12.13 MDA[0..63] <-> MDA0_63I
 11.12.13 DQSA[0..7] <-> DQSA0_7I

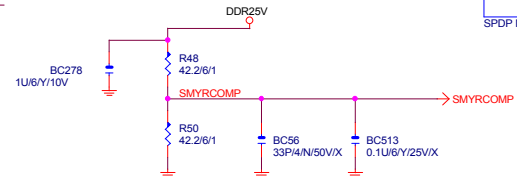
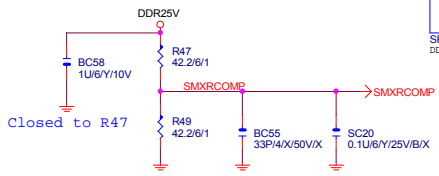
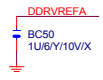
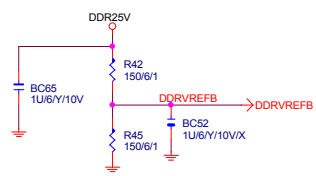
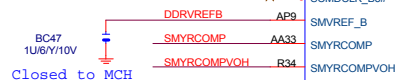
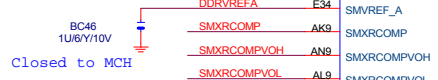
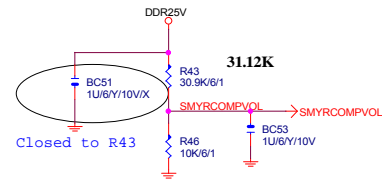
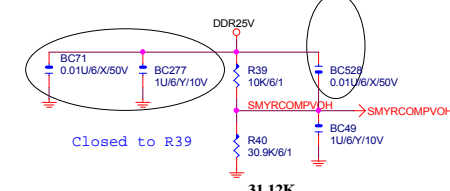
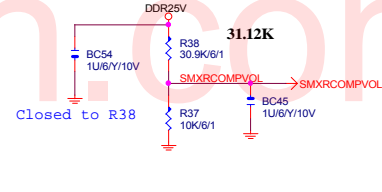
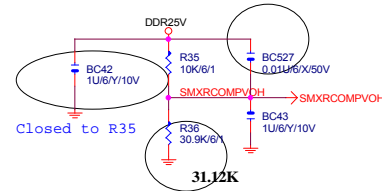
U1B
 MAAA0 AL34 SMAA_A0
 MAAA1 AL33 SMAA_A1
 MAAA2 AK29 SMAA_A2
 MAAA3 AN31 SMAA_A3
 MAAA4 AL30 SMAA_A4
 MAAA5 AL26 SMAA_A5
 MAAA6 AL28 SMAA_A6
 MAAA7 AN25 SMAA_A7
 MAAA8 AP26 SMAA_A8
 MAAA9 AP24 SMAA_A9
 MAAA10 AL33 SMAA_A10
 MAAA11 AN23 SMAA_A11
 MAAA12 AN21 SMAA_A12
 MABA1 AL34 SMAB_A1
 MABA2 AM34 SMAB_A2
 MABA3 AP32 SMAB_A3
 MABA4 AP31 SMAB_A4
 MABA5 AM26 SMAB_A5
 SWEA AB34 SWE_A#
 SCASA Y34 SCAS_A#
 SRASA AC33 SRA5_A#
 SBA0 AE33 SBA_A0
 SBA1 AH34 SBA_A1
 CSA0 CSA0 SCS_A0#
 CSA1 Y32 SCS_A1#
 CSA2 Y32 SCS_A2#
 CSA3 W34 SCS_A3#
 CKEA0 AL20 SCKE_A0
 CKEA1 AN19 SCKE_A1
 CKEA2 AM20 SCKE_A2
 CKEA3 AP20 SCKE_A3
 DCLKA0 AK32 SCMDCLK_A0
 DCLKA0# AK31 SCMDCLK_A0#
 DCLKA1 AP17 SCMDCLK_A1
 DCLKA1# AN17 SCMDCLK_A1#
 DCLKA2 N33 SCMDCLK_A2
 DCLKA2# N34 SCMDCLK_A2#
 DCLKA3 AK33 SCMDCLK_A3
 DCLKA3# AK34 SCMDCLK_A3#
 DCLKA4 AM16 SCMDCLK_A4
 DCLKA4# AL16 SCMDCLK_A4#
 DCLKA5 P31 SCMDCLK_A5
 DCLKA5# P32 SCMDCLK_A5#
 DDRVREFA E34 SMVREF_A
 SMXRCOMP AK9 SMXRCOMP
 SMXRCOMPVOH AN9 SMXRCOMPVOH
 SMXRCOMPVOL AL9 SMXRCOMPVOL

SDQS_A0 AN11 DQSA0
 SDQ_A0 AP12 MDA0
 SDQ_A1 AP11 MDA1
 SDQ_A2 AN12 MDA2
 SDQ_A3 AN13 MDA3
 SDQ_A4 AM10 MDA4
 SDQ_A5 AL10 MDA5
 SDQ_A6 AL12 MDA6
 SDQ_A7 AP13 MDA7
 SDQS_A1 AP15 DQSA1
 SDM_A1 AP16 MDA1
 SDQ_A8 AP14 MDA8
 SDQ_A9 AM14 MDA9
 SDQ_A10 AL18 MDA10
 SDQ_A11 AL14 MDA11
 SDQ_A12 AL14 MDA12
 SDQ_A13 AN15 MDA13
 SDQ_A14 AP18 MDA14
 SDQ_A15 AM18 MDA15
 SDQS_A2 AP23 DQSA2
 SDM_A2 AM24 MDA2
 SDQ_A16 AP22 MDA16
 SDQ_A17 AM22 MDA17
 SDQ_A18 AL24 MDA18
 SDQ_A19 AN27 MDA19
 SDQ_A20 AP21 MDA20
 SDQ_A21 AL22 MDA21
 SDQ_A22 AP25 MDA22
 SDQ_A23 AP27 MDA23
 SDQS_A3 AM30 DQSA3
 SDM_A3 AP30 MDA3
 SDQ_A24 AP28 MDA24
 SDQ_A25 AP29 MDA25
 SDQ_A26 AP33 MDA26
 SDQ_A27 AM33 MDA27
 SDQ_A28 AM28 MDA28
 SDQ_A29 AN29 MDA29
 SDQ_A30 AM31 MDA30
 SDQ_A31 AN34 MDA31
 SDQS_A4 AF34 DQSA4
 SDM_A4 AF31 MDA4
 SDQ_A32 AH32 MDA32
 SDQ_A33 AC34 MDA33
 SDQ_A34 AF32 MDA34
 SDQ_A35 AD32 MDA35
 SDQ_A36 AH31 MDA36
 SDQ_A37 AC33 MDA37
 SDQ_A38 AE34 MDA38
 SDQ_A39 AD34 MDA39
 SDQS_A5 V34 DQSA5
 SDM_A5 W33 DMA5
 SDQ_A40 AC34 MDA40
 SDQ_A41 AB31 MDA41
 SDQ_A42 V32 MDA42
 SDQ_A43 V31 MDA43
 SDQ_A44 AD31 MDA44
 SDQ_A45 AB32 MDA45
 SDQ_A46 U34 MDA46
 SDQ_A47 U33 MDA47
 SDQS_A6 M32 DQSA6
 SDM_A6 M34 DMA6
 SDQ_A48 T34 MDA48
 SDQ_A49 T32 MDA49
 SDQ_A50 K34 MDA50
 SDQ_A51 K32 MDA51
 SDQ_A52 T31 MDA52
 SDQ_A53 P34 MDA53
 SDQ_A54 L34 MDA54
 SDQ_A55 L33 MDA55
 SDQS_A7 H31 DQSA7
 SDM_A7 H32 DMA7
 SDQ_A56 J33 MDA56
 SDQ_A57 H34 MDA57
 SDQ_A58 E33 MDA58
 SDQ_A59 F33 MDA59
 SDQ_A59 K31 MDA60
 SDQ_A60 J34 MDA61
 SDQ_A61 G34 MDA62
 SDQ_A62 F34 MDA63

SDQS_A0 AN11 DQSA0
 SDQ_A0 AP12 MDA0
 SDQ_A1 AP11 MDA1
 SDQ_A2 AN12 MDA2
 SDQ_A3 AN13 MDA3
 SDQ_A4 AM10 MDA4
 SDQ_A5 AL10 MDA5
 SDQ_A6 AL12 MDA6
 SDQ_A7 AP13 MDA7
 SDQS_A1 AP15 DQSA1
 SDM_A1 AP16 MDA1
 SDQ_A8 AP14 MDA8
 SDQ_A9 AM14 MDA9
 SDQ_A10 AL18 MDA10
 SDQ_A11 AL14 MDA11
 SDQ_A12 AL14 MDA12
 SDQ_A13 AN15 MDA13
 SDQ_A14 AP18 MDA14
 SDQ_A15 AM18 MDA15
 SDQS_A2 AP23 DQSA2
 SDM_A2 AM24 MDA2
 SDQ_A16 AP22 MDA16
 SDQ_A17 AM22 MDA17
 SDQ_A18 AL24 MDA18
 SDQ_A19 AN27 MDA19
 SDQ_A20 AP21 MDA20
 SDQ_A21 AL22 MDA21
 SDQ_A22 AP25 MDA22
 SDQ_A23 AP27 MDA23
 SDQS_A3 AM30 DQSA3
 SDM_A3 AP30 MDA3
 SDQ_A24 AP28 MDA24
 SDQ_A25 AP29 MDA25
 SDQ_A26 AP33 MDA26
 SDQ_A27 AM33 MDA27
 SDQ_A28 AM28 MDA28
 SDQ_A29 AN29 MDA29
 SDQ_A30 AM31 MDA30
 SDQ_A31 AN34 MDA31
 SDQS_A4 AF34 DQSA4
 SDM_A4 AF31 MDA4
 SDQ_A32 AH32 MDA32
 SDQ_A33 AC34 MDA33
 SDQ_A34 AF32 MDA34
 SDQ_A35 AD32 MDA35
 SDQ_A36 AH31 MDA36
 SDQ_A37 AC33 MDA37
 SDQ_A38 AE34 MDA38
 SDQ_A39 AD34 MDA39
 SDQS_A5 V34 DQSA5
 SDM_A5 W33 DMA5
 SDQ_A40 AC34 MDA40
 SDQ_A41 AB31 MDA41
 SDQ_A42 V32 MDA42
 SDQ_A43 V31 MDA43
 SDQ_A44 AD31 MDA44
 SDQ_A45 AB32 MDA45
 SDQ_A46 U34 MDA46
 SDQ_A47 U33 MDA47
 SDQS_A6 M32 DQSA6
 SDM_A6 M34 DMA6
 SDQ_A48 T34 MDA48
 SDQ_A49 T32 MDA49
 SDQ_A50 K34 MDA50
 SDQ_A51 K32 MDA51
 SDQ_A52 T31 MDA52
 SDQ_A53 P34 MDA53
 SDQ_A54 L34 MDA54
 SDQ_A55 L33 MDA55
 SDQS_A7 H31 DQSA7
 SDM_A7 H32 DMA7
 SDQ_A56 J33 MDA56
 SDQ_A57 H34 MDA57
 SDQ_A58 E33 MDA58
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 SDQ_A62 F34 MDA63

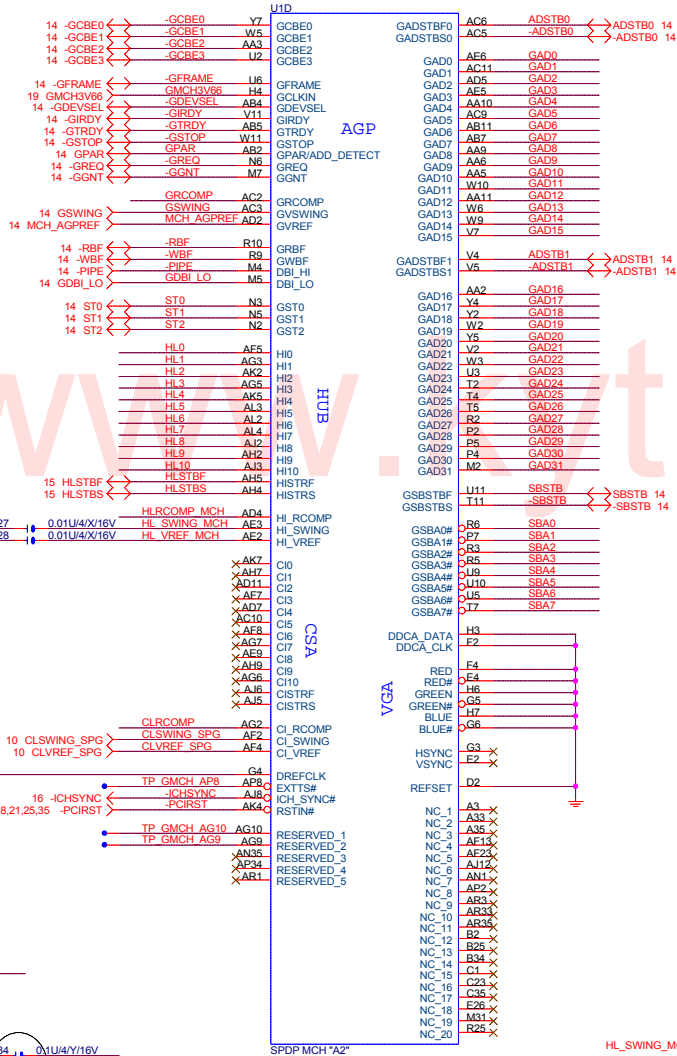
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 SMAA_B1 AP11 MDA1
 SMAA_B2 AL11 MDA2
 SMAA_B3 AN13 MDA3
 SMAA_B4 AL25 MDA4
 SMAA_B5 AE21 MDA5
 SMAA_B6 AL22 MDA6
 SMAA_B7 AL23 MDA7
 SMAA_B8 AE29 MDA8
 SMAA_B9 AL21 MDA9
 SMAA_B10 SMAA_B10
 SMAA_B11 SMAA_B11
 SMAA_B12
 SMAB_B1 AE27 MDA8
 SMAB_B2 AD26 MDA9
 SMAB_B3 AL29 MDA10
 SMAB_B4 AE23 MDA11
 SMAB_B5 AL27 MDA12
 SWE_B# W27 MDA14
 SCAS_B# W31 MDA14
 SRA5_B# W26 MDA15
 SBA_B0 Y25 MDA16
 SBA_B1 AA25 MDA17
 SCS_B# U26 MDA18
 SCS_B1# T28 MDA18
 SCS_B2# V25 MDA19
 SCS_B3# W25 MDA20
 SCKE_B0 AK19 MDA21
 SCKE_B1 AF19 MDA21
 SCKE_B2 AG19 MDA21
 SCKE_B3 AE18 MDA21
 SCMDCLK_B0 AG29 MDA25
 SCMDCLK_B0# AG30 MDA25
 SCMDCLK_B1 AE17 MDA25
 SCMDCLK_B1# AG17 MDA25
 SCMDCLK_B2 N27 MDA25
 SCMDCLK_B2# N26 MDA25
 SCMDCLK_B3 AH29 MDA25
 SCMDCLK_B3# AK15 MDA25
 SCMDCLK_B4 AL15 MDA25
 SCMDCLK_B4# N31 MDA25
 SCMDCLK_B5# N30 MDA25
 SMVREF_B SMVREF_B
 SMYRCOMP SMYRCOMP
 SMYRCOMPVOH R34 SMYRCOMPVOH
 SMYRCOMPVOL R33 SMYRCOMPVOL

SDQS_B0 AE15 MDA15
 SDQ_B0 AG11 MDA15
 SDQ_B1 AL10 MDA15
 SDQ_B2 AE15 MDA15
 SDQ_B3 SMAA_B3 MDA15
 SDQ_B4 SDQ_B4 MDA15
 SDQ_B5 AE19 MDA15
 SDQ_B6 AK11 MDA15
 SDQ_B7 AG12 MDA15
 SDQS_B1 AG13 MDA15
 SDM_B1 AG19 MDA15
 SDQ_B8 AE17 MDA15
 SDQ_B9 AL13 MDA15
 SDQ_B10 AK17 MDA15
 SDQ_B11 AL15 MDA15
 SDQ_B12 AK14 MDA15
 SDQ_B13 AL14 MDA15
 SDQ_B14 AL15 MDA15
 SDQ_B15 AL15 MDA15
 SDQS_B2 AG21 MDA15
 SDM_B2 AE21 MDA15
 SDQ_B16 AE19 MDA15
 SDQ_B17 AE20 MDA15
 SDQ_B18 AC24 MDA15
 SDQ_B19 AL19 MDA15
 SDQ_B20 AL12 MDA15
 SDQ_B21 AK21 MDA15
 SDQ_B22 AJ24 MDA15
 SDQ_B23 AE22 MDA15
 SDQS_B3 AH27 MDA15
 SDM_B3 AG24 MDA15
 SDQ_B24 AK25 MDA15
 SDQ_B25 AH26 MDA15
 SDQ_B26 AE27 MDA15
 SDQ_B27 SCMDCLK_B1# MDA15
 SDQ_B28 AJ26 MDA15
 SDQ_B29 AD26 MDA15
 SDQ_B30 AE28 MDA15
 SDQ_B31
 SDQS_B4 AD29 MDA15
 SDM_B4 AC31 MDA15
 SDQ_B32 AE30 MDA15
 SDQ_B33 AC34 MDA15
 SDQ_B34 Y29 MDA15
 SDQ_B35 Y29 MDA15
 SDQ_B36 AE34 MDA15
 SDQ_B37 AE29 MDA15
 SDQ_B38 AA26 MDA15
 SDQ_B39 AA27 MDA15
 SDQS_B5 U30 MDA15
 SDM_B5 U31 MDA15
 SDQ_B40 AA30 MDA15
 SDQ_B41 W30 MDA15
 SDQ_B42 U27 MDA15
 SDQ_B43 T25 MDA15
 SDQ_B44 V29 MDA15
 SDQ_B45 U25 MDA15
 SDQ_B46 R27 MDA15
 SDQ_B47
 SDQS_B6 L27 MDA15
 SDM_B6 M29 MDA15
 SDQ_B48 P29 MDA15
 SDQ_B49 R30 MDA15
 SDQ_B50 K28 MDA15
 SDQ_B51 L30 MDA15
 SDQ_B52 R31 MDA15
 SDQ_B53 R26 MDA15
 SDQ_B54 P25 MDA15
 SDQ_B55 L32 MDA15
 SDQS_B7 J30 MDA15
 SDM_B7 J31 MDA15
 SDQ_B56 K30 MDA15
 SDQ_B57 H29 MDA15
 SDQ_B58 F32 MDA15
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 SDQ_B61 M25 MDA15
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 SDQ_B63 G32 MDA15

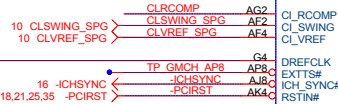


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Size	Document Number		Rev		
Custom	GA-81848P-G		2.01		
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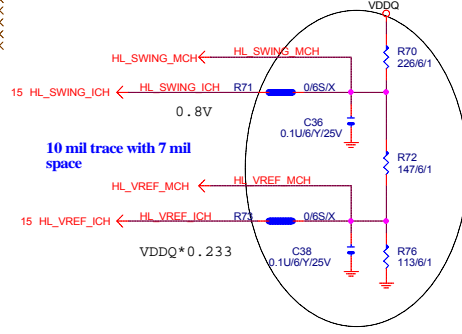
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 14 SBA[0..7] ↔ SBA[0..7]
 15 HL[0..10] ↔ HL[0..10]



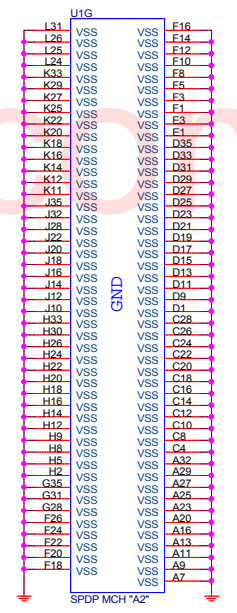
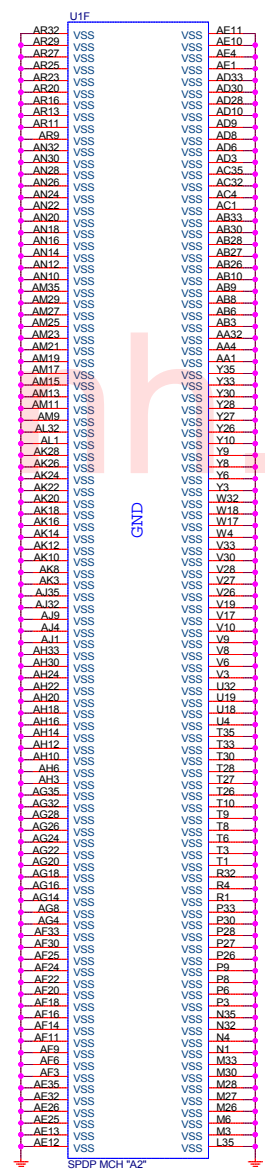
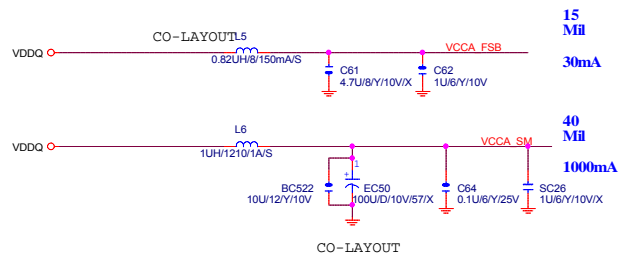
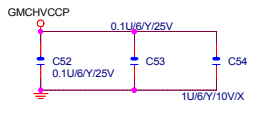
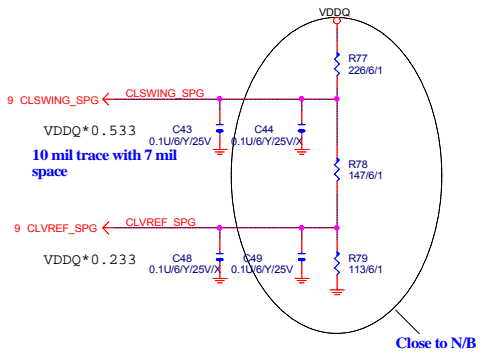
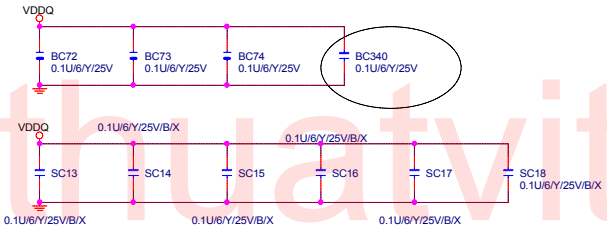
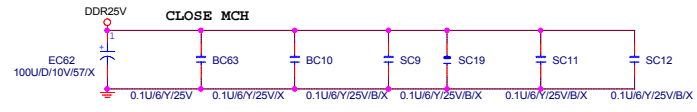
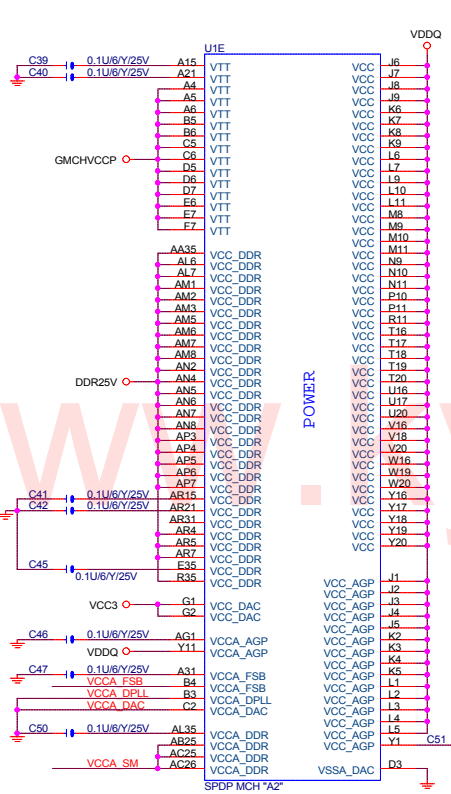
Close to MCH



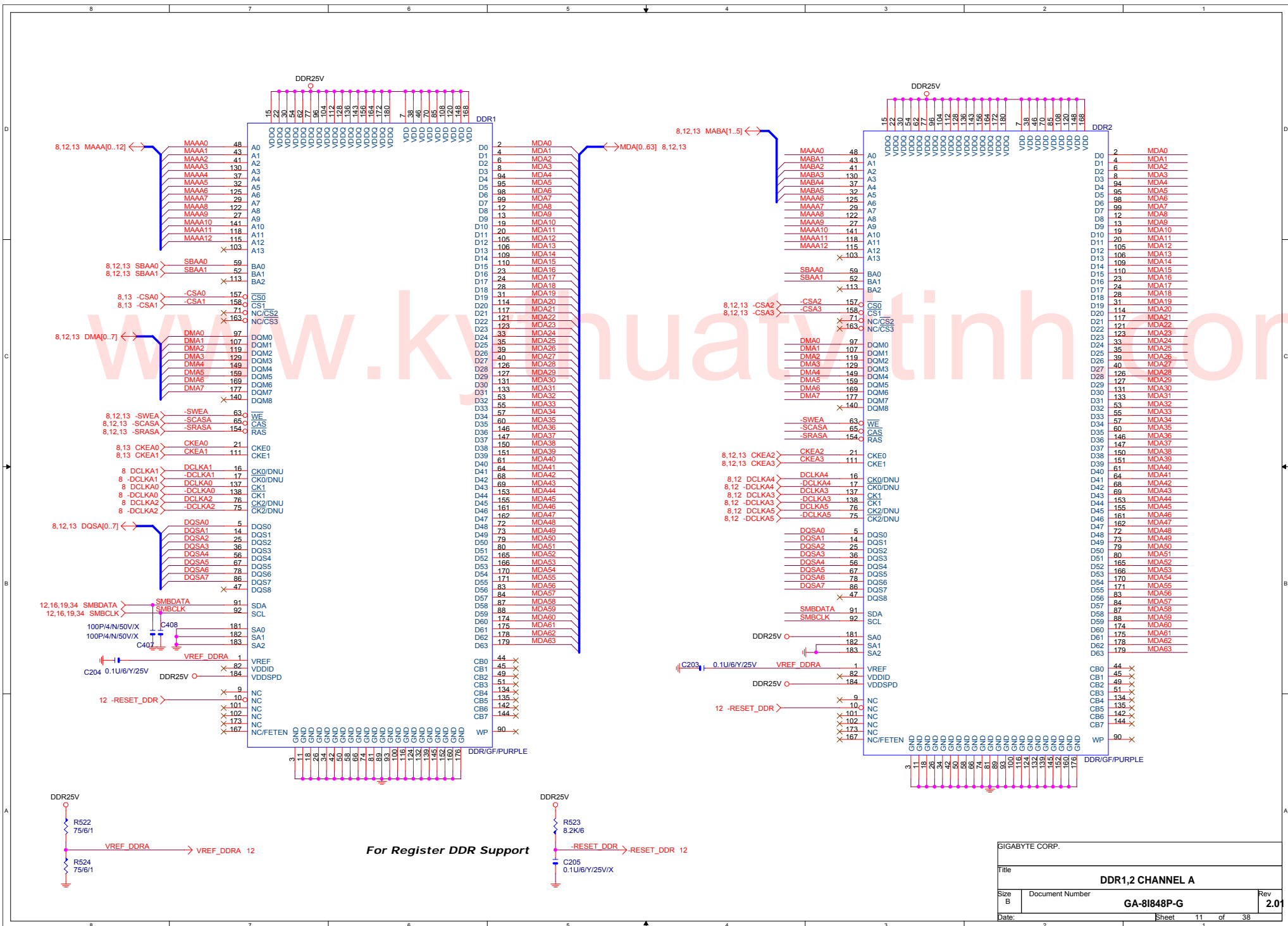
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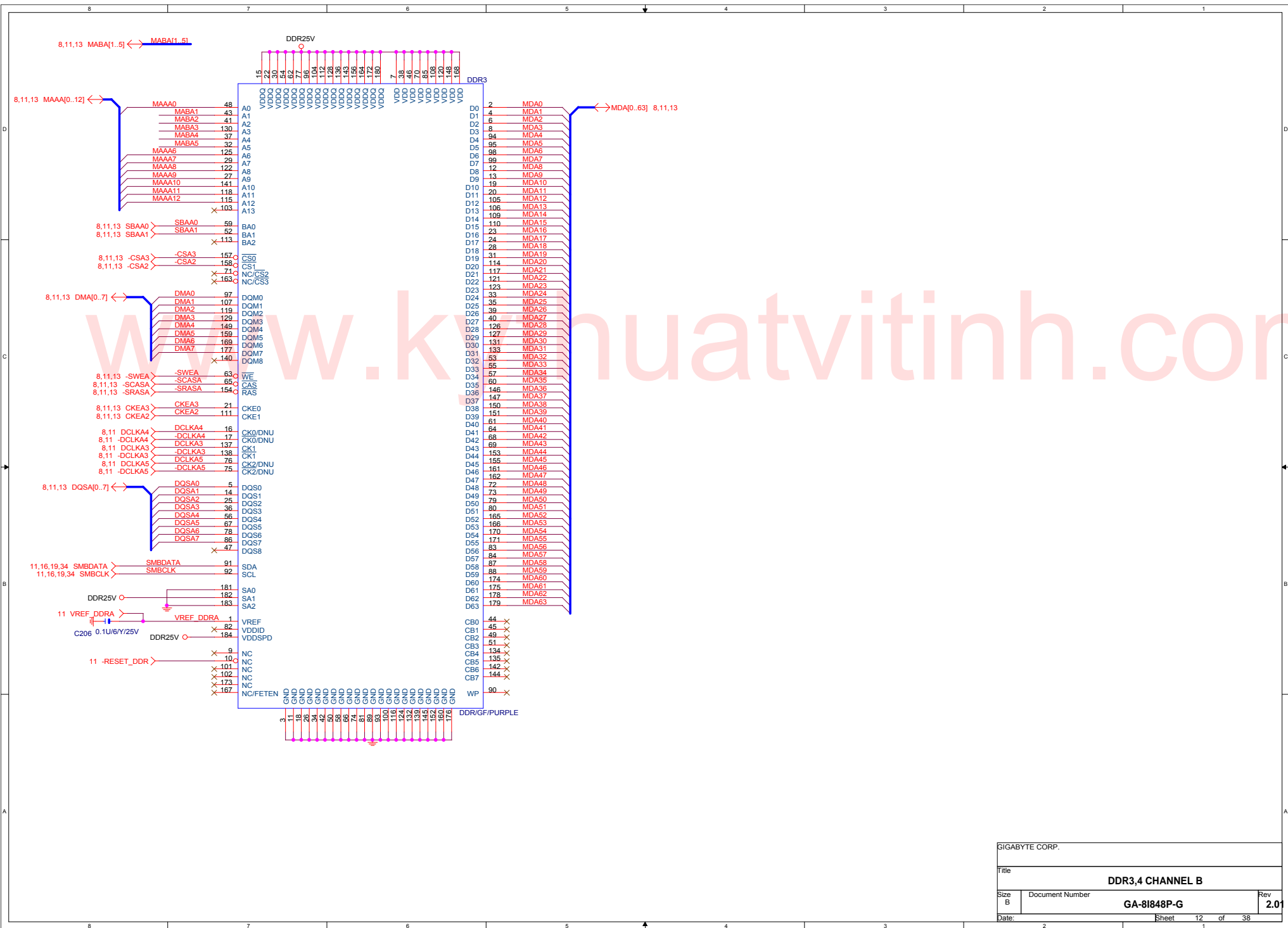
Title		
SPRINGDALE AGP,HUB,CSA,VGA		
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Title			
SPRINGDALE PWR			
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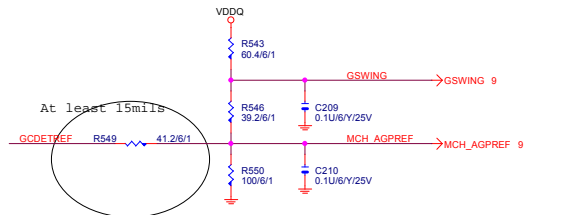
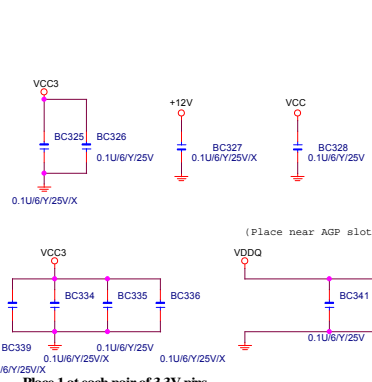
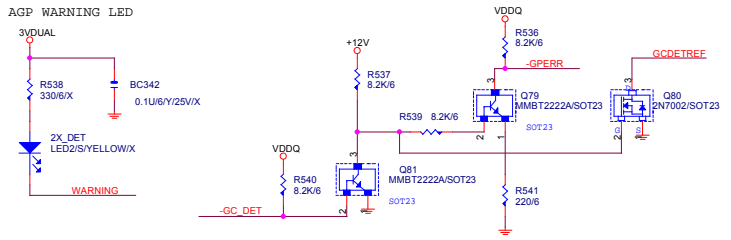
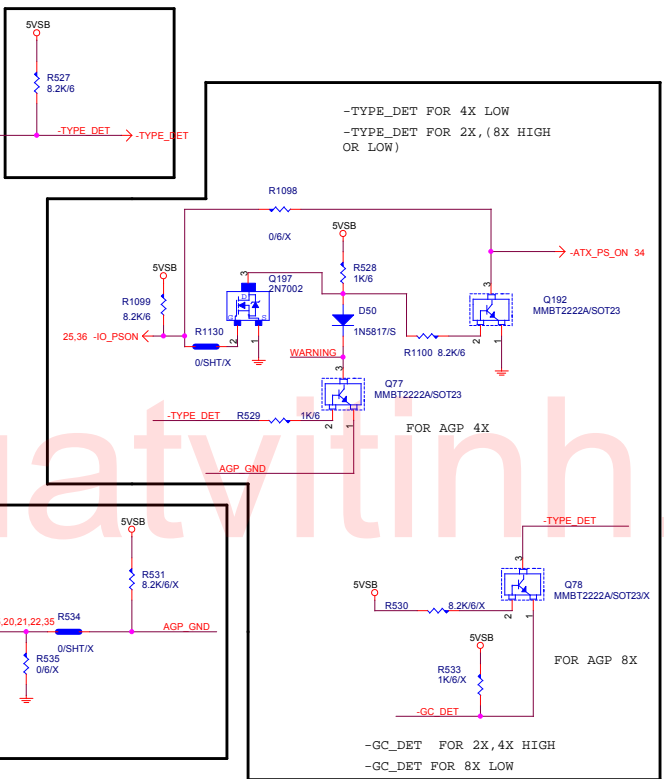
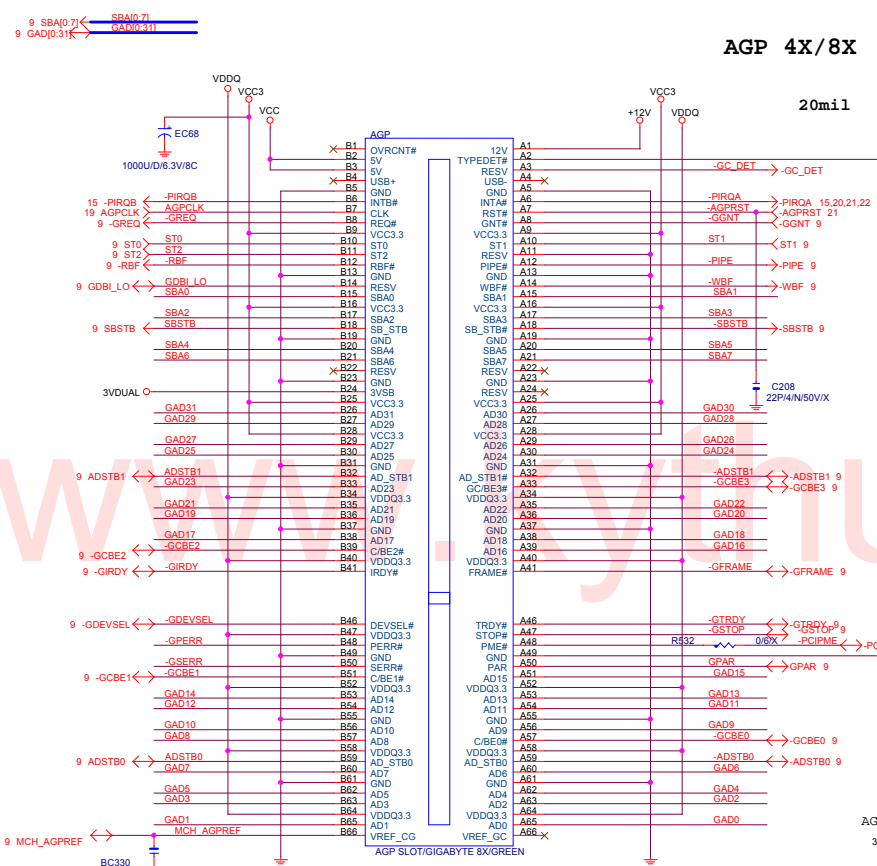


SIGABYTE CORP.		
Title		
DDR1,2 CHANNEL A		
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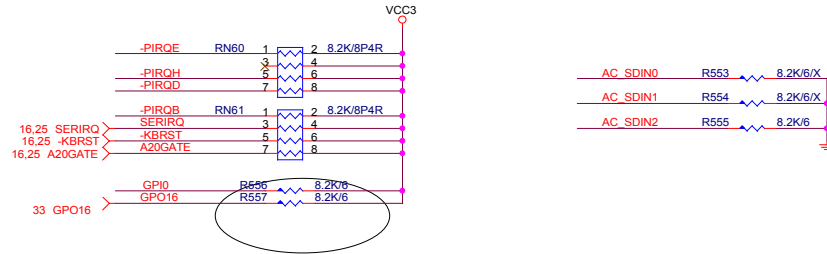
AGP 4X/8X

20mil

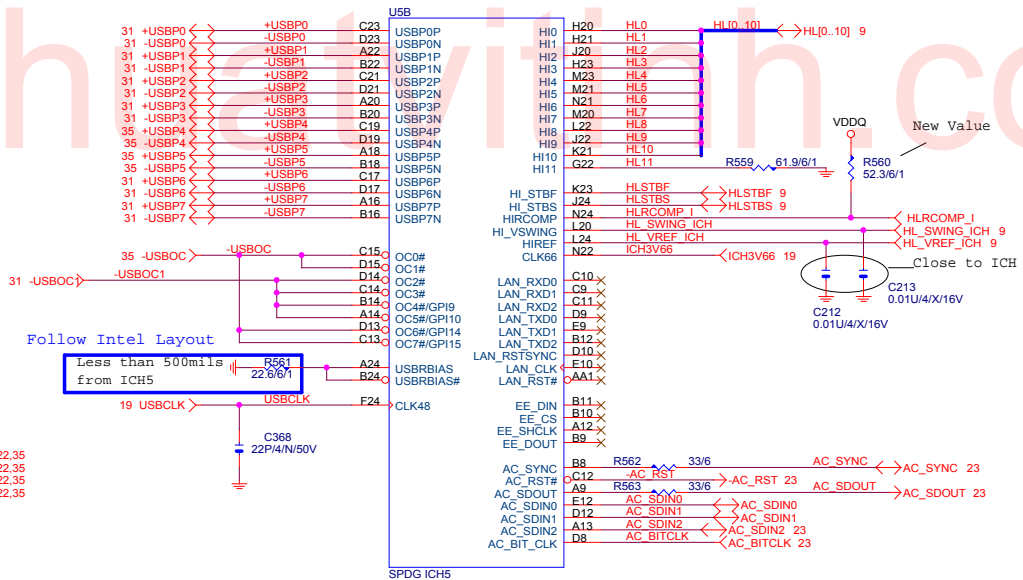
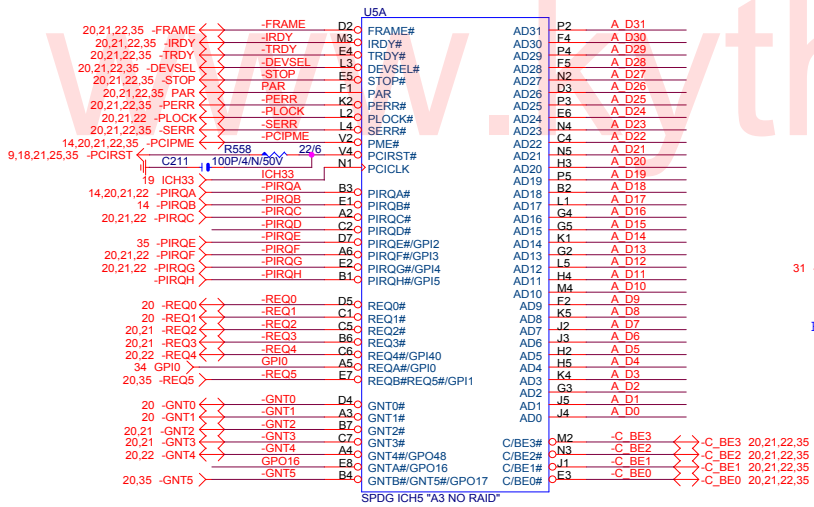


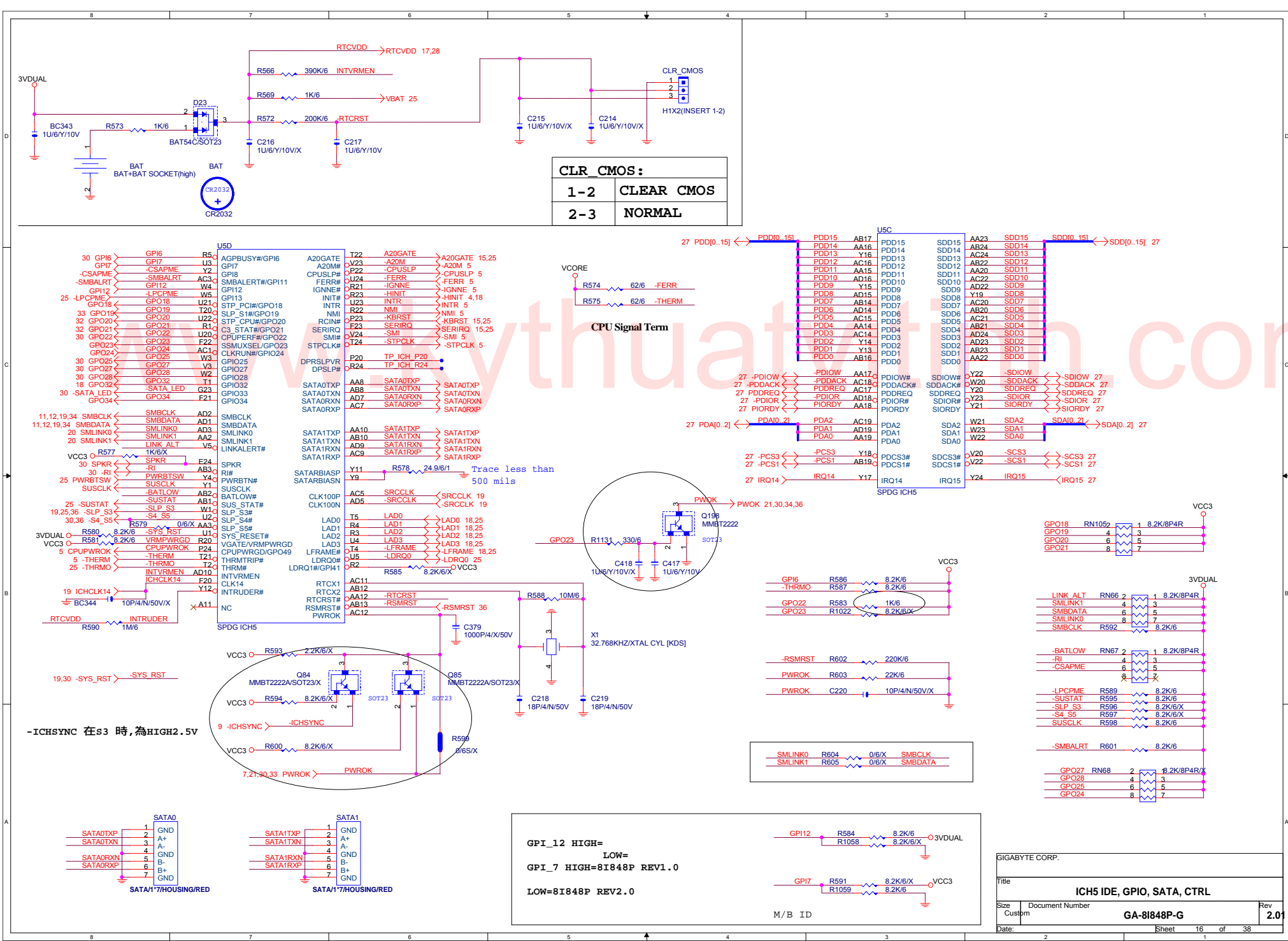
Place 1 at each pair of +3.3V pins
Place 1 at each pair of VDDQ pins
Place an additional for spread from A14 - A33

GIGABYTE CORP.		
AGP SLOT		
Title	Document Number	Rev
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A_D10_311 <-> A_D10_311 20.21.22.35

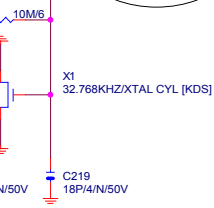
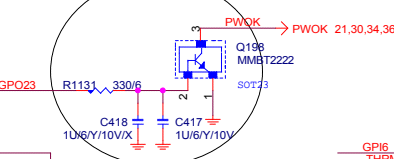
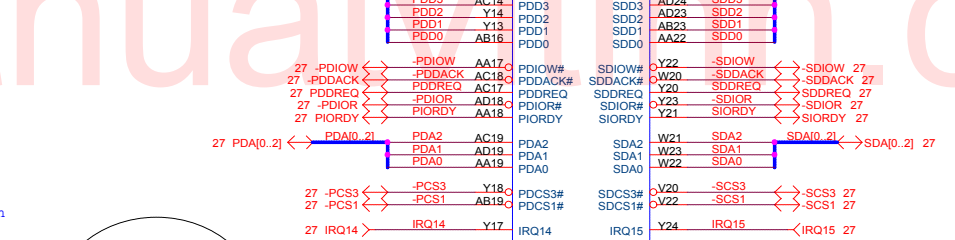




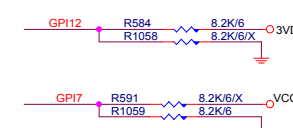
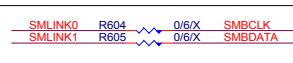
CLR_CMOS :

1-2	CLEAR CMOS
2-3	NORMAL

CPU Signal Term



GPI_12 HIGH=
LOW=
GPI_7 HIGH=8I848P REV1.0
LOW=8I848P REV2.0

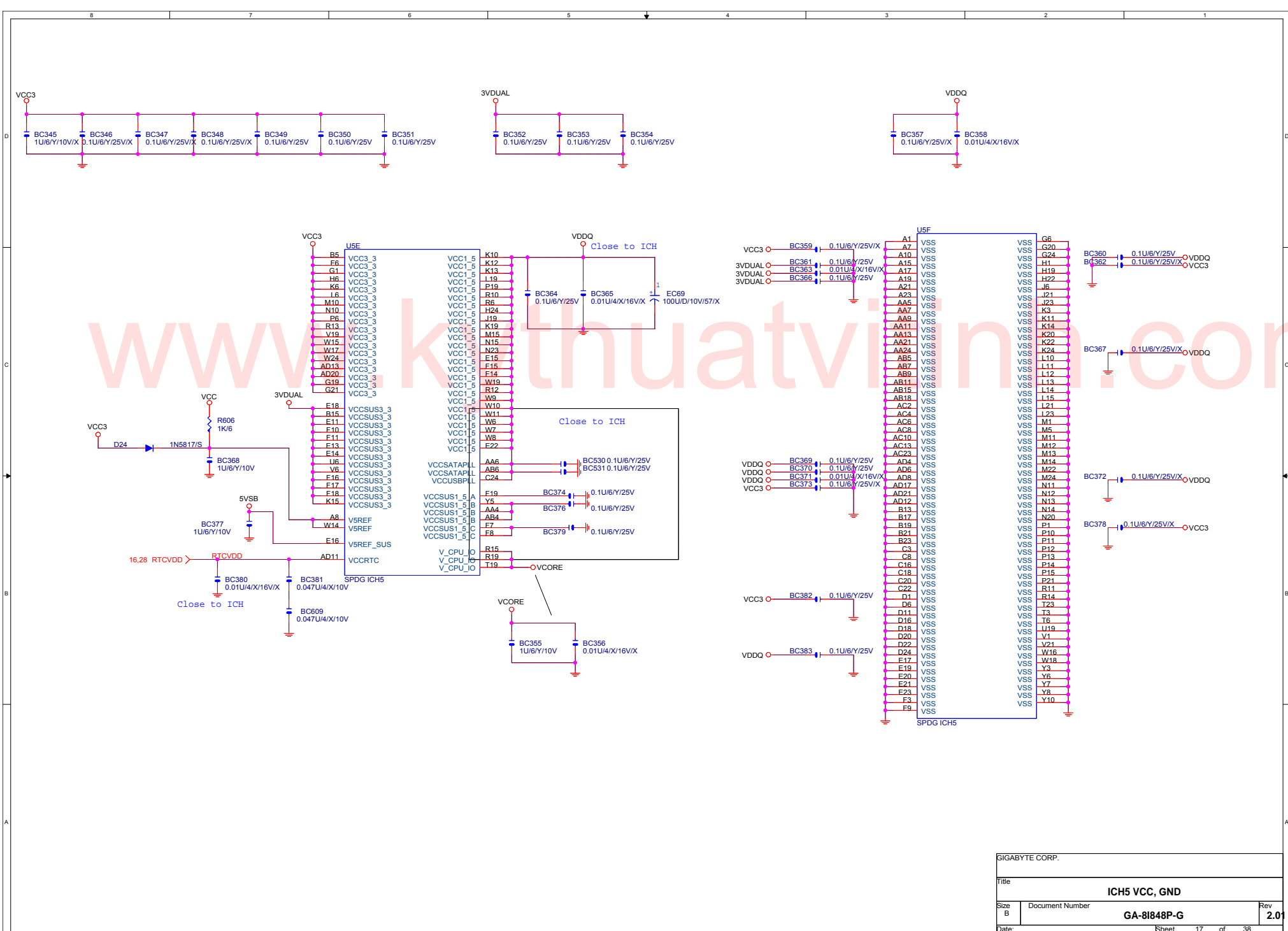


GIGABYTE CORP.

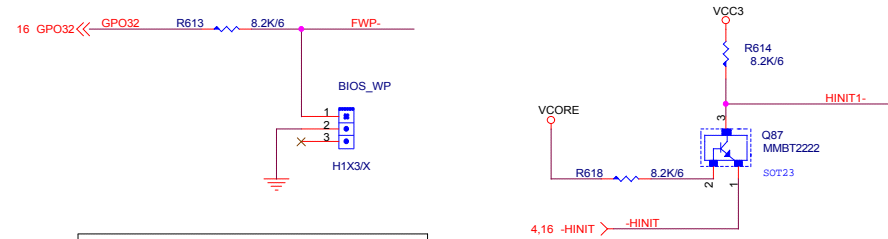
Title: **ICH5 IDE, GPIO, SATA, CTRL**

Size: Document Number: **GA-8I848P-G** Rev: **2.01**

Date: Sheet 16 of 38

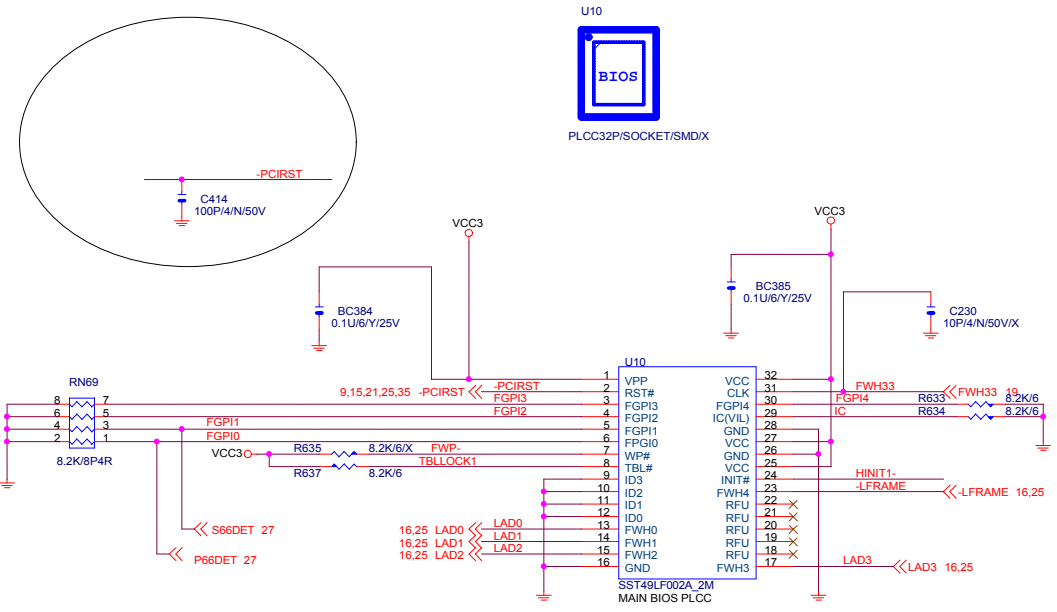


SIGABYTE CORP.		
Title		
ICH5 VCC, GND		
Size	Document Number	Rev
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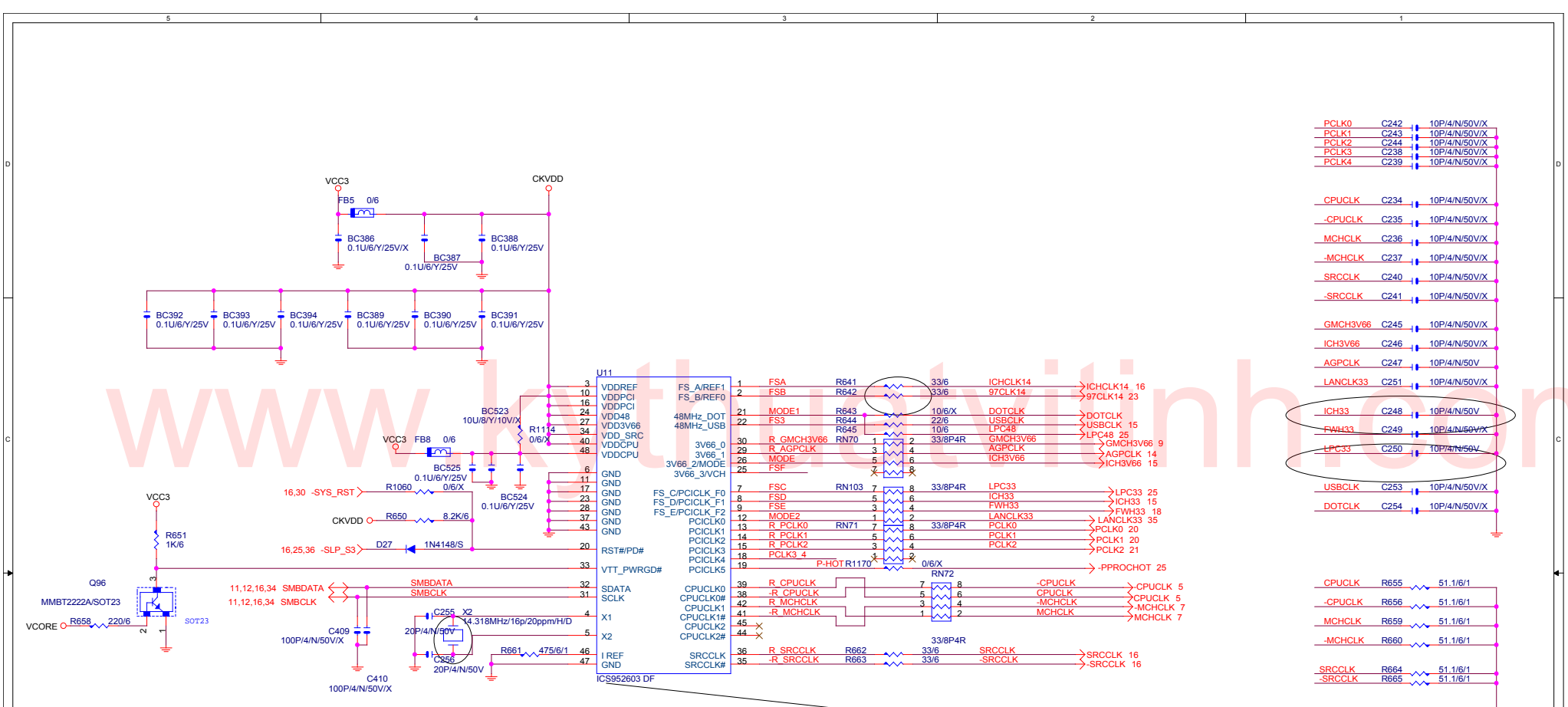
BIOS_WP :	
1-2	WRITE PROTECT
2-3	DISABLE

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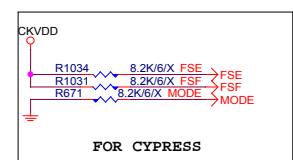
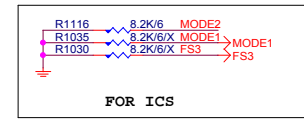
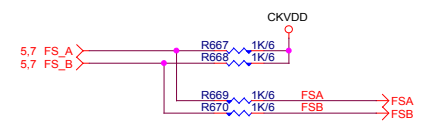
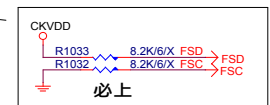
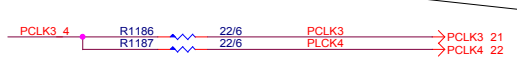


ADD WINBOUD FWH SEC. SOURCE

GIGABYTE CORP.		
Title		FWH
Size B	Document Number	GA-8I848P-G
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PCLK0	C242	10P/4/N/50V/X
PCLK1	C243	10P/4/N/50V/X
PCLK2	C244	10P/4/N/50V/X
PCLK3	C238	10P/4/N/50V/X
PCLK4	C239	10P/4/N/50V/X
CPUCLK	C234	10P/4/N/50V/X
-CPUCLK	C235	10P/4/N/50V/X
MCHCLK	C236	10P/4/N/50V/X
-MCHCLK	C237	10P/4/N/50V/X
SRCCLK	C240	10P/4/N/50V/X
-SRCCLK	C241	10P/4/N/50V/X
GMCH3V66	C245	10P/4/N/50V/X
ICH3V66	C246	10P/4/N/50V/X
AGPCLK	C247	10P/4/N/50V/X
LANCLK33	C251	10P/4/N/50V/X
ICH33	C248	10P/4/N/50V
FWH33	C249	10P/4/N/50V
LPC33	C250	10P/4/N/50V
USBCLK	C253	10P/4/N/50V/X
DOTCLK	C254	10P/4/N/50V/X
CPUCLK	R655	51.1/6/1
-CPUCLK	R656	51.1/6/1
MCHCLK	R659	51.1/6/1
-MCHCLK	R660	51.1/6/1
SRCCLK	R664	51.1/6/1
-SRCCLK	R665	51.1/6/1



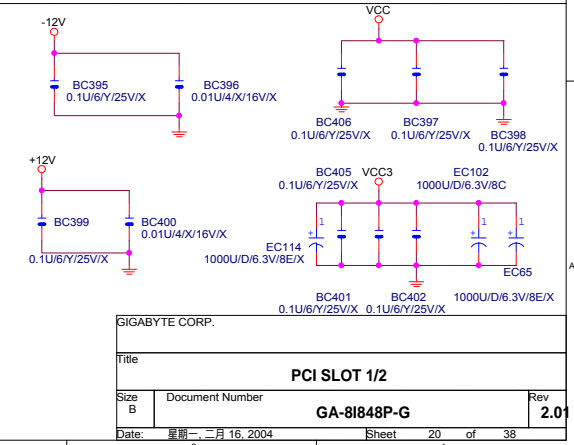
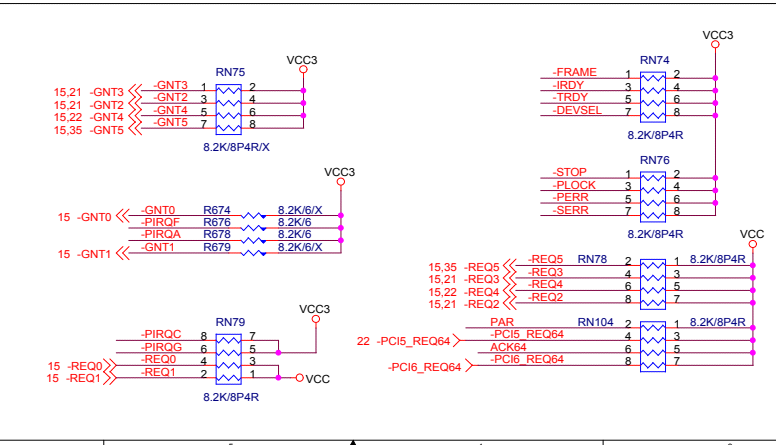
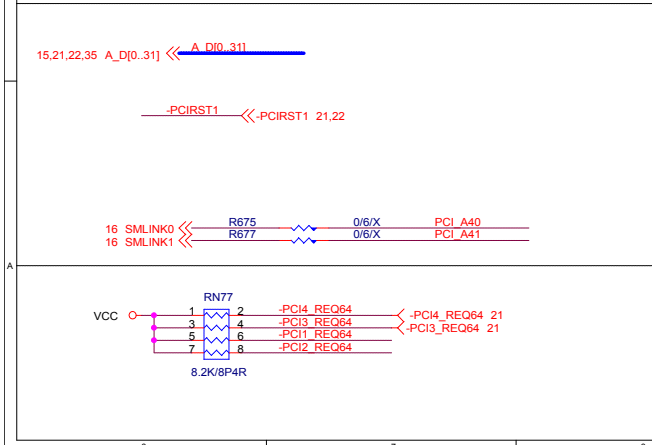
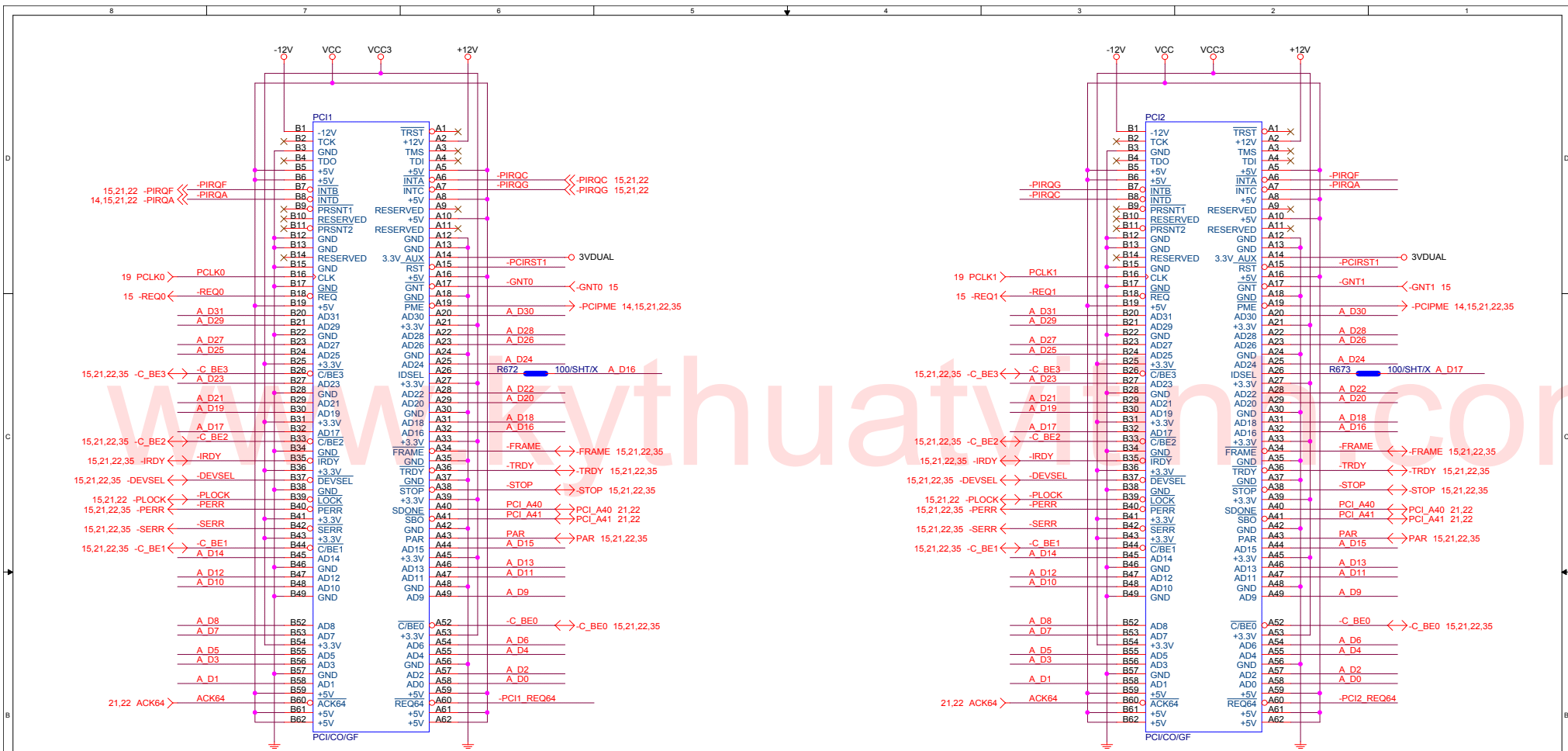
CYPRESS CY28405

FS_E	FS_D	FS_C	FS_A	FS_B	Clock
1	1	0	0	0	100MHz
1	1	0	1	0	133MHz
1	1	0	1	1	166MHz
1	1	0	0	1	200MHz

ICS952603

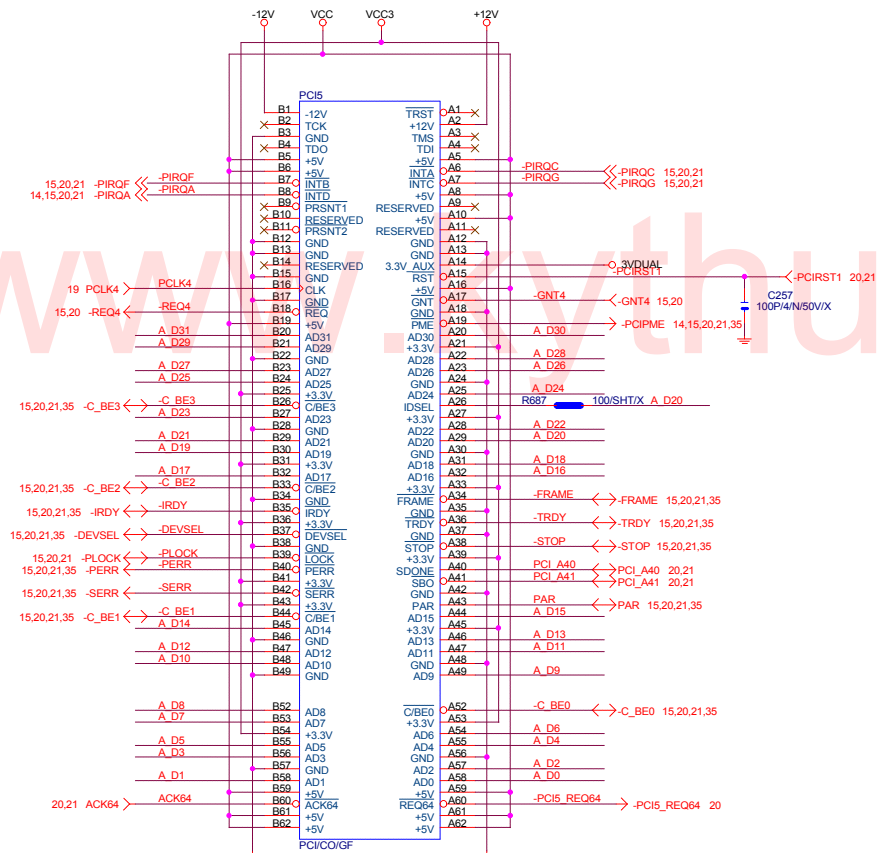
FS_D	FS_3	FS_C	FS_A	FS_B	Clock
1	0	0	0	0	100MHz
1	0	0	1	0	133MHz
1	0	0	1	1	166MHz
1	0	0	0	1	200MHz

CY28405 上 R1031,R1034,R671
不上 R1030,R1035
ICS952616 上 R1030,R1035
不上 R1031,R1034,R671



GIGABYTE CORP.		
Title		
PCI SLOT 1/2		
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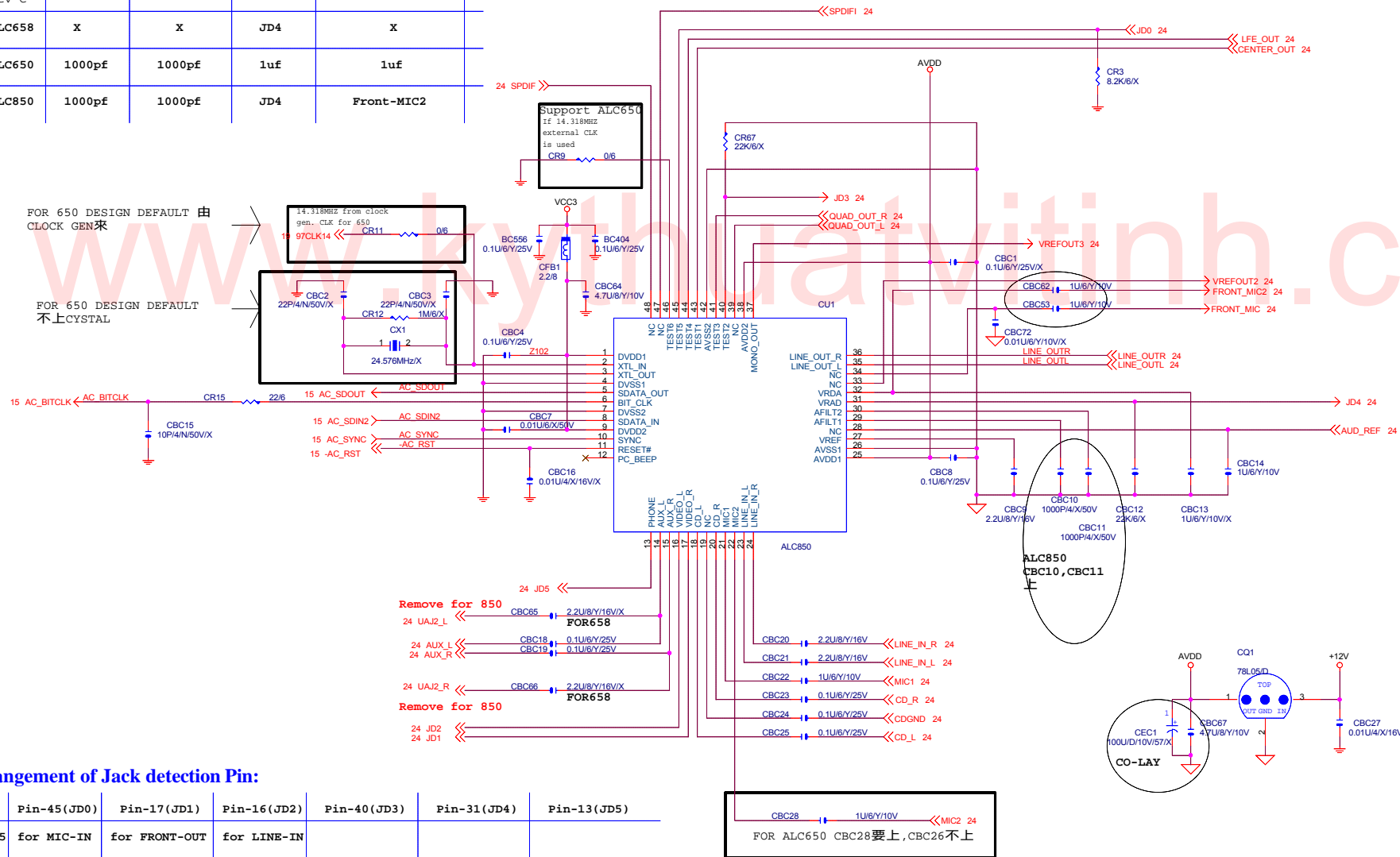
15,20,21,35 A_D[0..31] << A_D[0..31]



GIGABYTE CORP.			
Title			
PCI SLOT 5/6			
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Filter Cap design:

	Pin-29	Pin-30	Pin-31	Pin-32
ALC655 Rev D	1000pf	1000pf	1uf	Front-MIC2
ALC655 Rev C	1000pf	1000pf	1uf	X
ALC658	X	X	JD4	X
ALC650	1000pf	1000pf	1uf	1uf
ALC850	1000pf	1000pf	JD4	Front-MIC2

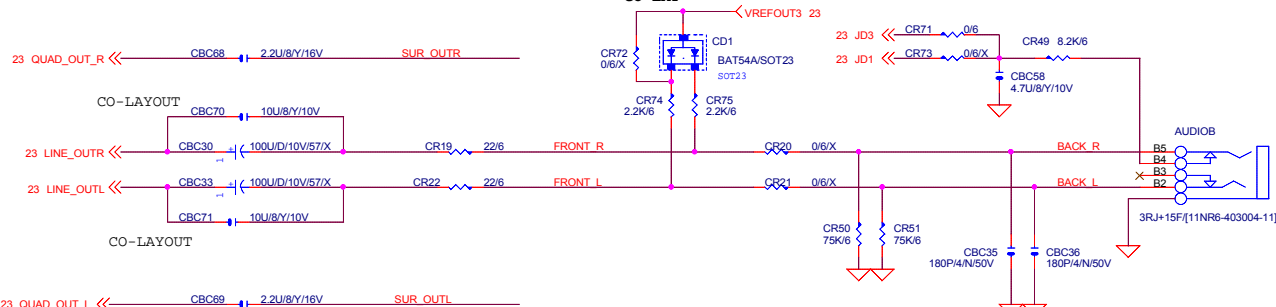


Arrangement of Jack detection Pin:

	Pin-45(JD0)	Pin-17(JD1)	Pin-16(JD2)	Pin-40(JD3)	Pin-31(JD4)	Pin-13(JD5)
ALC655	for MIC-IN	for FRONT-OUT	for LINE-IN			
ALC658	for MIC-IN	for UAJ1	for UAJ2	for FRONT-OUT External pull high is needed	for LINE-IN External pull high is needed	
ALC850	for MIC-IN	for Front Pannel OUT	for Front Pannel IN	for FRONT-OUT	for LINE-IN	for SurrBack Out

LINE OUT

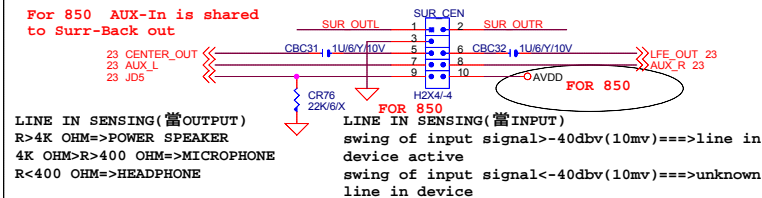
JDO,JD2,GPIO0 為偵測DEVICE INPUT 時由LOW TO HIGH Edge trigger(pop manual) 1/2(3.14)RC=1/2(3.14)8.2K*4.7U=4.3HZ以上AC 信號全部衰減 TO 0V 不會造成JDO 誤動作(無device 時play wav)



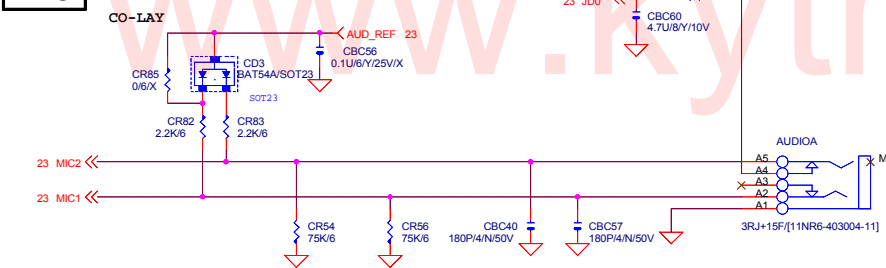
LINE OUT SENSING
 R>4K OHM=>POWER SPEAKER
 4K OHM>R>400 OHM=>MICROPHONE
 R<400 OHM=>HEADPHONE

2x5 header for 850
 For 850 if JD5 = low AUX-In is configured as input
 For 850 if JD5 = high AUX-In is configured as output, Surr-Back out

For 850 AUX-In is shared to Surr-Back out



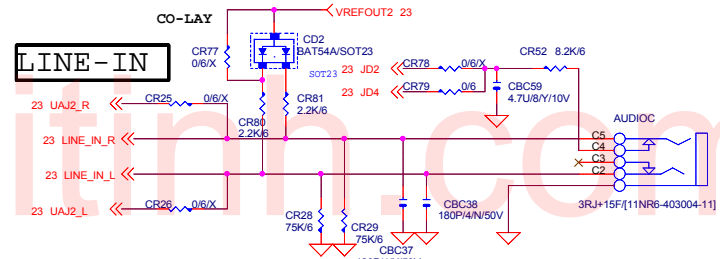
MIC



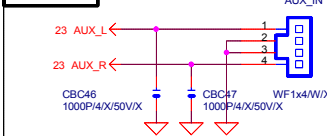
MICROPHONE IN SENSING(當INPUT)(利用vref 偏壓與CR43,CR32 並聯求出阻抗)
 7.1k ohm>R>2.3k ohm==>microphone in
 R<2.3k ohm or R>7.1k ohm==>unknown device

MICROPHONE IN SENSING(當OUTPUT)
 R>4K OHM=>POWER SPEAKER
 4K OHM>R>400 OHM=>MICROPHONE
 R<400 OHM=>HEADPHONE

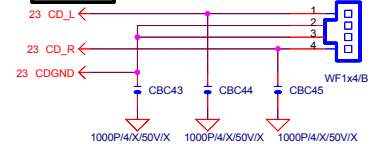
LINE-IN



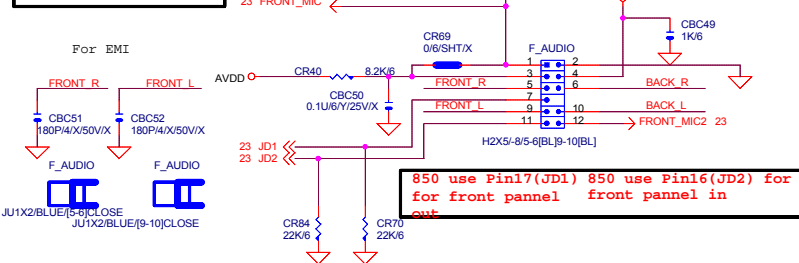
AUX IN DEFAULT NO POP



CD IN

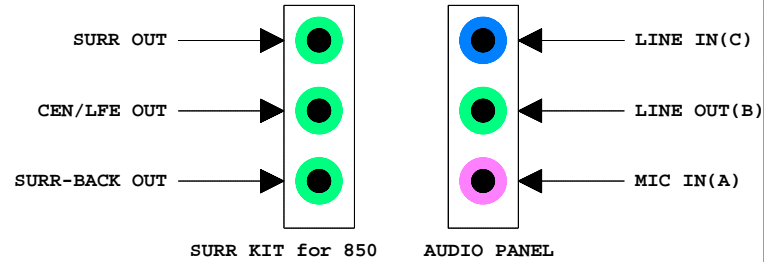
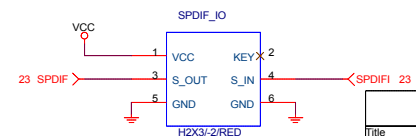


INTEL FRONT AUDIO



850 use Pin17(JD1) 850 use Pin16(JD2) for front panel front panel in out

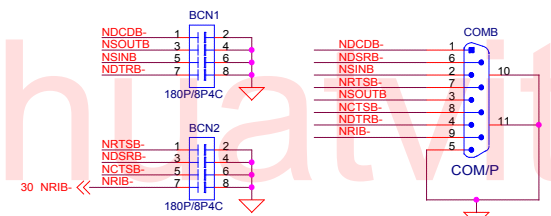
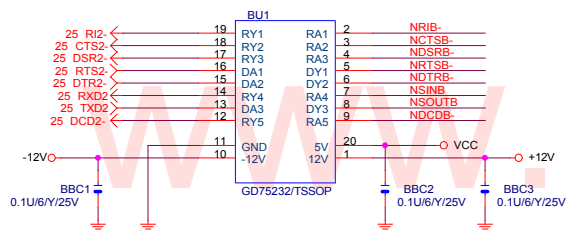
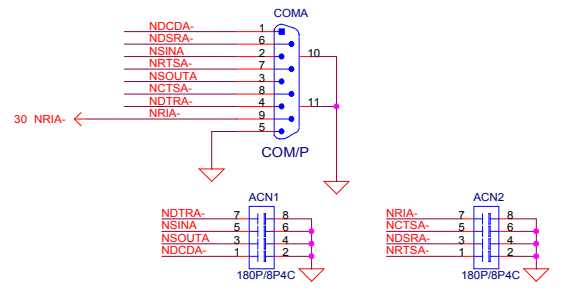
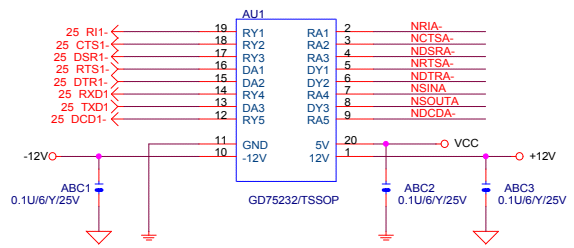
SPDIF_IO



GIGABYTE CORP.

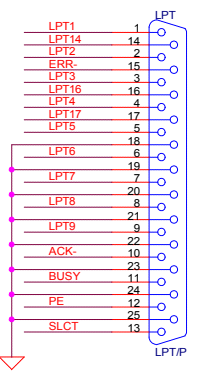
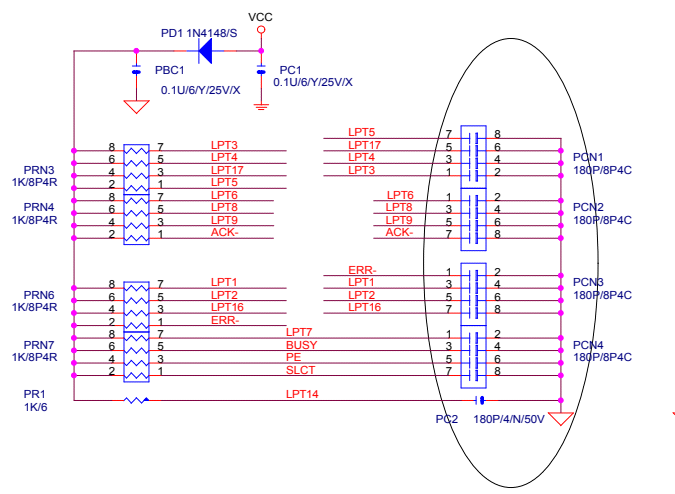
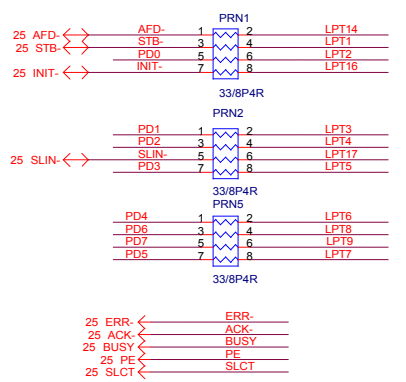
AUDIO OUTPUT, GAME PORT

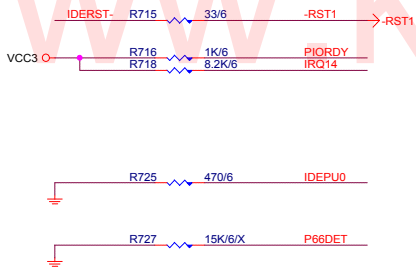
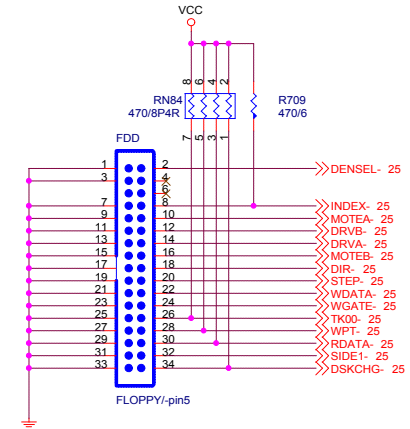
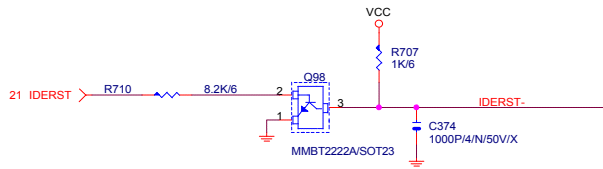
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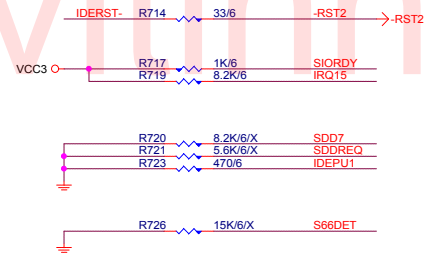
PLACE NEAR VGA_COM CONNECTOR

25 PD[0..7] ↔ PD[0..7]

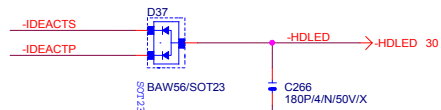
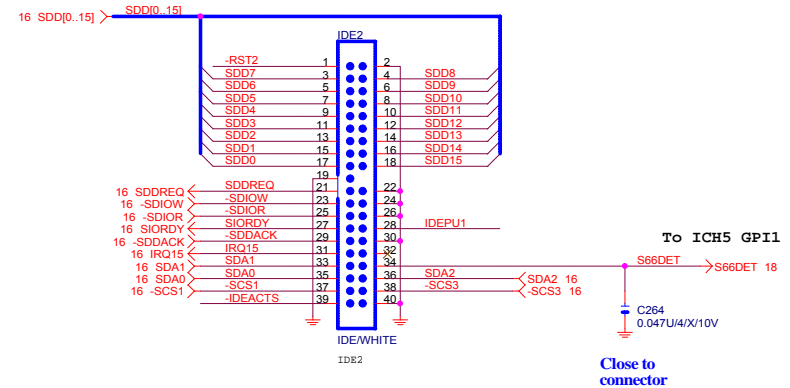
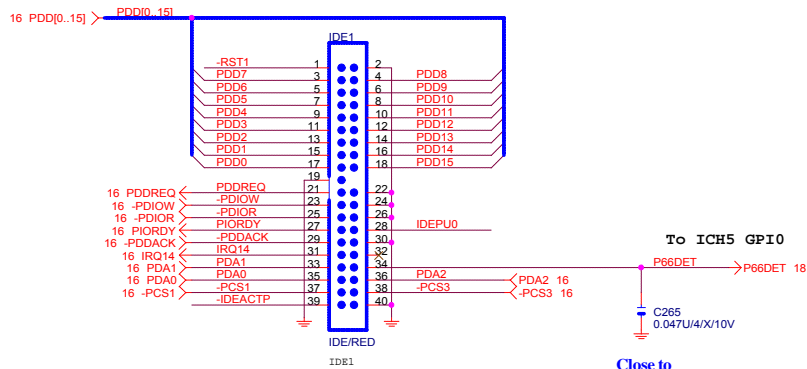




PRIMARY IDE CONNECTOR

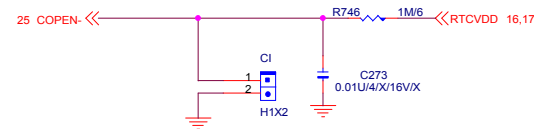
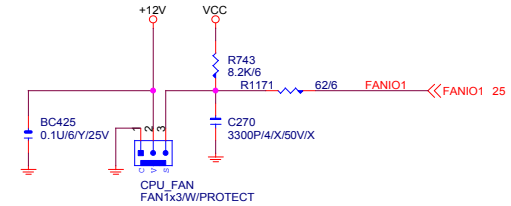
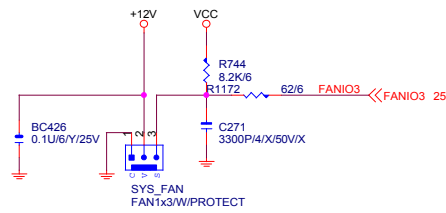
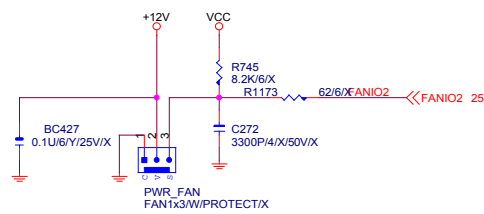
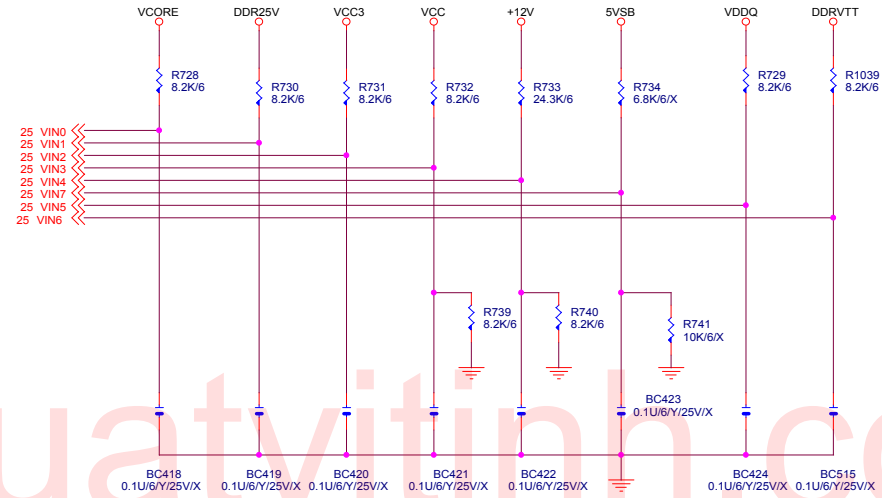
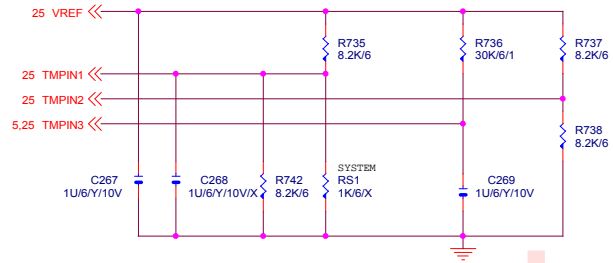


SECONDARY IDE CONNECTOR



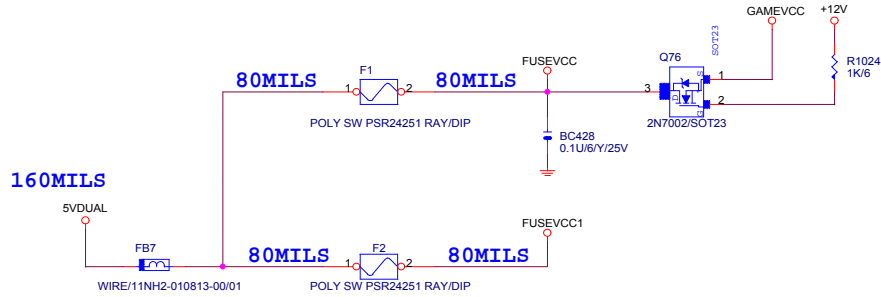
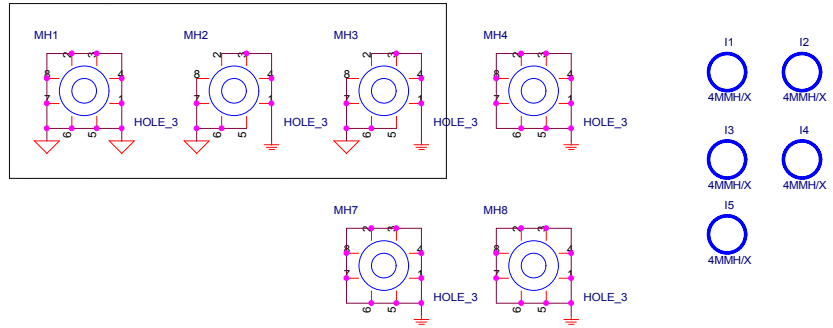
GIGABYTE CORP.		
Title		
IDE CONNECTOR		
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Hardware Monitor circuits

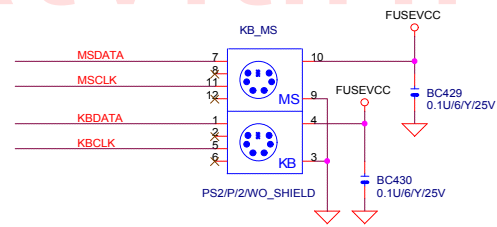
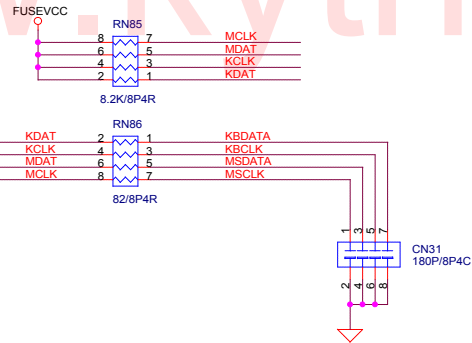


SIGABYTE CORP.		
Title		
FAN/HWMO		
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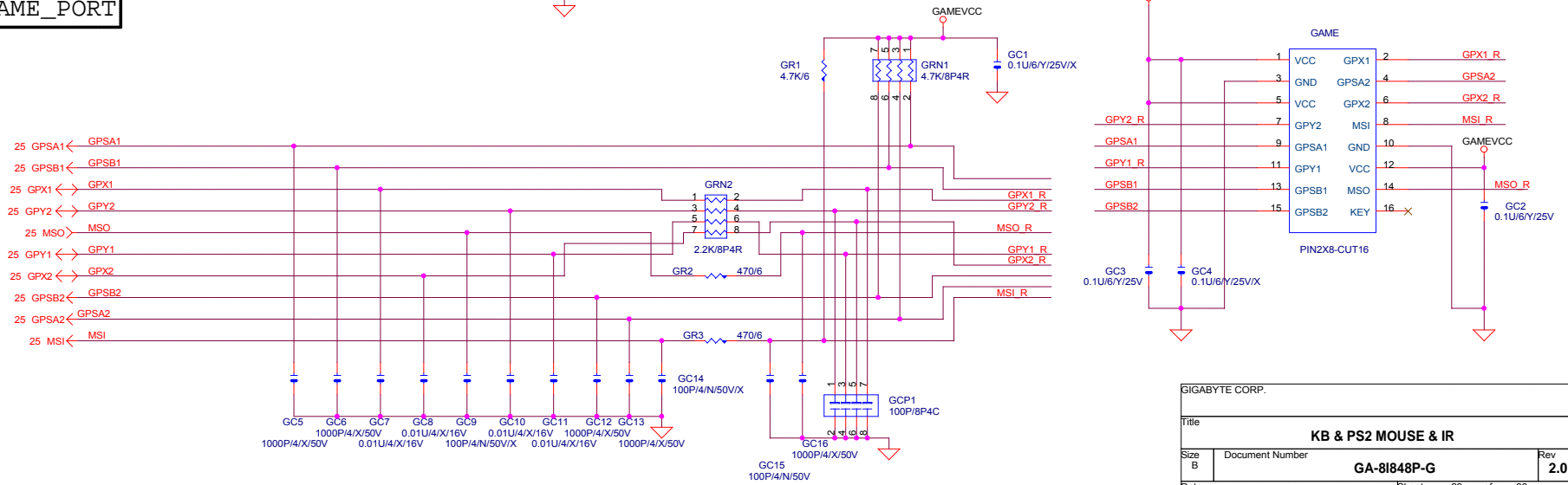
ATX AGND 與 GND 切割必須有三個



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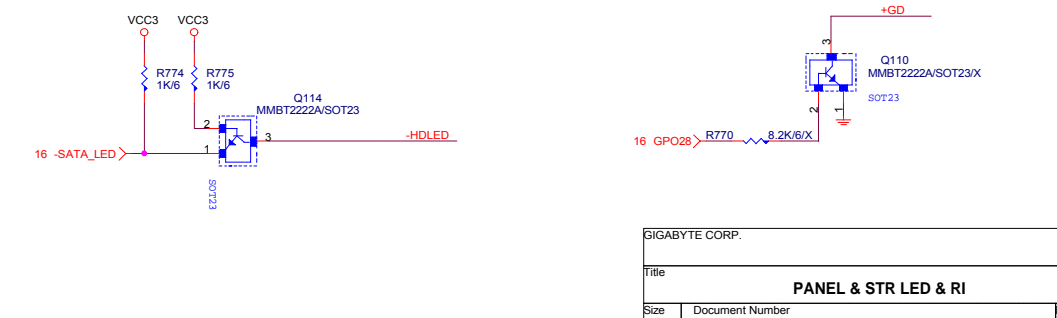
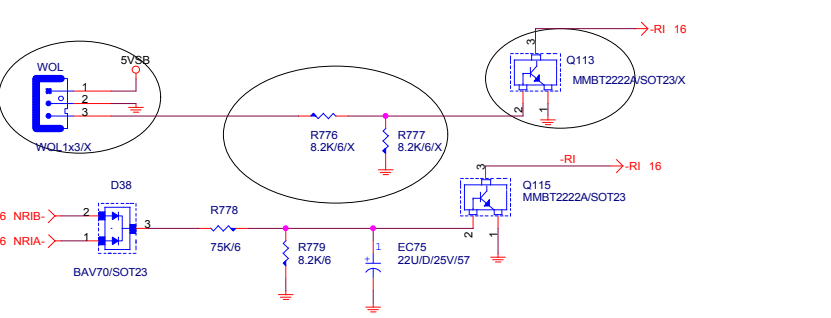
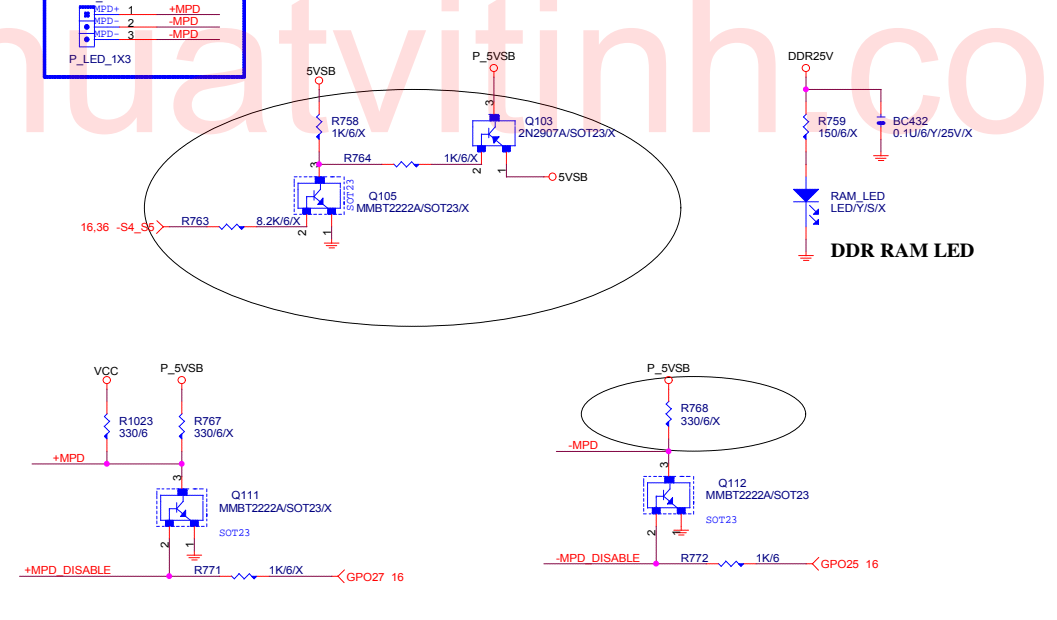
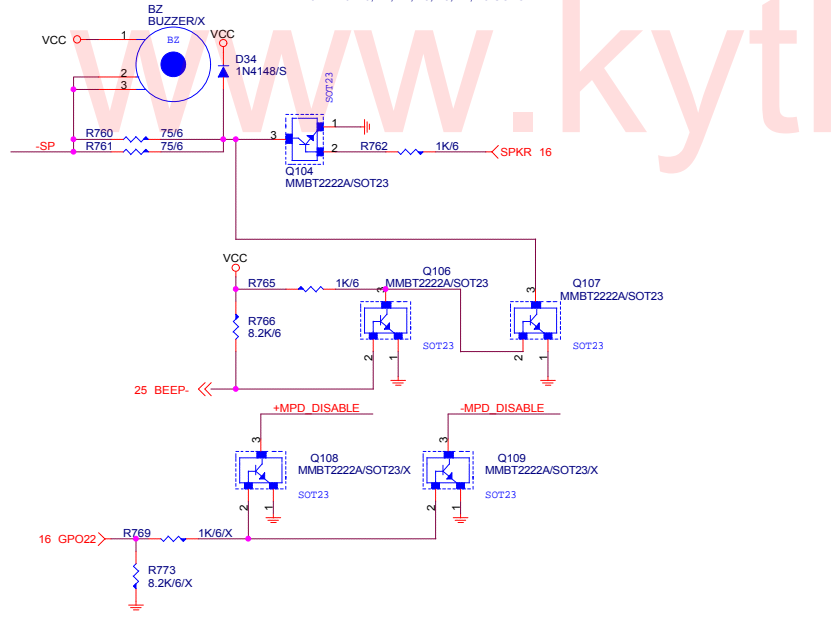
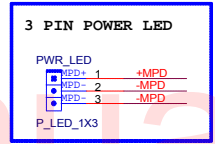
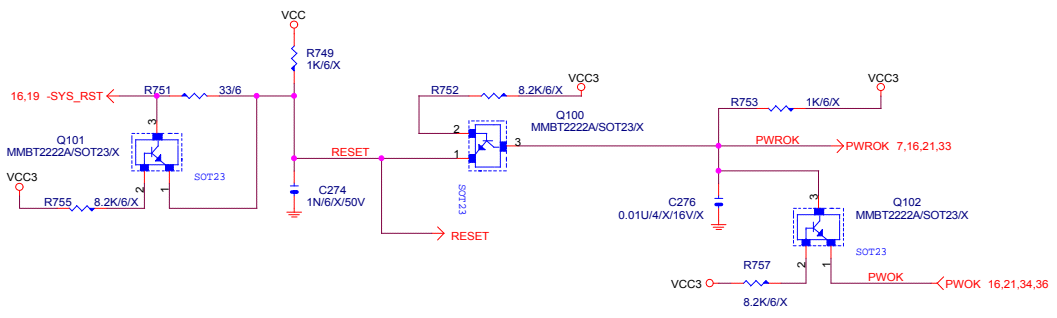
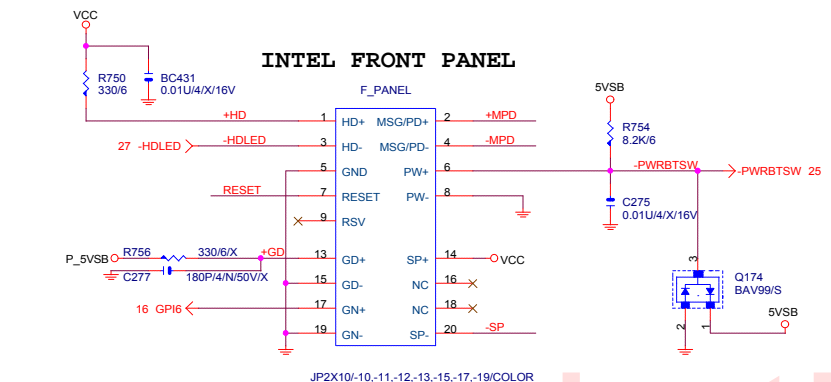


GAME_PORT



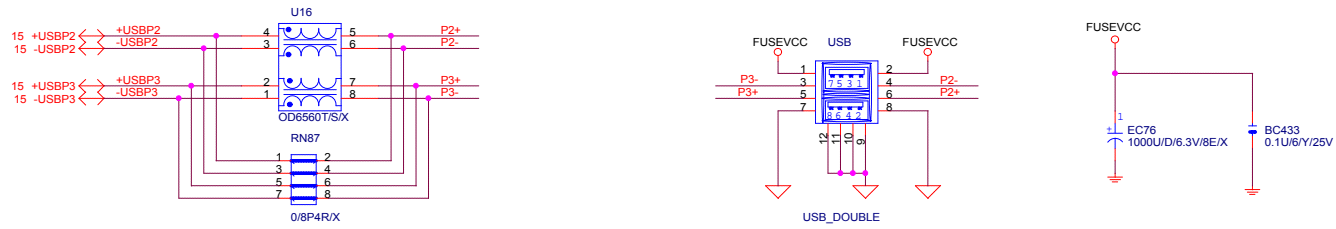
SIGABYTE CORP.		
Title		
KB & PS2 MOUSE & IR		
Size B	Document Number	Rev
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INTEL FRONT PANEL

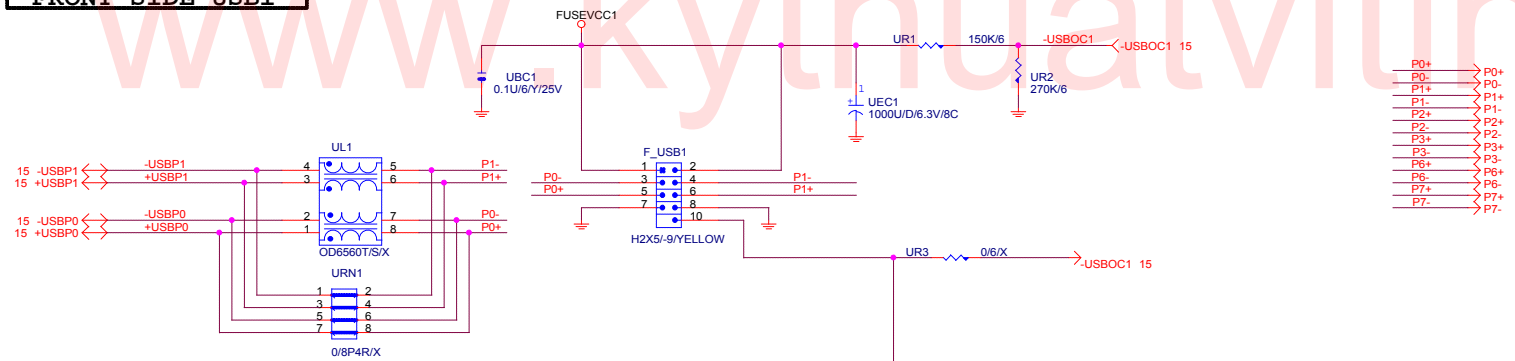


GIGABYTE CORP.		
Title		
PANEL & STR LED & RI		
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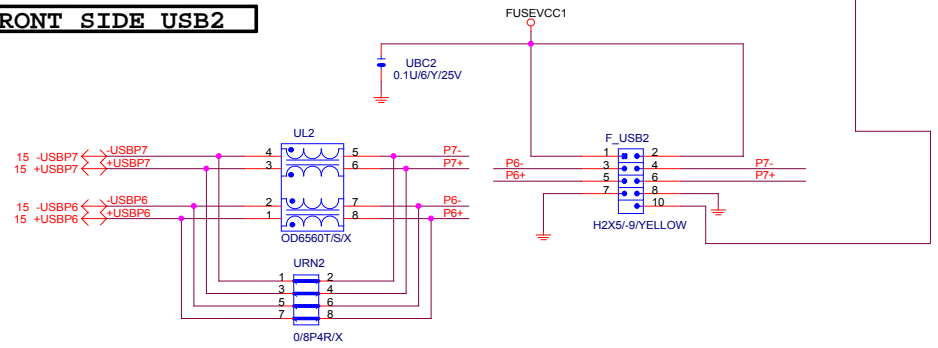
REAR USB



FRONT SIDE USB1

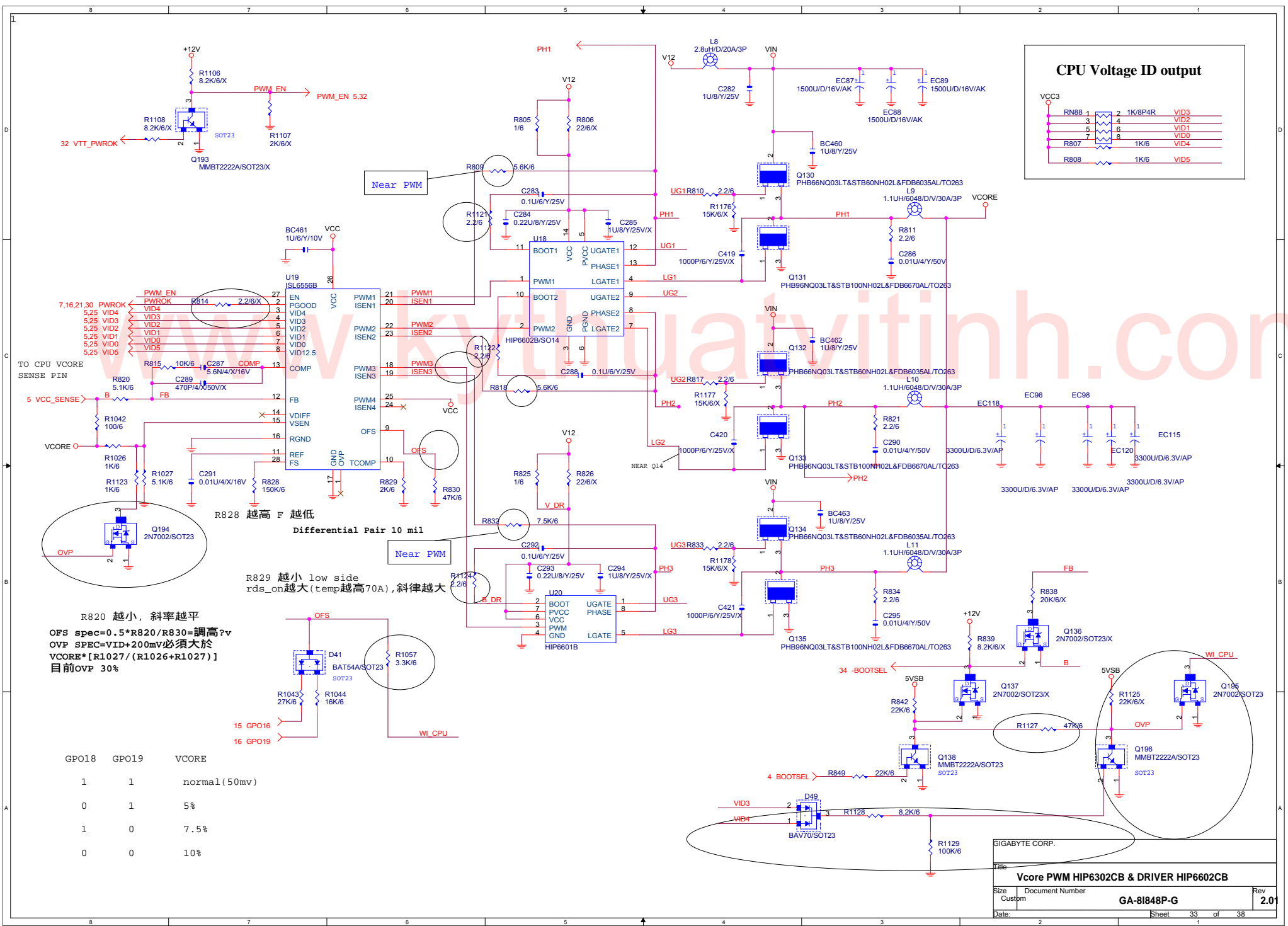
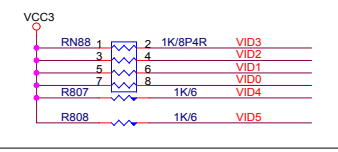


FRONT SIDE USB2



SIGABYTE CORP.		
Title: ICH USB PORT		
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CPU Voltage ID output



TO CPU VCORE SENSE PIN
 5 VCC_SENSE
 7.16, 21.30 PWROK
 5.25 VID4
 5.25 VID3
 5.25 VID2
 5.25 VID1
 5.25 VID0
 5.25 VID5

R828 越高 F 越低

Differential Pair 10 mil

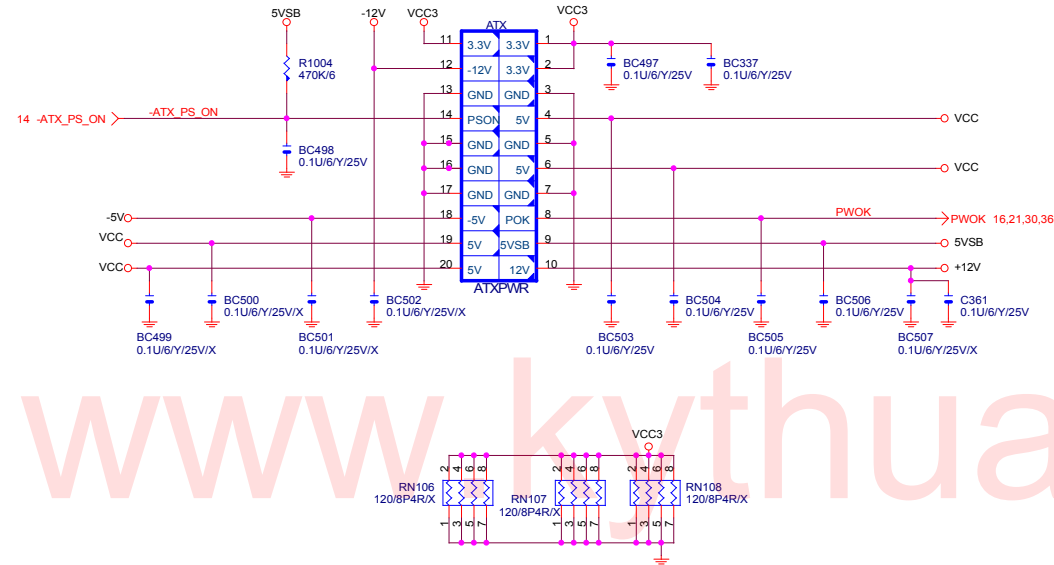
R829 越小 low side
 rds_on 越大 (temp 越高 70A), 斜率越大

R820 越小, 斜率越平

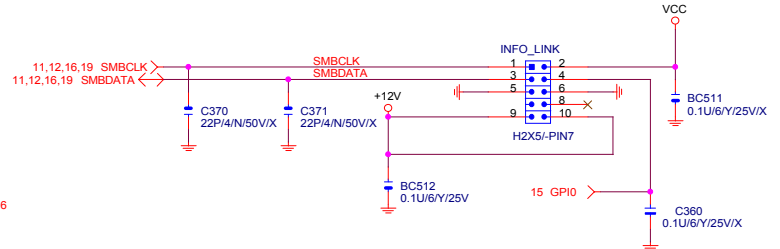
OFS spec = $0.5 * R820 / R830 = \text{調高 } \nu$
 OVP SPEC = VID + 200mV 必須大於
 VCORE * [R1027 / (R1026 + R1027)]
 目前 OVP 30%

GPO18	GPO19	VCORE
1	1	normal (50mv)
0	1	5%
1	0	7.5%
0	0	10%

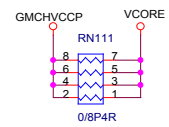
ATX POWER CONNECTOR



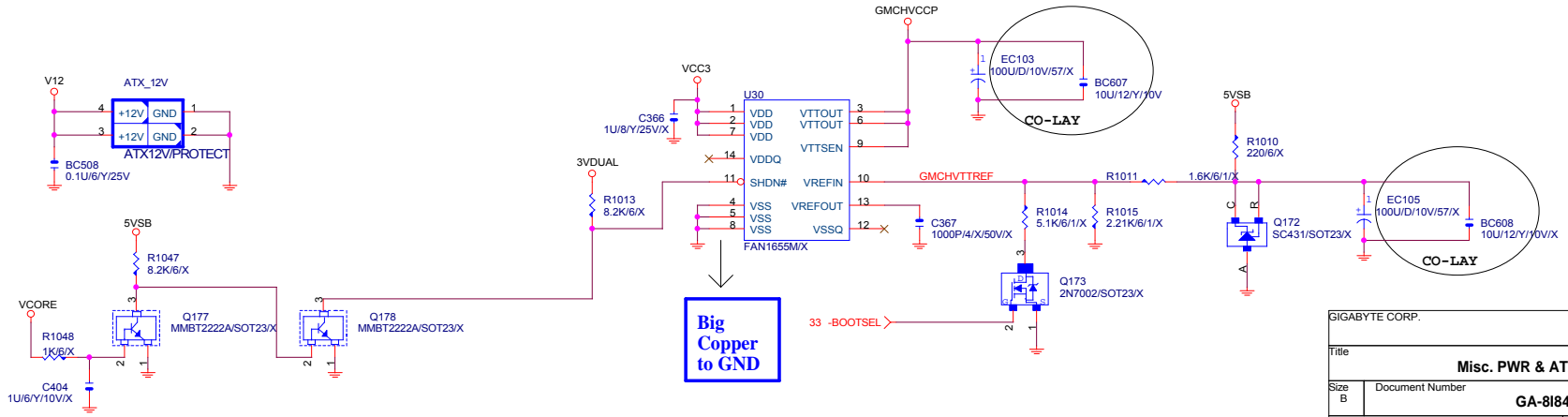
SMBUS CONN.



www.kythuatinh.com



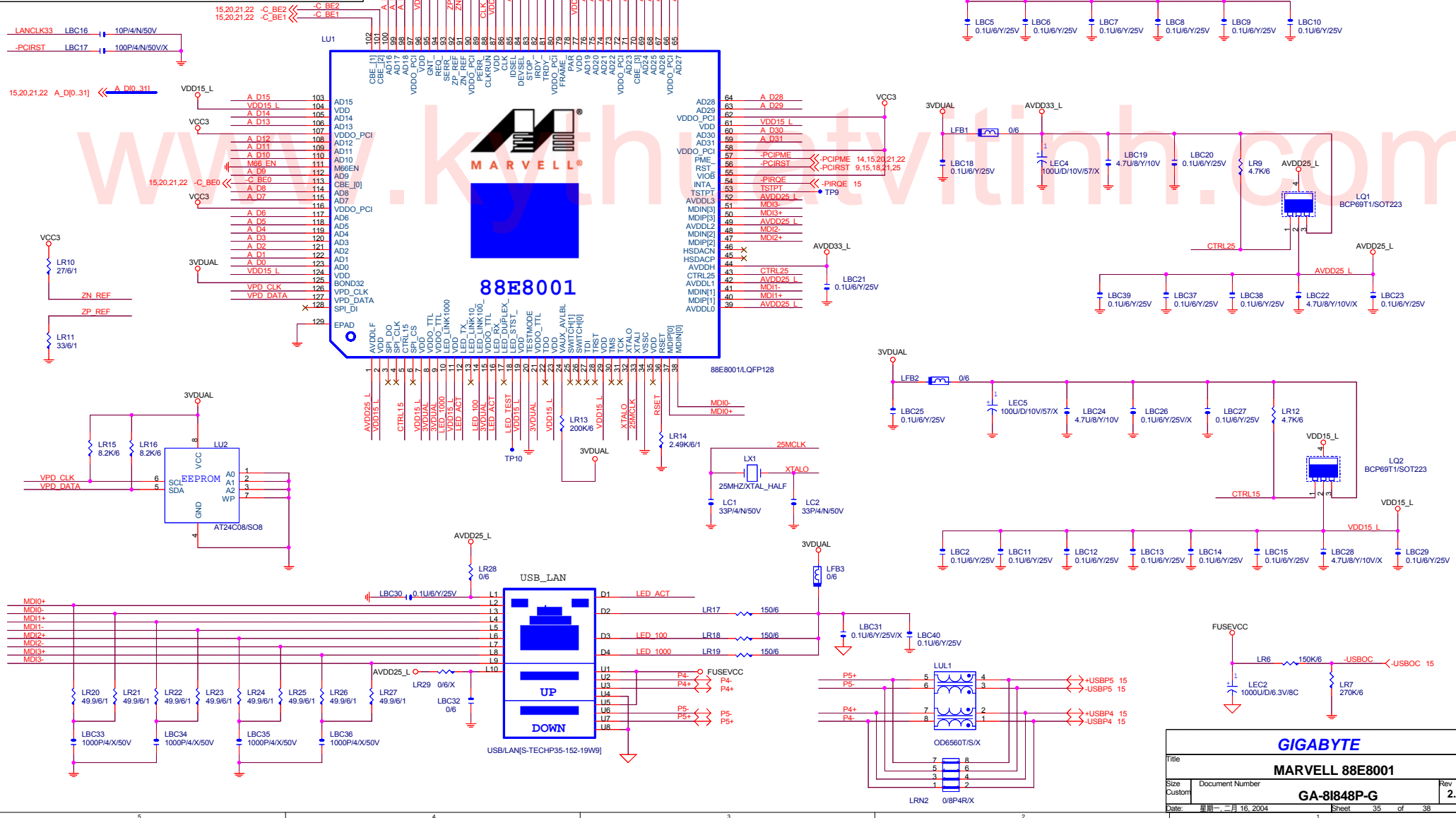
Northwood:+1.45V
Prescott:+1.225V



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GIGABYTE CORP.		
Title Misc. PWR & ATX CONN.		
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Layout Check 注意事項

1. LU1 PIN129 需下內層GND,打 12 VIA
2. 3VDUAL, VCC3, VDD15_L, AVDD25_L 至少走20mil寬,並且電容擺設每兩pin至少放一顆Bypass Cap.
3. X'TAL 25MHz 兩訊號線,TRACE 愈短愈好,線寬12mil
4. MDI正負0~3,TRACE 8:7:8, 每對之間保持 40mil



GIGABYTE		
MARVELL 88E8001		
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GIGABYTE GA-8I848P-G PCI ROUNTING LIST

PCI DEVICE	IDSEL	INT	CLOCK	REQ	GNT
PCI SLOT1	16	C,F,G,A	PCLK0	REQ0-	GNT0-
PCI SLOT2	17	F,G,A,C	PCLK1	REQ1-	GNT1-
PCI SLOT3	18	G,A,C,F	PCLK2	REQ2-	GNT2-
PCI SLOT4	19	A,C,F,G	PCLK3	REQ3-	GNT3-
PCI SLOT5	20	C,F,G,A	PCLK4	REQ4-	GNT4-
LAN (Marvell)	25	E	LANCLK33	-REQ5 (REQB#)	-GNT5 (GNTB#)

GIGABYTE CORP.

Title			PCI ROUNT LIST
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GIGABYTE GA-8I848P-G GPIO LIST

SHEET

TITLE

GPIIP	I/O	FUNCTION
GPI0/REQA-	I	PULL HIGH 8.2K to VCC3, SMB connector.
GPI1/REQ5-		PULL HIGH 8.2K to VCC, REQ5-.
GPI2/PIRQE-		PULL HIGH 8.2K to VCC3, PIRQE-.
GPI3/PIRQF-		PULL HIGH 8.2K to VCC3, PIRQF-.
GPI4/PIRQG-		PULL HIGH 8.2K to VCC, PIRQG-.
GPI5/PIRQH-	NA	PULL HIGH 8.2K to VCC
GPI6/AGPBUSY-	I	PULL 8.2K TO VCC3, PANEL GREEN_BUTTON
GPI7	I	DUAL BIOS FIRST BOOT SELECT.
GPI8	I	PULL 8.2K TO 3VDUAL, -CASPME.
GPI9/OC4-	NA	USB OC4-.
GPI10/OC5-	NA	USB OC5-.
GPI11/-SMBALRT	NA	PULL 8.2K TO 3VDUAL,-SMBALERT.
GPI12	I	PULL 8.2K TO VCC3,M/B REVERSION ID.
GPI13	I	LPC PME.
GPI14/OC6-	NA	USB OC6-.
GPI15/OC7-	NA	USB OC7-.
GPO16/GNTA-	NA	GPO16.
GPO17/GNT5-		GNT5-.
GPO18/STP_PCI-	NA	GPO18.
GPO19/SLP_S1-	O	DUAL BIOS.
GPO20/SLP_CPU-	O	DUAL BIOS.
GPO21/C3_SATA-	O	BLOCK TOP TABLE.
GPO22/CPUPERF-	O	PULL 8.2K TO VCC3,PANEL S3 POWER LED.

SHEET

TITLE

GPIIP	I/O	FUNCTION
GPO16		PULL 8.2K TO VCC3
GPO17		PULL 8.2K TO VCC3 (GNT5-)
GPO18		PULL 8.2K TO VCC3
GPO19		PULL 8.2K TO VCC3
GPO20		PULL 8.2K TO VCC3
GPO21		PULL 8.2K TO VCC3
GPO22		PULL 8.2K TO VCC3
GPO23		PULL 8.2K TO VCC3
GPO24		PULL 1K TO 3VDUAL (TOP BLOCK)
GPO25		PULL 4.7K TO 3VDUAL, LAN 100/10 DETECT.
GPO26		NOT IMPLEMENTED
GPO27		PULL 8.2K TO 3VDUAL, BIOS WRITE PROTECT.
GPO28		PULL 8.2K TO 3VDUAL

GIGABYTE CORP.

Title			GPIO LIST		
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