

Cover Sheet	1
Block Diagram	2
GPIO Spec.	3
Clock CY28324 & ATA100 IDE CONNECTORS	4
mPGA478-B INTEL CPU Sockets	5 - 6
INTEL Brookdale MCH -- North Bridge	7 - 8
INTEL ICH2 -- South Bridge	9 - 10
LPC I/O W83627HF	11
CNR RISER	12
AC'97 Codec	13
Audio Amp TL072 & GAME	14
FWH-- BIOS & VCCVID	15
SDR DIMM-168PIN DIMM1,2	16
AGP 4X SLOT (1.5V)	17
PCI SLOT 1 & 2 & 3	18
Front Panel & Connectors	19
USB & FAN Connectors	20
D-LED & AUDIO 6 CHANNEL CONTROL	21
Voltage Regulator	22
HIP6301V CPU Power (PWM)-VRM9.2	23
IO Connectors	24
Realtek RTL8100(L) LAN	25
DDR Damping	26
DDR Termination	27
DDR Termination Power	28
Jumper setting	29
Power Delivery Map	30

MS-6507

Version 0B
06/29/2001 Update

INTEL (R) Brookdale Chipset
Willamette/Northwood 478pin mPGA-B Processor Schematics

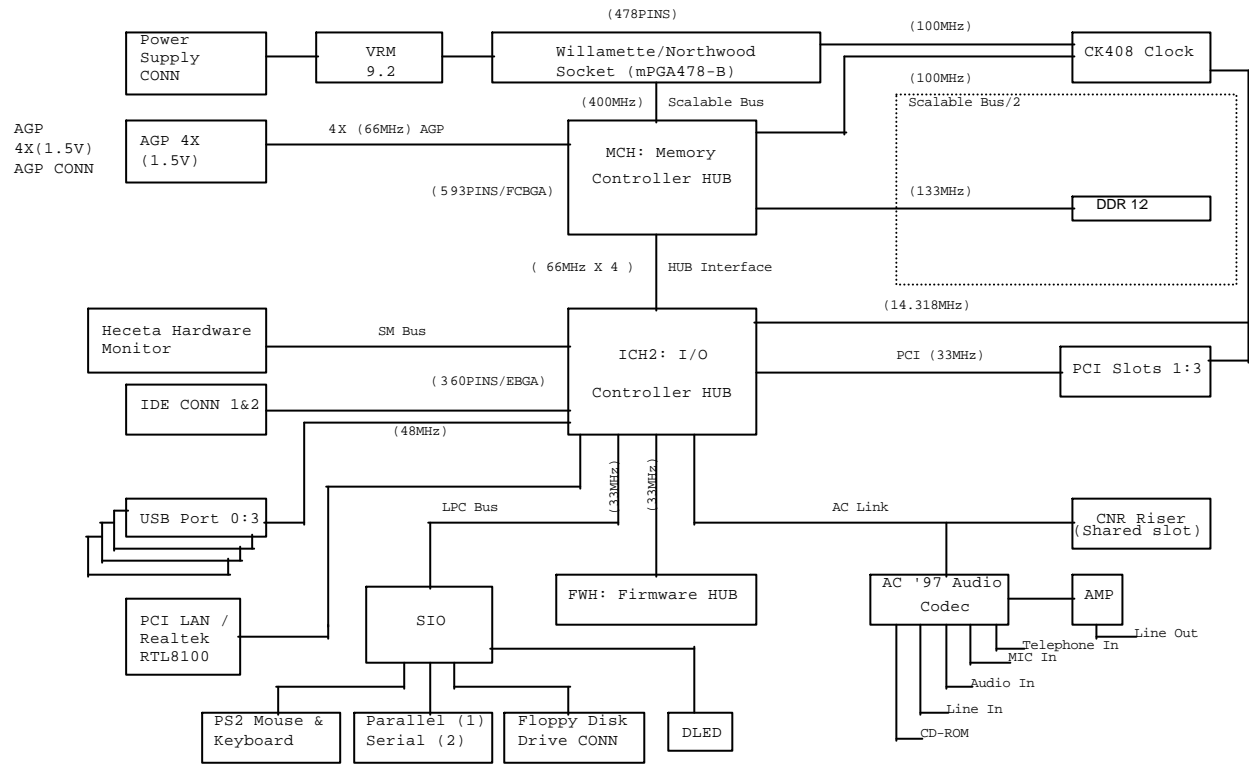
CPU:
Willamette/Northwood mPGA-478B Processor

System Brookdale Chipset:
INTEL MCH (North Bridge) +
INTEL ICH2 (South Bridge)

On Board Chipset:
BIOS -- FWH
LPC Super I/O -- W83627HF
Clock Generation -- CY28324
PCI SOUND -- C-MEDIA CMI8738

Expansion Slots:
AGP2.0 SLOT * 1
PCI2.2 SLOT * 3

Micro-Star	Title MS-6507	Rev 0B
Document Number Cover Sheet		
Last Revision Date: Monday, July 23, 2001		Sheet 1 of 36



Micro-Star	Title MS-6507	Rev 0B
Document Number		Block Diagram
Last Revision Date: Monday, July 23, 2001		Sheet 2 of 36

General Purpose I/O Spec.

ICH2

GPIO Pin	Type	Function
GPIO 0	I	Non Connect
GPIO 1	I	Non Connect
GPIO 2~4	I	Not Implemented
GPIO 5	I	Non Connect
GPIO 6	I	AC97 Enabled/Disabled
GPIO 7	I	None
GPIO 8	I	LAN Wake Up
GPIO 9	I	AC'97 Serial Data In
GPIO 10	I	Non Connect
GPIO 11	I	Non Connect
GPIO 12	I	External SMI
GPIO 13	I	LPC PME
GPIO 14~15	I	Not Implemented
GPIO 16	O	Non Connect
GPIO 17	O	Non Connect
GPIO 18	O	Not Implemented
GPIO 19	O	Not Implemented
GPIO 20	O	Not Implemented
GPIO 21	O	Audio 6 channel control
GPIO 22	O	Non
GPIO 23	OD	BIOS Locked/Unlocked
GPIO 24	O	Non
GPIO 25	O	Non
GPIO 26	O	Non
GPIO 27	I/O	Non
GPIO 28	I/O	non
GPIO 29~31	I/O	Not Implemented

FWH

GPIO Pin	Type	Function
GPI 0	I	ATA IDE 1 Detect
GPI 1	I	ATA IDE 2 Detect
GPI 2	I	Reserved
GPI 3	I	Reserved

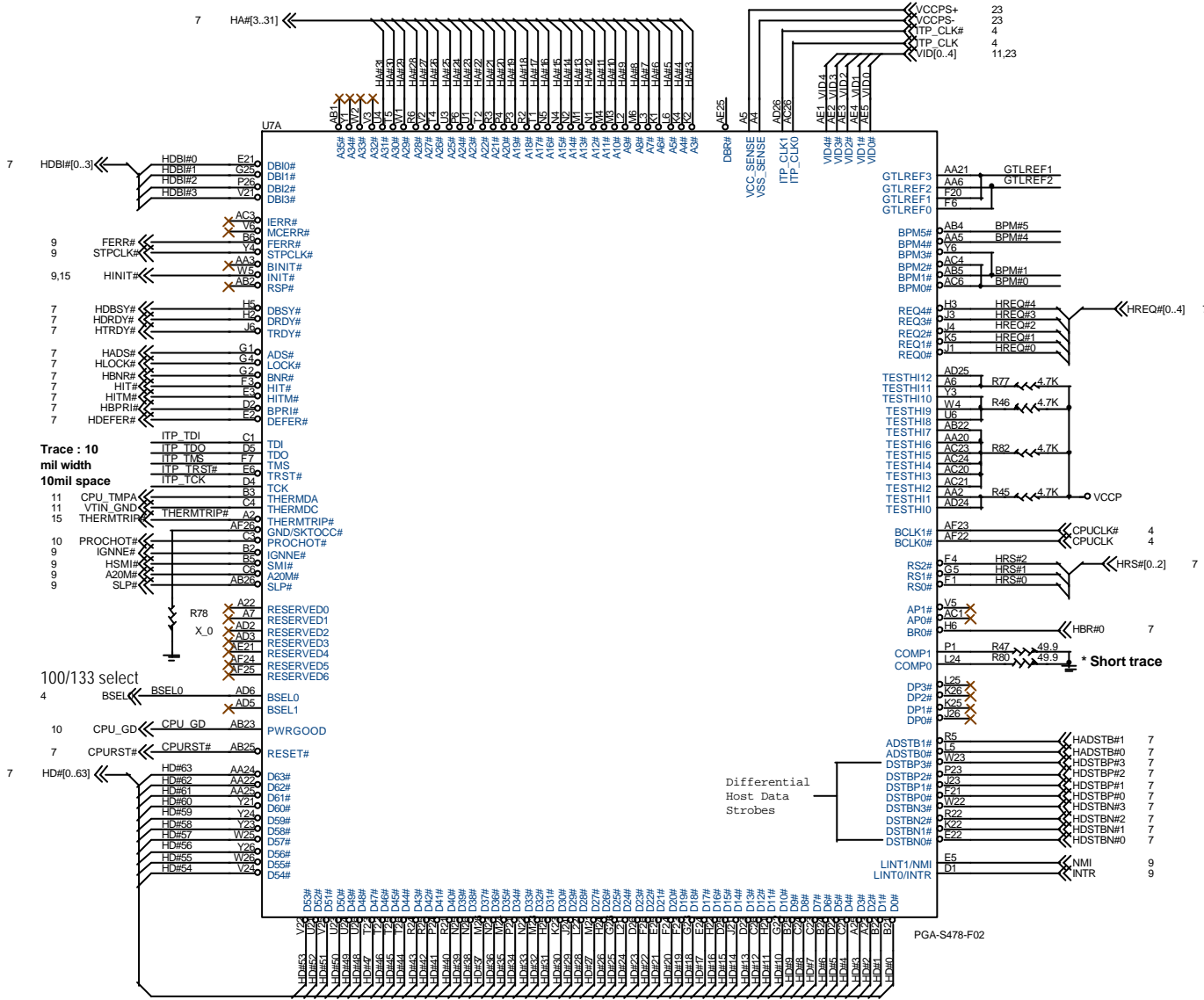
DLED-Super I/O

GPIO Pin	Type	Function
GP32	I/OD	DLED1
GP24	I/OD	DLED2
GP34	I/OD	DLED3
GP33	I/OD	DLED4

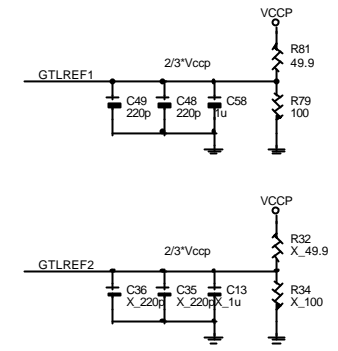
DEVICE	ICH INT Pin	IDSEL
PCI Slot 1	INTA# INTB# INTC# INTD#	AD16
PCI Slot 2	INTB# INTC# INTD# INTA#	AD17
PCI Slot 3	INTC# INTD# INTA# INTB#	AD18
PCI Audio	INTD#/INTE# INTA# INTB# INTC#	AD23
PCI Lan	INTC#/INTF# INTD# INTA# INTB#	AD22

Micro-Star	Title MS-6507	Rev 0B
Document Number GPIO Spec.		
Last Revision Date: Monday, July 23, 2001		Sheet 3 of 36

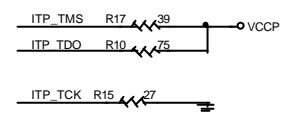
CPU SIGNAL BLOCK



CPU GTL REFERENCE VOLTAGE BLOCK

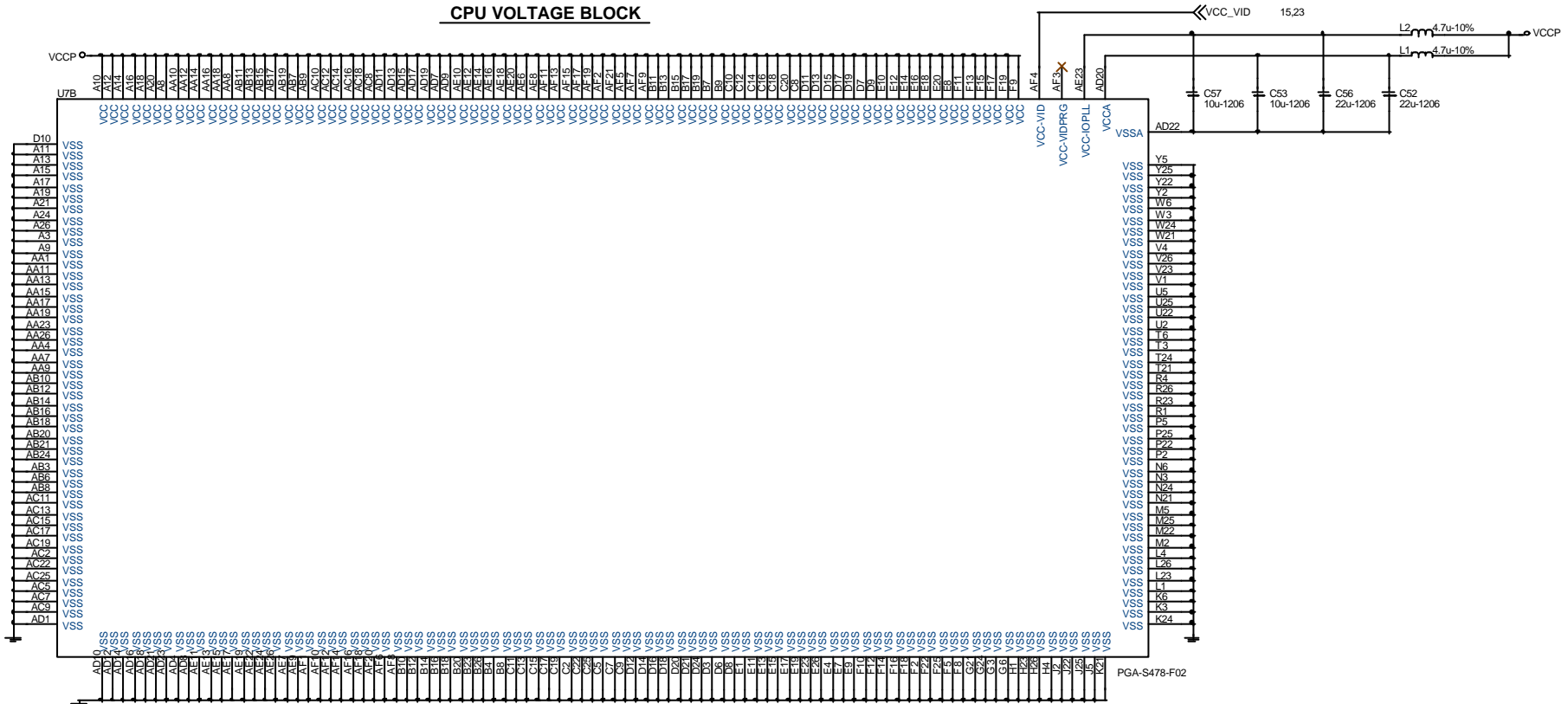


CPU ITP BLOCK

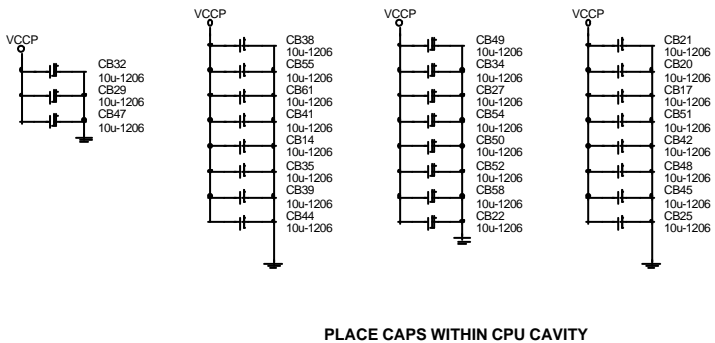


Micro-Star	Title MS-6507	Rev 0B
Document Number INTEL mPGA478-B CPU1		
Last Revision Date: Thursday, August 09, 2001		Sheet 5 of 36

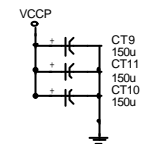
CPU VOLTAGE BLOCK



CPU DECOUPLING CAPACITORS



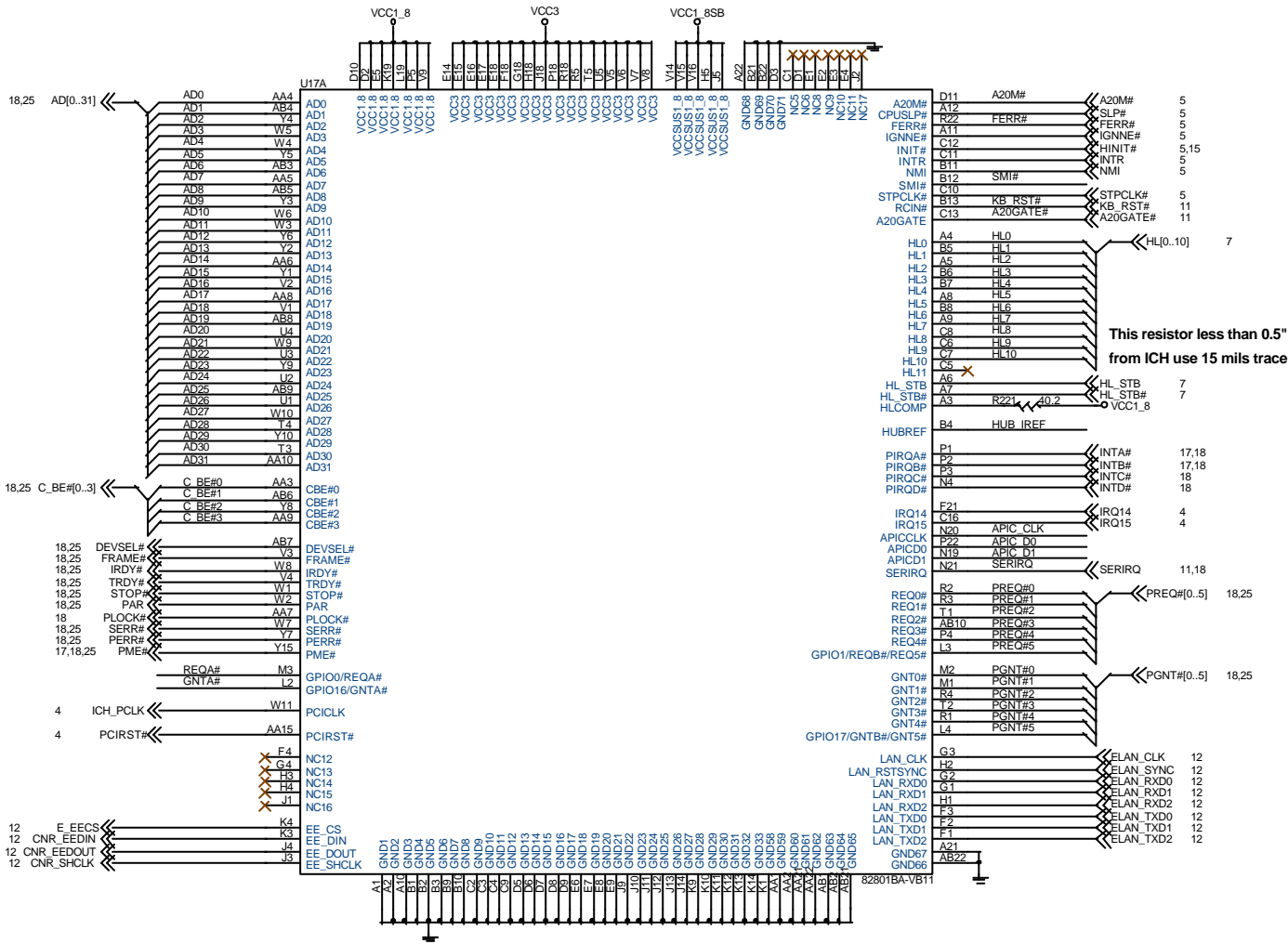
CPU DECOUPLING CAPACITORS



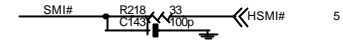
PLACE CAPS WITHIN CPU CAVITY SOLDER

Micro-Star	Title MS-6507	Rev 0B
Document Number INTEL mPGA478-B CPU2		
Last Revision Date: Monday, September 03, 2001		Sheet 6 of 36

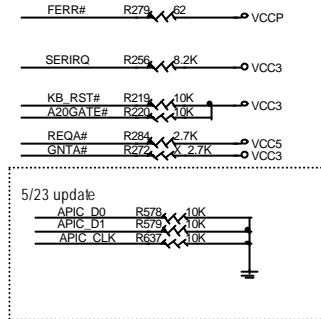
ICH2 PCI / HUB LINK / CPU / LAN / INTERRUPT SIGNALS



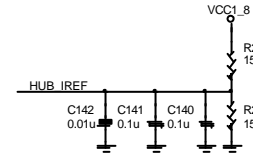
ICH2 SMI# SIGNAL



ICH2 STRAPPING RESISTORS

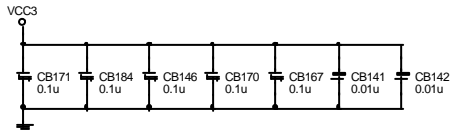


ICH2 REFERENCE VOLTAGE

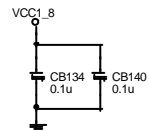


Place Cap. as Close as possible to ICH2
Trace width use 15 mils and 15mils space

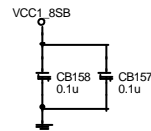
ICH2 DECOUPLING CAPACITORS



Place one 0.1U/0.01U pair in each corner and
2 on opposite sides close to ICH2 if it fit



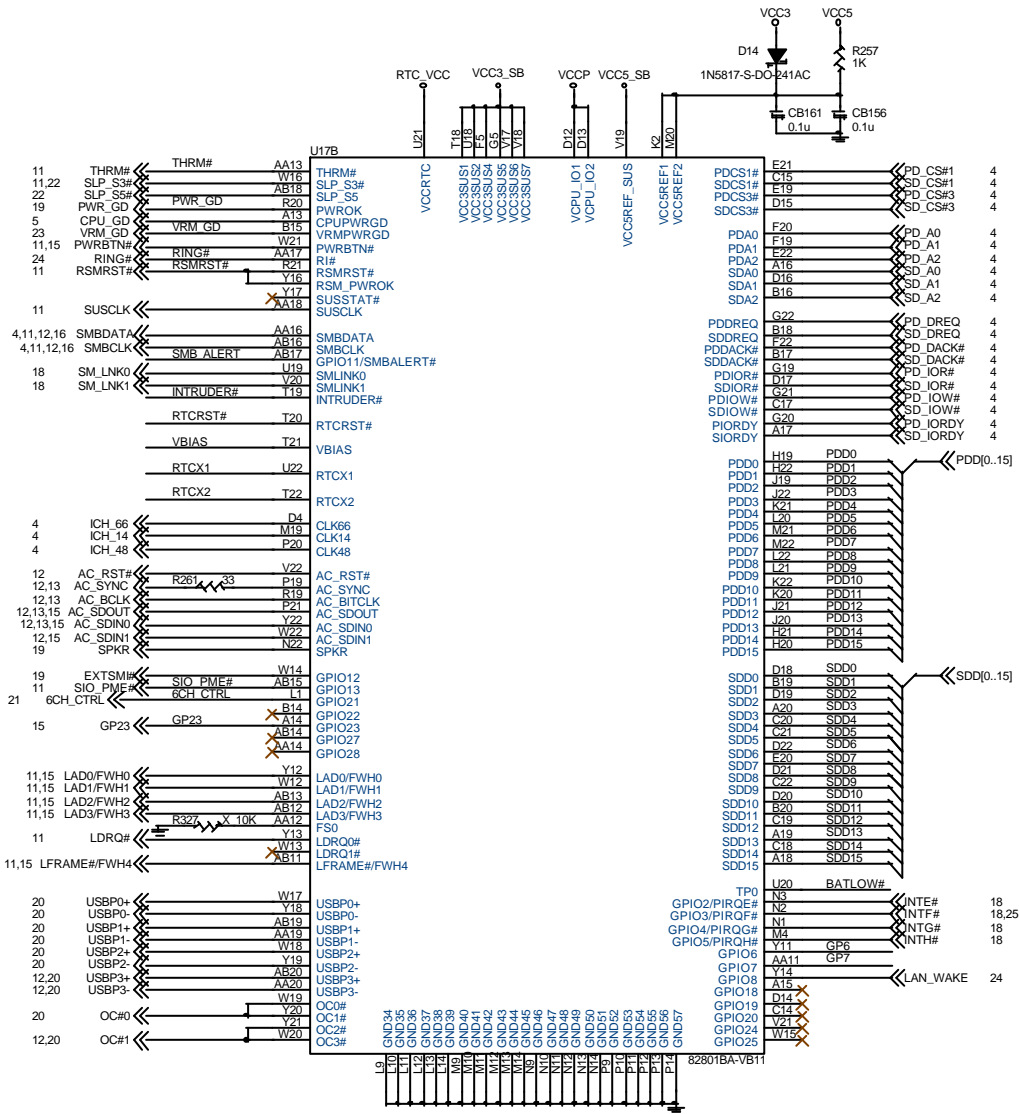
Distribute near the 1.8V
power pin of the ICH2



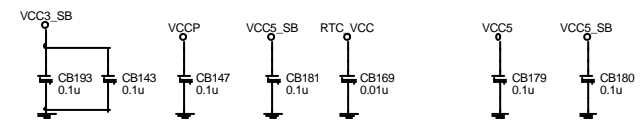
Distribute near the VCC1_8SB
Power pin of the ICH2

Micro-Star	Title MS-6507	Rev 0B
Document Number Brookdale ICH2 PCI		
Last Revision Date: Tuesday, July 24, 2001	Sheet g of 36	

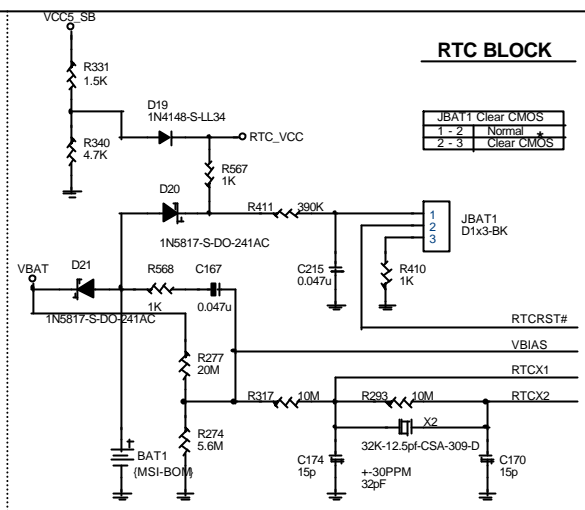
ICH2 ASIC / RTC / AC'97 / GPIO / LPC / USB / IDE SIGNALS



ICH2 DECOUPLING CAPACITOR

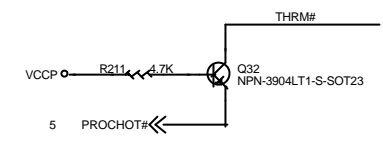


RTC BLOCK

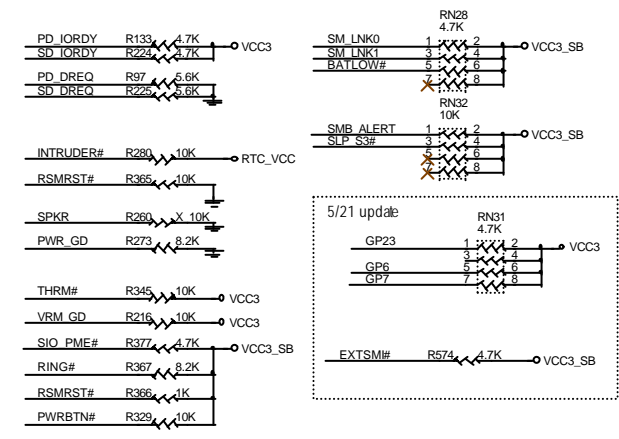


JBAT1 Clear CMOS	
1 - 2	Normal
2 - 3	Clear CMOS

PROCHOT BLOCK

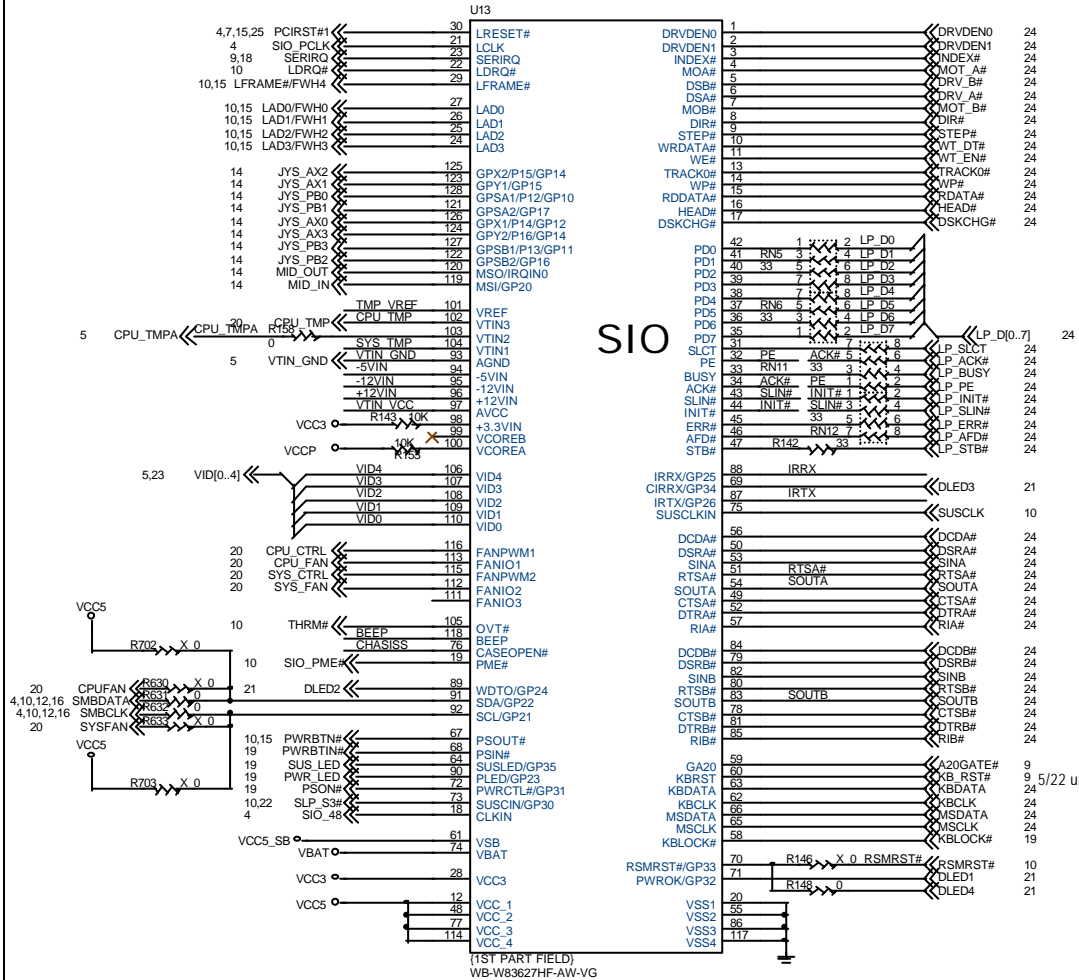


ICH2 STRAPPING RESISTORS

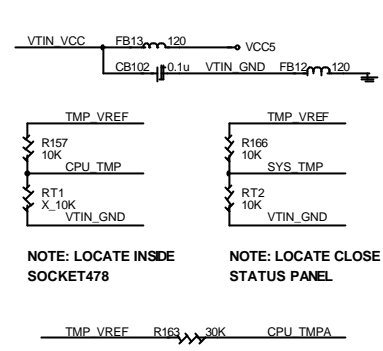


Micro-Star	Title	Rev
	MS-6507	0B
Document Number: Brookdale ICH2 Other		
Last Revision Date: Wednesday, August 29, 2001		Sheet 10 of 36

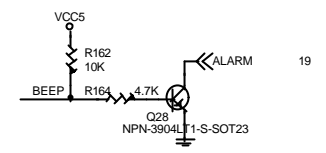
LPC SUPER I/O W83627HF



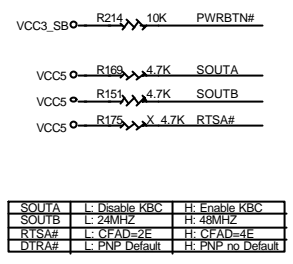
THERMAL RESISTOR BLOCK



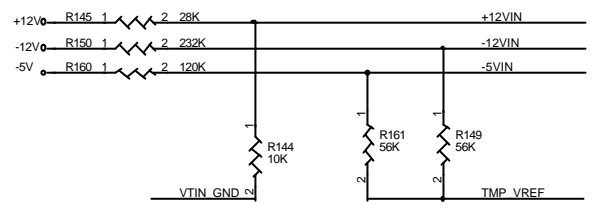
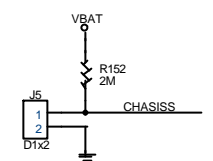
SPEAKER BLOCK



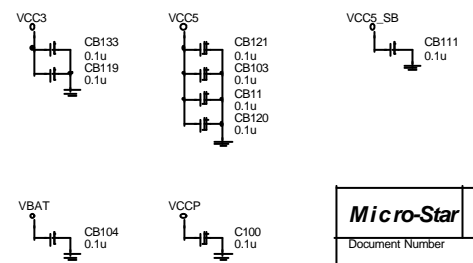
SUPER I/O STRAPPING RESISTOR



CHASSIS INTRUSION HEADER

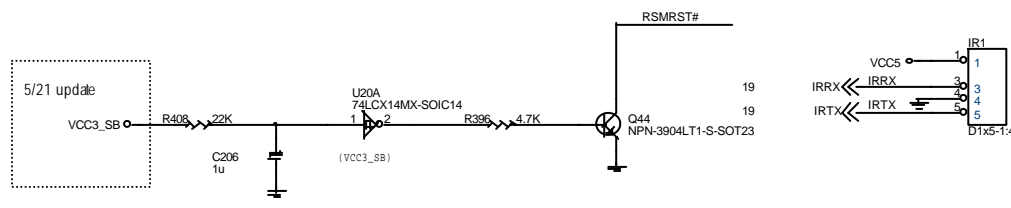


DECOUPLING CAPACITOR

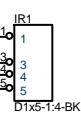


RESUME RESET CIRCUIT BLOCK

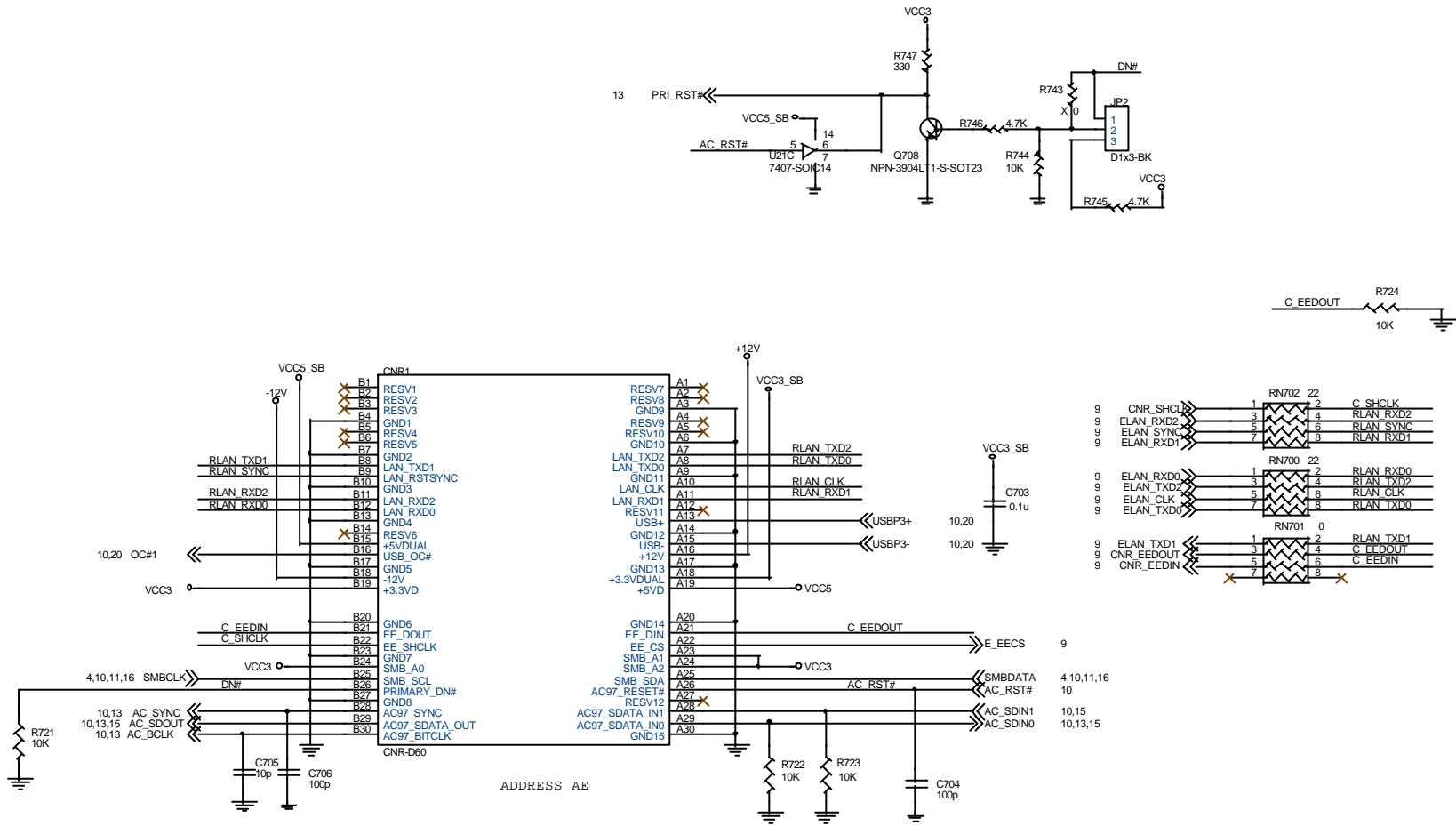
Stuff all for D Version bug



IR HEADER

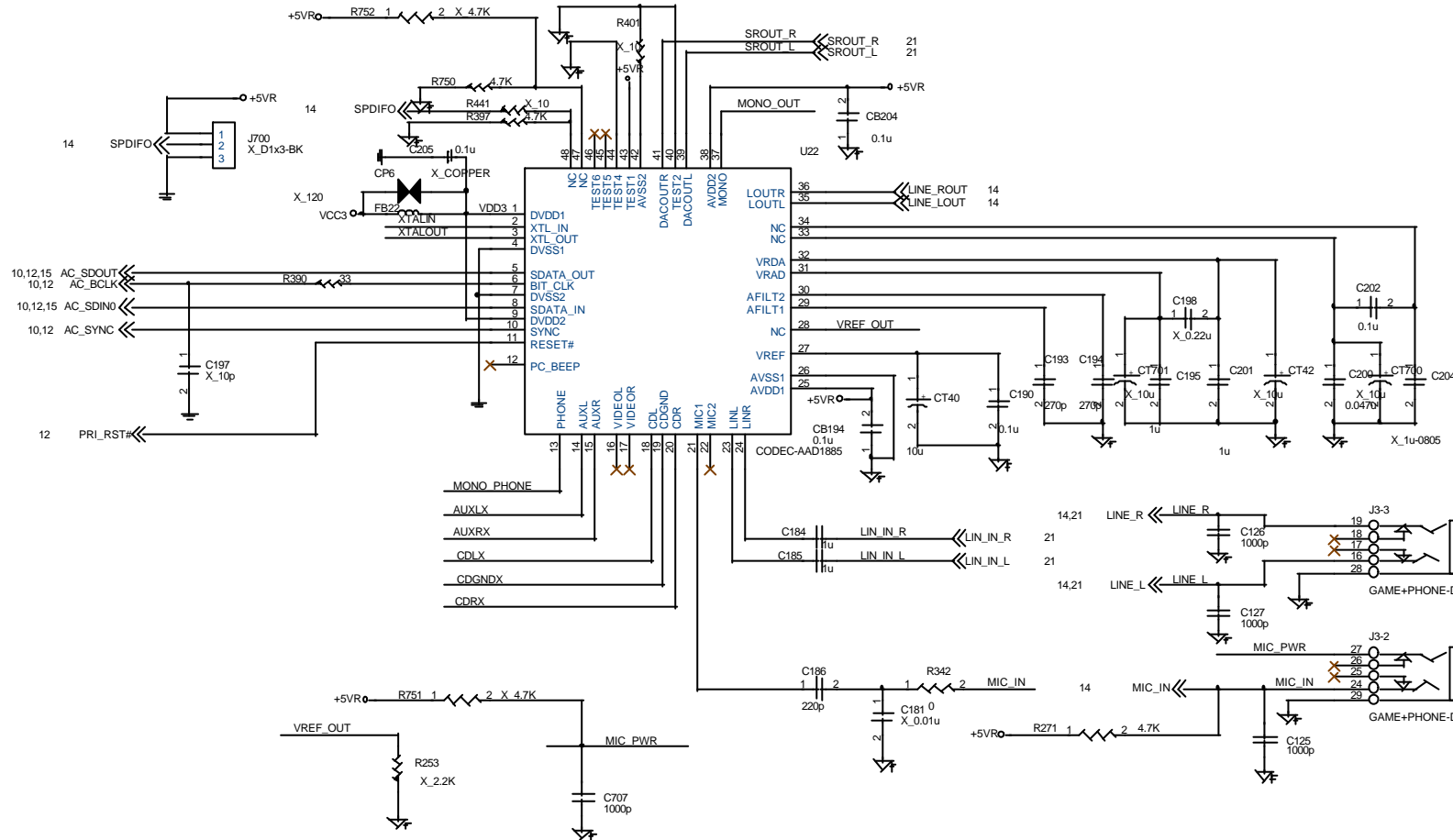


Micro-Star	Title	MS-6507	Rev
	Document Number	LPC I/O W83627HF	0B
Last Revision Date:		Wednesday, August 29, 2001	Sheet 11 of 36

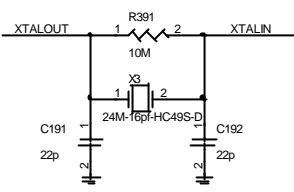


Micro-Star	Title MS-6507	Rev 0B
Document Number CNR RISER		
Last Revision Date: Thursday, August 09, 2001		Sheet 12 of 36

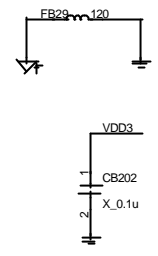
AD1885 AC97 CODEC



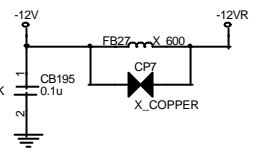
AUDIO CODE CRYSTAL CIRCUIT



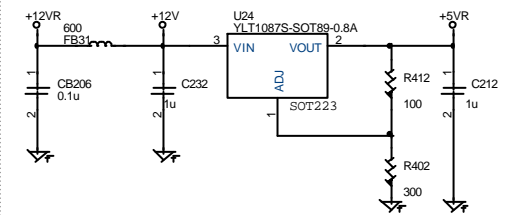
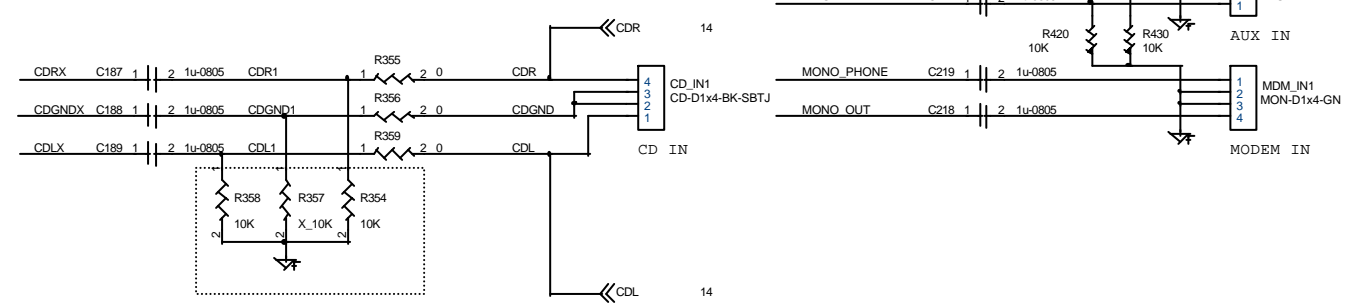
DECOUPLING CAPACITOR



AUDIO CODE REGULATORS

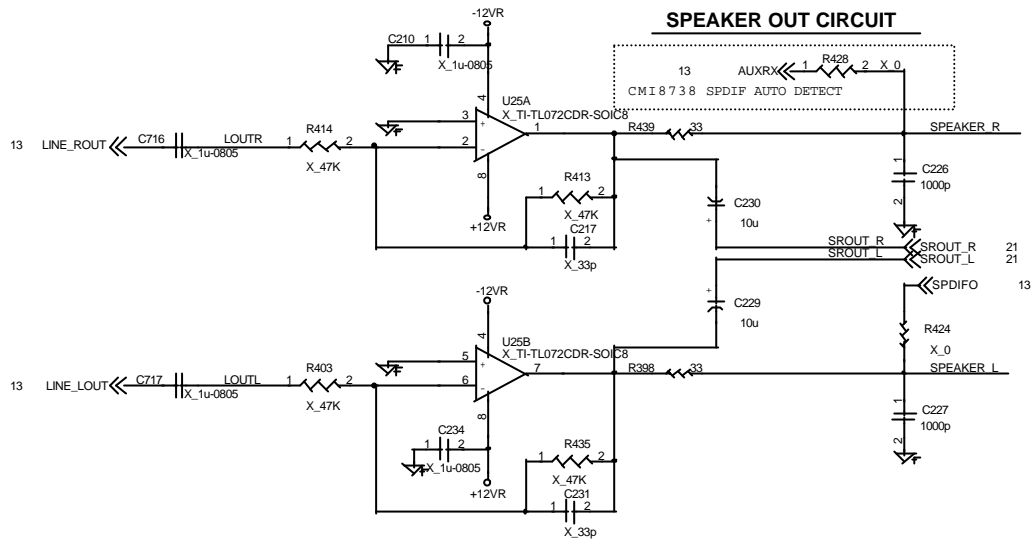


AUDIO CODE CD / AUX / MODEM IN HEADERS

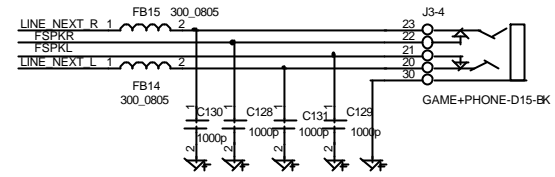


Micro-Star	Title	MS-6507	Rev	0B
Document Number		AC97 CODEC AD1885		
Last Revision Date:		Wednesday, August 29, 2001		
		Sheet	13	of 36

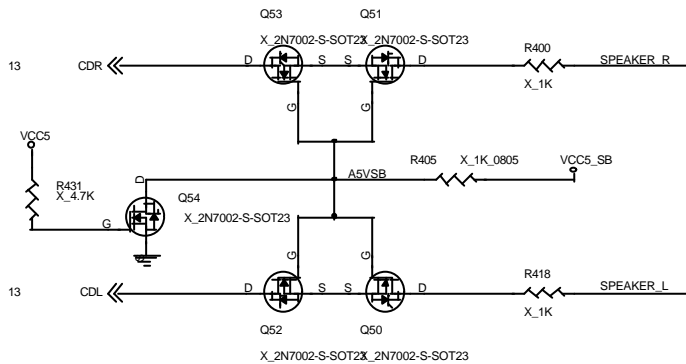
SPEAKER OUT CIRCUIT



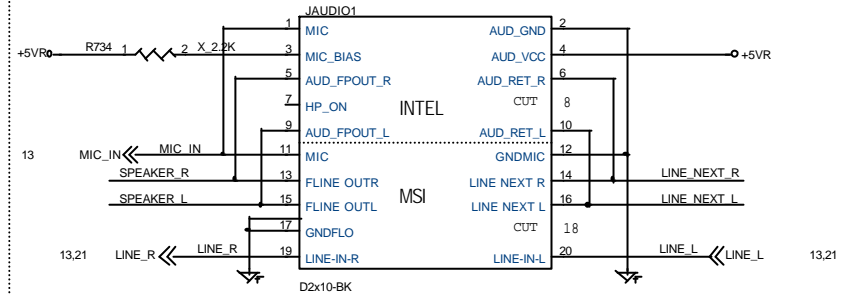
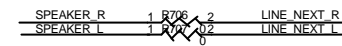
SPEAKER OUT JACK



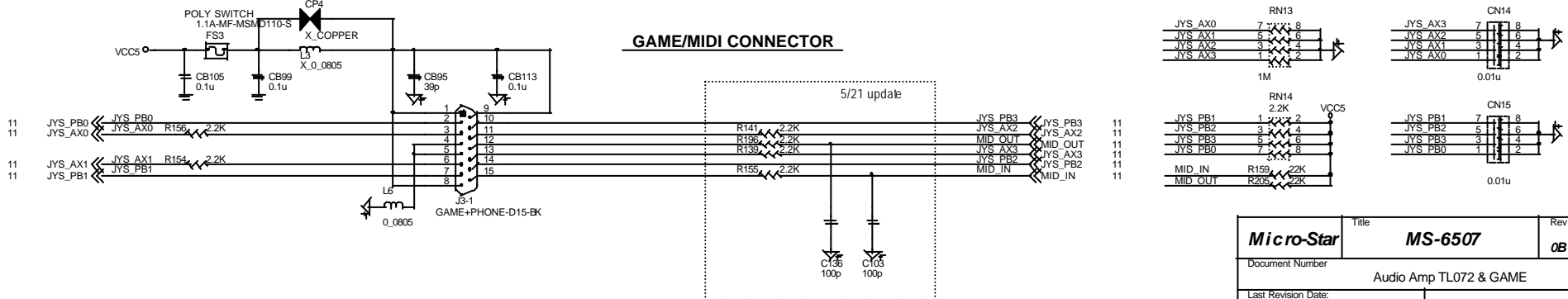
CD PANEL PLAY WITHOUT PC POWER_ON



FOR MSI INTERNAL HEADER

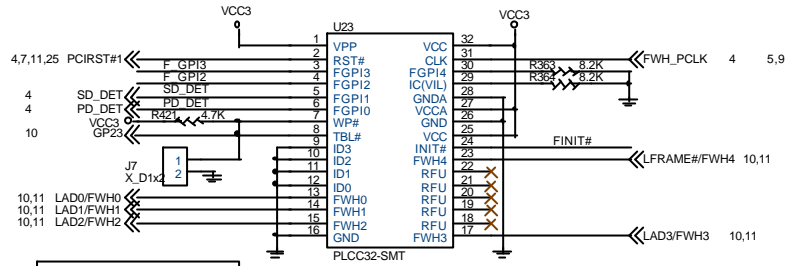


GAME/MIDI CONNECTOR



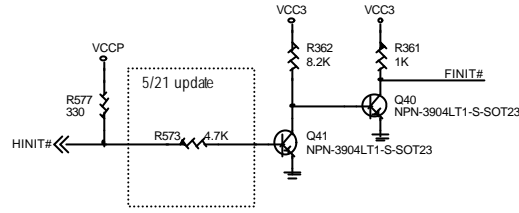
Micro-Star	Title	MS-6507	Rev	0B
Document Number		Audio Amp TL072 & GAME		
Last Revision Date:		Monday, August 06, 2001	Sheet	14 of 36

Firmware Hub (FWH)

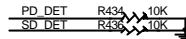


J7 BIOS Update	
SHORT	Locked
OPEN	Unlocked *

FWH INIT Signal Voltage Translation Block

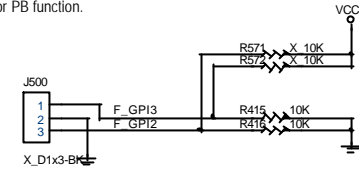


FWH RESISTORS

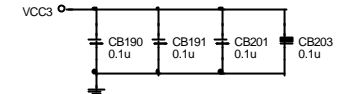


5/16 update

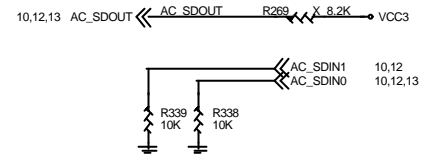
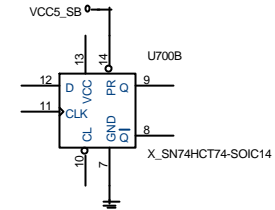
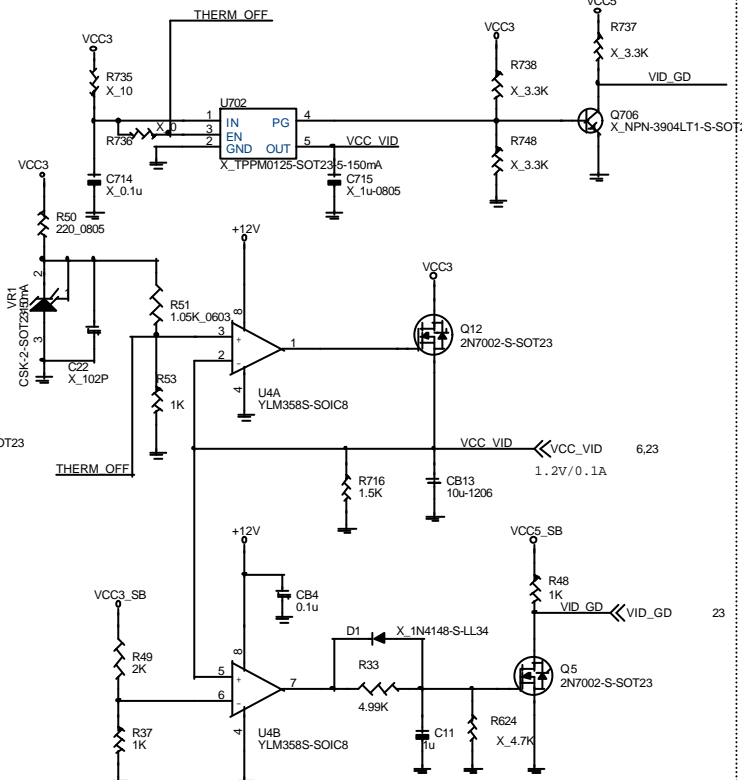
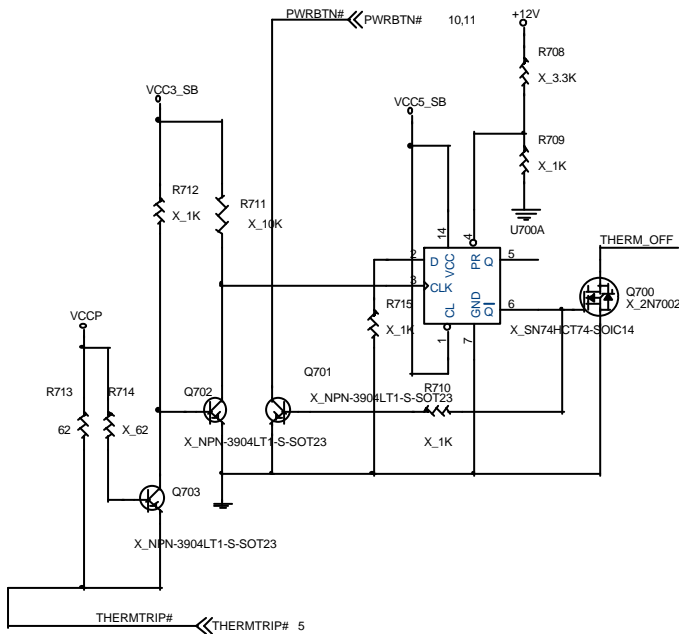
For PB function.



FWH DECOUPLING CAPACITORS

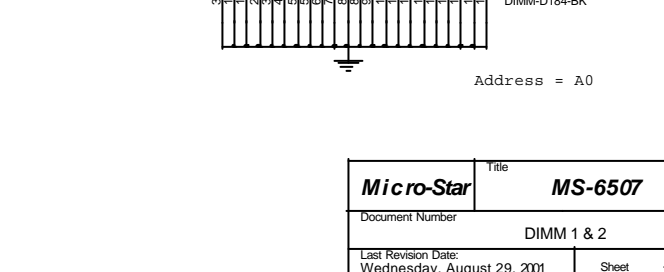
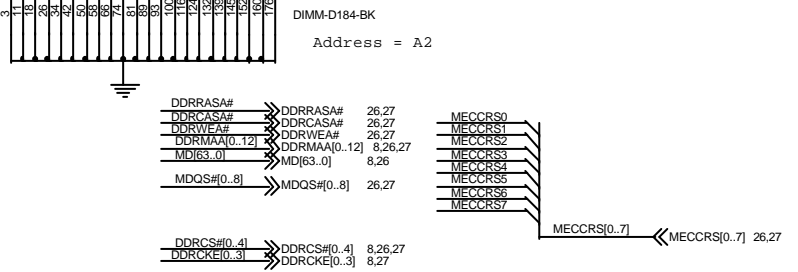
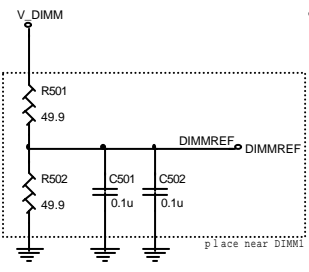
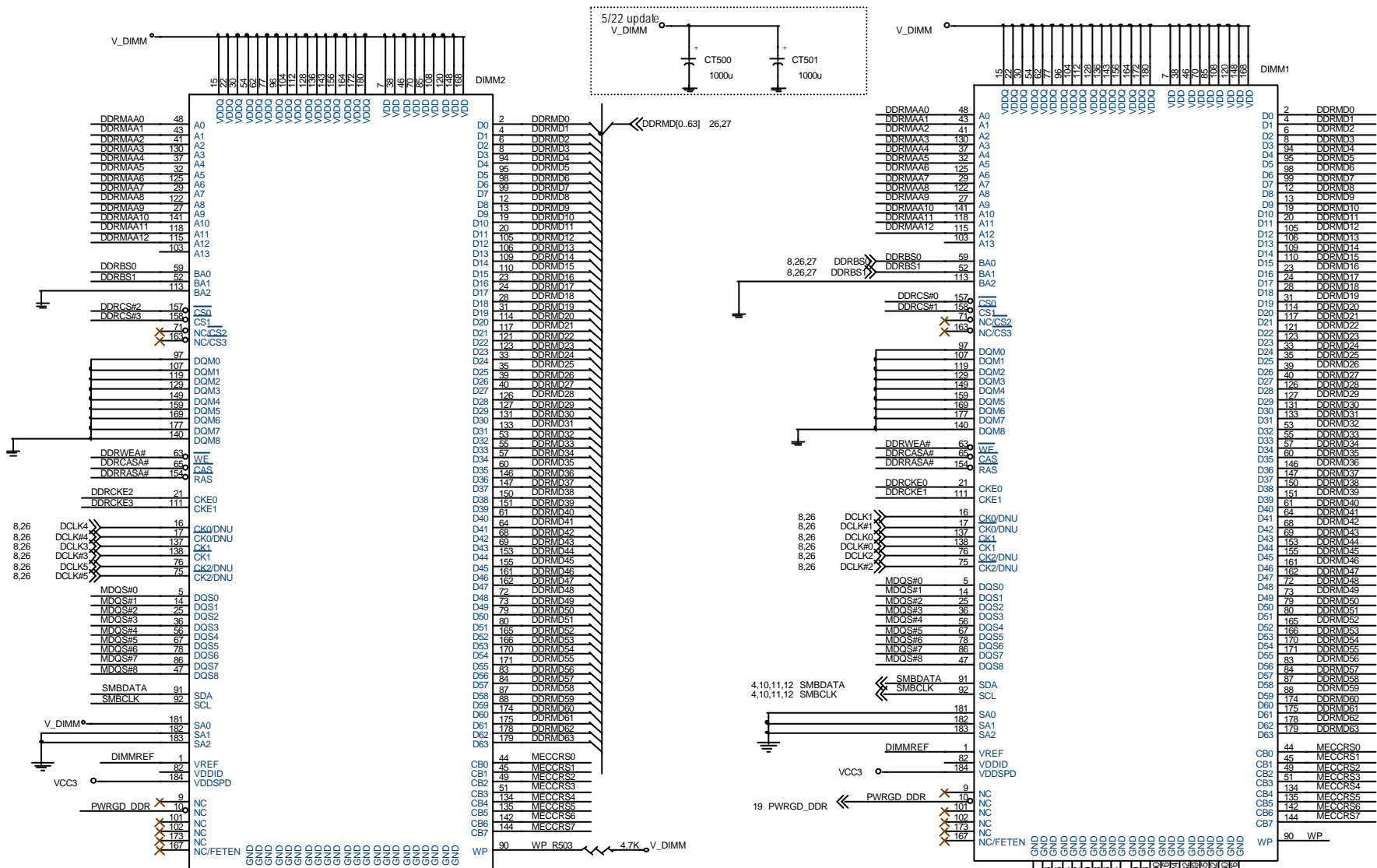


VCC_VID / VID_GOOD



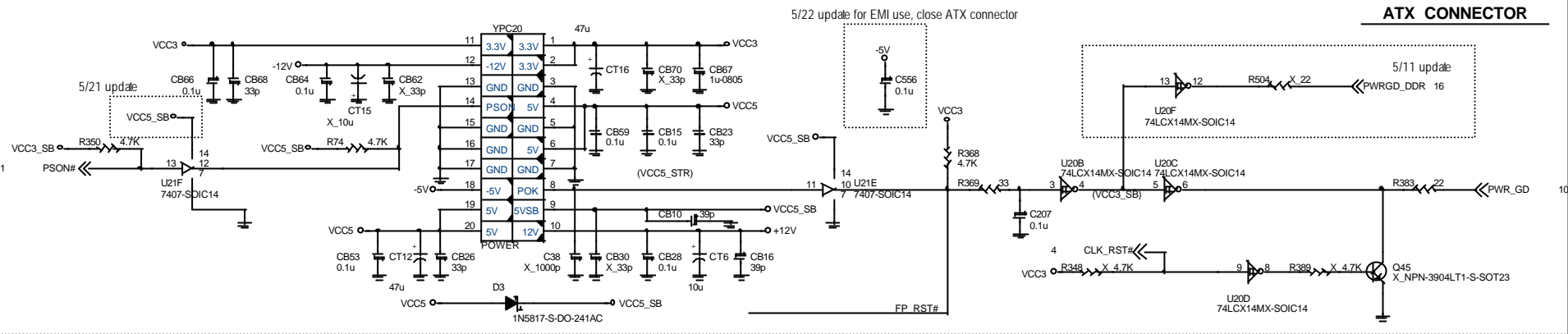
JP3	AUDIO DOWN
OPEN	Auto mode
SHORT	Disabled onboard audio codec

Micro-Star	Title MS-6507	Rev 0B
Document Number FWH & VCCVID		
Last Revision Date: Wednesday, August 29, 2001	Sheet	15 of 36

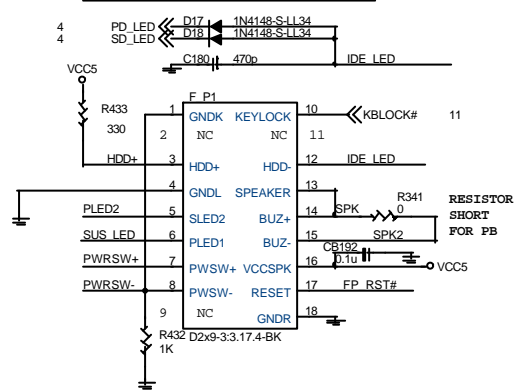


Micro-Star	Title MS-6507	Rev 0B
Document Number DIMM 1 & 2		
Last Revision Date: Wednesday, August 29, 2001		Sheet 16 of 36

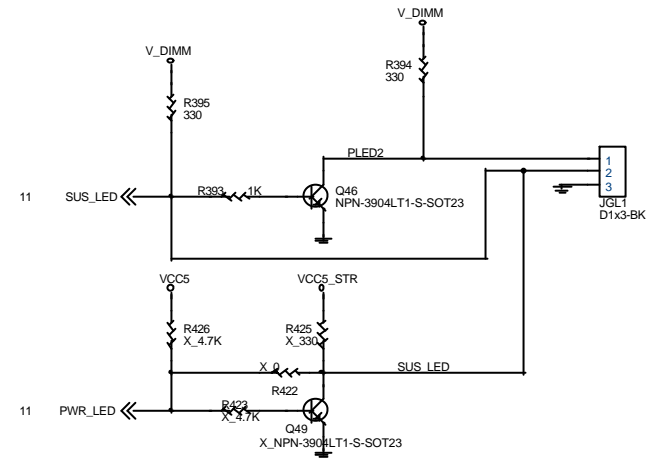
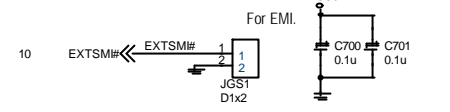
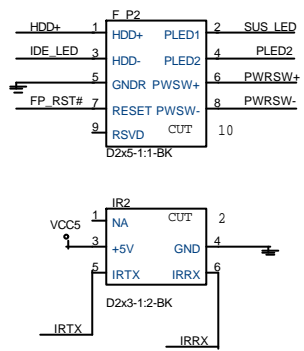
ATX CONNECTOR



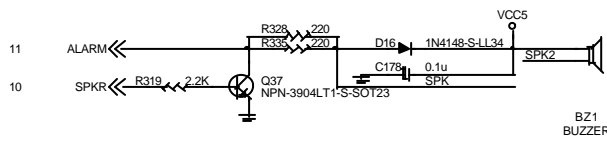
Brookdale FRONT PANEL-M



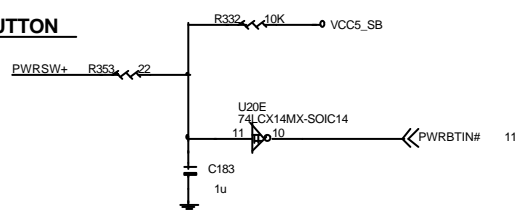
INTEL FRONT PANNEL PIN HEADER.



SPEAKER

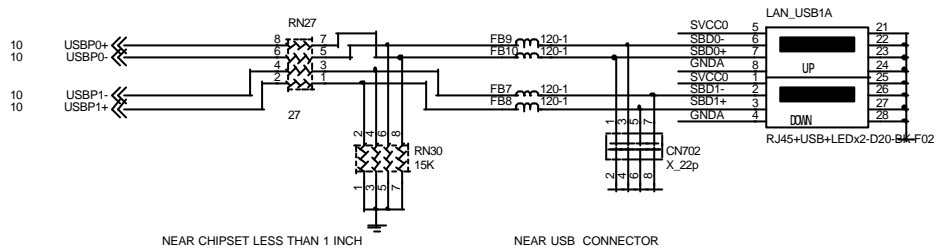


POWER BUTTON

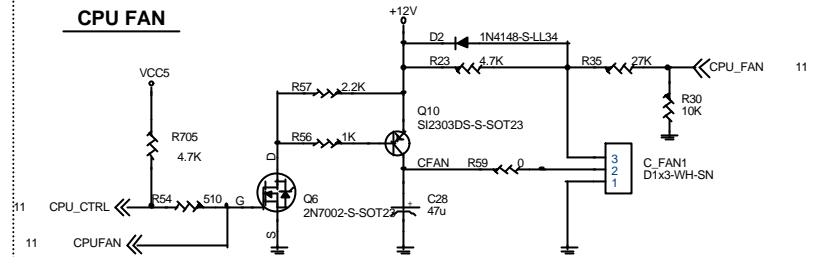


Micro-Star	Title	MS-6507	Rev
Document Number	Front Panel & Connector		0B
Last Revision Date:	Wednesday, August 29, 2001	Sheet	19 of 36

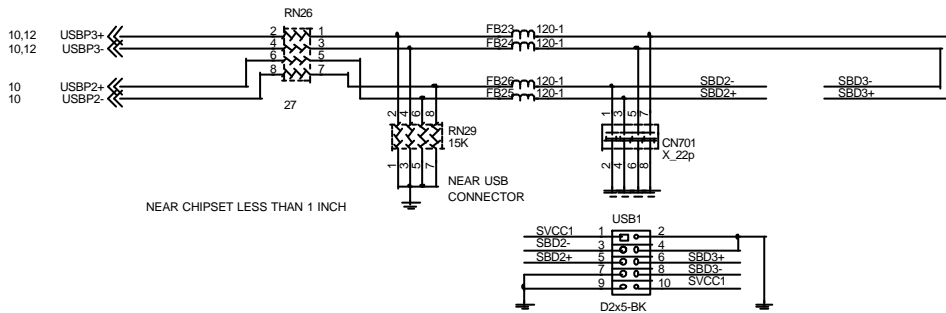
BACK PANEL USB CONNECTOR FOR USB PORT 0,1



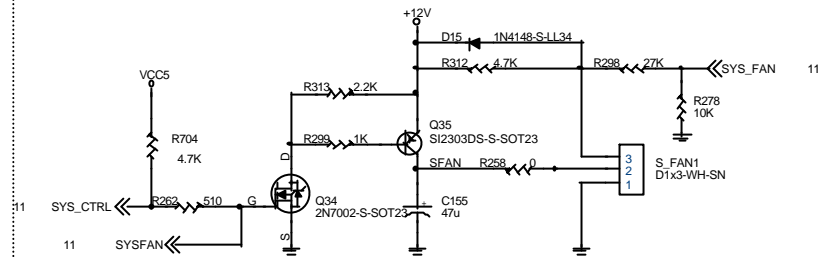
CPU FAN



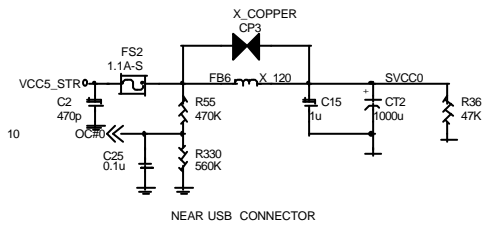
FRONT PANEL USB CONNECTOR FOR USB PORT 2,3



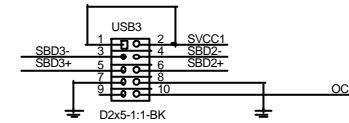
SYSTEM FAN



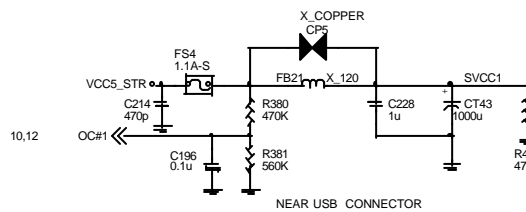
POWER CIRCUIT FOR USB PORT 0,1



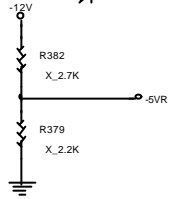
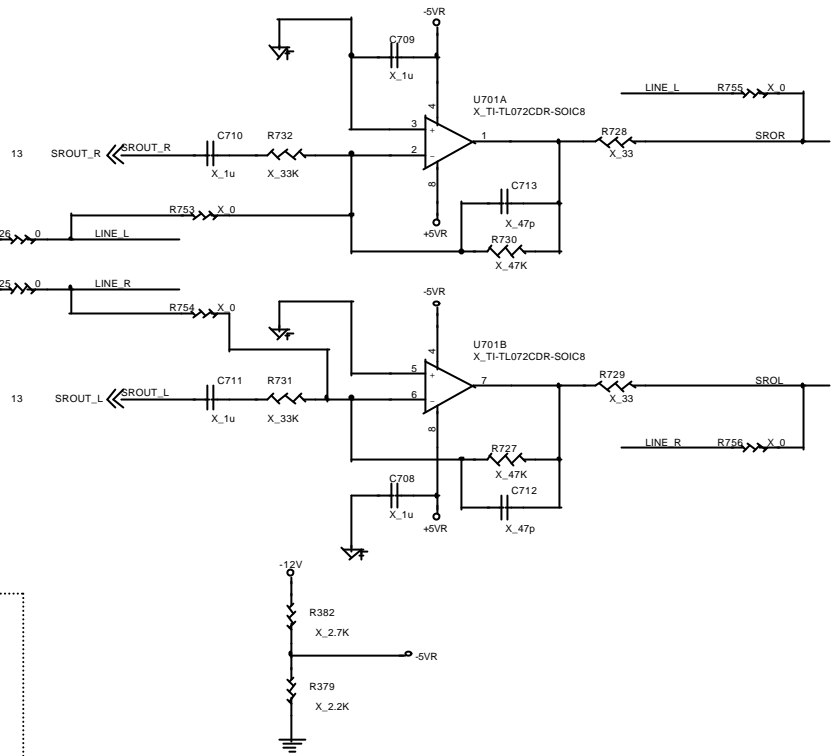
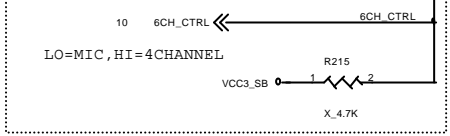
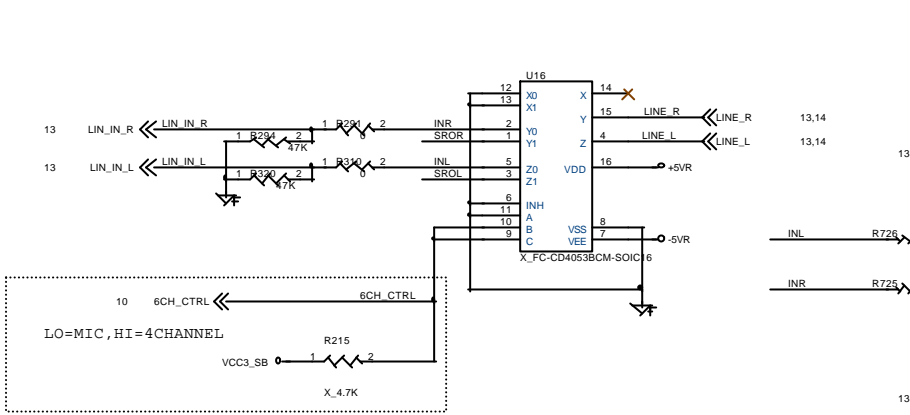
INTEL USB FRONT PANEL PIN HEADER



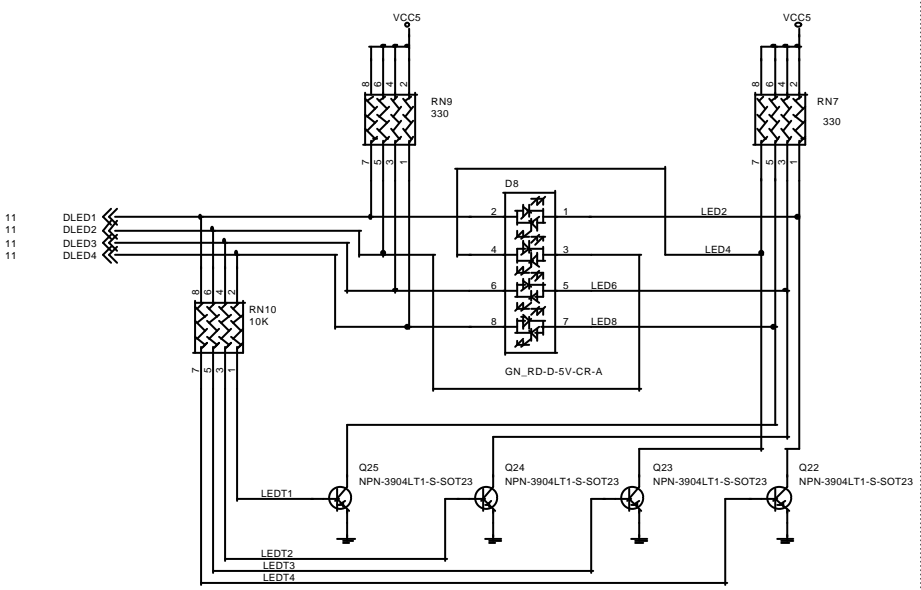
POWER CIRCUIT FOR USB PORT 2,3



Micro-Star	Title MS-6507	Rev 0B
Document Number USB & FAN Connectors		
Last Revision Date: Wednesday, August 29, 2001		Sheet 20 of 36

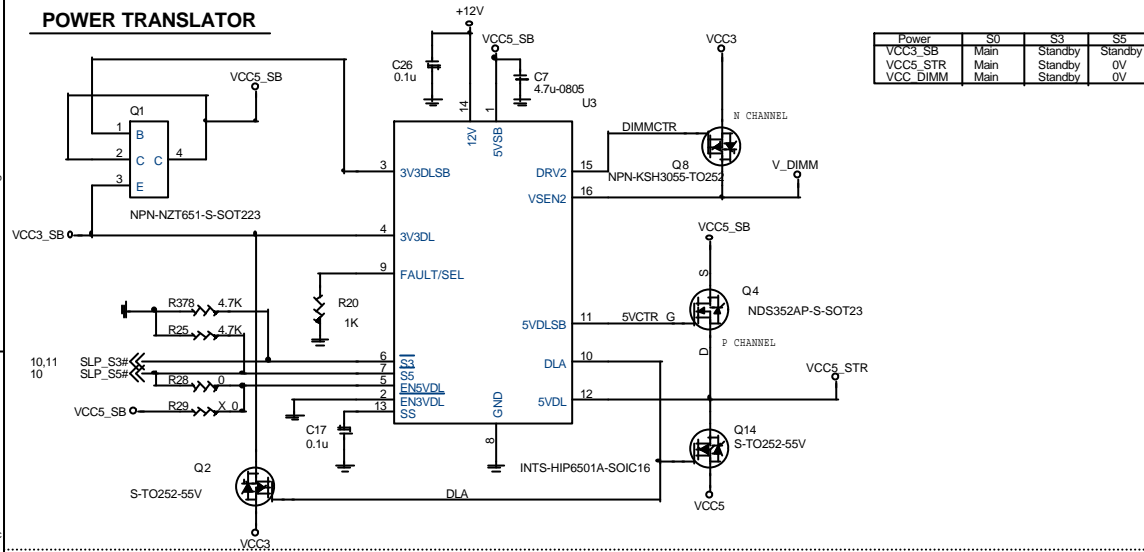


DLED



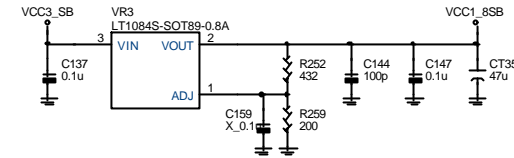
Micro-Star	Title MS-6507	Rev 0B
Document Number D-LED & 4 CHANNEL CONTROL		
Last Revision Date: Thursday, August 09, 2001		Sheet 21 of 36

POWER TRANSLATOR



Power	S0	S3	S5
VCC3_SB	Main	Standby	Standby
VCC3_STR	Main	Standby	0V
VCC3_DIMM	Main	Standby	0V

1.8V STANDBY POWER TRANSLATOR (40mils trace / 20 mils space)



POWER CONSUMPTION

	VCCP	VCC_AGP	VCC1_8	VCC3_DIMM	VCC3	VCC5	VCC5_SB	+12V	-12V
CPU	59.0A	0	0	0	0	0	0	NOTE4	0
PMCH	2.4A	NOTE1	0.2A	2.0A	0	0	0	0	0
ICH2	0	0	NOTE3	0	NOTE3	0	NOTE3	0	0
CY28334	0	0	0	0	0	0	0	0	0
AD1885	0	0	0	0	0	0	0	0	0
FVH_S3S1	0	0	0	0	0	0	0	0	0
WB3627HF	0	0	0	0	0	0	0	0	0
HIP6301	0	0	0	0	0	0	0	0	0
HIP6602A	0	0	0	0	0	0	0	0	0
HIP6601A	0	0	0	0	0	0	0	0	0
SC1527	0	0	0	0	0	0	0	0	0
DIMM	0	0	0	NOTE2	0	0	NOTE2	0	0
AGP	0	8.0A	0	0	6.0A	2.0A	?	1.0A	0
PCI	0	0	0	0	0	0	0	0	0
USB	0	0	0	0	0	0	0	0	0
USB_HUB	0	0	0	0	0	0	0	0	0
FAN	0	0	0	0	0	0	0	0	0
TTL	0	0	0	0	0	0	0	0	0
AMPLIFIER	0	0	0	0	0	0	0	0	0
OTHER	0	0	0	0	0	0	0	0	0

NOTE1 --- MCH
VCC_AGP = VCC1_5 (1.5A) + VCC_AGP (0.37A)

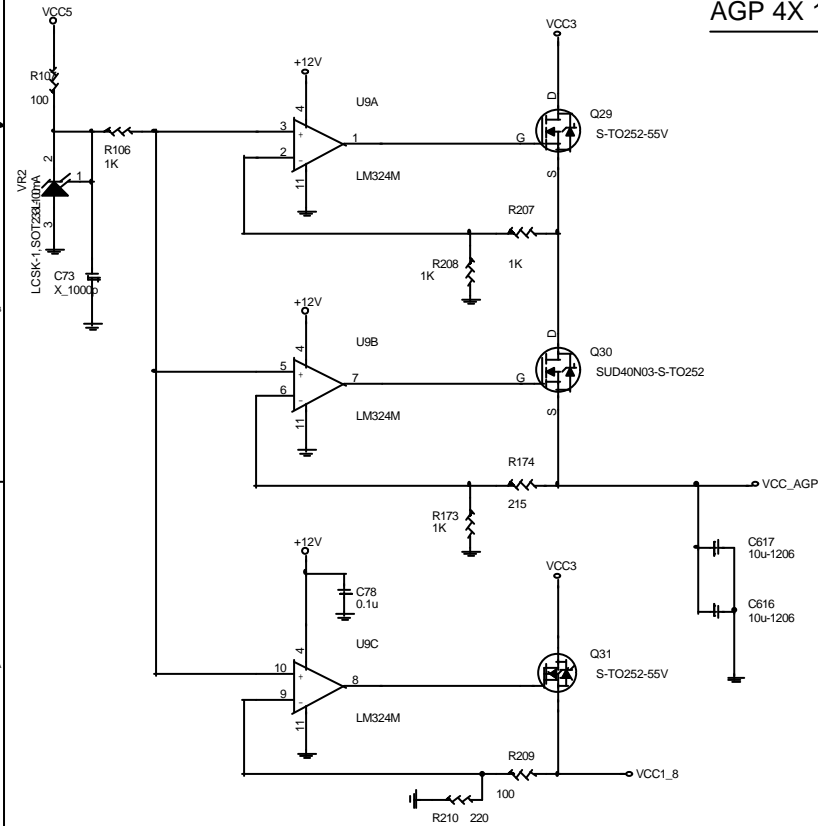
NOTE2 --- DIMM
S0 STATE --- 2.0A * 3 = 6.0A ---> VCC3
S1/S3 STATE --- 200mA * 3 = 600mA ---> VCC3_SB
VCC3_SB --> 600mA * 3.3V/5V = 396mA --> VCC5_SB

NOTE3 --- ICH2

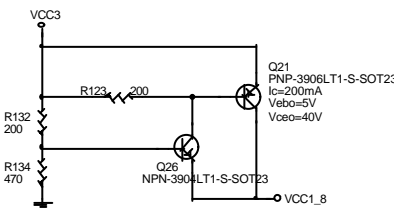
Power	S0	S1	S3/S4/S5
1.8V	300mA	100mA	N/A
1.8V LAN	36mA	28mA	N/A
VCC1_8SB	45mA	30mA	7mA
VCC3	410mA	5mA	N/A
VCC3+562ET	230mA	210mA	N/A
VCC3_SB	26mA	0.6mA	N/A

VCC3_SB =
VCC1_8SB =
VCC5_SB = VCC3_SB + VCC1_8SB

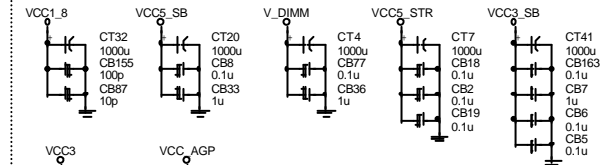
AGP 4X 1.5V POWER TRANSLATOR



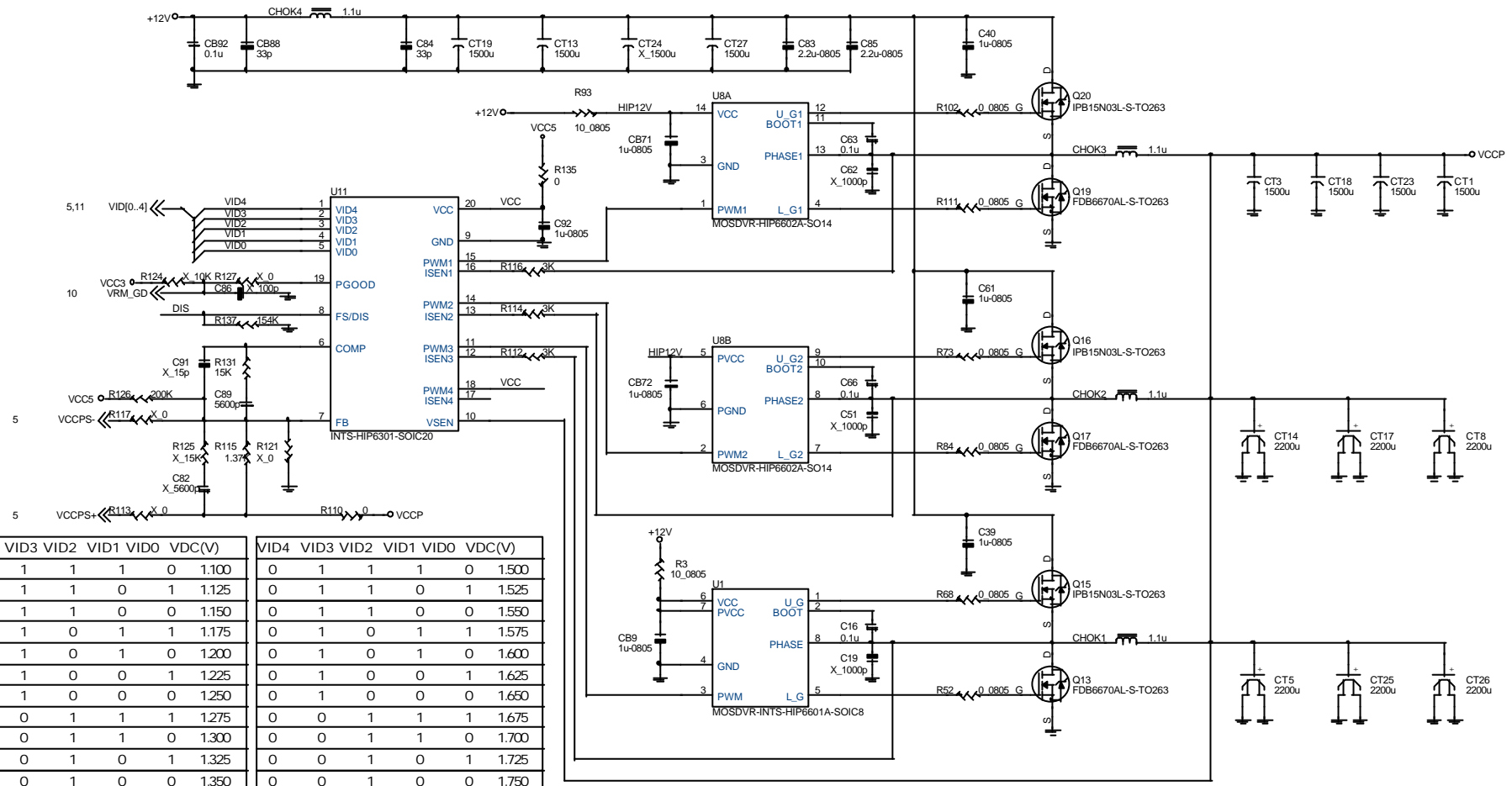
1.8V/3.3V SEQUENCE CIRCUIT



REGULATORS OUTPUT DECOUPLING CAPACITORS



Micro-Star	Title	MS-6507	Rev
Document Number	Voltage Regulator		0B
Last Revision Date:	Wednesday, August 29, 2001	Sheet	22 of 36

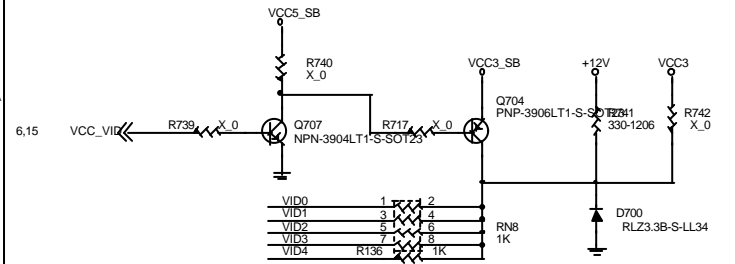


VID4	VID3	VID2	VID1	VID0	VDC(V)
1	1	1	1	0	1.100
1	1	1	0	1	1.125
1	1	1	0	0	1.150
1	1	0	1	1	1.175
1	1	0	1	0	1.200
1	1	0	0	1	1.225
1	1	0	0	0	1.250
1	0	1	1	1	1.275
1	0	1	1	0	1.300
1	0	1	0	1	1.325
1	0	1	0	0	1.350
1	0	0	1	1	1.375
1	0	0	1	0	1.400
1	0	0	0	1	1.425
1	0	0	0	0	1.450
0	1	1	1	1	1.475

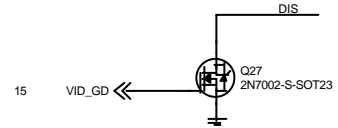
VID4	VID3	VID2	VID1	VID0	VDC(V)
0	1	1	1	0	1.500
0	1	1	0	1	1.525
0	1	1	0	0	1.550
0	1	0	1	1	1.575
0	1	0	1	0	1.600
0	1	0	0	1	1.625
0	1	0	0	0	1.650
0	0	1	1	1	1.675
0	0	1	1	0	1.700
0	0	1	0	1	1.725
0	0	1	0	0	1.750
0	0	0	1	1	1.775
0	0	0	1	0	1.800
0	0	0	0	1	1.825
0	0	0	0	0	1.850
1	1	1	1	1	OFF

VID PULL-UP RESISTORS

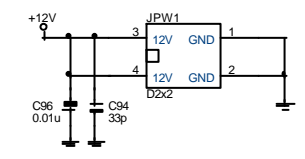
HIP6301V DON'T NEED PULL HIGH
HIP6301 NEED PULL HIGH



PWM GOOD



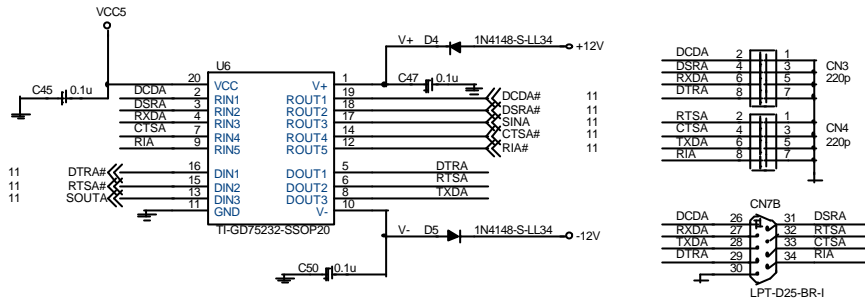
ATX12V POWER CONNECTOR



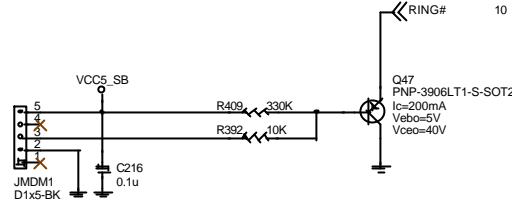
Micro-Star	Title MS-6507	Rev 0B
Document Number VRM 9.2		
Last Revision Date: Monday, September 03, 2001		Sheet 23 of 36

5/22 update

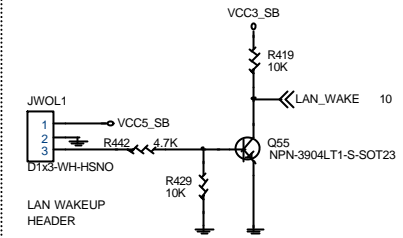
SERIAL PORT 1



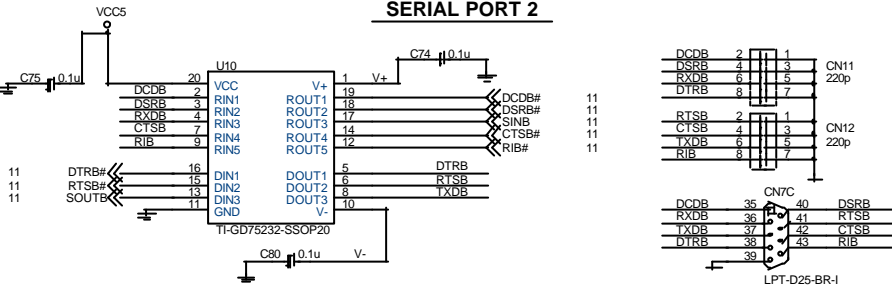
MODEM RING BLOCK



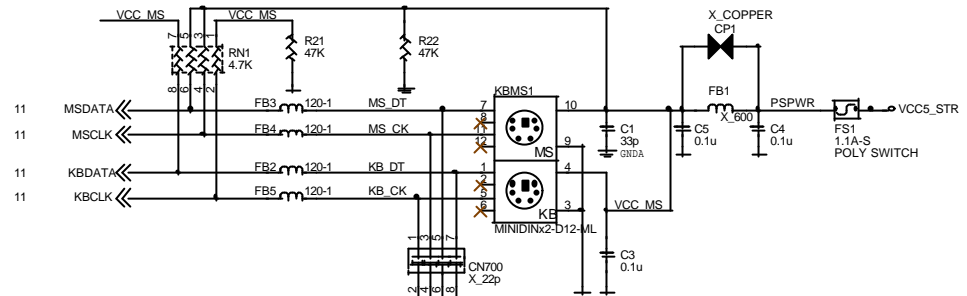
LAN WAKEUP BLOCK



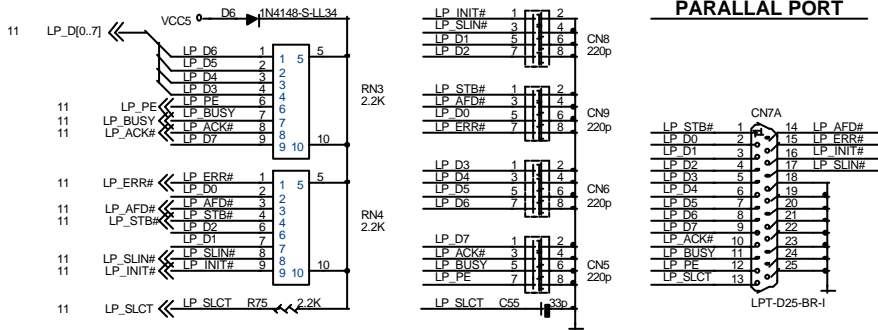
SERIAL PORT 2



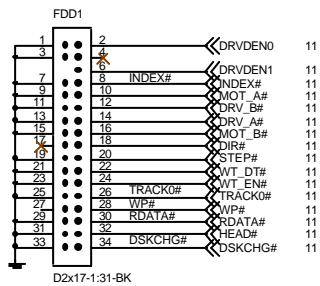
PS2 KEYBOARD & MOUSE CONNECTOR



PARALLAL PORT

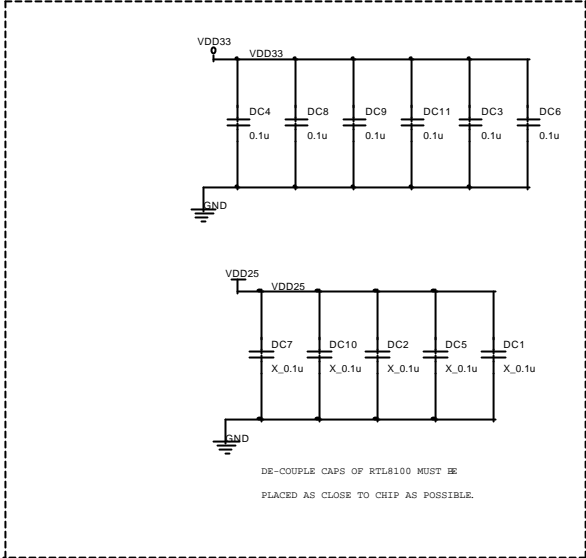
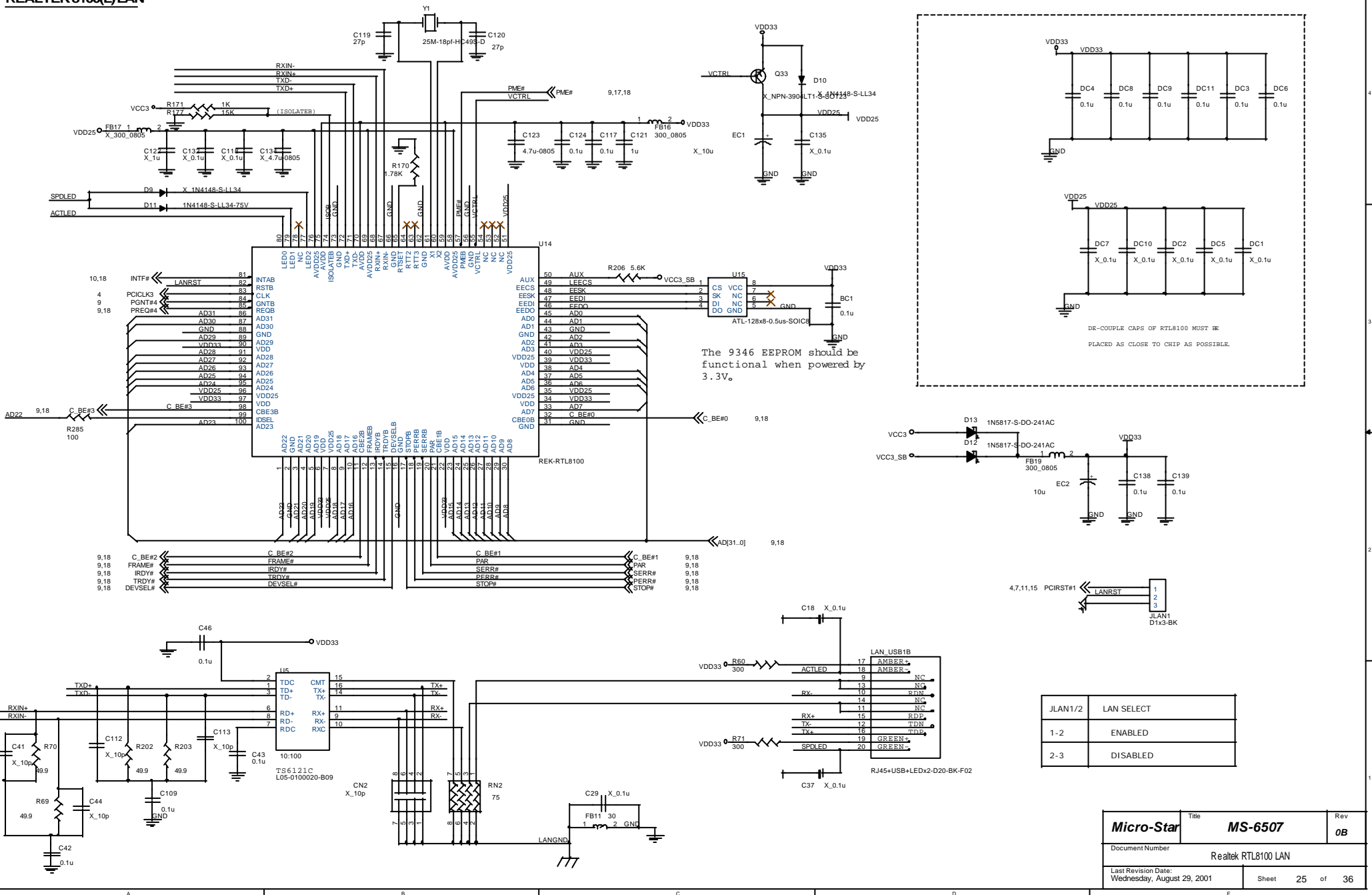


FLOPPY CONNECTOR

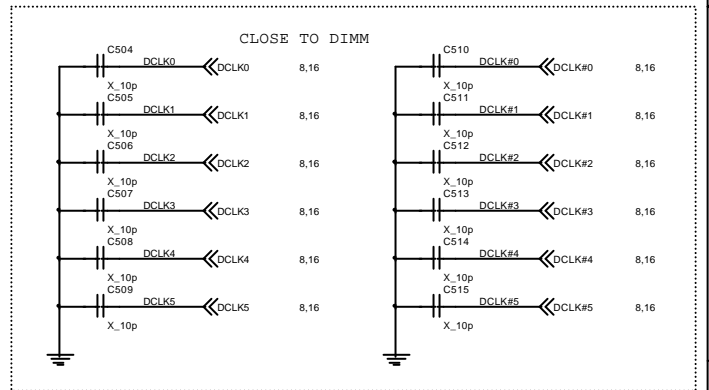
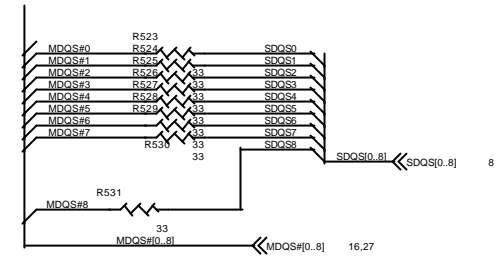
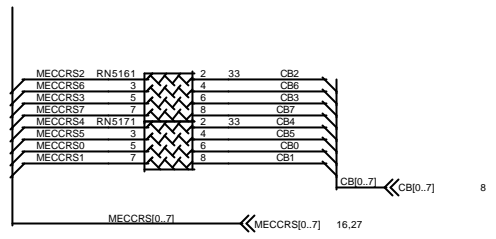
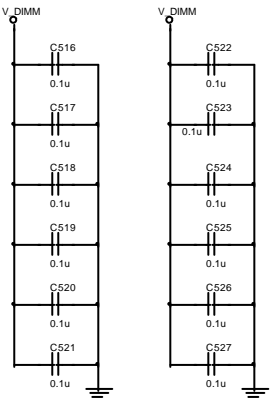
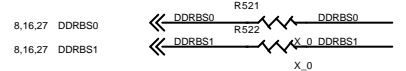
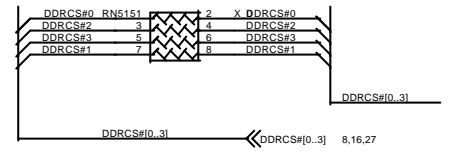
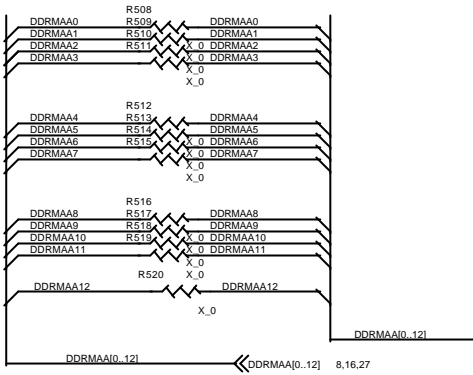
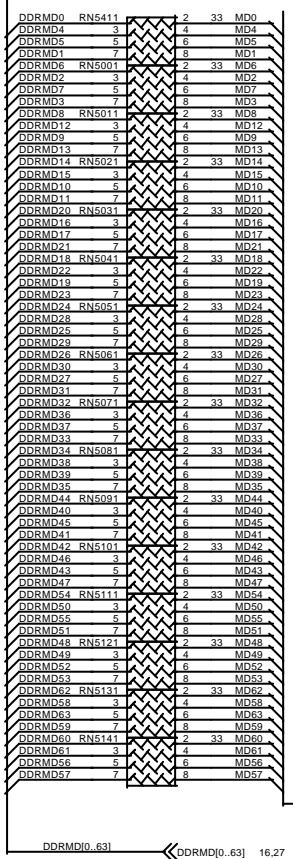


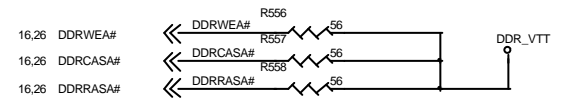
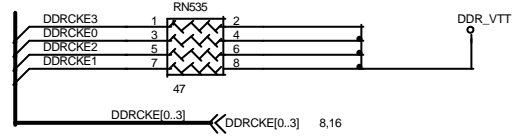
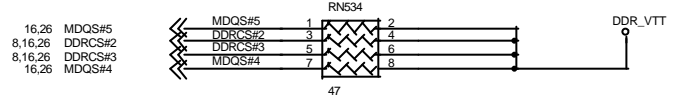
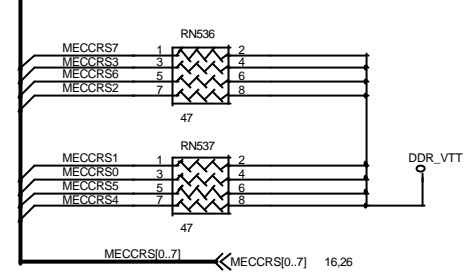
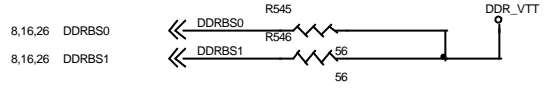
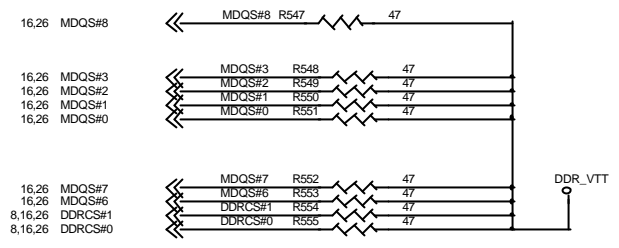
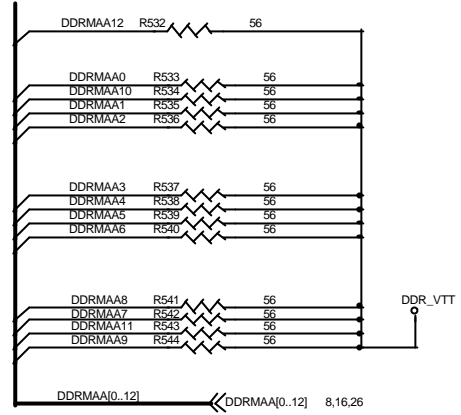
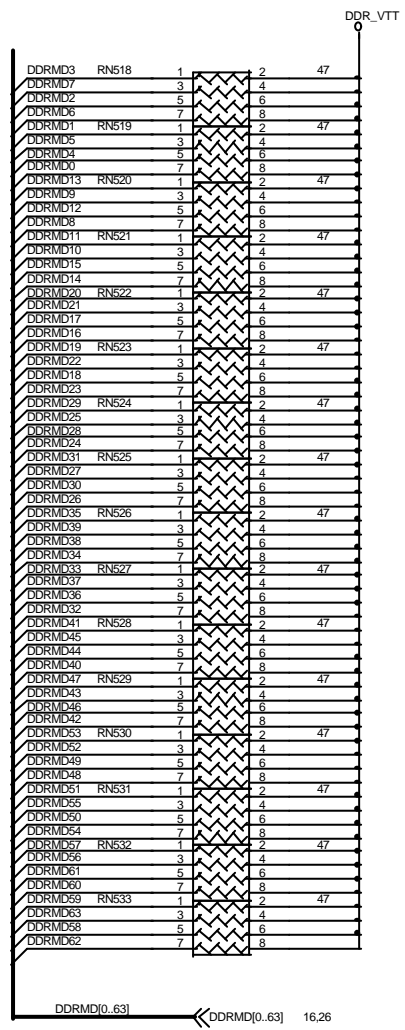
Micro-Star	Title	MS-6507	Rev
			OB
Document Number		IO Connector	
Last Revision Date:		Sheet 24 of 36	
Wednesday, August 29, 2001			

REALTEK 8100(L) LAN

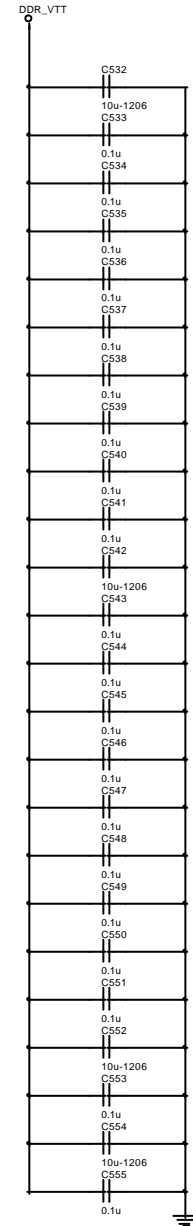
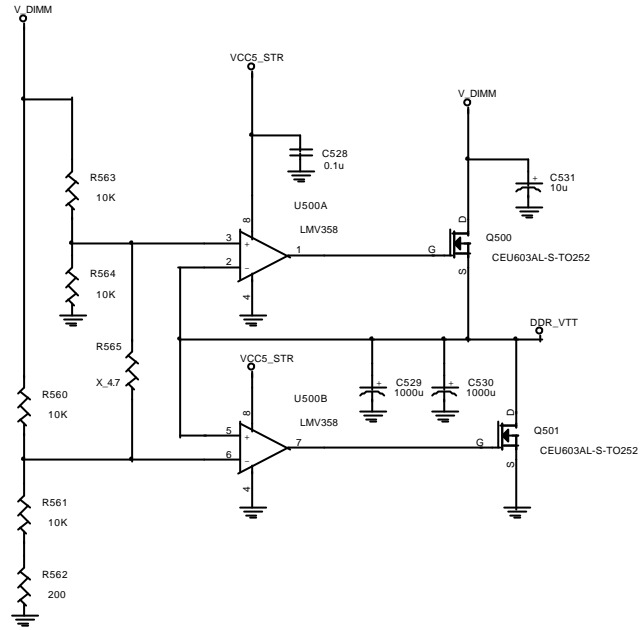


JLAN1/2	LAN SELECT
1-2	ENABLED
2-3	DISABLED





Micro-Star		Title	MS-6507	Rev	0B
Document Number					
DDR_TERMINATION					
Last Revision Date:			Sheet 27 of 36		
T u esday, July 24, 2001					



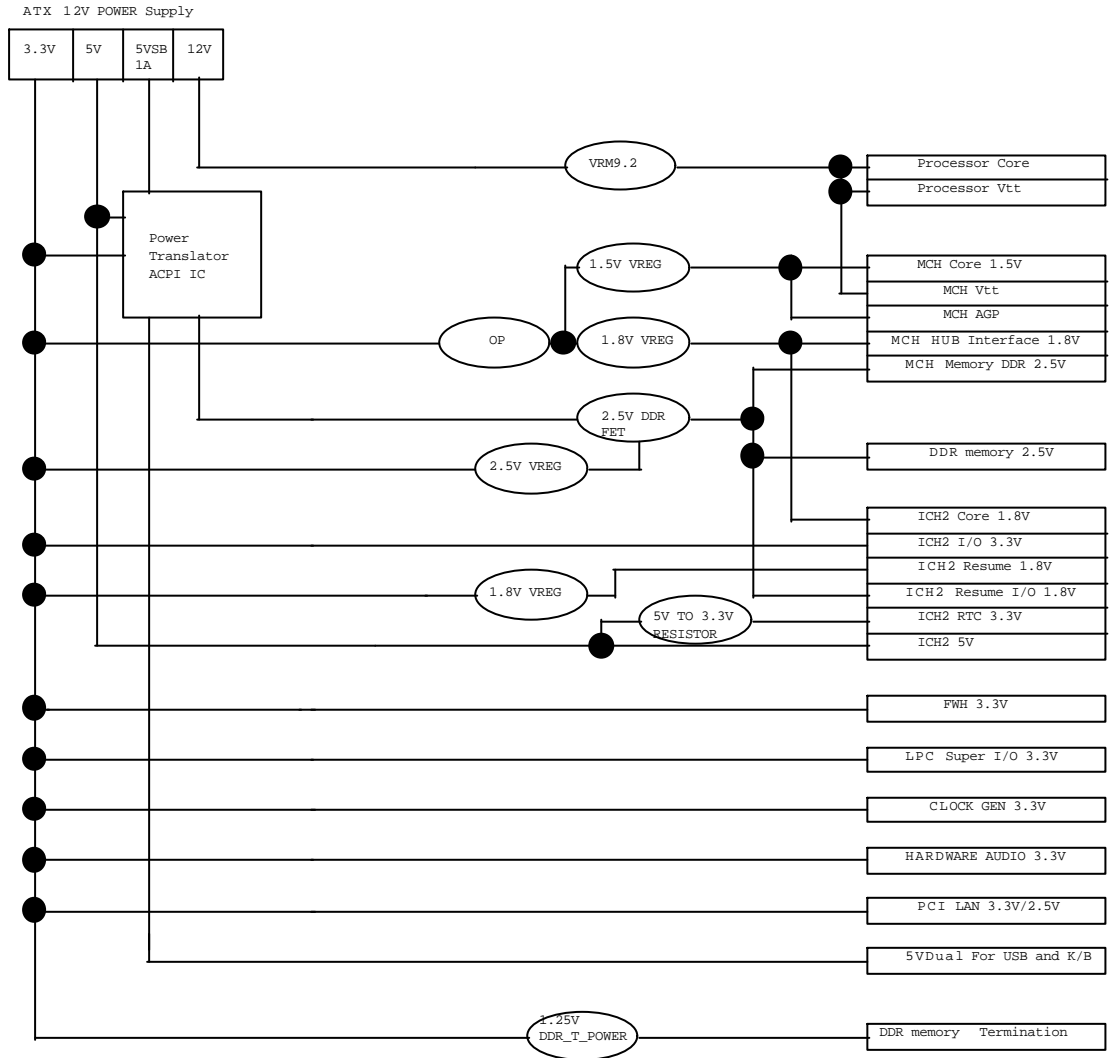
Micro-Star	Title MS-6507	Rev 0B
Document Number DDR_T_POWER		
Last Revision Date: Wednesday, August 23, 2001		Sheet 28 of 36

Jumper Setting & Connector Setting

Jumper	Description	Connector	Description
J1	INTERUDER HEADER	U3	INTEL mPGA478-B CPU
J2	CHASSIS INTRUSION HEADER	IDE1	Primary
J3	AUDIO REAR PHONE JACK (LINE_IN, LINE_OUT, MIC_IN)	IDE2	Secondary
J4	AUDIO AUX HEADER	DIM1	SDRAM DIMM1
J5	AUDIO FRONT PANEL HEADPHONE JACK HEADER	DIM2	SDRAM DIMM2
J6	AUDIO INTERNAL SPEAKER HEADER (ATAPI)	AGP1	AGP Slot
J7	BIOS function	PCI1	PCI Slot1
1-2	Normal (Default)	PCI2	PCI Slot2
2-3	Configuration Mode	PCI3	PCI Slot3
REMOVED	Recovery	COM1	Serial Port
		COM2	Serial Port
		LPT	Parallel Port
		FDD1	Floppy
JBAT1	CLEAR CMOS	JMDM1	MODEM RING HEADER
1-2	NORMAL (Default)	JWOL1	LAN WAKEUP HEADER
2-3	CLEAR CMOS	KBMS1	PS/2 Keyboard and PS/2 mouse
IR1	IR HEADER	C_FAN1	CPU FAN HEADER
CD_IN1	CDROM HEADER (ATAPI)	S_FAN	System FAN HEADER
MDM_IN1	TELEPHONY HEADER (ATAPI)	USB1	USB REAR CONNECTOR
JP1	CNR RISER CODEC SELECT HEADER	USB2	USB INTERNAL HEADER
1-2	AUTO MODE (Default)	POWER	ATX Power
2-3	PRIMARY AUDIO CODEC ONBOARD	JSMB1	SMBUS HEADER
		F_P1	Front Panel
		Pin1	Power of Hard LED
		Pin2	Power LED
		Pin3	Hard LED
		Pin4	Suspend LED
		Pin5,8,12,13	GND
		Pin6	Power Button
		Pin7	Reset Button
		Pin9	VCC
		P_FAN1	ATX FAN HEADER
		JPW1	ATX12V Power

Micro-Star	Title MS-6507	Rev 0B
Document Number JUMPER SETTING		
Last Revision Date: Monday, July 23, 2001		Sheet 29 of 36

Power Delivery Map



Micro-Star	Title MS-6507	Rev 0B
Document Number Power Delivery Map		
Last Revision Date: Monday, July 23, 2001	Sheet 30	of 36

Pentium 4 Processor /Northwood mPGA 478

Source Synchronous Signal Group and the Associated Strobes

Signals	Associated Strobe
REQ[4:0],A[16:3]#	ADSTB0#
A[31:17]#	ADSTB1#
D[15:0]#,DBI0#	DSTBP0#,DSTBN0#
D[31:16]#,DBI1#	DSTBP1#,DSTBN1#
D[47:32]#,DBI2#	DSTBP2#,DSTBN2#
D[63:48]#,DBI3#	DSTBP3#,DSTBN3#

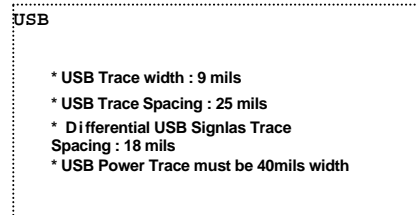
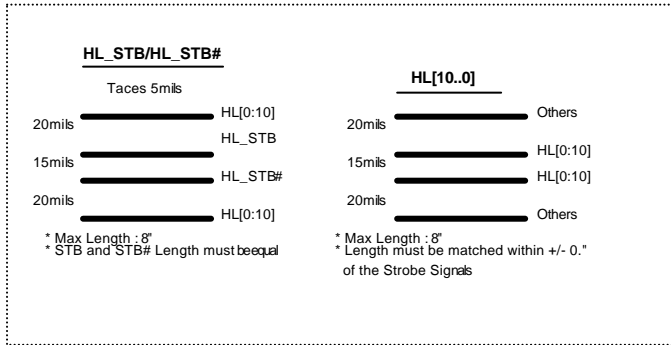
ADSTB0#
ADSTB1# should be +/- 25mils

Signals	Length	Inaccuracy
Data	2.0" to 10.0"	+/- 100 mil
Address	2.0" to 10.0"	+/- 200 mil
Strobe	2.0" to 10.0"	+/- 25 mil
Clock	2.0" to 10.0"	Don't need

* Delta=(CPU_pkglen.net-CPUpkglen.strobe)+(CS_pkglen.net-CS_pkglen.strobe)

Trace : 7 mil width 13mil space

Miscellaneous Signals



AGP

1X Timing group	2X/4X Timing group	SIGNALS	Maximum Length	Width	Space	Dismatch Length	Relative to
AGPCLK PPE# RBF# WBF# ST[2..0] GFRAME# GIRDY# GTRDY# GSTOP# GDEVSEL# GREQ# GGNT# GPAR	SET#1 GAD[15..0] GC_BE#[1..0] GAD_STB0 GAD_STB0# SET#2 GAD[31..16] GC_BE#[3..2] GAD_STB1 GAD_STB1# SET#3 SBAT[7..0] SB_STB SB_STB#	1X Timing group	7.5"	5 mil	5 mil	X	X
		2X/4X Timing group SET#1	7.25"	5 mil	20 mil	+/- 0.125"	GAD_STB0 GAD_STB0#
		2X/4X Timing group SET#2	7.25"	5 mil	20 mil	+/- 0.125"	GAD_STB1 GAD_STB1#
		2X/4X Timing group SET#3	7.25"	5 mil	20 mil	+/- 0.125"	SB_STB SB_STB#
		2X/4X Timing group SET#1	6"	5 mil	15 mil	+/- 0.25"	GAD_STB0 GAD_STB0#
		2X/4X Timing group SET#2	6"	5 mil	15 mil	+/- 0.25"	GAD_STB1 GAD_STB1#
		2X/4X Timing group SET#3	6"	5 mil	15 mil	+/- 0.25"	SB_STB SB_STB#

Micro-Star	Title MS-6507	Rev 0B
Document Number		Layout Guide
Last Revision Date: Monday, July 23, 2001		Sheet 31 of 36

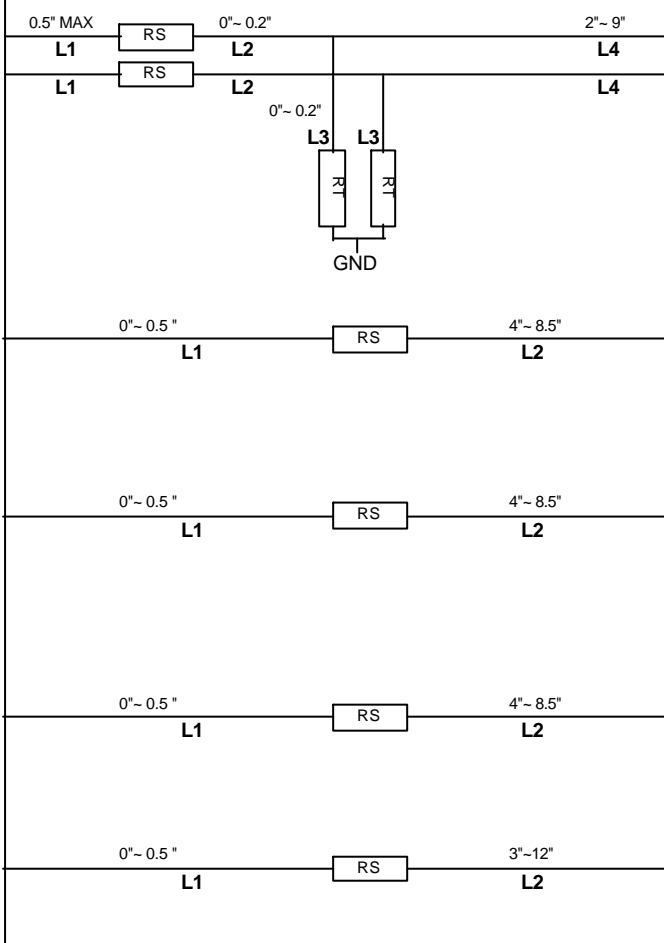
CPUCLK
MCHCLK
CPUCLK#
MCHCLK#

MCH_66
ICH_66
AGP_66

ICH_PCLK
FWH_PCLK
SIO_PCLK
ISAPCLK
PCICLK[4..0]

ICH_14
OSC

ICH_48
SIO_48



DEVICE	L1+L2
CPU	X
MCH	X
ITP	X

* Line Width :7.0mil
* Differential pair spacing :7.0mil
* Spacing to other traces :28mil
* BCLK0/BCLK1 LENGTH MATCH +/- 10mil

DEVICE	L1+L2
MCH	X
ICH	X +/- 100 mils
AGP	X-4"

* Line Width :5.0mil
* Spacing to other traces :20mil

DEVICE	L1+L2
ICH	X
FWH	X
SIO	X
PCI	X-2.5"

* Line Width :5.0mil
* Spacing to other traces :20mil
* L1/L2 TRACE SAME AS MCH_66 TRACE LENGTH

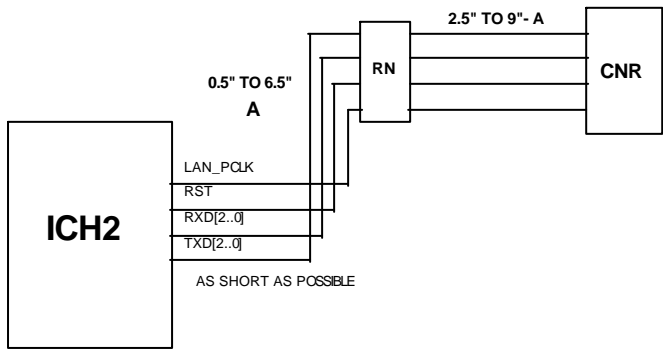
DEVICE	L1+L2
ICH	Y
ISA BRIDGE	Y

* Line Width :5.0mil
* Spacing to other traces :10mil

DEVICE	L1+L2
ICH	
SIO	

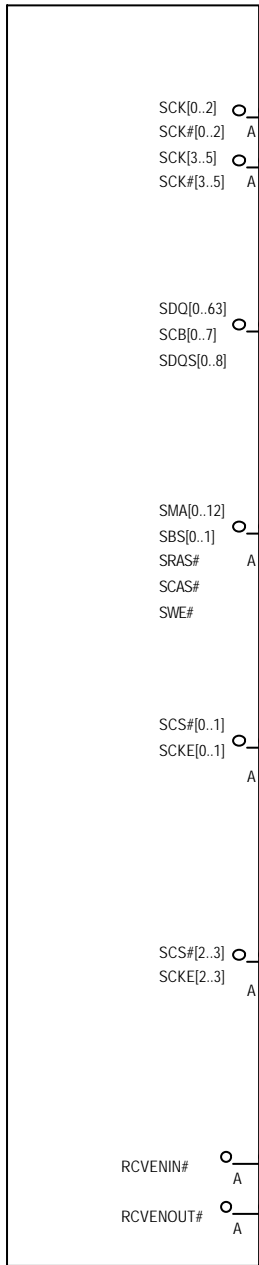
* Line Width :5.0mil
* Spacing to other traces :20mil

CK 408



* Line Width :7.0mil
* Differential signals space :14mils
* Differential signals length mismatch +/- 7mil

Micro-Star	Title MS-6507	Rev 0B
Document Number CK-408 and LAN Design Guide		
Last Revision Date: Monday, July 23, 2001		Sheet 32 of 36



Trace Width : 5 mils
 Differential pair spacing : 7 mils.
 Isolation spacing : 20 mils

A: 40 mils max
 B+D: 2" - 6.5"
 C+E: 2" - 7.0"

SCK[0..2]
 SCK#[0..2]
 SCK[3..5]
 SCK#[3..5]

Length: SCK[0..2] = SCK#[0..2]
 Length: SCK[3..5] = SCK#[3..5]

SDQ[0..63]
 SCB[0..7]
 SDQS[0..8]

Trace Width : 5 mils
 Trace spacing : 12 mils

A: 2" - 5"
 B: 0.5" MAX
 C: 0.3" - 0.5"
 D: 0.1" - 0.8"

Rs = 33 ohm +- 5%

RTT
 DDR_VTT = 1.5V
 Rtt = 47 ohm +- 5%

SMA[0..12]
 SBS[0..1]
 SRAS#
 SCAS#
 SWE#

Trace Width : 5 mils
 Trace spacing : 12 mils

A: 40 mils max
 B: 2" - 3.5"
 C: 0.5" max
 D: 0.3" - 0.5"
 E: 0.1" - 0.8"

Rs = 0 ohm +- 5%

RTT
 DDR_VTT = 1.5V
 Rtt = 56 ohm +- 5%

SCS#[0..1]
 SCKE[0..1]

Trace Width : 5 mils
 Trace spacing : 12 mils

A: 40 mils max
 B: 2" - 3.5"
 C: 0.5" max
 D: 0.4" - 1.3"

Rs = 0 ohm +- 5%

RTT
 DDR_VTT = 1.5V
 Rtt = 47 ohm +- 5%

SCS#[2..3]
 SCKE[2..3]

Trace Width : 5 mils
 Trace spacing : 12 mils

A: 40 mils max
 B: 2" - 3.5"
 C: 1.0" max
 D: 0.1" - 0.8"

Rs = 0 ohm +- 5%

RTT
 DDR_VTT = 1.5V
 Rtt = 47 ohm +- 5%

RCVENIN#
 RCVENOUT#

A: 40 mils max
 B: exactly 1"

DIMM1

DIMM2

$$\begin{aligned} \text{SCK}[0..2] \quad (A + B + D) &= \text{SDQS}[0..8] \quad (A + B) + (1" - 2") \\ \text{SCK}\#[0..2] & \end{aligned}$$

$$\begin{aligned} \text{SCK}[3..5] \quad (A + C + E) &= \text{SDQS}[0..8] \quad (A + B + C) + (1" - 2") \\ \text{SCK}\#[3..5] & \end{aligned}$$

SDQ[0..7]	SDQS0
SDQ[8..15]	SDQS1
SDQ[16..23]	SDQS2
SDQ[24..31]	SDQS3
SDQ[32..39]	SDQS4
SDQ[40..47]	SDQS5
SDQ[48..55]	SDQS6
SDQ[56..63]	SDQS7
SCB[0..7]	SDQS8

Matching requirement is +- 25 mils to strobe

$$\begin{aligned} \text{SCK}[0..2] \quad (A + B + D) &= \text{SMA}[0..12] \quad (A + B + C) + (1" - 4") \\ \text{SCK}\#[0..2] & \end{aligned}$$

$$\begin{aligned} \text{SCK}[3..5] \quad (A + C + E) &= \text{SMA}[0..12] \quad (A + B + C + D) + (1" - 4") \\ \text{SCK}\#[3..5] & \end{aligned}$$

$$\begin{aligned} \text{SCK}[0..2] \quad (A + B + D) &= \text{SCS}\#[0..1] \quad (A + B + C) + (1" - 4") \\ \text{SCK}\#[0..2] & \end{aligned}$$

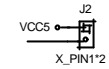
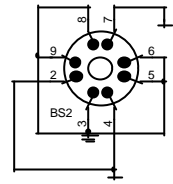
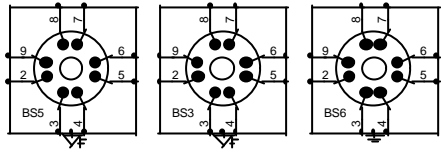
$$\begin{aligned} \text{SCK}[3..5] \quad (A + C + E) &= \text{SCS}\#[2..3] \quad (A + B + C) + (1" - 4") \\ \text{SCK}\#[3..5] & \end{aligned}$$

MCH

Micro-Star	Title MS-6507	Rev 0B
Document Number DDR DIMM DG		
Last Revision Date: Monday, July 23, 2001		Sheet 33 of 36

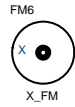
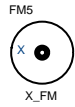
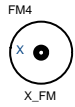
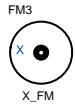
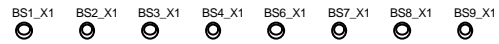
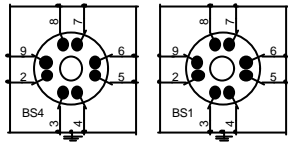
PCB OTHER COMPONENT

SIMULATION TRACE



SDR

AGP

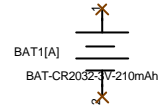


Micro-Star	Title MS-6507	Rev 0B
Document Number MANUAL		
Last Revision Date: Tuesday, July 24, 2001		Sheet 34 of 36

JBAT1 Clear CMOS		
1 - 2	Normal	*
2 - 3	Clear CMOS	



BAT SOCKET



J7 BIOS Update	
SHORT	Locked
OPEN	Unlocked *



BIOS

U23(1)			
1	VPP	32	VCC
2	RST#	31	CLK
3	FGPI3	30	FGPI4
4	FGPI2	29	IC(VIL)
5	FGPI1	28	GND4
6	FGPI0	27	VCCA
7	WP#	26	GND
8	TBL#	25	VCC
9	ID3	24	INIT#
10	ID2	23	FWH4
11	ID1	22	RFU
12	ID0	21	RFU
13	FWH0	20	RFU
14	FWH1	19	RFU
15	FWH2	18	RFU
16	GND	17	FWH3

SST-256K*8-33MHz-PLCC32

FRONT PANNEL BUZZER



JP2	On board codec
1-2	ENABLED
2-3	DISABLED



JLAN1	LAN SELECT
1-2	ENABLED
2-3	DISABLED



MS6507 PCB



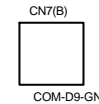
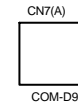
Heat sink



Hooker



COM



Micro-Star	Title MS-6507	Rev 0B
Document Number PACKING BOM		
Last Revision Date: Wednesday, August 29, 2001		Sheet 35 of 36

HISTORY

From 0A to 0B

1.Remove H/W Audio.
2.Add CNR Slot.
3.Reduce 1cm in width.
4.Add thermtrip circuit.
5.Fix no cpu can not shutdown issue.
6.Change super I/O to 627F compatible.
7.Fix power sequency issue.
8.Fix Glitch on DDR signal.
9.Modified Vcore power plane placement.
10.Add Intel front pannel pin header.

Micro-Star	Title MS-6507	Rev 0B
Document Number HISTORY		
Last Revision Date: Monday, July 23, 2001		Sheet 36 of 36